BU2 SYSTEM DIAGRAM

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT

DDRII-SODIMM1 PAGE 8 — DDRII 667/800 MHz

DDRII-SODIMM2 PAGE 8 — DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 4,5,6,7

CPU THERMAL SENSOR PAGE 6

14.318MHz

CLOCK GEN
ICS9LPRS480AKLFT
SLG8SP628VTR
RTM880N-795
PAGE 3

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

HT LINK

PCI-E

NORTH BRIDGE
RS780M
21mm X 21mm, 528pin BGA
PAGE 9,10,11

HDMI/CEC PAGE 18

CRT PAGE 19

LVDS PAGE 17

LED Driver PAGE 17 — LED Panel PAGE 17

X1 LAN
Marvell
PCIE-LAN
8040T/8072
(10/100/GagaLAN)
PAGE 24

RJ45/RJ11 Board PAGE 24

X1 Express Card
(NEW CARD)
PAGE 24

X1 Mini PCI-E Card
HD-DVD
(ROBSON/TV)
PAGE 23

X1 Mini PCI-E Card
(Wireless LAN)
PAGE 23

Mini PCI-E Card x1
HD DVD DECODER x1

SBSRC_CLK

PCIE X4

NAND FLASH CARD PAGE 23 — IDE/133

SATA - HDD PAGE 20 — SATA0 150MB

SATA - CD-ROM PAGE 20 — SATA1 150MB

E-SATA PAGE 20 — SATA2 150MB

SOUTH BRIDGE
SB700
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13,14,15,16

USB2.0

4,8

0,10,11 USB2.0 Ports X4 PAGE 20,23

1 Felice PAGE 25

2 Webcam X1 PAGE 17

5 Fingerprint PAGE 25

6 Bluetooth PAGE 25

7 NEW CARD PAGE 24

PAGE 19

PCI BUS / 33MHz

Azalia

PCMCIA Controller CB1410 PAGE21

O2 OZ129T PAGE22

PCMCIA PAGE 21

IEEE1394 CONN PAGE 22

Memory CardReader PAGE 22

SMBUS

LPC

G-Sensor LIS3L02AQ3 PAGE 19

Keyboard PAGE 29
CIR PAGE 28

Touch Pad PAGE 25
Kill SW PAGE 29

VR (AUDIO CONN) PAGE 27

WINBOND KBC
WPC8763LDG
PAGE 28

FAN PAGE 6

FLASH SPI PAGE 28

MDC/FM TUNER CONNECTOR PAGE 27

MDC/FM TUNER Module PAGE 27

Digital MIC PAGE 16,26

CONEXANT CX20561 PAGE 26

HP Amplifier G1412 PAGE 27

Audio Amplifier G1441 PAGE 26

AUDIO CONN (HP/ MIC) PAGE 27

SPEAKER Conn PAGE 26

SYSTEM CHARGER(ISL88731) PAGE 30

SYSTEM POWER ISL6237IRZA-T PAGE 31

CPU CORE ISL6265A PAGE 32

VCCP +1.1V AND +1.2V(MAX8717) PAGE 33

DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 34

DISCHARGE 1.5/1.25/1.2/1.1V PAGE 35

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTE#	OZ129T
REQ1# / GNT1#	AD18	INTF#	CB1410

NB4

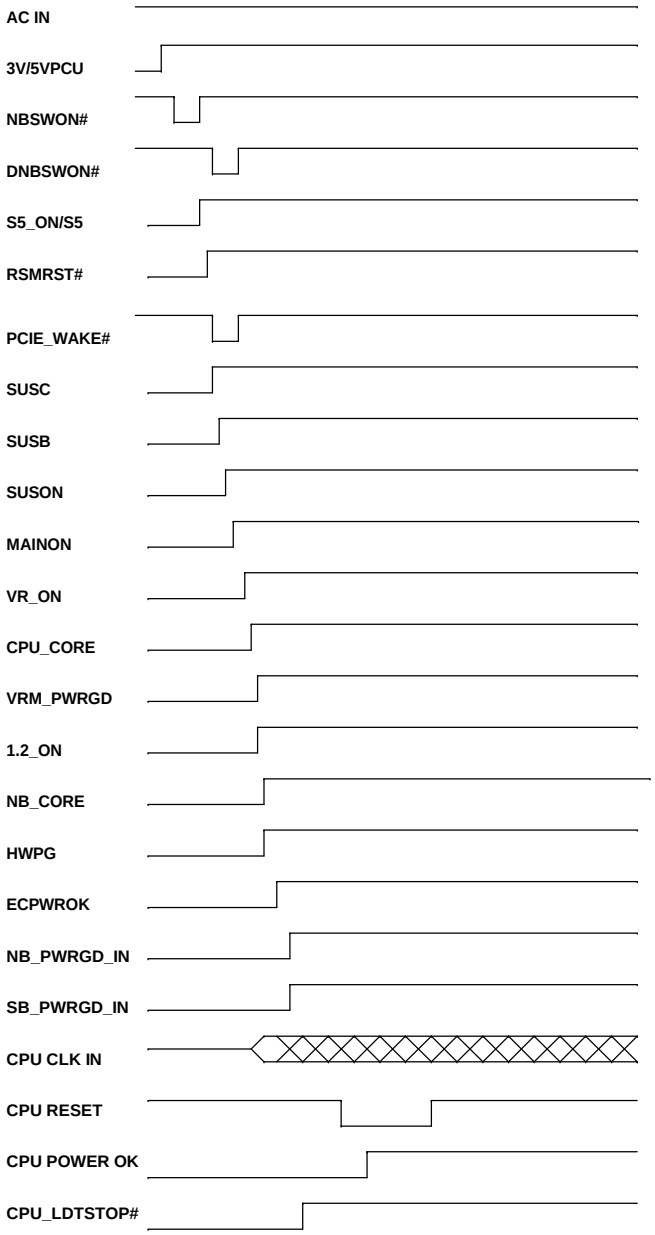
PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Wednesday, January 30, 2008 Sheet 1 of 35

INDEX

Power Sequence



02

SB700 SM BUS

SB700 SMBUS	SMBUS Function Define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card/New Card (+3VS5)
SMBCLK2 SMBDAT2	HDMI CEC (+3VS5)

KBC(EC) SM BUS

KBC SMBUS	SMBUS Function Define
MBCLK MBDAT	BATTERY (+3VPCU)
2ND_MBCLK 2ND_MBDATA	CPU THER / SENSOR/EC (+3V/PCU)
3ND_MBCLK 3ND_MBDATA	HDMI CEC / TOUCH SEN(+3VS5)

NB4

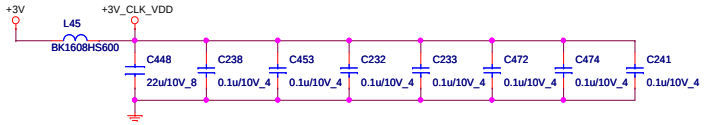
PROJECT : BU2
Quanta Computer Inc.

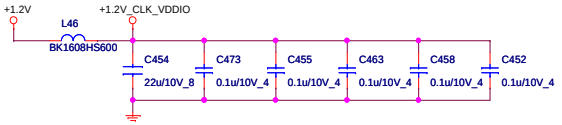
Size	Document Number	Rev
Custom	SYSTEM INFORMATION	1A

Date: Thursday, November 08, 2007 | Sheet 2 of 35

CLK_GEN_SLG8SP628

03





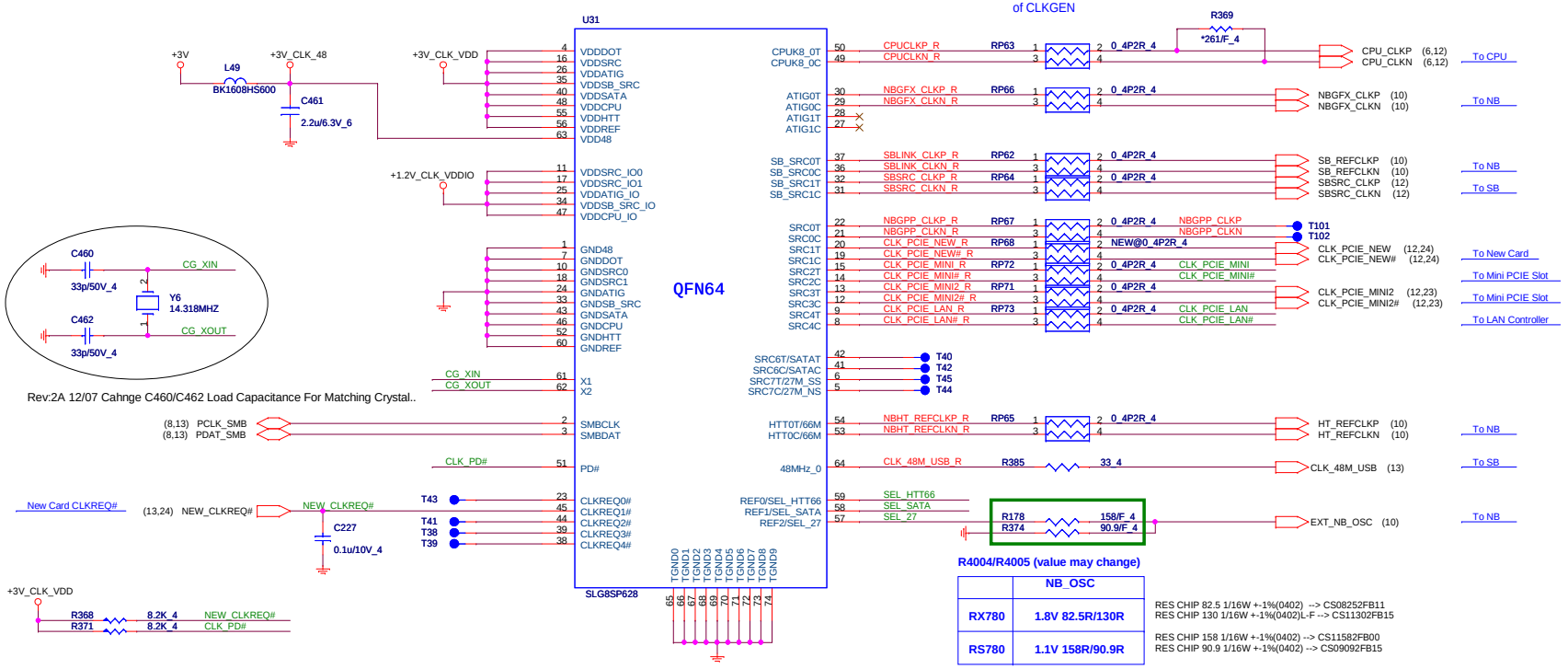
ICS9LPRS480 P/N :

SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN



R4004/R4005 (value may change)

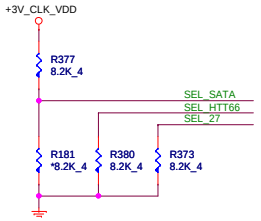
	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

RES CHIP 82.5 1/16W +-1%(0402) --> CS08252FB11
RES CHIP 130 1/16W +-1%(0402)L-F --> CS11302FB15

RES CHIP 158 1/16W +-1%(0402) --> CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) --> CS09092FB15

NB CLOCK INPUT TABLE

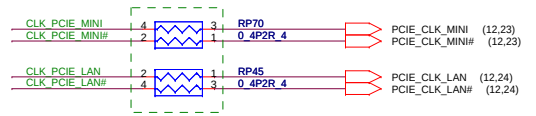
NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF



SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

FOR EXTERMAL/INTERNAL CLOCK



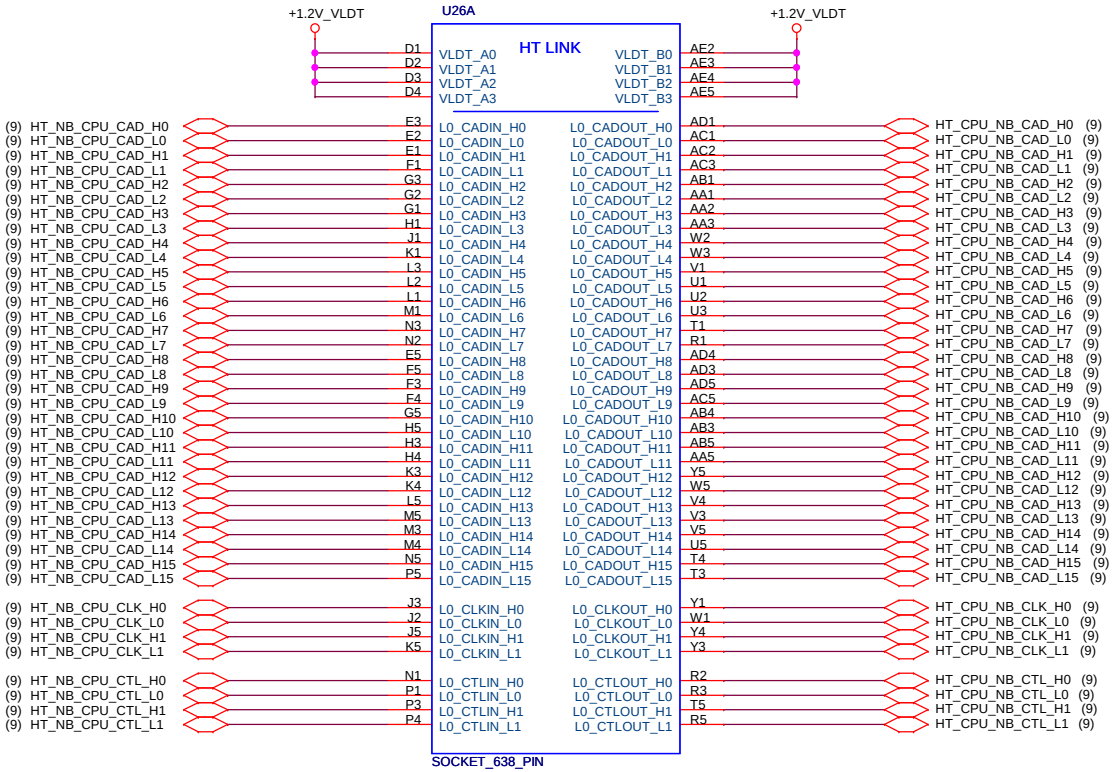
Place Close to Drivers Side

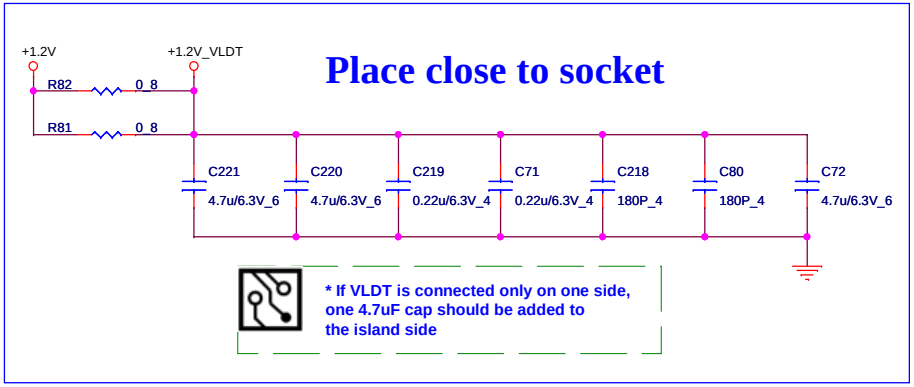
PROJECT : BU2
Quanta Computer Inc.

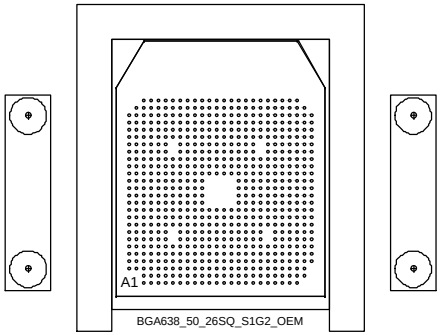
Size	Document Number	Rev
Custom	CLOCK GENERATOR_SLG8SP628	1A

Date: Thursday, July 24, 2008 Sheet 3 of 35

NB4





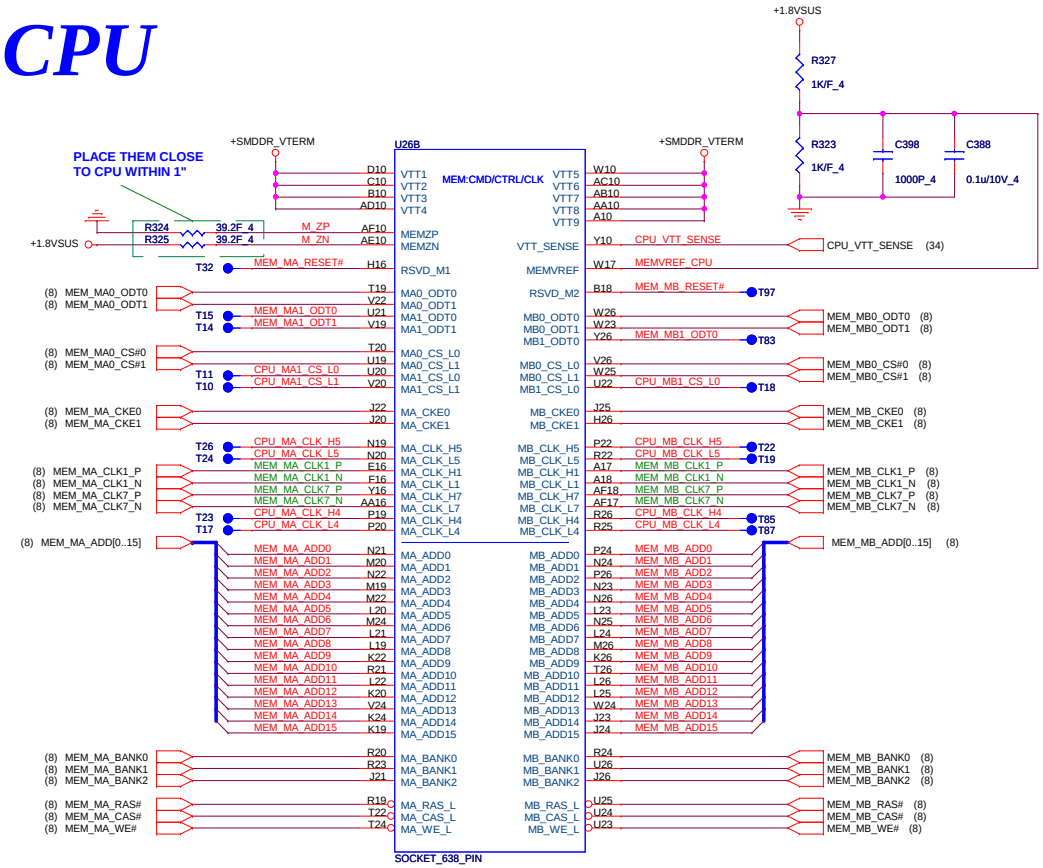


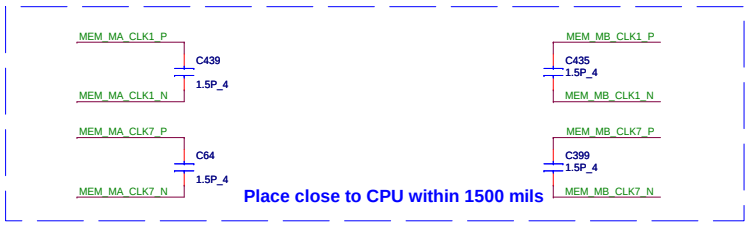
CPU

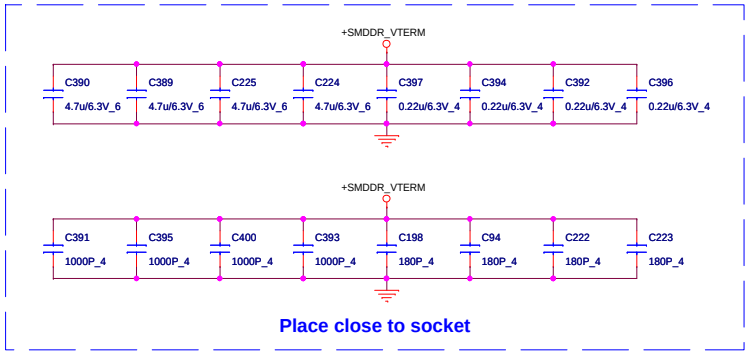
NB4	PROJECT : BU2 Quanta Computer Inc.	
Size B	Document Number S1G2 HT I/F 1/4	Rev 1A
Date: Thursday, July 24, 2008	Sheet 4 of 35	

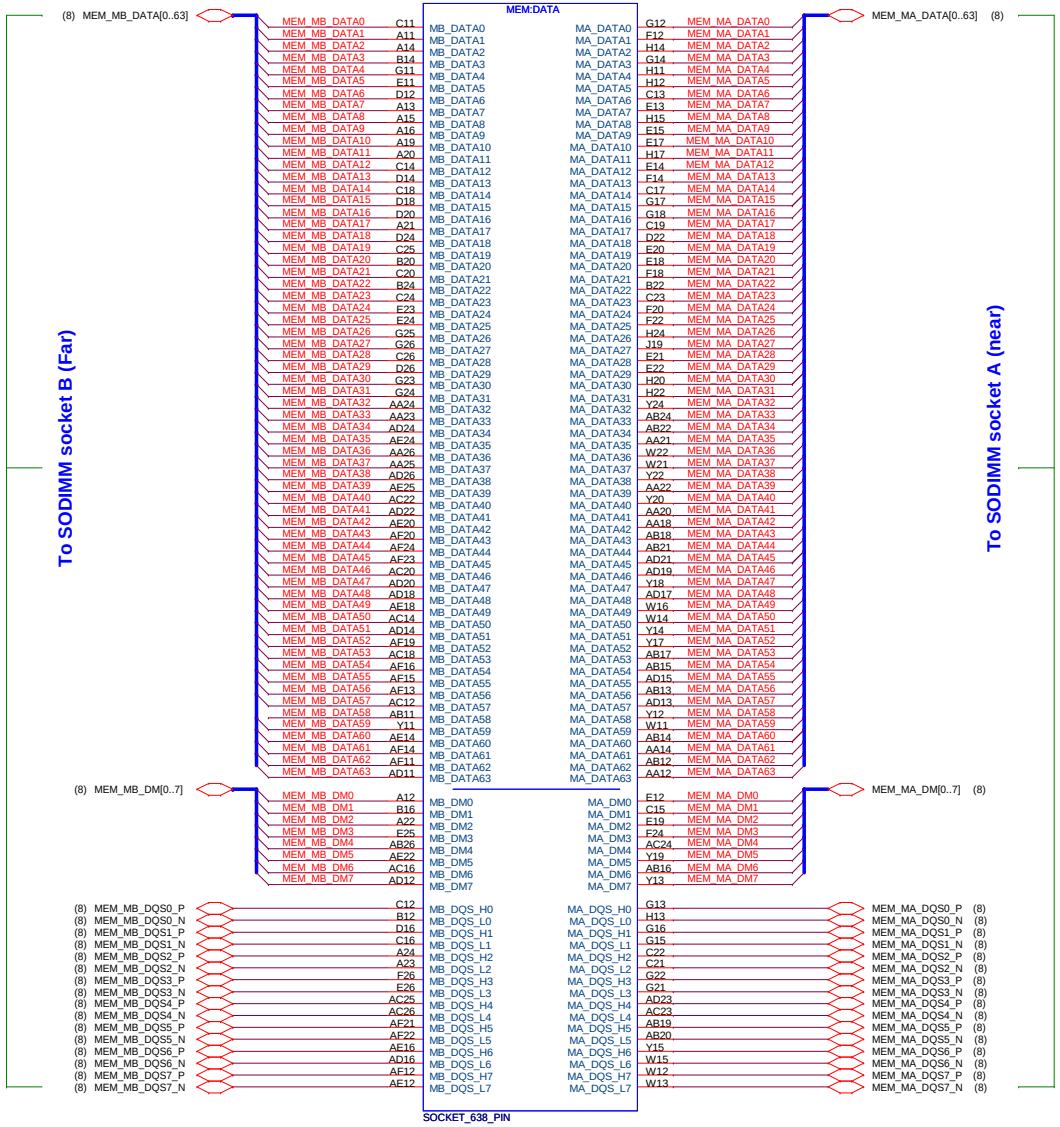
CPU

Processor Memory Interface









NB4	PROJECT : BU2 Quanta Computer Inc.	
Size: Custom	Document Number: S1G2 DDRII MEMORY I/F 2/4	Rev: 1A
Date: Thursday, July 24, 2008	Sheet 5 of 35	

CPU

W/S= 15 mil/20mil

250mA

CPU CLK

CPU POWER-UP

Rev:3A 01/29 Change to S0 domain save power during S3 since SB .

Rev:2A 12/06 Add 0.1u For AMD CPU issue.

Rev:3A 01/29 Change to 4.7K

For Debug Only

Rev:3C 05/09 Follow AMD Design Guide add termination resistor.

route as differential as short as possible testpoint under package

CPU THERM

06

Rev:3A 02/05 System will Leakage when system into G3 mode.

CPU FAN

FANPWR = 1.6*VSET

G995/Pin1- internal pull high (+5V)

Rev:3A 01/29 Change pull-up Resistors to 2.2K

Reserve Test Port

Rev:3A/3C 05/09 AMD CPU noise sensitivity be added termination resistor.

CPU H/W MONITOR

Rev:3A 02/29 GMT G781 Reverse R133 0 Ohm For Thermal Sensor issue.

MAX6657,G781P8,W83L771G

OVERT# Check EC Setting Degree

ADDRESS: 98H

Serial VID

Serial VID Clock

Serial VID Data

VFIX MODE / VID Override Circuit

SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

HDT Connector

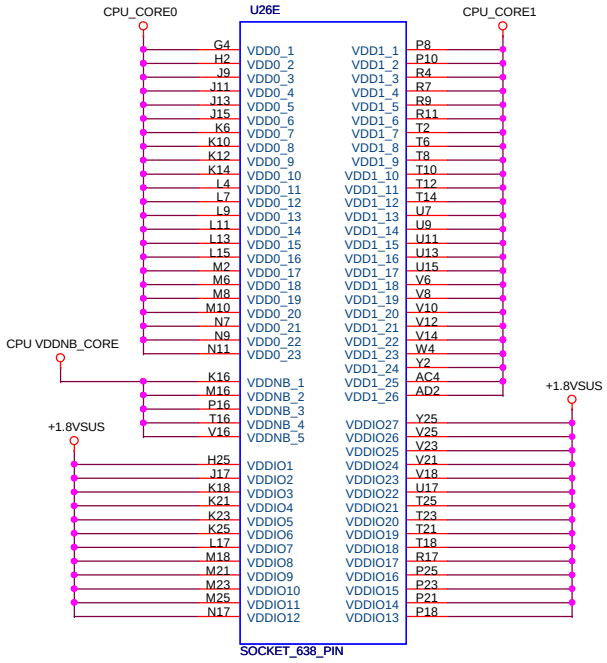
*HDT CONN

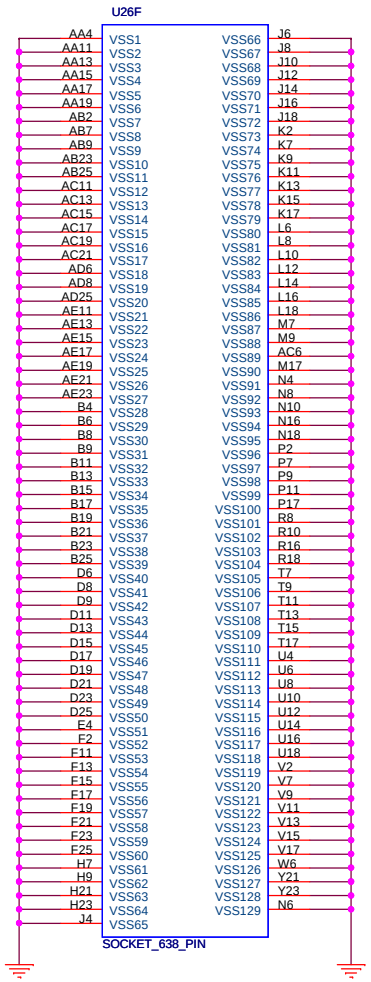
PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 CTRL & DEBUG 3/4	1A

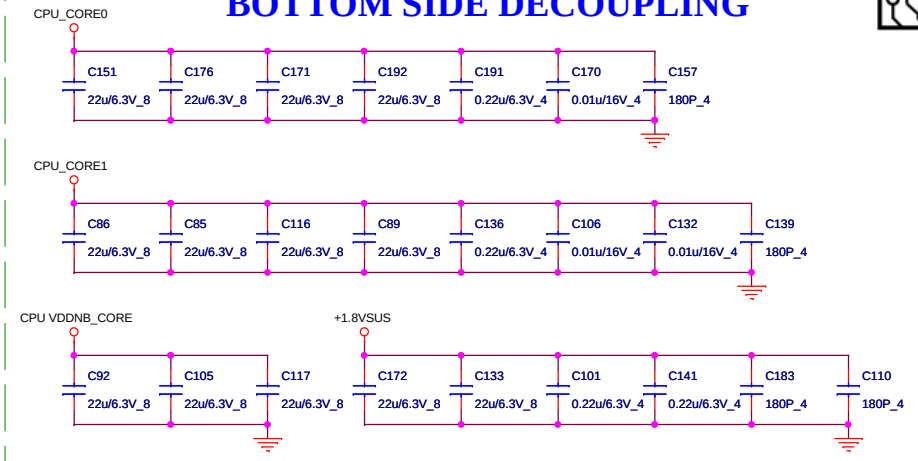
Date: Thursday, July 24, 2008 | Sheet 6 of 35

CPU

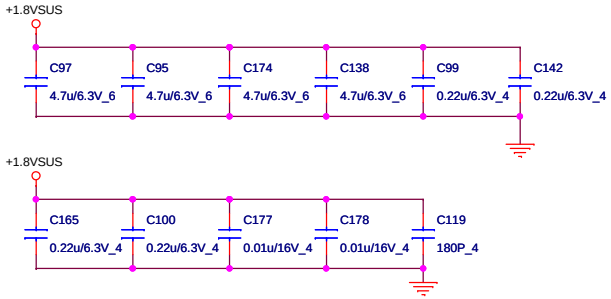




BOTTOM SIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



PROCESSOR POWER AND GROUND

NB4

PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 PWR & GND 4/4	1A

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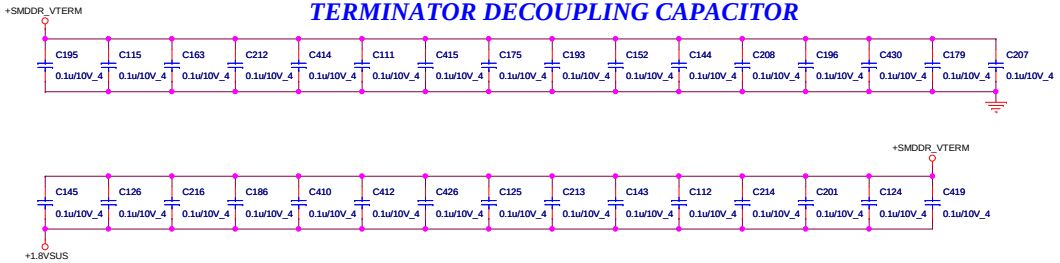
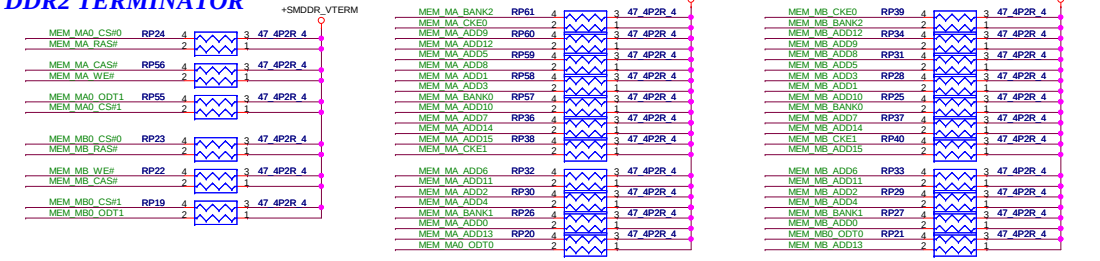
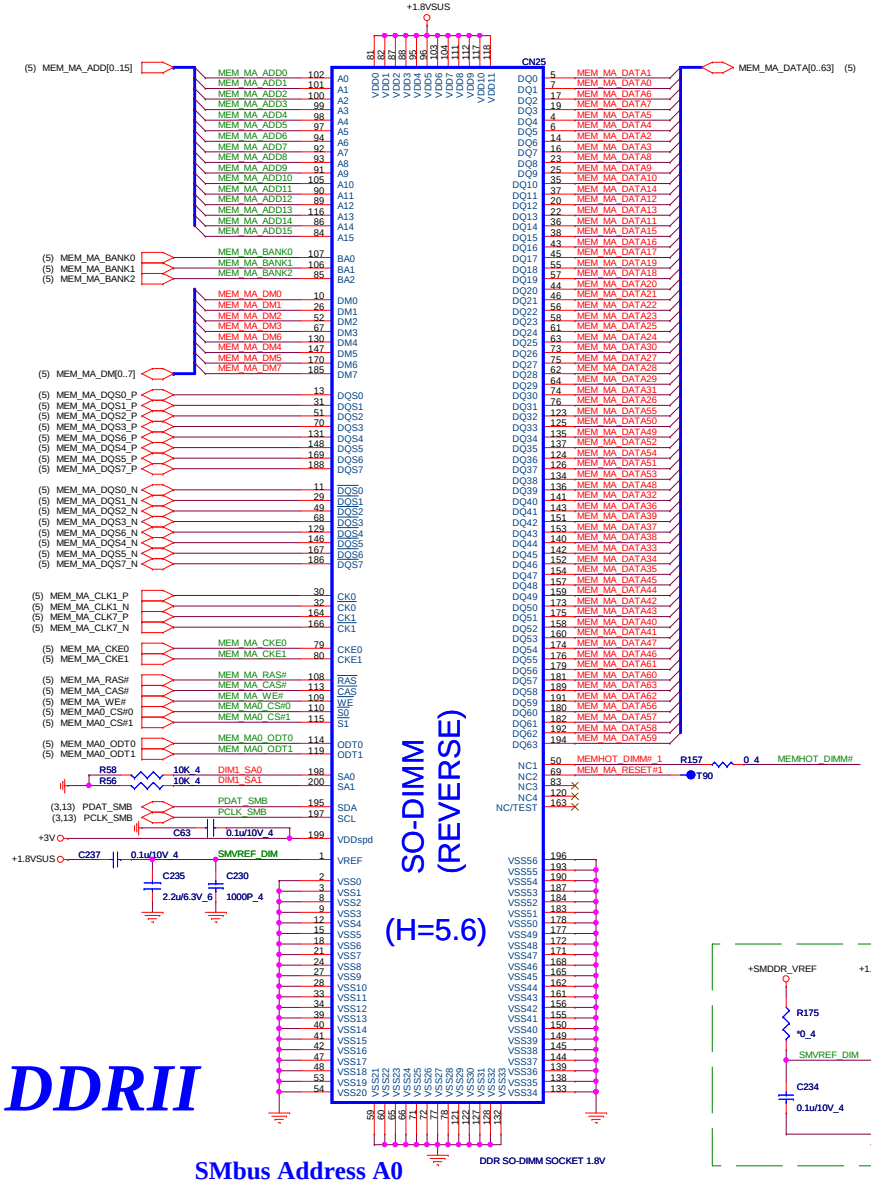
TERMINATOR DECOUPLING CAPACITOR



DDR2 TERMINATOR



08



DDRII

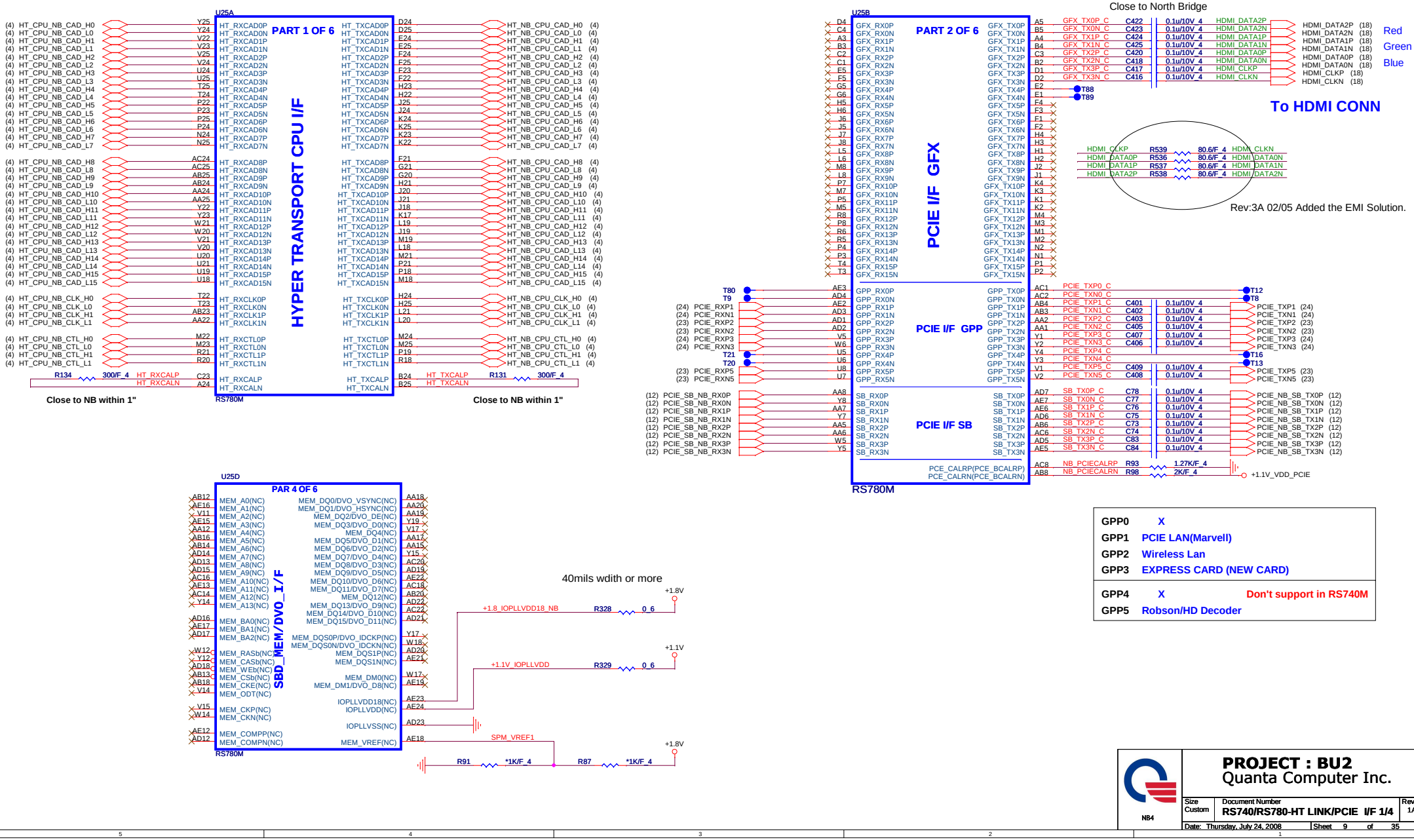
PROJECT : BU2 Quanta Computer Inc.		
Size: Custom	Document Number: DDR2 SODIMMS: A/B CHANNEL	Rev: 1A
Date: Thursday, July 24, 2008	Sheet 8 of 35	
NB4		

RS780

09

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1



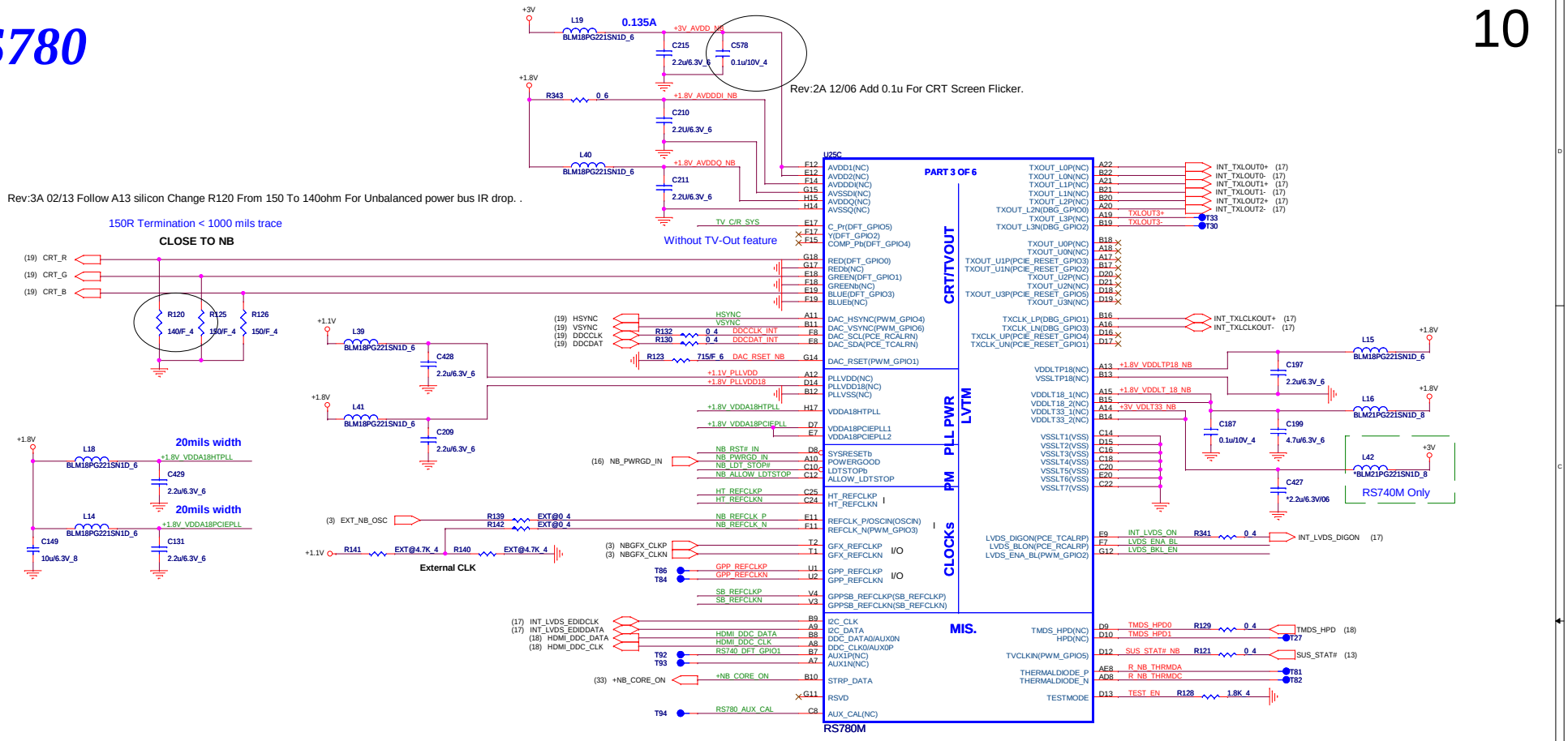
GPP0	X
GPP1	PCIE LAN(Marvell)
GPP2	Wireless Lan
GPP3	EXPRESS CARD (NEW CARD)
GPP4	X — Don't support in RS740M
GPP5	Robson/HD Decoder

PROJECT : BU2
Quanta Computer Inc.

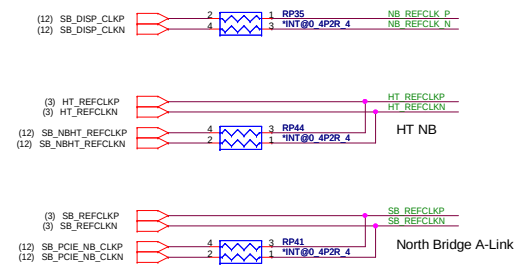
Size	Document Number	Rev
Custom	RS740/RS780-HT LINK/PCIE I/F 1/4	1A

Date: Thursday, July 24, 2008 Sheet 9 of 35

RS780

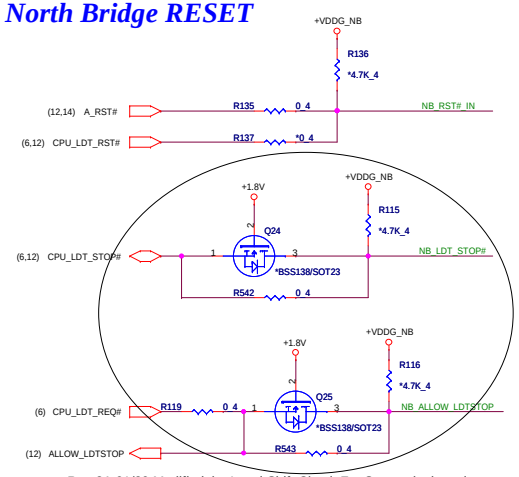


FOR SB INTERNAL CLOCK

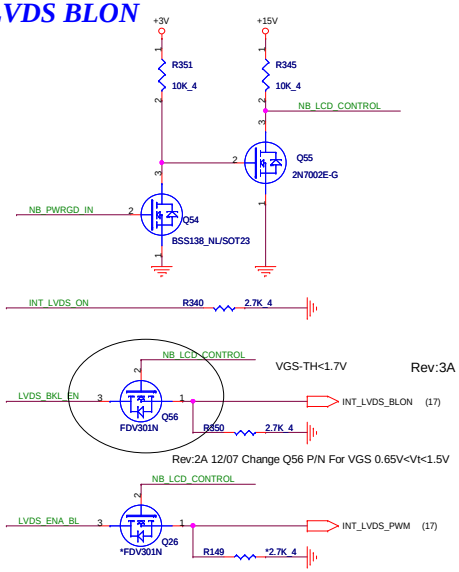


Reserve Pin

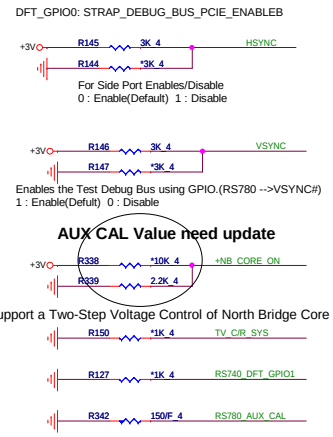
North Bridge RESET



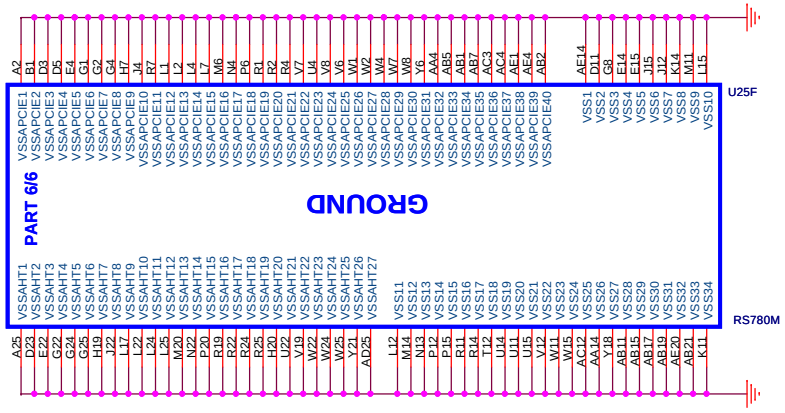
LVDS BLON



STRAP DEBUG BUS GPIO

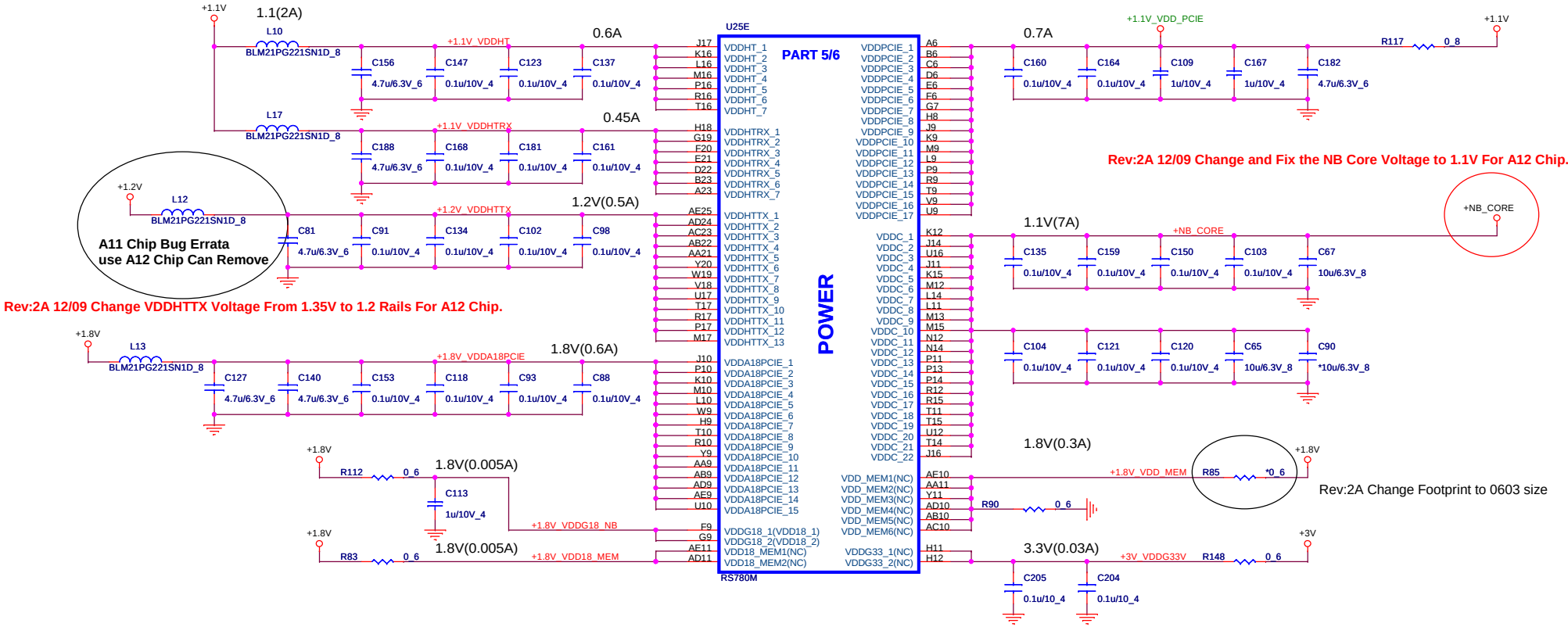


PROJECT : BU2 Quanta Computer Inc.		
Size: Custom	Document Number: RS740/RS780-SYSTEM I/F 3/5	Rev: 1A
Date: Thursday, July 24, 2008	Sheet 10 of 35	



RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



RS780

SB700

FOR INTERNAL CLOCK

(3,6) CPU_CLKP
(3,6) CPU_CLKN
RP42 *INT@0_4P2R_4 SB_CPU_CLKIN_P SB_CPU_CLKIN_N

(3,24) CLK_PCIE_NEW
(3,24) CLK_PCIE_NEW#
RP69 *INT@0_4P2R_4 SB_GPP_CLK1P SB_GPP_CLK1N

(3,23) CLK_PCIE_MINI2
(3,23) CLK_PCIE_MINI2#
RP77 *INT@0_4P2R_4 SB_GPP_CLK3P SB_GPP_CLK3N

Place close to CLK GEN

AC COUPLING CAPS CLOSE TO SB700

(18,23,24,28) PLTRST# R490 33_4
(10,14) A_RST# R491 33_4 A_RST#_SB

(9) PCIE_SB_NB_RX0P C470 0.1u/10V_4 A_RX0P_C
(9) PCIE_SB_NB_RX0N C471 0.1u/10V_4 A_RX0N_C
(9) PCIE_SB_NB_RX1P C469 0.1u/10V_4 A_RX1P_C
(9) PCIE_SB_NB_RX1N C468 0.1u/10V_4 A_RX1N_C
(9) PCIE_SB_NB_RX2P C466 0.1u/10V_4 A_RX2P_C
(9) PCIE_SB_NB_RX2N C467 0.1u/10V_4 A_RX2N_C
(9) PCIE_SB_NB_RX3P C464 0.1u/10V_4 A_RX3P_C
(9) PCIE_SB_NB_RX3N C465 0.1u/10V_4 A_RX3N_C

(9) PCIE_NB_SB_TX0P
(9) PCIE_NB_SB_TX0N
(9) PCIE_NB_SB_TX1P
(9) PCIE_NB_SB_TX1N
(9) PCIE_NB_SB_TX2P
(9) PCIE_NB_SB_TX2N
(9) PCIE_NB_SB_TX3P
(9) PCIE_NB_SB_TX3N

R383 562/F_4 SB_PCIE_CALRP
R382 2.05K/F_4 SB_PCIE_CALRN

+1.2V_PCIE_VDDR
+1.2V L24 BLM18PG221SN1D_6 +1.2V_PCIE_PVDD
C245 10u/6.3V_8 C247 1u/10V_4
40mA

1.PCIE Reference Clk(Ext Clk Gen)
2. A-Link Clk to North Bridge(Int Clk Gen)

Ext: Clk Gen
Int: A-Link Clock to NB

From Clk Gen Input (3) SBSRC_CLKP (3) SBSRC_CLKN RP48 EXT@0_4P2R_4 EXT

To NB A-Link CLK (10) SB_PCIE_NB_CLKP (10) SB_PCIE_NB_CLKN RP76 *INT@0_4P2R_4 INT PCIE_RCLKP N25 PCIE_RCLKN N24

For North Bridge (10) SB_DISP_CLKP (10) SB_DISP_CLKN RP47 *INT@0_4P2R_4 NB_DISP_CLKP K23 NB_DISP_CLKN K22

For North Bridge (10) SB_NBHT_REFCLKP (10) SB_NBHT_REFCLKN RP75 *INT@0_4P2R_4 NB_HT_CLKP M24 NB_HT_CLKN M25

For CPU Host Clk SB_CPU_CLKIN_P SB_CPU_CLKIN_N RP50 *INT@0_4P2R_4 CPU_HT_CLKP P17 CPU_HT_CLKN M18
Close to SB R196 *261/F_4

SLT_GFX_CLKP M23 SLT_GFX_CLKN M22

To Marvell Lan (3,24) PCIE_CLK_LAN (3,24) PCIE_CLK_LAN# RP46 *INT@0_4P2R_4 GPP_CLK0P J19 GPP_CLK0N J18

To New Card SB_GPP_CLK1P SB_GPP_CLK1N RP51 *INT@0_4P2R_4 GPP_CLK1P L20 GPP_CLK1N L19

(3,23) PCIE_CLK_MINI (3,23) PCIE_CLK_MINI# RP49 *INT@0_4P2R_4 GPP_CLK2P M19 GPP_CLK2N M20

To Mini Card 1,2 SB_GPP_CLK3P SB_GPP_CLK3N RP74 *INT@0_4P2R_4 GPP_CLK3P N22 GPP_CLK3N P22

T48 L18

C266 *22P_4 SB700_25M_X1 J21
Y4 *25MHZ R207 *10M_6
C270 *22P_4 SB700_25M_X2 J20
Install for Int Clk Gen

RTC_X1 A3
RTC_X2 B3
+1.8VSUS +1.8V
R194 *10K_4 R193 *10K_4

(10) ALLOW_LDTSTOP F23
(6) CPU_PROCHOT# F22
(6) CPU_PWRGD G25
(6,10) CPU_LDT_STOP# G24
(6,10) CPU_LDT_RST# F24

U34A
SB700
Part 1 of 5
SB700

A_RST# N2
PCIE_TX0P PCIE_TX0N PCIE_TX1P PCIE_TX1N PCIE_TX2P PCIE_TX2N PCIE_TX3P PCIE_TX3N
PCIE_RX0P PCIE_RX0N PCIE_RX1P PCIE_RX1N PCIE_RX2P PCIE_RX2N PCIE_RX3P PCIE_RX3N
PCIE_CALRP T25 PCIE_CALRN T24
PCIE_PVDD P24 PCIE_PVSS P25
PCIE EXPRESS INTERFACE

PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP NB_DISP_CLKN
NB_HT_CLKP NB_HT_CLKN 100MHZ
CPU_HT_CLKP CPU_HT_CLKN
SLT_GFX_CLKP SLT_GFX_CLKN
GPP_CLK0P GPP_CLK0N
GPP_CLK1P GPP_CLK1N
GPP_CLK2P GPP_CLK2N
GPP_CLK3P GPP_CLK3N
25M_48M_66M_OSC
25M_X1
25M_X2
CLOCK GENERATOR

X1 X2
RTC XTAL

ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
CPU

RTCCLK C3
INTRUDER_ALERT# C2
VBAT B2
RTC

PCI CLKS
PCICLK0 P4 PCI_CLK0_R R510 22_4 PCLK_OZ129 (22)
PCICLK1 P3 PCI_CLK1_R R509 CB@22_4 PCLK_PCM (21)
PCICLK2 P1 PCI_CLK2_R R493 22_4 PCI_CLK2 (16)
PCICLK3 P2 PCI_CLK3_R R514 22_4 PCI_CLK3 (16)
PCICLK4 T4 PCI_CLK4_R R498 22_4 PCI_CLK4 (16)
PCICLK5/GPIO41 T3 PCI_CLK5_R R496 22_4 PCI_CLK5 (16)

PCIRST# N1 PCIRST#_SB700 R492 33_4 PCIRST# (21,22)

PCI INTERFACE
AD[0..31] AD[0..31] (16,21,22)
AD0 U2 AD1 P7 AD2 V4 AD3 T1 AD4 V3 AD5 U1 AD6 V1 AD7 V2 AD8 T2 AD9 W1 AD10 T9 AD11 R6 AD12 R7 AD13 R5 AD14 U8 AD15 U5 AD16 Y7 AD17 W8 AD18 V9 AD19 Y8 AD20 AA8 AD21 Y4 AD22 Y3 AD23 Y2 AD24 AA2 AD25 AB4 AD26 AA1 AD27 AB3 AD28 AB2 AD29 AC1 AD30 AC2 AD31 AD1

+3V
REQ0# R424 *8.2K_4
REQ1# R422 *8.2K_4
GNT3# R474 8.2K_4
GNT3# R473 *8.2K_4
SB_GPIO65 R464 100K_4

CBE0# U7 CBE1# AA7 CBE2# Y1 CBE3# AA6 FRAME# W5 DEVSEL# AA5 IRDY# Y5 TRDY# U6 PAR W6 STOP# W4 PERR# V7 SERR# AC3 REQ0# AD4 REQ1# AB7 REQ2# AE6 REQ3#/GPIO70 AB6 REQ4#/GPIO71 AD2 GNT0# AE4 GNT1# AD5 GNT2# AC6 GNT3#/GPIO72 AE5 GNT4#/GPIO73 AD6 CLKRUN# V5 LOCK# AD3 INTE#/GPIO33 AC4 INTF#/GPIO34 AE2 INTG#/GPIO35 AE3 INTH#/GPIO36
CBE0# (21,22) CBE1# (21,22) CBE2# (21,22) CBE3# (21,22) FRAME# (21,22) DEVSEL# (21,22) IRDY# (21,22) TRDY# (21,22) PAR (21,22) STOP# (21,22) PERR# (21) SERR# (21) REQ0# (22) REQ1# (21)
T115 PORT_C# (26)
T124 GNT0# (22) GNT1# (21)
T118
Rev:2A 12/06 DEL G-Sensor SCI Event(GPIO).
T117 R470 0_4 CLKRUN# (22,28)
Rev:3C 05/09 Remove Test Ports For Space Limiting.
INTE# (22) INTF# (21)
R241 FM@0_4 R124 *CS@0_4 FM_INT (24) HDPINT (19)

LPC
LPCCLK0 G22 LPCCLK0_R R412 22_4 PCLK_591 (16,28)
LPCCLK1 E22 LPCCLK1_R R411 22_4 PCLK_DEBUG (16,23)
LAD0 H24 LAD1 H23 LAD2 J25 LAD3 J24 LFRAME# H25 LDRQ0# H22 LDRQ1#/GNT5#/GPIO68 AB8 BMREQ#/REQ5#/GPIO65 AD7 SERIRQ V15
LAD0 (23,28) LAD1 (23,28) LAD2 (23,28) LAD3 (23,28) LFRAME# (23,28) LDRQ#0 (23)
LDRQ1# SB T51
SB_GPIO65 T113
SERIRQ (21,23,28)

INTRUDER_ALERT# T119
RTC_CLK (16)
VCCRTC
20MIL
C537 1u/10V_4 C541 0.1u/10V_4

Rev:3B 04/02 As the same location Name(G1) For Toshiba Service Team Request.

+3VPCU D31 RB500 VCCRTC
TERM13 D33 RB500 +3VRTC R364 510/F_6
C443 1U/10V_4
G1 *SHORT_ PAD1
R366 1K_4

Rev:3A 02/13 RTC Circuit R363/R360/R359/R361 Follow Standar Circuit Value.

+5VPCU
TERM12 TERM11 TERM15
R363 2K/F_4 R360 2K/F_4
Q57 MMBT3904
R359 6.8K/F_4
20MIL
TERM14
CN27 ACS_85204-0200L
R361 15K/F_6

Rev:2A 12/07 Change Part Number.

RTC

Rev:3A 02/05 No-Stuff R194 For Leakage when system into G3 mode.

RTC_X1
Y8 32.768KHZ
R454 *20M_6
RTC_X2
R465 20M_6
C527 18P_4 C535 18P_4

NB4	PROJECT : BU2 Quanta Computer Inc.	
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SB700

EMI

CLK_48M_USB — R446 *10_4 — C514 *10P_4

+1.8VSUS

R66 2.2K_4 SB_SCLK3
R67 2.2K_4 SB_SDATA3

+3V_S5

R414 2.2K_4 SB_SCLK2
R418 2.2K_4 SB_SDATA2
R487 2.2K_4 SB_SMBCLK1
R486 2.2K_4 SB_SMBDATA1
R568 10K_4 USBOC5_GPM5

Rev:2A 12/06 Support the New Card Hot Plug Function.

Rev:3B 04/07 USB Overcurrent 5 Pull-up 10K For Open Drain.

+3V

R485 4.7K_4 SUS_STAT#
R434 *10K_4 SB_CLK_REQ1#
R227 2.2K_4 PCLK_SMB
R224 2.2K_4 PDAT_SMB

Rev:2A 12/06 DEL G-Sensor SCI Event(GPIO).

Rev:3A 02/05 Move Board ID4 Pin Name From GPIO66 to GPIO3.

G3 *SHORT_PAD1 SYS_RST#

Rev:3B 04/07 Added the USB Overcurrent 3 to Support USB 2.0 Ports.

Rev:3A 02/05 Move Hot Plug Pin Name From GEVENT5# to GPM1.

U34D — SB700 — Part 4 of 5 — 48MHz

(21,22) PCI_PME# — RI# — SLP_S2
(16,28) SUSB# — (28) SUSC# — (28) DNBSWON# — (16) SB_PWRGD_IN — (10) SUS_STAT#
R482 *2.2K_4 SB_TEST2
R483 *2.2K_4 SB_TEST1
R484 *2.2K_4 SB_TEST0
(28) GATEA20 — (28) RCIN# — (28) SCI# — T103 — T126 — SYS_RST#
(23,24) PCIE_WAKE# — T121 — GPM6#
(6) CPU_THERMTRIP# — (16) WD_PWRGD
(28) RSMRST# — R54 0_4 SB_RSMRST#

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

USBCLK/14M_25M_48M_OSC — C8 CLK_48M_USB — CLK_48M_USB (3) Input
USB_RCOMP — G8 USB_RCOMP_SB — R238 11.8K/F_6

USB MISC

USB 1.1

USB_FSD13P — E6
USB_FSD13N — E7
USB_FSD12P — F7
USB_FSD12N — E8
USB_HSD11P — H11 — USB_FSD11P — R477 0_4 — USBP7+
USB_HSD11N — J10 — USB_FSD11N — R572 0_4 — USBP7-
USB_HSD10P — E11 — USBP10+ (20)
USB_HSD10N — F11 — USBP10- (20)
USB_HSD9P — A11 — USB_FSD9P — T104
USB_HSD9N — B11 — USB_FSD9N — T105
USB_HSD8P — C10 — USBP8+ (23)
USB_HSD8N — D10 — USBP8- (23)
USB_HSD7P — G11 — USB_FSD7P — R573 *0_4 — USBP7+ — USBP7+ (20)
USB_HSD7N — H12 — USB_FSD7N — R574 *0_4 — USBP7- — USBP7- (20)
USB_HSD6P — E12 — USBP6+ (25)
USB_HSD6N — E14 — USBP6- (25)
USB_HSD5P — C12 — USBP5+ (25)
USB_HSD5N — D12 — USBP5- (25)
USB_HSD4P — B12 — USBP4+ (23)
USB_HSD4N — A12 — USBP4- (23)
USB_HSD3P — G12 — USBP3+ (24)
USB_HSD3N — G14 — USBP3- (24)
USB_HSD2P — H14 — USBP2+ (17)
USB_HSD2N — H15 — USBP2- (17)
USB_HSD1P — A13 — USBP1+ (25)
USB_HSD1N — B13 — USBP1- (25)
USB_HSD0P — B14 — USBP0+ (24)
USB_HSD0N — A14 — USBP0- (24)

USB 2.0

Rev:3C 04/08 Reserve the 0hm to USB7 Controller.
Rev:3A 03/03 Swap USB CONN From USB11 to USB7 For Controller ESATA Certification.
Rev:2A 12/11 Swap the New Card From USB7 to USB3 For OHCI Controllers.

E-SATA and USB Connector
TV/HD DECODER Min-Card
USB Connector
BLUETOOTH
FINGERPRINT
Min-Card
NEW CARD
CAMERA USB
Felica
USB Connector(RJ45/USB BOARD)

BOARD_ID2 — BOARD_ID1 — BOARD_ID0
(24) FM_CLK — R201 FM@0_4 FM_CLK_REQ0#
(3,24) NEW_CLKREQ# — R437 *0_4 SB_CLK_REQ1#
(24) FM_DATA — R200 FM@0_4 FM_DATA_REQ2#
(24) SPKR
(3,8) PCLK_SMB — PCLK_SMB
(3,8) PDAT_SMB — PDAT_SMB
(23,24) SB_SMBCLK1 — SB_SMBCLK1
(23,24) SB_SMBDATA1 — SB_SMBDATA1
(24) FM_DETECT — FM_DETECT
(23) PDMA66
(25) LOW_DET — T127 — LLB#/GPIO66
(19) HDPACT — R240 *GS@0_4 GEVENT7#

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#

GPIO

(6,8) CPU_MEMHOT# — D39 CH501H-40PT — CPU_MEMHOT# IN
(20,28) USBOC#5 — R445 0_4 — USBOC5_GPM5
T128 — R569 0_4 — USBOC4_GPM4 / USBOC3_GPM3
(24) NEW_DET# — T63 — R544 NEW@0_4 — SB_JTAG_TCK / USBOC1_GPM1
(24,28) USBOC#0

USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#

USB OC

(26) ACZ_SDIN0 — T58 — T71 — T116 — ACZ_BCLK / ACZ_SDOUT
(16) ACZ_RST# — ACZ_SYNC / ACZ_RST#

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#

HD AUDIO

IMC_GPIO8 — A18
IMC_GPIO9 — B18
IMC_PWM0/IMC_GPIO10 — F21
SCL2/IMC_GPIO11 — D21 — SB_SCLK2 — SB_SCLK2 (18)
SDA2/IMC_GPIO12 — F19 — SB_SDATA2 — SB_SDATA2 (18)
SCL3_LV/IMC_GPIO13 — E20 — SB_SCLK3 — SB_SCLK3 (6)
SDA3_LV/IMC_GPIO14 — E21 — SB_SDATA3 — SB_SDATA3 (6)
IMC_PWM1/IMC_GPIO15 — E19
IMC_PWM2/IMC_GPIO16 — D19 — SB_GPIO16 (16)
IMC_PWM3/IMC_GPO17 — E18 — SB_GPIO17 (16)

SPI/LPC define

IMC_GPIO18 — G20
IMC_GPIO19 — G21
IMC_GPIO20 — D25
IMC_GPIO21 — D24
IMC_GPIO22 — C25
IMC_GPIO23 — C24
IMC_GPIO24 — B25
IMC_GPIO25 — C23
IMC_GPIO26 — B24
IMC_GPIO27 — B23
IMC_GPIO28 — A23
IMC_GPIO29 — C22
IMC_GPIO30 — A22
IMC_GPIO31 — B22
IMC_GPIO32 — B21
IMC_GPIO33 — A21
IMC_GPIO34 — D20
IMC_GPIO35 — C20
IMC_GPIO36 — A20
IMC_GPIO37 — B20
IMC_GPIO38 — B19
IMC_GPIO39 — A19
IMC_GPIO40 — D18
IMC_GPIO41 — C18

INTEGRATED uC

+1.8V — R167 20K_4 — (23) HDD_AUX_RST#

IMC_GPIO0 — H19
IMC_GPIO1 — H20
SPI_CS2#/IMC_GPIO2 — H21
IDE_RST#/F_RST#/IMC_GPO3 — F25
IMC_GPIO4 — D22
IMC_GPIO5 — E24
IMC_GPIO6 — E25
IMC_GPIO7 — D23

INTEGRATED uC

SB700

Rev:3B 04/18 There is internal 8.2K of I/O Balls So Change Pull-Down Resistors From 10K to 1K.

HD Audio Interface

To Azalia
(26) BIT_CLK_AUDIO — R489 33_4 — ACZ_BCLK — C554 *10P_4

To Azalia
(26) ACZ_SDOUT_AUDIO — R488 33_4 — ACZ_SDOUT — C553 *10P_4

To Azalia
(26) ACZ_SYNC_AUDIO — R259 33_4 — ACZ_SYNC — C336 *10P_4

To Azalia
(26) ACZ_RST#_AUDIO — R504 33_4 — ACZ_RST#

MB ID Selection Table

BOARD_ID	BOARD_ID0	BOARD_ID1	BOARD_ID2	FM_DETECT	BOARD_ID4	LOW_DET
W/ New Crad W/ Crad Bus	H L					
W/ CCFL Panel W/ LED Panel		H L				
W/ G-Sensor W/O G-Sensor			H L			
W/O FM W/FM				H L		
W/ HDMI W/O HDMI					H L	
Main Strem Low Cost						H L

MB ID

+3V

R206 *CB@1K_4 BOARD_ID0 R205 NEW@10K_4
R215 *LED@1K_4 BOARD_ID1 R214 LCD@10K_4
R219 *W/O@1K_4 BOARD_ID2 R218 *GS@10K_4
R210 *FM@1K_4 FM_DETECT R209 W/O@10K_4
R245 *W/O@1K_4 BOARD_ID4 R250 HDM@10K_4
R203 *LOW@1K_4 LOW_DET R202 MAIN@10K_4

BOARD_ID4 — BOARD_ID4 (14)

N84

PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
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SB700

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

SATA HDD

E-SATA

SATA ODD

U34B

SB700
Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

HW MONITOR

SATA PWR

Rev:3B 04/18 Change HDD Control From Channel/2 to Channel/0 For Spin Down Issue.

Rev:3A 02/22 Change Setting the SATA ODD to be IDE Legacy class Mode..

NOTE:
R635 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

Rev:2A 12/07 Cahnge C259/C260 Load Capacitance For Matching Crystal.

Rev:3C 04/08 Reserve the Board ID For USB Controller.
Rev:3A 02/05 Added the Board ID4 to GPIO3..

Rev:3C 05/09 Remove Test Ports For Space Limiting.

Rev:3C 05/09 Remove Test Ports For Space Limiting.

Rev:2A 12/07 Change +3V Domain For System Leakage When System into S5 Mode.

77mA
1mA
5mA

Place near ball

AVDD--H/W Monitor Analog power

NB4	**PROJECT : BU2** Quanta Computer Inc.	
Size: Custom	Document Number: SB700-ACPI/GPIO/USB 2/4	Rev: 1A
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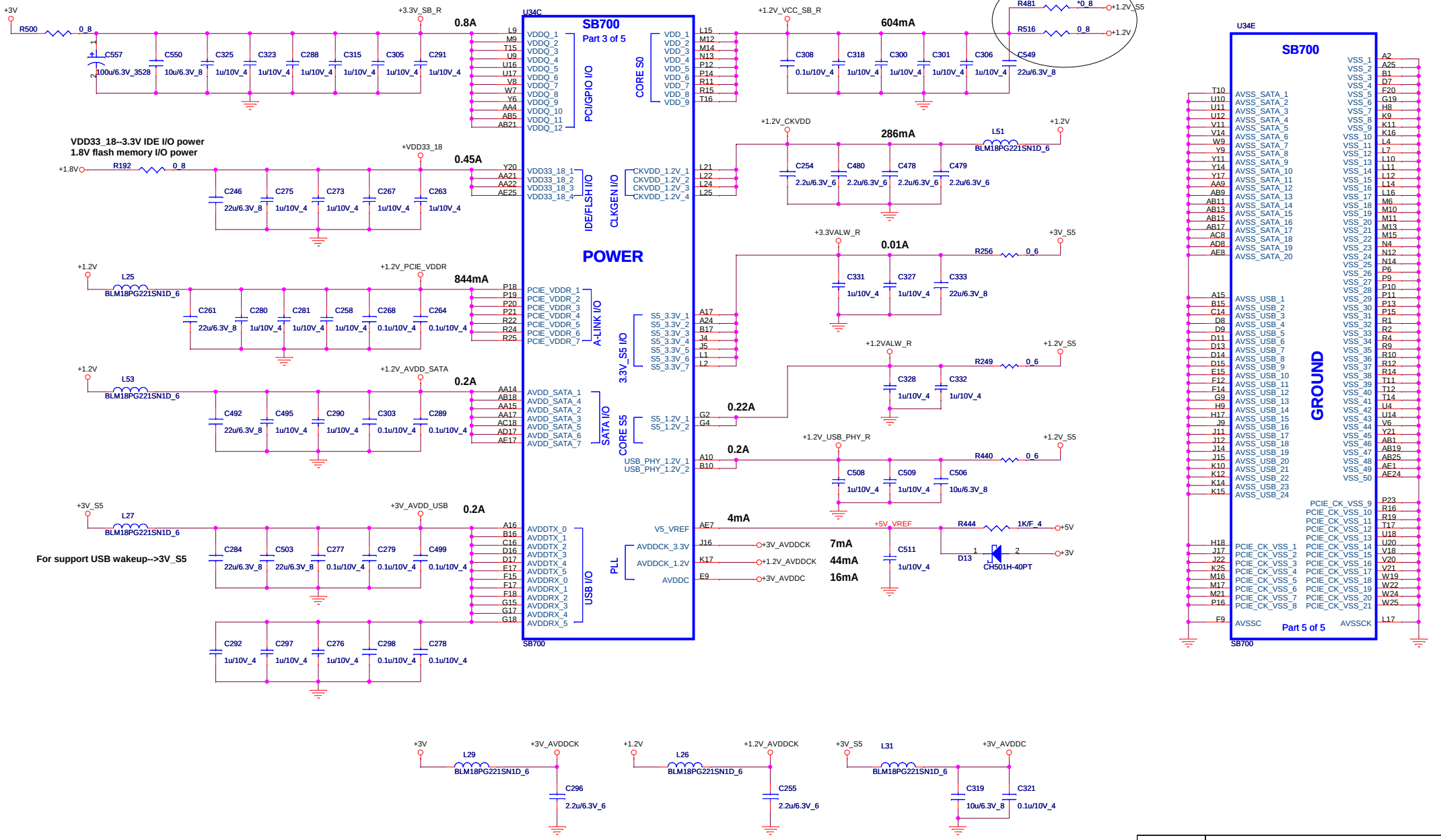
SB700

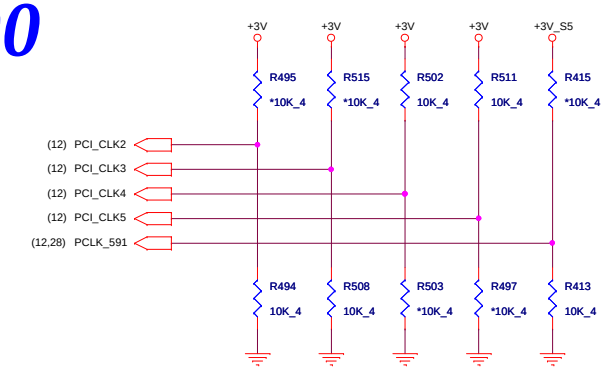
PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

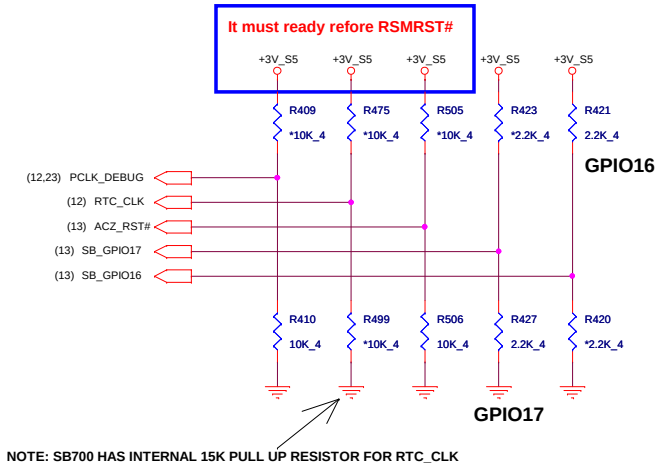
Rev:2A 12/10 The VDD Power Pin to be connected to S0_1.2V Power For A12 Chip.

A11 Chip Bug
use A12 Chip Can Remove



SB700





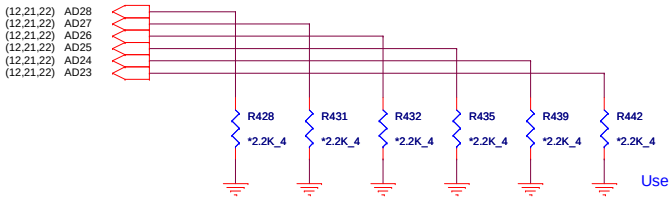
REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT

	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

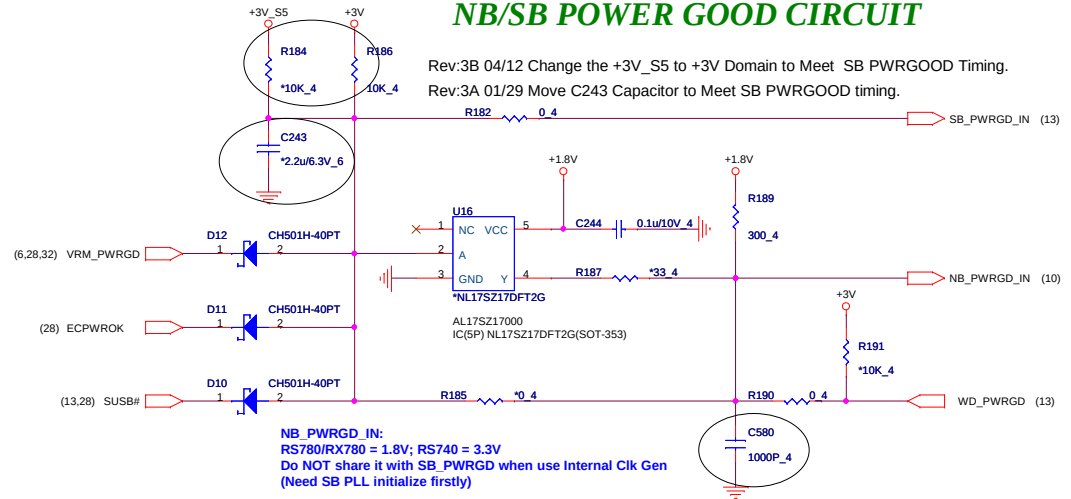


REQUIRED STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB/SB POWER GOOD CIRCUIT

Rev:3B 04/12 Change the +3V_S5 to +3V Domain to Meet SB PWRGOOD Timing.
Rev:3A 01/29 Move C243 Capacitor to Meet SB PWRGOOD timing.



NB4

PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-STRAPS & PWRGD	1A

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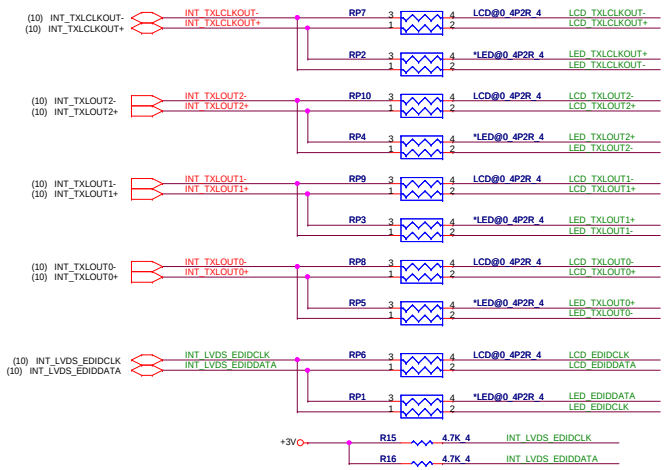
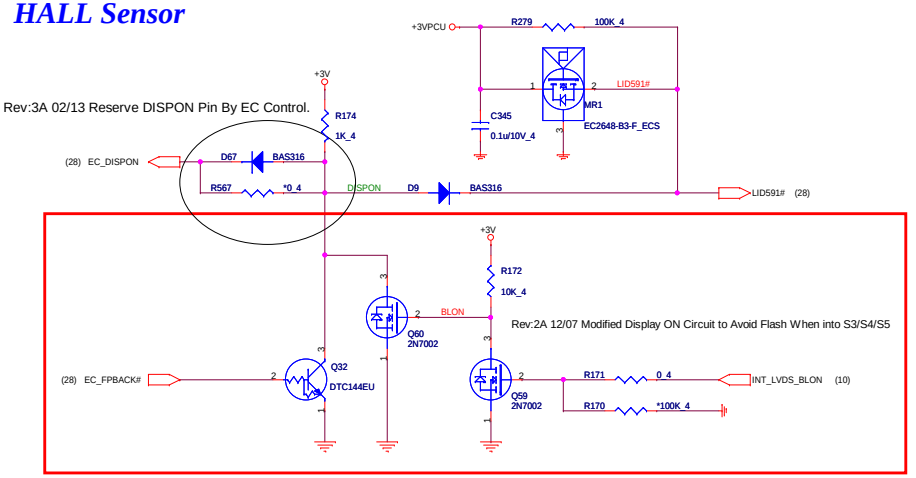
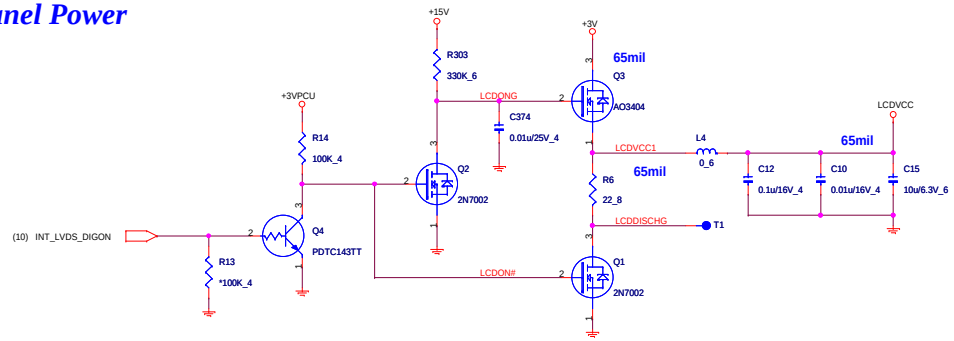
Panel Source



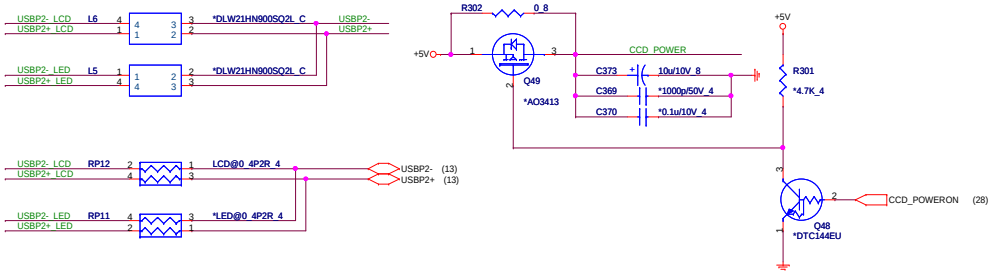
HALL Sensor



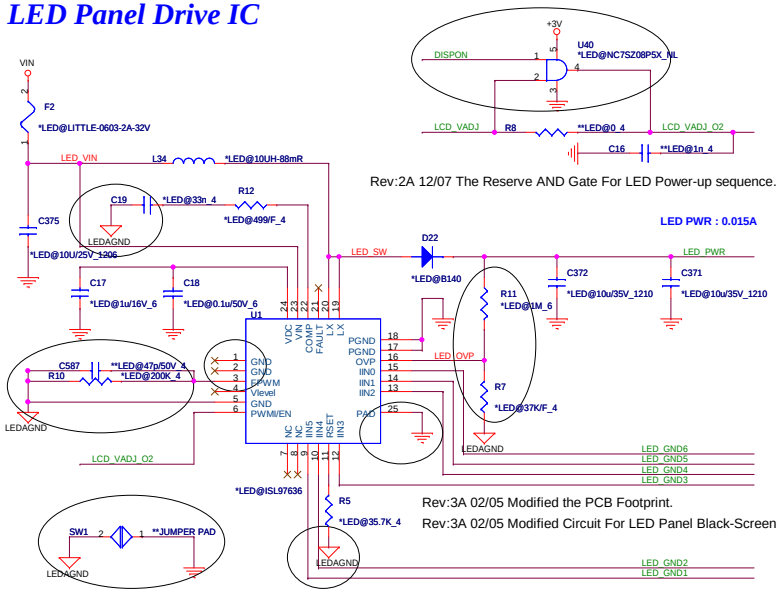
Panel Power



CAMERA Module



LED Panel Drive IC



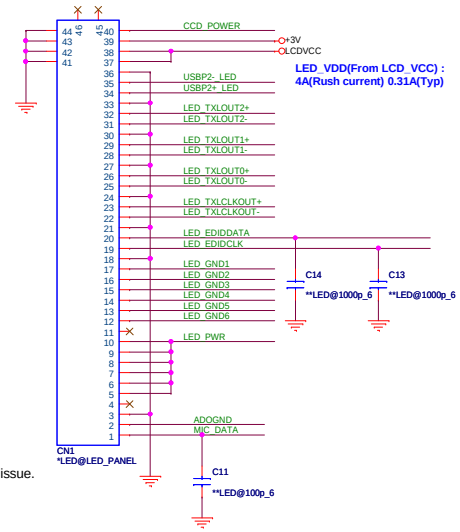
Rev:2A 12/07 The Reserve AND Gate For LED Power-up sequence.

LED PWR : 0.015A

Rev:3A 02/05 Modified the PCB Footprint.

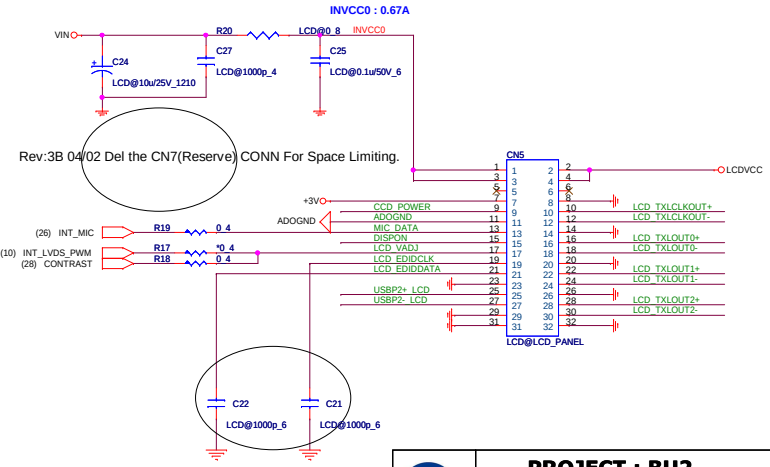
Rev:3A 02/05 Modified Circuit For LED Panel Black-Screen issue.

TOSHIBA LED Panel Module



LED_VDD(From LCD_VCC) : 4A(Rush current) 0.31A(Typ)

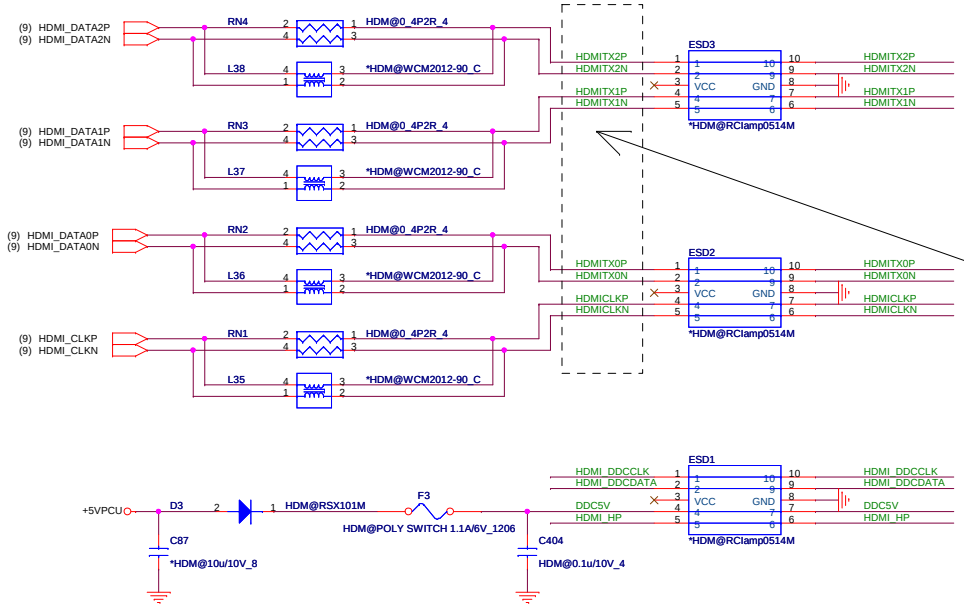
LCD Panel Module



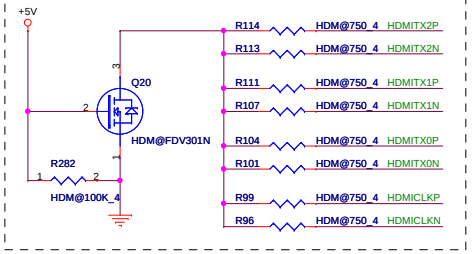
Rev:3B 04/12 Stuff C21/C22 For EMI Suggest.

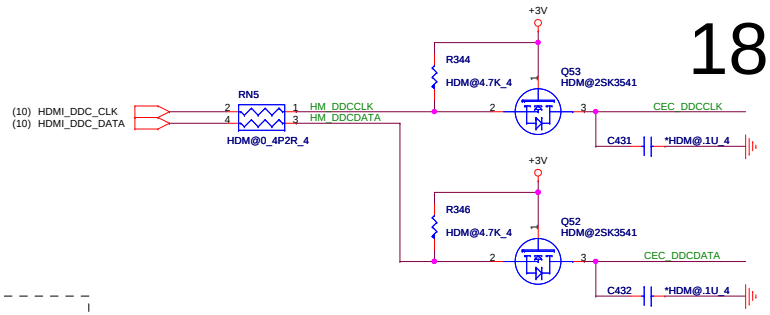
N84	PROJECT : BU2 Quanta Computer Inc.	
Size: Custom	Document Number: LCD/LED PANEL/LID/CAMERA	Rev: 1A
Date: Thursday, July 24, 2008	Sheet 17 of 35	

HDMI

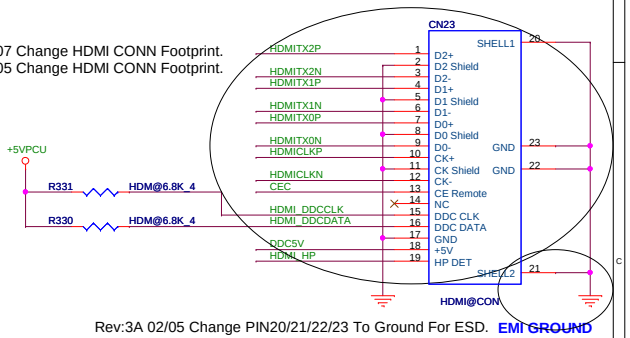


Place to HDMI Signal Pairs/ESD Side.



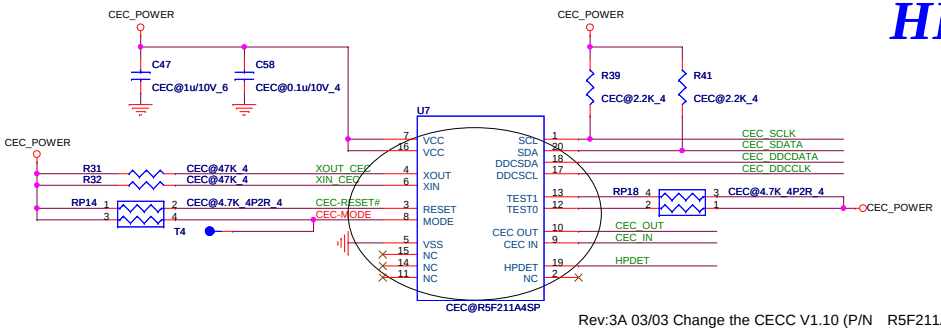


Rev:2A 12/07 Change HDMI CONN Footprint.
Rev:3A 02/05 Change HDMI CONN Footprint.

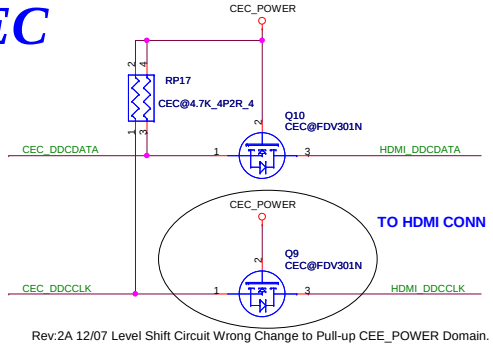


Rev:3A 02/05 Change PIN20/21/22/23 To Ground For ESD. **EMI GROUND**

HDMI-CEC

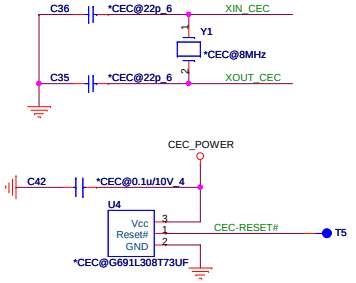


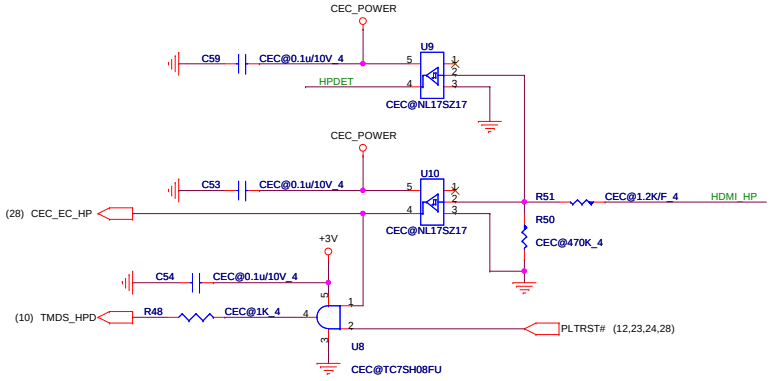
Rev:3A 03/03 Change the CECC V1.10 (P/N R5F211A4C22SP)

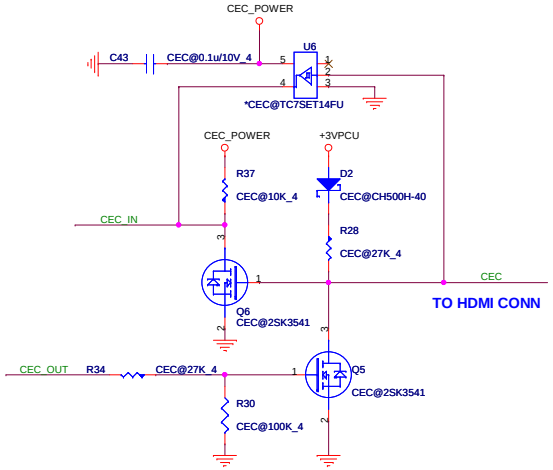


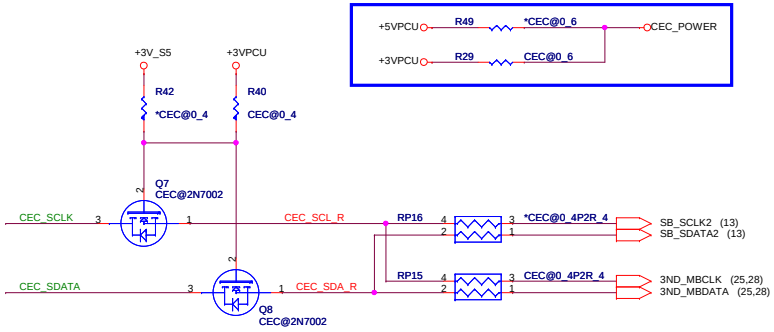
Rev:2A 12/07 Level Shift Circuit Wrong Change to Pull-up CEE_POWER Domain.

Clock/Test Pad





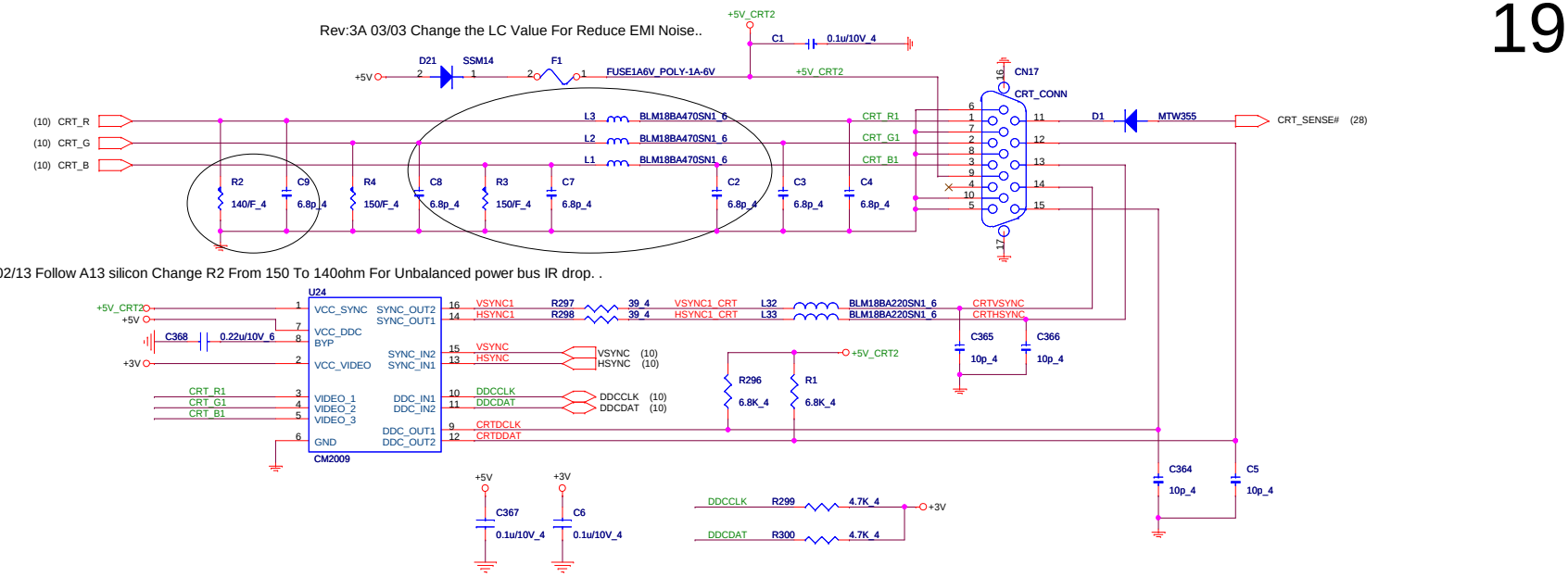




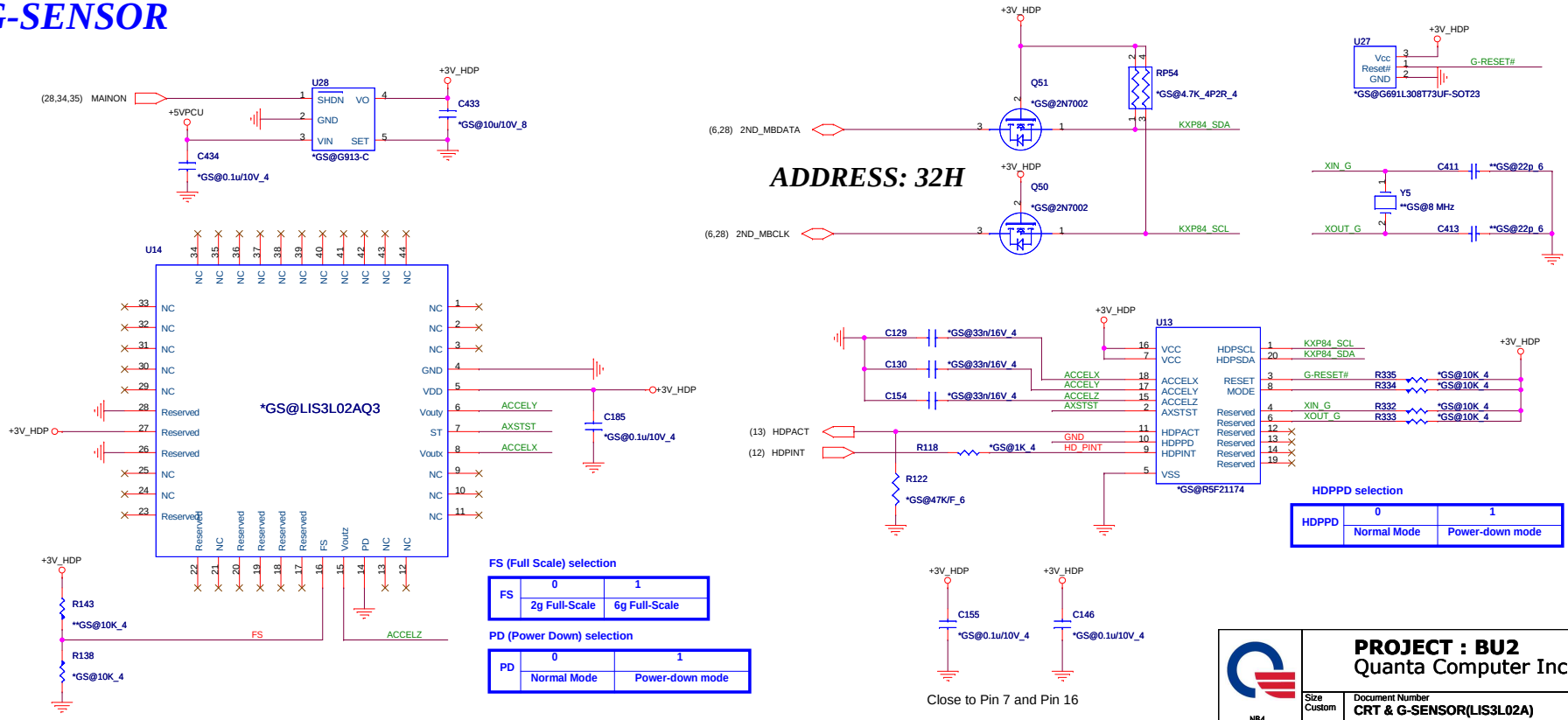
PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI/HDMI-CEC(R5F211A)	1A
NB4	Date: Thursday, July 24, 2008	Sheet 18 of 35

CRT



G-SENSOR



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

HDPPD	0	1
	Normal Mode	Power-down mode

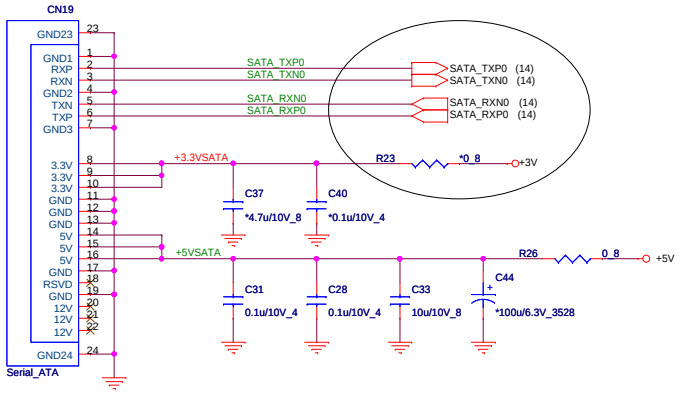
PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT & G-SENSOR(LIS3L02A)	1A

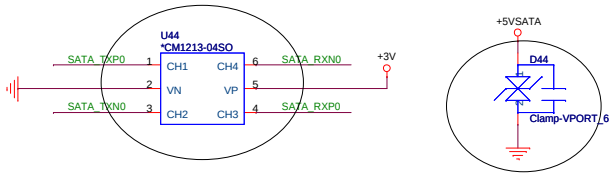
Date: Thursday, July 24, 2008 Sheet 19 of 35

NB4

SATA HDD



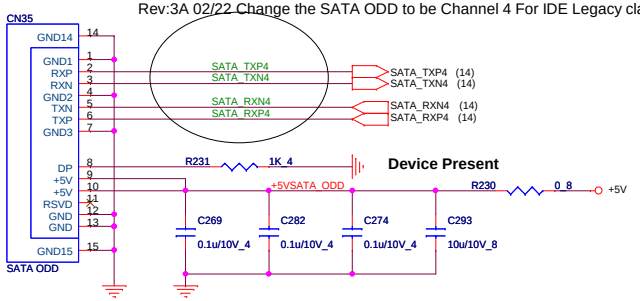
Rev:3B 04/18 Change HDD Control From Channel/2 to Channel/0 For Spin Down Issue.

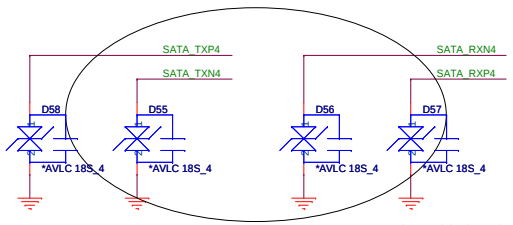


Rev:3B 04/18 Remove D51/D52/D53/D54 Varistor And Change to U44 CM1213-04SO ESD Protection Arrays.

SATA ODD

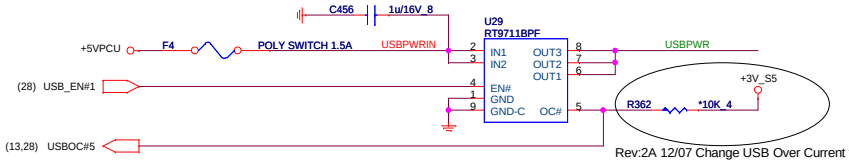
Rev:3A 02/22 Change the SATA ODD to be Channel 4 For IDE Legacy class Mode..





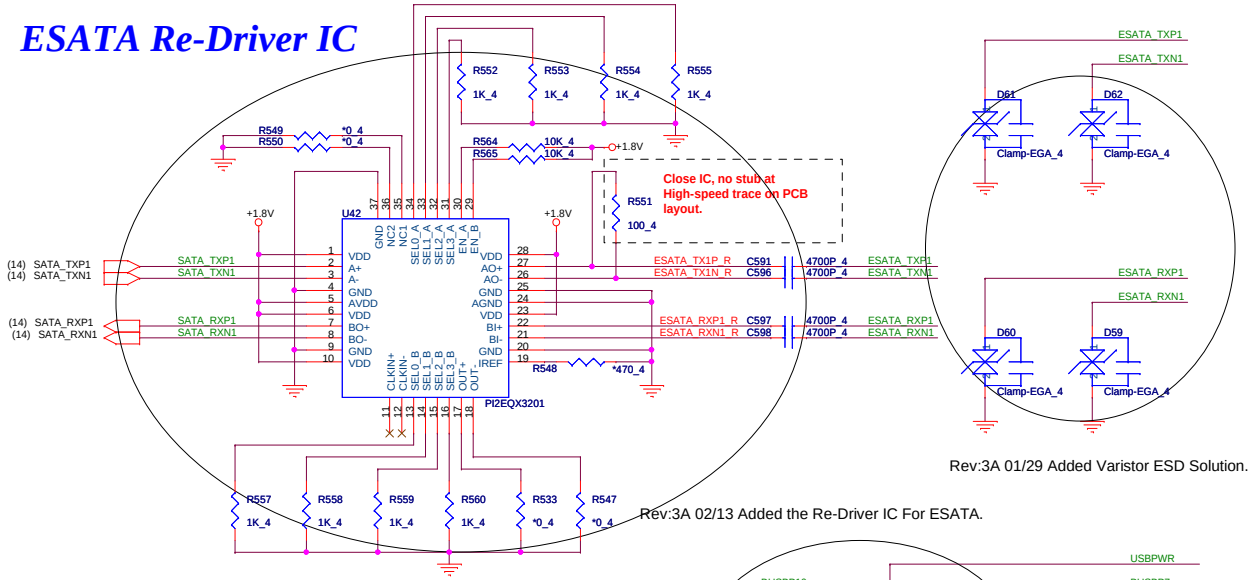
Rev:3A 01/29 Added Varistor ESD Solution.

USB & ESATA



Rev:2A 12/07 Change USB Over Current to +3V_S5 Domain.

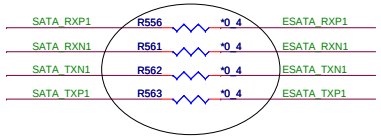
ESATA Re-Driver IC



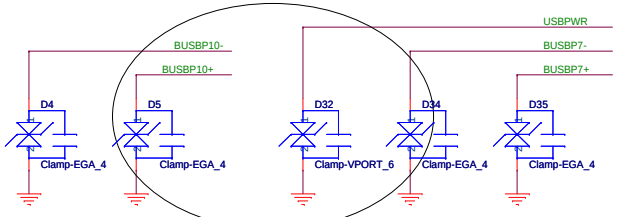
Rev:3A 01/29 Added Varistor ESD Solution.

Rev:3A 02/13 Added the Re-Driver IC For ESATA.

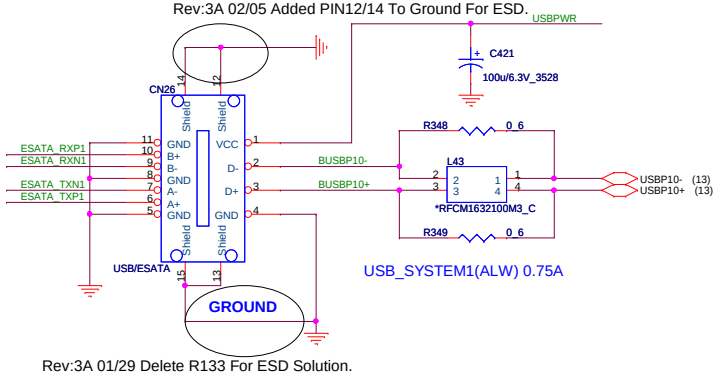
SEL0_X	SEL1_X	Eq	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				



Rev:3A 02/05 Added PIN12/14 To Ground For ESD.

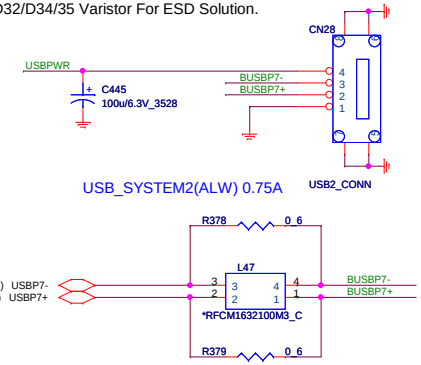


Rev:3A 03/03 Stuff the D4/D5/D32/D34/35 Varistor For ESD Solution.



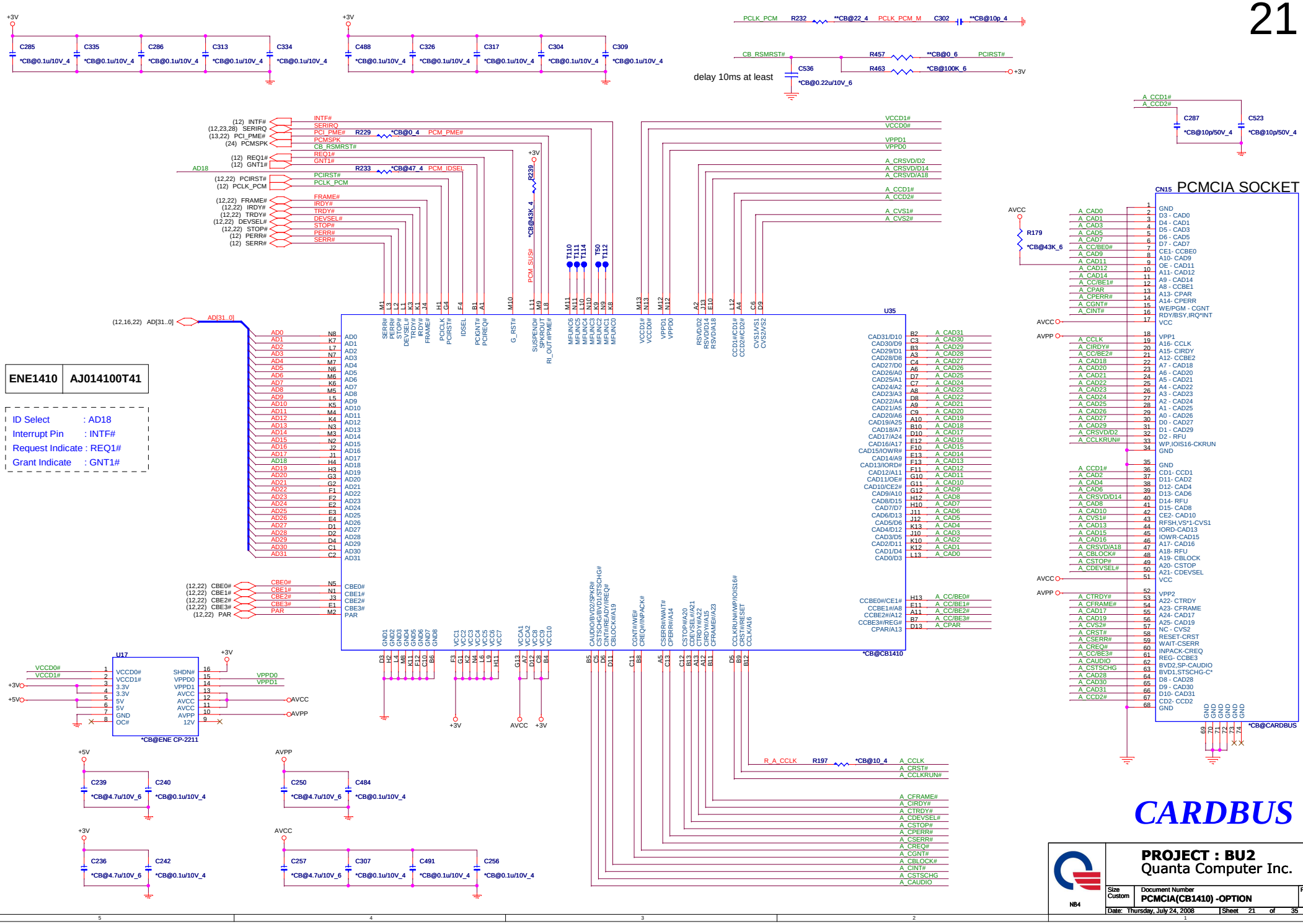
Rev:3A 01/29 Delete R133 For ESD Solution.

USB_SYSTEM1(ALW) 0.75A



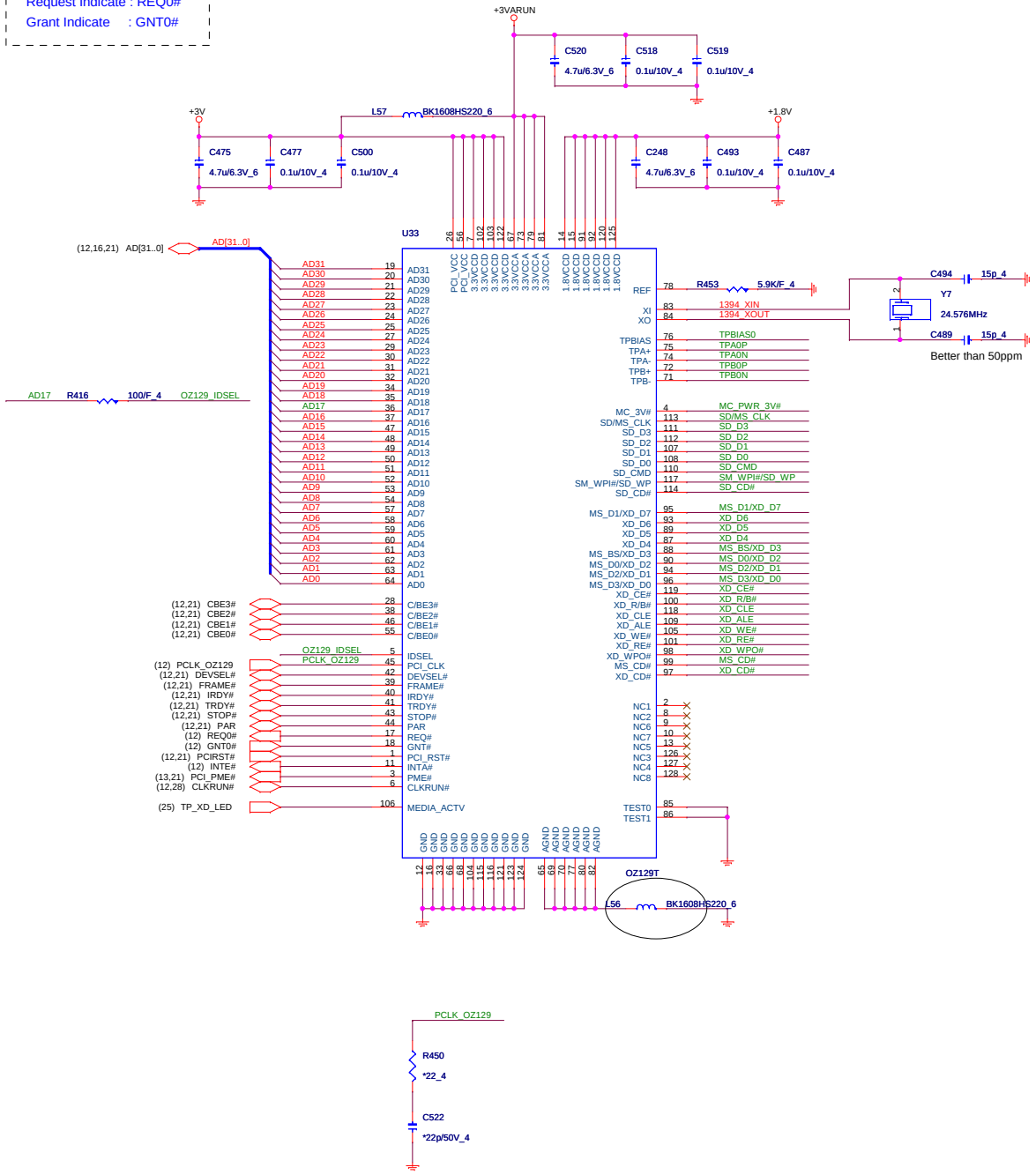
USB_SYSTEM2(ALW) 0.75A

NB4	PROJECT : BU2 Quanta Computer Inc.	
Size: Custom	Document Number: SATA HDD/ODD & ESATA/USB	Rev: 1A
Date: Tuesday, August 19, 2008	Sheet 20 of 35	

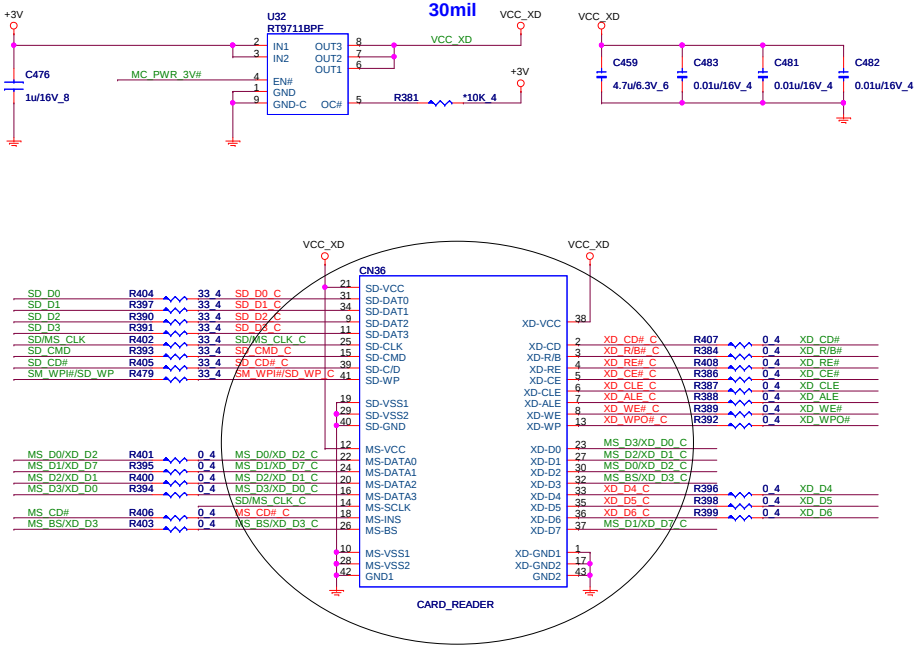

ENE1410 AJ014100T41
ID Select : AD18
Interrupt Pin : INTF#
Request Indicate : REQ1#
Grant Indicate : GNT1#
delay 10ms at least
U35
U17
*CB@ENE CP-2211
*CB@CB1410
CN15 PCMCIA SOCKET
*CB@CARDBUS
CARDBUS
PROJECT : BU2
Quanta Computer Inc.
PCMCIA(CB1410) -OPTION
Rev 1A
Date: Thursday, July 24, 2008
Sheet 21 of 35
NB4

OZ129 CardReader/1394

ID Select : AD17
Interrupt Pin : INTE#
Request Indicate : REQ0#
Grant Indicate : GNT0#

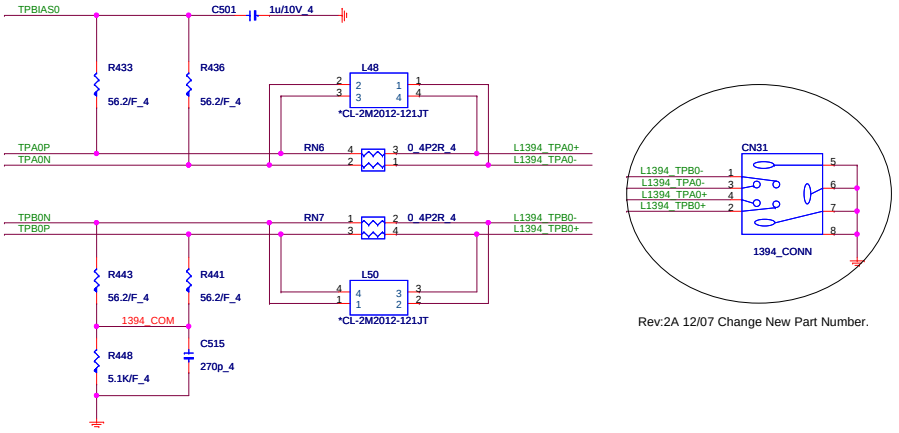


5 IN 1 Card Reader



Rev:2A 12/07 Modified the CN36 Footprint For Open Issue.

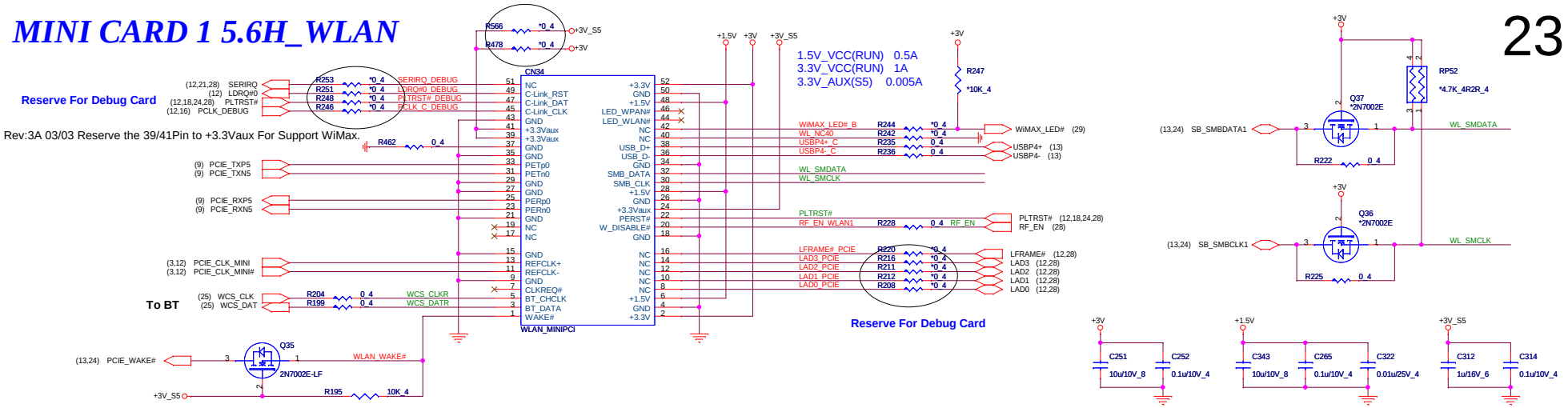
1394



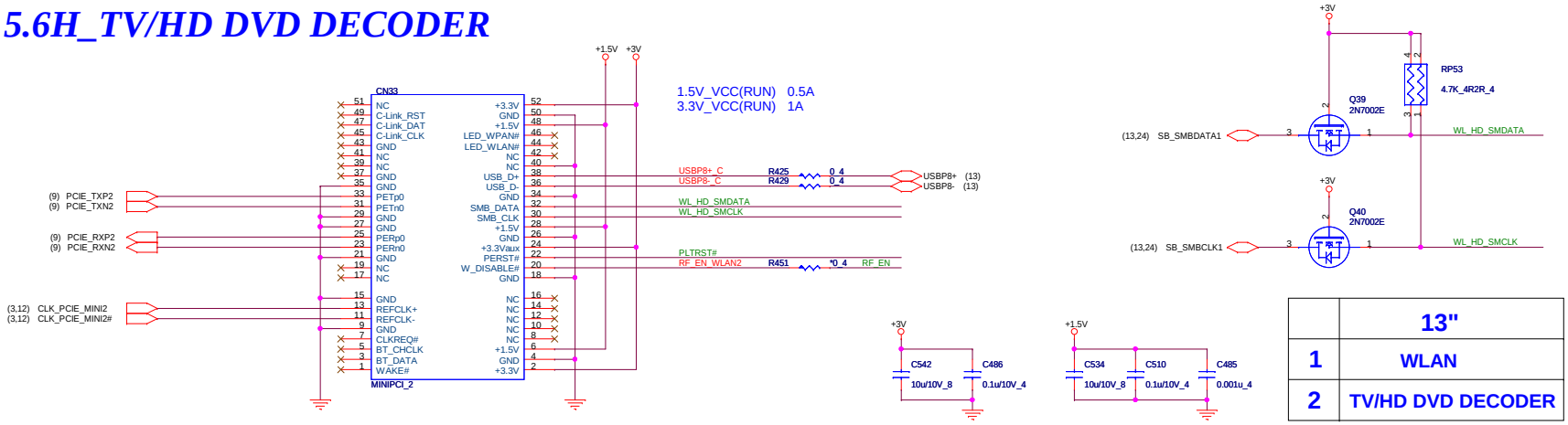
Rev:2A 12/07 Change New Part Number.

NB4	PROJECT : BU2 Quanta Computer Inc.	
Size: Custom	Document Number: OZ129T(5IN1/1394)	Rev: 1A
Date: Thursday, July 24, 2008	Sheet 22 of 35	

MINI CARD 1 5.6H_WLAN

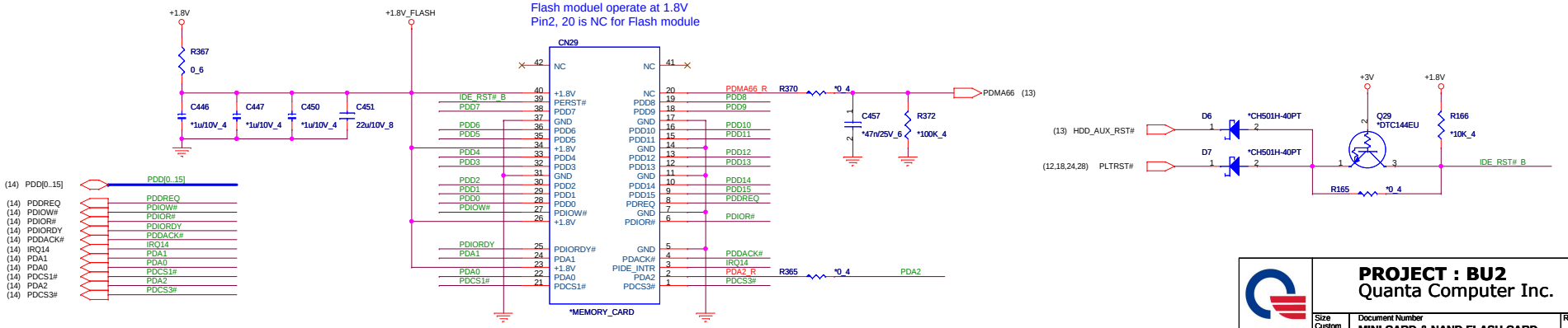


MINI Card 2 5.6H_TV/HD DVD DECODER



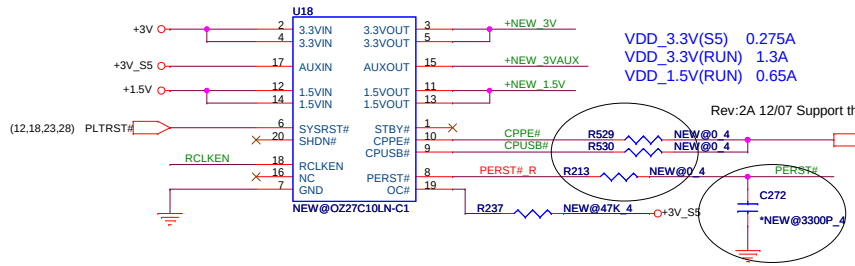
	13"
1	WLAN
2	TV/HD DVD DECODER

NAND FLASH MEMORY CARD



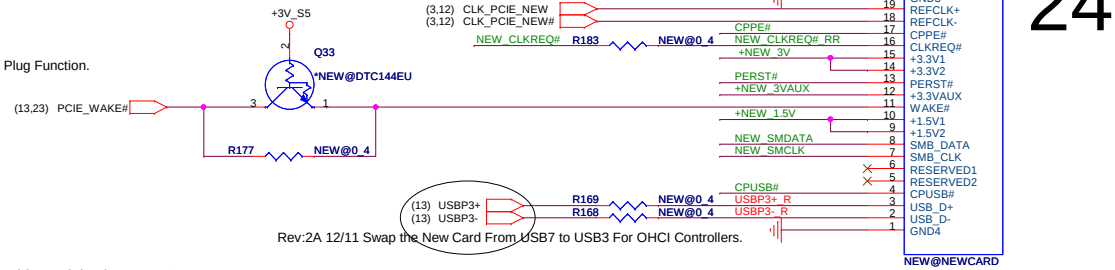
PROJECT : BU2	Quanta Computer Inc.
Size: Custom	Document Number: MINI CARD & NAND FLASH CARD
Rev: 1A	
Date: Thursday, July 24, 2008	Sheet 23 of 35
NB4	

NEW CARD(BTO)



VDD_3.3V(S5) 0.275A
VDD_3.3V(RUN) 1.3A
VDD_1.5V(RUN) 0.65A

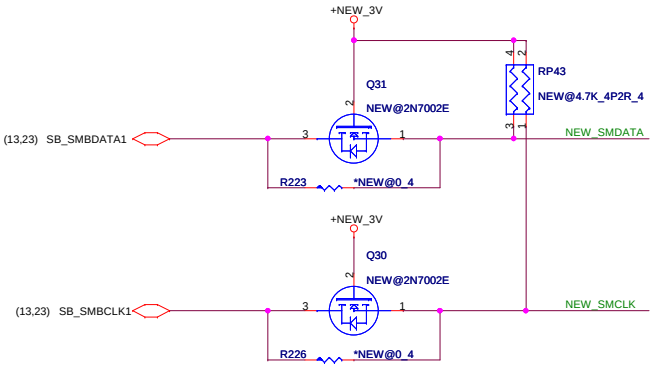
Rev:2A 12/07 Support the New Card's Hot Plug Function.

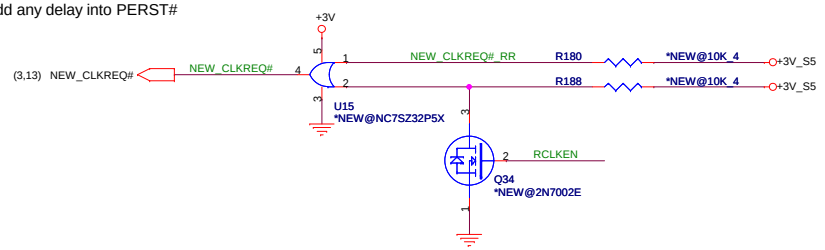


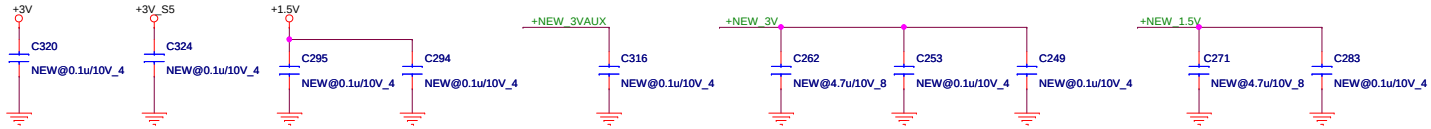
Rev:2A 12/11 Swap the New Card From USB7 to USB3 For OHCI Controllers.

NEW CARD'S POWER SWITCH

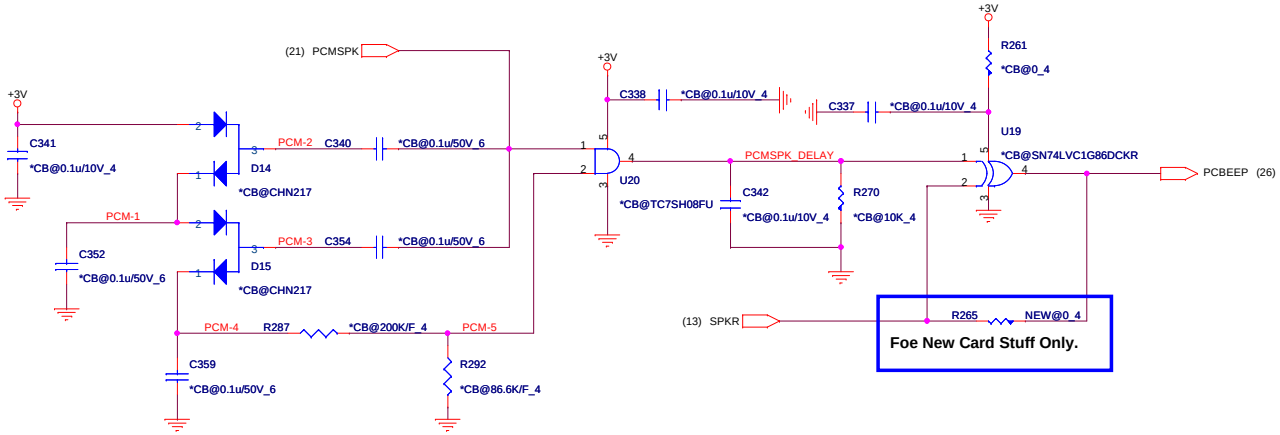
Rev:3A 03/03 As check with AE regarding to PERST# do not add any delay into PERST#





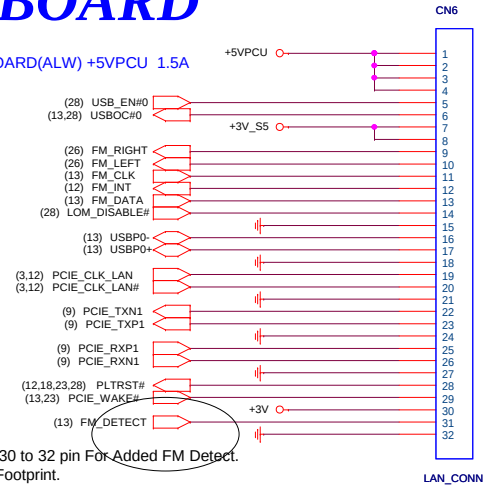


PC-BEEP



RJ45/USB BOARD

USB & LAN BOARD(ALW) +5VPCU 1.5A

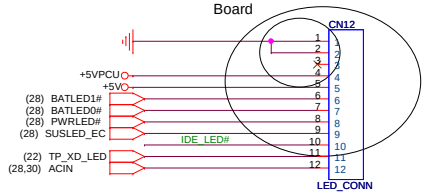


Rev:2A 12/07 Change Connector From 30 to 32 pin For Added FM Detect.
Rev:3A 02/05 Change Connector PCB Footprint.

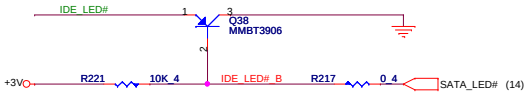
NB4	PROJECT : BU2 Quanta Computer Inc.	
Size: Custom	Document Number: NEW CARD & RJ45 BOARD/BEEP	Rev: 1A
Date: Thursday, July 24, 2008	Sheet 24 of 35	

LED BOARD

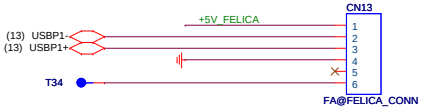
Rev:3A 02/05 NC PIN3 To Follow LED Board

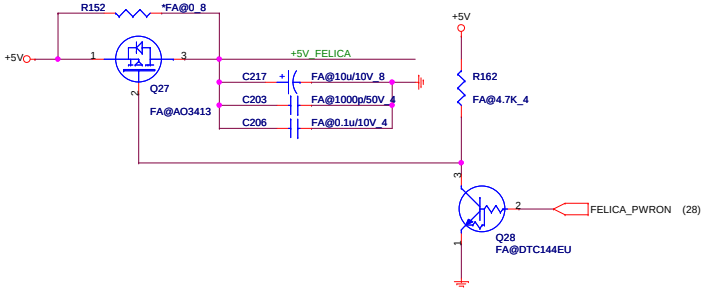


Rev:2A 12/07 Change CONN Footprint.



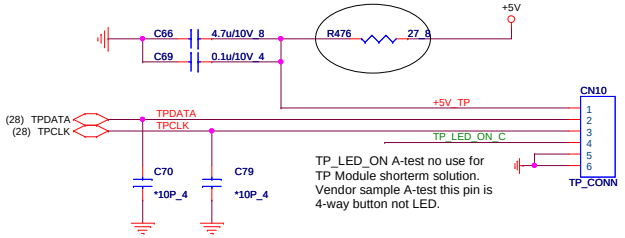
Felica





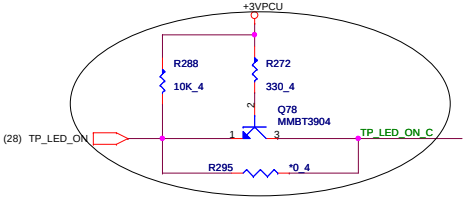
TP BOARD

Rev:3C 12/07 Change R476 Resistor PCB Footprint From 0605 to 0805.



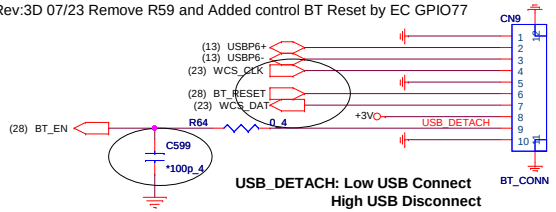
TP_LED_ON A-test no use for TP Module shorterm solution. Vendor sample A-test this pin is 4-way button not LED.

Rev:2A 12/07 Apply isolate TP_LED_ON From EC to Mainstream TP



Bluetooth Module

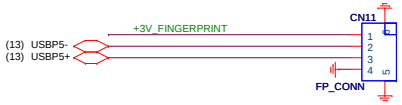
Rev:3D 07/23 Remove R59 and Added control BT Reset by EC GPIO77

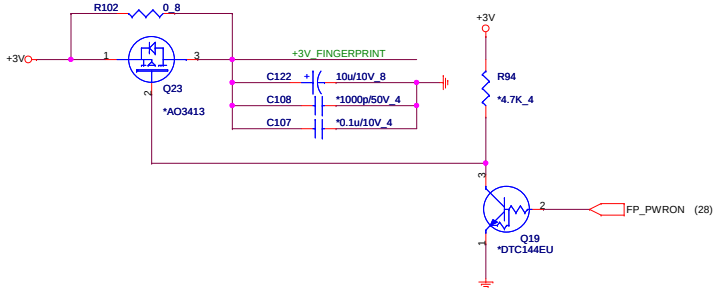


USB_DETACH: Low USB Connect
High USB Disconnect

Rev:3A 03/03 Reserve C599 Capacitors to Bluetooth Enable For EMI..

FINGER-PRINT

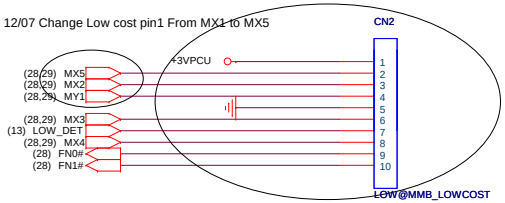




MMB

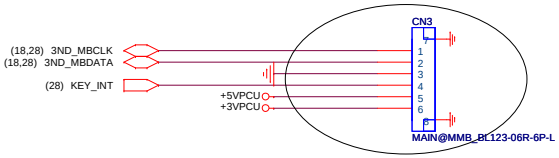
Rev:2A 12/07 Change Low cost pin1 From MX1 to MX5

Low cost

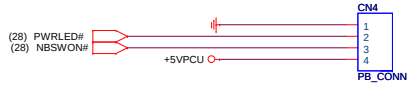


Rev:2A 12/07 Change CONN Footprint.

Main strem



POWER BOARD



NB4

PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TP/FP/BT/PB/FELICA/MMB CONN	1A
Date: Tuesday, August 19, 2008	Sheet 25 of 35	

CODEC(CX20561)

Rev:3A 02/05 Added the EMI Solution.

Rev:3B 04/12 Stuff R438/R447 0ohm For EMI Suggest.

Determining HDA use +1.5V/+3V

Rev:3B 04/18 Del the R476/R477 By EMI Suggest .

CX20561-12Z Not support digital MIC
CX20561-13Z support digital MIC

PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

INT SPEAKER

If Int Mic change to Port C, and Remove FM.Than NC R469

Rev:3A 02/05 Stuff C539/C544 For INT MIC Recording Noise.

Reserve INTMIC

Reserve FM

INT SPK AMP

Rev:3A 02/05 Page29 : Modify the Speaker Gain To 9.7dB.

H : AMP turn on
L : AMP power down

Rev:2A 12/07 NC D16 For there has "Bo-Bo" Sound while plug-in/out Headphone.

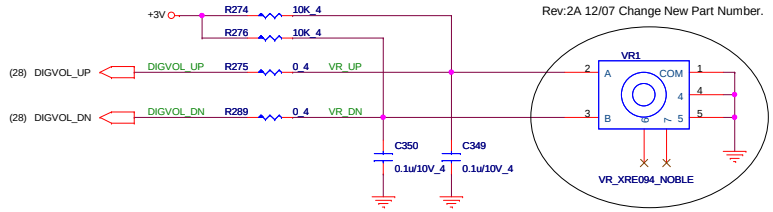
ESD Protect

PROJECT : BU2
Quanta Computer Inc.

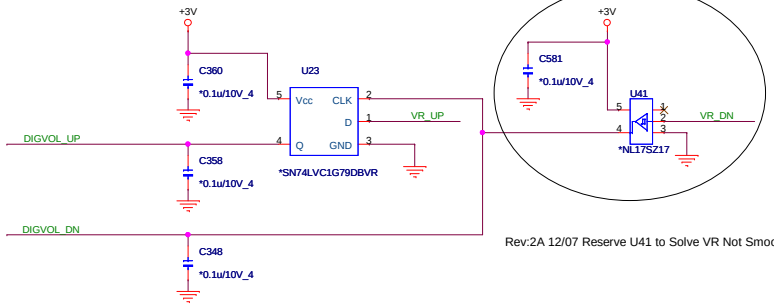
Size	Document Number	Rev
Custom	CONEXANT(CX205601)/SPK/AMP	1A

Date: Thursday, July 24, 2008 | Sheet 26 of 35

VR

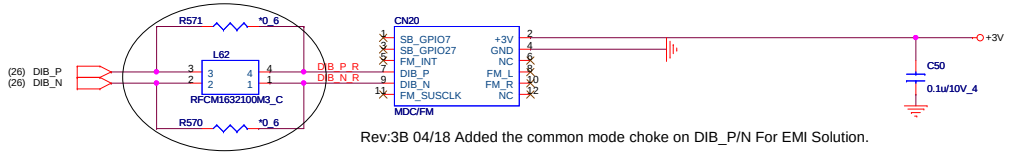


Rev:2A 12/07 Change New Part Number.



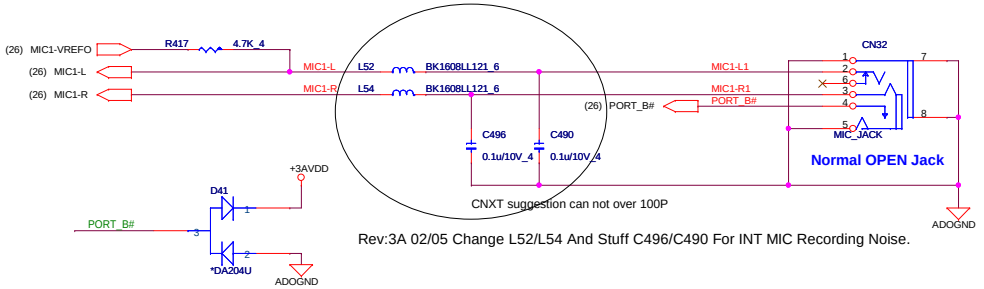
Rev:2A 12/07 Reserve U41 to Solve VR Not Smooth.

FM TUNER & MDC



Rev:3B 04/18 Added the common mode choke on DIB_P/N For EMI Solution.

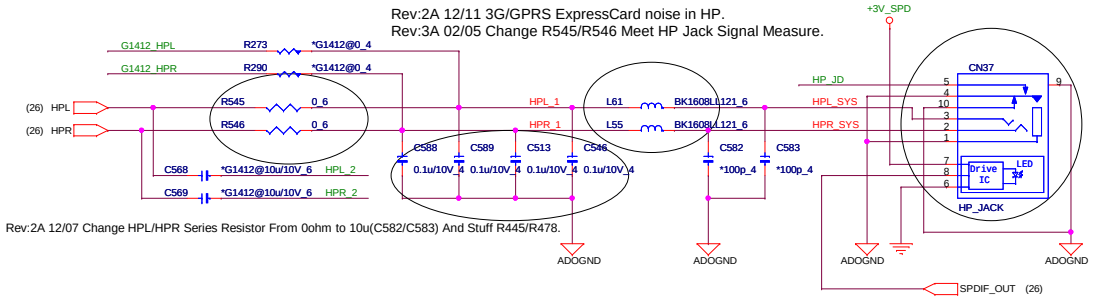
SYSTEM MIC



Rev:3A 02/05 Change L52/L54 And Stuff C496/C490 For INT MIC Recording Noise.

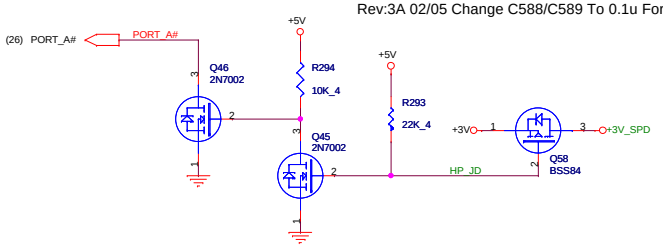
HP JACK

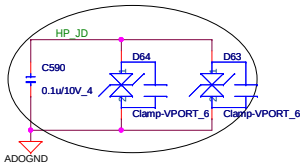
Rev:2A 12/11 3G/GPRS ExpressCard noise in HP.
Rev:3A 02/05 Change R545/R546 Meet HP Jack Signal Measure.



Rev:2A 12/07 Change HPL/HPR Series Resistor From 0ohm to 10u(C582/C583) And Stuff R445/R478.

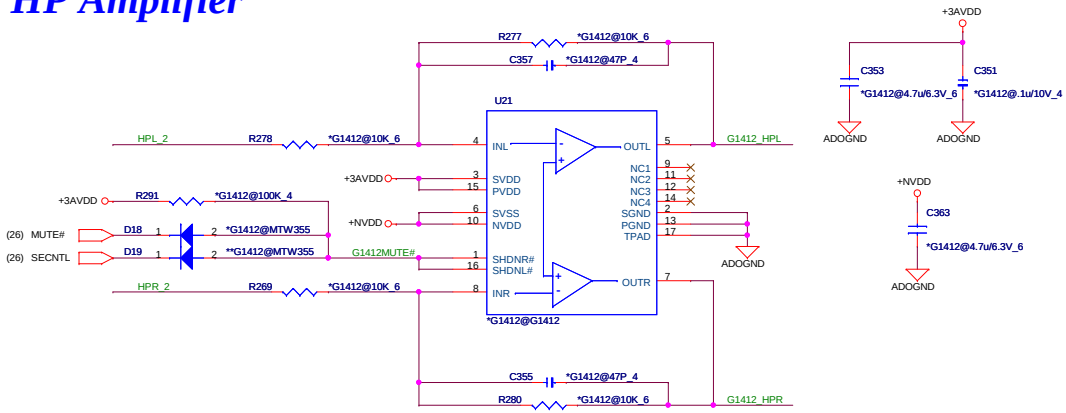
Rev:2A 12/13 CN37 9/10# Shield Pin to ADGND For ESD issue.
Rev:3A 02/05 Change C588/C589 To 0.1u For Enhance Avoid 3G Noise And Meet HP Jack Signal Measure

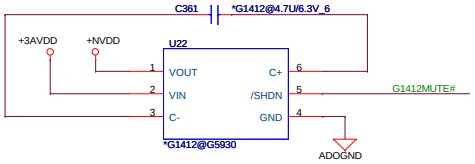




Rev:3A 02/05 Added the ESD Protect.

HP Amplifier





NB4
PROJECT : BU2
Quanta Computer Inc.
Size Custom
Document Number JACK/VR/FM/MIC/MDC/AMPLIFIER
Rev 1A
Date: Thursday, July 24, 2008
Sheet 27 of 35

EC(KBC)

Rev:3D 07/23 Add D68 to Avoid +3V Voltage Leakage.

Rev:2A 12/07 Add D57,D58 to Avoid Voltage Leakage.

Rev:3A 02/13 Reserve the DISPON Pin By EC Control.

Rev:3D 07/23 Bluetooth can't work issue.

Rev:2A 12/07 Add D57,D58 to Avoid Voltage Leakage.

Rev:2A 12/13 Add D49,D50 to Avoid Voltage Leakage.

Rev:3A 02/05 System will Leakage when system into G3 mode.

Rev:2A 12/07 Apply R528/R531/R532 Pull-up For Battery LED issue.

Rev:3A 02/08 Reserve the CPU PWRGOOD Diode For Sequence Timing.

Rev:2A 12/07 Short Pad to Replaced Power S/W.

SMBUS Table

SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	HDMI CEC Touch Sensor

SM BUS PU

I/O Base Address

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

Rev:2A 12/07 Stuff R38 And NC R36 For Boardcom BT issue.

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID

ADDRESS: A0H

SPI FLASH

2nd sorce

MXIC	MX25L8005M2C-15G	AKE5GFK0Z09
Winbond	W25X80VSSIG	AKE3GFP0N08
EON	EN25F80-75HCP	AKE3GZP0Q00

INTERNAL KEYBOARD STRIP SET

CIR

WPC8763LDG: AL008763B00 (w/o CIR)
WPC8769LDG: AJ087690F08 (w/CIR)

WPCE775L: AJ007750F00 (w/o CIR)
WPCE775C: AJ007750F01 (w/CIR)

For WPC8763

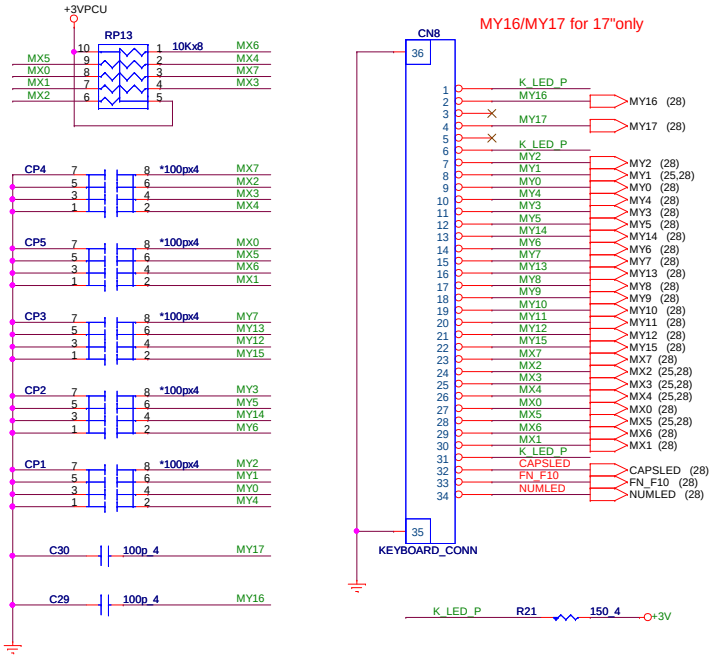
For WPCE775

PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC(KBC)-WPCPC8763/WPC8769	1A

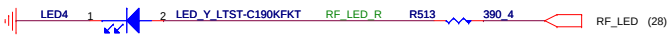
Date: Friday, August 01, 2008 Sheet 28 of 35

INT KEYBOARD

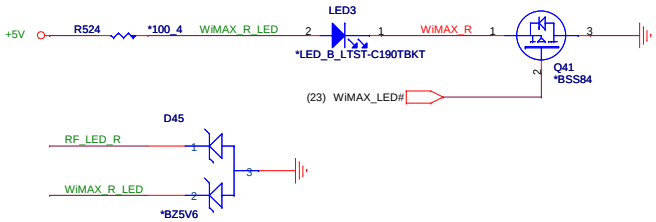


W-LAN&BT LED

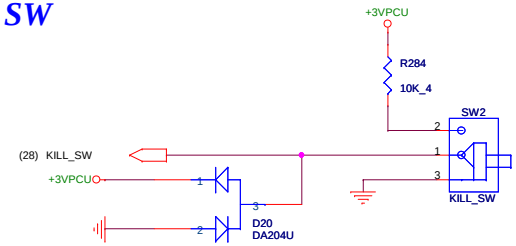
Mainstream --> Orange
Low Cost --> Orange



WiMAX LED

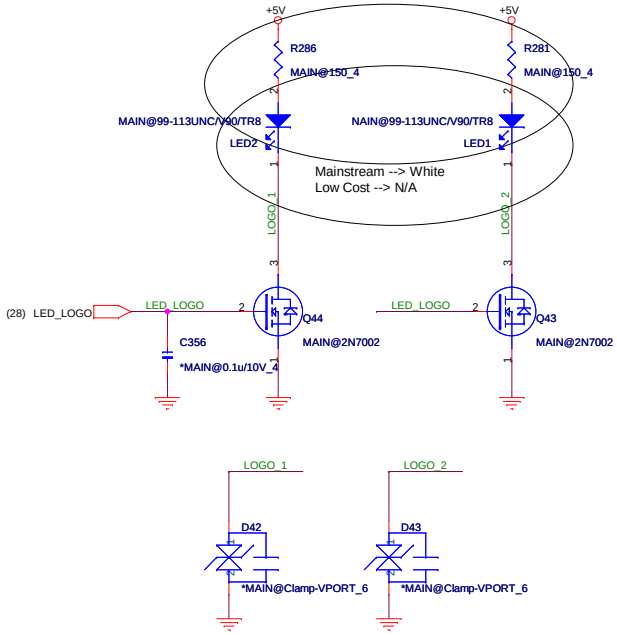


KILL SW



Satellite LED

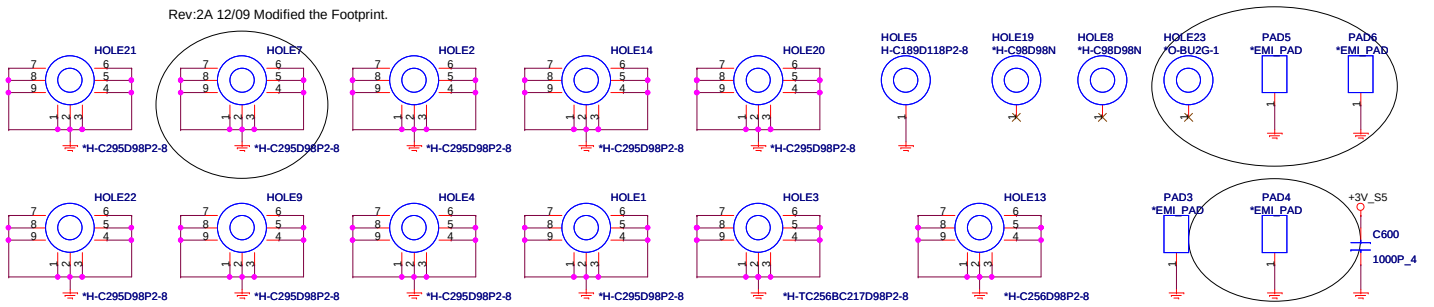
Rev:2A 12/07 Updated the LED1/LED2 Footprint And Part Number.
Rev:3A 02/05 Change R281/R286 and R375 To 150ohm For LED Light Not Enough



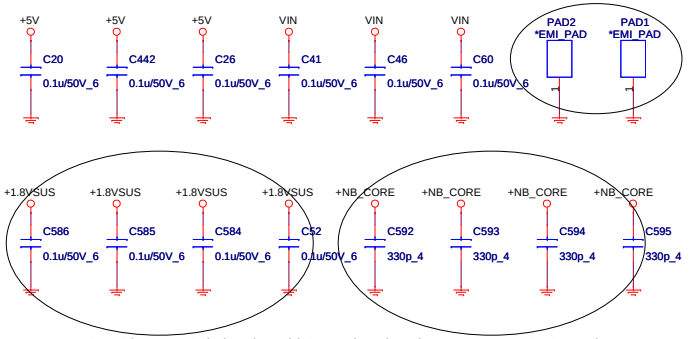
HOLE

Rev:2A 12/09 Modified the Footprint.

Rev:3B 04/18 ESD Solution the Added the Ground Pad.

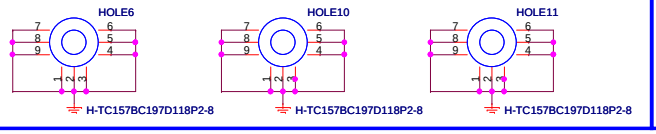


EMI

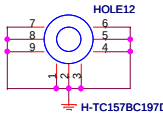


Rev:2A 12/11 EMI Solution the add Ground Pad And 0.1u Cap on 1.8VSUS Plane.
Rev:3A 02/05 EMI Solution the add 0.1u Cap on +NB_CORE Plane.

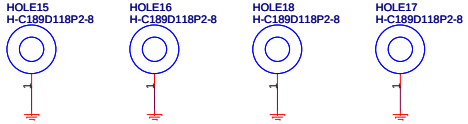
CPU



NB



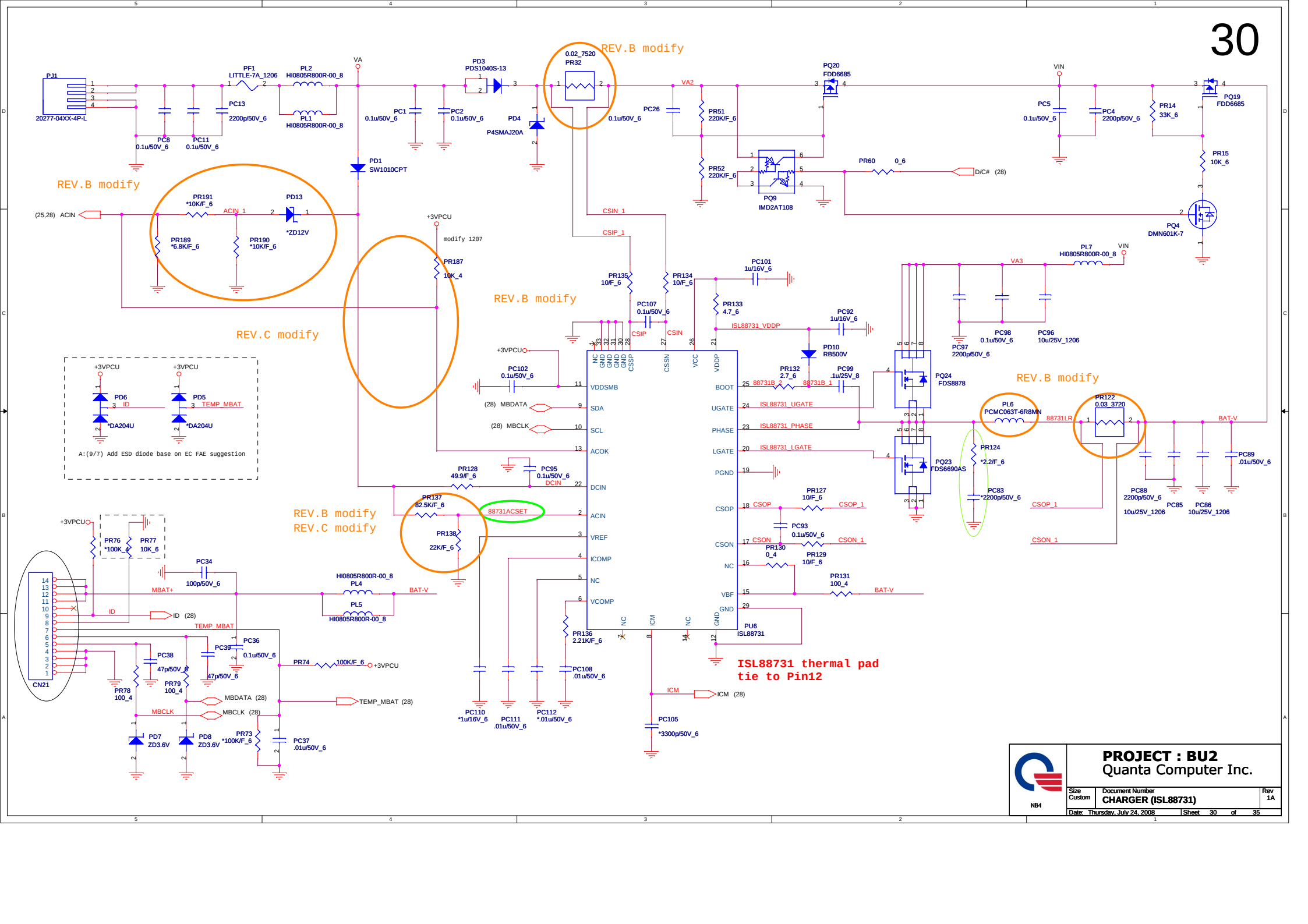
MINI CARD



PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KEYBOARD/LED/KILL SW/HOLE	1A
Date: Thursday, July 24, 2008	Sheet 29 of 35	

NB4



NB4	**PROJECT : BU2** Quanta Computer Inc.		
	Size: Custom	Document Number: **CHARGER (ISL88731)**	Rev: 1A
	Date: Thursday, July 24, 2008	Sheet 30 of 35	

Rev:2A 12/12 Move the Short Pad.

Rev:2A 12/12 Move the Short Pad.

MAIND (34,35)

SUSD (35)

(6) SYS_SHDN#

PR182 0_4

VIN

PC133 100u/25V_6X7.7

PC129 0.1u/50V_6

PC131 2.2n/50V_6

PC134 *10u/25V_1206

PC136 10u/25V_1206

09/07 Change PC123 placement

VL

PR183 39K/F_4

3V5V_EN

PR172 115K/F_4

PR173 390K_4

PC150 0.1u/50V_6

PC154 4.7u/10V_8

PR167 0_4

PC144 1u/10V_6

PR161 0_4

PC147 *0.01u/16V_4

PC142 0.1u/50V_6

REF

PR159 *0_6

09/07 Add PR154.

PC128 0.1u/50V_6

PC130 2.2n/50V_4

PC132 10u/25V_1206

OCP: 10A

+5VPCU

PL13 2.2uH

PR176 *0_4

PR181 0_4

PC158

PC149

PC160

10u/25V_1206

330u/6.3V_6X5.7

0.1u/50V_6

PQ37 FDS8878

5V_DH

5V_LX

5V_DL

PR179 2.2F_6

PC151 2.2n/50V_6

PQ36 FDS6690AS

PC153 0.1u/50V_6

PR166 237K/F_6

DDPWRGD_R

3V5V_EN

PU11 ISL6237

DOREFIN VIN NC ONLDO VCC TON REF

BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD

REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2

BST1 DL1 PVCC NC GND PGND DL2 BST2

PR180 1/F_6

PR163 1/F_6

PC141 0.1u/50V_6

9/12 PR44 Change to 196K.

PR160 196K/F_6

REFIN2

SKIP

DDPWRGD_R

3V5V_EN

3V_DH

3V_LX

3V_DL

PQ33 FDS8878

PQ35 FDS6690AS

PL12 2.2uH

PR104 2.2/F_6

PC65 2.2n/50V_6

PR155 0_6

PR156 *0_6

PC159 0.1u/50V_6

PC157 330u/6.3V_6X5.7

+3VPCU

OCP : 8A

8/27 Add SYS_HWPG.

PC148 0.1u/50V_6

PR192 *0_6

0_6

PR193

3V_DL

PC146 0.1u/50V_6

PD12 1PS302

PD11 1PS302

PC155 0.1u/50V_6

REV.B modify

PR170 0_6

PC145 1u/16V_6

SKIP

PR154 *0_6

REF

PR153 0_6

OCP:10A

L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A

Iocp=10-(4.18/2)=7.91A
Vth=7.91A*15mOhm=131mV
R(Ilim)=(105mV*10)/5uA
~237K

OCP:8A

L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A

Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=100.05mV
R(Ilim)=(100.05mV*10)/5uA
~200.1K

PR178 10K_6

PR177 0_6

SYS_HWPG (28)

9/13 Stuff the PR178.

+15V

PR162 22_8

+15V_ALWP

PC156 0.1u/50V_6

PR171 *200K_4

PR169 *39K/F_4

PR168 *0_6

REFIN2

08/29 Del PQ15.

9/07 Add PR155.

VIN

+3V_S5

+1.2V_S5

+15V

PR8 1M_6

PR185 22_8

PR107 22_8

PR1 1M_6

S5D

(28,35) S5_ON

PQ3 DTC144EU

PR7 1M_6

PQ43 DMN601K-7

PQ17 DMN601K-7

PQ1 DMN601K-7

09/12 Addition

+5VPCU

MAIND

PQ41 FDS8884

+5V

+3VPCU

MAIND

PQ40 FDS8878

+3V

+3VPCU

S5D

PQ39 FDC653N_NL

+3V_S5

+3VPCU

SUSD

PQ38 FDC653N_NL

+3VSUS

NB4

PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM 5V/3V (ISL6237)	1A

Date: Thursday, July 24, 2008 | Sheet 31 of 35

OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

3A

20A

20A

Rev:2A 12/12 Move the Short Pad.

Pin 49 is GND Pin

Close to CPU socket

Parallel

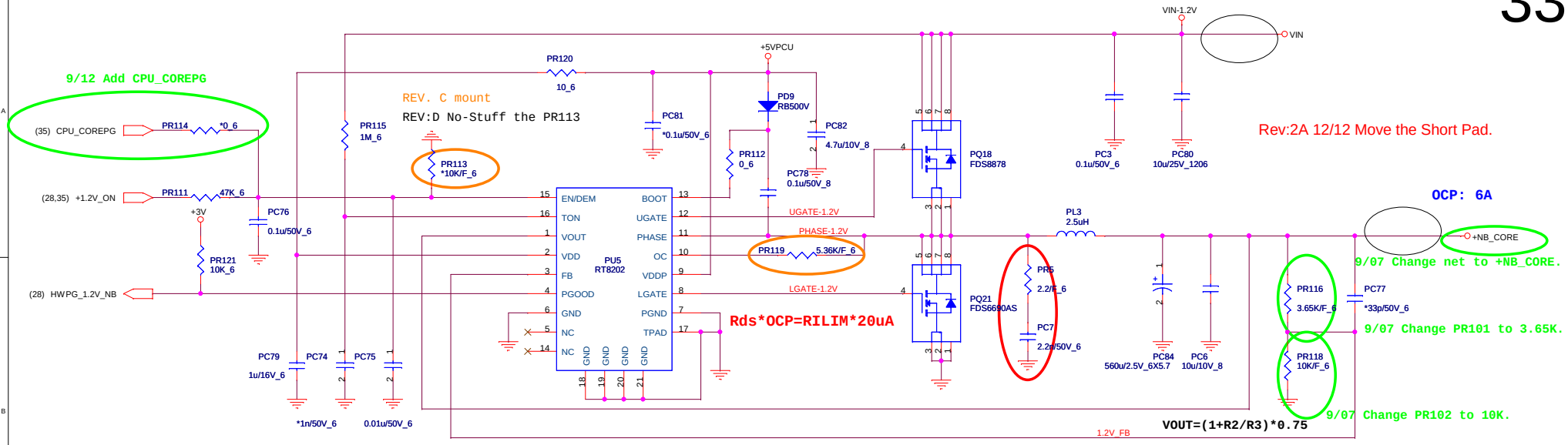
Close to CPU socket

PU1 ISL6265

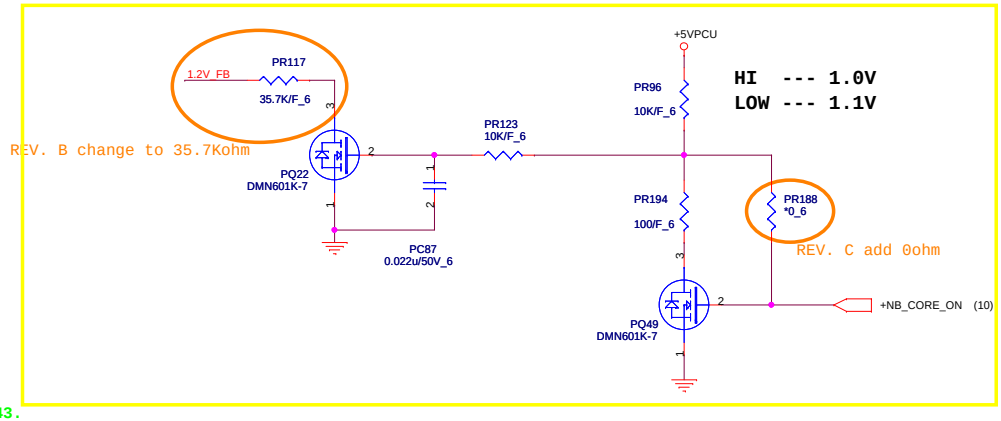
PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
C	AMD GRIFFIN CPU (ISL6265)	1A

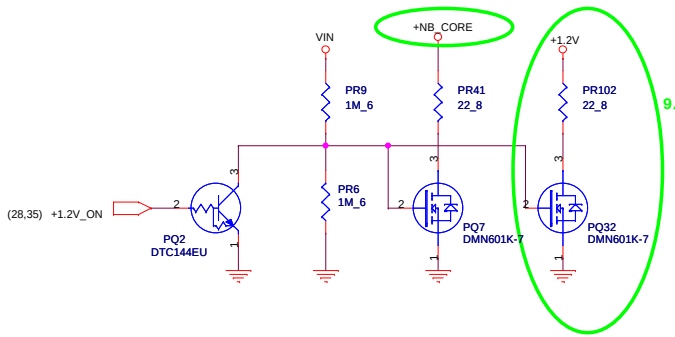
Date: Thursday, July 24, 2008 Sheet 32 of 35



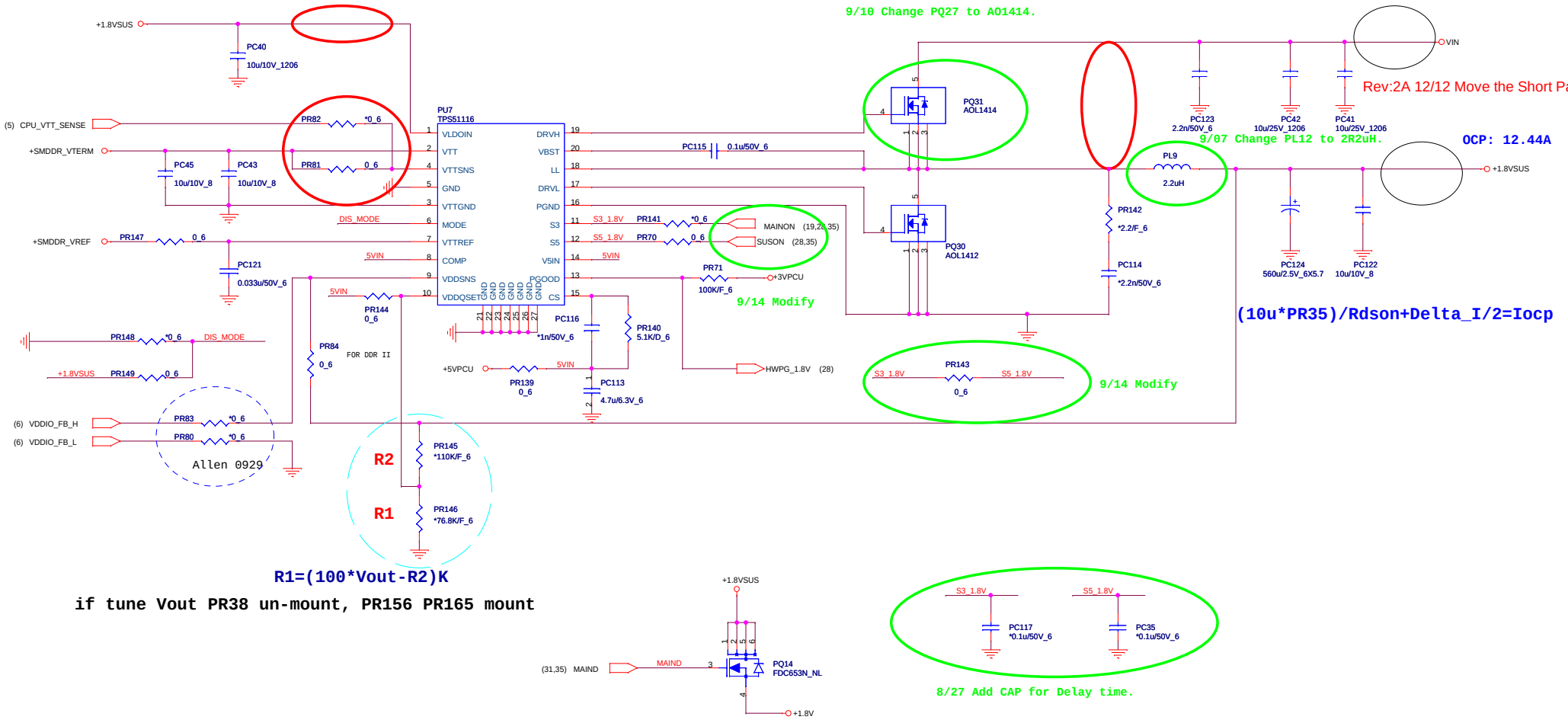
1/30 modify



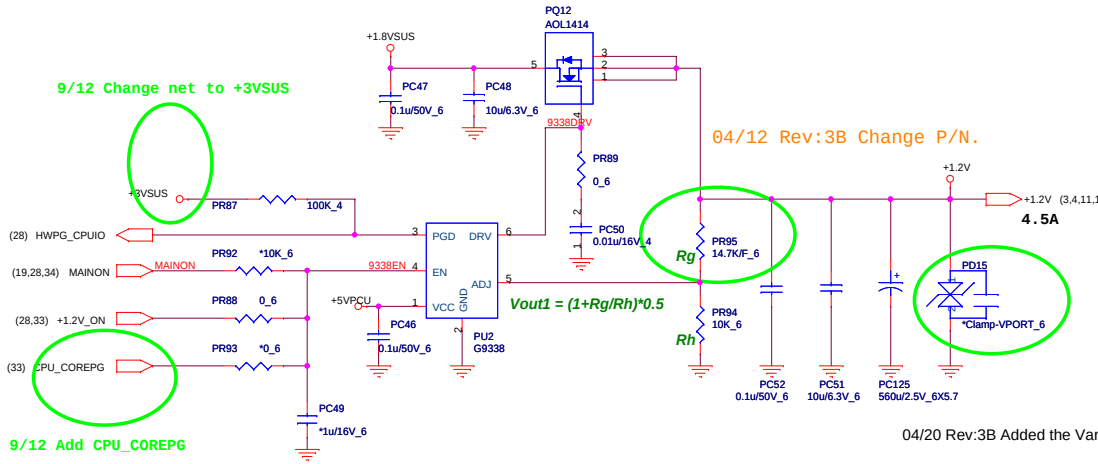
9/07 Change net to +NB_CORE.



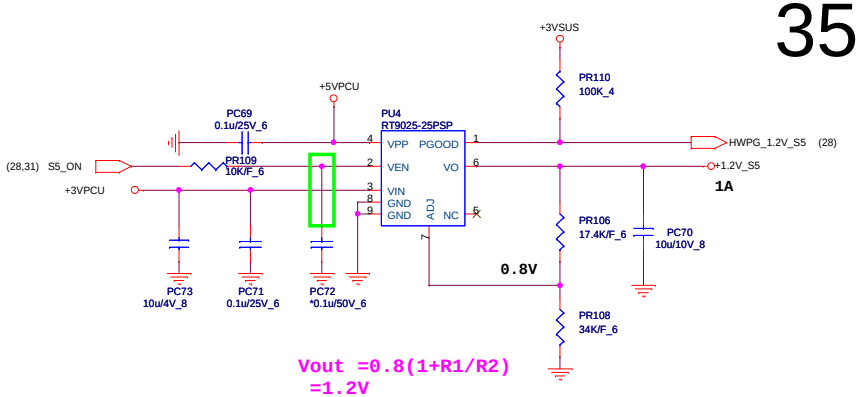
NB4	PROJECT : BU2 Quanta Computer Inc.	
Size: Custom	Document Number: +NB_CORE (RT8202)	Rev: 1A
Date: Thursday, July 24, 2008	Sheet 33 of 35	

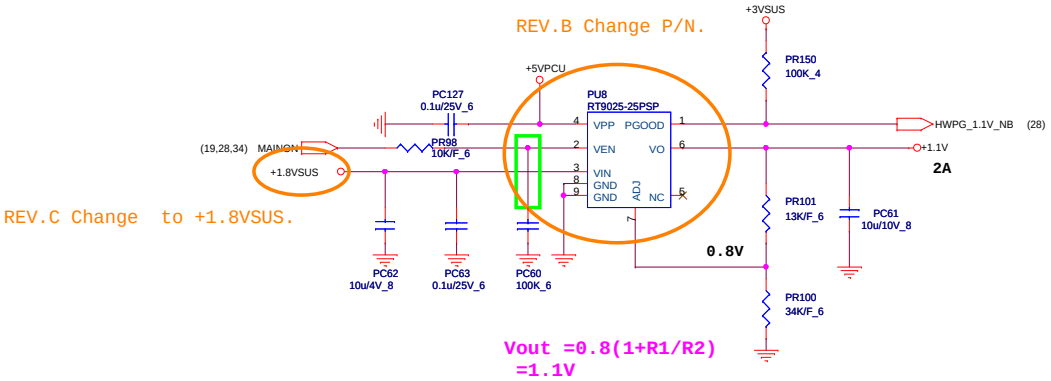


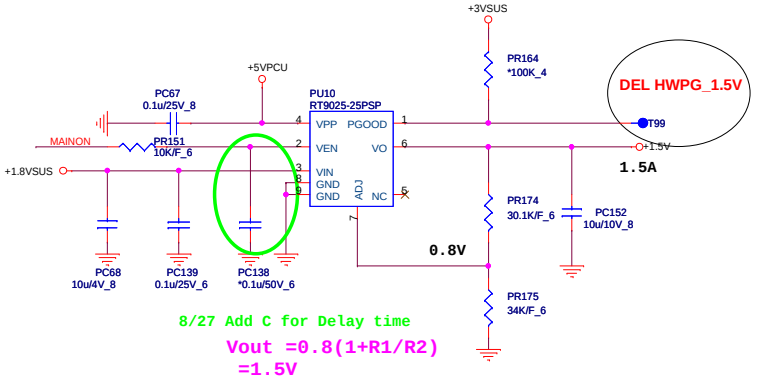
NB4	**PROJECT : BU2** Quanta Computer Inc.	
Size: Custom	Document Number: DDR 1.8V(TPS51116)	Rev: 1A
Date: Thursday, July 24, 2008	Sheet 34 of 35	

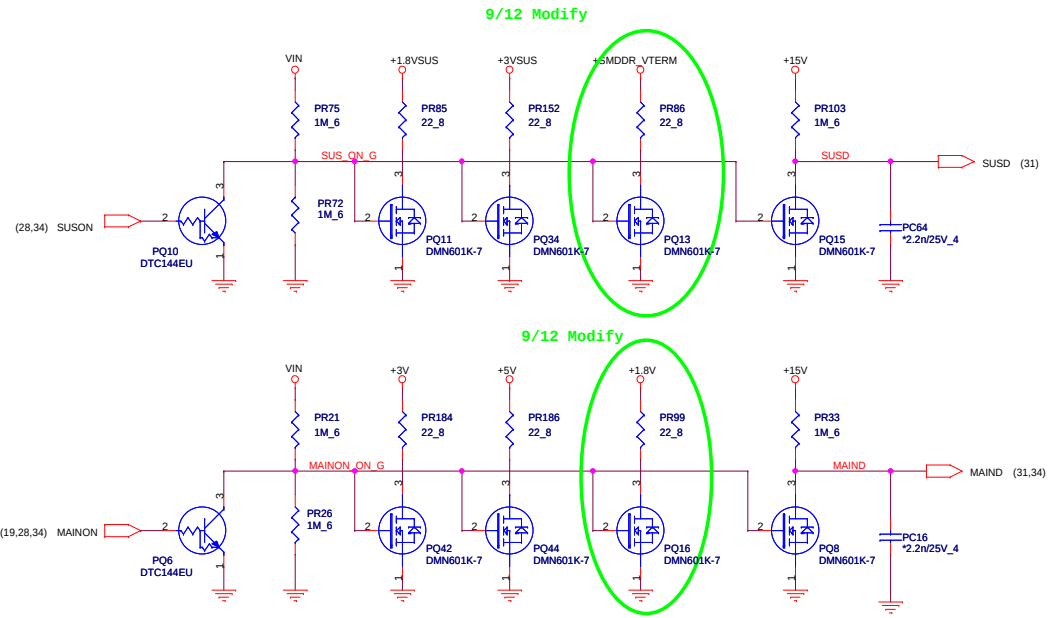


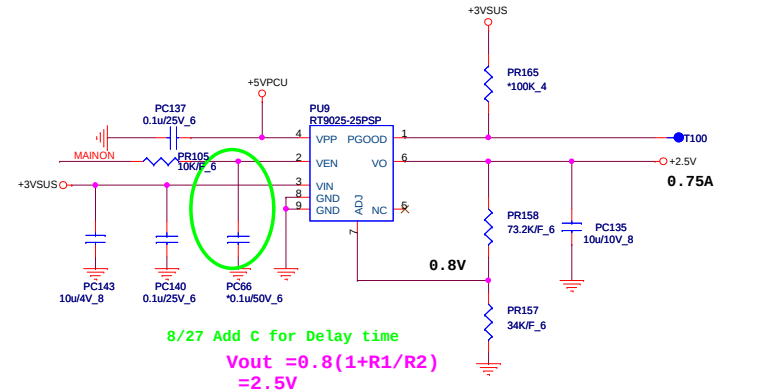
04/20 Rev:3B Added the Varistor in +1.2V Domain.











NB4

PROJECT : BU2
Quanta Computer Inc.

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Custom	DISCHARGE (1.25V/1.5V/1.2V)	1A
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