Husk/Petra
UMA/Muxless Schematics Document
Ivy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

DIS IVB Touch

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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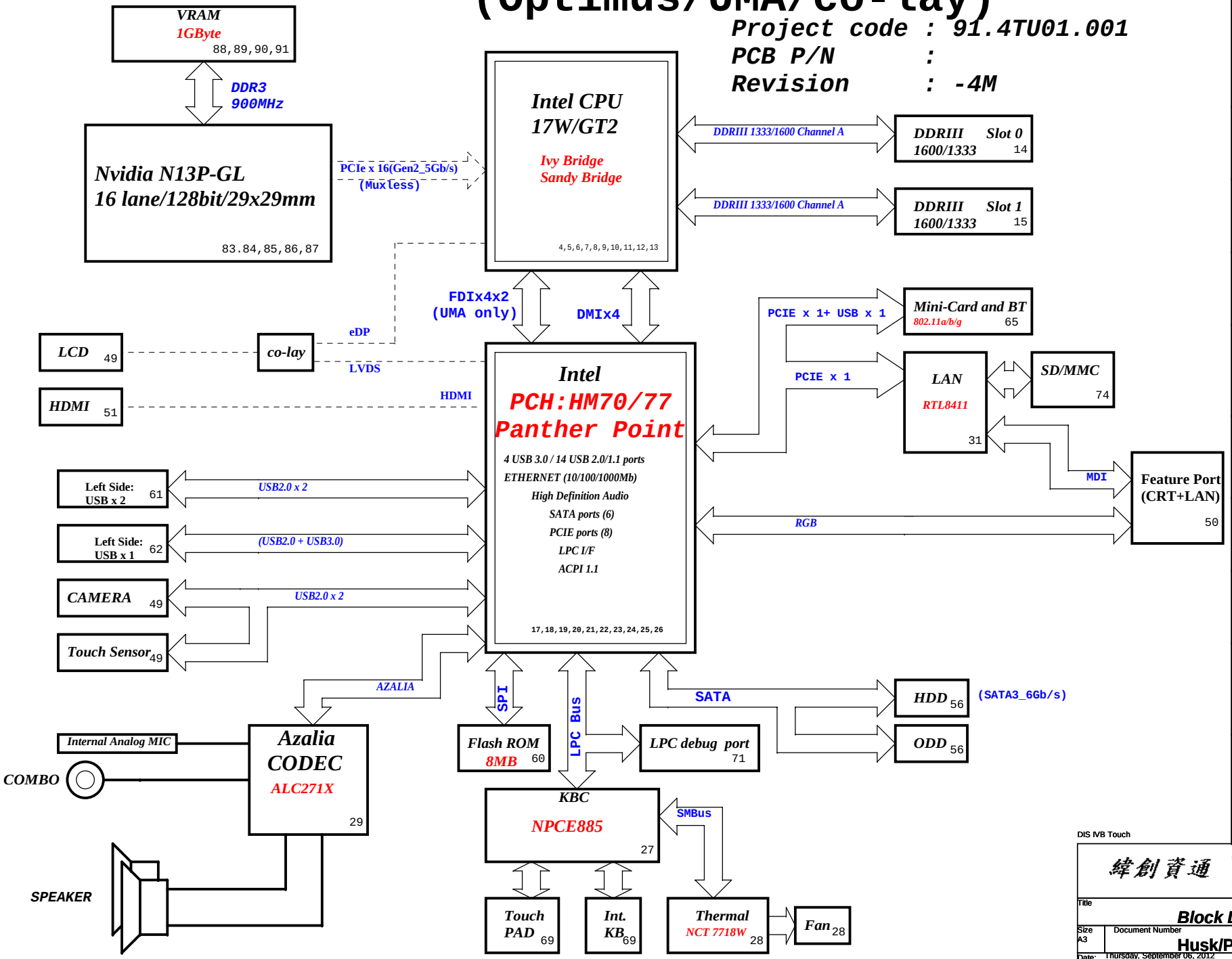
Title		
	Cover Page	
Size A3	Document Number Husk/Petra	Rev -4M
Date: Thursday, September 06, 2012	Sheet 1 of 103	

Husk and Petra Block Diagram (Optimus/UMA/co-lay)

Project code : 91.4TU01.001
PCB P/N :
Revision : -4M



CHARGER BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8223MGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

CPU DC/DC ISL95836HRTZ 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC ISL95836HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC TPS51218DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

LDO RT9025-25ZSP 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

LDO G978 48	
INPUTS	OUTPUTS
1D05_VTT	0D85V_S0

VGA ISL62882CHRTZ 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches 93	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1D05V_VGA_S0
1D5V_S3	1D5V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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Title: Block Diagram

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 2 of 103

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

DIS IVB Touch

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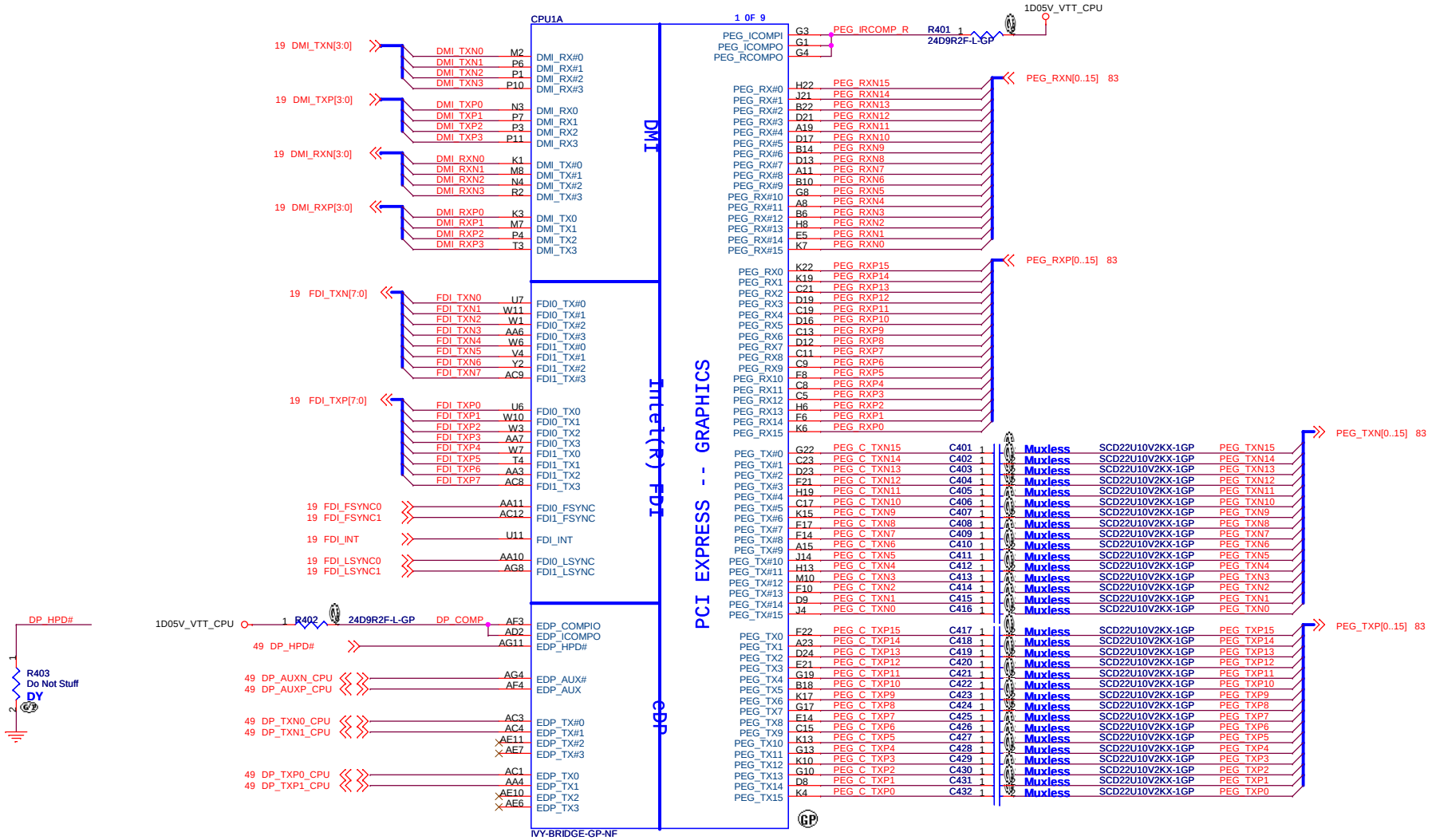
Title: *Table of Content*

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 3 of 103

SSID = CPU



71.00IVY.A0U

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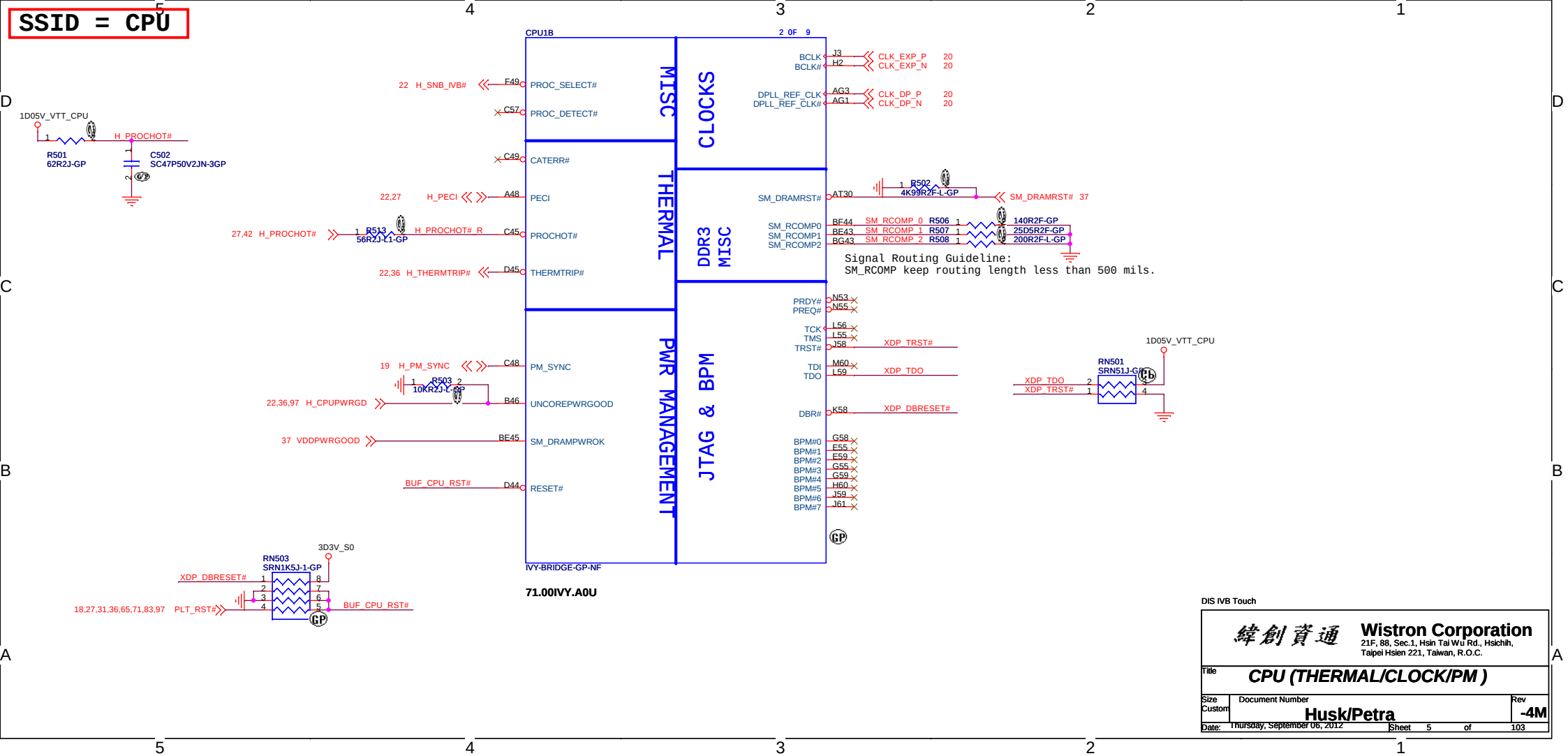
Title	***CPU (PCIE/DMI/FDI)***
Size A3	Document Number **Husk/Petra** Rev **-4M**
Date: Thursday, September 06, 2012	Sheet 4 of 103

SSID = CPU



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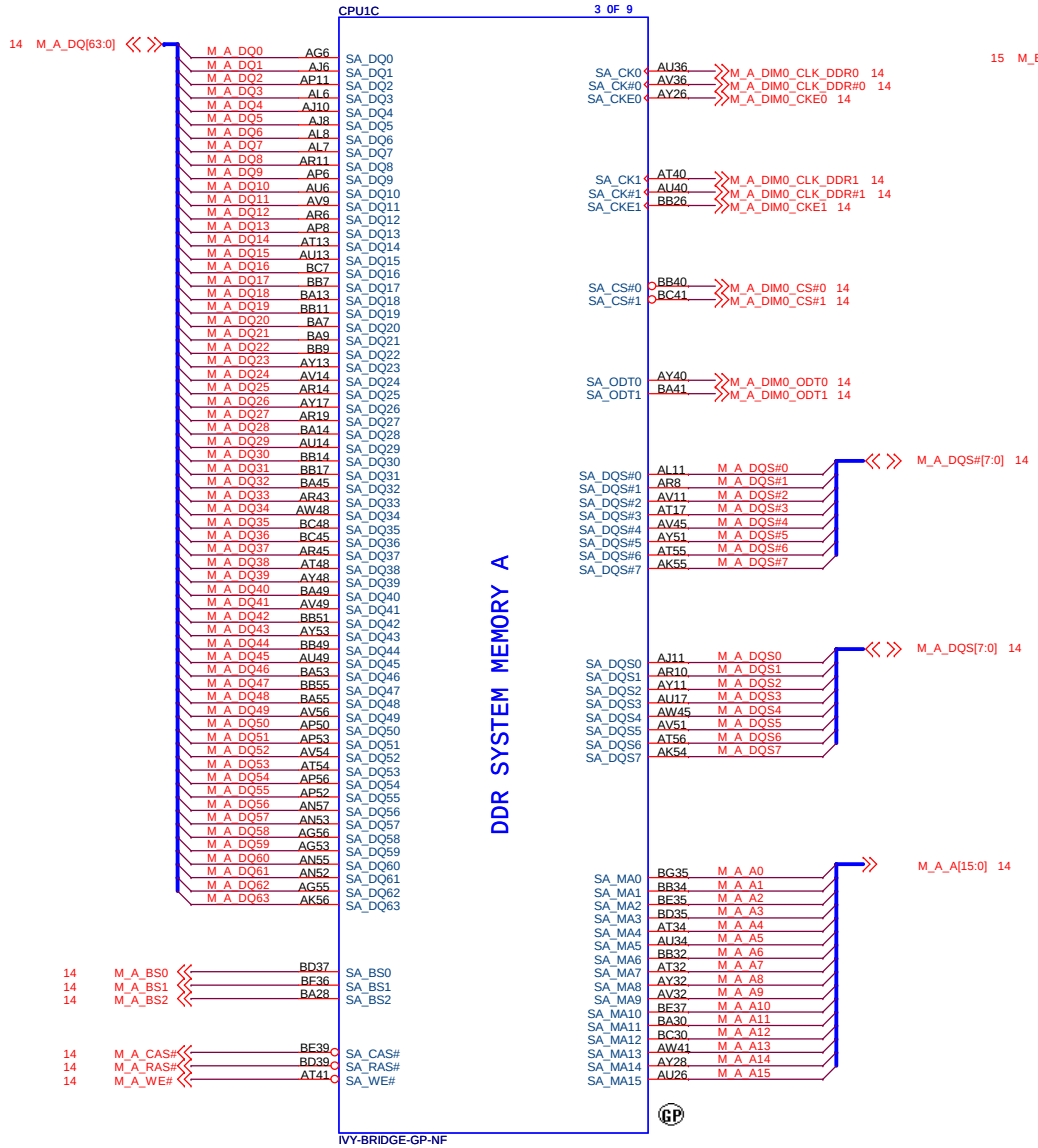
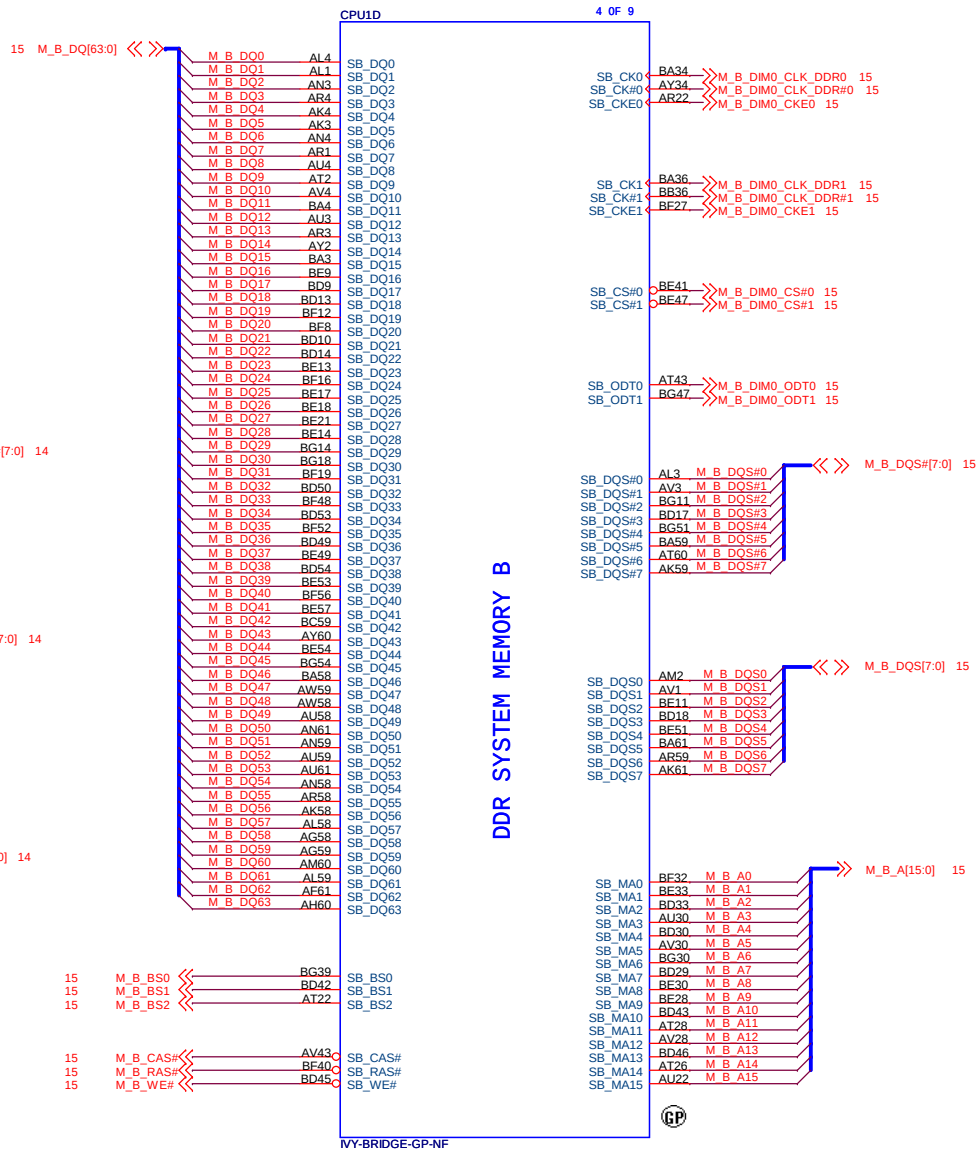
Title	***CPU (THERMAL/CLOCK/PM)***
Size: Custom	Document Number: **Husk/Petra** — Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 5 of 103

SSID = CPU





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Taipei Hsien 221, Taiwan, R.O.C.

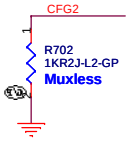
Title: CPU (DDR)

Size: A3 | Document Number: Husk/Petra | Rev: -4M

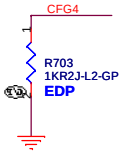
Date: Thursday, September 06, 2012 | Sheet 6 of 103

SSID = CPU

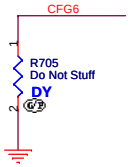
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



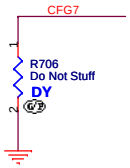
Enabl EDP function	
CFG4	1:Disable 0:Enable

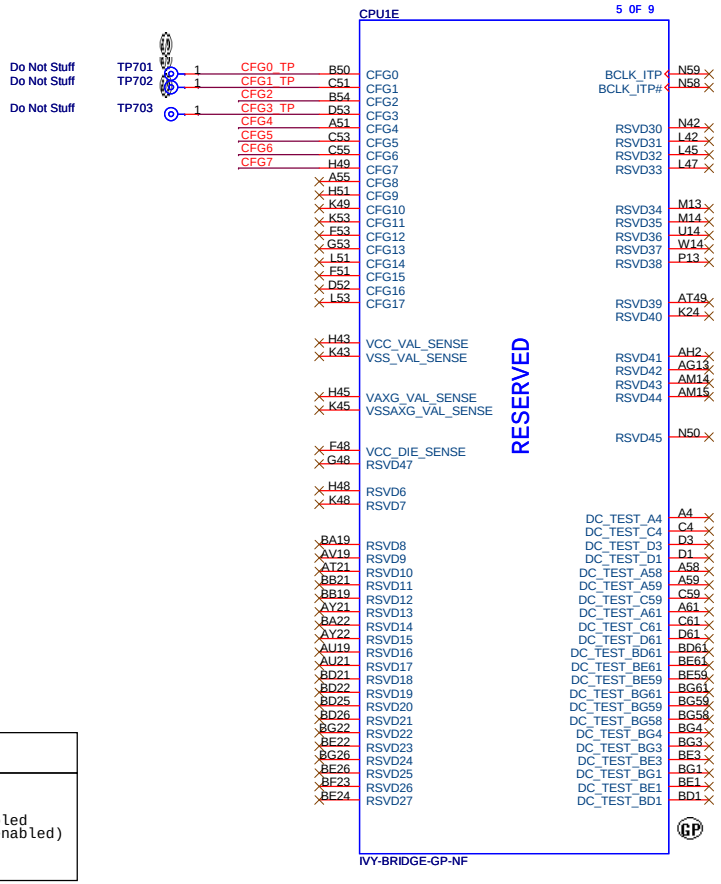


PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





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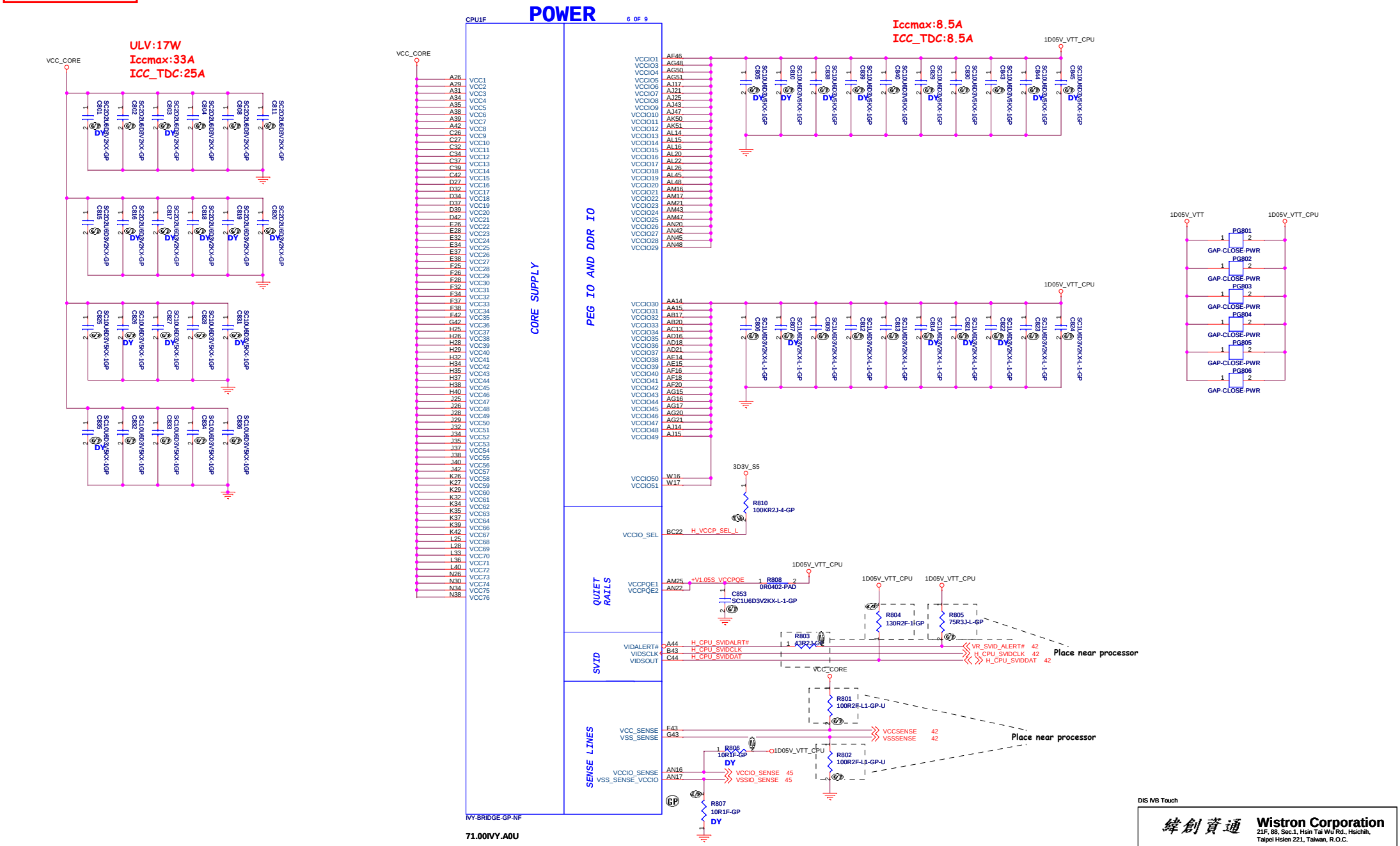
Title: CPU (RESERVED)

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 7 of 103

SSID = CPU



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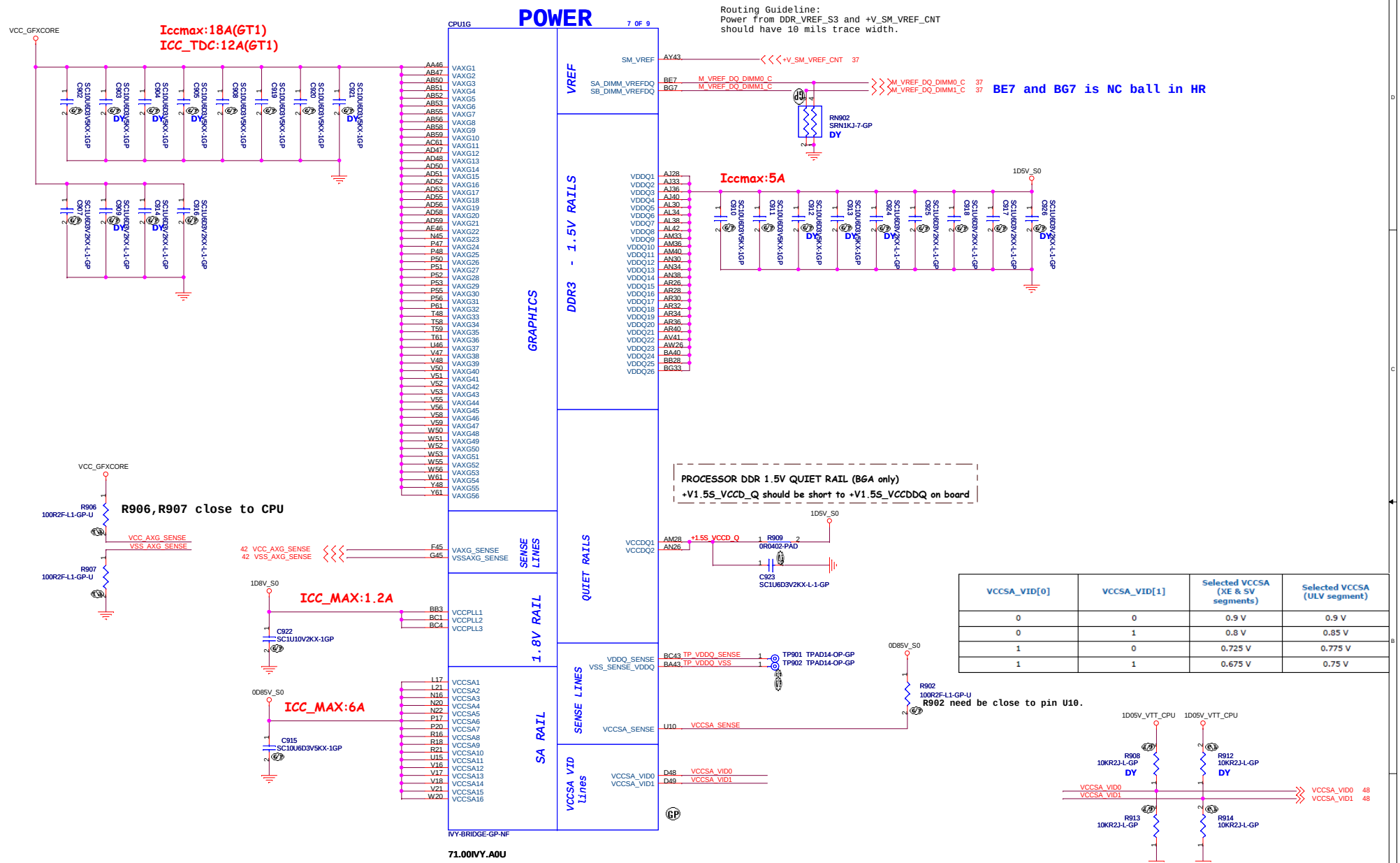
Title: CPU (VCC_CORE)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Monday, September 17, 2012 | Sheet 8 of 103

SSID = CPU



VCCSA_VID[0]	VCCSA_VID[1]	Selected VCCSA (XE & SV segments)	Selected VCCSA (ULV segment)
0	0	0.9 V	0.9 V
0	1	0.8 V	0.85 V
1	0	0.725 V	0.775 V
1	1	0.675 V	0.75 V

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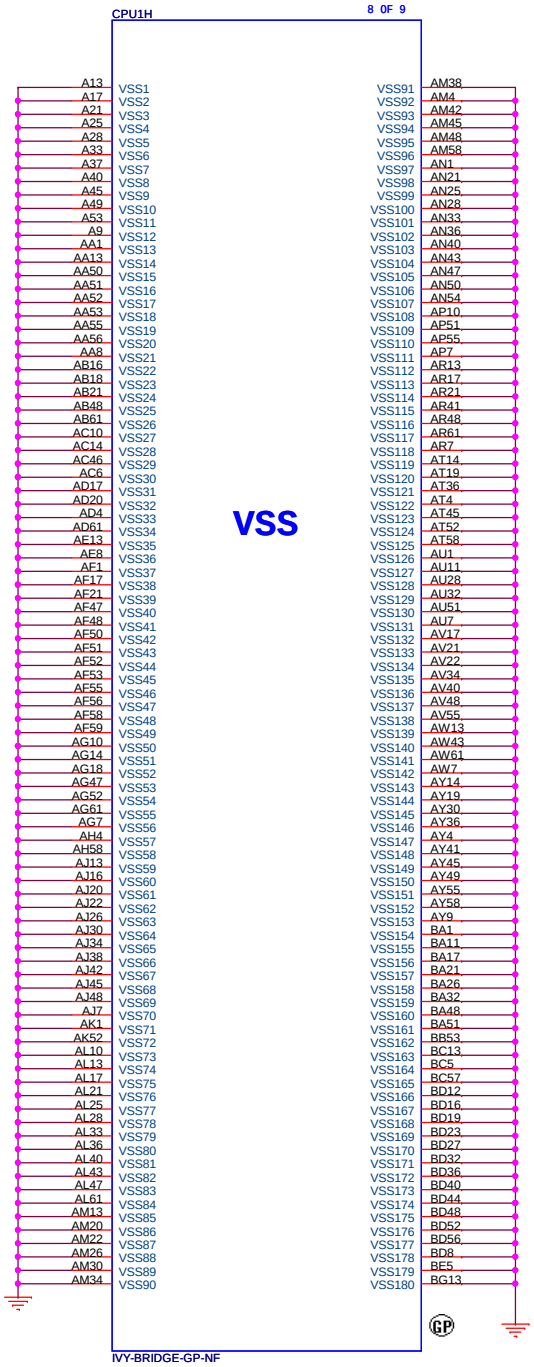
Title: CPU (VCC_GFXCORE)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Monday, September 17, 2012 | Sheet 9 of 103

SSID = CPU



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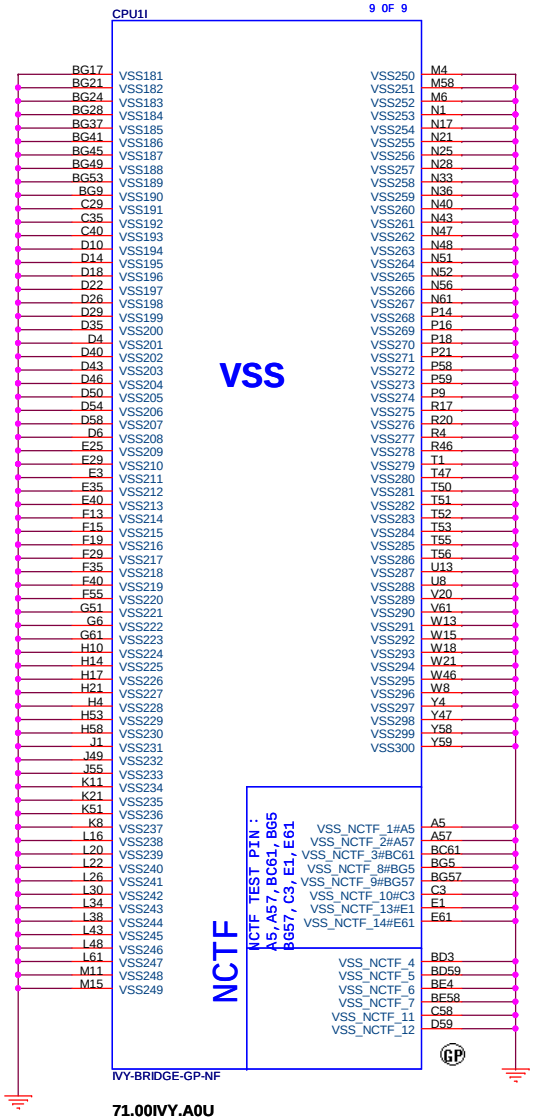

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Title		
	CPU (VSS)	
Size A3	Document Number Husk/Petra	Rev -4M
Date: Thursday, September 06, 2012	Sheet 10 of 103	

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Title		
	XDP	
Size A3	Document Number **Husk/Petra**	Rev **-4M**
Date: Thursday, September 06, 2012	Sheet 11 of 103	

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Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 12 of 103

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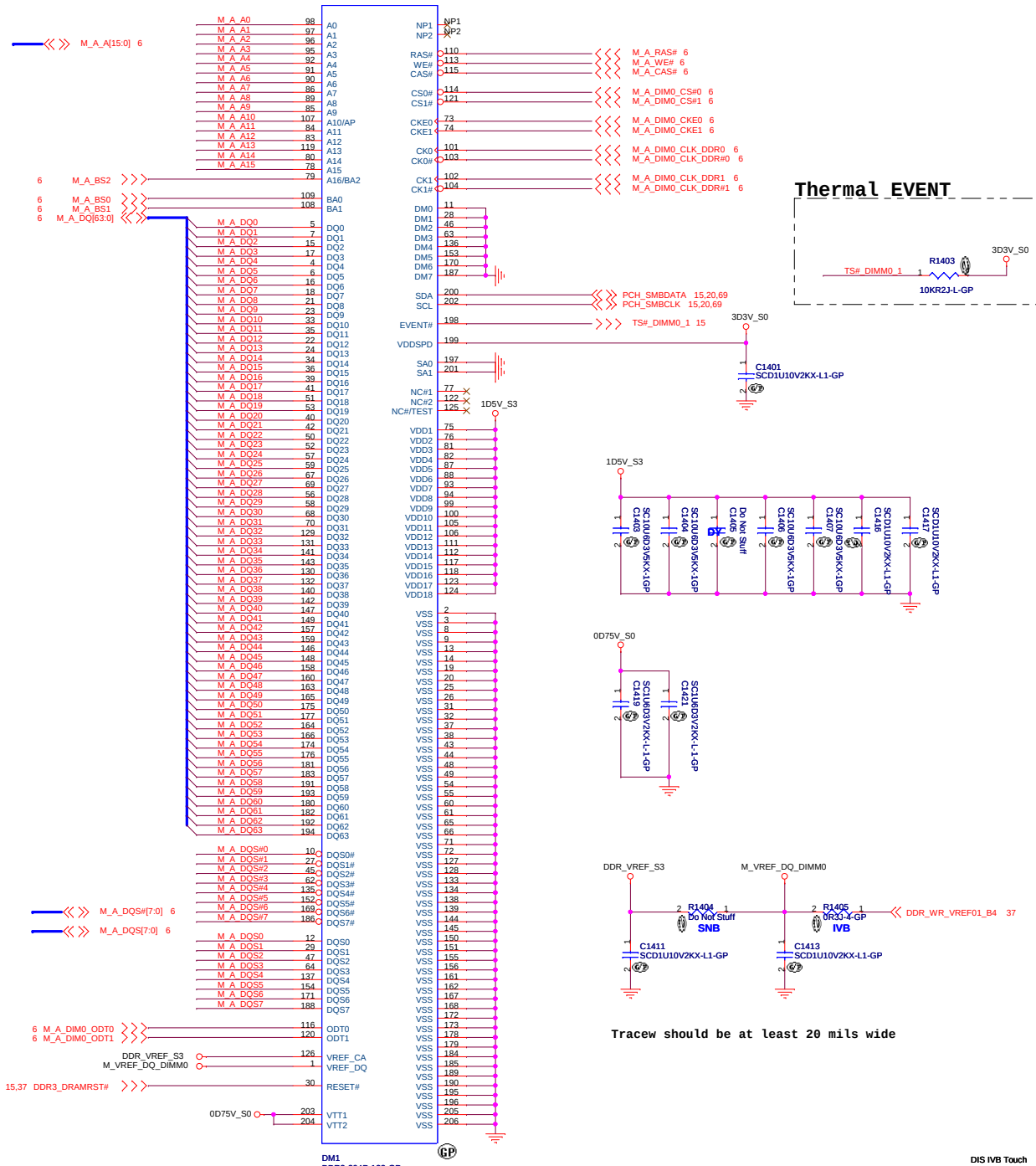
Title: ***Reserved***

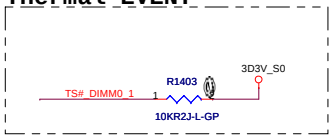
Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 13 of 103

SSID = MEMORY



Thermal EVENT



Tracew should be at least 20 mils wide

DIS IVB Touch

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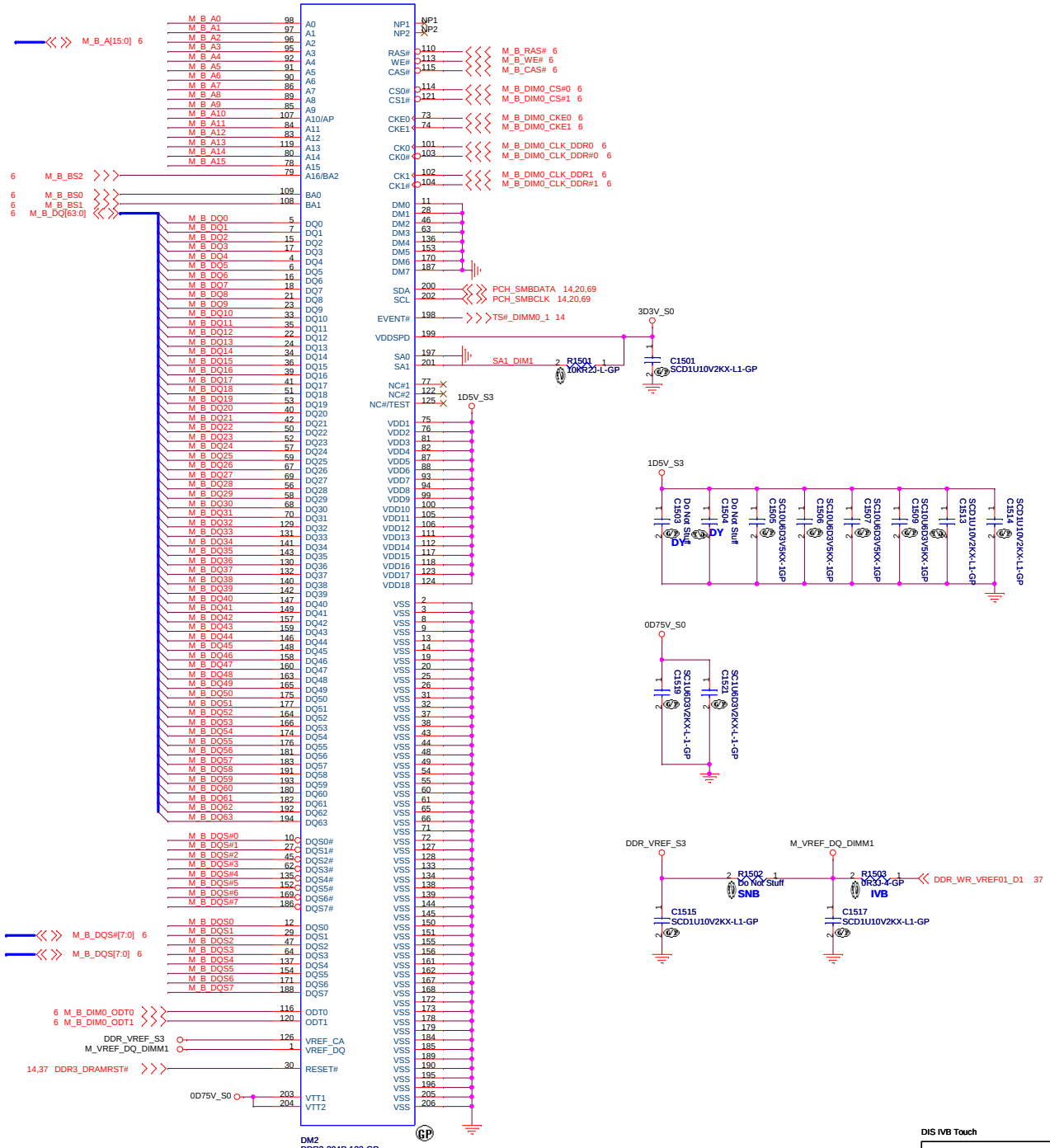
Title: **DDR3-SODIMM1**

Size: Custom | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 14 of 103

SSID = MEMORY



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Title: **DDR3-SODIMM2**

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 15 of 102

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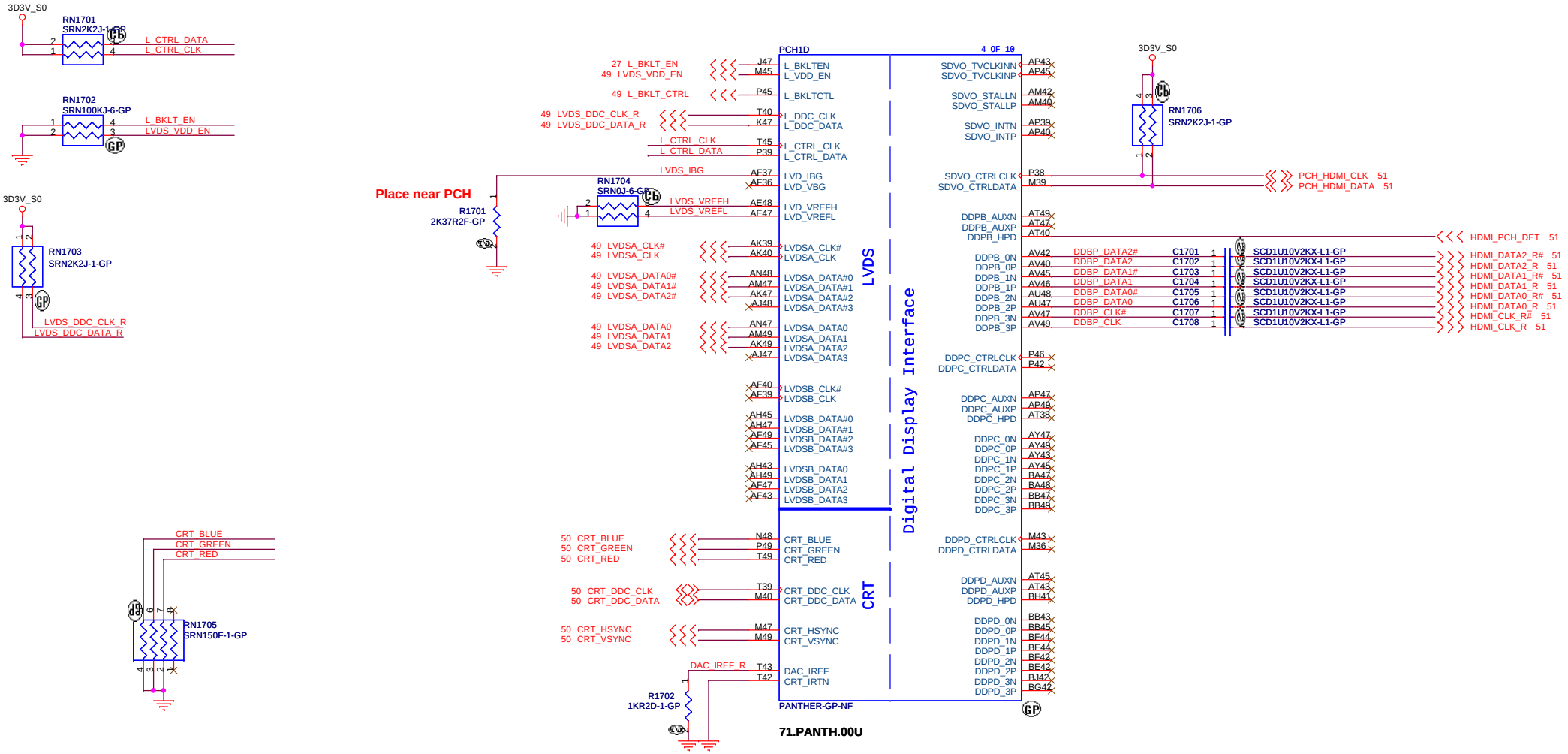
Title: DDR3-SODIMM2

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 16 of 103



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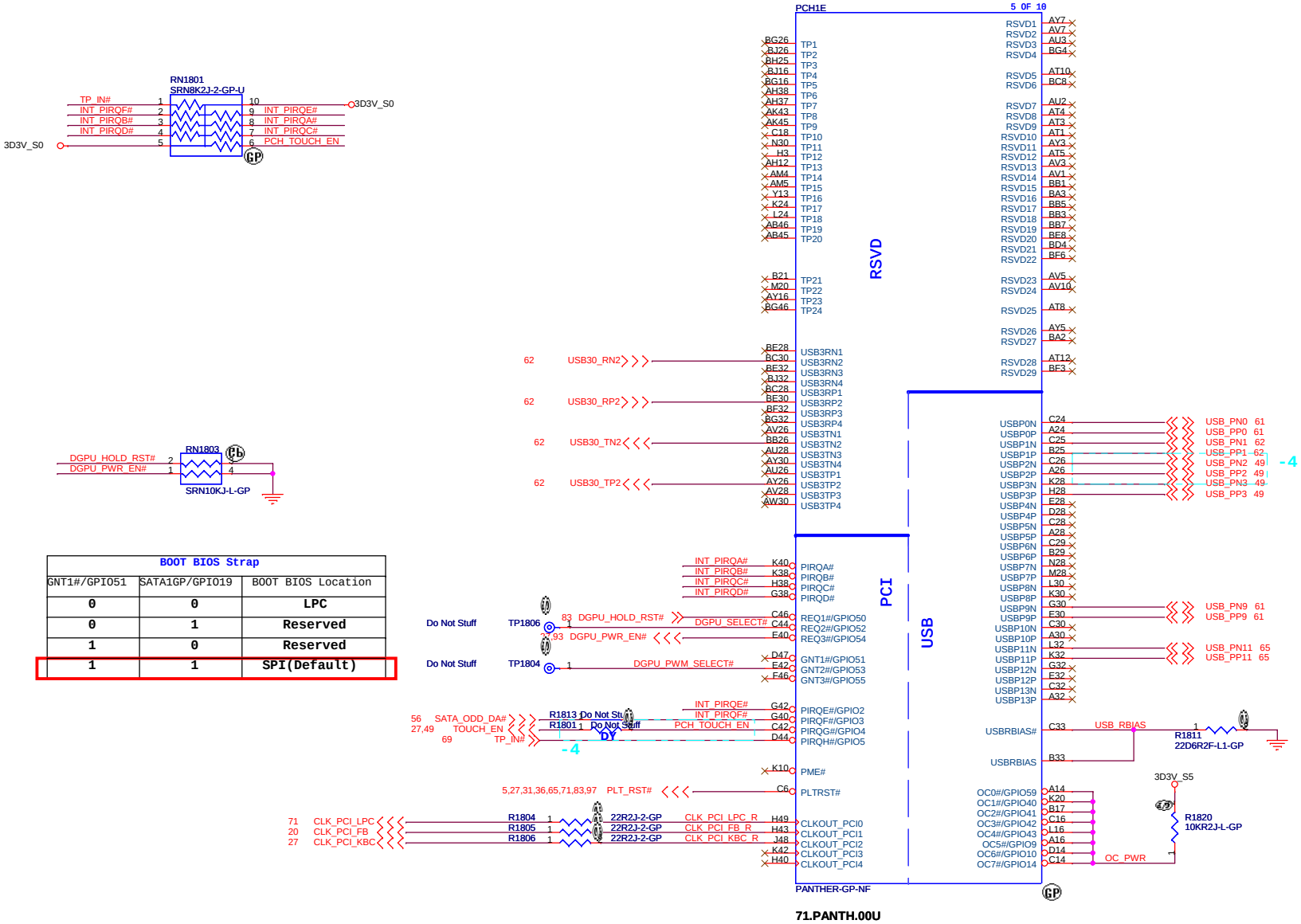
Title: ***PCH (LVDS/CRT/DDI)***

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 17 of 103

SSID = PCH



BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Table

Pair	Device
0	USB2.0 Ext. port 1
1	USB3.0/USB2.0 Ext. port 2
2	Touch panel
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

DIS IVB Touch

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 18 of 103

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

PCH1C — 3 OF 10

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP, DMI_ZCOMP, DMI_IRCOMP, DMI2RBIAS

FDI: FDI_RXN0, FDI_RXN1, FDI_RXN2, FDI_RXN3, FDI_RXN4, FDI_RXN5, FDI_RXN6, FDI_RXN7, FDI_RXP0, FDI_RXP1, FDI_RXP2, FDI_RXP3, FDI_RXP4, FDI_RXP5, FDI_RXP6, FDI_RXP7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

System Power Management: SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#, DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29

PANTHER-GP-NF

71.PANTH.00U

1D05V_VTT
R1901 1 49D9R2F-GP DMI_COMP_R
R1902 1 750R2F-GP RBIAS_CPY

SUS_PWR_ACK# — SUSACK#
3D3V_S0 — R1905 1 10KR2J-L-GP — SYS_RESET#
DY R1926 1 Do Not Stuff — SYS_PWROK
R1904 1 100KR2J-4-GP — PWROK
36 SYS_PWROK
27 S0_PWR_GOOD — R1924 2 1 Do Not Stuff — PWROK
37 PM_DRAM_PWRGD
PM_RSMRST#
SUS_PWR_ACK_R
27,97 PM_PWRBTN#
27 AC_PRESENT
BATLOW#
PM_RI#

DSWODVREN
PCH_DPWROK — R1910 1 Do Not Stuff, R1911 1 Do Not Stuff DY — PM_RSMRST# — RTC_AUX_S5
PCIE_WAKE#
PM_CLKRUN# 27
PCH_SUSCLK_KBC 27
PM_SLP_S4# 27,46
PM_SLP_S3# 27,29,36,37,47
SLLP_SUS#_TP — TP1904 Do Not Stuff
H_PM_SYNC 5

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
R1917 1 330KR2J-L1-GP
DSWODVREN — R1918 1 DY Do Not Stuff

3D3V_S0
PM_CLKRUN# — R1919 1 8K2R2J-3-GP

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

3D3V_S5
RN1901 SRN10KJ-6-GP
8 1 BATLOW#
7 2 PM_RI#
6 3 AC_PRESENT
5 4 SUS_PWR_ACK_R
R1921 1 10KR2J-L-GP — PCIE_WAKE#
R1922 1 10KR2J-L-GP — SUS_PWR_ACK#
R1908 1 100KR2J-4-GP — PM_RSMRST#

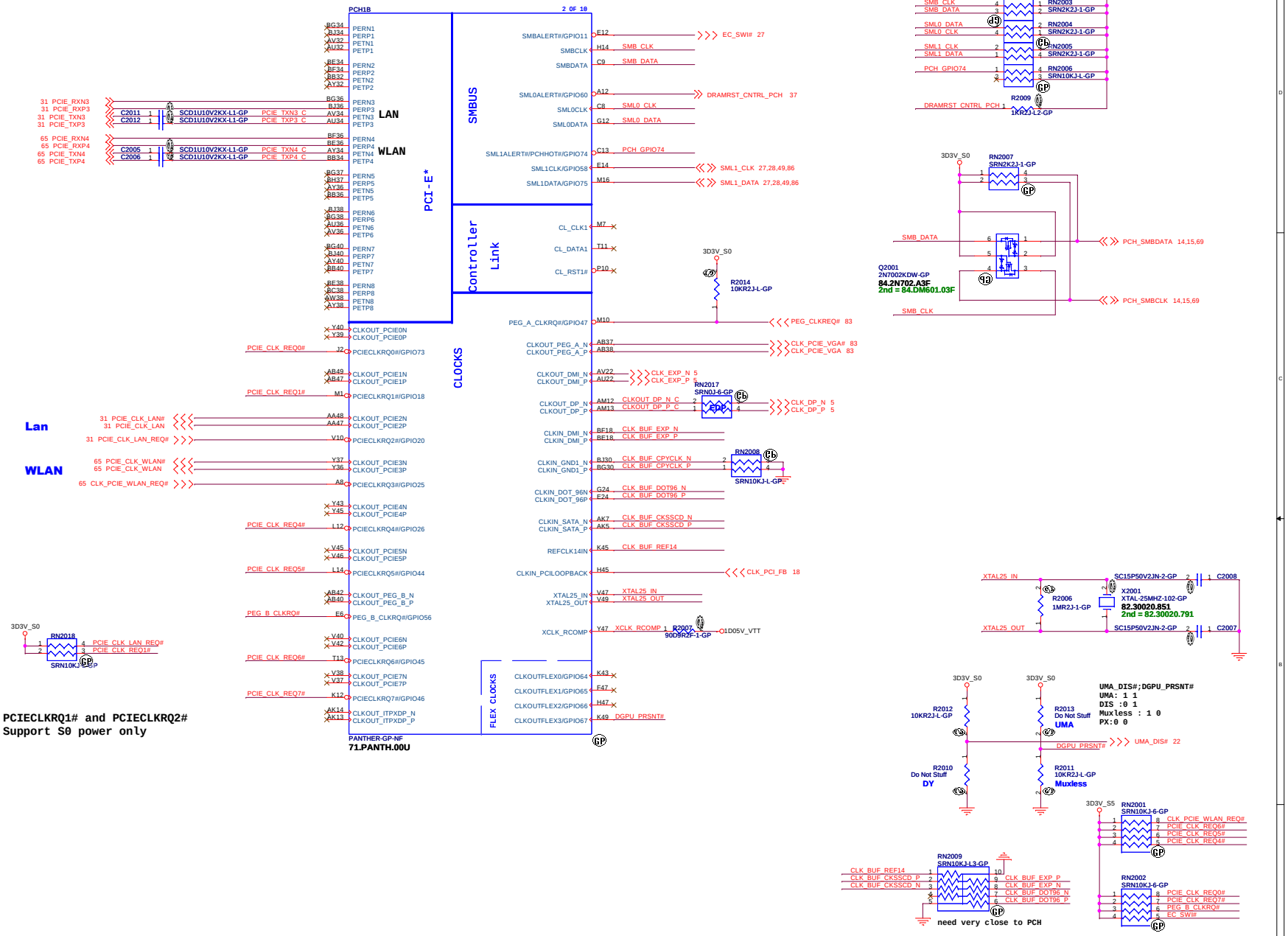
3D3V_AUX_S5
R1909 1 100KR2J-4-GP
R1916 10KR2J-L-GP
3V_5V_POK_#
PM_RSMRST# — R1912 1 1KR2J-L2-GP 2 — RSMRST#_KBC 27
3V_5V_POK 41
Q1901 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
3rd = 84.2N702.F3F

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**
Size: A3 | Document Number: **Husk/Petra** | Rev: **-4M**
Date: Thursday, September 06, 2012 | Sheet 19 of 103

SSID = PCH



DIS IVB Touch

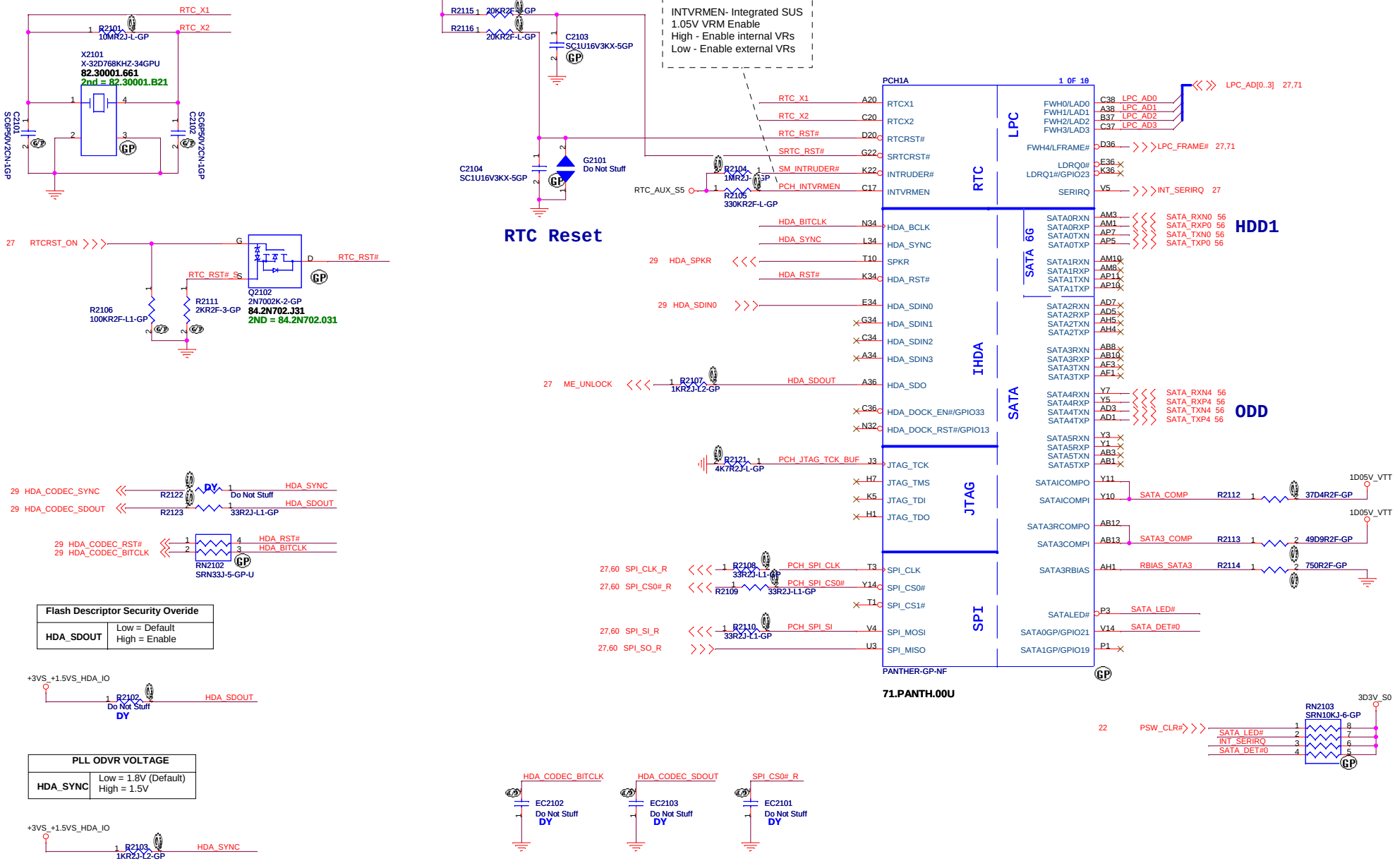
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 20 of 103

SSID = PCH



Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

DIS IVB Touch

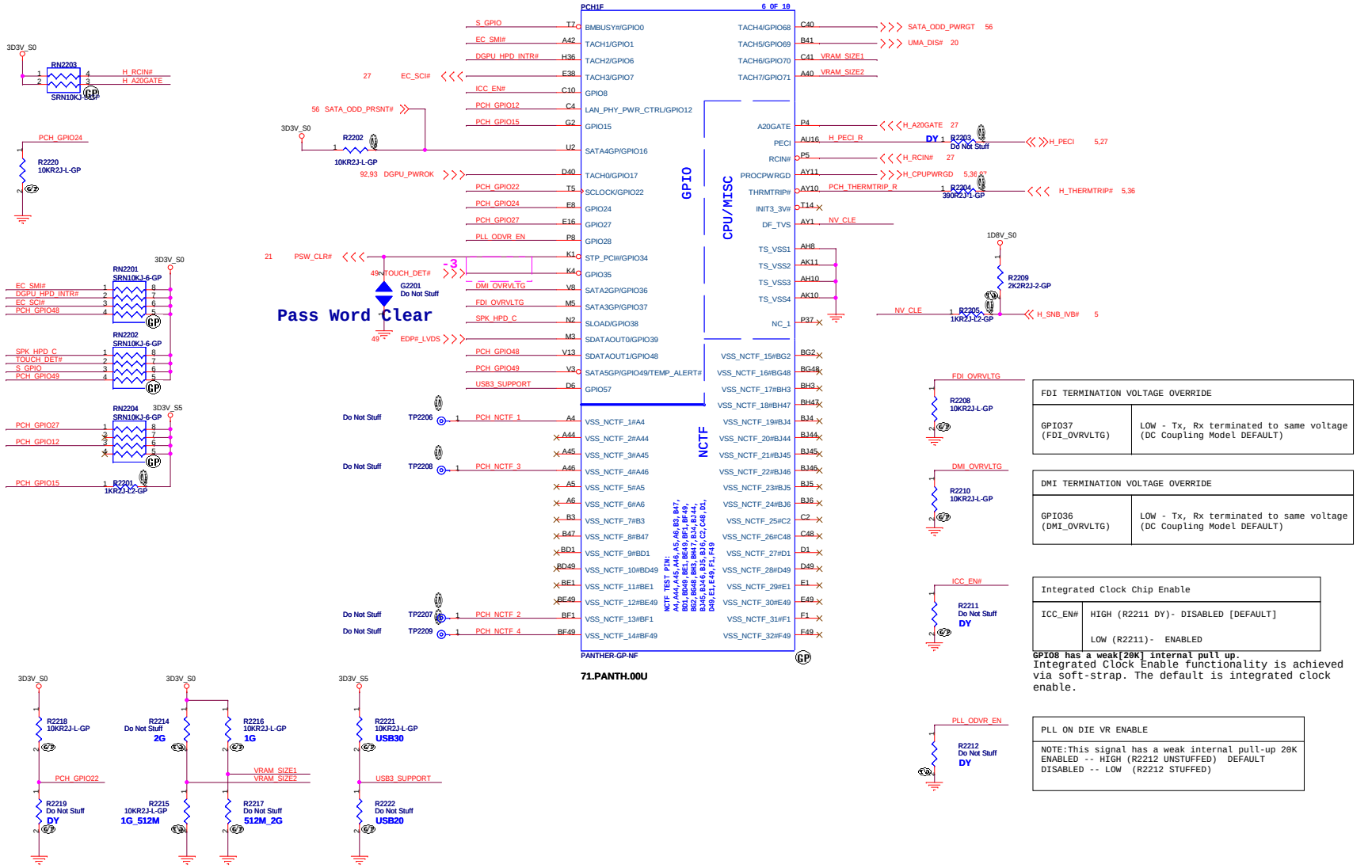
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 21 of 103

SSID = PCH



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

DIS IVB Touch

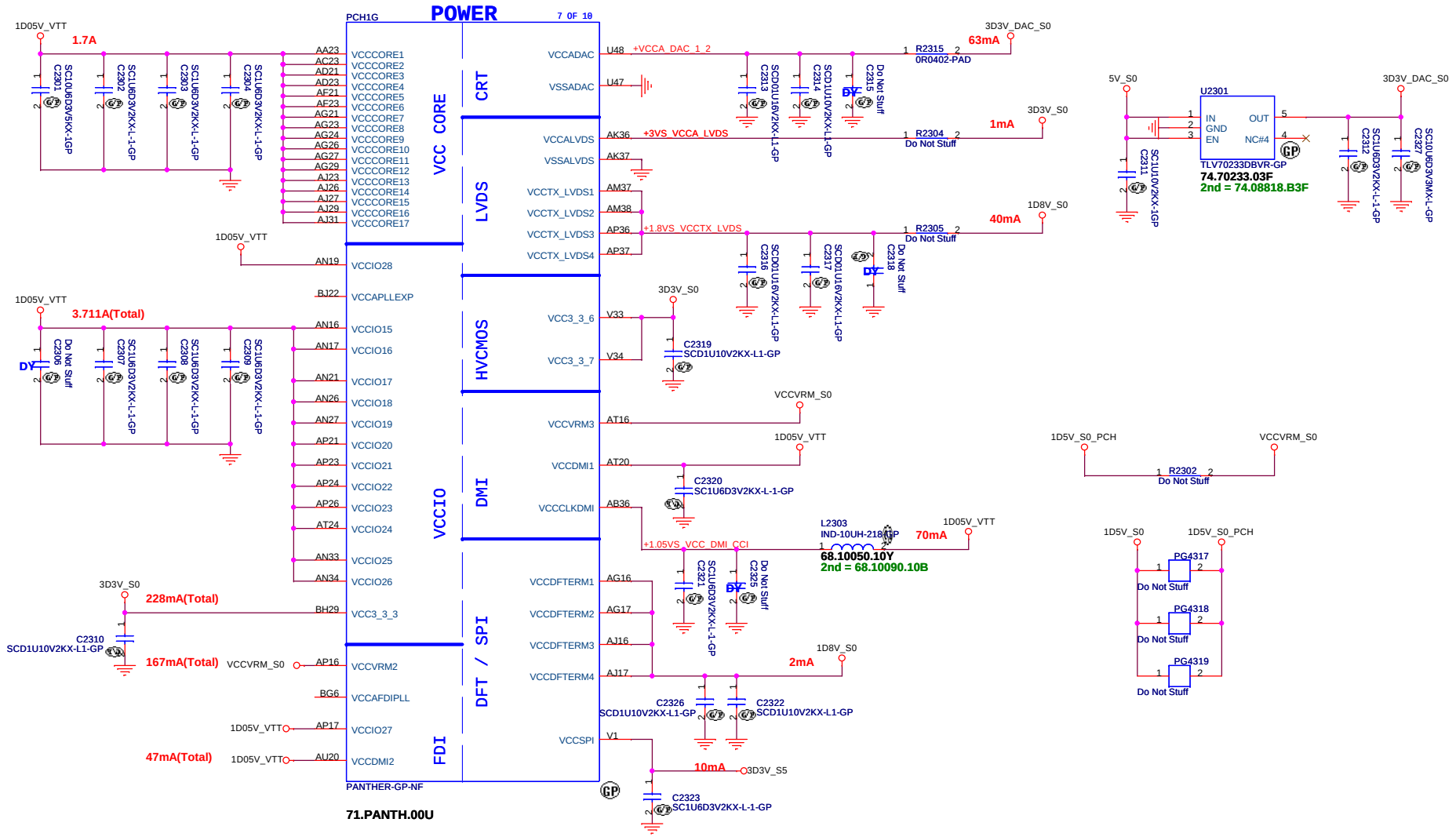
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 22 of 103

SSID = PCH



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER1)**

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 23 of 103

SSID = PCH

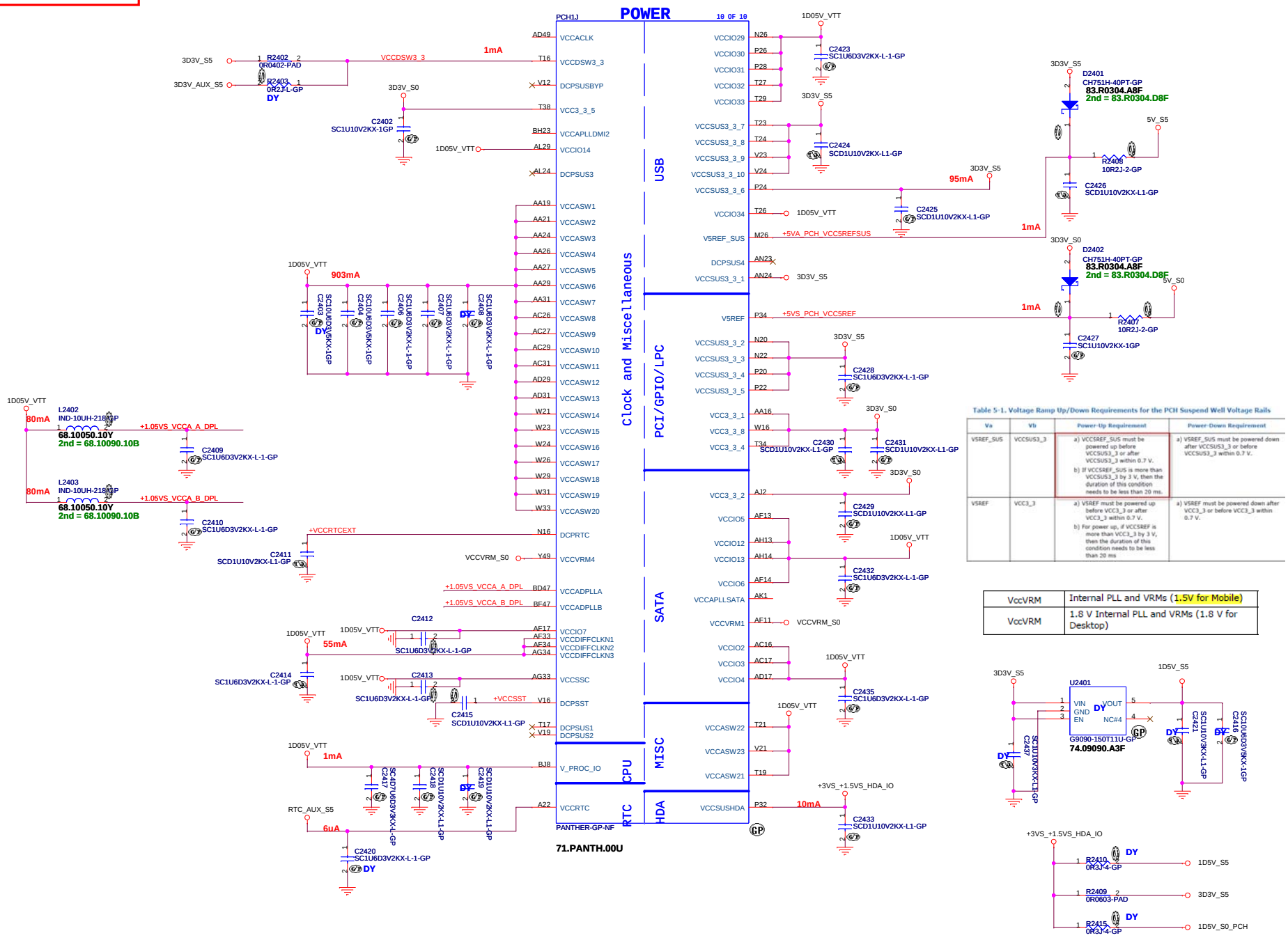


Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VCCSREF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCCSREF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCCSREF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)

DIS IVB Touch

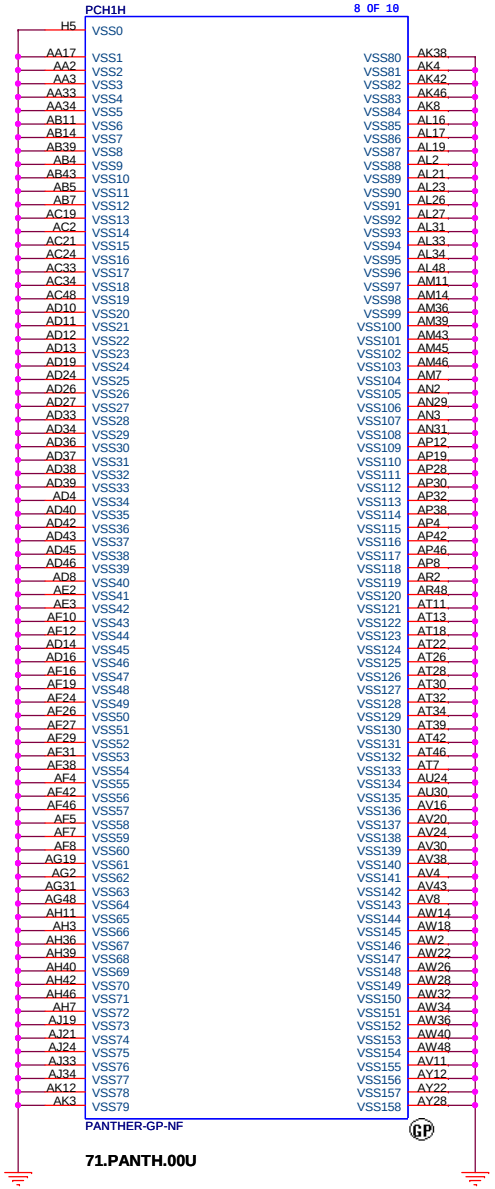
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

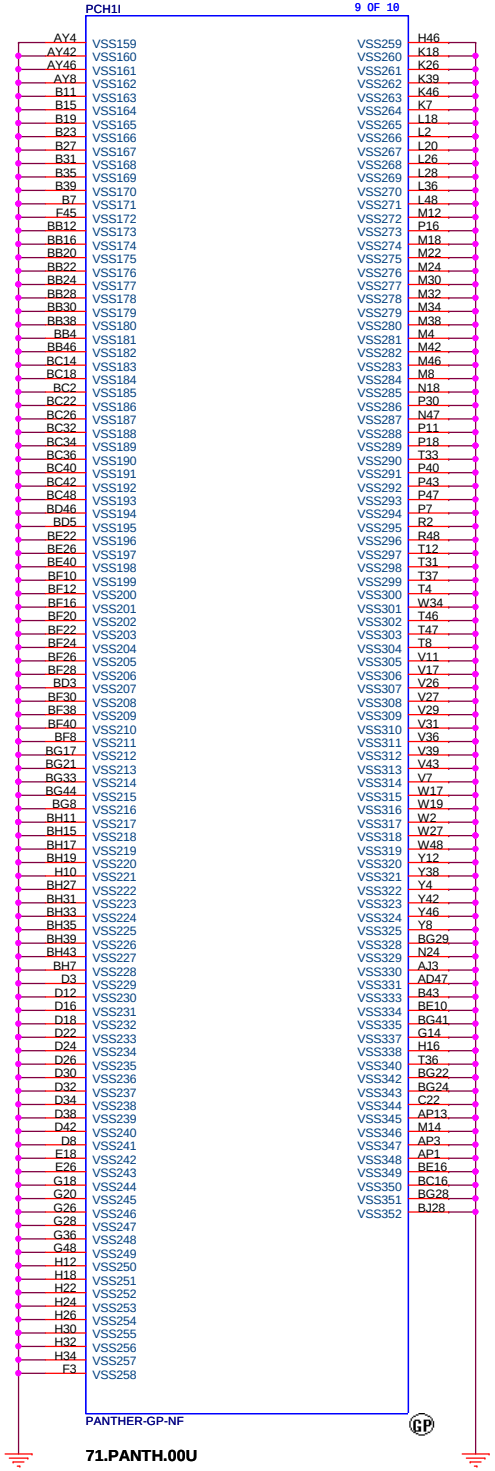
Title: PCH (POWER2)

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Monday, September 17, 2012 | Sheet 24 of 103

SSID = PCH





DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 25 of 103

DIS IVB Touch

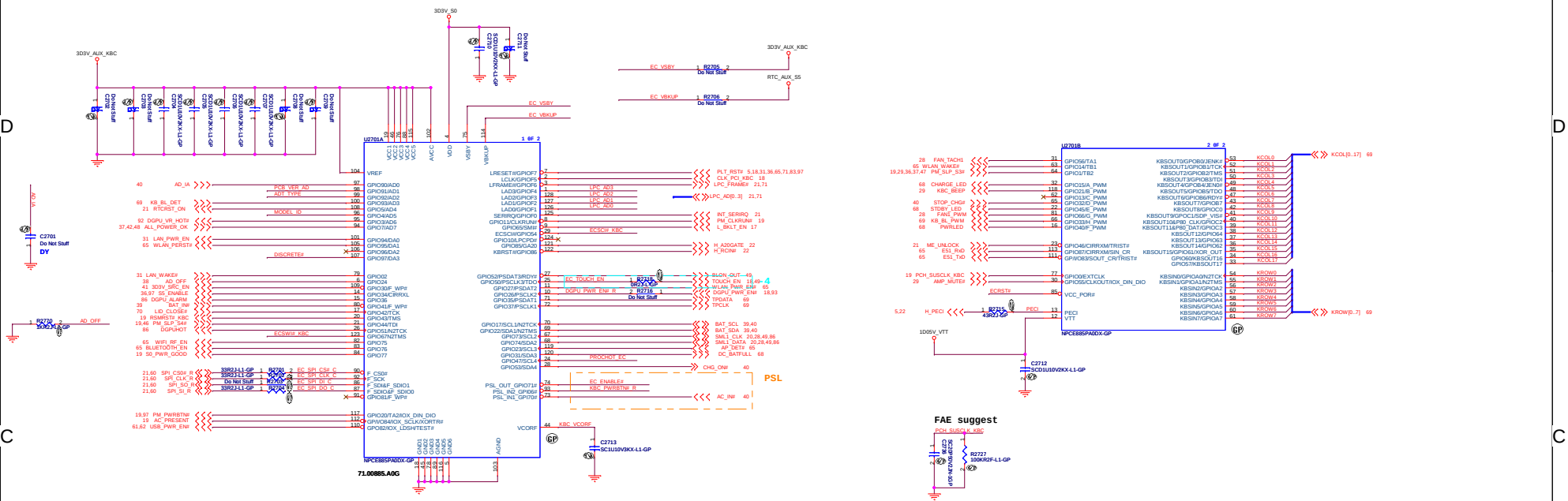
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

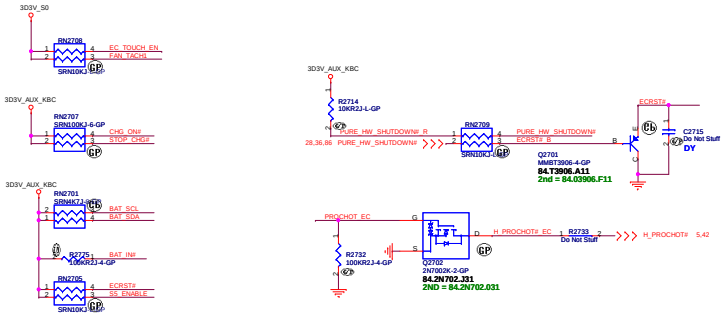
Title
Clock(colay)

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

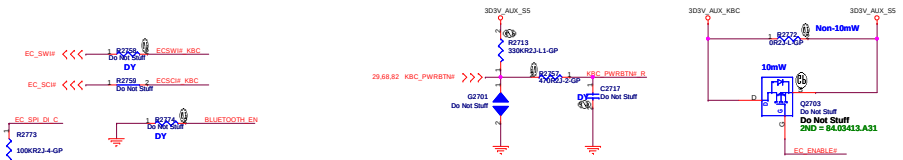
Date: Thursday, September 06, 2012 Sheet 26 of 103

SSID = KBC



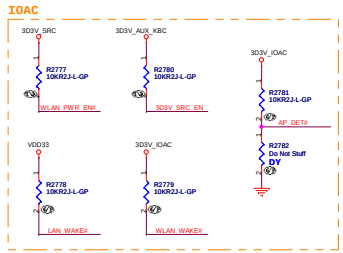


PSL Function

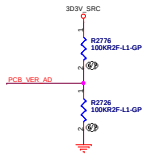


AC_IN#	KBC_PWRBTN#	EC_ENABLE#

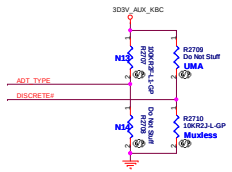
Inputs			Output
PSL_IN1_GPI76	PSL_IN2_GPI66	Bit 1 of P7DOUT Register	PSL_OUT_GPIO71
Low	X	X	Low
High	High-to-Low	X	Low
High	X	0-to-1	High



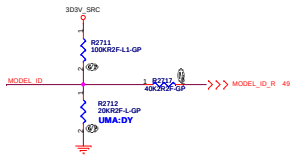
PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
-1	100.0K	33.0K	2.48V
-2	100.0K	47.0K	2.24V
-3	100.0K	64.9K	2.0V
-4	100.0K	76.8K	1.87V
-4M	100.0K	100K	1.65V
	100.0K	143.0K	1.358V
	100.0K	174.0K	1.204V
	100.0K	215.0K	1.047V



ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V



MODEL_ID	Pull-Low Register(R2712)	Pull-High Register(R2711)	SERIES RESISTOR(R3712)	Typical Voltage
14"(AMD)	30.0 K	100.0 K	40.2K	0.7615V
15"(AMD)	30.0 K	100.0 K	40.2K	0.4838V
14"(INV)	20.0 K	100.0 K	40.2K	0.55V
15"(INV)	20.0 K	100.0 K	40.2K	0.3888V
14"(UMA)	DY	100.0 K	40.2K	3.3V
15"(UMA)	DY	100.0 K	40.2K	0.9462V



DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

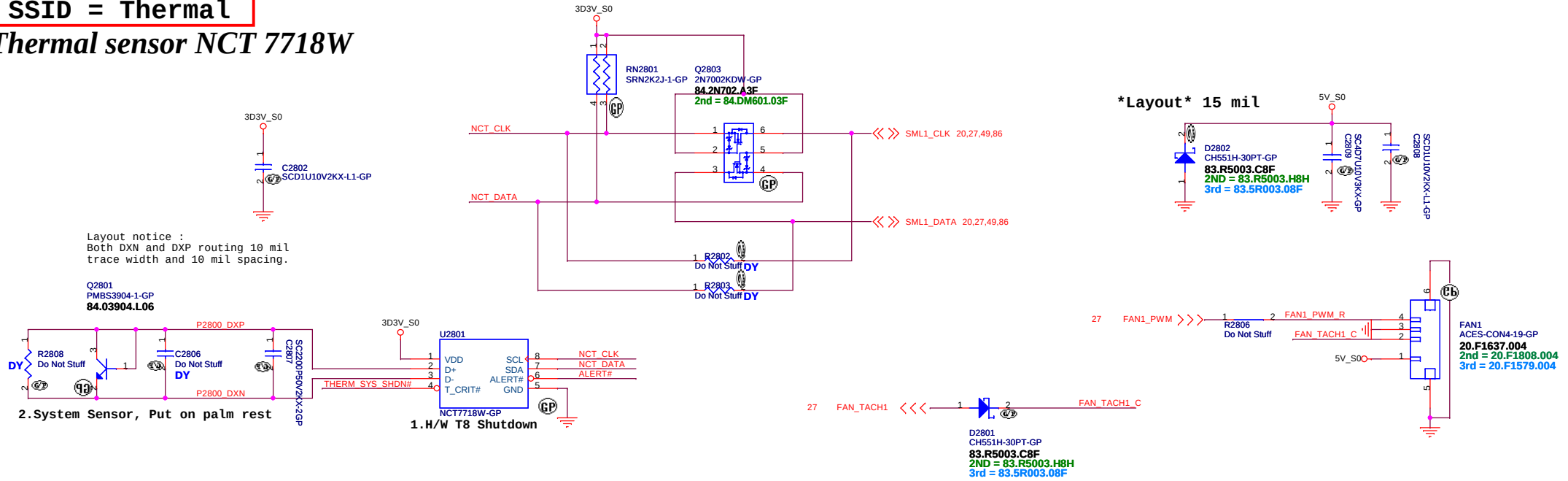
Title: KBC NPCE885

Size: Custom | Document Number: Husk/Petra | Rev: -4M

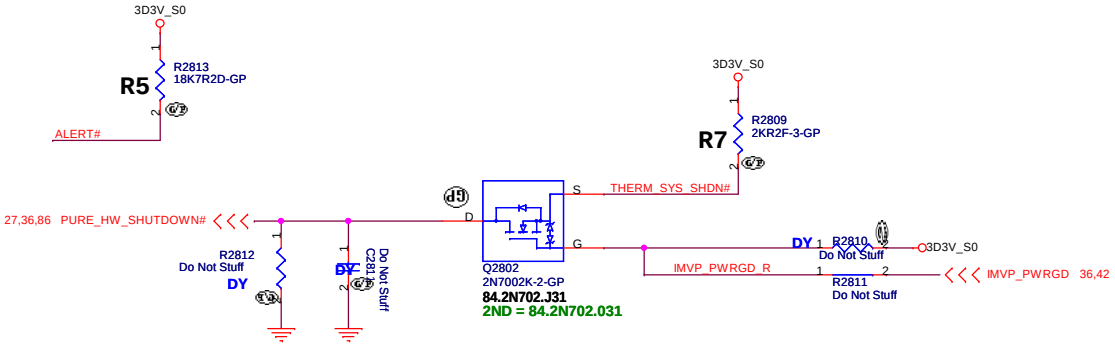
Date: Thursday, September 05, 2024 | Sheet 27 of 103

SSID = Thermal

Thermal sensor NCT 7718W



ALERT# /T_CRIT# Pull-up Resistor



R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

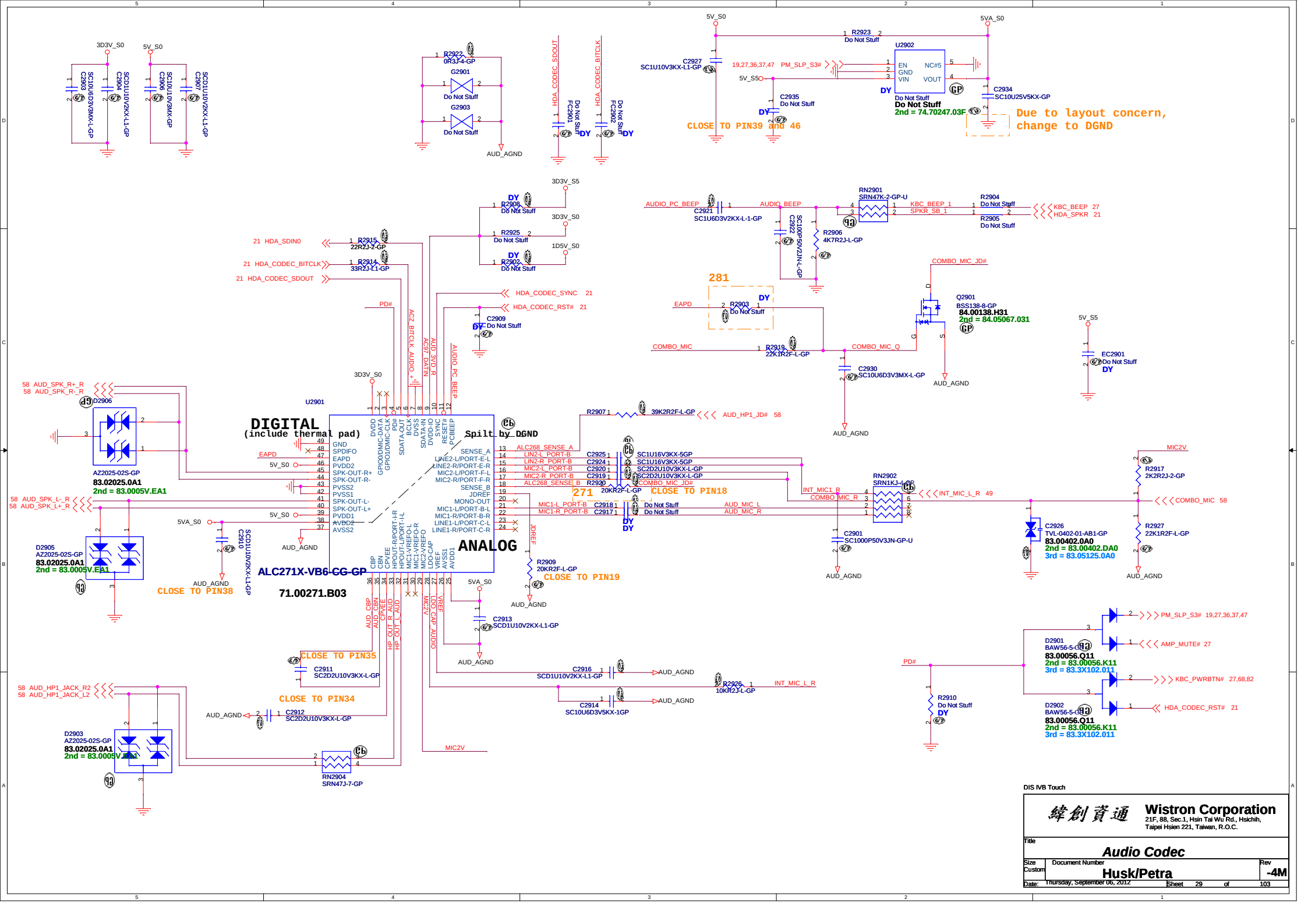
T_CRIT temperature strapping point

SB T8=85 degree

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Thermal NCT7718		
Size: Custom	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 28 of 103	


DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB6-CG-GP
71.00271.B03
U2901
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN39 and 46
CLOSE TO PIN18
CLOSE TO PIN19
Due to layout concern, change to DGND
U2902
2nd = 74.70247.03F
Q2901
BSS138-8-GP
84.00138.H31
2nd = 84.05067.031
AZ2025-02S-GP
83.02025.0A1
2nd = 83.0005V.EA1
D2901
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
3rd = 83.3X102.011
D2902
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
3rd = 83.3X102.011
C2901
SC1000P50V3JN-GP-U
C2926
TVL-0402-01-AB1-GP
83.00402.0A0
2nd = 83.00402.DA0
3rd = 83.05125.0A0
RN2904
SRN47J-7-GP
RN2902
SRN1KJ-4-GP
RN2901
SRN47K-2-GP-U
281
271
DIS IVB Touch
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec
Size
Custom
Document Number
Husk/Petra
Rev
-4M
Date: Thursday, September 06, 2012
Sheet 29 of 103

DIS IVB Touch

緯創資通 **Wistron Corporation**

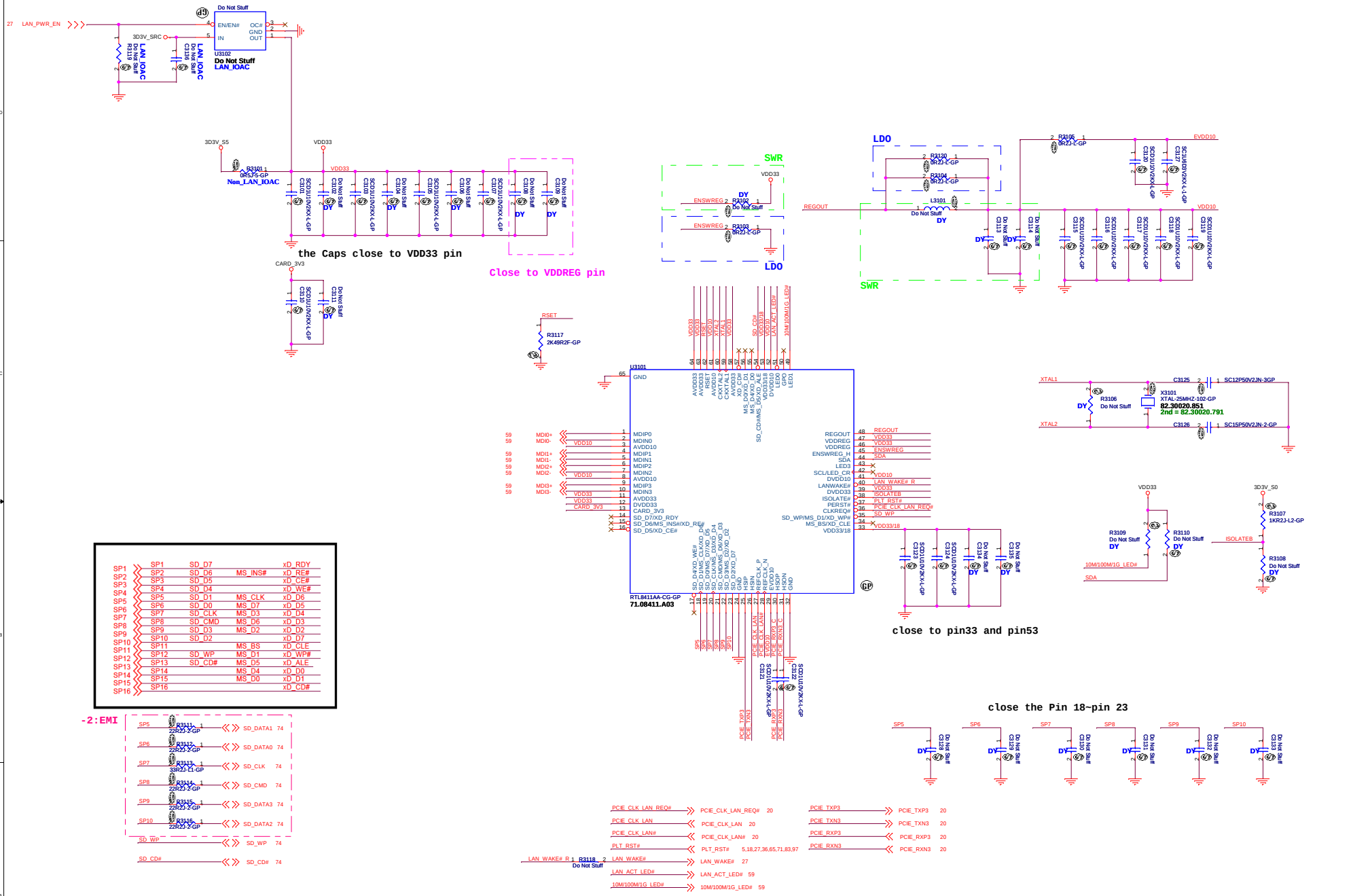
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio AMP

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 30 of 103



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN(RTL8411)***

Size: Custom | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 31 of 103

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *RTS5159 (CARD READER)*

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 32 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 33 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 34 of 103

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

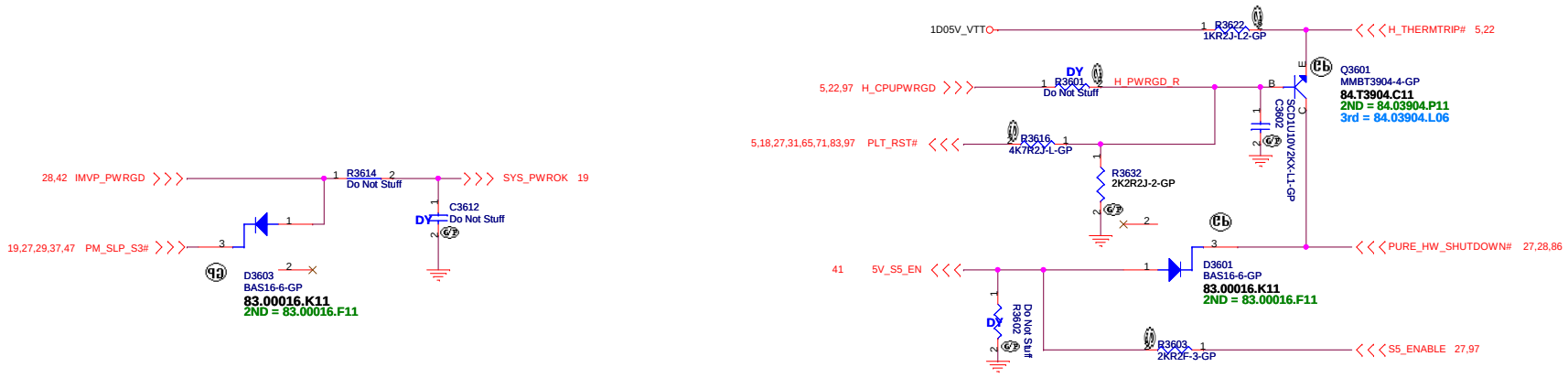
Title

USB 3.0 Controller

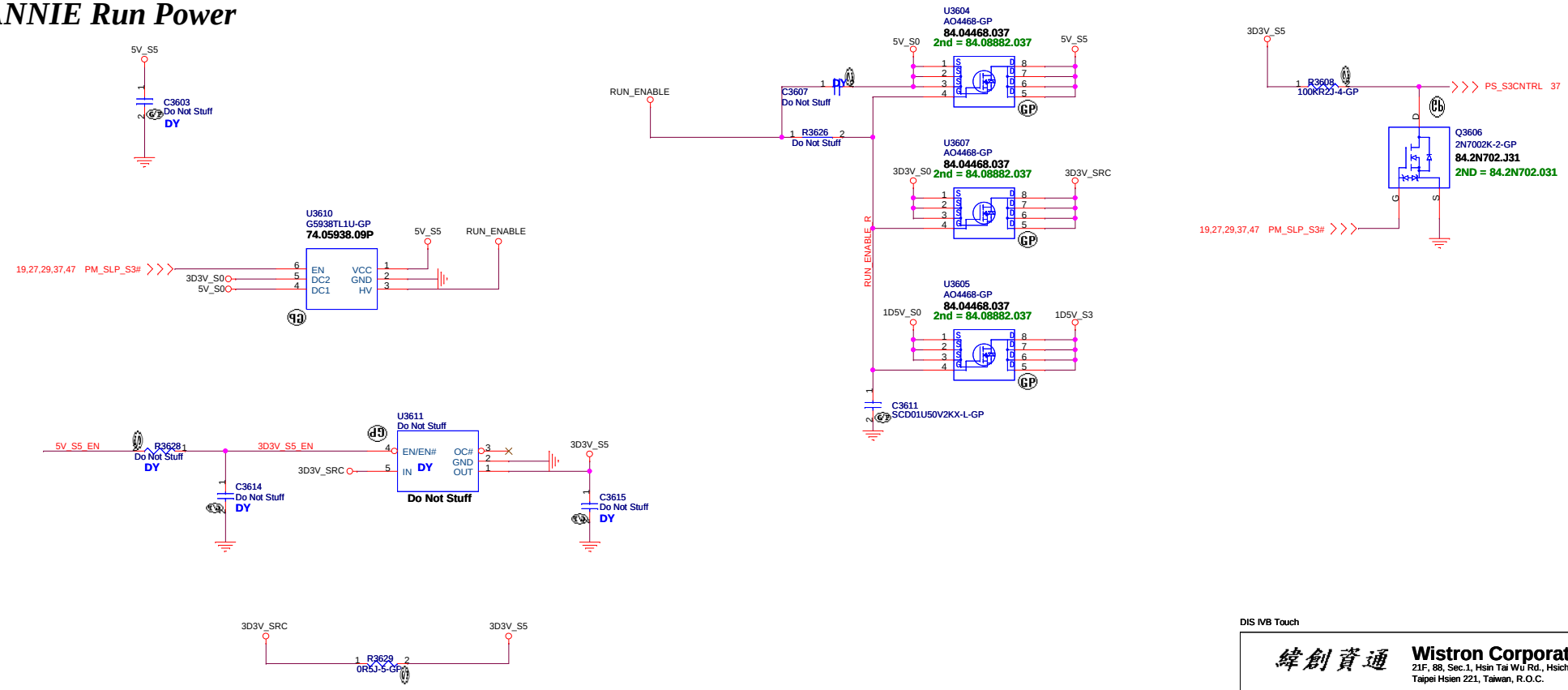
Size	Document Number	Rev
Custom	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 35 of 103

Power Sequence



ANNIE Run Power



DIS IVB Touch

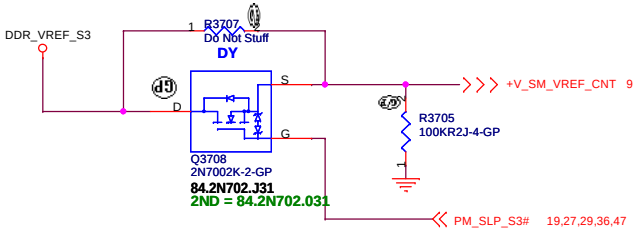
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

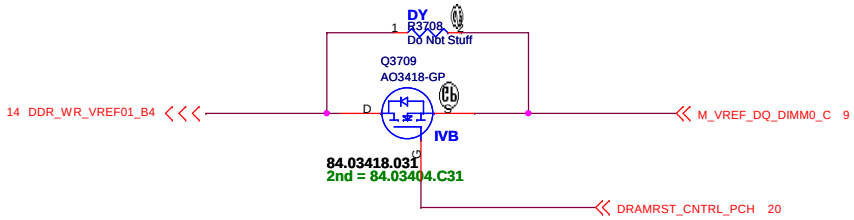
Title: **Power Plane Enable**

Size	Document Number	Rev
Custom	Husk/Petra	-4M

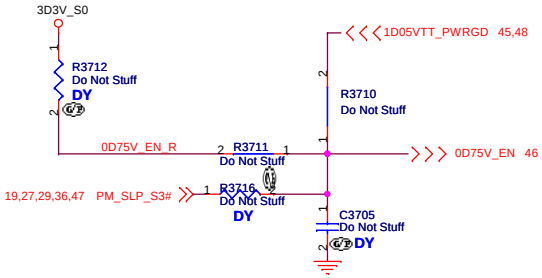
Date: Thursday, September 06, 2012 Sheet 36 of 103

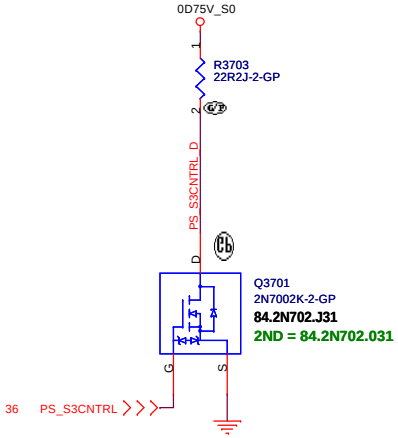
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

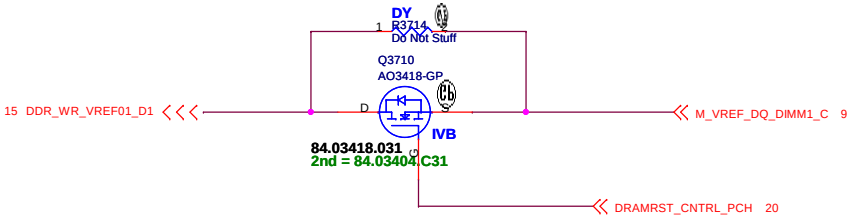




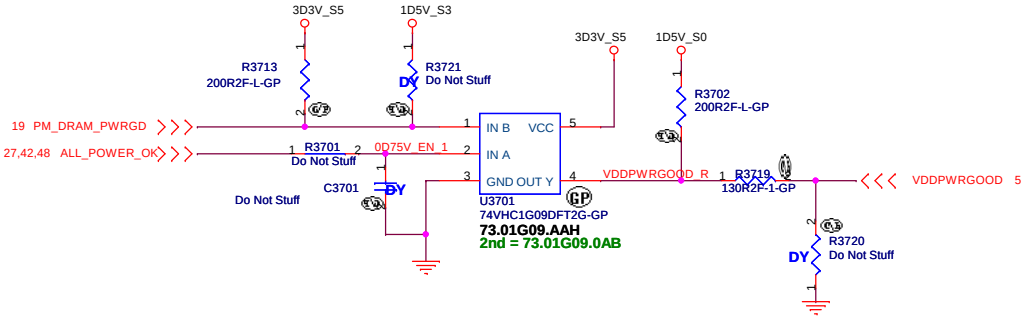
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



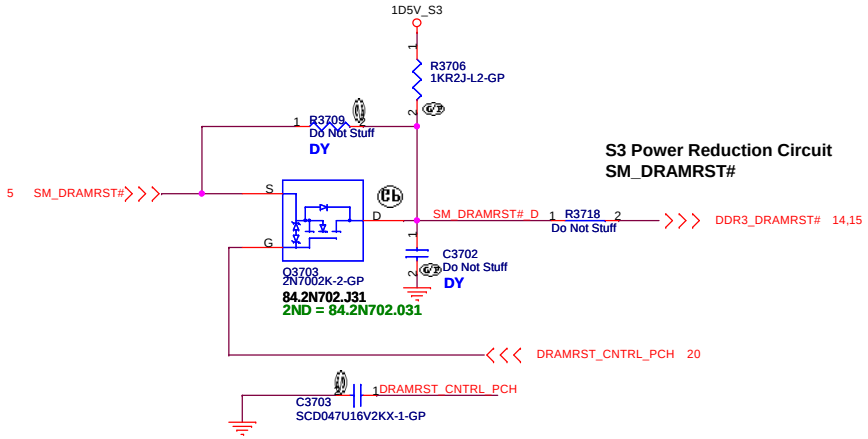




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



S3 Power Reduction Circuit SM_DRAMRST#

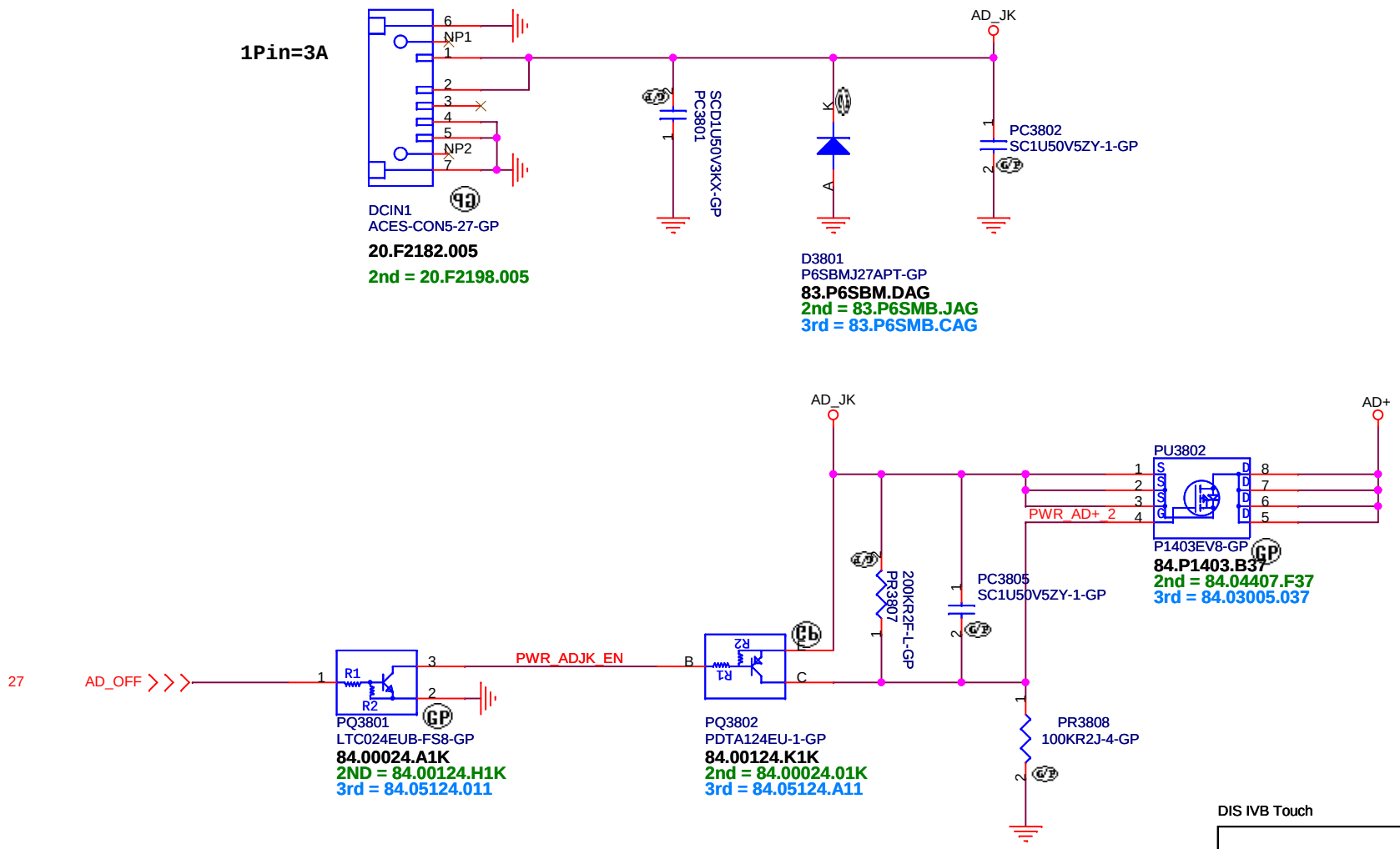
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADAPTER**

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 37 of 103



DIS IVB Touch

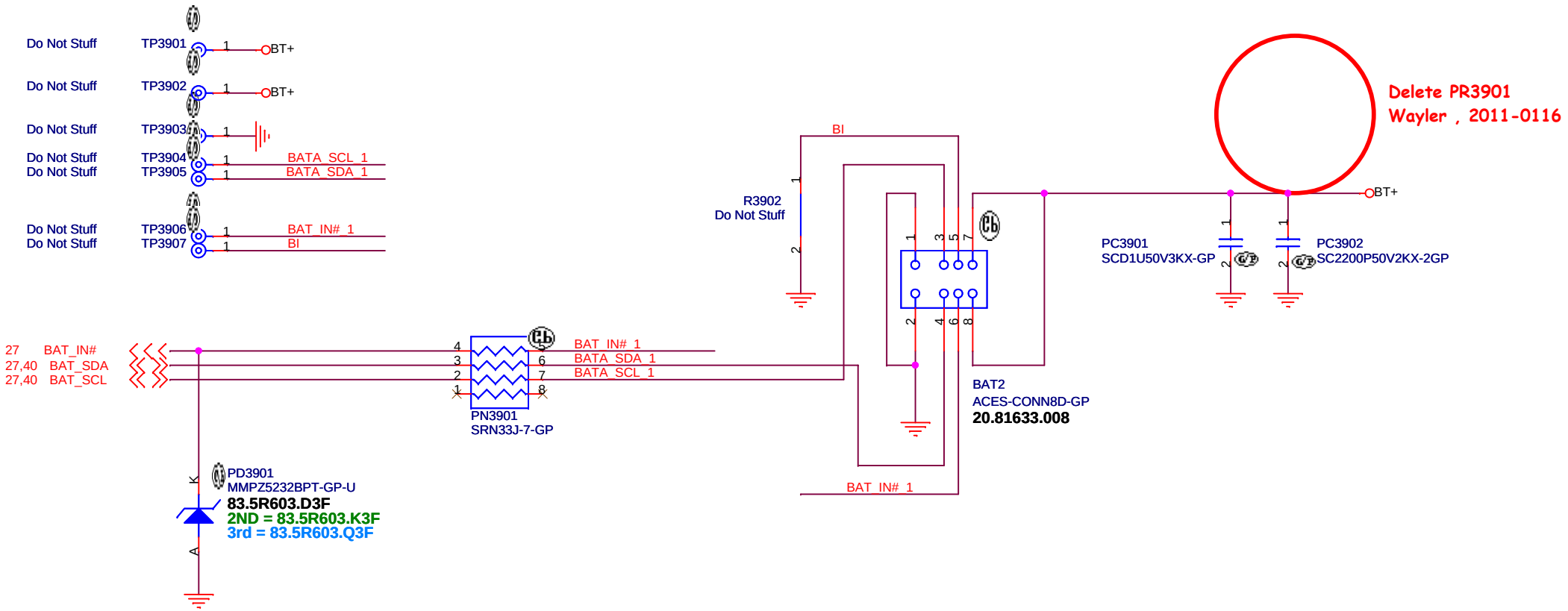
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN JACK**

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 38 of 103

BATTERY CONNECTOR



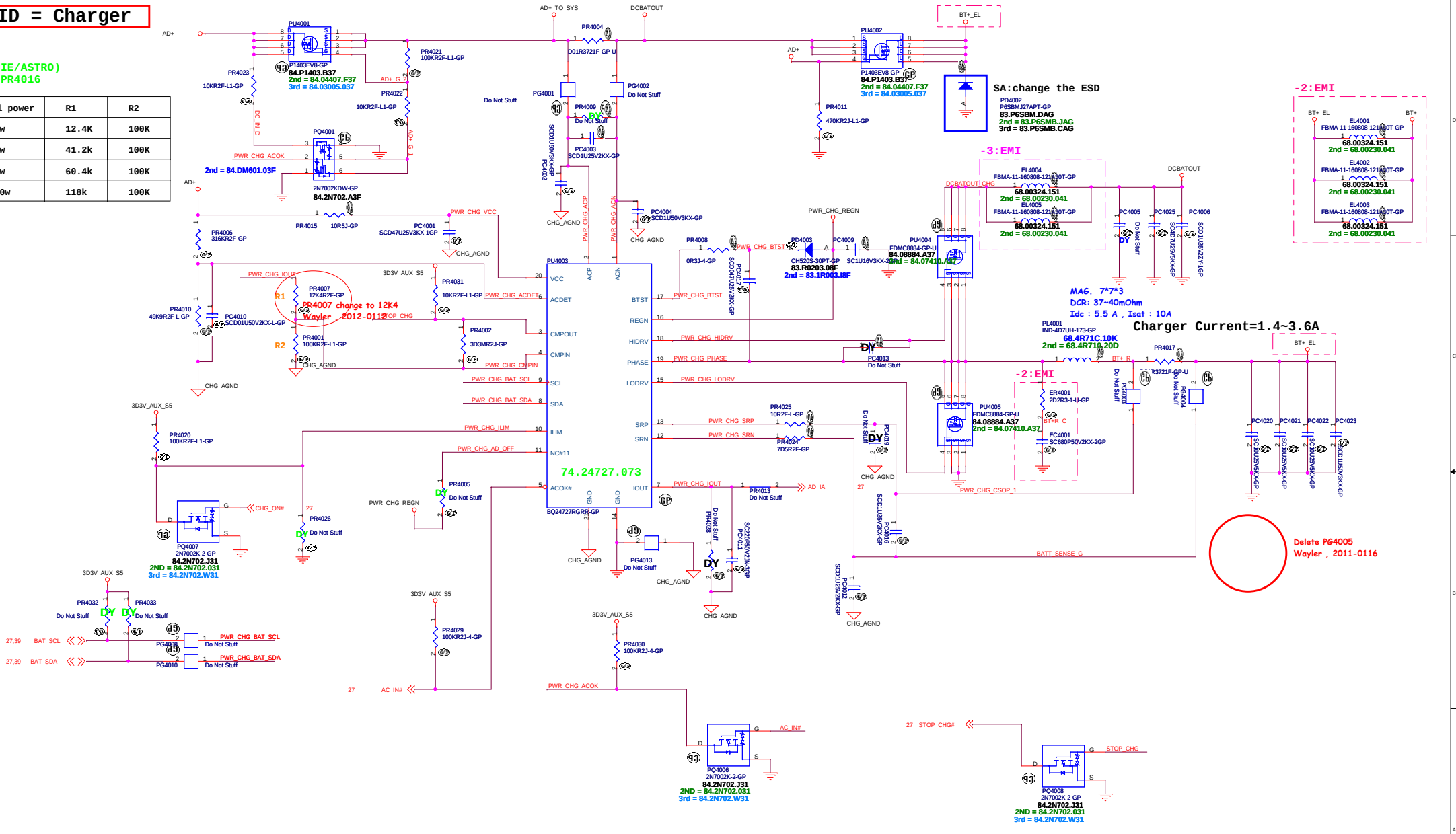
DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BATT CONN***	
Size A4	Document Number **Husk/Petra**	Rev **-4M**
Date: Thursday, September 06, 2012	Sheet 39 of 103	

SSID = Charger

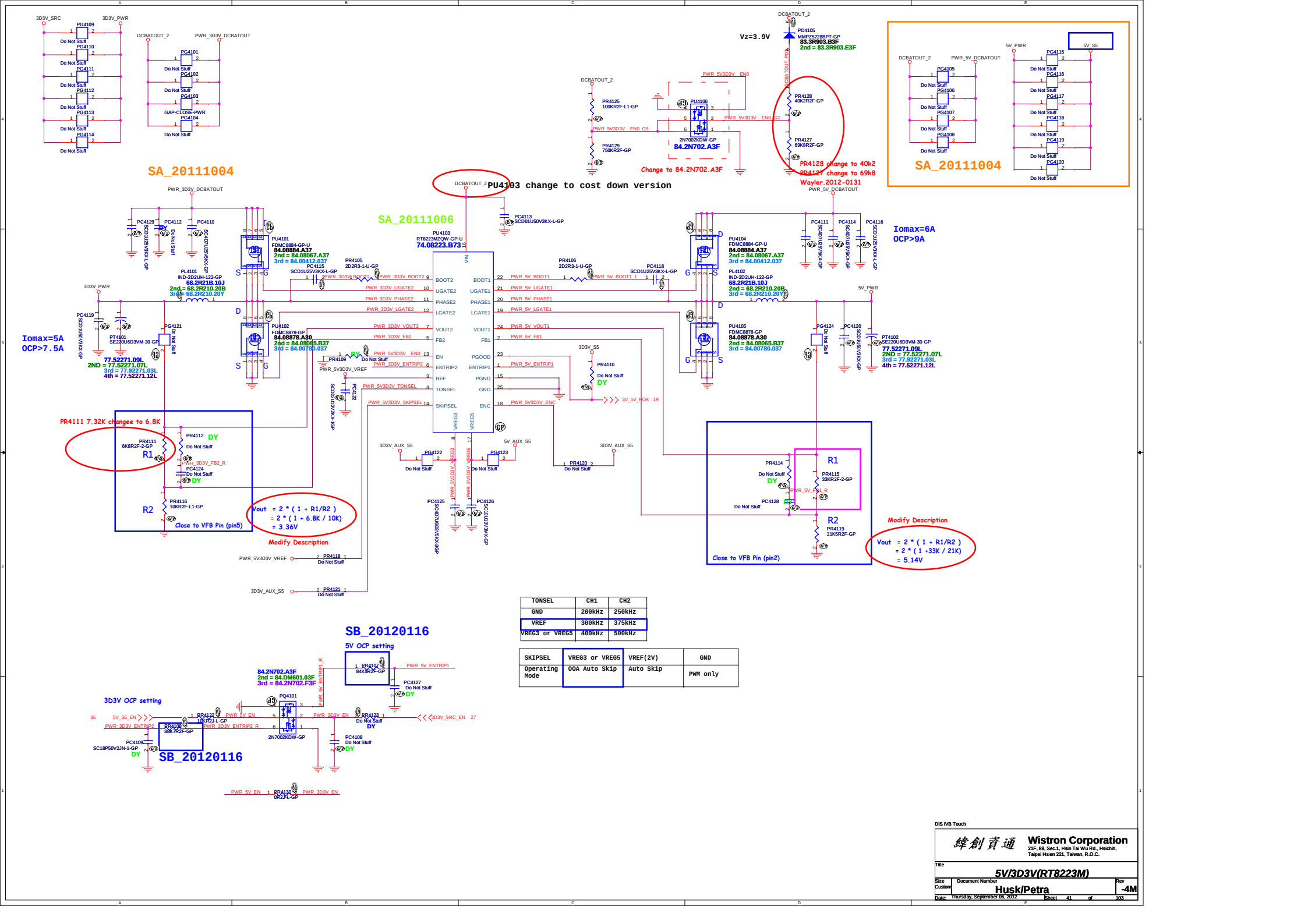
A8(ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



DIS IVB Touch

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CHARGER BQ24707A
Size: Custom	Document Number: Husk/Petra
Rev	-4M
Date: Thursday, September 06, 2012	Sheet 40 of 108



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

DIS IVB Touch

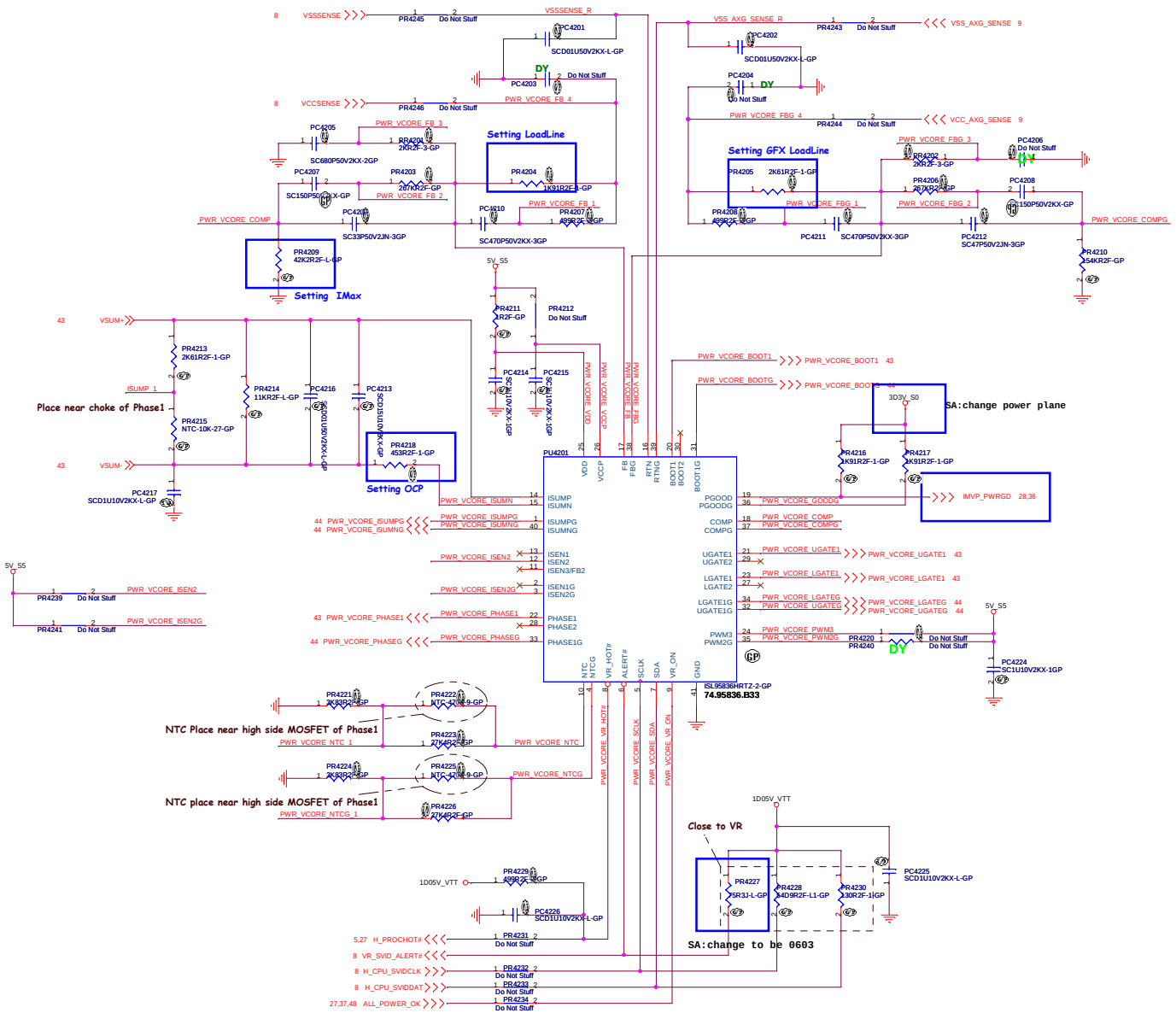
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **5V/3D3V(RT8223M)**

Size: Custom | Document Number: **Husk/Petra** | Rev: **-4M**

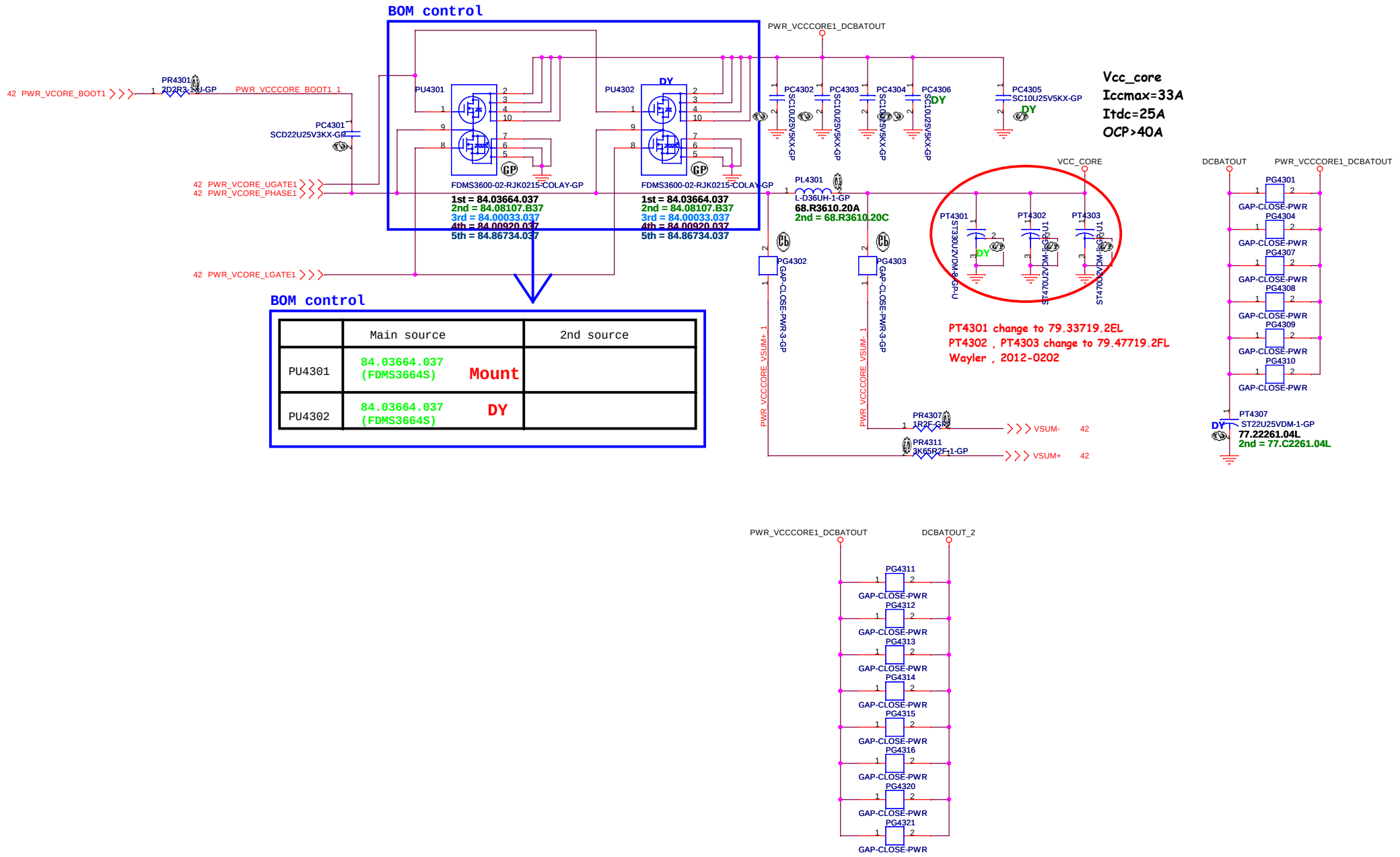
Date: Thursday, September 06, 2012 | Sheet 41 of 103

SSID = CPU.Regulator



DIS IVB Touch

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ISL95836_CPU_CORE(1/3)	
Size: Custom	Document Number: Husk/Petra	Rev: -4M
Date: Thursday, September 06, 2012	Sheet 42 of 102	



BOM control

	Main source	2nd source
PU4301	84.03664.037 (FDMS3664S) Mount	
PU4302	84.03664.037 (FDMS3664S) DY	

DIS IVB Touch

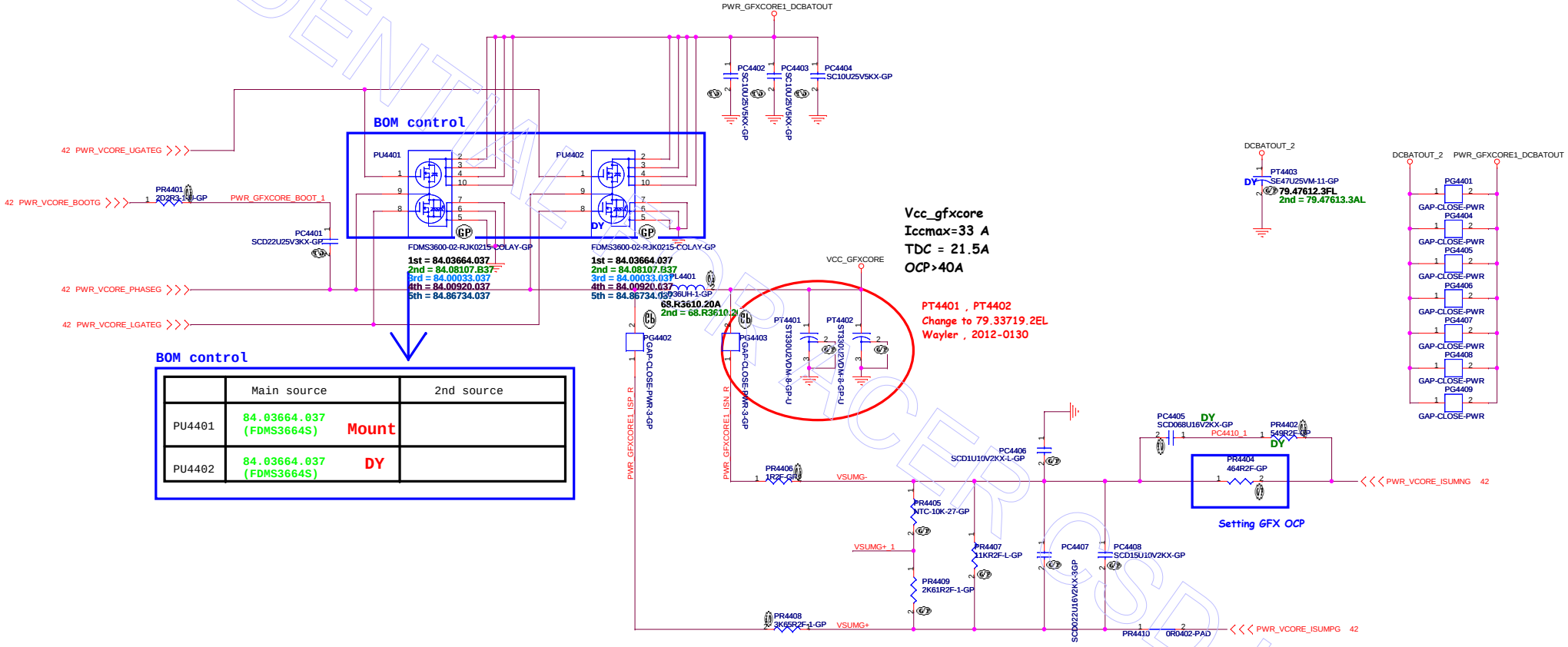
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(2/3)

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Monday, September 17, 2012 | Sheet 43 of 102

CONFIDENTIAL
WISTRON CORPORATION
FOR INTERNAL USE ONLY



	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S) Mount	
PU4402	84.03664.037 (FDMS3664S) DY	

DIS IVB Touch

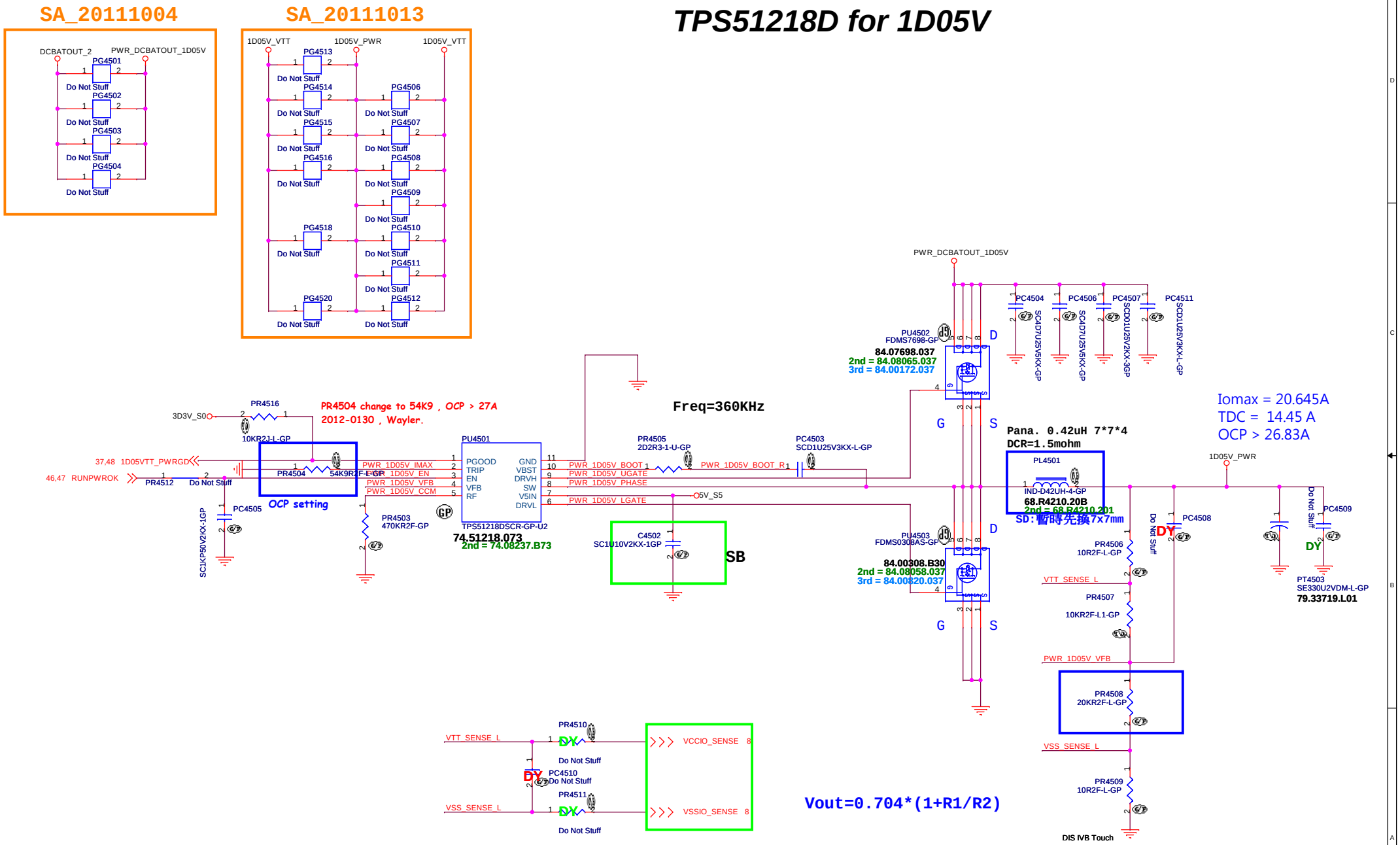
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(3/3)

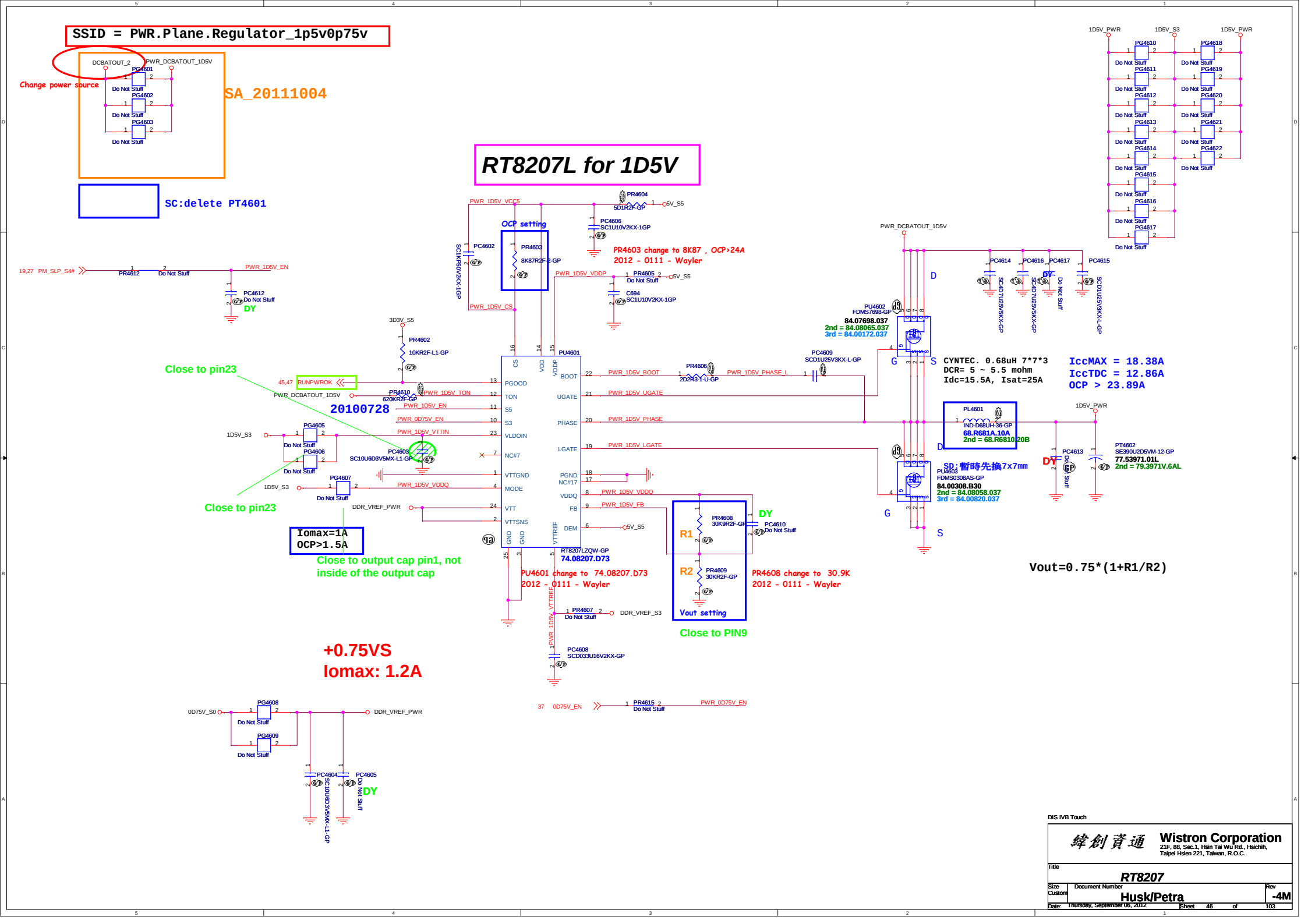
Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Monday, September 17, 2012 | Sheet 44 of 102

TPS51218D for 1D05V

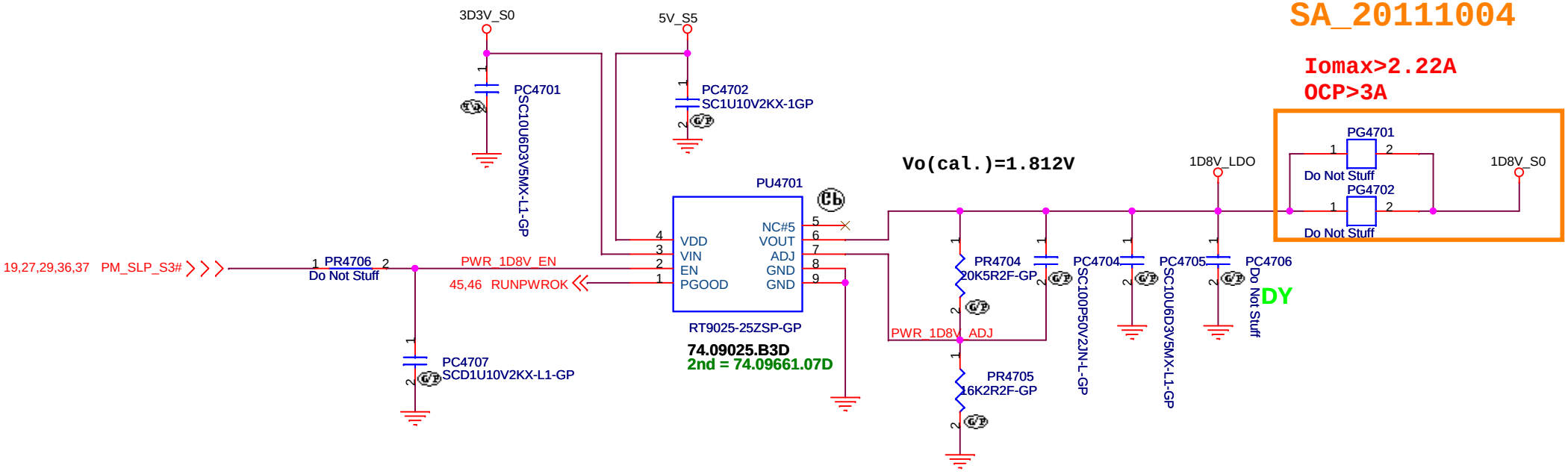


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DC to DC 1D05V(TPS51218D)
Size A3	Document Number: Husk/Petra
Rev	-4M
Date: Thursday, September 06, 2012	Sheet 45 of 103


SSID = PWR.Plane.Regulator_1p5v0p75v
Change power source
SA_20111004
SC:delete PT4601
RT8207L for 1D5V
OCP setting
PR4603 change to 8K87 , OCP>24A
2012 - 0111 - Wayler
Close to pin23
20100728
Iomax=1A
OCP>1.5A
Close to output cap pin1, not inside of the output cap
PU4601 change to 74.08207.D73
2012 - 0111 - Wayler
PR4608 change to 30.9K
2012 - 0111 - Wayler
Close to PIN9
+0.75VS
Iomax: 1.2A
CYNTEC. 0.68uH 7*7*3
DCR= 5 ~ 5.5 mohm
Idc=15.5A, Isat=25A
IccMAX = 18.38A
IccTDC = 12.86A
OCP > 23.89A
SD:暫時先換7x7mm
Vout=0.75*(1+R1/R2)
Wistron Corporation
Husk/Petra
RT8207

SSID = PWR.Plane.Regulator_1p8v

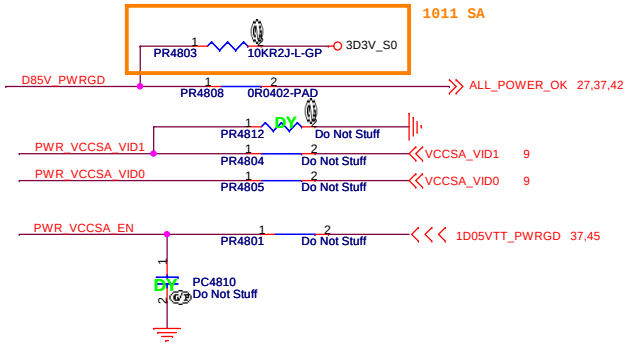
RT9025 for 1D8V_S0



DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LDO_1D8V(RT9025)***	
Size A4	Document Number **Husk/Petra**	Rev **-4M**
Date: Thursday, September 06, 2012	Sheet 47 of 103	

LDO G978 for VCCSA



D0, D1 V_O Selection Table

D0	D1	V_O MODE=0	V_O MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

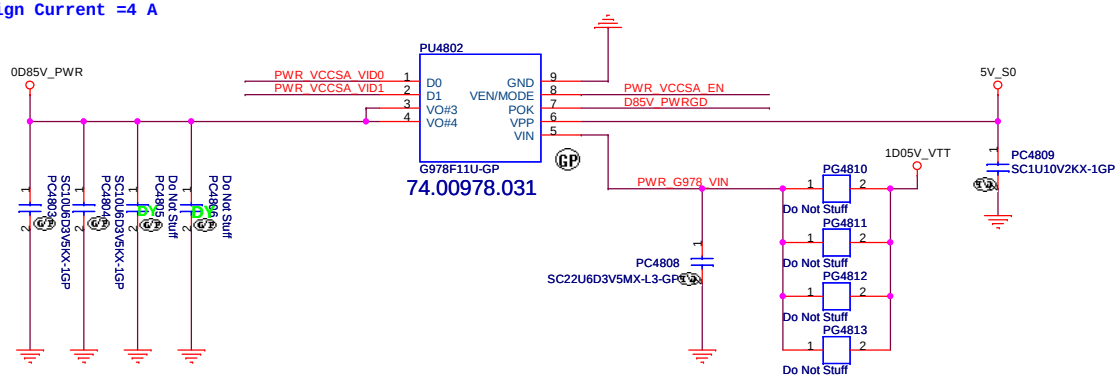
"x" means "don't care".

VEN/MODE Logic

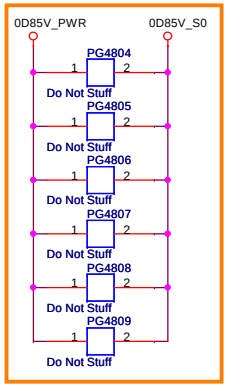
VEN/MODE (VPP=5V)	EN logic
<0.6V	0
>1.0V	1

VEN/MODE (VPP=5V)	MODE logic
<2.0V	0
>2.6V	1

Design Current =4 A



1011 SA



DIS IVB Touch

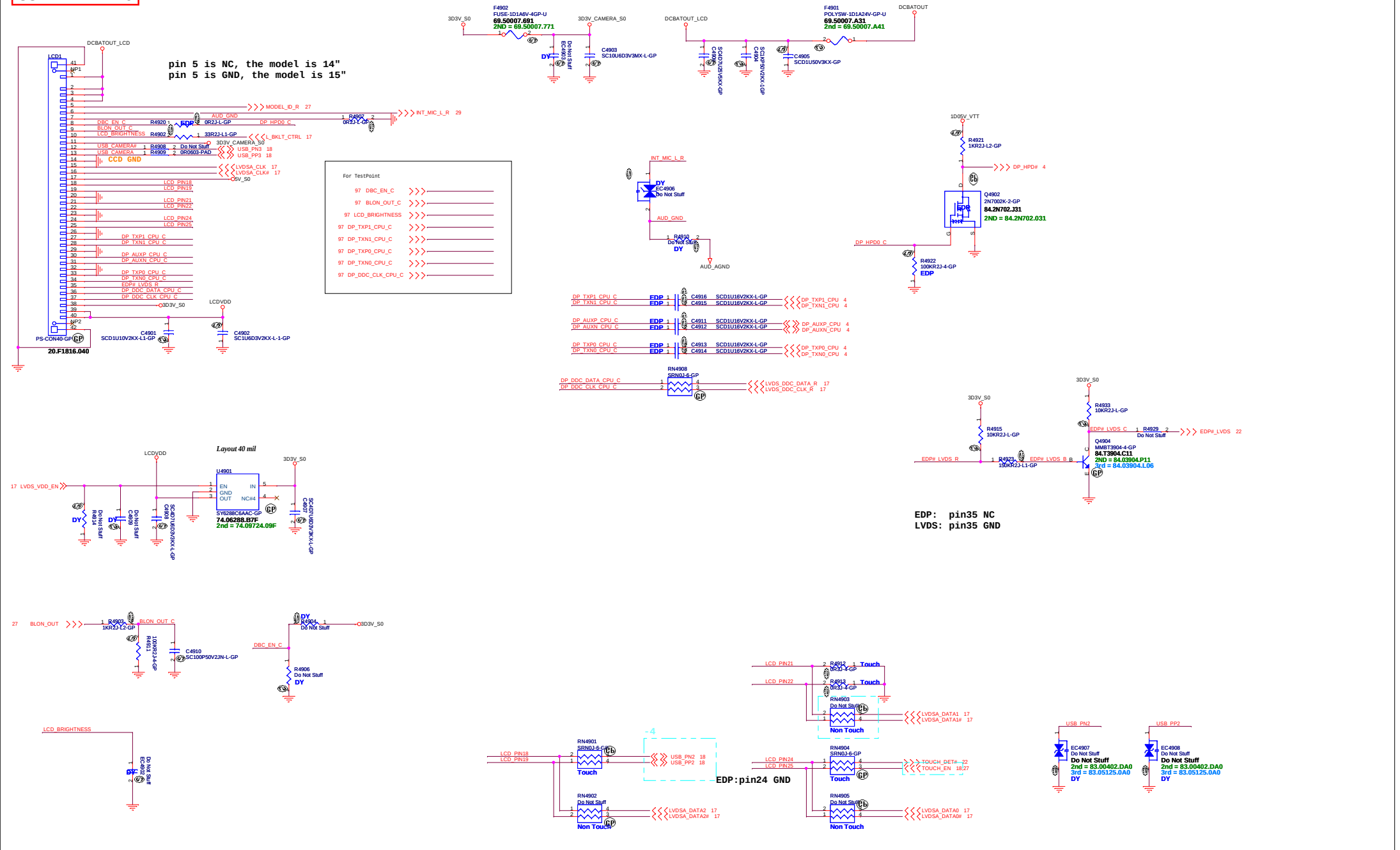
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VCCSA LDO G978

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 48 of 103

SSID = VIDEO



DIS IVB Touch

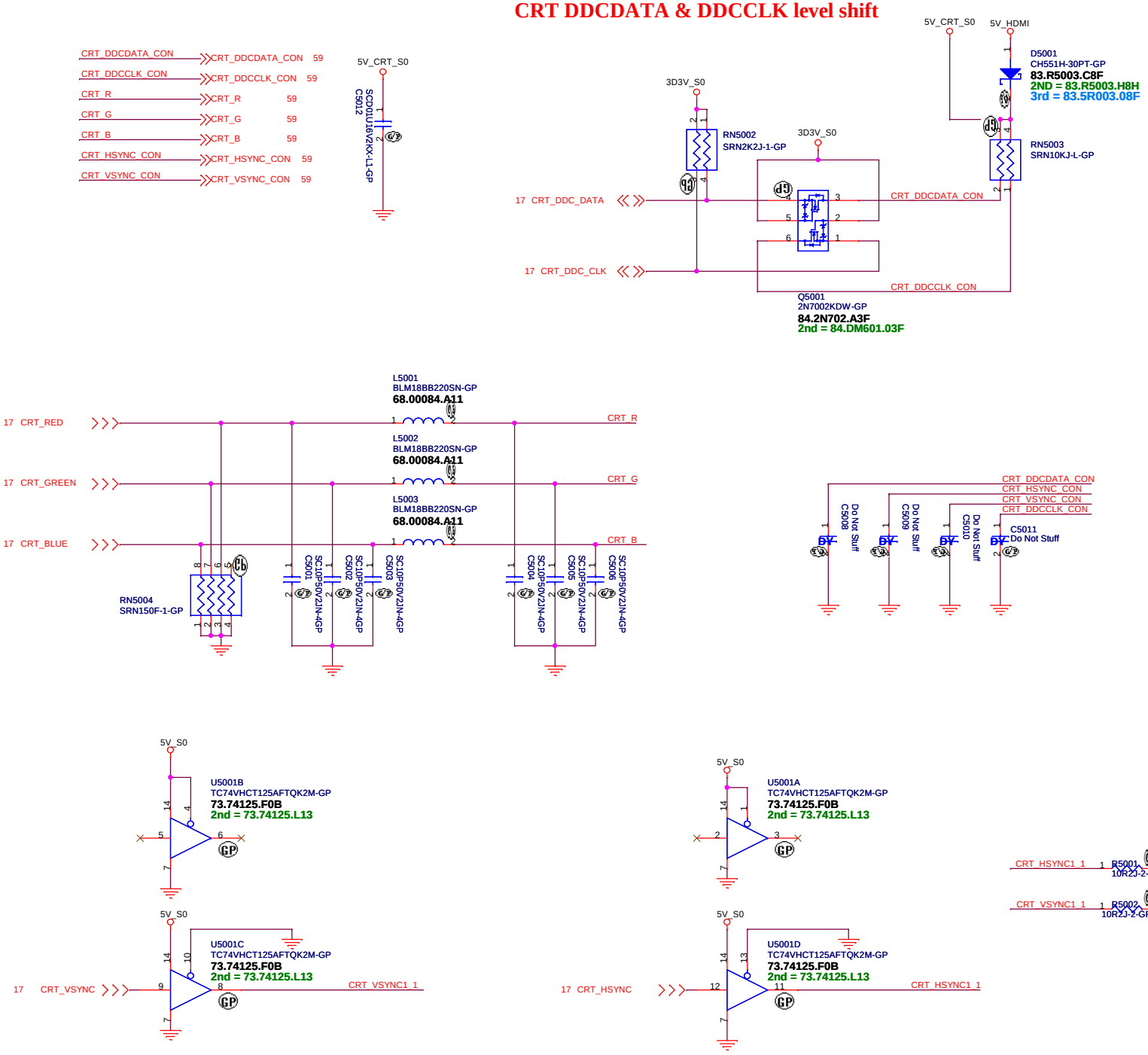
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD Connector**

Size: A2 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 49 of 103

CRT DDCDATA & DDCCLK level shift



DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

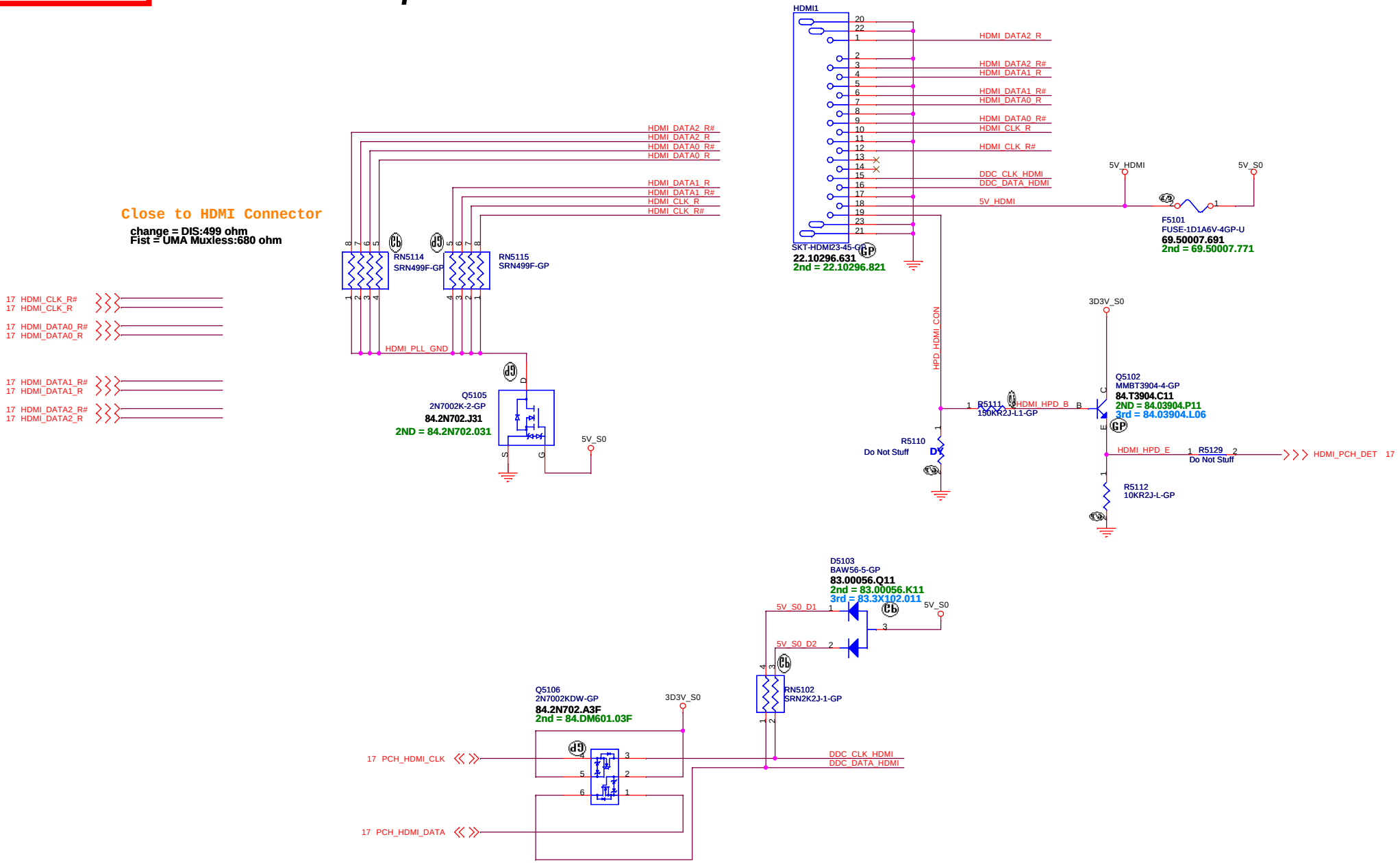
Title: ***CRT Connector***

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 50 of 103

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDMI Level Shifter/Connector***	
Size A3	Document Number **Husk/Petra**	Rev **-4M**
Date: Thursday, September 06, 2012	Sheet 51 of 103	

LED BACKLIGHT CONVERTER POWER

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: eDP

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 52 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **S-VIDEO**

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 53 of 103

(Blanking)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

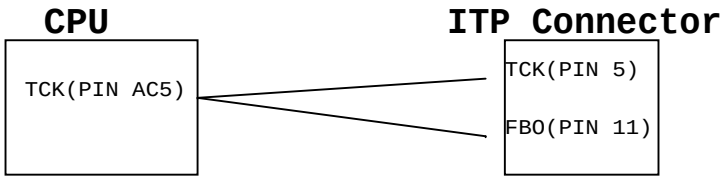
Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.



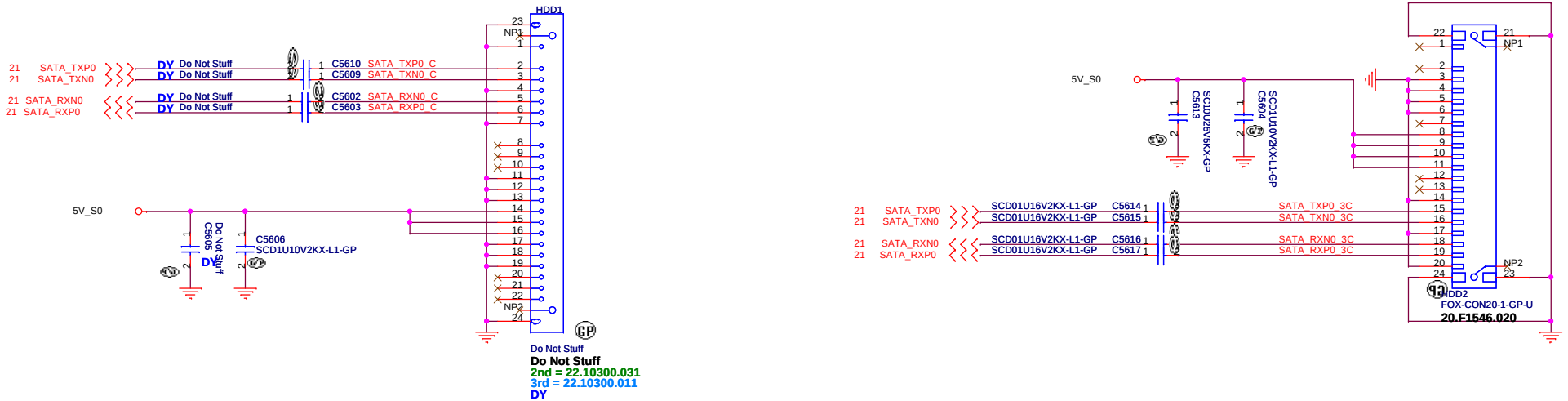
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*ITP*	
Size A4	Document Number **Husk/Petra**	Rev **-4M**
Date: Thursday, September 06, 2012	Sheet 55 of 103	

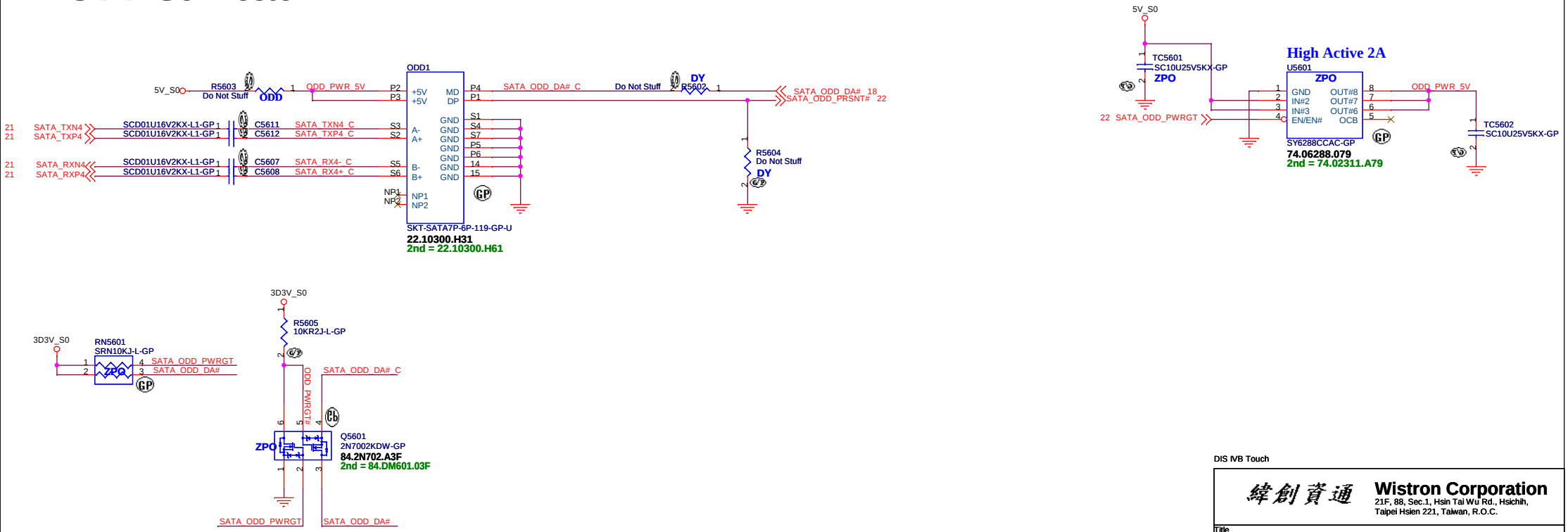
SSID = SATA

SATA HDD Connector



ODD Connector

SATA Zero Power ODD



DIS IVB Touch

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD/ODD	
Size A3	Document Number Husk/Petra	Rev -4M
Date: Thursday, September 06, 2012	Sheet 56 of 103	

DIS IVB Touch

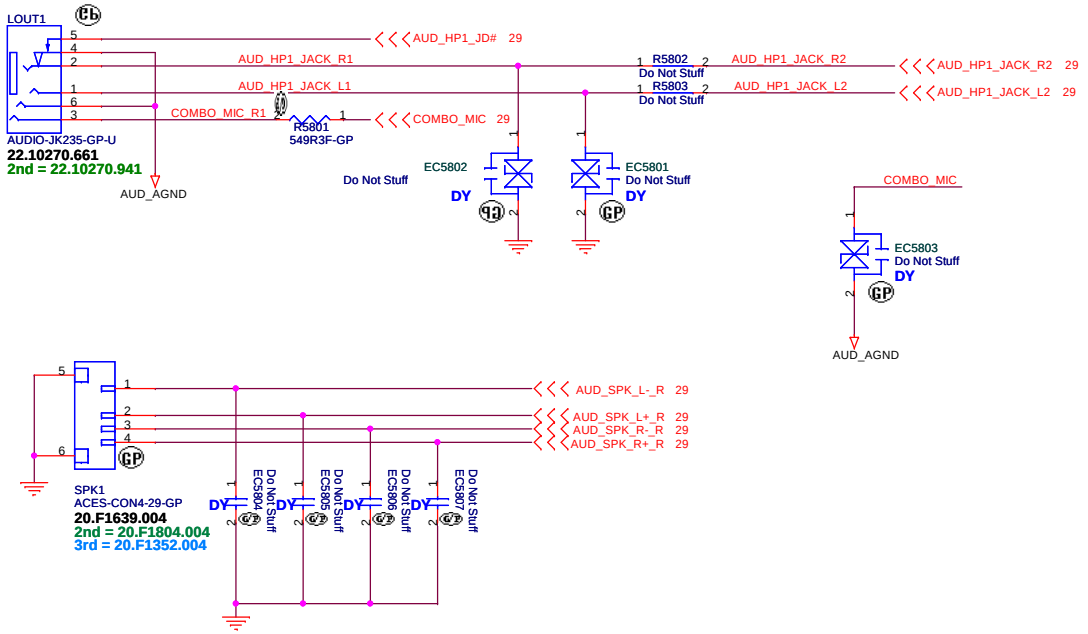
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *E-SATA/USB CHARGER*

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 57 of 103

SSID = AUDIO



DIS IVB Touch

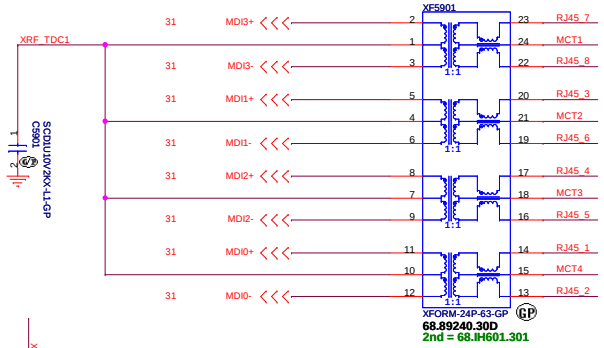
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

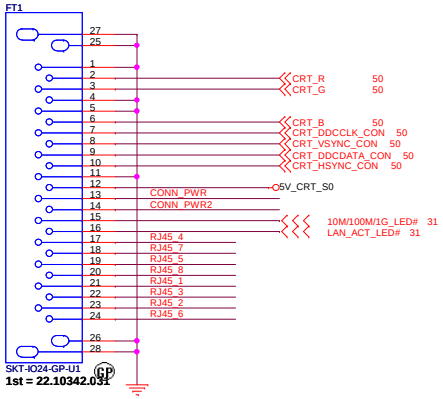
Title: ***Audio Jack***

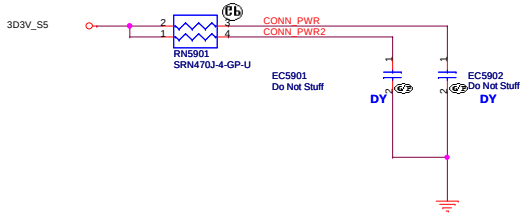
Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

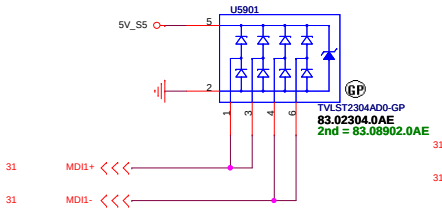
Date: Thursday, September 06, 2012 Sheet 58 of 103

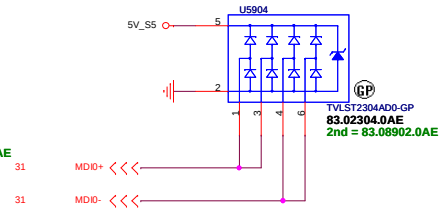
SSID = LAN

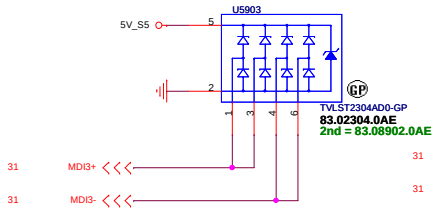


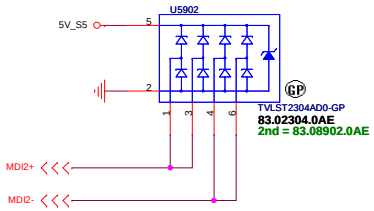


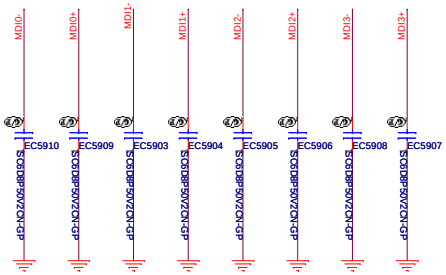


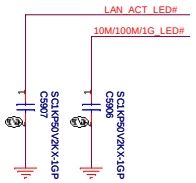


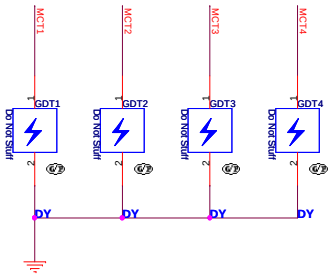


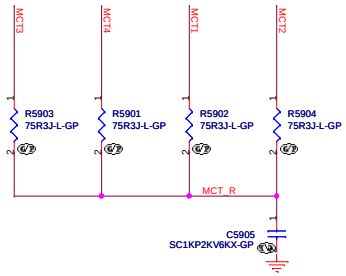












DIS IVB Touch

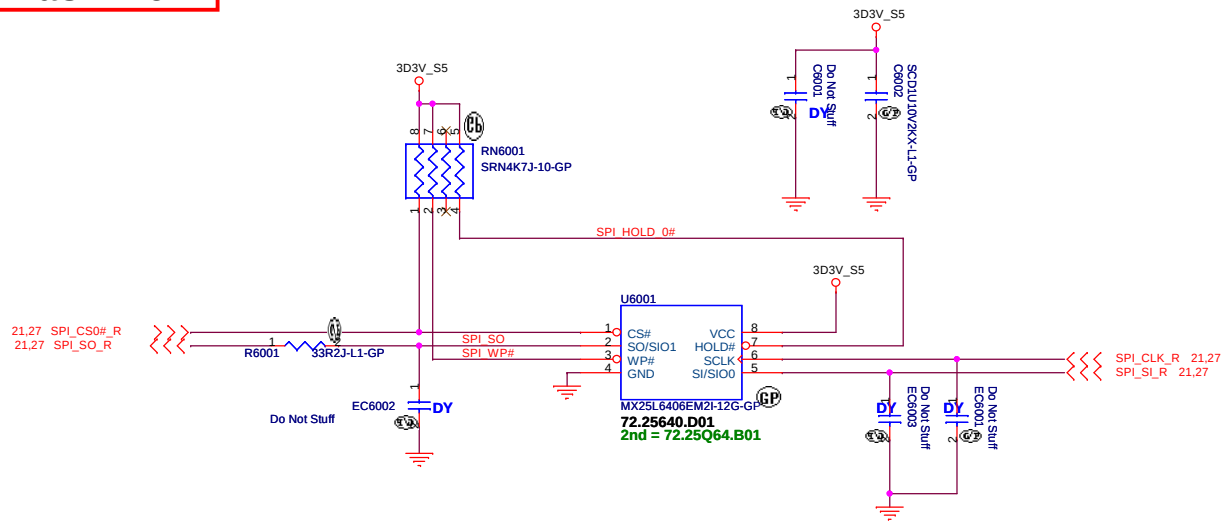
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONNECTOR**

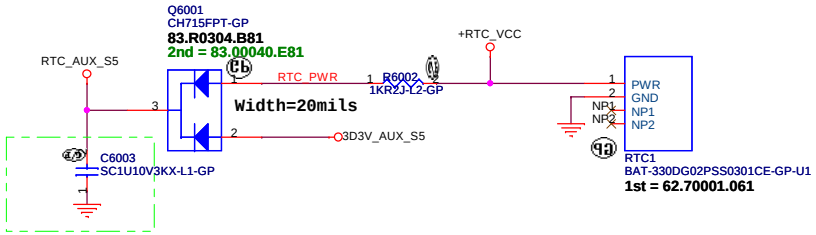
Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Monday, November 12, 2012 Sheet 59 of 103

SSID = Flash.ROM



SSID = RTC



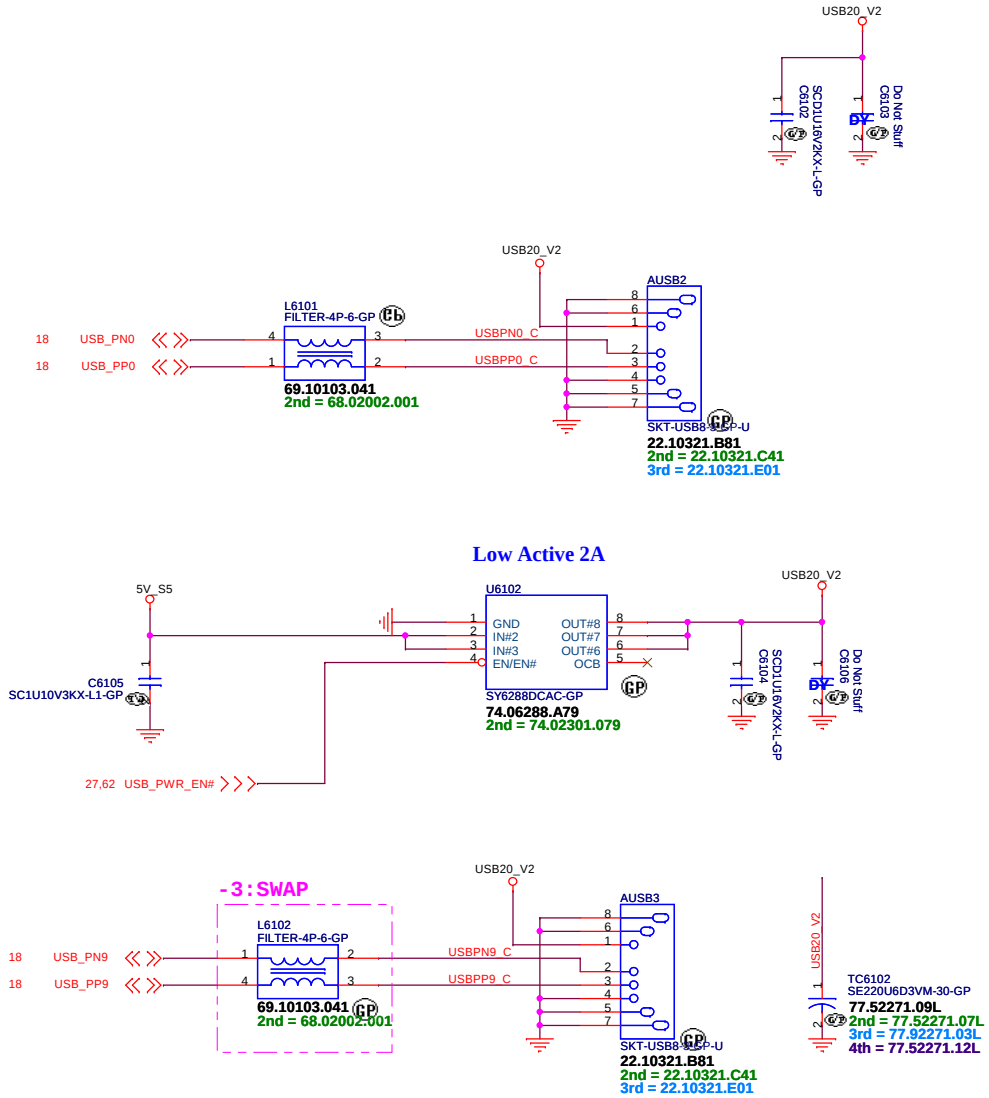
-4M_20120806

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Flash/RTC*	
Size: Custom	Document Number: **Husk/Petra**	Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 60 of 103	

SSID = USB



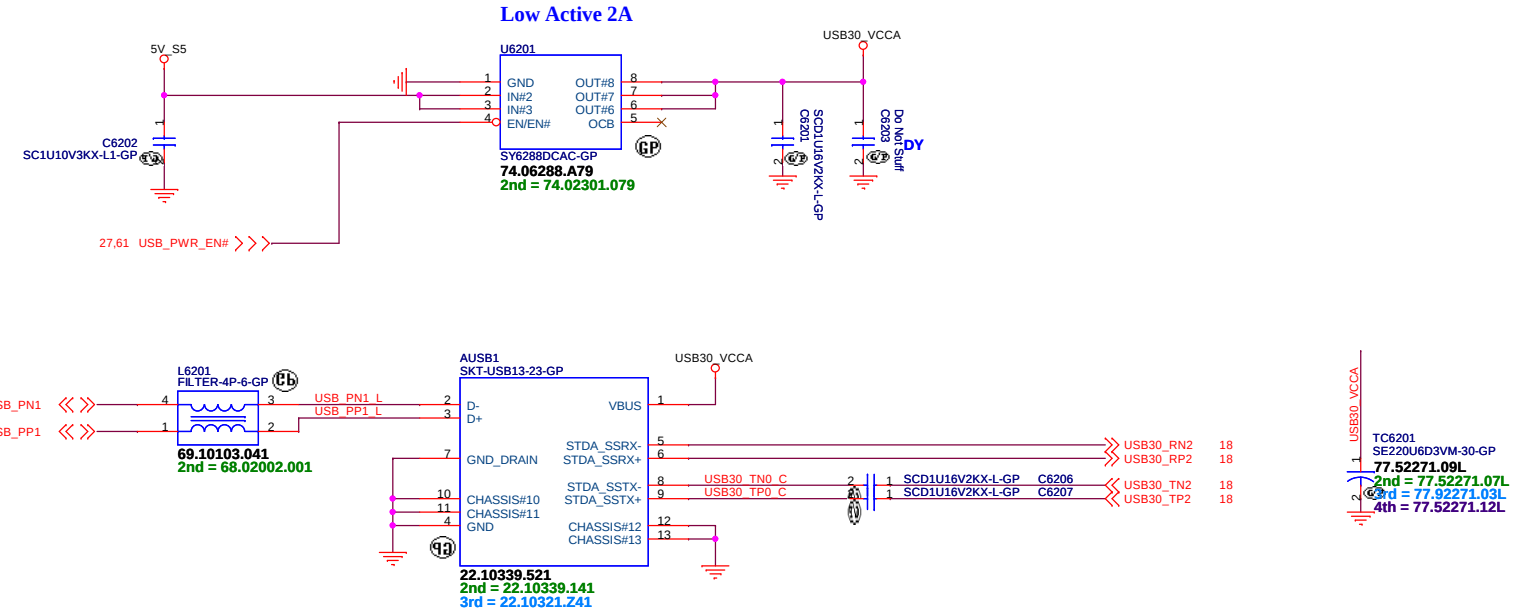
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

Date: Thursday, September 13, 2012 Sheet 61 of 103



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 3.0 Port**

Size: A3 | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 13, 2012 | Sheet 62 of 103

SSID = User.Interface

Bluetooth Module conn.

ANNIE Bluetooth Module

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Bluetooth***	
Size A4	Document Number **Husk/Petra**	Rev **-4M**
Date: Thursday, September 06, 2012	Sheet 63 of 103	

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

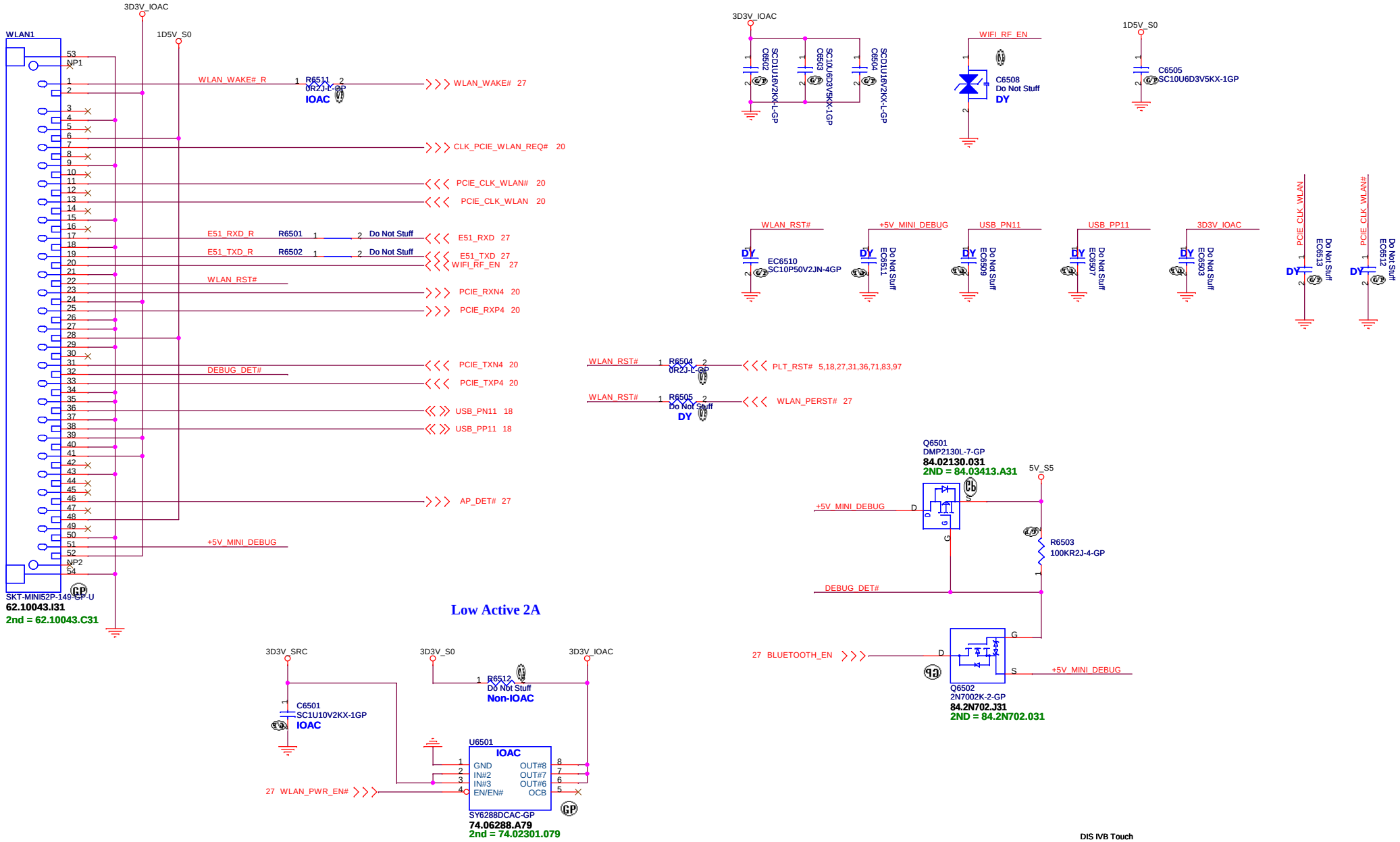
RESERVED

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 64 of 103

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MINICARD(WLAN)/ITP CONN***
Size A3	Document Number **Husk/Petra** Rev **-4M**
Date: Friday, December 21, 2012	Sheet 65 of 103

SSID = Wireless

Mini Card Connector(WWAN)

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 66 of 103

(Blanking)

DIS IVB Touch

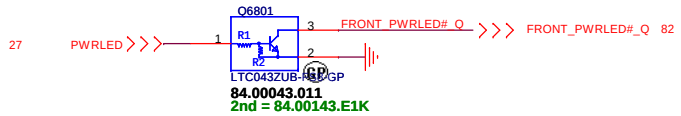
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

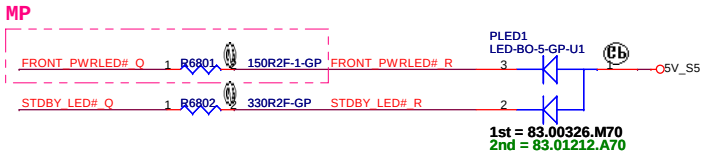
Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

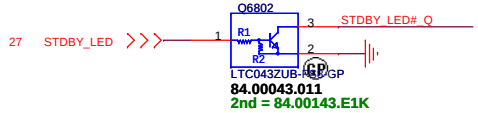
Date: Thursday, September 06, 2012 Sheet 67 of 103

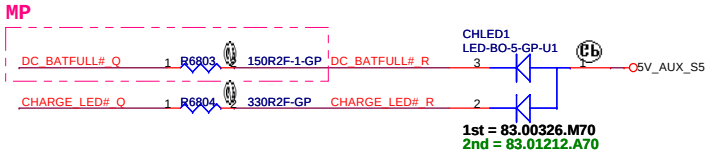
Power button LED



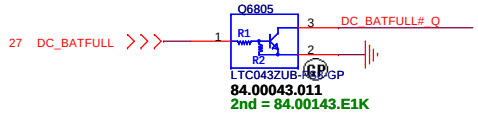


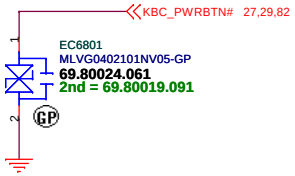
Power STDBY_LED



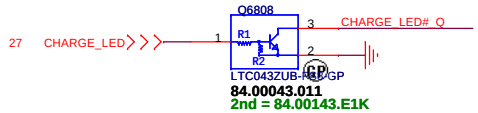


Battery LED2(DC_BATFULL)





Battery LED1(CHARGE)



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

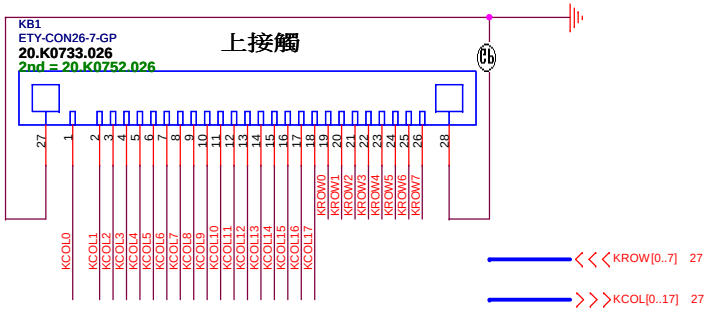
Title: *LED Bard/Power Button*

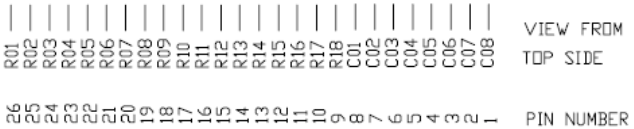
Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 68 of 103

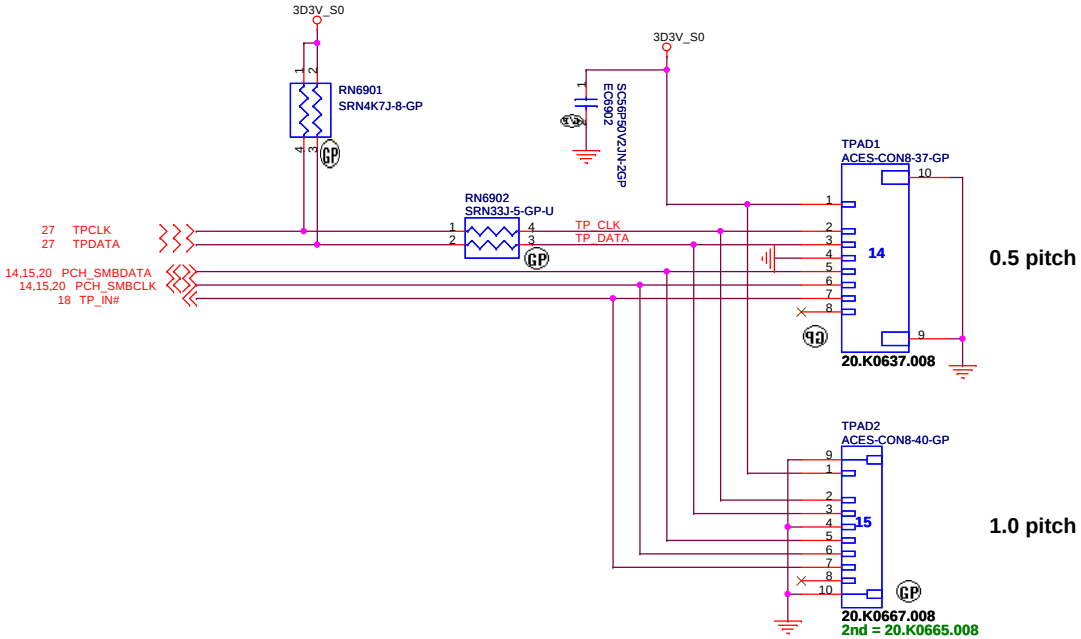
SSID = KBC

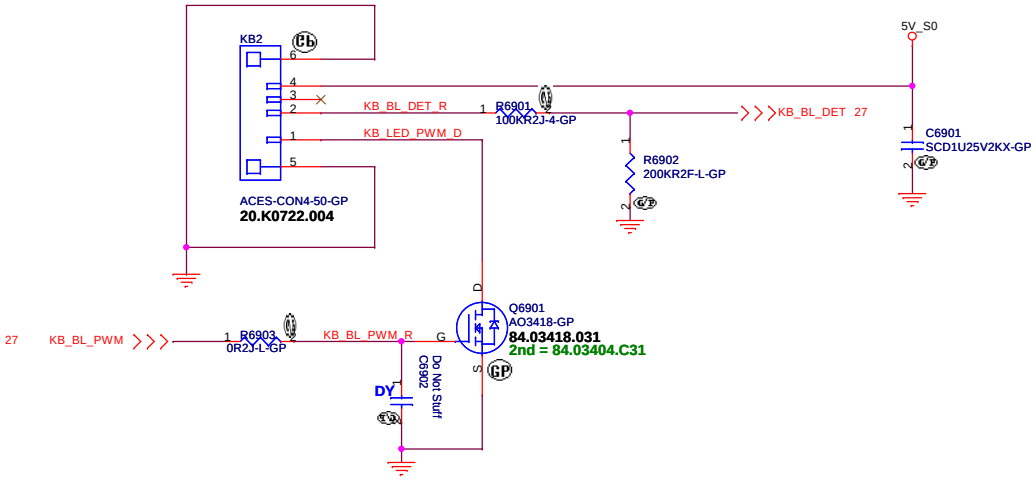
Internal KeyBoard Connector





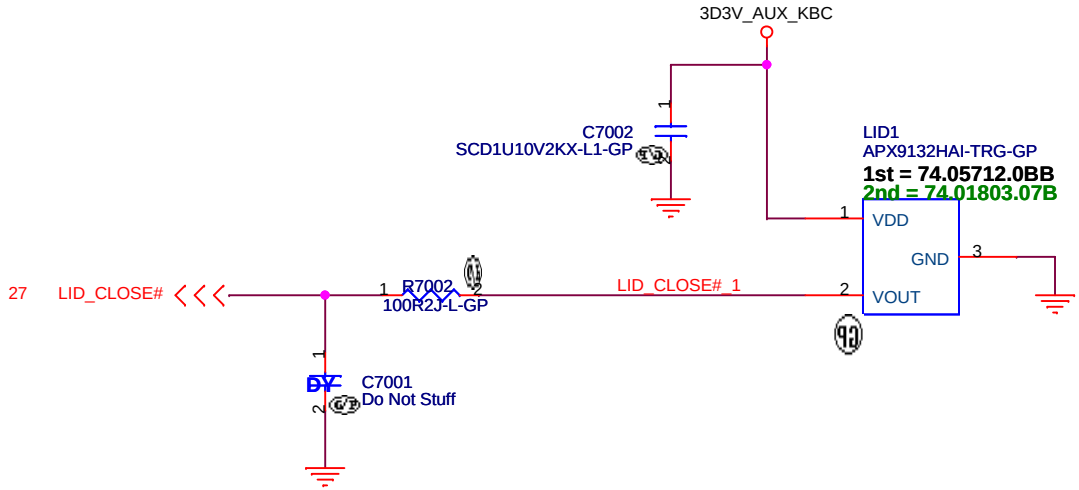
TOUCH PAD





DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Key Board/Touch Pad***
Size A3	Document Number **Husk/Petra** Rev **-4M**
Date: Thursday, September 06, 2012	Sheet 69 of 103



DIS IVB Touch

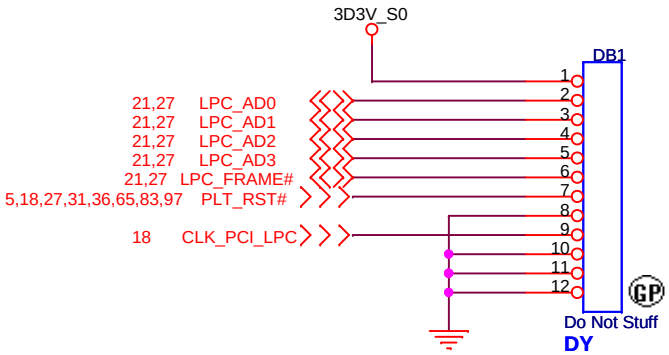
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size	Document Number	Rev
A4	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 70 of 103



DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Dubug connector

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 71 of 103

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DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 72 of 103

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DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

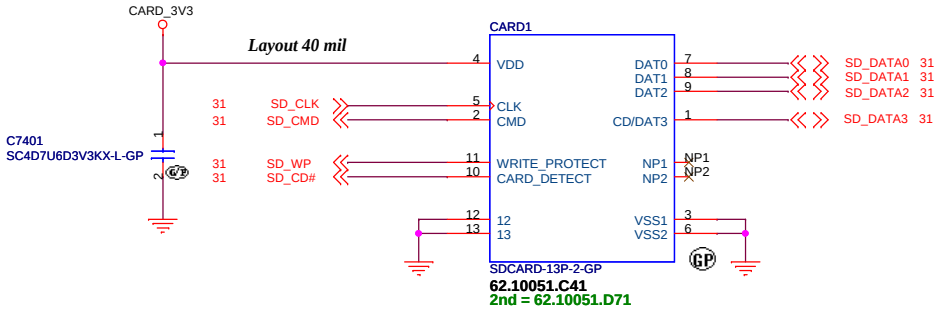
Title: ***Reserved***

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 73 of 103

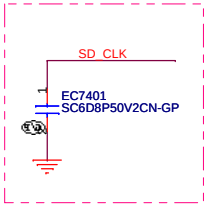
SSID = SDIO

SD/MMC Card Reader



SP1	SP1	SD_D7		xD_RDY
SP2	SP2	SD_D6	MS_INS#	xD_RE#
SP3	SP3	SD_D5		xD_CE#
SP4	SP4	SD_D4		xD_WE#
SP5	SP5	SD_D1	MS_CLK	xD_D6
SP6	SP6	SD_D0	MS_D7	xD_D5
SP7	SP7	SD_CLK	MS_D3	xD_D4
SP8	SP8	SD_CMD	MS_D6	xD_D3
SP9	SP9	SD_D3	MS_D2	xD_D2
SP10	SP10	SD_D2		xD_D7
SP11	SP11		MS_BS	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14		MS_D4	xD_D0
SP15	SP15		MS_D0	xD_D1
SP16	SP16			xD_CD#

-2:EMI



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size: Custom | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2012 | Sheet 74 of 103

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card

Size	Document Number	Rev
A3	Husk/Petra	-4M

Date: Thursday, September 06, 2012 Sheet 75 of 103

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DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 76 of 103

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DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 77 of 103

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DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 78 of 103

SSID = User.Interface

Free Fall Sensor

```
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can
```

DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G- Sensor	
Size A4	Document Number Husk/Petra	Rev -4M
Date: Thursday, September 06, 2012	Sheet 79 of 103	

DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 80 of 103

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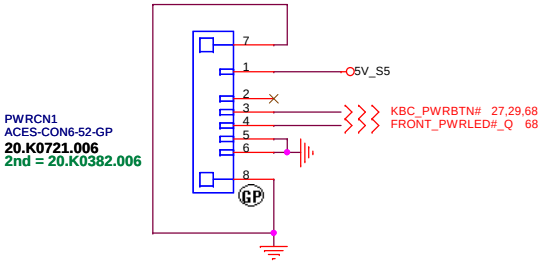
DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 81 of 103



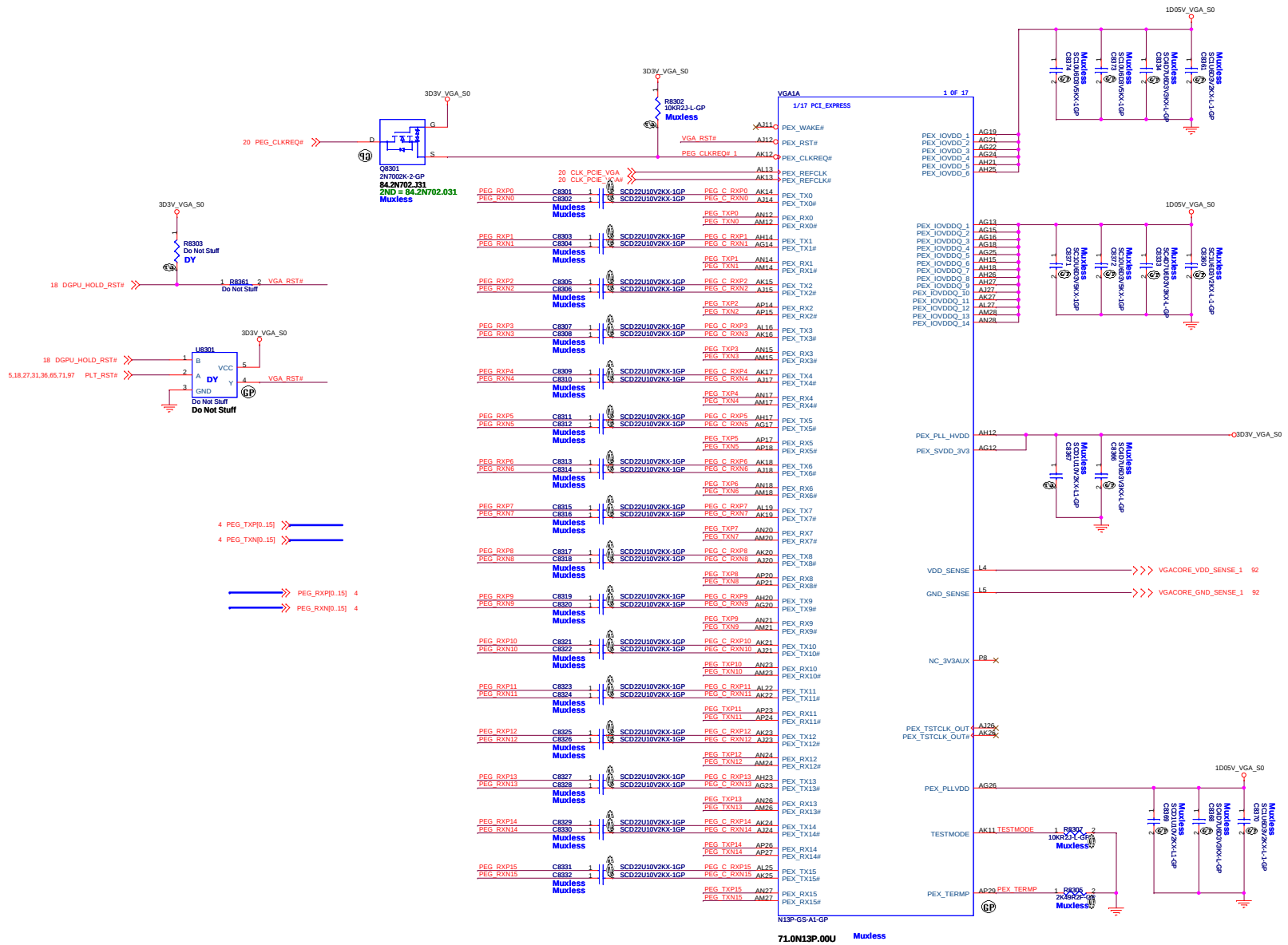
DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

Date: Thursday, September 06, 2012 Sheet 82 of 103



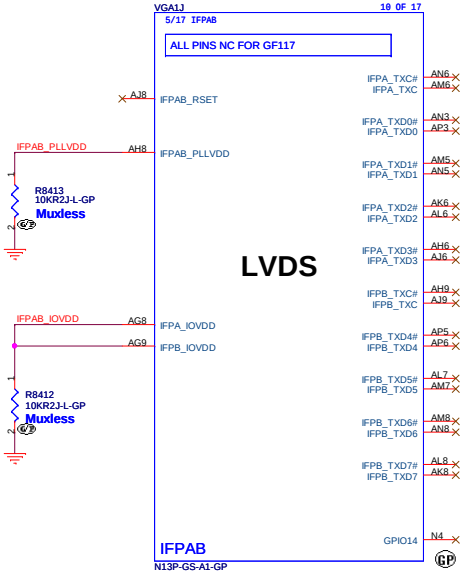
DIS IVB Touch

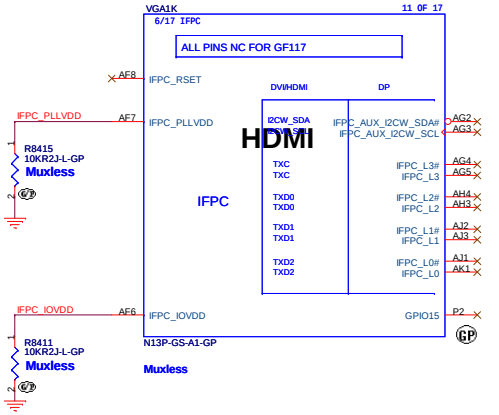
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

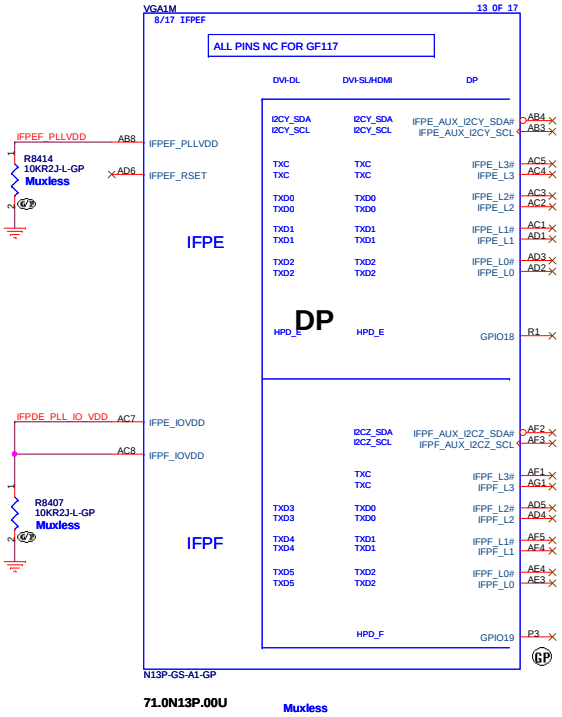
Title: **GPU_PCIE/STRAPPING(1/5)**

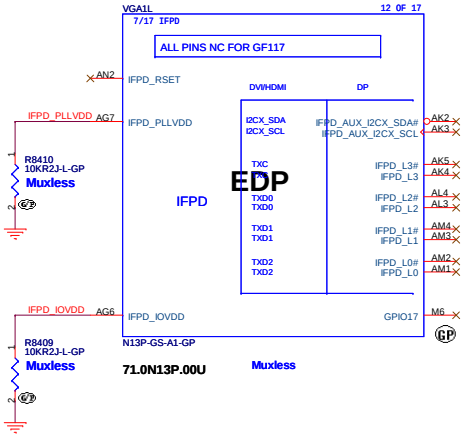
Size: A2 | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 83 of 103



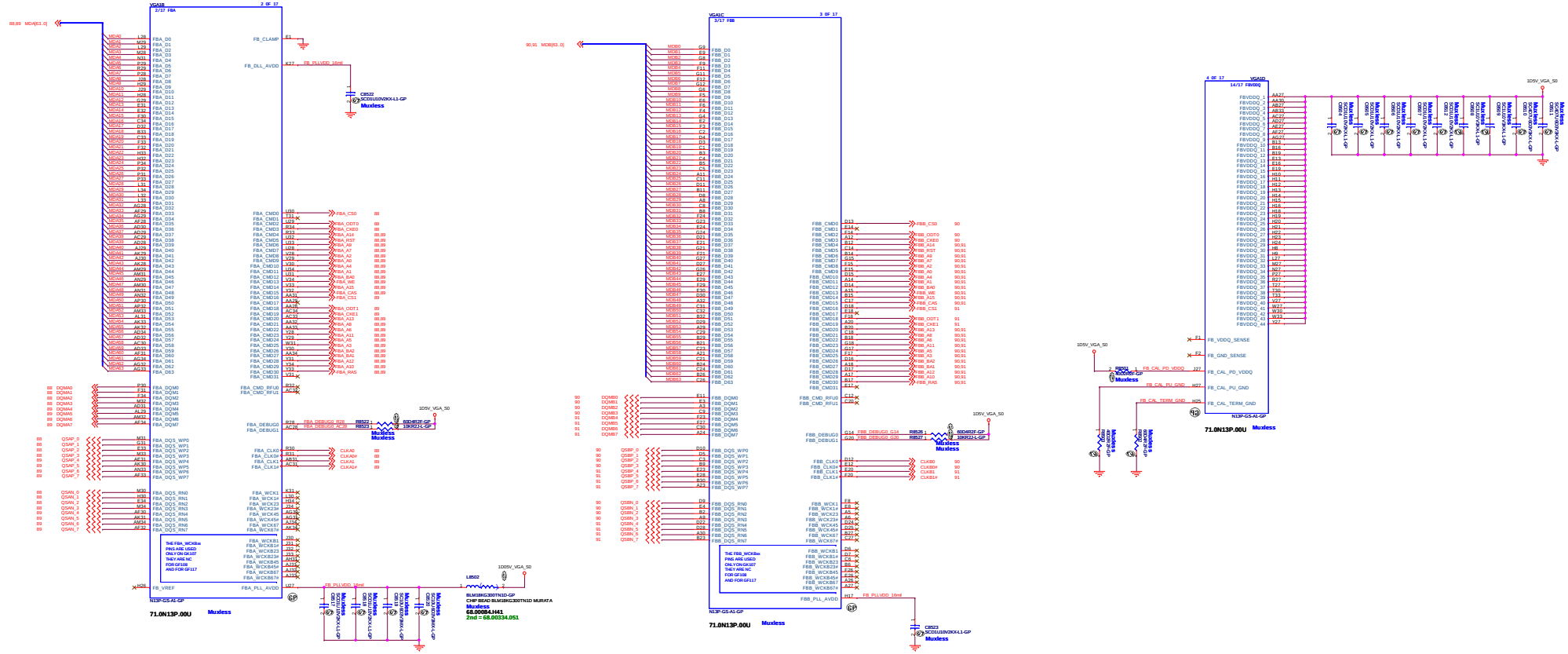






DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU Memory(2/5)***	
Size: Custom	Document Number: **Husk/Petra**	Rev: **-4M**
Date: Thursday, September 06, 2012	Sheet 84 of 103	



FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

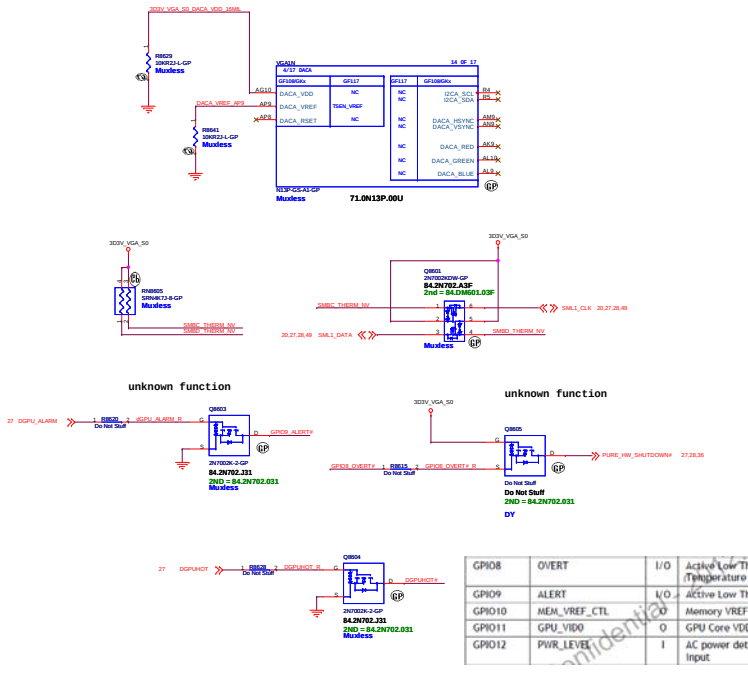
DIS M/B Touch

Wistron Corporation
2Fl., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

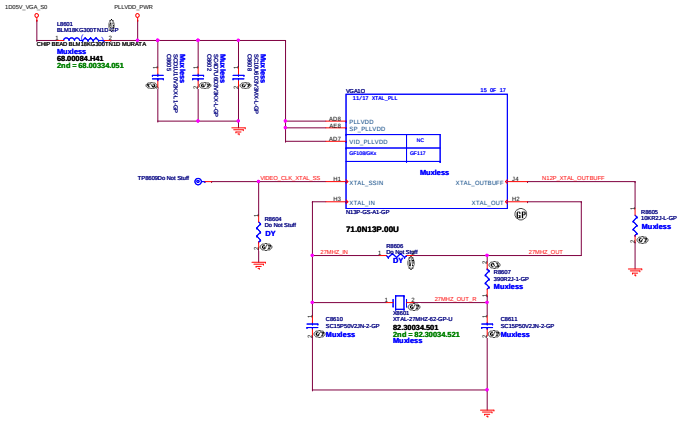
GPU_DP/LVDS/CRT/GPIO(3/5)

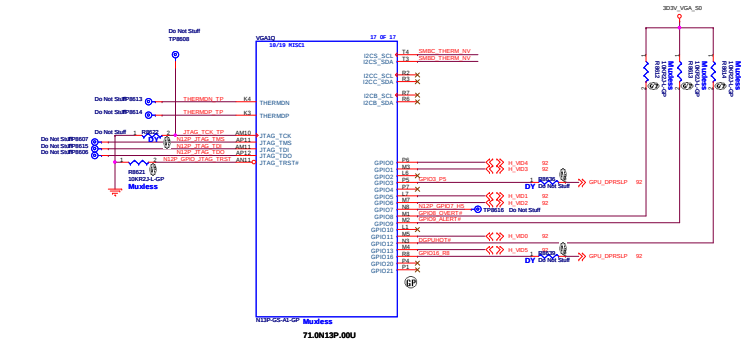
Size: A1 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, September 06, 2007 | Sheet 35 of 109



GPI08	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPI09	ALERT	I/O	Active Low Thermal Alert
GPI010	MEM_VREF_CTL	O	Memory VREF Control
GPI011	GPU_VID0	O	GPU Core VDD VID0
GPI012	PWR_LEVEL	I	AC power detect or power supply overdraw input





VRAM Table(N13P-GS/GT/LP/GL/GLP/NS/GE)

	Hynix 2G_B-Die 0110(0x6) 128*16	Hynix 1G_D-die 0010(0x2) 64*16	Samsung 2G_C-Die 0111(0x7) 128*16	Samsung 1G_G-die 0011(0x3) 64*16
ROM_SI R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	45Kohm 64.45325.6DL	20Kohm 64.20025.6DL

5Kohm
64.49915.6DL

10Kohm
64.10025.L0L

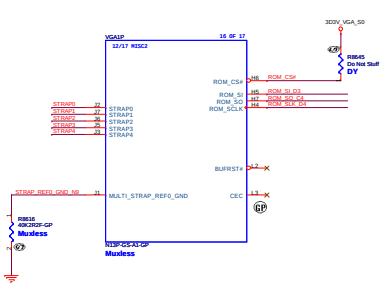
VRAM Table(N13M-GS/NS)

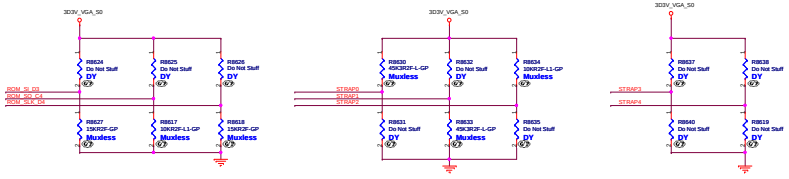
Hynix 2G_D-die 1100(0xC) 128*16	Hynix 2G_B-die 0110(0x6) 128*16

Mode	Product	NVCLK (MHz)	MCLK (MHz)	NVVDD (V)
MAX Point (MP)	N13P-GL/-NS1	800	900	--
	N13P-GLP	660	900	--
TDP Point (TP)	N13P-GL/-NS1	660	900	--
	N13P-GLP	475	900	--
HW Boot Voltage	N13P-GL/-NS1	--	--	0.95
	N13P-GLP	--	--	0.90

```
Logical Strap Bit Mapping
Resistor  Pull-up Pull-down
 5Kohms   1000    0000
10Kohms   1001    0001
15Kohms   1010    0010
20Kohms   1011    0011
25Kohms   1100    0100
30Kohms   1101    0101
35Kohms   1110    0110
45Kohms   1111    0111
```

Strap Pin Nmae	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/	PEX_PLL_EN_TERM	
	0	0	1	0	15K ohm pull-down
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	
	0	0	0	1	10K ohm pull-down
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	
	1	1	1	1	45K ohm pull-up
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
	0	1	1	1	45K ohm pull-down
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	
	1	0	0	1	10K ohm pull-up
STRAP3	N/A	N/A	N/A	N/A	
STRAP4	N/A	N/A	N/A	N/A	





DIS MB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin-Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size: A1 | Document Number: Husk/Petra | Rev: -4M

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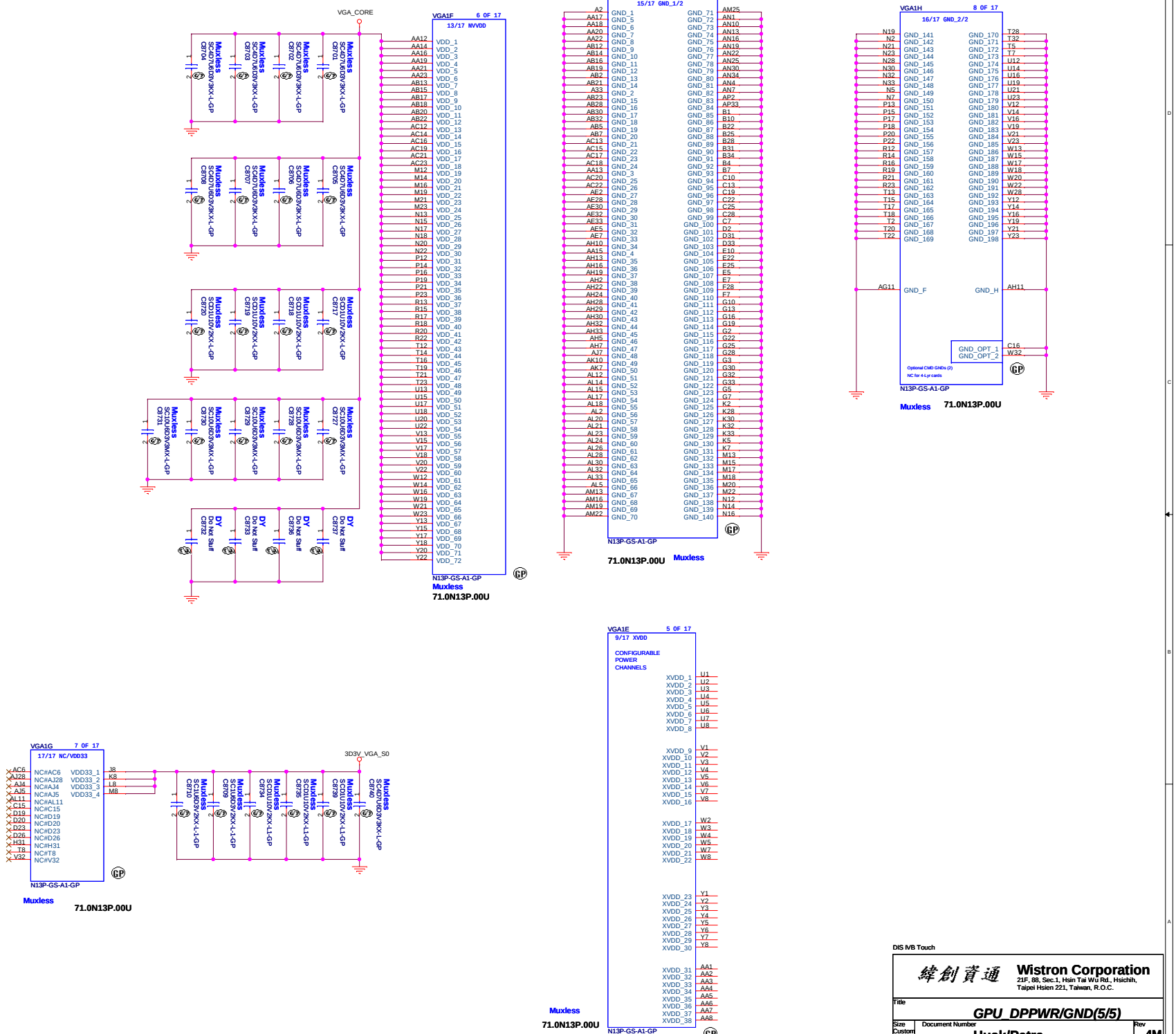

DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU_DPPWR/GND(5/5)***
Size: Custom	Document Number: **Husk/Petra**
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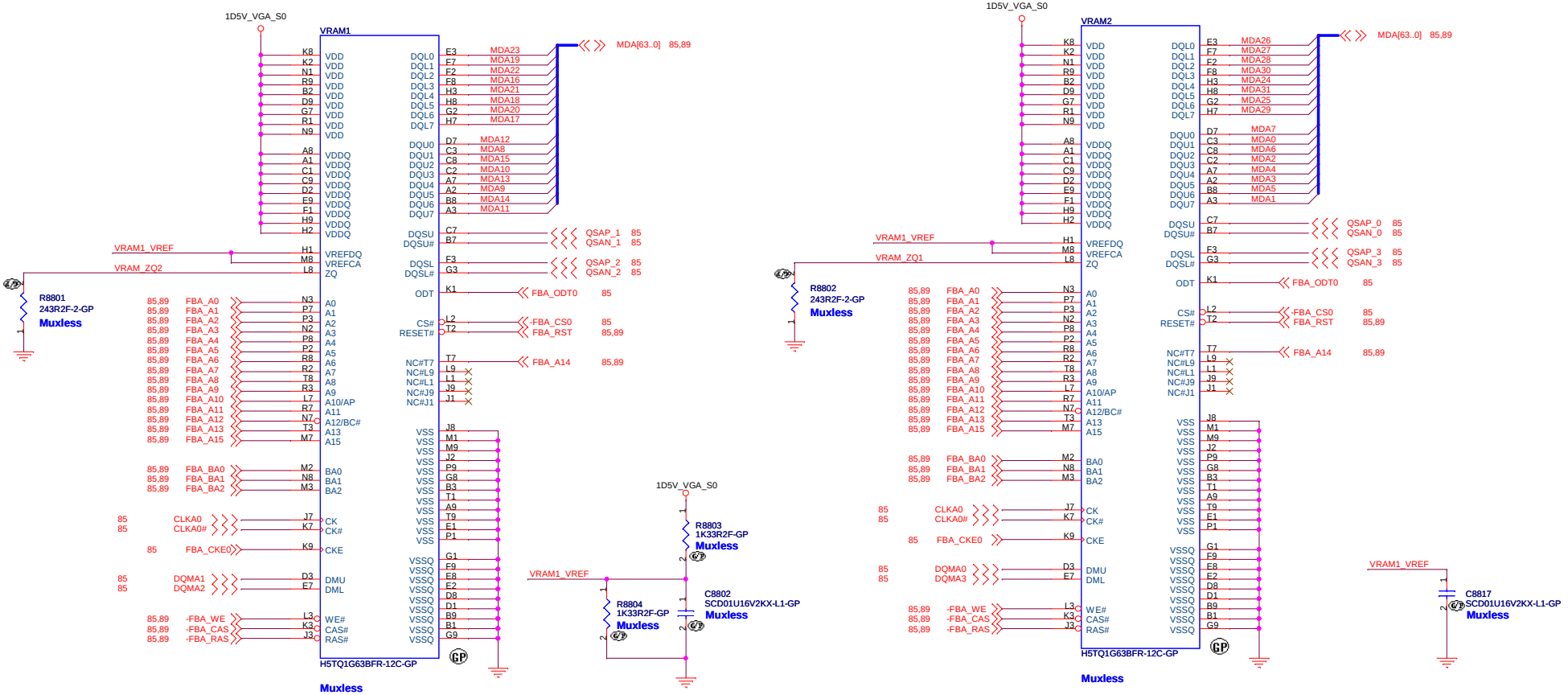
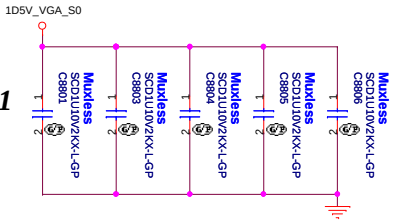
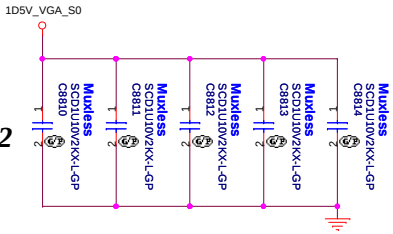
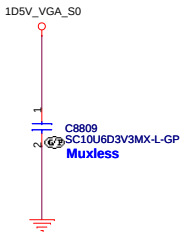


FOR VRAM1



FOR VRAM2





DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM1,2 (1/4)**

Size: Custom | Document Number: **Husk/Petra** | Rev: **-4M**

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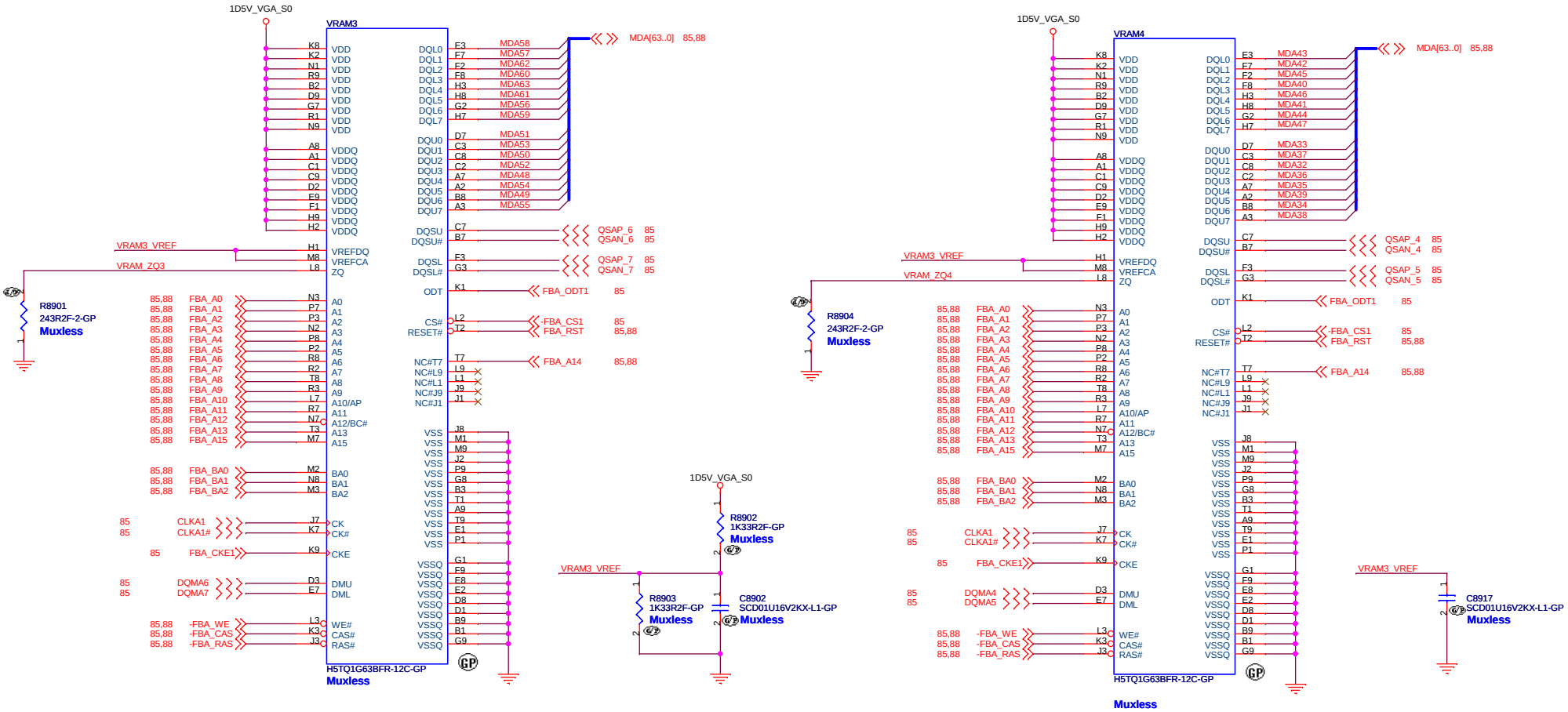
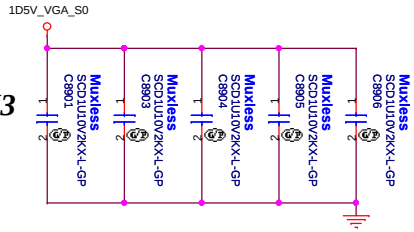
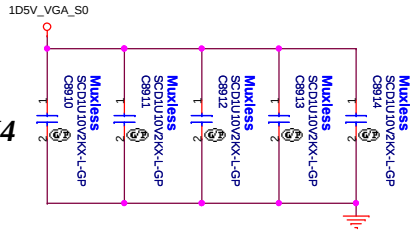
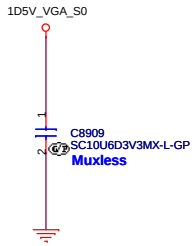


FOR VRAM3



FOR VRAM4





DIS IVB Touch

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU-VRAM3,4 (2/4)***	
Size Custom	Document Number **Husk/Petra**	Rev **-4M**
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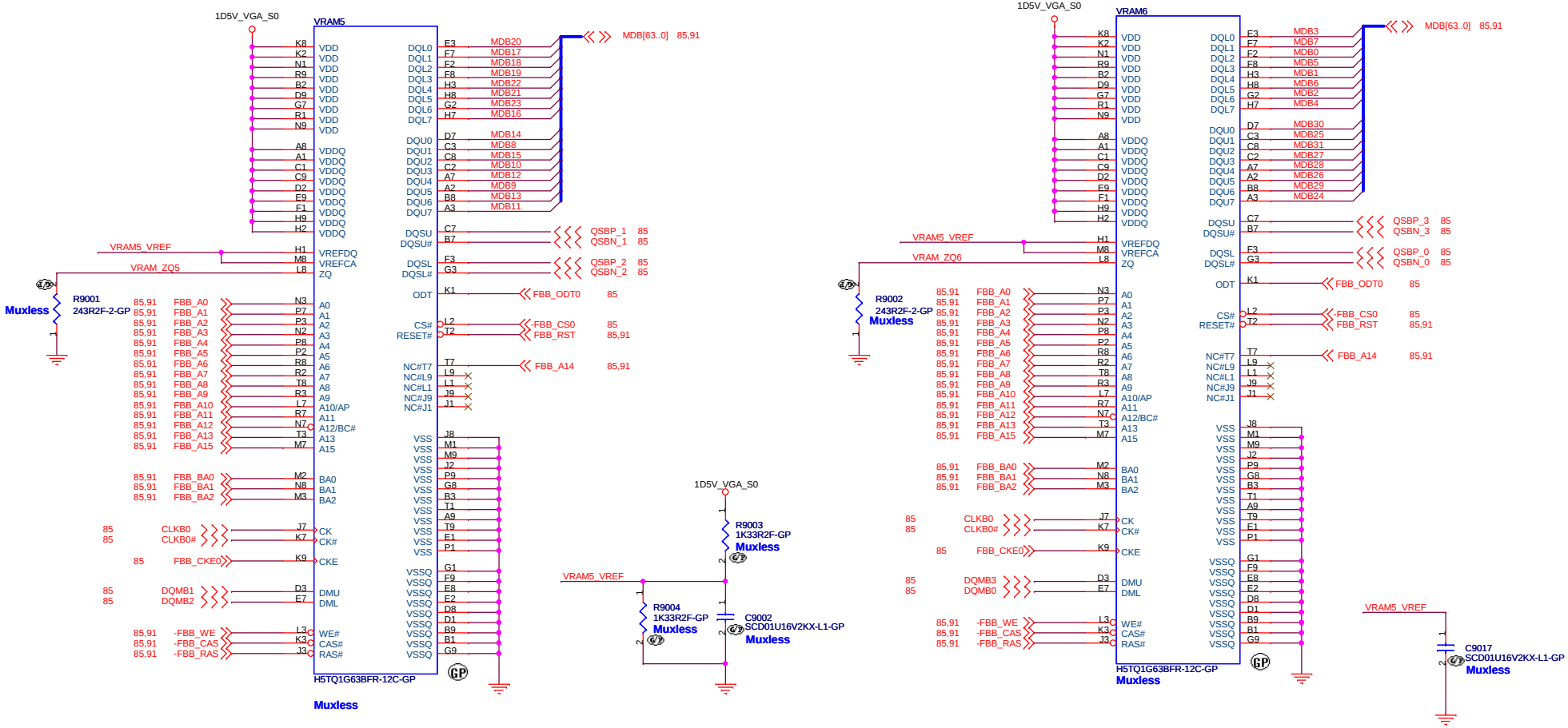
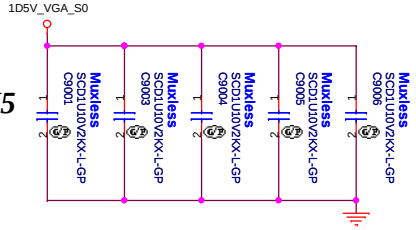
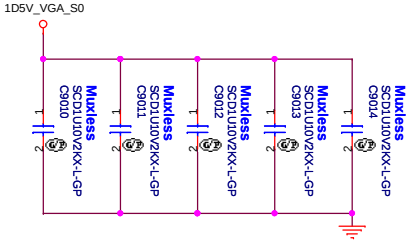
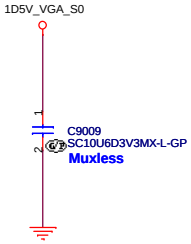


FOR VRAM5



FOR VRAM6





DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM5,6 (3/4)***

Size	Document Number	Rev
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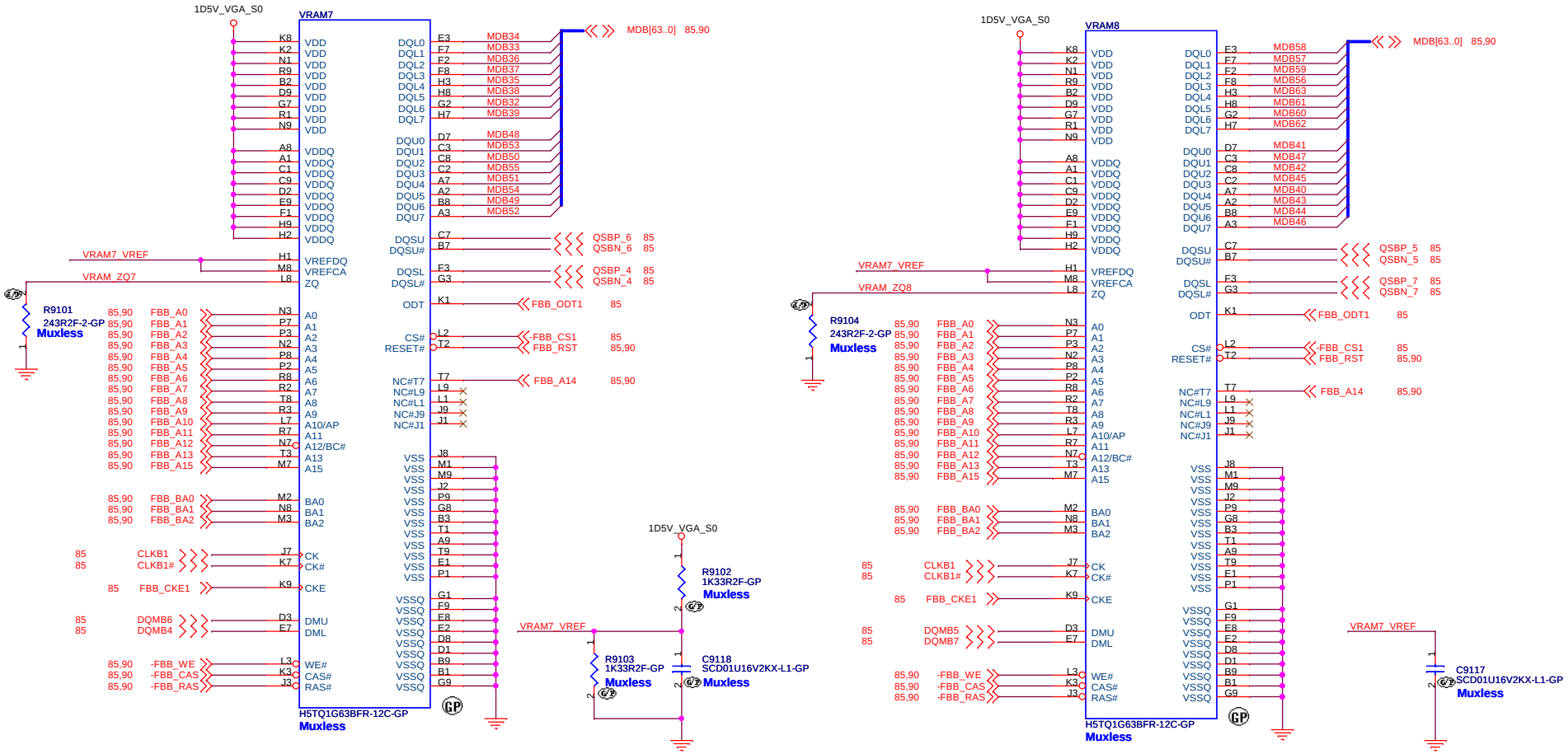
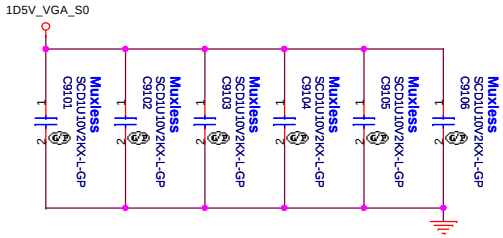
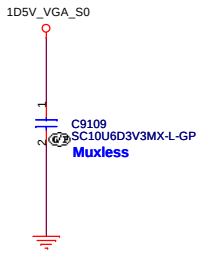
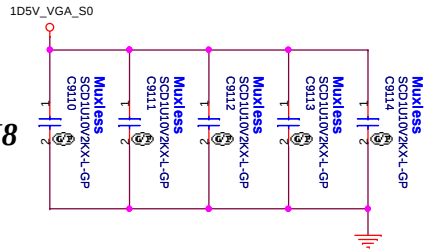


FOR VRAM7





FOR VRAM8



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM7,8 (4/4)**

Size: Custom | Document Number: **Husk/Petra** | Rev: **-4M**

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SSID = PWR.Plane.Regulator_GFX

Change power source Net
Wayler 12/07

		N13P-GS-LP 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U
NVVDD Boot Voltage		0.9V VID[6:0]=0110000	0.95V VID[6:0]=0101100	0.875V VID[6:0]0110010
NV_VID1	PR9215	DY	DY	63.10334.L0L
	PR9230	63.10334.L0L	63.10334.L0L	DY
NV_VID3	PR9217	DY	63.10334.L0L	DY
	PR9232	63.10334.L0L	DY	63.10334.L0L
NV_VID4	PR9218	63.10334.L0L	DY	63.10334.L0L
	PR9233	DY	63.10334.L0L	DY

PR9218 Mount , PR9233 DY For N13M-GS Vboot = 0.875V

1 phase change 0ohm

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

Vga_core
Iccmax=24A
OCP>40A

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

1phase PR9261 mount
2phase PR9261 DY

1phase PR9259 , PR9260 mount
2phase PR9259 , PR9260 DY

DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51728_VGA_CORE

Size | Document Number: Husk/Petra | Rev: -4M

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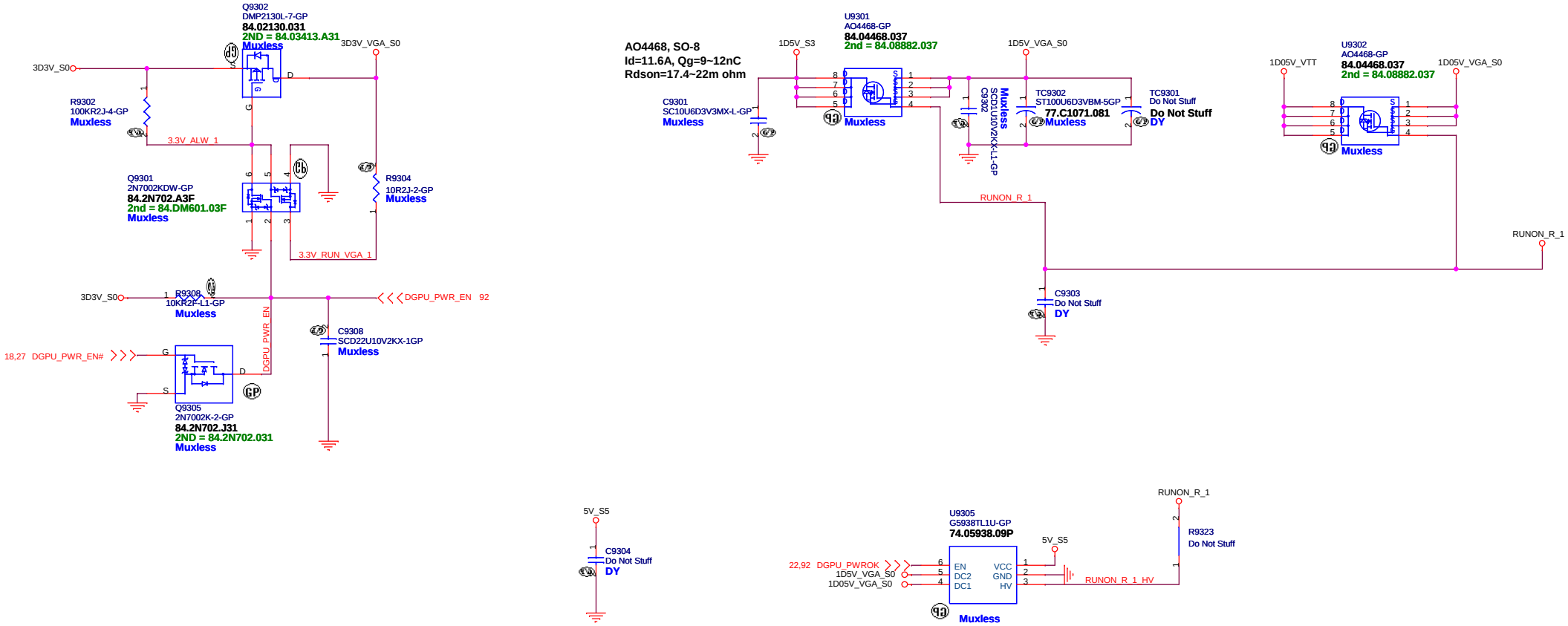

DIS IVB Touch

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DISCRETE VGA POWER***

Size	Document Number	Rev
Custom	**Husk/Petra**	**-4M**

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DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LVDS_Switch

Size	Document Number	Rev
A4	**Husk/Petra**	**-4M**

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DIS IVB Touch

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT_Switch

Size	Document Number	Rev
A3	**Husk/Petra**	**-4M**

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SSID = SDIO

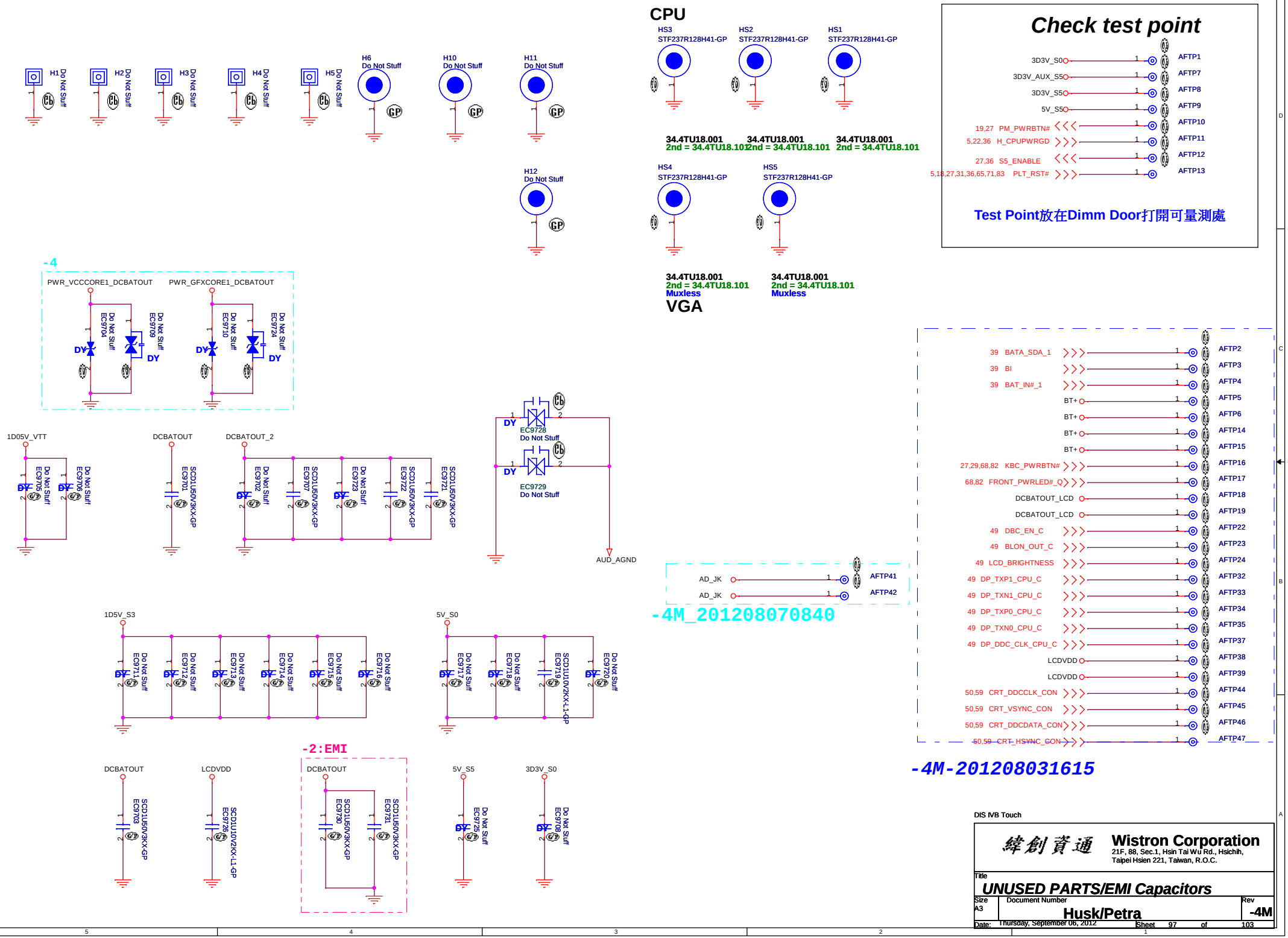
DIS IVB Touch

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TOUCH PANEL***

Size: A2 | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Thursday, September 06, 2012 | Sheet 96 of 103


CPU
HS3 STF237R128H41-GP
HS2 STF237R128H41-GP
HS1 STF237R128H41-GP
34.4TU18.001
2nd = 34.4TU18.101
HS4 STF237R128H41-GP
HS5 STF237R128H41-GP
34.4TU18.001
2nd = 34.4TU18.101
Muxless
VGA
H1 Do Not Stuff
H2 Do Not Stuff
H3 Do Not Stuff
H4 Do Not Stuff
H5 Do Not Stuff
H6 Do Not Stuff
H10 Do Not Stuff
H11 Do Not Stuff
H12 Do Not Stuff
Check test point
3D3V_S0 AFTP1
3D3V_AUX_S5 AFTP7
3D3V_S5 AFTP8
5V_S5 AFTP9
19,27 PM_PWRBTN# AFTP10
5,22,36 H_CPUPWRGD AFTP11
27,36 S5_ENABLE AFTP12
5,18,27,31,36,65,71,83 PLT_RST# AFTP13
Test Point放在Dimm Door打開可量測處
-4
PWR_VCCCORE1_DCBATOUT
PWR_GFXCORE1_DCBATOUT
Do Not Stuff EC9704
Do Not Stuff EC9709
Do Not Stuff EC9710
Do Not Stuff EC9724
DY
1D05V_VTT
DCBATOUT
DCBATOUT_2
Do Not Stuff EC9705
Do Not Stuff EC9706
SCD1U50V3KX-GP EC9701
Do Not Stuff EC9702
SCD1U50V3KX-GP EC9707
Do Not Stuff EC9723
SCD1U50V3KX-GP EC9722
SCD1U50V3KX-GP EC9721
EC9728 Do Not Stuff
EC9729 Do Not Stuff
AUD_AGND
AD_JK AFTP41
AD_JK AFTP42
-4M_201208070840
39 BATA_SDA_1 AFTP2
39 BI AFTP3
39 BAT_IN#_1 AFTP4
BT+ AFTP5
BT+ AFTP6
BT+ AFTP14
BT+ AFTP15
27,29,68,82 KBC_PWRBTN# AFTP16
68,82 FRONT_PWRLED#_Q AFTP17
DCBATOUT_LCD AFTP18
DCBATOUT_LCD AFTP19
49 DBC_EN_C AFTP22
49 BLON_OUT_C AFTP23
49 LCD_BRIGHTNESS AFTP24
49 DP_TXP1_CPU_C AFTP32
49 DP_TXN1_CPU_C AFTP33
49 DP_TXP0_CPU_C AFTP34
49 DP_TXN0_CPU_C AFTP35
49 DP_DDC_CLK_CPU_C AFTP37
LCDVDD AFTP38
LCDVDD AFTP39
50,59 CRT_DDCCLK_CON AFTP44
50,59 CRT_VSYNC_CON AFTP45
50,59 CRT_DDCDATA_CON AFTP46
50,59 CRT_HSYNC_CON AFTP47
-4M-201208031615
1D5V_S3
5V_S0
Do Not Stuff EC9711
Do Not Stuff EC9712
Do Not Stuff EC9713
Do Not Stuff EC9714
Do Not Stuff EC9715
Do Not Stuff EC9716
Do Not Stuff EC9717
Do Not Stuff EC9718
SCD1U10V2KX-L1-GP EC9719
Do Not Stuff EC9720
-2:EMI
DCBATOUT
LCDVDD
5V_S5
3D3V_S0
SCD1U50V3KX-GP EC9703
SCD1U10V2KX-L1-GP EC9726
SCD1U50V3KX-GP EC9730
SCD1U50V3KX-GP EC9731
Do Not Stuff EC9725
Do Not Stuff EC9708
DIS IVB Touch
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
UNUSED PARTS/EMI Capacitors
Size A3
Document Number
Husk/Petra
Rev -4M
Date: Thursday, September 06, 2012
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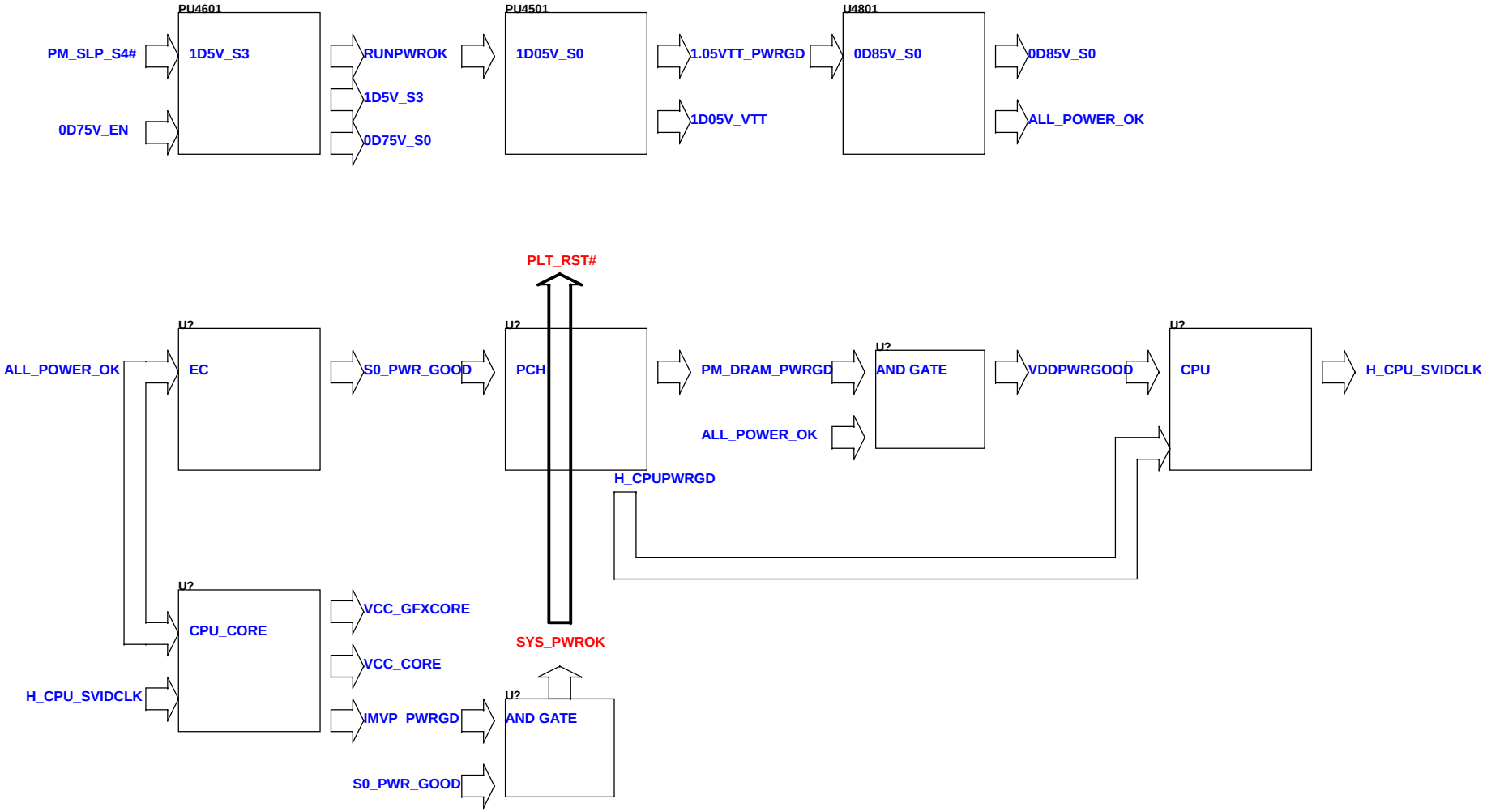
Power Sequence



DIS IVB Touch

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size	Document Number	Rev
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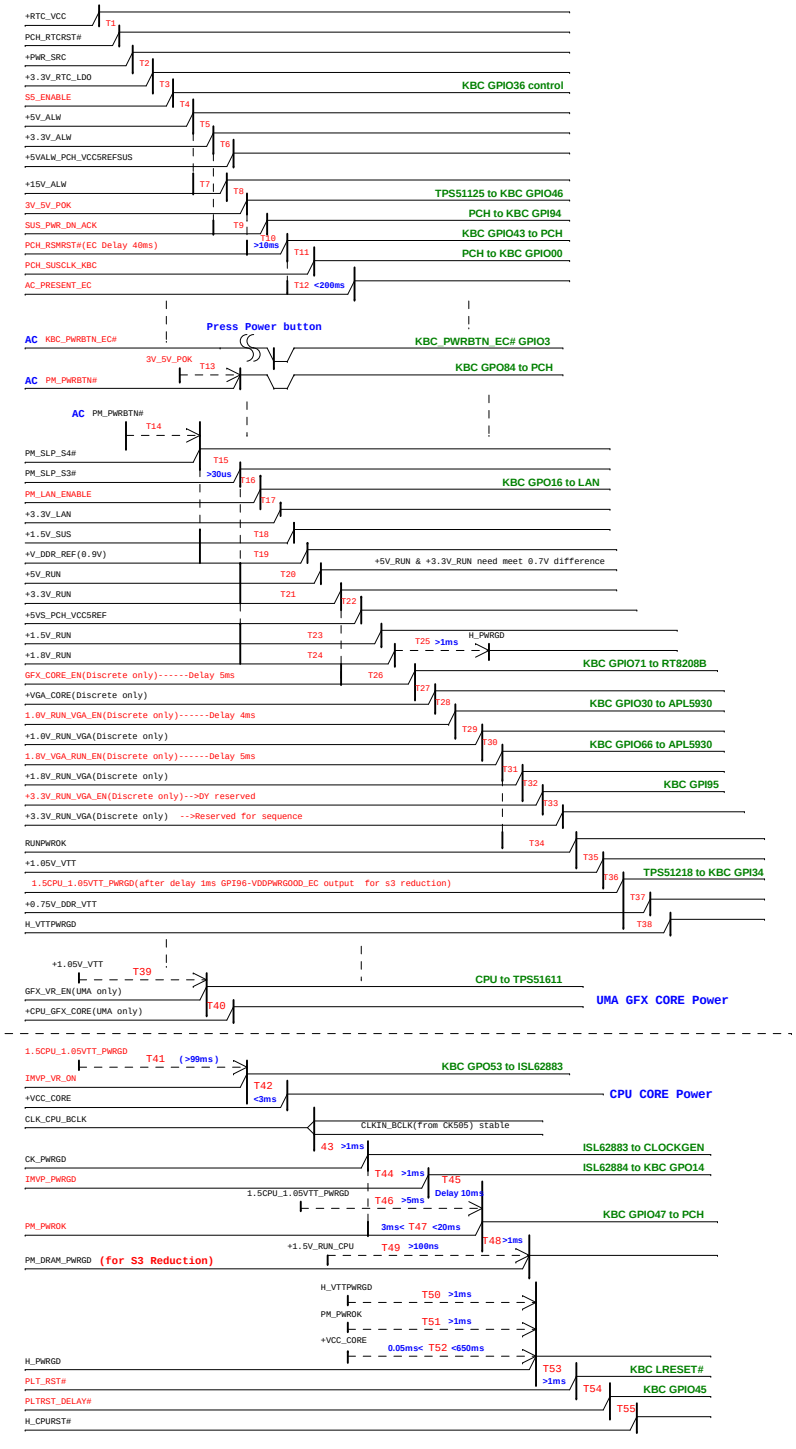
Intel-Power Up Sequence

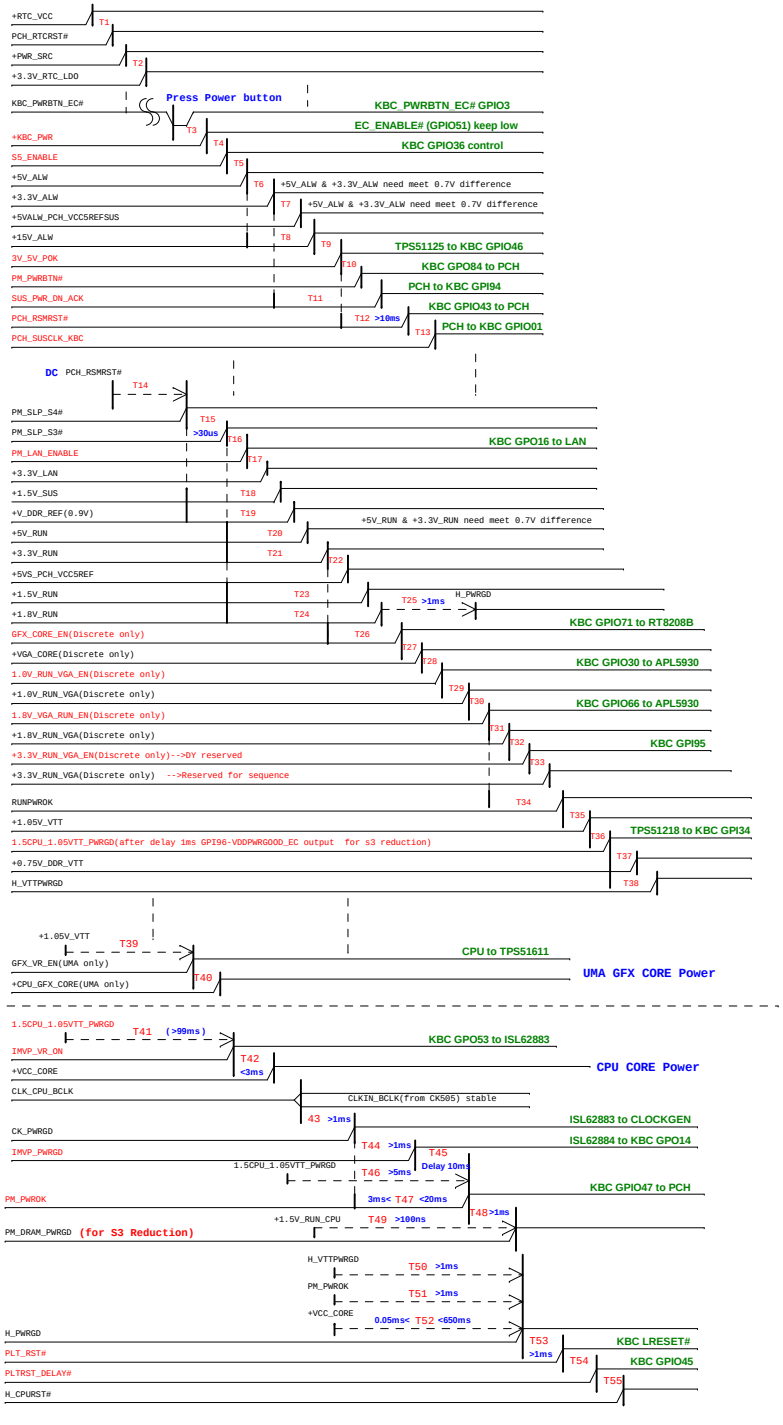
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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Title: Power Sequence

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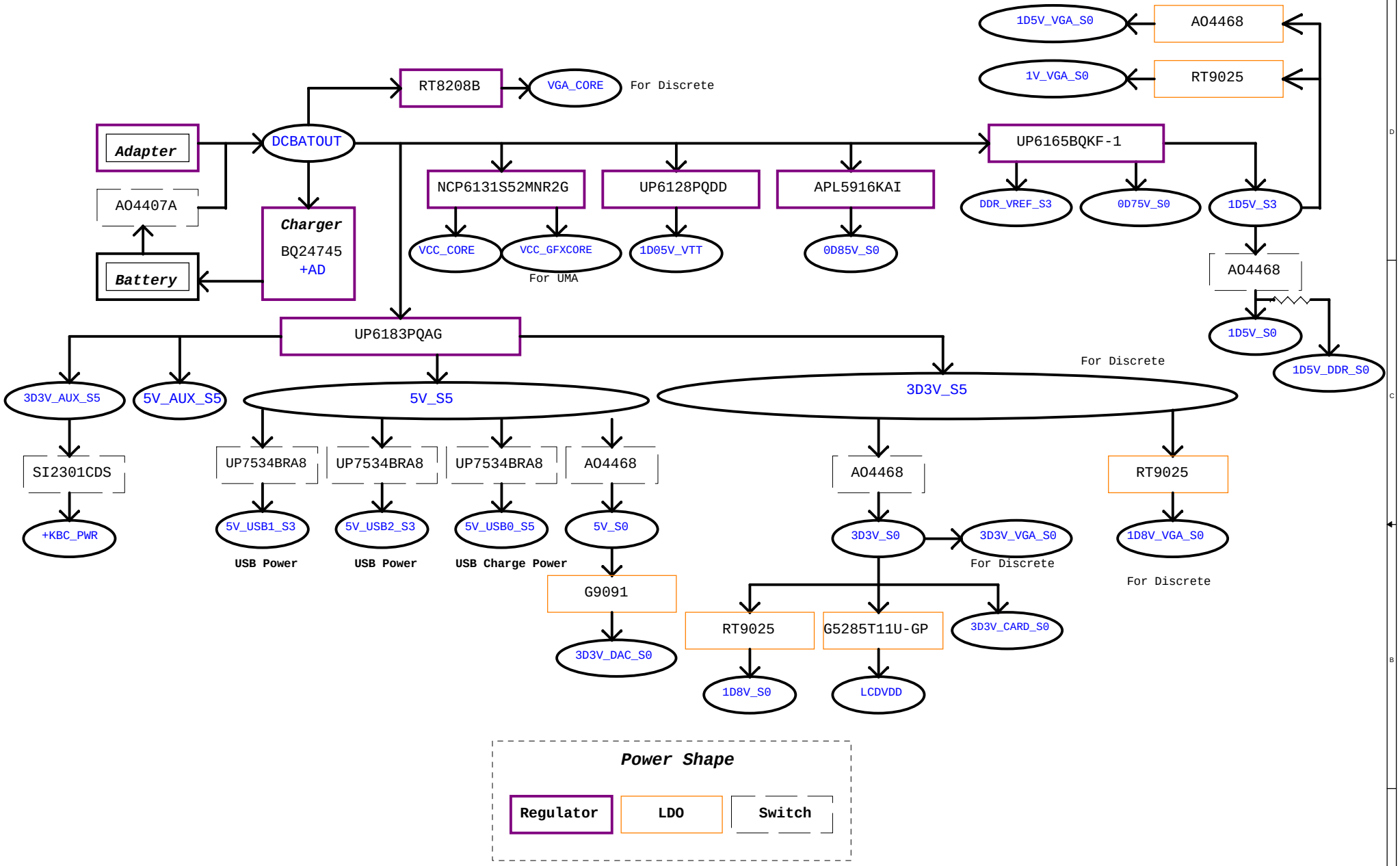

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Title	***Power Block Diagram***	
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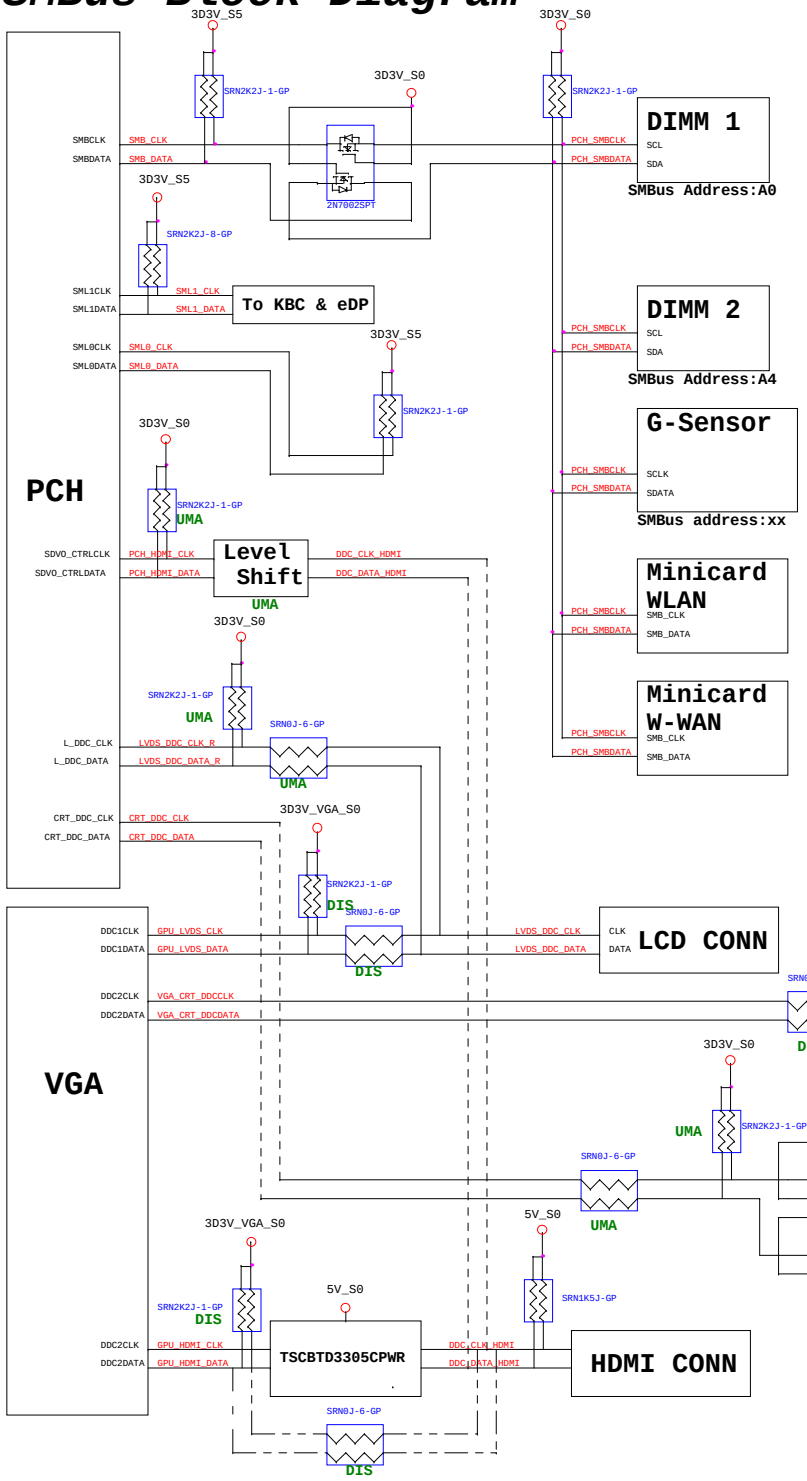
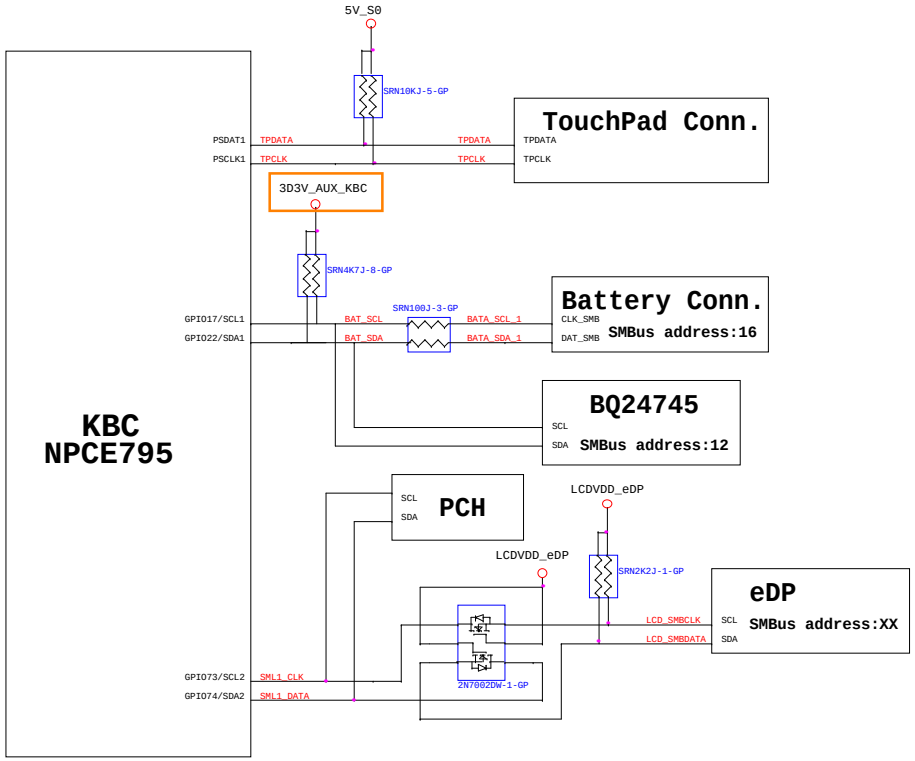
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram		
Size: A2	Document Number: Husk/Petra	Rev: -4M
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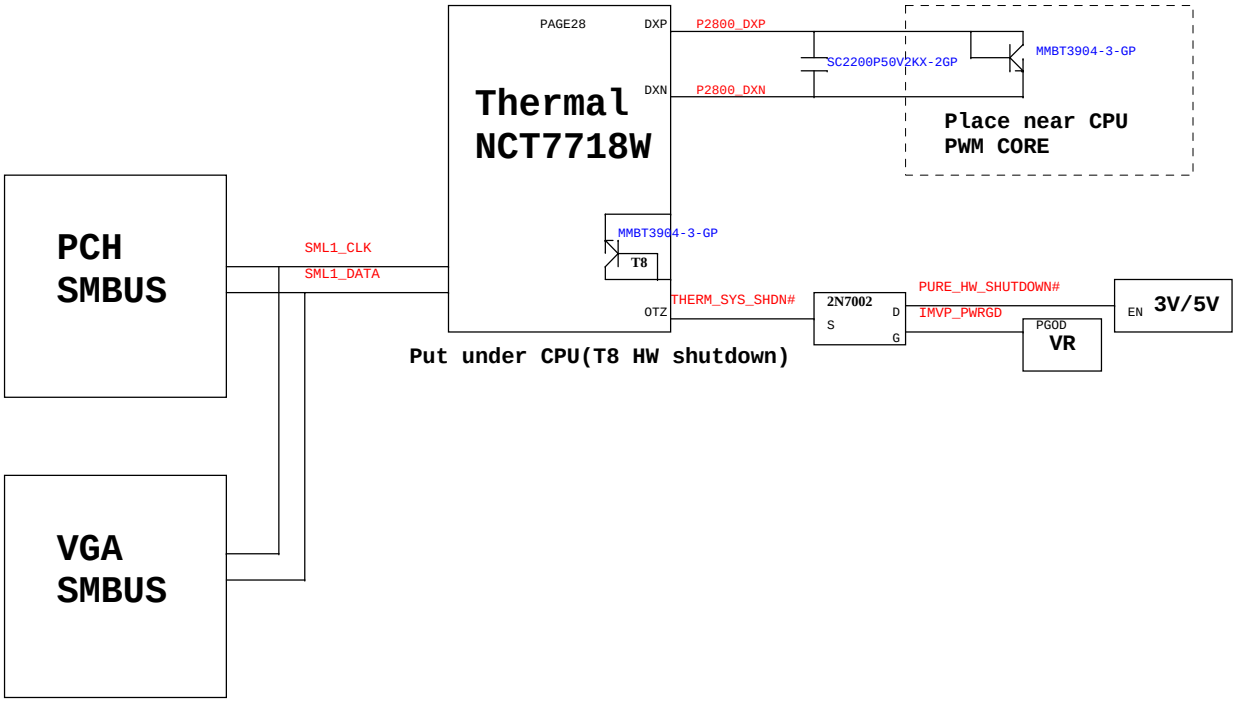
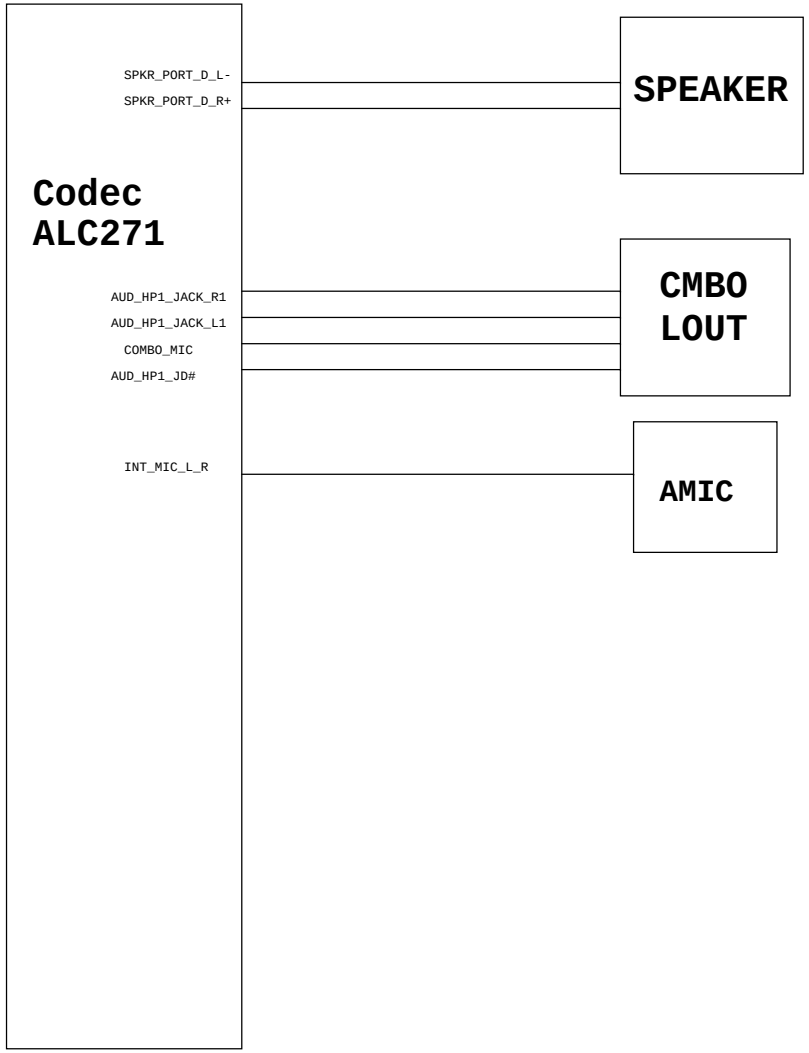
Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
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Title: *USB charger*

Size	Document Number	Rev
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