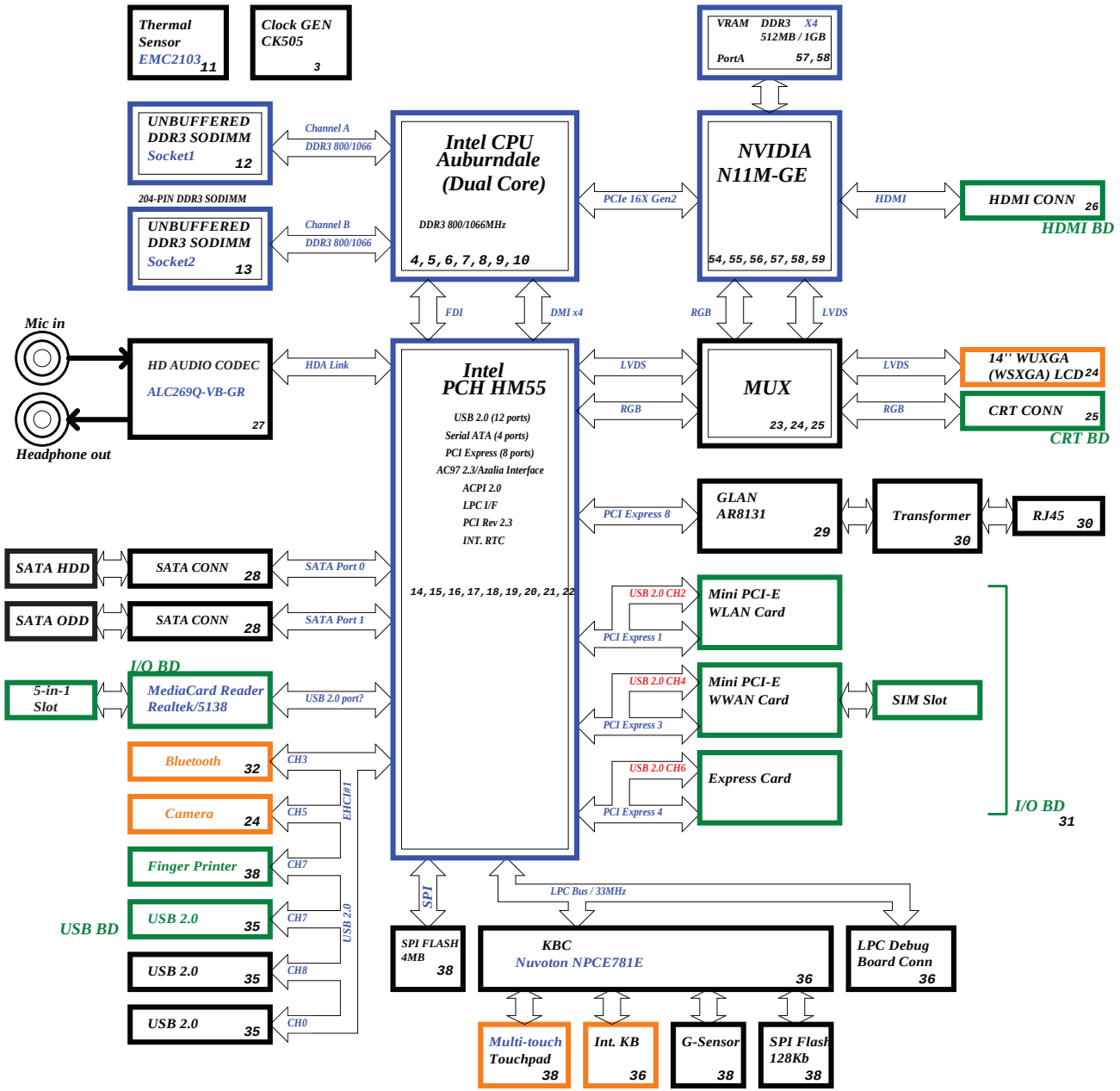
LA46 Switchable Graphics System Schematics

Project Code: 91.4GV01.001
PCB(Raw Card): 09911-1



USB BD
I/O BD
CRT BD
Power BD
Finger Printer BD
HDMI BD
BT BD
AV BD

PCB LAYER

L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Signal

CPU DC/DC ISL62882 38,39

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51123 40

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8209E 41

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8209E 41

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC RT8209E 42

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO RT9025 43

INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT9026 43

INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC ISL62881 44

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC ISL62872 45

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

CHARGER BQ24745 46

INPUTS	OUTPUTS
DCBATOUT	BT+

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

Title: 01 Block Diagram
Size: Custom | Document Number: LA46 MB DIS | Rev: -1
Date: Wednesday, January 27, 2010 | Sheet 1 of 58

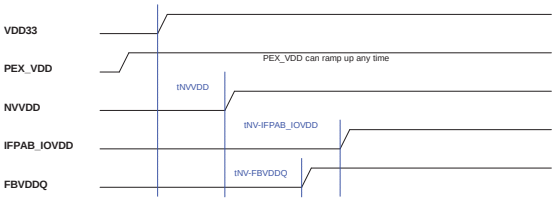
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

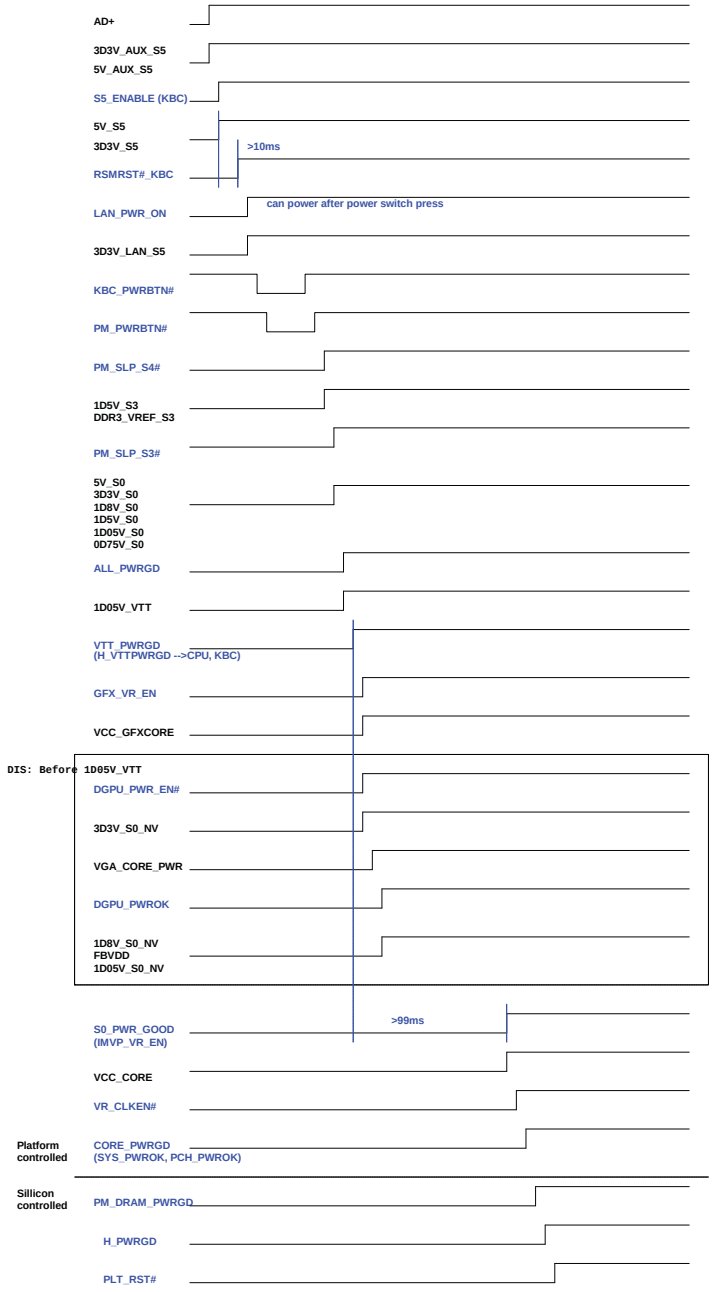
PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

N11M-GE Power Sequence

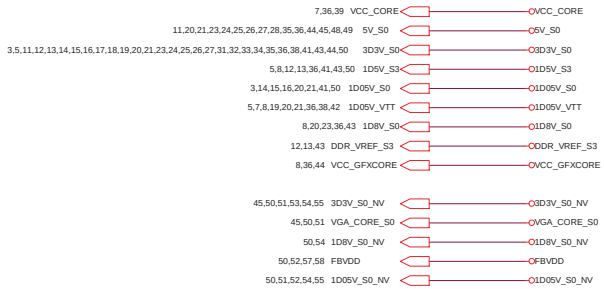


Sequence AC



PLANAR_ID[1..0]

KBC GPIn	31	23	Planar ID Version	Planar PCB Version
PLANAR_IDn	1	0		
	0	0	LA46 - SA	SA
	0	1	LA46 - SB	SB
	1	0	LA46 - SB	SC
	1	1		-1



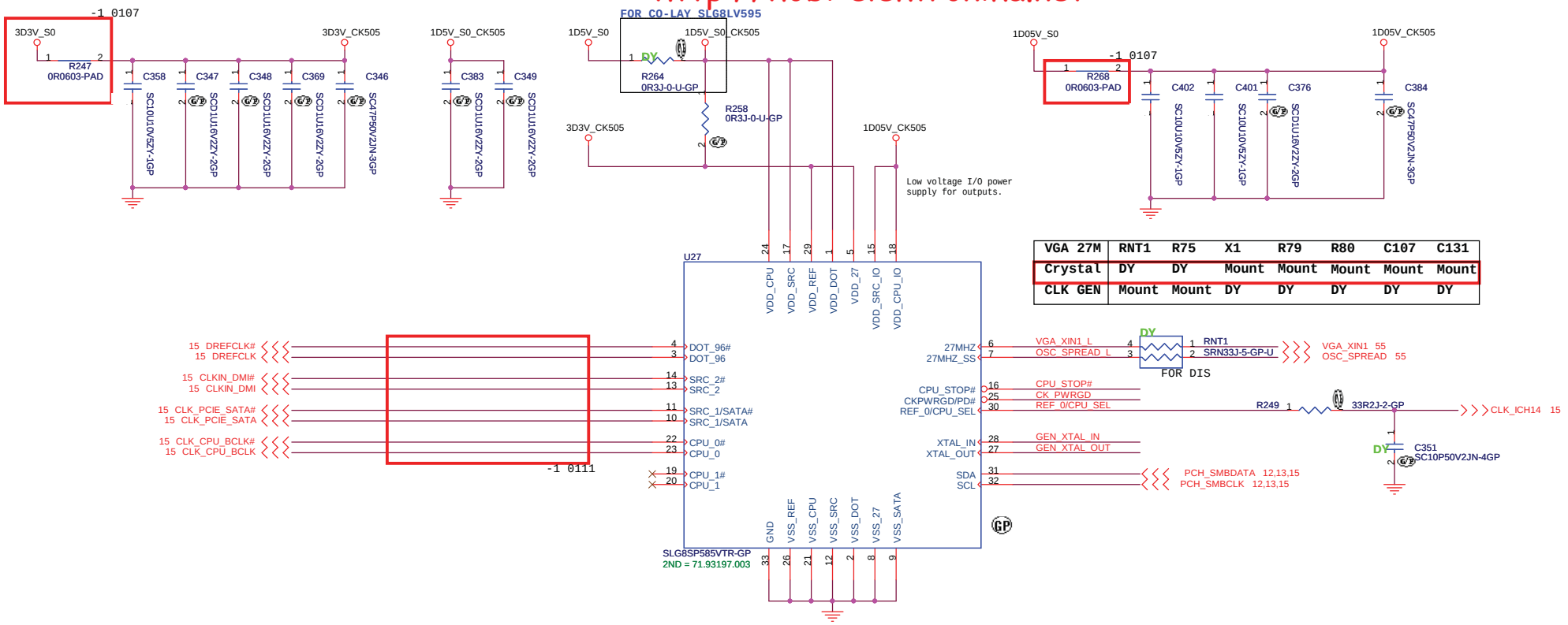
<Core Design>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

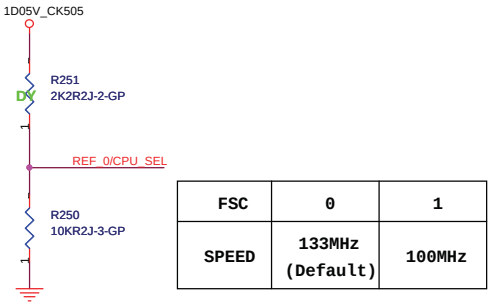
Title: 02_Reference

Size	Document Number	Rev
A2	LA46 MB	-1

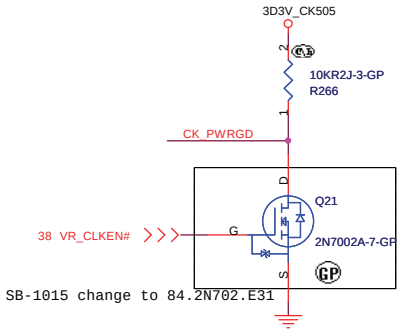
Date: Wednesday, January 27, 2010 Sheet 2 of 58



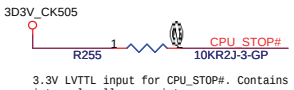
VGA 27M	RNT1	R75	X1	R79	R80	C107	C131
Crystal	DY	DY	Mount	Mount	Mount	Mount	Mount
CLK GEN	Mount	Mount	DY	DY	DY	DY	DY



FSC	0	1
SPEED	133MHz (Default)	100MHz

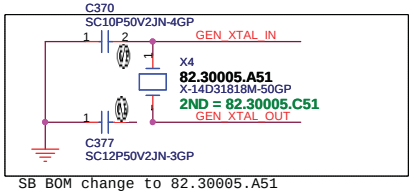


SB-1015 change to 84.2N702.E31



3.3V LVTTL input for CPU_STOP#. Contains internal pull-up resistor.

CL=20pF±0.2pF



SB BOM change to 82.30005.A51

Layout Notes:

Make sure that the stubs to the test points(CK_PWRGD, CLK_EN#, GEN_XTAL_OUT) in the layout are as short as possible on the high speed signals.

<Core Design>

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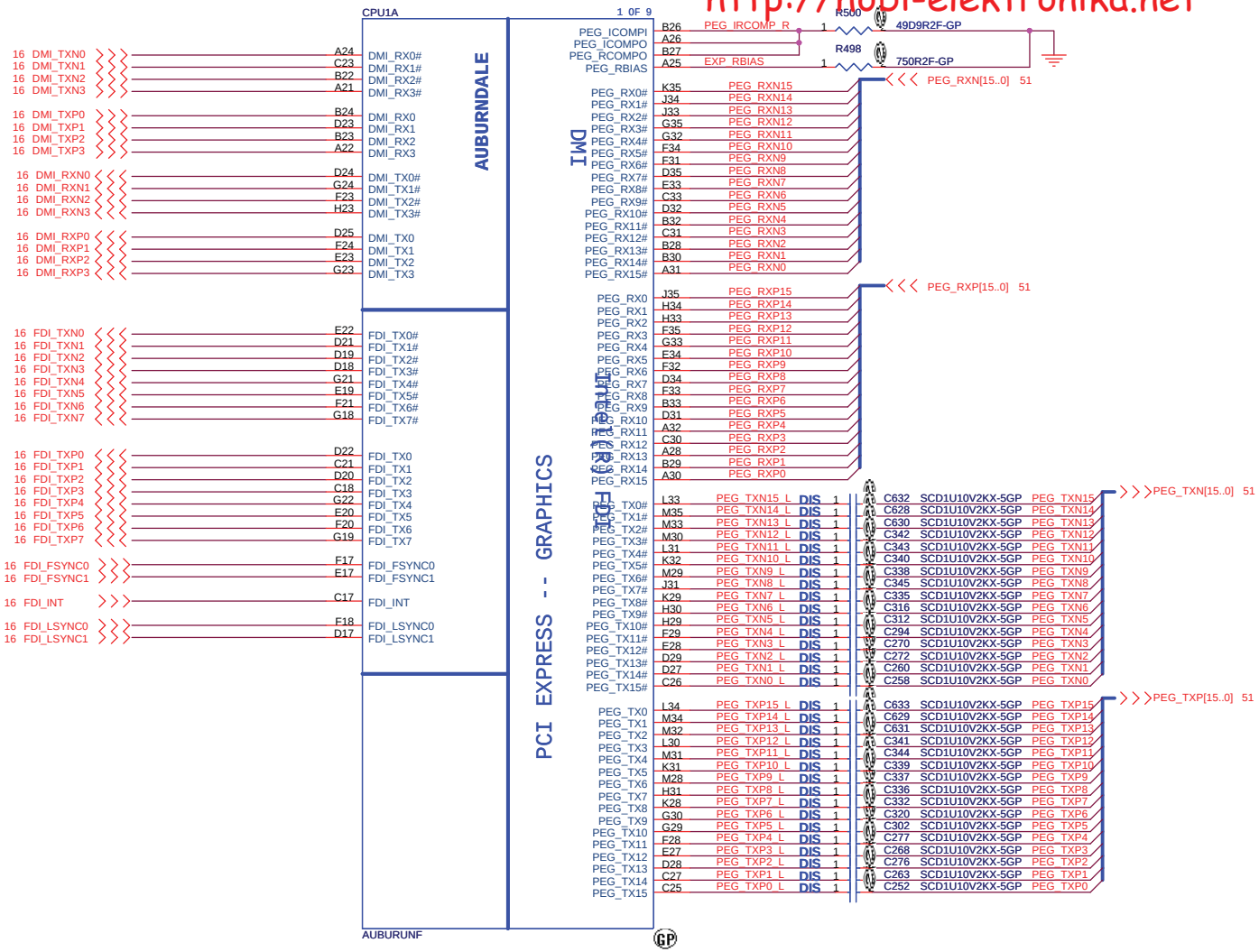
Title: 03_Clock Generator SLG8SP585

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

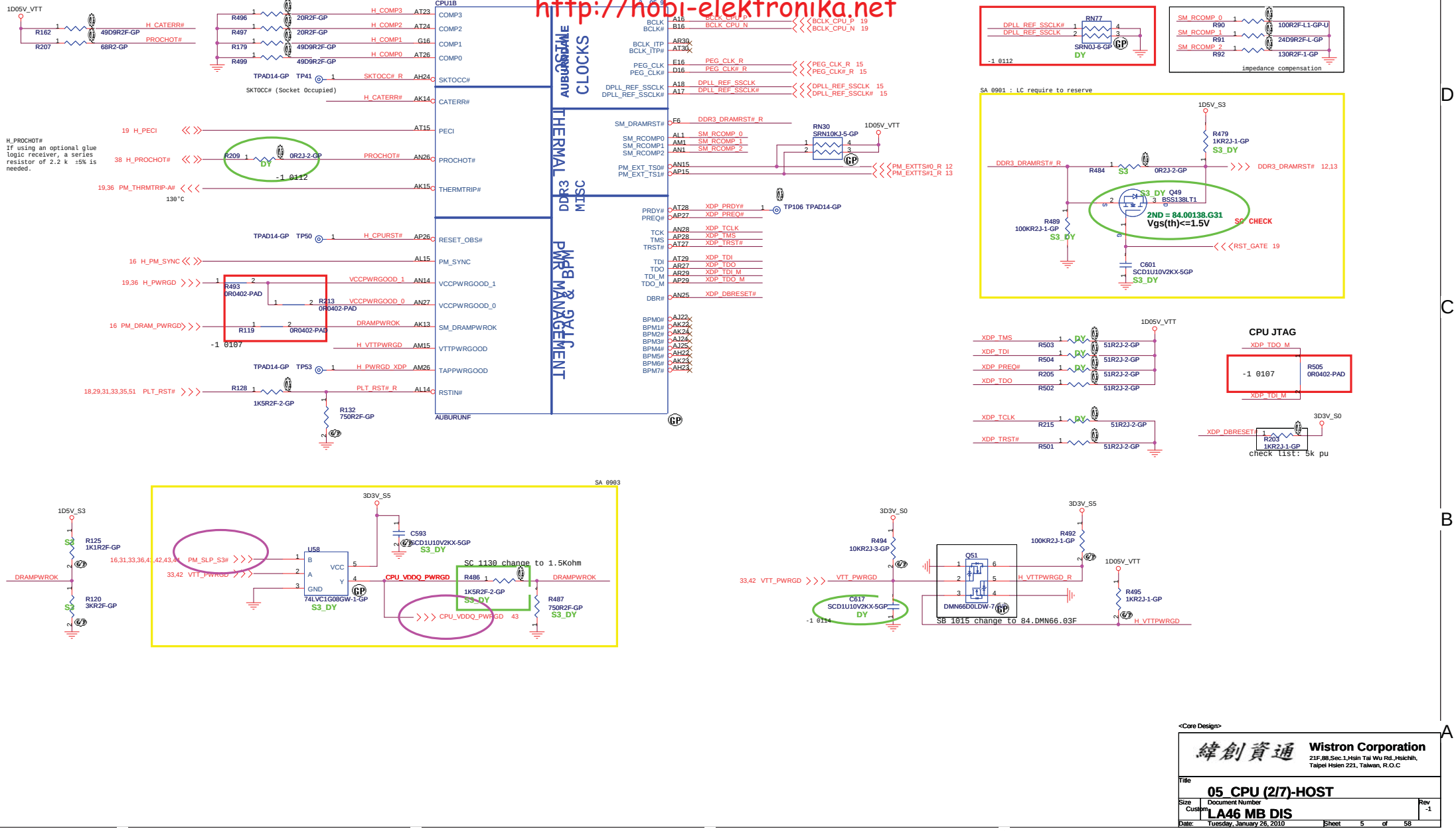
Date: Tuesday, January 26, 2010 | Sheet 3 of 58



Title
04_CPU (1/7)-PEG / DMI / FDI

Size	Document Number	Rev
A3	**LA46 MB DIS**	-1

Date: Tuesday, January 26, 2010 Sheet 4 of 58

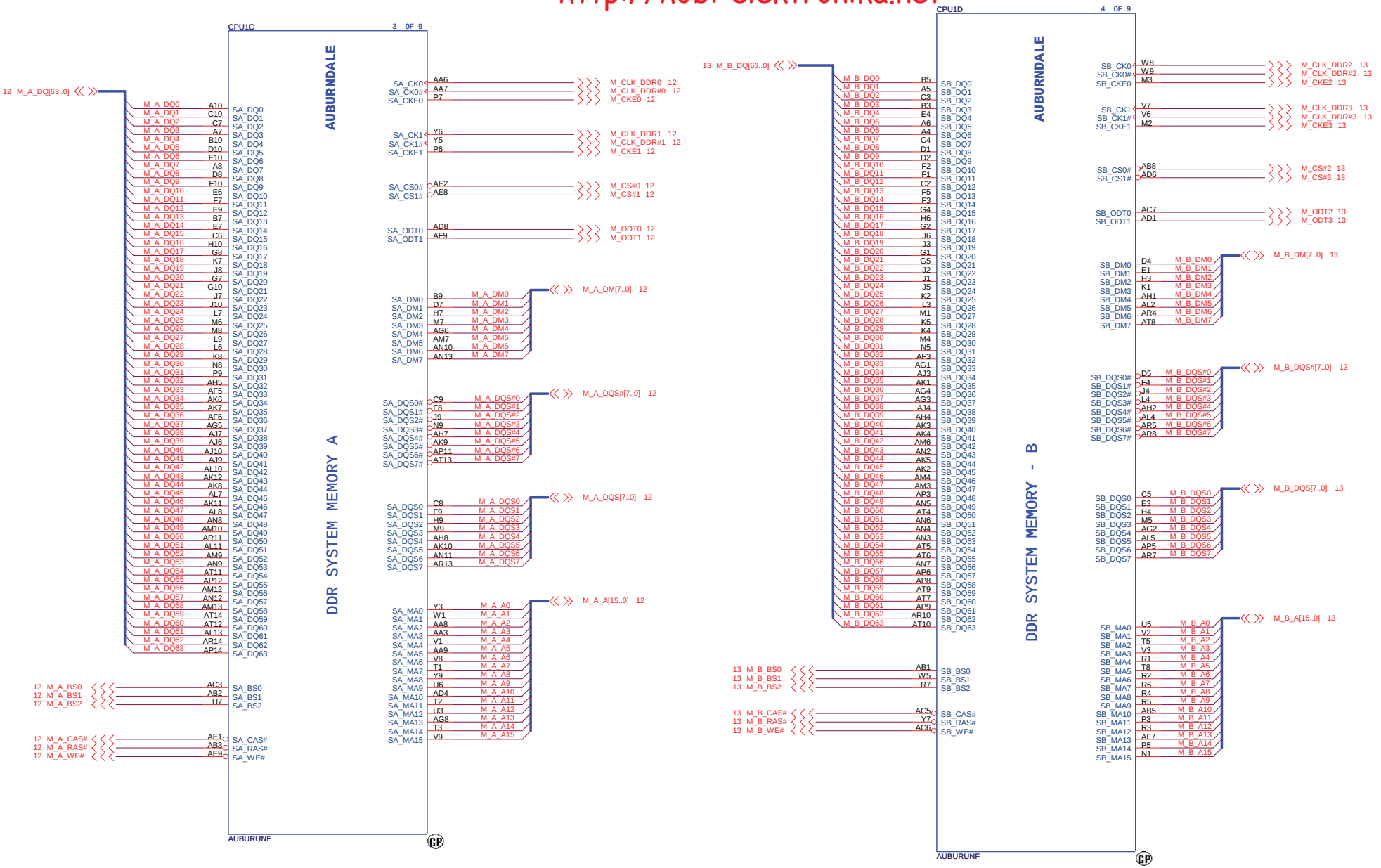


<Core Design>
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 05_CPU (2/7)-HOST

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 5 of 58



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C

Title: 06_CPU (3/7)-MEM INTERFACE

Size	Document Number	Rev
Custom	LA46 MB DIS	-1

Date: Tuesday, January 26, 2010 Sheet 6 of 58

PROCESSOR CORE POWER

48A -->Arrandale

VCC_CORE

C244 C235 C236 C238 C237 C239 — SC10U6D3V3MX-GP

C240 C618 C619 C620 C241 — SC10U6D3V3MX-GP

C267 C251 — SC10U6D3V3MX-GP

C242 C243 C627 C634 C635 — SC10U6D3V3MX-GP

CPU1F

AUBURNDALE

AUBURUNF

VCC_CORE: AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

1.1V RAIL POWER

VTT0: AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

1D05V_VTT

C621 C616 C613 C605 C603 C604 C611 — SC10U6D3V3MX-GP

SA_0917

1D05V_VTT

C636 SCD1U10V2KX-5GP DY

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

CPU CORE SUPPLY

VTT0: AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

1D05V_VTT

C602 C218 — SC10U6D3V3MX-GP

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

POWER

CPU VIDS

PSI# AN33 → PSI# 38

VID0 AK35 H_VID0
VID1 AK33 H_VID1
VID2 AK34 H_VID2
VID3 AL35 H_VID3
VID4 AL33 H_VID4
VID5 AM33 H_VID5
VID6 AM35 H_VID6
→ H_VID[6..0] 38

PROC_DPRSLPVR AM34 → PM_DPRSLPVR 38

VTT_SELECT G15 — H_VTTVID1 — TP35 TPAD14-GP

Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V

SENSE LINES

ISENSE AN35 → IMVP_IMON 38

VCC_CORE

R238 100R2F-L1-GP-U

VCC_SENSE AJ34 → VCC_SENSE 38
VSS_SENSE AJ35 → VSS_SENSE 38

R232 100R2F-L1-GP-U

VTT_SENSE B15 → VTT_SENSE 42
VSS_SENSE_VTT A15

SB 1019 remove test point

<Core Design>

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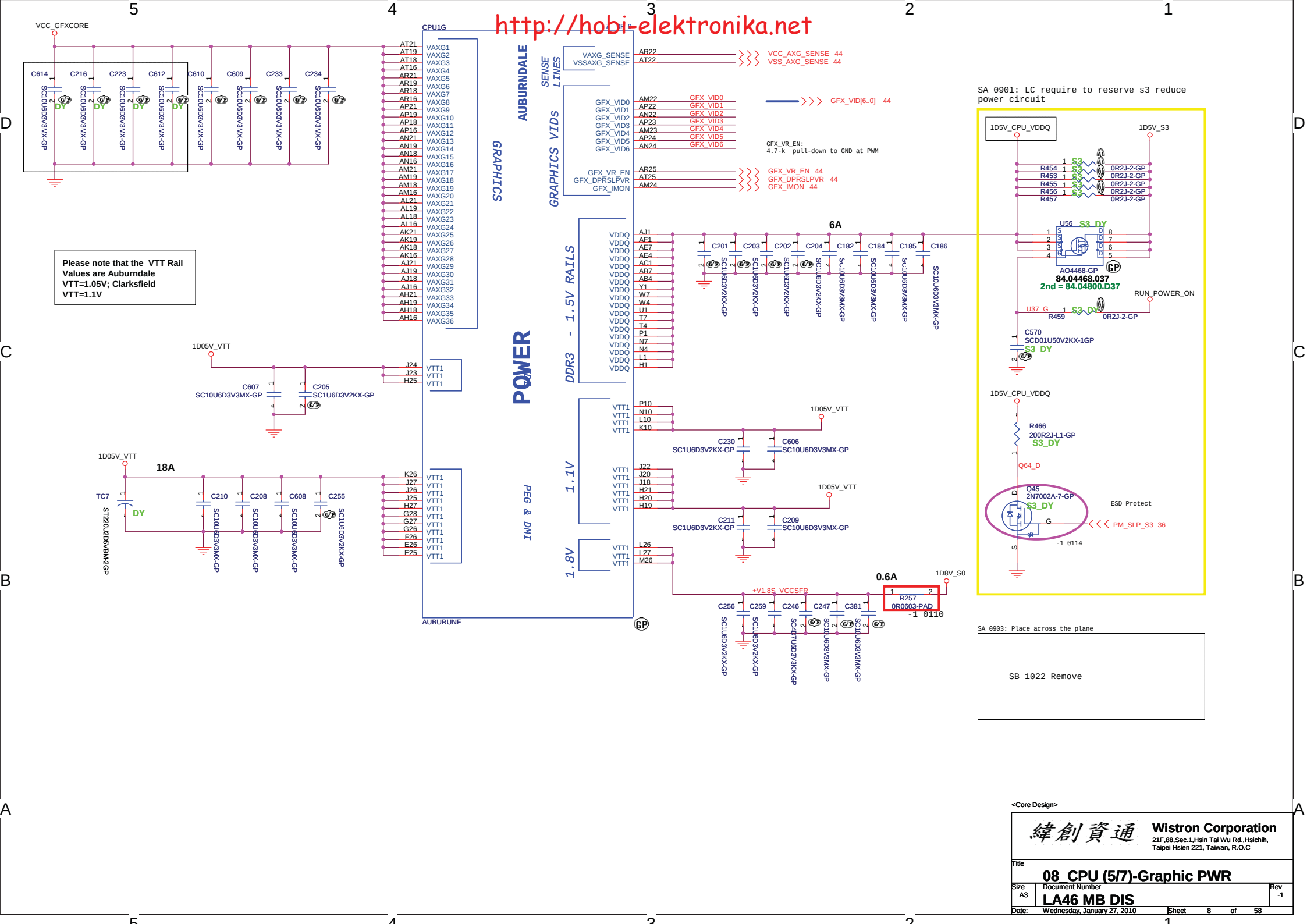
Taipei Hsien 221, Taiwan, R.O.C

Title: 07_CPU (4/7)-POWER

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 7 of 58

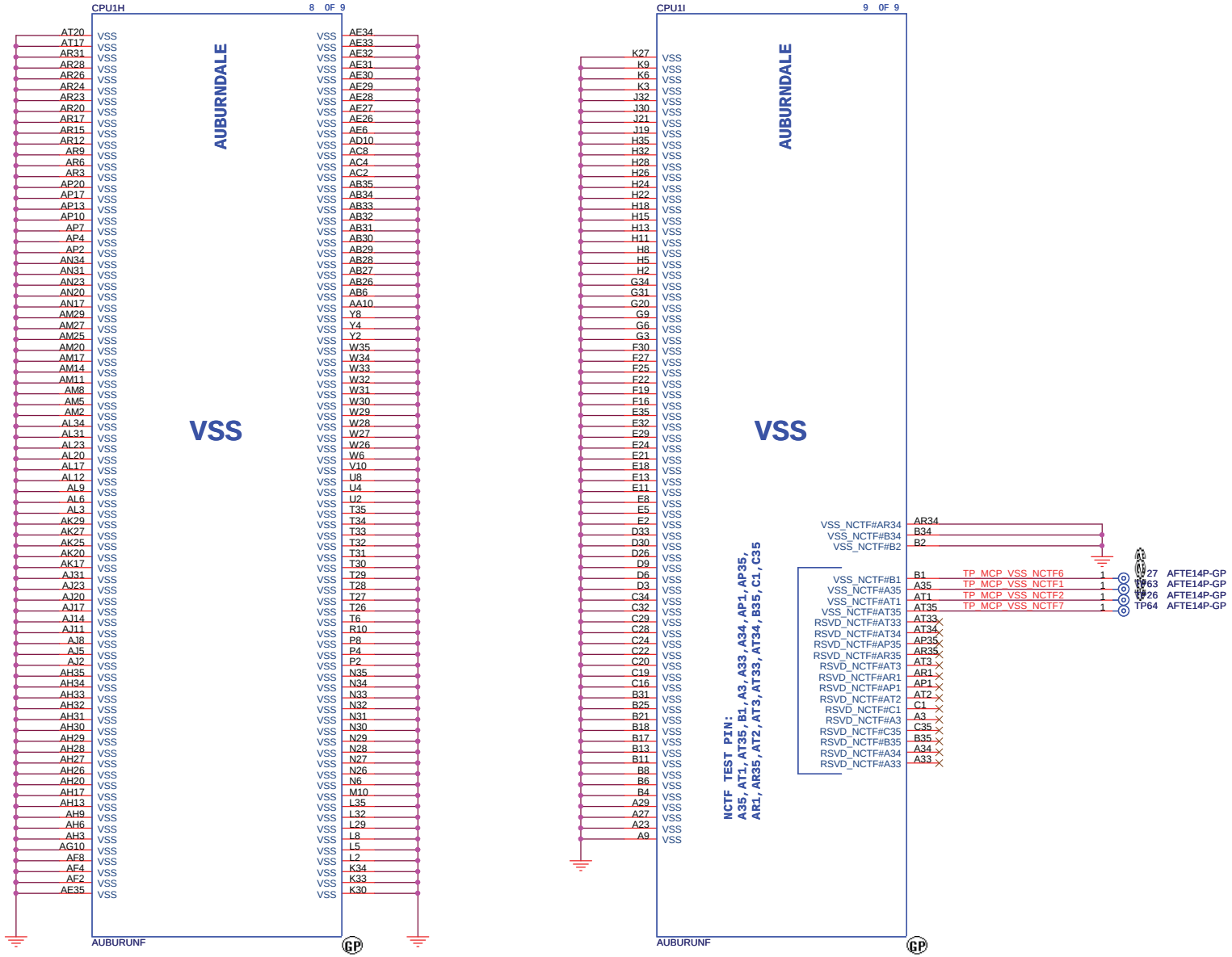


<Core Design>
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 08_CPU (5/7)-Graphic PWR

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 8 of 58



<Core Design>

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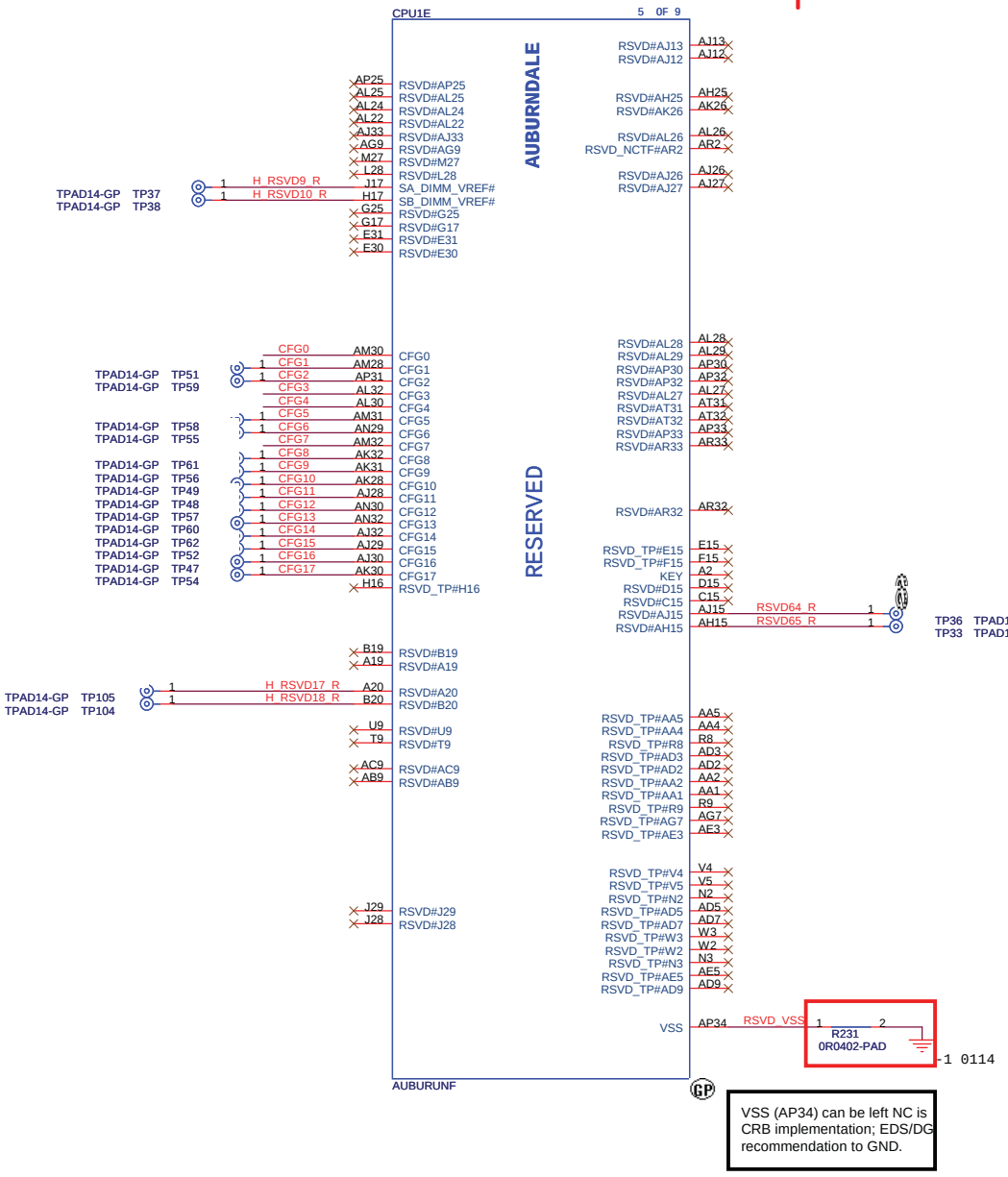
Taipei Hsien 221, Taiwan, R.O.C

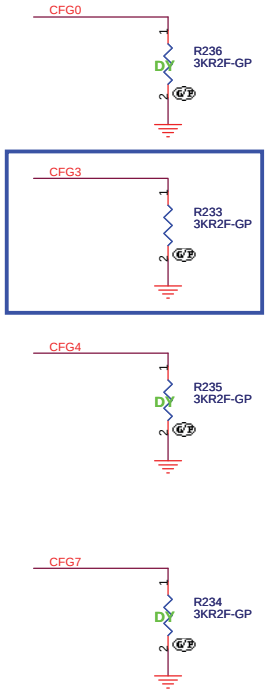
Title: 09_CPU (6/7)-VSS

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 9 of 58



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

<Core Design>

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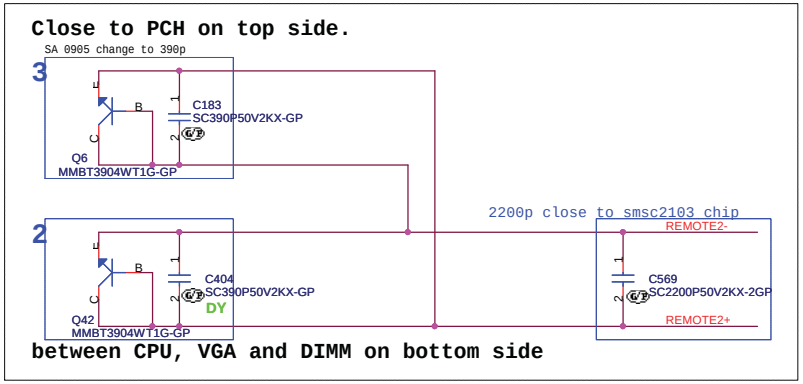
Title: 10_CPU (7/7)-RESERVED

Size	Document Number	Rev
A3	LA46 MB DIS	-1

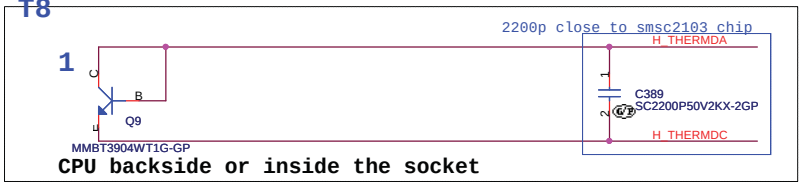
Date: Tuesday, January 26, 2010 Sheet 10 of 58

Close to PCH on top side.



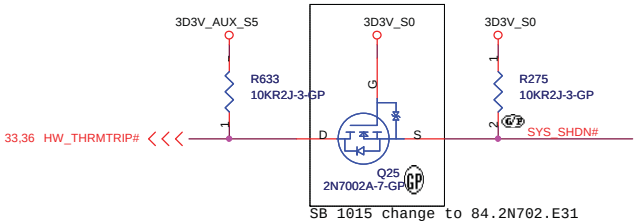
between CPU, VGA and DIMM on bottom side

T8

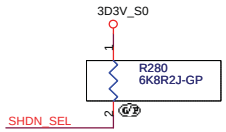


CPU backside or inside the socket

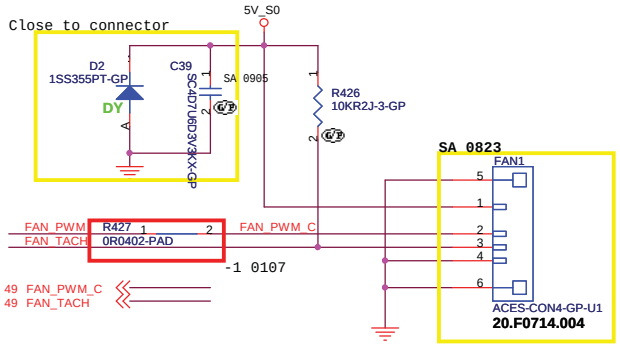
CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.



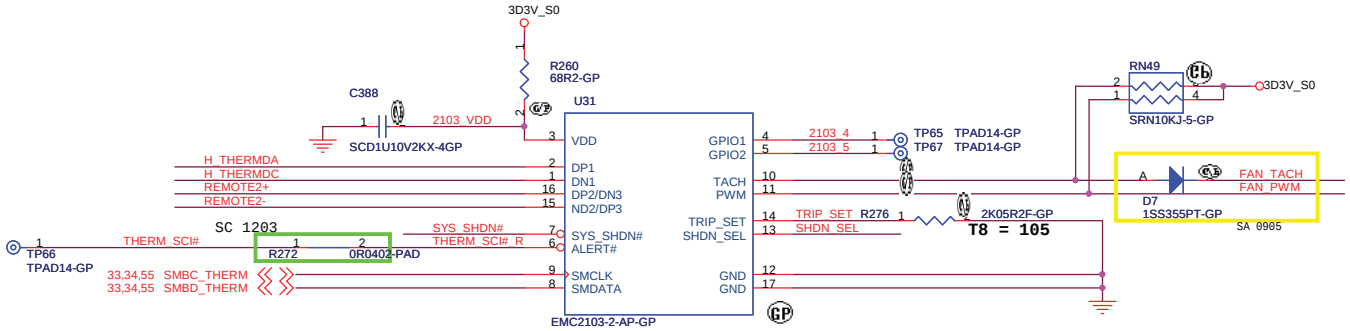
SB 1015 change to 84.2N702.E31



SHDN --> 2N3904 ON External diode



4 WIRE PWM Fan Control circuit



pin6, ALERT# OD
pin7, SYS_SHDN# OD

<Core Design>

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21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: **11_THERMAL SMSC2103**

Size	Document Number	Rev
A3	**LA46 MB DIS**	-1

Date: Tuesday, January 26, 2010 Sheet 11 of 58

SA 0820

DM1

6 M_A_A[15..0]
6 M_A_BS2
6 M_A_BS0
6 M_A_BS1
6 M_A_DQ[63..0]
6 M_A_DQS#[7..0]
6 M_A_DQS[7..0]
6 M_ODT0
6 M_ODT1
5,13 DDR3_DRAMRST#

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15
79 A16/BA2
109 BA0
108 BA1

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 15 DQ2
M_A_DQ3 17 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 16 DQ6
M_A_DQ7 18 DQ7
M_A_DQ8 21 DQ8
M_A_DQ9 23 DQ9
M_A_DQ10 33 DQ10
M_A_DQ11 35 DQ11
M_A_DQ12 22 DQ12
M_A_DQ13 24 DQ13
M_A_DQ14 34 DQ14
M_A_DQ15 36 DQ15
M_A_DQ16 39 DQ16
M_A_DQ17 41 DQ17
M_A_DQ18 51 DQ18
M_A_DQ19 53 DQ19
M_A_DQ20 40 DQ20
M_A_DQ21 42 DQ21
M_A_DQ22 50 DQ22
M_A_DQ23 52 DQ23
M_A_DQ24 57 DQ24
M_A_DQ25 59 DQ25
M_A_DQ26 67 DQ26
M_A_DQ27 69 DQ27
M_A_DQ28 56 DQ28
M_A_DQ29 58 DQ29
M_A_DQ30 68 DQ30
M_A_DQ31 70 DQ31
M_A_DQ32 129 DQ32
M_A_DQ33 131 DQ33
M_A_DQ34 141 DQ34
M_A_DQ35 143 DQ35
M_A_DQ36 130 DQ36
M_A_DQ37 132 DQ37
M_A_DQ38 140 DQ38
M_A_DQ39 142 DQ39
M_A_DQ40 147 DQ40
M_A_DQ41 149 DQ41
M_A_DQ42 157 DQ42
M_A_DQ43 159 DQ43
M_A_DQ44 146 DQ44
M_A_DQ45 148 DQ45
M_A_DQ46 158 DQ46
M_A_DQ47 160 DQ47
M_A_DQ48 163 DQ48
M_A_DQ49 165 DQ49
M_A_DQ50 175 DQ50
M_A_DQ51 177 DQ51
M_A_DQ52 164 DQ52
M_A_DQ53 166 DQ53
M_A_DQ54 174 DQ54
M_A_DQ55 176 DQ55
M_A_DQ56 181 DQ56
M_A_DQ57 183 DQ57
M_A_DQ58 191 DQ58
M_A_DQ59 193 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63

M_A_DQS#0 10 DQS0#
M_A_DQS#1 27 DQS1#
M_A_DQS#2 45 DQS2#
M_A_DQS#3 62 DQS3#
M_A_DQS#4 135 DQS4#
M_A_DQS#5 152 DQS5#
M_A_DQS#6 169 DQS6#
M_A_DQS#7 186 DQS7#

M_A_DQS0 12 DQS0
M_A_DQS1 29 DQS1
M_A_DQS2 47 DQS2
M_A_DQS3 64 DQS3
M_A_DQS4 137 DQS4
M_A_DQS5 154 DQS5
M_A_DQS6 171 DQS6
M_A_DQS7 188 DQS7

116 ODT0
120 ODT1
M_VREF_CA_DIMM0 126 VREF_CA
M_VREF_DQ_DIMM0 1 VREF_DQ
30 RESET#
MA_VTT 203 VTT1
204 VTT2

NP1 NP2

RAS# 110 M_A_RAS# 6
WE# 113 M_A_WE# 6
CAS# 115 M_A_CAS# 6
CS0# 114 M_CS#0 6
CS1# 121 M_CS#1 6
CKE0 73 M_CKE0 6
CKE1 74 M_CKE1 6
CK0 101 M_CLK_DDR0 6
CK0# 103 M_CLK_DDR#0 6
CK1 102 M_CLK_DDR1 6
CK1# 104 M_CLK_DDR#1 6
M_A_DM[7..0] 6

DM0 11 M_A_DM0
DM1 28 M_A_DM1
DM2 46 M_A_DM2
DM3 63 M_A_DM3
DM4 136 M_A_DM4
DM5 153 M_A_DM5
DM6 170 M_A_DM6
DM7 187 M_A_DM7

SDA 200 SODIMM0_1_SMB_DATA_R
SCL 202 SODIMM0_1_SMB_CLK_R
EVENT# 198 TS#_DIMM0
VDDSPD 199
SA0 197 SA0_DIM0
SA1 201 SA1_DIM0
NC#1 77
NC#2 122
NC#TEST 125

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

VSS 2,3,8,9,13,14,19,20,25,26,31,32,37,38,43,44,48,49,54,55,60,61,65,66,71,72,127,128,133,134,138,139,144,145,150,151,155,156,161,162,167,168,172,173,178,179,184,185,189,190,195,196,205,206

62.10017.M11
62.10017.M41
DDR3-204P-31-GP-U

SB 1024 Change to 62.10017.M41

H = 4mm

SA 0902

1D5V_S3
DDR_VREF_S3
R63 1KR2F-3-GP DY
R64 1KR2F-3-GP DY
R66 0R0603-PAD
DIMM0_VREF_CADQ
-1 0114

DIMM0_VREF_CADQ
R59 1 2 0R0603-PAD
C82 SCD1U10V2KX-5GP
-1 0107
M_VREF_CA_DIMM0
C89 SC2D2U6D3V3KX-GP

DIMM0_VREF_CADQ
R42 1 2 0R0603-PAD
C53 SCD1U10V2KX-5GP
M_VREF_DQ_DIMM0
C55 SC2D2U6D3V3KX-GP

SB 1026 change to 78.22520.5BL

0D75_S0
R46 0R0603-PAD
-1 0107
MA_VTT

Place these caps close to VTT1 and VTT2.

C48 C58 C60 C70 SC1U6D3V2KX-GP

3D3V_S0
R43 10KR2J-3-GP DY
R45 10KR2J-3-GP
R44 10KR2J-3-GP
SA0_DIM0
SA1_DIM0

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SC 1203
R53 1 2 0R0402-PAD
R54 1 2 0R0402-PAD
PCH_SMBDATA 3,13,15
PCH_SMBCLK 3,13,15
R52 1 2 0R0402-PAD
-1 0107
PM_EXTTS#0_R 5
C54 SCD1U10V2KX-5GP
C57 SC2D2U6D3V3KX-GP
SB 1026 change to 78.22520.5BL

SODIMM A DECOUPLING

1D5V_S3
C47 C46 C86 C87 C88 SC10U6D3V9MX-GP
C81 C83 C84 C85 C51 C52 SCD1U10V2KX-1GP SCD1U10V2KX-5GP

Place these Caps near SO-DIMMA.

<Core Design>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 12_DDR3-SODIMM1
Size: Custom
Document Number: LA46 MB DIS
Rev: -1
Date: Wednesday, January 27, 2010
Sheet 12 of 58

SA 0820

DM2

6 M_B_A[15..0]

M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14 M_B_A15

6 M_B_BS2

6 M_B_BS0
6 M_B_BS1

6 M_B_DQ[63..0]

M_B_DQ0 M_B_DQ1 M_B_DQ2 M_B_DQ3 M_B_DQ4 M_B_DQ5 M_B_DQ6 M_B_DQ7 M_B_DQ8 M_B_DQ9 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ13 M_B_DQ14 M_B_DQ15 M_B_DQ16 M_B_DQ17 M_B_DQ18 M_B_DQ19 M_B_DQ20 M_B_DQ21 M_B_DQ22 M_B_DQ23 M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ27 M_B_DQ28 M_B_DQ29 M_B_DQ30 M_B_DQ31 M_B_DQ32 M_B_DQ33 M_B_DQ34 M_B_DQ35 M_B_DQ36 M_B_DQ37 M_B_DQ38 M_B_DQ39 M_B_DQ40 M_B_DQ41 M_B_DQ42 M_B_DQ43 M_B_DQ44 M_B_DQ45 M_B_DQ46 M_B_DQ47 M_B_DQ48 M_B_DQ49 M_B_DQ50 M_B_DQ51 M_B_DQ52 M_B_DQ53 M_B_DQ54 M_B_DQ55 M_B_DQ56 M_B_DQ57 M_B_DQ58 M_B_DQ59 M_B_DQ60 M_B_DQ61 M_B_DQ62 M_B_DQ63

6 M_B_DQS#[7..0]

M_B_DQS#0 M_B_DQS#1 M_B_DQS#2 M_B_DQS#3 M_B_DQS#4 M_B_DQS#5 M_B_DQS#6 M_B_DQS#7

6 M_B_DQS[7..0]

M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7

6 M_ODT2
6 M_ODT3

M_VREF_CA_DIMM1
M_VREF_DQ_DIMM1

5,12 DDR3_DRAMRST#

MB_VTT
MB_VTT

DDR3-204P-51-GP
62.10017.P51
62.10017.P91

SB 1024 Change to 62.10017.P91

M_B_RAS# 6
M_B_WE# 6
M_B_CAS# 6

M_CS#2 6
M_CS#3 6

M_CKE2 6
M_CKE3 6

M_CLK_DDR2 6
M_CLK_DDR#2 6

M_CLK_DDR3 6
M_CLK_DDR#3 6

M_B_DM[7..0] 6

M_B_DM0 M_B_DM1 M_B_DM2 M_B_DM3 M_B_DM4 M_B_DM5 M_B_DM6 M_B_DM7

SODIMM1_1_SMB_DATA_R
SODIMM1_1_SMB_CLK_R

TS#_DIMM1

SA0_DIM1
SA1_DIM1

NC#1 NC#2 NC#/TEST

1D5V_S3

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18

VSS

SA 0902

1D5V_S3

R420 1KR2F-3-GP DY
R421 1KR2F-3-GP DY

DDR_VREF_S3

R419 0R0603-PAD

DIMM1_VREF_CADQ

-1 0114

-1 0107

R425 0R0603-PAD
R423 0R0603-PAD

C547 SCD1U10V2KX-5GP
C544 SCD1U10V2KX-5GP

C543 SC2D2U6D3V3KX-GP
C538 SC2D2U6D3V3KX-GP

M_VREF_CA_DIMM1
M_VREF_DQ_DIMM1

SB 1026 change to 78.22520.5BL

SC 1203

R38 0R0402-PAD

-1 0107

PM_EXTTS#1_R 5

3D3V_S0

R39 0R0402-PAD
R40 0R0402-PAD

PCH_SMBDATA 3,12,15
PCH_SMBCLK 3,12,15

C548 SCD1U10V2KX-5GP

C546 SC2D2U6D3V3KX-GP

SB 1026 change to 78.22520.5BL

3D3V_S0

R36 10KR2J-3-GP

R424 10KR2J-3-GP DY
R37 10KR2J-3-GP

SA1_DIM1
SA0_DIM1

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SODIMM B DECOUPLING

1D5V_S3

C45 C44 C535 C536 C537

C539 C540 C541 C542 C49 C50

0D75_S0

-1 0107

R41 0R0603-PAD

Place these caps close to VTT1 and VTT2.

C40 C41 C42 C43

H =8mm

SO-DIMMB is placed farther from the Processor than SO-DIMMA

<Core Design>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C

Title: 13_DDR3-SODIMM2

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 13 of 58

integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

SA 0906

SC-BOM Change to 6p
-1 0109 10ppm
check 20ppm + 5.6p

-1 0126 BOM Change

PCH: 71.0IBEX.G0U

HDD

ODD

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

CHECK

When unused all JTAG pins may be NC

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required

SB 1015 change to 83.00040.Q81
SB 1030 change to 83.00040.R81

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

Low: Flash Descriptor Security will be overridden

IBEXPEAK-M-GP-NF

SA-0914

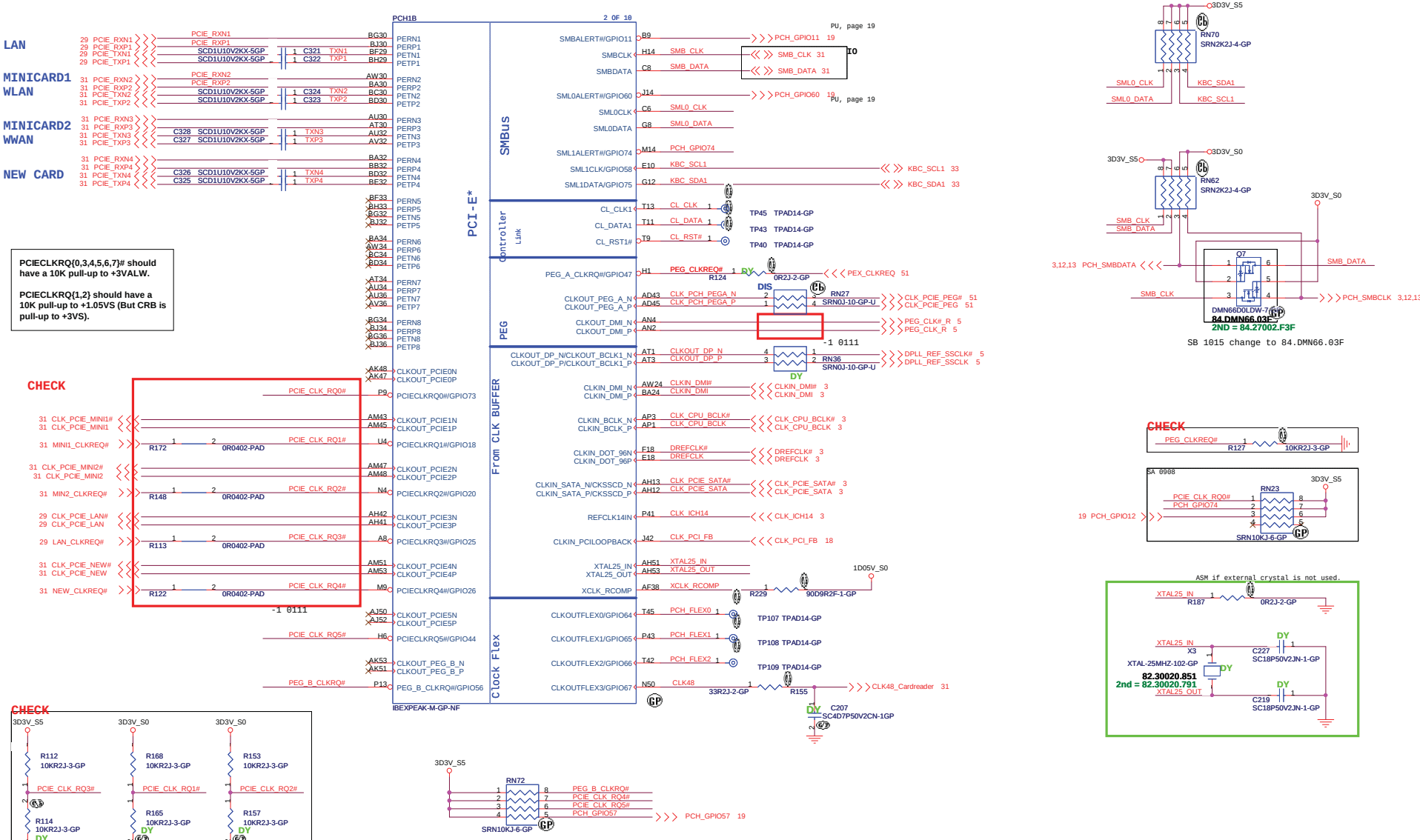
<Core Design>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 14_PCH (1/9)-SATA/SPI/LPC/HDA

Size	Document Number	Rev
Custom	LA46 MB DIS	-1

Date: Wednesday, January 27, 2010 Sheet 14 of 58

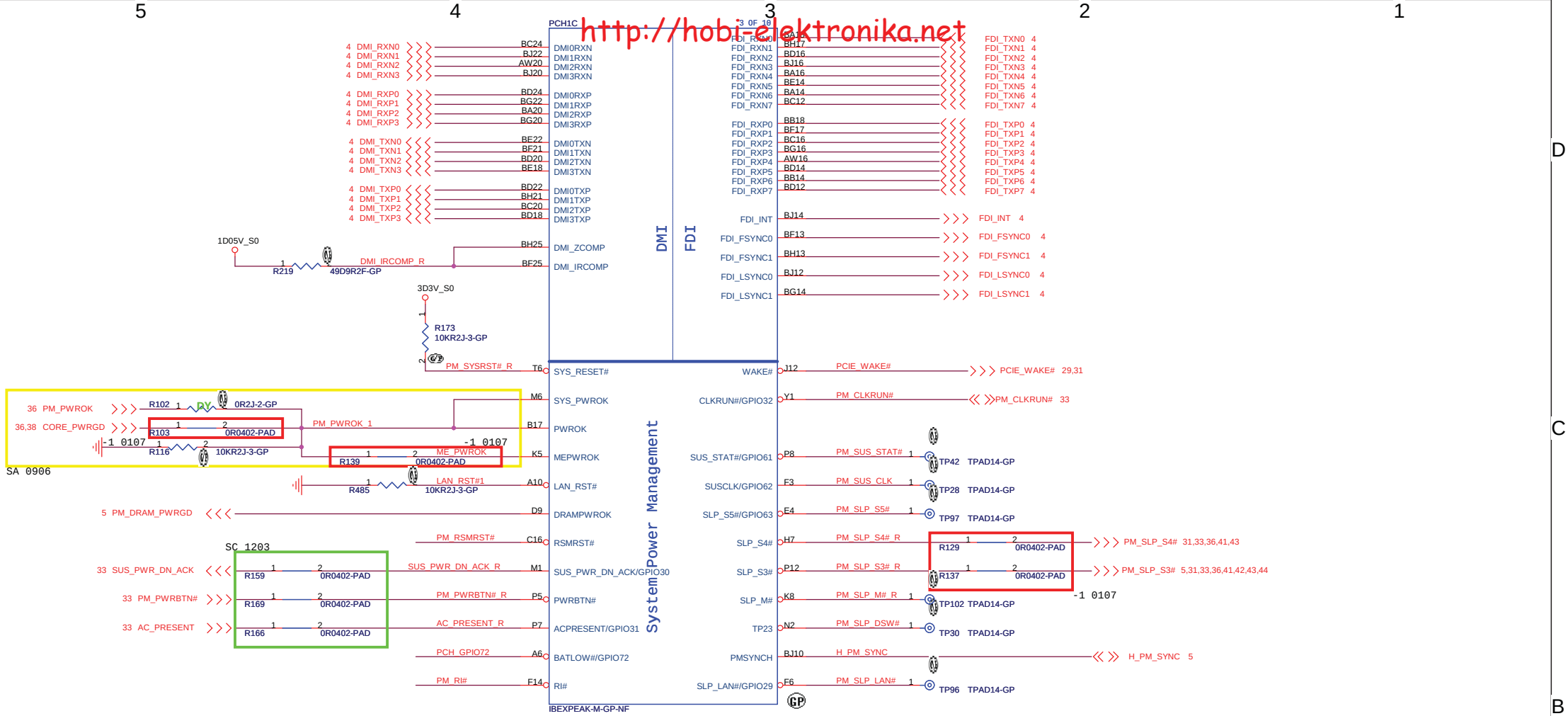


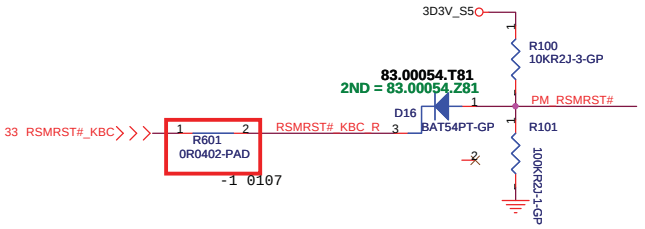
<Core Design>
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

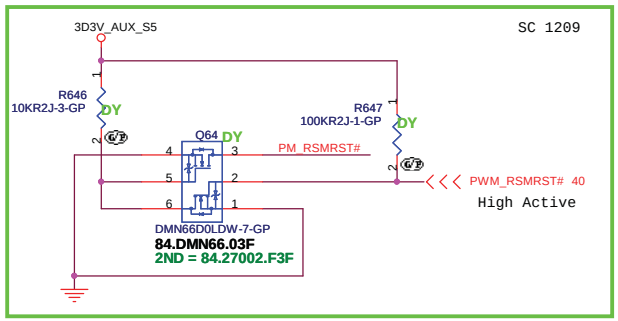
Title: 15_PCH (2/9)-PCIE / SMBUS / CLK

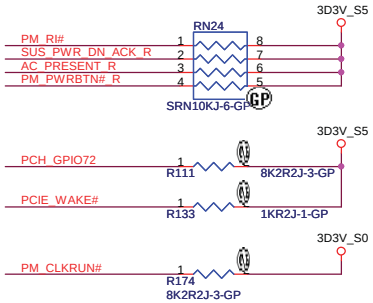
Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 15 of 58









<Core Design>
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 16_PCH (3/9)-DMI / FDI / PM

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 16 of 58

SA 0908 Add
3D3V_S0
RN22 SRN2K2J-1-GP
UMA
PCH_HDMI_CLK
PCH_HDMI_DATA

SA 0904 Add
3D3V_S0
RN67 SRN2K2J-1-GP
CLK_DDC_EDID
DAT_DDC_EDID

3D3V_S0
RN26 SRN10KJ-5-GP
LCTL_CLK
LCTL_DATA

R195 2K37R2F-GP
LIBG
LVDS reference current.

SA 0908 Add
R191 100KR2J-1-GP
PCH_HDMI_DETECT

SA 0904 Add
3D3V_S0
RN66 SRN2K2J-1-GP
PCH_DDCCLK
PCH_DDCDATA

RN29 SRN150F-1-GP
PCH_BLUE
PCH_GREEN
PCH_RED

Reserve PD at SW
23 PCH_BL_ON
24 PCH_LCDVDD_ON
24 L_BKLTCTL
23 CLK_DDC_EDID
23 DAT_DDC_EDID
TPAD14-GP TP44
R196 0R0402-PAD
LVDS_VREF
23 PCH_TXACLK-
23 PCH_TXACLK+
23 PCH_TXAOUT0-
23 PCH_TXAOUT1-
23 PCH_TXAOUT2-
23 PCH_TXAOUT0+
23 PCH_TXAOUT1+
23 PCH_TXAOUT2+
23 PCH_BLUE
23 PCH_GREEN
23 PCH_RED
25 PCH_DDCCLK
25 PCH_DDCDATA
25 PCH_HSYNC
25 PCH_VSYNC
R177 1KR2D-1-GP
1K 0.5% ohm
CRT_IREF
Intel check list recommend use 1K 0.5%

PCH1D
4 OF 10
T48 L_BKLTEN
T47 L_VDD_EN
Y48 L_BKLTCTL
AB48 L_DDC_CLK
Y45 L_DDC_DATA
AB46 L_CTRL_CLK
V48 L_CTRL_DATA
AP39 LVD_IBG
AP41 LVD_VBG
AT43 LVD_VREFH
AT42 LVD_VREFL
AV53 LVDSA_CLK#
AV51 LVDSA_CLK
BB47 LVDSA_DATA#0
BA52 LVDSA_DATA#1
AY48 LVDSA_DATA#2
AV47 LVDSA_DATA#3
BB48 LVDSA_DATA0
BA50 LVDSA_DATA1
AY49 LVDSA_DATA2
AV48 LVDSA_DATA3
AP48 LVDSB_CLK#
AP47 LVDSB_CLK
AY53 LVDSB_DATA#0
AT49 LVDSB_DATA#1
AU52 LVDSB_DATA#2
AT53 LVDSB_DATA#3
AY51 LVDSB_DATA0
AT48 LVDSB_DATA1
AU50 LVDSB_DATA2
AT51 LVDSB_DATA3
LVDS
AA52 CRT_BLUE
AB53 CRT_GREEN
AD53 CRT_RED
V51 CRT_DDC_CLK
V53 CRT_DDC_DATA
Y53 CRT_HSYNC
Y51 CRT_VSYNC
AD48 DAC_IREF
AB51 CRT_IRTN
CRT
IBEXPEAK-M-GP-NF

Digital Display Interface

SDVO_TVCLKINN BJ46
SDVO_TVCLKINP BG46
SDVO_STALLN BJ48
SDVO_STALLP BG48
SDVO_INTN BF45
SDVO_INTP BH45
SDVO_CTRLCLK T51 PCH_HDMI_CLK → PCH_HDMI_CLK 26
SDVO_CTRLDATA T53 PCH_HDMI_DATA → PCH_HDMI_DATA 26
DDPB_AUXN BG44
DDPB_AUXP BJ44
DDPB_HPD AU38 PCH_HDMI_DETECT → PCH_HDMI_DETECT 26
DDPB_0N BD42 PCH_HDMI_DATA2- L
DDPB_0P BC42 PCH_HDMI_DATA2+ L C288
DDPB_1N BJ42 PCH_HDMI_DATA1- L C289
DDPB_1P BC42 PCH_HDMI_DATA1+ L C286
DDPB_2N BB40 PCH_HDMI_DATA0- L C287
DDPB_2P BA40 PCH_HDMI_DATA0+ L C284
DDPB_3N AW38 PCH_HDMI_CLK- L C285
DDPB_3P BA38 PCH_HDMI_CLK+ L C283
C282
SCD1U10V2KX-5GP
→ PCH_HDMI_DATA2- 26
→ PCH_HDMI_DATA2+ 26
→ PCH_HDMI_DATA1- 26
→ PCH_HDMI_DATA1+ 26
→ PCH_HDMI_DATA0- 26
→ PCH_HDMI_DATA0+ 26
→ PCH_HDMI_CLK- 26
→ PCH_HDMI_CLK+ 26
DDPC_CTRLCLK Y49
DDPC_CTRLDATA AB49
DDPC_AUXN BE44
DDPC_AUXP BD44
DDPC_HPD AV40
DDPC_0N BE40
DDPC_0P BD40
DDPC_1N BF41
DDPC_1P BH41
DDPC_2N BD38
DDPC_2P BC38
DDPC_3N BB36
DDPC_3P BA36
DDPD_CTRLCLK U50
DDPD_CTRLDATA U52
DDPD_AUXN BC46
DDPD_AUXP BD46
DDPD_HPD AT38
DDPD_0N BJ40
DDPD_0P BG40
DDPD_1N BJ38
DDPD_1P BG38
DDPD_2N BF37
DDPD_2P BH37
DDPD_3N BE36
DDPD_3P BD36
GP

<Core Design>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 17_PCH (4/9)-LVDS / CRT
Size: A3
Document Number: LA46 MB DIS
Rev: -1
Date: Tuesday, January 26, 2010
Sheet 17 of 58

These pins are left as NC, because the function is disable.

These pins are left as NC, because the function is disable.

SB 1015 R105 change to ASM

SC 1208, BOM Change to 20ohm for fine tune USB signal

-1 0114

DMI Termination Voltage

NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

Pair	Device
0	NC
1	USB3
2	USB1
3	WLAN
4	Card Reader
5	WWAN
6	Disable (HM55)
7	Disable (HM55)
8	USB2
9	Blue Tooth
10	Finger Print
11	NC
12	Express Card
13	Camera

BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

OC#0	Port 0 & 1	EHCI 1
OC#1	Port 2 & 3	
OC#2	Port 4 & 5	
OC#3	Port 6 & 7	
OC#4	Port 8 & 9	EHCI 2
OC#5	Port 10 & 11	
OC#6	Port 12 & 13	
OC#7	Floater OC# (not used)	

<Core Design>

Wistron Corporation
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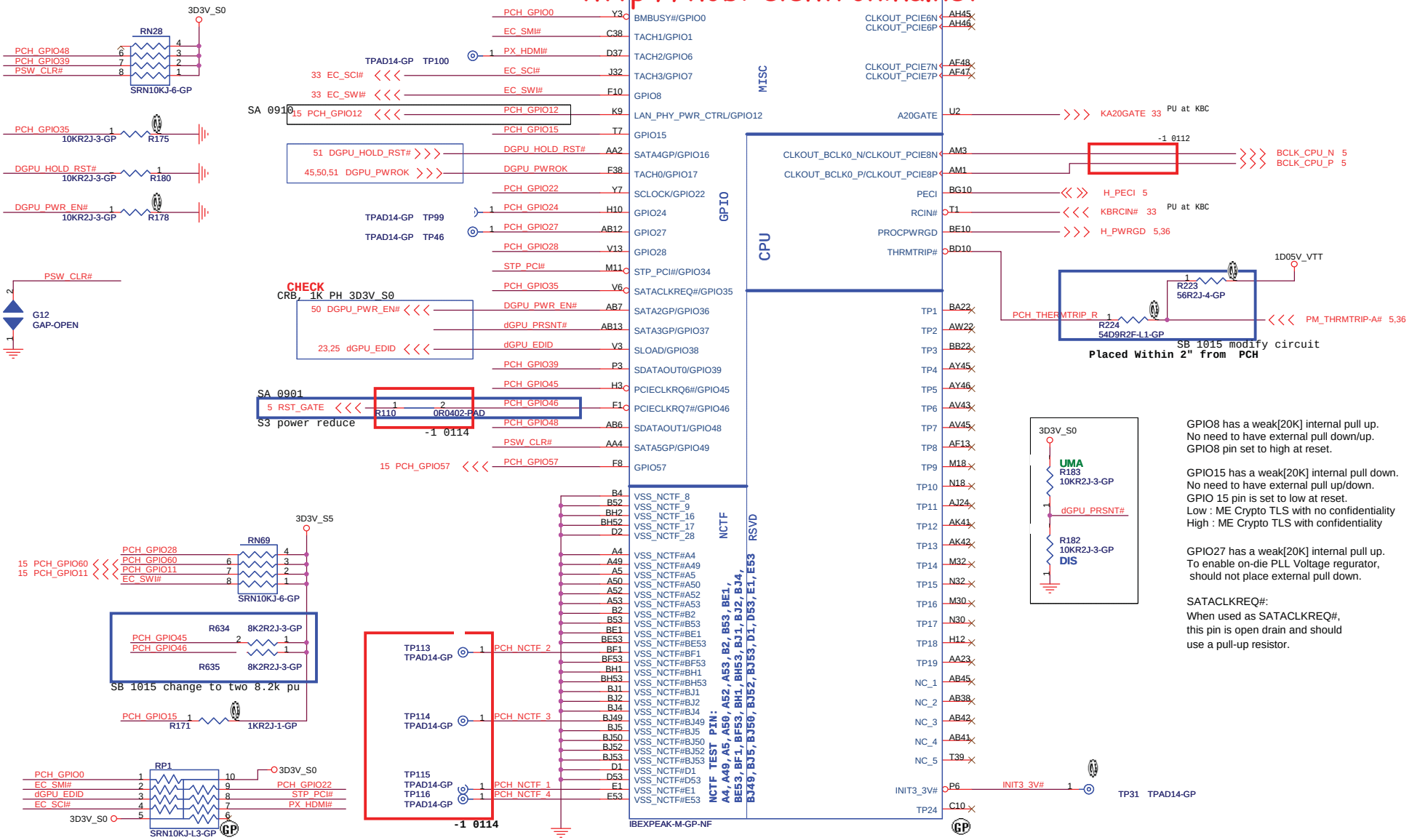
Taipei Hsien 221, Taiwan, R.O.C

Title: 18_PCH (5/9)-PCI / USB

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 18 of 58



GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

SATACLKREQ#:
When used as SATACLKREQ#,
this pin is open drain and should
use a pull-up resistor.

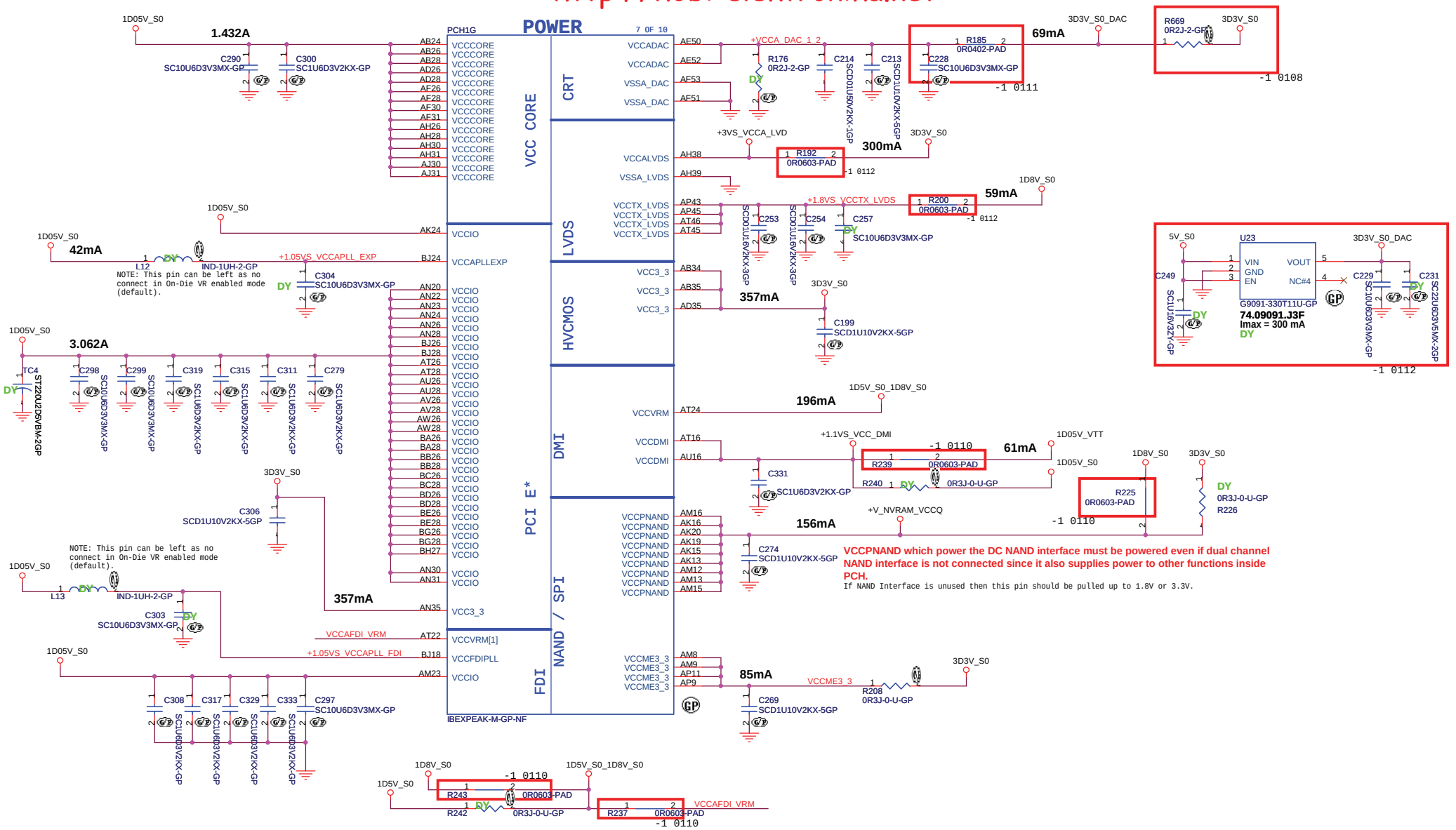
<Core Design>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 19_PCH (6/9)-GPIO/VSS_NCTF/RSVD

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 19 of 58



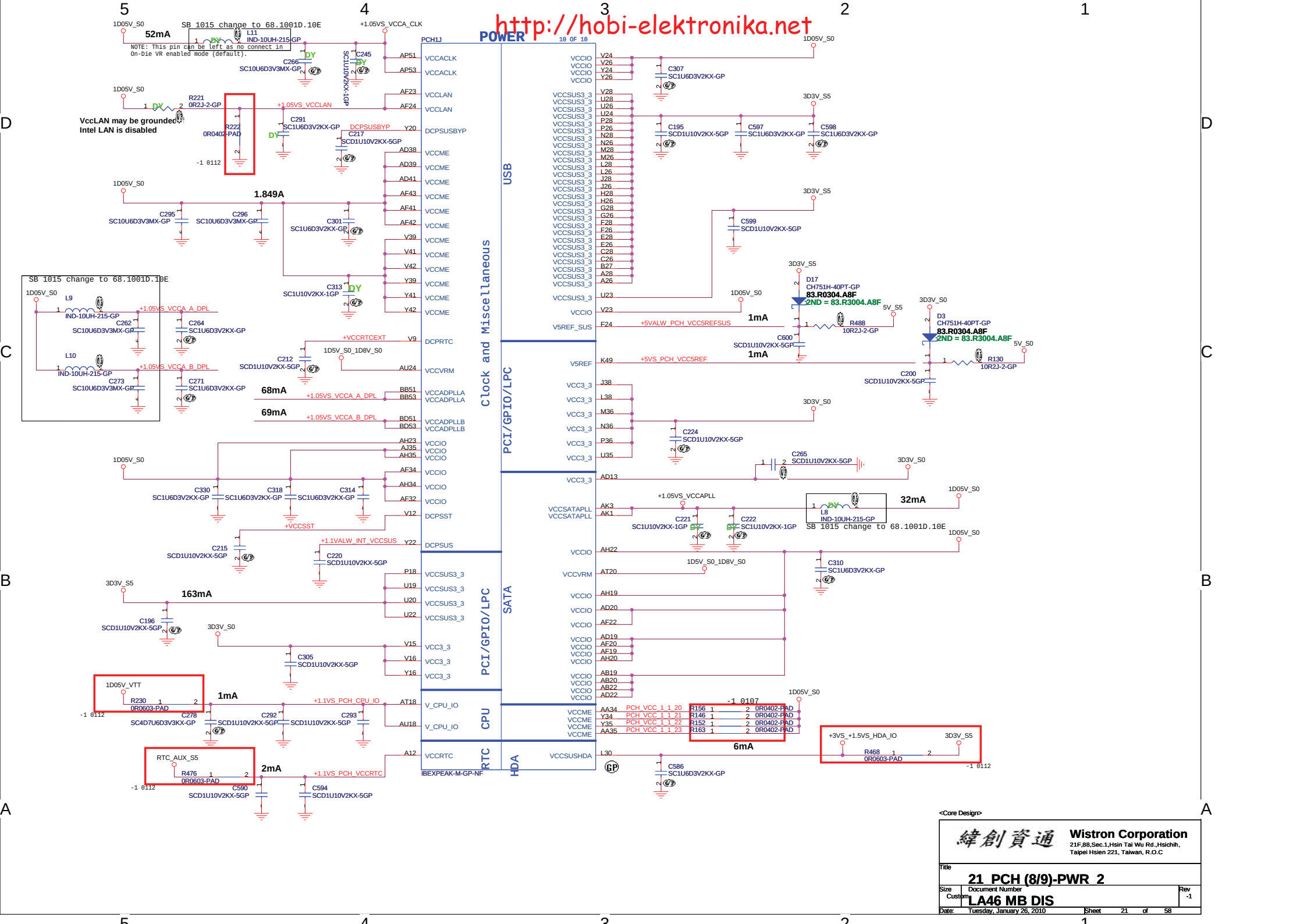
<Core Design>

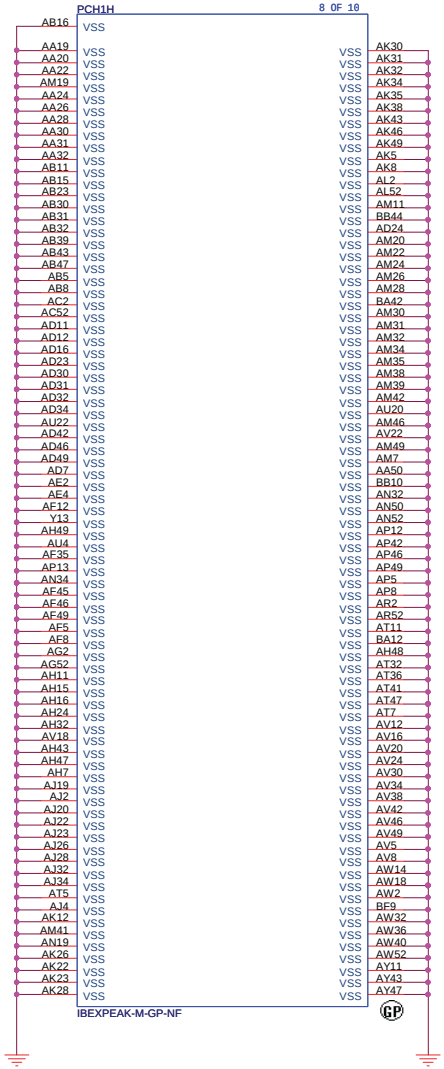
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

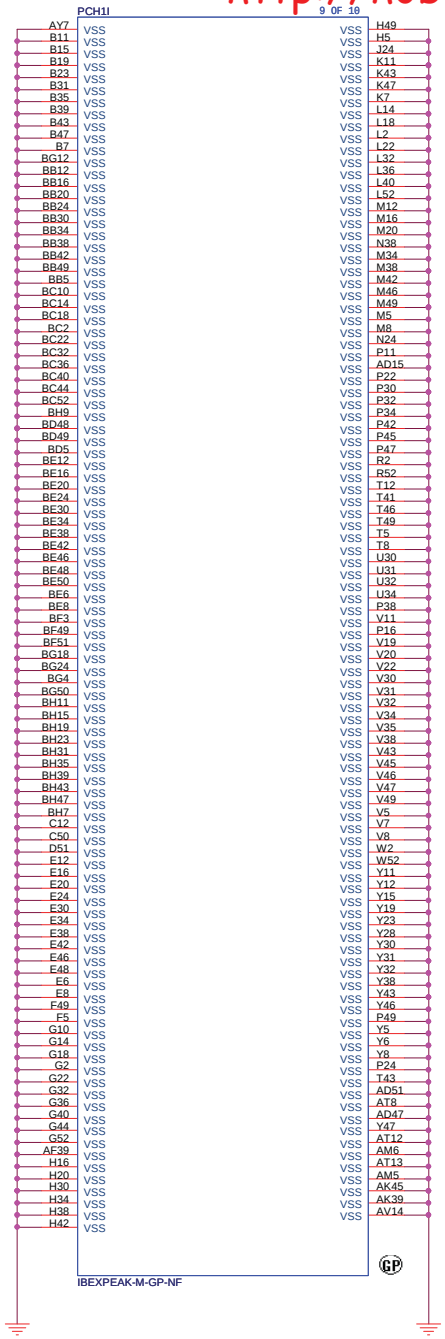
Title: 20_PCH (7/9)-PWR_1

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 20 of 58







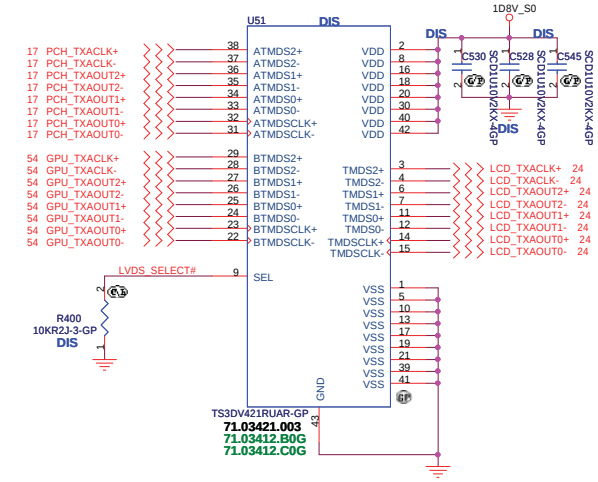
<Core Design>

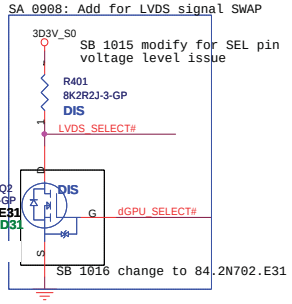
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

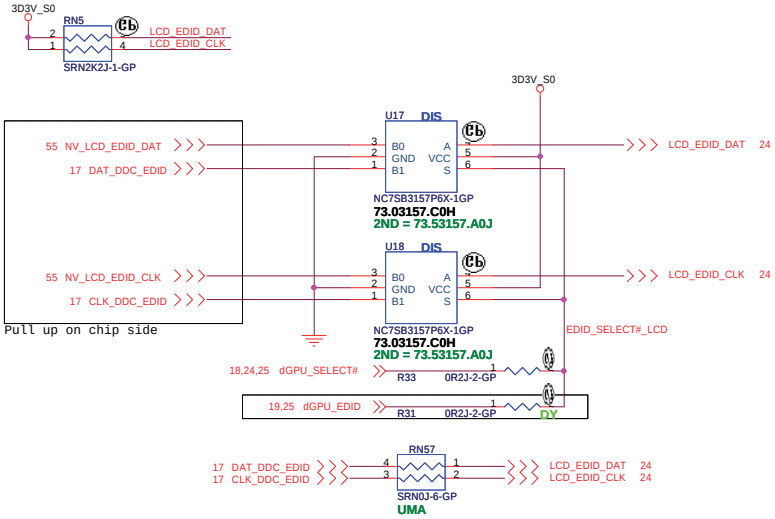
Title: 22_PCH (9/9)-VSS

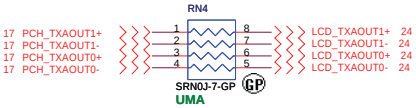
Size: Custom | Document Number: LA46 MB DIS | Rev: -1

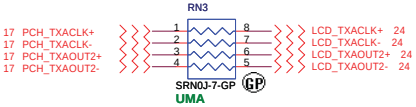
Date: Tuesday, January 26, 2010 | Sheet 22 of 58

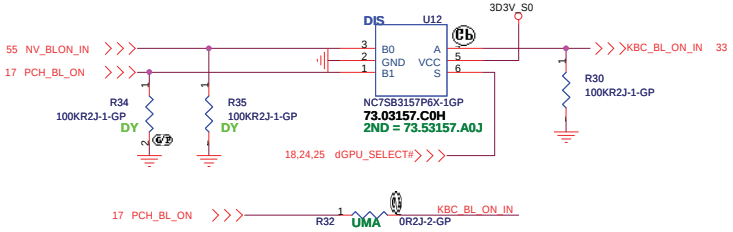


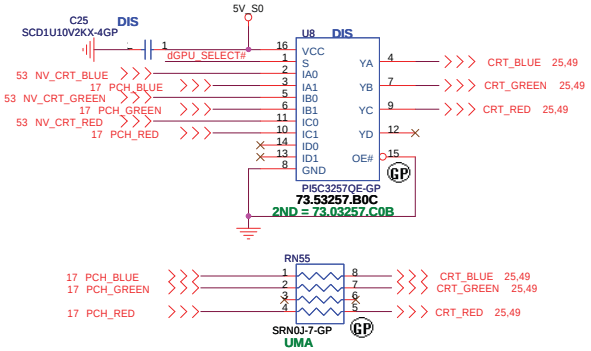












FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

<Core Design>

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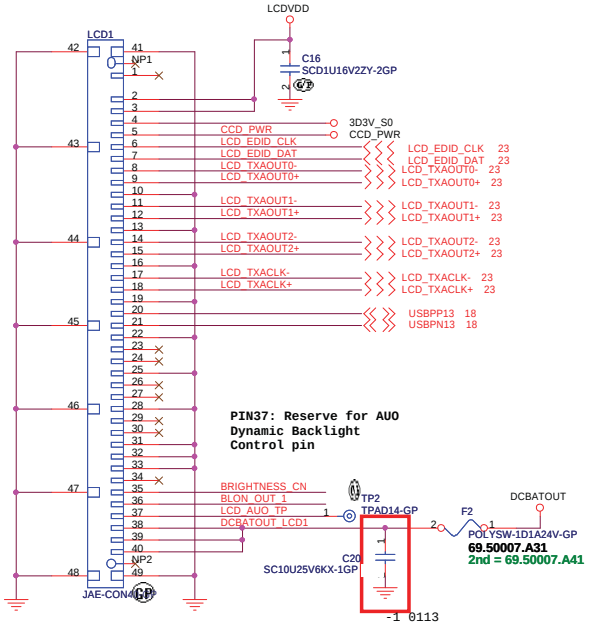
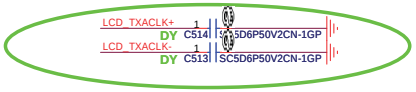
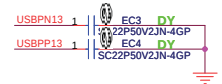
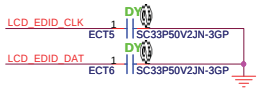
Title: 23_Display MUX
Size: Custom | Document Number: LA46 MB DIS | Rev: -1
Date: Tuesday, January 26, 2010 | Sheet 23 of 58

LCD/INVERTER/CCD CONN

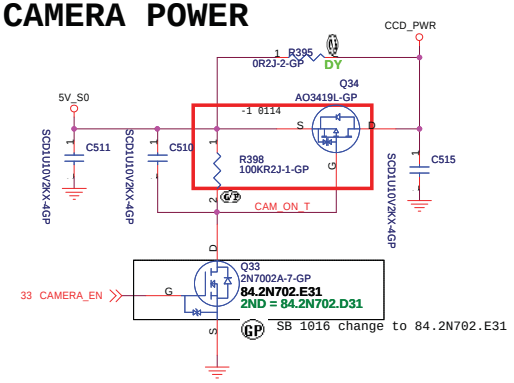


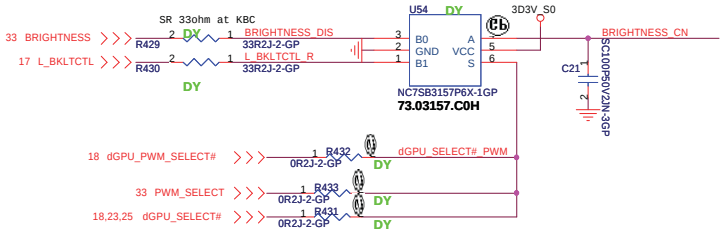


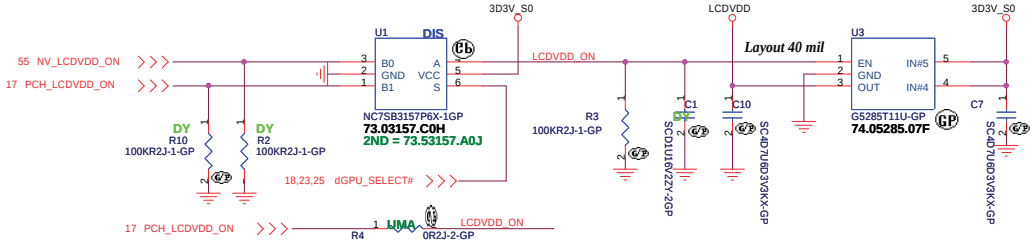


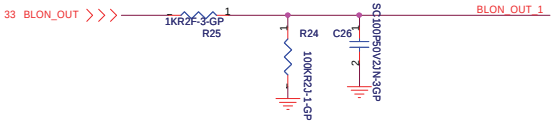


CAMERA POWER









<Core Design>
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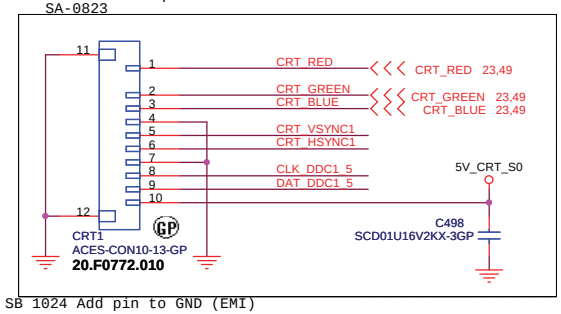
Title: 24_LCD & CCD
Size: Custom | Document Number: LA46 MB DIS | Rev: -1
Date: Tuesday, January 26, 2010 | Sheet 24 of 58

SA-0820 Move pi filter to CRT board.
SA-0823



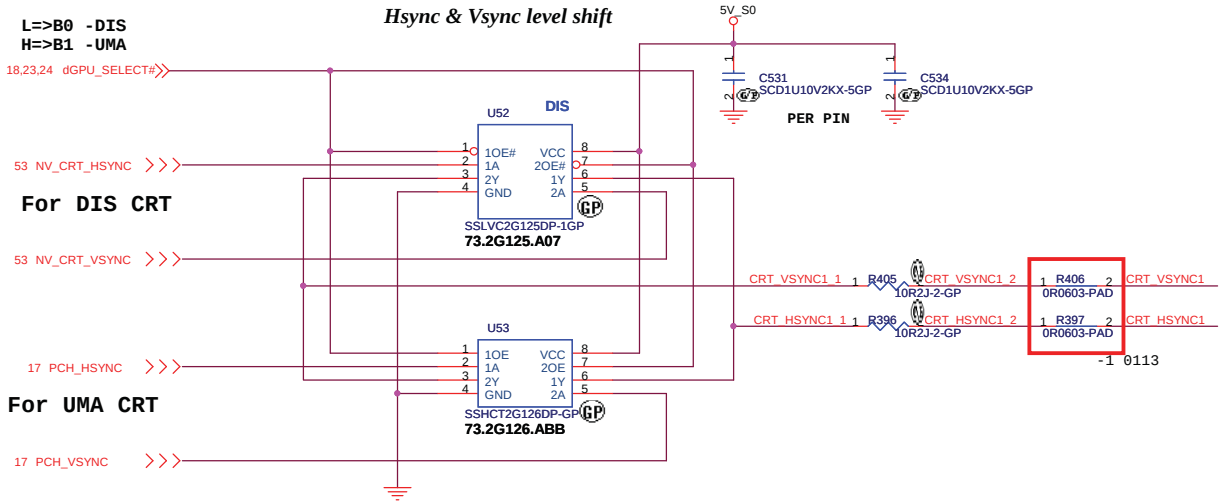
SB 1024 Add pin to GND (EMI)

CLK_DDC1_5 → CLK_DDC1_5 49
DAT_DDC1_5 → DAT_DDC1_5 49

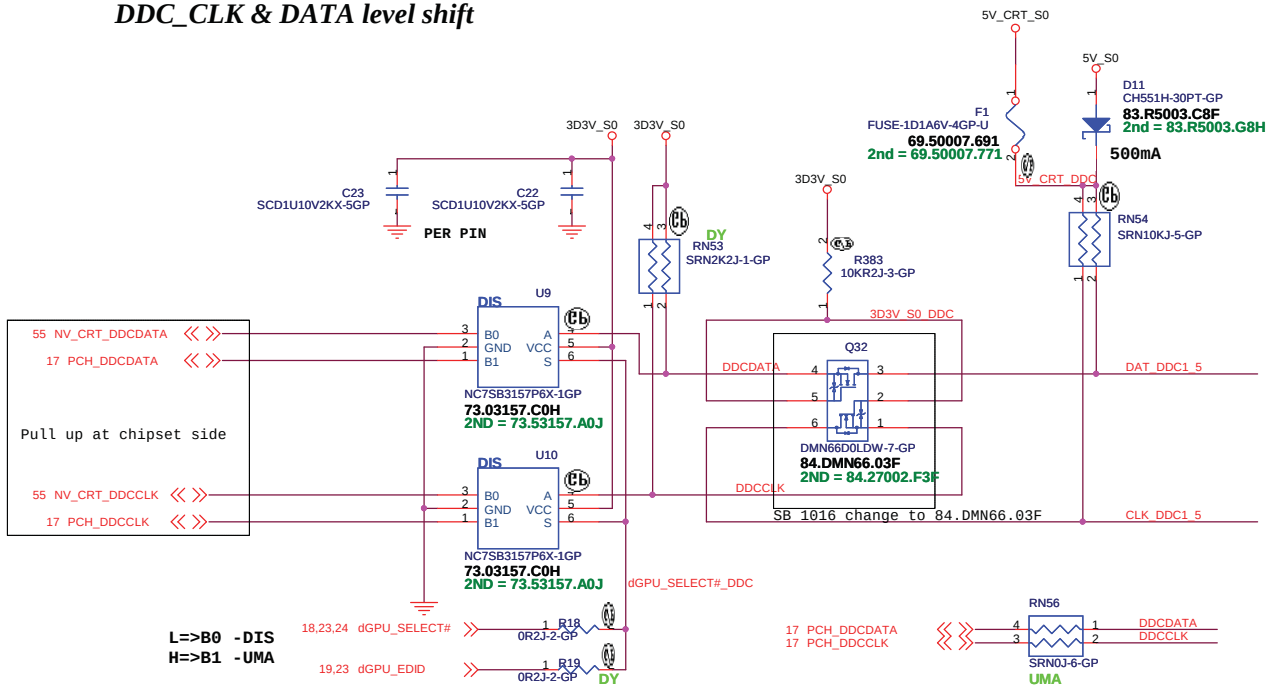
CRT_VSYNC1 → CRT_VSYNC1 49
CRT_HSYNC1 → CRT_HSYNC1 49

Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA



DDC_CLK & DATA level shift



<Core Design>

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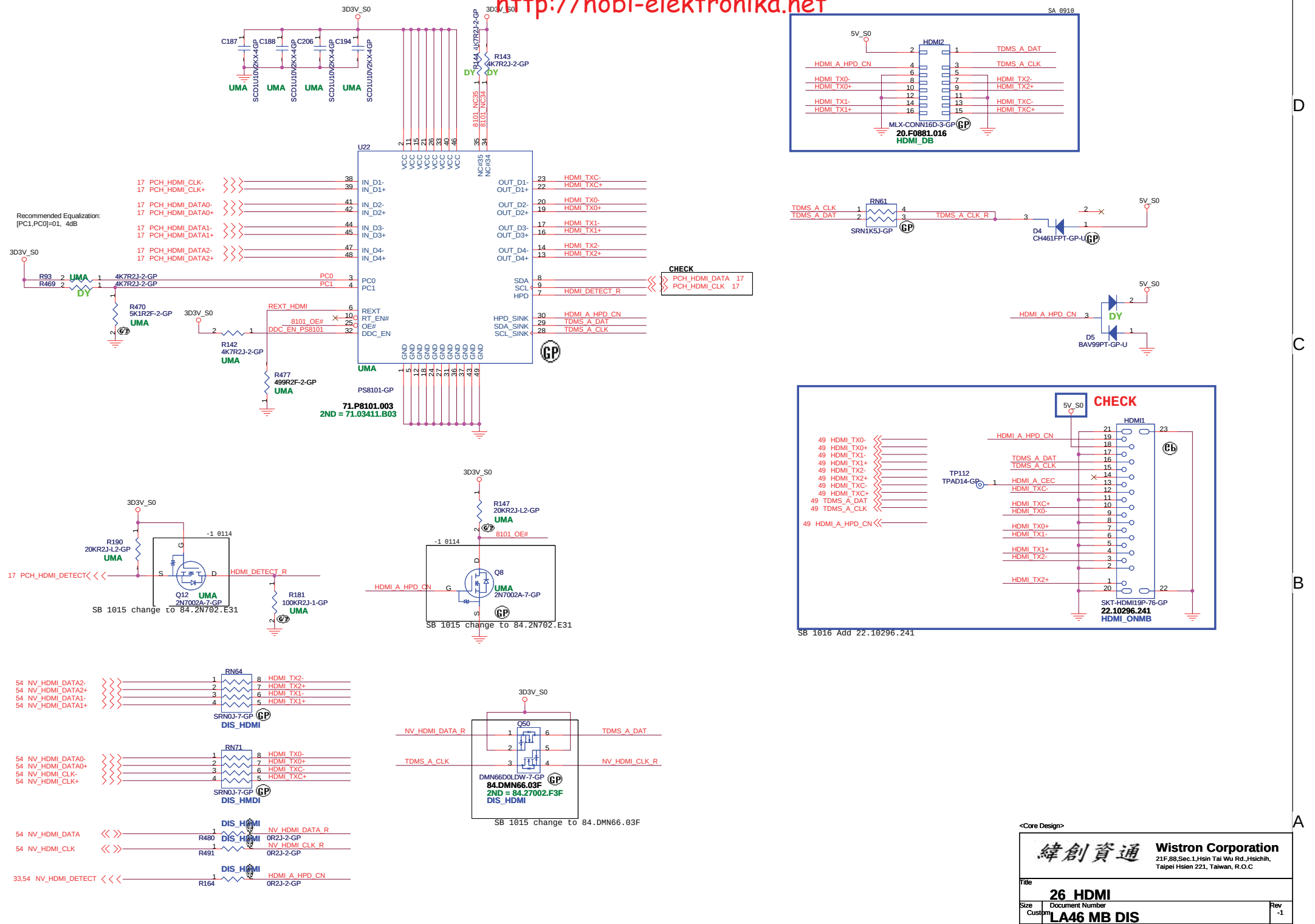
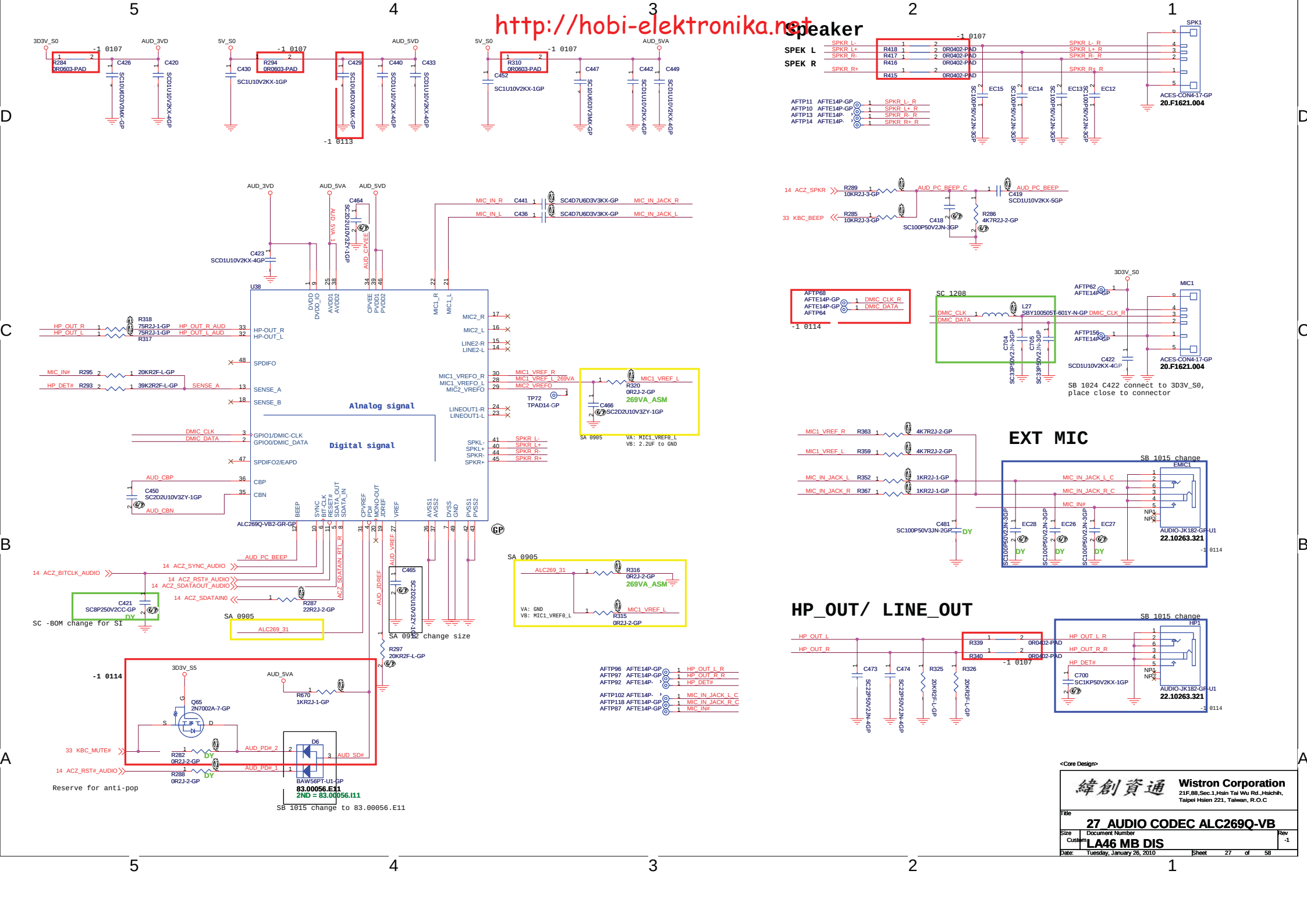
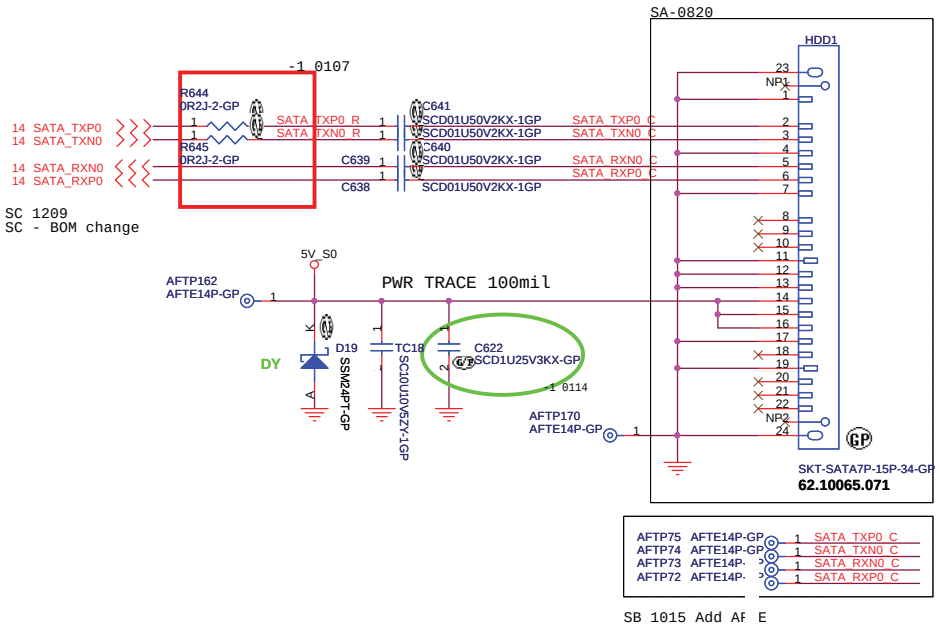
Title: 25_CRT
Size: A3
Document Number: LA46 MB DIS
Rev: -1
Date: Tuesday, January 26, 2010
Sheet 25 of 58

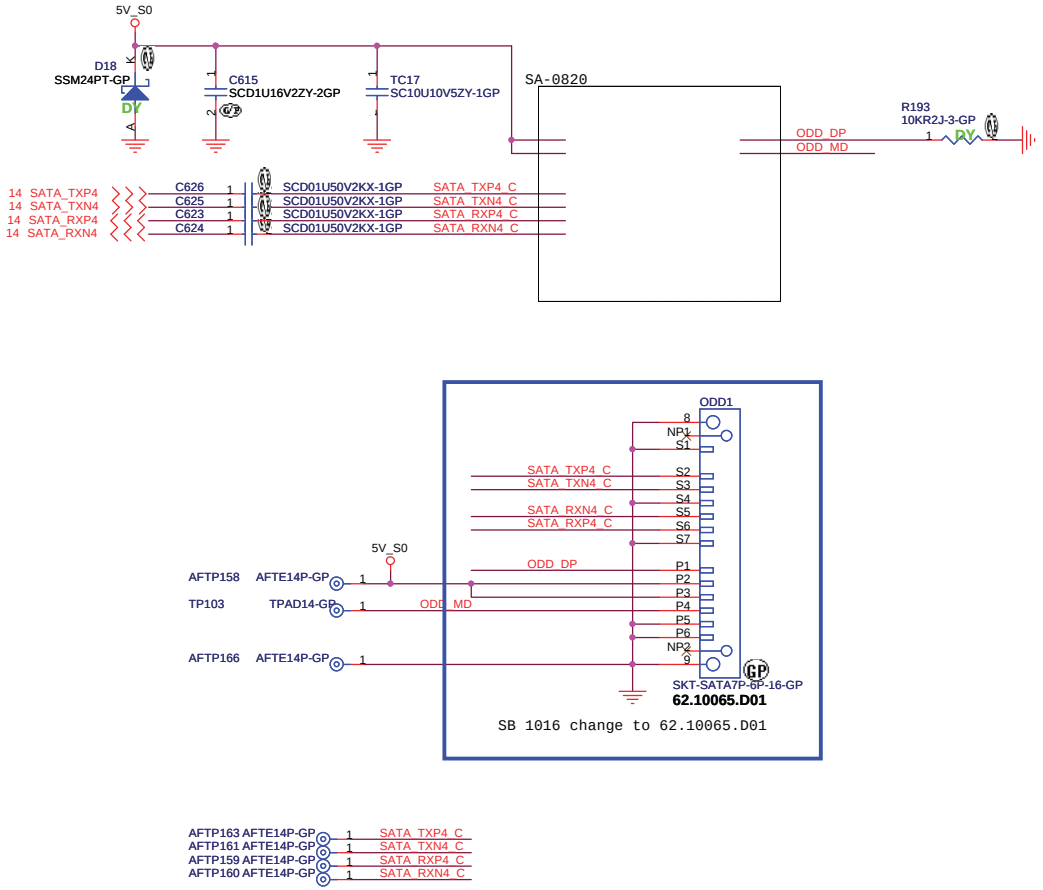




SATA Connector



ODD Connector



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Title: 28_HDD & ODD

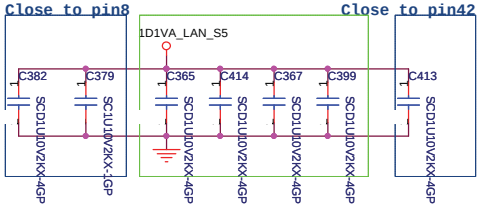
Size: A3 | Document Number: LA46 MB DIS | Rev: -1

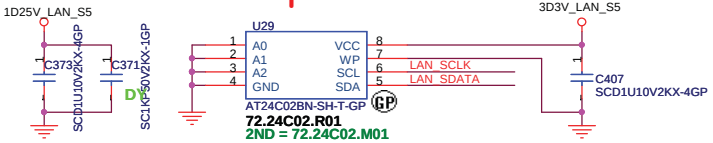
Date: Tuesday, January 26, 2010 | Sheet 28 of 58

Close to pin16,pin22,pin36,pin39

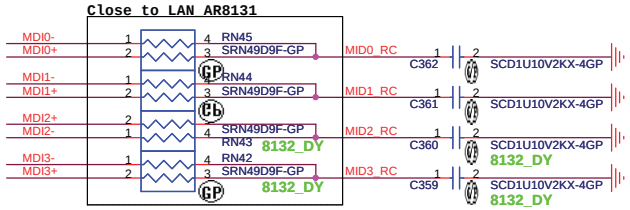
Close to pin8

Close to pin42



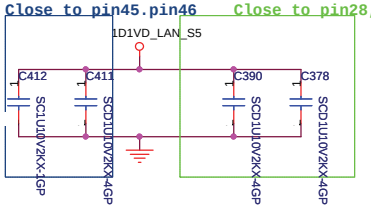


Close to LAN AR8131

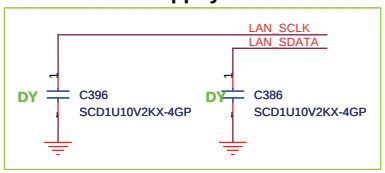


Close to pin45.pin46

Close to pin28,pin32

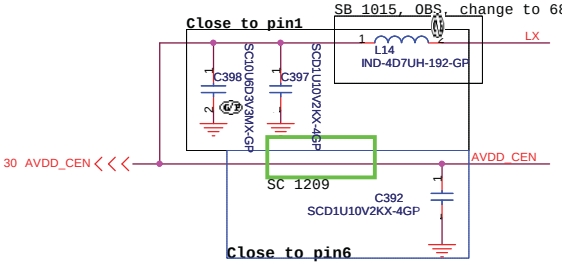


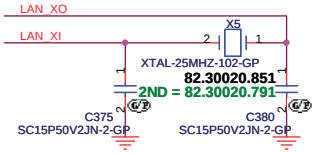
for AR8131M apply in the future



SB_1015, OBS, change to 68.4R750.20C

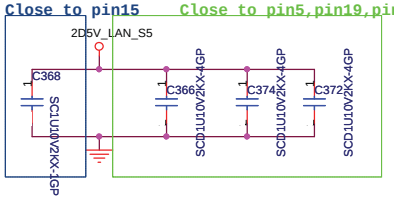
Close to pin1



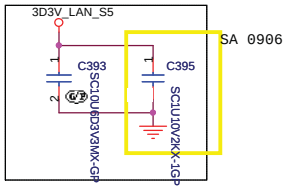


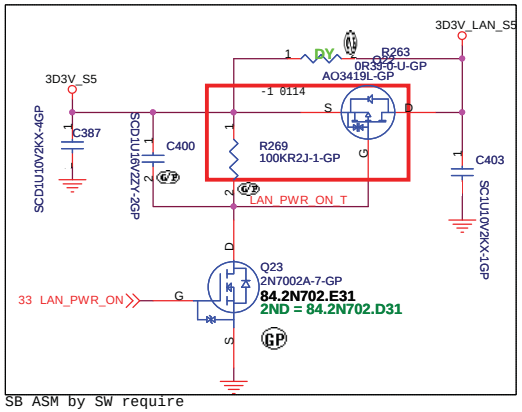
Close to pin15

Close to pin5,pin19,pin25

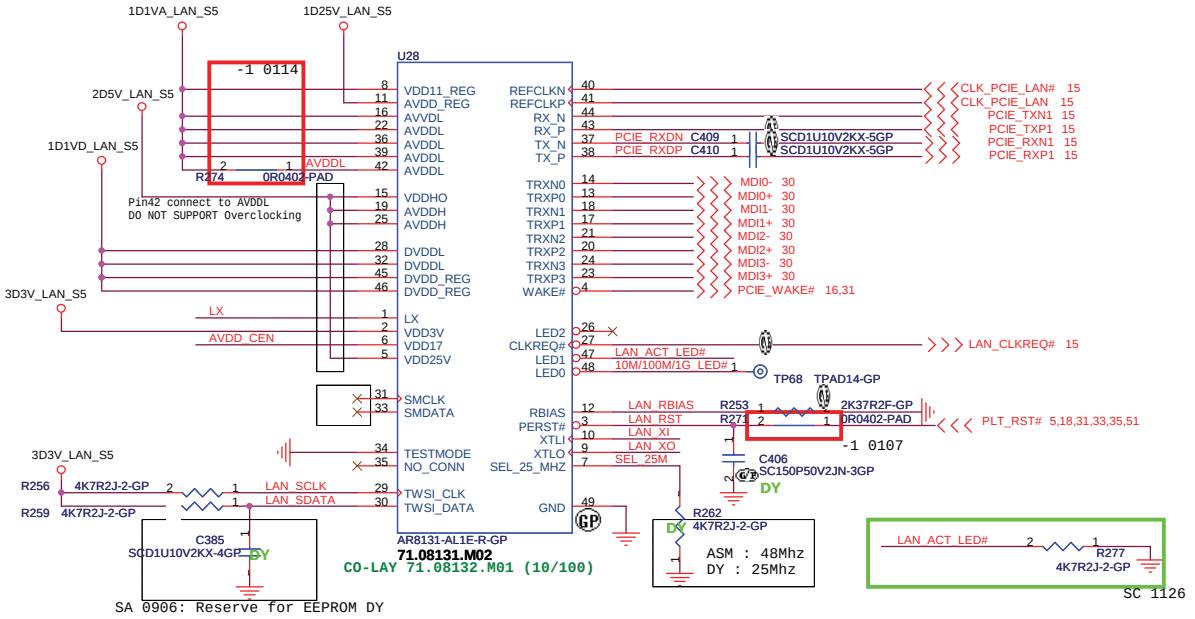


Close to pin2





SB ASM by SW require



SA 0906: Reserve for EEPROM DY

<Core Design>

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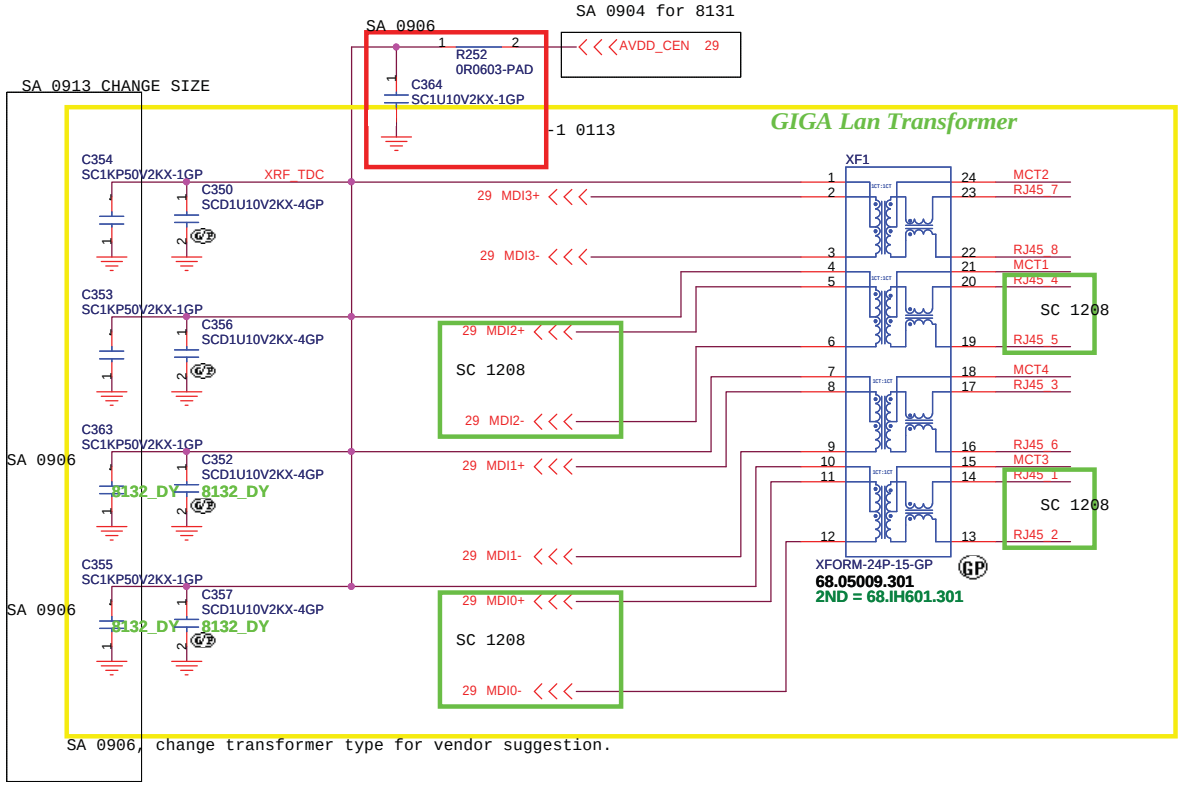
Title: 29_LAN AR8131/8132

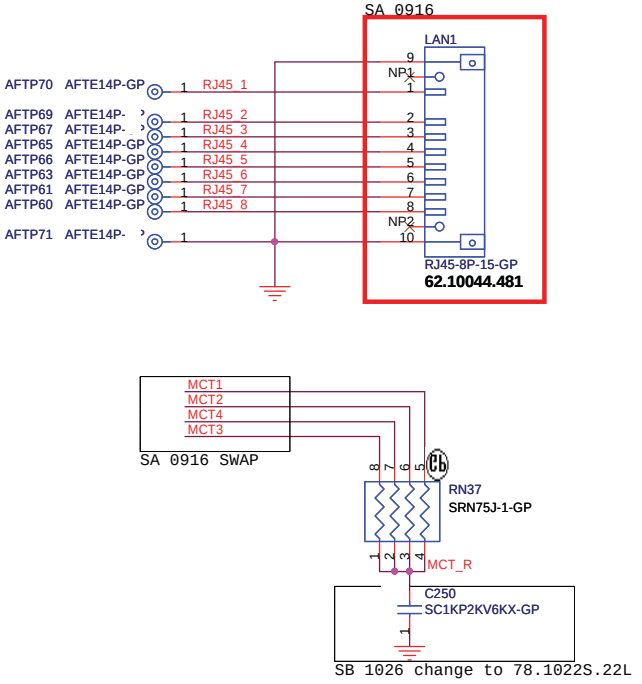
Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 29 of 58

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector





<Core Design>

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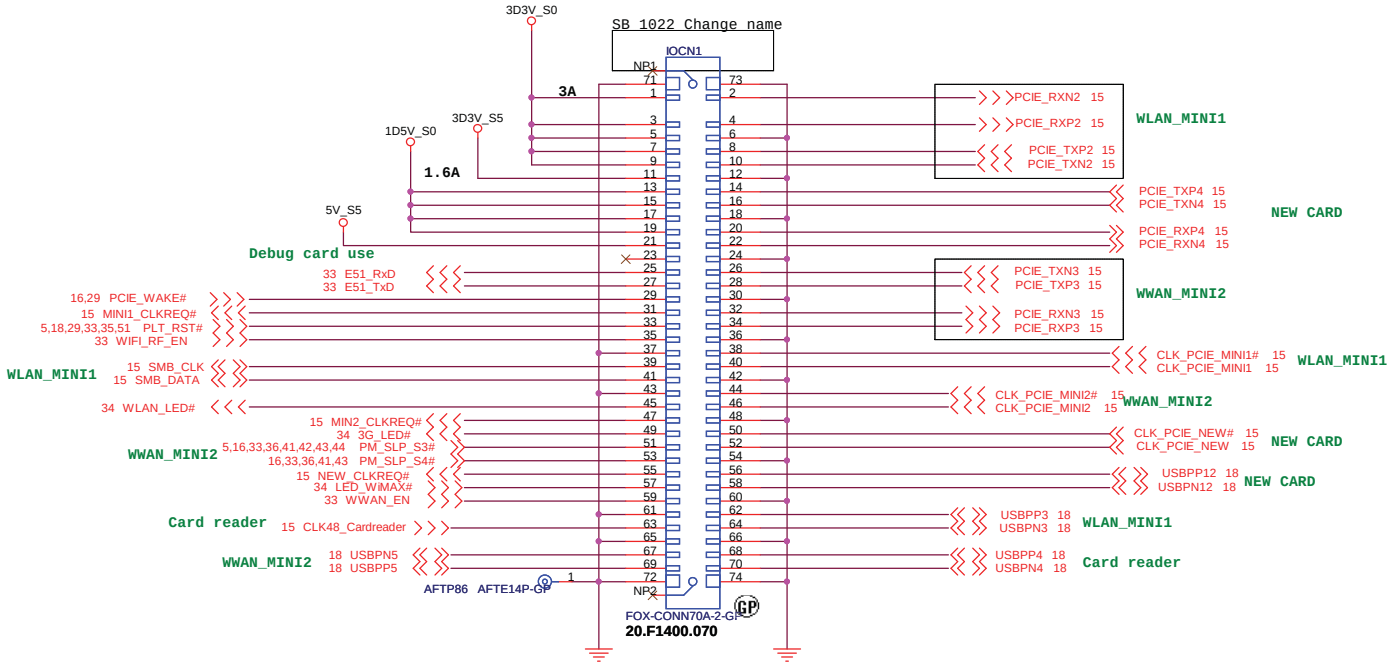
Title	30 LAN CONN	
Size: Custom	Document Number: LA46 MB DIS	Rev: -1
Date: Tuesday, January 26, 2010	Sheet 30 of 58	



AFTP107 AFTE14P-GP 1 3D3V_S0
AFTP103 AFTE14P- 1 3D3V_S5
AFTP104 AFTE14P-GP 1 1D5V_S0
AFTP99 AFTE14P- 1 5V_S5

AFTP98 AFTE14P-GP 1 E51_RxD
AFTP93 AFTE14P-GP 1 E51_TxD
AFTP91 AFTE14P- 1 PCIE_WAKE#
AFTP84 AFTE14P- 1 MINI1_CLKREQ#
AFTP190 AFTE14P-GP 1 CLK_PCIE_MINI1#
AFTP188 AFTE14P- 1 CLK_PCIE_MINI1
AFTP109 AFTE14P- 1 PCIE_RXN2
AFTP108 AFTE14P- 1 PCIE_RXP2
AFTP105 AFTE14P- 1 PCIE_TXN2
AFTP106 AFTE14P-GP 1 PCIE_TXP2
AFTP185 AFTE14P- 1 PLT_RST#
AFTP184 AFTE14P- 1 WIFI_RF_EN
AFTP182 AFTE14P-GP 1 SMB_CLK
AFTP181 AFTE14P- 1 SMB_DATA
AFTP180 AFTE14P- 1 WLAN_LED#
AFTP178 AFTE14P- 1 MIN2_CLKREQ#
AFTP187 AFTE14P- 1 USBPN3
AFTP189 AFTE14P-GP 1 USBPP3
AFTP177 AFTE14P- 1 CLK_PCIE_MINI2#
AFTP179 AFTE14P- 1 CLK_PCIE_MINI2

AFTP194 AFTE14P-GP 1 USBPP4
AFTP193 AFTE14P-GP 1 USBPN4
AFTP176 AFTE14P-GP 1 CLK48_Cardreader
AFTP101 AFTE14P-GP 1 PCIE_TXP4
AFTP100 AFTE14P- 1 PCIE_TXN4
AFTP95 AFTE14P- 1 PCIE_RXP4
AFTP94 AFTE14P-GP 1 PCIE_RXN4
AFTP174 AFTE14P-GP 1 CLK_PCIE_NEW
AFTP173 AFTE14P- 1 CLK_PCIE_NEW#
AFTP80 AFTE14P- 1 USBPP12
AFTP79 AFTE14P- 1 USBPN12
AFTP81 AFTE14P-GP 1 3G_LED#
AFTP78 AFTE14P- 1 PM_SLP_S3#
AFTP82 AFTE14P- 1 PM_SLP_S4#
AFTP83 AFTE14P- 1 NEW_CLKREQ#
AFTP89 AFTE14P- 1 PCIE_TXN3
AFTP88 AFTE14P-GP 1 PCIE_TXP3
AFTP90 AFTE14P- 1 PCIE_RXN3
AFTP85 AFTE14P- 1 PCIE_RXP3
AFTP192 AFTE14P- 1 USBPN5
AFTP191 AFTE14P- 1 USBPP5
AFTP77 AFTE14P-GP 1 LED_WiMAX#
AFTP76 AFTE14P- 1 WWAN_EN

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

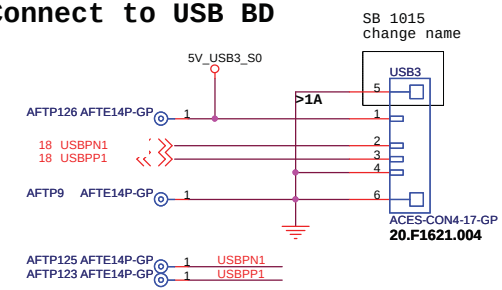
Title: 31_IO CONN

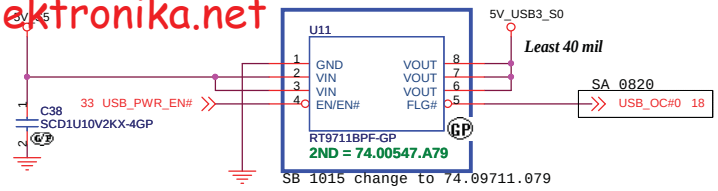
Size	Document Number	Rev
A3	LA46 MB DIS	-1

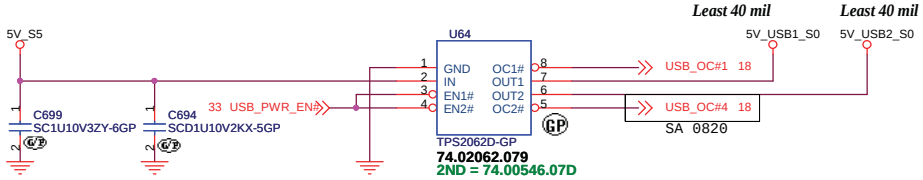
Date: Tuesday, January 26, 2010 Sheet 31 of 58

USB3

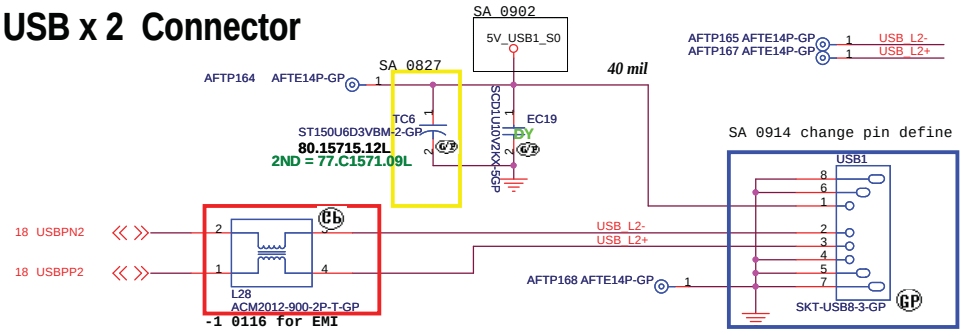
Connect to USB BD

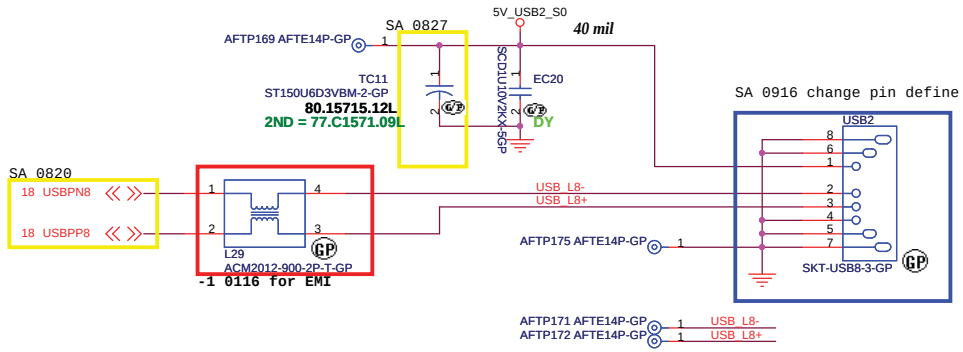




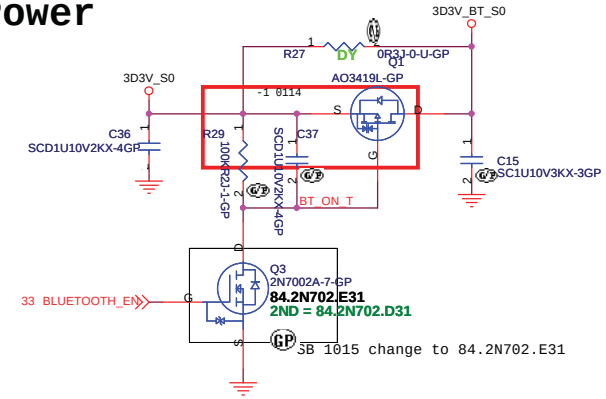


USB x 2 Connector

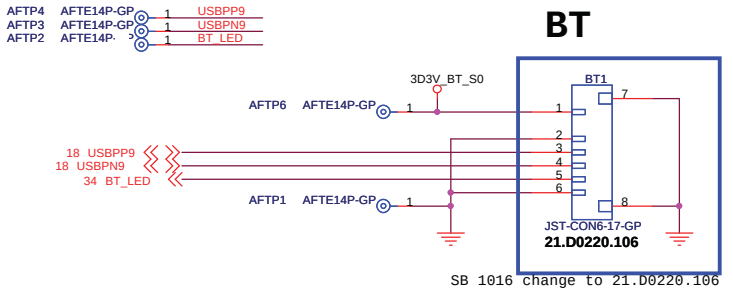




Bluetooth Power



BT



Pin	Pin Name
1	V3V3
2	GND
3	USB D+
4	USB D-
5	LINK_IND

<Core Design>

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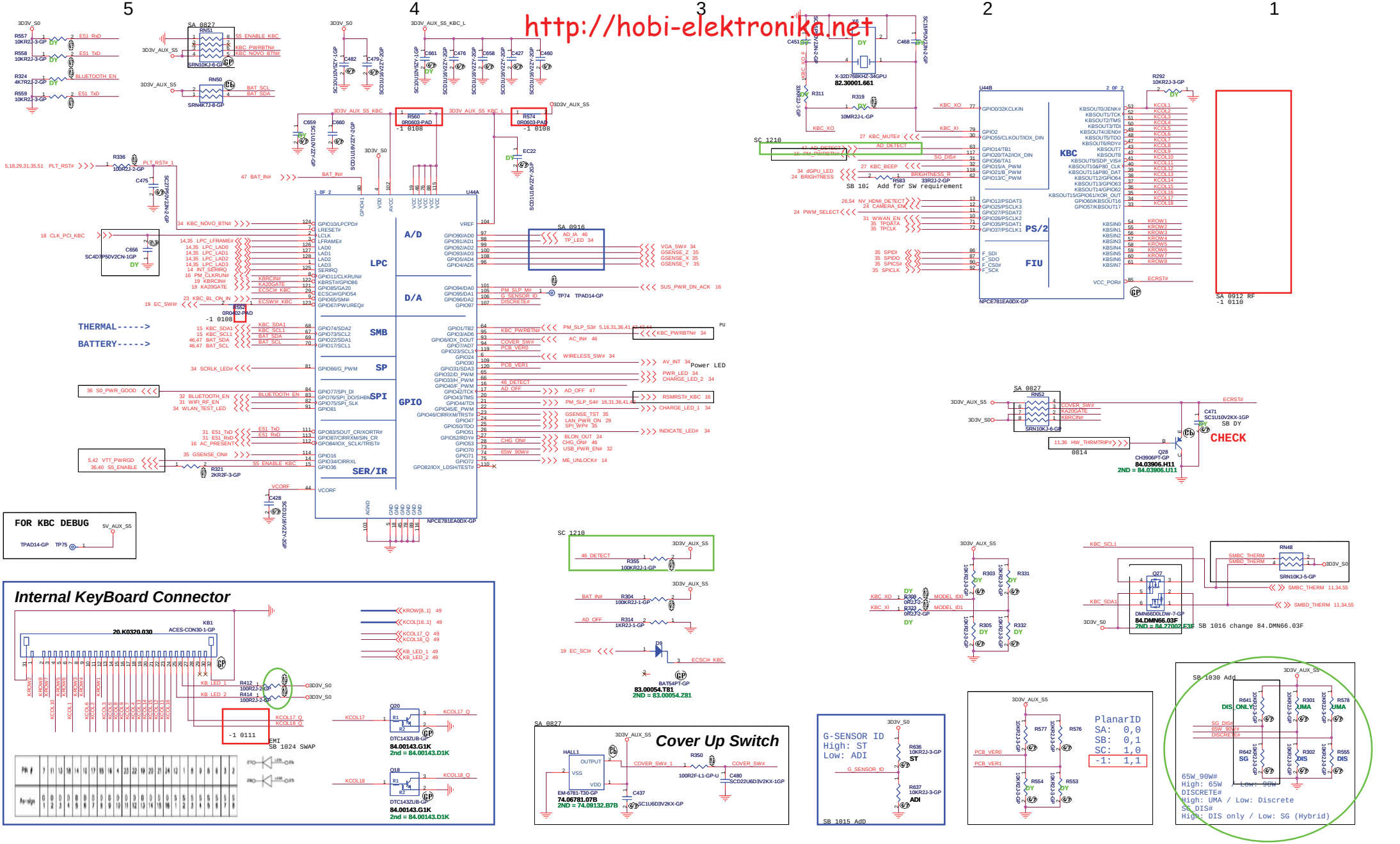
Title: 32_USB & BT

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 32 of 58



<Core Design>
緯創資通 Wistron Corporation
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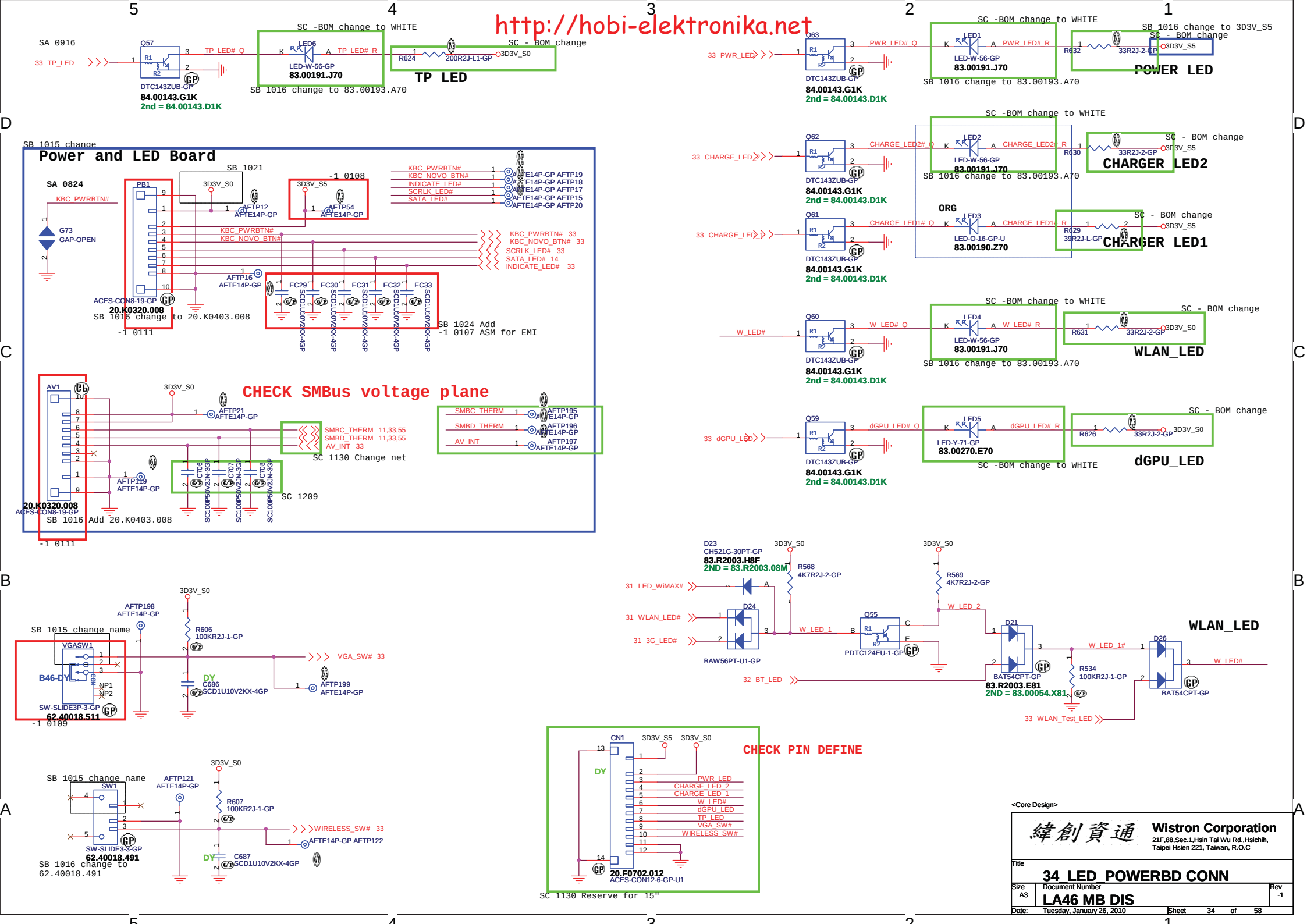
Taipei Hsien 221, Taiwan, R.O.C

Title: 33_KBC_NPCE781E

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 33 of 58



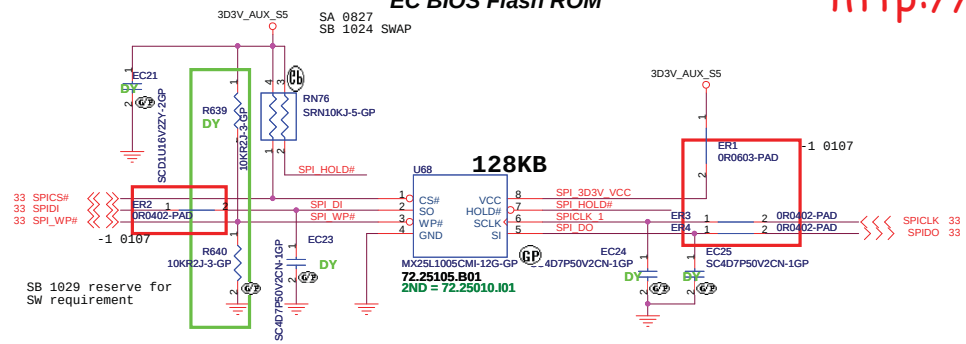
<Core Design>
緯創資通
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 34_LED_POWERBD CONN

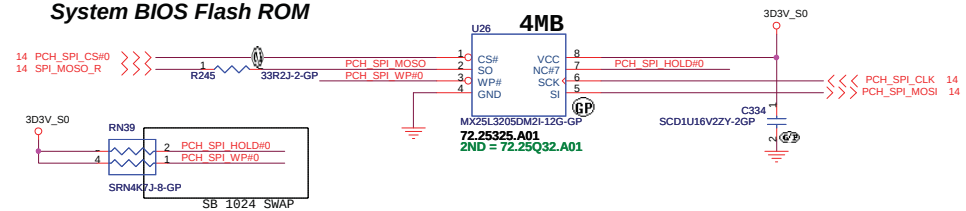
Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 34 of 58

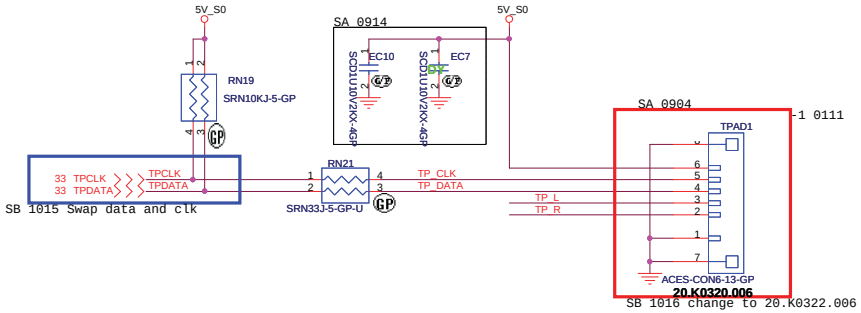
EC BIOS Flash ROM

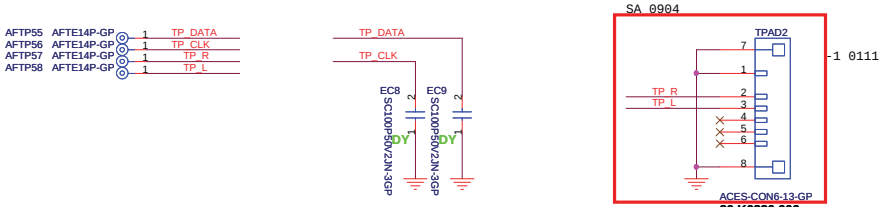


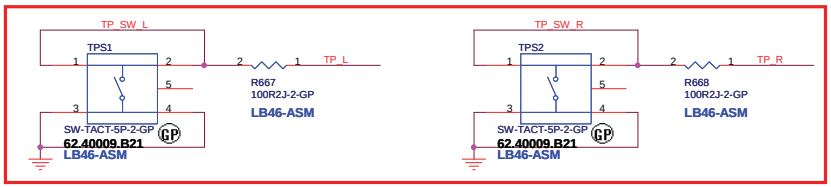
System BIOS Flash ROM



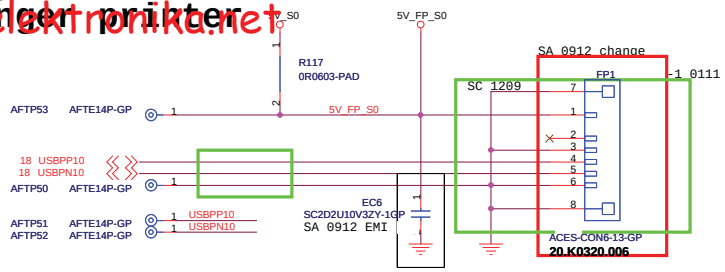
TOUCH PAD



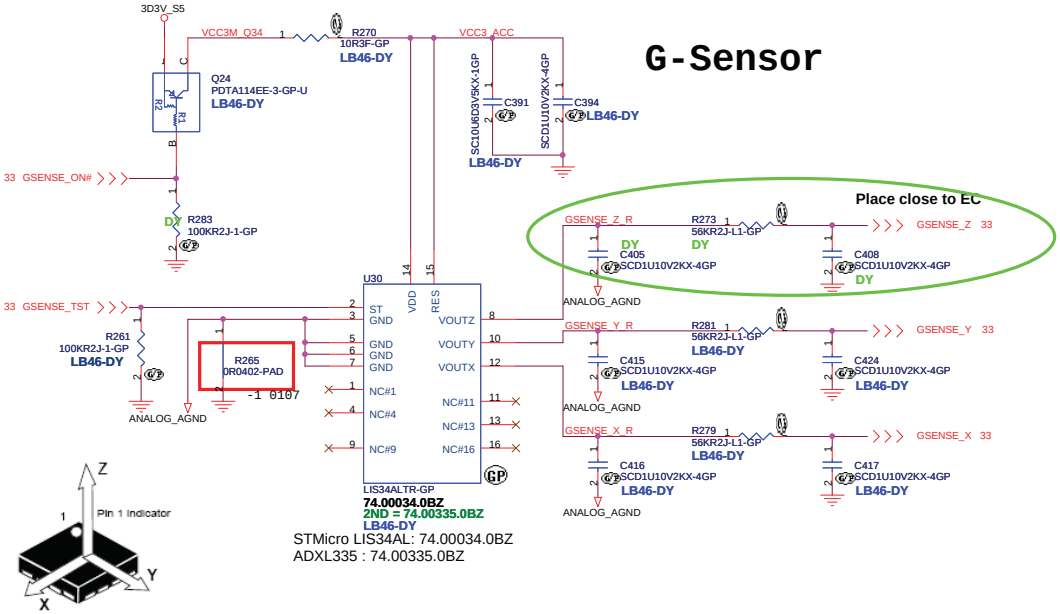




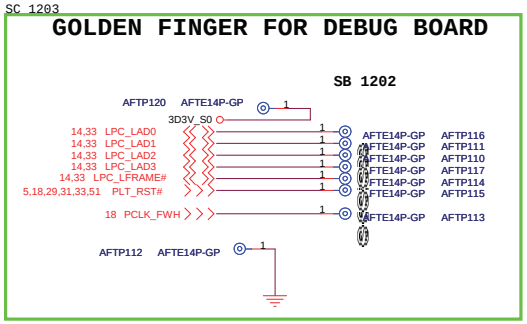
Finger printer



G-Sensor



GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

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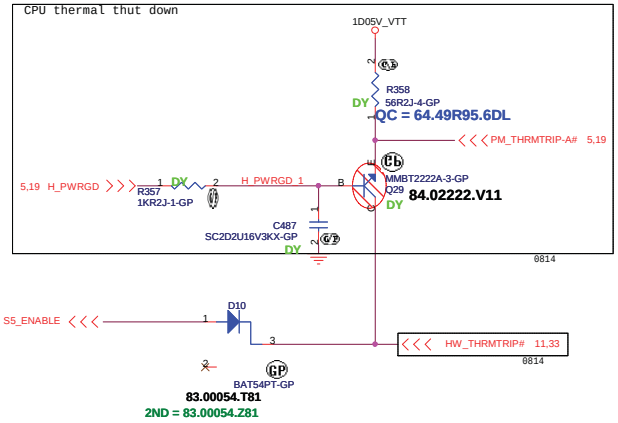
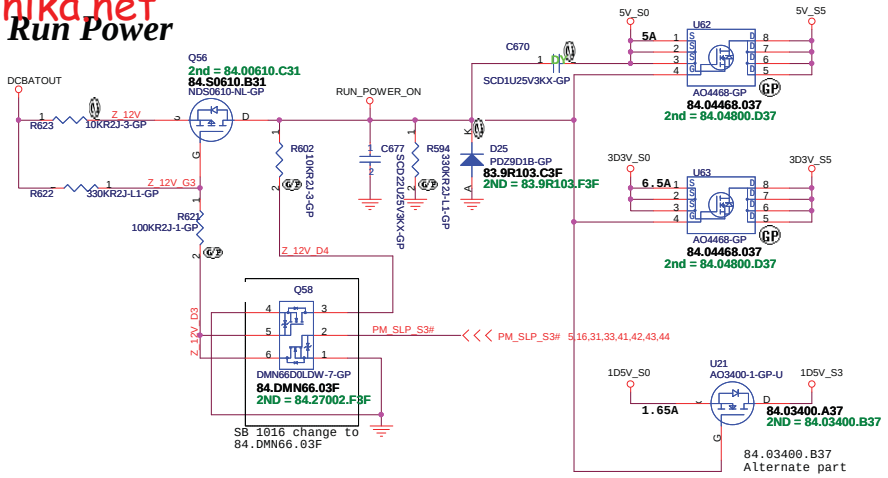
Title: 35_BIOS & TP & G-Sensor & FP

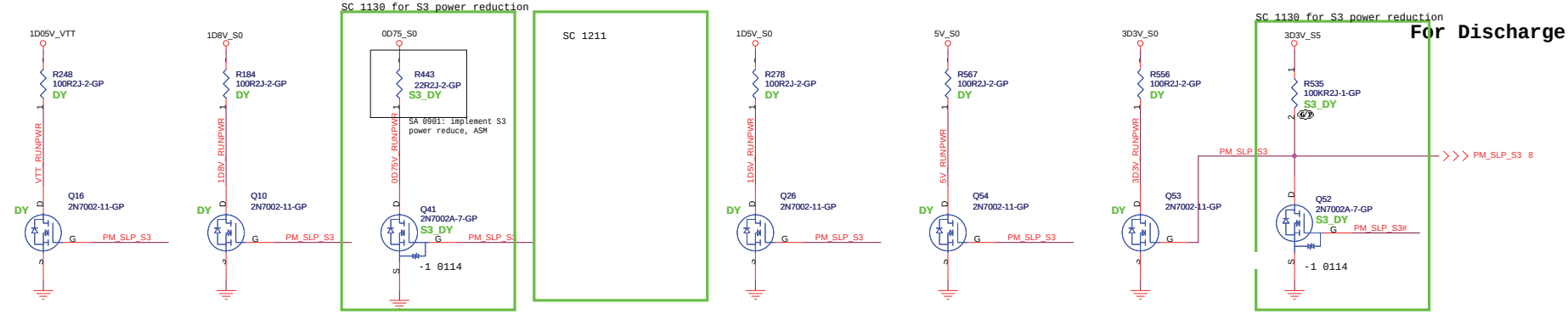
Size: Custom | Document Number: LA46 MB DIS | Rev: SC

Date: Wednesday, January 27, 2010 | Sheet 35 of 58

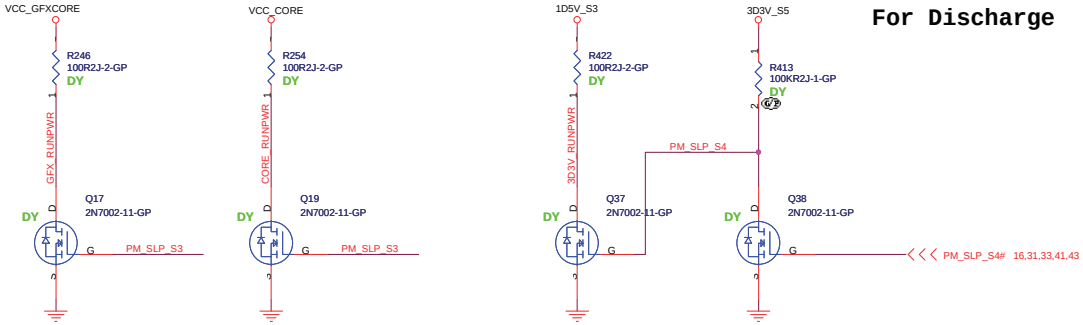
Run Power



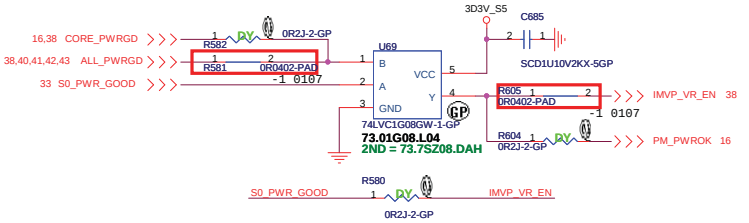




For Discharge



For Discharge



<Core Design>
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C

Title: 36_Run PWR

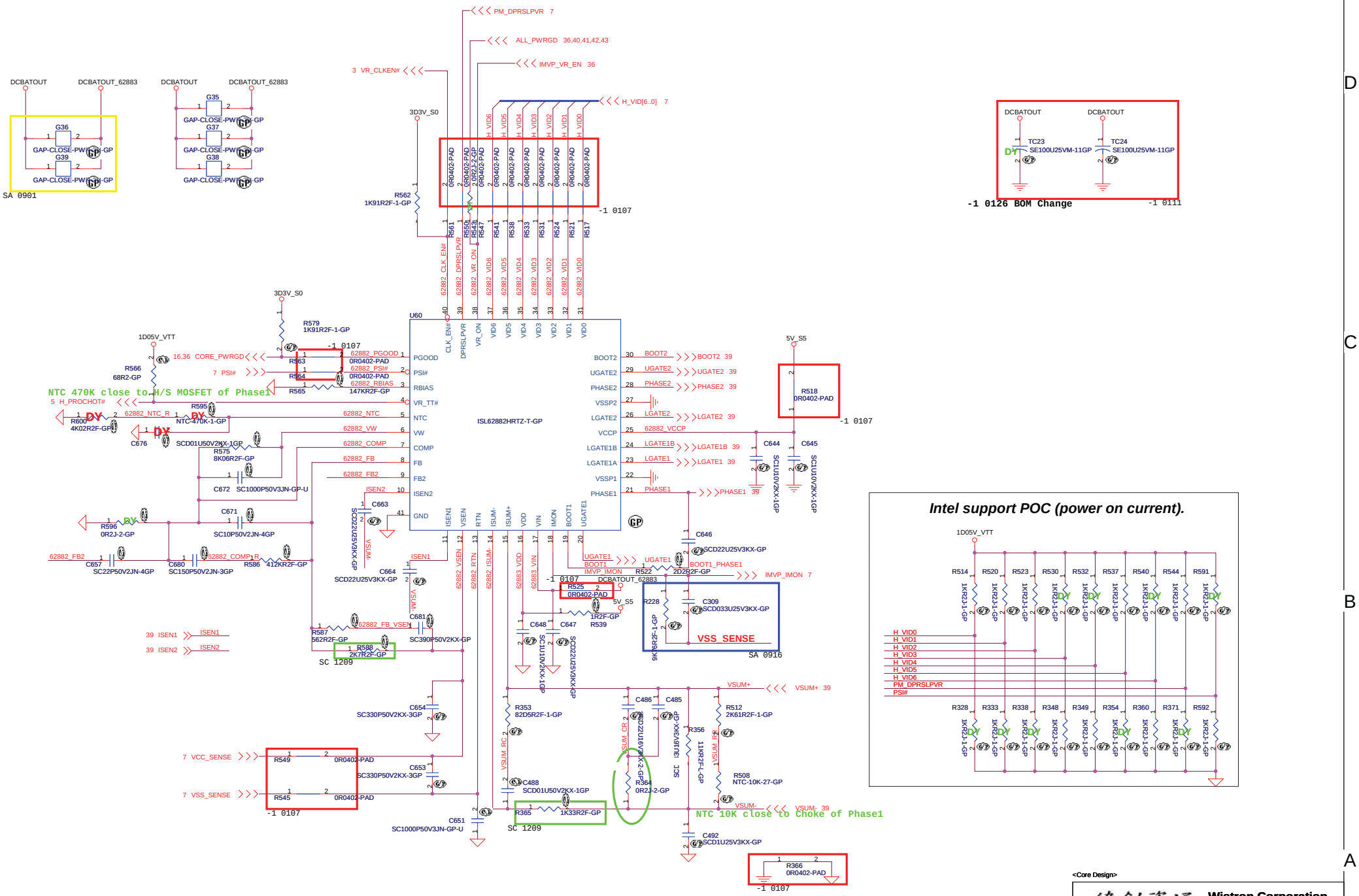
Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 36 of 58

<Core Design>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title	37_BLANK	
Size: A3	Document Number: LA46 MB	Rev: SA
Date: Tuesday, January 26, 2010	Sheet 37 of 58	



<Core Design>
緯創資通 Wistron Corporation
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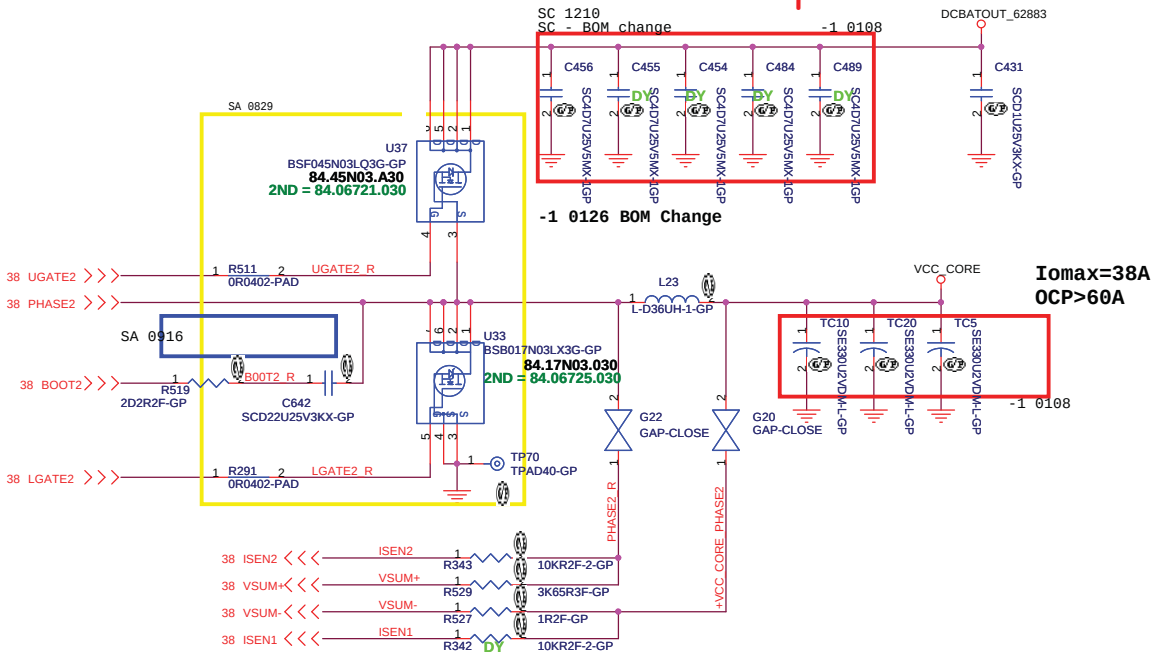
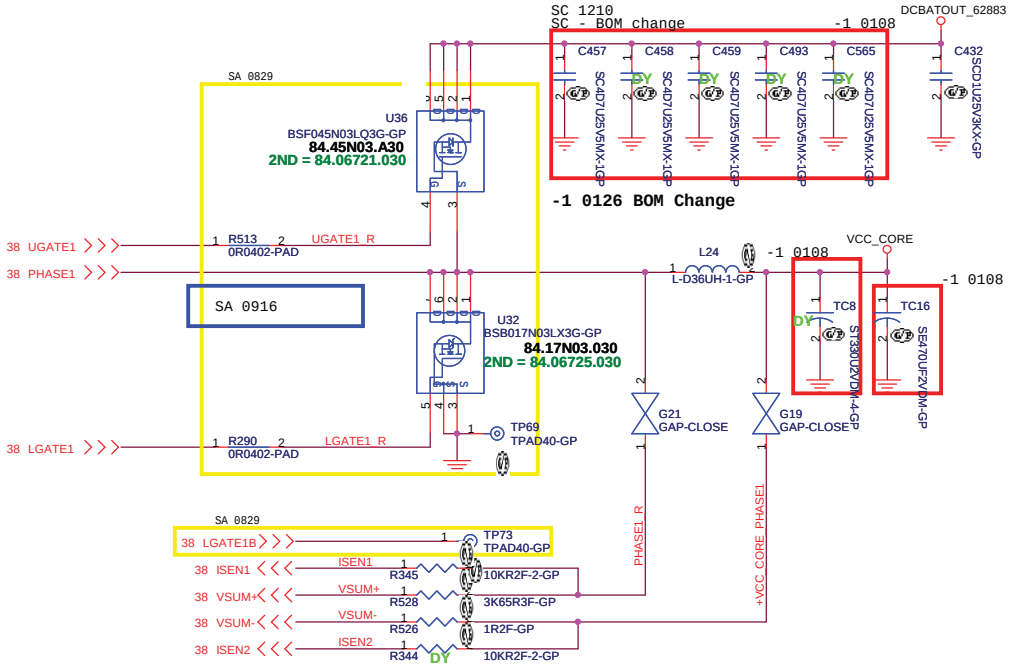
Taipei Hsien 221, Taiwan, R.O.C

Title: 38_ISL62882_CPU_CORE (1 of 2)

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 38 of 58





<Core Design>

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Title: 39_ISL62882_CPU_CORE (2 of 2)

Size	Document Number	Rev
A3	LA46 MB DIS	-1

Date: Wednesday, January 27, 2010 Sheet 39 of 58

-1 0126 BOM Change

SC 1210
SC - BOM change

Iomax=6A
OCP=9A

SB 1026 delete G68

SB 1029 Reserve for SW requirement

SC 1209

Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm

SC -BOM change for 5.1V

Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

Vout=2*(1+R1/R2)

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Core Design>

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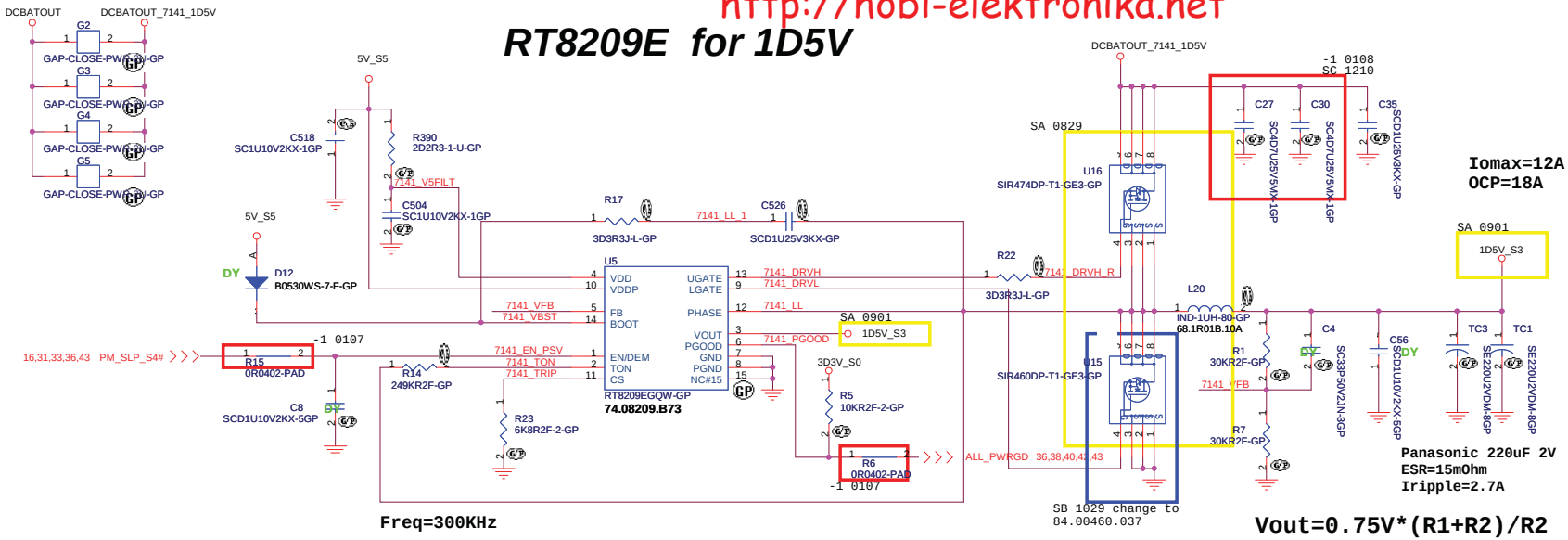
Taipei Hsien 221, Taiwan, R.O.C

Title: 40_TPS51123_5V/3D3V

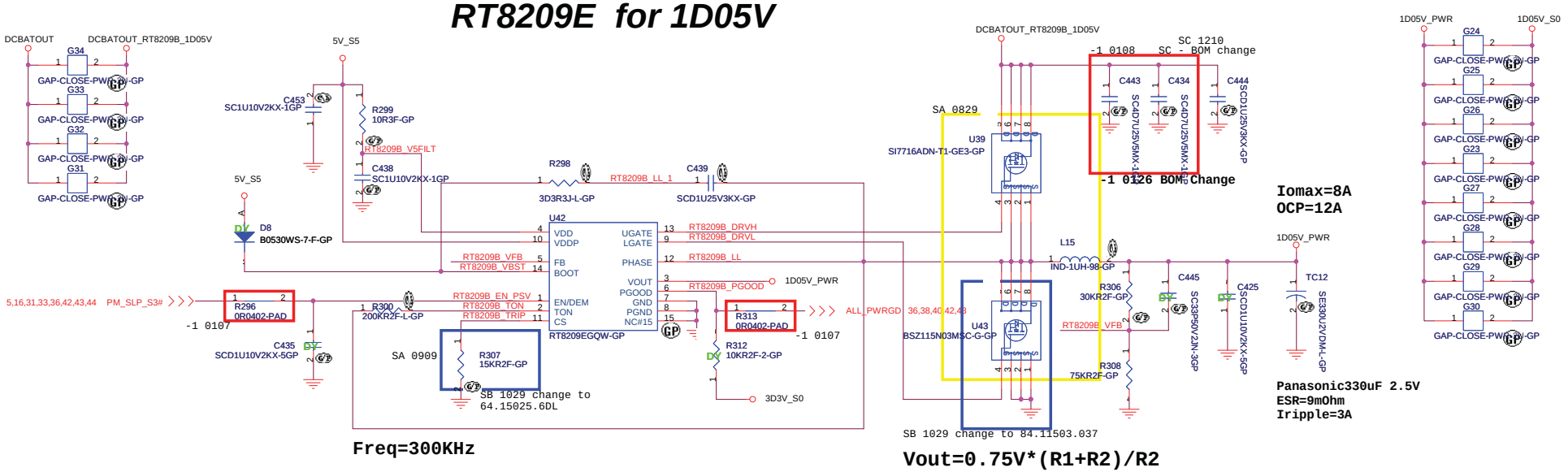
Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 40 of 58

RT8209E for 1D5V



RT8209E for 1D05V



<Core Design>
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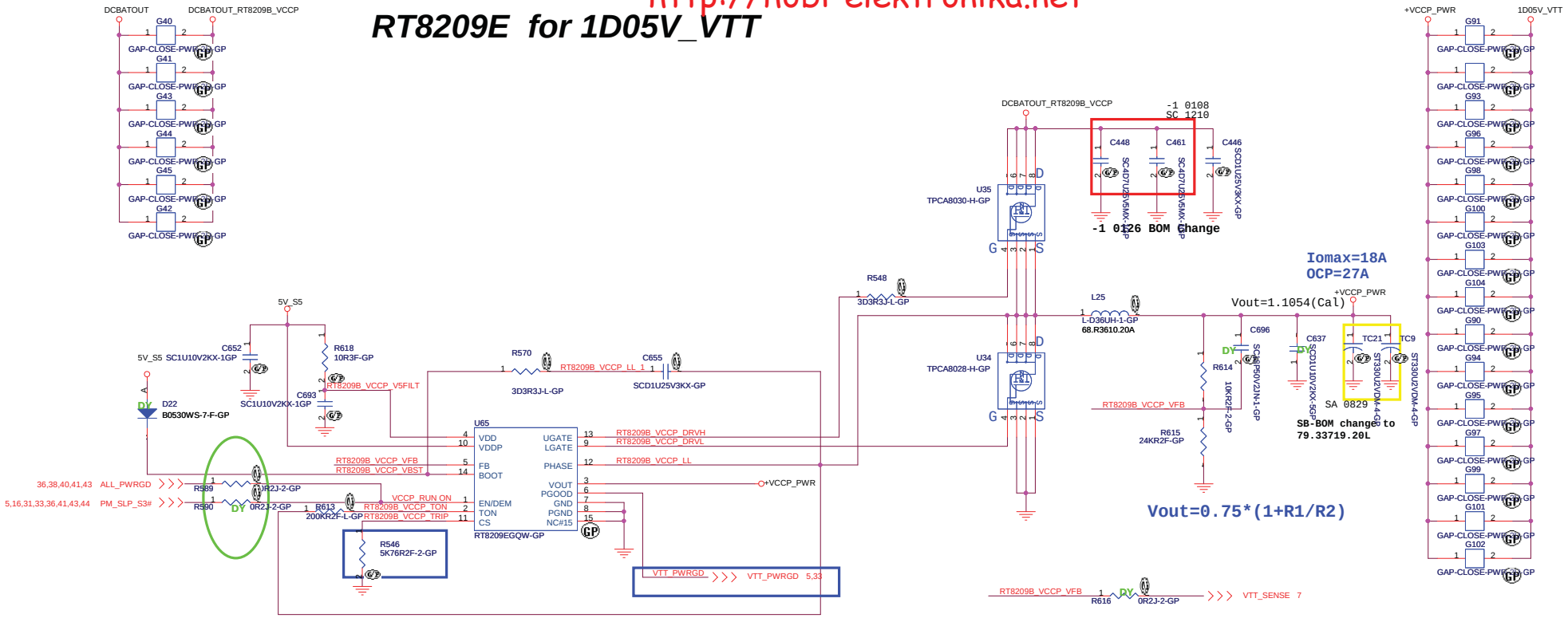
Taipei Hsien 221, Taiwan, R.O.C

Title: 41_RT8209E_1D5V / RT8209E_1D05V

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 41 of 58

RT8209E for 1D05V_VTT



<Core Design>

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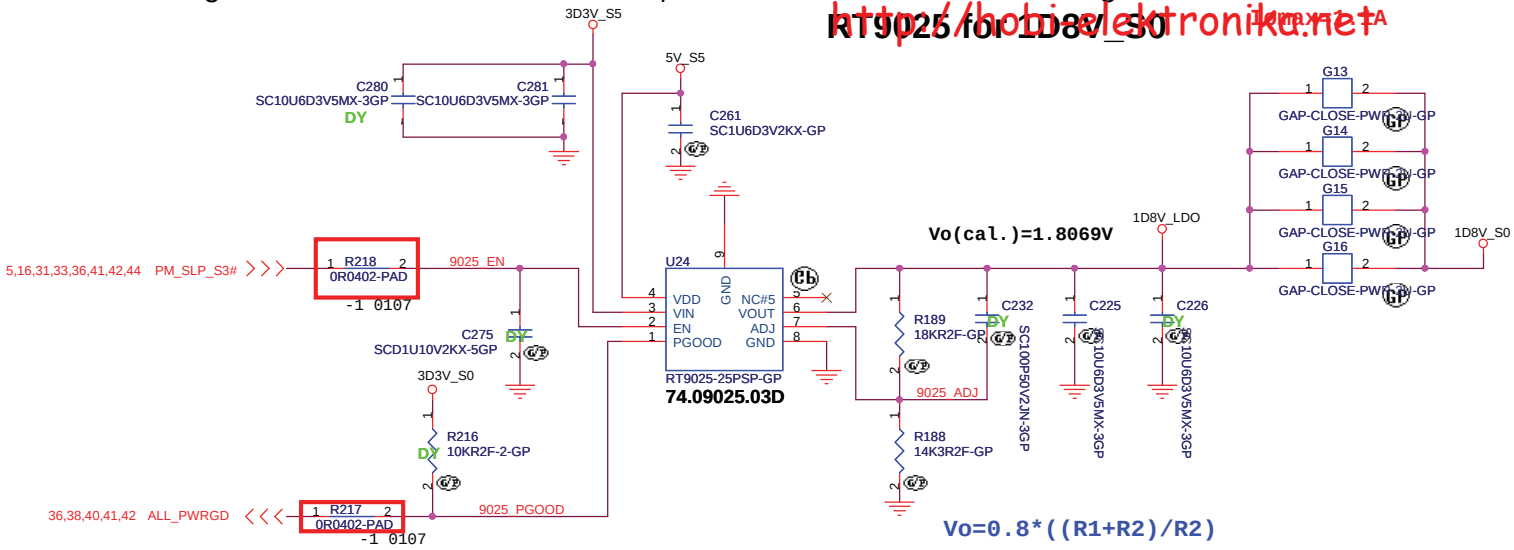
Taipei Hsien 221, Taiwan, R.O.C

Title: 42_RT8209E_1D05V_VTT

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

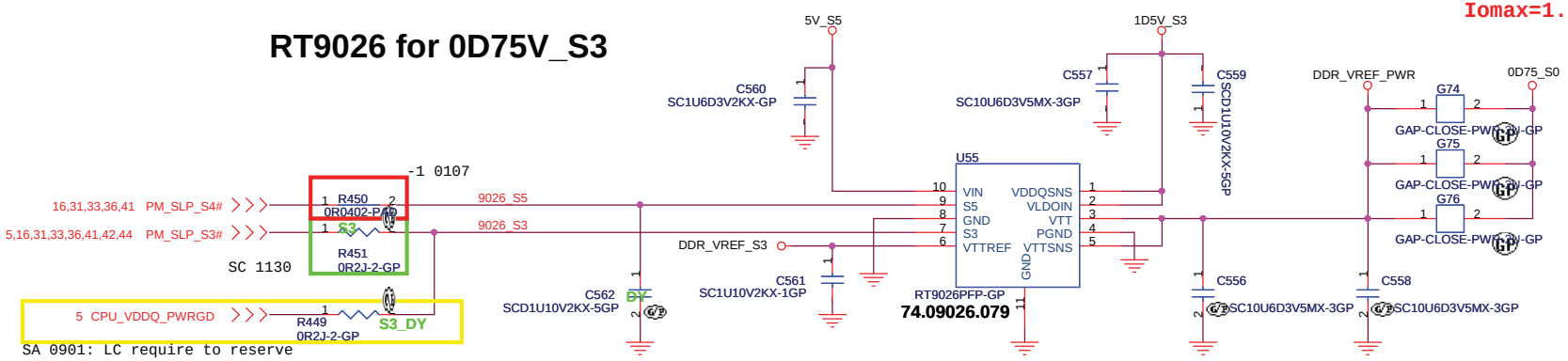
Date: Wednesday, January 27, 2010 | Sheet 42 of 58

RT9025 for 1D8V_S0



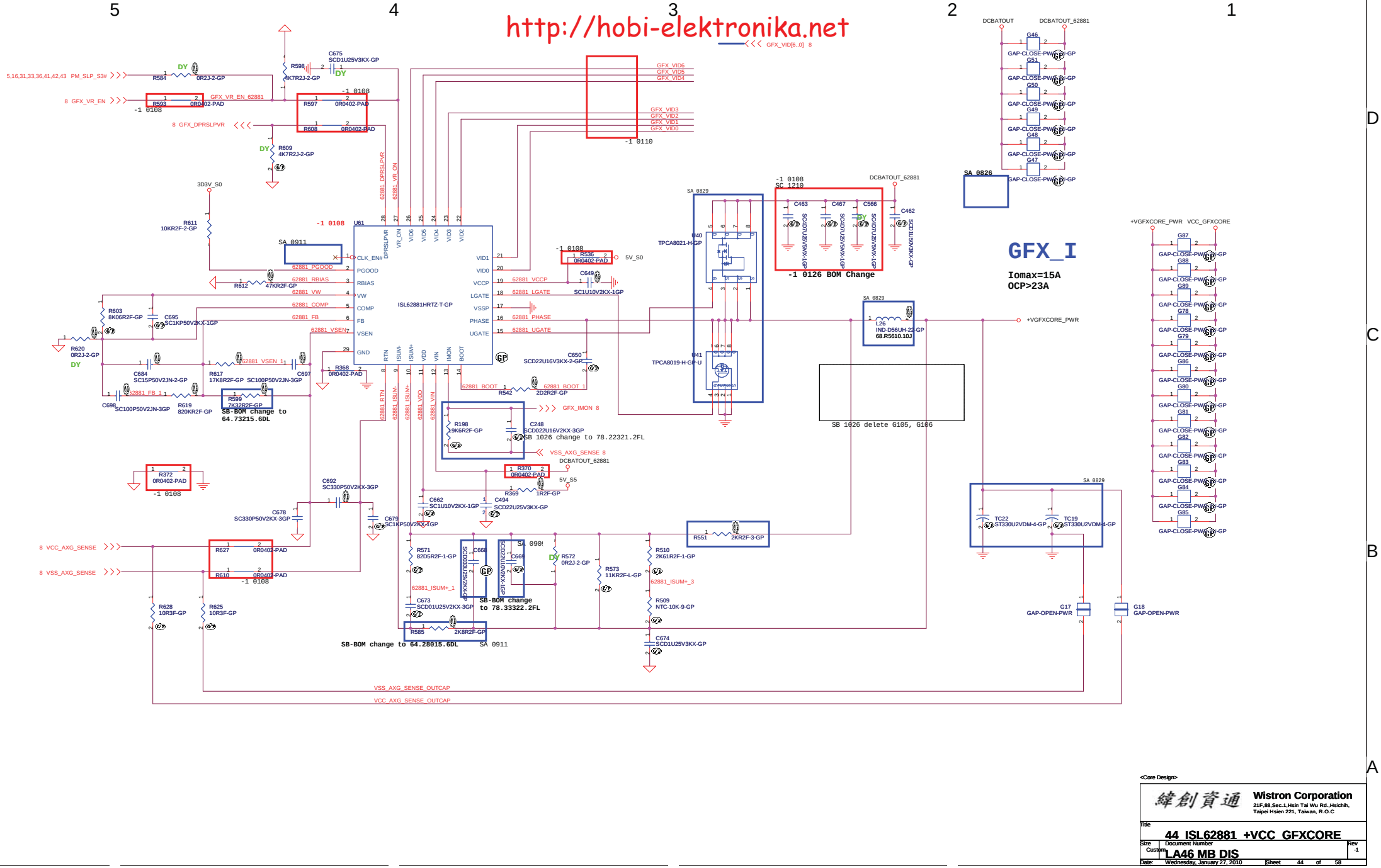
RT9026 for 0D75V_S3

Iomax=1.2A



<Core Design>

緯創資通 Wistron Corporation	21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C
Title	43_RT9025_1D8V/ RT9026_0D75
Size: Custom	Document Number: LA46 MB DIS
Rev: -1	
Date: Tuesday, January 26, 2010	Sheet 43 of 58



<Core Design>
緯創資通 Wistron Corporation
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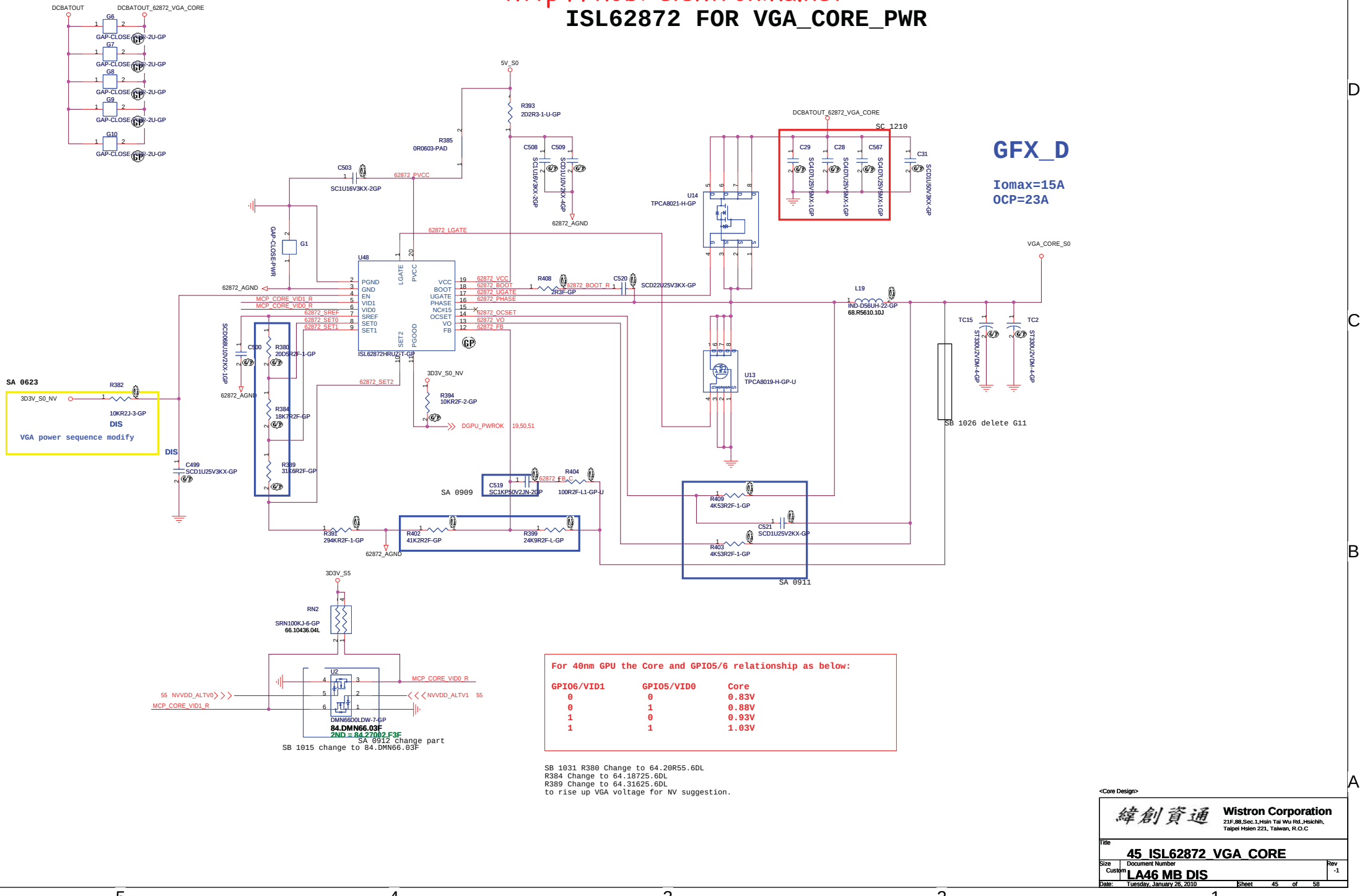
Taipei Hsien 221, Taiwan, R.O.C

Title: 44 ISL62881 +VCC_GFXCORE

Size	Document Number	Rev
Custom	LA46 MB DIS	-1

Date: Wednesday, January 27, 2010 Sheet 44 of 58

ISL62872 FOR VGA_CORE_PWR



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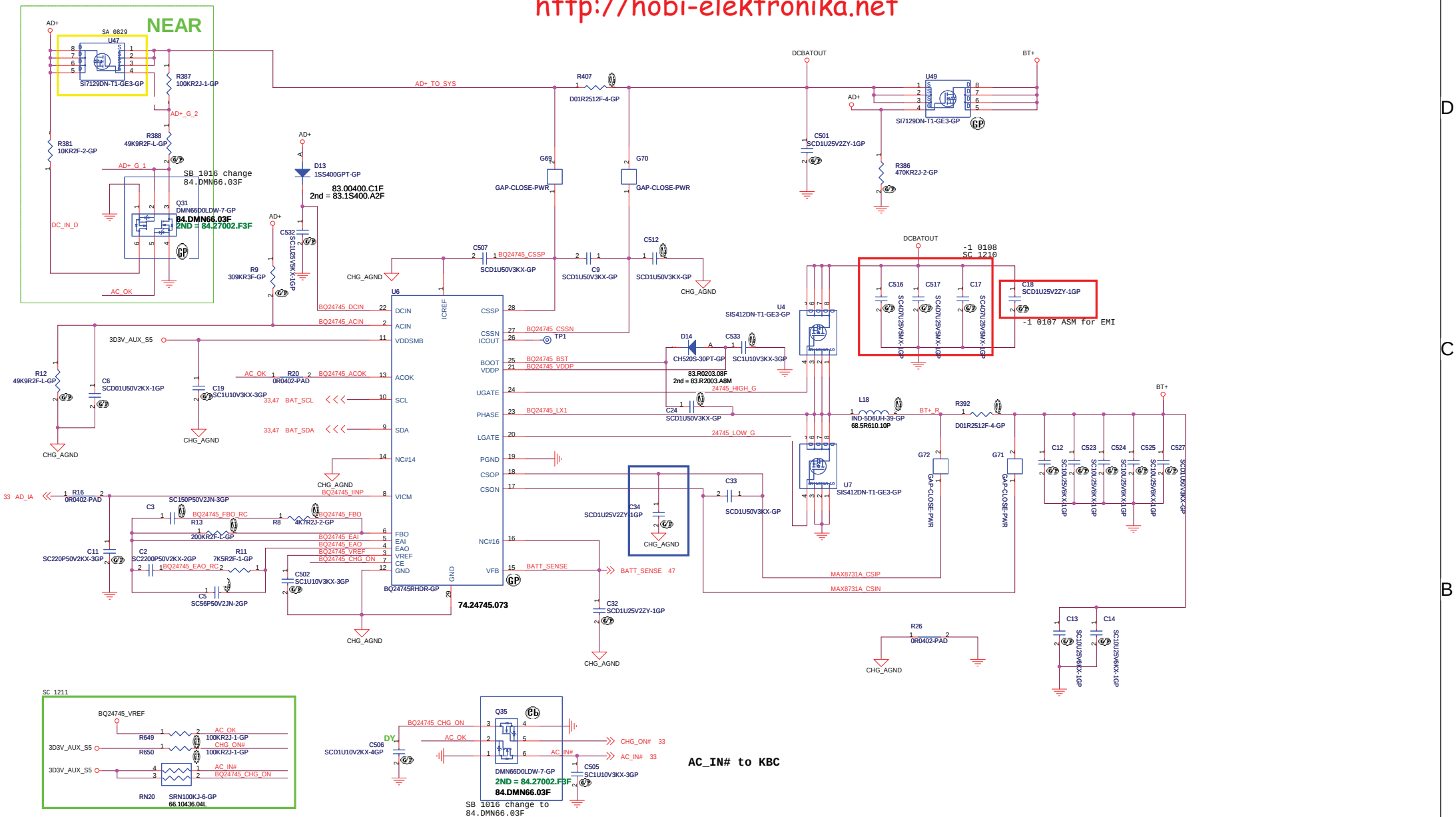
Taipei Hsien 221, Taiwan, R.O.C

Title: 45_ISL62872_VGA_CORE
Size: Custom | Document Number: LA46 MB DIS | Rev: -1
Date: Tuesday, January 26, 2010 | Sheet 45 of 58



<Core Design>
緯創資通 Wistron Corporation
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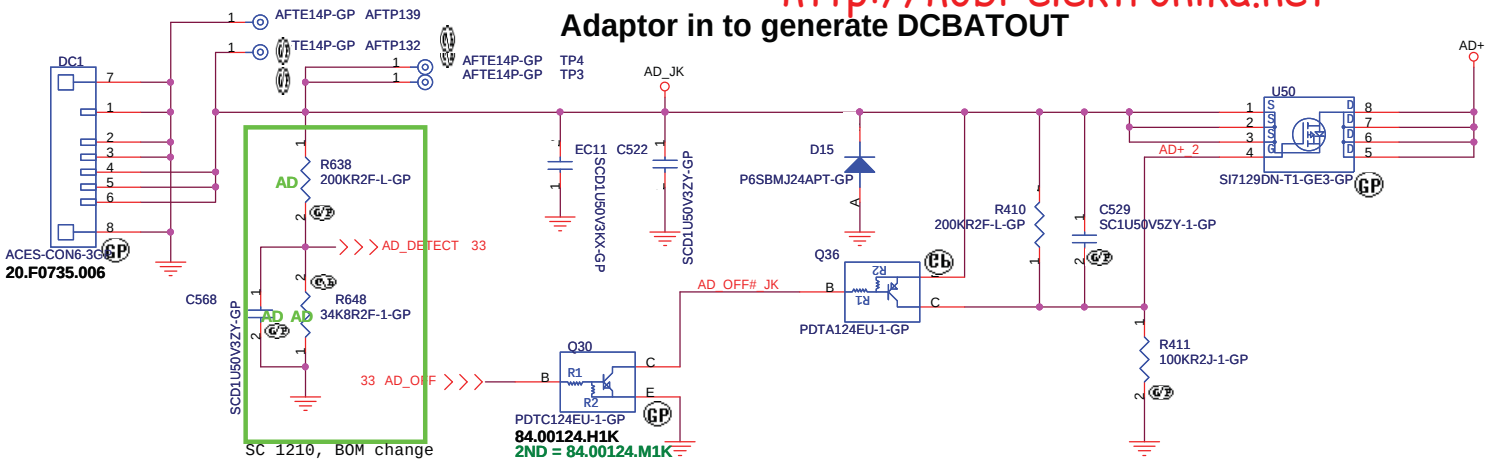
Taipei Hsien 221, Taiwan, R.O.C

Title: 46_BQ24745_CHARGER

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

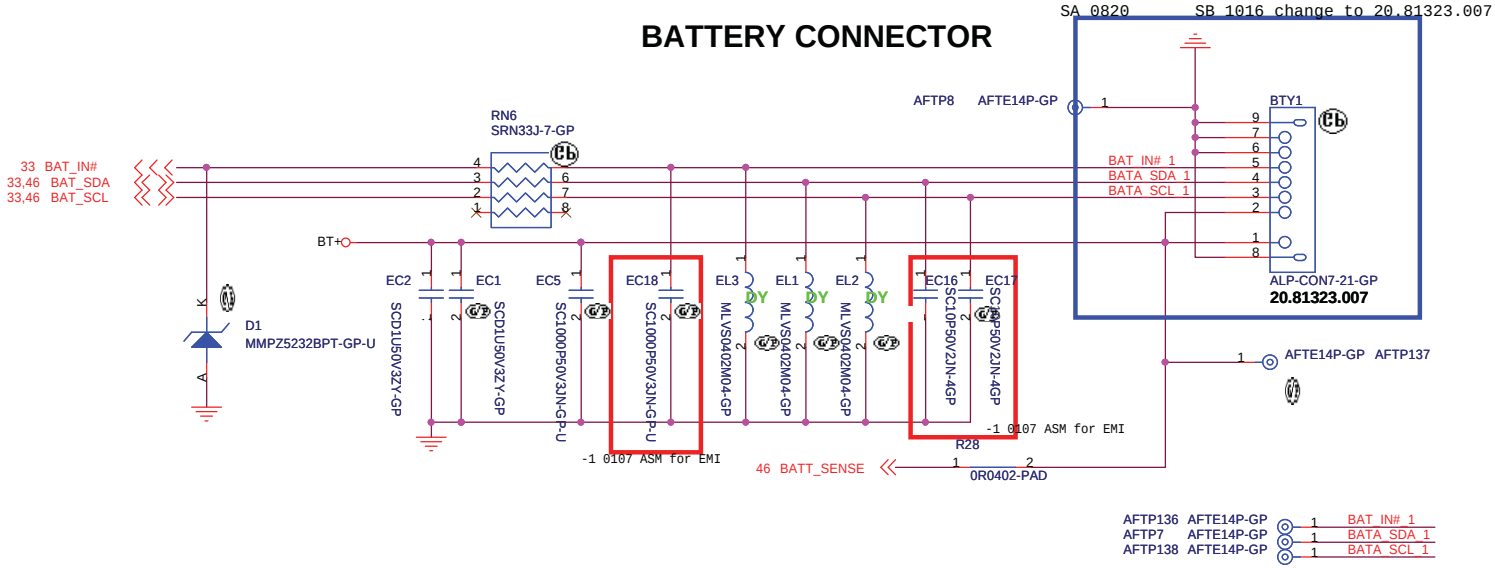
Date: Tuesday, January 26, 2010 | Sheet 46 of 58

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

SA_0820 SB_1016 change to 20.81323.007



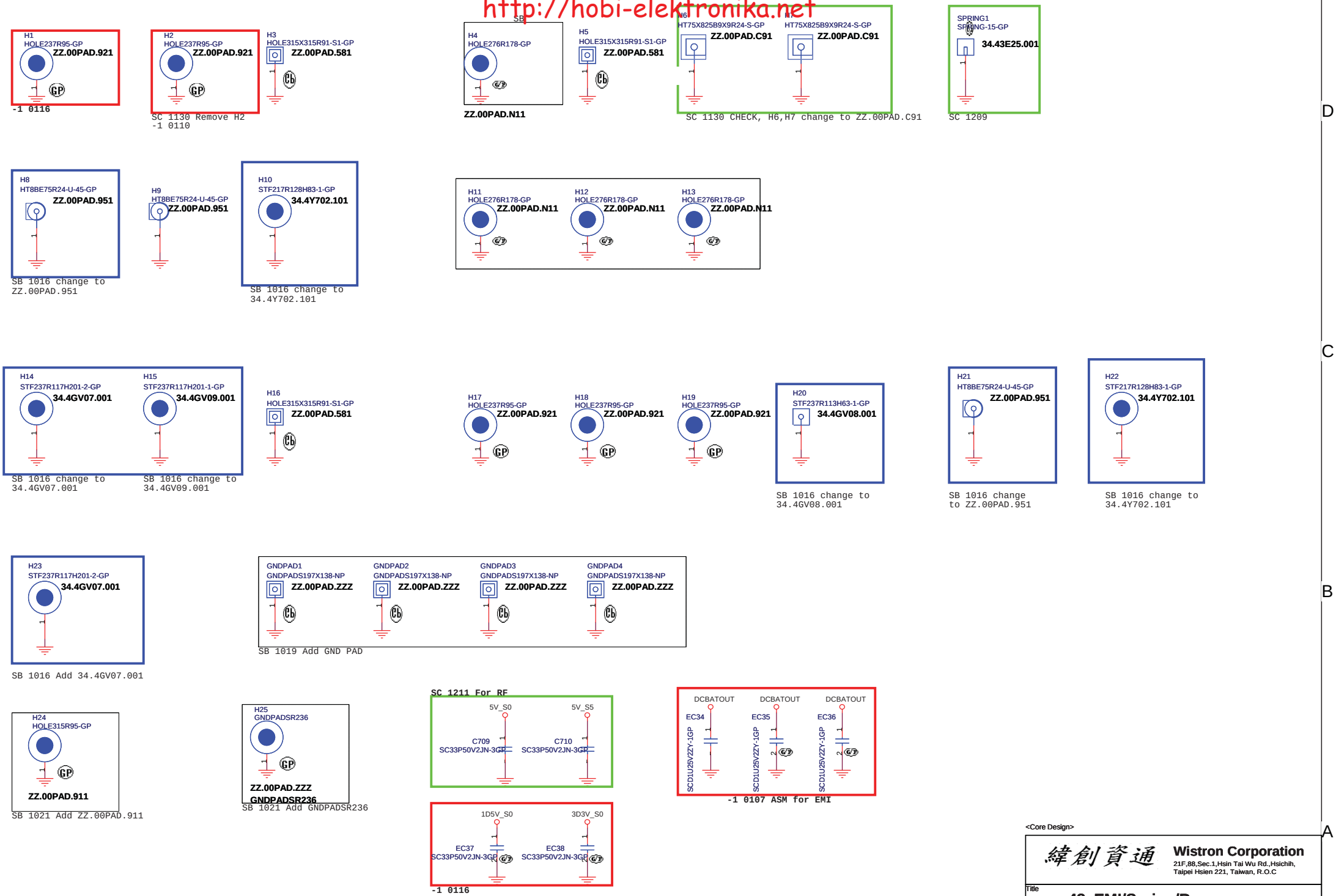
<Core Design>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 47 AD / BATT CONN

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 47 of 58



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C

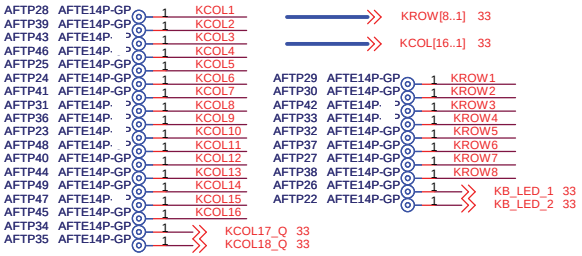
Title: 48_EMI/Spring/Boss

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

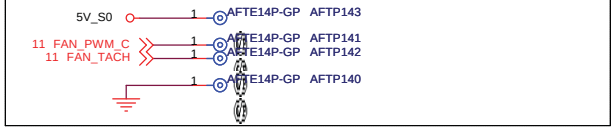
Date: Tuesday, January 26, 2010 | Sheet 48 of 58

SB_1016_Add_AFTE

Near KB1 Keyboard

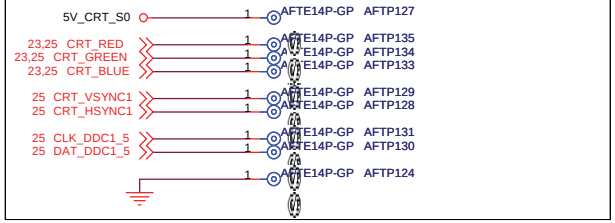


Near FAN1

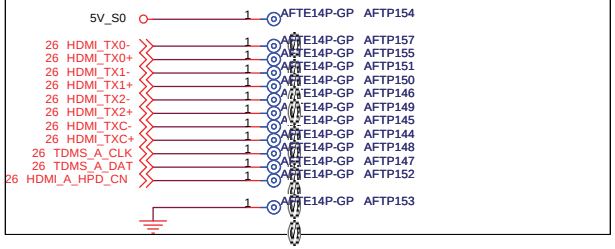


Near RTC1

Near CRT_CN1



Near HDMI_CN1



<Core Design>

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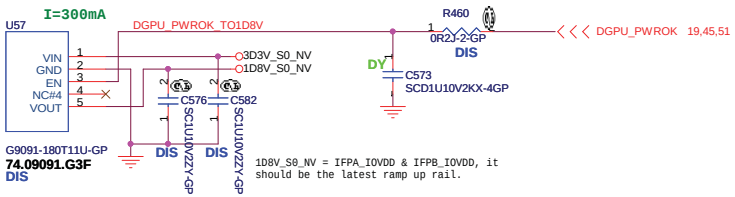
Title: 49_AFTE_TP

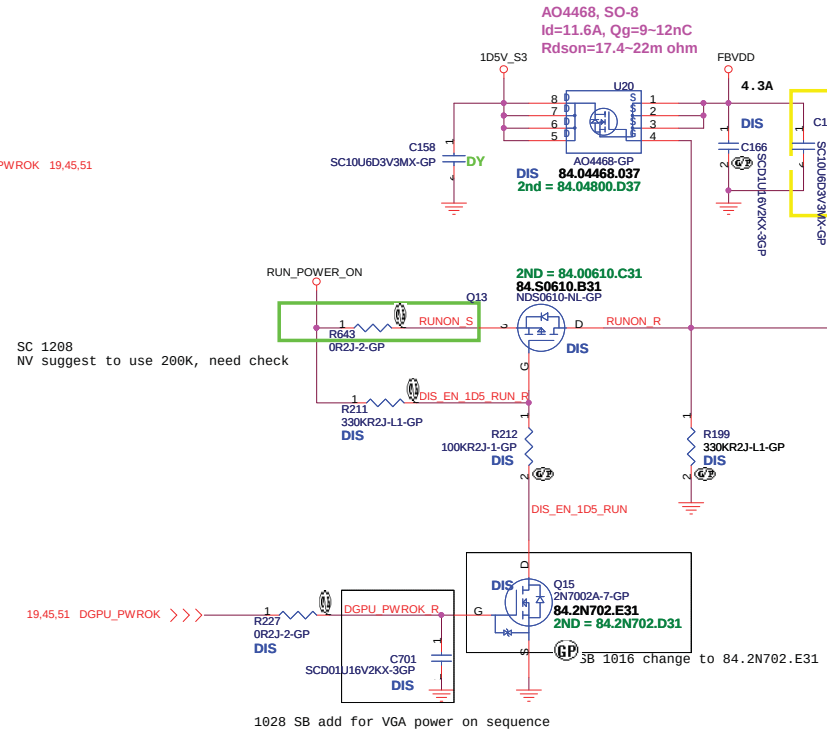
Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 49 of 58

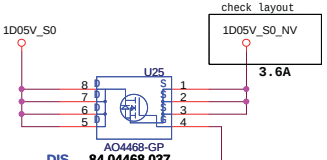
+3VS to 1.8V Transfer



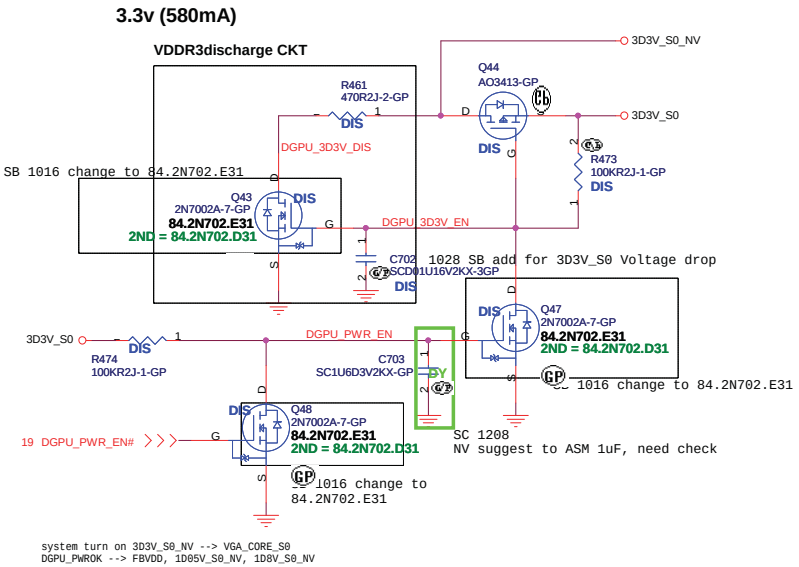
+1.5V to FBVDD Transfer

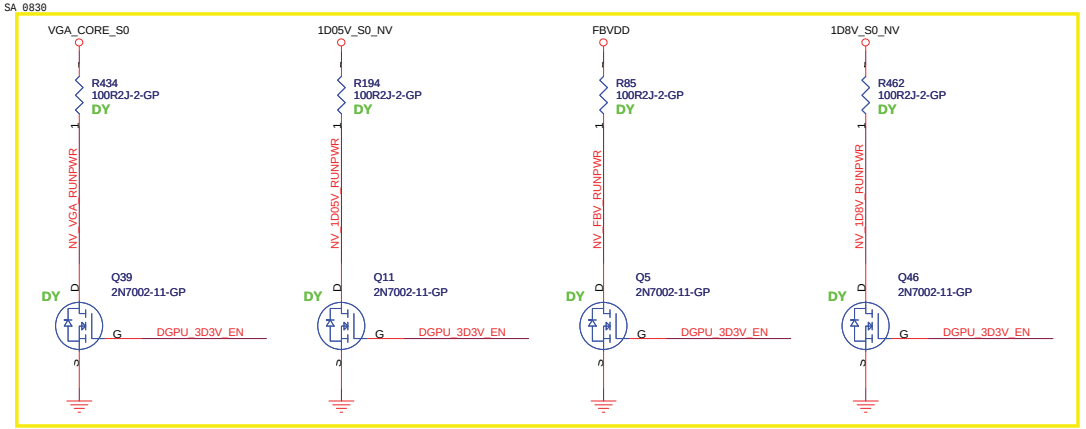


+1.05V to +1.05V_NV Transfer



+3VS to 3.3V_DELAY Transfer





<Core Design>

Wistron Corporation
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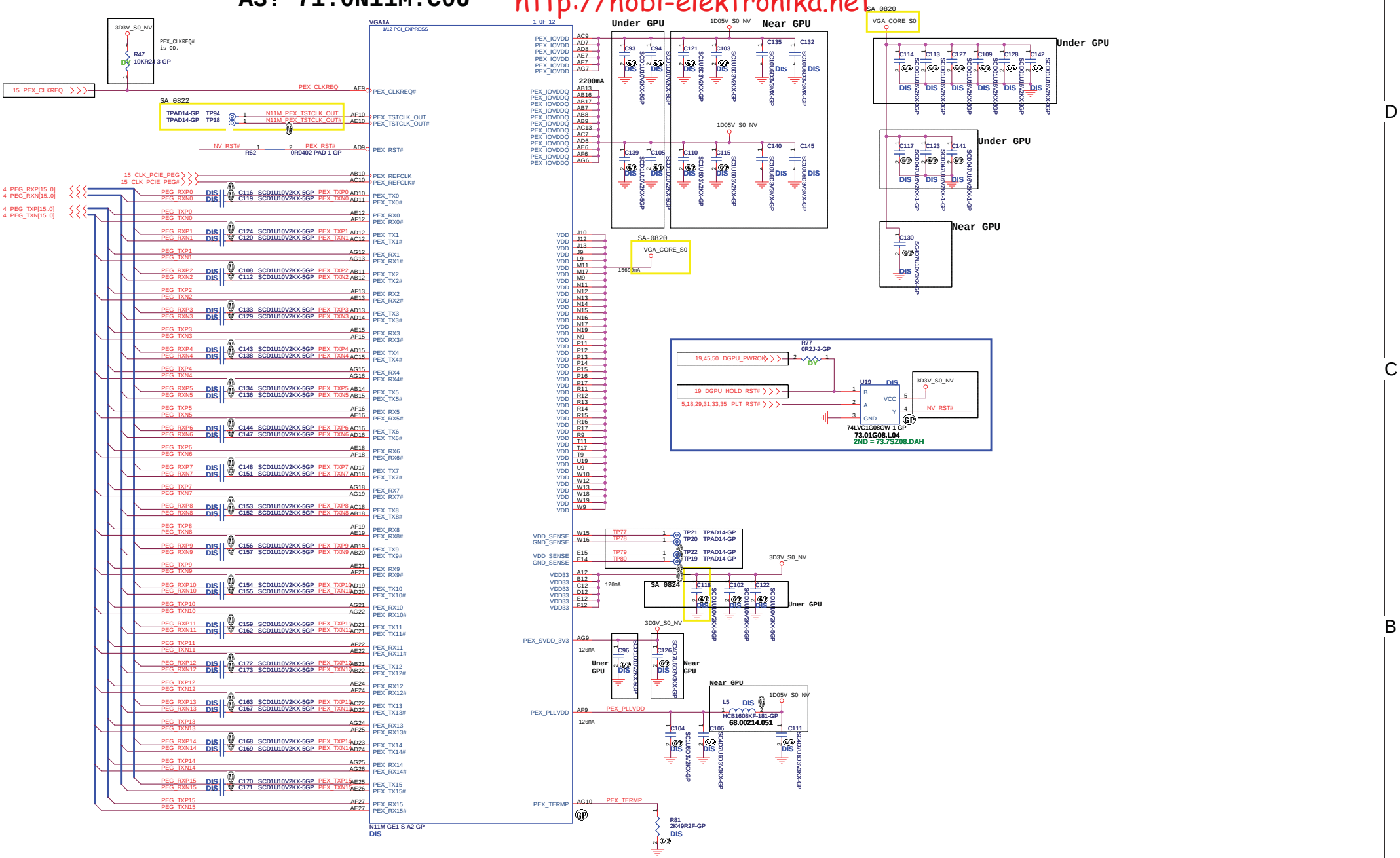
Taipei Hsien 221, Taiwan, R.O.C

Title: 50_NV power

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 50 of 58



Wistron Corporation
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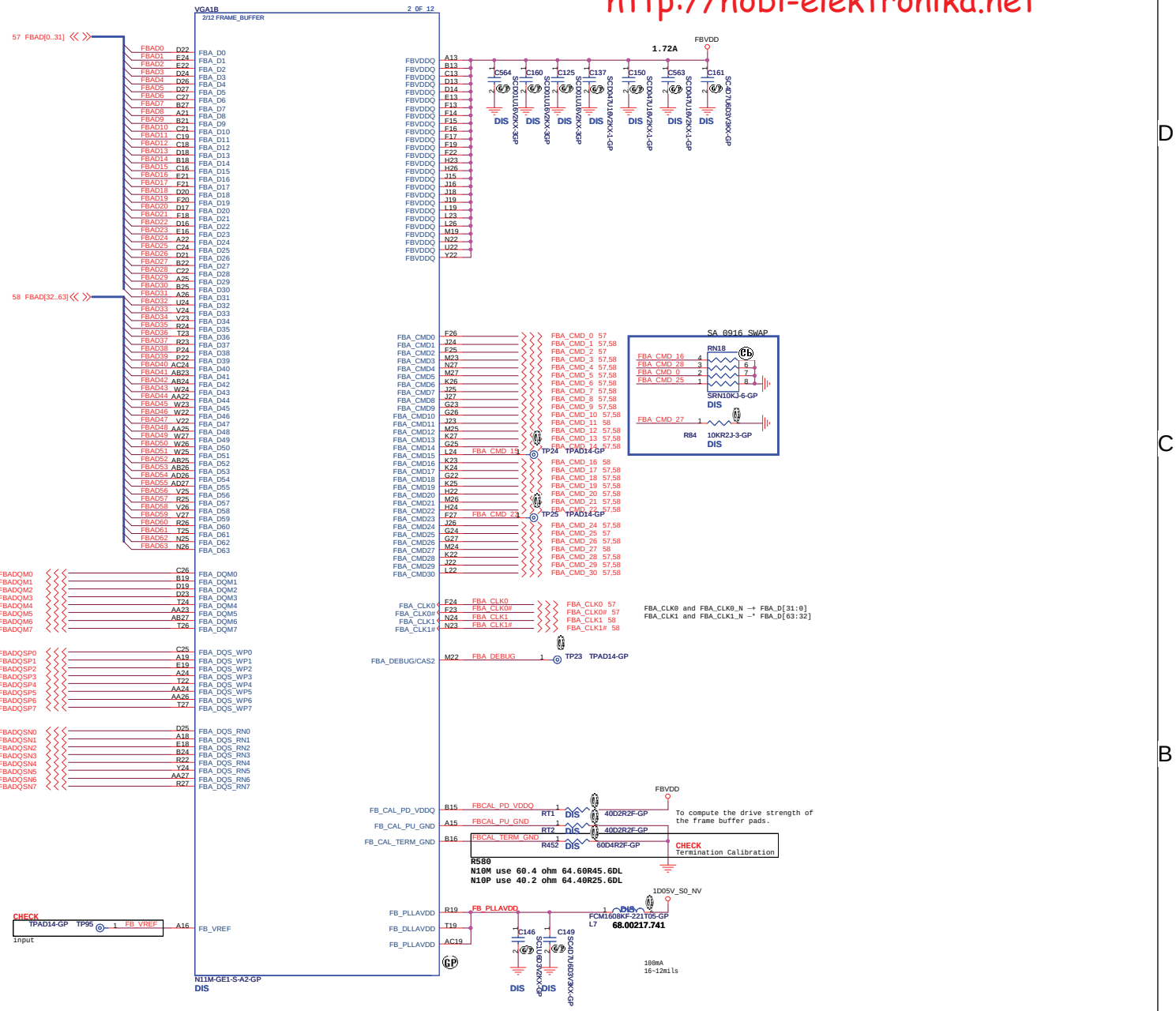
Taipei Hsien 221, Taiwan, R.O.C



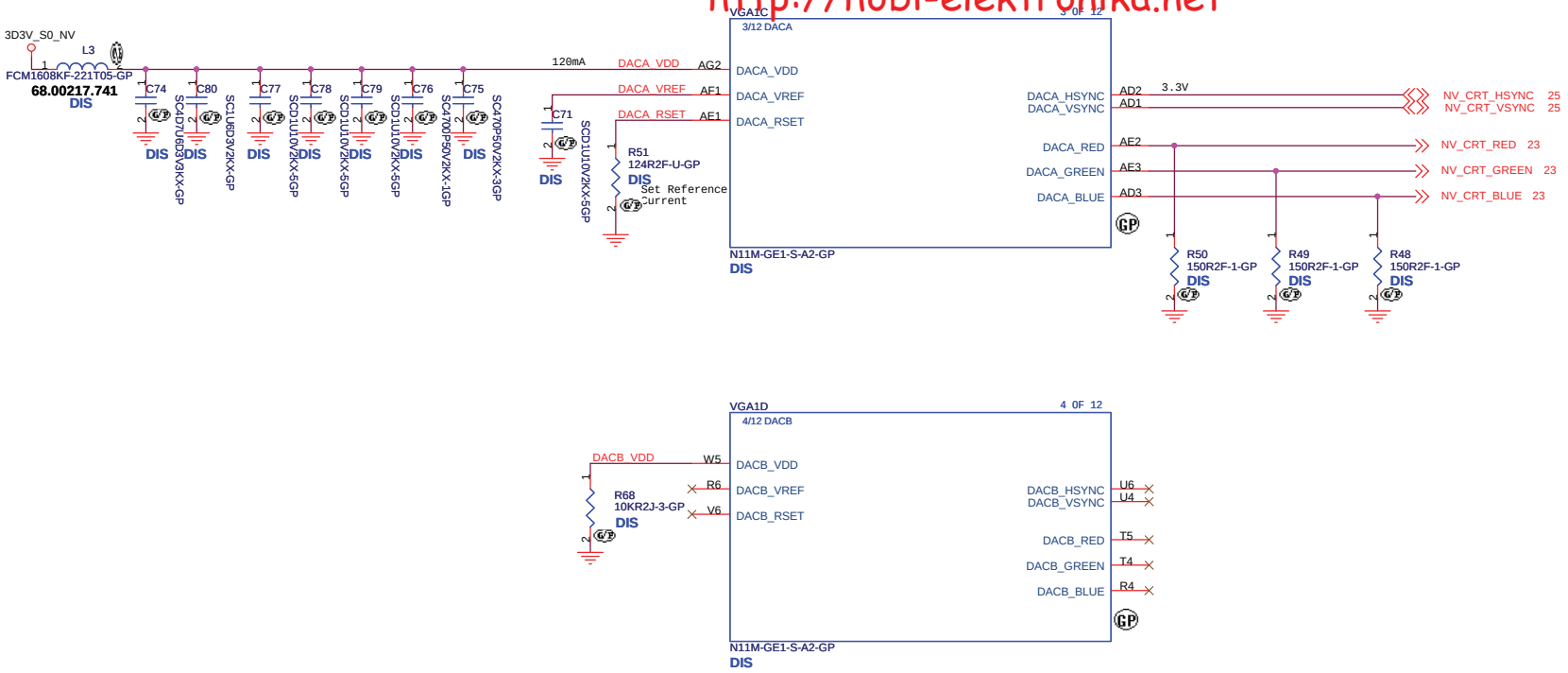
<Core Design>

Wistron Corporation
21F.88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 52_N11M(2/6)_MEM

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 52 of 58



<Core Design>

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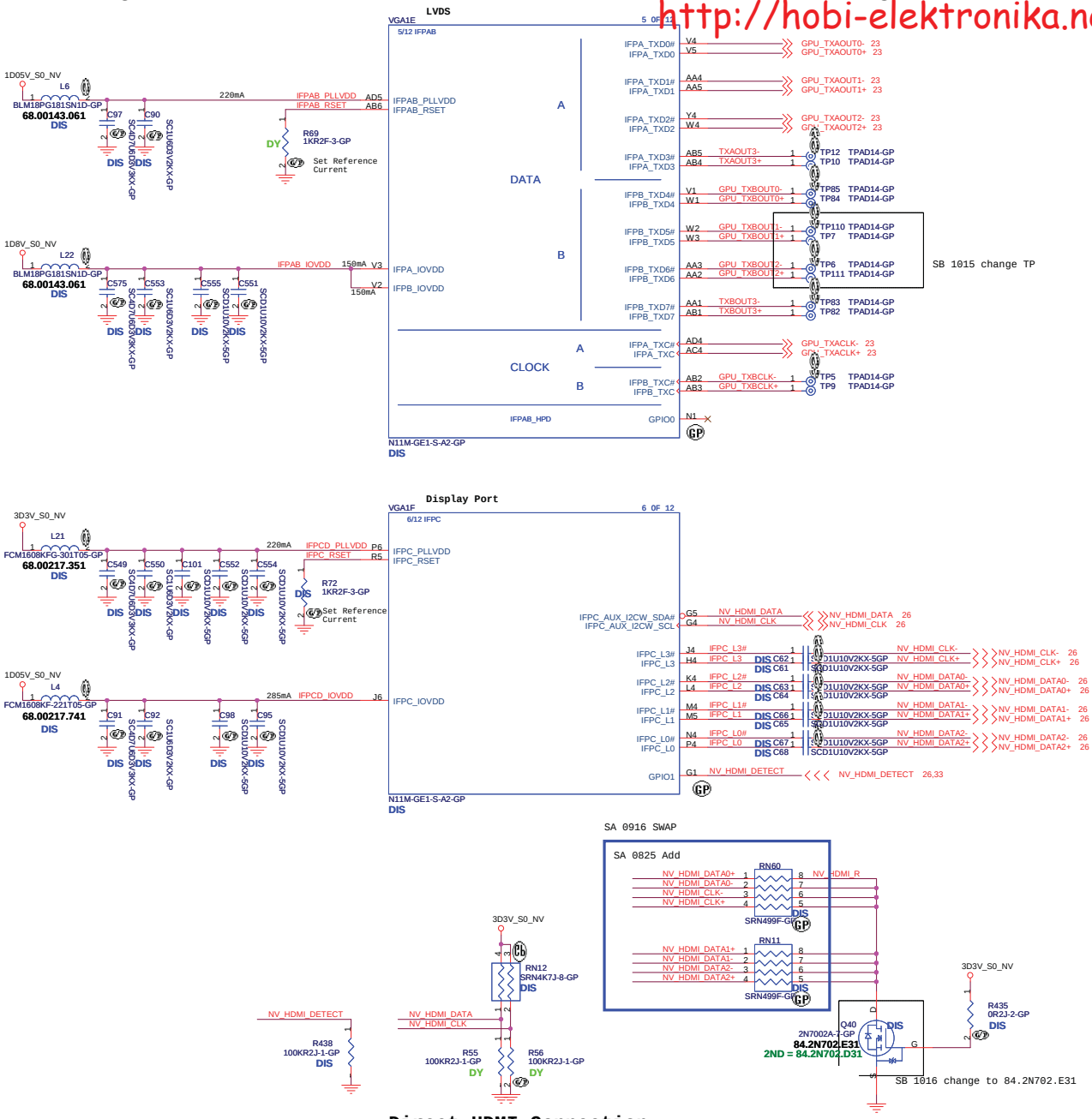
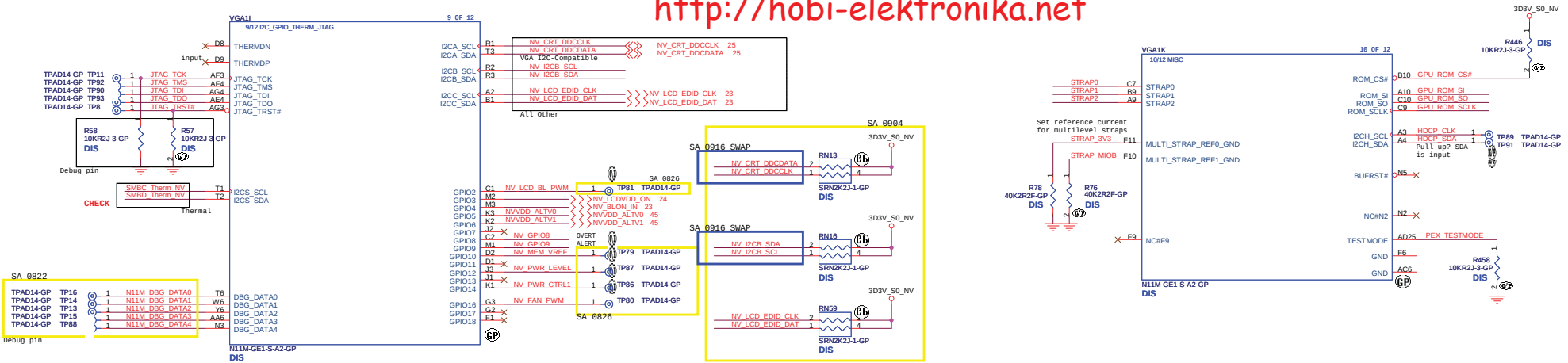
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

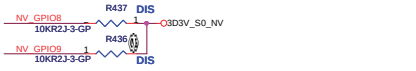
Title: 53 N11M(3/6) DAC

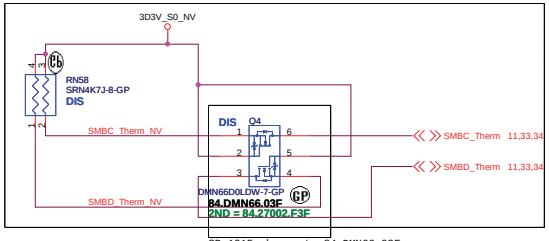
Size: Custom | Document Number: LA46 MB DIS | Rev: -1

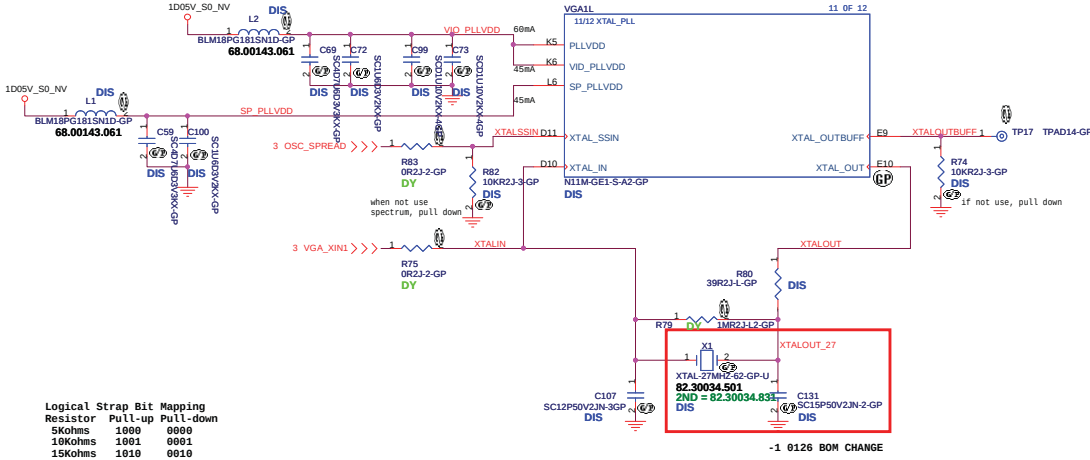
Date: Tuesday, January 26, 2010 | Sheet 53 of 58











STRAP0

USER[0]=1	DeviceID
USER[1]=1	N11P-LM1(0x0A2B) ?
USER[2]=1	N11M-GE1(0x0A75) 1-0101
USER[3]=1	

STRAP1

3GIO_PADCFG[0]=0
3GIO_PADCFG[1]=1
3GIO_PADCFG[2]=1
3GIO_PADCFG[3]=1

STRAP2

	N11M-LP1	N11M-GE1
PCI_DEVID[0]=1	[0] 1	1
PCI_DEVID[1]=0	[1] 1	0
PCI_DEVID[2]=1	[2] 0	1
PCI_DEVID[3]=0	[3] 1	0

GPU_ROM_SI

for Hynix VRAM	for Samsung VRAM
RAM_CFG[0]=0	RAM_CFG[0]=1
RAM_CFG[1]=1	RAM_CFG[1]=1
RAM_CFG[2]=0	RAM_CFG[2]=0
RAM_CFG[3]=0	RAM_CFG[3]=0

GPU_ROM_SO

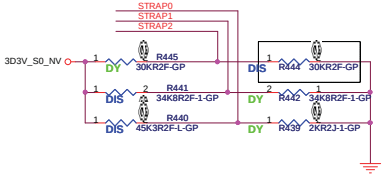
VGA_DEVICE	=1
SMB_ALT_ADDR	=0
FB_0_BAR_SIZE	=0
XCLK_417	=0

GPU_ROM_SCLK

		N11M-LP1	N11M-GE1
PEX_PLL_EN_TERM	=0		
SLOT_CLK_CFG	=1		
SUB_VENDOR	=0		
PCI_DEVID[4]	=1	[4] 0	1

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111



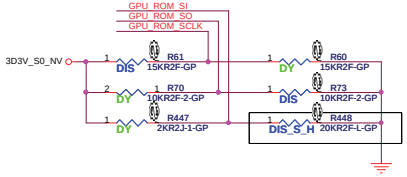


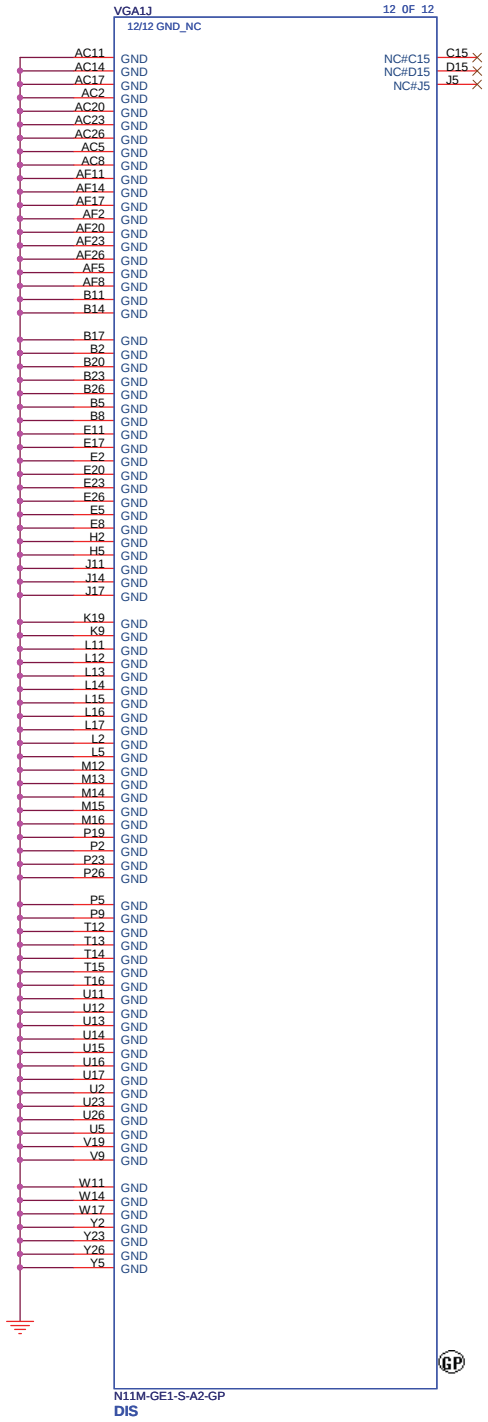
TABLE
KENDO VIDEO MEMORY

	SAMSUNG 0011	HYNIX 0010
R448	20KOHM 64.20025.6DL	15KOHM 64.15025.6DL

<Core Design>
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 55_N11M(5/6)_STRAP/ GPIO

Size	Document Number	Rev
Custom	LA46 MB DIS	-1
Date: Wednesday, January 27, 2010	Sheet 55 of 58	



<Core Design>

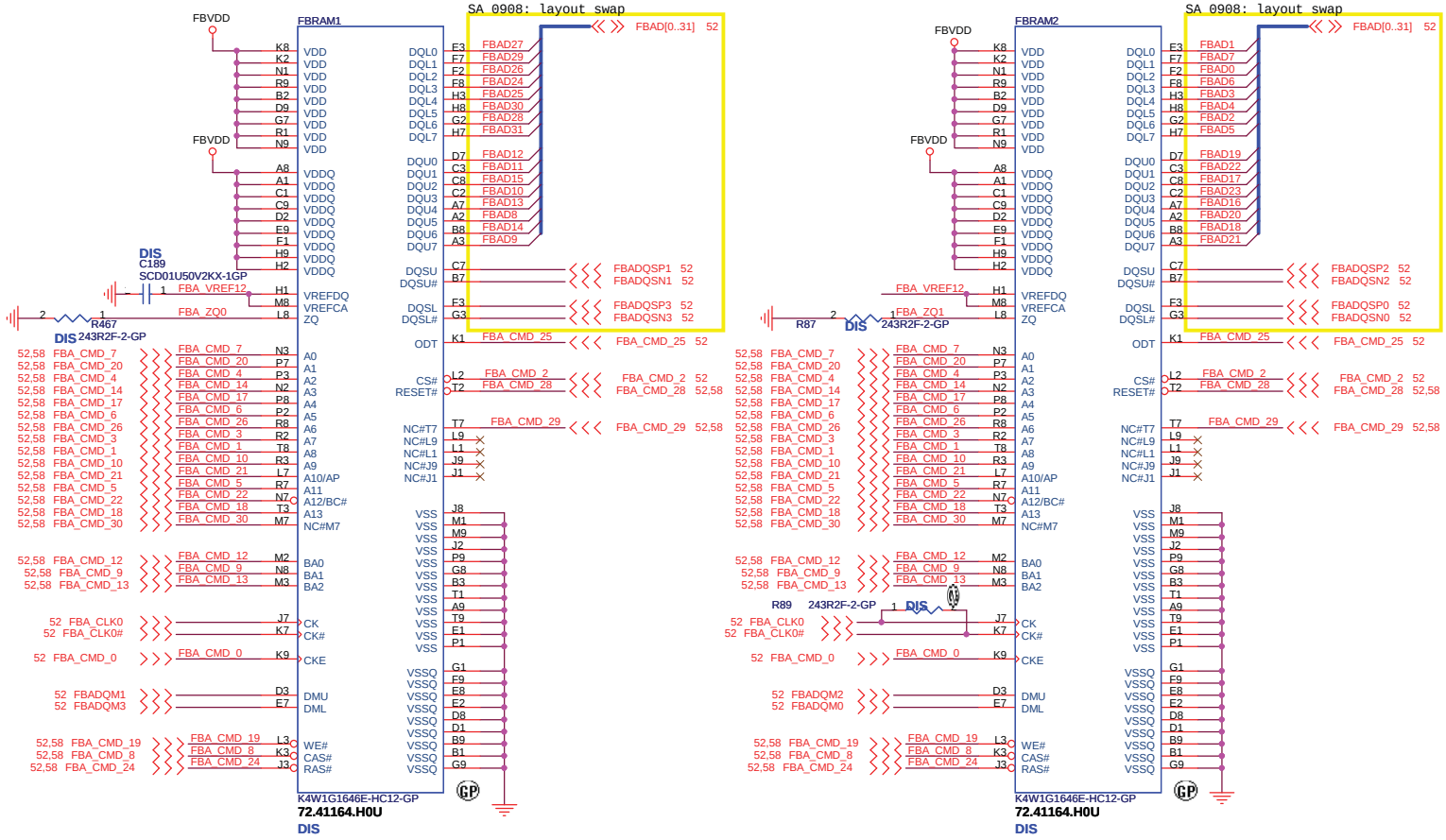
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

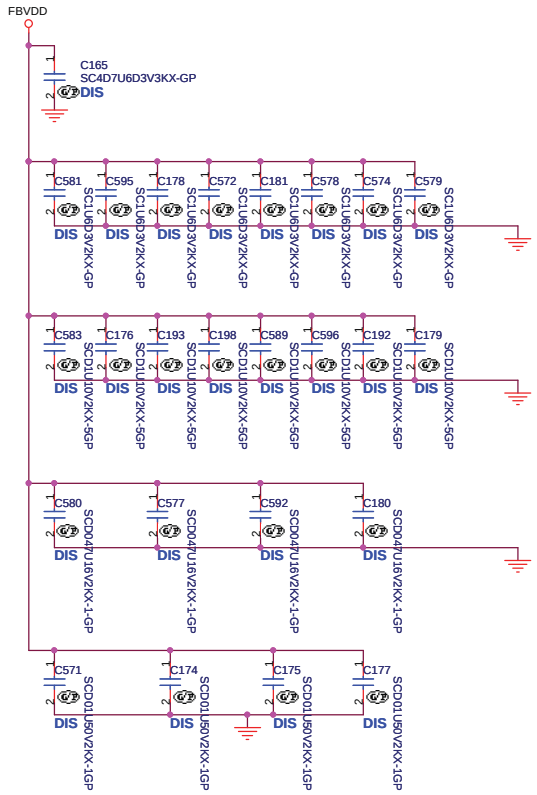
Title: 56_N11M(6/6)_GND

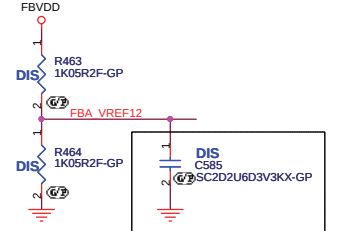
Size	Document Number	Rev
Custom	LA46 MB DIS	-1

Date: Tuesday, January 26, 2010 Sheet 56 of 58

Mode C Command Mapping





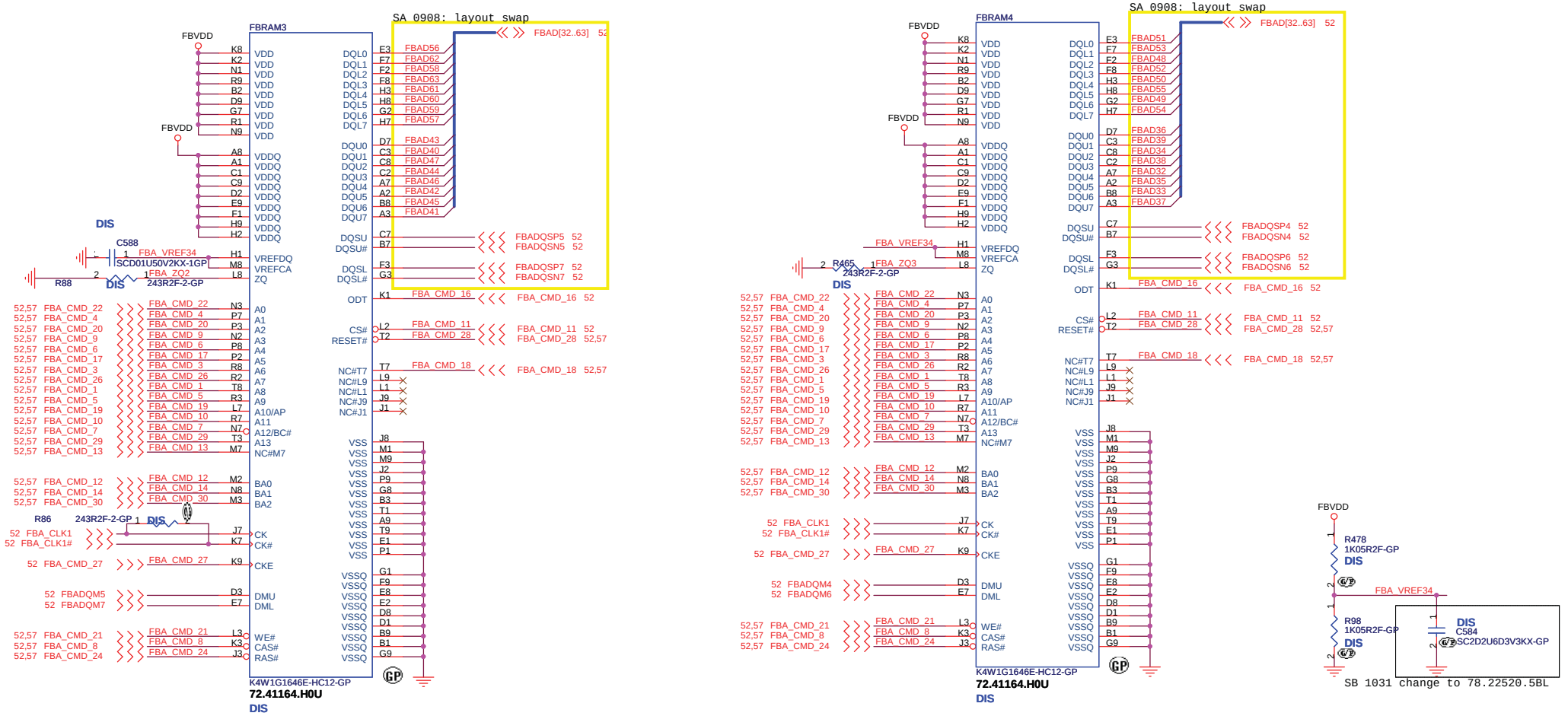


SB 1031 change to 78.22520.5BL

2nd: 72.51G63.C0U (IC SDRAM H5TQ1G63BFR-12C FBGA)

<Core Design>

緯創資通	Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title	57_VRAM(1/2)	
Size: Custom	Document Number: LA46 MB DIS	Rev: -1
Date: Tuesday, January 26, 2010	Sheet 57 of 58	



<Core Design>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title	58 VRAM(2/2)	
Size: Custom	Document Number: LA46 MB DIS	Rev: -1
Date: Tuesday, January 26, 2010	Sheet 58 of 58	