Hummingbird1_HR
DIS/UMA/Muxless Schematics Document
Sandy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

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Project code : 91.4QP01.001
PCB P/N :
Revision : 2

Hummingbird1_HR Block Diagram

SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

Intel CPU
Sandy Bridge
FSB: 1066 MHz
4,5,6,7,8,9,10,11,12,13

DDRIII 1066/1333 Channel A

RAM x 8 | RAM x 8
RAM x 8 | RAM x 8
RAM x 8 | RAM x 8
RAM x 8 | RAM x 8

FDIx4x2
DMIx4

HDMI 51
LCD 49
HDMI
LVDS(Single Channel)

Intel
PCH
Cougar Point
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
17,18,19,20,21,22,23,24,25,26

FPC
FFC
MINI Board
PCI-E x1
USB x1
Mini-Card
802.11a/b/g
SATA x1
M-SATA
Charger signal
Charger Circuit

Left Side: USB x 2
CAMERA 49
USB2.0 x 3

FFC
Card Reader Board
USB 2.0 x 1
CardReader
RTS5129
SD/MMC

AZALIA
SPI
LPC Bus
SATA x1
HDD 56

Internal Digital MIC
HP1
Azalia CODEC
ALC271X-VB3
29
2CH SPEAKER

Flash ROM 4MB 60
LPC debug port 71

KBC
NUVOTON
NPCE795P 27
SMBus

Touch PAD 69
Int. KB 69
Thermal ENE P2800 28
Fan 28

HR PX

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Title		
Block Diagram		
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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA Pair	SATA Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Variant Name>

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

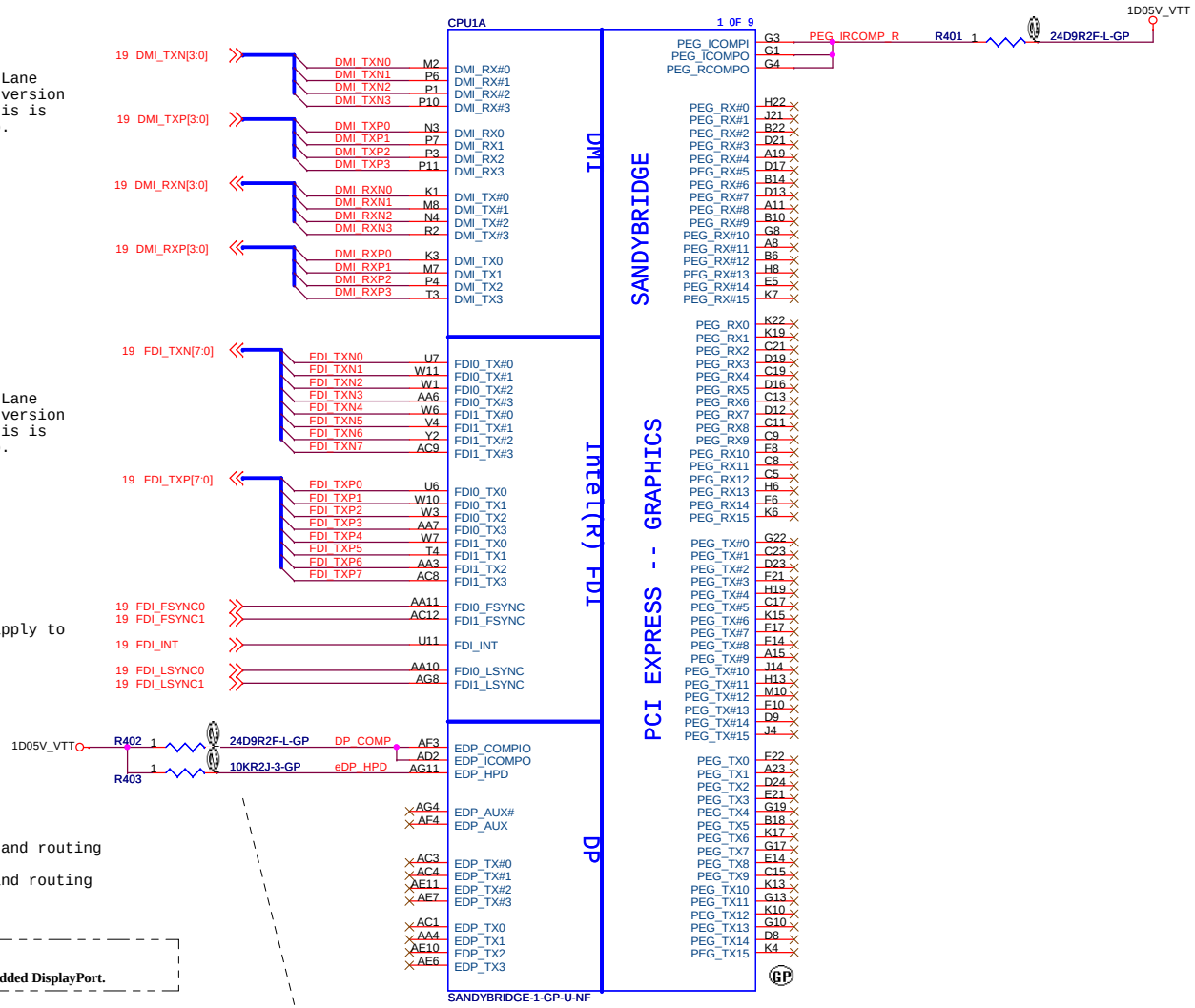
Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.



SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics or without eDP
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5%
resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5%
resistorpower (~15 mW) may be wasted.

CPU1B — 2 OF 9

SANDYBRIDGE-1-GP-U-NF

MISC
- PROC_SELECT# (F49) ← 18 H_SNB_IVB#
- PROC_DETECT# (C57)

CLOCKS
- BCLK (J3) / BCLK# (H2) → CLK_EXP_P 20 / CLK_EXP_N 20
- DPLL_REF_CLK (AG3) / DPLL_REF_CLK# (AG1) → CLK_DP_P_R / CLK_DP_N_R → RN504 SRN1KJ-7-GP → 1D05V_VTT
- BCLK_ITP (N59) / BCLK_ITP# (N58)

SANDYBRIDGE THERMAL
- CATERR# (C49)
- PECI (A48) ↔ 22,27 H_PECI
- PROCHOT# (C45) ← 27,42 H_PROCHOT# — R513 1 — H_PROCHOT#_R — 56R2J-4-GP
- THERMTRIP# (D45) ← 22,36 H_THERMTRIP#

DDR3 MISC
- SM_DRAMRST# (AT30) → SM_DRAMRST# 37 — 4K99R2F-L-GP — R502
- SM_RCOMP0 (BF44) — SM_RCOMP_0 R506 — 140R2F-GP
- SM_RCOMP1 (BE43) — SM_RCOMP_1 R507 — 25D5R2F-GP
- SM_RCOMP2 (BG43) — SM_RCOMP_2 R508 — 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

JTAG & BPM
- PRDY# (N53) / PREQ# (N55)
- TCK (L56) / TMS (L55) / TRST# (J58) → XDP_TRST#
- TDI (M60) / TDO (L59) → XDP_TDO
- DBR# (K58) → XDP_DBRESET#
- BPM#0 (G58) / BPM#1 (E55) / BPM#2 (E59) / BPM#3 (G55) / BPM#4 (G59) / BPM#5 (H60) / BPM#6 (J59) / BPM#7 (J61)

PWR MANAGEMENT
- PM_SYNC (C48) ← 19 H_PM_SYNC
- UNCOREPWRGOOD (B46) ← 22,36,97 H_CPUPWRGD — R503 10KR2J-3-GP
- SM_DRAMPWROK (BE45) ← 19,37 PM_DRAM_PWRGD — R505 0R2J-2-GP (DY) — VDDPWRGOOD ← 37 VDDPWRGOOD
- RESET# (D44) ← BUF_CPU_RST#

1D05V_VTT — R501 62R2J-GP — H_PROCHOT# — C502 SC47P50V2JN-3GP

CRB : 47pf
CEKLT:43pf

Connect EC to PROCHOT# through inverting OD buffer.

1D05V_VTT — RN502 SRN51J-GP — XDP_TDO / XDP_TRST#

3D3V_S0 — RN503 SRN1K5J-1-GP — XDP_DBRESET# / 18,27,36,71,82,97 PLT_RST# → BUF_CPU_RST#

<Core Design>

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Title: CPU (THERMAL/CLOCK/PM)

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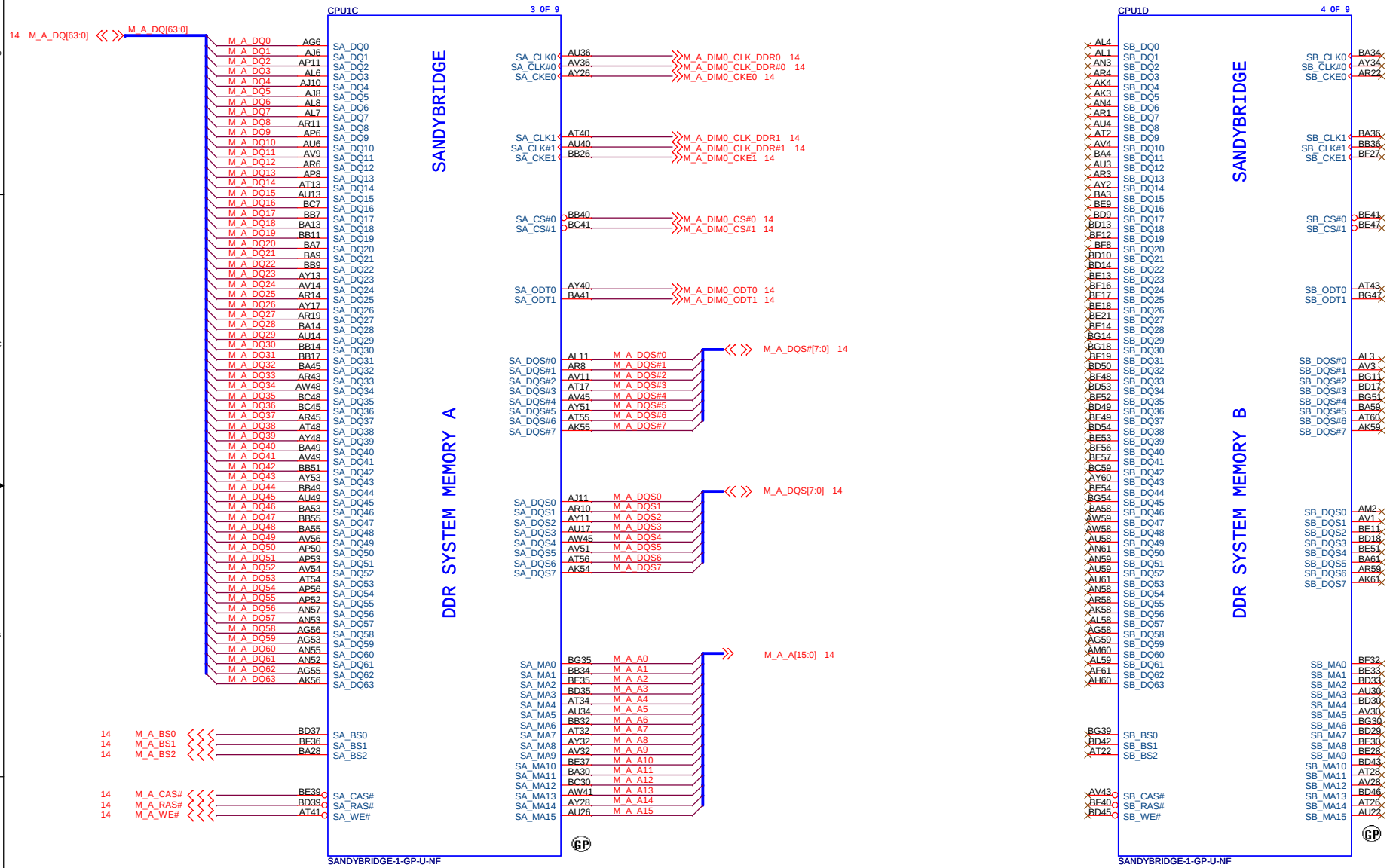
SSID = CPU



<Core Design>

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Title: CPU (DDR)

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

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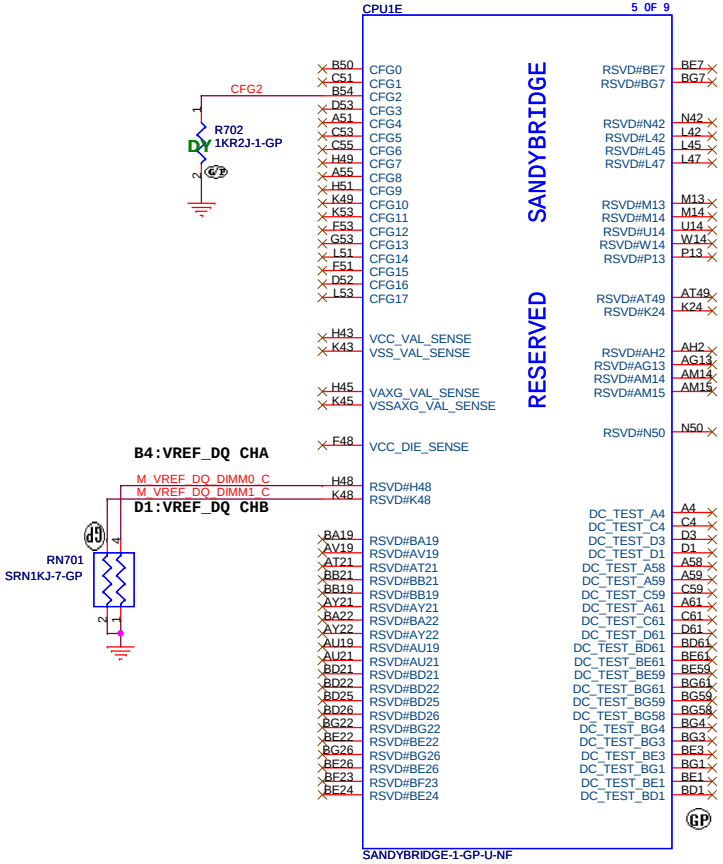
SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

<Core Design>

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Title: CPU (RESERVED)

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SSID = CPU

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

VCC_CORE

PROCESSOR CORE POWER: 53A

SC2D2U6D3V2MX-GP: C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834

Layout Note: 2.2u Cap place under CPU

SC2D2U6D3V2MX-GP: C837, C841, C847, C848

VCC Output Decoupling CAP Recommendation:

1. 1.9m ohm loadline design:(for 3V)
4 x 470 uF
25 x 22 uF
35 x 2.2uF

2. 2.9m ohm loadline design: (for ULV/LV)
3 x 330uF
12 x 22uF
16 x 2.2uF

CPU1F — 6 OF 9 — SANDYBRIDGE

VCC_CORE

VCC: A26, A29, A31, A34, A35, A38, A39, A42, C26, C27, C32, C34, C37, C39, C42, D27, D32, D34, D37, D39, D42, E26, E28, E32, E34, E37, E38, F25, F26, F28, F32, F34, F37, F38, F42, G42, H25, H26, H28, H29, H32, H34, H35, H37, H38, H40, J25, J26, J28, J29, J32, J34, J35, J37, J38, J40, J42, K26, K27, K29, K32, K34, K35, K37, K39, K42, L25, L28, L33, L36, L40, N26, N30, N34, N38

CORE SUPPLY

VCCIO: AF46, AG48, AG50, AG51, AJ17, AJ21, AJ25, AJ43, AJ47, AK50, AK51, AL14, AL15, AL16, AL20, AL22, AL26, AL45, AL48, AM16, AM17, AM21, AM43, AM47, AN20, AN42, AN45, AN48

VCCIO Output Decoupling CAP Recommendation:
2 x 330 uF 10 x 10 uF (0603)
26 x 1uF(0402)

PROCESSOR VCCIO: 8.5A

1D05V_VTT

C853 SC10U6D3V3MX-GP, C854 SC10U6D3V3MX-GP, C856 SC10U6D3V3MX-GP

Layout Note: 10u Cap place during CPU & VR

PEG AND DDR

VCCIO: AA14, AA15, AB17, AB20, AC13, AD16, AD18, AD21, AE14, AE15, AE16, AE18, AF20, AG15, AG16, AG17, AG20, AG21, AJ14, AJ15

1D05V_VTT

C857 SC1U10V2KX-1GP, C858 SC1U10V2KX-1GP, C859 SC1U10V2KX-1GP, C860 SC1U10V2KX-1GP, C861 SC1U10V2KX-1GP, C862 SC1U10V2KX-1GP, C863 SC1U10V2KX-1GP, C864 SC1U10V2KX-1GP, C866 SC1U10V2KX-1GP

Layout Note: 1u Cap place under CPU

C883 SC1U10V2KX-1GP, C884 SC1U10V2KX-1GP, C885 SC1U10V2KX-1GP, C886 SC1U10V2KX-1GP, C887 SC1U10V2KX-1GP, C878 SC1U10V2KX-1GP, C880 SC1U10V2KX-1GP

VCCIO: W16, W17

Check Pull high ??

VCCIO_SEL — BC22 H_VCCP_SEL_L — TP805

PROCESSOR 1.05V Quiet rail for DDR block (BGA only)
+V1.05S_VCCPQE should be short to +V1.05S_VCCP_DDR_R on board

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

QUIET RAILS

VCCPQE: AM25, AN22 — +V1.05S_VCCPQE — R806 0R0402-PAD — C877 SC1U6D3V2KX-GP

1D05V_VTT

SVID

VIDALERT# A44 H_CPU_SVIDALRT# — R803 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK B43 H_CPU_SVIDCLK — H_CPU_SVIDCLK 42
VIDSOUT C44 H_CPU_SVIDDAT — H_CPU_SVIDDAT 42

R804 130R2F-1-GP

SENSE LINES

VCC_CORE

R801 100R2F-L1-GP-U

VCC_SENSE F43 — VCCSENSE 42
VSS_SENSE G43 — VSSSENSE 42

R805 10R2F-L-GP — 1D05V_VTT — DY

VCCIO_SENSE AN16 — VCCIO_SENSE 45
VSS_SENSE_VCCIO AN17 — VSSIO_SENSE 45

R802 100R2F-L1-GP-U

R807 10R2F-L-GP — DY

Place near processor

SANDYBRIDGE-1-GP-U-NF

<Core Design>

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Title: **CPU (VCC_CORE)**

Size: Custom | Document Number: Hummingbird1_HR | Rev: -2

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SSID = CPU

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SANDYBRIDGE

POWER

GRAPHICS

DDR3 - 1.5V RAILS

SENSE LINES

QUIET RAILS

1.8V RAIL

SA RAIL

SENSE LINES

SANDYBRIDGE-1-GP-U-NF

S3 power reduction DDR Vref schematic

Refer to the latest Huron River Mainstream PDG (Doc# 438297) for more details

SM_VREF AY43 +V_SM_VREF_CNT → +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

VCC_GFXCORE

VAXG: AA46 AB47 AB50 AB51 AB52 AB53 AB55 AB56 AB58 AB59 AC61 AD47 AD48 AD50 AD51 AD52 AD53 AD55 AD56 AD58 AD59 AE46 N45 P47 P48 P50 P51 P52 P53 P55 P56 P61 T48 T58 T59 T61 U46 V47 V48 V50 V51 V52 V53 V55 V56 V58 V59 W50 W51 W52 W53 W55 W56 W61 Y48 Y61

C919 C940 C941 C942 C943 C949 C950 — SC1U10V2KX-1GP

C911 C912 C913 C914 C915 C916 C917 C918 — SC1U10V2KX-1GP

VAXG Output Decoupling CAP Recommendation:

1. 3.9m ohm loadline design:(for GT2)
2 x 470 uF 6 x 22 uF (0805)
6 x 10 uF (0603) 11 x 1 uF (0402)

2. 4.6m ohm loadline design:(for GT1)
2 x 330 uF 5 x 22 uF (0805)
6 x 10 uF (0603) 6 x 1 uF (0402)

VCC_GFXCORE

R906 10R2F-L-GP

42 VCC_AXG_SENSE
42 VSS_AXG_SENSE

R907 10R2F-L-GP

VCC_AXG_SENSE F45 VAXG_SENSE
VSS_AXG_SENSE G45 VSSAXG_SENSE

1D8V_S0

PROCESSOR VCCPLL: 1.2A

BB3 BC1 BC4 VCCPLL

C928 C929 — SC1U10V2KX-1GP

VCCPLL Output Decoupling CAP Recommendation:
1 x 330 uF
2 x 1 uF (0402)

1D05V_VTT 0D85V_S0

PROCESSOR VCCSA: 6A

R911 Celeron
R910 0R5J-5-GP Celeron
0R5J-5-GP
R913 Celeron
0R5J-5-GP

C921 C923 — SC10U6D3V3MX-GP

Layout Note: Place under CPU

C927 C851 — SC1U10V2KX-1GP

VCCSA: L17 L21 N16 N20 N22 P17 P20 R16 R18 R21 U15 V16 V17 V18 V21 W20

PROCESSOR VDDQ: 10A

1D5V_S0

VDDQ: AJ28 AJ33 AJ36 AJ40 AL30 AL34 AL38 AL42 AM33 AM36 AM40 AN30 AN34 AN38 AR26 AR28 AR30 AR32 AR34 AR36 AR40 AV41 AW26 BA40 BB28 BG33

C930 C931 C932 C933 — SC22U4V3MX-GP

EC901 — SCD1U50V3KX-GP

Layout Note: Place during CPU & VR

Layout Note: Place under CPU

C936 C937 C938 C939 C952 C953 C954 C955 C956 — SC1U10V2KX-1GP

Layout Note:
Place near SM_VREF pin

VDDQ Output Decoupling Recommendation:
1 x 330 uF 8 x 10uF (0603)
10 x 1 uF (0402)

1D5V_S0

VCCDQ: AM28 AN26

+1.5S_VCCD_Q R909 0R0402-PAD

C948 SC1U6D3V2KX-GP

PROCESSOR DDR 1.5V QUIET RAIL (BGA only)
+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

VDDQ_SENSE BC43 TP_VDDQ_SENSE
VSS_SENSE_VDDQ BA43 TP_VDDQ_VSS

TP901 TPAD14-GP
TP902 TPAD14-GP

VCCSA_SENSE U10 → VCCSA_SENSE

R912 10R2J-2-GP **Notice: pull-high 100k or 10k**

Delete off page VCCSA_SENSE SA

VID0 VID1

VCCSA_VID D48 H_FC_C22
VCCSA_VID D49 VCCSA_SEL → VCCSA_SEL 48

Delete off page H_FC_C22 SA

RN901 SRN1KJ-11-GP-U

Power Delivery DG; #139028
A 1-K pull-down resistor should be placed on the VCCSA_VID lines.

<Core Design>

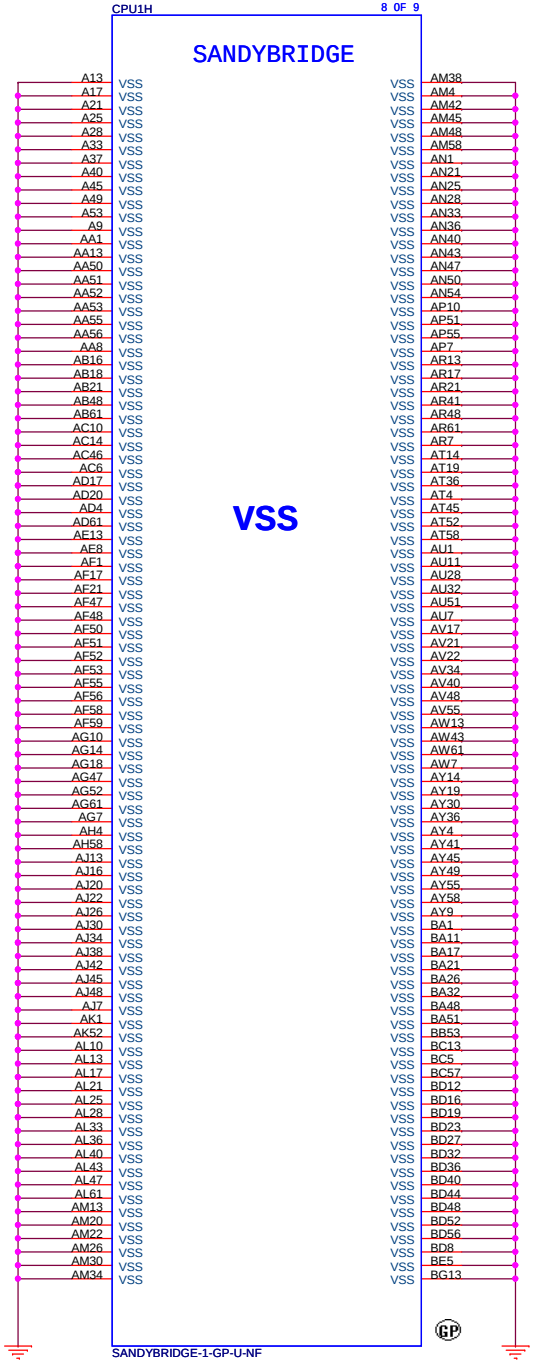
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

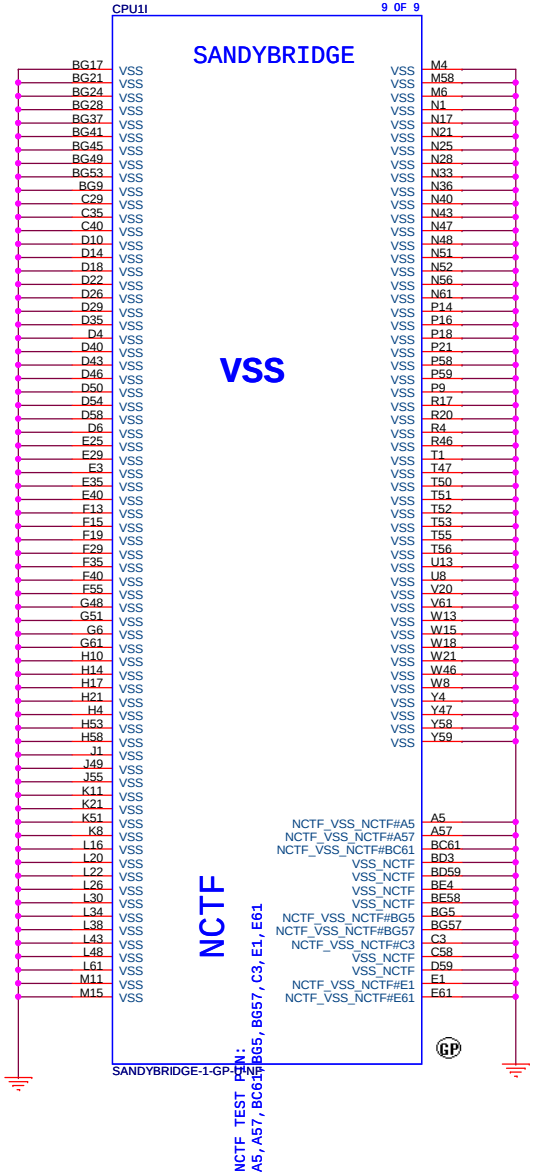
Title: CPU (VCC_GFXCORE)

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 9 of 102

SSID = CPU





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 10 of 102

Blanking

HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***XDP***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 11 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 12 of 102

(Blanking)

<Variant Name>

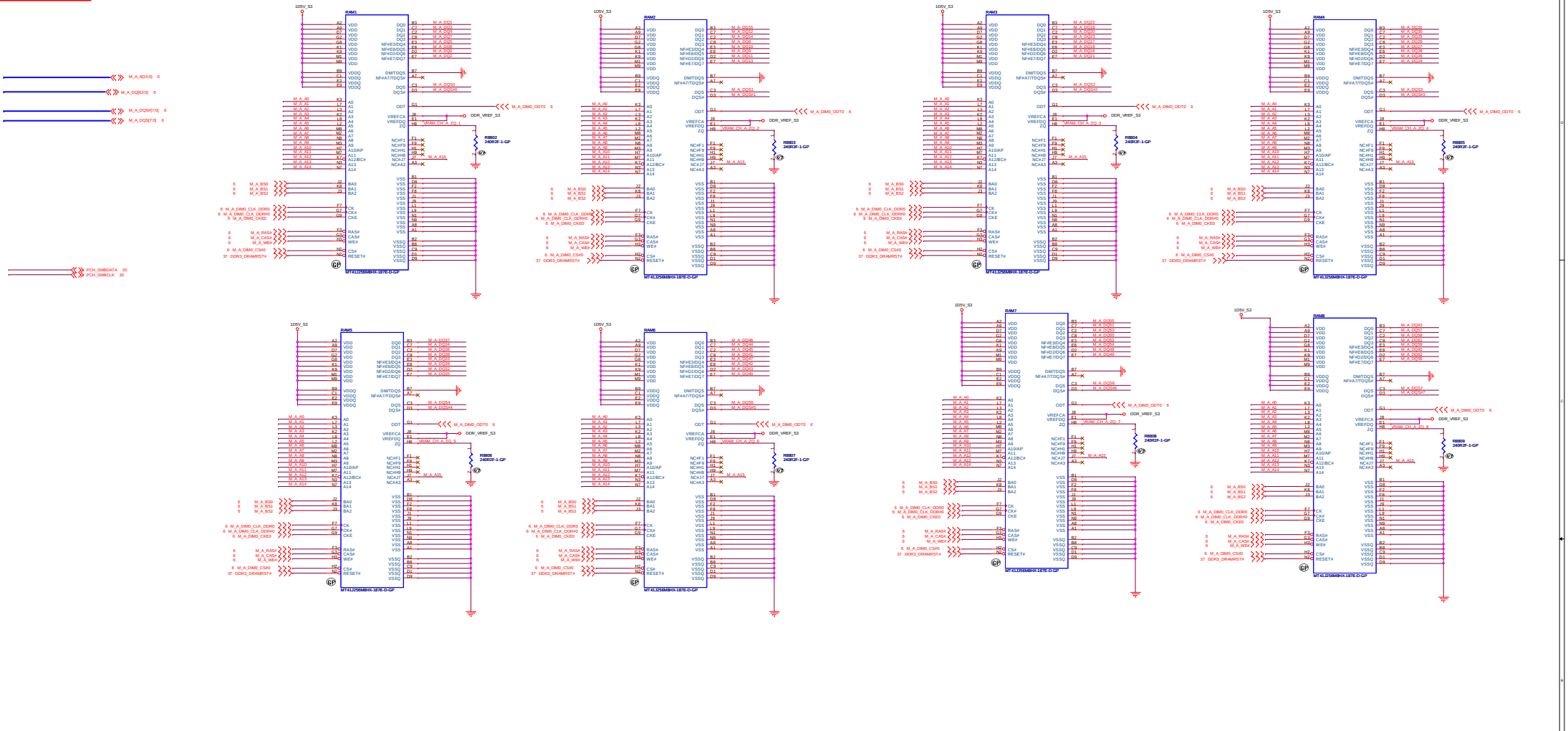
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

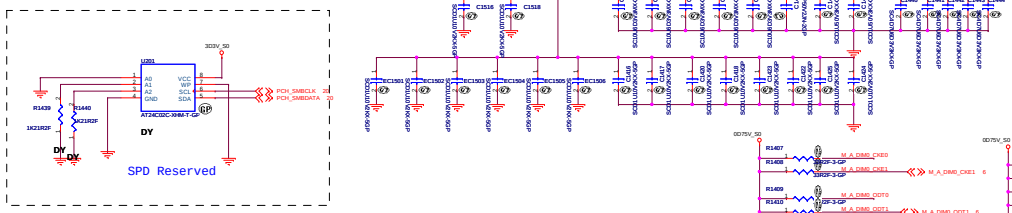
Title: ***Reserved***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 13 of 102

SSID = MEMORY





緯創資通 Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: DDR3-SODIMM1			
Size: A1	Document Number: Hummingbird1_HR	Rev: -2	
Date: Tuesday, April 17, 2012	Sheet 14 of 39		

SSID = MEMORY

HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
Custom	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 15 of 102

(Blanking)

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DDR3-SODIMM2

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 16 of 102

3D3V_S0

RN1703 SRN2K2J-1-GP
LVDS_DDC_CLK
LVDS_DDC_DATA

RN1701 SRN2K2J-1-GP
L_CTRL_DATA
L_CTRL_CLK

RN1702 SRN100KJ-6-GP
PANEL_BLEN
LCDVDD_EN

L_DDC_DATA(PAGE17):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is used for the local flat panel display

Place near PCH

R1701 2K37R2F-GP

RN1704 SRN0J-6-GP

Impedance:90 ohm

PCH1D — 4 OF 10 — Cougar Point — Digital Display Interface

27 PANEL_BLEN, 49 LCDVDD_EN	J47, M45	L_BKLTEN, L_VDD_EN	
49 LBKLT_CTL	P45	L_BKLTCTL	
49 LVDS_DDC_CLK, 49 LVDS_DDC_DATA	T40, K47	L_DDC_CLK, L_DDC_DATA	
L_CTRL_CLK, L_CTRL_DATA	T45, P39	L_CTRL_CLK, L_CTRL_DATA	
LVDS_IBG	AF37, AF36	LVD_IBG, LVD_VBG	
LVDS_VREFH, LVDS_VREFL	AE48, AE47	LVD_VREFH, LVD_VREFL	
49 LVDSA_CLK#, 49 LVDSA_CLK	AK39, AK40	LVDSA_CLK#, LVDSA_CLK	LVDS
49 LVDSA_DATA0#, 49 LVDSA_DATA1#, 49 LVDSA_DATA2#	AN48, AM47, AK47, AJ48	LVDSA_DATA#0, LVDSA_DATA#1, LVDSA_DATA#2, LVDSA_DATA#3	LVDS
49 LVDSA_DATA0, 49 LVDSA_DATA1, 49 LVDSA_DATA2	AN47, AM49, AK49, AJ47	LVDSA_DATA0, LVDSA_DATA1, LVDSA_DATA2, LVDSA_DATA3	LVDS
	AF40, AF39	LVDSB_CLK#, LVDSB_CLK	
	AH45, AH47, AF49, AF45	LVDSB_DATA#0, LVDSB_DATA#1, LVDSB_DATA#2, LVDSB_DATA#3	
	AH43, AH49, AF47, AF43	LVDSB_DATA0, LVDSB_DATA1, LVDSB_DATA2, LVDSB_DATA3	
SDVO_TVCLKINN, SDVO_TVCLKINP	AP43, AP45		
SDVO_STALLN, SDVO_STALLP	AM42, AM40		
SDVO_INTN, SDVO_INTP	AP39, AP40		
SDVO_CTRLCLK, SDVO_CTRLDATA	P38, M39		
DDPB_AUXN, DDPB_AUXP, DDPB_HPD	AT49, AT47, AT40		
DDPB_0N, DDPB_0P, DDPB_1N, DDPB_1P, DDPB_2N, DDPB_2P, DDPB_3N, DDPB_3P	AV42, AV40, AV45, AV46, AU48, AU47, AV47, AV49		
DDPC_CTRLCLK, DDPC_CTRLDATA	P46, P42		
DDPC_AUXN, DDPC_AUXP, DDPC_HPD	AP47, AP49, AT38		
DDPC_0N, DDPC_0P, DDPC_1N, DDPC_1P, DDPC_2N, DDPC_2P, DDPC_3N, DDPC_3P	AY47, AY49, AY43, AY45, BA47, BA48, BB47, BB49		
DDPD_CTRLCLK, DDPD_CTRLDATA	M43, M36		
DDPD_AUXN, DDPD_AUXP, DDPD_HPD	AT45, AT43, BH41		
DDPD_0N, DDPD_0P, DDPD_1N, DDPD_1P, DDPD_2N, DDPD_2P, DDPD_3N, DDPD_3P	BB43, BB45, BF44, BE44, BF42, BE42, BJ42, BG42		
	N48, P49, T49	CRT_BLUE, CRT_GREEN, CRT_RED	
DDCCLK, DDCDATA	T39, M40	CRT_DDC_CLK, CRT_DDC_DATA	CRT
	M47, M49	CRT_HSYNC, CRT_VSYNC	
DAC_IREF_R	T43, T42	DAC_IREF, CRT_IRTN	

COUGAR-GP-U2-NF

3D3V_S0

RN1707 SRN4K7J-8-GP

DDCCLK
DDCDATA

R1702 1KR2D-1-GP
DAC_IREF_R

Close to PCH side

3D3V_S0

RN1706 SRN2K2J-1-GP
HDMI

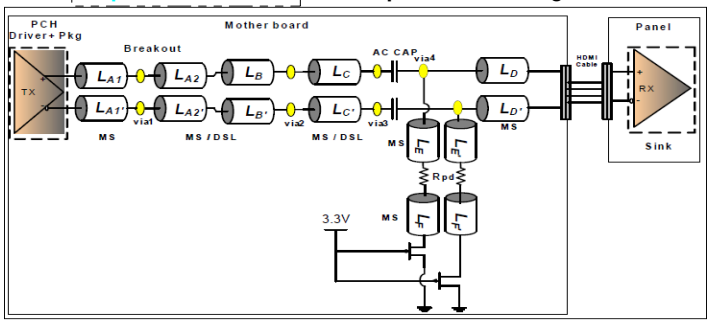
DDI Port B Detect:(SDVO_CTRL_ DATA)
1: Port B detected
0: Port B not detected

PCH_HDMI_CLK 51
PCH_HDMI_DATA 51
HDMI_PCH_DET 51

DDBP_DATA2#	HDMI 1	C1701	SCD1U10V2KX-5GP	HDMI_DATA2_R# 51
DDBP_DATA2	HDMI 1	C1702	SCD1U10V2KX-5GP	HDMI_DATA2_R 51
DDBP_DATA1#	HDMI 1	C1703	SCD1U10V2KX-5GP	HDMI_DATA1_R# 51
DDBP_DATA1	HDMI 1	C1704	SCD1U10V2KX-5GP	HDMI_DATA1_R 51
DDBP_DATA0#	HDMI 1	C1705	SCD1U10V2KX-5GP	HDMI_DATA0_R# 51
DDBP_DATA0	HDMI 1	C1706	SCD1U10V2KX-5GP	HDMI_DATA0_R 51
DDBP_CLK#	HDMI 1	C1707	SCD1U10V2KX-5GP	HDMI_CLK_R# 51
DDBP_CLK	HDMI 1	C1708	SCD1U10V2KX-5GP	HDMI_CLK_R 51

Close to Connector side

Impedance:90 ohm TM request to change 85-ohm



Delete CRT pull down resistor

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 17 of 102

SSID = PCH

RN1801
SRN8K2J-2-GP-U

INT_PIRQF#	1	10	3D3V_S0
INT_PIRQD#	2	9 USB30_SMI#	
INT_PIRQC#	3	8 INT_PIRQA#	
INT_PIRQB#	4	7 INT_PIRQE#	
3D3V_S0	5	6 INT_PIRQH#	

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

CRB : 2.2K
CFKLT: 1K

Sandy Bridge / Ivy Bridge Processor
PROC_SELECT# connected to DF_TVS via 1kΩ (MB), via 4.7kΩ (DT).
DF_TVS needs PU via 2.2kΩ to VccDFTERM

1D8V_S0
R1808 2K2R2J-2-GP
NV_CLE — R1809 1KR2J-1-GP — H_SNB_IVB# 5

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

RN1803
SRN10KJ-5-GP
DGPU_HOLD_RST# 2
DGPU_PWR_EN# 1
4
DY

PCH1E — 5 OF 10 — Cougar Point — COUGAR-GP-U2-NF

RSVD: TP1–TP20, TP21–TP24, TP25–TP40
NVRAM
PCI
USB

USB Ext. port 1 (HS)
External debug port use on Huron river platform

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

DGPU_HOLD_RST#
DGPU_PWR_EN#
TPAD14-GP TP1806
TPAD14-GP TP1804
Strap pin ,Internal PU
DGPU_PWM_SELECT#

INT_PIRQA# INT_PIRQB# INT_PIRQC# INT_PIRQD# → PIRQA# PIRQB# PIRQC# PIRQD#
DGPU_HOLD_RST# DGPU_SELECT# DGPU_PWR_EN# → REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54
GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55
INT_PIRQE# INT_PIRQF# USB30_SMI# INT_PIRQH# → PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5
PME#
5,27,36,71,82,97 PLT_RST# → PLTRST#

DEBUG Card 71 CLK_PCI_LPC — R1804 22R2J-2-GP — CLK_PCI_LPC_R → CLKOUT_PCI0
PCH 20 CLK_PCI_FB — R1805 22R2J-2-GP — CLK_PCI_FB_R → CLKOUT_PCI1
KBC 27 CLK_PCI_KBC — R1806 22R2J-2-GP — CLK_PCI_KBC_R → CLKOUT_PCI2
CLKOUT_PCI3
CLKOUT_PCI4

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USBRBIAS# — USB_RBIAS — R1811 22D6R2F-L1-GP — USBRBIAS

OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO9 OC6#/GPIO10 OC7#/GPIO14 → OC
3D3V_S5 — R1820 10KR2J-3-GP

USB Table

Pair	Device
0	Touch Panel / 3G SIM(DY)
1	USB Ext. port 1 (HS)
2	Fingerprint(DY)
3	BLUETOOT
4	Mini Card2 (WWAN) (DY)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA(DY)
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card(DY)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

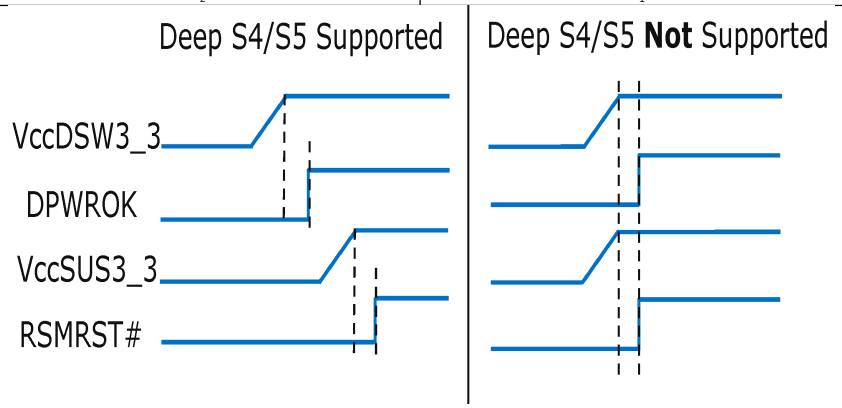
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

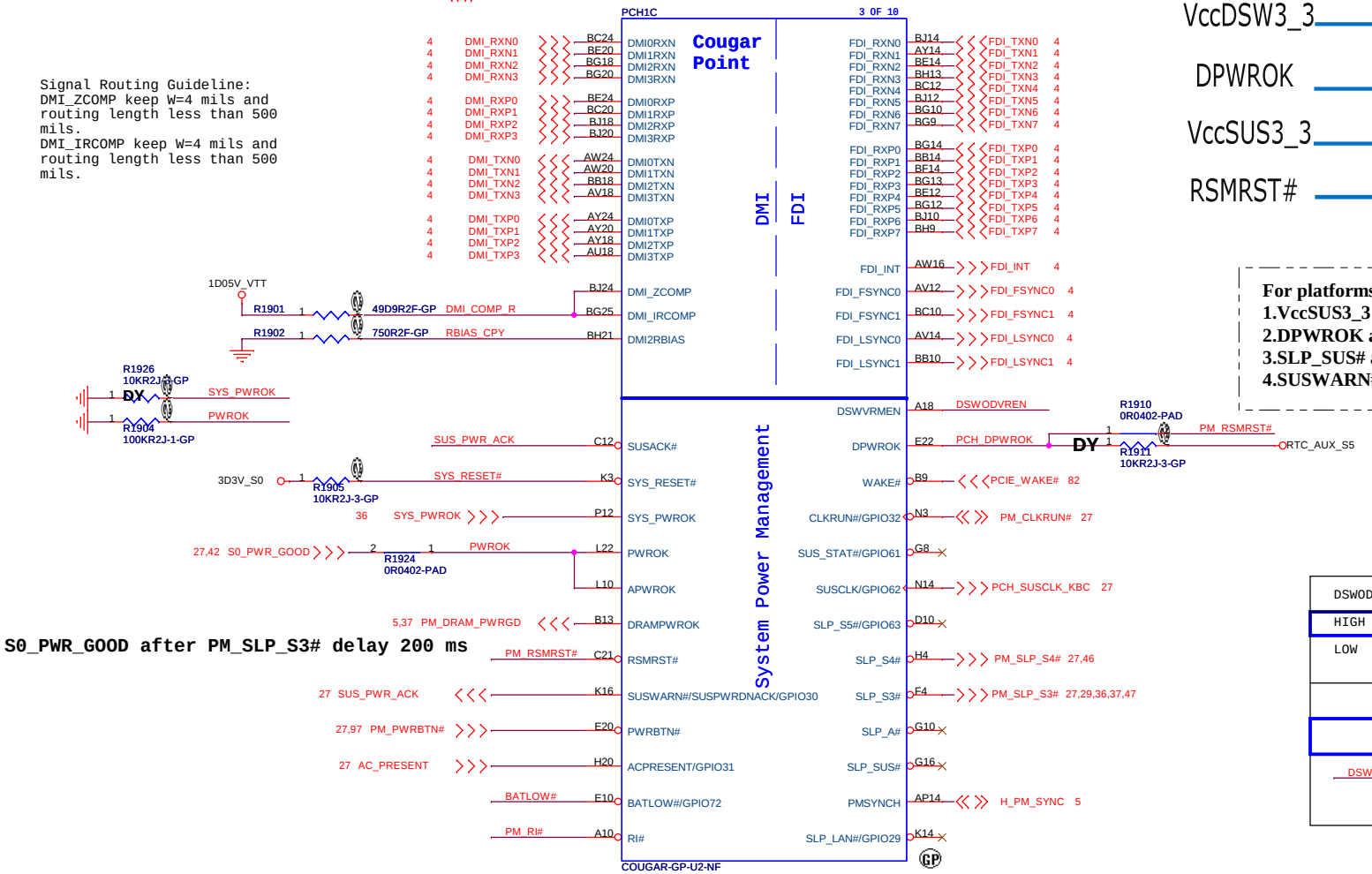
Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: Hummingbird1_HR | Rev: -2
Date: Tuesday, April 17, 2012 | Sheet 18 of 102

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

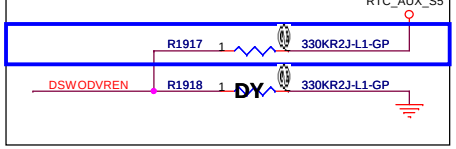


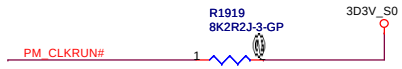
For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

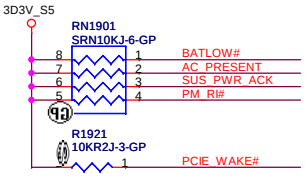


S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

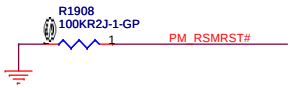




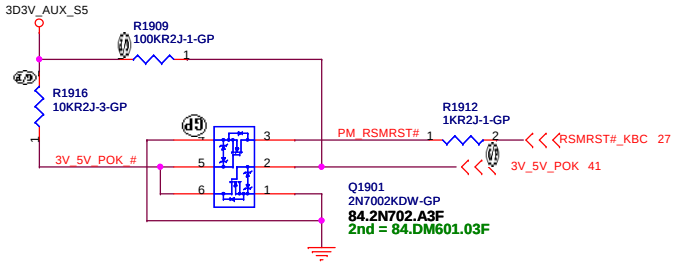


PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor



PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K



84.2N702.A3F
2nd = 84.DM601.03F

<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size: A3 | Document Number: Hummingbird1_HR | Rev: -2
Date: Tuesday, April 17, 2012 | Sheet 19 of 102

SSID = PCH

USB3.0 CLK

3D3V_S0 — RN2018 SRN10KJ-5-GP — PCIE_CLK_RQ2# — CLK_PCIE_WLAN_REQ1#

PCIECLKRQ1# and PCIECLKRQ2# Support S0 power only

check list:
A 10K-ohm PU still need to be used

WWAN CLK

WLAN CLK

PCH1B — 2 OF 10 — Cougar Point

PCI-E*: W-WAN, WLAN, Card Reader, LAN, USB3.0, Intel GBE LAN, Dock, NEW CARD

SMBUS: SMBALERT#/GPIO11 (E12) → EC_SW# 27; SMBCLK (H14) → SMB_CLK; SMBDATA (C9) → SMB_DATA

SMBUS: SML0ALERT#/PCHHOT#/GPIO60 (A12) → DRAMRST_CNTRL_PCH 37; SML0CLK (C8) → SML0_CLK; SML0DATA (G12) → SML0_DATA

SMBUS: SML1ALERT#/PCHHOT#/GPIO74 (C13) → PCH_GPIO74; SML1CLK/GPIO58 (E14) → SML1_CLK 27; SML1DATA/GPIO75 (M16) → SML1_DATA 27

Controller Link: CL_CLK1 (M7), CL_DATA1 (T11), CL_RST1# (P10)

CLOCKS: CLKOUT_PCIE0N/P (Y40/Y39) → CLK_PCIE_WWAN_REQ# (J2) PCIECLKRQ0#/GPIO73

CLOCKS: CLKOUT_PCIE1N/P (AB49/AB47) → CLK_PCIE_WLAN_REQ1# (M1) PCIECLKRQ1#/GPIO18

CLOCKS: CLKOUT_PCIE2N/P (AA48/AA47) → PCIE_CLK_RQ2# (V10) PCIECLKRQ2#/GPIO20

CLOCKS: CLKOUT_PCIE3N/P (Y37/Y36) → PCIE_CLK_LAN_RQ# (A8) PCIECLKRQ3#/GPIO25

CLOCKS: CLKOUT_PCIE4N/P (Y43/Y45) → USB3_PEGB_CLKREQ# (L12) PCIECLKRQ4#/GPIO26

CLOCKS: CLKOUT_PCIE5N/P (V45/V46) → PCIE_CLK_REQ5# (L14) PCIECLKRQ5#/GPIO44

CLOCKS: CLKOUT_PEG_B_N/P (AB42/AB40) → PEG_B_CLKRQ# (E6) PEG_B_CLKRQ#/GPIO56

CLOCKS: CLKOUT_PCIE6N/P (V40/V42) → PCIE_CLK_REQ6# (T13) PCIECLKRQ6#/GPIO45

CLOCKS: CLKOUT_PCIE7N/P (V38/V37) → CLK_PCIE_NEW_REQ# (K12) PCIECLKRQ7#/GPIO46

CLOCKS: CLKOUT_ITPXDP_N/P (AK14/AK13)

RN2012 SRN0J-6-GP: CLK_PCH_SRC6_N (V45), CLK_PCH_SRC6_P (V46)

FLEX CLOCKS: CLKOUTFLEX0/GPIO64 (K43), CLKOUTFLEX1/GPIO65 (F47) → VRAM_SIZE3 (K49) DGPU_PRSNT#, CLKOUTFLEX2/GPIO66 (H47), CLKOUTFLEX3/GPIO67 (K49)

COUGAR-GP-U2-NF

PEG_A_CLKRQ#/GPIO47 (M10) → PEG_CLKREQ# R

CLKOUT_PEG_A_N/P (AB37/AB38)

CLKOUT_DMI_N/P (AV22/AU22) → CLK_EXP_N 5 / CLK_EXP_P 5

CLKOUT_DP_N/P (AM12/AM13)

CLKIN_DMI_N/P (BF18/BE18) → CLK_BUF_EXP_N / CLK_BUF_EXP_P

CLKIN_GND1_N/P (BJ30/BG30) → CLK_BUF_CPYCLK_N / CLK_BUF_CPYCLK_P

RN2008 SRN10KJ-5-GP

CLKIN_DOT_96N/P (G24/E24) → CLK_BUF_DOT96_N / CLK_BUF_DOT96_P

CLKIN_SATA_N/P (AK7/AK5) → CLK_BUF_CKSSCD_N / CLK_BUF_CKSSCD_P

REFCLK14IN (K45) → CLK_BUF_REF14

CLKIN_PCILOOPBACK (H45) → CLK_PCI_FB 18

XTAL25_IN (V47) / XTAL25_OUT (V49)

XCLK_RCOMP (Y47) → R2007 90D9R2F-1-GP → 1D05V_VTT

DDR3 DIMM

KBC

3D3V_S0 — RN2007 SRN2K2J-1-GP

SMB_DATA — Q2001 2N7002KDW-GP — PCH_SMBDATA 14

84.2N702.A3F
2nd = 84.DM601.03F

SMB_CLK — PCH_SMBCLK 14

For DIS_PX mode or MXM mode.

3D3V_S5 — R2004 10KR2J-3-GP — PEG_CLKREQ# R

XTAL25_IN — R2006 1M1R2J-GP — X2001 XTAL-25MHZ-102-GP 82.30020.851 2nd = 82.30020.791 — XTAL25_OUT

C2008 SC12P50V2JN-3GP

C2007 SC12P50V2JN-3GP

3D3V_S0 — RN2010 SRN10KJ-5-GP — DGPU_PRSNT# — UMA_DIS# 22

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

Delete Pull down R

check list:
A 10K-ohm PU still need to be used

RN2009 SRN10KJ-L3-GP: CLK_BUF_REF14, CLK_BUF_CKSSCD_P, CLK_BUF_CKSSCD_N, CLK_BUF_EXP_P, CLK_BUF_EXP_N, CLK_BUF_DOT96_N, CLK_BUF_DOT96_P

need very close to PCH

3D3V_S5

-SA Athero suggest PU 4.7K

R2003 4K7R2J-2-GP — PCIE_CLK_LAN_RQ#

CLK_PCIE_WWAN_REQ# — USB3_PEGB_CLKREQ# — RN2001 SRN10KJ-5-GP

RN2002 SRN10KJ-6-GP: PCIE_CLK_REQ5#, CLK_PCIE_NEW_REQ#, EC_SW#, PCH_GPIO24

PCH_GPIO24 — PCH_GPIO24 22

3D3V_S5 — RN2003 SRN2K2J-1-GP: SMB_CLK, SMB_DATA

RN2004 SRN2K2J-1-GP: SML0_DATA, SML0_CLK

RN2005 SRN2K2J-1-GP: SML1_CLK, SML1_DATA

RN2006 SRN10KJ-5-GP: PCH_GPIO74, PCIE_CLK_REQ6#

R2009 1KR2J-1-GP — DRAMRST_CNTRL_PCH

– Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
– Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

<Variant Name>

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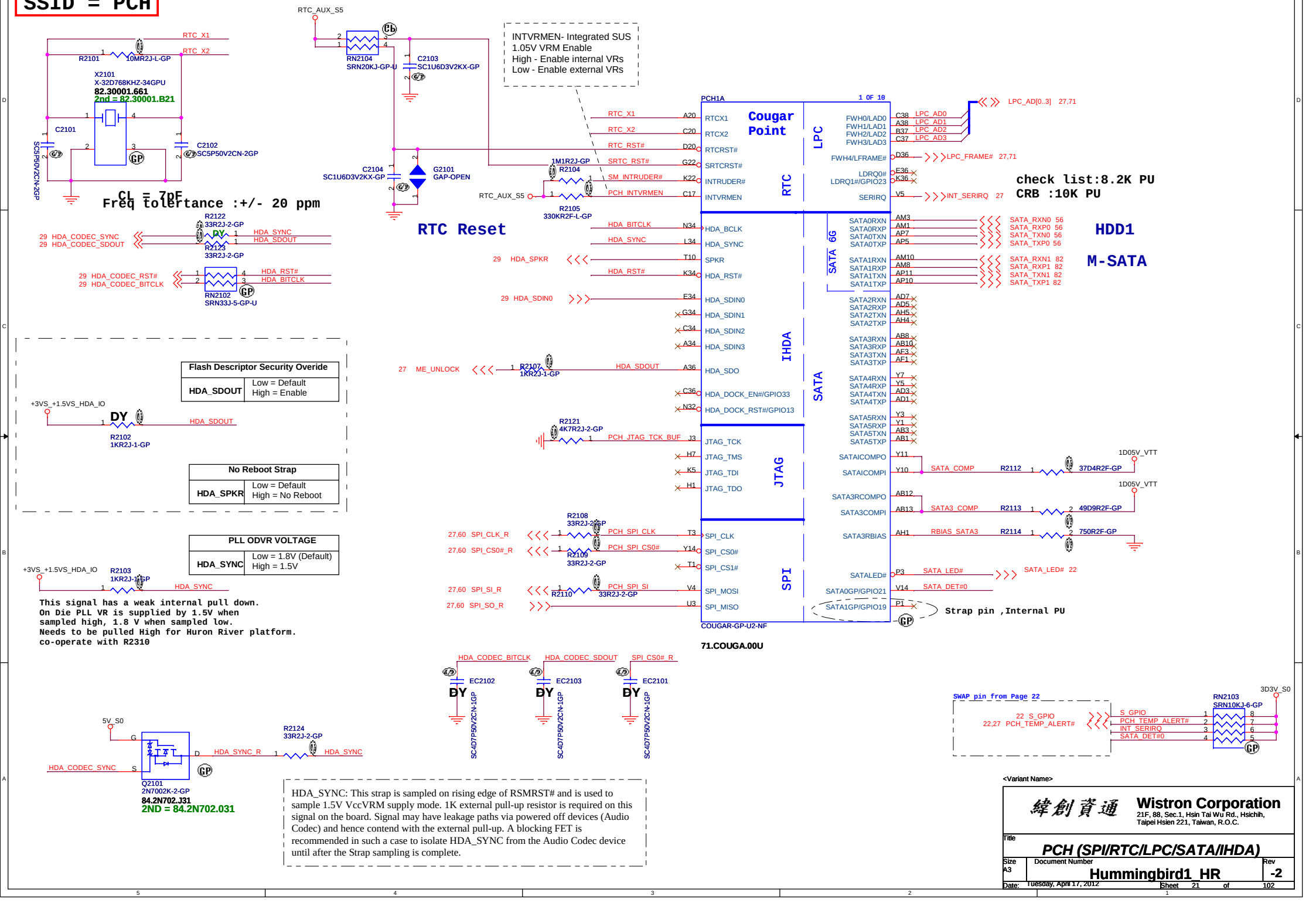
Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 20 of 102

SSID = PCH



<variant_name>

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Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 21 of 102

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_RCIN# — H_A20GATE

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

check list:
if are unused,PU or PD

Pass Word Clear

GFX_CRB_DET — R2206 100KR2J-1-GP

3D3V_S0 — R2202 10KR2J-3-GP — SATA_ODD_PRSNT#

TPAD14-GP TP2204 — DGPU_PWROK

TPAD14-GP TP2203 — PCH_GPIO27

PSW_CLR# — G2201 GAP-OPEN

RN2201 SRN10KJ-6-GP — EC_SMI# / EC_SCI# / DGPU_HPD_INTR#

RN2202 SRN10KJ-6-GP — PSW_CLR# / FP_DET# / MFG_MODE / SATA_LED#

SWAP pin from Page 20 — 21 SATA_LED#

RN2204 SRN10KJ-6-GP — PEG_B_CLKRQ# / USB3_PWR_ON / PCH_GPIO12

SWAP pin from Page 20 — 20 PEG_B_CLKRQ#

PCH_GPIO15 — R2201 1KR2J-1-GP

PCH1F — 6 OF 10

Cougar Point

GPIO:
- S_GPIO — T7 BMBUSY#/GPIO0
- EC_SMI# — A42 TACH1/GPIO1
- DGPU_HPD_INTR# — H36 TACH2/GPIO6
- EC_SCI# — E38 TACH3/GPIO7
- ICC_EN# — C10 GPIO8
- PCH_GPIO12 — C4 LAN_PHY_PWR_CTRL/GPIO12
- PCH_GPIO15 — G2 GPIO15
- SATA_ODD_PRSNT# — U2 SATA4GP/GPIO16
- DGPU_PWROK — D40 TACH0/GPIO17
- PCH_GPIO22 — T5 SCLOCK/GPIO22
- PCH_GPIO24 — E8 GPIO24/MEM_LED
- PCH_GPIO27 — E16 GPIO27
- PLL_ODVR_EN — P8 GPIO28
- PSW_CLR# — K1 STP_PCI#/GPIO34
- FP_DET# — K4 GPIO35
- DMI_OVRVLTG — V8 SATA2GP/GPIO36
- FDI_OVRVLTG — M5 SATA3GP/GPIO37
- MFG_MODE — N2 SLOAD/GPIO38
- GFX_CRB_DET — M3 SDATAOUT0/GPIO39
- VRAM_SIZE4 — V13 SDATAOUT1/GPIO48
- PCH_TEMP_ALERT# — V3 SATA5GP/GPIO49
- USB3_PWR_ON — D6 GPIO57

CPU/MISC:
- TACH4/GPIO68 — C40 SATA_ODD_PWRGT — TP2205 TPAD14-GP
- TACH5/GPIO69 — B41 UMA_DIS# 20
- TACH6/GPIO70 — C41 VRAM_SIZE1
- TACH7/GPIO71 — A40 VRAM_SIZE2
- A20GATE — P4 H_A20GATE 27
- PECI — AU16 H_PECI_R — R2203 0KR2J-2-GP DY — H_PECI 5,27
- RCIN# — P5 H_RCIN# 27
- PROCPWRGD — AY11 H_CPUPWRGD 5,36,97
- THRMTRIP# — AY10 PCH_THERMTRIP_R
- INIT3_3V# — T14

PCH_THERMTRIP_R — R2204 390R2F-2GP — H_THERMTRIP# 5,36

design guide and CRB cirucit stuff 390-ohm
JE40_HR stuff 54.9-ohm

- TS_VSS1 — AH8
- TS_VSS2 — AK11
- TS_VSS3 — AH10
- TS_VSS4 — AK10
- NC_1 — P37

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

NCTF:
- NCTF_VSS#A4 — A4
- NCTF_VSS#A44 — A44
- NCTF_VSS#A45 — A45
- NCTF_VSS#A46 — A46
- NCTF_VSS#A5 — A5
- NCTF_VSS#A6 — A6
- NCTF_VSS#B3 — B3
- NCTF_VSS#B47 — B47
- NCTF_VSS#BD1 — BD1
- NCTF_VSS#BD49 — BD49
- NCTF_VSS#BE1 — BE1
- NCTF_VSS#BE49 — BE49
- NCTF_VSS#BF1 — BF1
- NCTF_VSS#BF49 — BF49
- NCTF TEST PIN: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49
- NCTF_VSS#BG2 — BG2
- NCTF_VSS#BG48 — BG48
- NCTF_VSS#BH3 — BH3
- NCTF_VSS#BH47 — BH47
- NCTF_VSS#BJ4 — BJ4
- NCTF_VSS#BJ44 — BJ44
- NCTF_VSS#BJ45 — BJ45
- NCTF_VSS#BJ46 — BJ46
- NCTF_VSS#BJ5 — BJ5
- NCTF_VSS#BJ6 — BJ6
- NCTF_VSS#C2 — C2
- NCTF_VSS#C48 — C48
- NCTF_VSS#D1 — D1
- NCTF_VSS#D49 — D49
- NCTF_VSS#E1 — E1
- NCTF_VSS#E49 — E49
- NCTF_VSS#F1 — F1
- NCTF_VSS#F49 — F49
- NCTF TEST PIN: BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49

COUGAR-GP-U2-NF

FDI_OVRVLTG — R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI_OVRVLTG — R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

ICC_EN# — R2211 1KR2J-1-GP

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL_ODVR_EN — R2212 1KR2J-1-GP DY

VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

3D3V_S0 — R2218 10KR2J-3-GP — PCH_GPIO22 — R2219 10KR2J-3-GP DY

3D3V_S0 — R2214 4G — R2220 MICRON_ELPIDA — R2216 ELPIDA_S/H — R2221 2G — R2215 NANY_S/H — R2217 MICRON_NANY

(GPIO48 Pin4) VRAM_SIZE4 — (GPIO70 Pin2) VRAM_SIZE1 — (GPIO71 Pin1) VRAM_SIZE2

3D3V_S0 — R2230 DYRAM — R2231 RAM — VRAM_SIZE3 — VRAM_SIZE3 20 (GPIO65 Pin3)

GPIO48 DRAM_Type4	GPIO65 DRAM_Type3	GPIO70 DRAM_Type1	GPIO71 DRAM_Type2	Status
0	0	0	0	Nanya 2G
0	0	0	1	Micron 2G
0	0	1	0	HYNIX 2G
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	Nanya 4G
1	0	0	1	Micron 4G
1	0	1	0	Samsung 4G
1	0	1	1	ELPIDA 4G
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

<Core Design>

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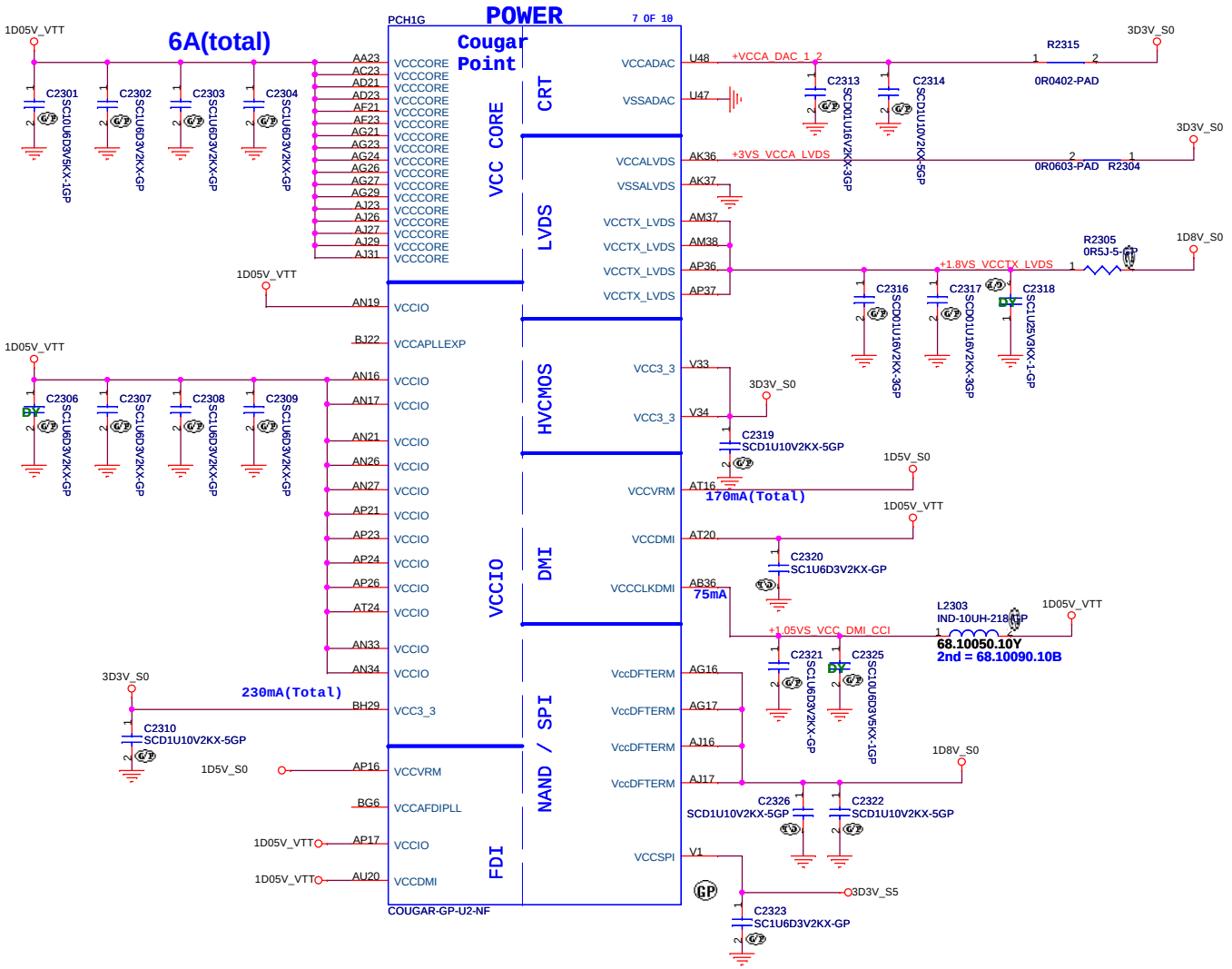
Title: **PCH (GPIO/CPU)**

Size: A3 | Document Number: **Hummingbird1_HR** | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 22 of 102


POWER
Cougar Point
PCH1G
7 OF 10
6A(total)
VCC CORE
CRT
LVDS
HVCMOS
DMI
VCCIO
NAND / SPI
FDI
COUGAR-GP-U2-NF
1D05V_VTT
3D3V_S0
1D8V_S0
1D5V_S0
3D3V_S5
170mA(Total)
75mA
230mA(Total)
68.10050.10Y
2nd = 68.10090.10B
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (POWER1)
Hummingbird1_HR
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Tuesday, April 17, 2012
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SSID = PCH

POWER

PCH1J — Cougar Point — 10 OF 10

Clock and Miscellaneous

AD49	VCCACLK		
T16	VCCDSW3_3	3D3V_S5	0.002A
V12	DCPSUSBYP		(0.1uFx1)
T38	VCC3_3	3D3V_S0	(10uFx1) (1uFx1)
BH23	VCCAPLLDMI2	C2402 SC1U10V2KX-1GP	
AL29	VCCIO	1D05V_VTT	(10uFx1)
AL24	DCPSUS		

USB

N26	VCCIO	1D05V_VTT	(1uFx1) C2423 SC1U6D3V2KX-GP
P26	VCCIO		
P28	VCCIO		
T27	VCCIO		
T29	VCCIO		
T23	VCCSUS3_3	3D3V_S5	0.097A (Totally current of VCCSUS3_3)
T24	VCCSUS3_3		(0.1uFx1) C2424 SCD1U10V2KX-5GP
V23	VCCSUS3_3		
V24	VCCSUS3_3	3D3V_S5	
P24	VCCSUS3_3		(0.1uFx1) C2425 SCD1U10V2KX-5GP
T26	VCCIO	1D05V_VTT	
M26	V5REF_SUS	+5VA_PCH_VCC5REFSUS	0.001A
AN23	DCPSUS		
AN24	VCCSUS3_3	3D3V_S5	

3D3V_S5 — D2401 CH751H-40PT-GP 83.R0304.A8F 2nd = 83.R2004.B8F — 5V_S5
R2408 10R2J-2-GP (0.1uFx1) C2426 SCD1U10V2KX-5GP

3D3V_S0 — D2402 CH751H-40PT-GP 83.R0304.A8F 2nd = 83.R2004.B8F — 5V_S0
R2407 10R2J-2-GP (1uFx1) C2427 SC1U10V2KX-1GP

AA19	VCCASW	1D05V_VTT	1.01A (Total current of VCCASW)
AA21	VCCASW		C2403 C2404 C2406 C2407 C2408
AA24	VCCASW		Change to 0603 package
AA26	VCCASW		DY
AA27	VCCASW		SC10U6D3V3MX-GP SC10U6D3V3MX-GP SC1U6D3V2KX-GP SC1U6D3V2KX-GP SC1U6D3V2KX-GP
AA29	VCCASW		(22uFx2_0603) (1uFx3)
AA31	VCCASW		
AC26	VCCASW		
AC27	VCCASW		
AC29	VCCASW		
AC31	VCCASW		
AD29	VCCASW		
AD31	VCCASW		
W21	VCCASW		
W23	VCCASW		
W24	VCCASW		
W26	VCCASW		
W29	VCCASW		
W31	VCCASW		
W33	VCCASW		

PCI/GPIO/LPC

P34	V5REF	+5VS_PCH_VCC5REF	0.001A
N20	VCCSUS3_3	3D3V_S5	(1uFx1) C2428 SC1U6D3V2KX-GP
N22	VCCSUS3_3		
P20	VCCSUS3_3		
P22	VCCSUS3_3		
AA16	VCC3_3	3D3V_S0	(0.1uFx2) C2430 SCD1U10V2KX-5GP C2431 SCD1U10V2KX-5GP
W16	VCC3_3		
T34	VCC3_3		
AJ2	VCC3_3	3D3V_S0	(0.1uFx1) C2429 SCD1U10V2KX-5GP
AF13	VCCIO		
AH13	VCCIO		
AH14	VCCIO	1D05V_VTT	(1uFx1) C2432 SC1U6D3V2KX-GP
AF14	VCCIO		
AK1	VCCAPLLSATA		
AF11	VCCVRM	1D05V_S0	
AC16	VCCIO		
AC17	VCCIO	1D05V_VTT	(1uFx1) C2435 SC1U6D3V2KX-GP
AD17	VCCIO		
T21	VCCASW	1D05V_VTT	
V21	VCCASW		
T19	VCCASW		
P32	VCCSUSHDA	+3VS_+1.5VS_HDA_IO	0.01A (0.1uFx1) C2433 SCD1U10V2KX-5GP

SATA

BD47	VCCADPLLA	+1.05VS_VCCA_A_DPL	
BF47	VCCADPLLB	+1.05VS_VCCA_B_DPL	
AF17	VCCIO	1D05V_VTT	C2412 SC1U6D3V2KX-GP (1uFx1)
AF33	VCCDIFFCLKN		
AF34	VCCDIFFCLKN		
AG34	VCCDIFFCLKN		
AG33	VCCSSC	1D05V_VTT	C2413 SC1U6D3V2KX-GP JE40 modify (1uFx1) 0.095A
V16	DCPSST	+VCCSST	(0.1uFx1) C2415 SCD1U10V2KX-5GP
T17	DCPSUS		
V19	DCPSUS		

CPU

BJ8	V_PROC_IO	1D05V_VTT	0.001A (0.1uFx2) (4.7uFx1_0603) C2417 C2418 DY C2419
A22	VCCRTC	RTC_AUX_S5	6uA (0.1uFx2) (1uFx1) C2420 DY SC1U6D3V2KX-GP

COUGAR-GP-U2-NF

AFR suggest DY Cayp to prevent leakage current

MISC

N16	DCPRTC	+VCCRTCEXT	C2411 SCD1U10V2KX-5GP (0.1uFx1)
Y49	VCCVRM	1D5V_S0	0.16A (Totally current of VCCVRM)

RTC

HDA

L2402 IND-10UH-218-GP — +1.05VS_VCCA_A_DPL — 68.10050.10Y / 2nd = 68.10090.10B — (1uFx1) (220uFx1) C2409 SC1U6D3V2KX-GP

L2403 IND-10UH-218-GP — +1.05VS_VCCA_B_DPL — 68.10050.10Y / 2nd = 68.10090.10B — (1uFx1) (220uFx1) C2410 SC1U6D3V2KX-GP

1D5V_S0 — C2421 SCD1U16V2KX-3GP — C2422 SCD1U16V2KX-3GP

Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
V5REF_SUS	VCCSUS3_3	a) VCC5REF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCC5REF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) V5REF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
V5REF	VCC3_3	a) V5REF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCC5REF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms	a) V5REF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)

+3VS_+1.5VS_HDA_IO — R2409 0R3J-0-U-GP — 3D3V_S5
R2415 DY 0R3J-0-U-GP — 1D5V_S0

<Variant Name>

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Title: PCH (POWER2)

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

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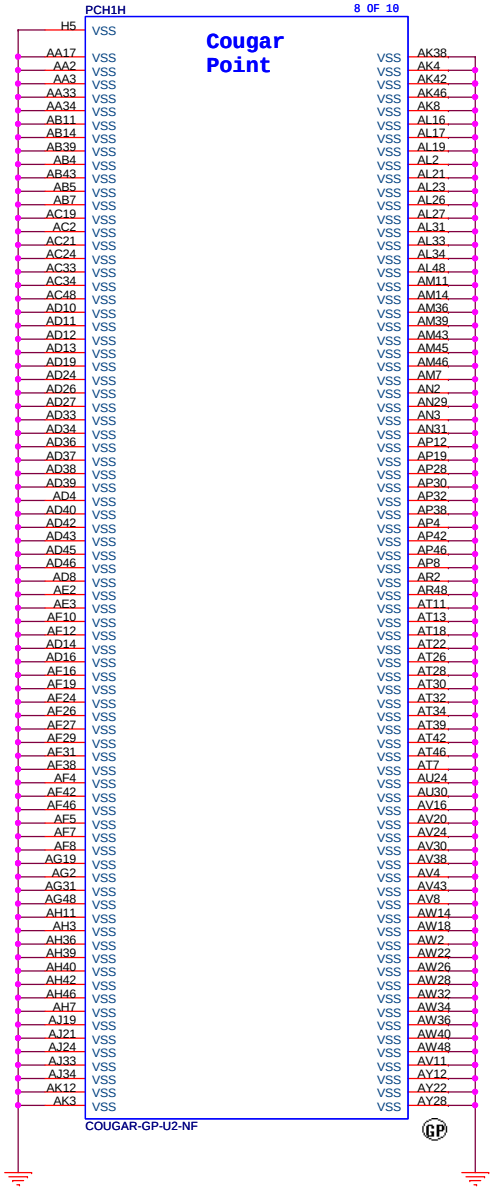
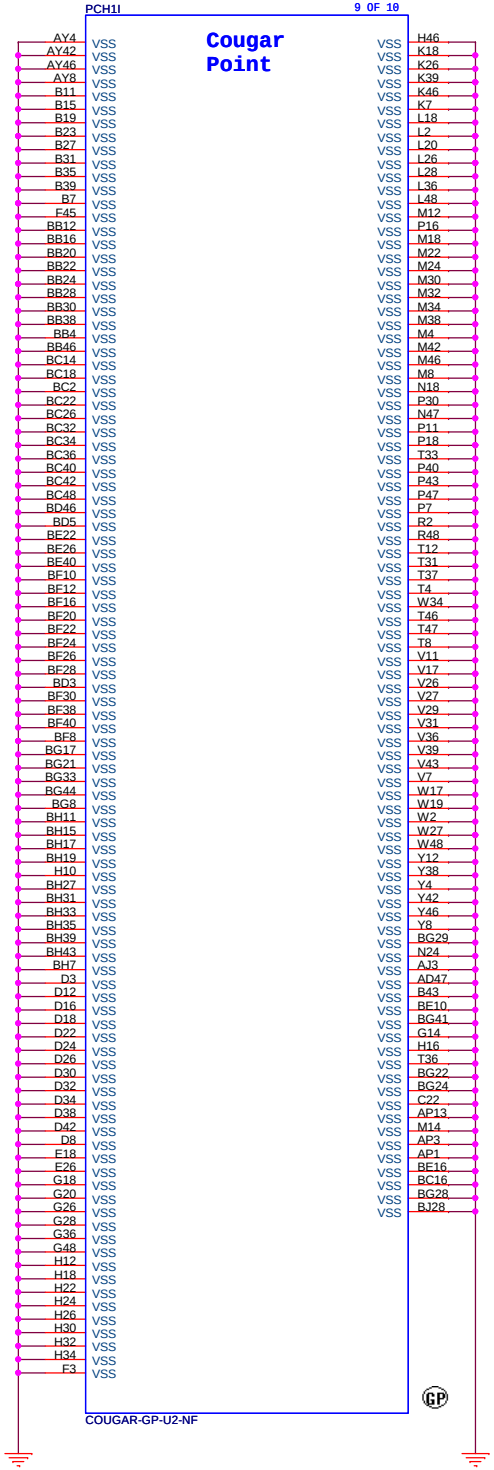
SSID = PCH





<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 25 of 102

Blanking

<Variant Name>

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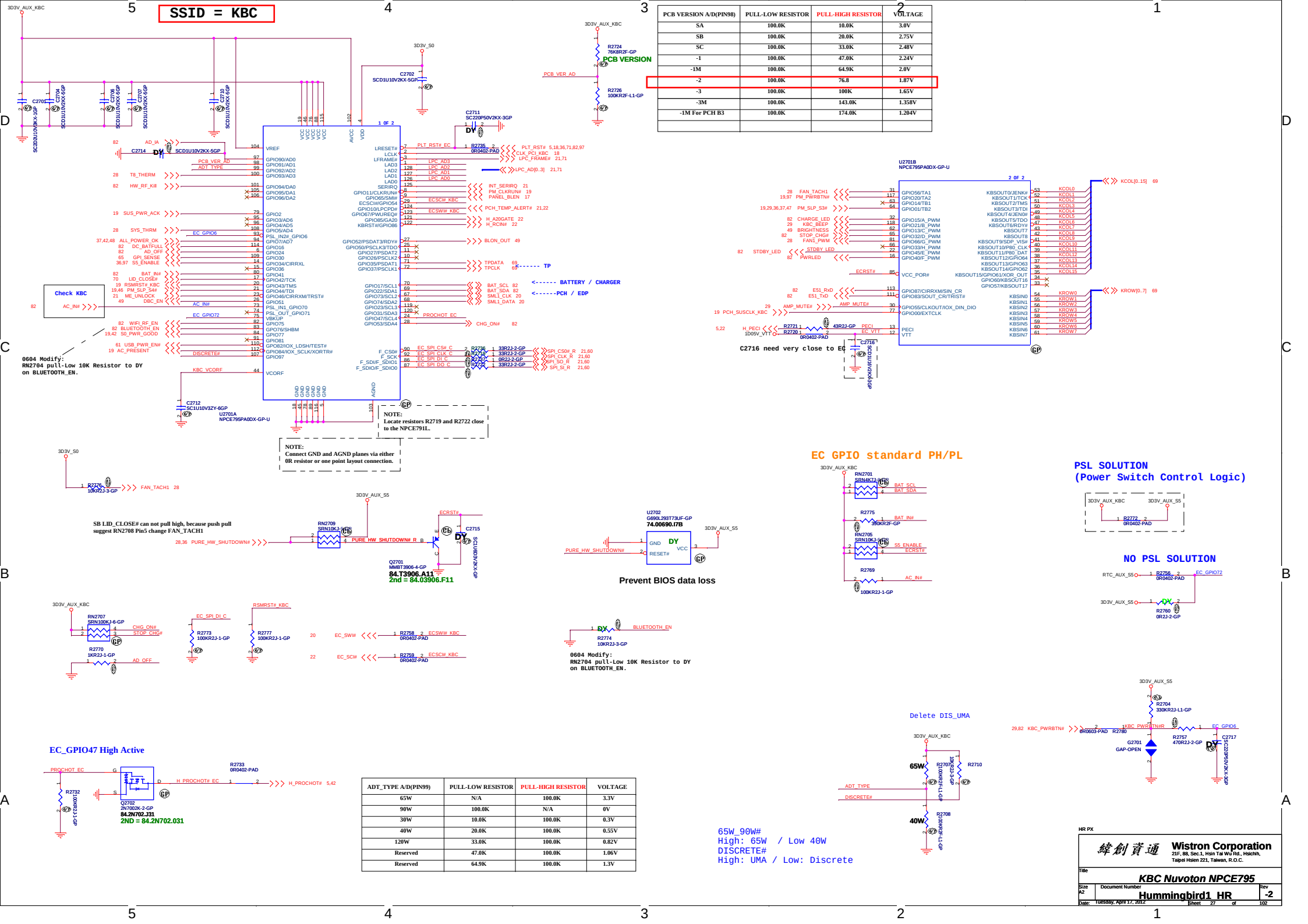
Title: ***Clock(colay)***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 26 of 102

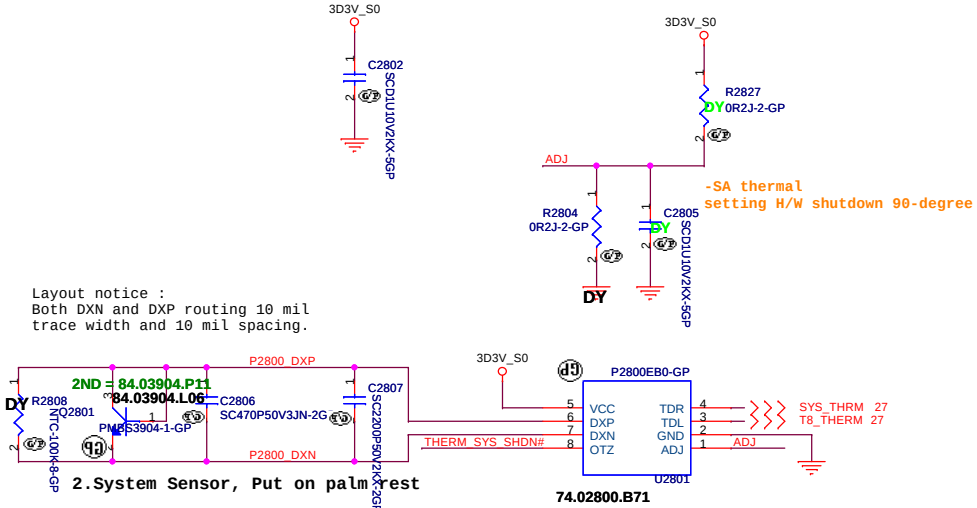


PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
-1M	100.0K	64.9K	2.0V
-2	100.0K	76.8	1.87V
-3	100.0K	100K	1.65V
-3M	100.0K	143.0K	1.358V
-1M For PCH B3	100.0K	174.0K	1.204V

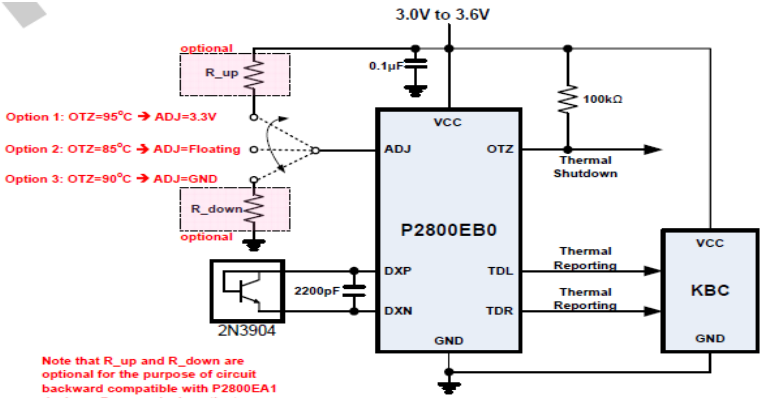
ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

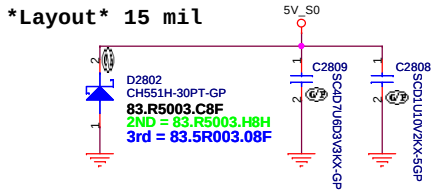
SSID = Thermal

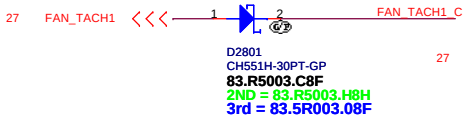
Thermal sensor P2800

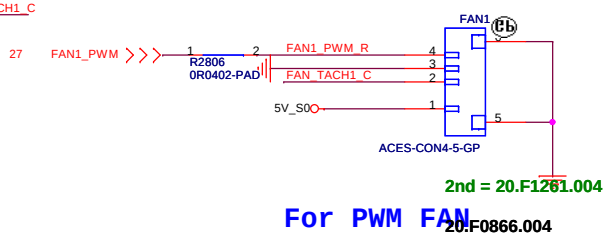


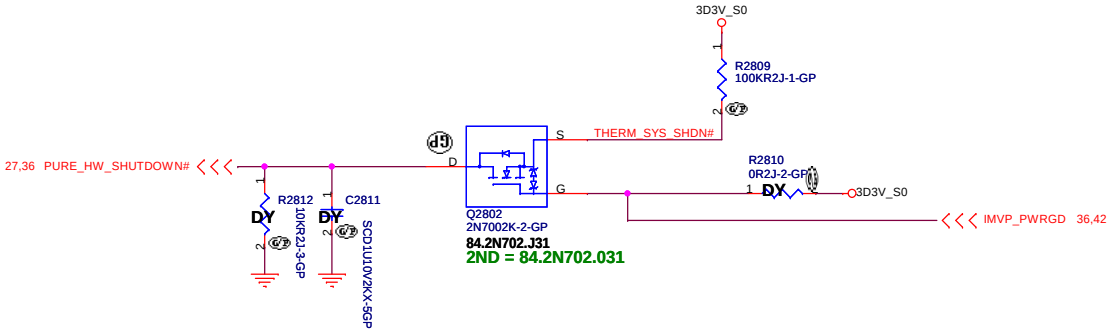
[Rev B]











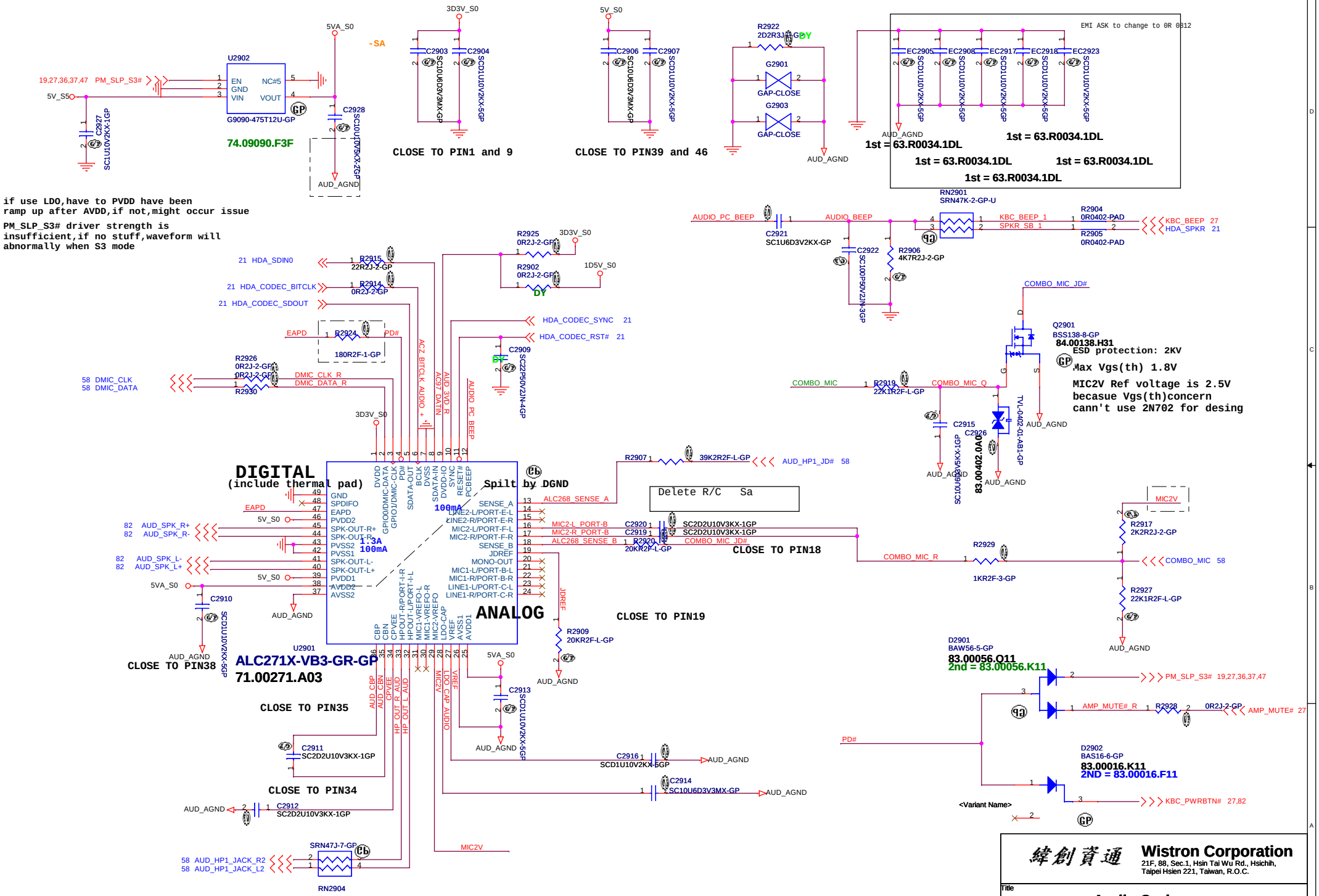
HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal P2800/Fan Controllor P2793***

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 28 of 102


5VA_S0
-SA
U2902
19,27,36,37,47 PM_SLP_S3#
5V_S5
EN
GND
VIN
NC#5
VOUT
G9090-475T12U-GP
74.09090.F3F
C2927
SC1U10V2KX-1GP
C2928
SC10U10V5KX-2GP
AUD_AGND
3D3V_S0
C2903
C2904
SC10U6D3V3MX-GP
SCD1U10V2KX-5GP
CLOSE TO PIN1 and 9
5V_S0
C2906
C2907
CLOSE TO PIN39 and 46
R2922
2D2R3J-GP
DY
G2901
GAP-CLOSE
G2903
EMI ASK to change to 0R 0812
EC2905
EC2908
EC2917
EC2918
EC2923
1st = 63.R0034.1DL
if use LDO,have to PVDD have been
ramp up after AVDD,if not,might occur issue
PM_SLP_S3# driver strength is
insufficient,if no stuff,waveform will
abnormally when S3 mode
RN2901
SRN47K-2-GP-U
AUDIO_PC_BEEP
AUDIO_BEEP
C2921
SC1U6D3V2KX-GP
C2922
SC100P50V2JN-3GP
R2906
4K7R2J-2-GP
KBC_BEEP_1
SPKR_SB_1
R2904
0R0402-PAD
R2905
0R0402-PAD
KBC_BEEP 27
HDA_SPKR 21
21 HDA_SDIN0
21 HDA_CODEC_BITCLK
21 HDA_CODEC_SDOUT
R2915
22R2J-GP
R2914
0R2J-2-GP
R2925
0R2J-2-GP
R2902
0R2J-2-GP
1D5V_S0
HDA_CODEC_SYNC 21
HDA_CODEC_RST# 21
EAPD
R2924
180R2F-1-GP
PD#
C2909
SC22P50V2JN-4GP
R2926
0R2J-2-GP
R2930
0R2J-2-GP
58 DMIC_CLK
58 DMIC_DATA
DMIC_CLK_R
DMIC_DATA_R
AC97_BITCLK_AUDIO
AUDIO_VDAC_R
AUDIO_PC_BEEP
COMBO_MIC_JD#
Q2901
BSS138-8-GP
84.00138.H31
ESD protection: 2KV
Max Vgs(th) 1.8V
MIC2V Ref voltage is 2.5V
becasue Vgs(th)concern
cann't use 2N702 for desing
COMBO_MIC
R2919
22K1R2F-L-GP
COMBO_MIC_Q
TVL-0402-01-AB1-GP
C2915
C2926
SC100P50V5KX-1GP
83.00402.0A0
AUD_AGND
DIGITAL
(include thermal pad)
Spilt by DGND
100mA
1.3A
100mA
R2907
39K2R2F-L-GP
AUD_HP1_JD# 58
Delete R/C Sa
ALC268_SENSE_A
MIC2-L_PORT-B
MIC2-R_PORT-B
ALC268_SENSE_B
C2920
C2919
C2921
SC2D2U10V3KX-1GP
20KR2F-L-GP
COMBO_MIC_JD#
CLOSE TO PIN18
COMBO_MIC_R
R2929
1KR2F-3-GP
MIC2V
R2917
2K2R2J-2-GP
COMBO_MIC 58
R2927
22K1R2F-L-GP
GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
SDATA-OUT
BCLK
SDATA-IN
SYNC
RESET#
PCBEEP
SENSE_A
LINE2-L/PORT-E-L
LINE2-R/PORT-E-R
MIC2-L/PORT-F-L
MIC2-R/PORT-F-R
SENSE_B
JDREF
MONO-OUT
MIC1-L/PORT-B-L
MIC1-R/PORT-B-R
LINE1-L/PORT-C-L
LINE1-R/PORT-C-R
ANALOG
CLOSE TO PIN19
R2909
20KR2F-L-GP
82 AUD_SPK_R+
82 AUD_SPK_R-
82 AUD_SPK_L-
82 AUD_SPK_L+
SPK-OUT-R+
SPK-OUT-R-
SPK-OUT-L-
SPK-OUT-L+
PVSS2
PVSS1
PVDD1
AVDD2
AVSS2
C2910
SCD1U10V2KX-5GP
CLOSE TO PIN38
U2901
ALC271X-VB3-GR-GP
71.00271.A03
CLOSE TO PIN35
CLOSE TO PIN34
C2911
SC2D2U10V3KX-1GP
C2912
SC2D2U10V3KX-1GP
C2913
C2916
SCD1U10V2KX-5GP
C2914
SC10U6D3V3MX-GP
SRN47J-7-GP
58 AUD_HP1_JACK_R2
58 AUD_HP1_JACK_L2
RN2904
D2901
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
PM_SLP_S3# 19,27,36,37,47
AMP_MUTE# R
R2928
0R2J-2-GP
AMP_MUTE# 27
D2902
BAS16-6-GP
83.00016.K11
2ND = 83.00016.F11
KBC_PWRBTN# 27,82
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec
Size A3
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Rev -2
Date: Tuesday, April 17, 2012
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AUDIO OP AMPLIFIER

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Audio AMP*

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 30 of 102

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AR8158***		
Size: A3	Document Number: **Hummingbird1_HR**	Rev: **-2**
Date: Tuesday, April 17, 2012	Sheet 31 of 102	

Card reader move to small board

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5159 (CARD READER)***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 32 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 33 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

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Blanking

HR PX

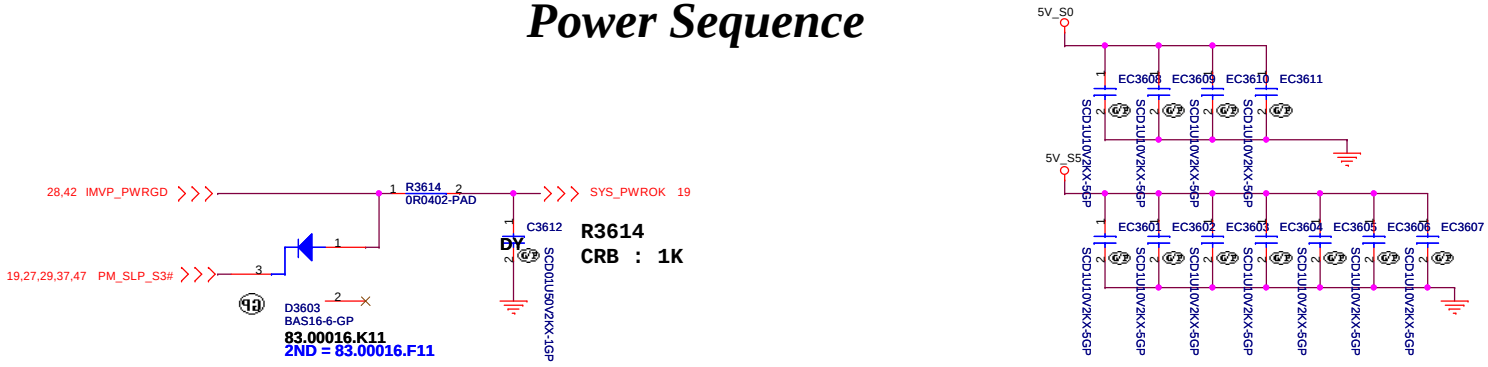
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB 3.0 Controller*

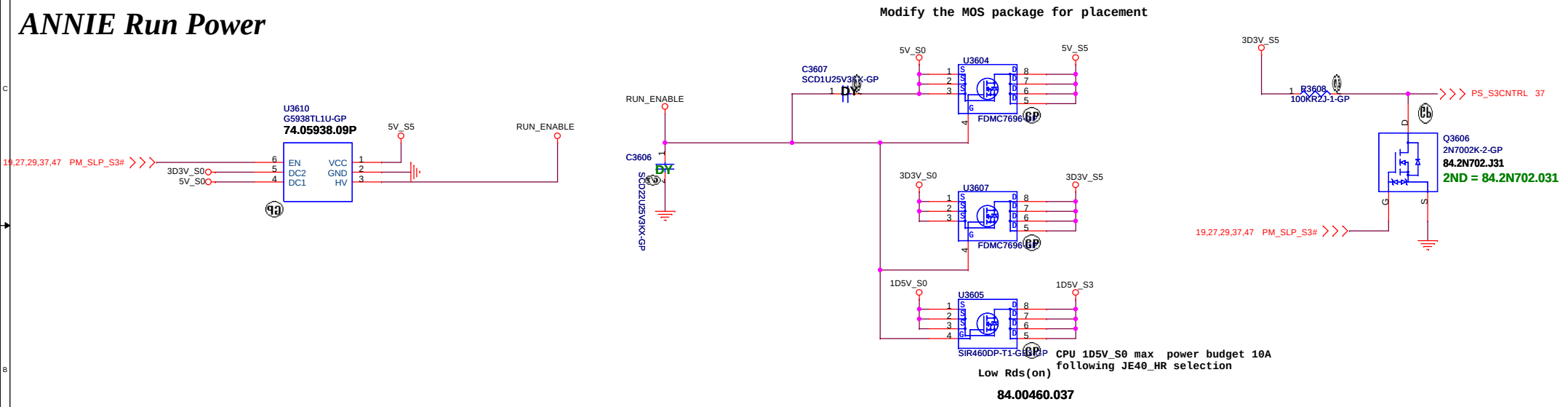
Size	Document Number	Rev
A3	Hummingbird1_HR	-2

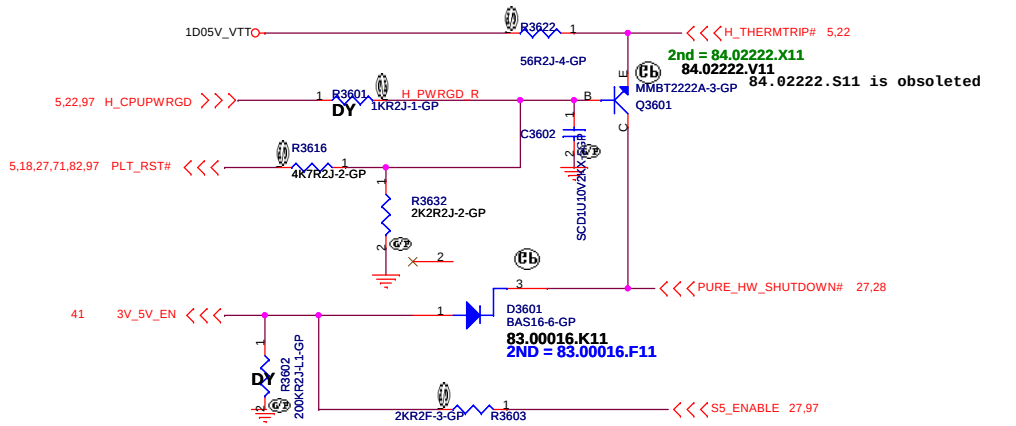
Date: Tuesday, April 17, 2012 Sheet 35 of 102

Power Sequence



ANNIE Run Power





HR PX

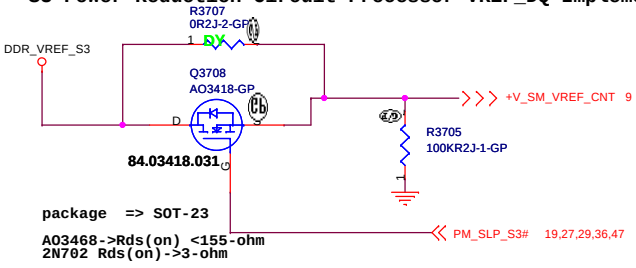
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

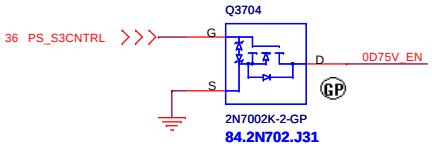
Date: Tuesday, April 17, 2012 Sheet 36 of 102

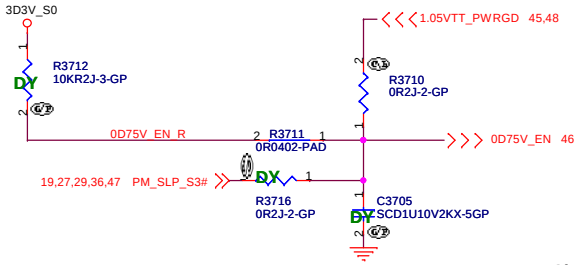
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



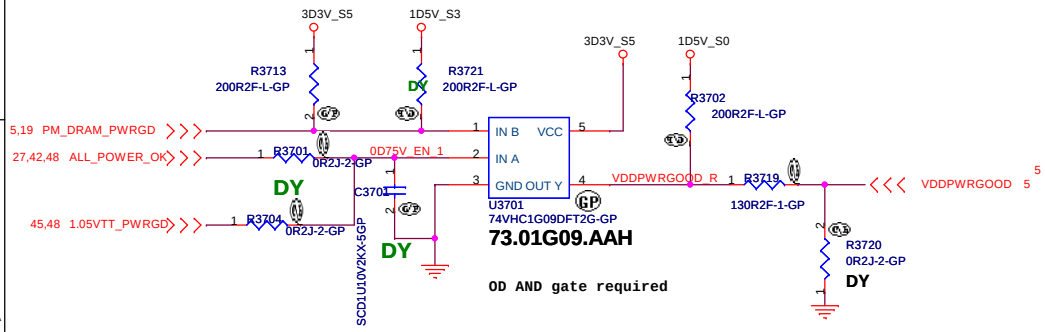
package => SOT-23

AO3468->Rds(on) <155-ohm
2N702 Rds(on)->3-ohm





Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

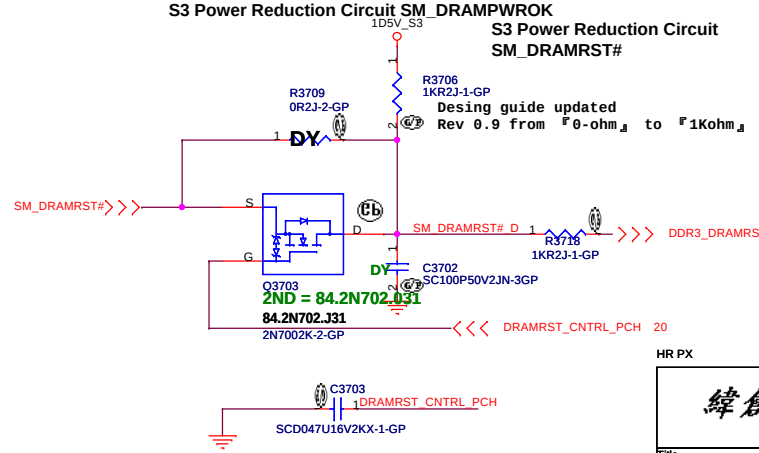


OD AND gate required

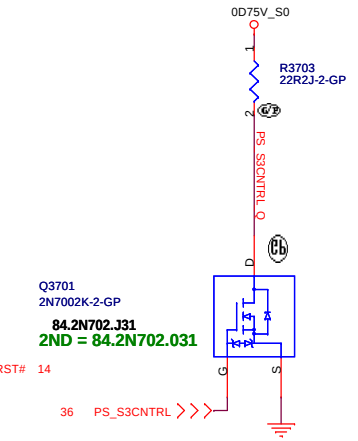
For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

S3 Power Reduction Circuit SM_DRAMRST#



Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADAPTER**

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 37 of 102

Move to small board

HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DCIN JACK***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 38 of 102

Move to small board

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BATT CONN***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 39 of 102

Move to small board

<Variant Name>

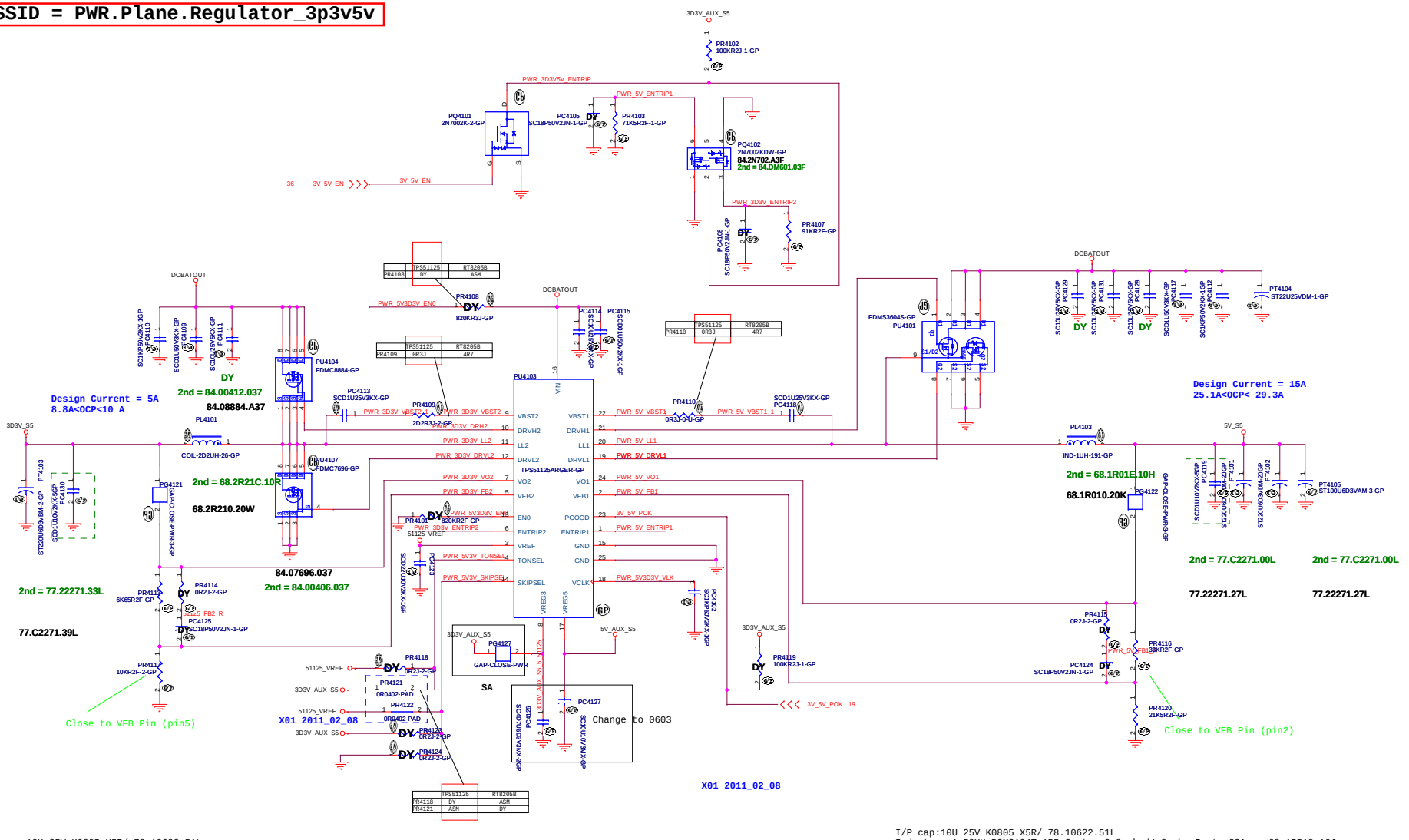
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CHARGER BQ24745*

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 40 of 102

SSID = PWR.Plane.Regulator_3p3v5v

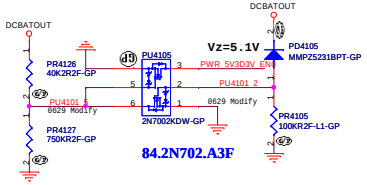


I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =10Arms 68.2R210.20B
O/P cap: ST220U6D3VDM-20GP 25mOhm / 77.22271.27L
H/S: FDMC8884-GP / 22mOhm/30mOhm@4.5Vgs / 84.08884.A37
L/S: FDMC7692-GP / 9.5mOhm/11.5mOhm@4.5Vgs / 84.07692.A37

I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.50UH PCMC104T-1R5 Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: ST220U6D3VDM-20GP 25mOhm / 77.22271.27L
H/S: SIR172DP-T1-GE3-GP / 10.3mOhm/12.4mOhm@4.5Vgs / 84.00172.037
L/S: SIR460DP-T1-GE3-GP / 4.9mOhm/6.1mOhm@4.5Vgs / 84.00460.037

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit



TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

<Variant Name>

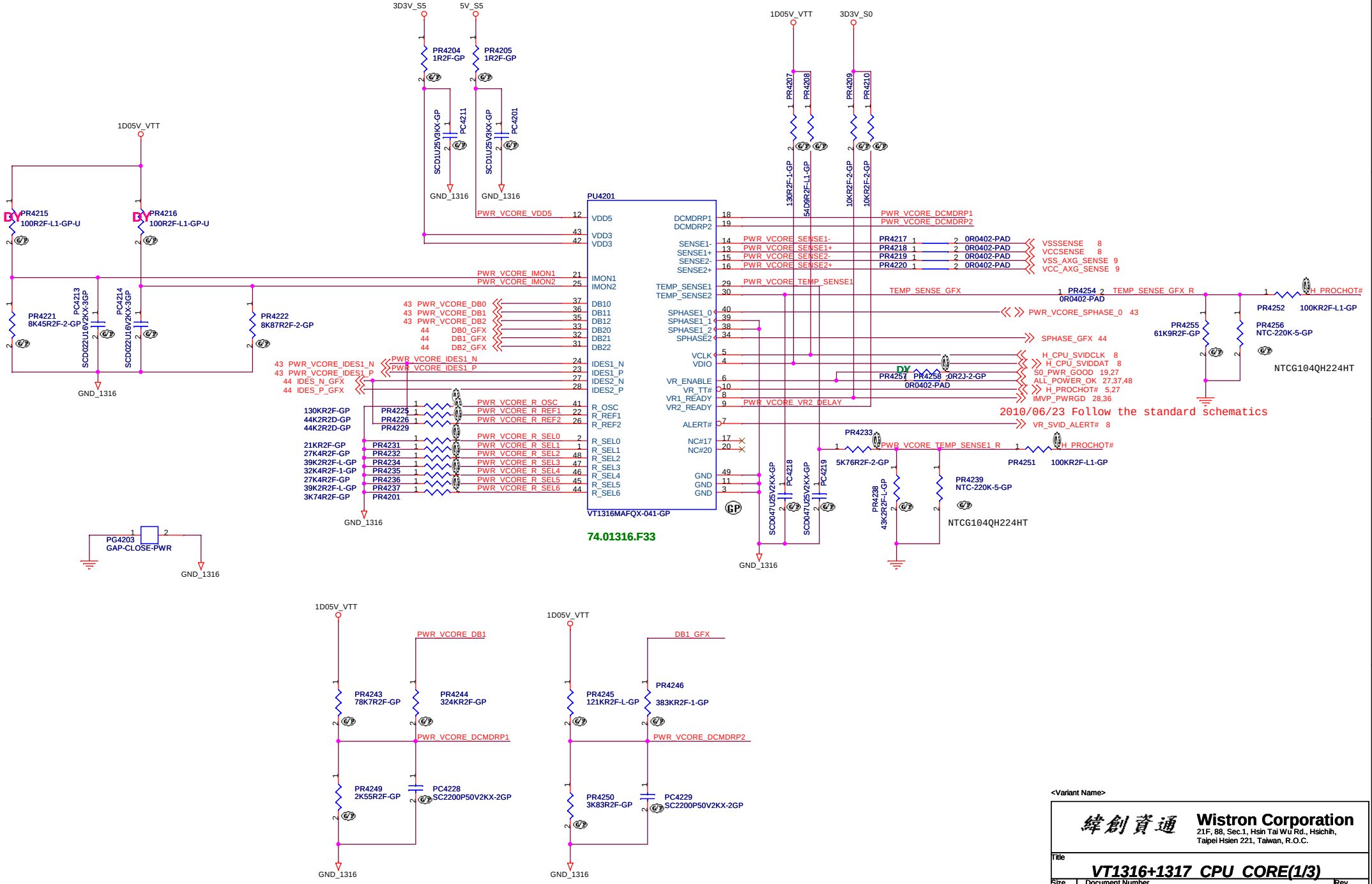
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51125A_5V/3D3V

Size: Custom | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 41 of 102

SSID = CPU.Regulator



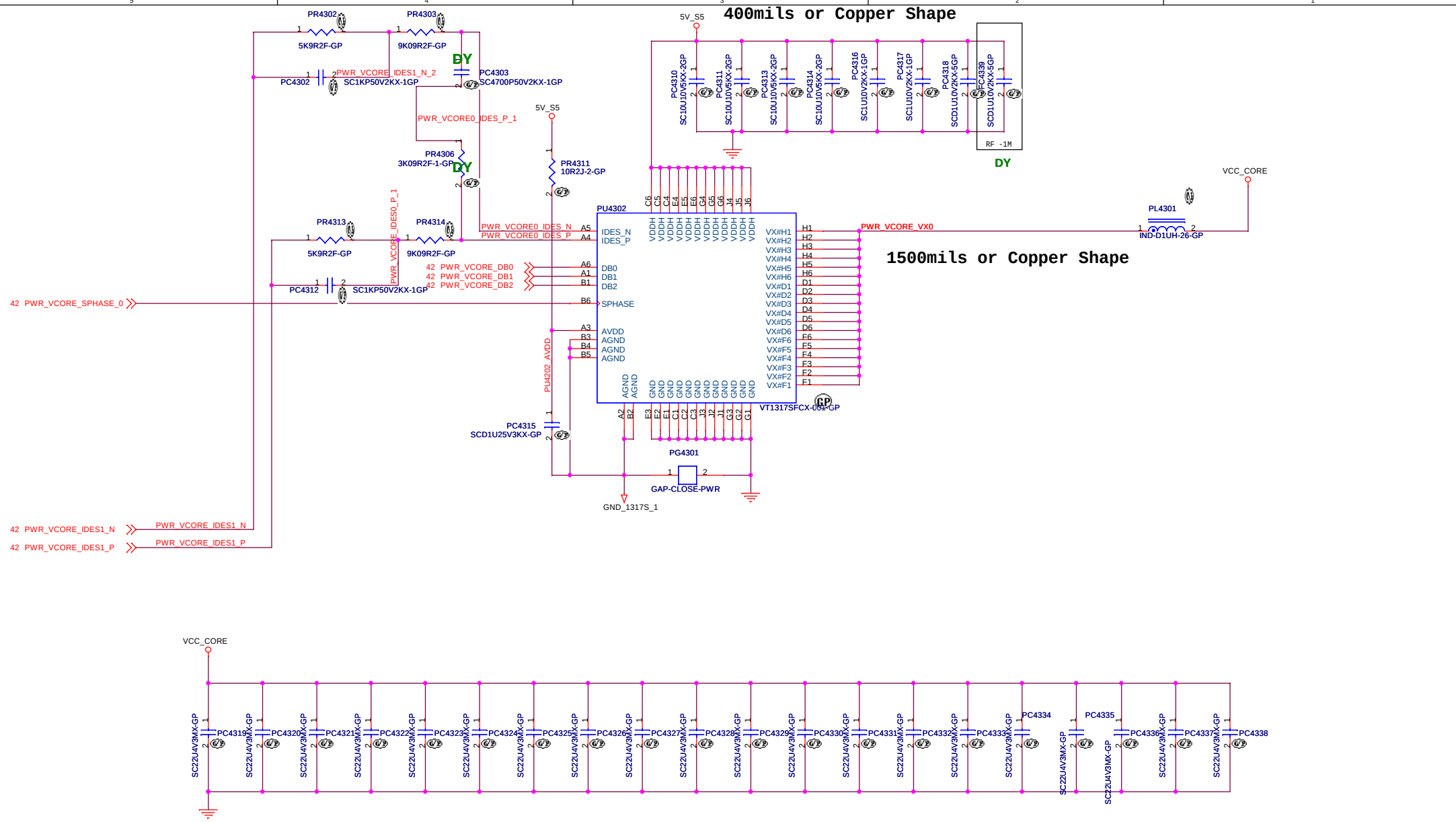
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: VT1316+1317 CPU CORE(1/3)

Size: A3 | Document Number: Hummingbird1 HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 42 of 102



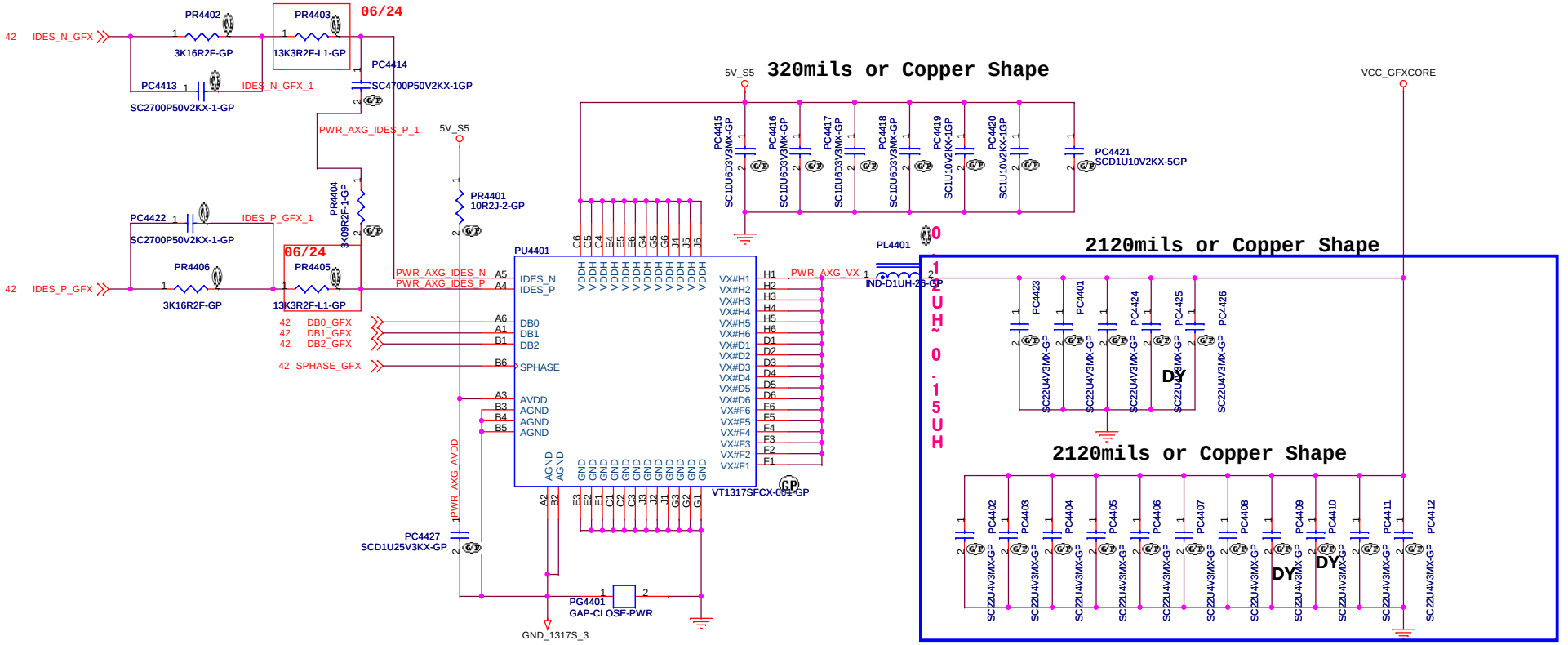
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VT1316+1317 CPU CORE(2/3)*

Size	Document Number	Rev
A3	Hummingbird1 HR	-2

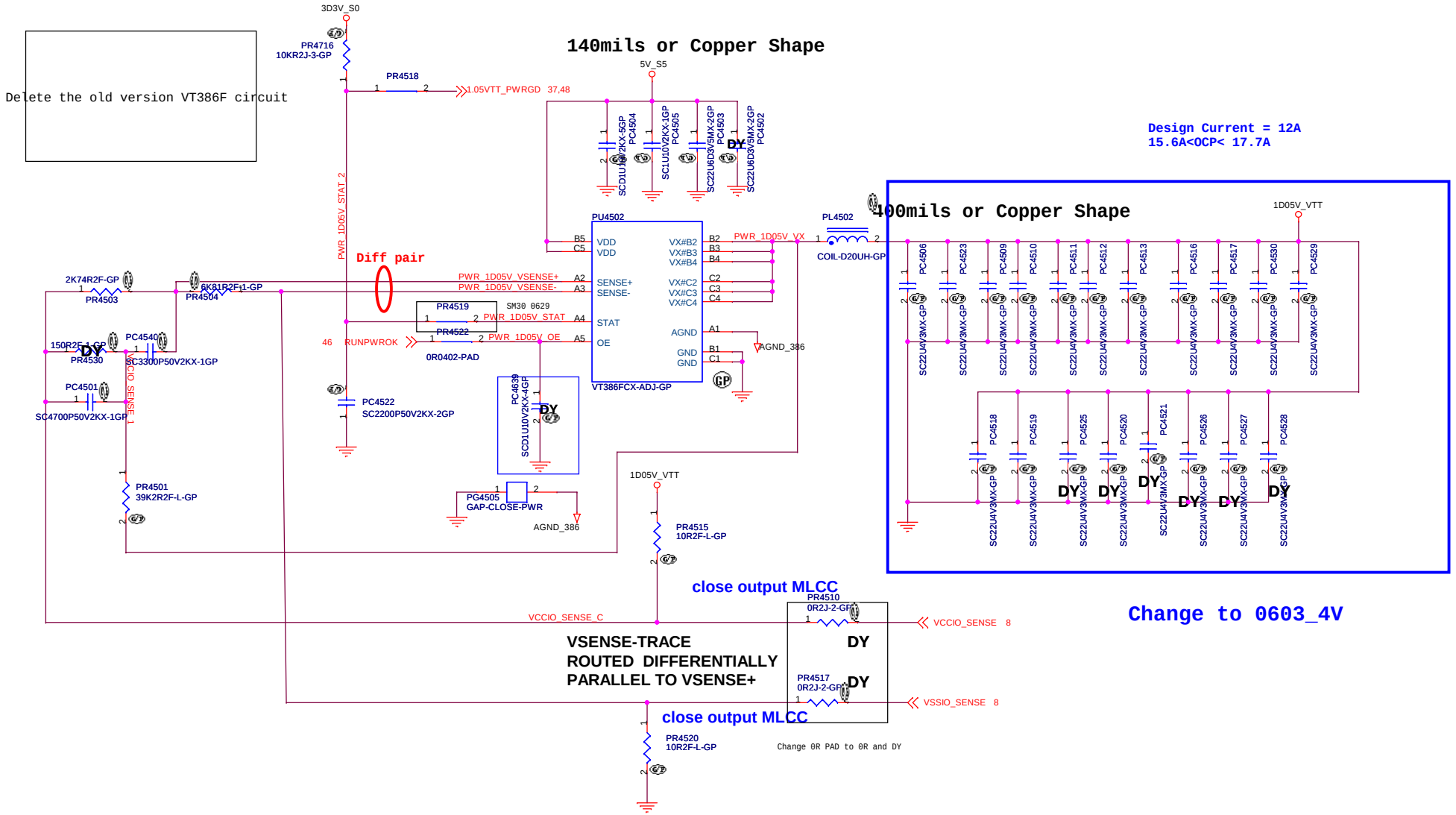
Date: Tuesday, April 17, 2012 Sheet 43 of 102



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

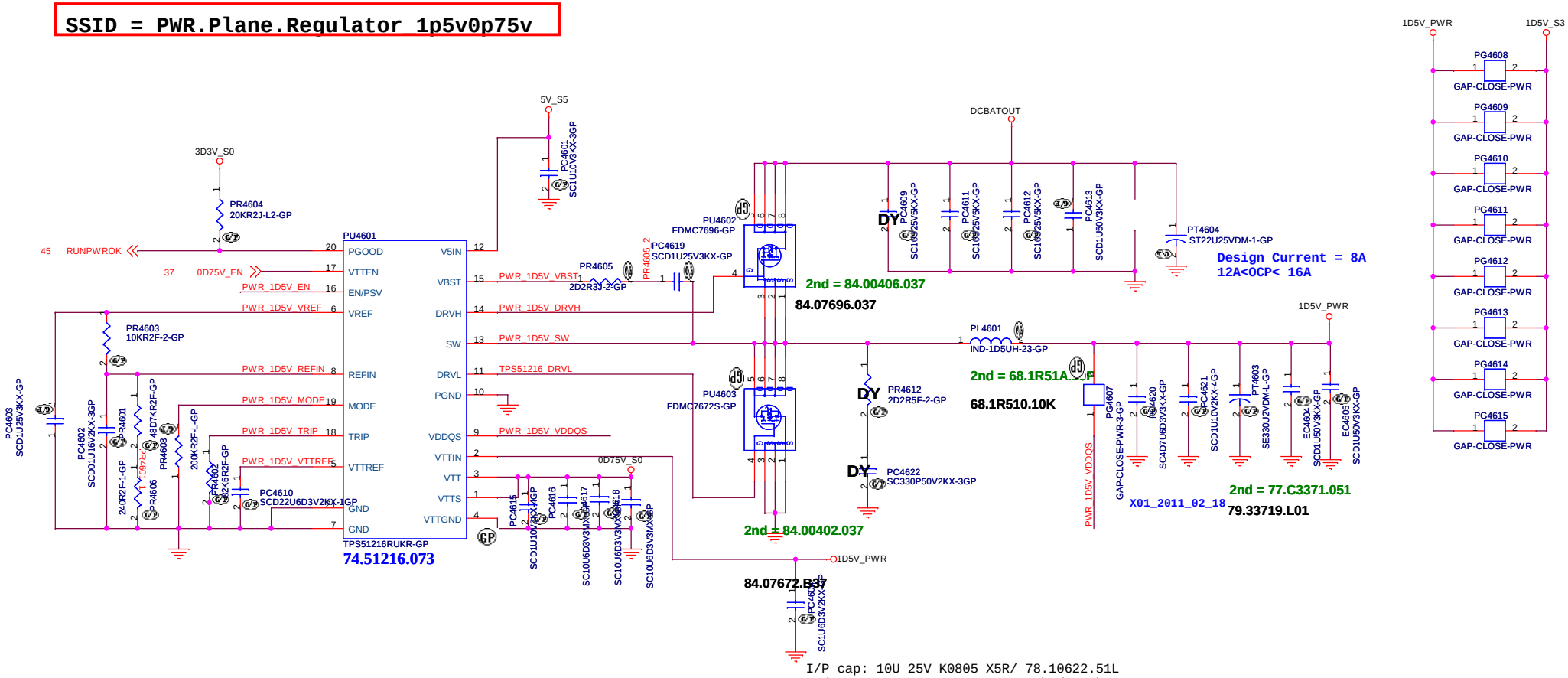
Title	VT1316+1317 CPU CORE(3/3)	
Size A3	Document Number Hummingbird1 HR	Rev -2
Date: Tuesday, April 17, 2012	Sheet 44 of 102	



<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VT386 +1.05V VTT		
Size: A3	Document Number: Hummingbird1 HR	Rev: -2
Date: Tuesday, April 17, 2012	Sheet 45 of 102	

SSID = PWR.Plane.Regulator 1p5v0p75v



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: IND-1D5UH-23-GP 14mohm/15mohm Isat =18Arms 68.1R510.10K
O/P cap: SE330U2VDM-L-GP 9mOhm / 79.33719.L01
H/S: SIS412DN-T1-GE3-GP / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S: SI7716ADN-T1-GE3-GP / 13.5mOhm/16.5mOhm@4.5Vgs / 84.07716.037

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR5003	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

DDR_VREF_S3
PWR_1D5V_VTTREF
PR4611 0R0603-PAD

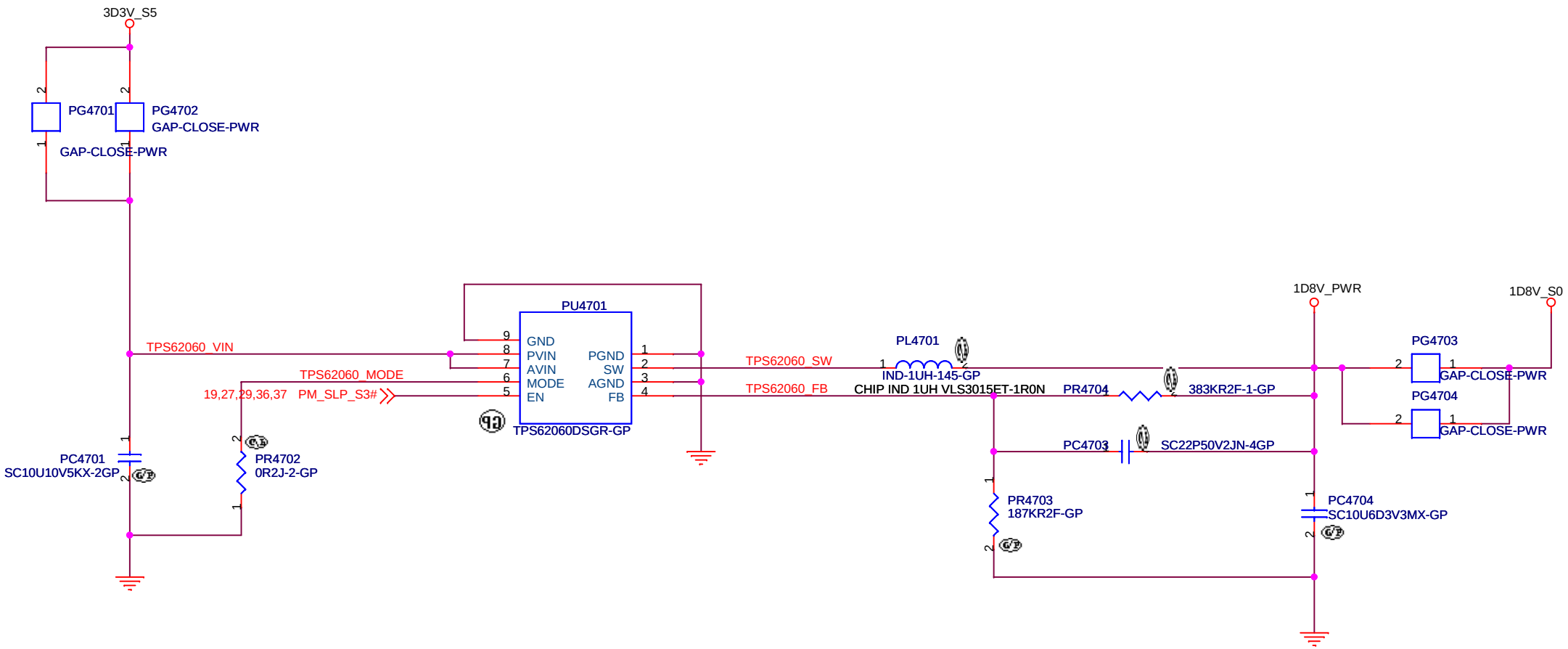
19,27 PM_SLP_S4#
PR4607 0R0402-PAD
PWR_1D5V_EN

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 +1.5V SUS
Size: A3
Document Number: Hummingbird1 HR
Rev: -2
Date: Tuesday, April 17, 2012
Sheet 46 of 102

SSID = PWR.Plane.Regulator_1p8v

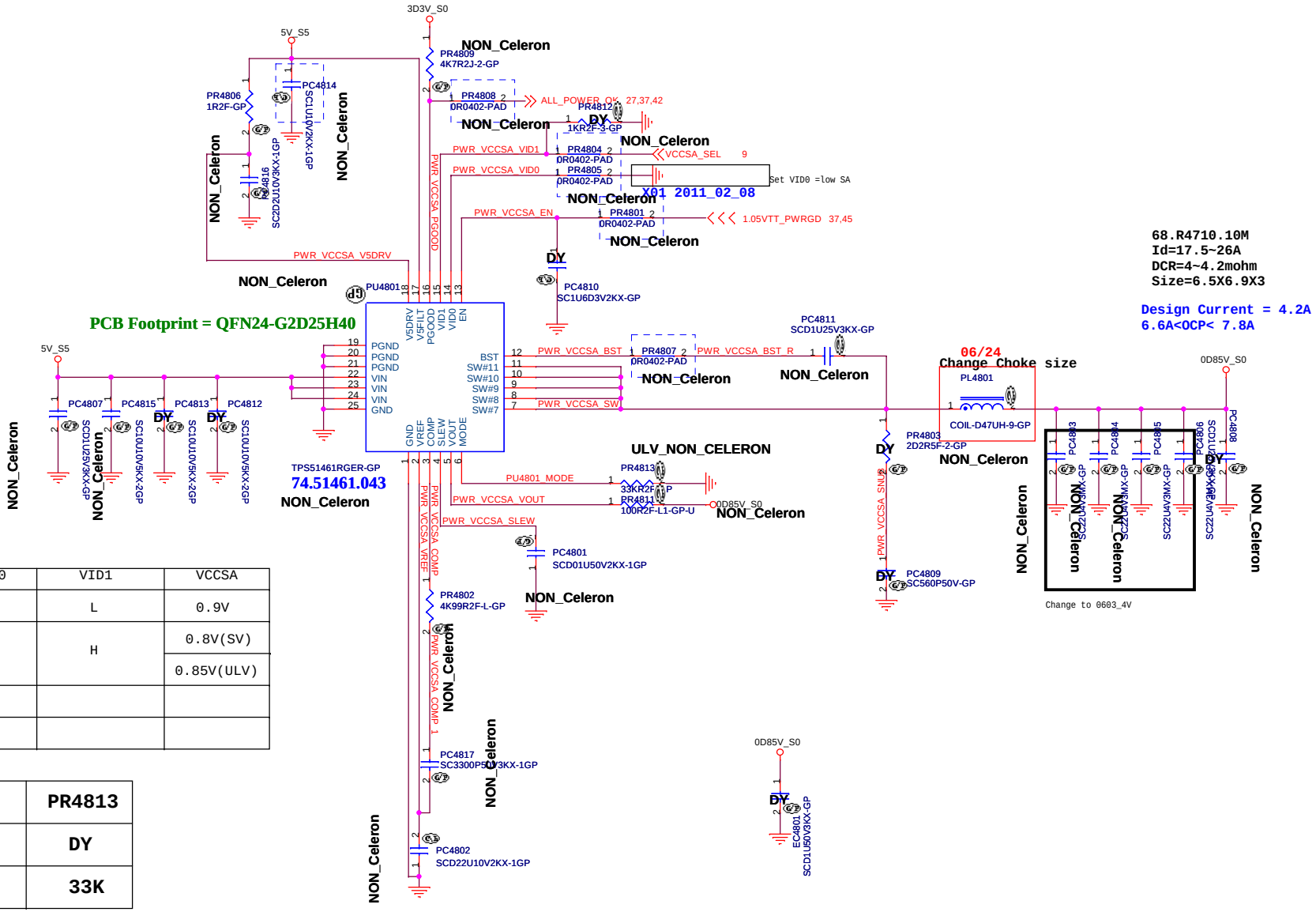


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC CONVERTER_1D8V	
Size A4	Document Number Hummingbird1_HR	Rev -2
Date: Tuesday, April 17, 2012	Sheet 47 of 102	

TPS51461 for VCCSA



68.R4710.10M
Id=17.5~26A
DCR=4~4.2mohm
Size=6.5X6.9X3

Design Current = 4.2A
6.6A<OCP< 7.8A

VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V(SV)
		0.85V(ULV)

TYPE	PR4813
SV	DY
ULV	33K

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51461_VCCSA

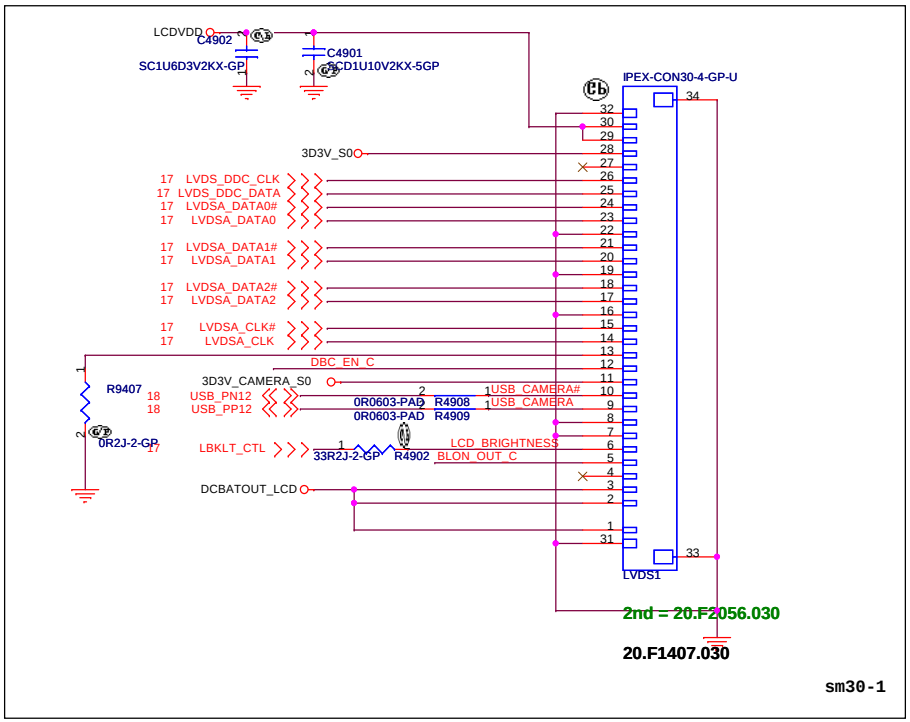
Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 48 of 102

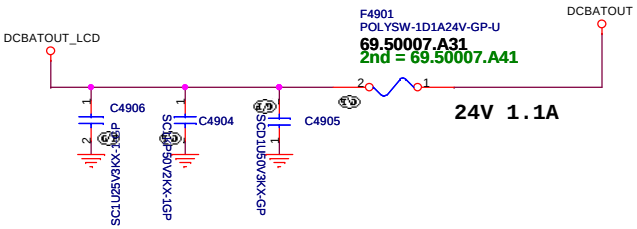
SSID = VIDEO

Reverse the pin define becasue of cable issue

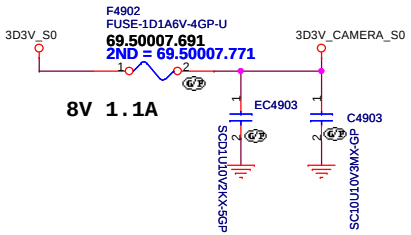
LVDS CONNECTOR



INVERTER POWER

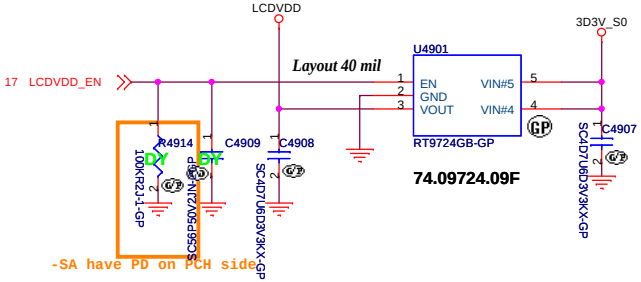


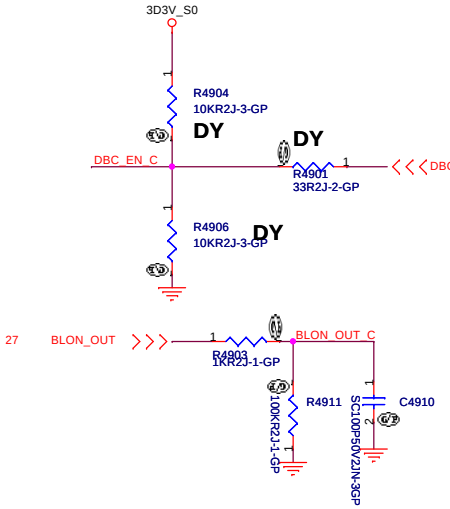
Camera Power



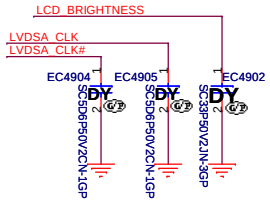
SSID = VIDEO

LCD POWER for ANNIE

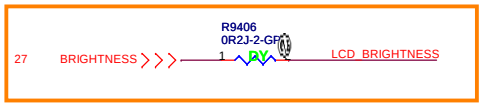




For EMI request
Close to LVDS connector



-SA



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 49 of 102

Pull High 5V Design on CRT Board

CRT DDCDATA & DDCCLK level shift

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 50 of 102

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

17 HDMI_CLK_R#
17 HDMI_CLK_R
17 HDMI_DATA0_R#
17 HDMI_DATA0_R
17 HDMI_DATA1_R#
17 HDMI_DATA1_R
17 HDMI_DATA2_R#
17 HDMI_DATA2_R

Close to HDMI Connector

HDMI_CLK_R#
HDMI_CLK_R
HDMI_DATA0_R#
HDMI_DATA0_R
HDMI_DATA1_R#
HDMI_DATA1_R
HDMI_DATA2_R#
HDMI_DATA2_R

RN5114
SRN499F-GP
RN5115
SRN499F-GP

Intel desging suggestion Stuff 680-ohm,
CRB board stuff 618-ohm
TM said that following JE40_HR stuff 499-ohm

HDMI_PLL_GND

Q5105
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

5V_S0

Close to Level Shift

3D3V_S0

17 PCH_HDMI_CLK
17 PCH_HDMI_DATA

Q5104
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

5V_S0

RN5101
SRN2K2J-1-GP

DDC_CLK_HDMI
DDC_DATA_HDMI

HDMI1
SKT-HDMI25-GP-GP

HDMI_DATA2_R
HDMI_DATA2_R#
HDMI_DATA1_R
HDMI_DATA1_R#
HDMI_DATA0_R
HDMI_DATA0_R#
HDMI_CLK_R
HDMI_CLK_R#
DDC_CLK_HDMI
DDC_DATA_HDMI

2nd = 22.10296.311
3rd = 22.10296.501
22.10296.271

5V_S0
F5101
FUSE-1D1A6V-4GP-U
69.50007.691
8V 1.1A
2nd = 69.50007.771

FC5101
SCD1U10V2KX-5GP
DY

HPD_HDMI_CON

84.03904.L06
2ND = 84.03904.P11
Q5102
PMBS3904-1-GP
HDMI_HPD_B
R5111
150KR2J-L1-GP
R5110
200KR2J-L1-GP
DY

3D3V_S0

HDMI_DET
R5113
10KR2J-2-GP
HDMI_PCH_DET 17
R5112
10KR2J-3-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector
Size: A3
Document Number: Hummingbird1_HR
Rev: -2
Date: Tuesday, April 17, 2012
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LED BACKLIGHT CONVERTER POWER

HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***eDP***

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 52 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *S-VIDEO*

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 53 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

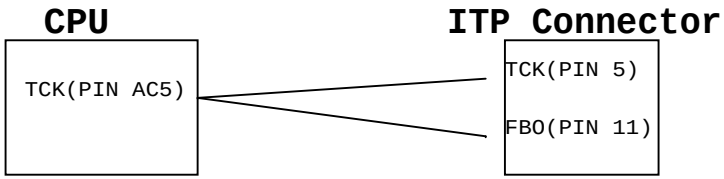
Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

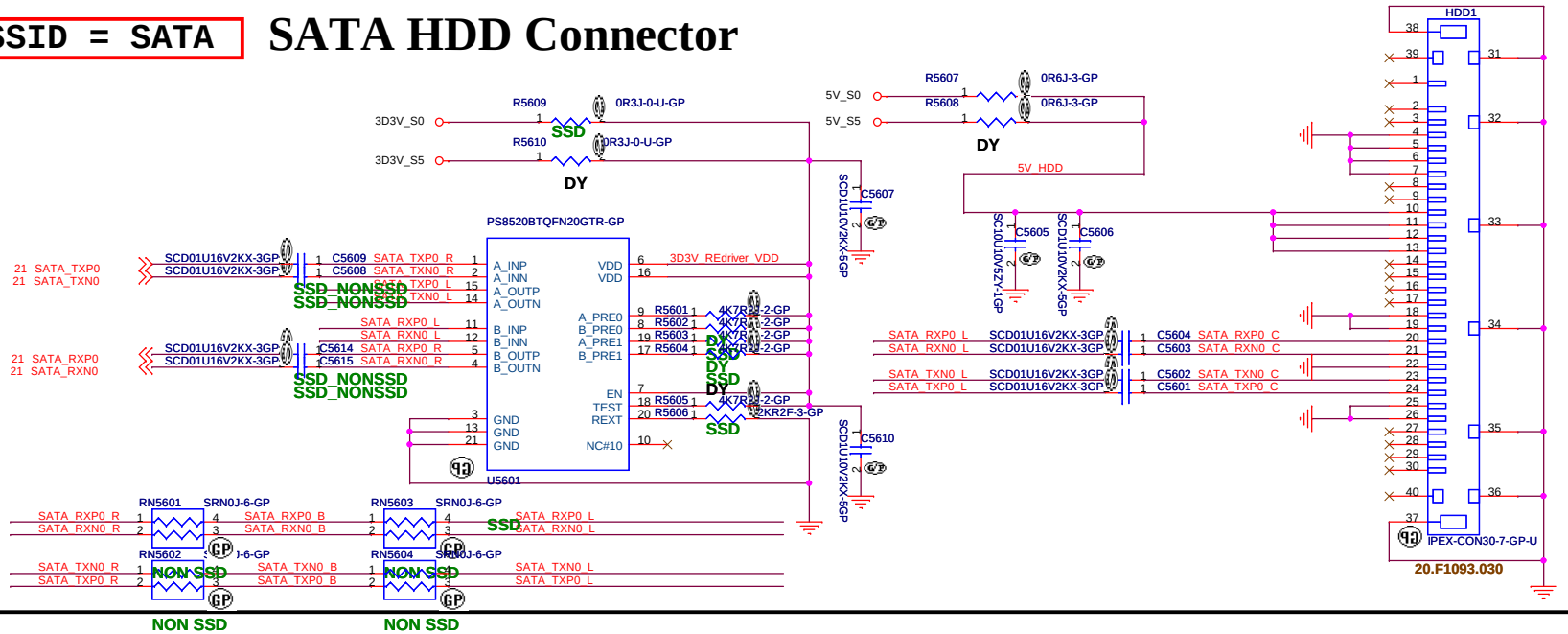
Title: ITP

Size: A4 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 55 of 102

SSID = SATA

SATA HDD Connector



ODD Connector

Without ODD

ESATA Power

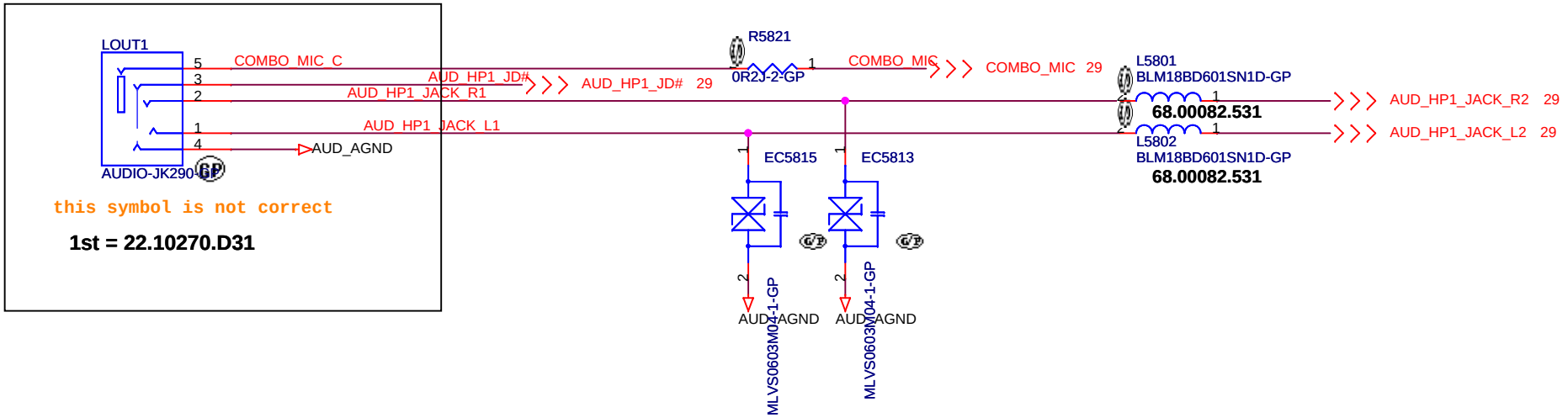
USB CHARGER

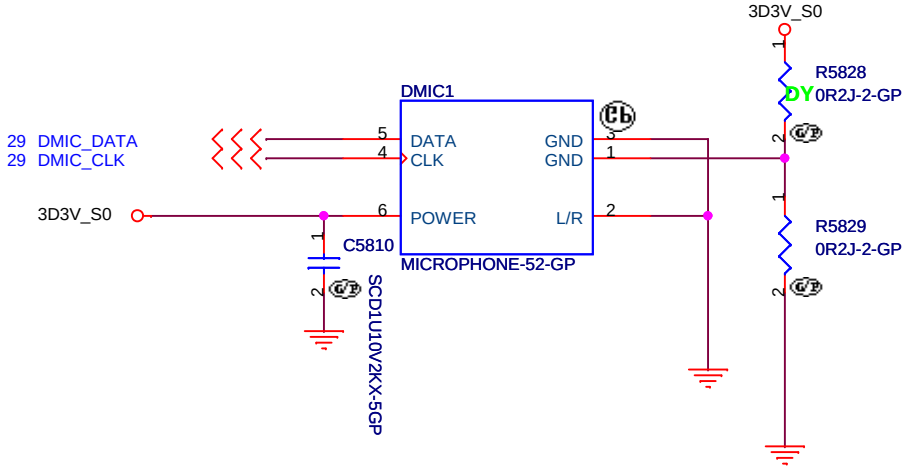
<Variant Name>

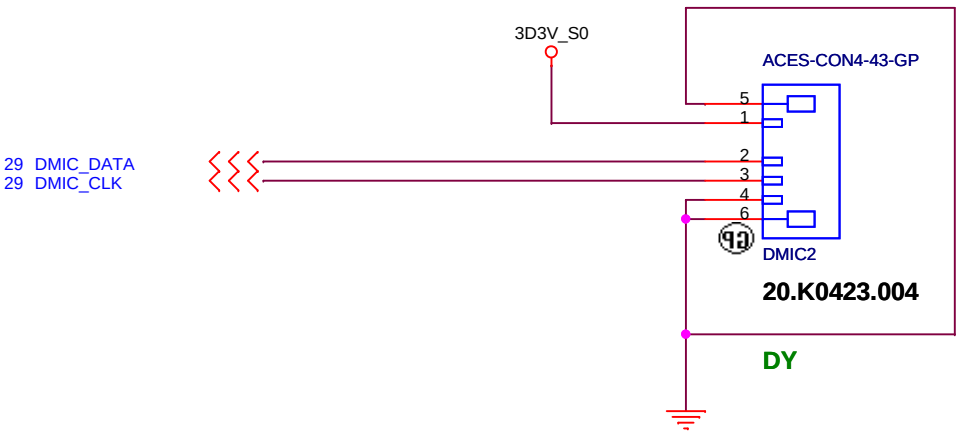
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *E-SATA/USB CHARGER*		
Size: A3	Document Number: Hummingbird1_HR	Rev: -2
Date: Tuesday, April 17, 2012	Sheet 57 of 102	

SSID = AUDIO







<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio Jack***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 58 of 102

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

Without LAN

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

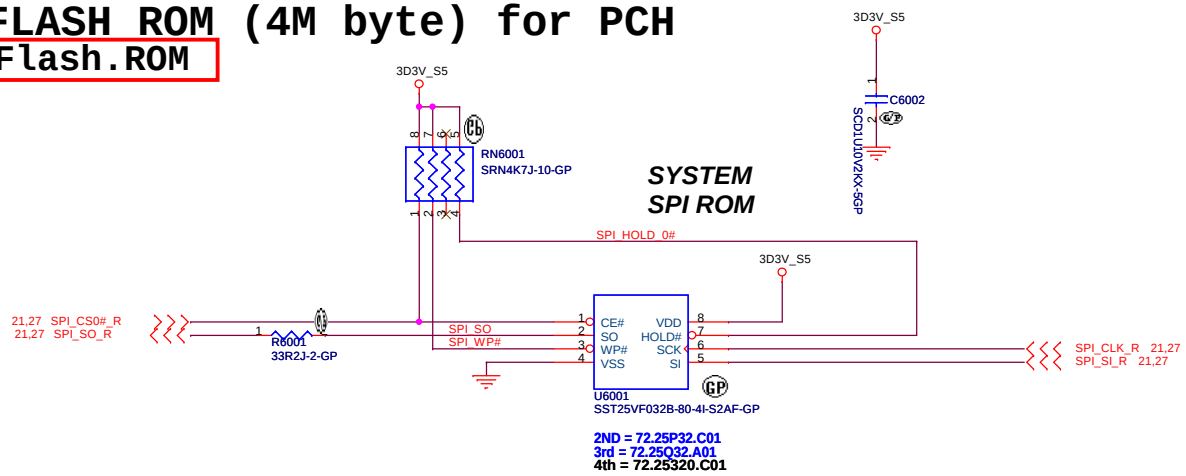
Title: ***LAN CONNECTOR***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

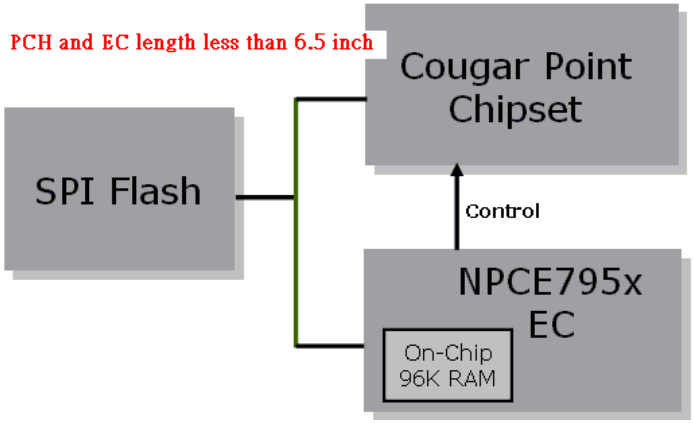
Date: Tuesday, April 17, 2012 Sheet 59 of 102

SPI FLASH ROM (4M byte) for PCH

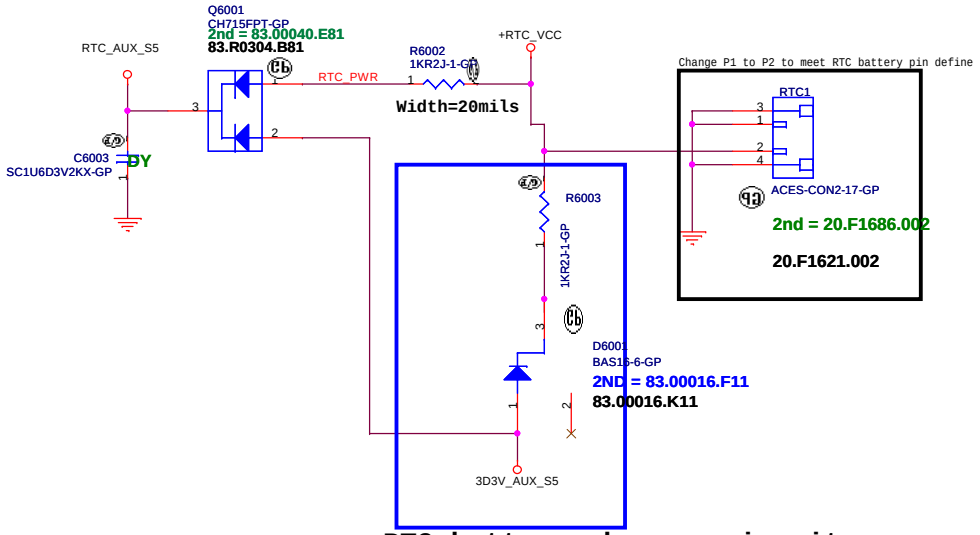
SSID = Flash.ROM



SPI ROM Equal length need to less than 500mil
SPI ROM Equal length need to less than 500mil



SSID = RBATT



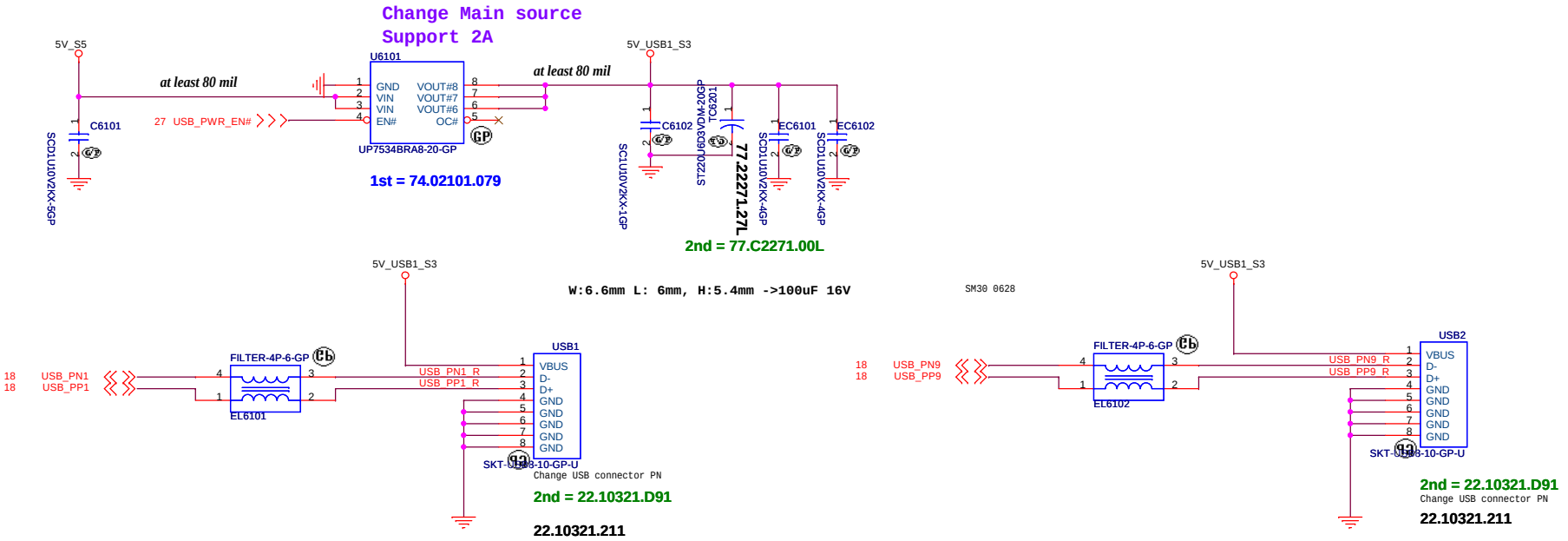
RTC battery charger sircuit

HR PX

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Flash/RTC*		
Size: A3	Document Number: Hummingbird1 HR	Rev: -2
Date: Tuesday, April 17, 2012	Sheet 60 of 102	

SSID = USB

IO Board USB Power



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 61 of 102

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB 3.0 Port*

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 62 of 102

SSID = User.Interface

Bluetooth Module conn.

Without BT

<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

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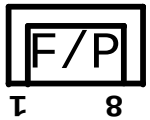
Finger printer

JE40 delete FP function



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

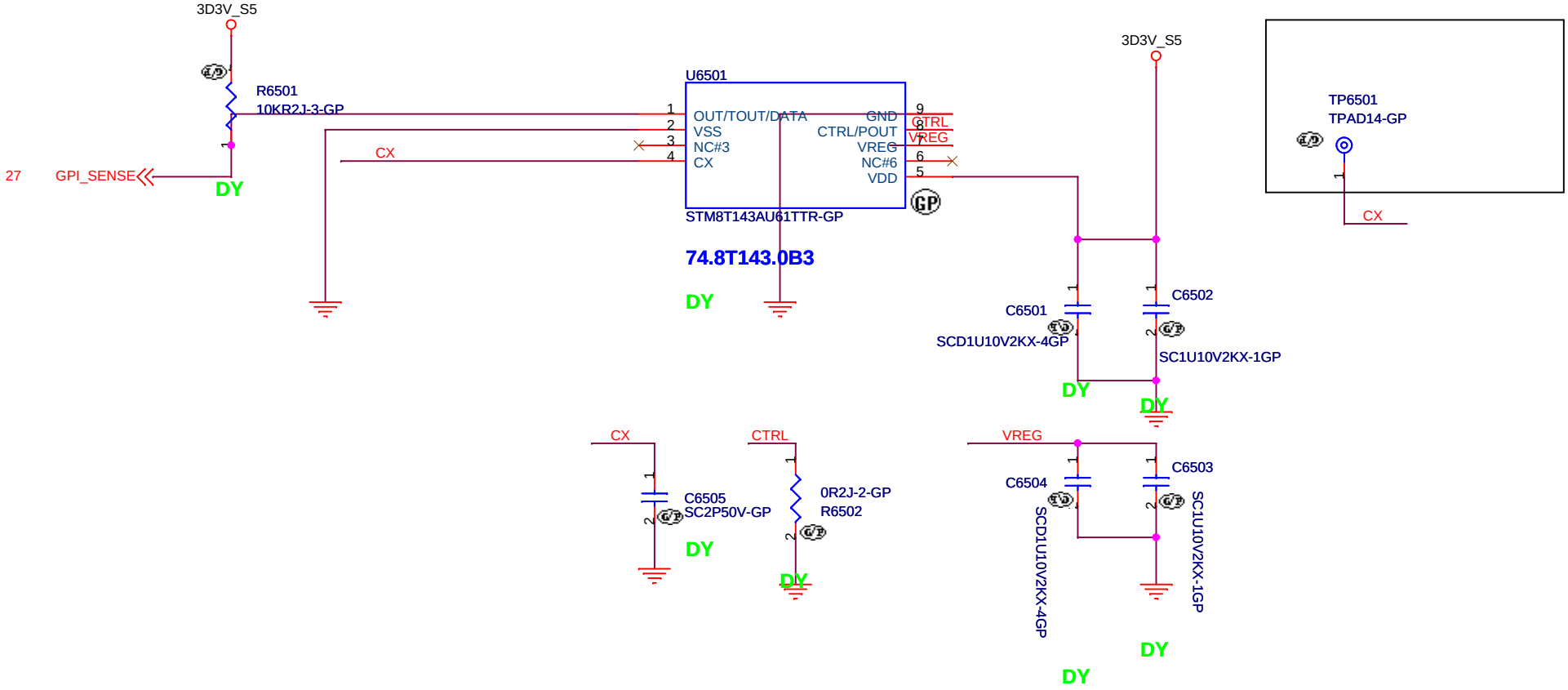
Title
RESERVED

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 64 of 102

SSID = Wireless

C Sensor



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MINICARD(WLAN)/ITP CONN***
Size: A4	Document Number: **Hummingbird1_HR**
Rev: **-2**	
Date: Tuesday, April 17, 2012	Sheet 65 of 102

SSID = Wireless

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***WWAN Connector***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 66 of 102

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***M-SATA***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 67 of 102

SSID = User.Interface

Move to power board

for factory test

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

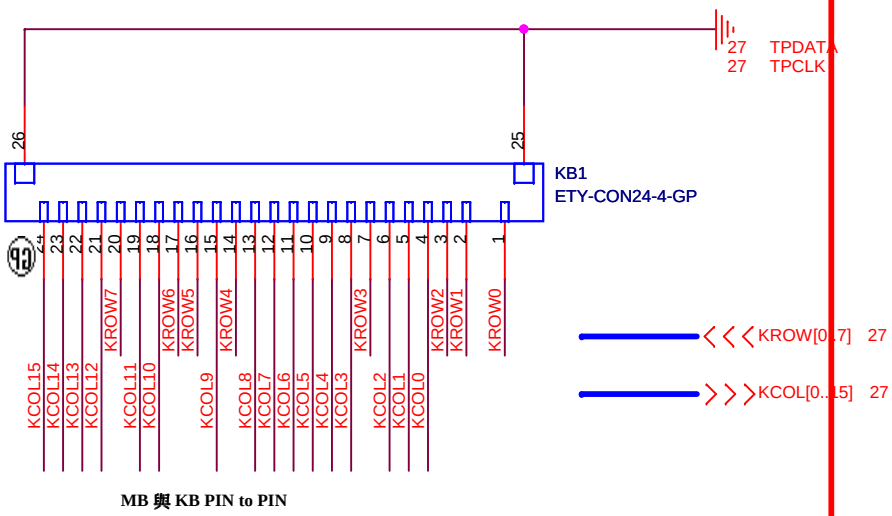
Size: Custom | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 68 of 102

TOUCH PAD

SSID = KBC

Internal KeyBoard Connector

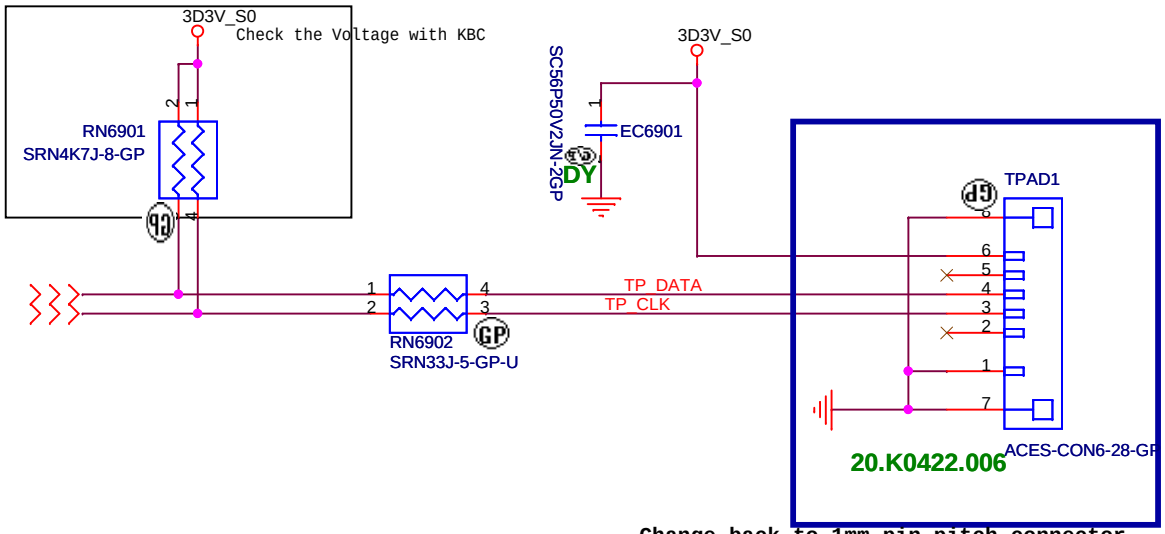


MB 與 KB PIN to PIN

1 K/B 26

Change KB from 下接觸 to 上接觸

KB Pin define need to check again



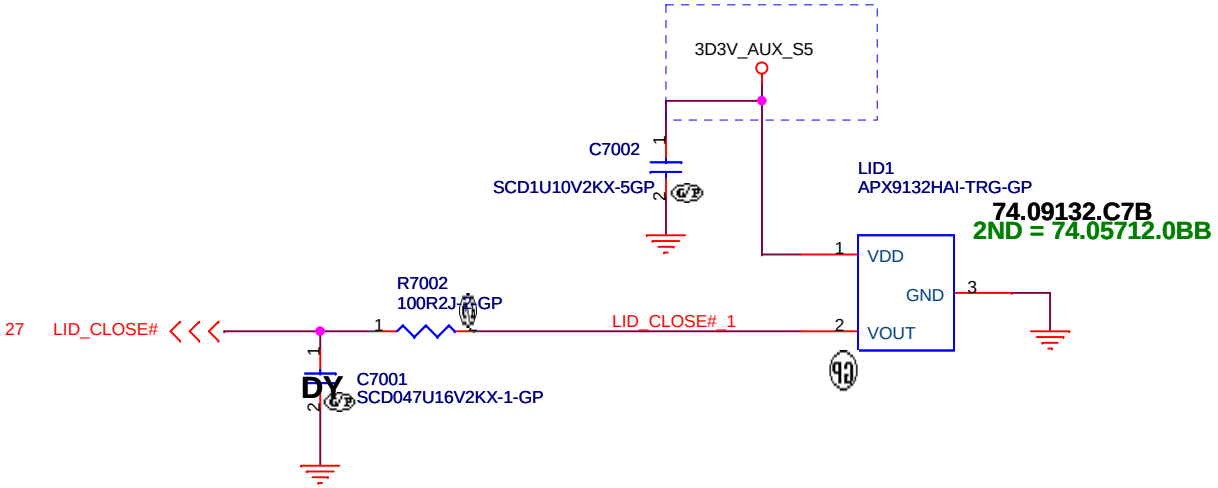
Change back to 1mm pin pitch connector

Switch the pin order SA

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Key Board/Touch Pad		
Size: A4	Document Number: Hummingbird1 HR	Rev: -2
Date: Tuesday, April 17, 2012	Sheet 69 of 102	

Change from 3D3V_AUX_KBC to 3D3V_AUX_S5



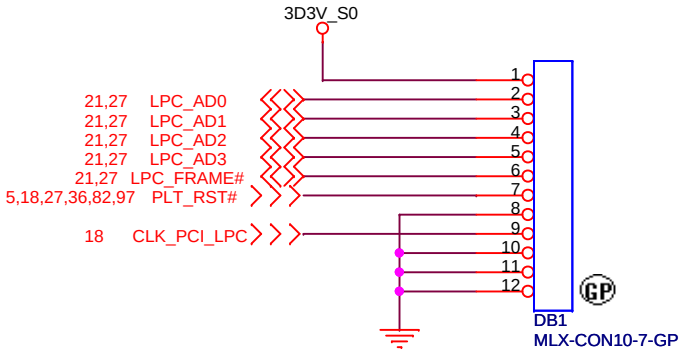
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	-2

Date: Tuesday, April 17, 2012 Sheet 70 of 102



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 71 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 72 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 73 of 102

SD/XD/MS Card Reader

Card reader move to small board

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARD Reader CONN***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 74 of 102

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *New Card*

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 75 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 76 of 102

(Blanking)

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 77 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 78 of 102

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Delete G Sensor Function

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*		
Size: A4	Document Number: Hummingbird1_HR	Rev: -2
Date: Tuesday, April 17, 2012	Sheet 79 of 102	

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

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(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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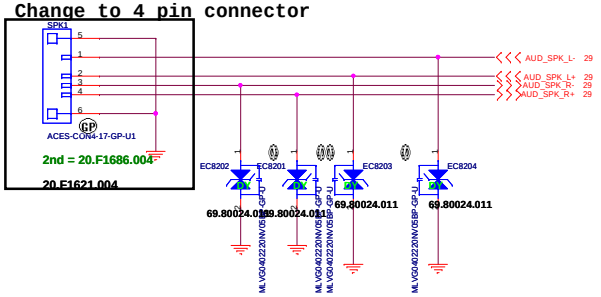
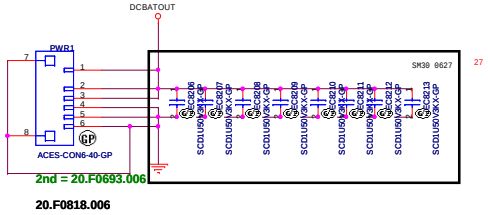
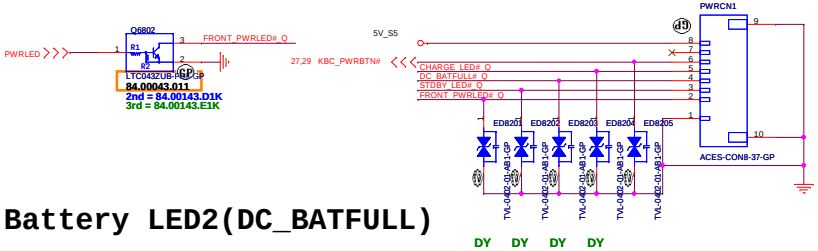
Change to 4 pin connector

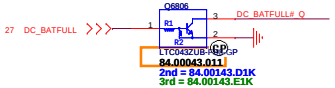


Change the connection

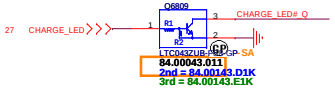




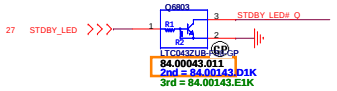
Battery LED2(DC_BATFULL)

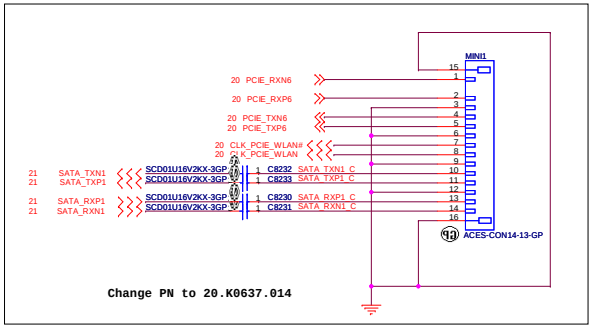


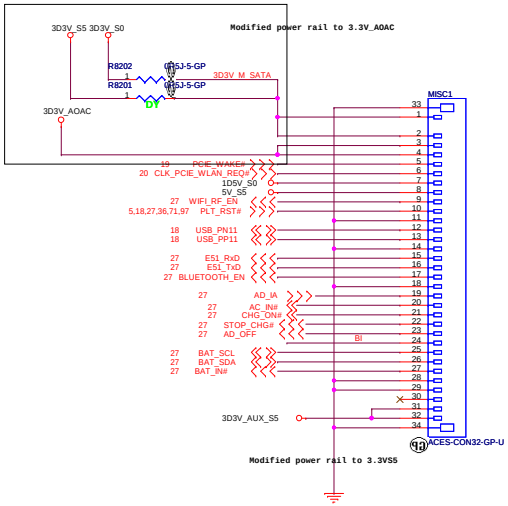
Battery LED1(CHARGE)

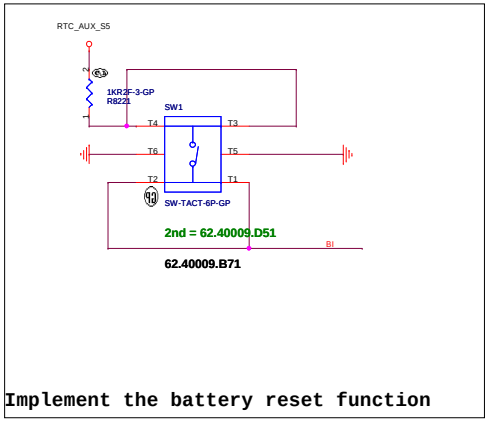


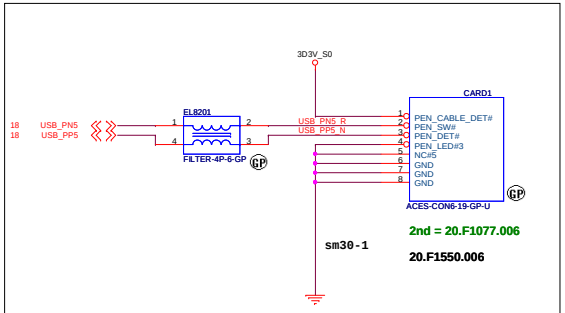
Power STDBY_LED



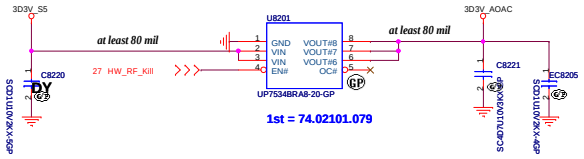








AOAC circuit



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
Size: A2
Document Number: Hummingbird1_HR
Rev: -2
Date: Tuesday, April 17, 2012
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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU_PCIE/STRAPPING(1/5)***

Size	Document Number	Rev
A2	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 83 of 102

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size	Document Number	Rev
Custom	Hummingbird1_HR	-2
Date: Tuesday, April 17, 2012	Sheet 84 of 102	

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size	Document Number	Rev
Custom	Hummingbird1_HR	-2

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size	Document Number	Rev
A1	Hummingbird1 HR	-2

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<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU_DPPWR/GND(5/5)***

Size	Document Number	Rev
A3	**Hummingbird1_HR**	**-2**

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM1,2 (1/4)***

Size	Document Number	Rev
Custom	**Hummingbird1_HR**	**-2**

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM3,4 (2/4)***

Size	Document Number	Rev
Custom	**Hummingbird1_HR**	**-2**

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
Custom	Hummingbird1_HR	-2
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<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM7,8 (4/4)***

Size	Document Number	Rev
Custom	**Hummingbird1_HR**	-2

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***RT8208B +VGA CORE***

Size	Document Number	Rev
Custom	**Hummingbird1 HR**	-2

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DISCRETE VGA POWER***

Size	Document Number	Rev
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LVDS Channel A

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

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Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT_Switch***

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A4	**Hummingbird1_HR**	**-2**

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SSID = SDIO

Blanking

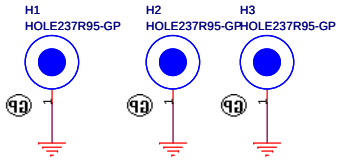
<Variant Name>

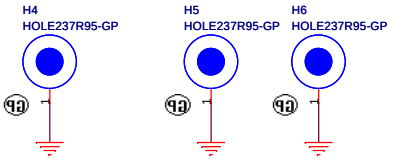
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

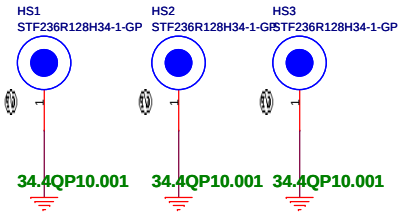
Title: TOUCH PANEL

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

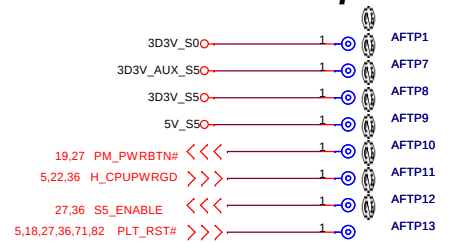
Date: Tuesday, April 17, 2012 Sheet 96 of 102



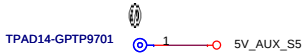


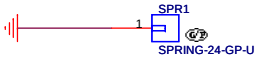


Check test point



Test Point放在Dimm Door打開可量測處





<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS/EMI Capacitors***

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 97 of 102

(1) change U6001 to socket 62.10089.001

(2) change SW_L1 and SW_R1 PN to 『62.40089.221』

(3) KI.G6501.001 / IC BD82HM65 SLH9D MM#908753 B2 FCBGA 989
KI.G6501.004 / IC BD82HM65 SLJ4P MM#914377 B3 FCBGA989P

(4)U3101 change PN to 71.08158.M02
(5)DM2 1st -> change PN to 62.10024.G01
(6) IMIC1 =>82.40012.001
(7) RJ1 =>22.10177.J71
(8) CPU1 =>1st change PN to 62.10055.321
(9) USB2 =>1st change PN to22.10218.G01 -> only Lab stage

-SA

-SB

-1

-2

[Lab] S01G ==>1st
S02G ==>2nd(NEC Cap)

Coin Battery:
1st:23.20068.001
2nd:23.22063.001

<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

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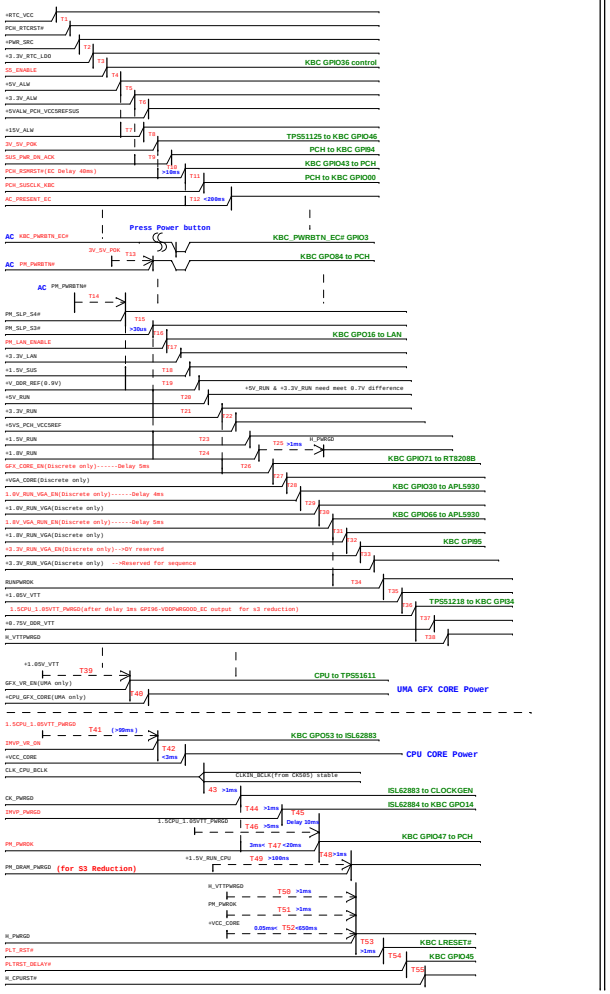
Intel-Power Up Sequence

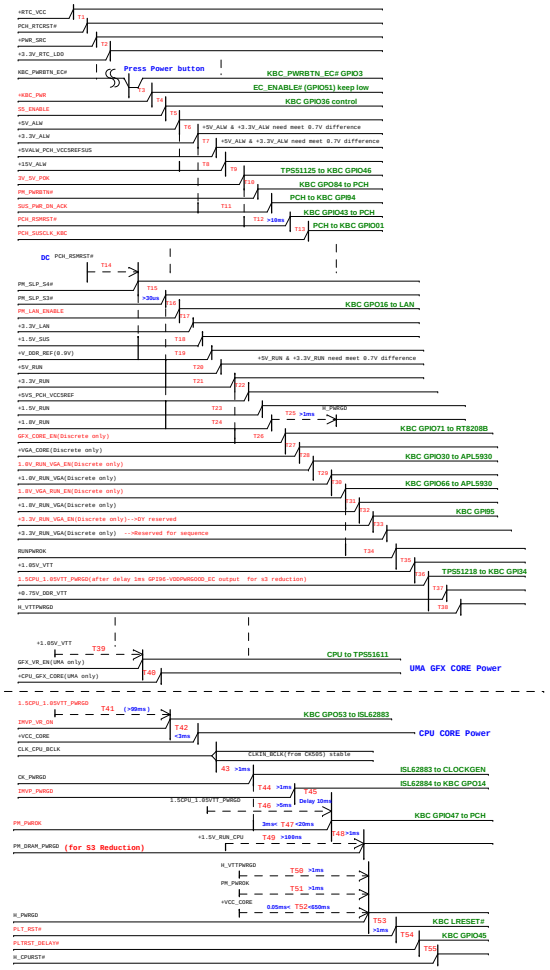
(AC mode)

red word: KBC GPIO

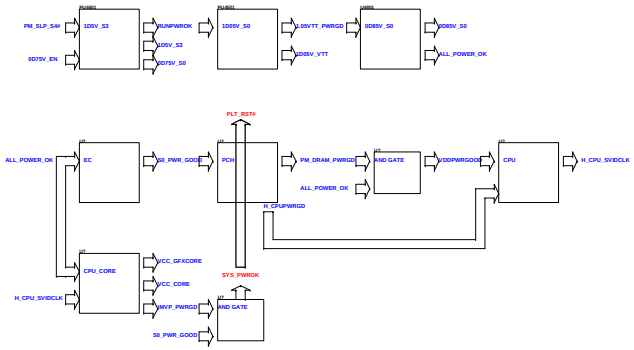


(DC mode)

red word: KBC GPIO



Power Sequence

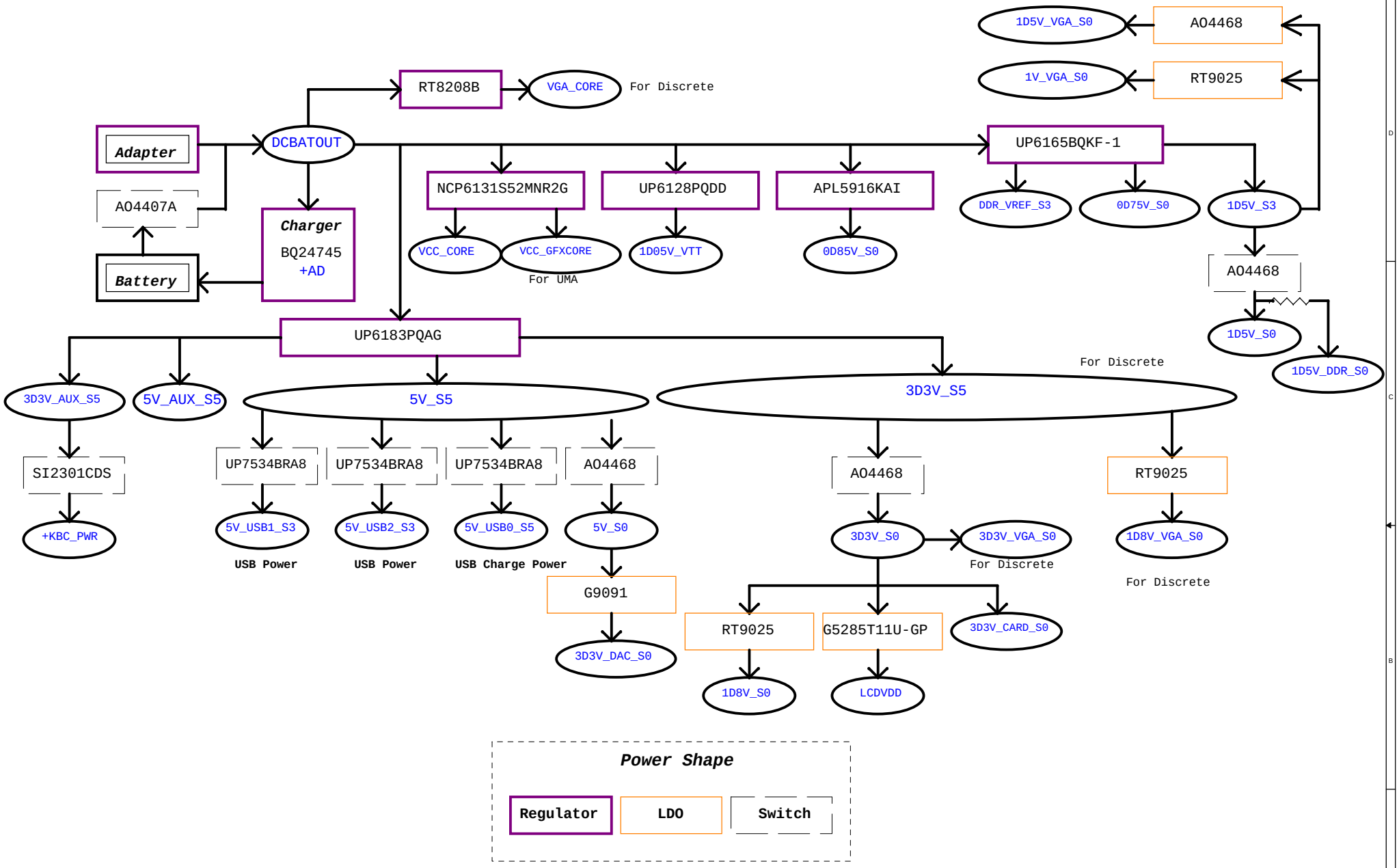


Wistron Corporation

Power Sequence

Humminbird1_HR

2



HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
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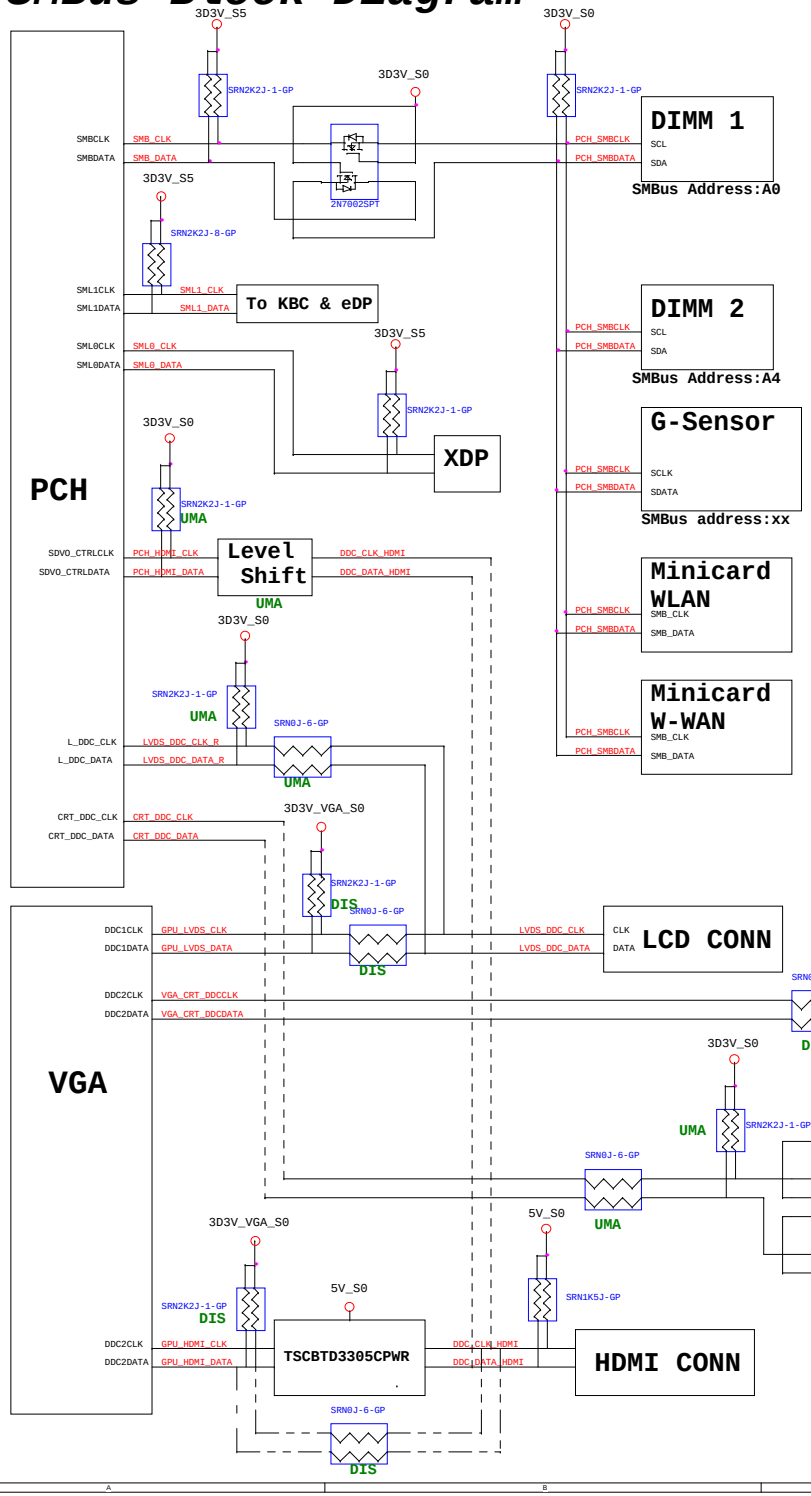
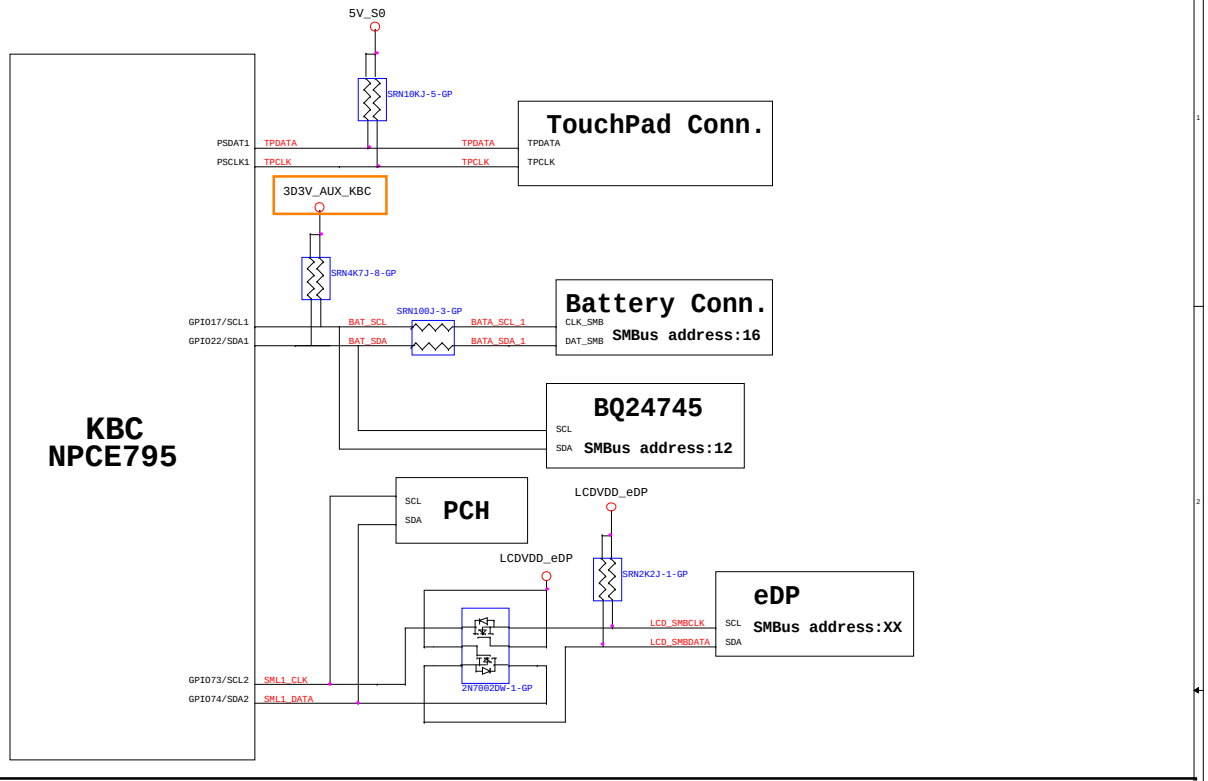
PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Variant Name>

Wistron Corporation
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Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	Hummingbird1_HR	-2

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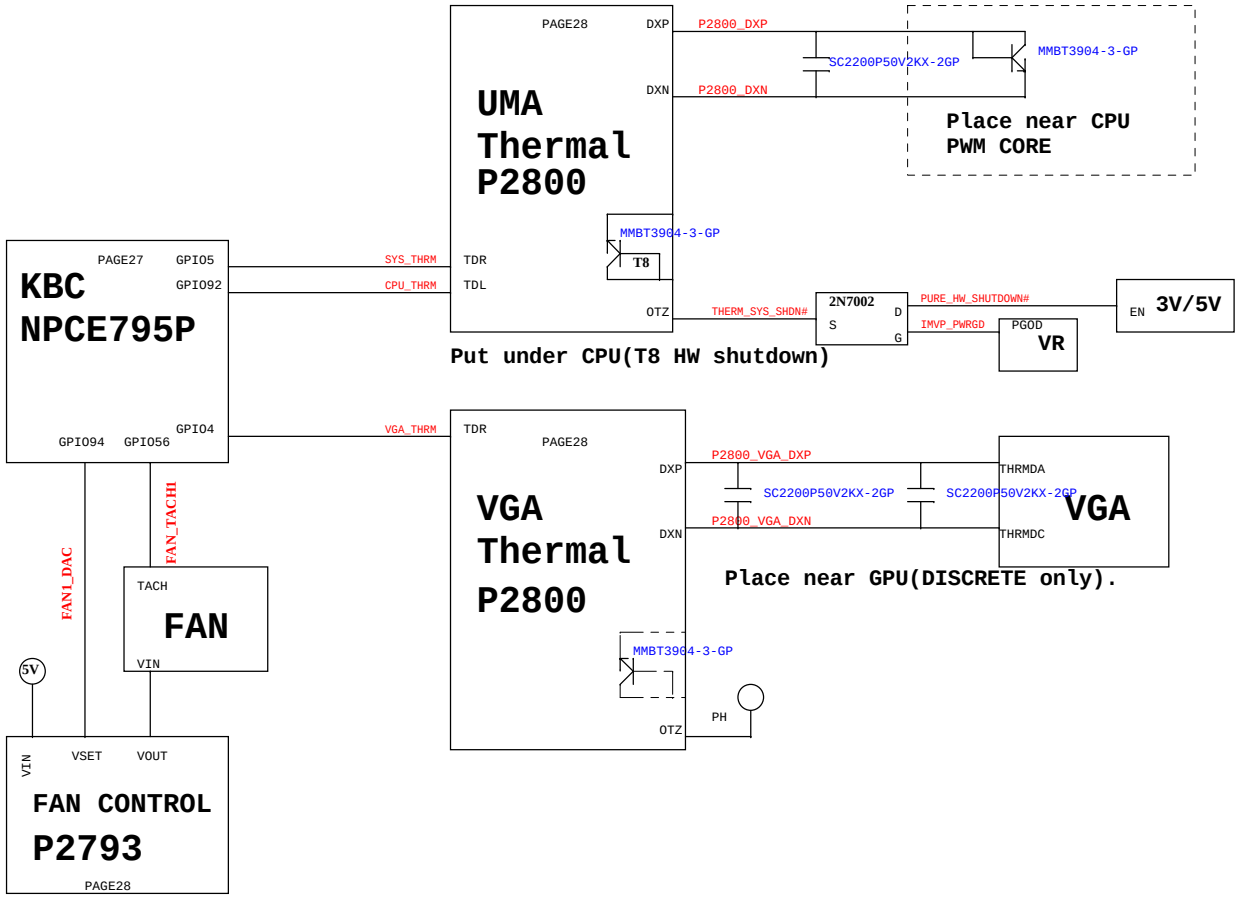
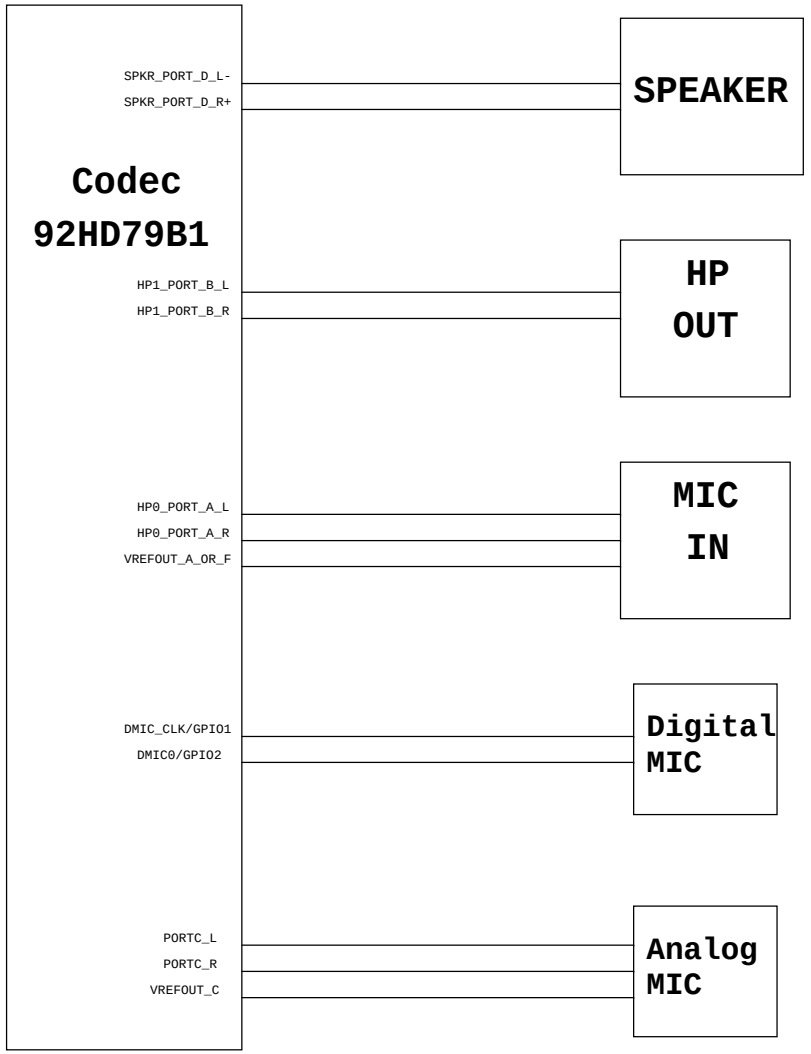
Thermal Block Diagram



Audio Block Diagram



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

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