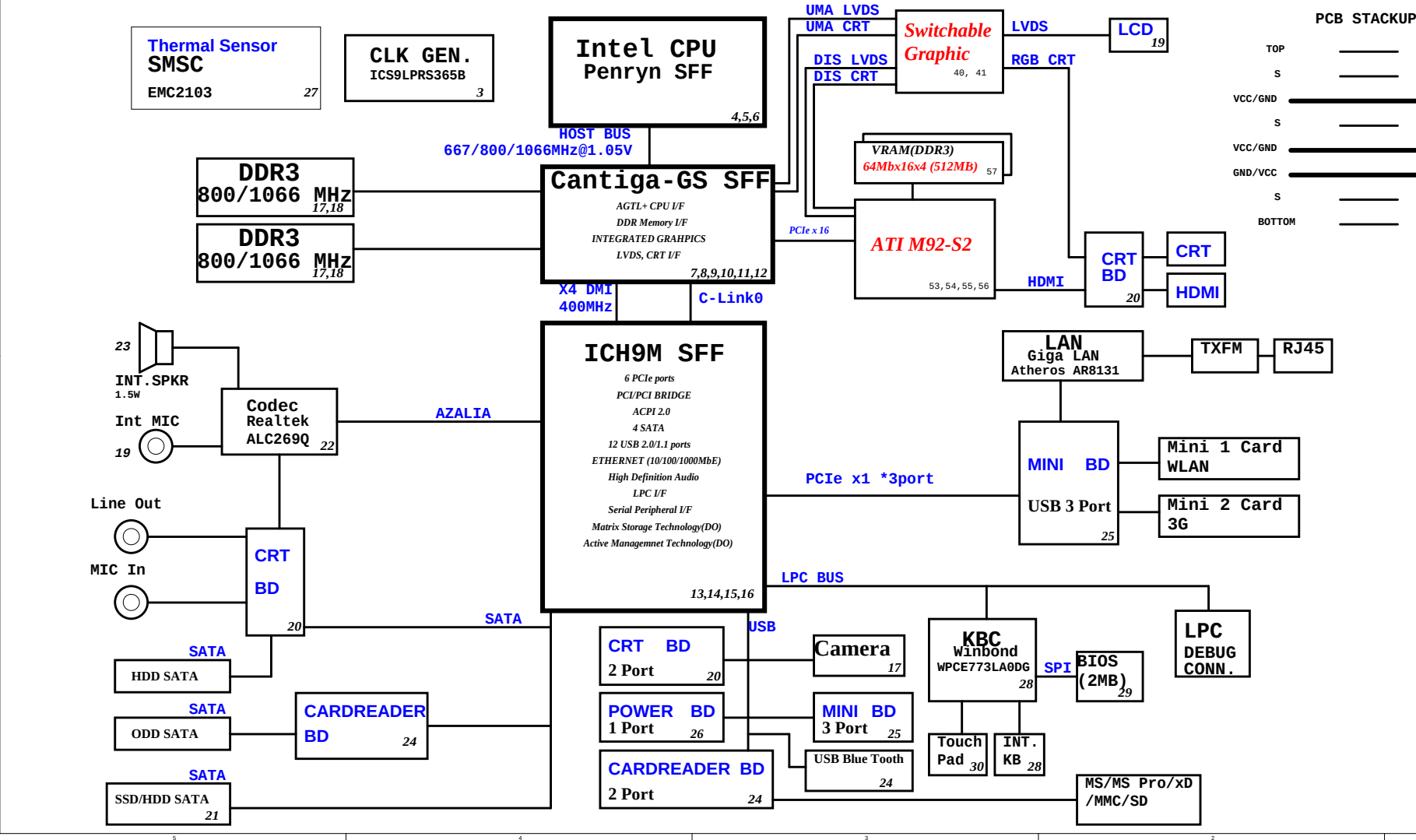


JM41/JM51 Discrete Block Diagram

Project code: 91.4CQ01.001
PCB P/N : 48.4CQ01.0SB
REVISION : 08274-1



PCB STACKUP

TOP	_____	L1
S	_____	L2
VCC/GND	_____	L3
S	_____	L4
VCC/GND	_____	L5
GND/VCC	_____	L6
S	_____	L7
BOTTOM	_____	L8

SYSTEM DC/DC TPS51125 36	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5
RT8202 37	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A)
RT8202 38	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(11A)
RT9026 39	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3(1.2A)
CHARGER MAX8731A 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC ADP3207A 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 64A
VGA ISL6263A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

DIS

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File

BLOCK DIAGRAM

Size Custom

Document Number

Date: Tuesday, April 07, 2009

Sheet 1 of 48

Rev -1

JM41 Discrete

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPI020	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPI049	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

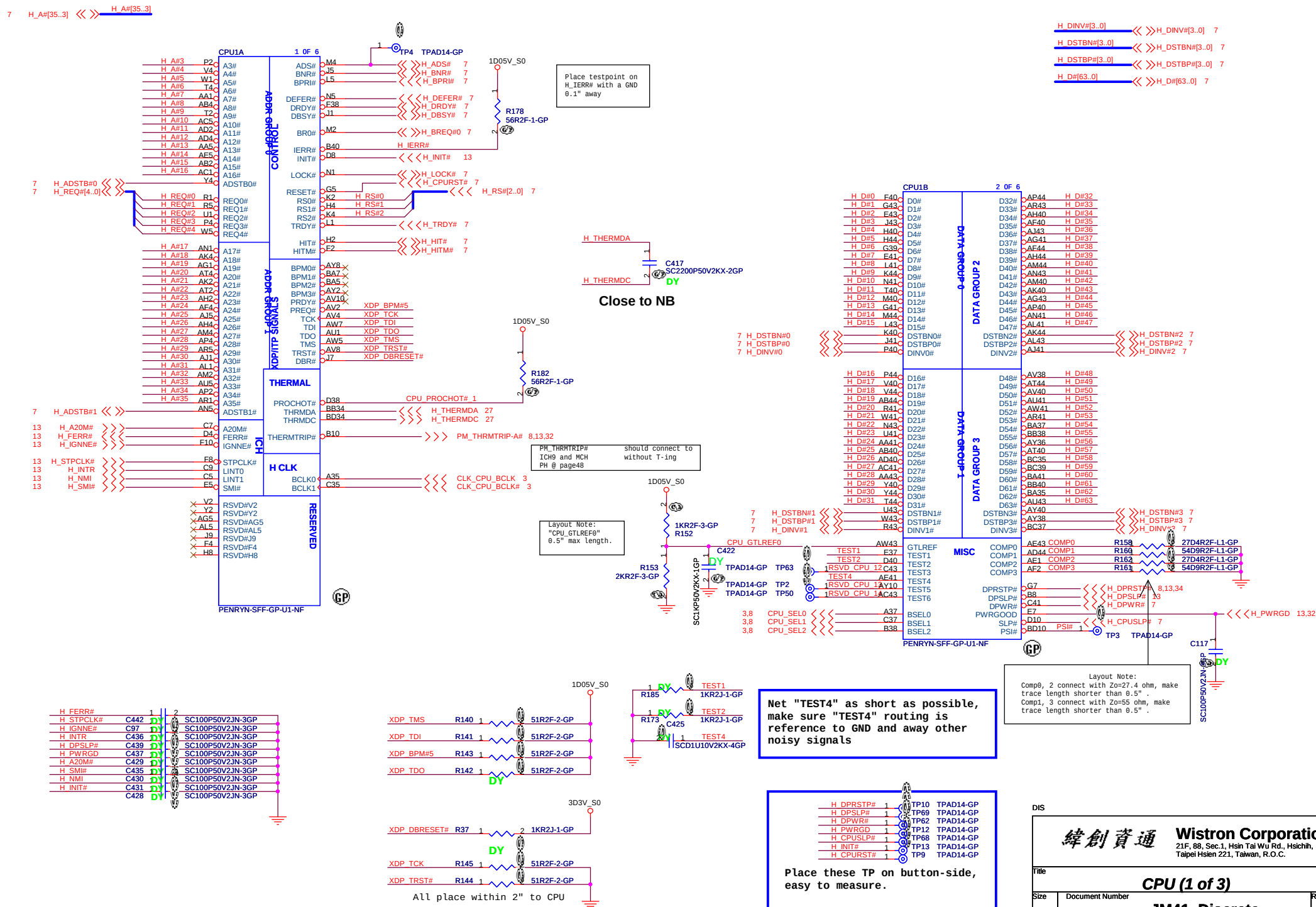
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

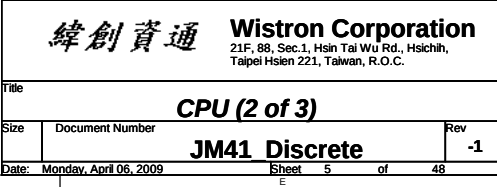
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

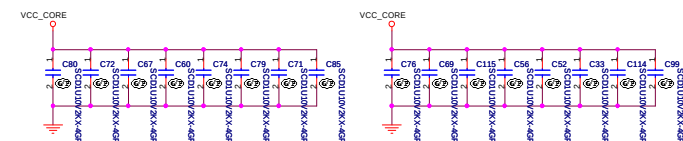
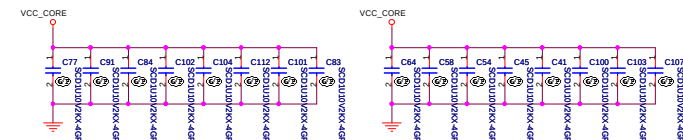
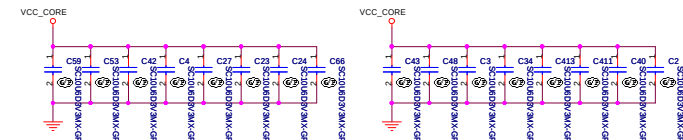
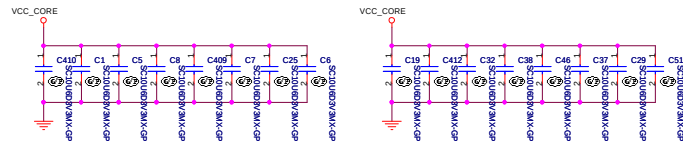
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display port and PCie are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

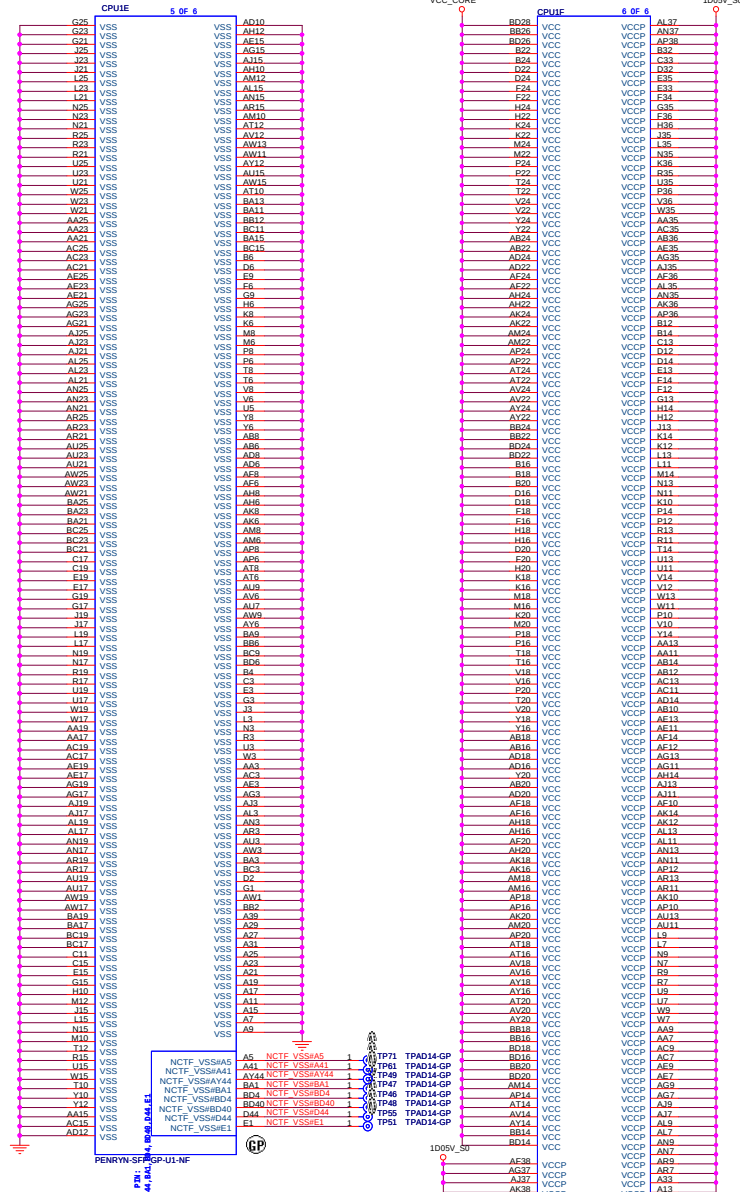
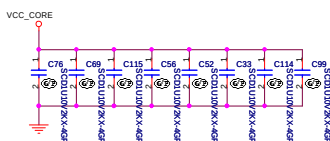
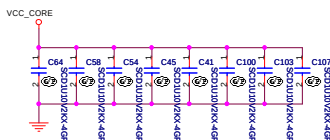
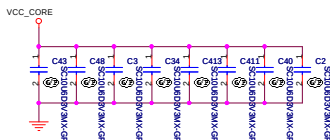
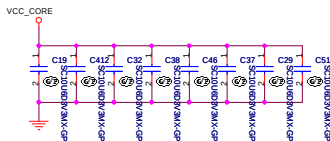
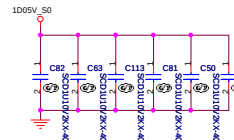




Place these inside socket cavity on L8(North side Secondary)

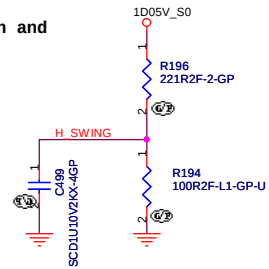


Place these inside socket cavity on L8(North side Secondary)

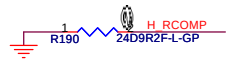


H_SWING routing Trace width and Spacing use 10 / 20 mil

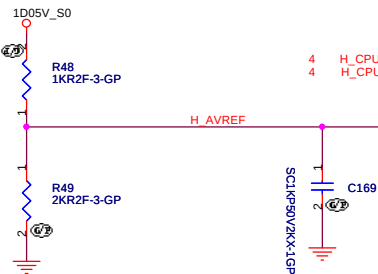
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5"



H_SWING B6
H_RCOMP D4

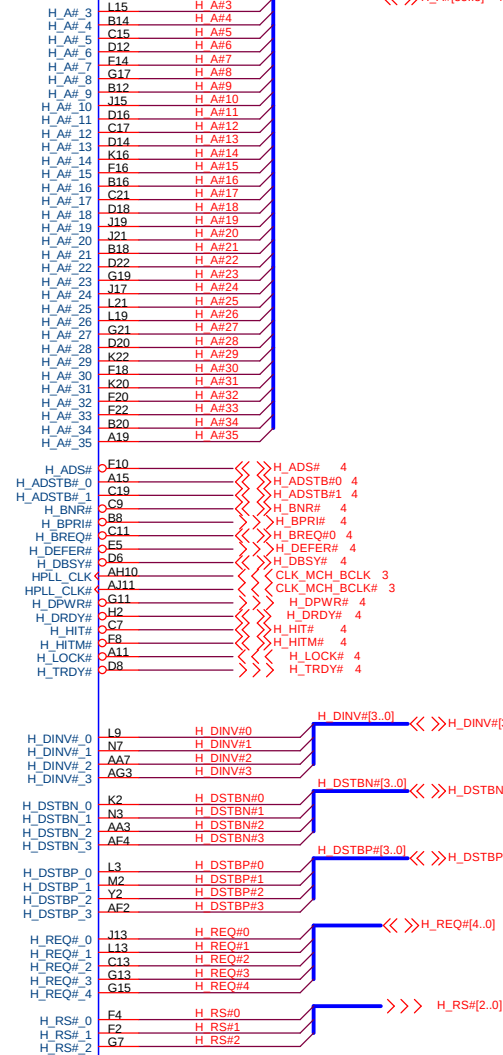
4 H_CPURST# J11
4 H_CPUSLP# G9

H_AVREF L17
H_DVREF K18

CANTIGA-GS-GP-NF

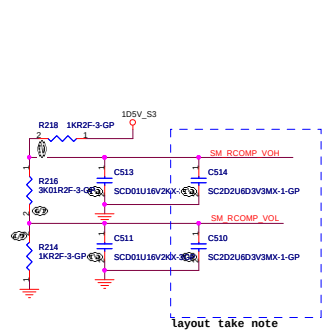
NB1A 1 OF 18

HOST

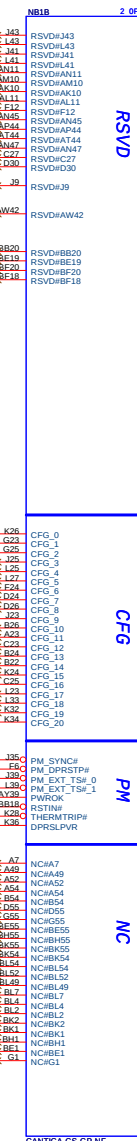
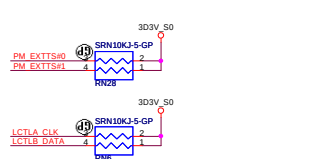
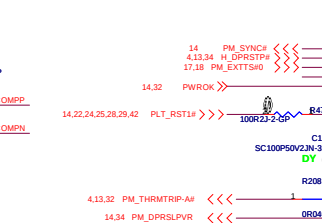
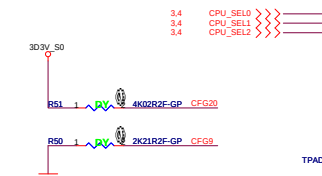


DIS

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layout take note



RSVD
CFG
PM
ME
MISC
HDA

DDR CLK/ CONTROL/COMPENSATION
CLK
GRAPHICS VID DMI
VGA

PCI EXPRESS
VGA

Close to GMCH as 500 mils.

0.75V

for debug only

FOR Cantiga: 1.02k 1% ohm
Teenah: 1.3k ohm
CRT IREF routing Trace width use 20 mil

FOR Cantiga: 500 ohm
Teenah: 392 ohm

0.75V

0.75V

0.75V

0.75V

0.75V

0.75V

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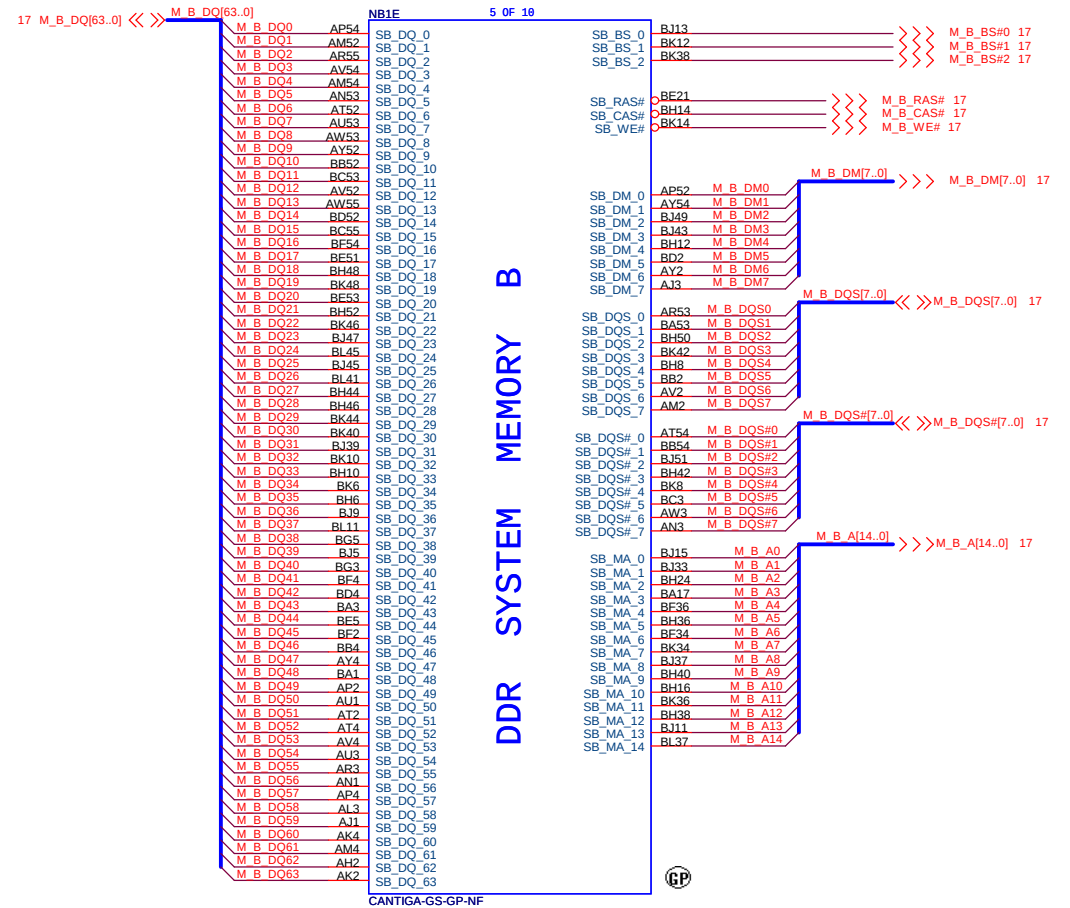
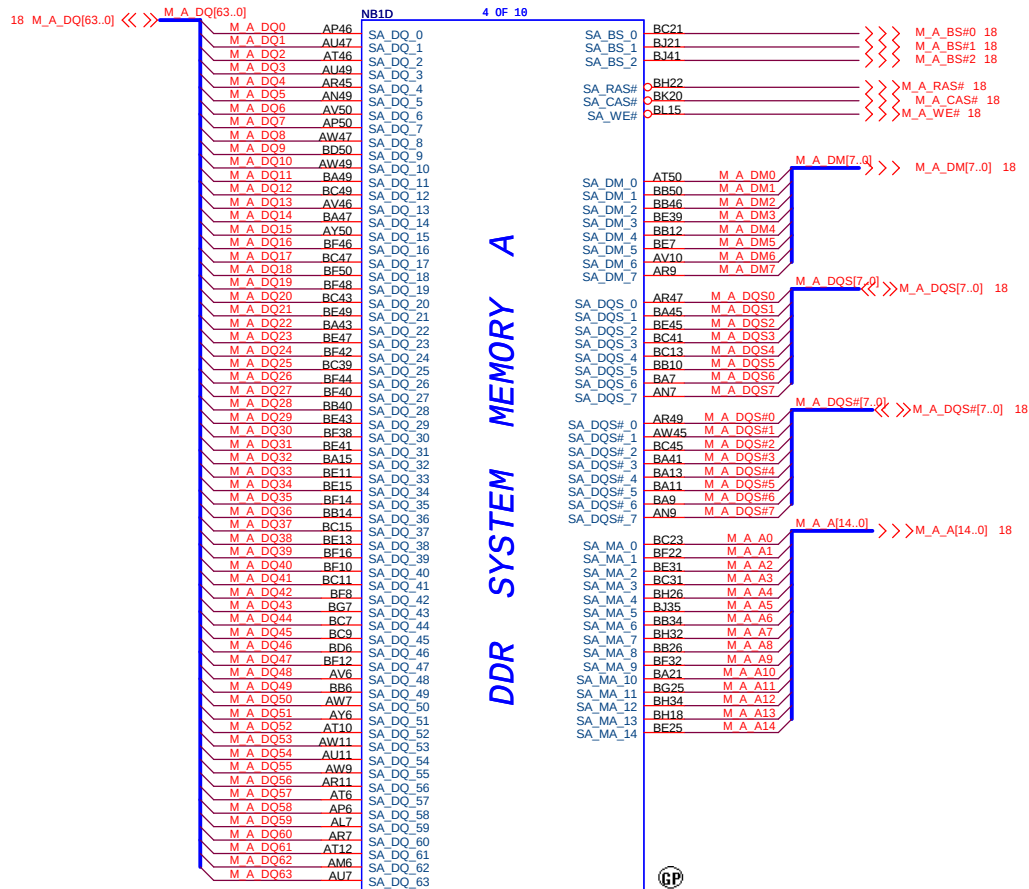
0.75V

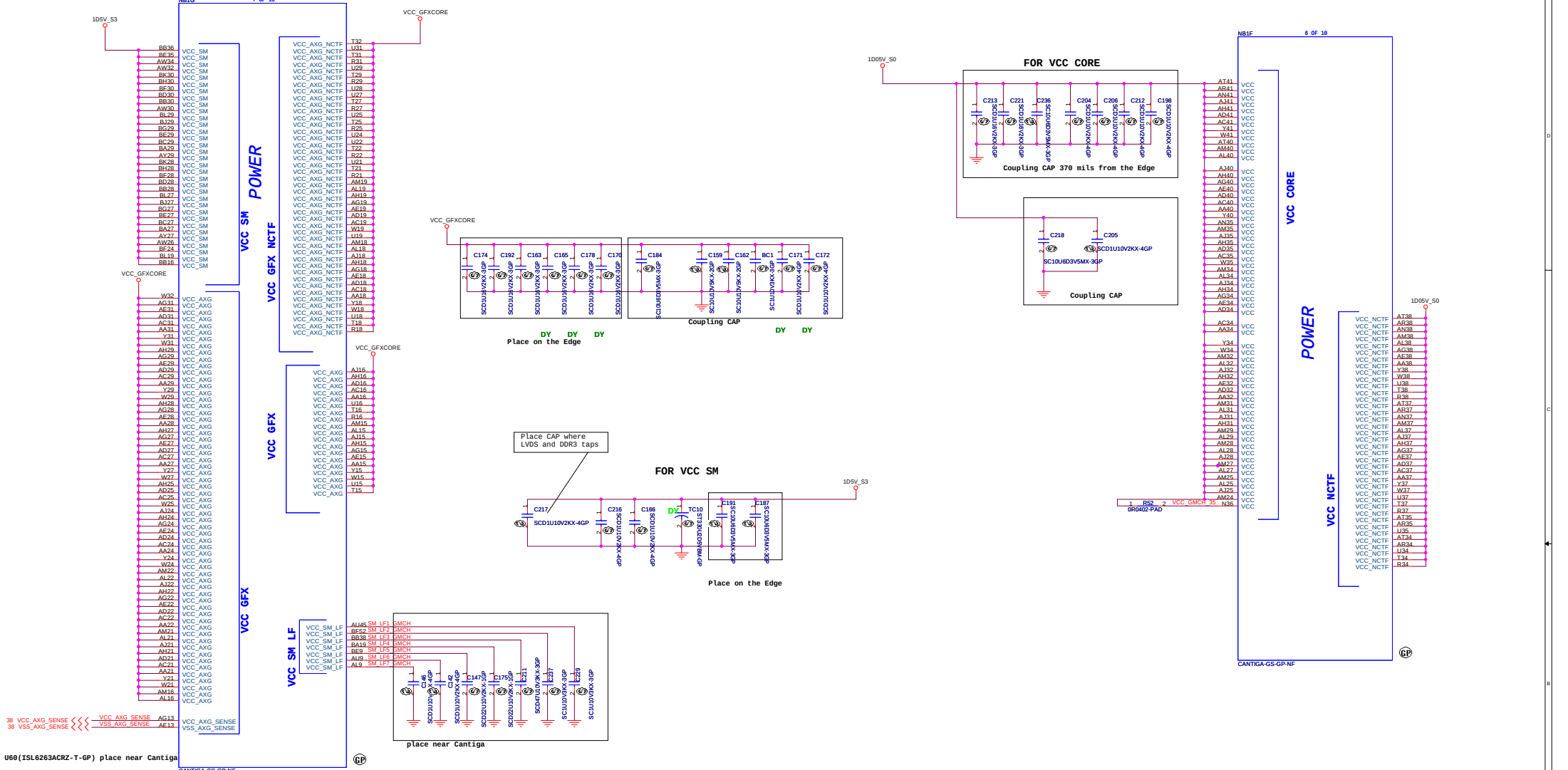
0.75V

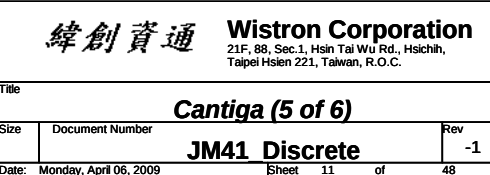
0.75V

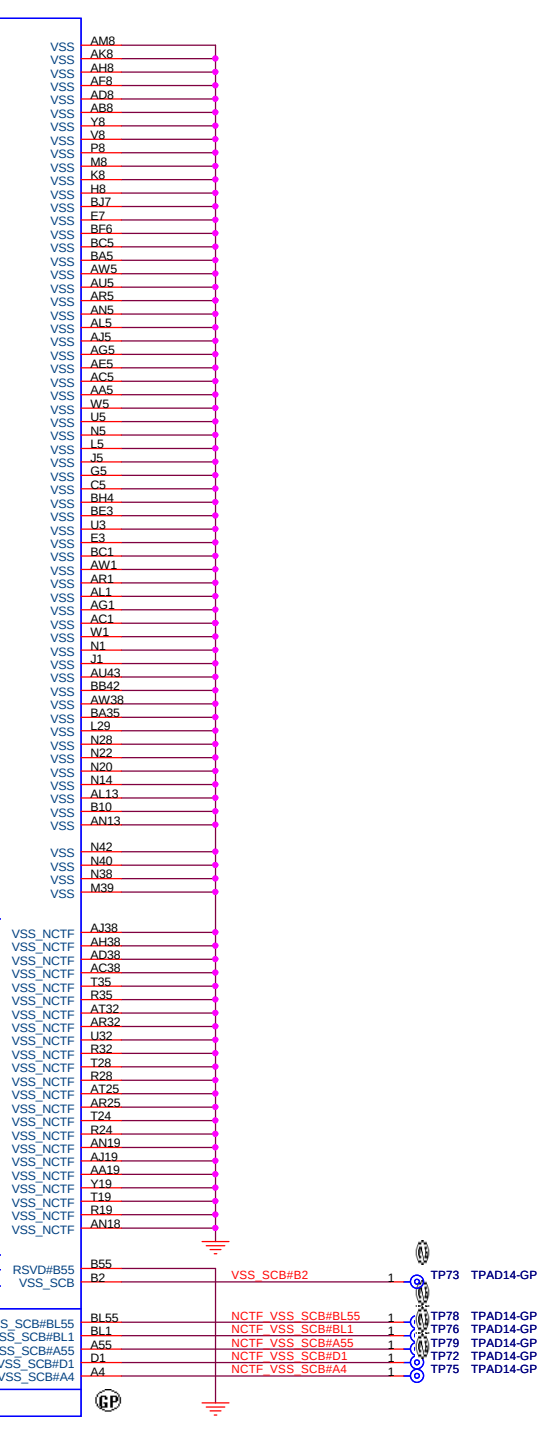
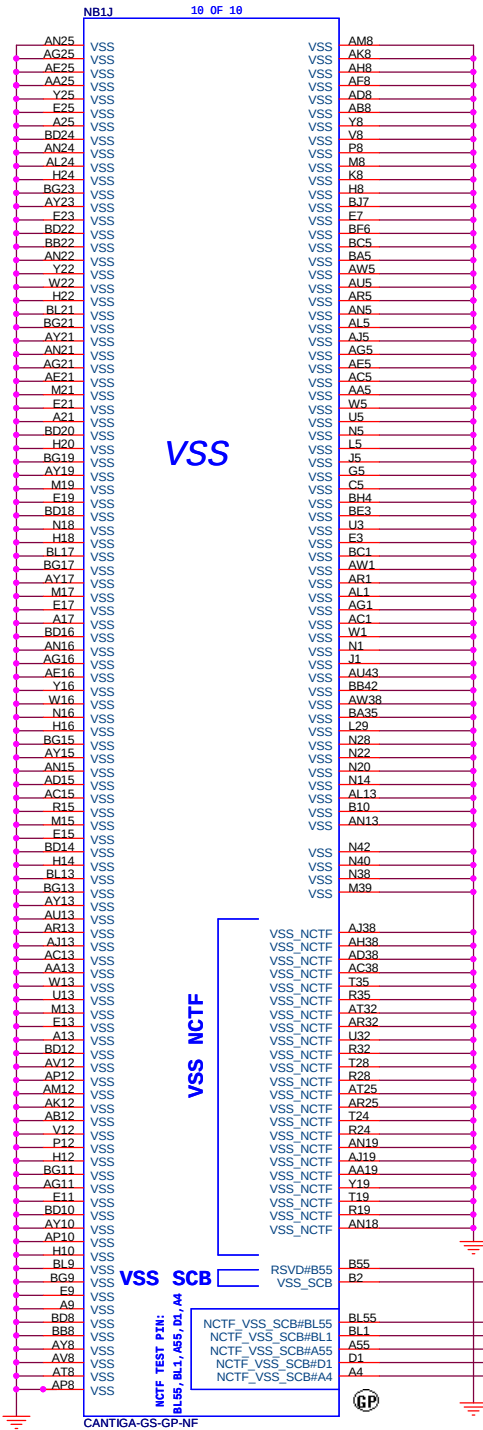
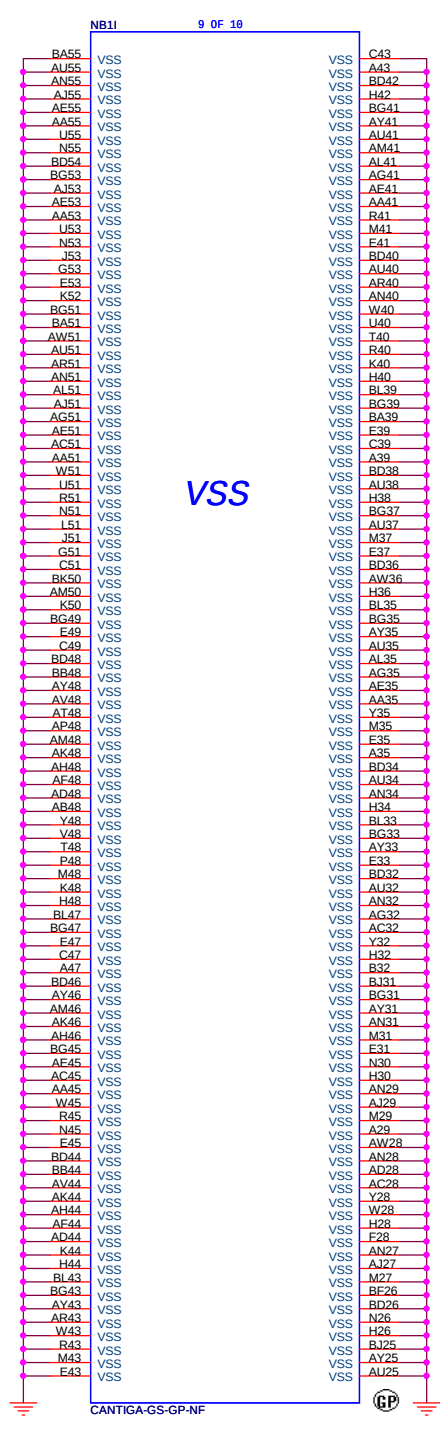
0.75V

0.75V

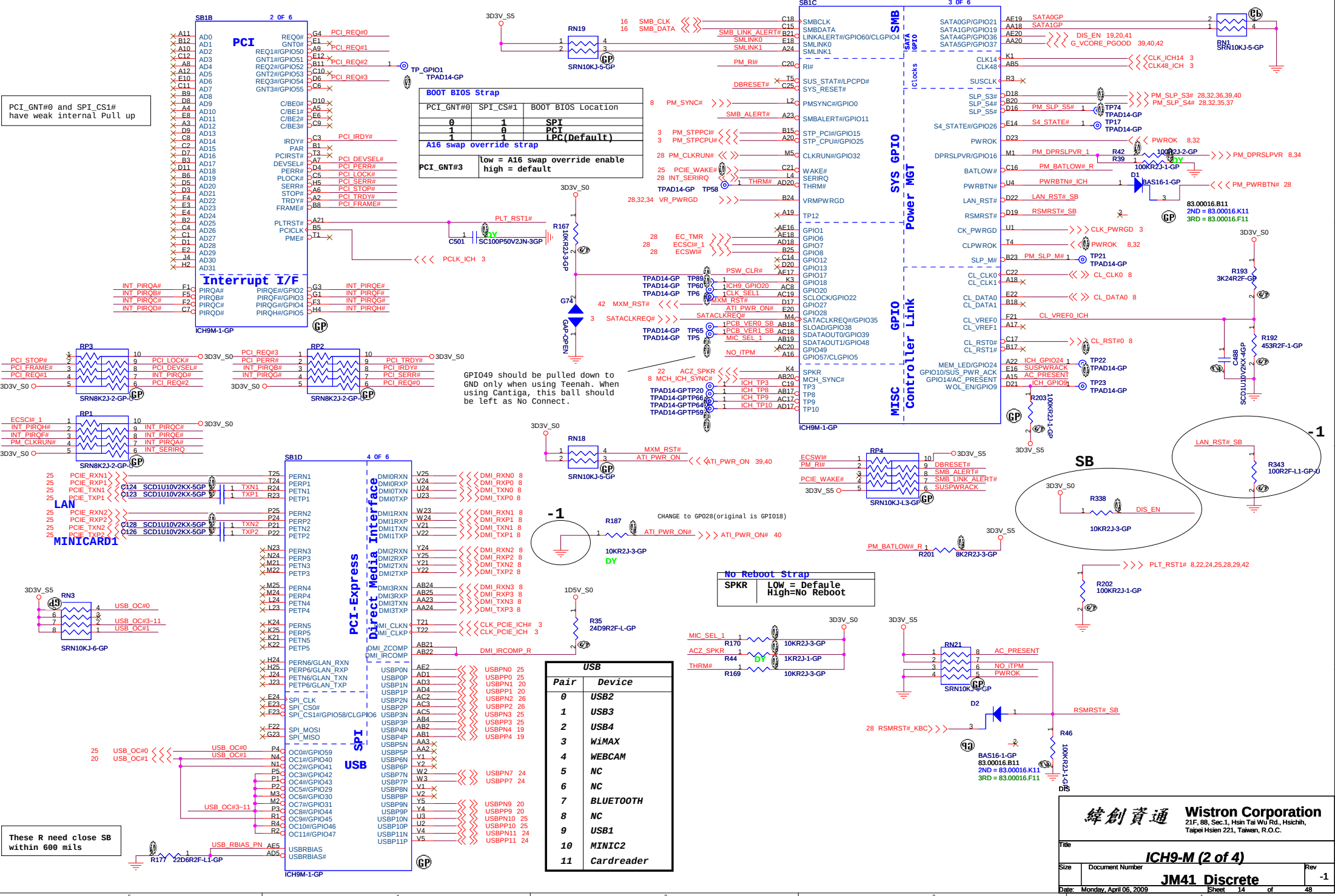








PCI_GNT#0 and SPI_CS1#
have weak internal Pull up



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Title

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Monday, April 06, 2009

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of

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Rev

-1

JM41 Discrete

657mA

6uA in G3

1.13A

23mA

50mA

1mA

VCC3_3=278mA

32mA

32mA

177mA

18mA

47mA

SATA+USB=1.56A

USBPLL=10mA

23mA

80mA

1mA

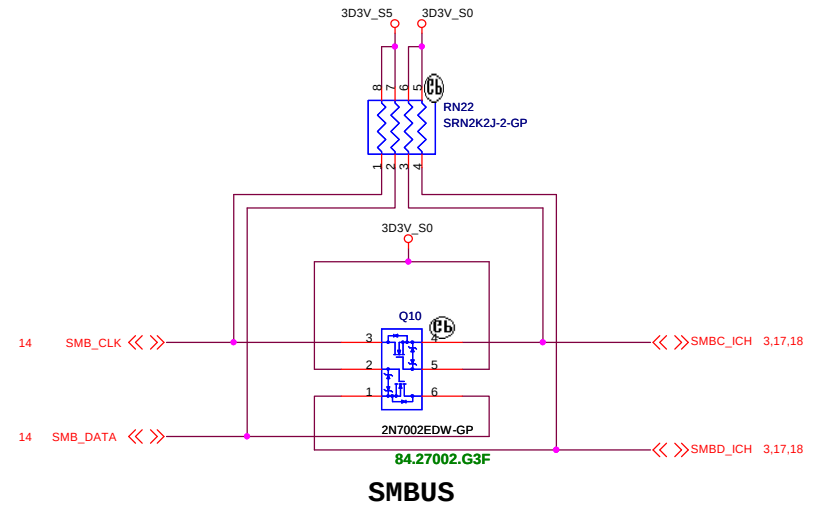
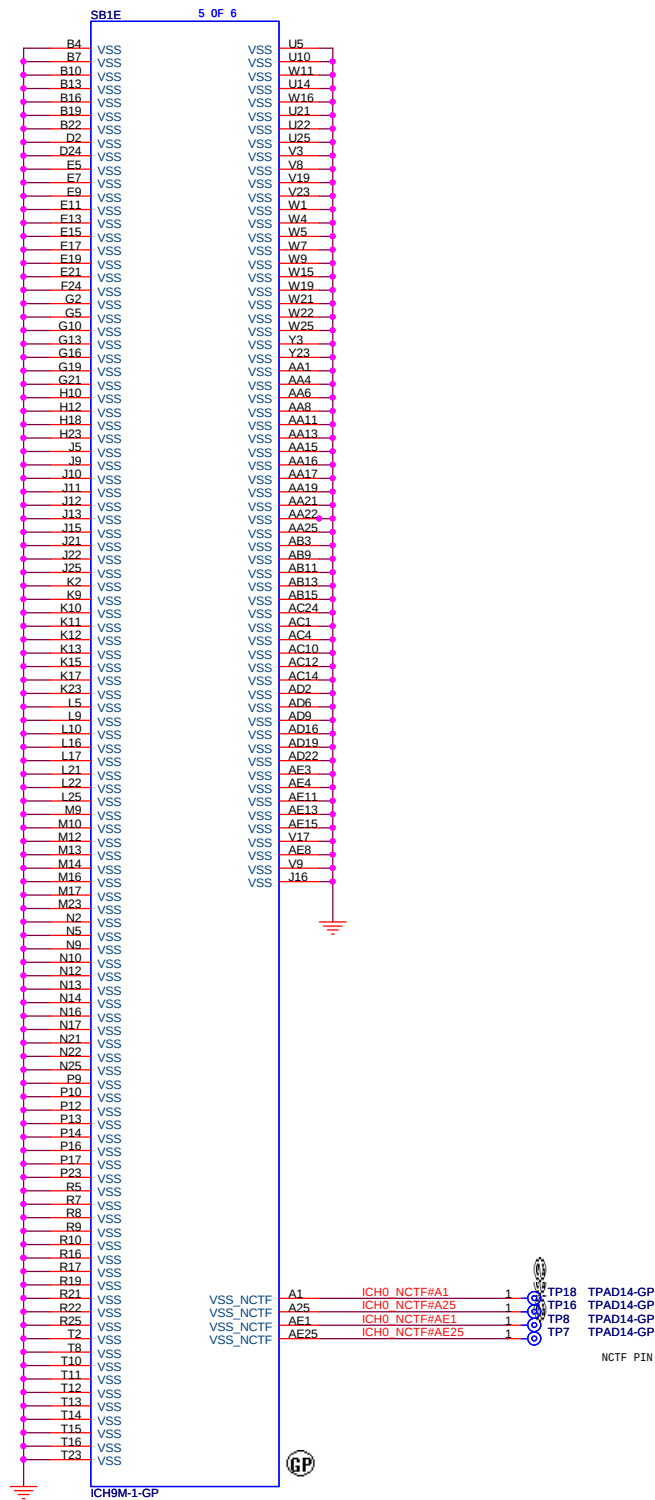
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

2mA

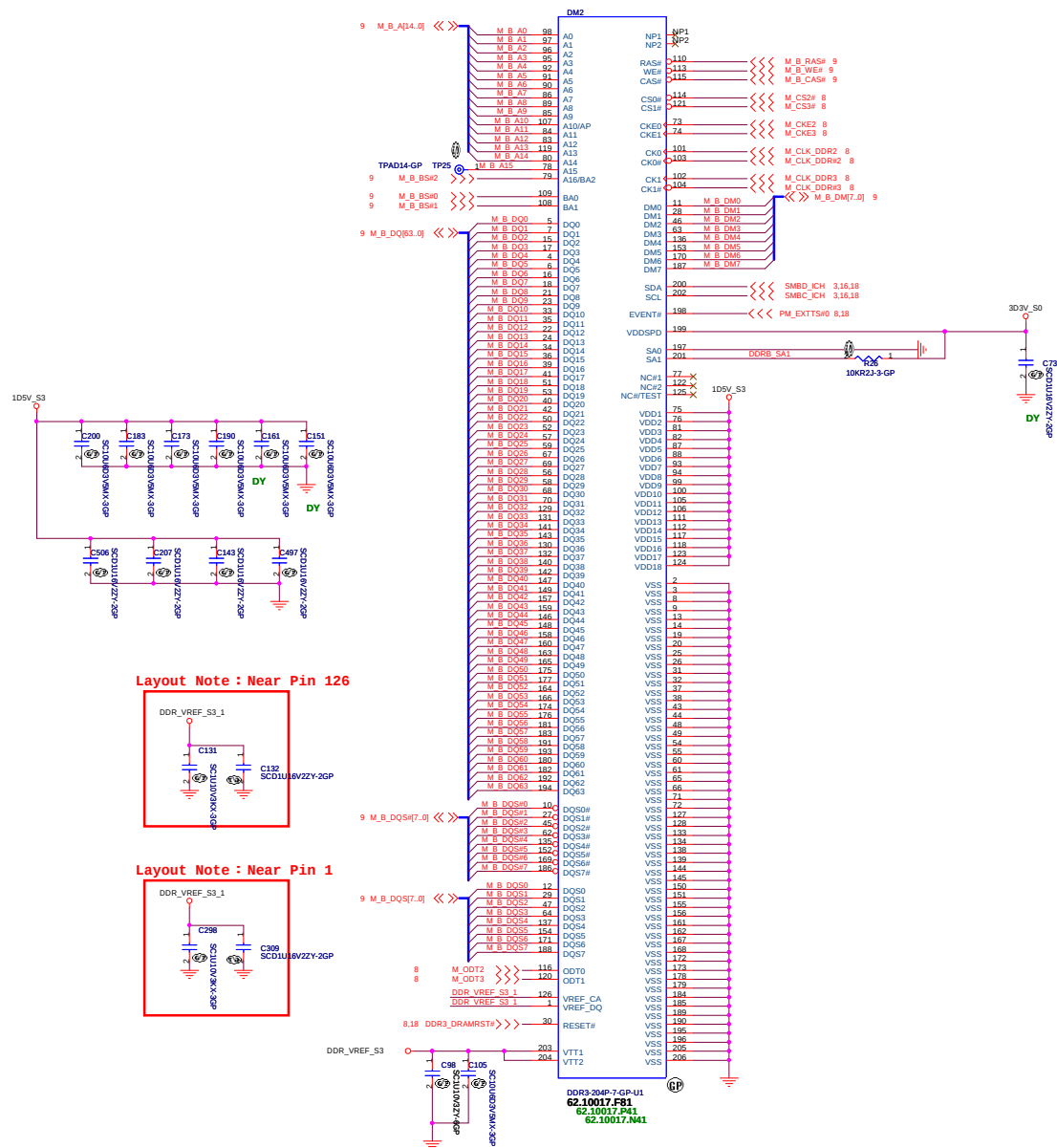
2mA

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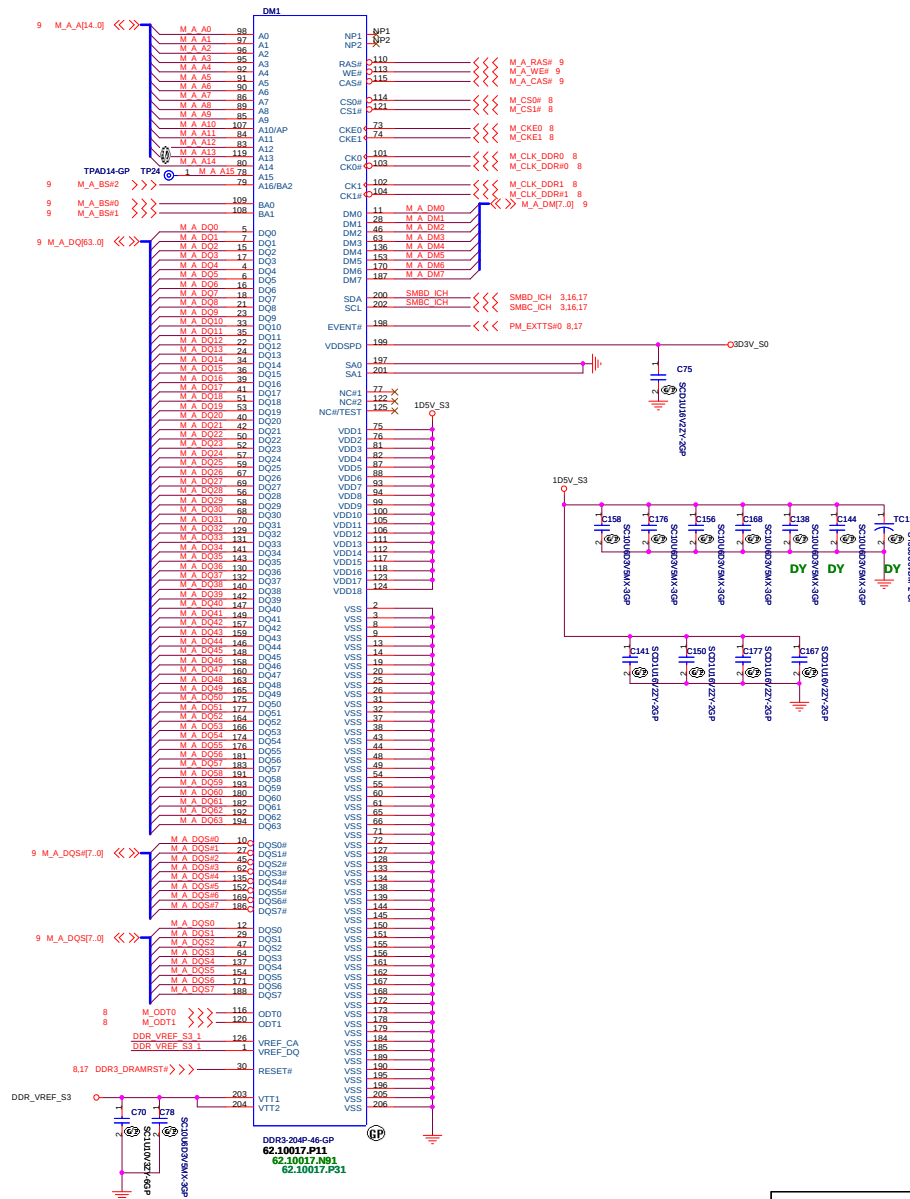
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Size Document Number JM41 Discrete Rev -1
Date: Monday, April 06, 2009 Sheet 15 of 48



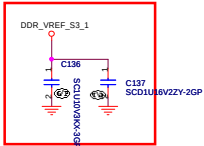
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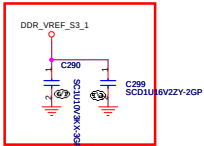
DDR3 SOCKET_2



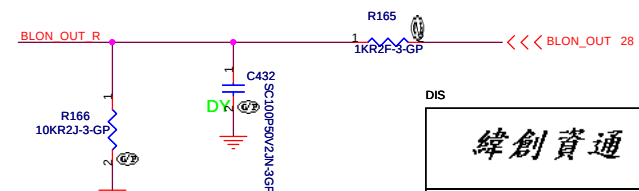
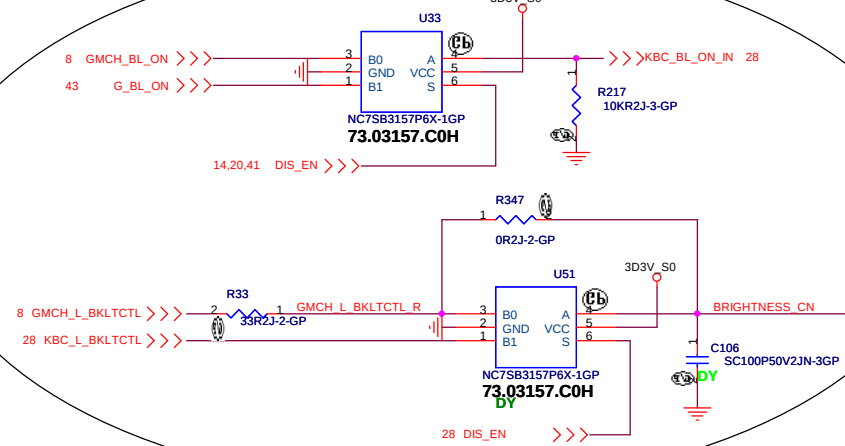
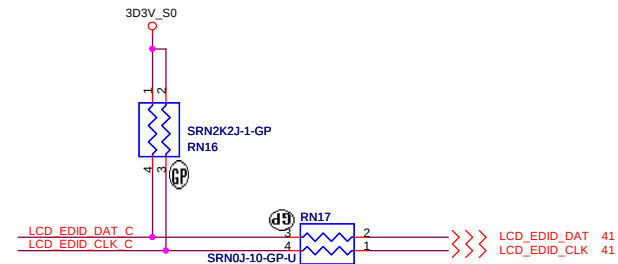
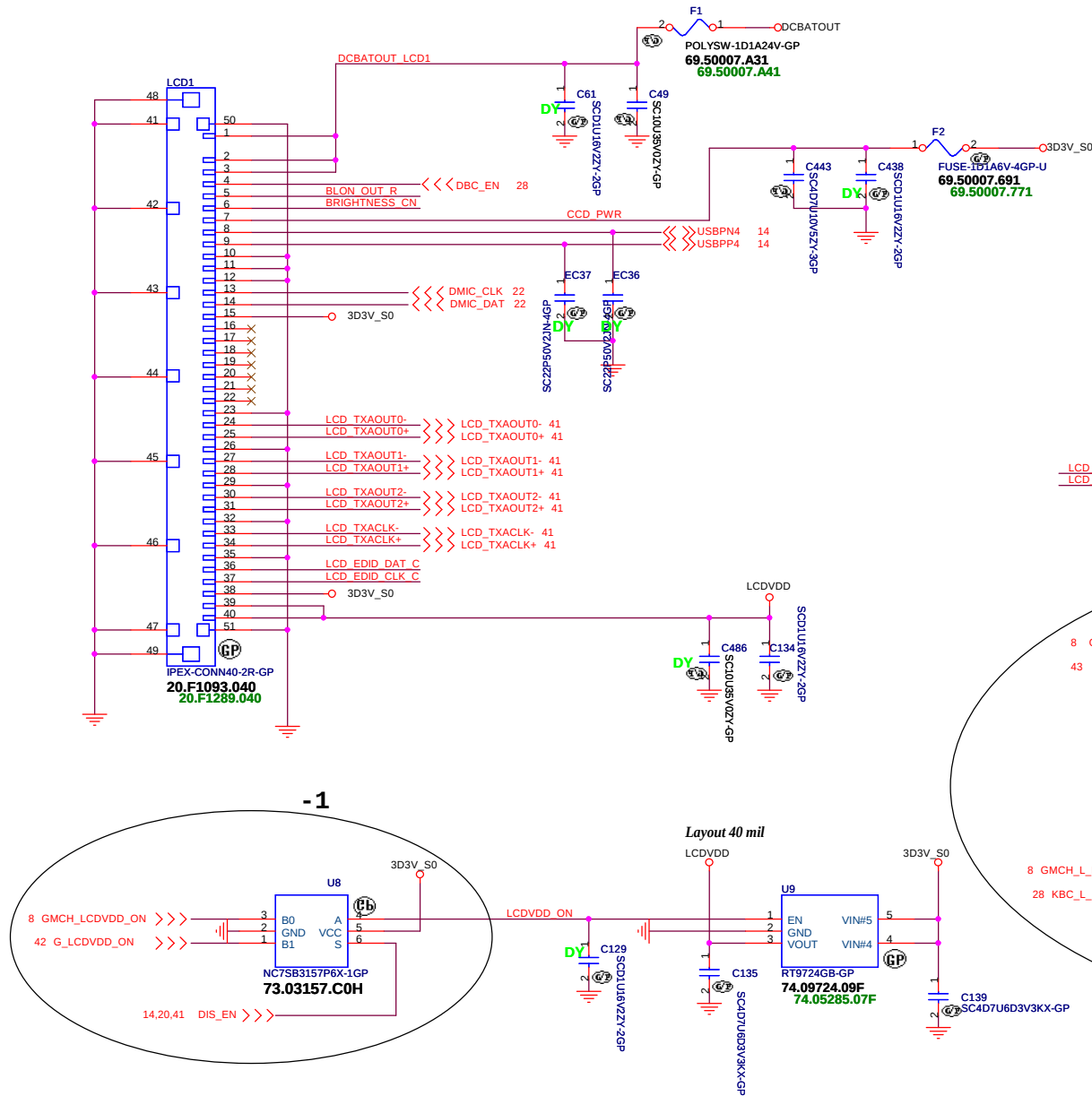
Layout Note : Near Pin 126



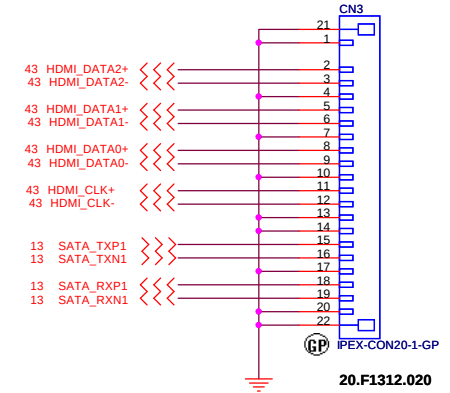
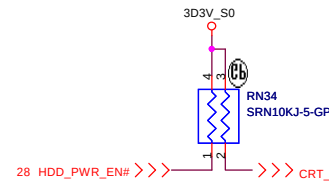
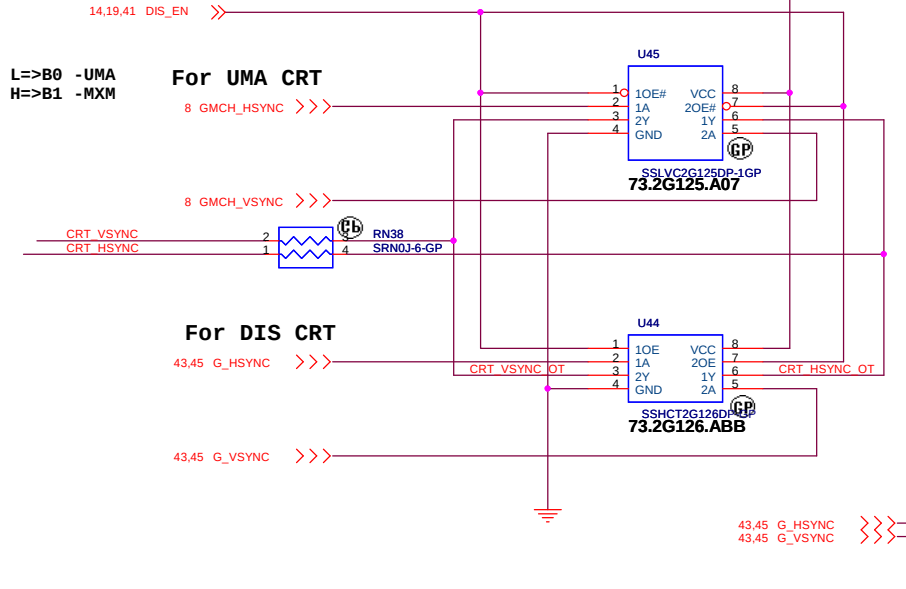
Layout Note : Near Pin 1



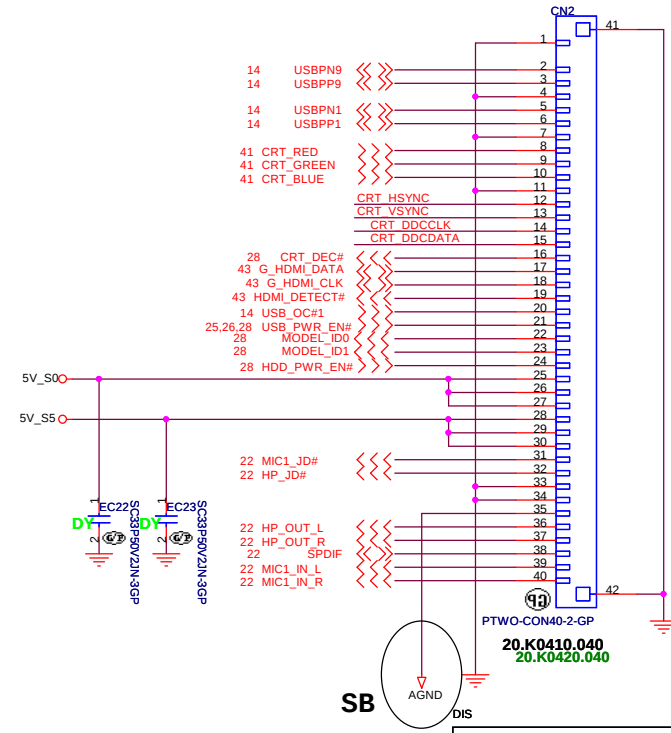
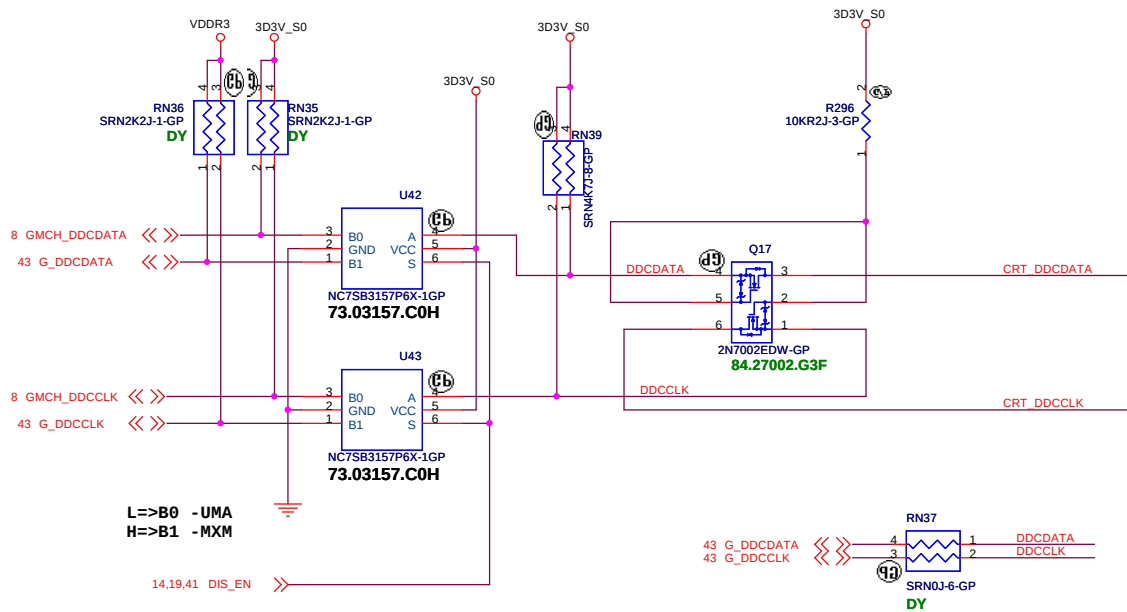
Internal MIC



Hsync & Vsync level shift

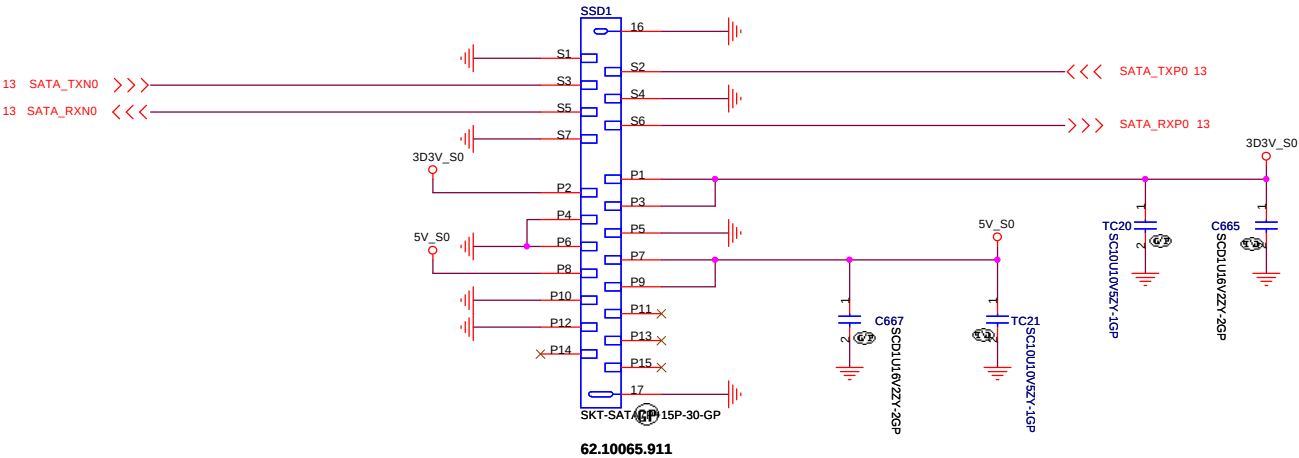


DDC_CLK & DATA level shift

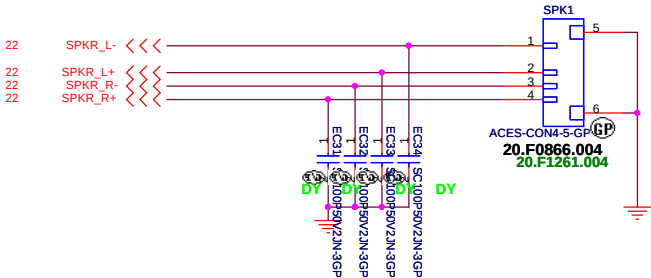


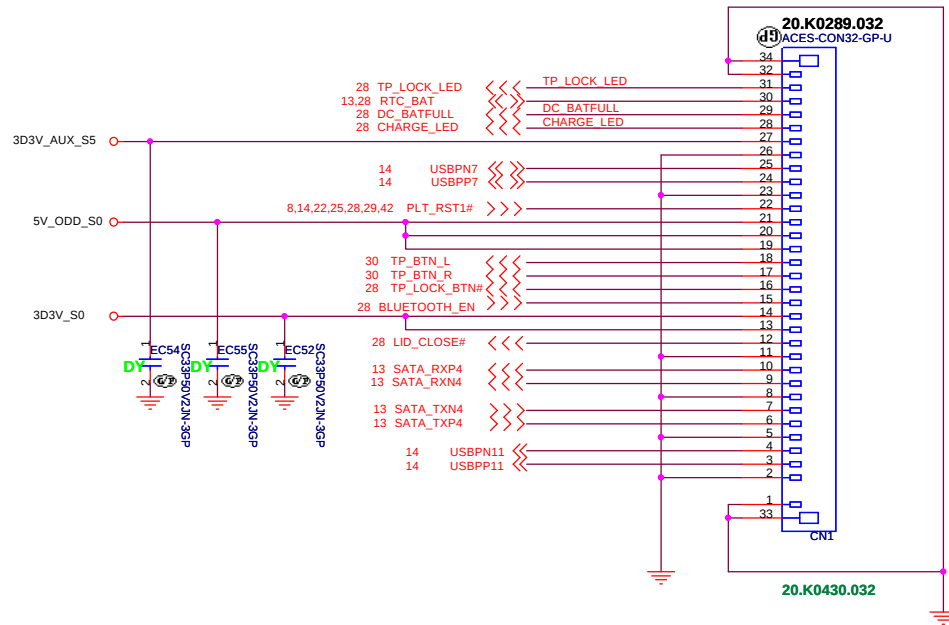
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SSD SATA Connector



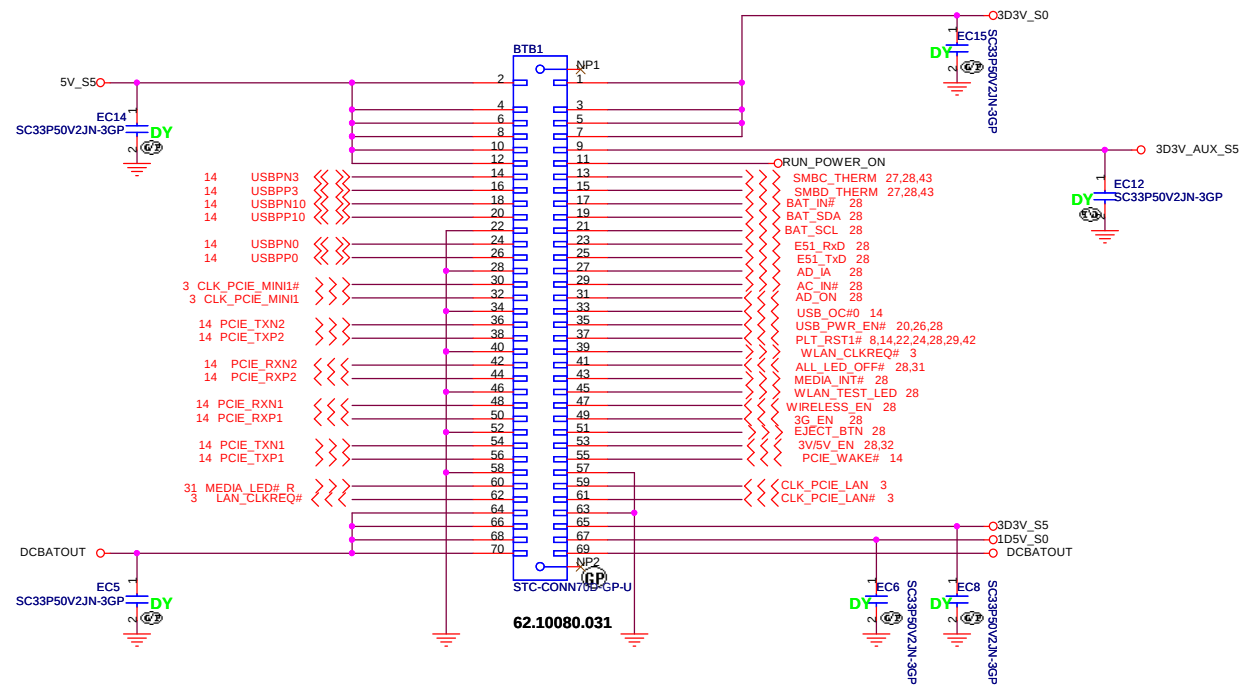
Internal Speaker





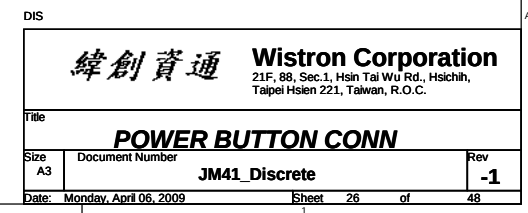
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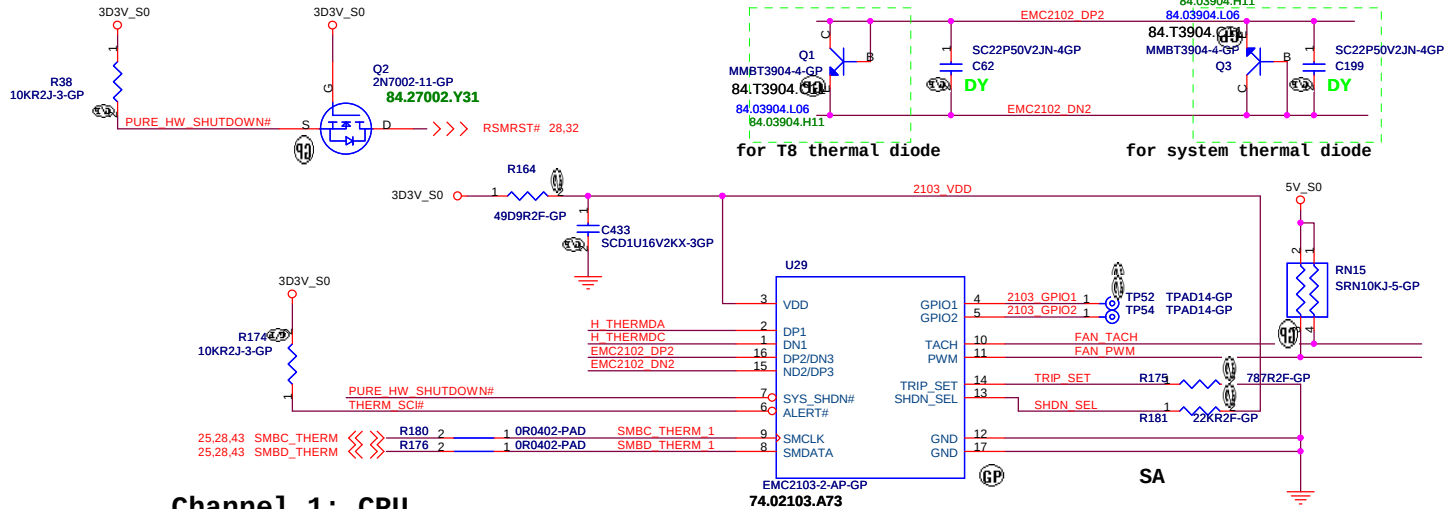
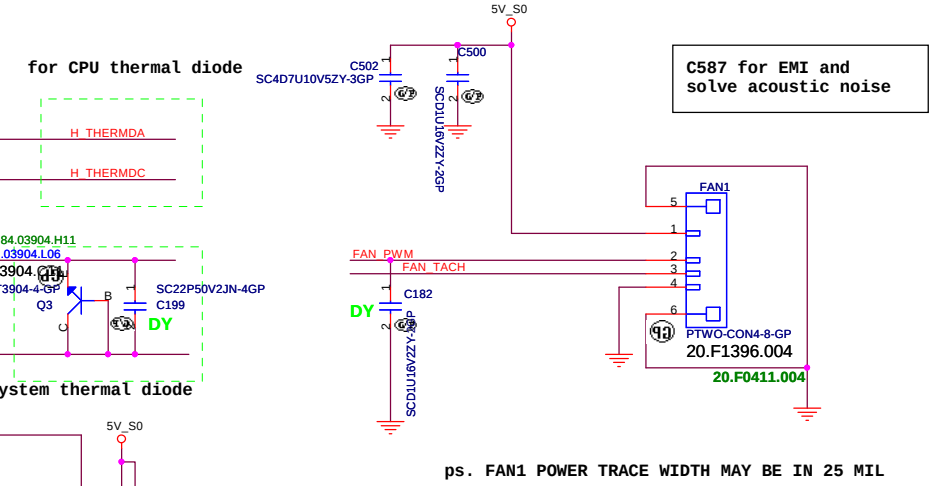
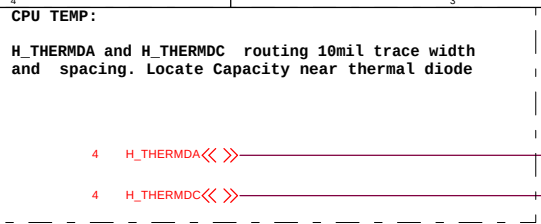
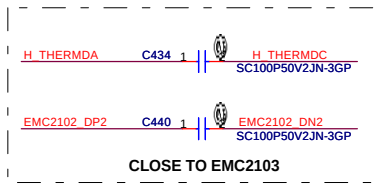
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Cardreader BD Conn			
Size	Document Number	Rev	
		-1	
Date: Thursday, April 09, 2009	Sheet 24 of 48		



DIS

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
MINI BD CONN		
Size	Document Number	Rev
A3	JM41_Discrete	-1
Date:	Monday, April 06, 2009	Sheet 25 of 48





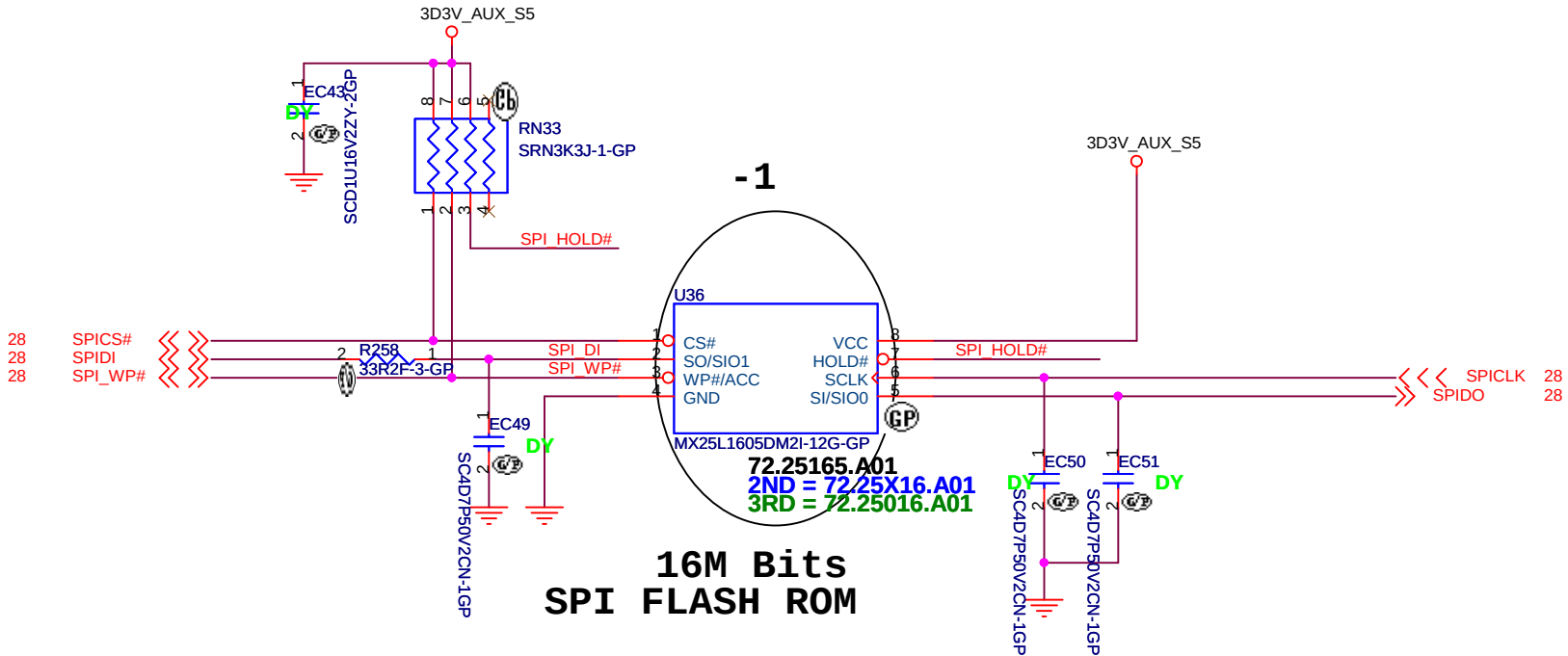
Channel 1: CPU
Channel 2: Palmrest
Channel 3: T8

SHDN SEL

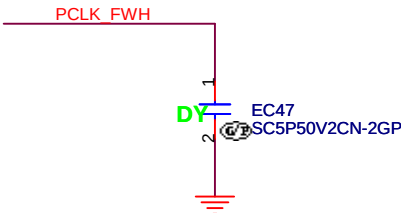
PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED, REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED, REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED

TRIP SET

Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100



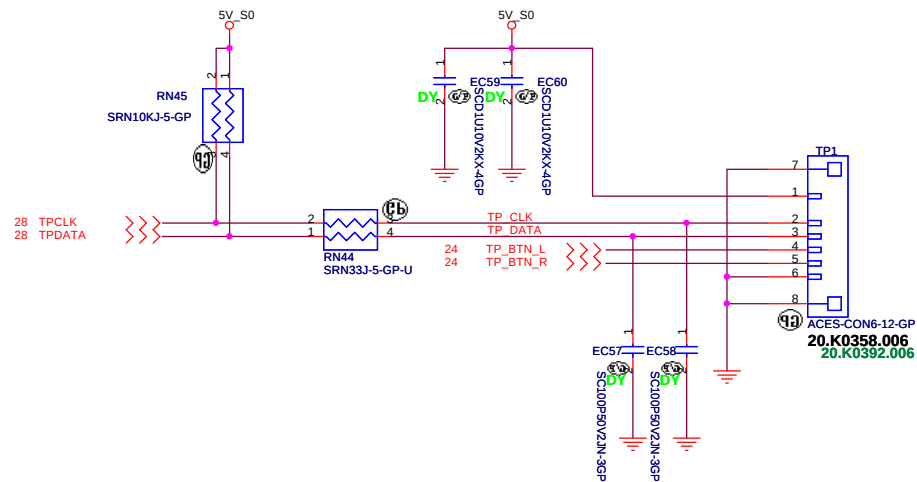
GOLDEN FINGER FOR DEBUG BOARD



DIS

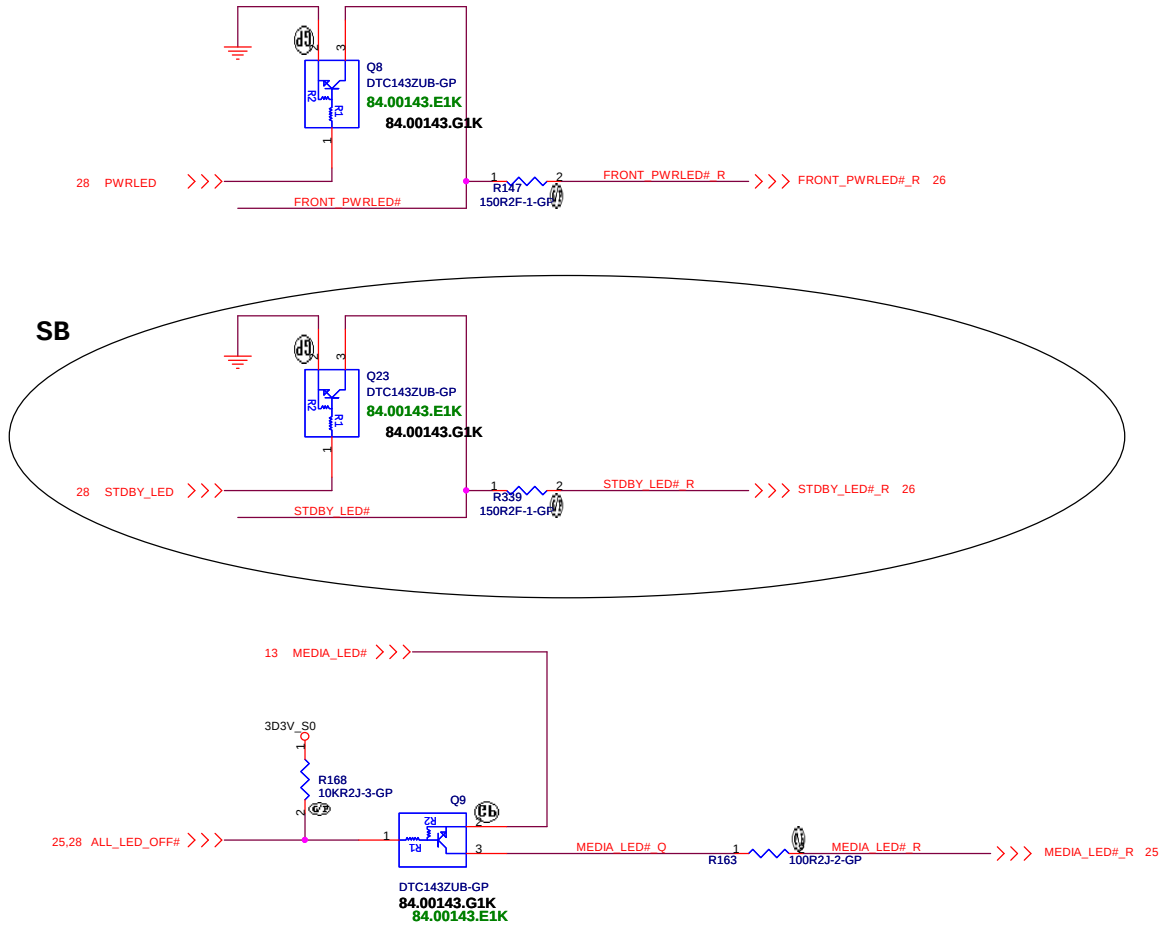
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
BIOS			
Size	Document Number		Rev
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TOUCH PAD

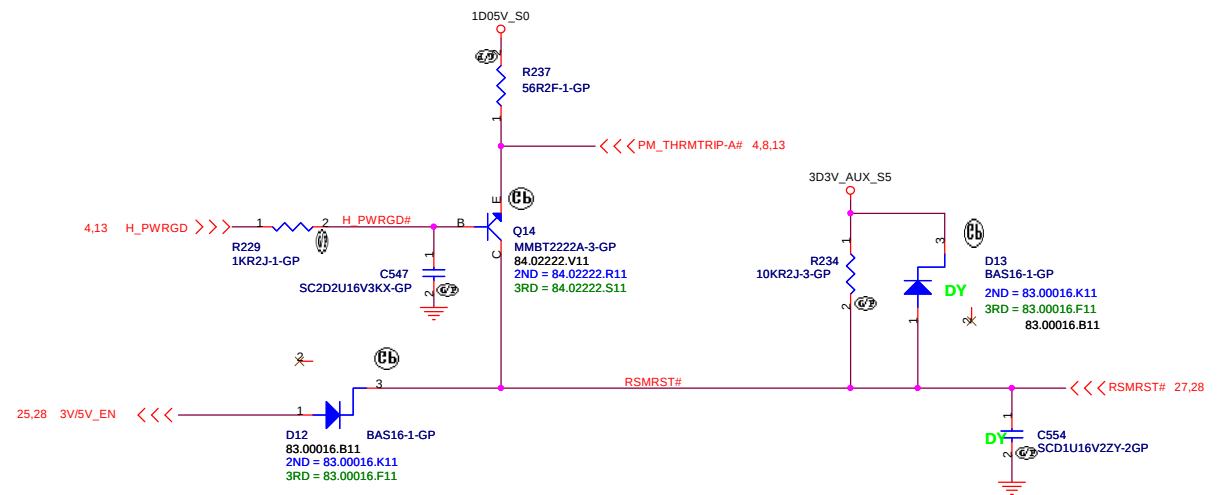
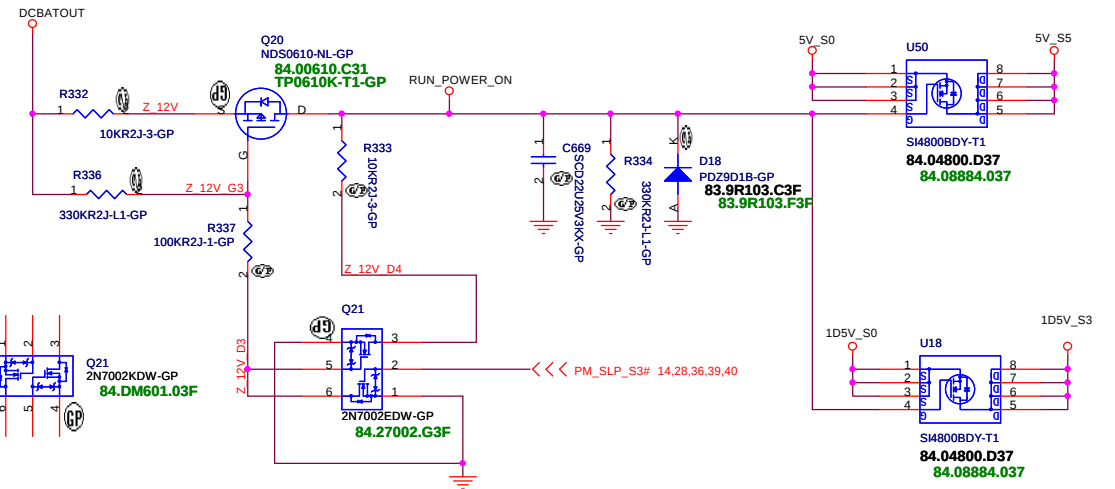


DIS

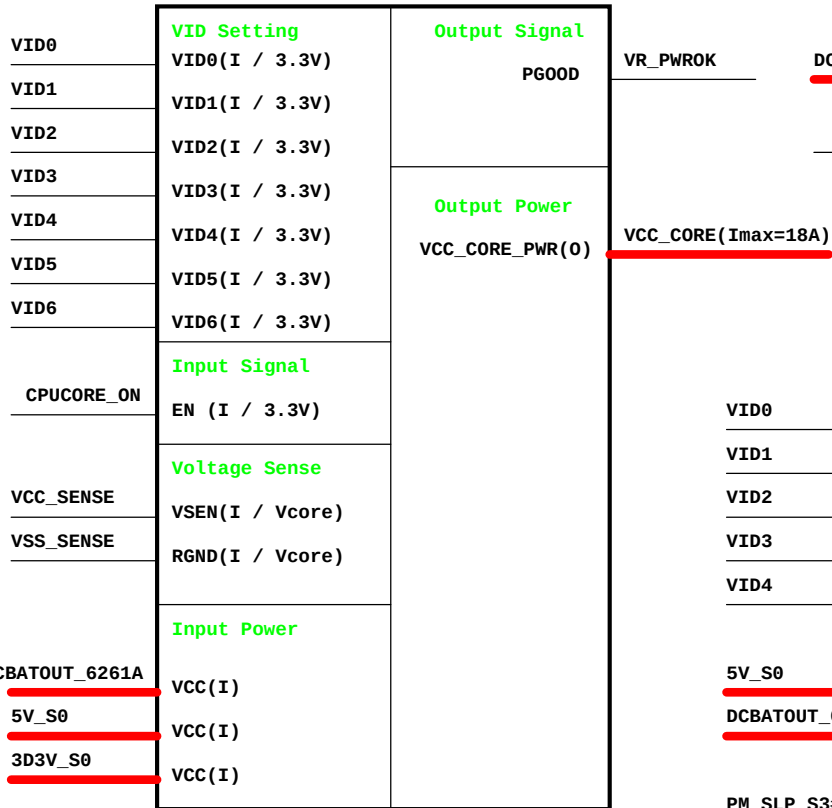
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Title Touch PAD			
Size	Document Number		Rev
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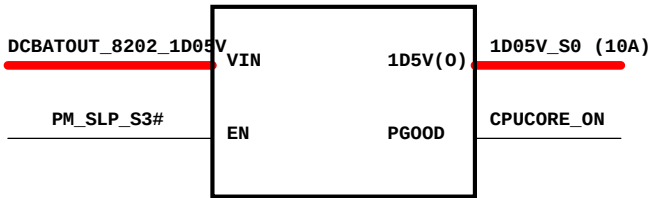
Run Power



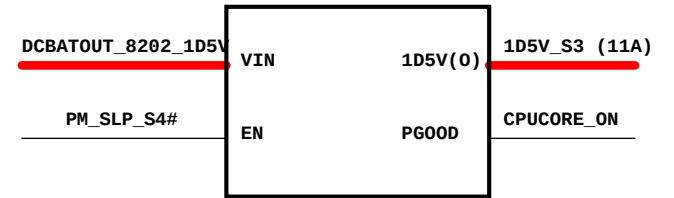
CPU_CORE
ISL6261A



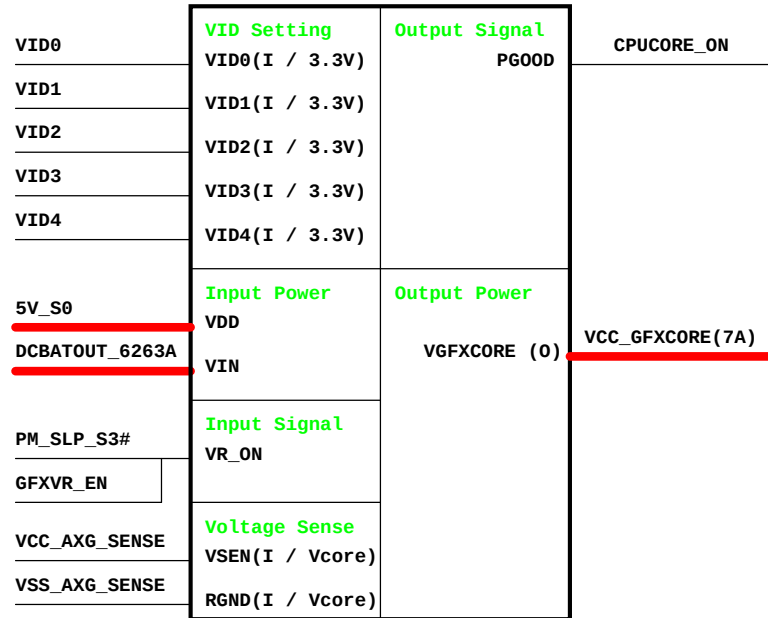
RT8202 1D05V_S0



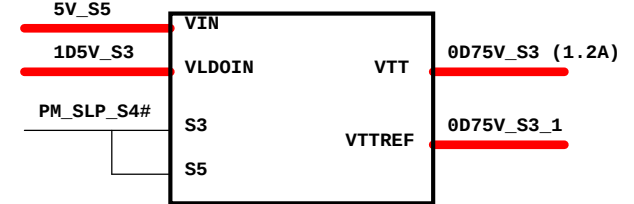
RT8202 1D5V_S3



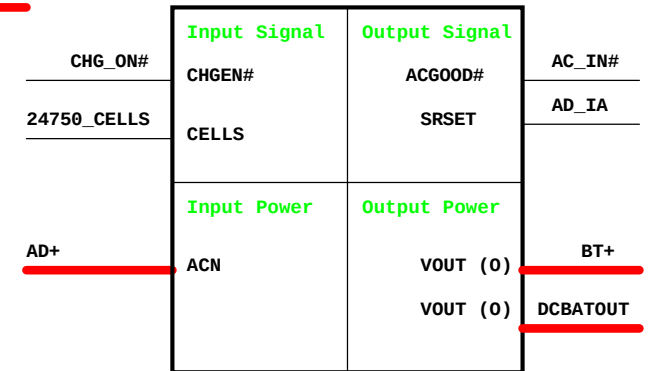
GFX_CORE
ISL6263A



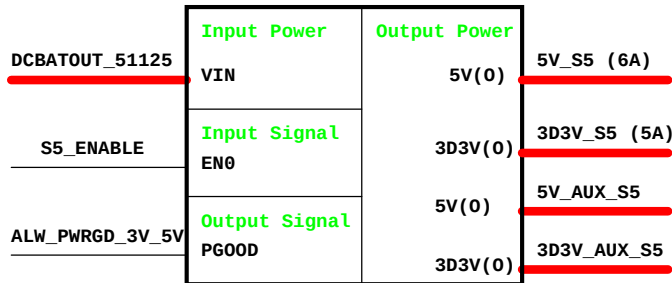
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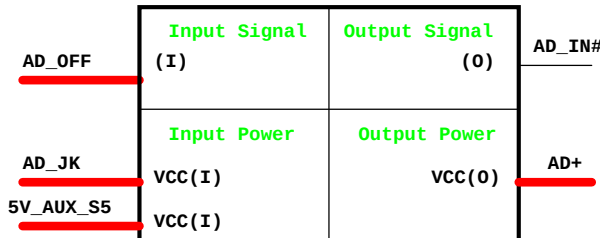
Charger MAX8731A



TPS51125
5V/3D3V



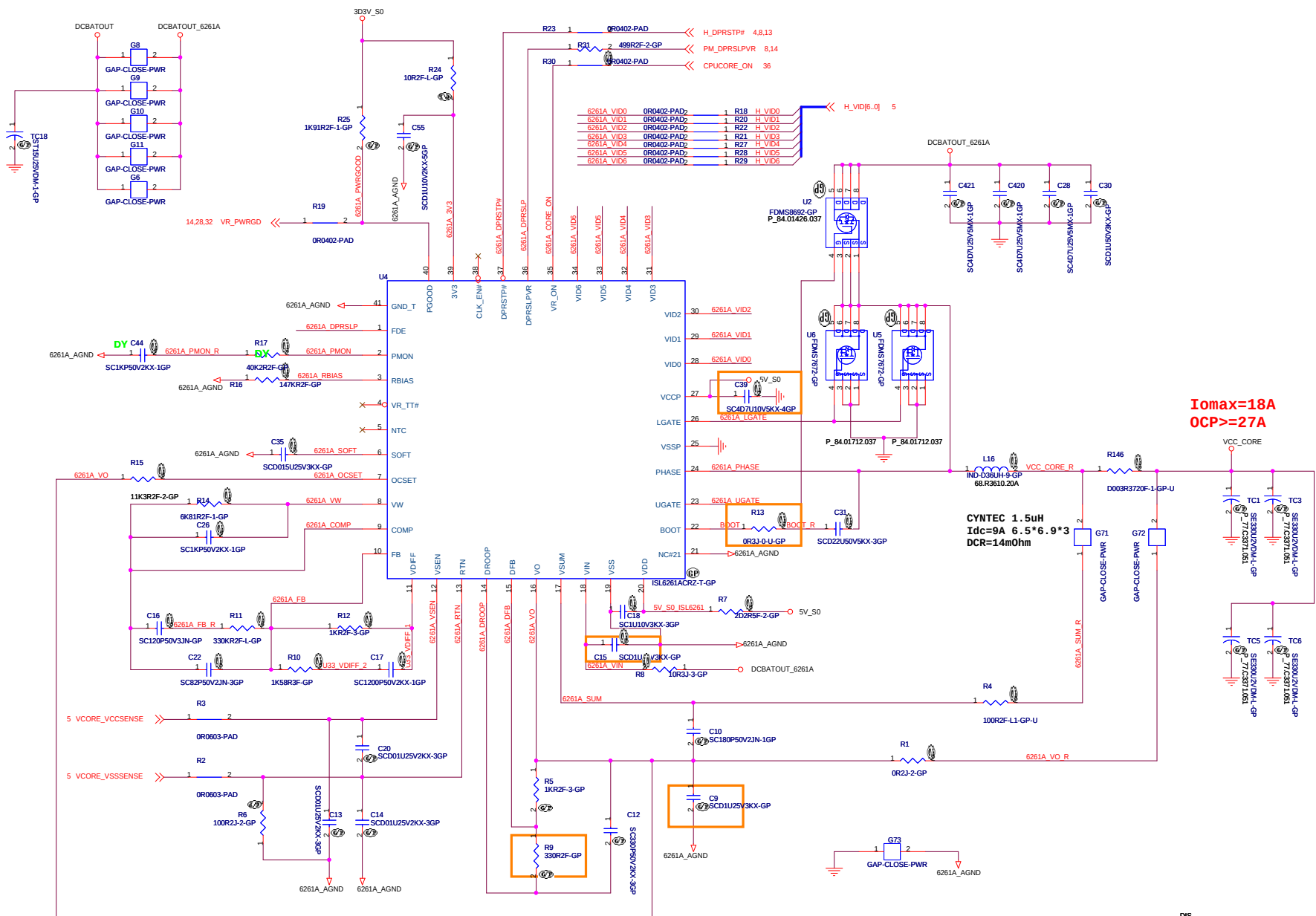
Adapter



緯創資通

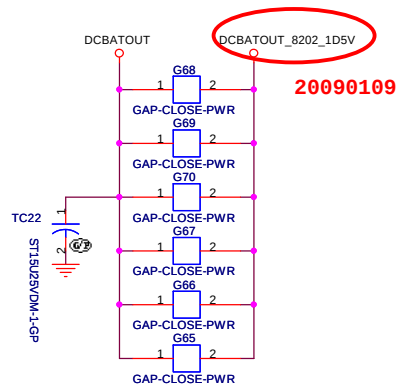
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Power Sequence Logic		
Size B	Document Number	Rev
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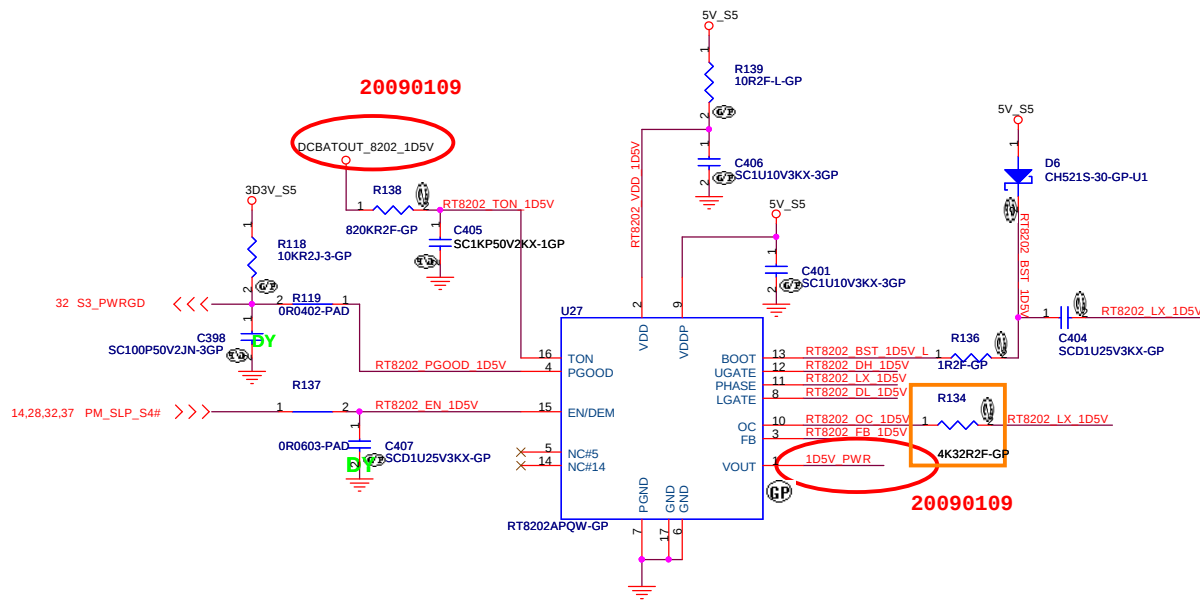
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OCP>=27A

DIS

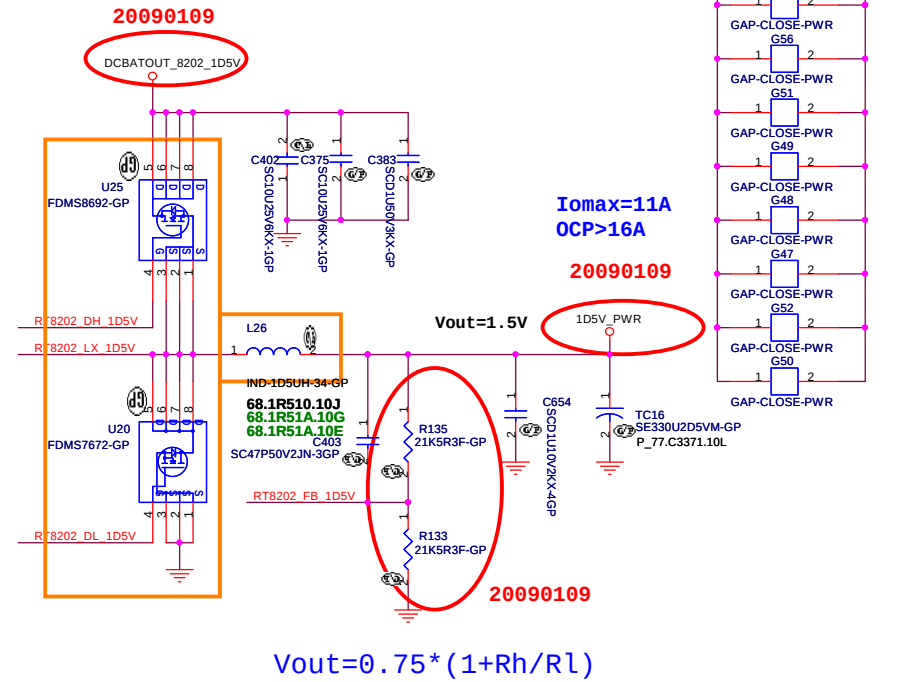


20090109

DCBATOUT_8202_1D5V



20090109



$I_{omax}=11A$
 $OCP>16A$

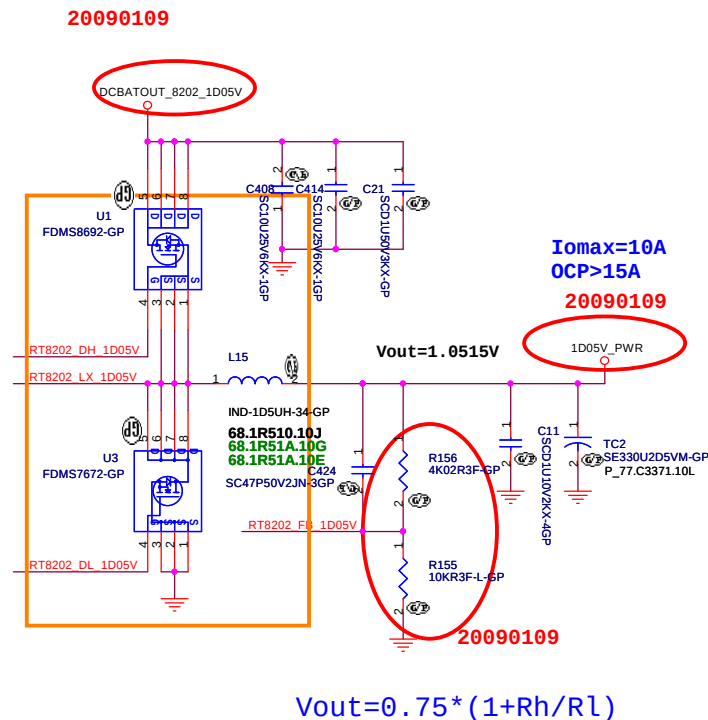
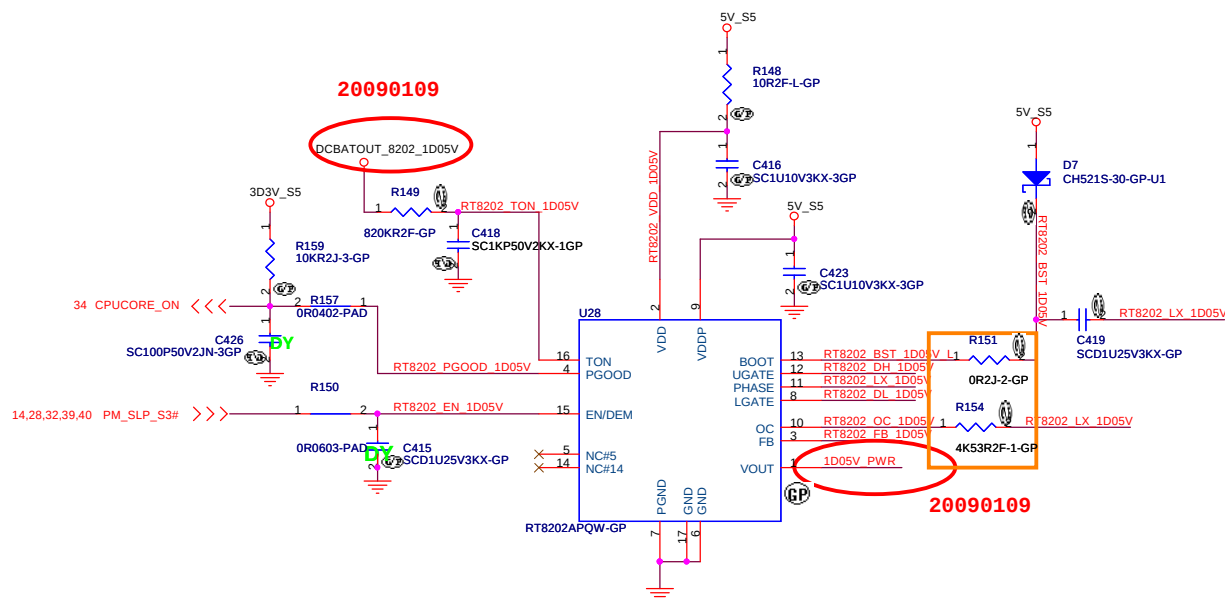
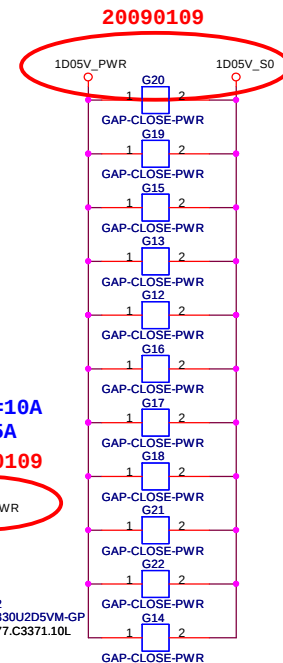
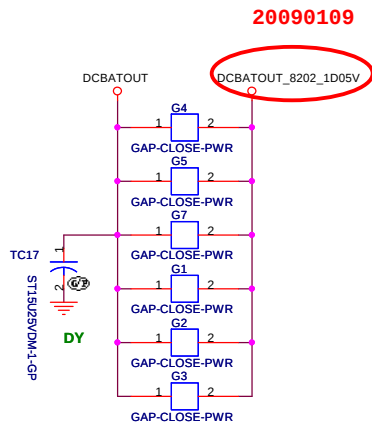
20090109

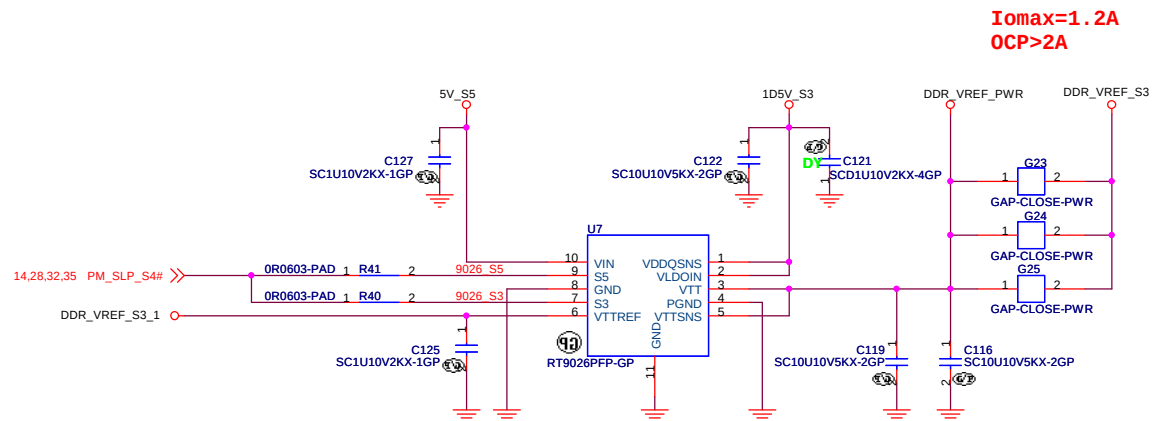
$$V_{out}=0.75*(1+R_h/R_l)$$

DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

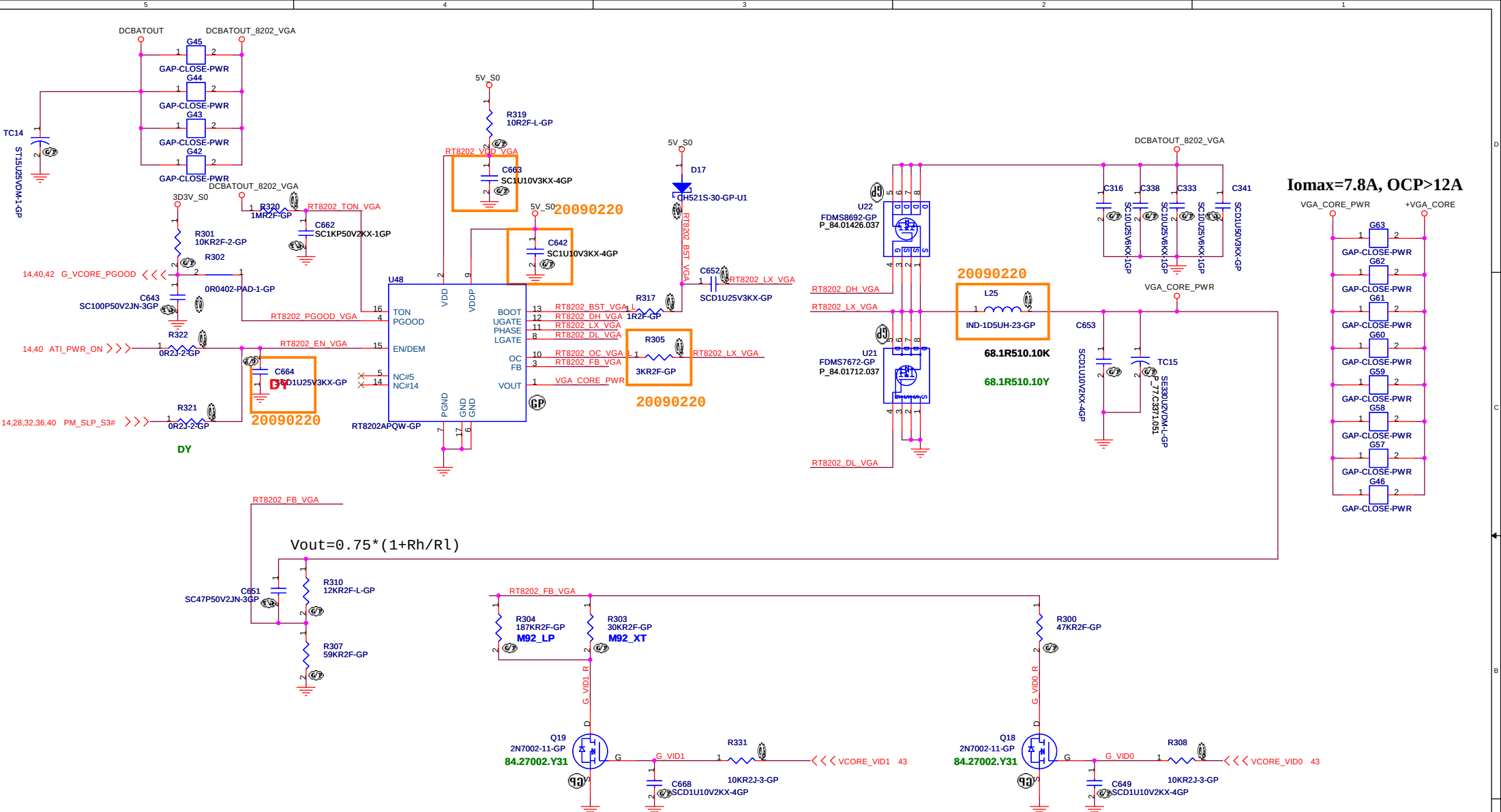
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Size	Document Number	JM41 Discrete		Rev
A3				-1
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DIS

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		RT9026 0D75V	
Size A3	Document Number	JM41 Discrete	Rev -1
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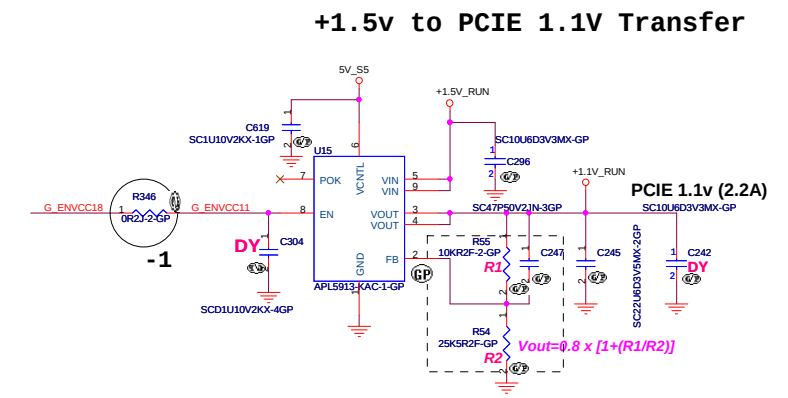
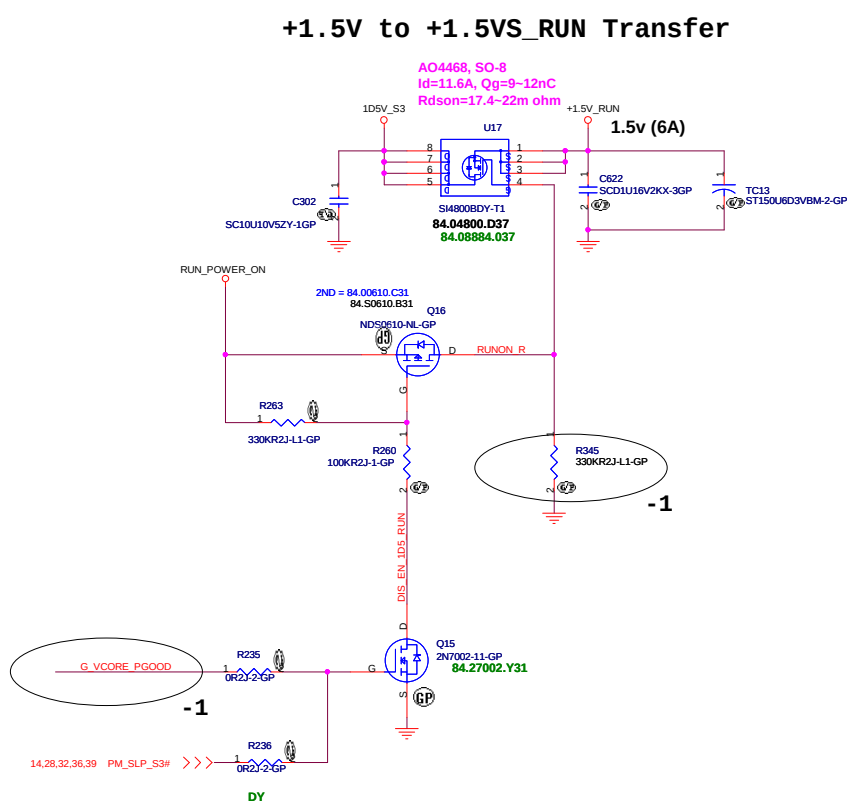
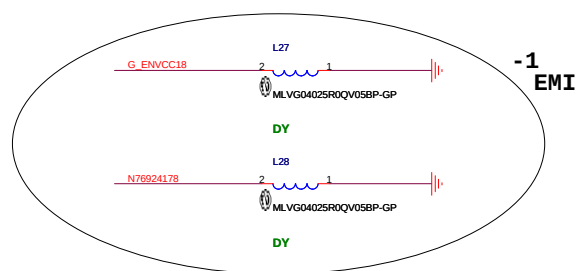
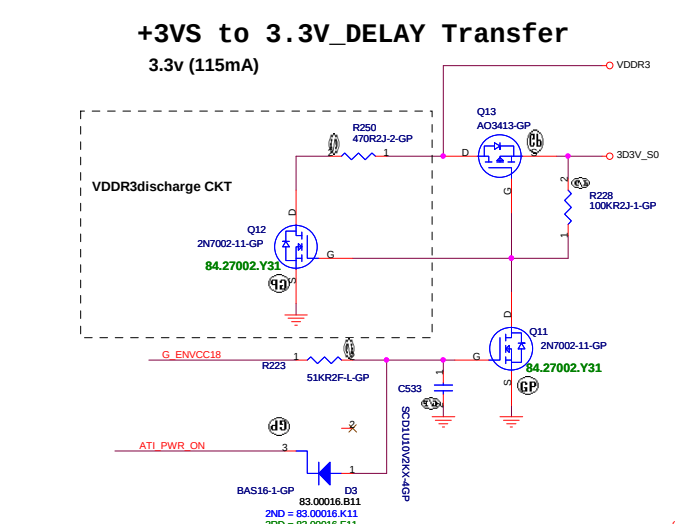
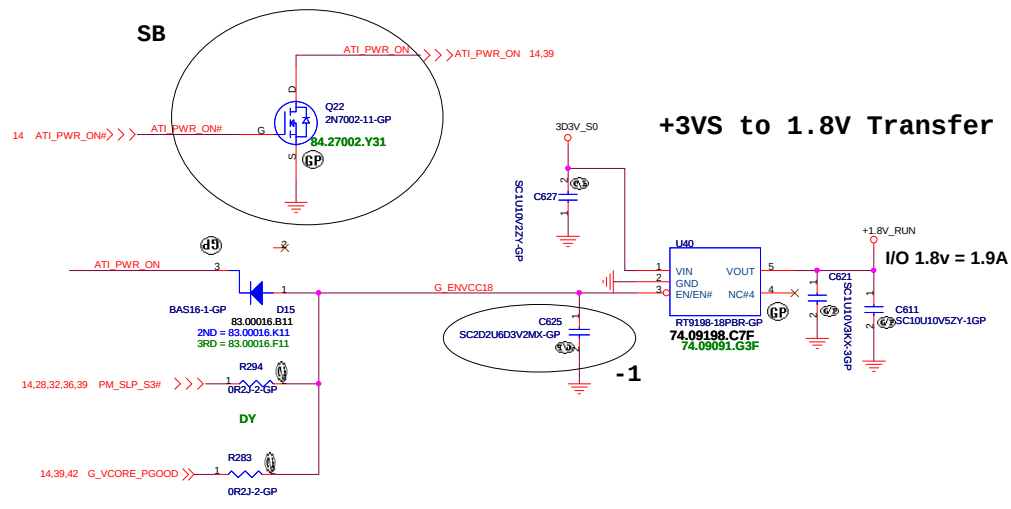


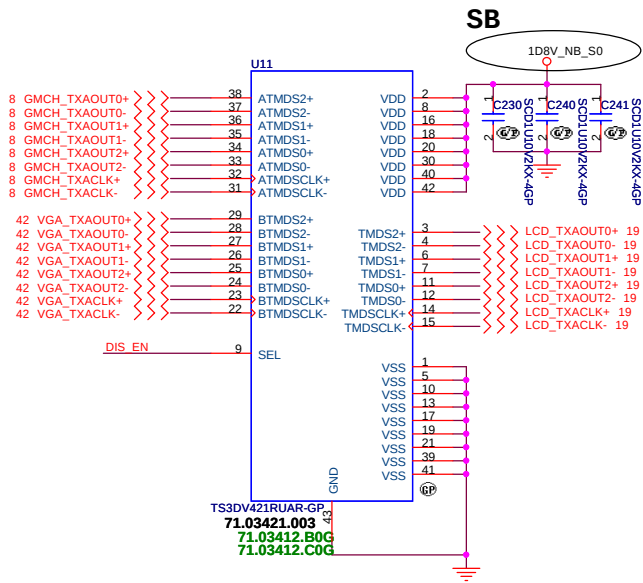
$$V_{out} = 0.75 * (1 + R_h / R_l)$$

M92_LP core power		
ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	0.95V

M92_XT core power		
ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	1.2V

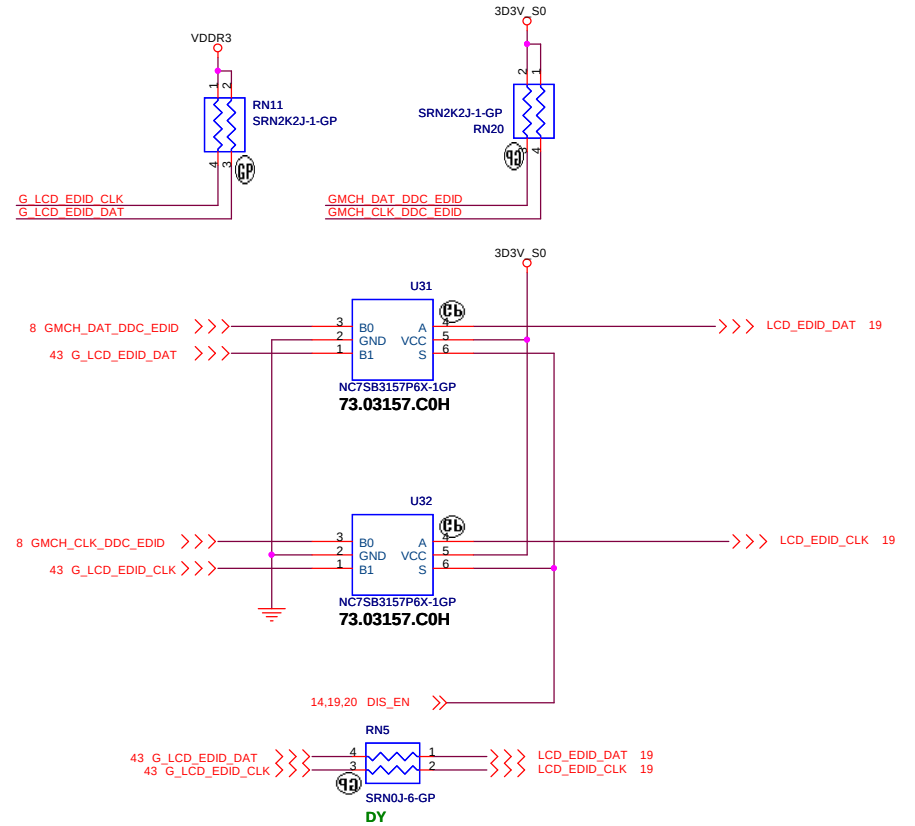
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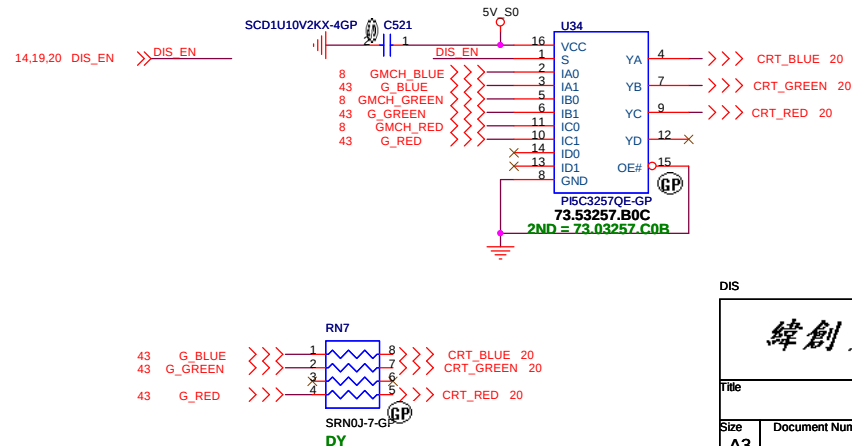
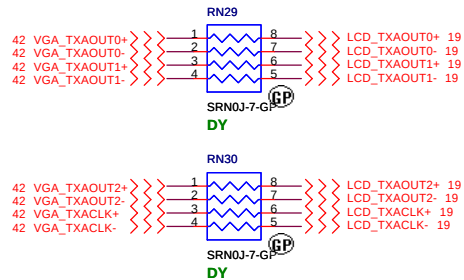


FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

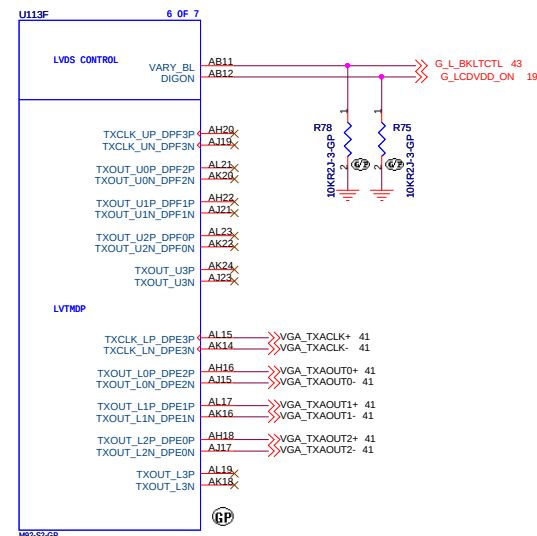
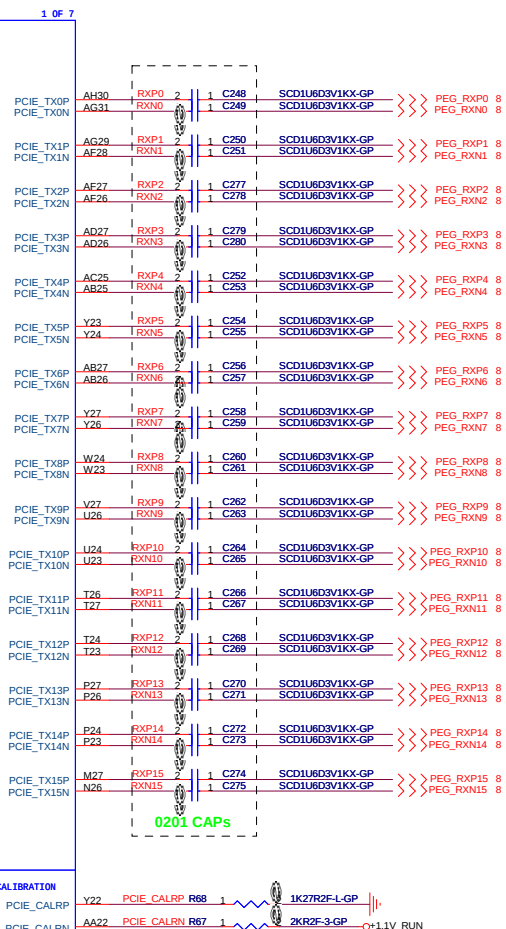
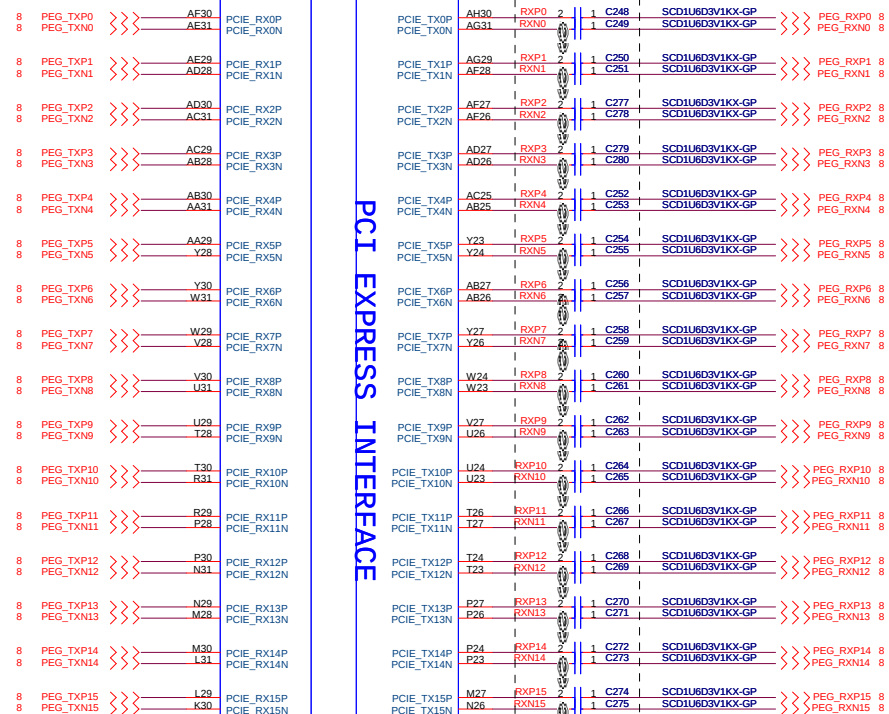


$\bar{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



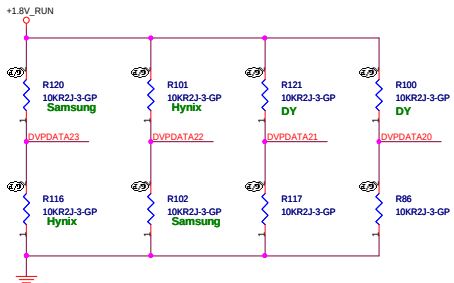
DIS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
PX SWITCH	
Size	Document Number
A3	
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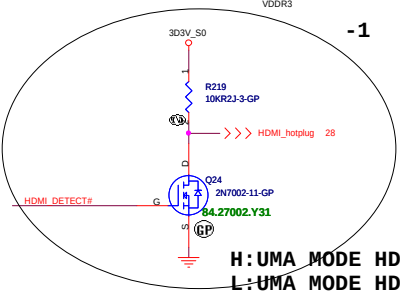
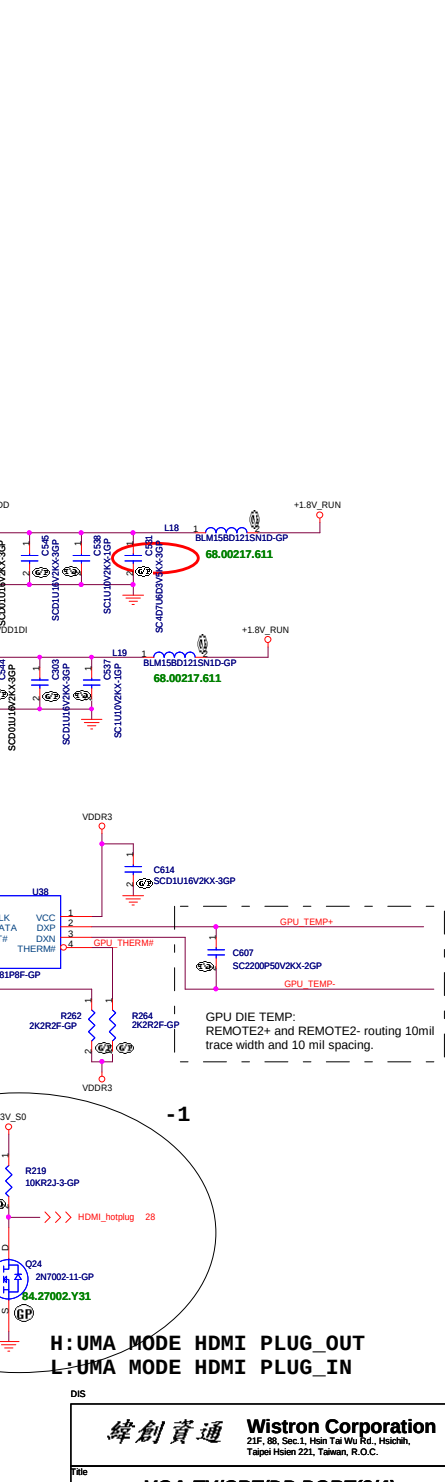
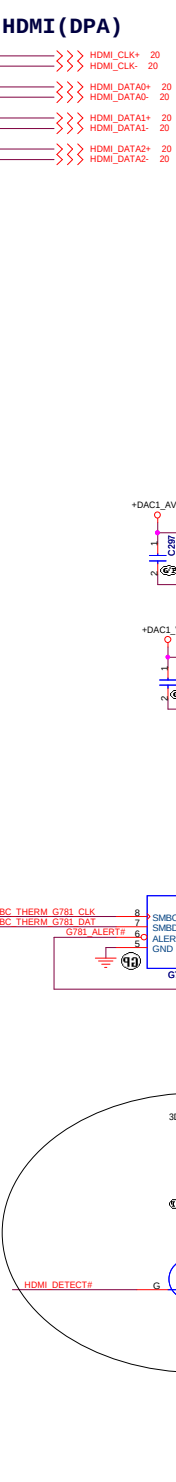
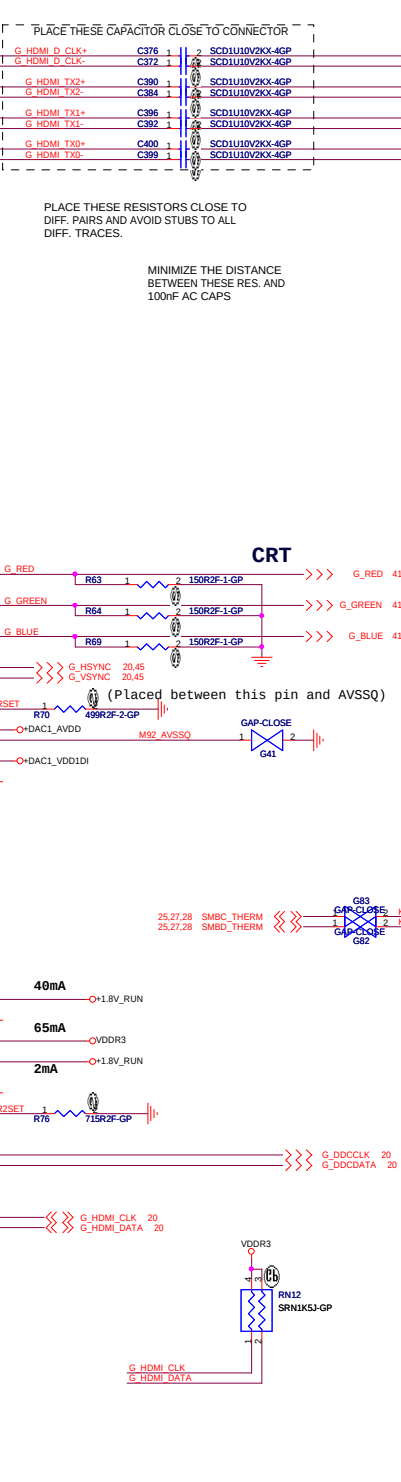
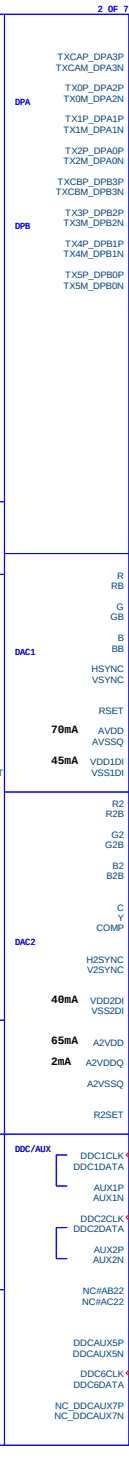
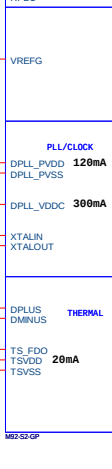
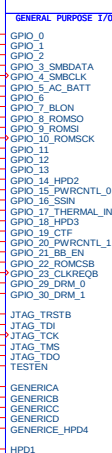
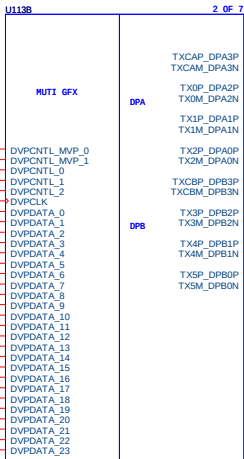
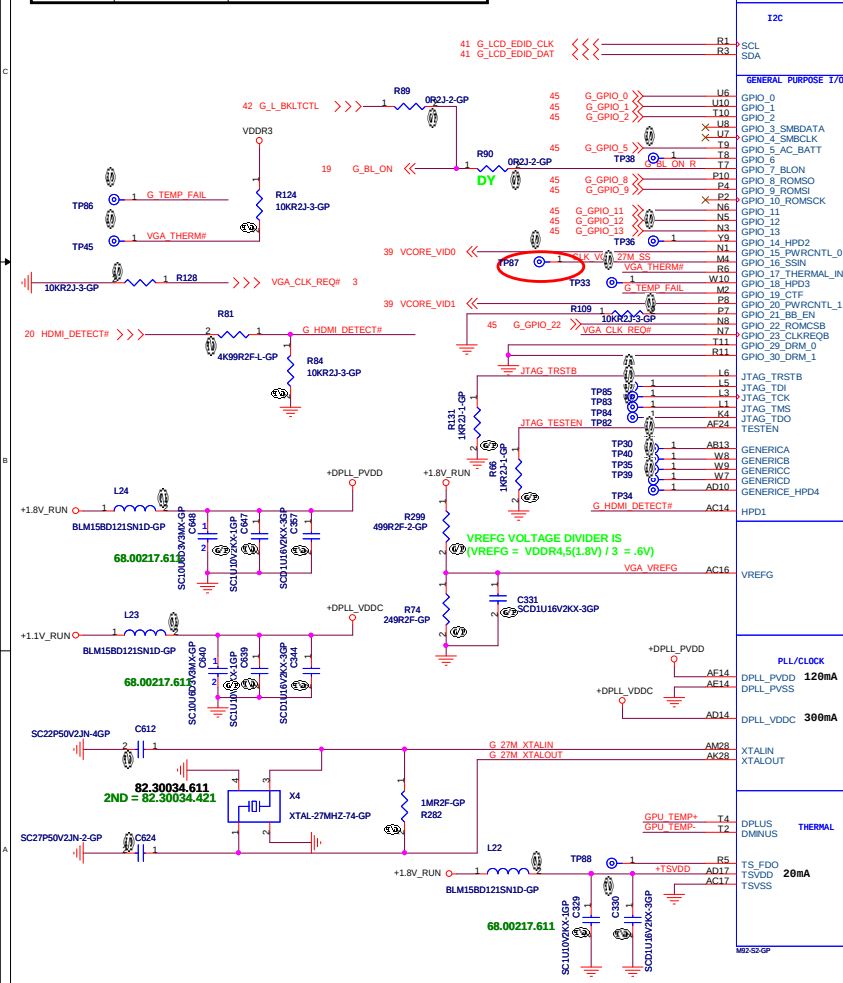


SSID = VIDEO

```
DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung
```

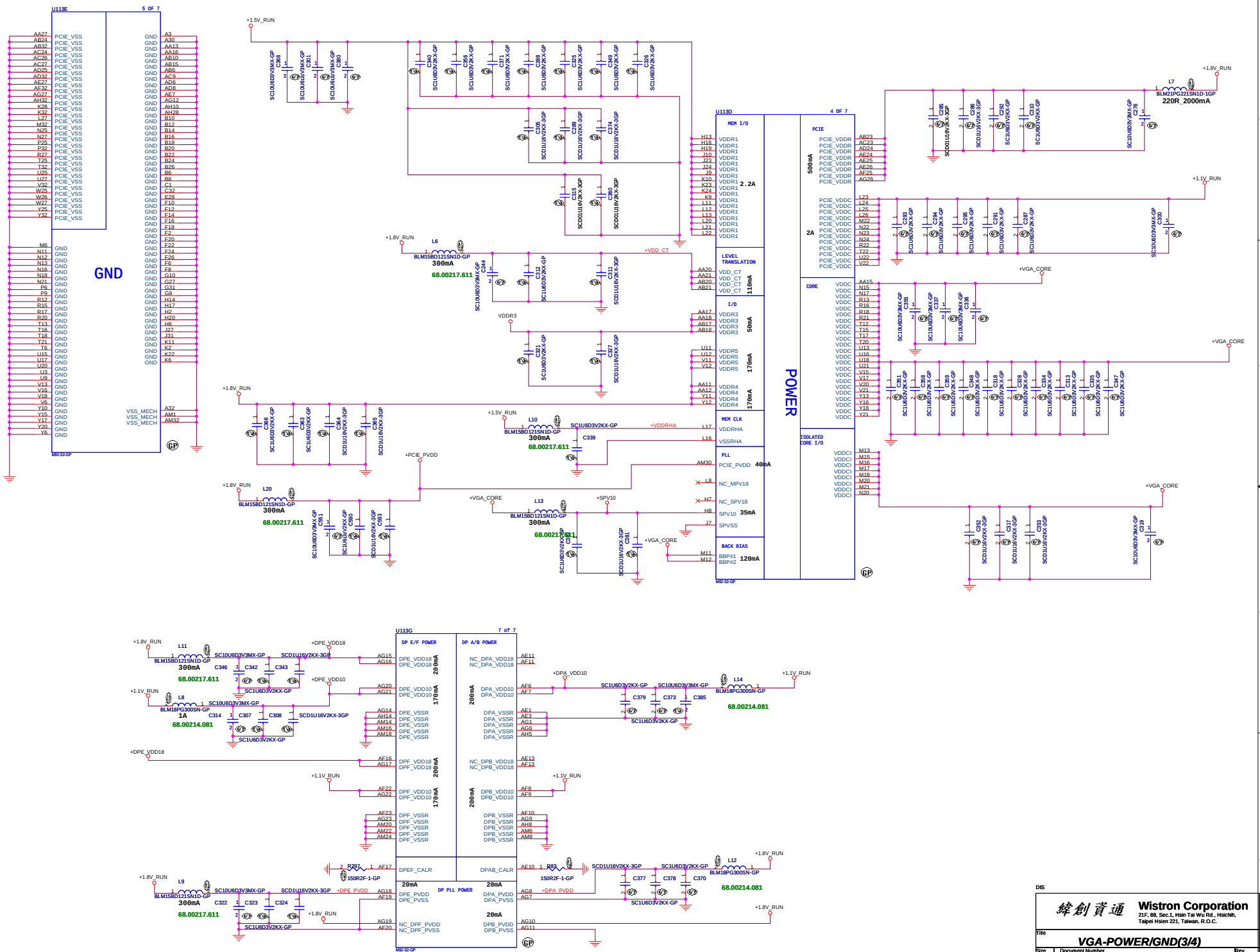


STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPPDATA(23:20) (Internal PD)	MEMORY TYPE, MAKE AND SIZE INFO 0000 - GDDR3 16Mx32 Qimonda 0001 - GDDR3 32Mx32 Hynix 0010 - GDDR3 32Mx32 Qimonda 0011 - GDDR3 32Mx32 Samsung

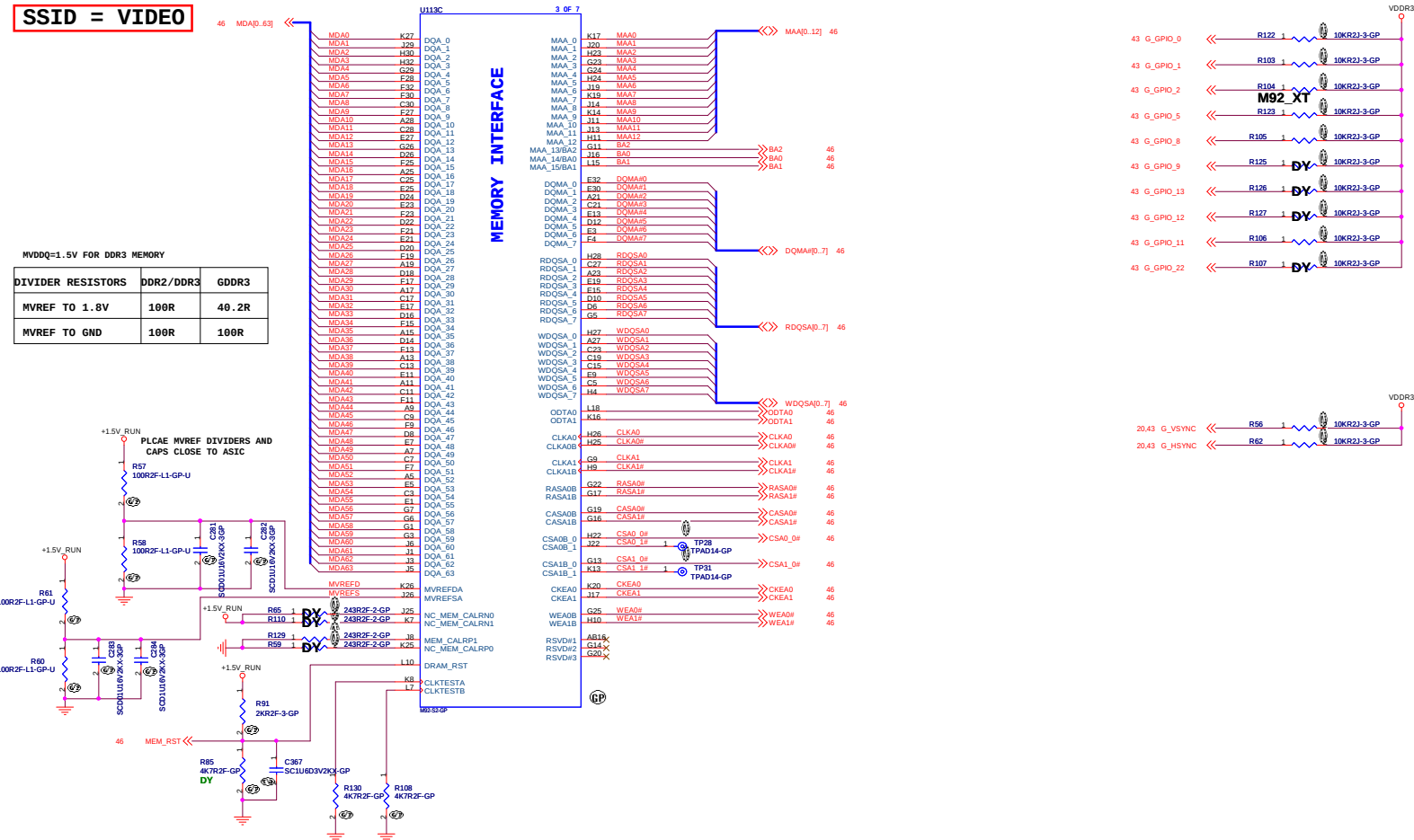


```
H:UMA MODE HDMI PLUG_OUT
L:UMA MODE HDMI PLUG_IN
```


SSID = VIDEO



SSID = VIDEO



ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESE

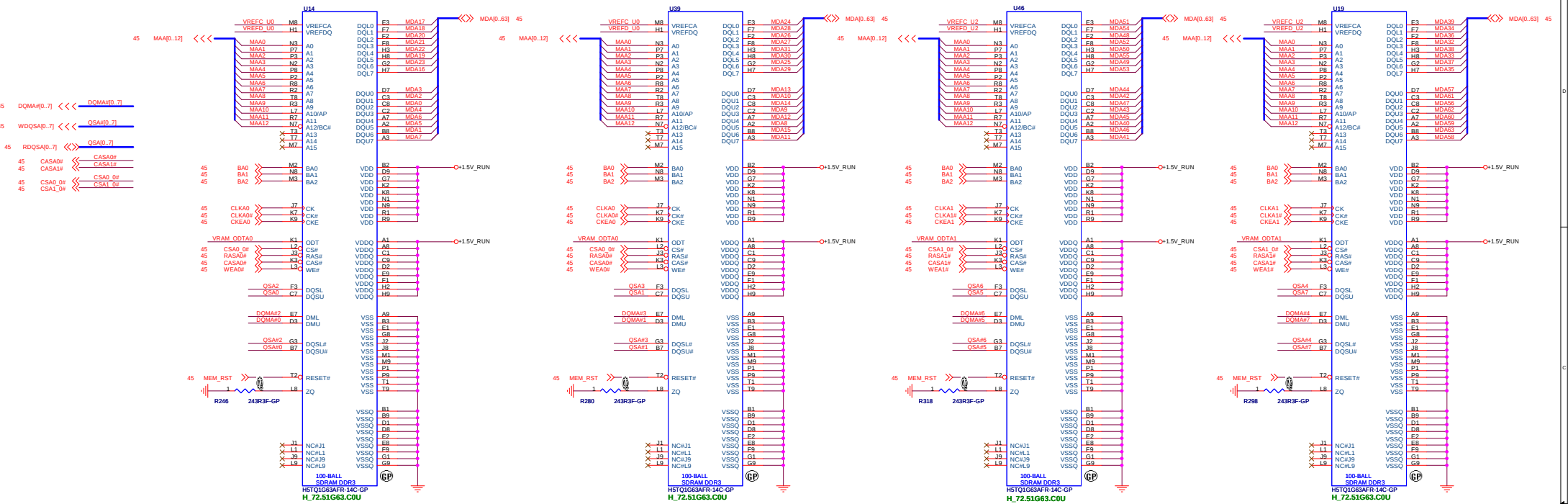
GPI03 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0			If BIOS_ROM_EN (GPIO22) = 1			
Size of the primary memory apertures			GPIO[9,13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V	128MB	x000	ST Microelectronics	M25P05A	0100	
	256MB	x001		M25P10A	0101	
	64MB	x010		M25P20	0101	
	32MB	x		M25P40	0101	
	512MB	x	M25P80	0101		
	16B	x	Chingis (formerly PMC)	Pm25LV512A	0100	
	26B	x		Pm25LV010A	0101	
	46B	x				

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPI08	Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing ✓
TX_DEEMPH_EN (Internal PD)	GPI01	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPI02	✓ 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPI08	0= Disable CLKREQ# power management capability 1= Enable CLKREQ# power management capability ✓
ROMIDCFG[3:0] (Internal PD)	GPI0[13, 12, 11]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPI0_22_ROMCSB	✓ Enable external BIOS ROM device 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI ✓

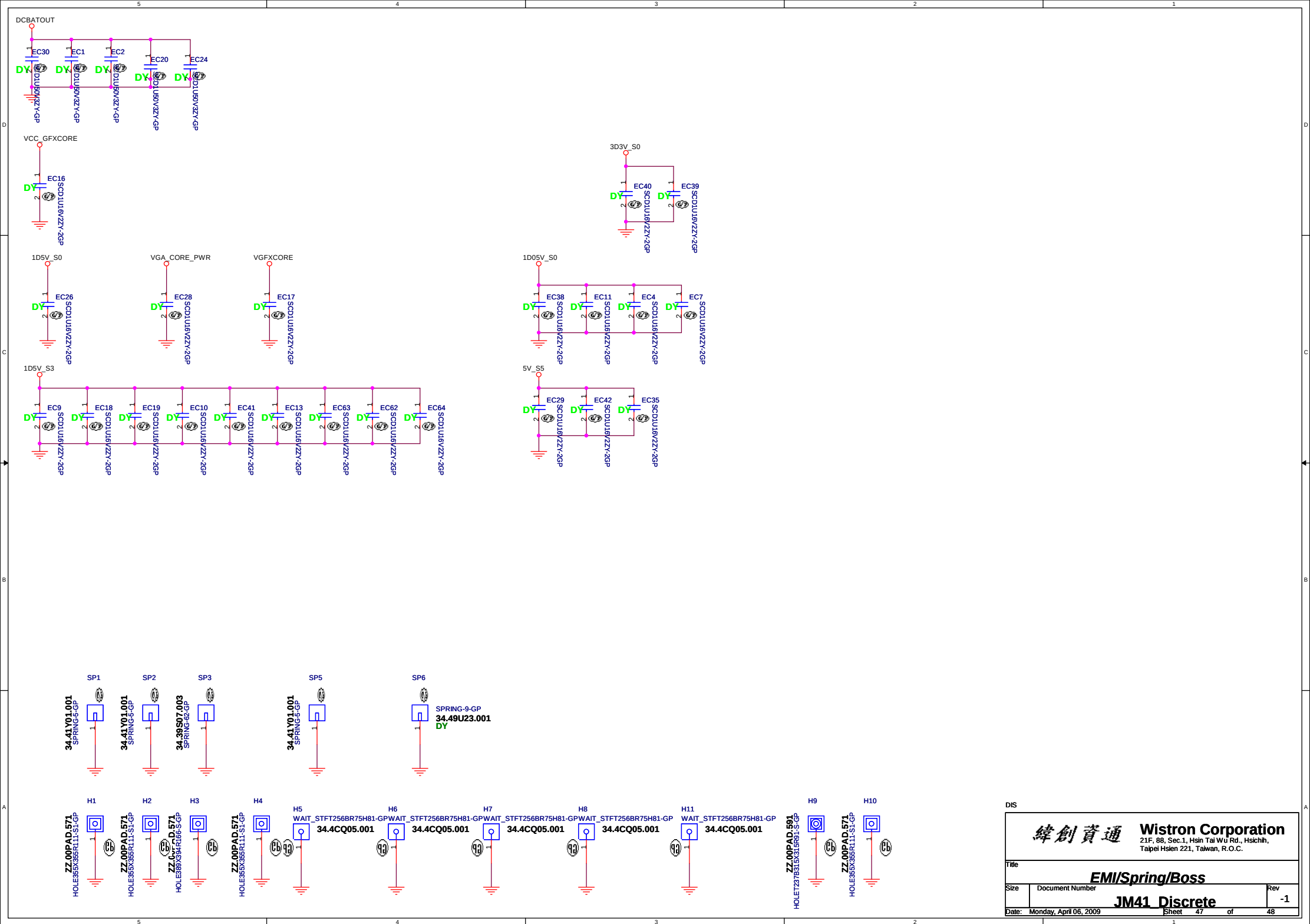
512MB DDR3



Samsung : K4W1G1646E-EC12

Hynix : H5TQ1G63BFR-12C





JM41/JM51 DIS Schematic EC Tracking Record

EC #/ Page / Description / Part Affected

EC SC01/11/connect NB1.A31 to GND(For power save)
EC SC02/14/inet DIS_EN pull high 10K to 3D3V_S0
EC SC03/20/CN2.pin35 change to AGND
EC SC04/22/R311 change to 39.2K
EC SC05/22/U24.pin2 change to AGND
EC SC06/26/BTB2.pin9 add stand by led control signal
EC SC07/28/U16.pin66 add stand by led control signal
EC SC08/28/add circuit to support green adapter
EC SC09/28/inet EJECT_BTN pull high 10K to 3D3V_S0
EC SC10/31/add circuit to stand by led control
EC SC11/40/change GPU power enable signal to ATI_PWR_ON#(low active)
EC SC12/41/change U11 power plane to 1D8V_NB_S0

DIS

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY

Size
A2

Document Number

Rev

JM41_Discrete

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Date: Wednesday, April 15, 2009

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