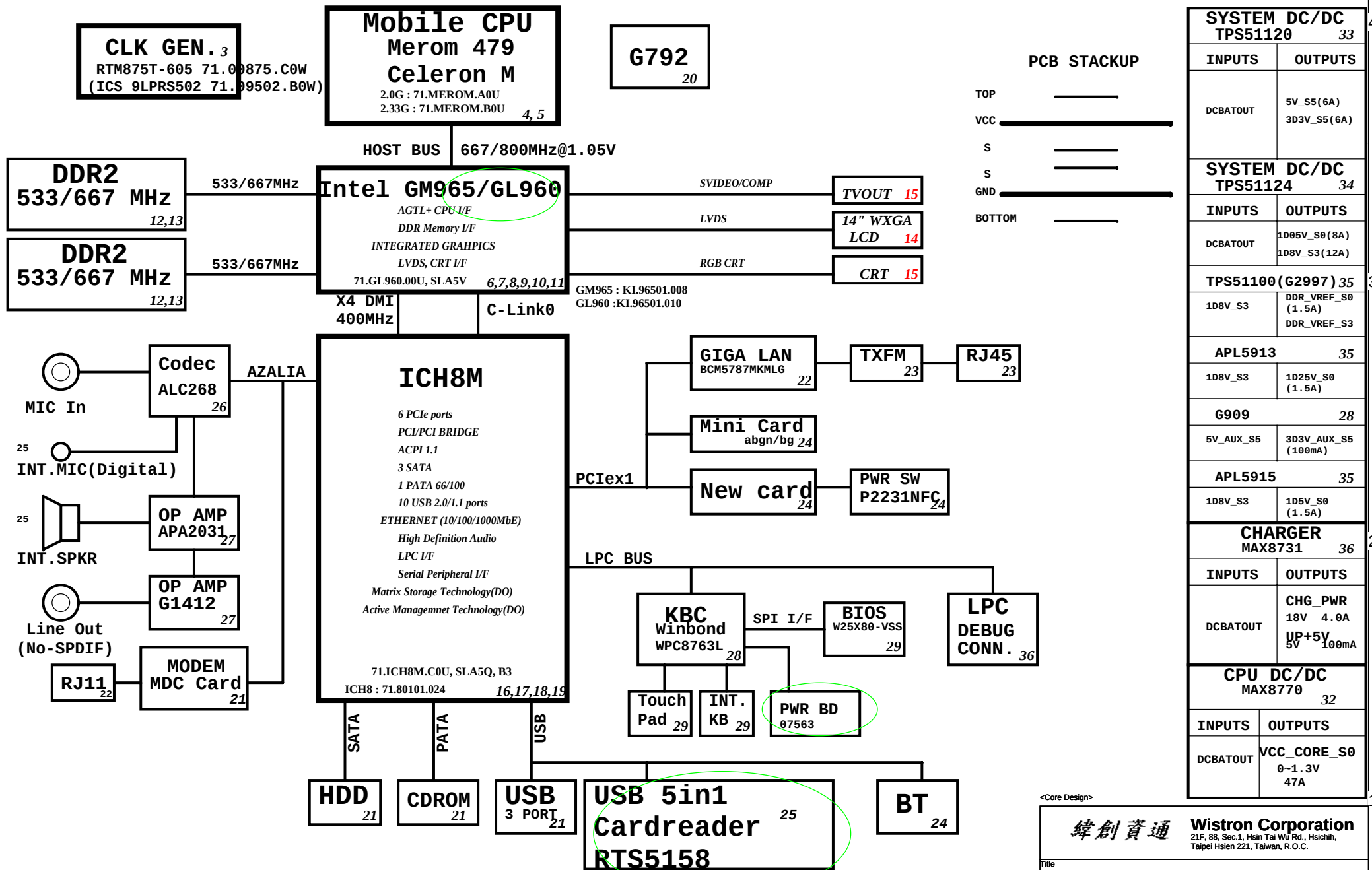


Calado Block Diagram

Project code: 91.4X401.001

PCB P/N : 07227

REVISION : -1



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

BLOCK DIAGRAM			
Size A3	Document Number	Rev	-1
Calado			
Date: Thursday, September 13, 2007	Sheet 1	of	39

ICH8M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPI020	Reserved	This signal should not be pulled high.
GNT1#/ GPI051	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSusi_05, VccSusi_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSusi_05, VccSusi_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOw#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCIE Routing

LANE1	LAN Marvell
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	BT
6	Cardreader
7	MINICARD
8	CCD
9	NEW1

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K ?
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K ?
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

Crestline Strapping Signals and Configuration

Crestline EDS 20954 1.0 page 7

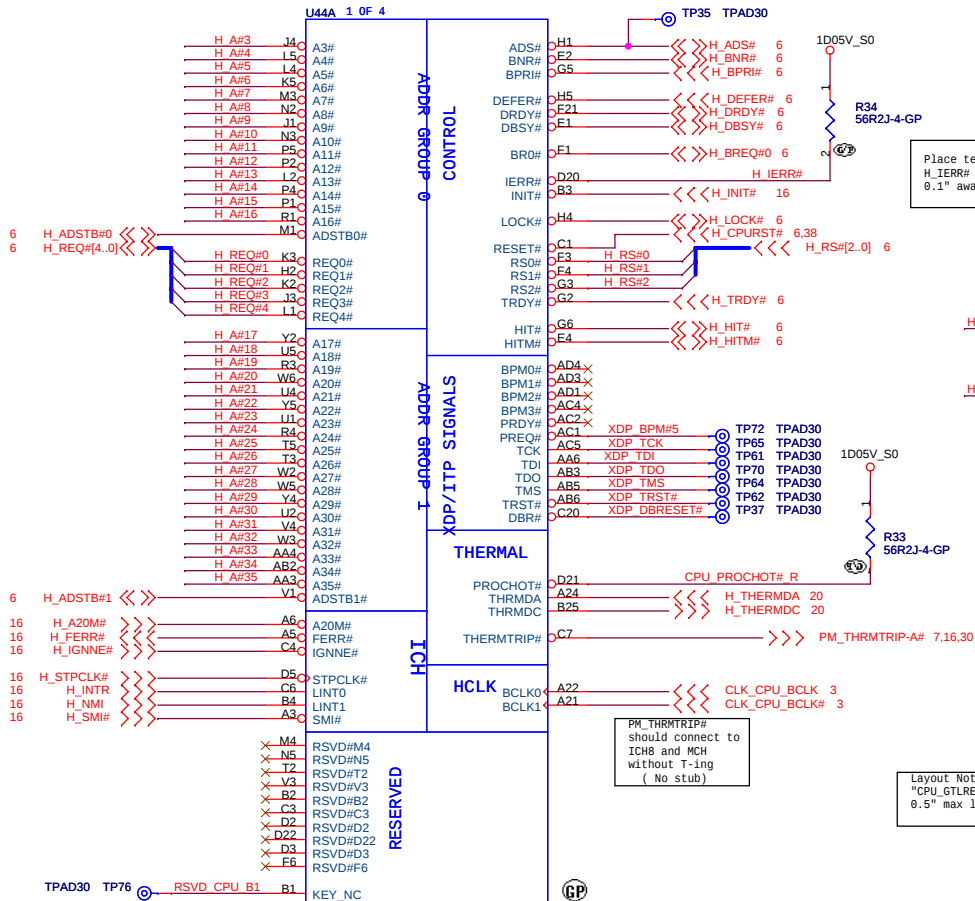
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

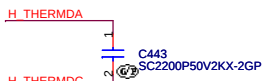
<Core Design>

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Title			
Reference			
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A3		-1	
Date:	Monday, September 10, 2007	Sheet	2 of 39

6 H_A#(35..3) <<>> H_A#(35..3)



Place testpoint on H_IERR# with a GND 0.1" away

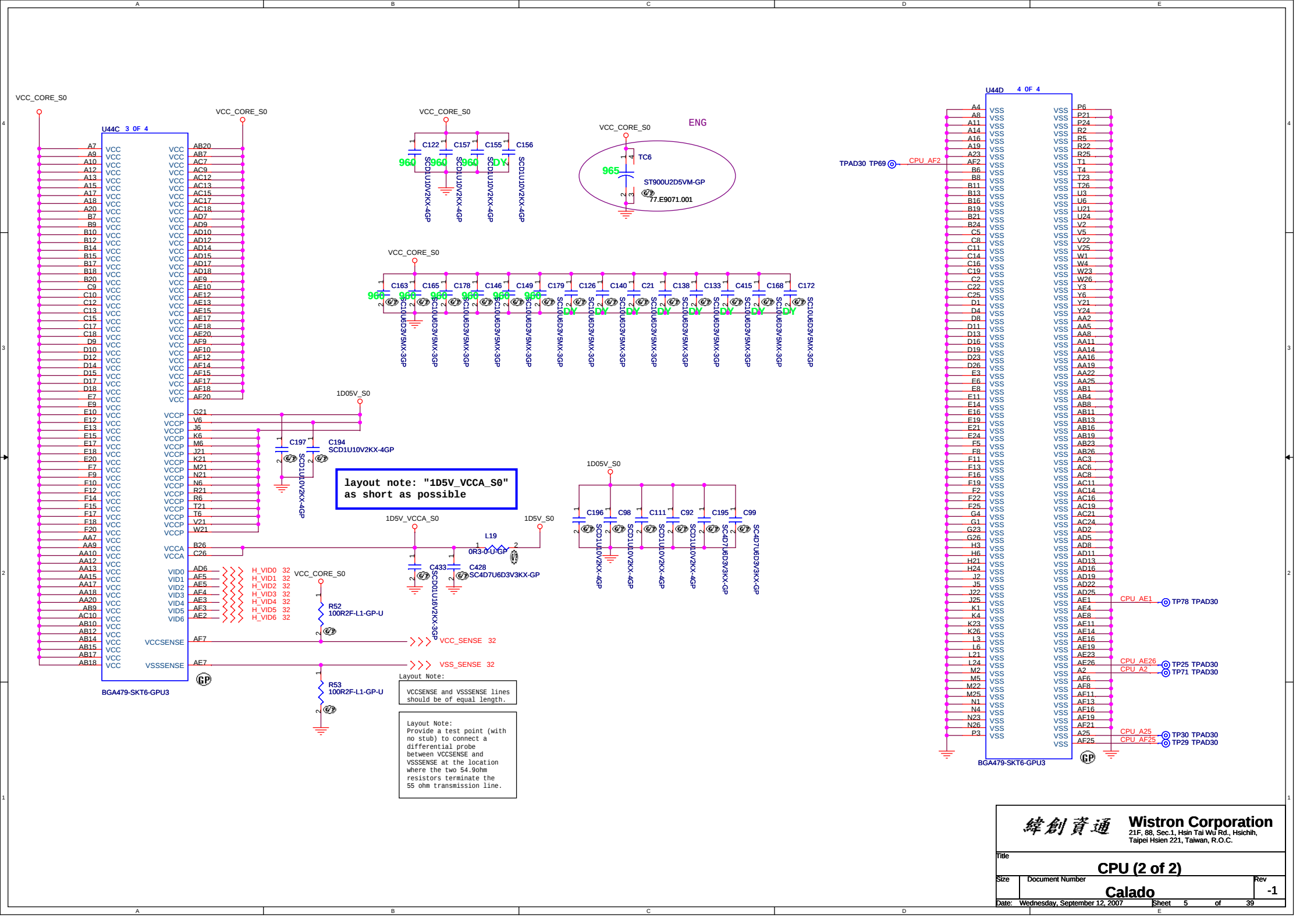


Layout Note:
"CPU_GTLREF0"
0.5" max length.

Net "TEST4" as short as possible,
make sure "TEST4" routing is
reference to GND and away from
noisy signals

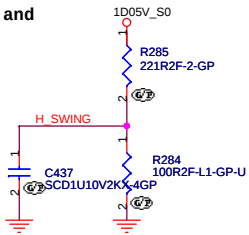
H_DINV#(3..0) <<>> H_DINV#(3..0) 6
H_DSTBN#(3..0) <<>> H_DSTBN#(3..0) 6
H_DSTBP#(3..0) <<>> H_DSTBP#(3..0) 6
H_D#(63..0) <<>> H_D#(63..0) 6

Layout Note:
Comp0, 2 connect with Z0=27.4 ohm, make
trace length shorter than 0.5"
Comp1, 3 connect with Z0=55 ohm, make
trace length shorter than 0.5"

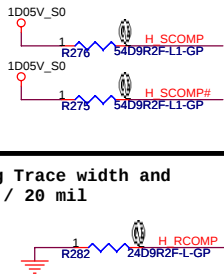


H_SWING routing Trace width and Spacing use 10 / 20 mil

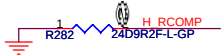
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

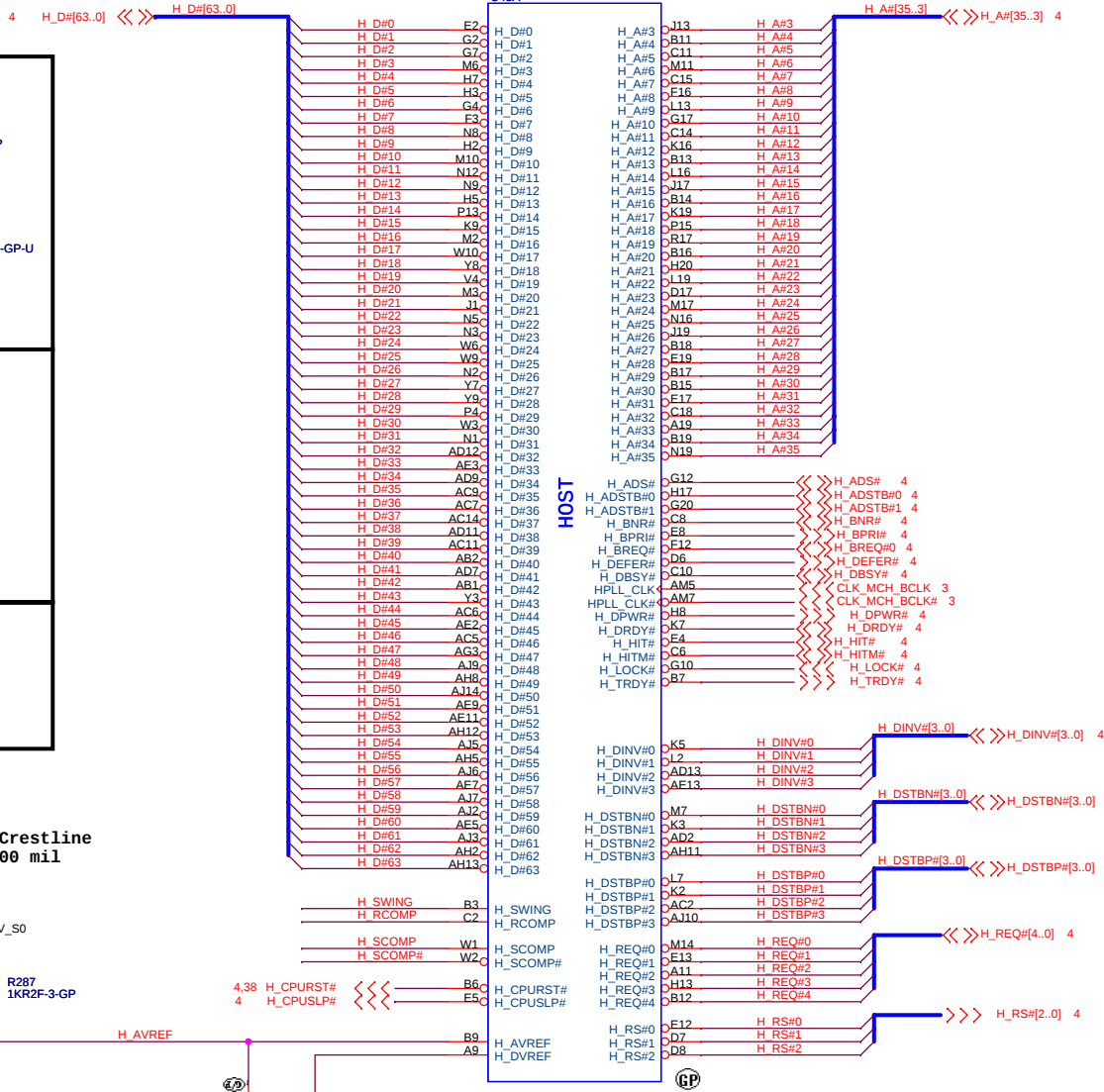
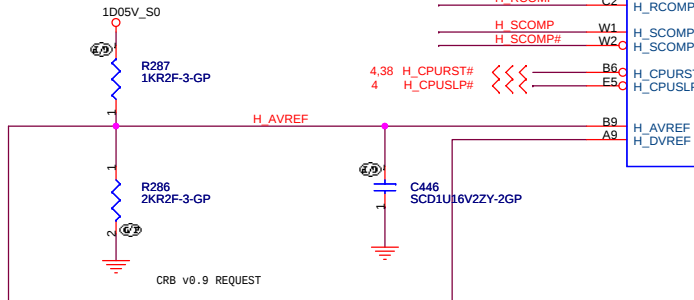


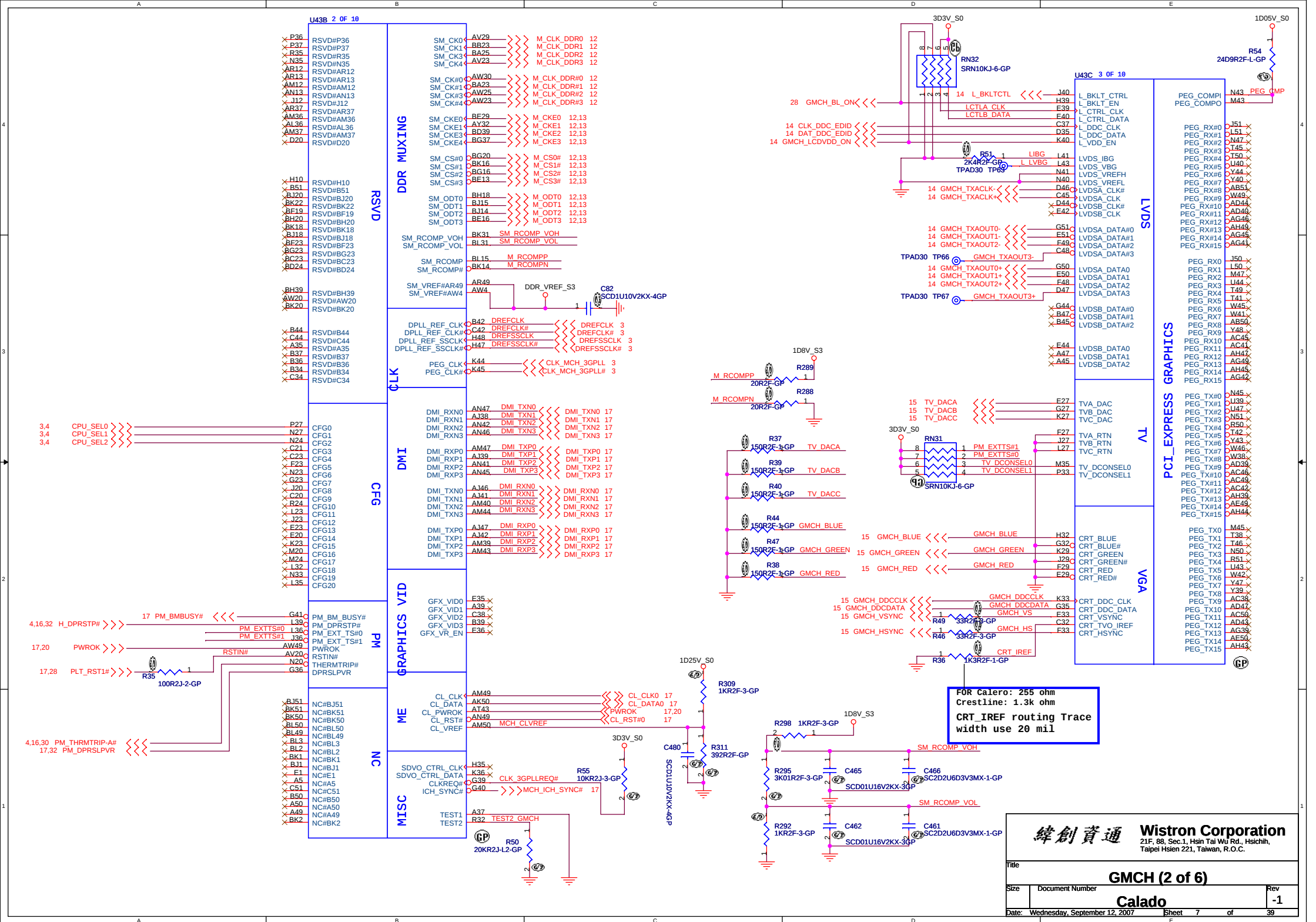
H_RCOMP routing Trace width and Spacing use 10 / 20 mil

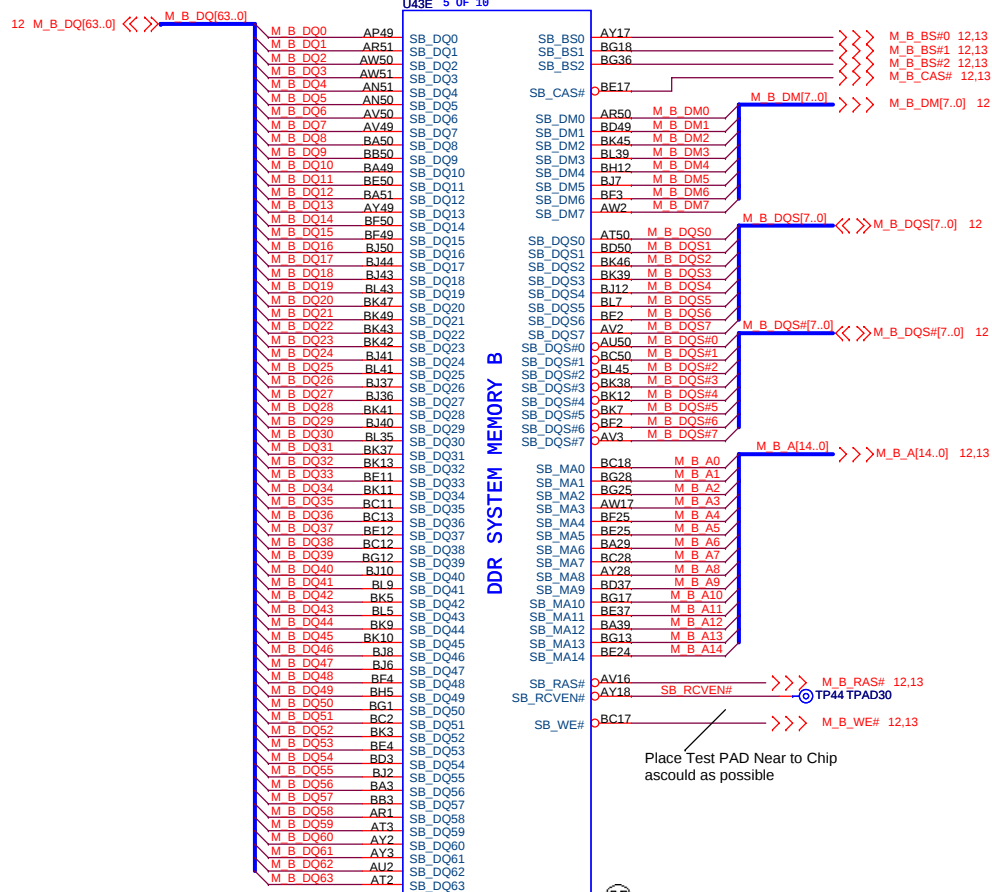


Place them near to the chip (< 0.5")

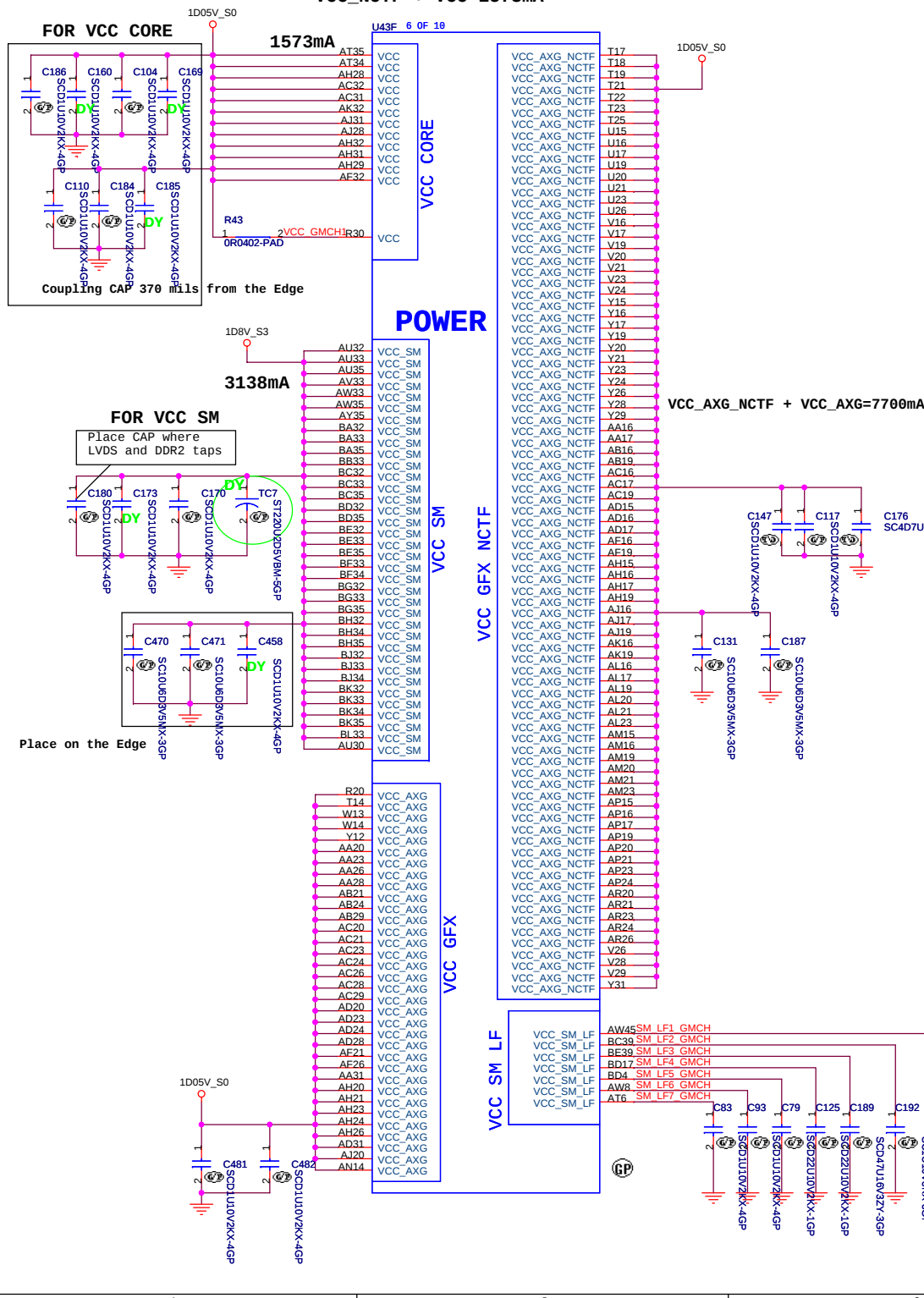
H_REF Decoupling Crestline close Crestline 100 mil



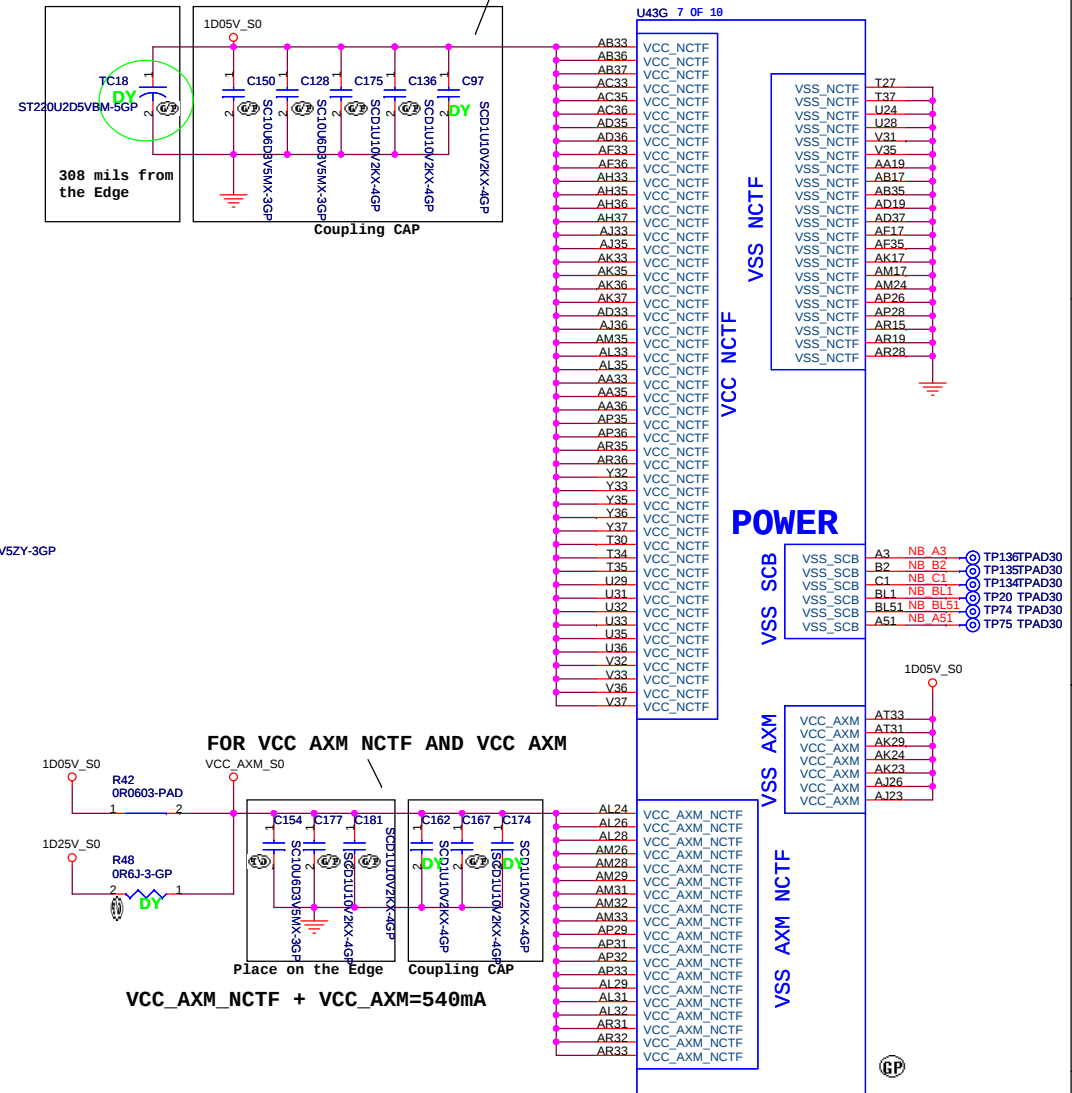


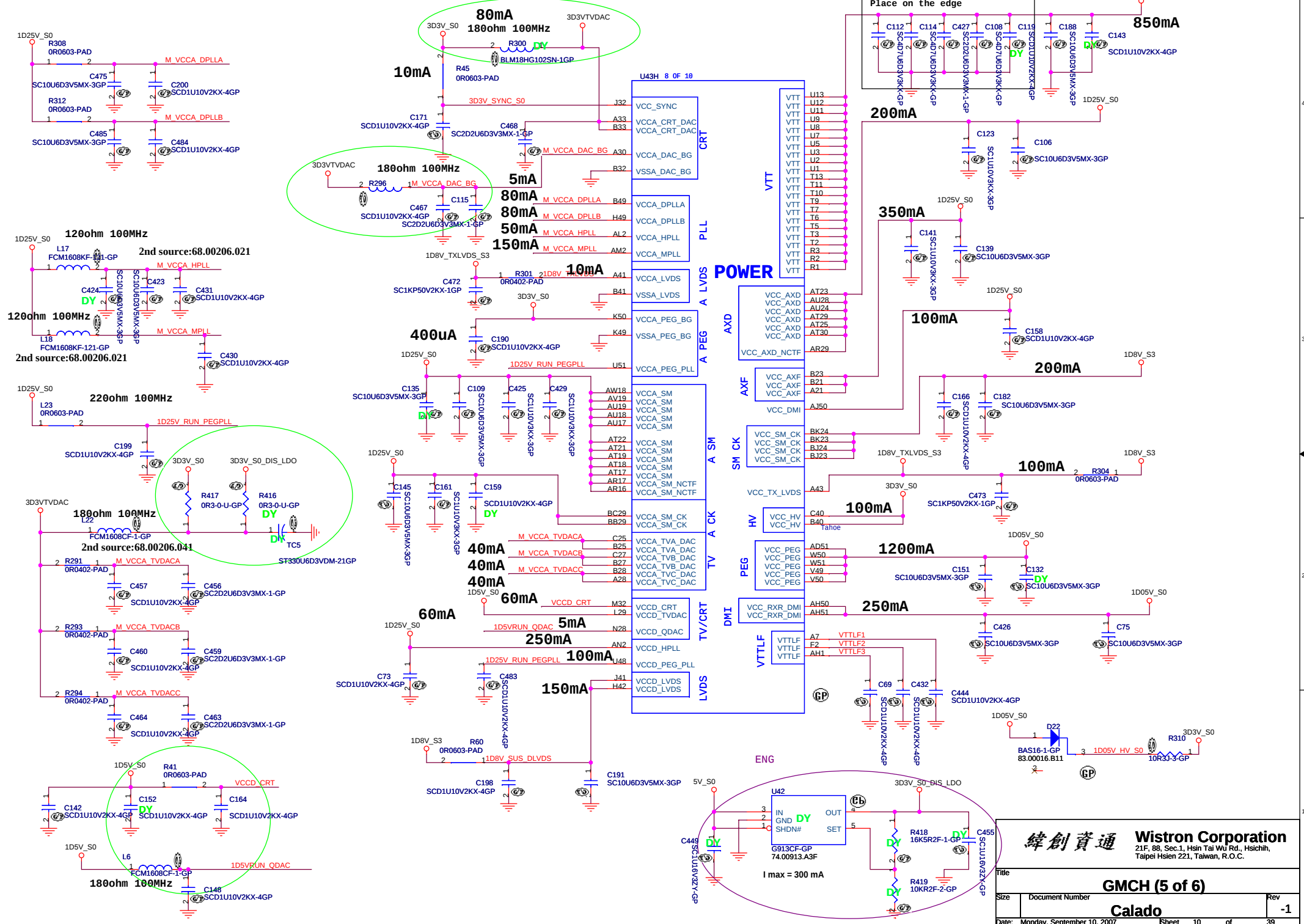


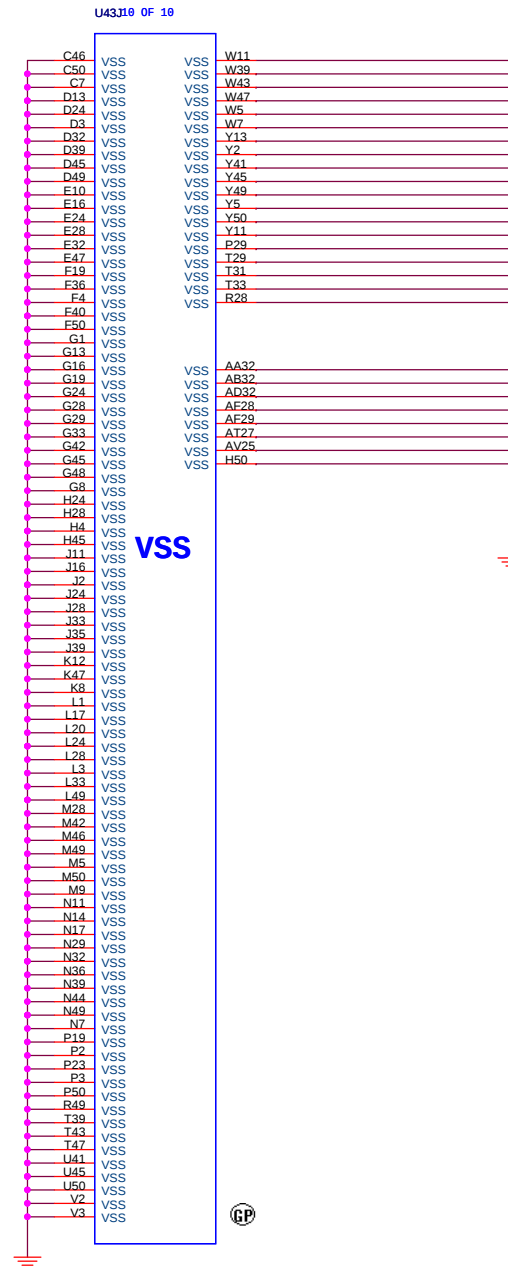
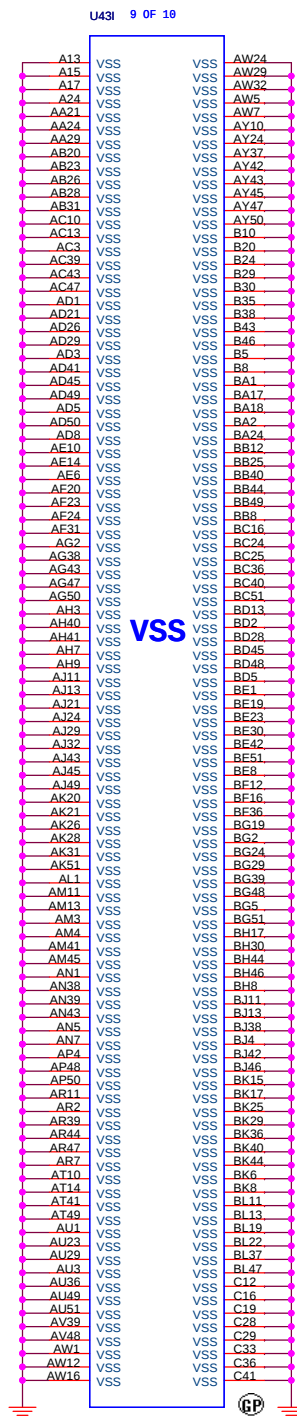
VCC_NCTF + VCC=1573mA

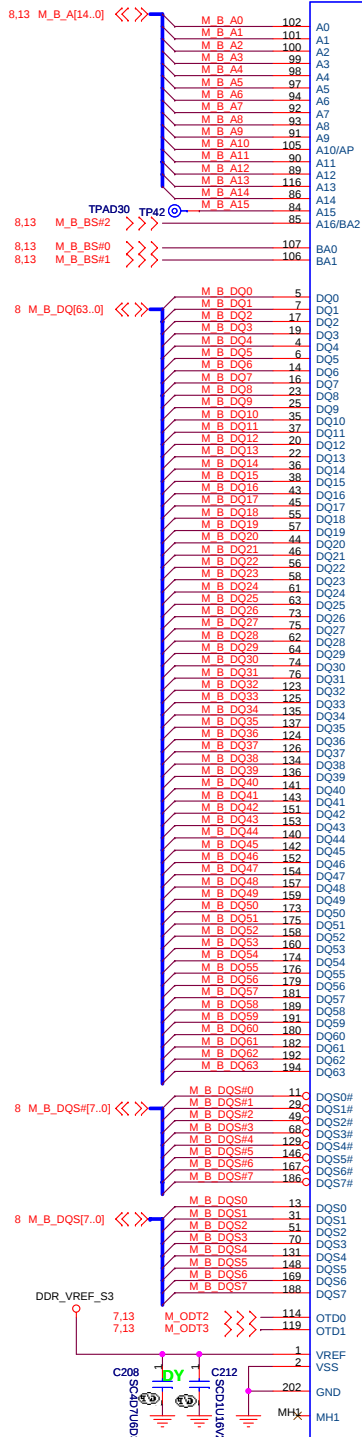


FOR VCC CORE AND VCC NCTF

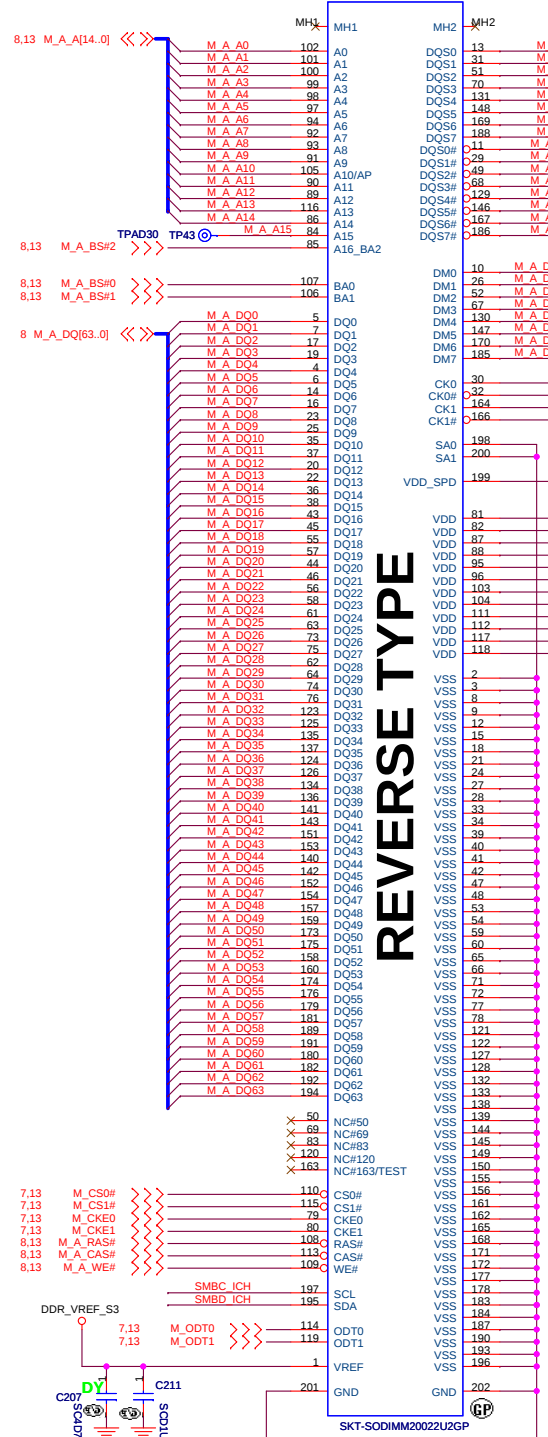
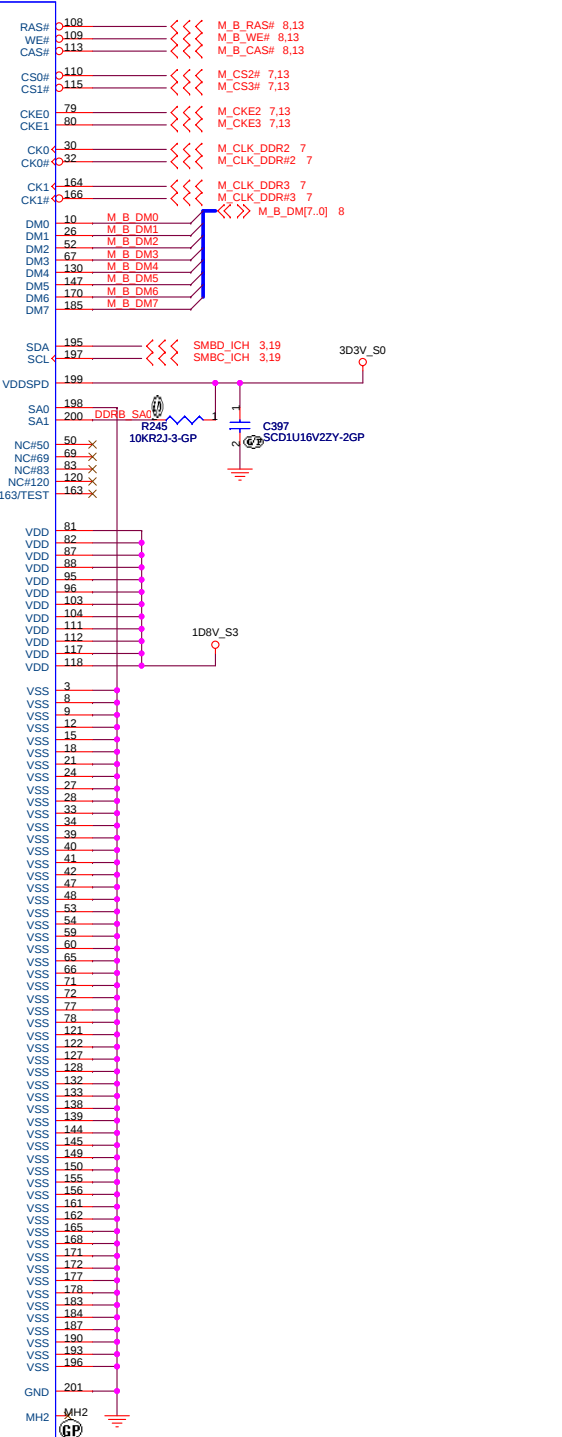








REVERSE TYPE



REVERSE TYPE

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Title: DDR2 Socket

Size: Document Number

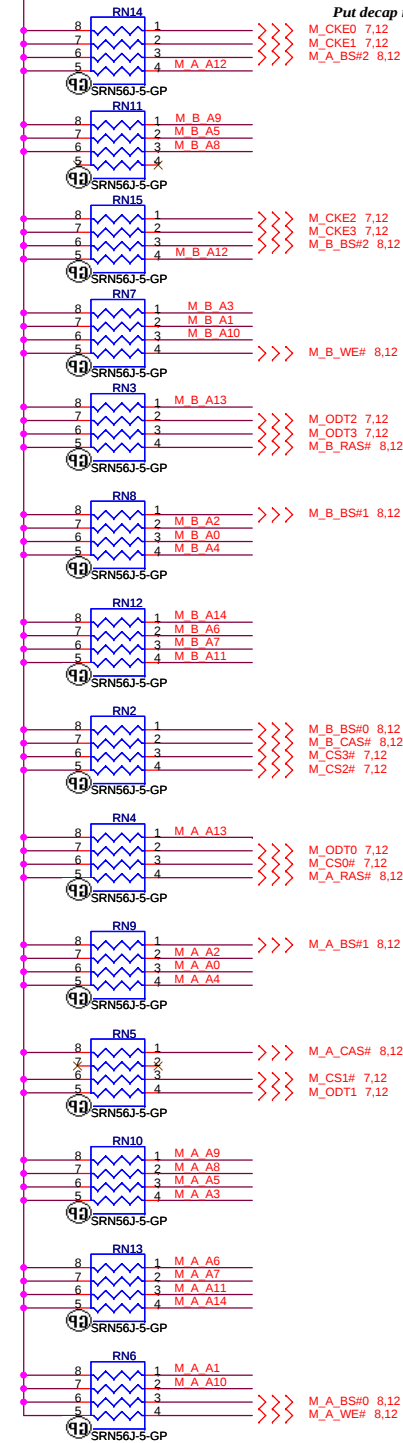
Date: Wednesday, September 12, 2007

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PARALLEL TERMINATION

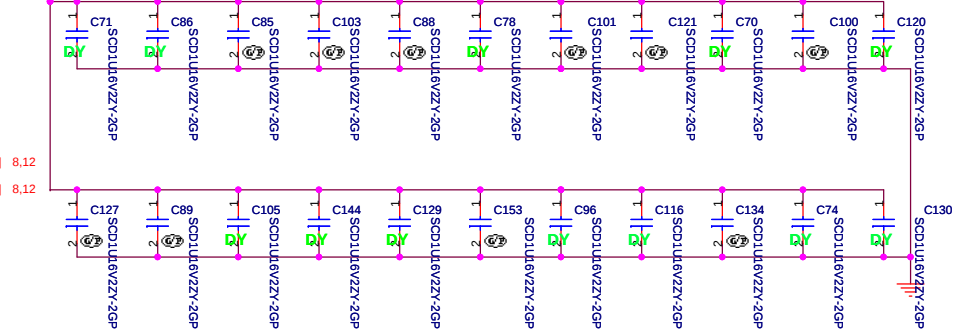
DDR_VREF_S0



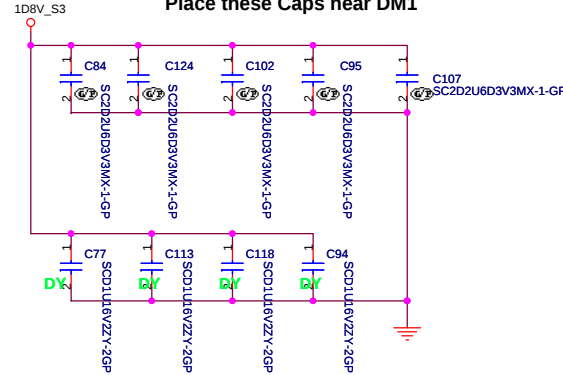
M_A_A[14..0] << M_A_A[14..0] 8,12
M_B_A[14..0] << M_B_A[14..0] 8,12

Decoupling Capacitor

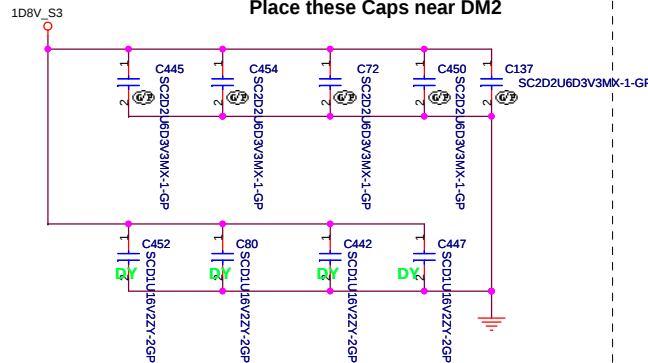
DDR_VREF_S0



Place these Caps near DM1



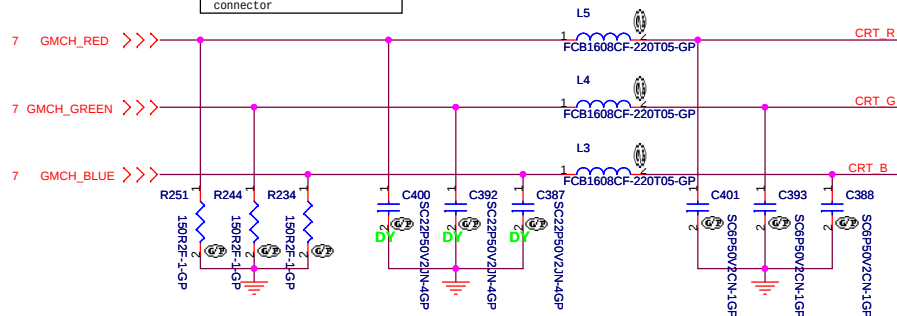
Place these Caps near DM2



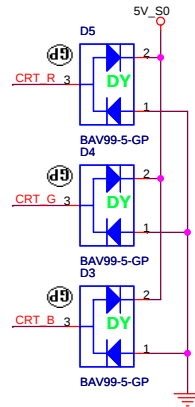
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Taipei Hsien 221, Taiwan, R.O.C.

Layout Note:
Place these resistors
close to the CRT-out
connector

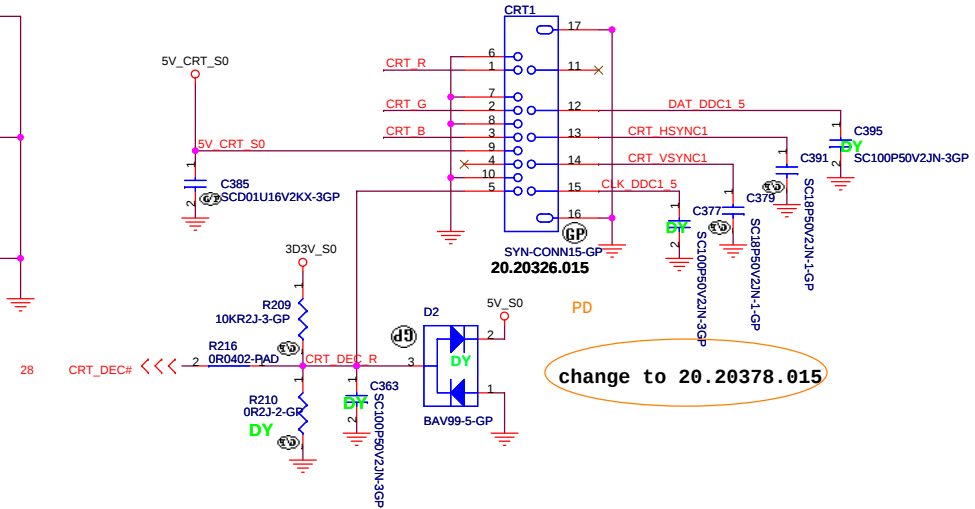
Ferrite bead impedance: 22 ohm@100MHz
from 10 ohm change to 22 ohm for EMI



Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

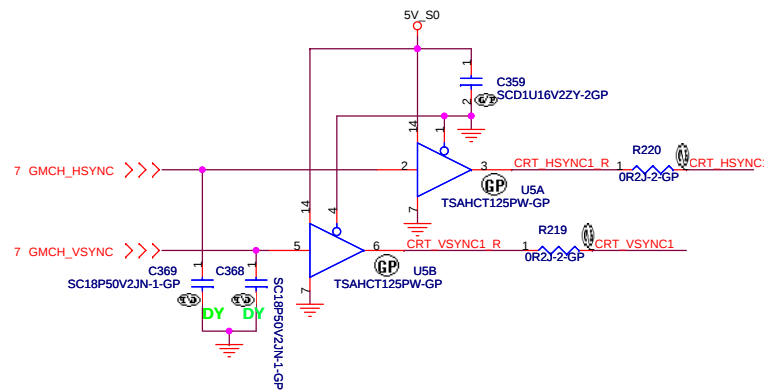


CRT I/F & CONNECTOR

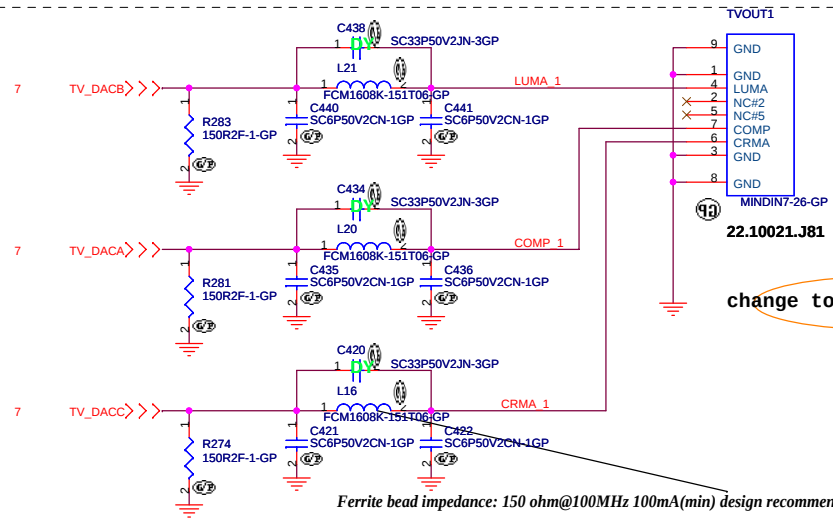


change to 20.20378.015

Hsync & Vsync level shift

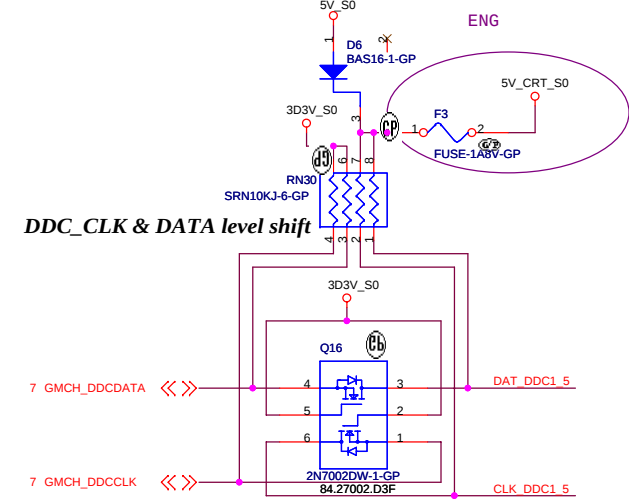


TV CONN



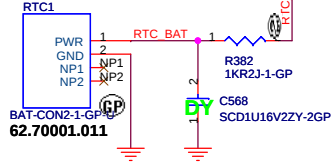
change to 22.10021.H61

Ferrite bead impedance: 150 ohm@100MHz 100mA(min) design recommend



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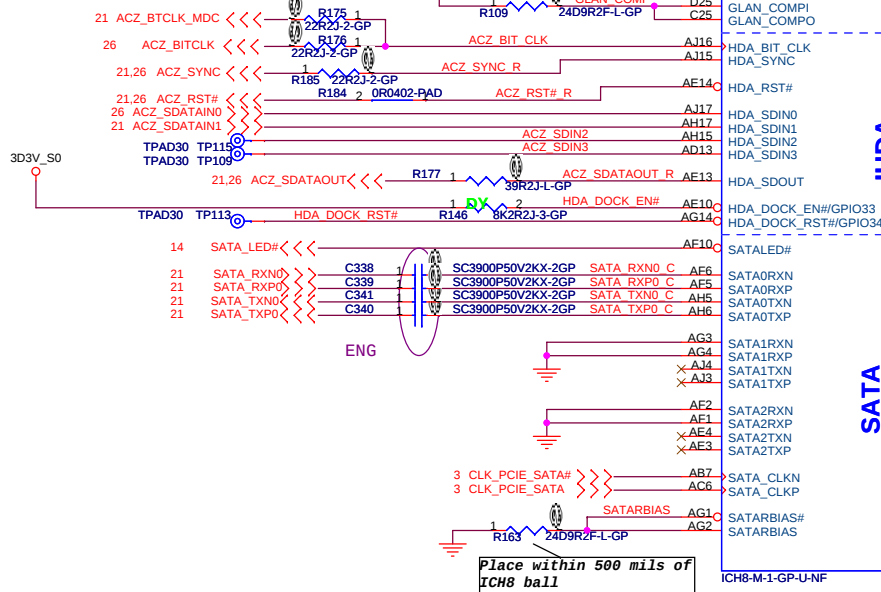
RTC circuitry



EMI capacitor

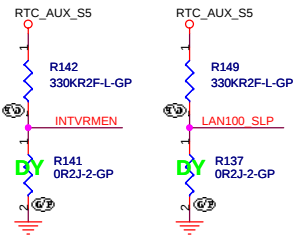


GLAN_COMP place within 500 mil of ICH8M



Place within 500 mils of ICH8 ball

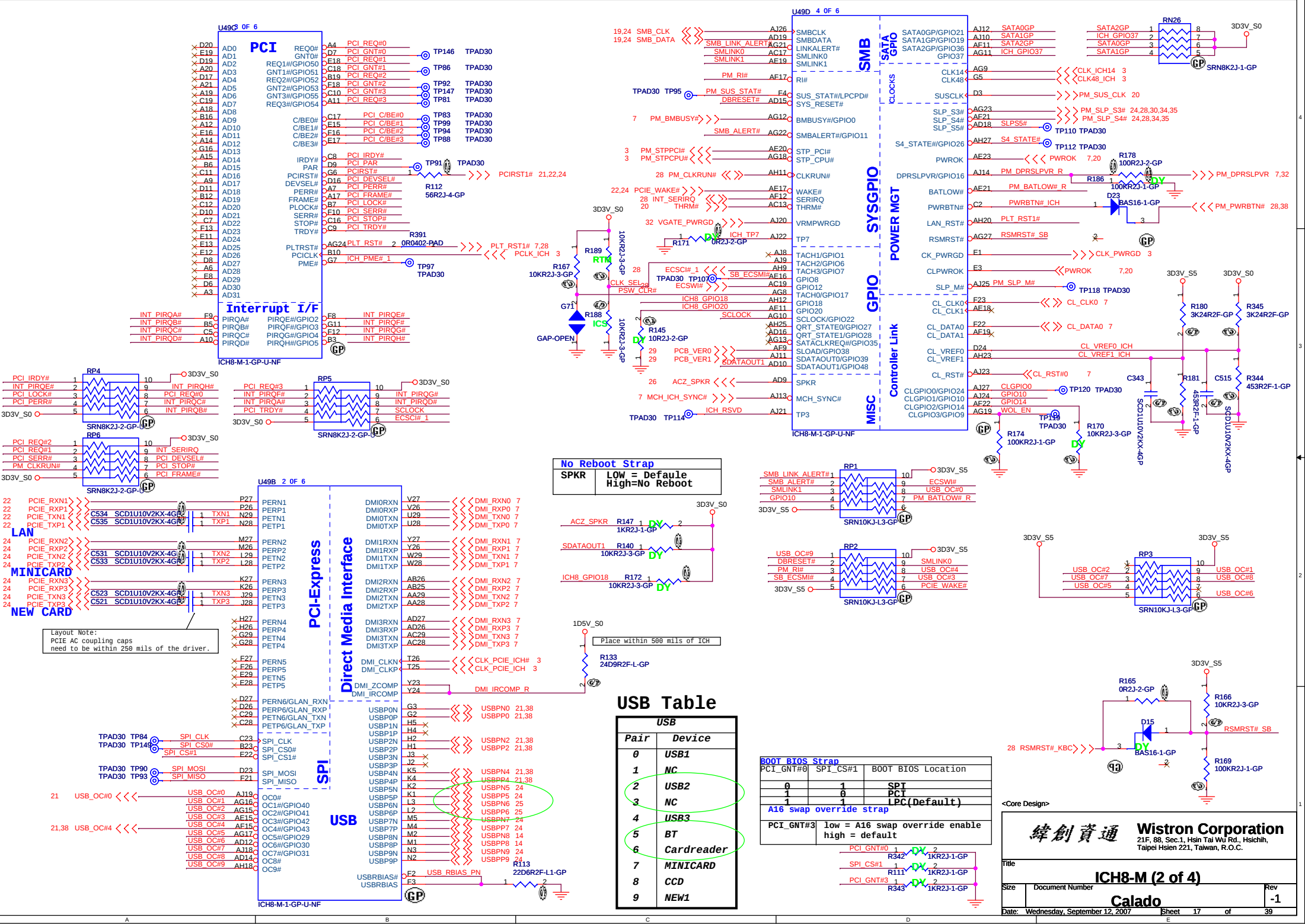
Change to 24.9 1% ohm when use SATA HD



Integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable

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No Reboot Strap
SPKR LOW = Default
High = No Reboot

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	BT
6	Cardreader
7	MINICARD
8	CCD
9	NEW1

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default
-----------	--

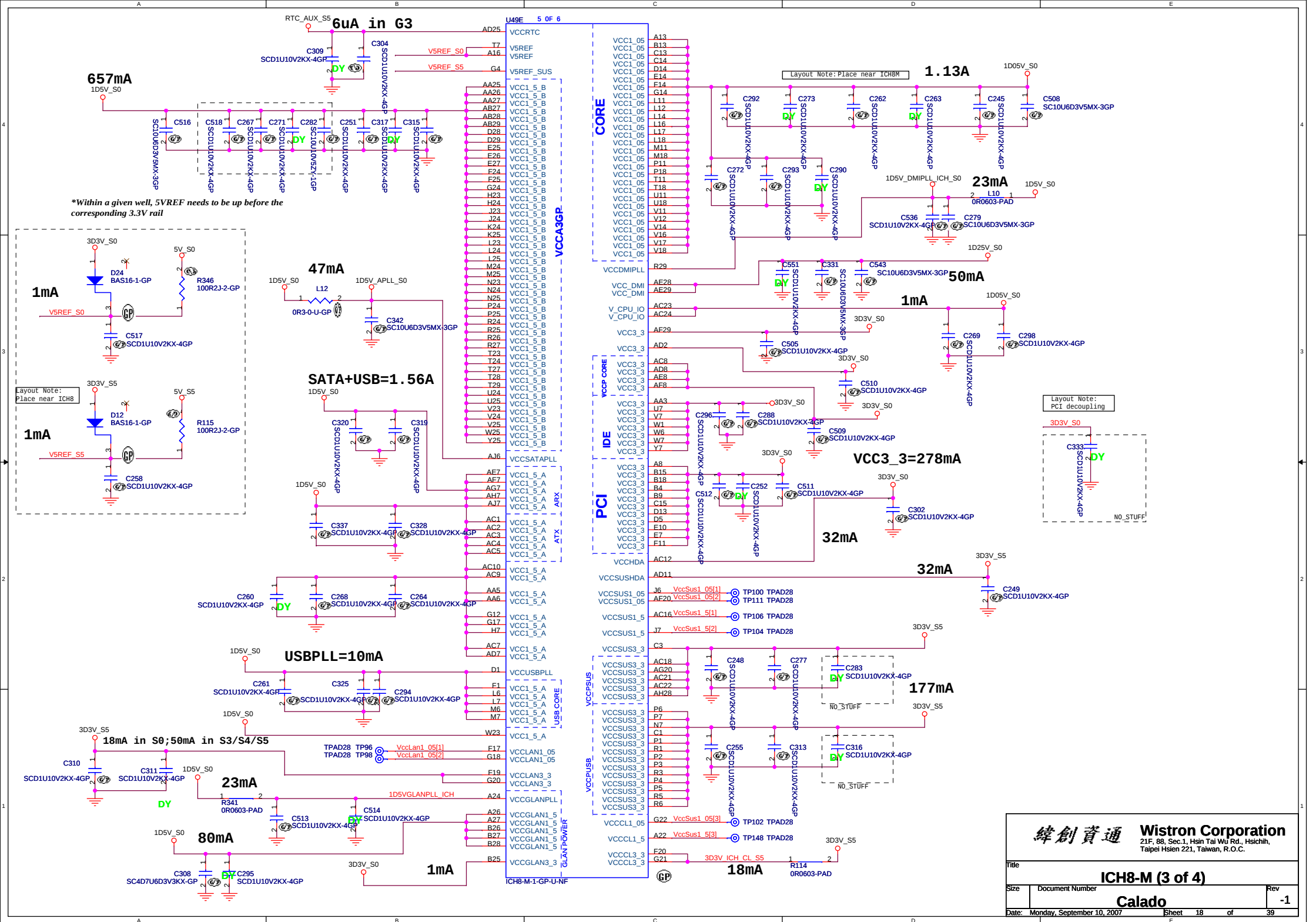
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

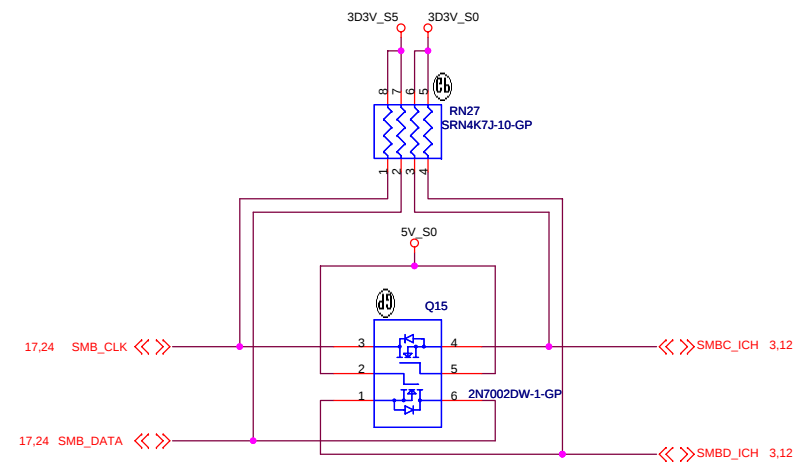
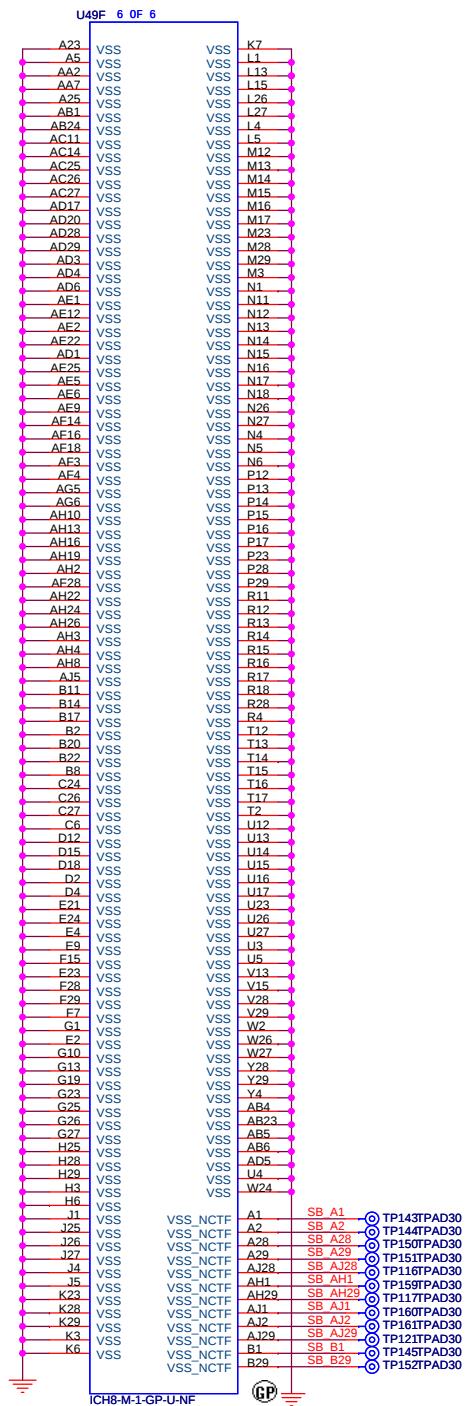
ICH8-M (2 of 4)

Calado

Title	Document Number	Rev
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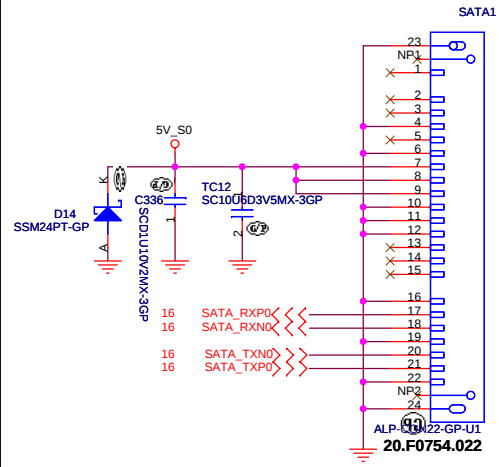
Date: Wednesday, September 12, 2007 Sheet 17 of 39



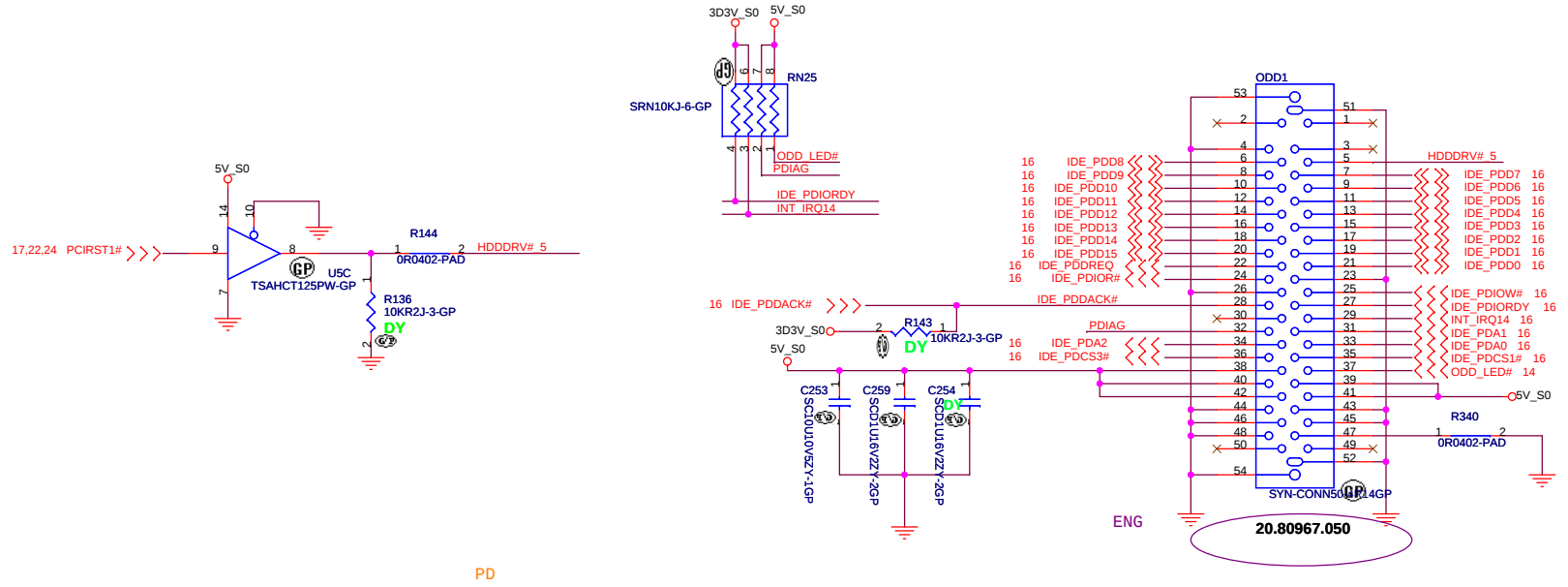


SMBUS

SATA HD Connector

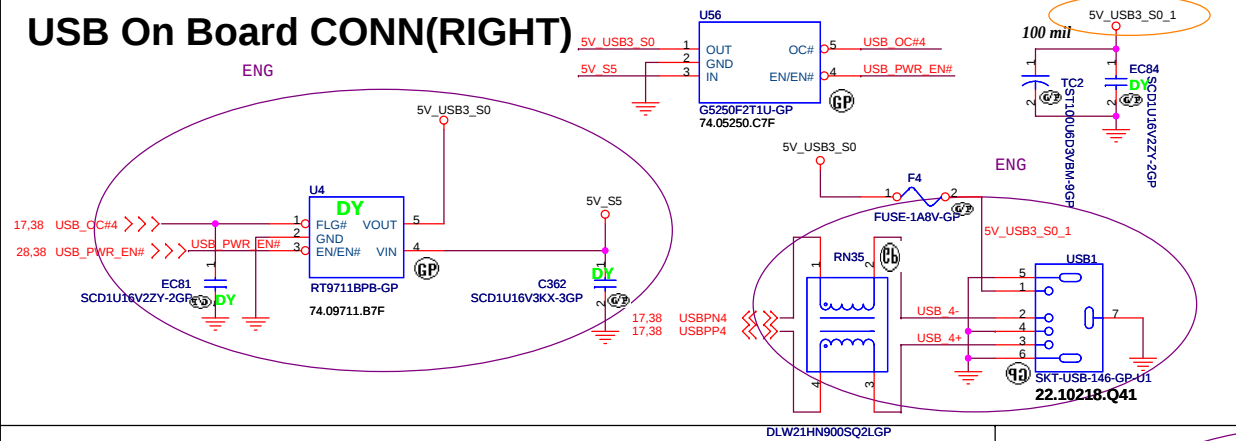


ODD Connector

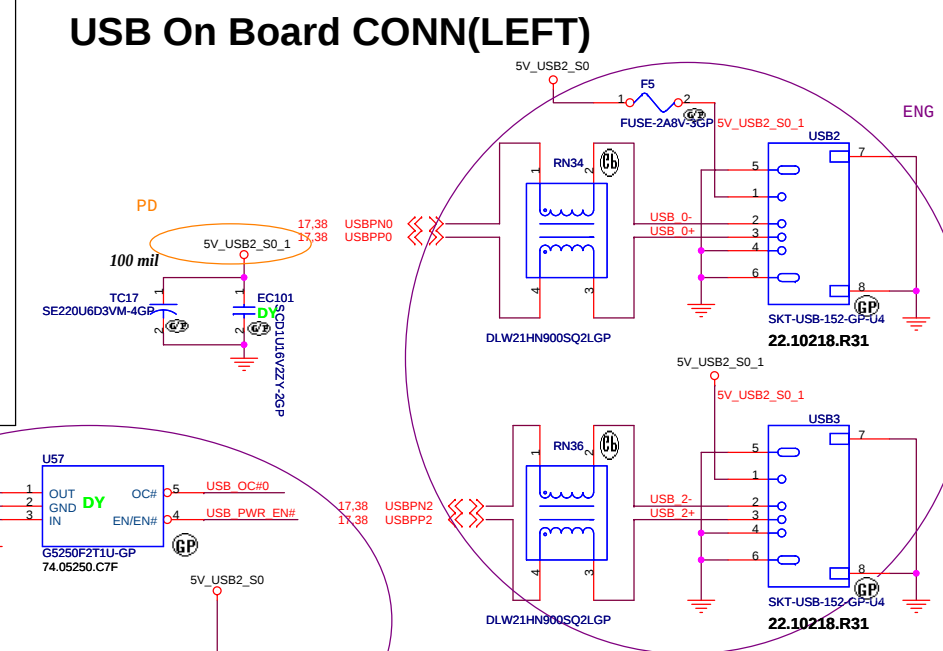


PD

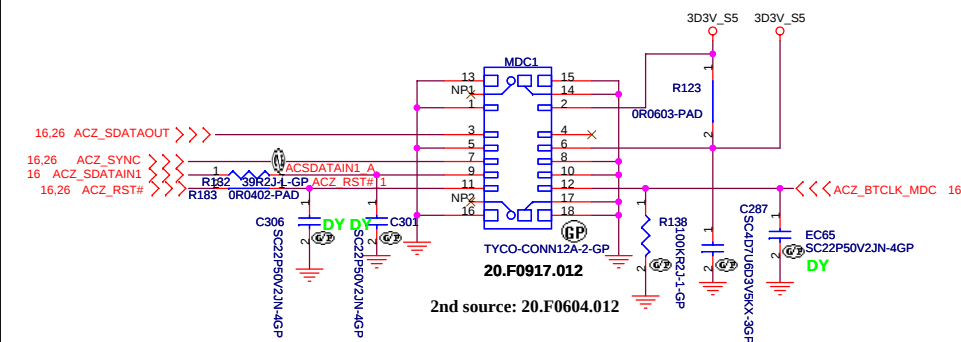
USB On Board CONN(RIGHT)



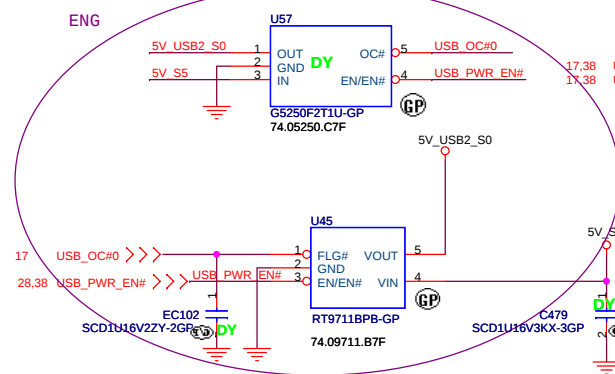
USB On Board CONN(LEFT)



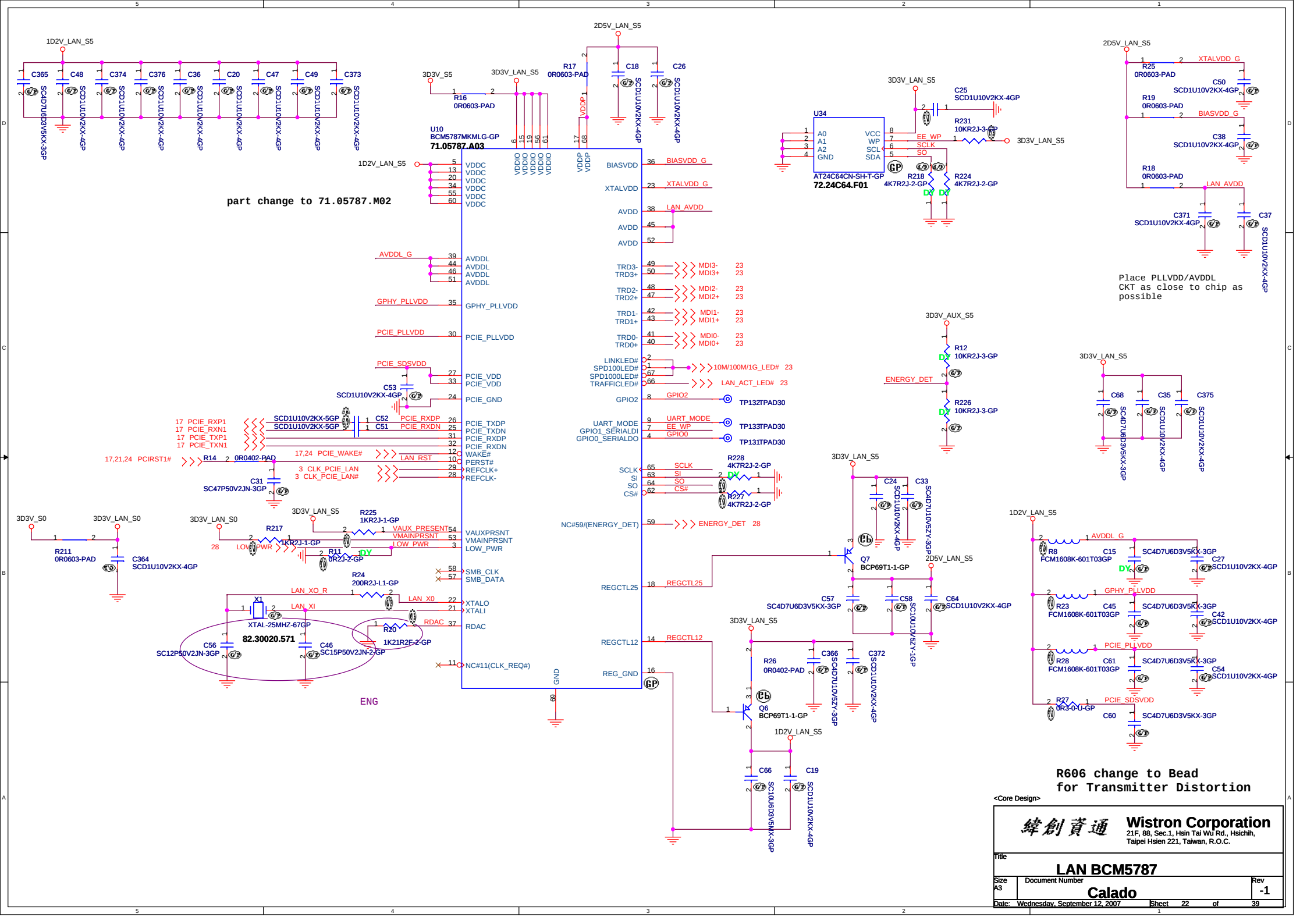
MDC 1.5 CONN



2nd source: 20.F0604.012

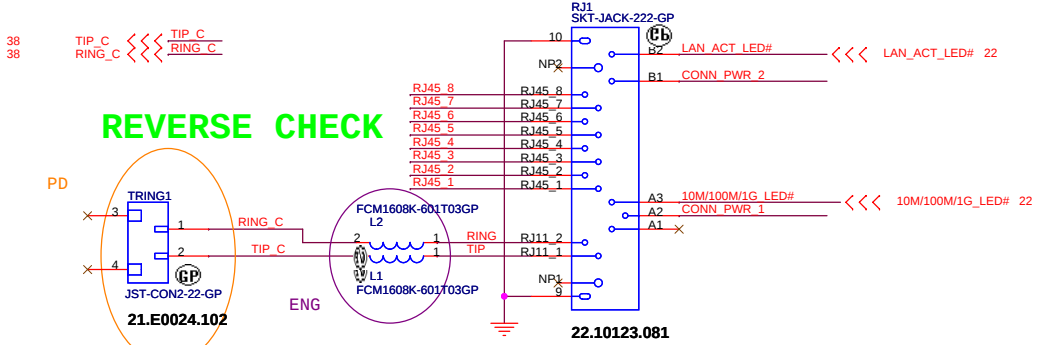


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Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector

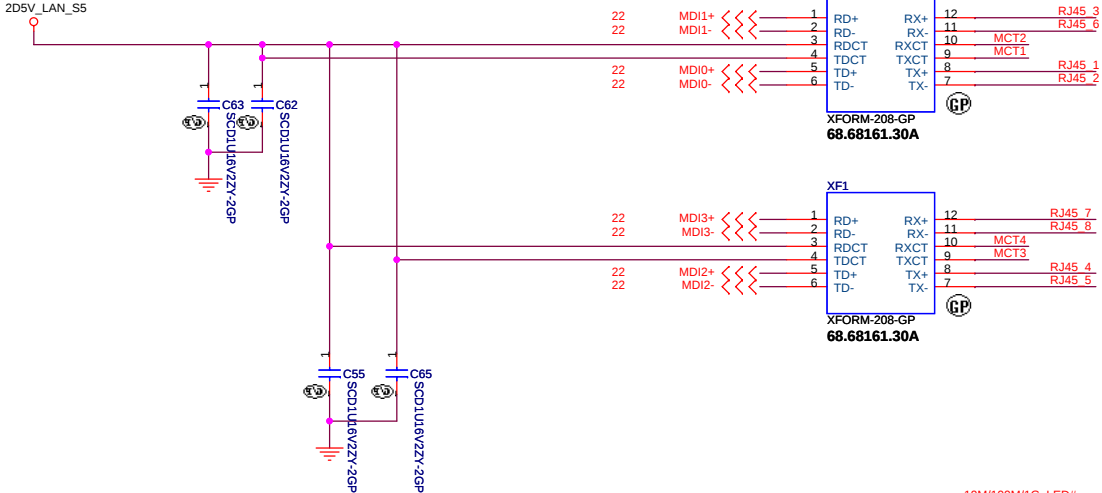


REVERSE CHECK

A3:Green
B2:YELLOW

LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

GIGA Lan Transformer

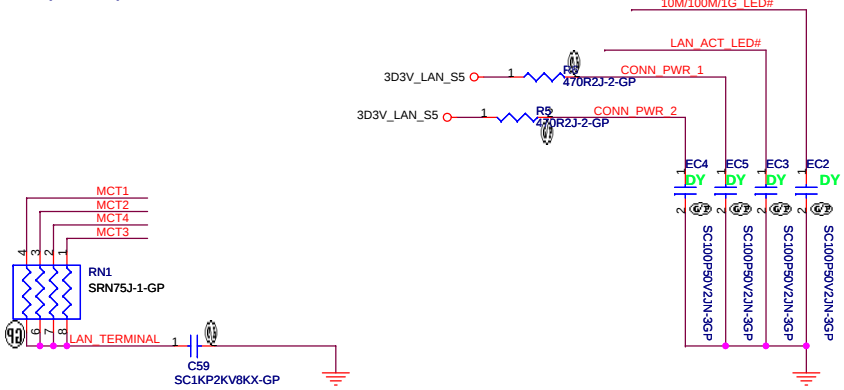


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



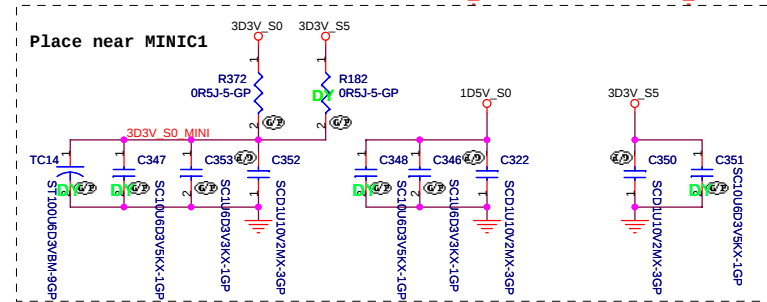
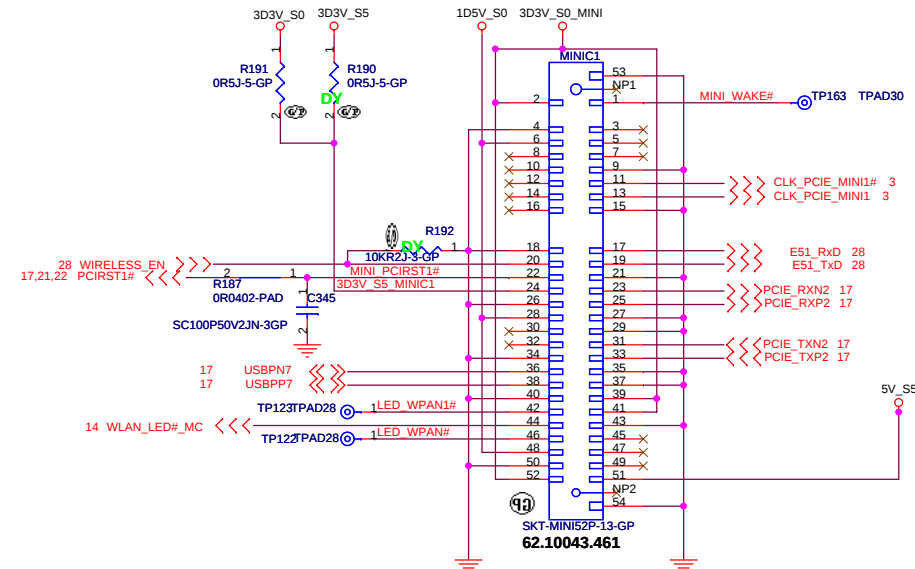
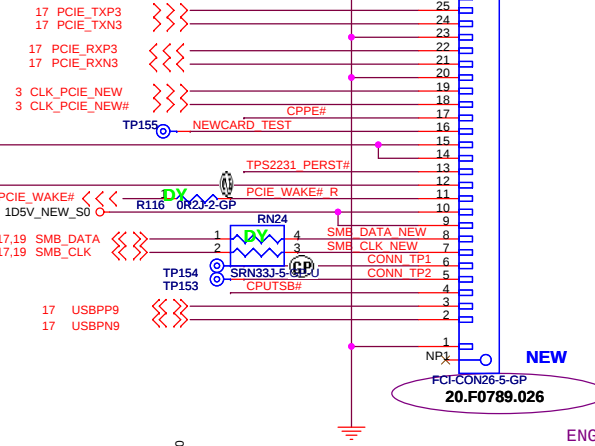
<Core Design>

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Title: **LAN Connector**

Size A3	Document Number	Rev -1
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Reserve the symbol
for bottom side
connector



BT MODULE

3D3V_BT_S0

3D3V_BT_S0

EC118
SCD1U16V2ZY-2GP

U53
RT9711-APBG-GP
74.09711.A7F

3D3V_S0

C567
SC4D7U6D3V5KX-3GP

BLUETOOTH_EN 28

ENG

EC21 put near BLUE1 / all USB put one choke near connector by EMI request

BLUE1

3D3V_BT_S0

USB 5+
USB 5-

R194 1 0R0402-PAD
R195 1 0R0402-PAD

USBPP5 17
USBPN5 17

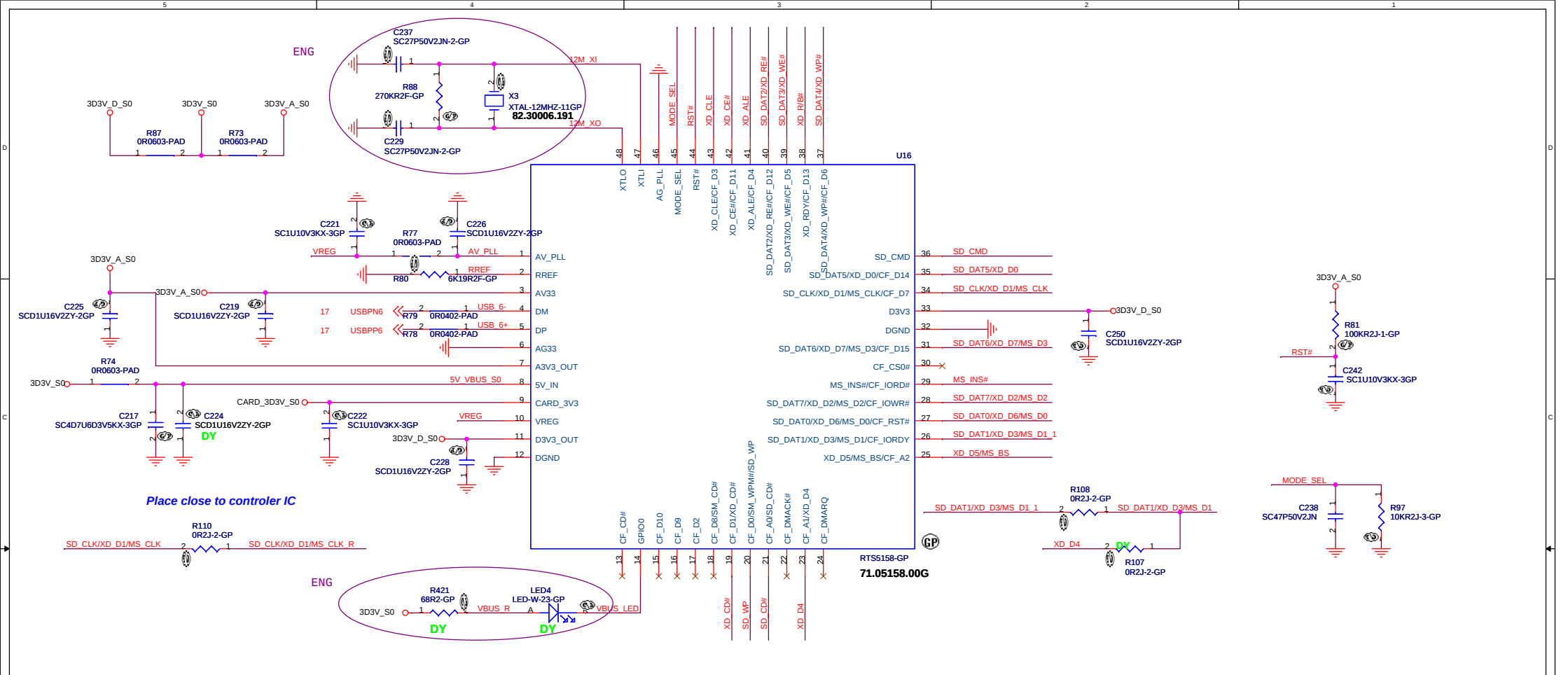
ACES-CON4-1-GP-U1

ICS

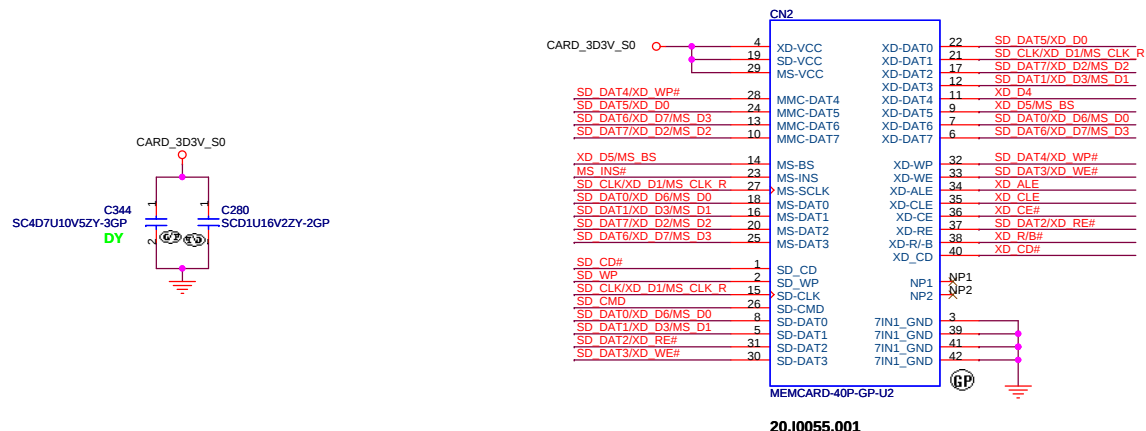
20.D0197.104

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Taipei Hsien 221, Taiwan, R.O.C.

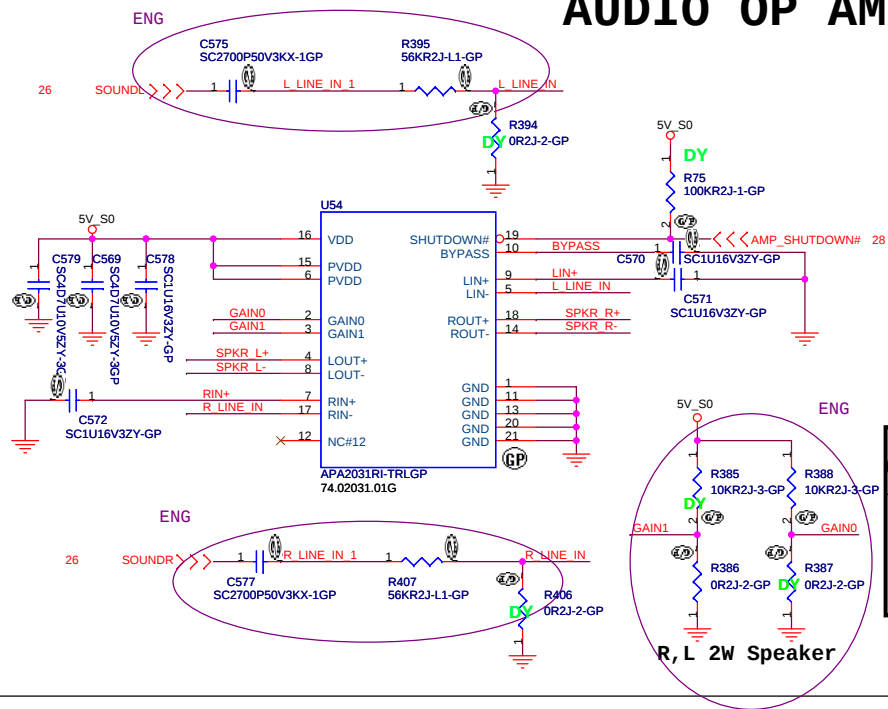
Title			
MINI CARD / NEW CARD/BT			
Size	Document Number		Rev
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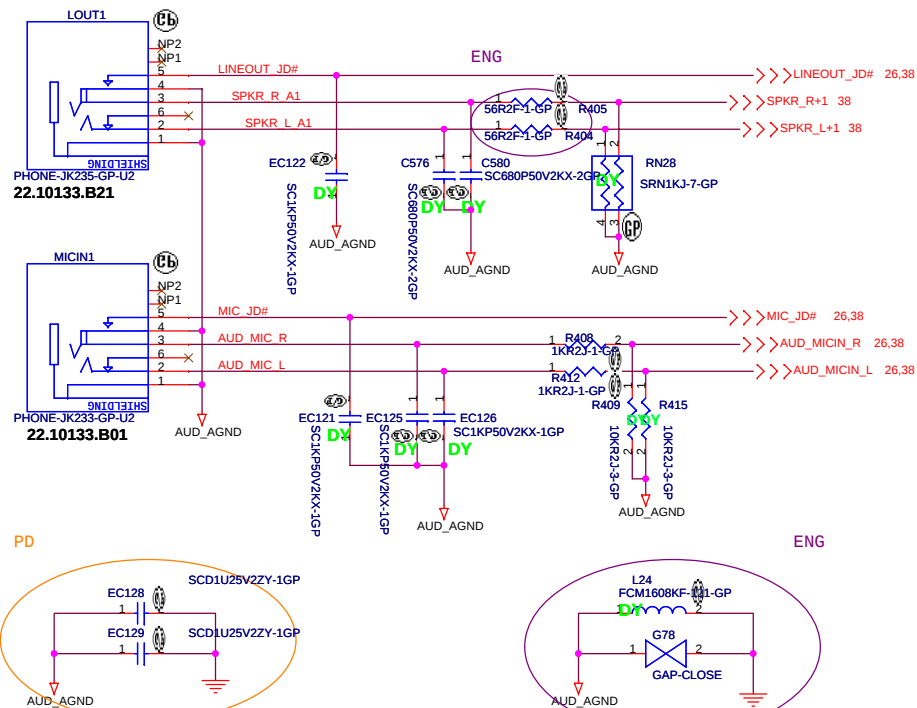
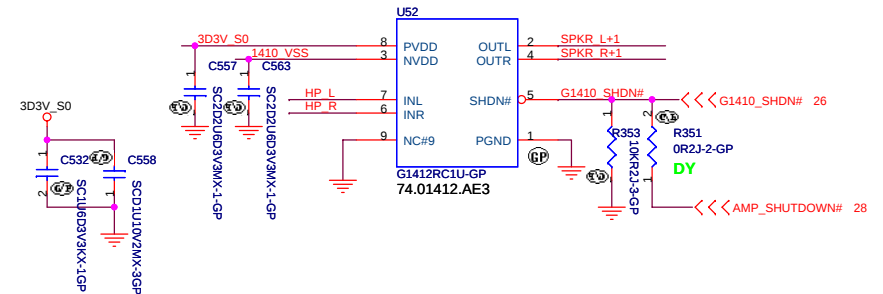
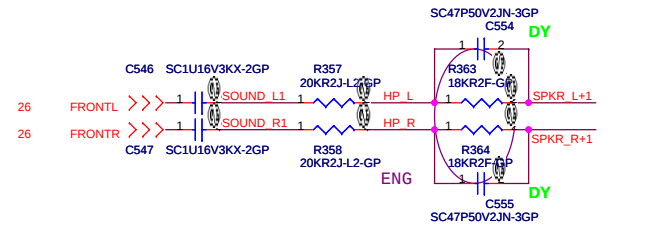
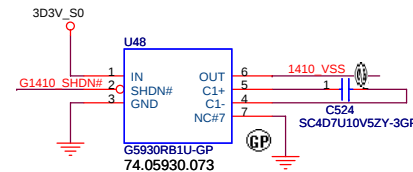
4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



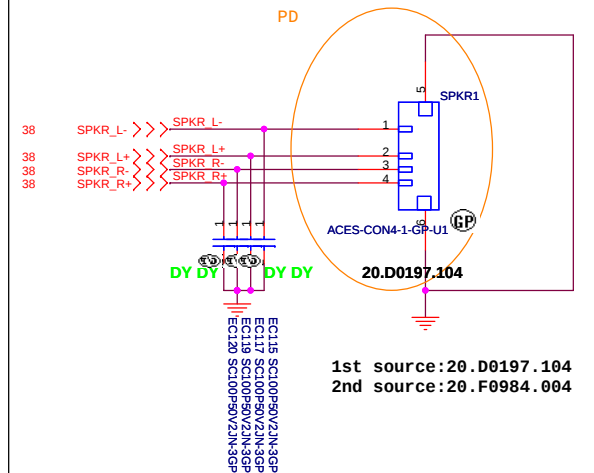
AUDIO OP AMPLIFIER



	GAIN0	GAIN1	Av (dB)
0	0	6	
0	1	10	
1	0	15.6	
1	1	21.6	



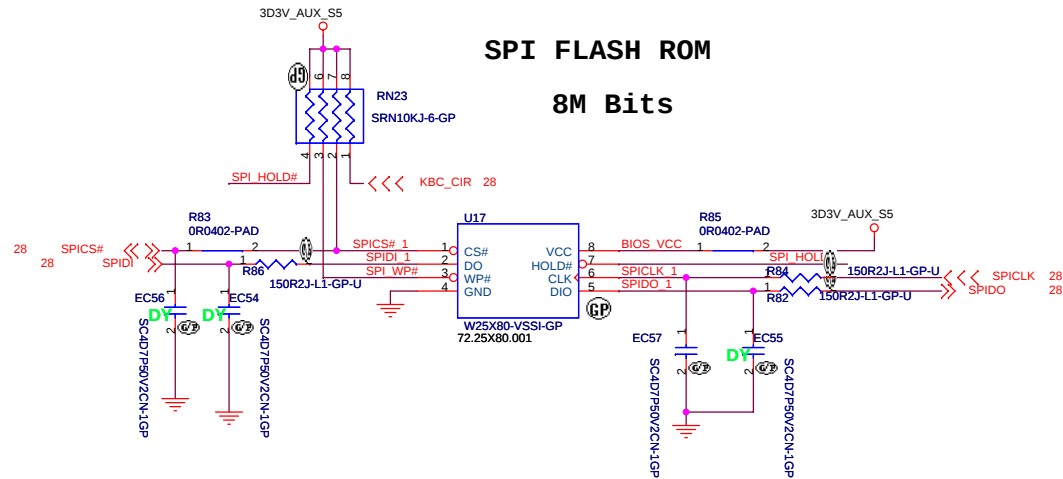
Internal Speaker



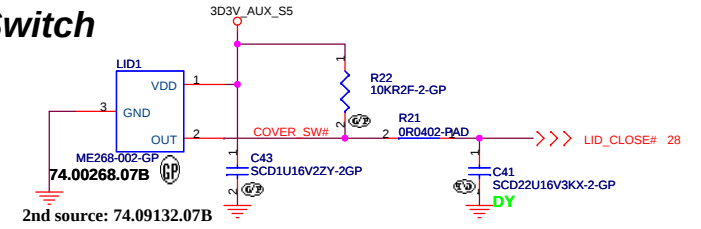
1st source: 20.D0197.104
2nd source: 20.F0984.004



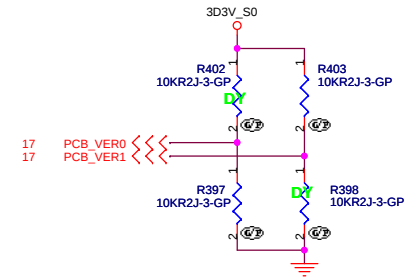
SPI FLASH ROM 8M Bits



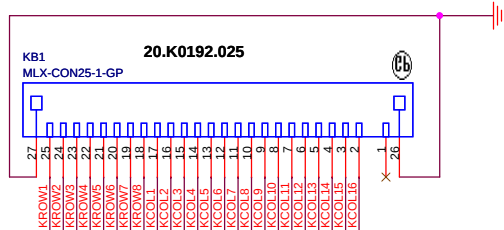
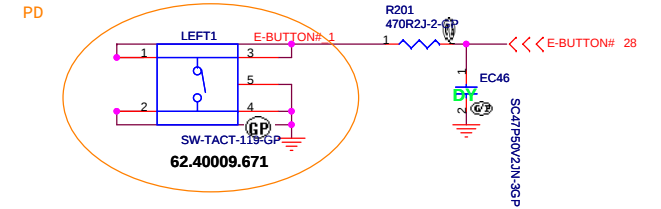
Hall Switch



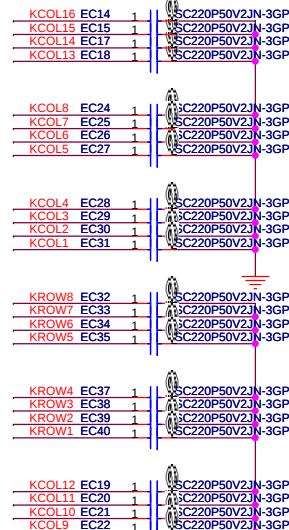
PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
-2: 1,1



E-key



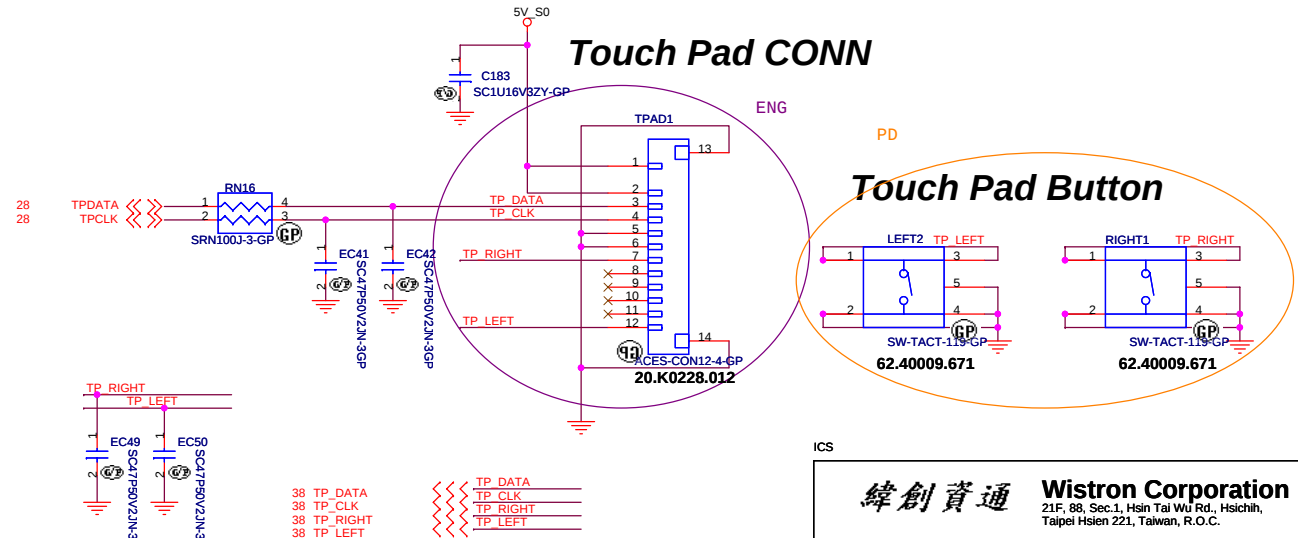
EMI Bypass cap.



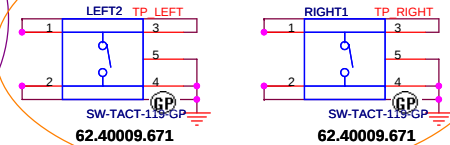
Internal Keyboard CONN



Touch Pad CONN

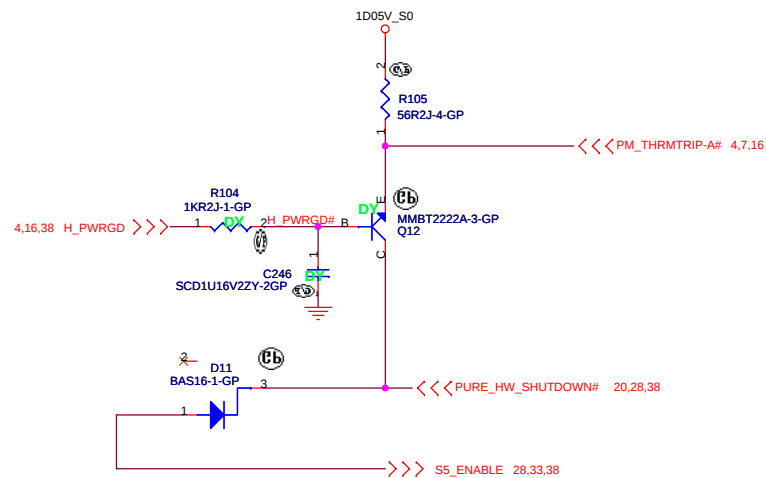
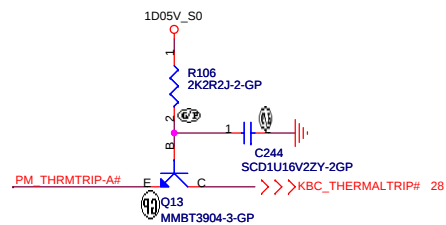
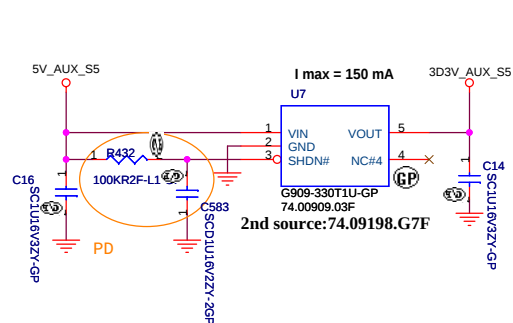


Touch Pad Button

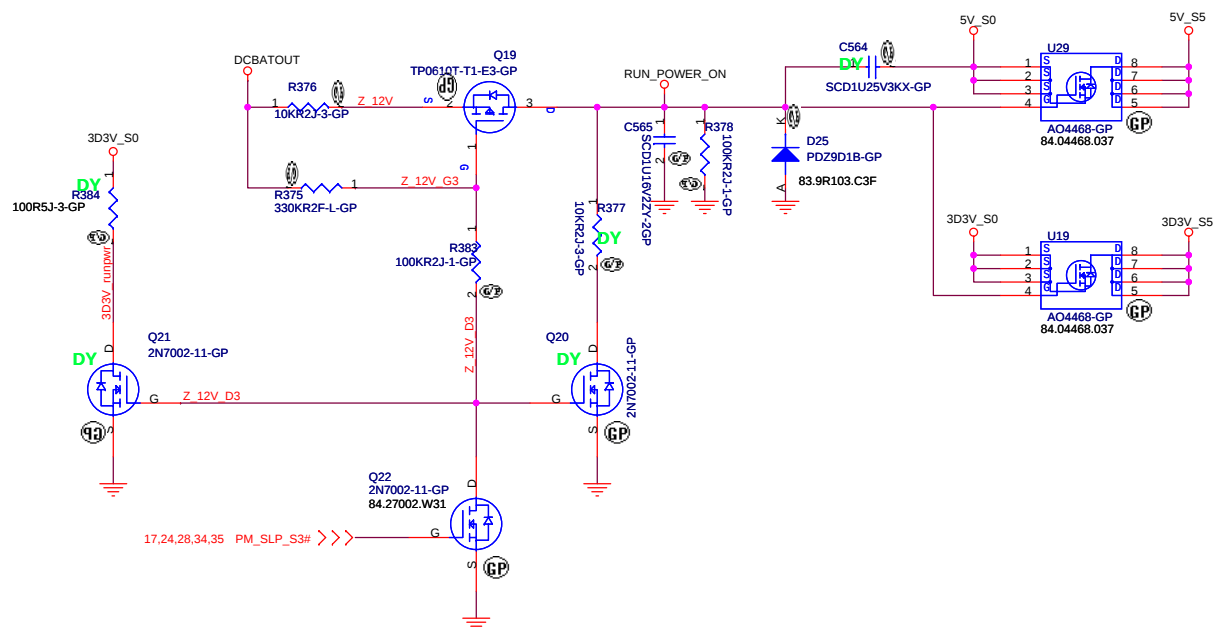


Aux Power

3D3V_AUX_S5



Run Power



ICS

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Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER and 3D3V AUX S5
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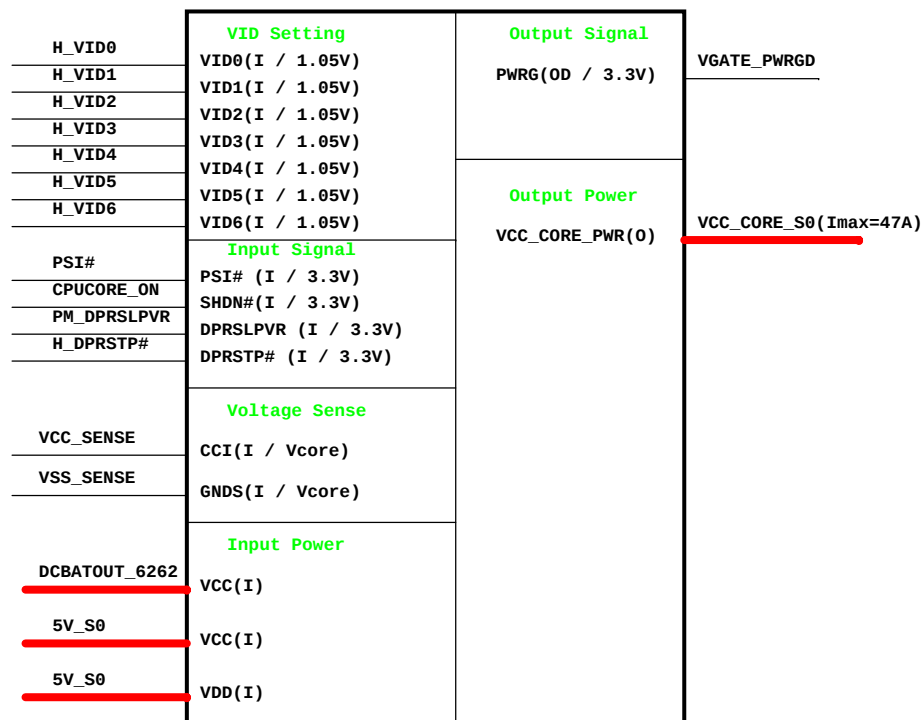
Size	Document Number
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Calado

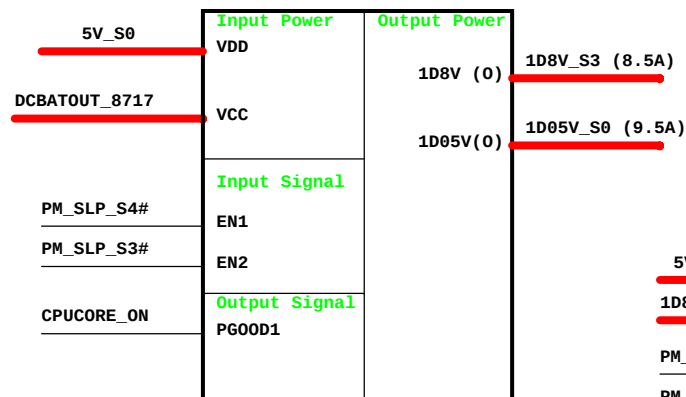
-1

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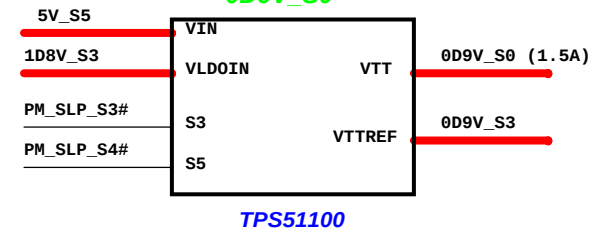
CPU_CORE MAX8770



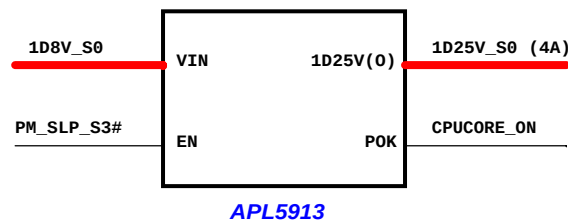
TPS51124 1D8V/1D05V



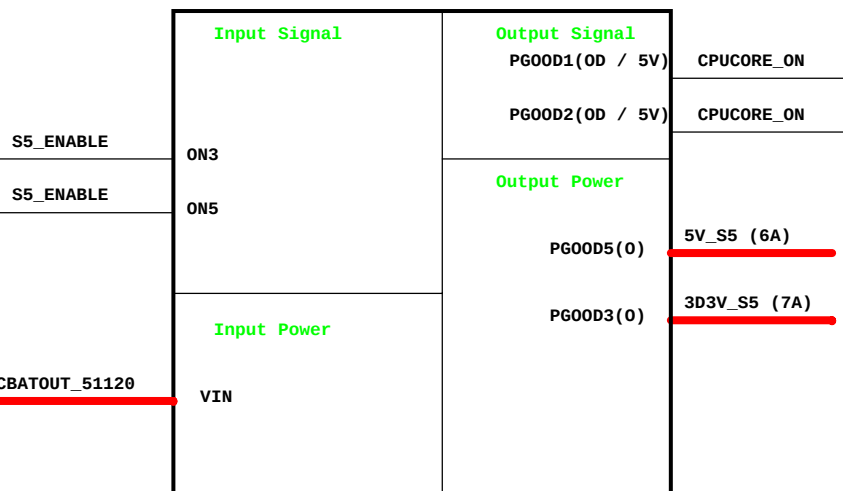
0D9V_S0



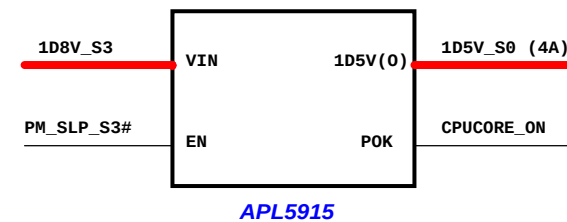
1D25V_S0



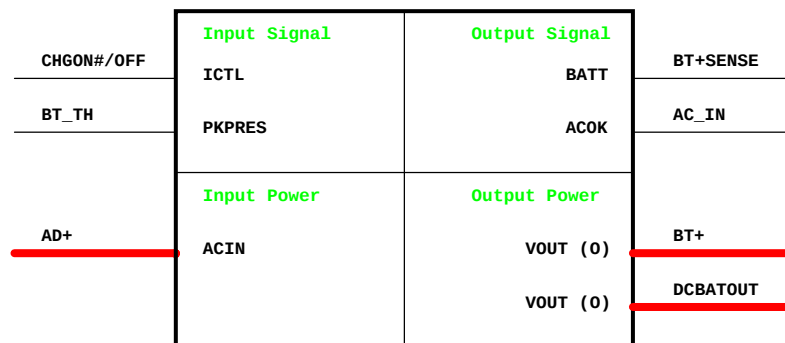
TPS51120 5V/3D3V

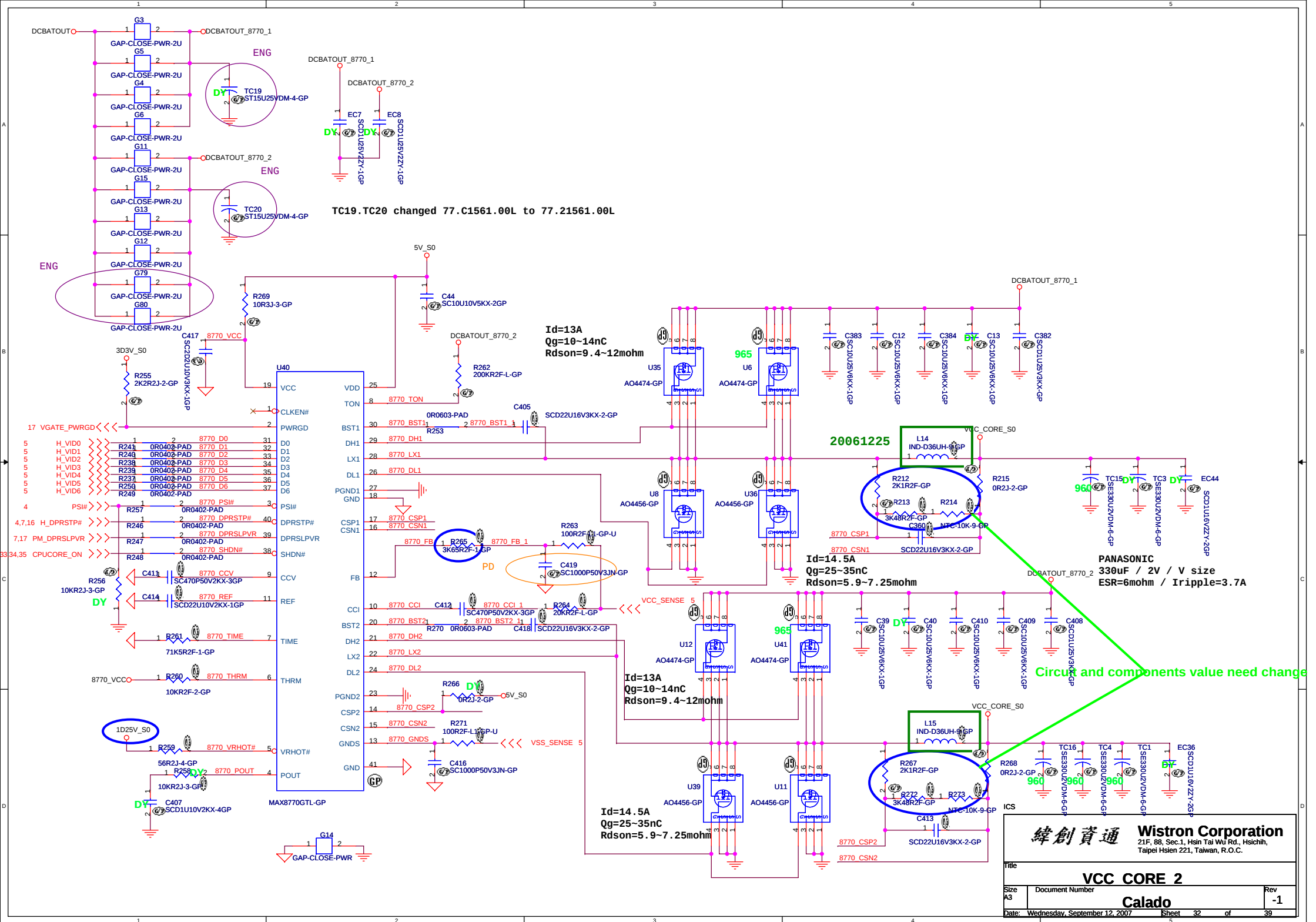


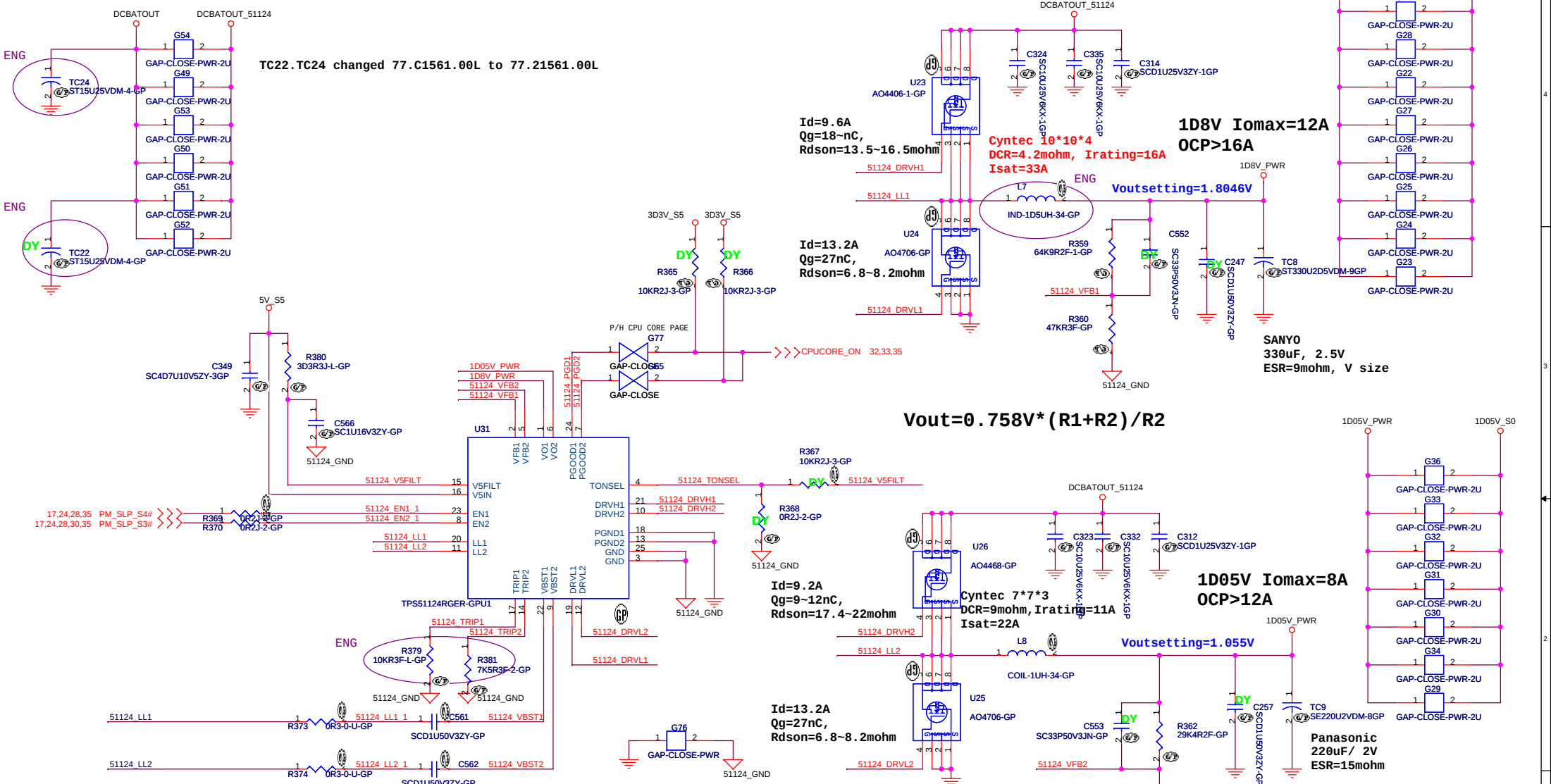
1D5V_S0



Charger MAX8731



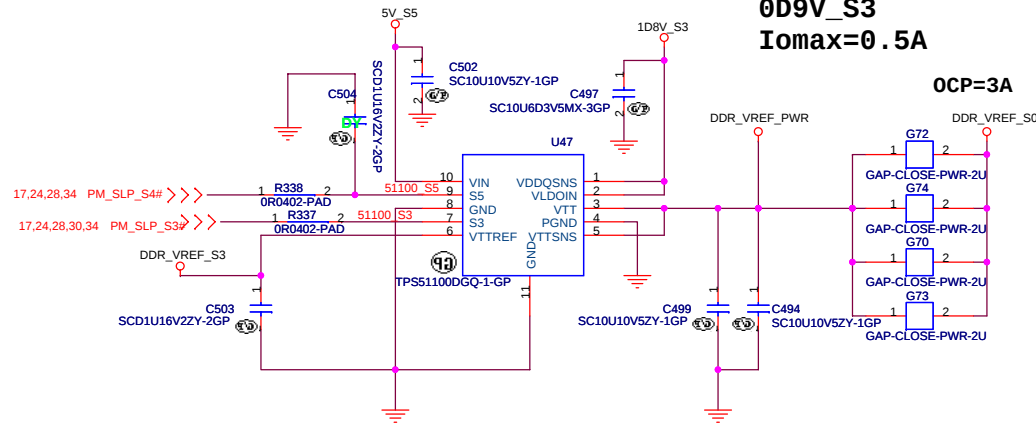




	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

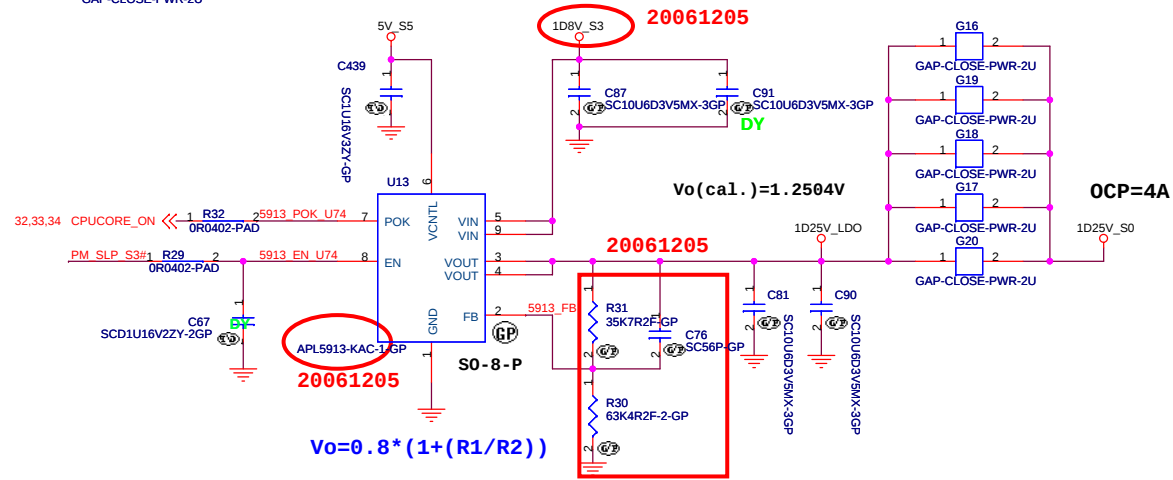
0D9V_S3 Iomax=0.5A

OCP=3A



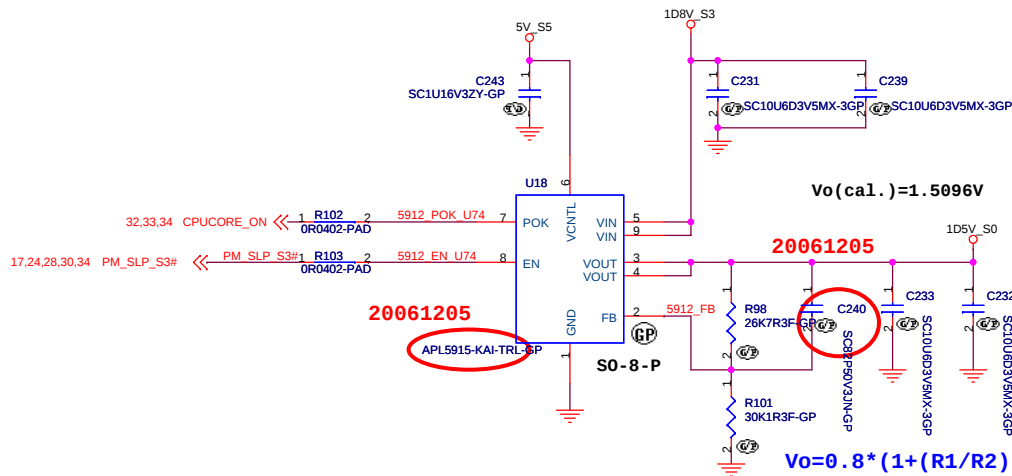
1D25V_S0 Iomax=2A

OCP=4A



$$Vo=0.8*(1+(R1/R2))$$

1D5V_S0 Iomax=1.5A OCP>1.8A



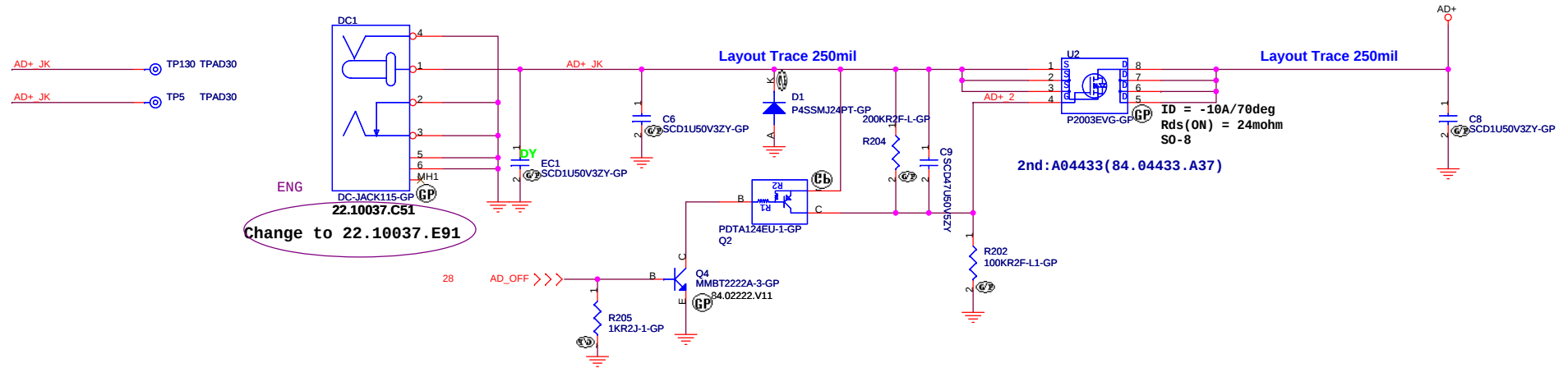
$$Vo=0.8*(1+(R1/R2))$$

ICS

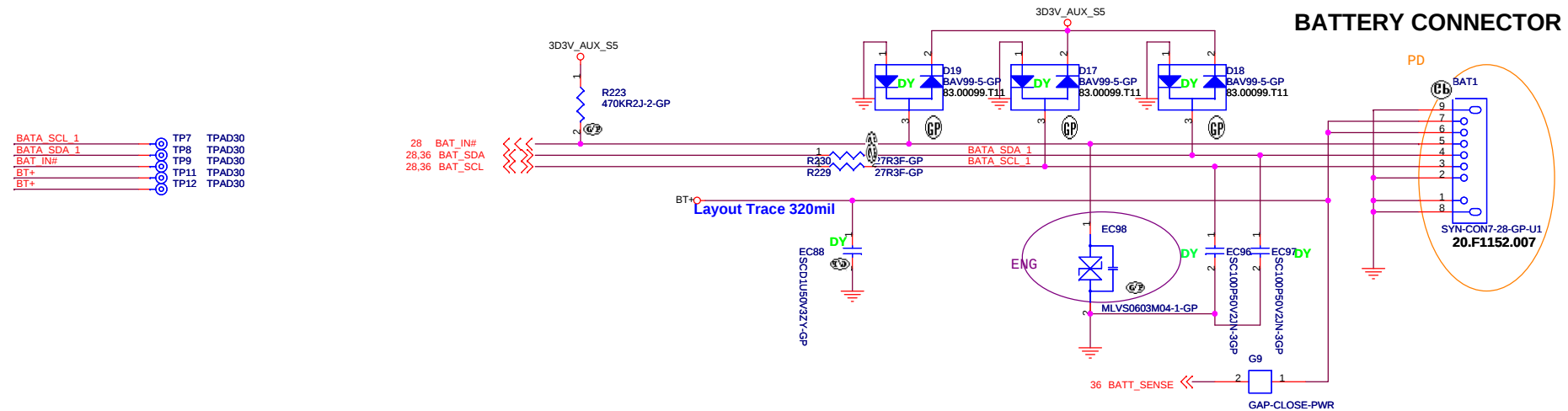
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			0D9V/1D25V/1D5V
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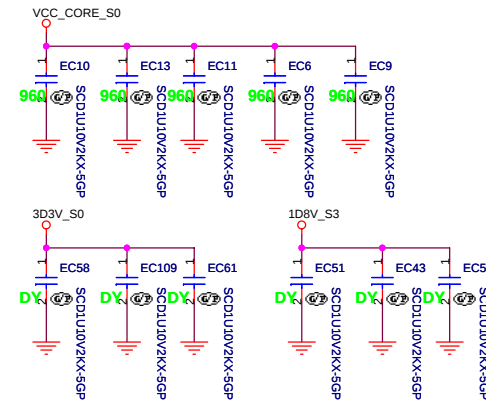
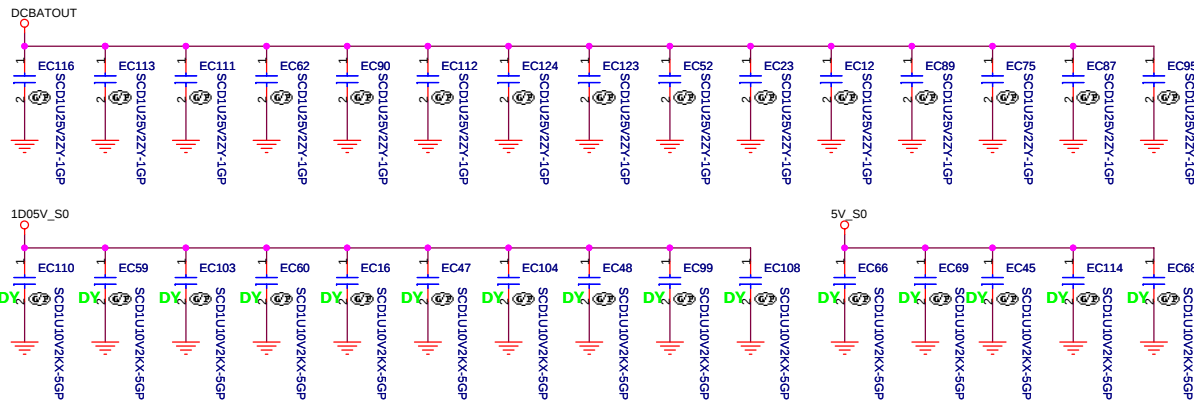
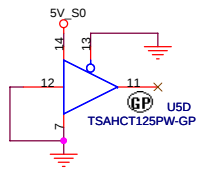
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



ICS

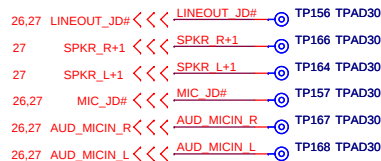


FAN CONN

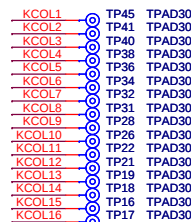


Audio Connector

Internal KeyBoard CONN



Test Point



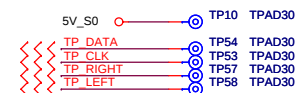
TRING CONN

Test Point



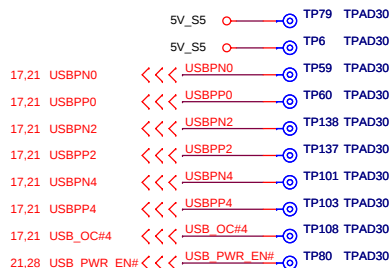
Touch Pad CONN

Test Point near TPAD1

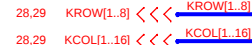


USB ZIF CONN

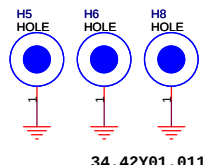
Test Point



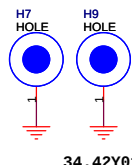
Internal Speaker



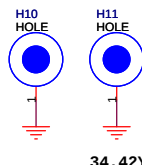
CPU NB MDC MINI CARD



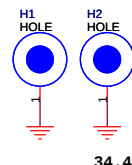
34.42Y01.011



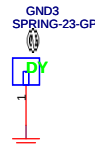
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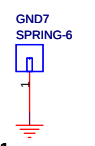
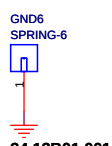
34.42Y01.011



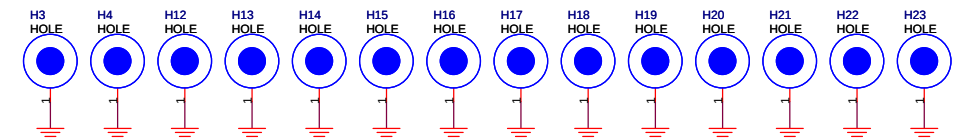
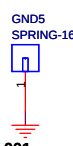
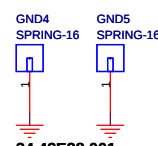
34.46502.001



34.13B01.001



34.43E28.001



34.49U23.001

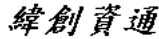


Test Point 放在Dimm Door打開可量測處

ICS		
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Title		
EMI/Spring/Boss		
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SA to SB
1.TC6 change to 900U
2.modify U42(change to G913 300mA) add R417 for TV CRT ripple.
3.add Q27 for BT LED signal
4.change LED1 to 83.01221.I70(right angle)
5.add U55 BLON_5V for LED panel
6.change U1 to 74.04280.C9P for source request
7.add polyswitch F3 for safety.
8.C338 C339 C341 C340 change to 0402 size for SATA signal.
9.FAN1 change to 20.F1000.003 for ME.
10.USB1 swap pin3 pin4 signal.
11.USB2 USB3 change to 22.10218.R31 for ME.
12.add polyswitch F4 F5 for safety.
13.change U4 U45 to 74.09711.B7F ,U56 U57 74.05250.C7F for source request.
14.R20 change to 1.21K for IEEE.
15.C56 change to 12P for Oscillation report.
16.U53 change to 74.09711.A7F for source request.
17.NEW1 change to 20.F07890.026.SK1 change to 21.H0153.001 for ME
18.add R421 LED4 for CardReader test.
19.C237 C229 change to 27P for Oscillation report.
20.R350 change to 4.99K for jack detection.
21.R363 R364 change to 18K.R404 R405 change to 56 ohm for audio report.
22.add AUD_AGND.L24 for audio niose.
23.C575 C577 change to 2700p Cut frequency at 500HZ
24.add BT_LED to KBC GPIO50.
25.add TC19 TC20 TC21 TC22 TC23 TC24 for acoustic noise.
26.C419 change to 1000p for power team.
27.U21 change to 84.04712.037.L9 change to 68.3R310.20A for power team.
28.R151 change to 16.5K.R124 change to 13K for OCP.
29.L7 change to 68.1R510.10J for power team.
30.R379 change to 10K.R381 change to 7.5K for OCP.
31,BAT1 change to 20.80977.007 for ME.
32.EC98 add 69.80007.031 for EC damaged.
33.R402 change to 10K.R397 DY for planar ID.
34.ODD1 change to 20.80967.050 for ME.
35.add G79.G80 for power.
36.R385.R386.R388.R387 change for Gain.R395.R407 change to 56K.
37.add EC6.EC9.EC10.EC11.EC13 to 960 for EMI.
38.add EC41.EC42.EC49.EC50.EC127 for EMI.
39.add R423.R422 for EMI.
40.add RN34.RN35.RN36 for EMI.
41.remove Golden finger
42.swap Touchpad pin define.
43.change L1 L2 to 68.00084.371.
44.change DC1 to 22.10037.E91 for ME.
45.change TVOUT1 to 22.10021.F41 for ME.
SB to -1
1.add AFTE test point for power board Conn.
2.add R432.C583 change G47 to R433 for 3D3V_AUX_S5 power option
3.change to 0 ohm pad for R45.R41.R216.R391.R183.R184.R14.R162.
R78.R79.R74.R87.R73.R77.R390.R21.R194.R187
4.change SPKR1 to 20.D0197.104 for ME.
5.change TRING1 to 21.E0024.102 for ME.
6.remove D7.D8.D9 for EMI.
7.add EC116.EC113.EC111.EC62.EC90.EC112.EC124.EC123.EC52.EC23.EC12.EC89.EC75.EC87.EC95.
8.change R422.R423 to 33 ohm.add EC71.EC72 to 33P for EMI.
9.add EC128.EC129 for EMI.
10.change c419 to 78.10234.1BL for source OBSOLETED.
11.change LEFT1.LEFT2.RIGHT1 to 62.40009.671 for ME.
12.change TVOUT1 to 22.10021.H61 for ME.
13.change BAT1 to 20.F1152.007 for ME.
14.add D26 for EMI.
15.change TC17 to 79.22710.3AL for USB droop test fial.
16.change TC2.EC84 to 5V_USB3_S0_1,change TC17.EC101 to5V_USB2_S0_1 for UPT2 fail.
17.add GND6.GND7.GND8.GND9.GND10.GND11.GND12.GND13 fot EMI.
18.change CRT1 to 20.20378.015 for ME.
19.del GND1.GND2.

ICS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Change List			
Size	Document Number		Rev
	Calado		-1
Date:	Thursday, September 13, 2007		Sheet 39 of 39