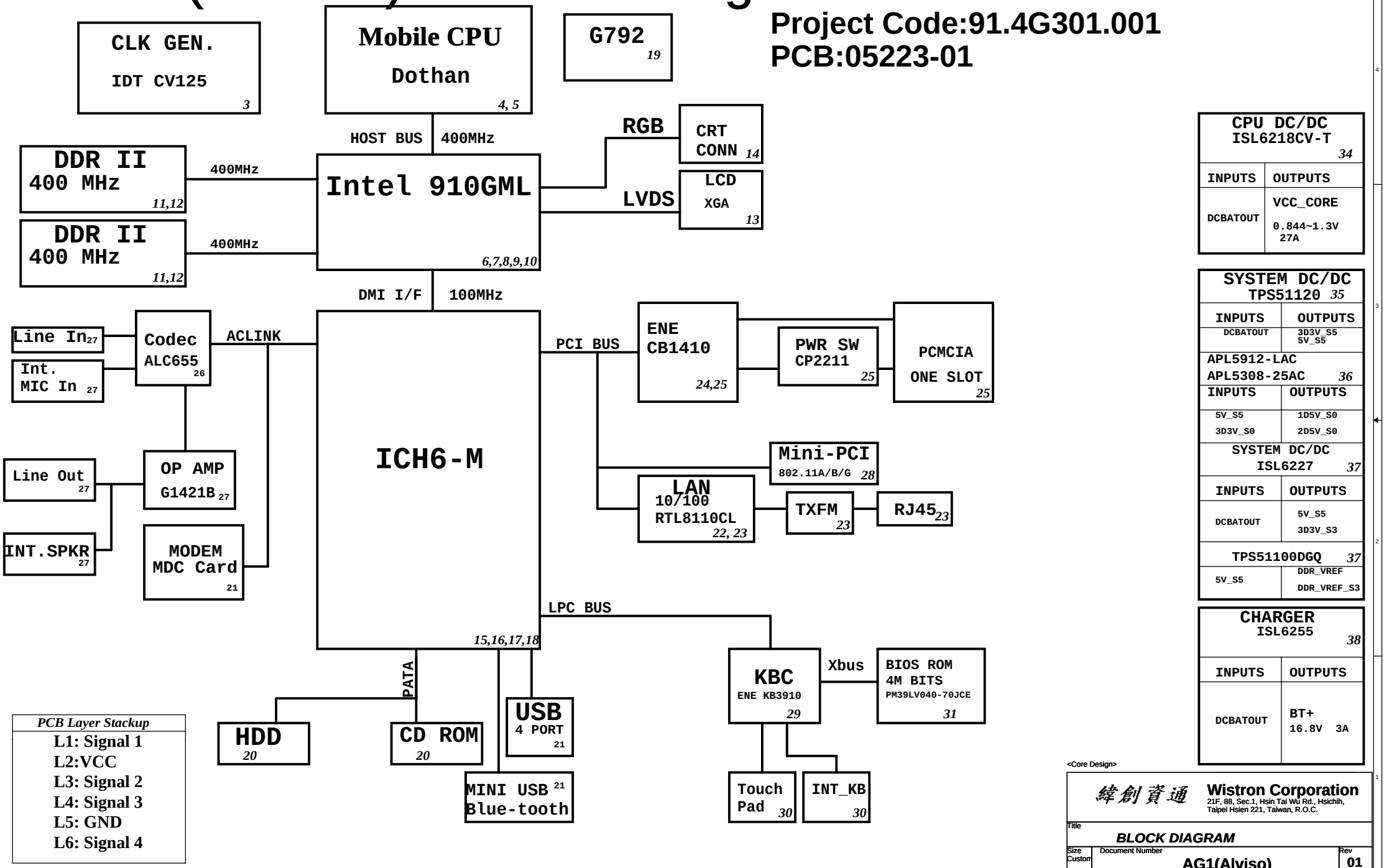
AG1(Alviso) Block Diagram 2005/11/01

Project Code:91.4G301.001
PCB:05223-01



CPU DC/DC
ISL6218CV-T *34*

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

SYSTEM DC/DC
TPS51120 *35*

INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

APL5912-LAC
APL5308-25AC *36*

INPUTS	OUTPUTS
5V_S5 3D3V_S0	1D5V_S0 2D5V_S0

SYSTEM DC/DC
ISL6227 *37*

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S3

TPS51100DGQ *37*

INPUTS	OUTPUTS
5V_S5	DDR_VREF DDR_VREF_S3

CHARGER
ISL6255 *38*

INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

PCB Layer Stackup

L1: Signal 1
L2:VCC
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLOCK DIAGRAM***

Size: Custom | Document Number: **AG1(Alviso)** | Rev: **01**

Date: Tuesday, November 01, 2005 | Sheet 1 of 40

Alviso Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott **1 = Dothan** (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

PCI Routing

	IDSEL	IRQ	REQ/GNT
1410	25	B.F.G	0
MiniPCI	21	F	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

<Core Design>

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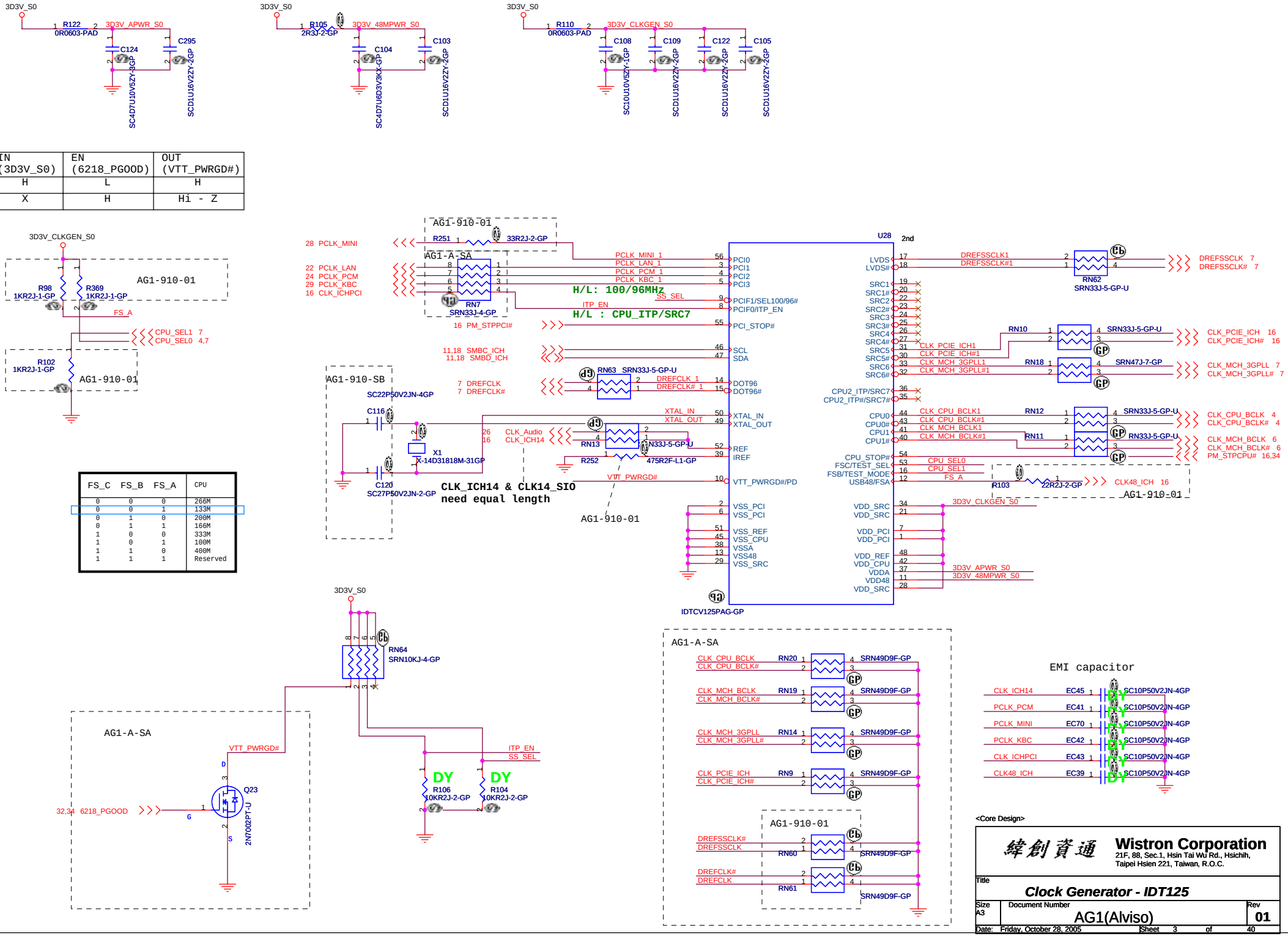
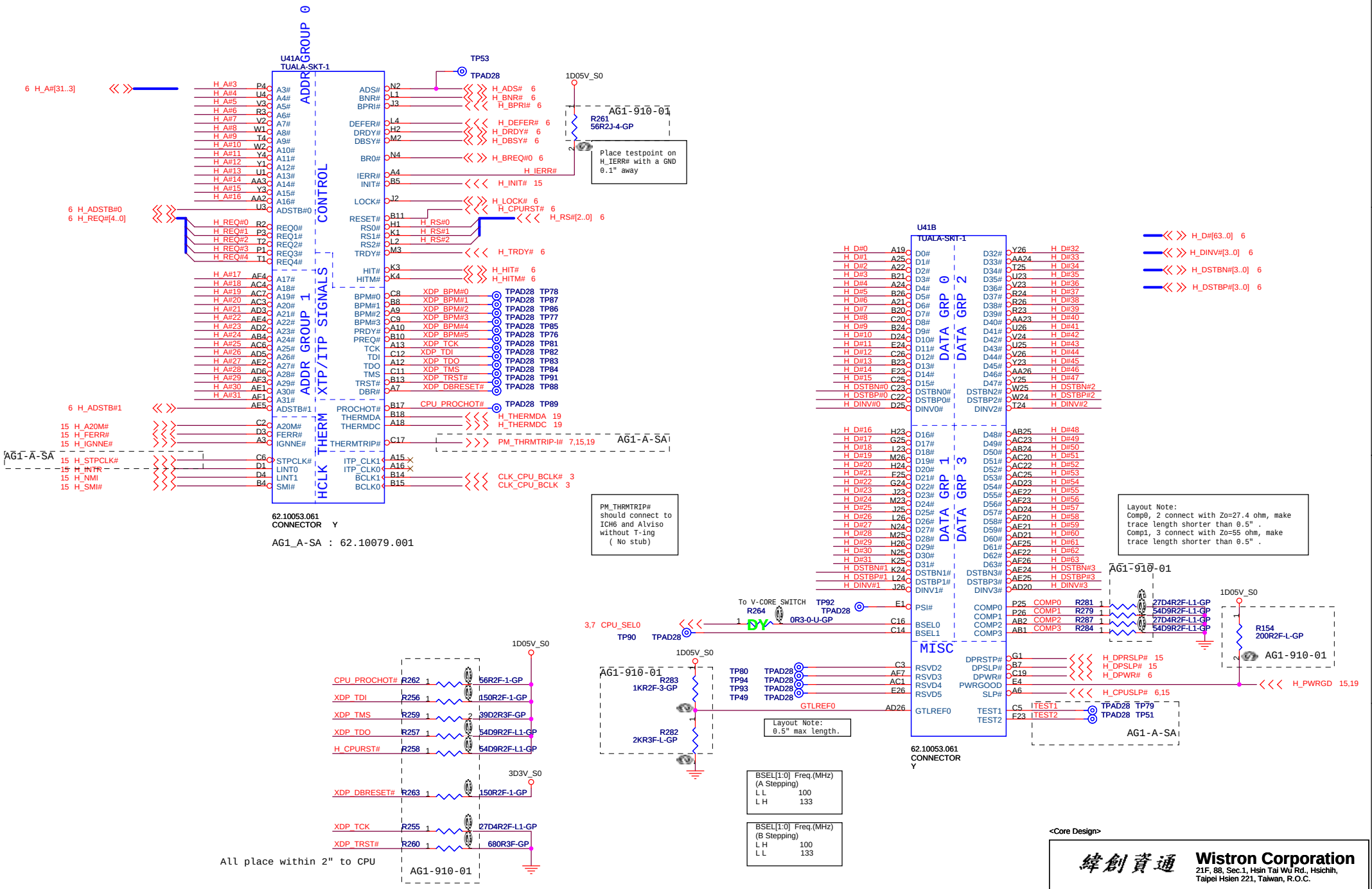
Taipei Hsien 221, Taiwan, R.O.C.

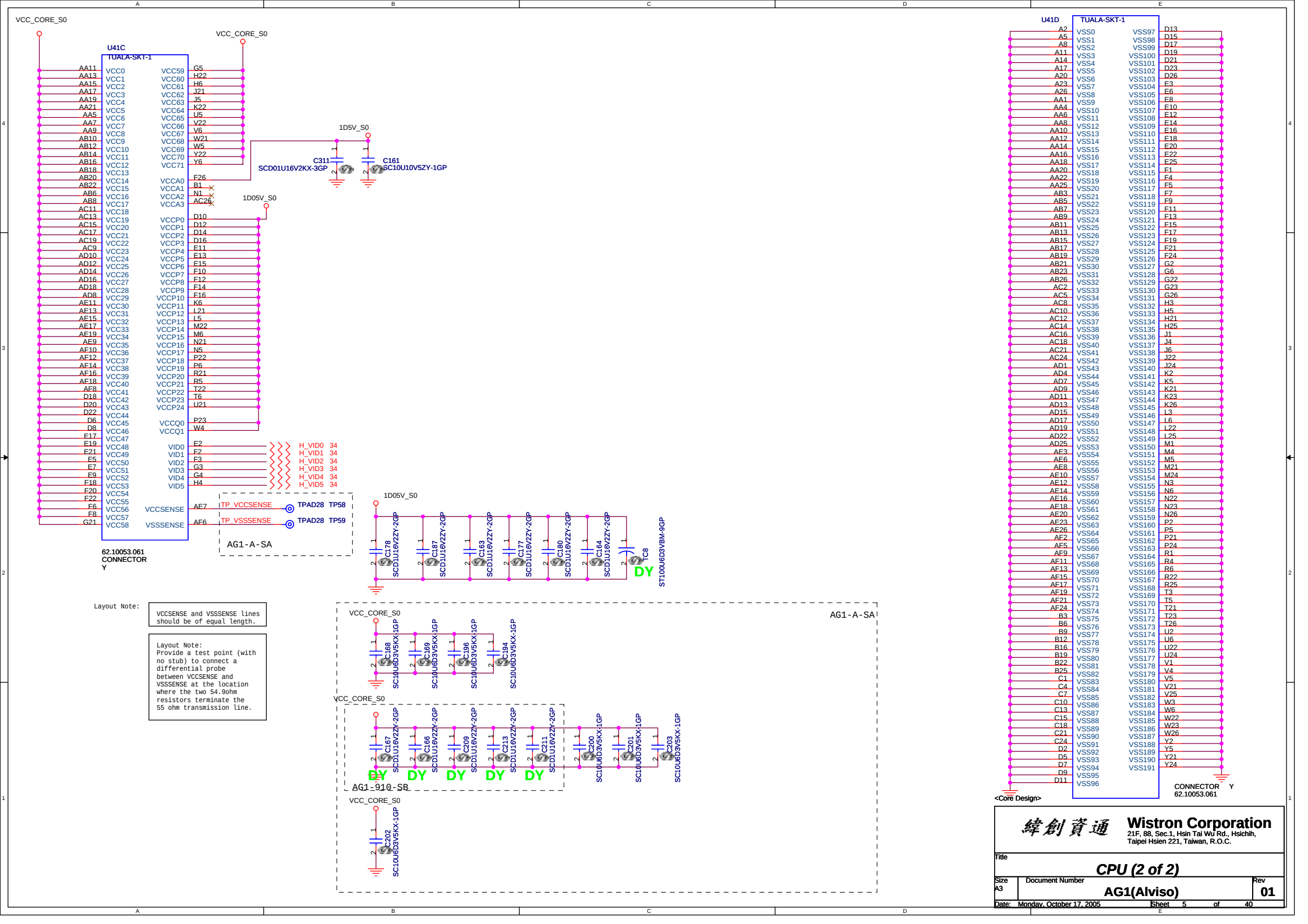
Title: Memo

Size: A3 | Document Number: AG1(Alviso) | Rev: 01

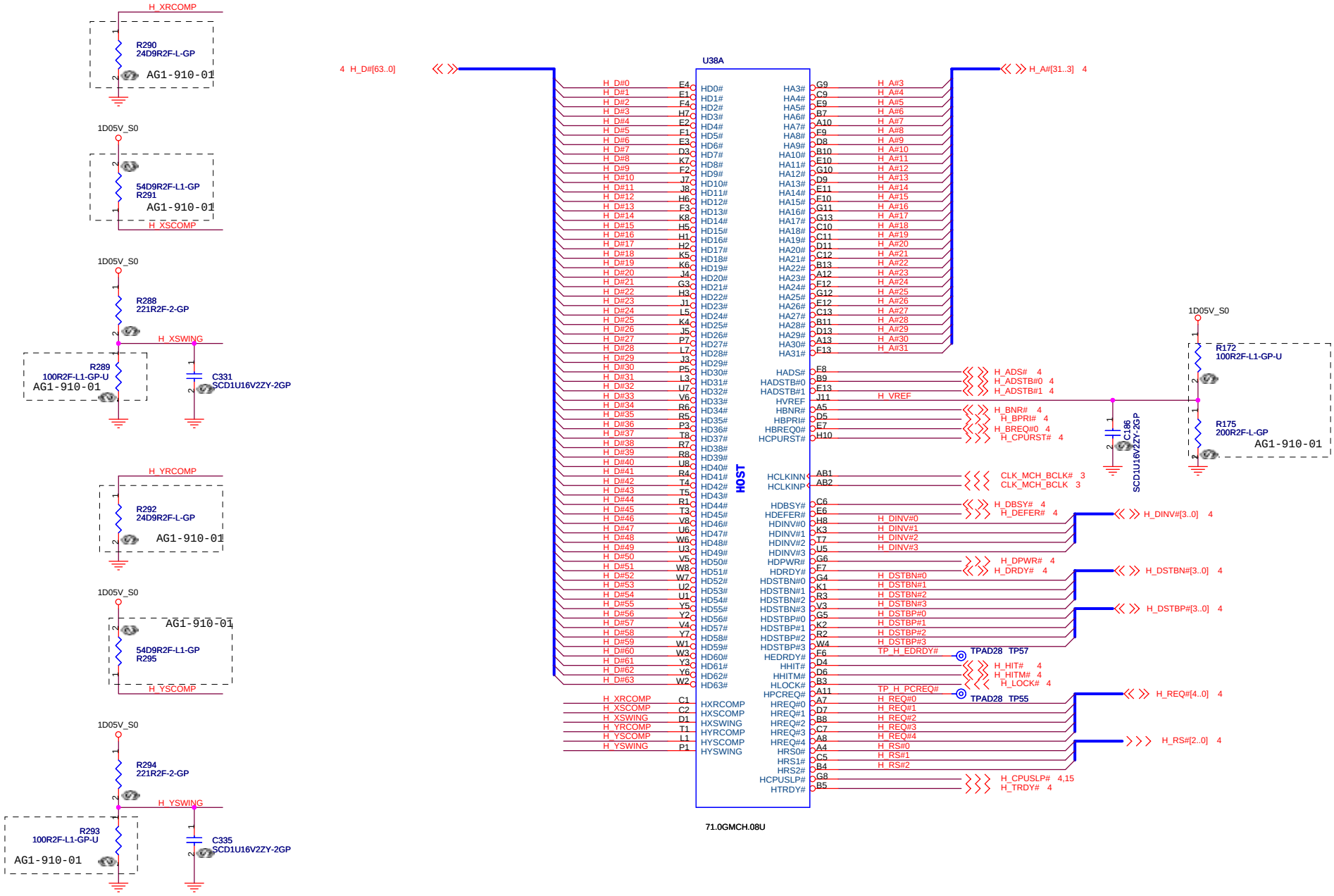
Date: Tuesday, November 01, 2005 | Sheet 2 of 40


3D3V_S0
R122 0R0603-PAD
3D3V_APWR_S0
C124
C295
SC4D7U10V5ZY-3GP
SCD1U16V2ZY-2GP
R105 2R3J-2-GP
3D3V_48MPWR_S0
C104
C103
SC4D7U6D3V3KX-GP
SCD1U16V2ZY-2GP
R110 0R0603-PAD
3D3V_CLKGEN_S0
C108
C109
C122
C105
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
IN (3D3V_S0) | EN (6218_PGOOD) | OUT (VTT_PWRGD#)
H | L | H
X | H | Hi - Z
3D3V_CLKGEN_S0
AG1-910-01
R98 1KR2J-1-GP
R369 1KR2J-1-GP
FS_A
CPU_SEL1 7
CPU_SEL0 4,7
R102 1KR2J-1-GP
AG1-910-01
FS_C FS_B FS_A CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved
AG1-910-01
R251 33R2J-2-GP
28 PCLK_MINI
AG1-A-SA
22 PCLK_LAN
24 PCLK_PCM
29 PCLK_KBC
16 CLK_ICHPCI
RN7 SRN33J-4-GP
PCLK_MINI_1
PCLK_LAN_1
PCLK_PCM_1
PCLK_KBC_1
H/L: 100/96MHz
SS_SEL
ITP_EN
H/L : CPU_ITP/SRC7
16 PM_STPPCI#
11,18 SMBC_ICH
11,18 SMBD_ICH
7 DREFCLK
7 DREFCLK#
RN63 SRN33J-5-GP-U
DREFCLK_1
DREFCLK#_1
AG1-910-SB
SC22P50V2JN-4GP
C116
X1
X-14D31818M-31GP
C120
SC27P50V2JN-2GP
26 CLK_Audio
16 CLK_ICH14
RN13 SRN33J-5-GP-U
R252 475R2F-L1-GP
XTAL_IN
XTAL_OUT
REF
IREF
VTT_PWRGD#
CLK_ICH14 & CLK14_SIO need equal length
AG1-910-01
PCI0
PCI1
PCI2
PCI3
PCIF1/SEL100/96#
PCIF0/ITP_EN
PCI_STOP#
SCL
SDA
DOT96
DOT96#
XTAL_IN
XTAL_OUT
REF
IREF
VTT_PWRGD#/PD
VSS_PCI
VSS_PCI
VSS_REF
VSS_CPU
VSSA
VSS48
VSS_SRC
IDTCV125PAG-GP
U28
2nd
LVDS
LVDS#
DREFSSCLK1
DREFSSCLK#1
RN62 SRN33J-5-GP-U
DREFSSCLK 7
DREFSSCLK# 7
SRC1
SRC1#
SRC2
SRC2#
SRC3
SRC3#
SRC4
SRC4#
SRC5
SRC5#
SRC6
SRC6#
CLK_PCIE_ICH1
CLK_PCIE_ICH#1
CLK_MCH_3GPLL1
CLK_MCH_3GPLL#1
RN10 SRN33J-5-GP-U
RN18 SRN47J-7-GP
CLK_PCIE_ICH 16
CLK_PCIE_ICH# 16
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
CPU2_ITP/SRC7
CPU2_ITP#/SRC7#
CPU0
CPU0#
CPU1
CPU1#
CLK_CPU_BCLK1
CLK_CPU_BCLK#1
CLK_MCH_BCLK1
CLK_MCH_BCLK#1
RN12 SRN33J-5-GP-U
RN11 SRN33J-5-GP-U
CLK_CPU_BCLK 4
CLK_CPU_BCLK# 4
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
PM_STPCPU# 16,34
CPU_STOP#
FSC/TEST_SEL
FSB/TEST_MODE
USB48/FSA
CPU_SEL0
CPU_SEL1
FS_A
R103 22R2J-2-GP
CLK48_ICH 16
AG1-910-01
VDD_SRC
VDD_SRC
VDD_PCI
VDD_PCI
VDD_REF
VDD_CPU
VDDA
VDD48
VDD_SRC
3D3V_CLKGEN_S0
3D3V_APWR_S0
3D3V_48MPWR_S0
3D3V_S0
RN64 SRN10KJ-4-GP
AG1-A-SA
VTT_PWRGD#
Q23
2N7002PT-U
32,34 6218_PGOOD
ITP_EN
SS_SEL
DY
R106 10KR2J-2-GP
R104 10KR2J-2-GP
AG1-A-SA
CLK_CPU_BCLK
CLK_CPU_BCLK#
RN20 SRN49D9F-GP
CLK_MCH_BCLK
CLK_MCH_BCLK#
RN19 SRN49D9F-GP
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
RN14 SRN49D9F-GP
CLK_PCIE_ICH
CLK_PCIE_ICH#
RN9 SRN49D9F-GP
AG1-910-01
DREFSSCLK#
DREFSSCLK
RN60 SRN49D9F-GP
DREFCLK#
DREFCLK
RN61 SRN49D9F-GP
EMI capacitor
CLK_ICH14 EC45 SC10P50V2JN-4GP
PCLK_PCM EC41 SC10P50V2JN-4GP
PCLK_MINI EC70 SC10P50V2JN-4GP
PCLK_KBC EC42 SC10P50V2JN-4GP
CLK_ICHPCI EC43 SC10P50V2JN-4GP
CLK48_ICH EC39 SC10P50V2JN-4GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator - IDT125
Size A3
Document Number
AG1(Alviso)
Rev
01
Date: Friday, October 28, 2005
Sheet 3 of 40


U41A
TUALA-SKT-1
ADDR GROUP 0
ADDR GROUP 1
XTP/ITP SIGNALS
CONTROL
HCLK THERM
TP53
TPAD28
1D05V_S0
AG1-910-01
R261
56R2J-4-GP
Place testpoint on H_IERR# with a GND 0.1" away
AG1-A-SA
62.10053.061
CONNECTOR Y
AG1_A_SA : 62.10079.001
PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)
U41B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
To V-CORE_SWITCH
R264
0R3-0-U-GP
TP92
TP90
3,7 CPU_SEL0
R154
200R2F-L-GP
27D4R2F-L-GP
54D9R2F-L-GP
R283
1KR2F-3-GP
R282
2KR3F-L-GP
GTLREF0
Layout Note: 0.5" max length.
BSEL[1:0] Freq.(MHz) (A Stepping)
L L 100
L H 133
BSEL[1:0] Freq.(MHz) (B Stepping)
L H 100
L L 133
All place within 2" to CPU
3D3V_S0
56R2F-1-GP
150R2F-1-GP
39D2R3F-GP
680R3F-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (1 of 2)
Size A3
Document Number AG1(Alviso)
Rev 01
Date: Monday, October 31, 2005
Sheet 4 of 40



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU (2 of 2)***
Size: A3	Document Number: **AG1(Alviso)**
Rev:	**01**
Date: Monday, October 17, 2005	Sheet 5 of 40



Place them near to the chip

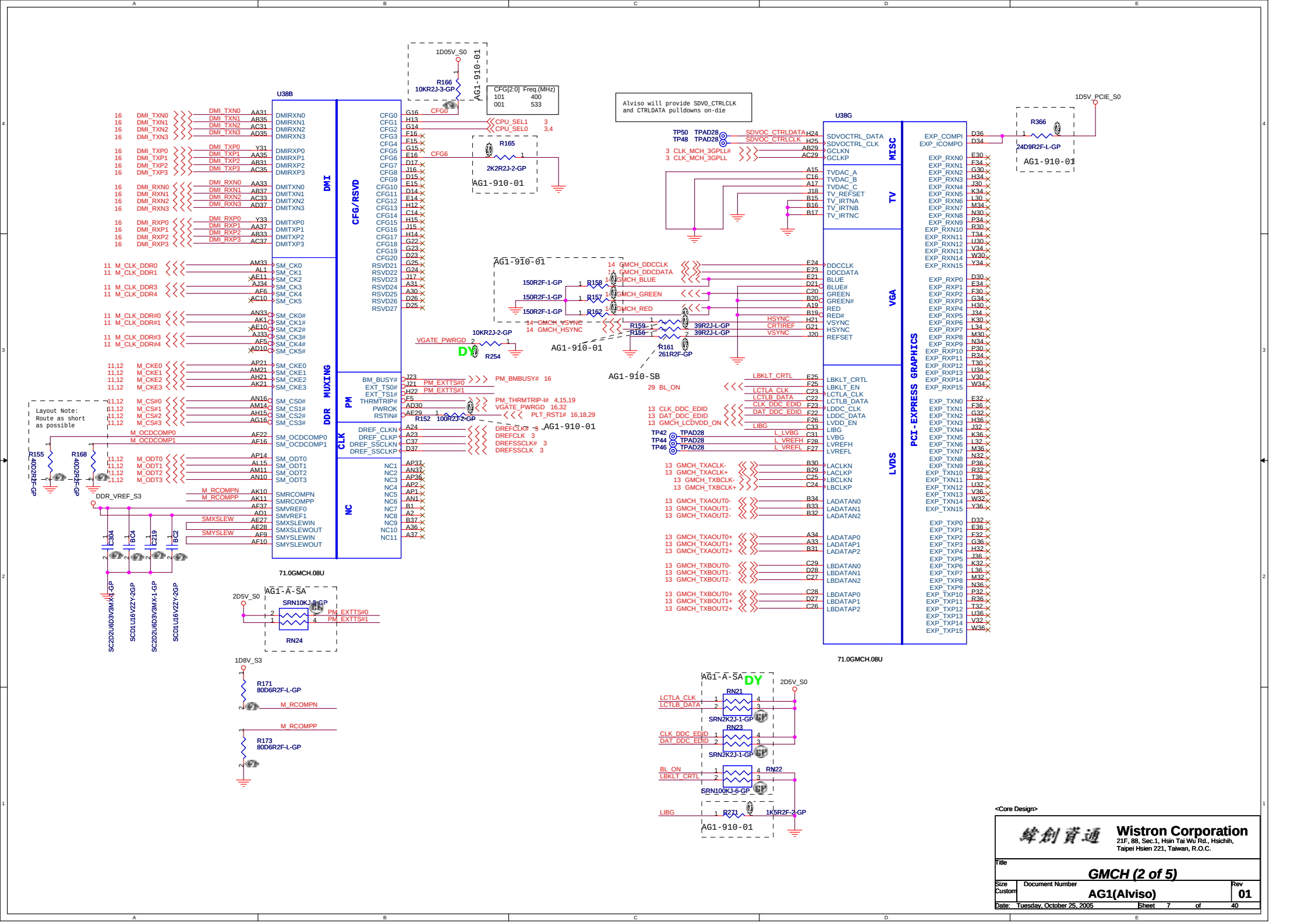
<Core Design>

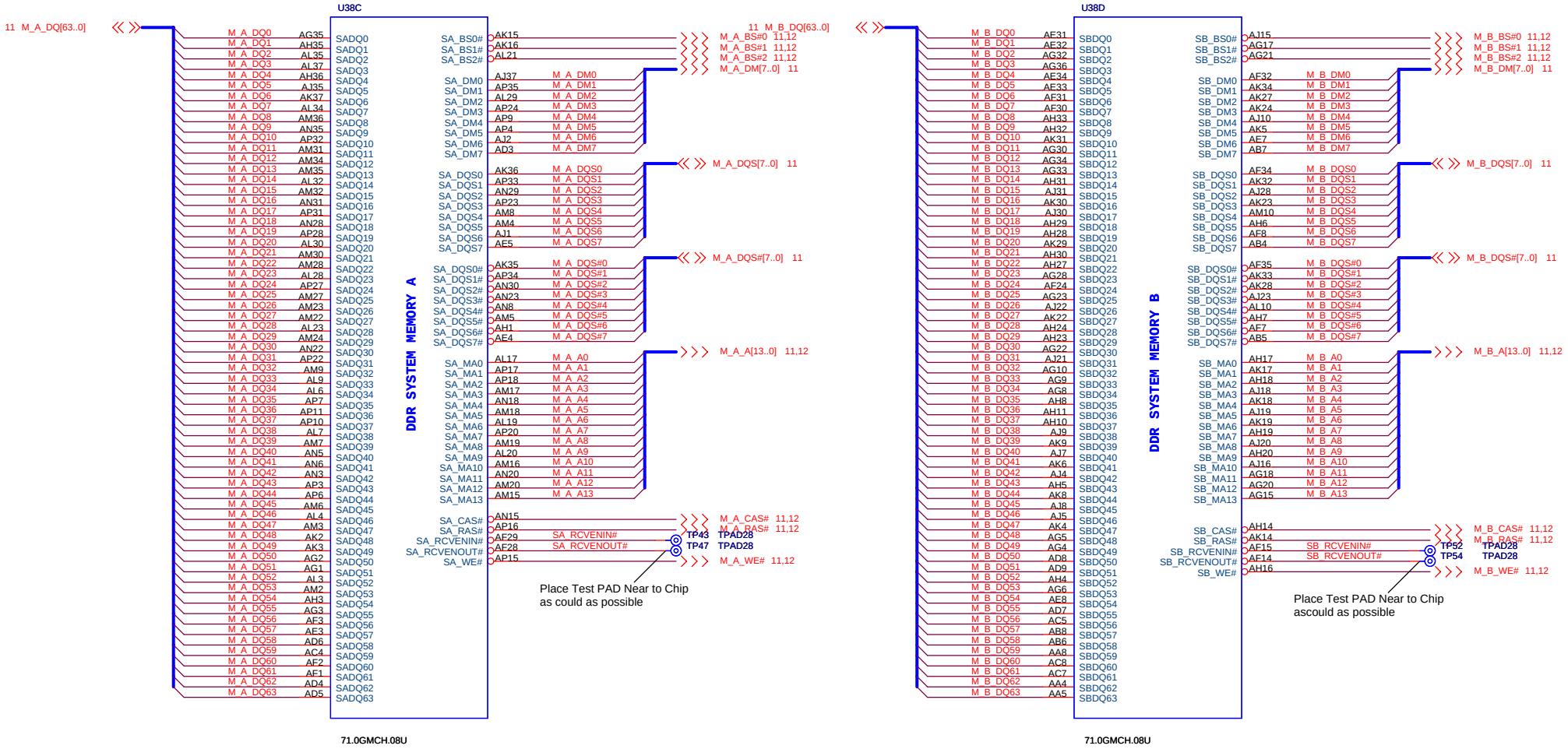
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GMCH (1 of 5)***

Size	Document Number	Rev
A3	AG1(Alviso)	01

Date: Tuesday, October 25, 2005 Sheet 6 of 40


U38B
DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
DMI_TXN0
DMI_TXN1
DMI_TXN2
DMI_TXN3
DMI_TXP0
DMI_TXP1
DMI_TXP2
DMI_TXP3
DMI_RXN0
DMI_RXN1
DMI_RXN2
DMI_RXN3
DMI_RXP0
DMI_RXP1
DMI_RXP2
DMI_RXP3
DMIRXN0
DMIRXN1
DMIRXN2
DMIRXN3
DMIRXP0
DMIRXP1
DMIRXP2
DMIRXP3
DMITXN0
DMITXN1
DMITXN2
DMITXN3
DMITXP0
DMITXP1
DMITXP2
DMITXP3
CFG0
CFG1
CFG2
CFG3
CFG4
CFG5
CFG6
CFG7
CFG8
CFG9
CFG10
CFG11
CFG12
CFG13
CFG14
CFG15
CFG16
CFG17
CFG18
CFG19
CFG20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
1D05V_S0
R166
10KR2J-3-GP
AG1-910-01
CFG[2:0] Freq.(MHz)
101 400
001 533
CPU_SEL1
CPU_SEL0
R165
2K2R2J-2-GP
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR3
M_CLK_DDR4
M_CLK_DDR#0
M_CLK_DDR#1
M_CLK_DDR#3
M_CLK_DDR#4
SM_CK0
SM_CK1
SM_CK2
SM_CK3
SM_CK4
SM_CK5
SM_CK0#
SM_CK1#
SM_CK2#
SM_CK3#
SM_CK4#
SM_CK5#
M_CKE0
M_CKE1
M_CKE2
M_CKE3
SM_CKE0
SM_CKE1
SM_CKE2
SM_CKE3
M_CS#0
M_CS#1
M_CS#2
M_CS#3
SM_CS0#
SM_CS1#
SM_CS2#
SM_CS3#
M_ODCOMP0
M_ODCOMP1
SM_OCDCOMP0
SM_OCDCOMP1
M_ODT0
M_ODT1
M_ODT2
M_ODT3
SM_ODT0
SM_ODT1
SM_ODT2
SM_ODT3
M_RCOMPN
M_RCOMPP
SMRCOMPN
SMRCOMPP
SMVREF0
SMVREF1
SMXSLEWIN
SMXSLEWOUT
SMYSLEWIN
SMYSLEWOUT
SMXSLEW
SMYSLEW
Layout Note:
Route as short
as possible
R155
R168
40D2R2F-GP
DDR_VREF_S3
C304
C4
C219
C2
SC2D2U6D3V3MX-1-GP
SCD1U16V2ZY-2GP
71.0GMCH.08U
BM_BUSY#
EXT_TS0#
EXT_TS1#
THRMTRIP#
PWROK
RSTIN#
PM_BMBUSY# 16
PM_EXTTS#0
PM_EXTTS#1
PM_THRMTRIP-I# 4,15,19
VGATE_PWRGD 16,32
PLT_RST1# 16,18,29
R152
100R2J-2-GP
DREF_CLKN
DREF_CLKP
DREF_SSCLKN
DREF_SSCLKP
DREFCLK# 3
DREFCLK 3
DREFSSCLK# 3
DREFSSCLK 3
AG1-A-SA
2D5V_S0
SRN10KJ-5-GP
RN24
1D8V_S3
R171
80D6R2F-L-GP
R173
80D6R2F-L-GP
M_RCOMPN
M_RCOMPP
Alviso will provide SDVO_CTRLCLK
and CTRLDATA pulldowns on-die
U38G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
SDVOCTRL_DATA
SDVOCTRL_CLK
GCLKN
GCLKP
TVDAC_A
TVDAC_B
TVDAC_C
TV_REFSET
TV_IRTNA
TV_IRTNB
TV_IRTNC
DDCCLK
DDCDATA
BLUE
BLUE#
GREEN
GREEN#
RED
RED#
VSYNC
HSYNC
REFSET
LBKLT_CRTL
LBKLT_EN
LCTLA_CLK
LCTLB_DATA
LDDC_CLK
LDDC_DATA
LVDD_EN
LIBG
LVBG
LVREFH
LVREFL
LACLKN
LACLKP
LBCLKN
LBCLKP
LADATAN0
LADATAN1
LADATAN2
LADATAP0
LADATAP1
LADATAP2
LBDATAN0
LBDATAN1
LBDATAN2
LBDATAP0
LBDATAP1
LBDATAP2
EXP_COMPI
EXP_ICOMPO
EXP_RXN0
EXP_RXN1
EXP_RXN2
EXP_RXN3
EXP_RXN4
EXP_RXN5
EXP_RXN6
EXP_RXN7
EXP_RXN8
EXP_RXN9
EXP_RXN10
EXP_RXN11
EXP_RXN12
EXP_RXN13
EXP_RXN14
EXP_RXN15
EXP_RXP0
EXP_RXP1
EXP_RXP2
EXP_RXP3
EXP_RXP4
EXP_RXP5
EXP_RXP6
EXP_RXP7
EXP_RXP8
EXP_RXP9
EXP_RXP10
EXP_RXP11
EXP_RXP12
EXP_RXP13
EXP_RXP14
EXP_RXP15
EXP_TXN0
EXP_TXN1
EXP_TXN2
EXP_TXN3
EXP_TXN4
EXP_TXN5
EXP_TXN6
EXP_TXN7
EXP_TXN8
EXP_TXN9
EXP_TXN10
EXP_TXN11
EXP_TXN12
EXP_TXN13
EXP_TXN14
EXP_TXN15
EXP_TXP0
EXP_TXP1
EXP_TXP2
EXP_TXP3
EXP_TXP4
EXP_TXP5
EXP_TXP6
EXP_TXP7
EXP_TXP8
EXP_TXP9
EXP_TXP10
EXP_TXP11
EXP_TXP12
EXP_TXP13
EXP_TXP14
EXP_TXP15
1D5V_PCIE_S0
R366
24D9R2F-L-GP
AG1-910-01
71.0GMCH.08U
AG1-910-SB
GMCH_DDCCLK
GMCH_DDCDATA
GMCH_BLUE
GMCH_GREEN
GMCH_RED
GMCH_VSYNC
GMCH_HSYNC
150R2F-1-GP
R158
R157
R152
R159
R156
39R2J-L-GP
R161
261R2F-GP
R254
10KR2J-2-GP
VGATE_PWRGD
DY
BL_ON
CLK_DDC_EDID
DAT_DDC_EDID
GMCH_LCDVDD_ON
TP42
TP44
TP46
TPAD28
L_LVBG
L_VREFH
L_VREFL
GMCH_TXACLK-
GMCH_TXACLK+
GMCH_TXBCLK-
GMCH_TXBCLK+
GMCH_TXAOUT0-
GMCH_TXAOUT1-
GMCH_TXAOUT2-
GMCH_TXAOUT0+
GMCH_TXAOUT1+
GMCH_TXAOUT2+
GMCH_TXBOUT0-
GMCH_TXBOUT1-
GMCH_TXBOUT2-
GMCH_TXBOUT0+
GMCH_TXBOUT1+
GMCH_TXBOUT2+
TP50
TP48
SDVOC_CTRLDATA
SDVOC_CTRLCLK
CLK_MCH_3GPLL#
CLK_MCH_3GPLL
AG1-A-SA
DY
2D5V_S0
RN21
RN23
RN22
SRN2K2J-1-GP
SRN100KJ-6-GP
LCTLA_CLK
LCTLB_DATA
CLK_DDC_EDID
DAT_DDC_EDID
BL_ON
LBKLT_CRTL
LIBG
R271
1K5R2F-2-GP
AG1-910-01
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (2 of 5)
Size
Custom
Document Number
AG1(Alviso)
Rev
01
Date: Tuesday, October 25, 2005
Sheet 7 of 40



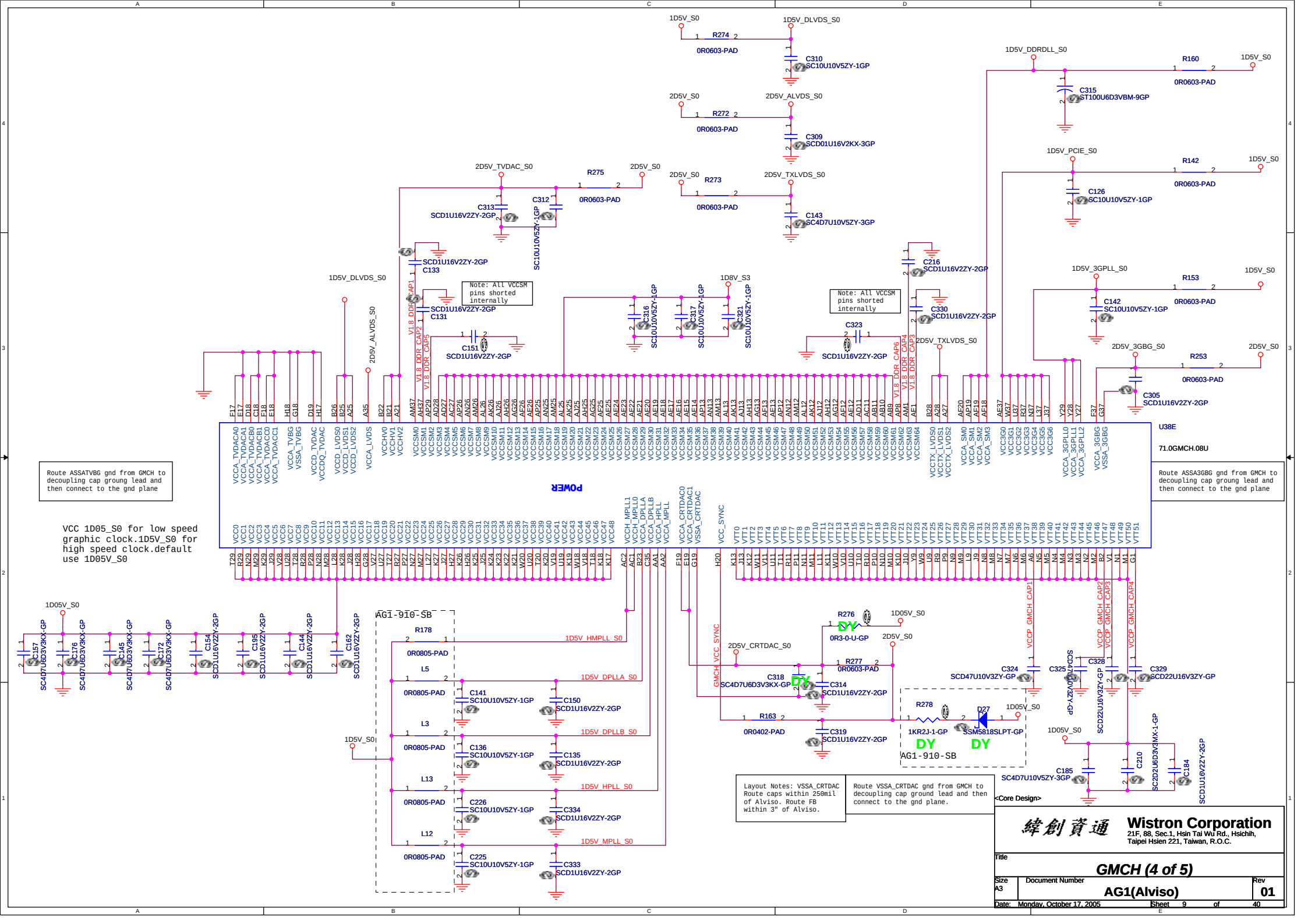
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GMCH (3 of 5)***

Size	Document Number	Rev
A3	AG1(Alviso)	01

Date: Monday, October 17, 2005 Sheet 8 of 40

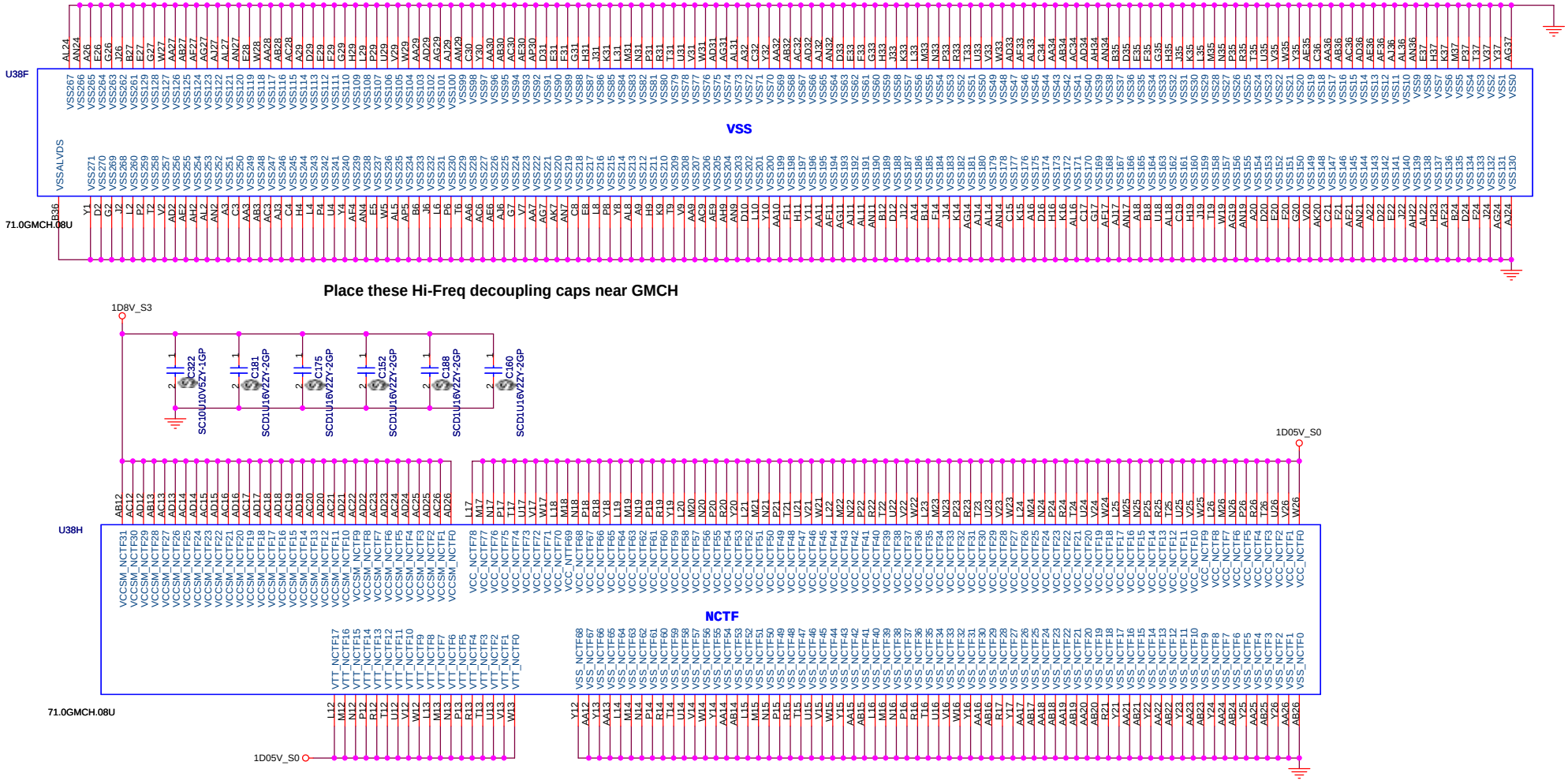


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (4 of 5)

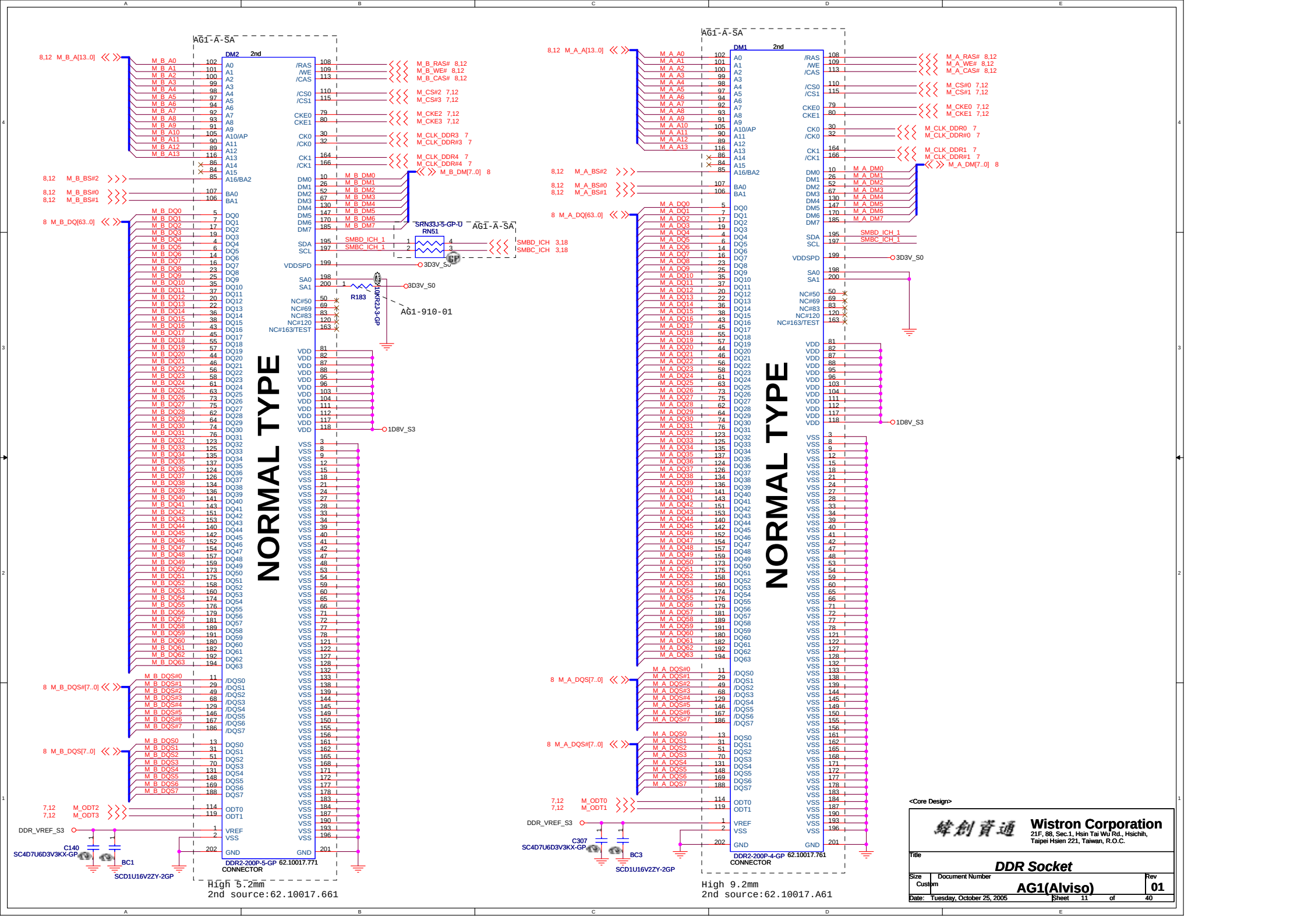
Size	Document Number	Rev
A3	AG1(Alviso)	01

Date: Monday, October 17, 2005 Sheet 9 of 40



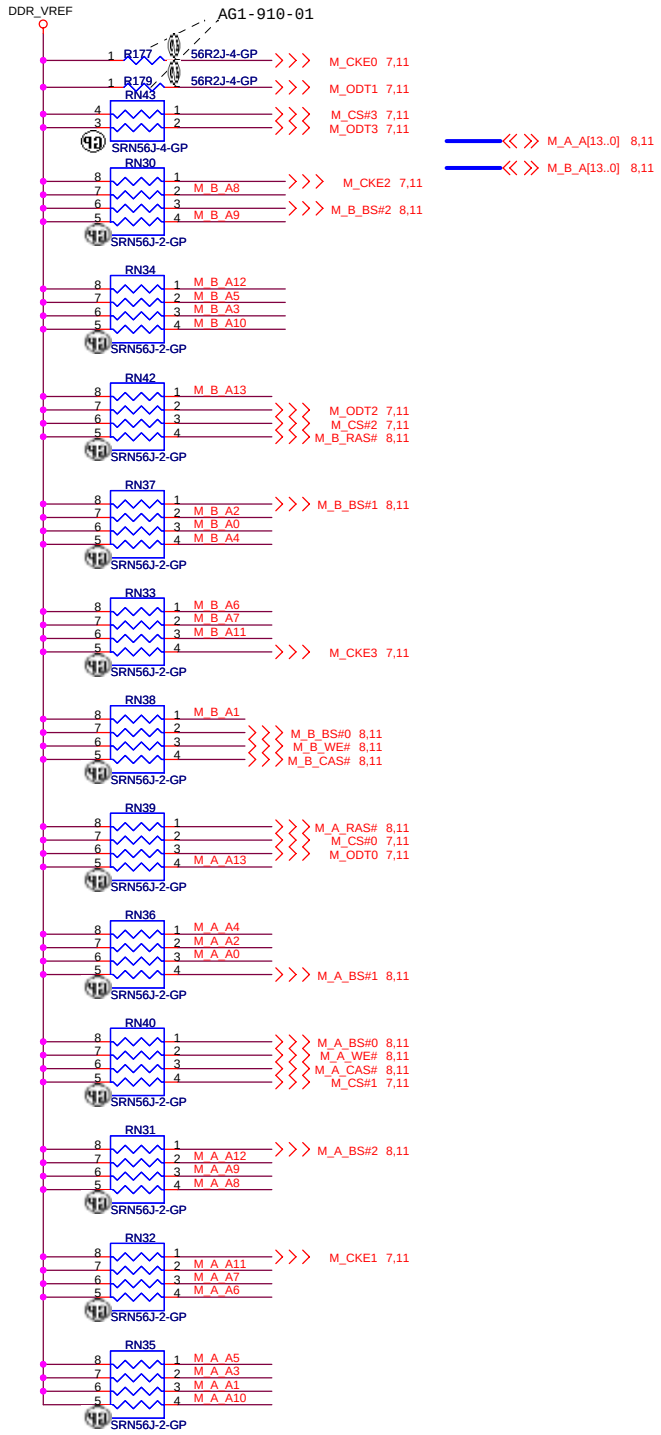
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GMCH (5 of 5)***
Size: A3	Document Number: **AG1(Alviso)**
Rev: 01	
Date: Monday, October 17, 2005	Sheet 10 of 40

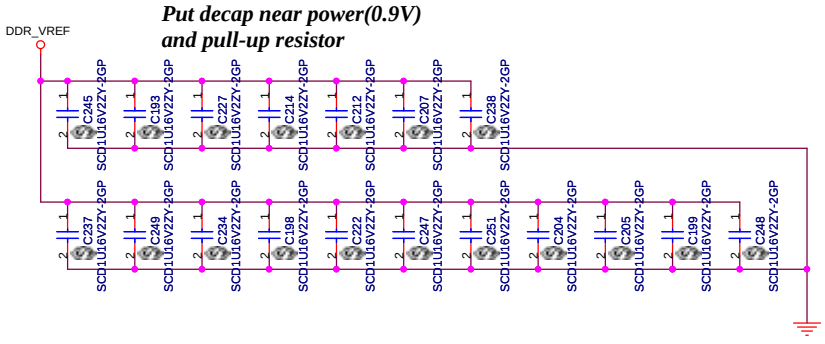

AG1-A-SA
DM2
2nd
NORMAL TYPE
M_B_A[13..0]
M_B_DQ[63..0]
M_B_DQS#[7..0]
M_B_DQS[7..0]
M_B_BS#2
M_B_BS#0
M_B_BS#1
M_ODT2
M_ODT3
DDR_VREF_S3
C140
SC4D7U6D3V3KX-GP
BC1
SCD1U16V2ZY-2GP
M_B_RAS# 8,12
M_B_WE# 8,12
M_B_CAS# 8,12
M_CS#2 7,12
M_CS#3 7,12
M_CKE2 7,12
M_CKE3 7,12
M_CLK_DDR3 7
M_CLK_DDR#3 7
M_CLK_DDR4 7
M_CLK_DDR#4 7
M_B_DM[7..0] 8
SMBD_ICH_1
SMBC_ICH_1
SMBD_ICH 3,18
SMBC_ICH 3,18
SRN33J-5-GP-U
RN51
3D3V_S0
R183
10KR2J-3-GP
AG1-910-01
1D8V_S3
DDR2-200P-5-GP 62.10017.771
CONNECTOR
High 5.2mm
2nd source:62.10017.661
AG1-A-SA
DM1
2nd
NORMAL TYPE
M_A_A[13..0]
M_A_DQ[63..0]
M_A_DQS[7..0]
M_A_DQS#[7..0]
M_A_BS#2
M_A_BS#0
M_A_BS#1
M_ODT0
M_ODT1
DDR_VREF_S3
C307
SC4D7U6D3V3KX-GP
BC3
SCD1U16V2ZY-2GP
M_A_RAS# 8,12
M_A_WE# 8,12
M_A_CAS# 8,12
M_CS#0 7,12
M_CS#1 7,12
M_CKE0 7,12
M_CKE1 7,12
M_CLK_DDR0 7
M_CLK_DDR#0 7
M_CLK_DDR1 7
M_CLK_DDR#1 7
M_A_DM[7..0] 8
SMBD_ICH_1
SMBC_ICH_1
3D3V_S0
1D8V_S3
DDR2-200P-4-GP 62.10017.761
CONNECTOR
High 9.2mm
2nd source:62.10017.A61
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR Socket
Size
Custom
Document Number
AG1(Alviso)
Rev
01
Date: Tuesday, October 25, 2005
Sheet 11 of 40

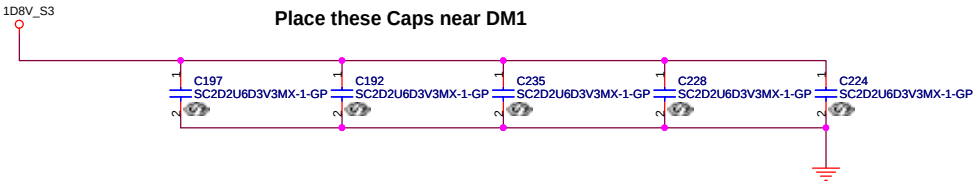
PARALLEL TERMINATION

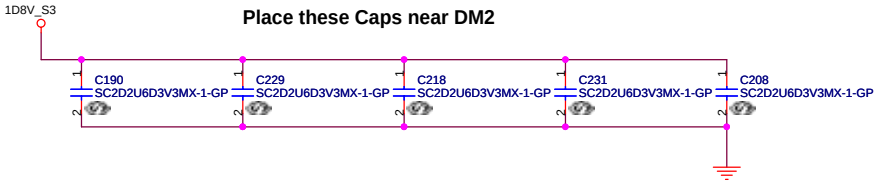
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor







<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	AG1(Alviso)	01

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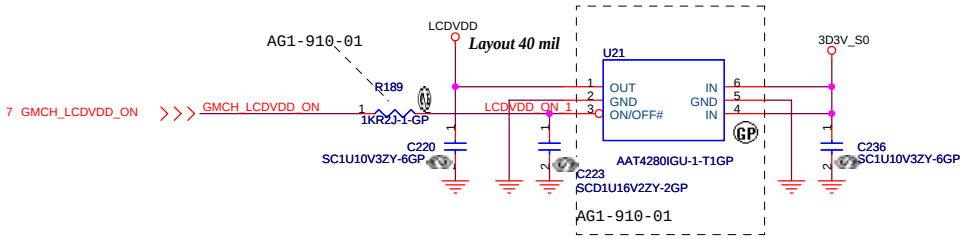
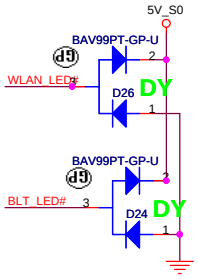
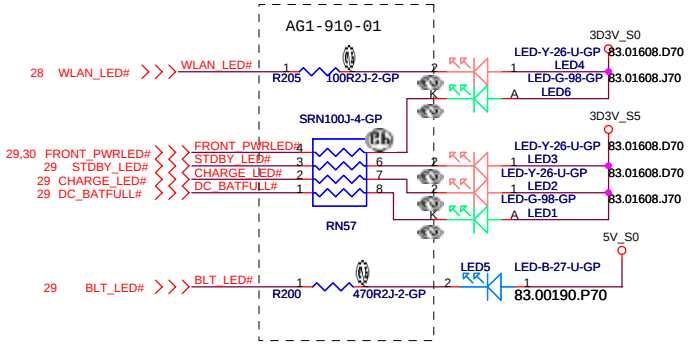
LED







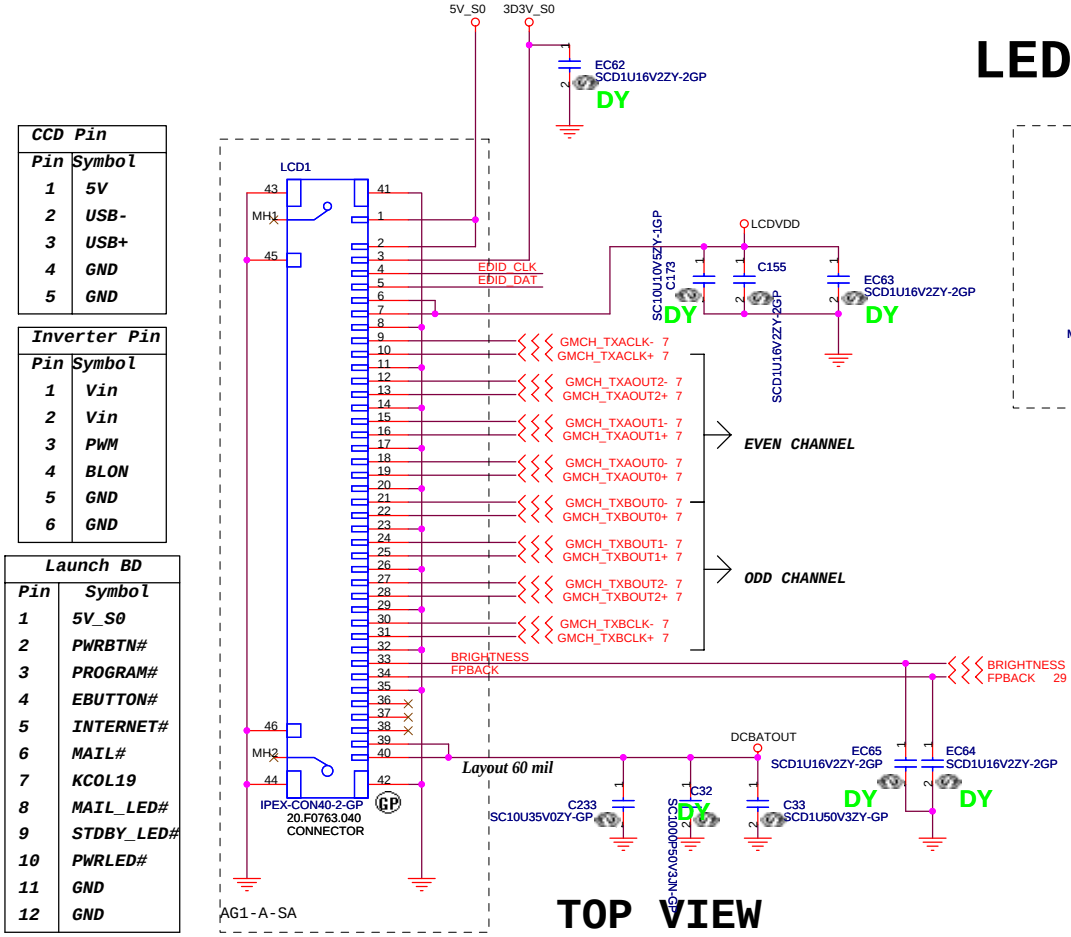
LCD/INVERTER/CCD CONN

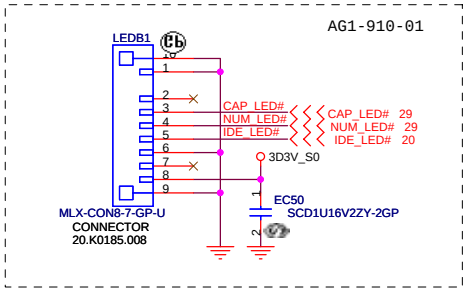
LED BD CONN

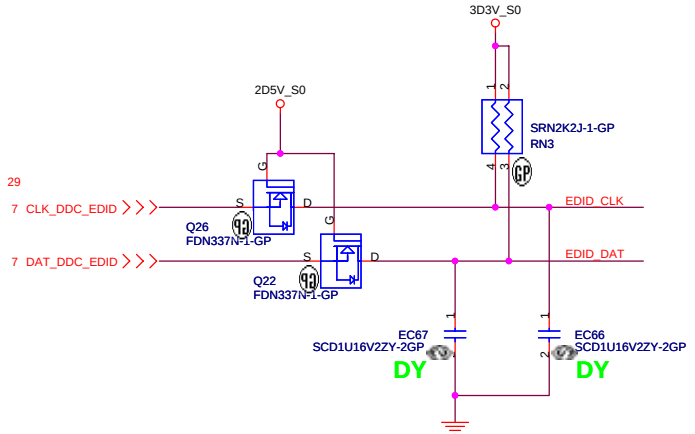
CCD Pin	
Pin	Symbol
1	5V
2	USB-
3	USB+
4	GND
5	GND

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Launch BD	
Pin	Symbol
1	5V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	KCOL19
8	MAIL_LED#
9	STDBY_LED#
10	PWRLED#
11	GND
12	GND







TOP VIEW

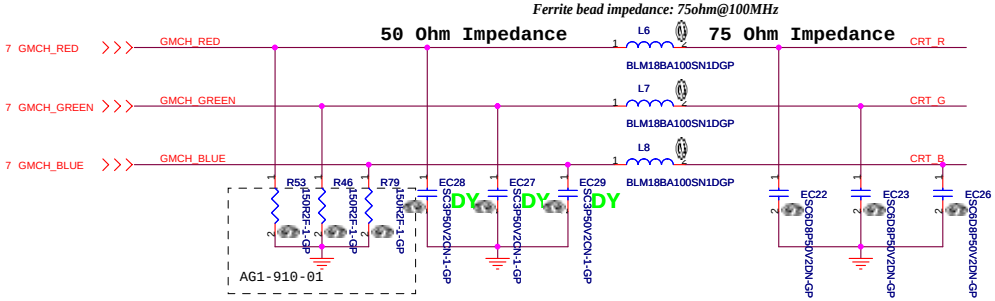
LCD

<Core Design>

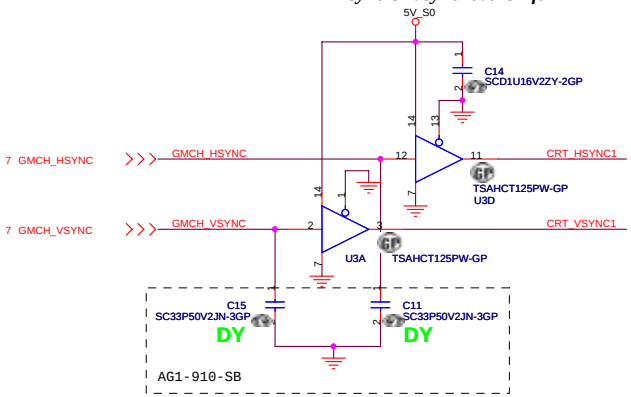
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LCD CONN & LED
Size A3	Document Number AG1(Alviso) Rev 01
Date: Friday, October 28, 2005	Sheet 13 of 40

CRT CONNECTOR

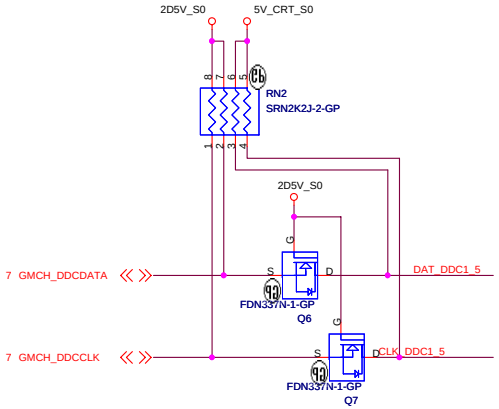
Ferrite bead impedance: 75ohm@100MHz

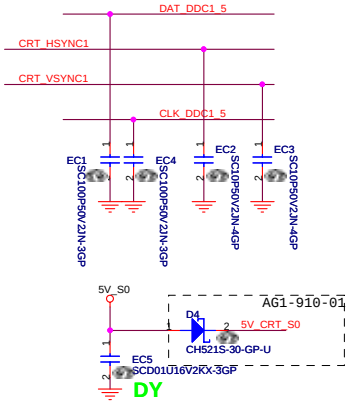


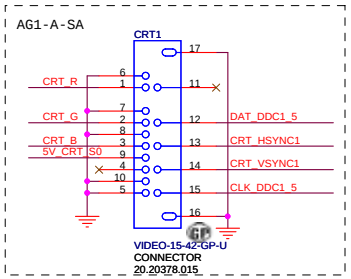
Hsync & Vsync level shift



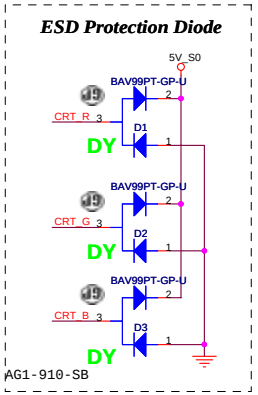
DDC_CLK & DATA level shift







ESD Protection Diode



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *CRT Connector*		
Size: Custom	Document Number: AG1(Alviso)	Rev: 01
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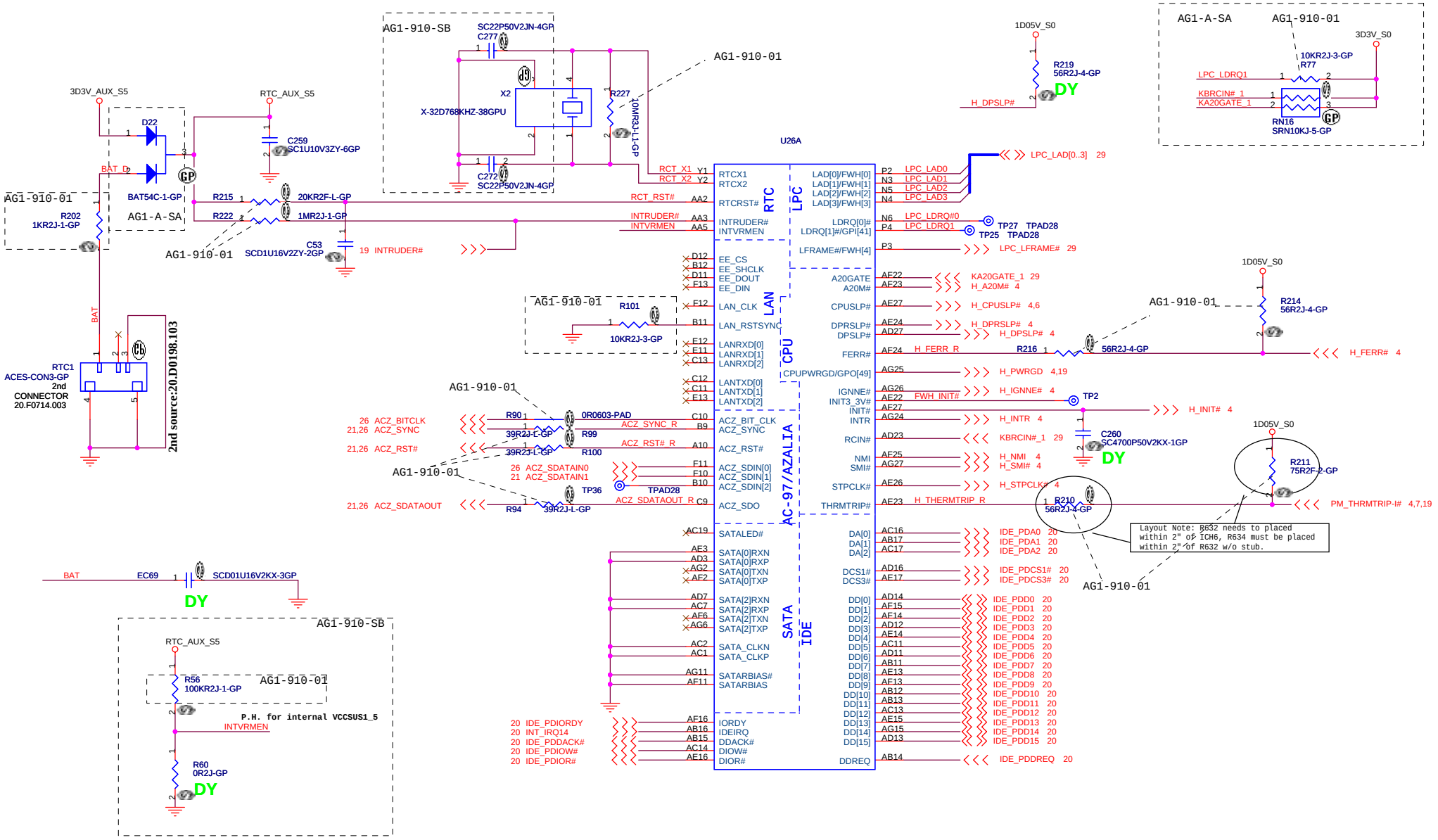


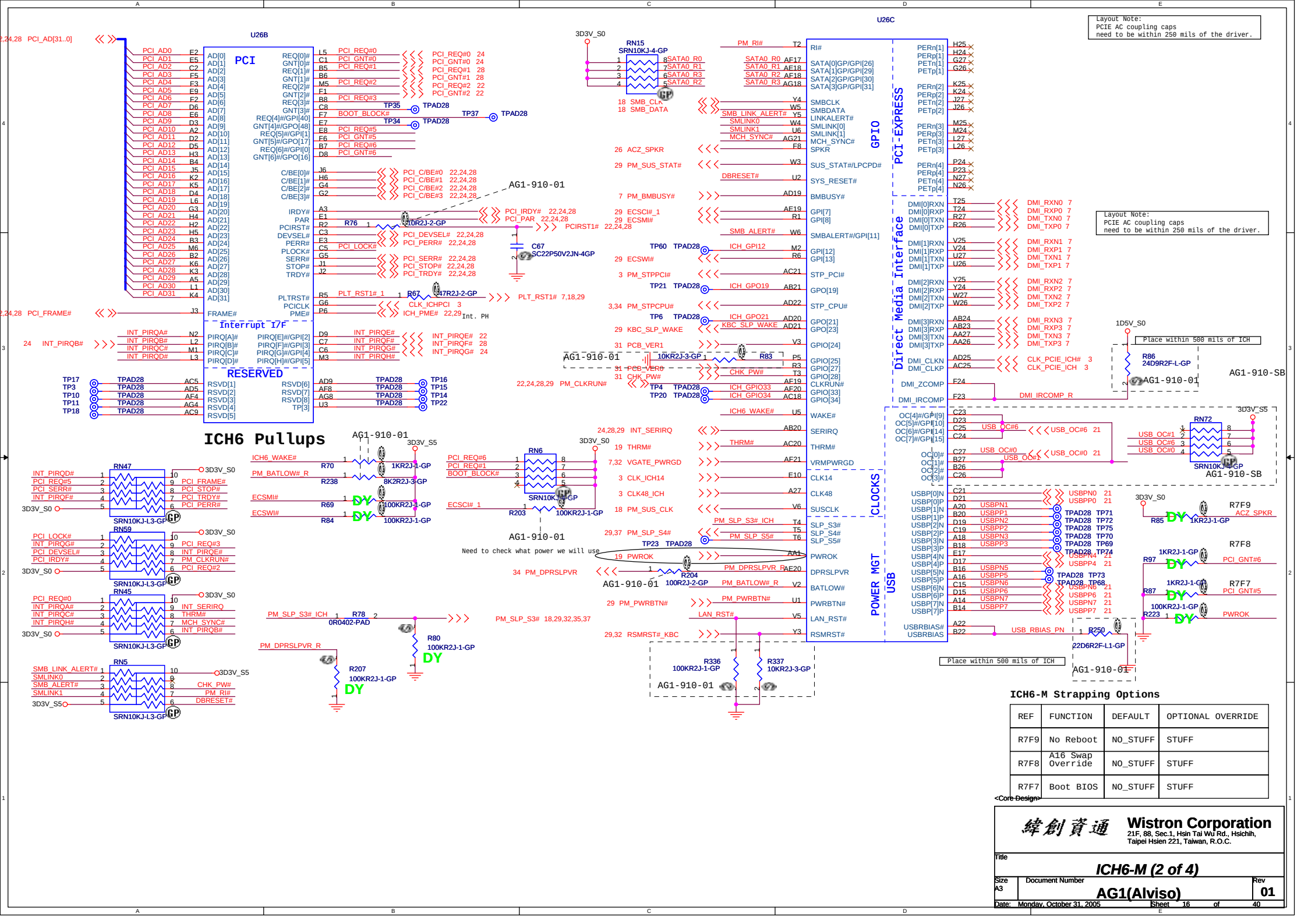
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH6-M (1 of 4)

Size: A3 | Document Number: AG1(Alviso) | Rev: 01

Date: Wednesday, November 02, 2005 | Sheet 15 of 40


U26B
PCI
Interrupt I/F
RESERVED
U26C
GPIO
PCI-EXPRESS
Direct Media Interface
CLOCKS
USB
POWER MGT
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
ICH6 Pullups
Need to check what power we will use
Place within 500 mils of ICH
AG1-910-01
AG1-910-SB
ICH6-M Strapping Options
REF | FUNCTION | DEFAULT | OPTIONAL OVERRIDE
R7F9 | No Reboot | NO_STUFF | STUFF
R7F8 | A16 Swap Override | NO_STUFF | STUFF
R7F7 | Boot BIOS | NO_STUFF | STUFF
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (2 of 4)
Size A3
Document Number
AG1(Alviso)
Rev 01
Date: Monday, October 31, 2005
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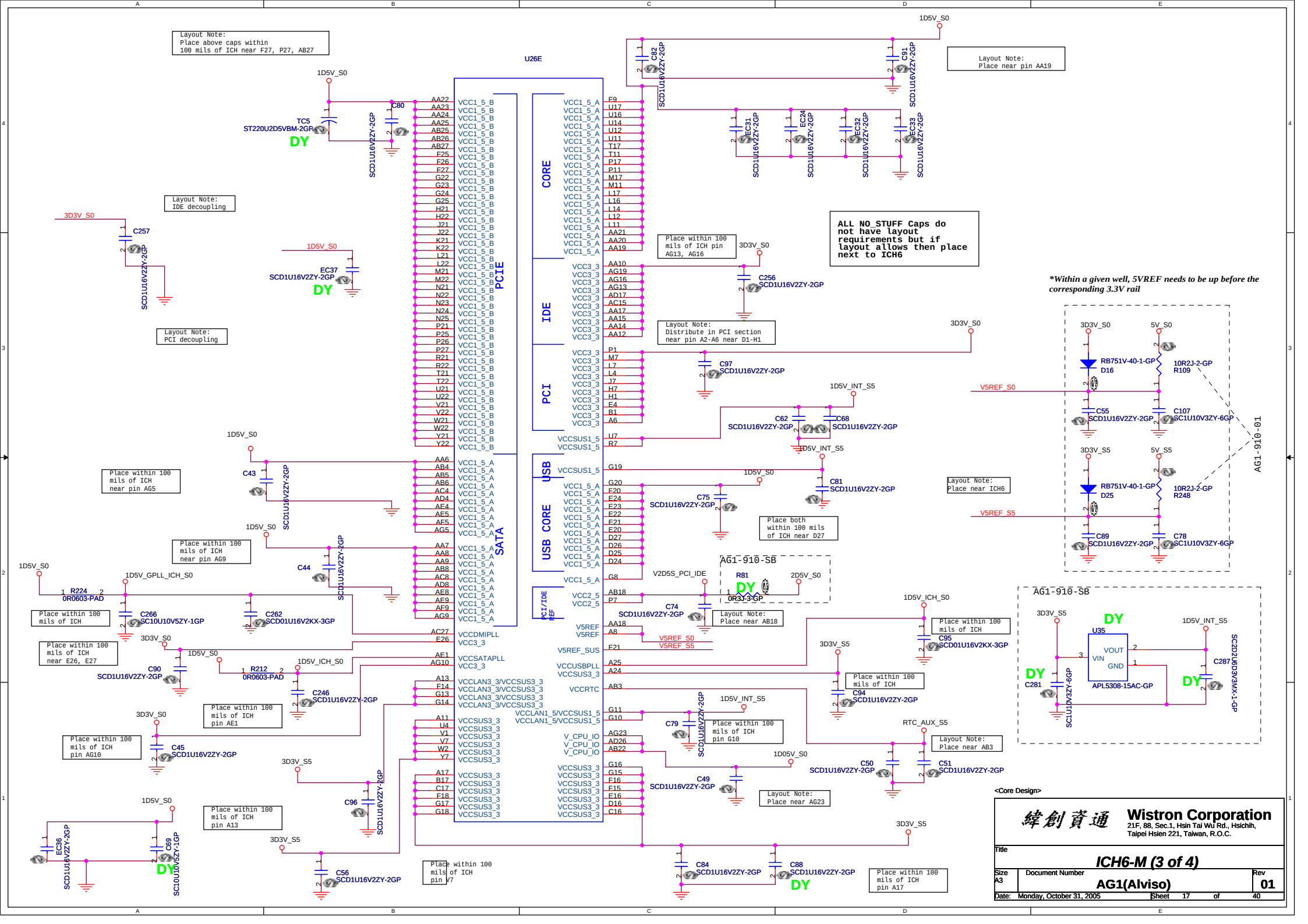
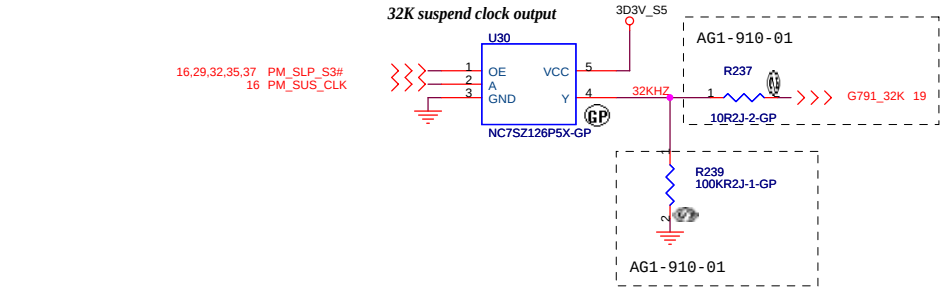
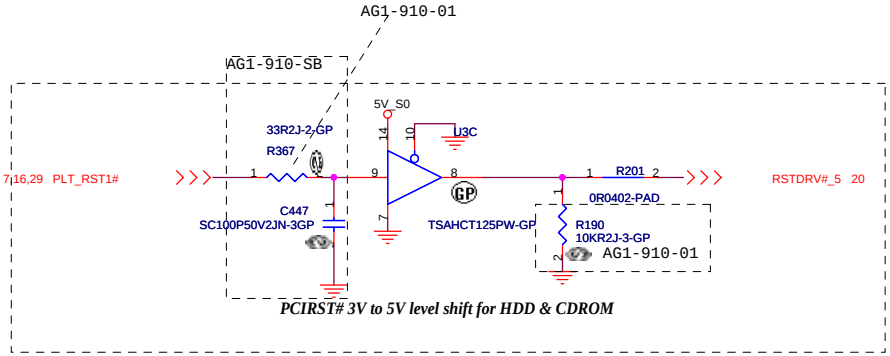
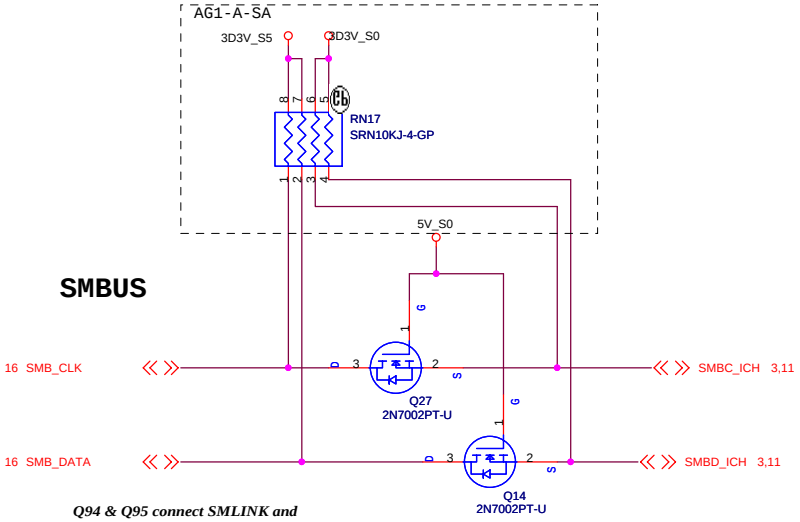
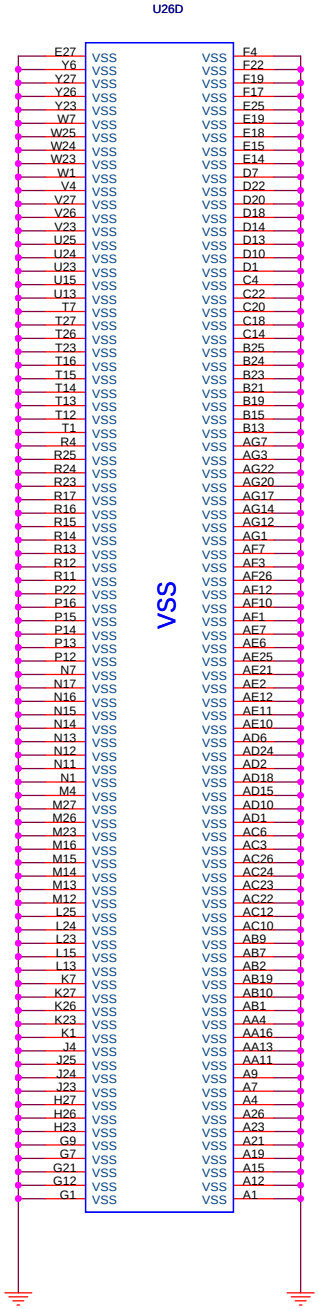

U26E
PCIE
SATA
CORE
IDE
PCI
USB
USB CORE
PCI/IDE REF
Layout Note: Place above caps within 100 mils of ICH near F27, P27, AB27
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Layout Note: Place near pin AA19
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
Place within 100 mils of pin AG13, AG16
Layout Note: Distribute in PCI section near pin A2-A6 near D1-H1
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin AG10
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin V7
Place within 100 mils of ICH pin A17
Place within 100 mils of ICH pin G10
Place both within 100 mils of ICH near D27
Layout Note: Place near AB18
Layout Note: Place near ICH6
Layout Note: Place near AB3
Layout Note: Place near AG23
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
AG1-910-SB
AG1-910-01
Core Design
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (3 of 4)
Size A3
Document Number
AG1(Alviso)
Rev 01
Date: Monday, October 31, 2005
Sheet 17 of 40









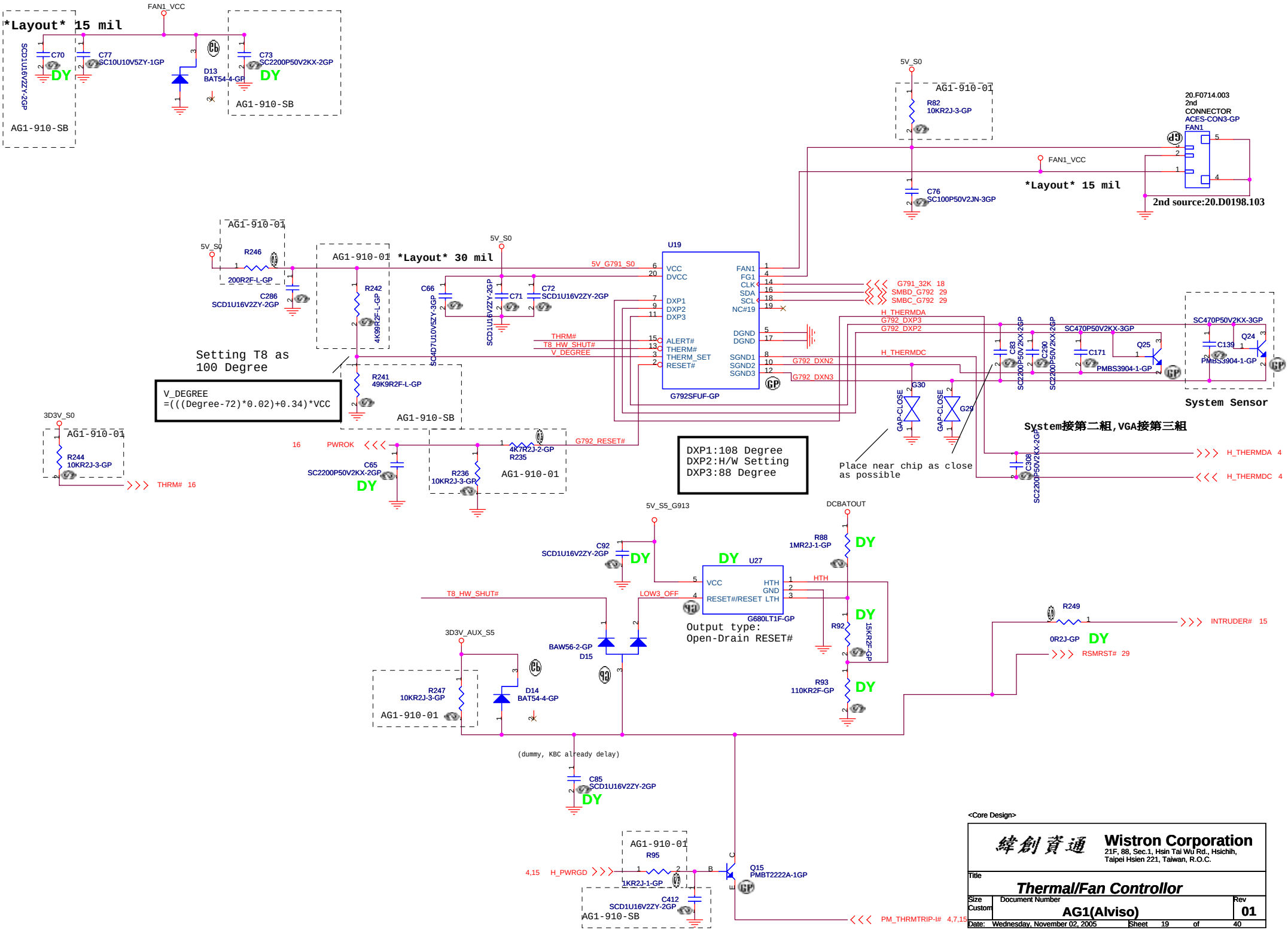
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

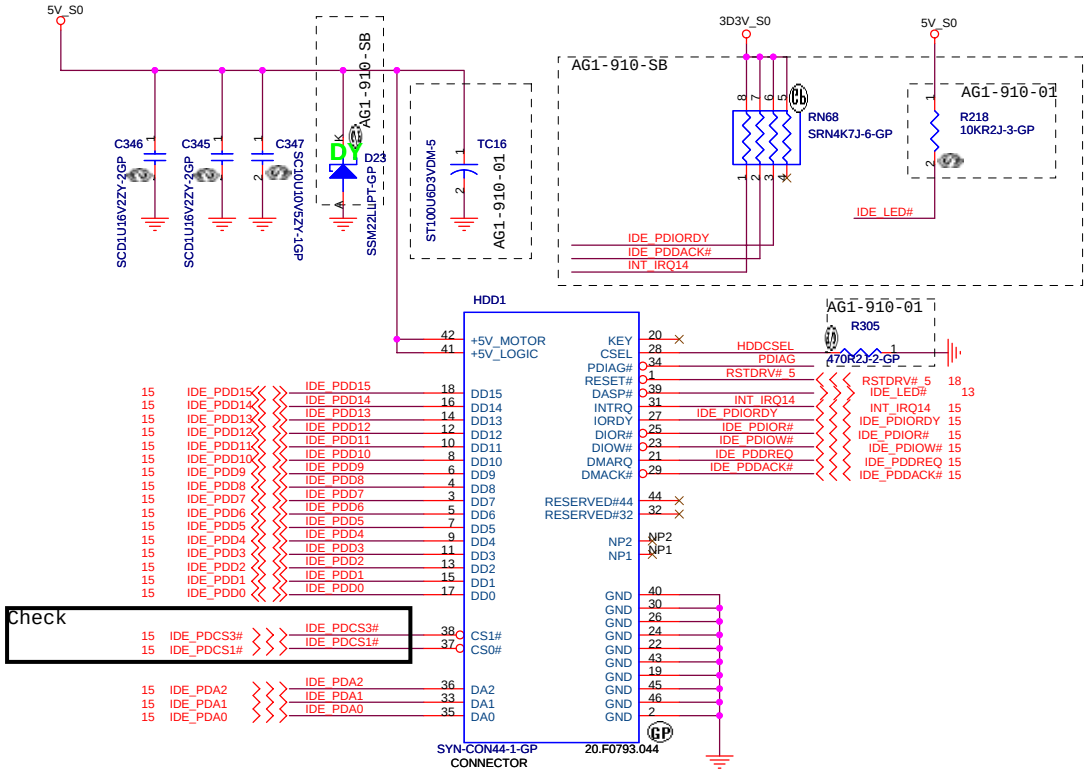
Title: ICH6-M (4 of 4)

Size: A3 | Document Number: AG1(Alviso) | Rev: 01

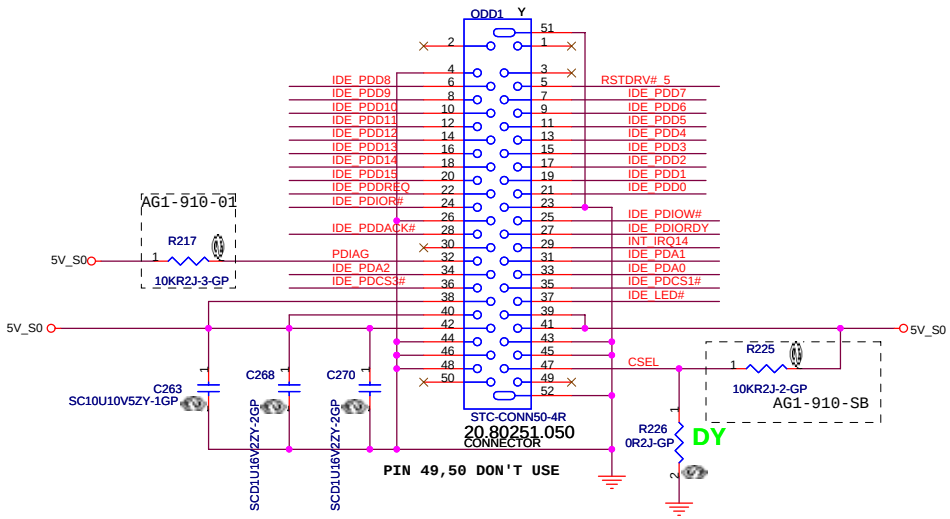
Date: Tuesday, October 25, 2005 | Sheet 18 of 40


Layout 15 mil
FAN1_VCC
C70
DY
C77
SC10U10V5ZY-1GP
D13
BAT54-4-GP
C73
SC2200P50V2KX-2GP
DY
AG1-910-SB
SCD1U16V2ZY-2GP
5V_S0
AG1-910-01
R82
10KR2J-3-GP
20.F0714.003
2nd
CONNECTOR
ACES-CON3-GP
FAN1
FAN1_VCC
Layout 15 mil
C76
SC100P50V2JN-3GP
2nd source:20.D0198.103
R246
200R2F-L-GP
C286
SCD1U16V2ZY-2GP
Layout 30 mil
R242
4K99R2F-L-GP
C66
SC4D7U10V5ZY-3GP
C71
SCD1U16V2ZY-2GP
C72
SCD1U16V2ZY-2GP
5V_G791_S0
U19
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792SFUF-GP
G791_32K 18
SMBD_G792 29
SMBC_G792 29
THRM#
T8_HW_SHUT#
V_DEGREE
H_THERMDA
G792_DXP3
G792_DXP2
H_THERMDC
G792_DXN2
G792_DXN3
Setting T8 as
100 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
R241
49K9R2F-L-GP
AG1-910-SB
3D3V_S0
R244
10KR2J-3-GP
THRM# 16
16 PWROK
C65
SC2200P50V2KX-2GP
DY
R236
10KR2J-3-GP
R235
4K7R2J-2-GP
G792_RESET#
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close
as possible
G30
GAP-CLOSE
G29
GAP-CLOSE
C83
SC2200P50V2KX-2GP
C290
SC2200P50V2KX-2GP
SC470P50V2KX-3GP
C171
Q25
PMBS3904-1-GP
SC470P50V2KX-3GP
C139
Q24
PMBS3904-1-GP
System Sensor
System接第二組,VGA接第三組
C308
SC2200P50V2KX-2GP
H_THERMDA 4
H_THERMDC 4
5V_S5_G913
C92
SCD1U16V2ZY-2GP
DY
U27
VCC
HTH
GND
RESET#/RESET
LTH
G680LT1F-GP
T8_HW_SHUT#
LOW3_OFF
HTH
R88
1MR2J-1-GP
DY
R92
15KR2F-GP
DY
R93
110KR2F-GP
DY
Output type:
Open-Drain RESET#
DCBATOUT
3D3V_AUX_S5
BAW56-2-GP
D15
R247
10KR2J-3-GP
AG1-910-01
D14
BAT54-4-GP
R249
0R2J-GP
DY
INTRUDER# 15
RSMRST# 29
(dummy, KBC already delay)
C85
SCD1U16V2ZY-2GP
DY
R95
1KR2J-1-GP
4,15 H_PWRGD
Q15
PMBT2222A-1GP
C412
SCD1U16V2ZY-2GP
PM_THRMTRIP-I# 4,7,15
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Custom
Document Number
AG1(Alviso)
Rev
01
Date: Wednesday, November 02, 2005
Sheet 19 of 40

HDD Connector



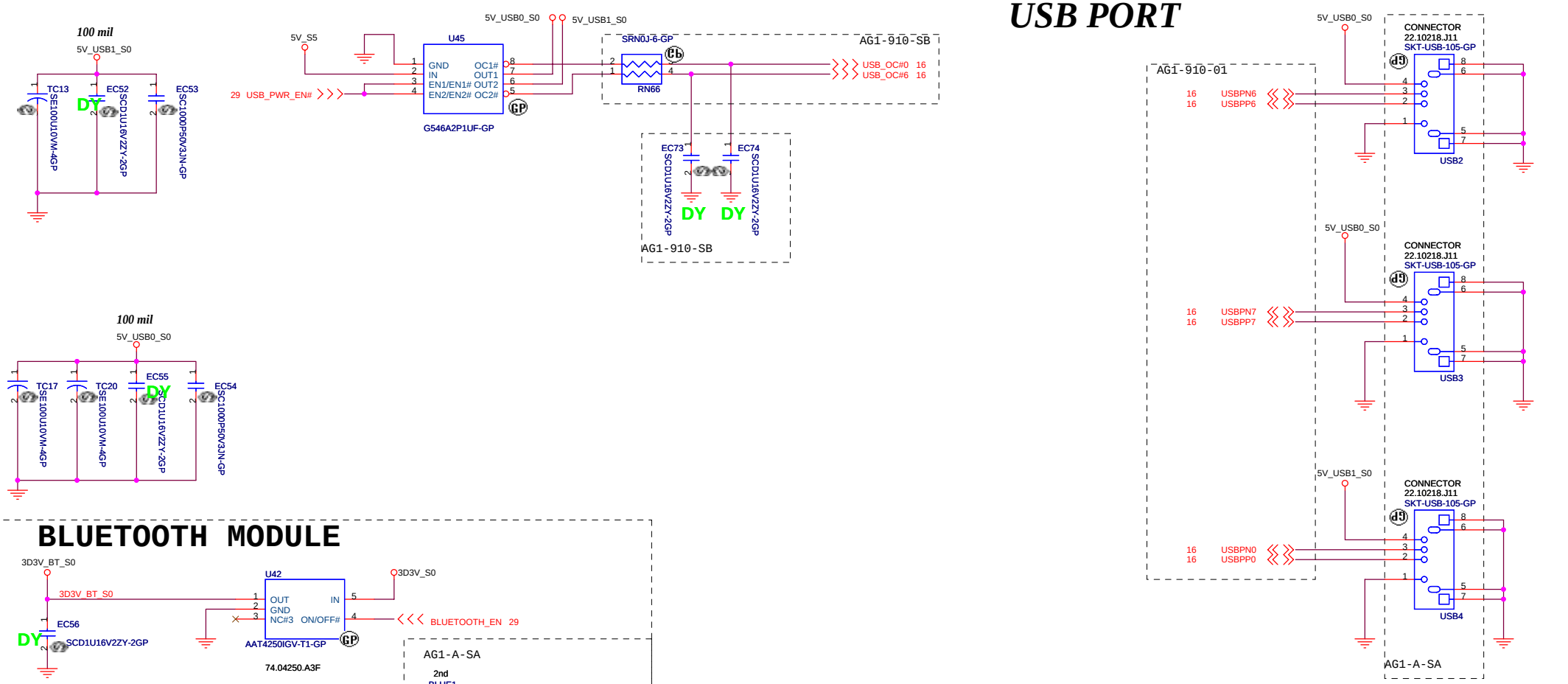
CD-ROM Connector



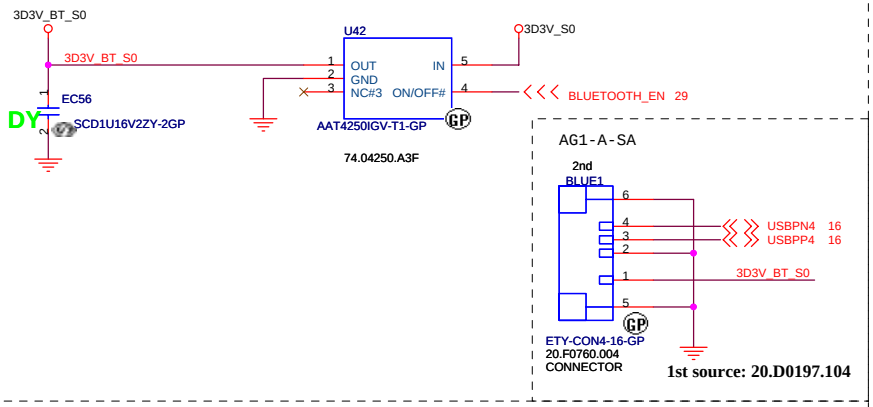
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD and CDROM		
Size: A3	Document Number: AG1(Alviso)	Rev: 01
Date: Monday, October 31, 2005	Sheet 20 of 40	

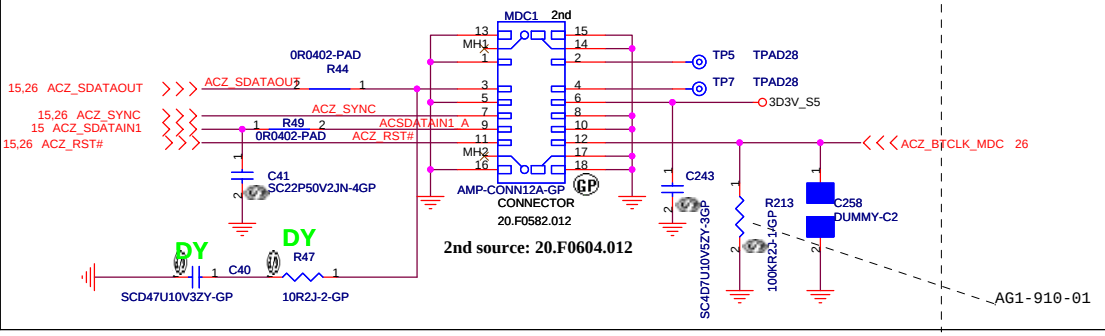
USB PORT



BLUETOOTH MODULE

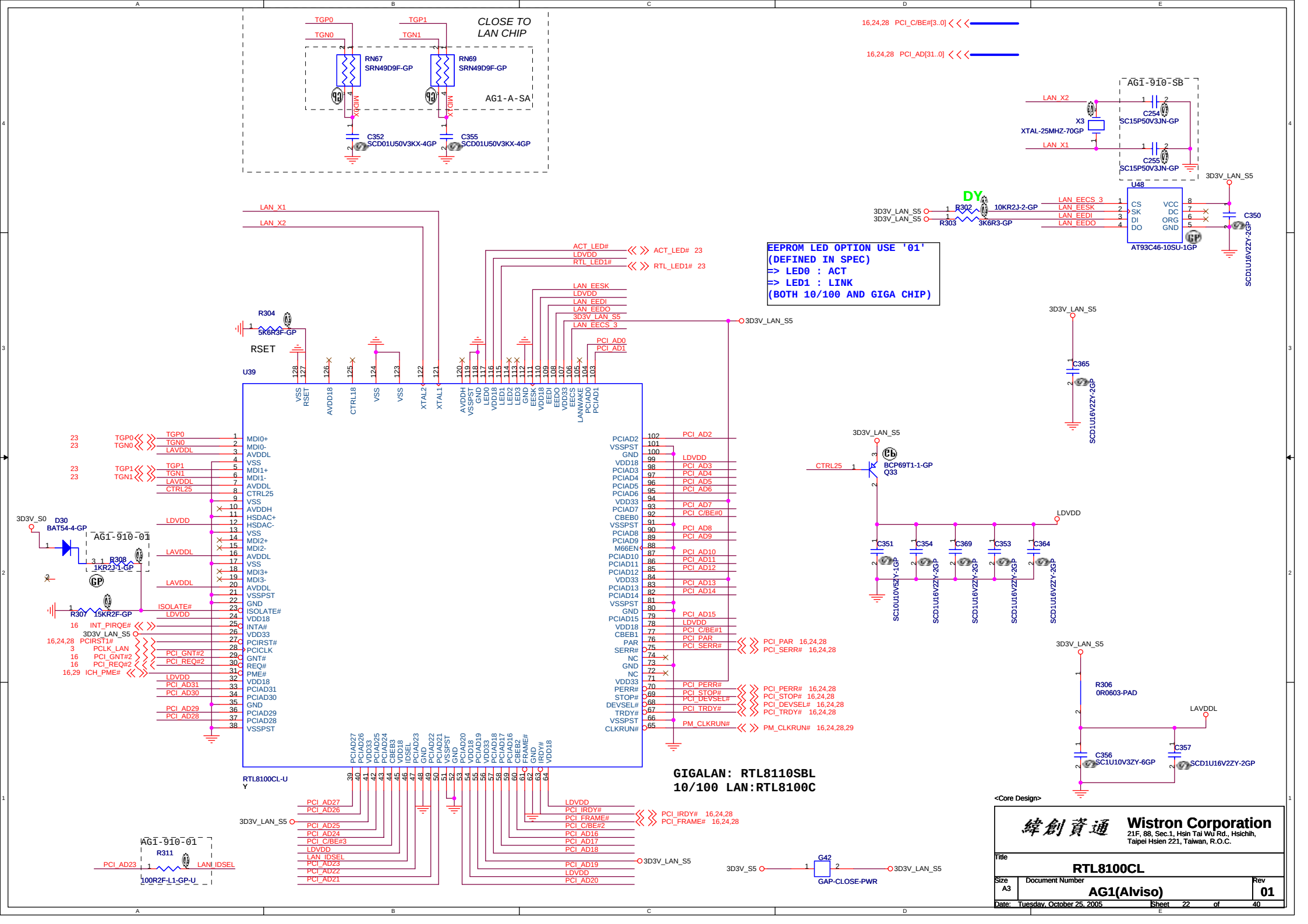


MDC 1.5 CONNECTOR

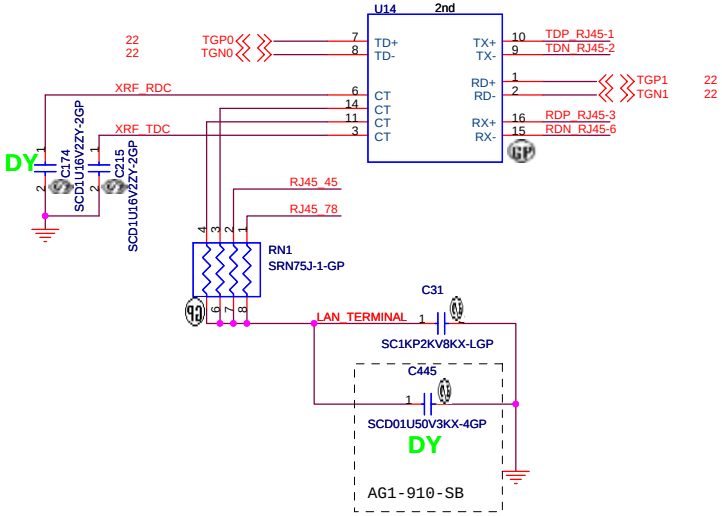


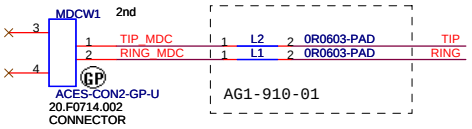
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB / MDC / BLUETOOTH		
Size: A3	Document Number: AG1(Alviso)	Rev: 01
Date: Friday, October 28, 2005	Sheet 21 of 40	


CLOSE TO LAN CHIP
RN67 SRN49D9F-GP
RN69 SRN49D9F-GP
AG1-A-SA
C352 SCD01U50V3KX-4GP
C355 SCD01U50V3KX-4GP
AG1-910-SB
X3 XTAL-25MHZ-70GP
C254 SC15P50V3JN-GP
C255 SC15P50V3JN-GP
DY
R302 10KR2J-2-GP
R303 3K6R3-GP
U48
AT93C46-10SU-1GP
C350 SCD1U16V2ZY-2GP
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
R304 5K6R3F-GP
RSET
U39
RTL8100CL-U
Y
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
C365 SCD1U16V2ZY-2GP
BCP69T1-1-GP Q33
C351 SC10U10V5ZY-1GP
C354 SCD1U16V2ZY-2GP
C369 SCD1U16V2ZY-2GP
C353 SCD1U16V2ZY-2GP
C364 SCD1U16V2ZY-2GP
D30 BAT54-4-GP
R308 1KR2J-1-GP
R307 15KR2F-GP
R306 0R0603-PAD
C356 SC1U10V3ZY-6GP
C357 SCD1U16V2ZY-2GP
R311 100R2F-L1-GP-U
G42 GAP-CLOSE-PWR
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8100CL
Size A3
Document Number AG1(Alviso)
Rev 01
Date: Tuesday, October 25, 2005
Sheet 22 of 40

10/100M Lan Transformer

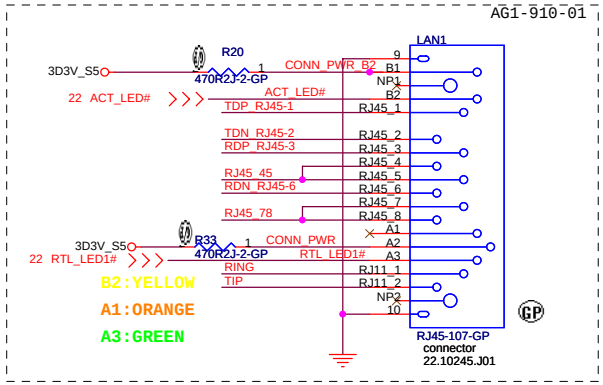




2nd source: 20.D0196.102

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

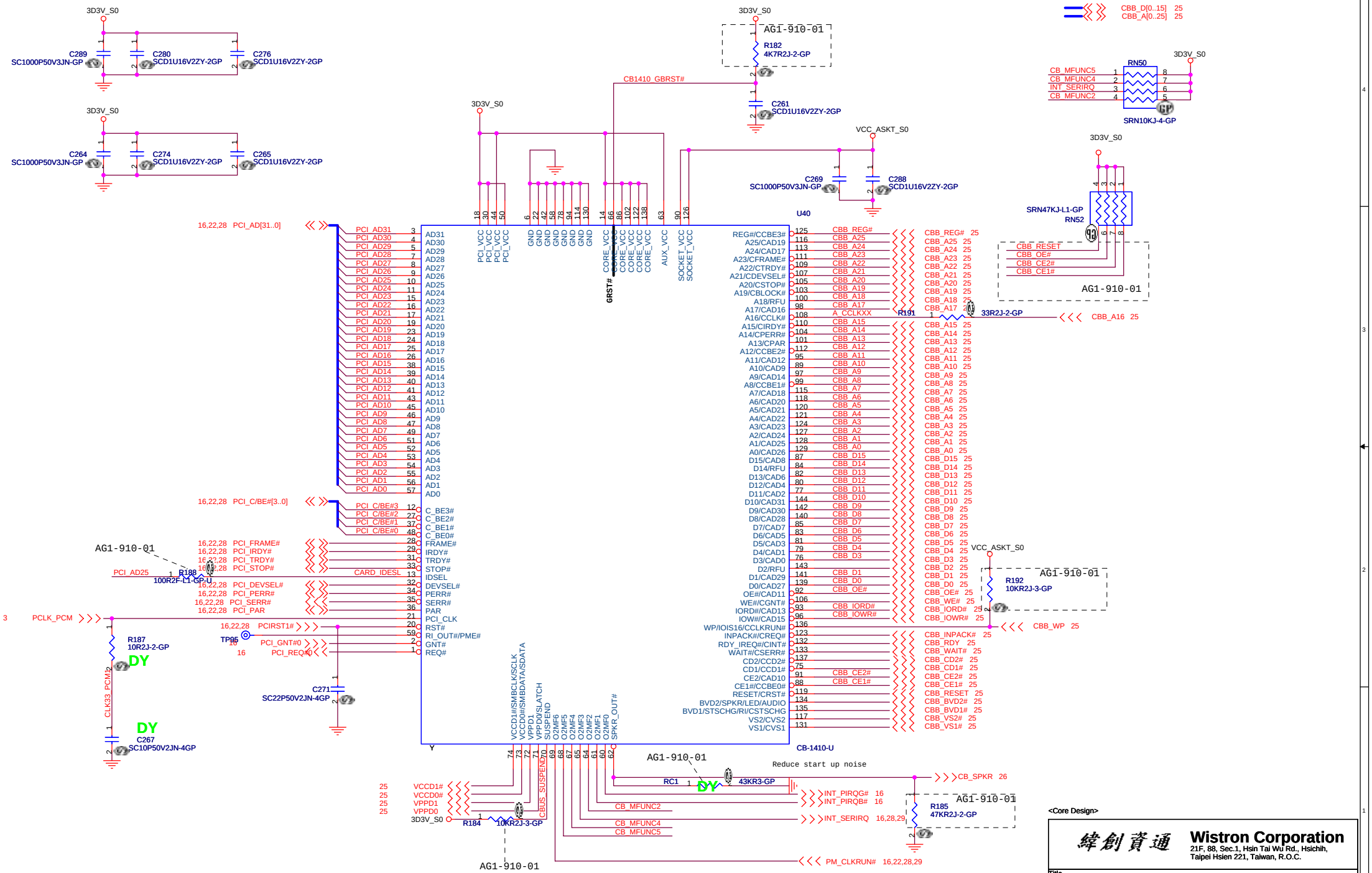
LAN Connector



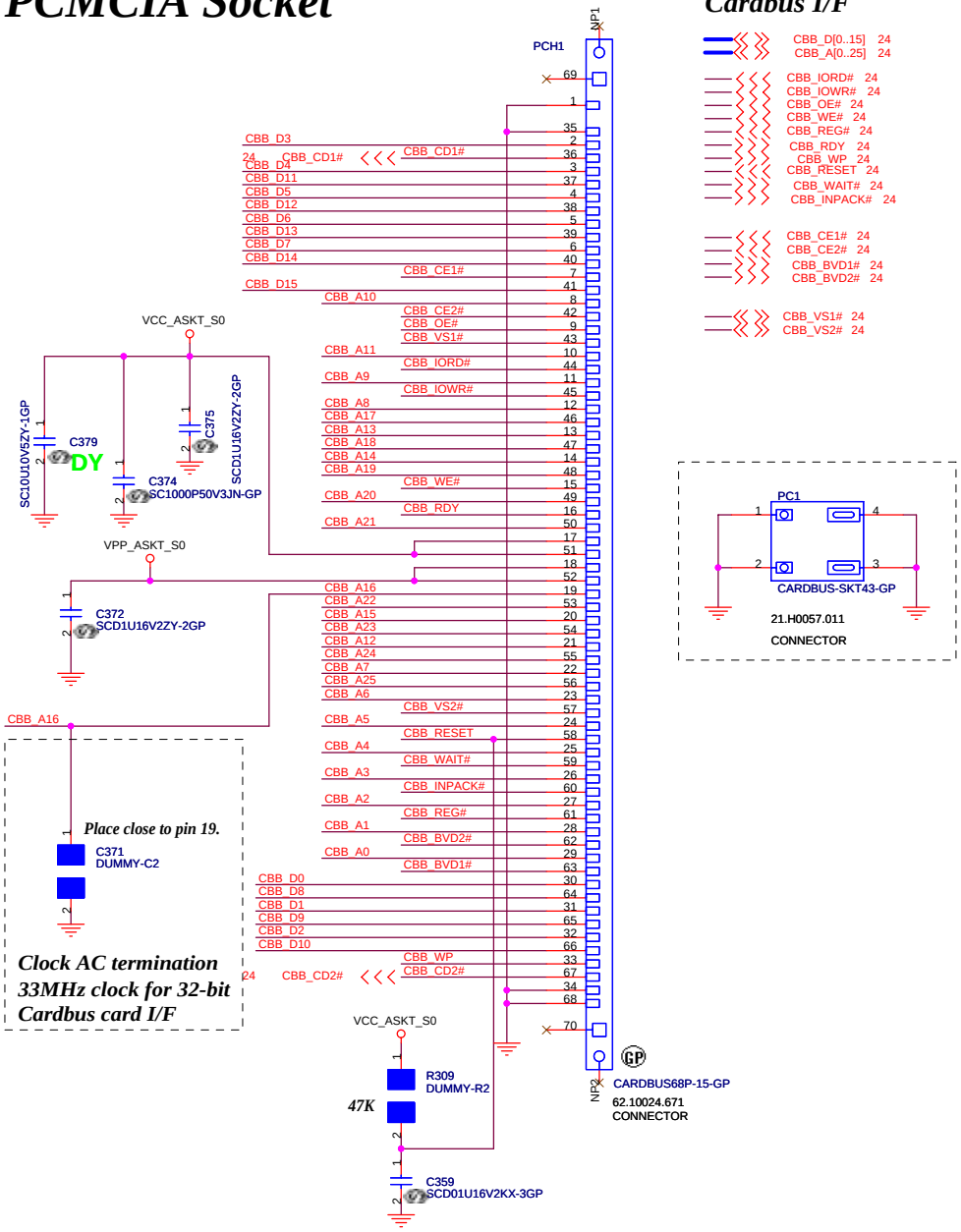
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LAN CONN		
Size: A3	Document Number: **AG1(Alviso)**	Rev: **01**
Date: Saturday, October 29, 2005	Sheet 23 of 40	

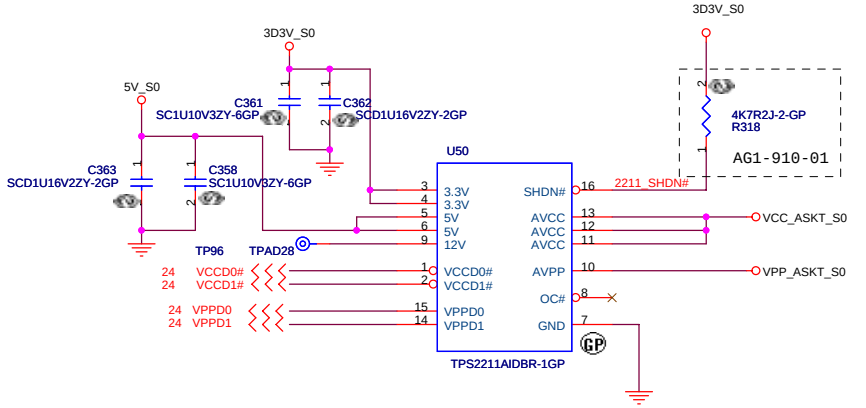

3D3V_S0
C289 SC1000P50V3JN-GP
C280 SCD1U16V2ZY-2GP
C276 SCD1U16V2ZY-2GP
C264 SC1000P50V3JN-GP
C274 SCD1U16V2ZY-2GP
C265 SCD1U16V2ZY-2GP
AG1-910-01
R182 4K7R2J-2-GP
C261 SCD1U16V2ZY-2GP
CB1410_GBRST#
VCC_ASKT_S0
C269 SC1000P50V3JN-GP
C288 SCD1U16V2ZY-2GP
CBB_D[0..15] 25
CBB_A[0..25] 25
RN50
CB_MFUNC5
CB_MFUNC4
INT_SERIRQ
CB_MFUNC2
SRN10KJ-4-GP
SRN47KJ-L1-GP
RN52
CBB_RESET
CBB_OE#
CBB_CE2#
CBB_CE1#
U40
16,22,28 PCI_AD[31..0]
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28 PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_AD23 PCI_AD22 PCI_AD21 PCI_AD20 PCI_AD19 PCI_AD18 PCI_AD17 PCI_AD16 PCI_AD15 PCI_AD14 PCI_AD13 PCI_AD12 PCI_AD11 PCI_AD10 PCI_AD9 PCI_AD8 PCI_AD7 PCI_AD6 PCI_AD5 PCI_AD4 PCI_AD3 PCI_AD2 PCI_AD1 PCI_AD0
16,22,28 PCI_C/BE#[3..0]
PCI_C/BE#3 PCI_C/BE#2 PCI_C/BE#1 PCI_C/BE#0
16,22,28 PCI_FRAME#
16,22,28 PCI_IRDY#
16,22,28 PCI_TRDY#
16,22,28 PCI_STOP#
16,22,28 PCI_DEVSEL#
16,22,28 PCI_PERR#
16,22,28 PCI_SERR#
16,22,28 PCI_PAR
16,22,28 PCIRST1#
PCI_GNT#0
PCI_REQ#0
CARD_IDESL
PCI_AD25
R188 100R2F-L1-GP-U
PCLK_PCM
R187 10R2J-2-GP
DY
CLK33_PCM
C267 SC10P50V2JN-4GP
C271 SC22P50V2JN-4GP
TP85
PCI_VCC GND CORE_VCC AUX_VCC SOCKET_VCC
GRST#
REG#/CCBE3# A25/CAD19 A24/CAD17 A23/CFRAME# A22/CTRDY# A21/CDEVSEL# A20/CSTOP# A19/CBLOCK# A18/RFU A17/CAD16 A16/CCLK# A15/CIRDY# A14/CPERR# A13/CPAR A12/CCBE2# A11/CAD12 A10/CAD9 A9/CAD14 A8/CCBE1# A7/CAD18 A6/CAD20 A5/CAD21 A4/CAD22 A3/CAD23 A2/CAD24 A1/CAD25 A0/CAD26 D15/CAD8 D14/RFU D13/CAD6 D12/CAD4 D11/CAD2 D10/CAD31 D9/CAD30 D8/CAD28 D7/CAD7 D6/CAD5 D5/CAD3 D4/CAD1 D3/CAD0 D2/RFU D1/CAD29 D0/CAD27 OE#/CAD11 WE#/CGNT# IORD#/CAD13 IOW#/CAD15 WP/IOIS16/CCLKRUN# INPACK#/CREQ# RDY_IREQ#/CINT# WAIT#/CSERR# CD2/CCD2# CD1/CCD1# CE2/CAD10 CE1#/CCBE0# RESET/CRST# BVD2/SPKR/LED/AUDIO BVD1/STSCHG/RI/CSTSCHG VS2/CVS2 VS1/CVS1
CBB_REG# CBB_A25 CBB_A24 CBB_A23 CBB_A22 CBB_A21 CBB_A20 CBB_A19 CBB_A18 CBB_A17 A_CCLKXX CBB_A15 CBB_A14 CBB_A13 CBB_A12 CBB_A11 CBB_A10 CBB_A9 CBB_A8 CBB_A7 CBB_A6 CBB_A5 CBB_A4 CBB_A3 CBB_A2 CBB_A1 CBB_A0 CBB_D15 CBB_D14 CBB_D13 CBB_D12 CBB_D11 CBB_D10 CBB_D9 CBB_D8 CBB_D7 CBB_D6 CBB_D5 CBB_D4 CBB_D3 CBB_D1 CBB_D0 CBB_OE# CBB_IORD# CBB_IOWR# CBB_INPACK# CBB_RDY CBB_WAIT# CBB_CD2# CBB_CD1# CBB_CE2# CBB_CE1#
R191 33R2J-2-GP
CBB_A16 25
R192 10KR2J-3-GP
CBB_WP 25
CBB_RESET CBB_OE# CBB_WE# CBB_IORD# CBB_IOWR# CBB_BVD2# CBB_BVD1# CBB_VS2# CBB_VS1#
CB-1410-U
VCCD1#/SMBCLK/SCLK VCCD0#/SMBDATA/SDATA VPPD1 VPPD0/SLATCH SUSPEND O2MF6 O2MF5 O2MF4 O2MF3 O2MF2 O2MF1 O2MF0 SPKR_OUT#
CBUS_SUSPEND
Reduce start up noise
RC1 43KR3-GP
CB_SPKR 26
INT_PIRQG# 16
INT_PIRQB# 16
INT_SERIRQ 16,28,29
CB_MFUNC2
CB_MFUNC4
CB_MFUNC5
R185 47KR2J-2-GP
VCCD1# VCCD0# VPPD1 VPPD0
R184 10KR2J-3-GP
PM_CLKRUN# 16,22,28,29
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CardBus_ENE CB1410
Size A3
Document Number
AG1(Alviso)
Rev 01
Date: Tuesday, November 01, 2005
Sheet 24 of 40

PCMCIA Socket



Cardbus I/F

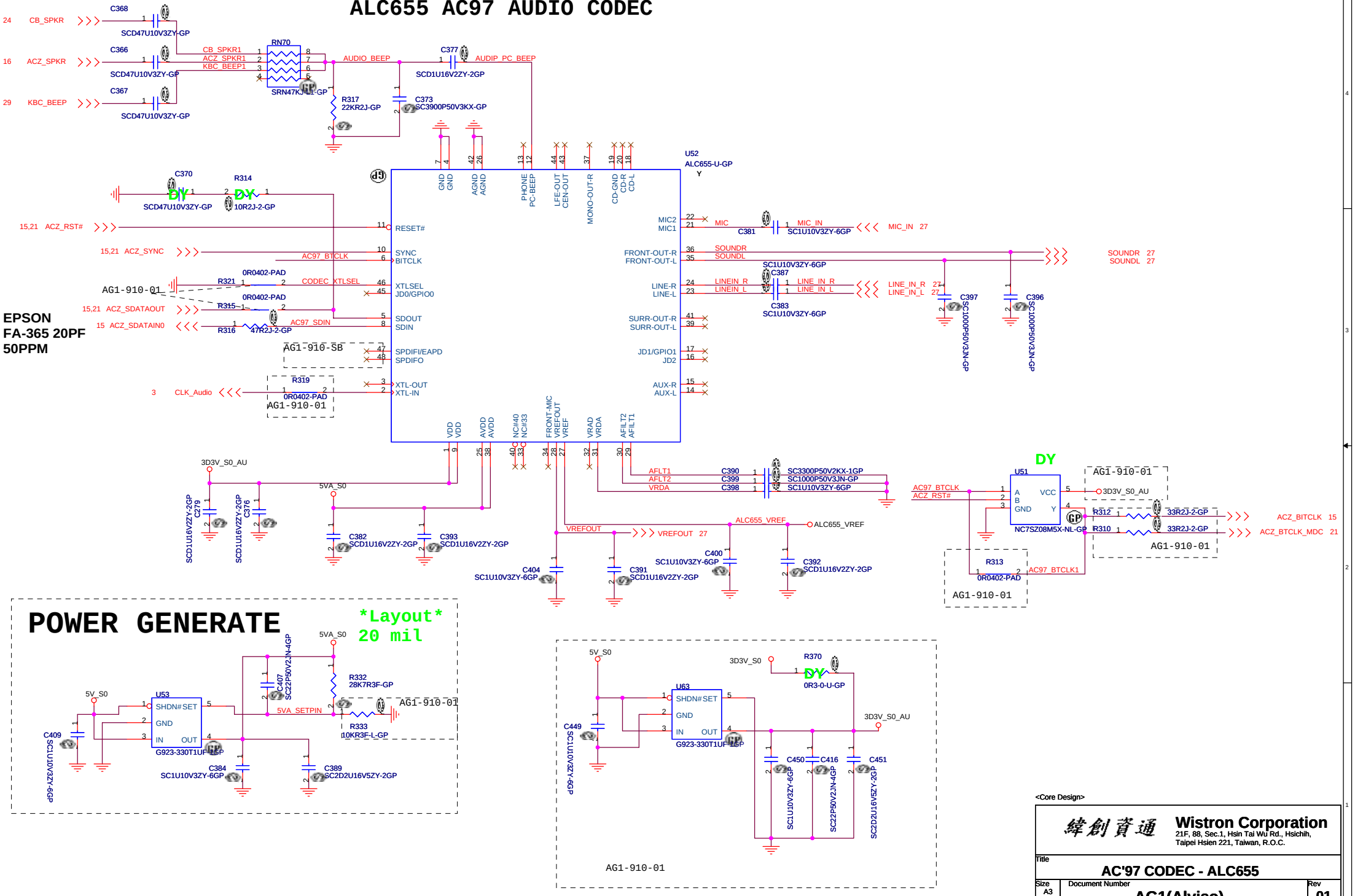
Power switch



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**PCMCA**
Size A3	Document Number **AG1(Alviso)** Rev **01**
Date: Tuesday, October 25, 2005	Sheet 25 of 40

ALC655 AC97 AUDIO CODEC



POWER GENERATE

Layout
20 mil

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AC'97 CODEC - ALC655

Size	Document Number	Rev
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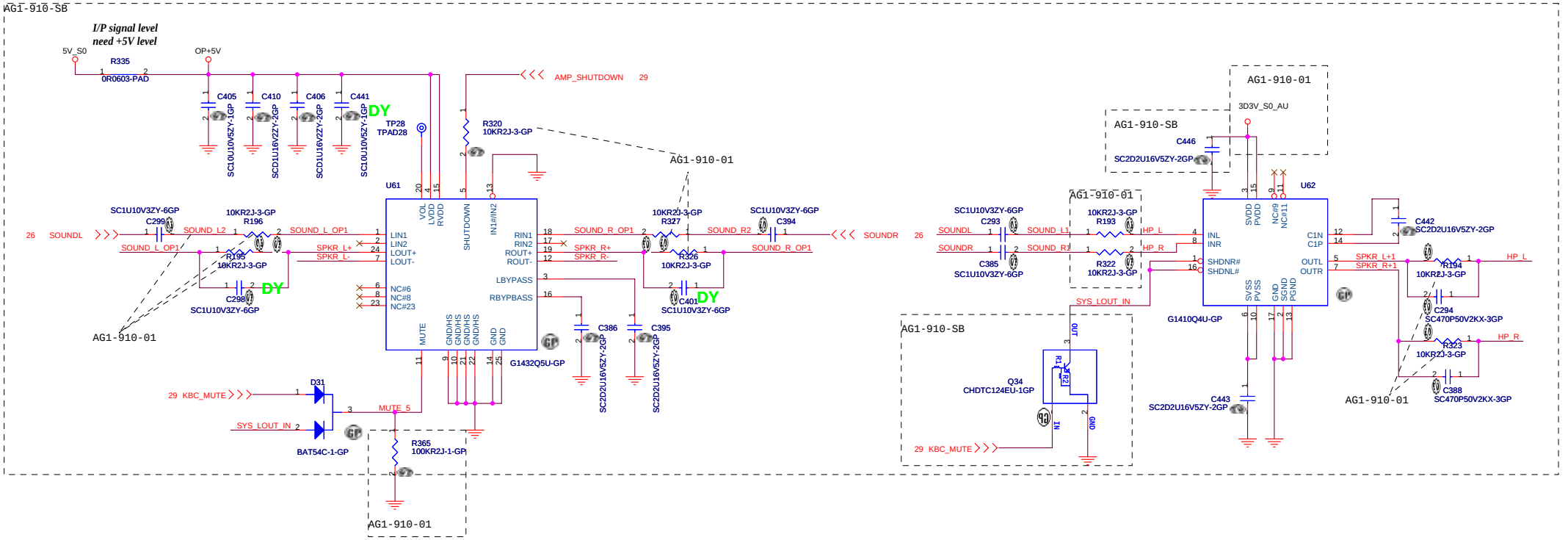
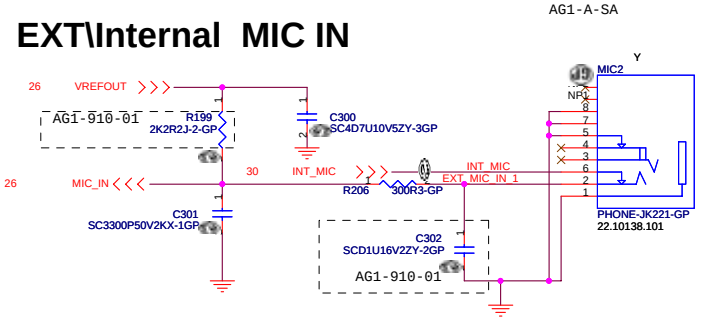
Date: Tuesday, November 01, 2005 Sheet 26 of 40

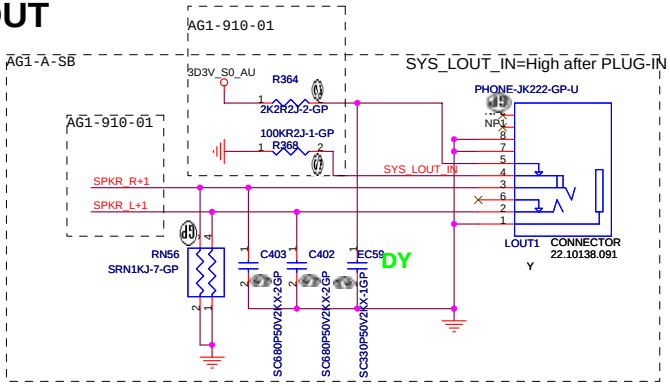
AUDIO OP AMPLIFIER



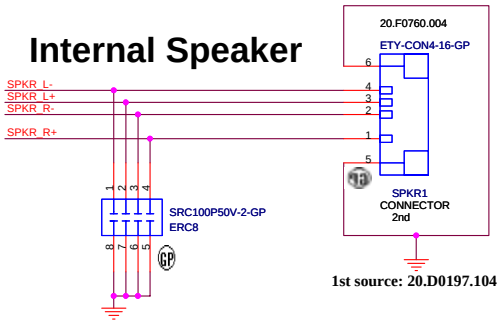
EXT\Internal MIC IN



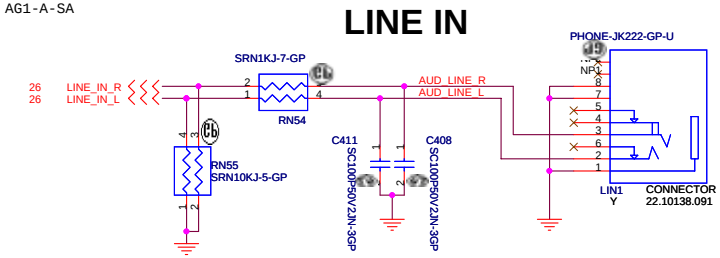
LINE OUT



Internal Speaker



LINE IN

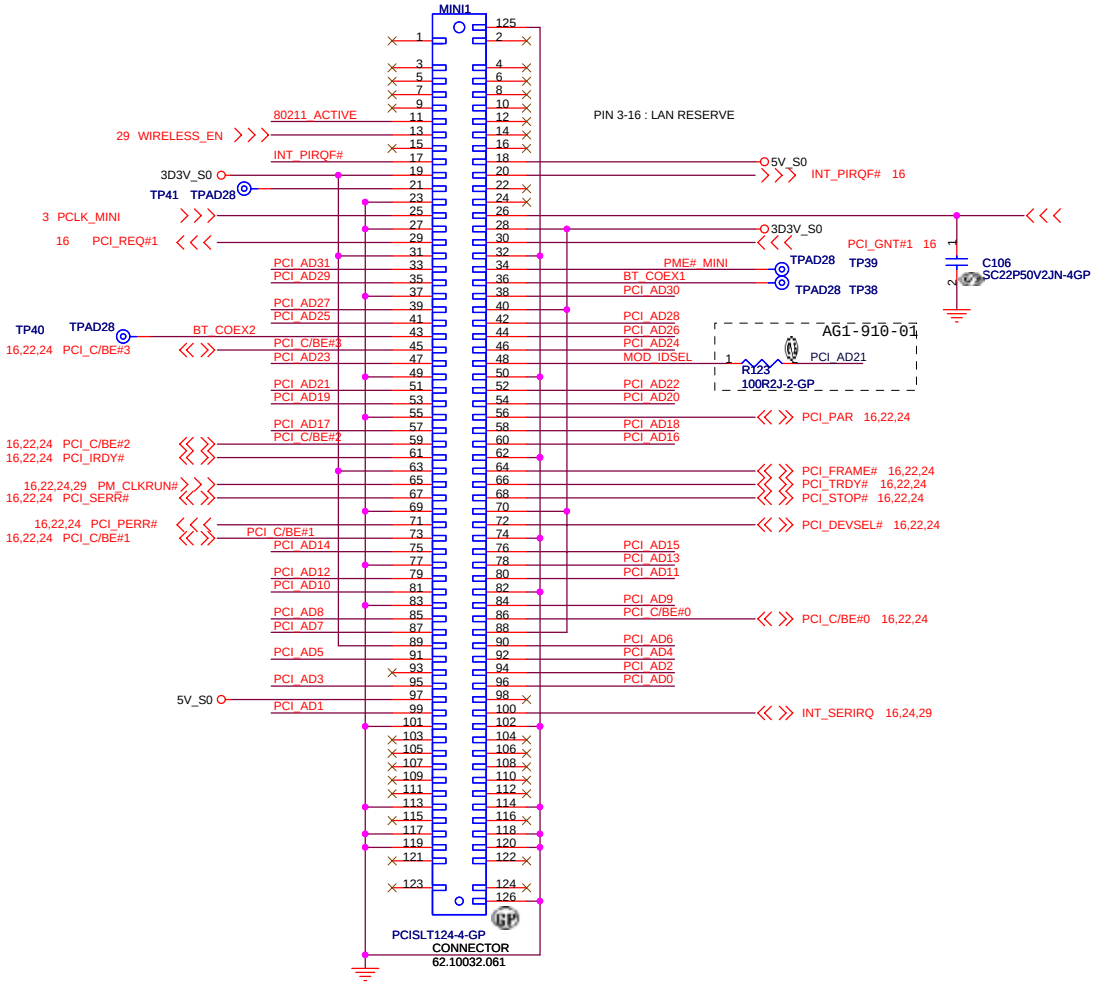


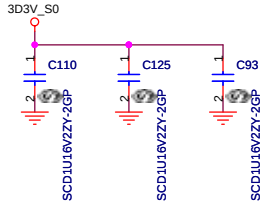
<Core Design>

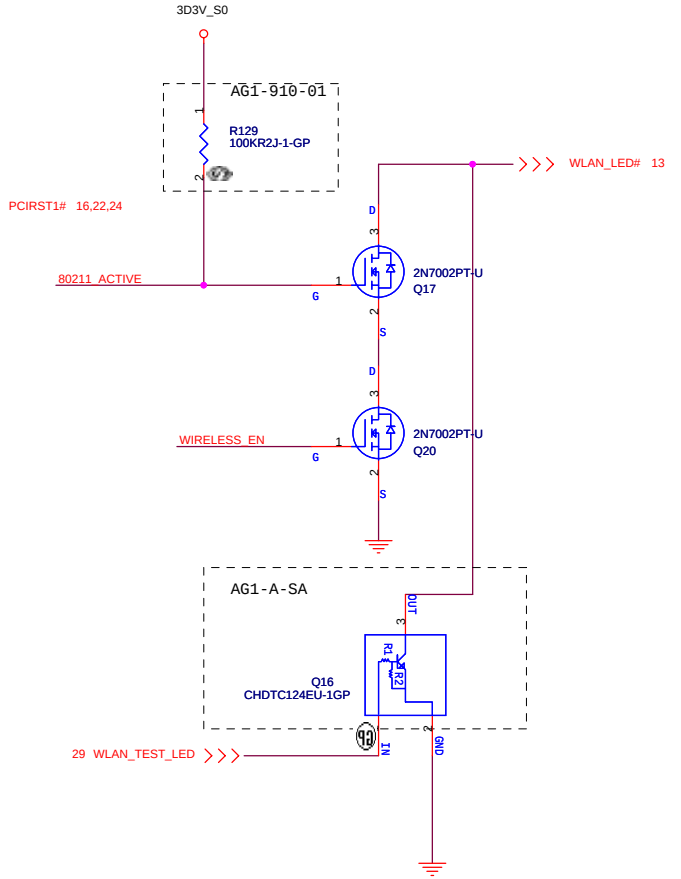
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio AMP and Jack	
Size	Document Number: AG1(Alviso)	Rev: 01
Date: Monday, October 31, 2005	Sheet 27 of 40	

16,22,24 PCI_AD[31..0]







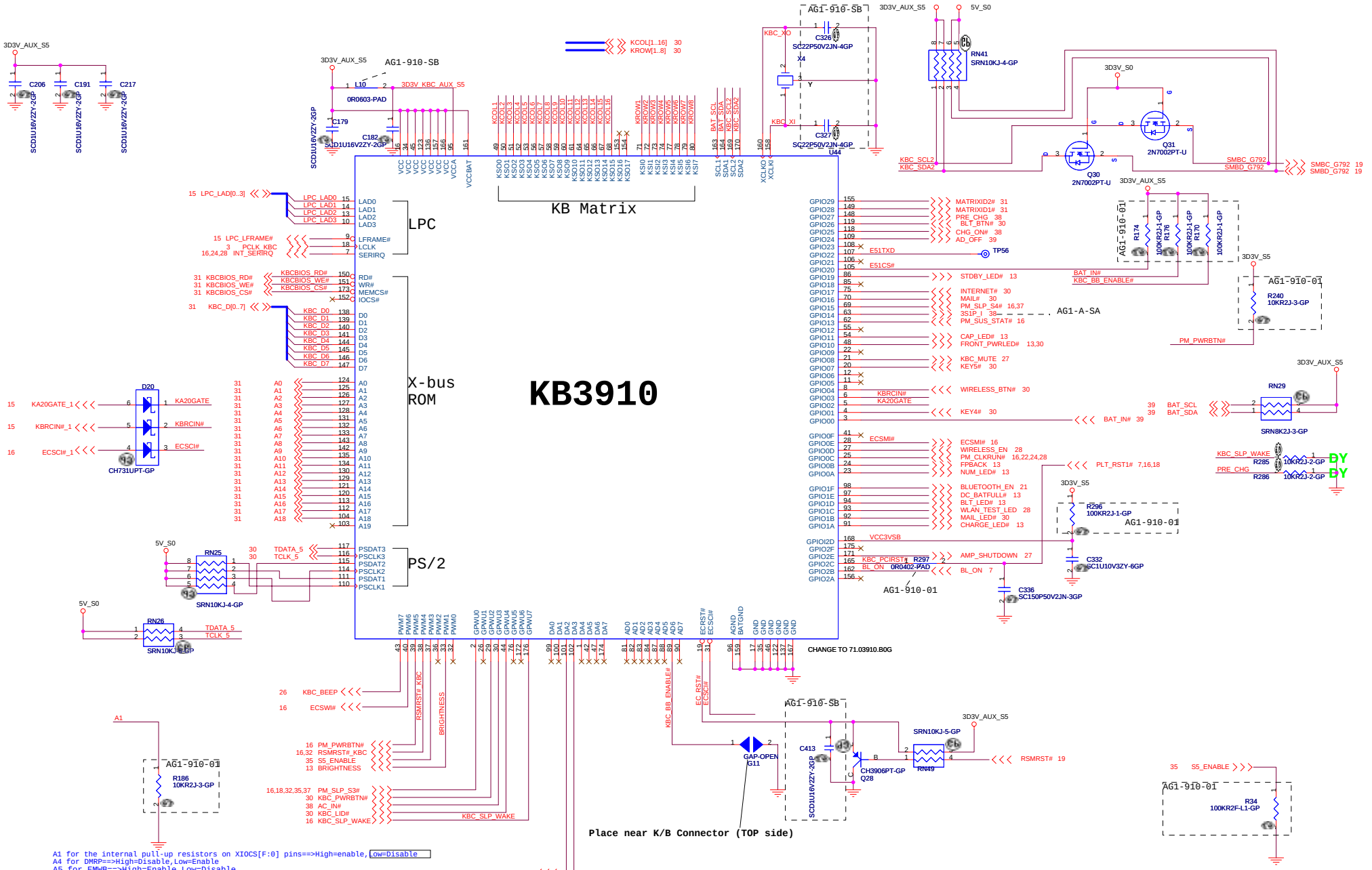
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINI-PCI***

Size	Document Number	Rev
A3	AG1(Alviso)	01

Date: Tuesday, October 25, 2005 Sheet 28 of 40



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

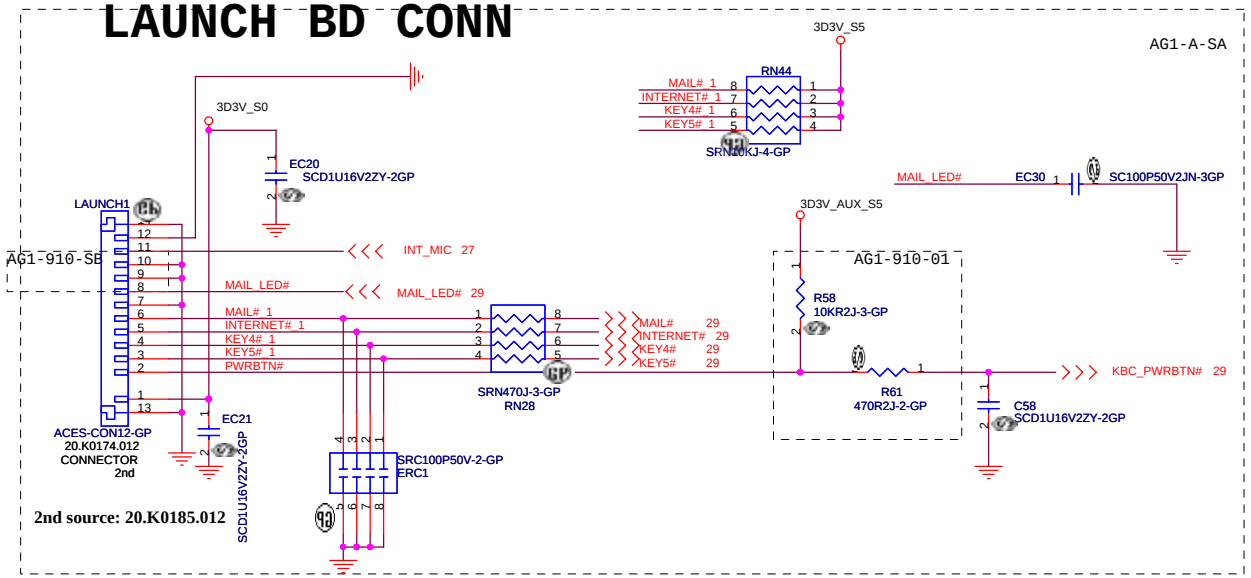
<Core Design>

Title: KBC ENE

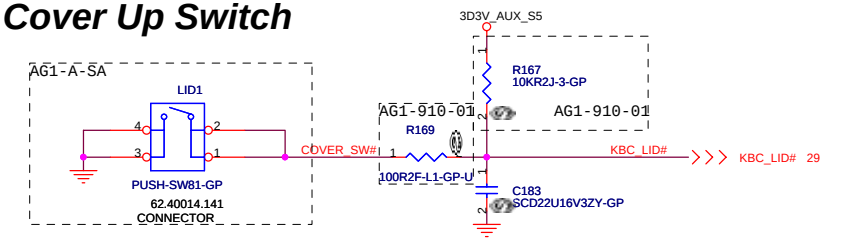
Size: Custom | Document Number: AG1(Alviso) | Rev: 01

Date: Thursday, October 27, 2005 | Sheet 29 of 40

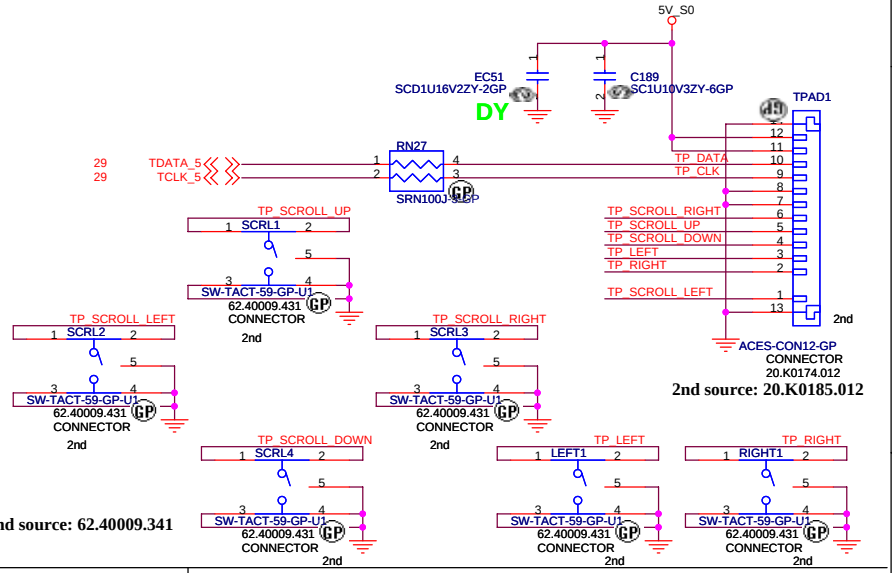
LAUNCH BD CONN

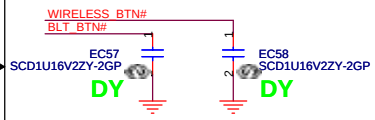


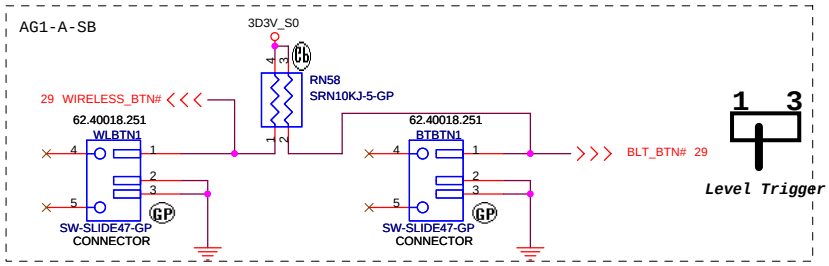
Cover Up Switch



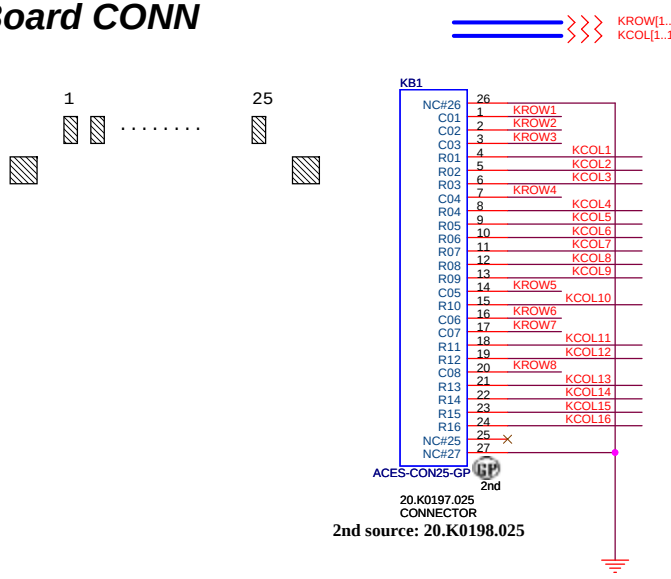
TOUCH PAD





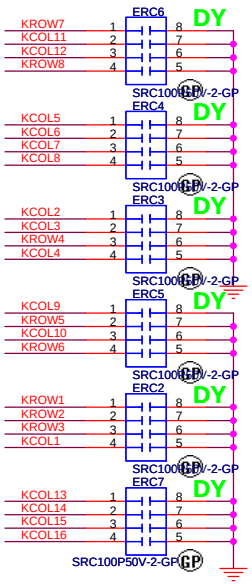


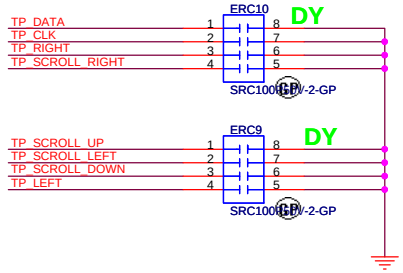
Internal KeyBoard CONN



Pin1 ==>*R01
Pin2 ==>*R02
Pin3 ==>*R03
Pin4 ==> C01
Pin5 ==> C02
Pin6 ==> C03
Pin7 ==>*R04
Pin8 ==> C04
Pin9 ==> C05
Pin10 ==> C06
Pin11 ==> C07
Pin12 ==> C08
Pin13 ==> C09
Pin14 ==>*R05
Pin15 ==> C10
Pin16 ==>*R06
Pin17 ==>*R07
Pin18 ==> C11
Pin19 ==> C12
Pin20 ==>*R08
Pin21 ==> C13
Pin22 ==> C14
Pin23 ==> C15
Pin24 ==> C16
Pin25 ==> NC

EMI Bypass cap.





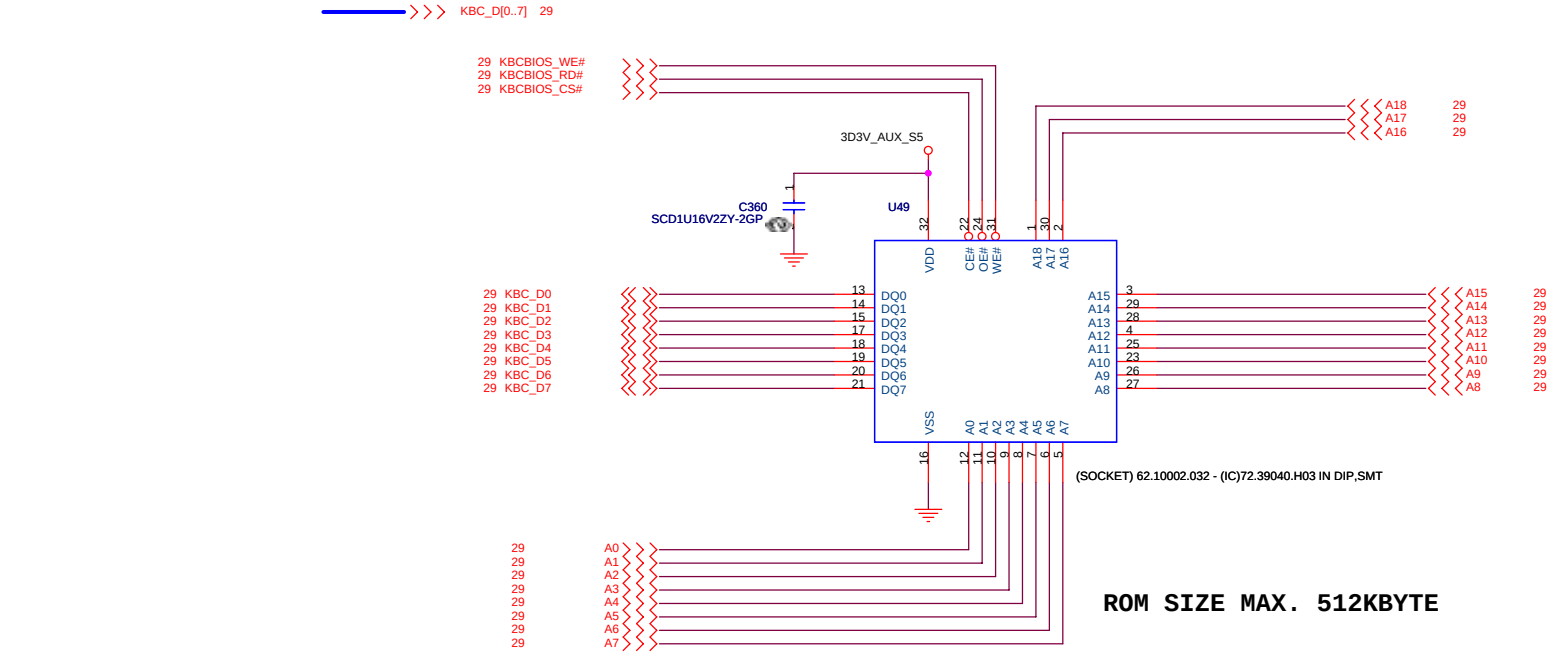
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BUTTONs / KB / TOUCHPAD

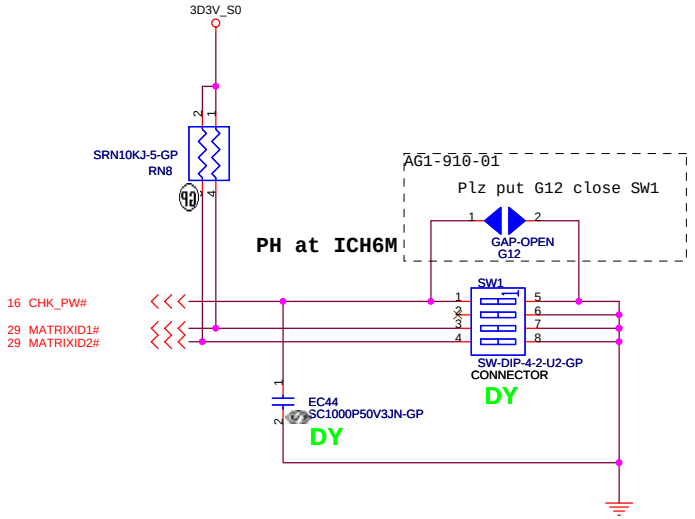
Size	Document Number	Rev
A3	AG1-910	01

Date: Wednesday, November 02, 2005 Sheet 30 of 40



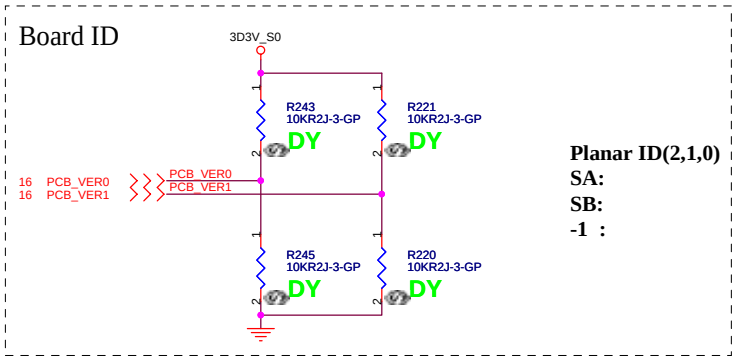
ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0



Planar ID(2,1,0)
SA:
SB:
-1 :

<Core Design>

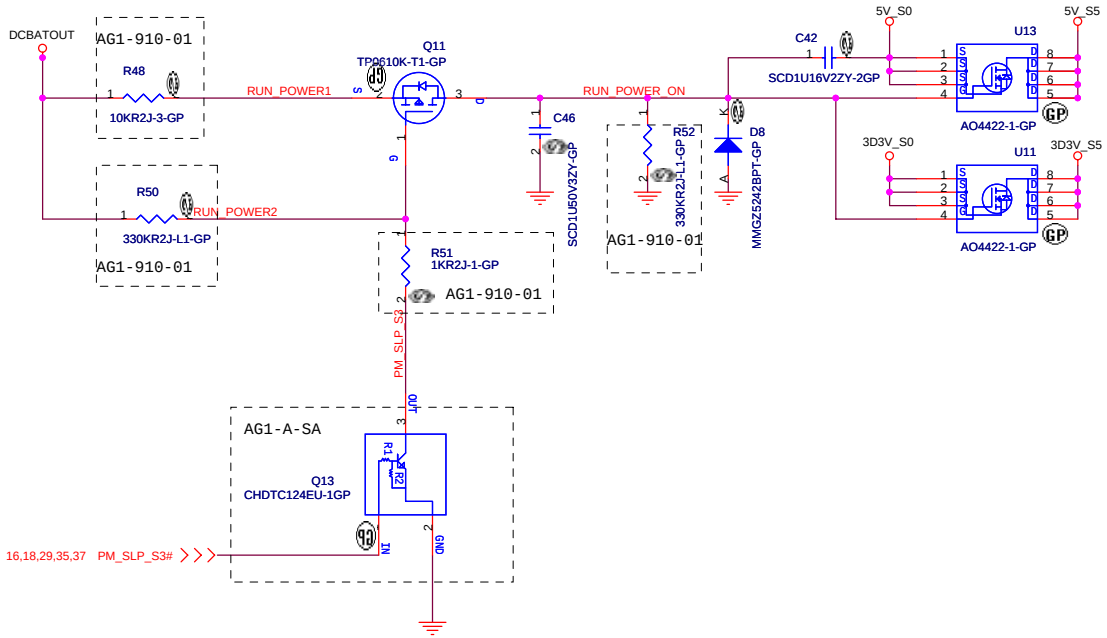
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS ROM**

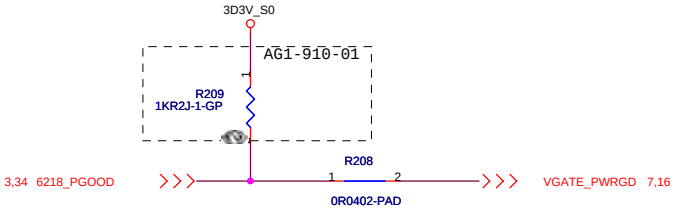
Size: A3 | Document Number: **AG1-910** | Rev: **01**

Date: Tuesday, November 01, 2005 | Sheet 31 of 40

Run Power



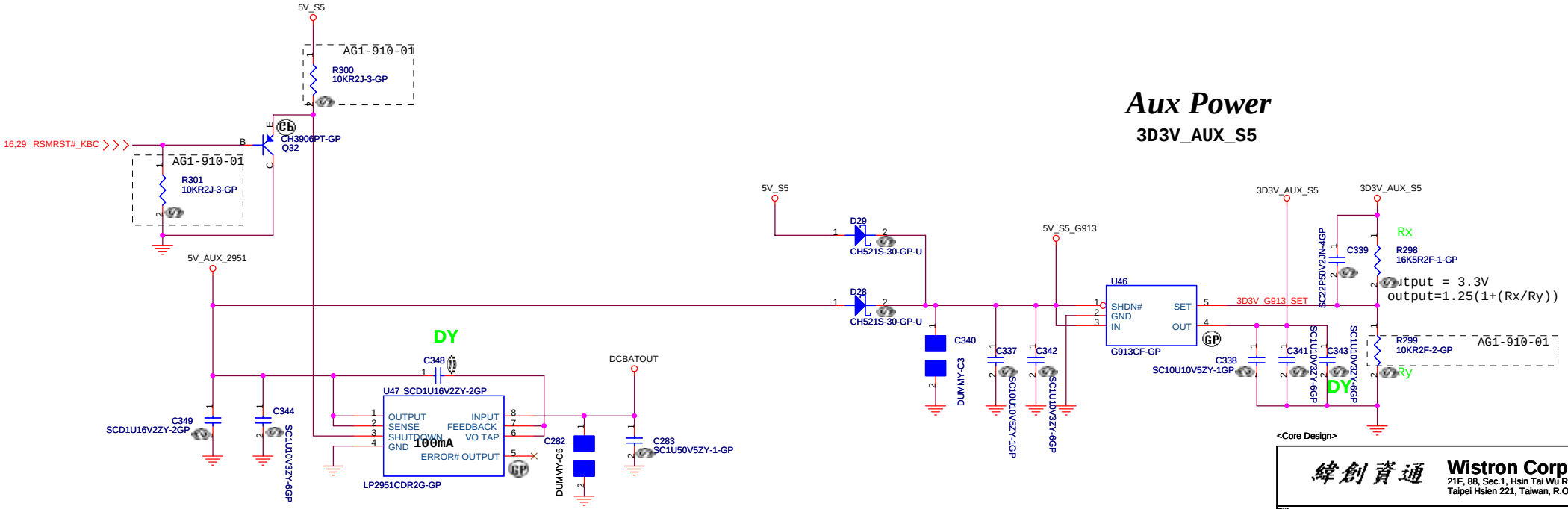
PWRGD for NB and SB



PWRGD to Turn on CPU_Core_Power

Aux Power

3D3V_AUX_S5



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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A3	AG1-910	01

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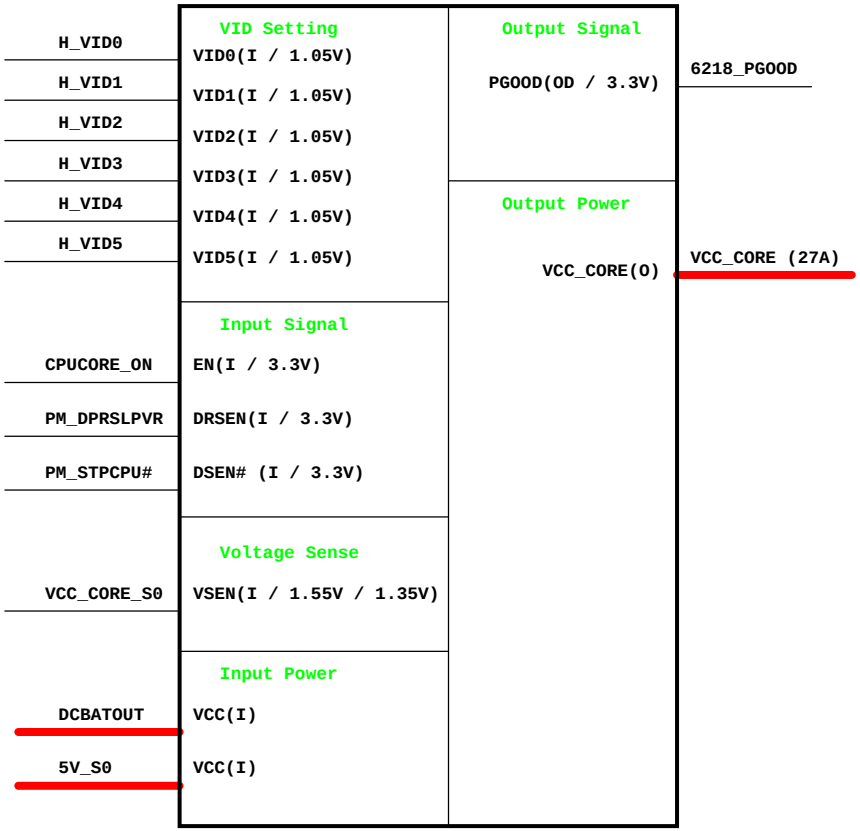
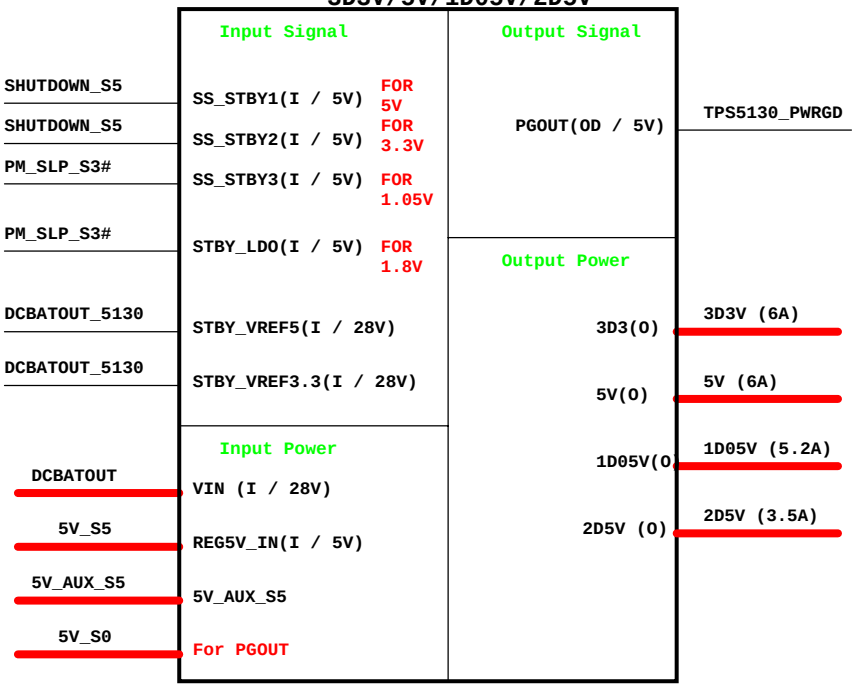
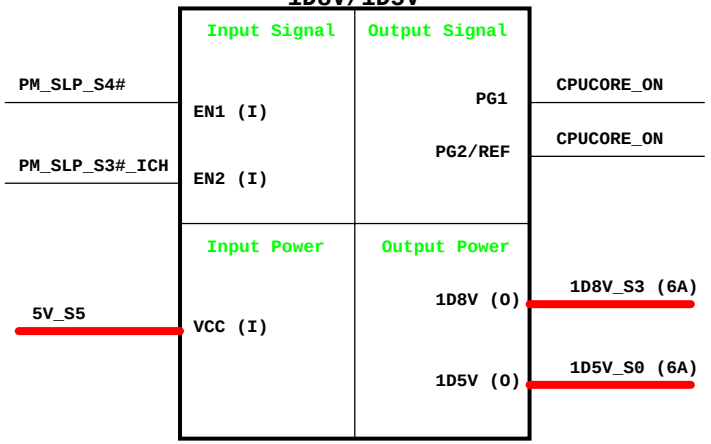
CPU_CORE ISL6218CV



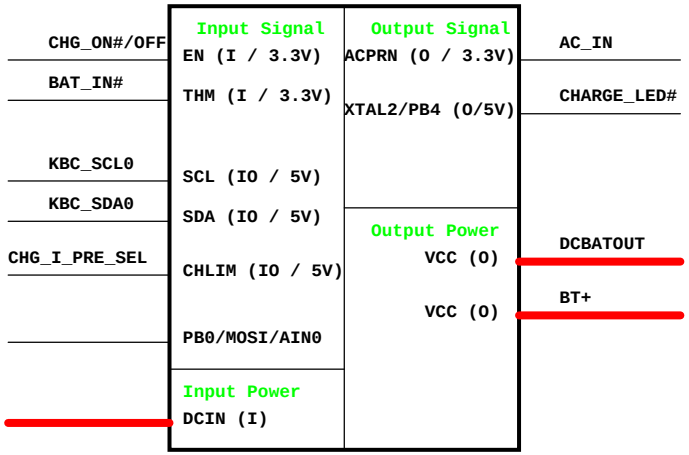
TPS5130 3D3V/5V/1D05V/2D5V



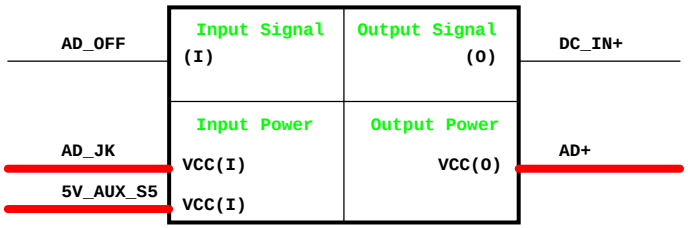
ISL6227 1D8V/1D5V



Charger_ISL6255



Adapter



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Diagram**

Size	Document Number	Rev
A3	AG1(Alviso)	01

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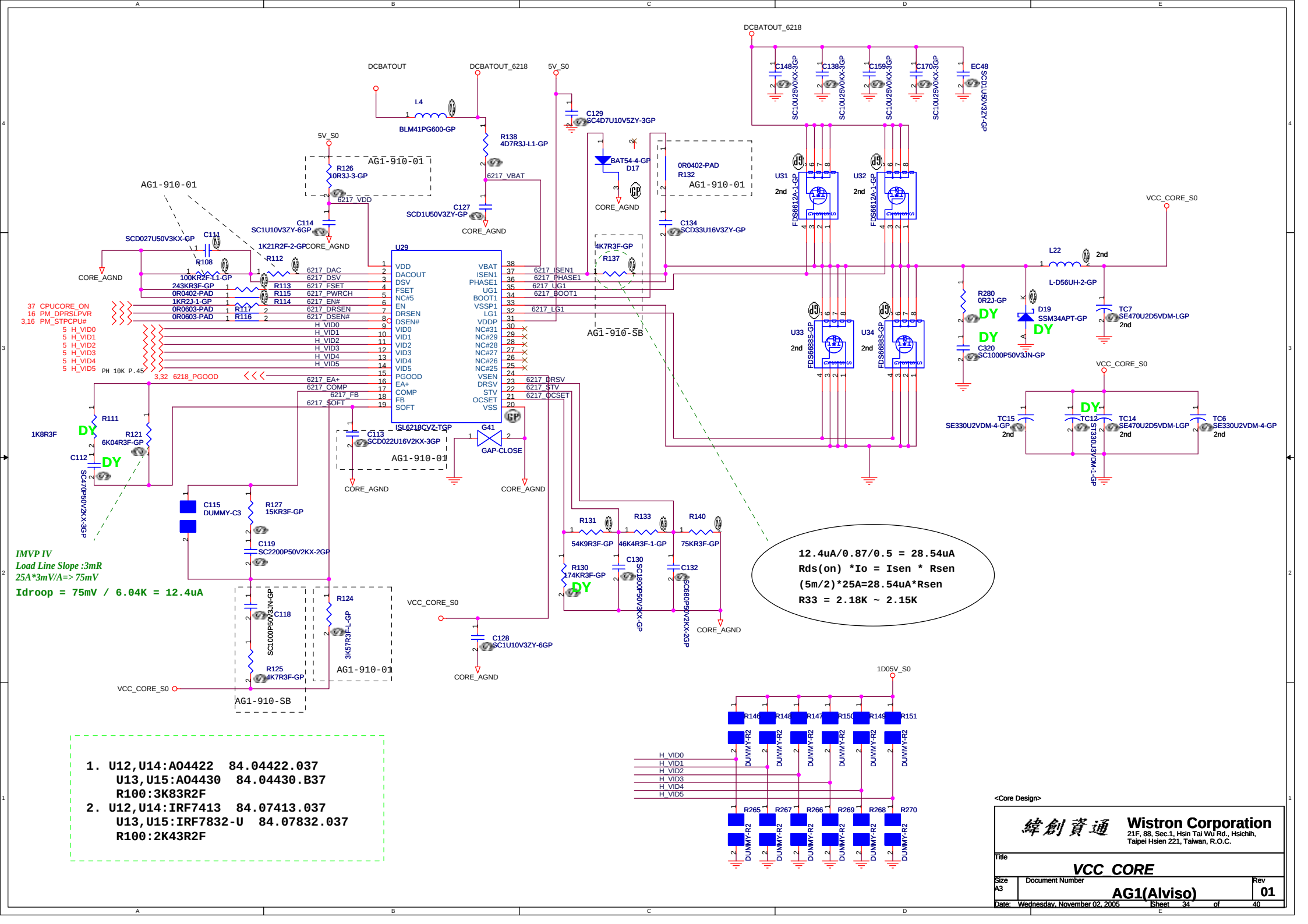
DCBATOUT_6218
DCBATOUT
5V_S0
L4
BLM41PG600-GP
R138
4D7R3J-L1-GP
6217_VBAT
C129
SC4D7U10V5ZY-3GP
BAT54-4-GP
D17
CORE_AGND
0R0402-PAD
R132
AG1-910-01
C134
SCD33U16V3ZY-GP
C148
C138
C159
C170
EC48
SC10U25V0KX-3GP
SCD1U25V0NX3ZY-GP
U31
U32
2nd
FDS6612A-1-GP
VCC_CORE_S0
L22
L-D56UH-2-GP
R280
0R2J-GP
D19
SSM34APT-GP
C320
SC1000P50V3JN-GP
TC7
SE470U2D5VDM-LGP
U33
U34
FDS6688S-GP
TC15
SE330U2VDM-4-GP
TC12
ST330U3VDM-1-GP
TC14
TC6
SE330U2VDM-4-GP
AG1-910-01
R126
10R3J-3-GP
6217_VDD
C114
SC1U10V3ZY-6GP
C127
SCD1U50V3ZY-GP
SCD027U50V3KX-GP
C111
R108
100KR2F-L1-GP
R112
1K21R2F-2-GP
R113
243KR3F-GP
R115
0R0402-PAD
R114
1KR2J-1-GP
R117
0R0603-PAD
R116
0R0603-PAD
37 CPUCORE_ON
16 PM_DPRSLPVR
3,16 PM_STPCPU#
5 H_VID0
5 H_VID1
5 H_VID2
5 H_VID3
5 H_VID4
5 H_VID5
PH 10K P.45
3,32 6218_PGOOD
U29
ISL6218CVZ-TGP
VDD
DACOUT
DSV
FSET
NC#5
EN
DRSEN
DSEN#
VID0
VID1
VID2
VID3
VID4
VID5
PGOOD
EA+
COMP
FB
SOFT
VBAT
ISEN1
PHASE1
UG1
BOOT1
VSSP1
LG1
VDDP
NC#31
NC#29
NC#28
NC#27
NC#26
NC#25
VSEN
DRSV
STV
OCSET
VSS
6217_DAC
6217_DSV
6217_FSET
6217_PWRCH
6217_EN#
6217_DRSEN
6217_DSEN#
6217_EA+
6217_COMP
6217_FB
6217_SOFT
6217_ISEN1
6217_PHASE1
6217_UG1
6217_BOOT1
6217_LG1
6217_DRSV
6217_STV
6217_OCSET
4K7R3F-GP
R137
AG1-910-SB
R111
1K8R3F
R121
6K04R3F-GP
C112
SC470P50V2KX-3GP
C113
SCD022U16V2KX-3GP
G41
GAP-CLOSE
C115
DUMMY-C3
R127
15KR3F-GP
C119
SC2200P50V2KX-2GP
C118
SC1000P50V3JN-GP
R125
4K7R3F-GP
R124
3K57R3F-L-GP
R131
54K9R3F-GP
R133
46K4R3F-1-GP
R140
75KR3F-GP
R130
174KR3F-GP
C130
SC1800P50V3KX-GP
C132
SC6800P50V2KX-3GP
C128
SC1U10V3ZY-6GP
1D05V_S0
R146
R148
R147
R150
R149
R151
R265
R267
R266
R269
R268
R270
DUMMY-R2
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
IMVP IV
Load Line Slope :3mR
25A*3mV/A=> 75mV
Idroop = 75mV / 6.04K = 12.4uA
12.4uA/0.87/0.5 = 28.54uA
Rds(on) *Io = Isen * Rsen
(5m/2)*25A=28.54uA*Rsen
R33 = 2.18K ~ 2.15K
1. U12,U14:AO4422 84.04422.037
U13,U15:AO4430 84.04430.B37
R100:3K83R2F
2. U12,U14:IRF7413 84.07413.037
U13,U15:IRF7832-U 84.07832.037
R100:2K43R2F
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VCC_CORE
Size
A3
Document Number
AG1(Alviso)
Rev
01
Date: Wednesday, November 02, 2005
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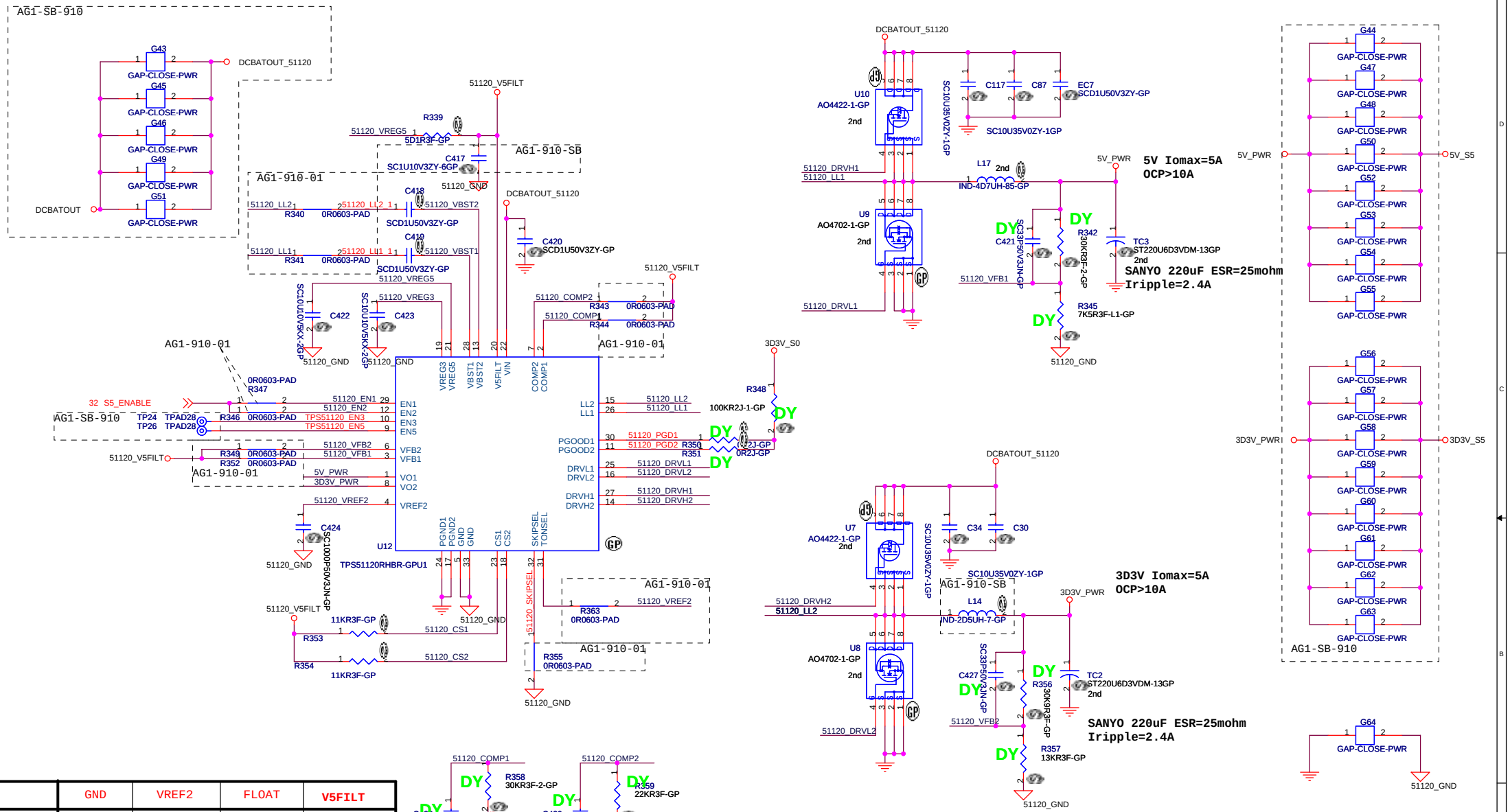

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

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Title: ***TPS51120_3D3V_5V***

Size	Document Number	Rev
A3	**AG1(Alviso)**	**01**

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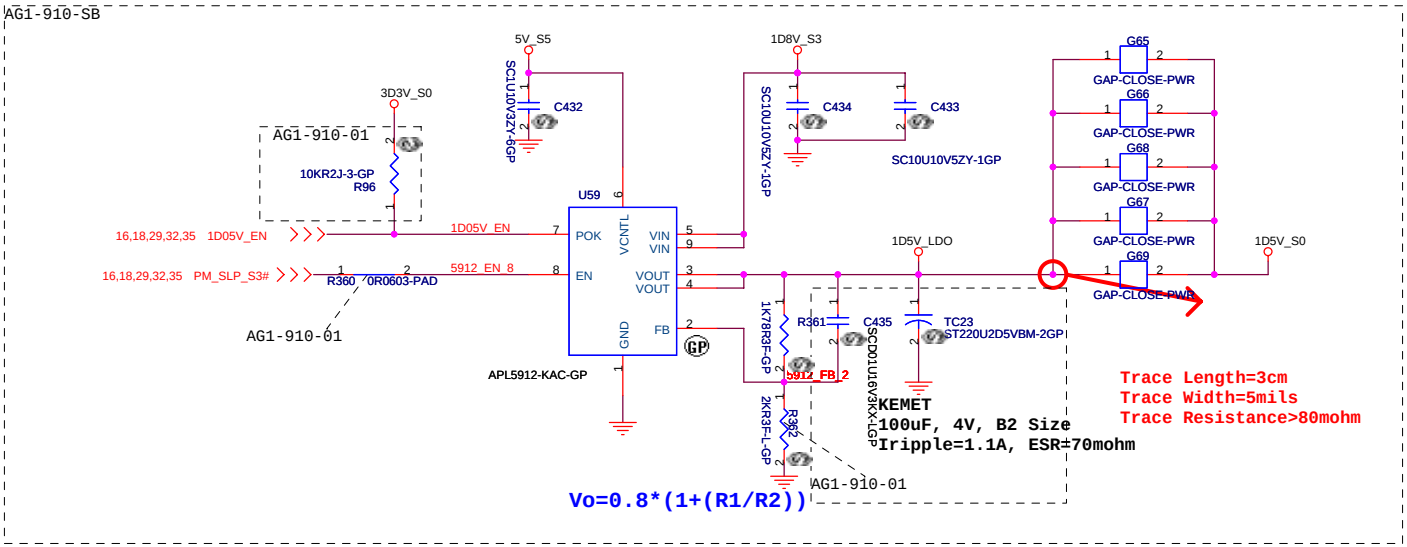

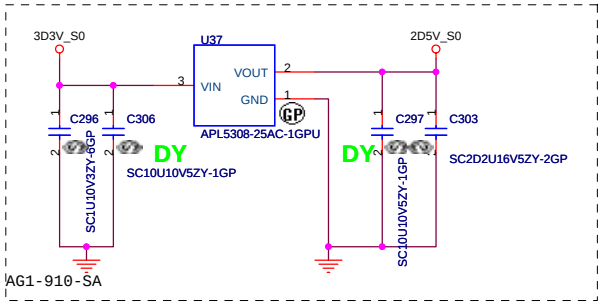

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D5V/2D5V(LDO)

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A3	AG1(Alviso)	01

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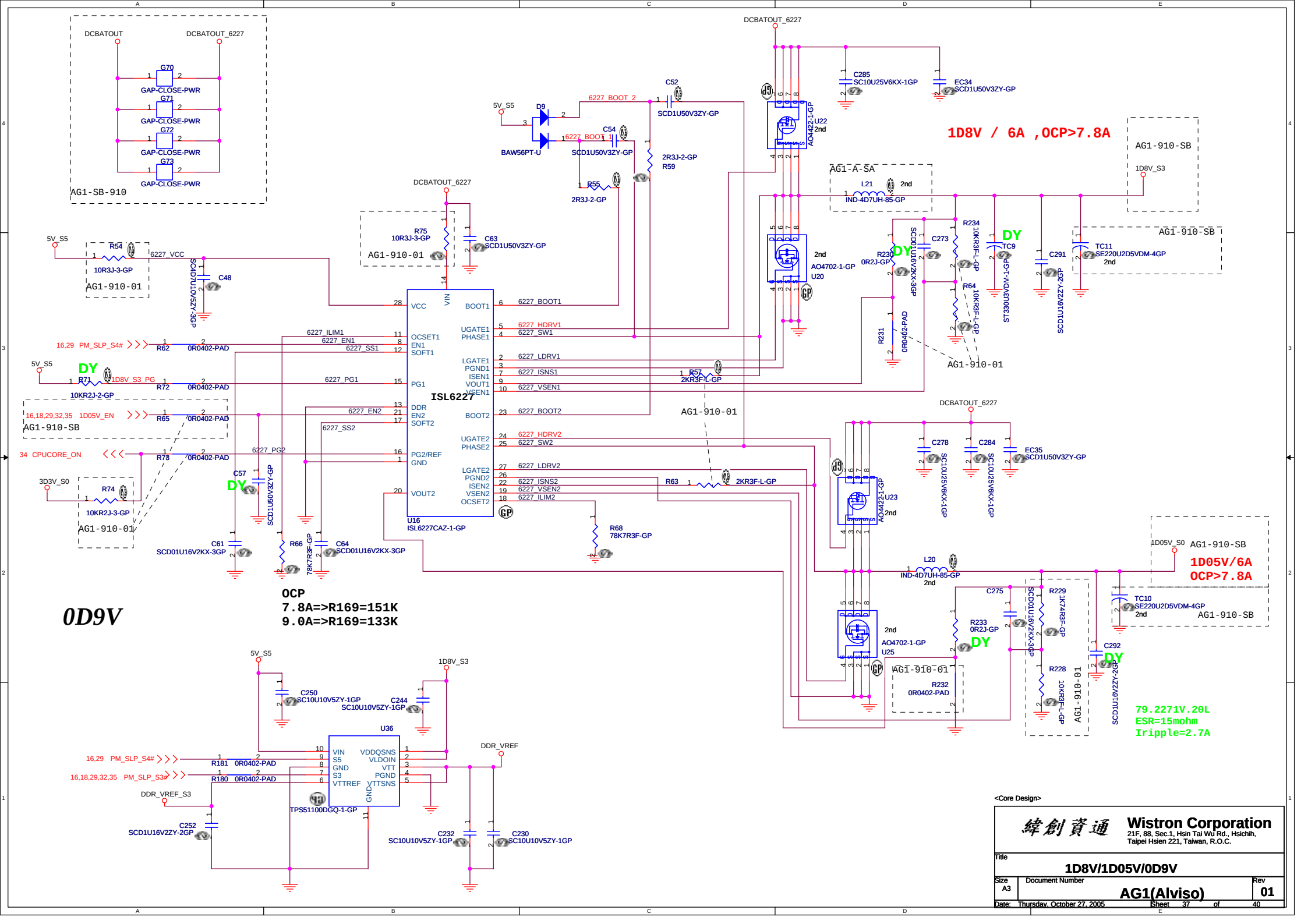
DCBATOUT
DCBATOUT_6227
G70
G71
G72
G73
GAP-CLOSE-PWR
AG1-SB-910
1D8V / 6A ,OCP>7.8A
AG1-910-SB
1D8V_S3
AG1-A-SA
L21
IND-4D7UH-85-GP
ISL6227
U16
ISL6227CAZ-1-GP
AO4422-1-GP
U22
AO4702-1-GP
U20
U23
U25
U36
TPS51100DGQ-1-GP
0D9V
OCP
7.8A=>R169=151K
9.0A=>R169=133K
1D05V/6A
OCP>7.8A
79.2271V.20L
ESR=15mohm
Iripple=2.7A
DDR_VREF
DDR_VREF_S3
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
1D8V/1D05V/0D9V
Size A3
Document Number
AG1(Alviso)
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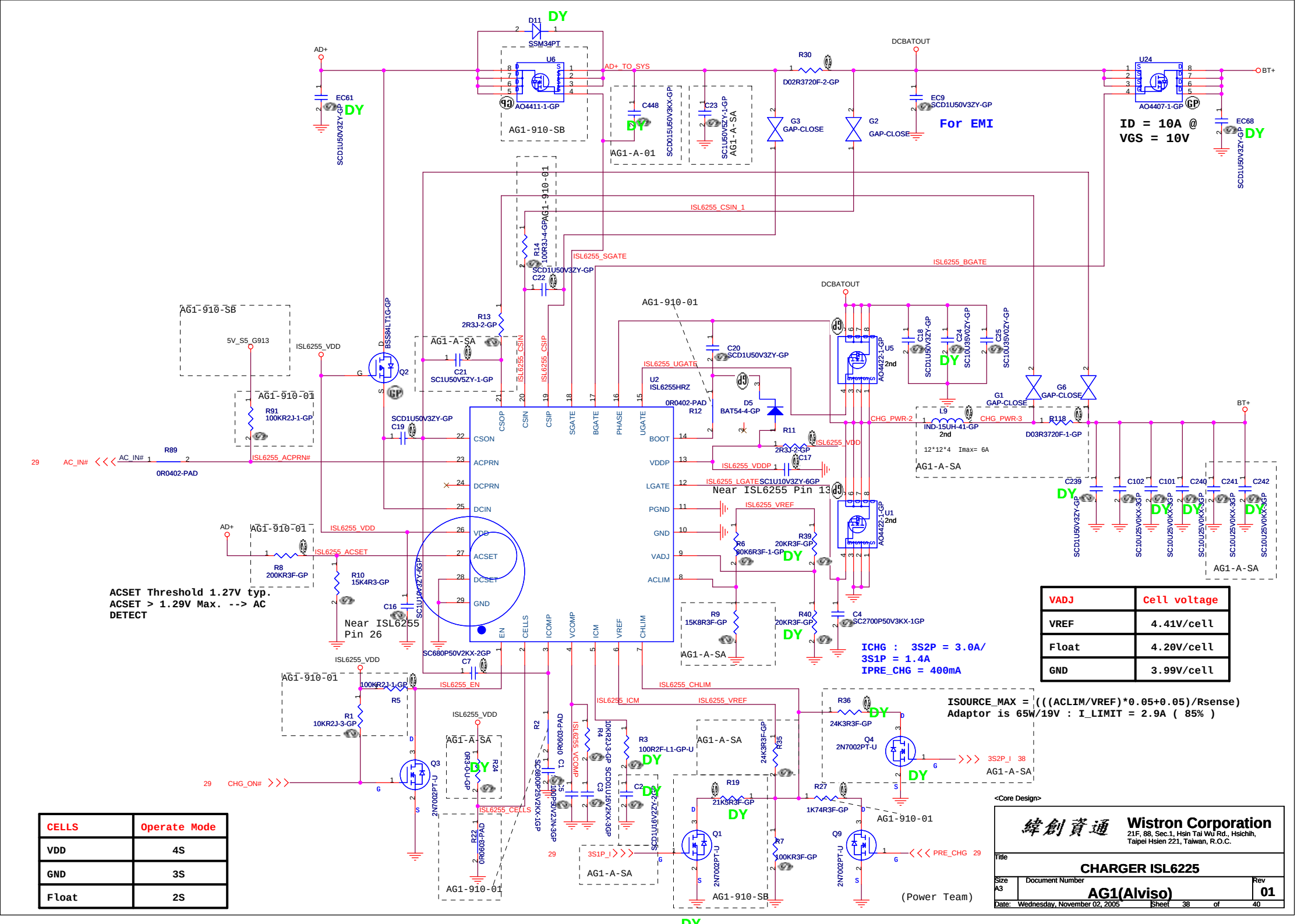

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

<Core Design>
緯創資通 Wistron Corporation
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Title: CHARGER ISL6225

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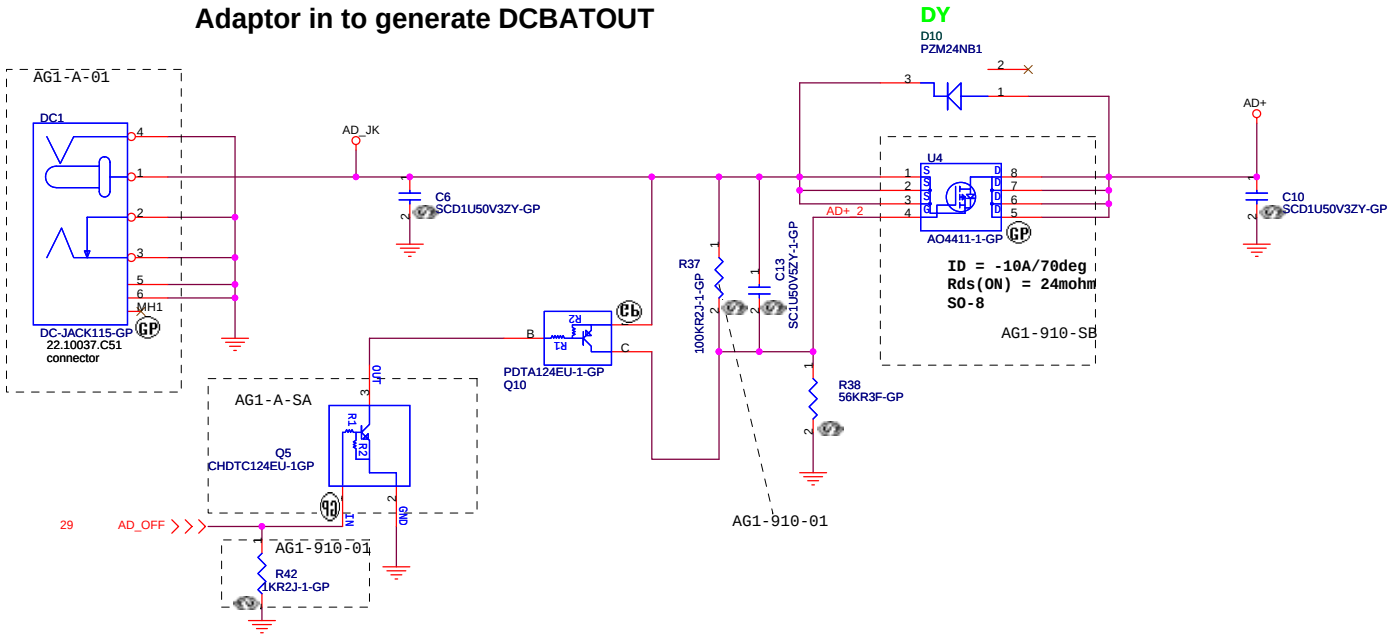
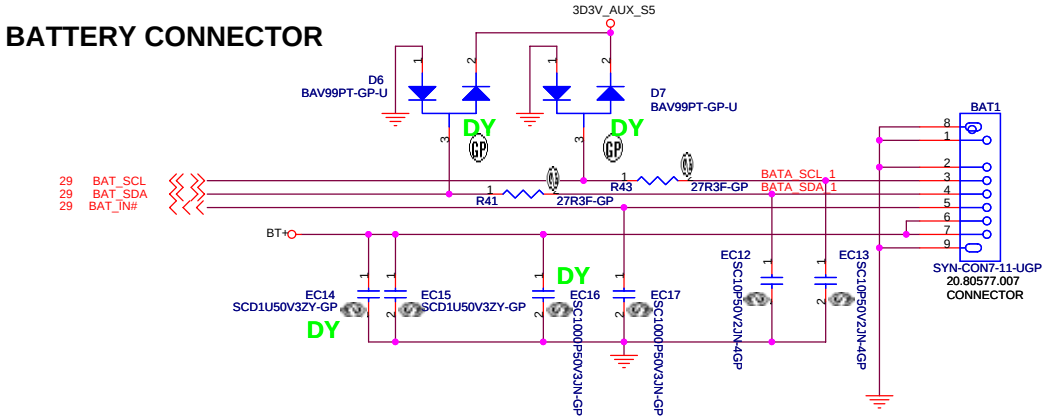
Adaptor in to generate DCBATOUT

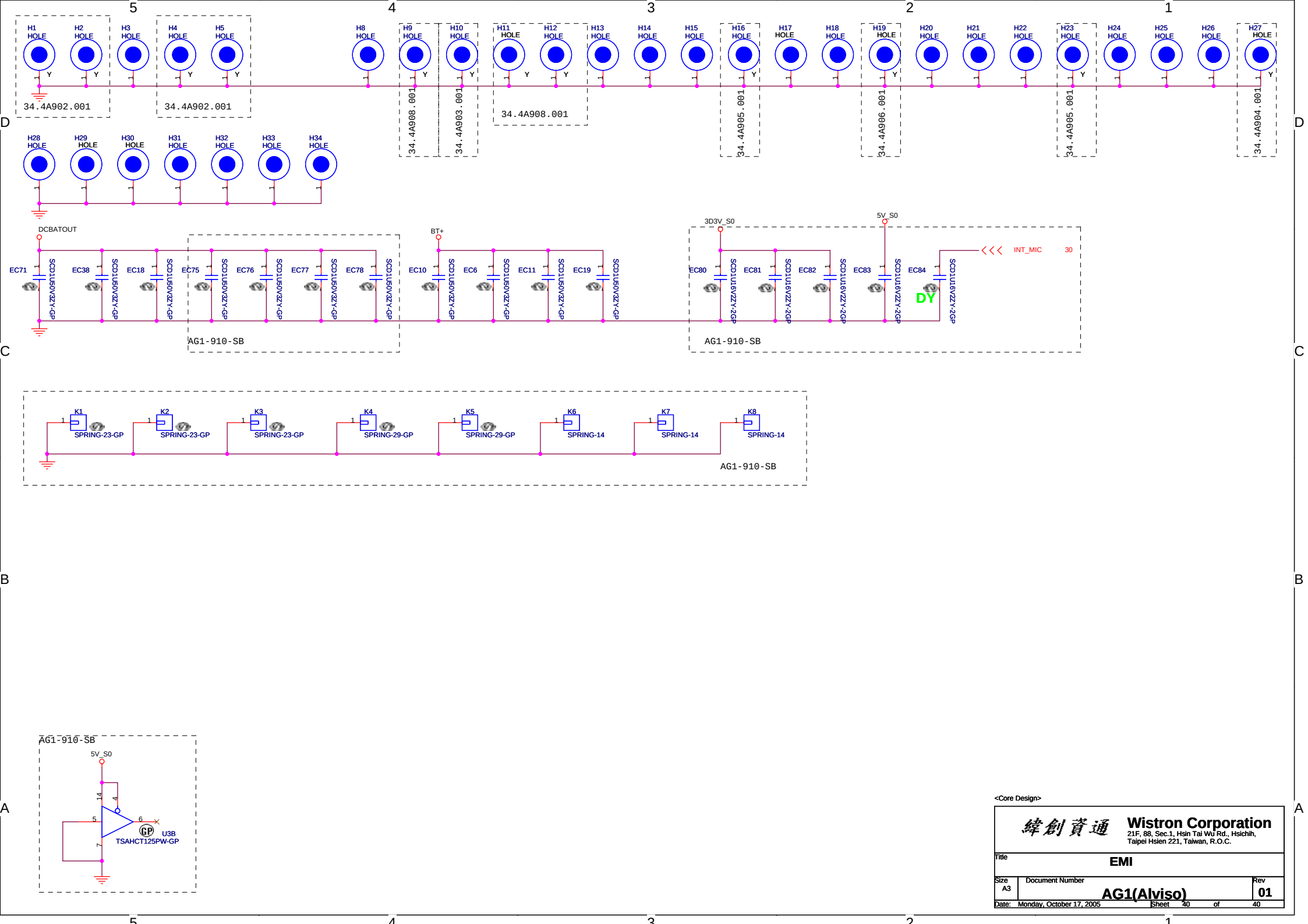


BATTERY CONNECTOR



<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AD/BATT CONN
Size A3 / Document Number	AG1(Alviso) / Rev 01
Date: Tuesday, November 01, 2005	Sheet 39 of 40



<Core Design>

緯創資通 **Wistron Corporation**
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Title	EMI	
Size A3	Document Number AG1(Alviso)	Rev 01
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