SM30 Block Diagram

Project code: 91.4BT01.001
PCB P/N : 48.4BT01.001
Revision : 08239-SA

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

Crystal 14.318MHz
CLK GEN. ICS 9LPRS929 3
Mobile CPU Penryn 4, 5
SMSC EMC2103 29
HOST BUS 667/800/1066MHz@1.05V
DDR3 800/1033 MHz 12,13
DDR3 800/1033 MHz 12,13
Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11
LCD 15
CRT 17
X4 DMI 400MHz
C-Link0
Crystal 32.768KHz
Crystal 25MHz
LAN Giga LAN BCM5764
TXFM
RJ45
Mini Card (Robson2/3G)
Mini Card Kedron a/b/g/n 28 (WLAN)
PCIe
ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
18,19,20,21
Int MIC 15
MIC In 32
32
Line Out (SPDIF)
Codec ALC272 30
AZALIA
32
INT.SPKR 1.5W
OP AMP G1454 31
LPC BUS
Crystal 32.768KHz
KBC Winbond WPCE773LA0DG 33
SPI
BIOS (2MB) 34
Launch Buttom 35
LPC DEBUG CONN. 34
Touch Pad 33
INT. KB 33
Daughter Board 08621
Launch Board
SATA
USB
HDD SATA 23
ODD SATA 22
Mini USB Blue Tooth 24
Finger Printer 26
USB 2 Port 25
Camera 15
USB 1 Port
CardReader Realtek RTS5159 27
MS/MS Pro/xD /MMC/SD 5 in 1 27

SYSTEM DC/DC TPS51125 50	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 51	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M(16A) 1D5V_S3(12A)

RT9026 52	
1.5V_S3	DDR_VREF_S3 (1.2A)

G9131 52	
3D3V_S0	2D5V_S0 (300mA)

TPS51117 54	
DCBATOUT	1D8V_S0 (9.4A)

CHARGER BQ24750 55	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ISL6266A 49	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A

GFX DC/DC ISL6263 53	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

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Title: BLOCK DIAGRAM
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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

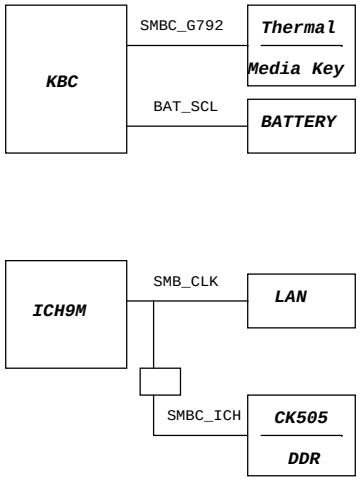
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SMBus



USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	NC
3	MINIC2(WLAN)
4	CAMERA
5	NC
6	FingerPrint
7	BLUETOOTH
8	NC
9	USB1(IO board)
10	MINIC1(IO BOARD)
11	CARD READER

PCIE Routing

LANE1	LAN BCM5764
LANE2	MiniCard WLAN
LANE3	MiniCard(Robson2G/3G)

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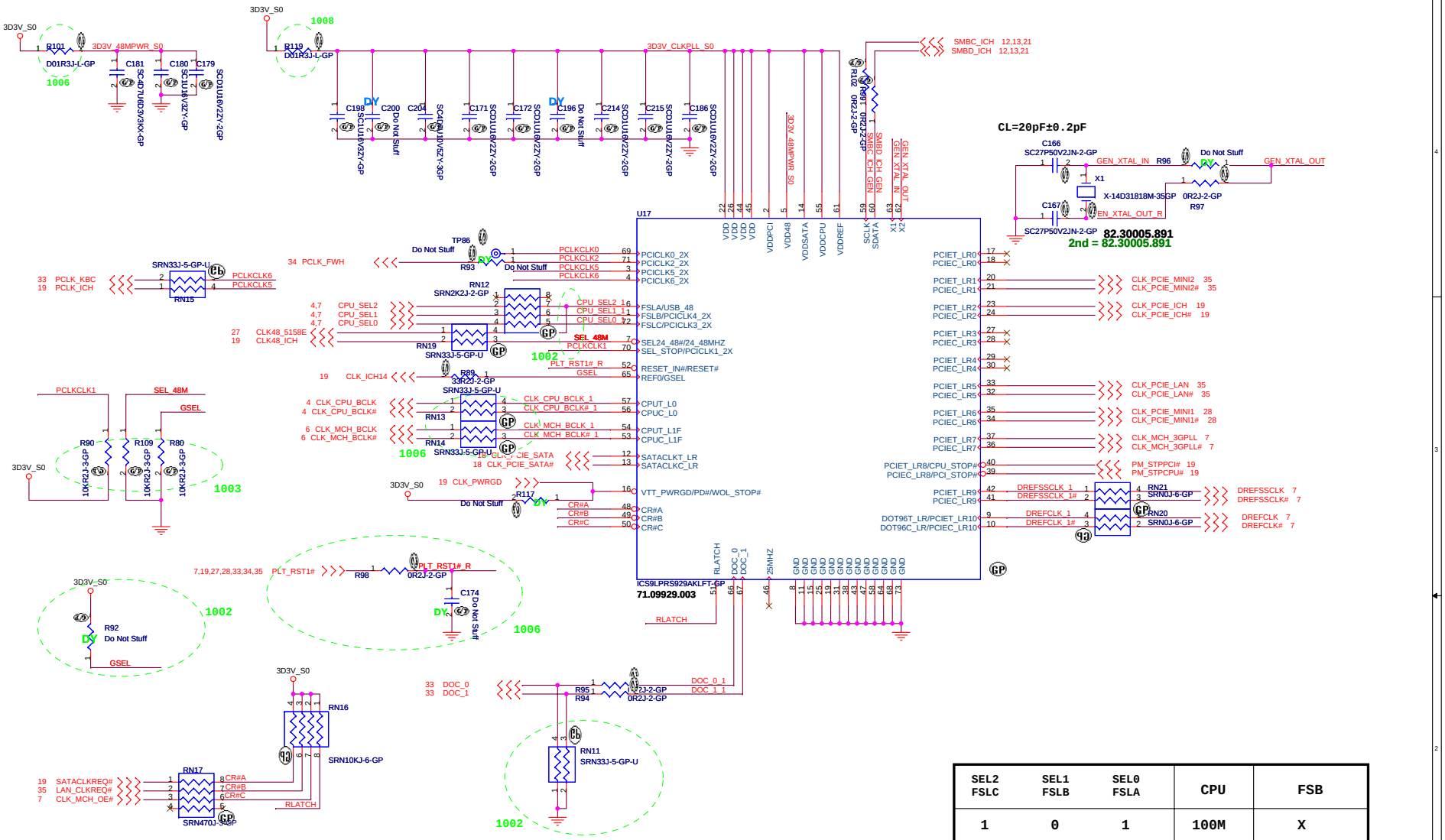

SEL2 FSLC	SEL1 FSLB	SEL0 FSLA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

GSEL	DOT Freq
0	100MHZ
1	96MHZ

SEL_STOP	Selects pin 39/40
0	PCI_STOP#/CPU_STOP#
1	PCIEX outputs

SEL24_48#/24_48MHZ	OUTPUT
0	24MHZ
1	48MHZ

DOC_0	Real Time Frequency
0	Normal
1	Frequency will transition to a preprogrammed value in the I2C

DOC_1	Real Time Frequency
0	Normal
1	Frequency will transition to a preprogrammed value in the I2C

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Title: **Clock Generator**

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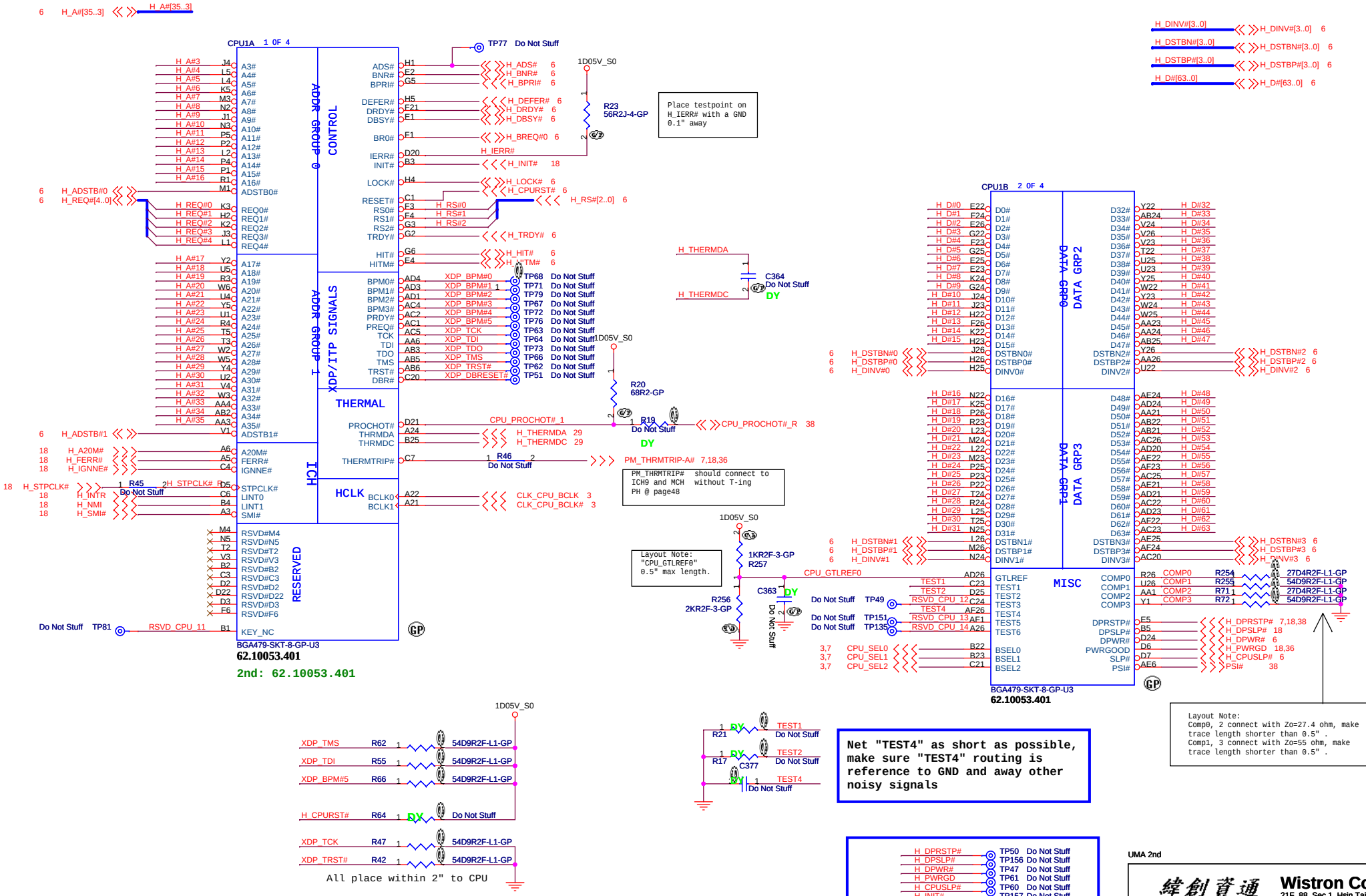
CPU1A 1 OF 4
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
HCLK
RESERVED
ICH
BGA479-SKT-8-GP-U3
62.10053.401
2nd: 62.10053.401
CPU1B 2 OF 4
DATA GRP2
DATA GRP0
DATA GRP3
DATA GRP1
MISC
BGA479-SKT-8-GP-U3
62.10053.401
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
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Title: CPU (1 of 2)
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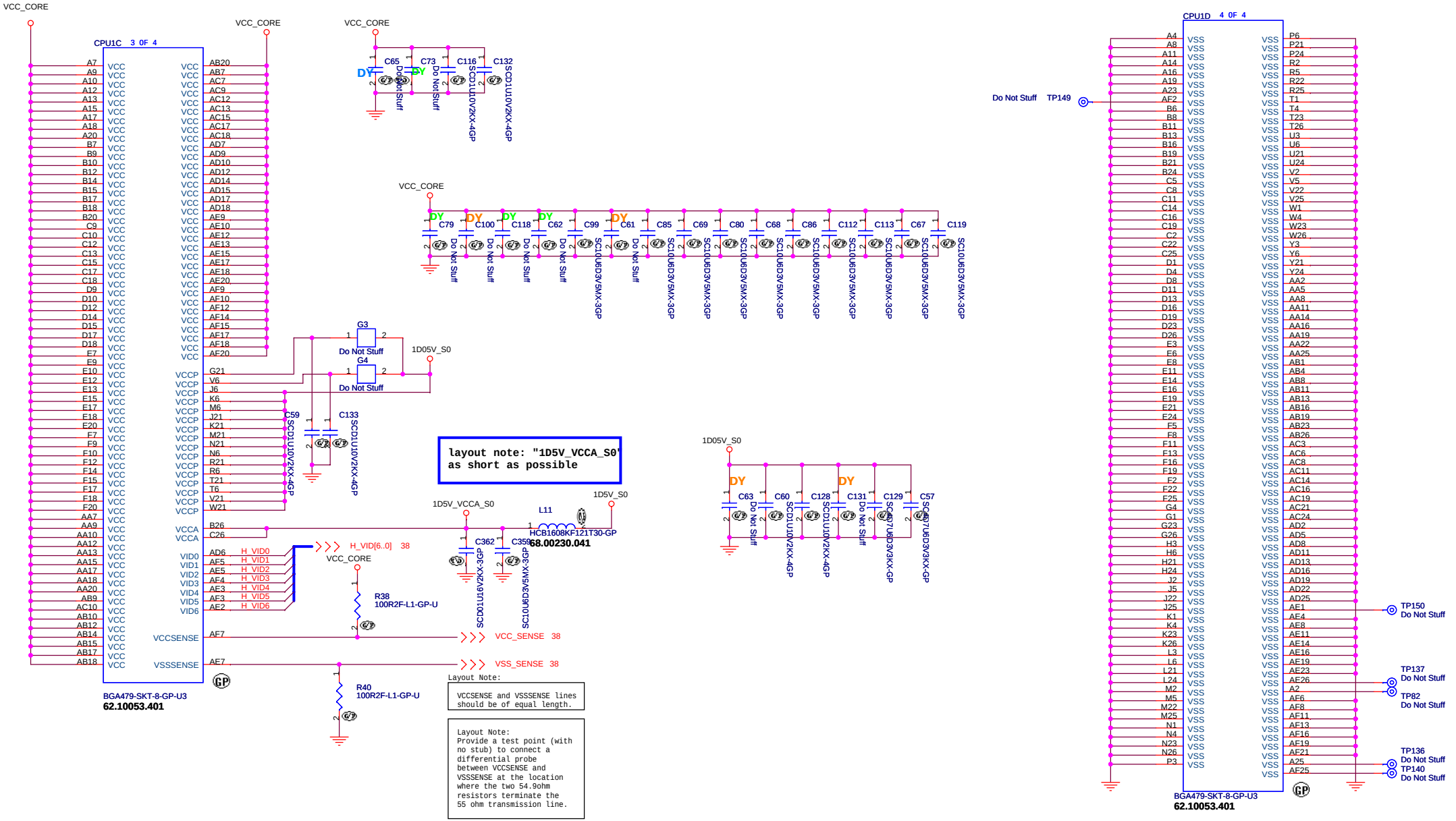

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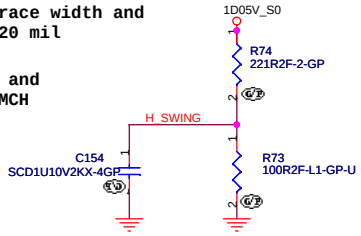
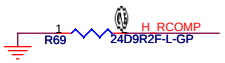
H_SWING routing Trace width and Spacing use 10 / 20 mil

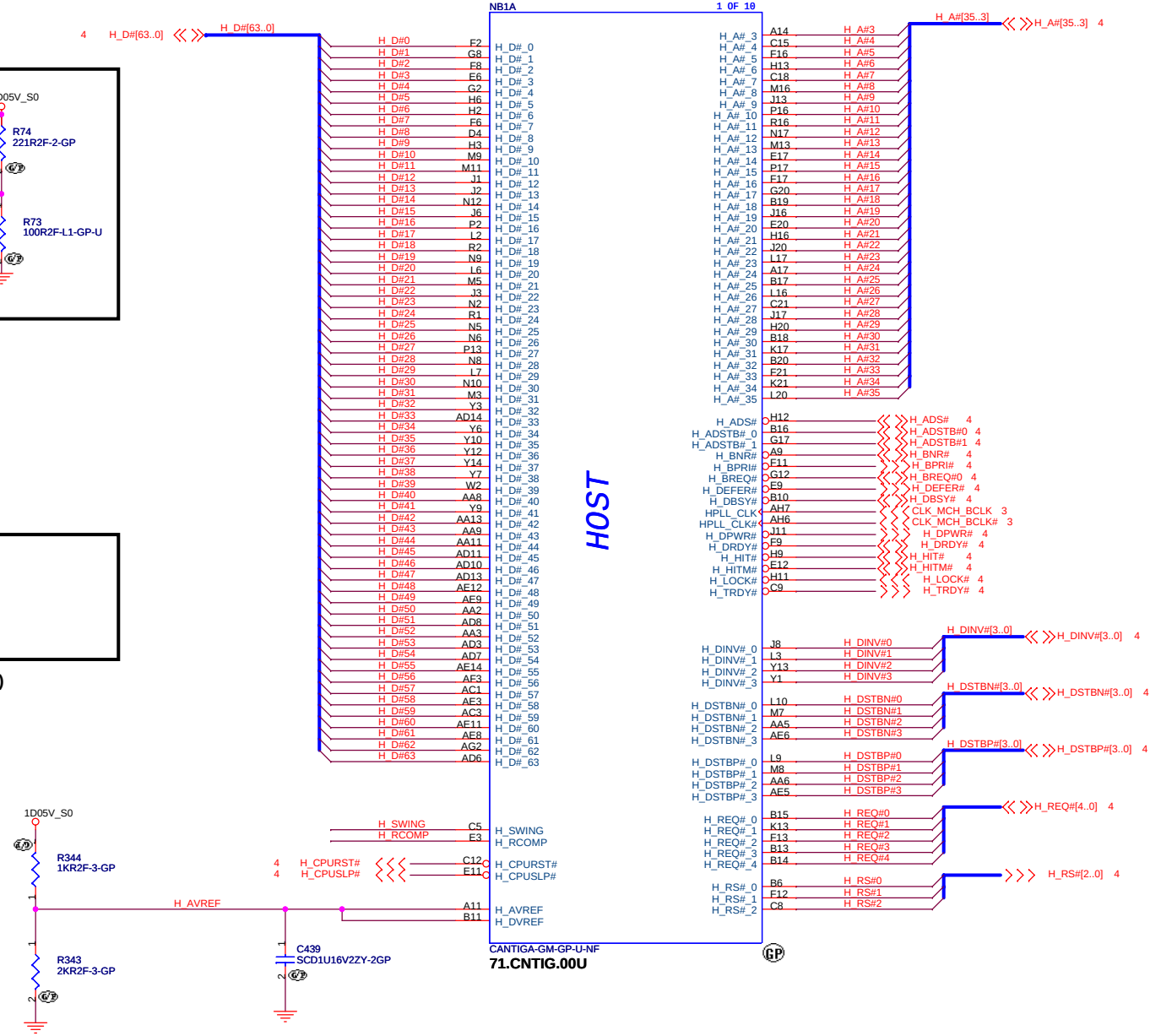
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Title	***Cantiga (1 of 6)***	
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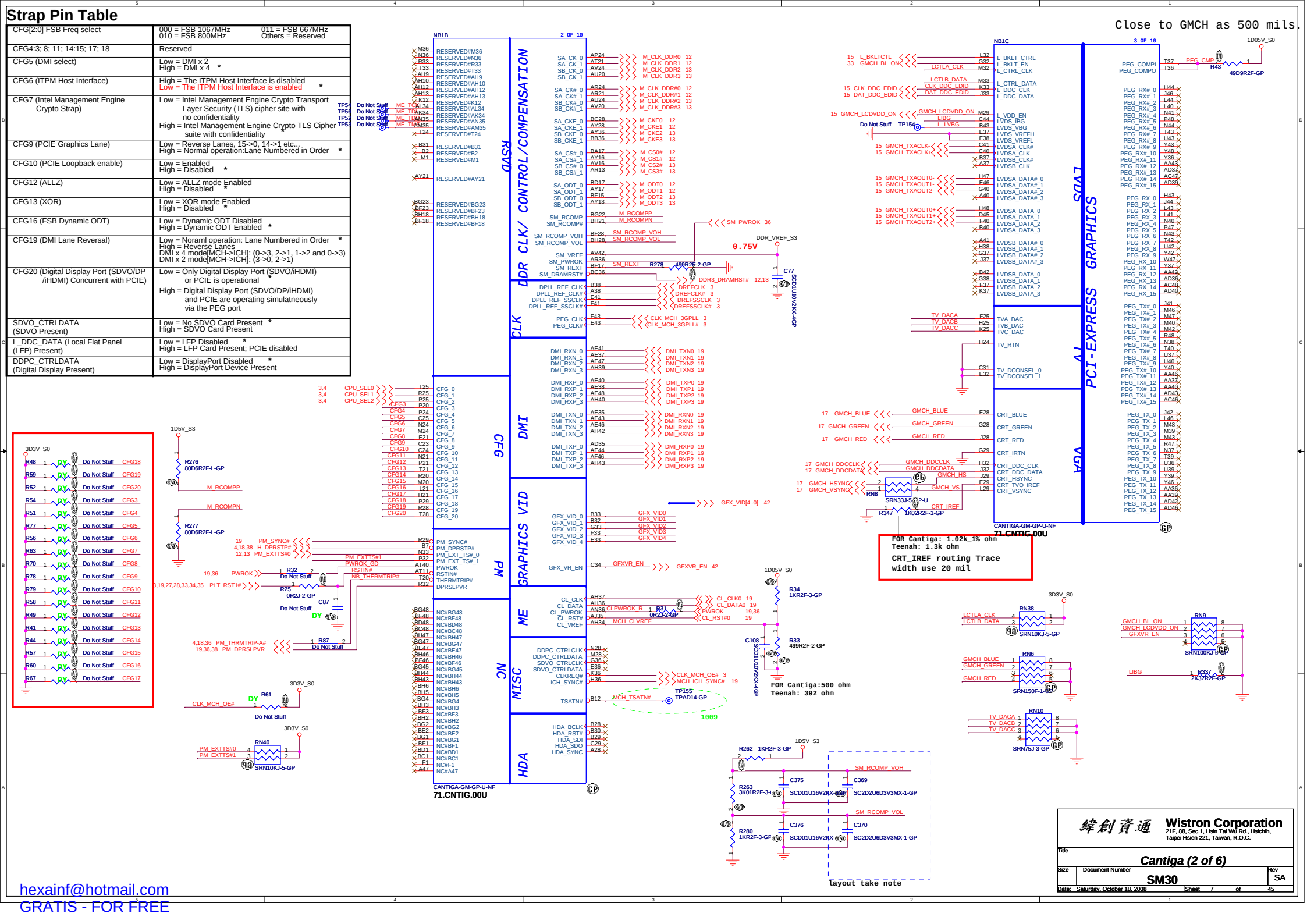
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1067MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG4:3; 8; 11; 14:15; 17; 18	Reserved
CFG5 (DMI select)	Low = DMI x 2 High = DMI x 4 *
CFG6 (ITPM Host Interface)	High = The ITPM Host Interface is disabled Low = The ITPM Host Interface is enabled *
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher site with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality *
CFG9 (PCIE Graphics Lane)	Low = Reverse Lanes, 15->0, 14->1 etc... High = Normal operation:Lane Numbered in Order *
CFG10 (PCIE Loopback enable)	Low = Enabled High = Disabled *
CFG12 (ALLZ)	Low = ALLZ mode Enabled High = Disabled *
CFG13 (XOR)	Low = XOR mode Enabled High = Disabled *
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled *
CFG19 (DMI Lane Reversal)	Low = Noraml operation: Lane Numbered in Order * High = Reverse Lanes DMI x 4 mode[MCH->ICH]: (0->3, 2->1, 1->2 and 0->3) DMI x 2 mode[MCH->ICH]: (3->0, 2->1)
CFG20 (Digital Display Port (SDVO/DP /iHDMI) Concurrent with PCIE)	Low = Only Digital Display Port (SDVO/iHDMI) or PCIE is operational * High = Digital Display Port (SDVO/DP/iHDMI) and PCIE are operating simulatneously via the PEG port
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present * High = SDVO Card Present
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled * High = LFP Card Present; PCIE disabled
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled * High = DisplayPort Device Present

Close to GMCH as 500 mils.



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Title: Cantiga (2 of 6)	
Size:	Document Number: SM30 Rev: SA
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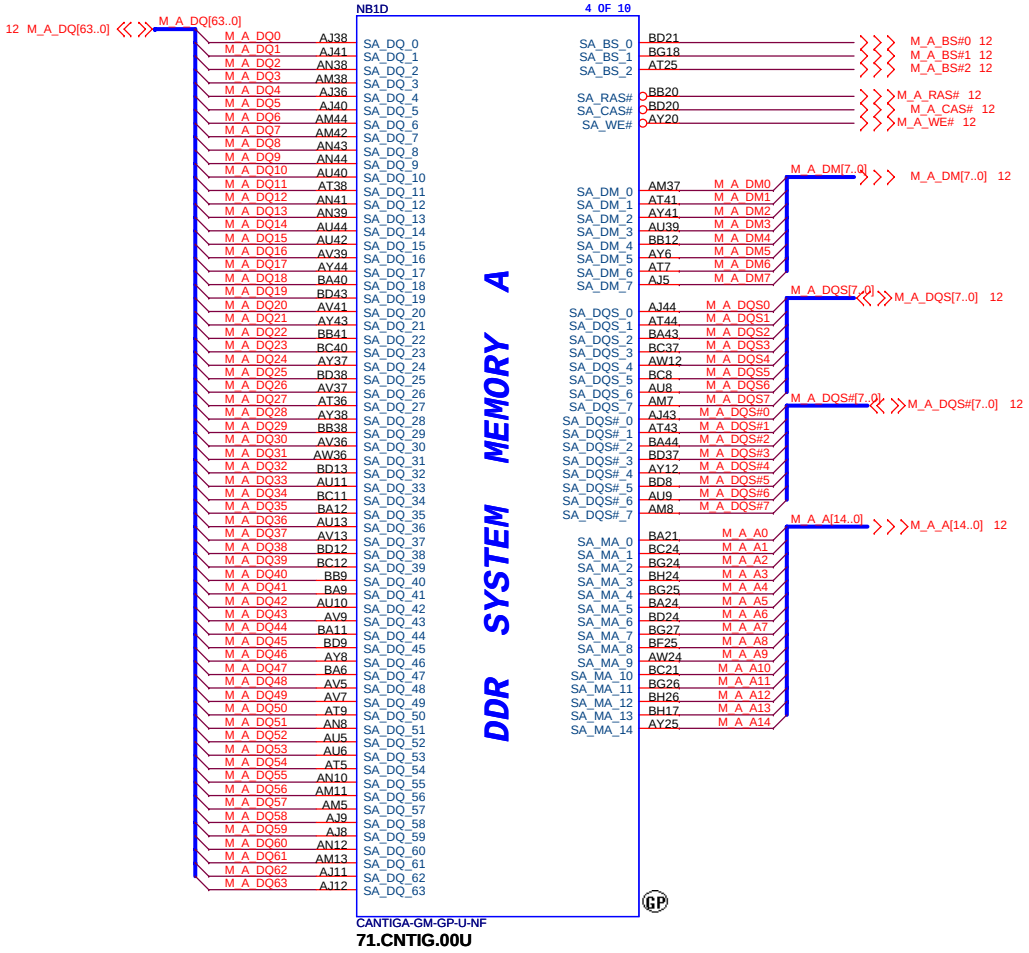

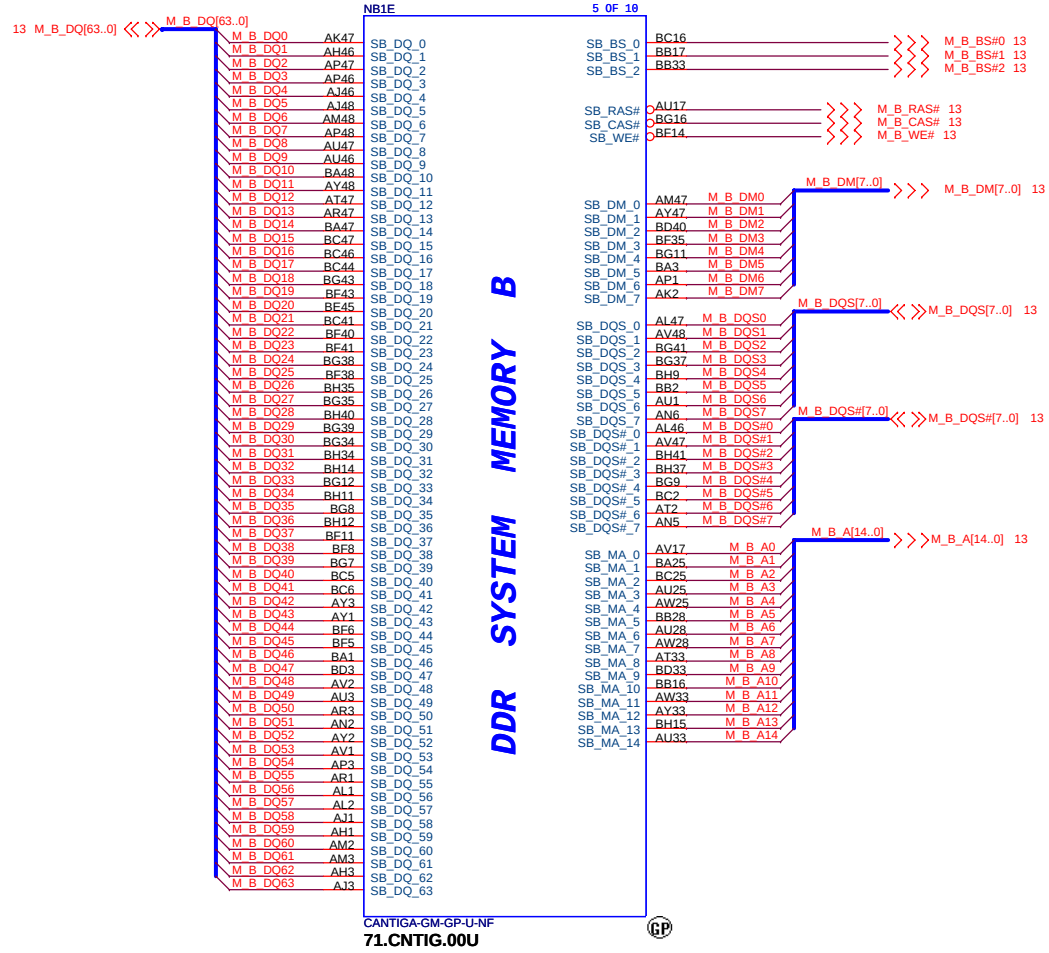

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Title: Cantiga (3 of 6)

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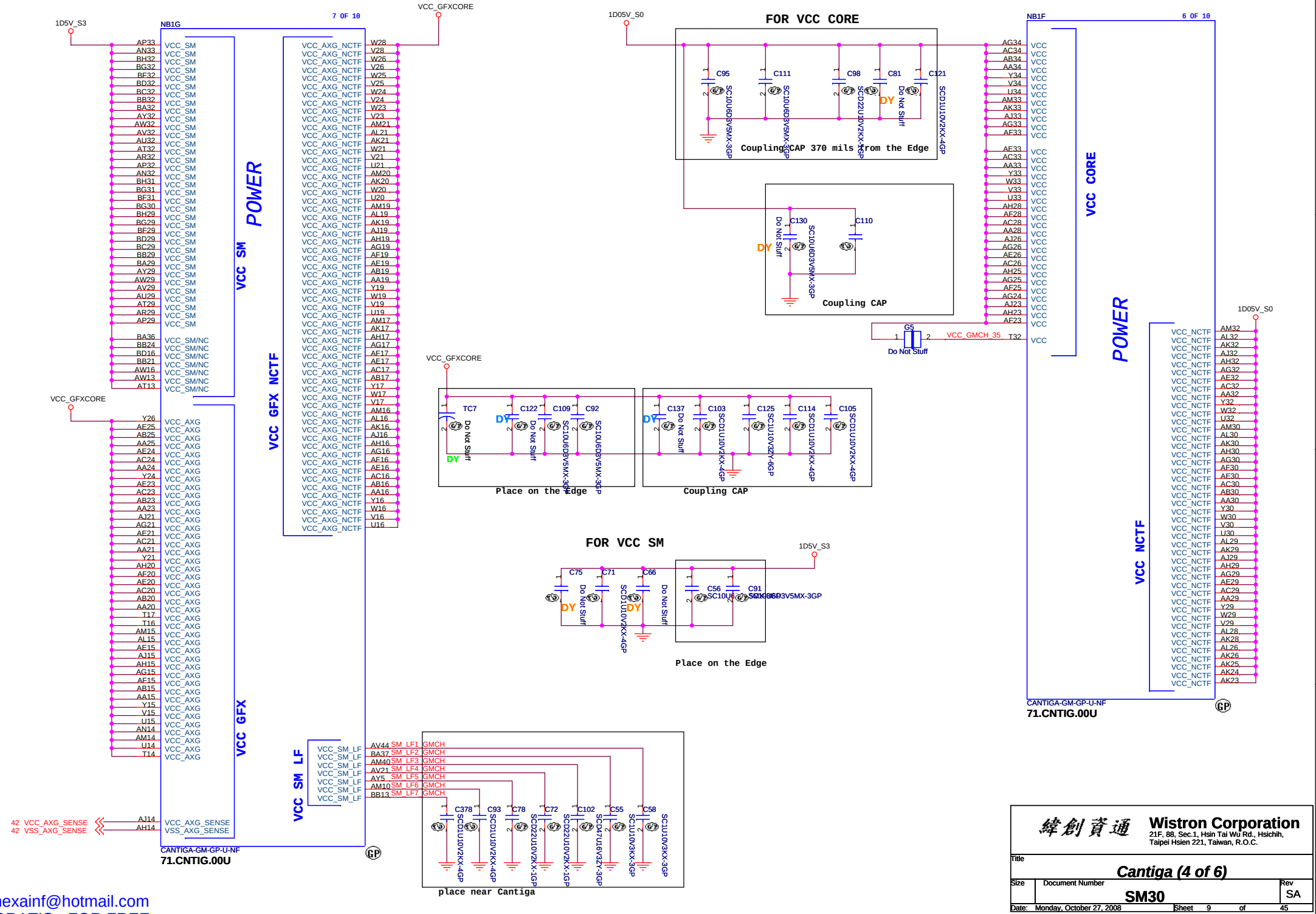

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Title	*Cantiga (4 of 6)*
Size	Document Number: **SM30** Rev: SA
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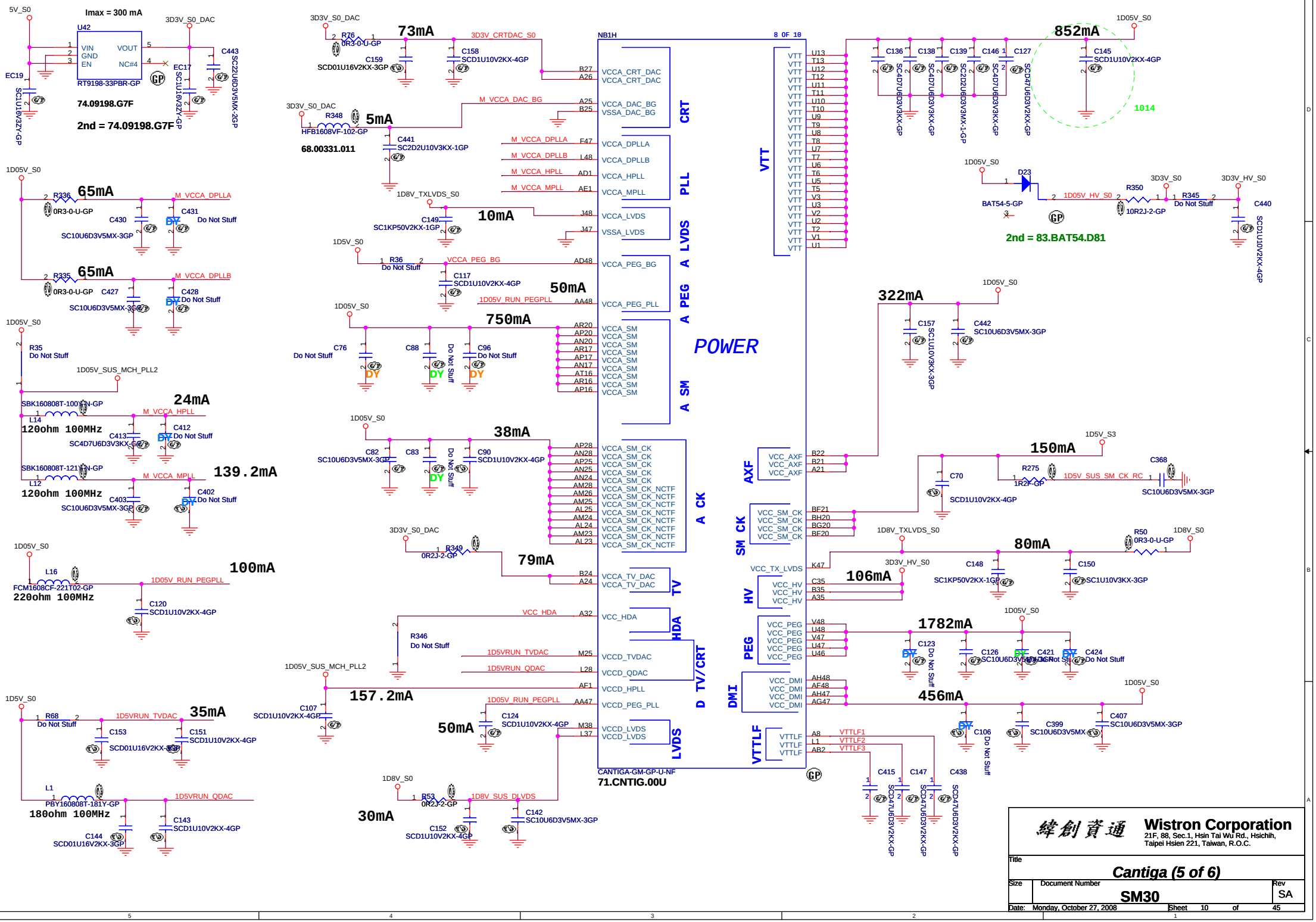

Title	Cantiga (5 of 6)
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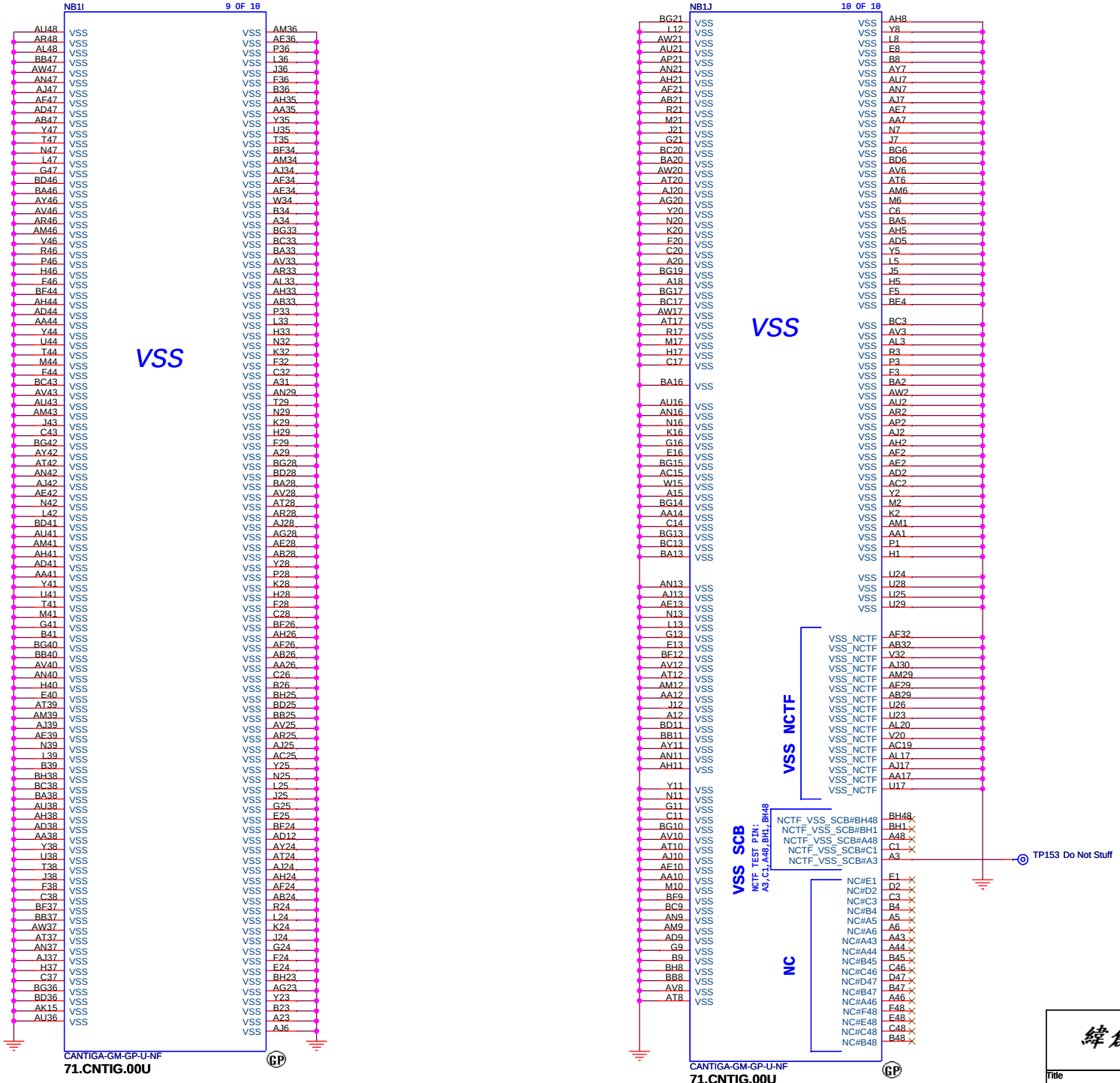

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Title: ***Cantiga (6 of 6)***

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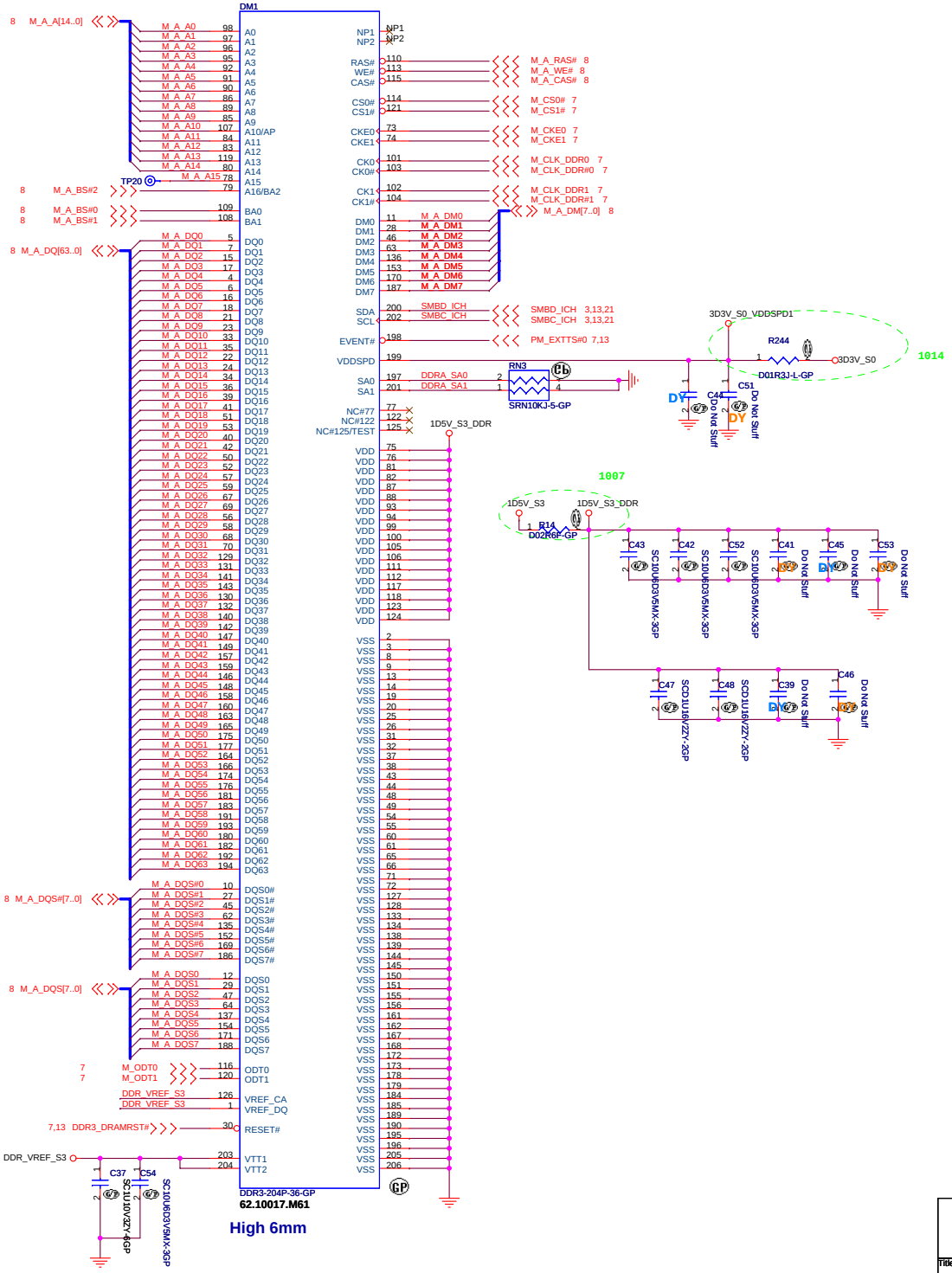
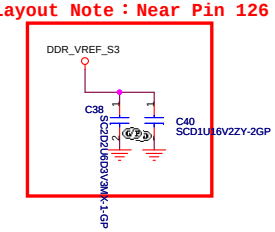
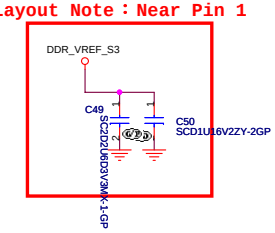
DDR3 SOCKET_1



Layout Note：Near Pin 126



Layout Note：Near Pin 1



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Title	DDR3 Socket		
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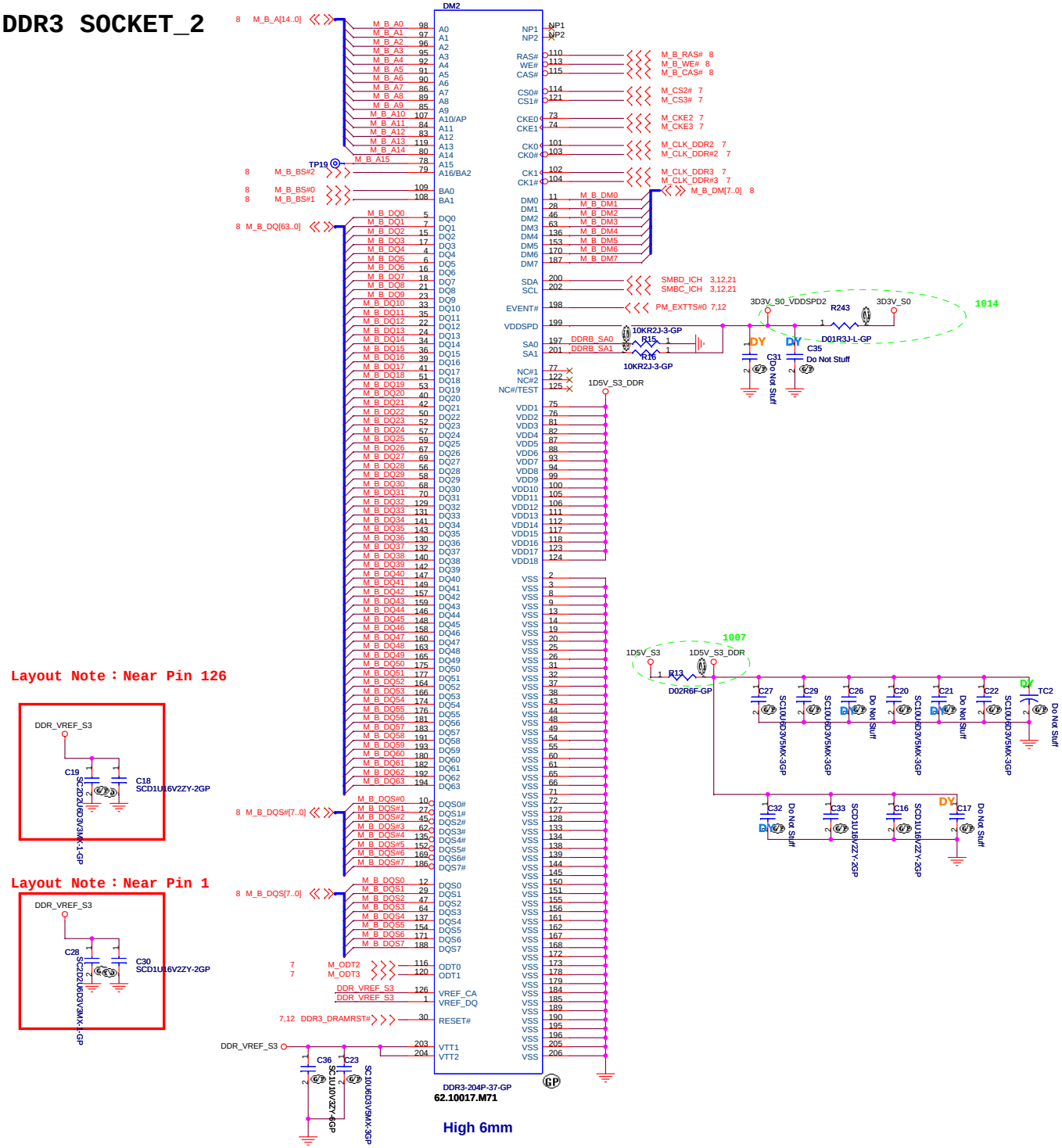
DDR3 SOCKET_2



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Title	DDR3 Termination Resistor	
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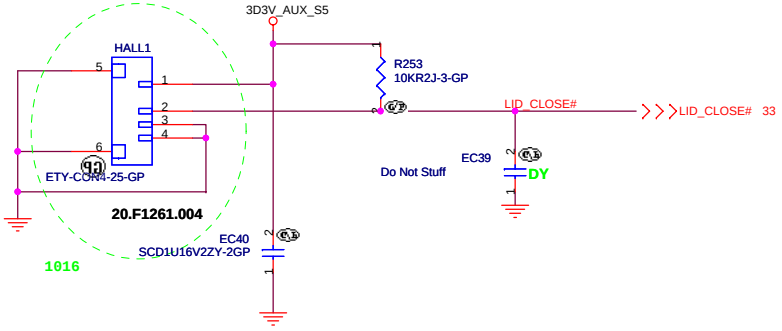
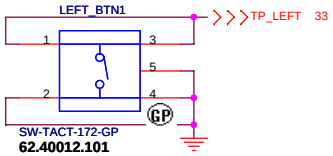
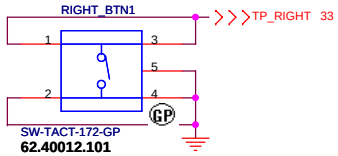
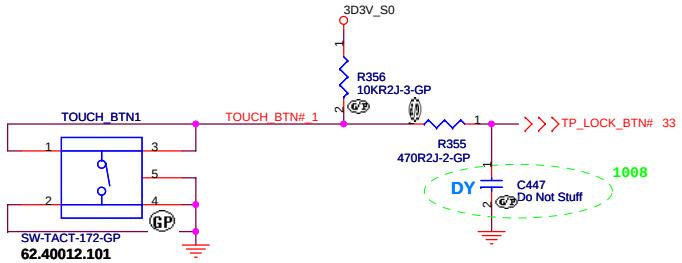
Cover Up Switch

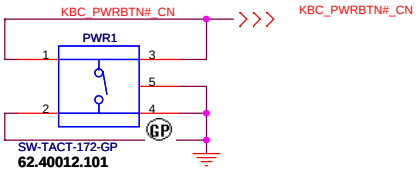


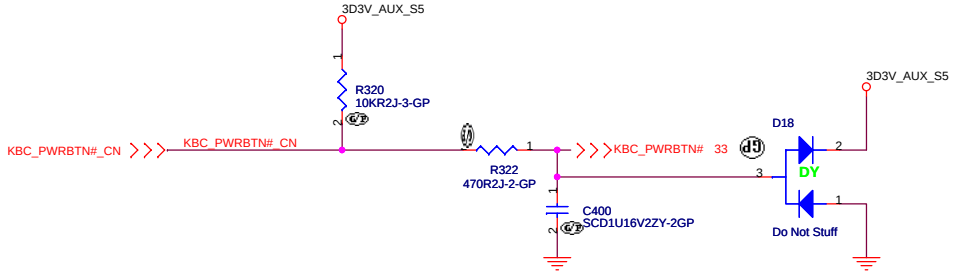
74.00268.A7B
74.00268.C7B











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Title: SWITCH / Button

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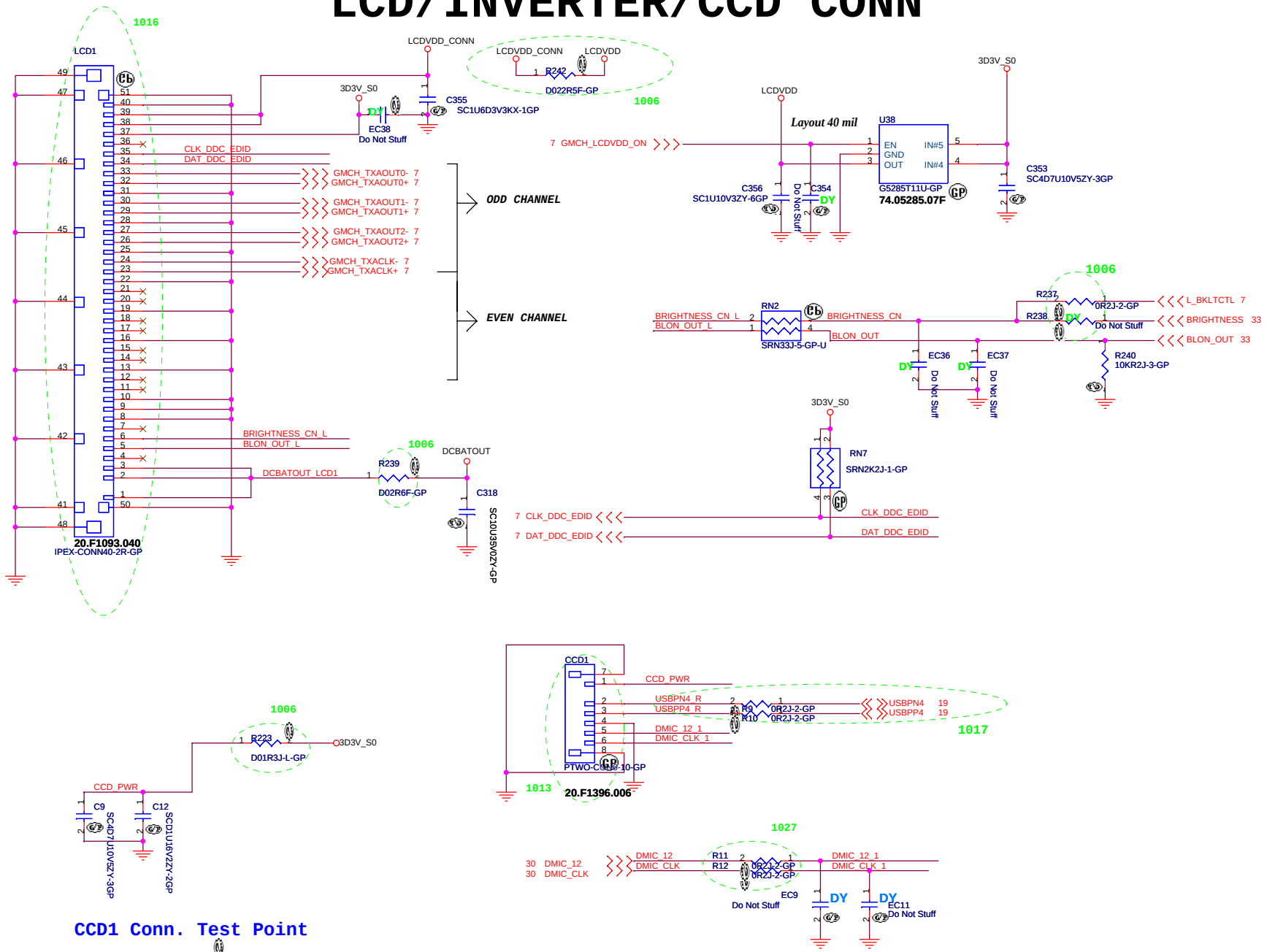
LCD/INVERTER/CCD CONN



UMA 2nd

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LCD CONN***	
Size	Document Number **SM30**	Rev SA
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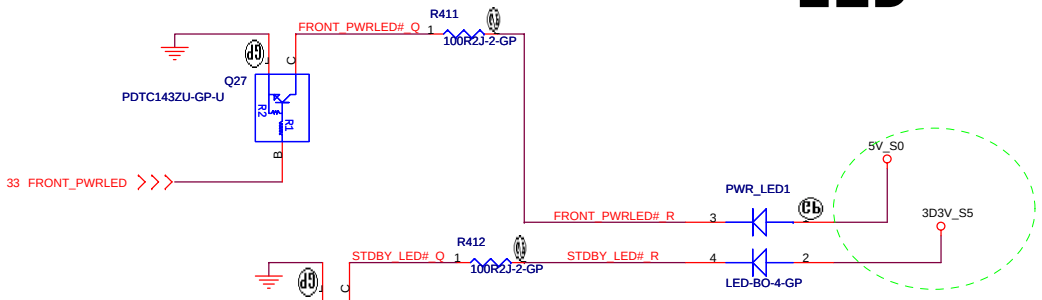
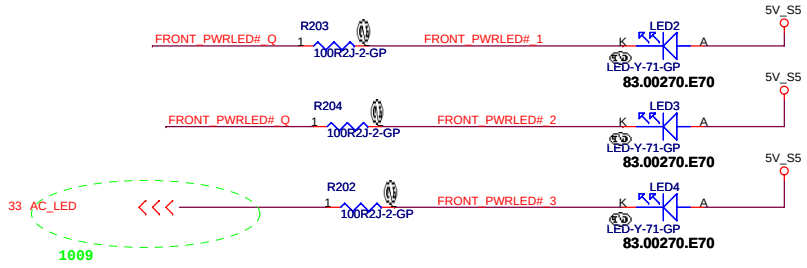
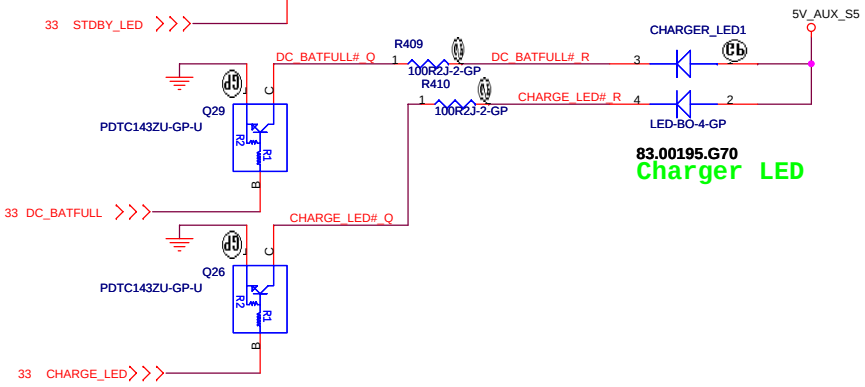
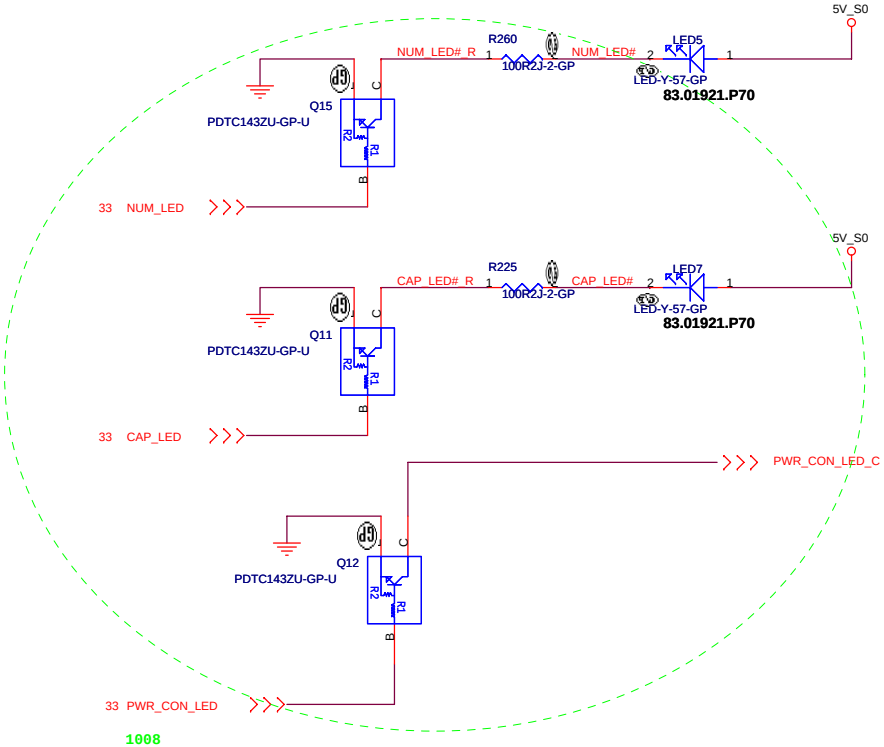
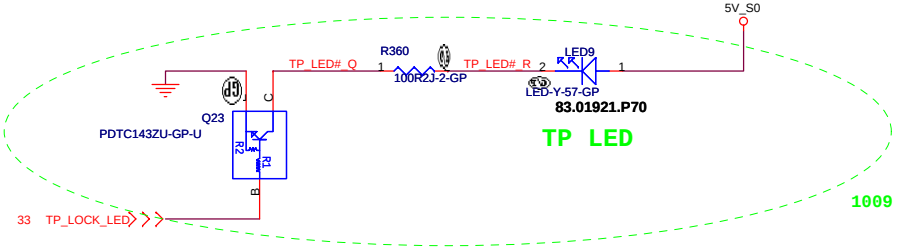
LED

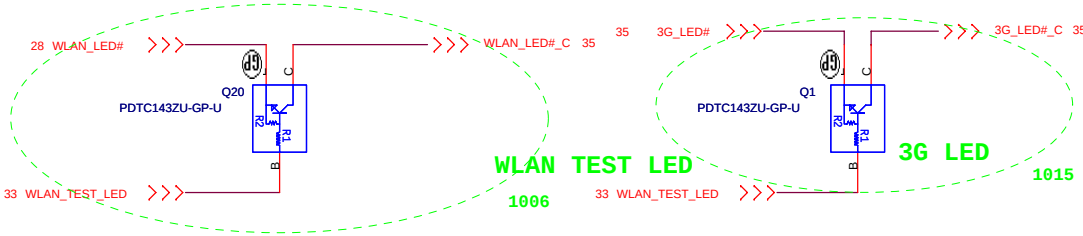












UMA 2nd

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LED***
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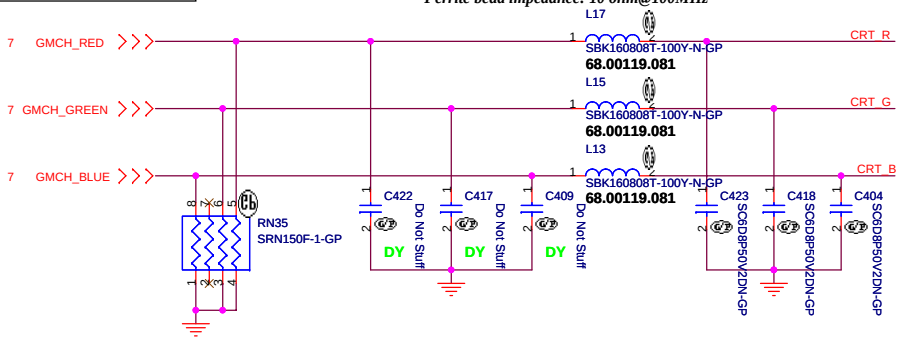
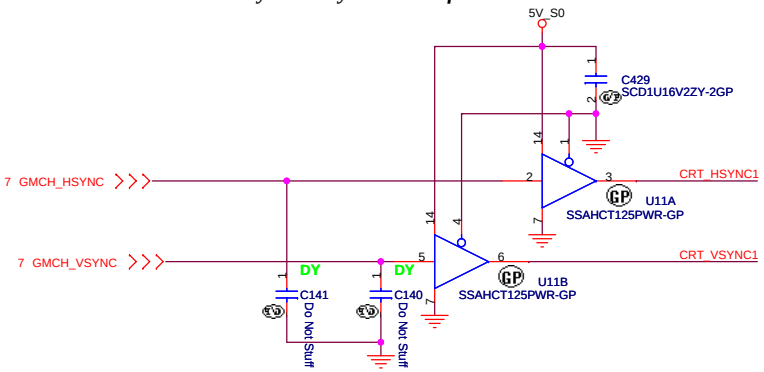
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

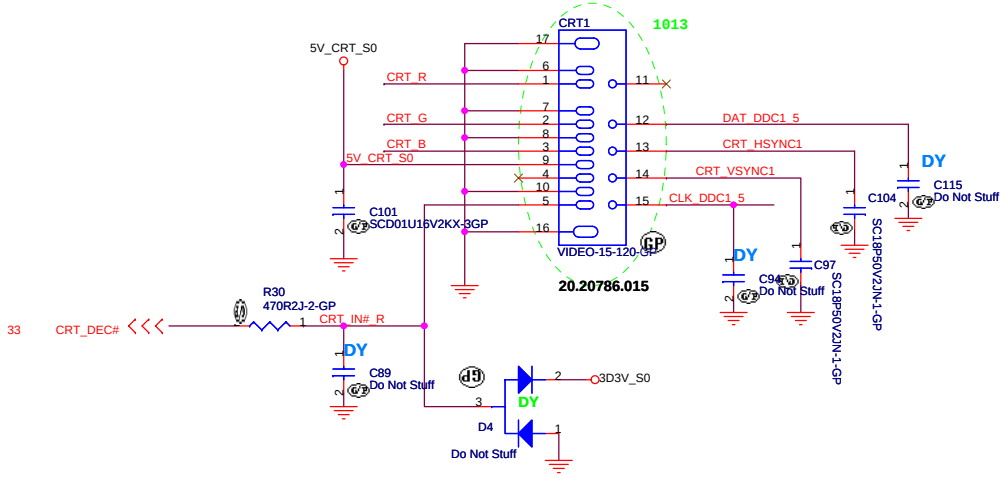


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

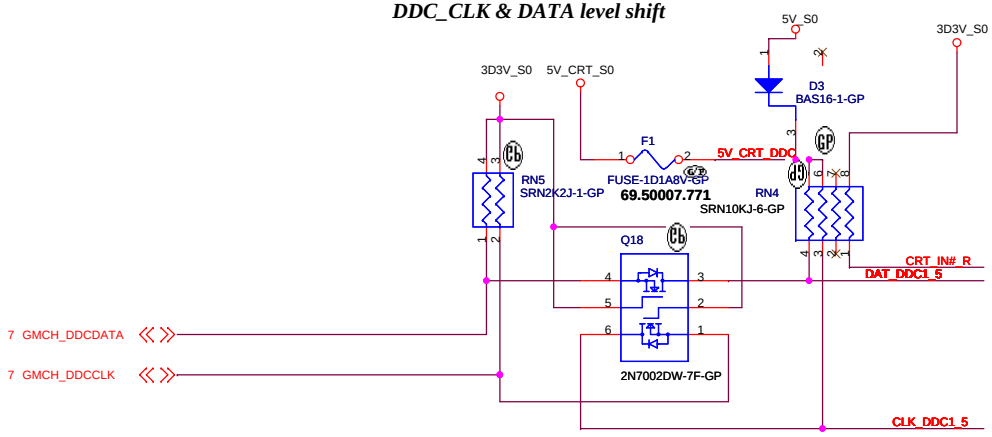
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



UMA 2nd

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT CONN		
Size	Document Number	Rev
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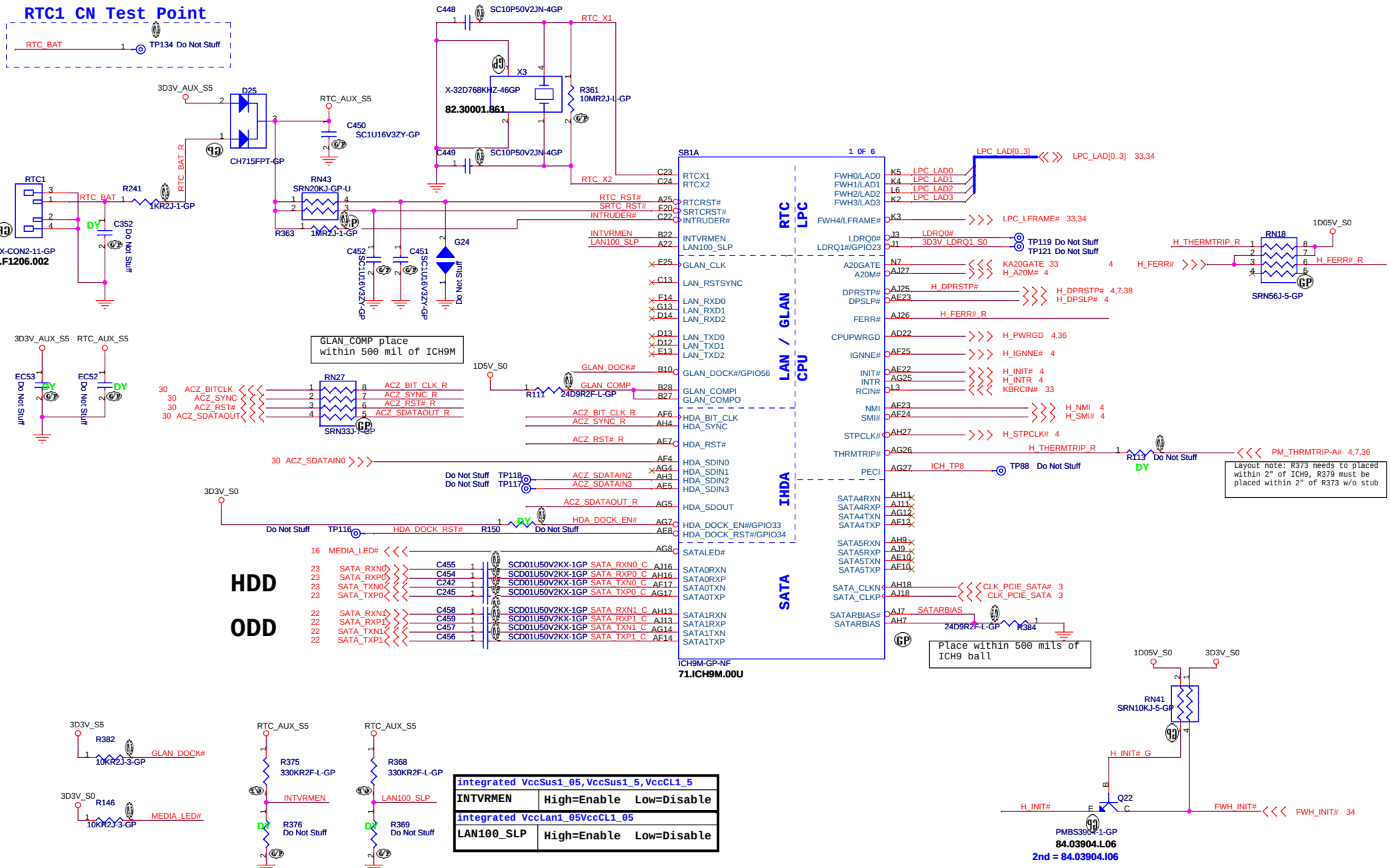
RTC1 CN Test Point
RTC_BAT
TP134 Do Not Stuff
3D3V_AUX_S5
D25
CH715FPT-GP
RTC_AUX_S5
C450
SC1U16V3ZY-GP
RTC_BAT_R
RTC1
MLX-CON2-11-GP
20.F1206.002
R241
1KR2J-1-GP
C352
DY
Do Not Stuff
RN43
SRN20KJ-GP-U
R363
1MR2J-1-GP
C452
C451
G24
C448
SC10P50V2JN-4GP
X3
X-32D768KHZ-46GP
82.30001.861
R361
10MR2J-L-GP
C449
RTC_X1
RTC_X2
RTC_RST#
SRTC_RST#
INTRUDER#
INTVRMEN
LAN100_SLP
SB1A
1 0F 6
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
RTC
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
LAN / GLAN
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
IHDA
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
LPC
CPU
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH9M-GP-NF
71.ICH9M.00U
LPC_LAD[0..3]
LPC_LFRAME#
TP119 Do Not Stuff
TP121 Do Not Stuff
KA20GATE
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#_R
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
KBRCIN#
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP_R
ICH_TP8
TP88 Do Not Stuff
R113 Do Not Stuff
PM_THRMTRIP-A#
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATARBIAS
24D9R2F-L-GP
R384
Place within 500 mils of ICH9 ball
RN18
SRN56J-5-GP
1D05V_S0
GLAN_COMP place within 500 mil of ICH9M
EC53
EC52
RN27
SRN33J-7-GP
ACZ_BITCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDATAOUT
ACZ_BIT_CLK_R
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDATAOUT_R
R111
24D9R2F-L-GP
GLAN_DOCK#
GLAN_COMP
ACZ_SDATAIN0
ACZ_SDATAIN2
ACZ_SDATAIN3
TP118
TP117
R150
HDA_DOCK_RST#
HDA_DOCK_EN#
TP116
MEDIA_LED#
HDD
ODD
SCD01U50V2KX-1GP
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
R382
10KR2J-3-GP
R146
R375
330KR2F-L-GP
R376
R368
330KR2F-L-GP
R369
INTVRMEN
LAN100_SLP
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
RN41
SRN10KJ-5-GP
H_INIT#_G
Q22
PMBS3904-1-GP
84.03904.L06
2nd = 84.03904.I06
FWH_INIT#
UMA 2nd
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
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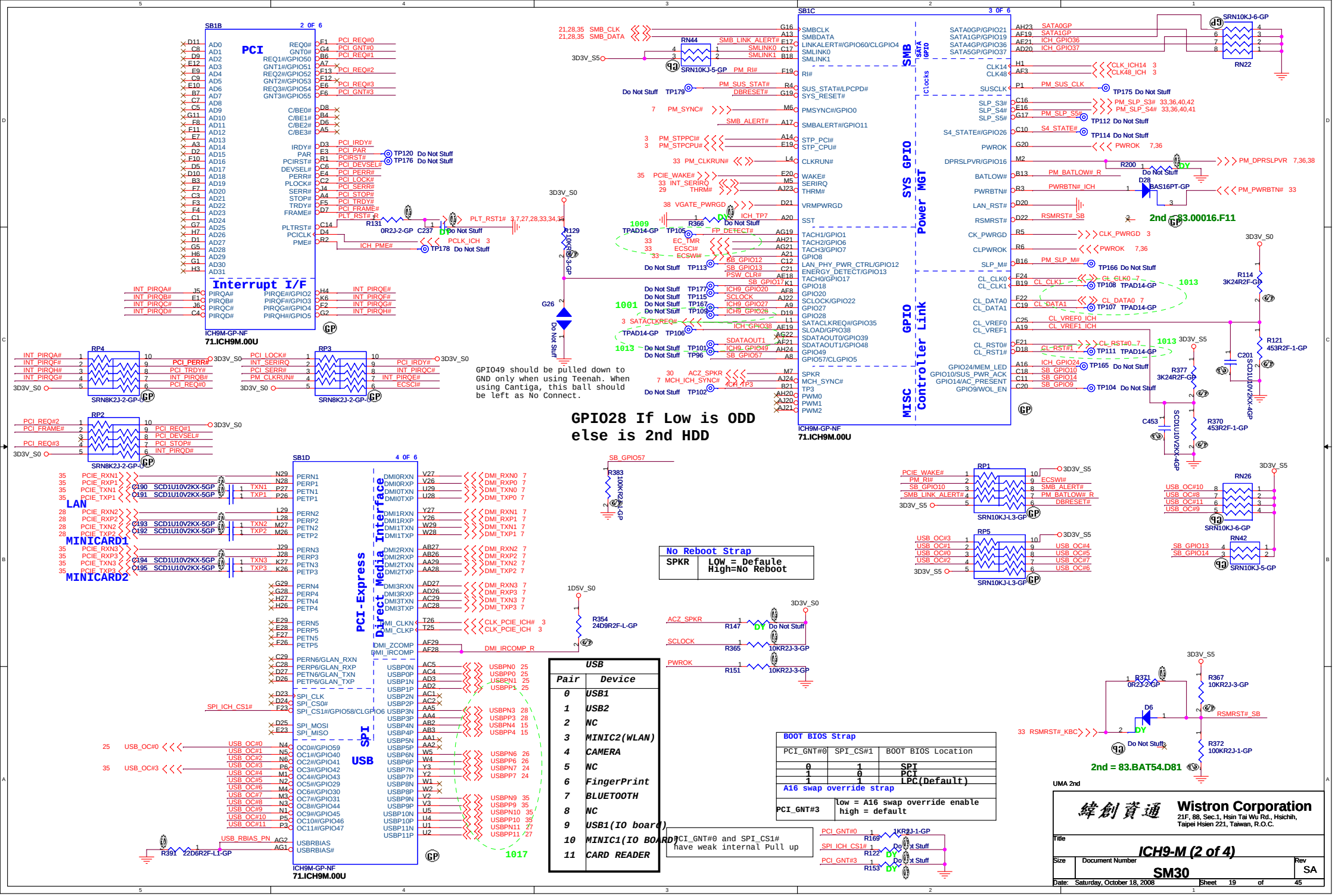

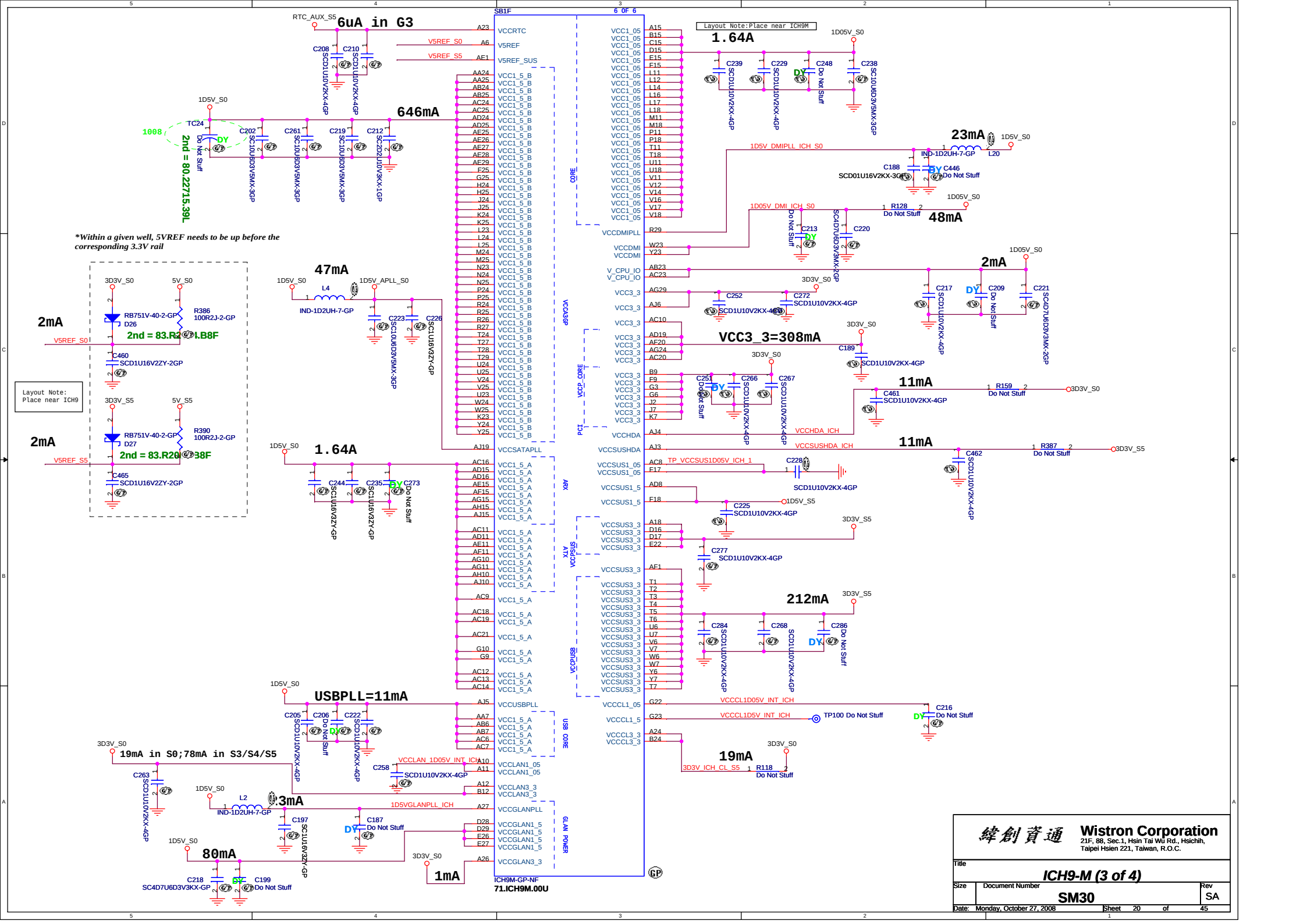
6uA in G3
646mA
1.64A
23mA
48mA
2mA
47mA
VCC3_3=308mA
11mA
212mA
19mA in S0;78mA in S3/S4/S5
USBPLL=11mA
3mA
80mA
1mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
SM30
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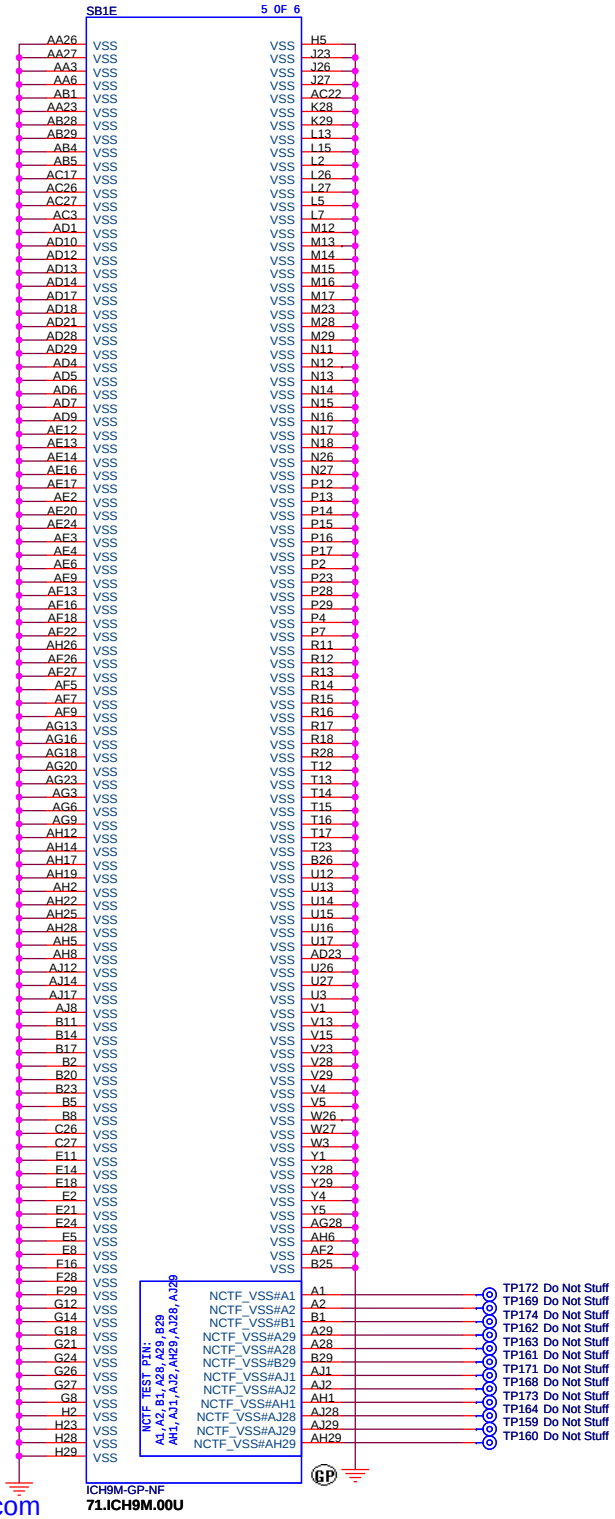
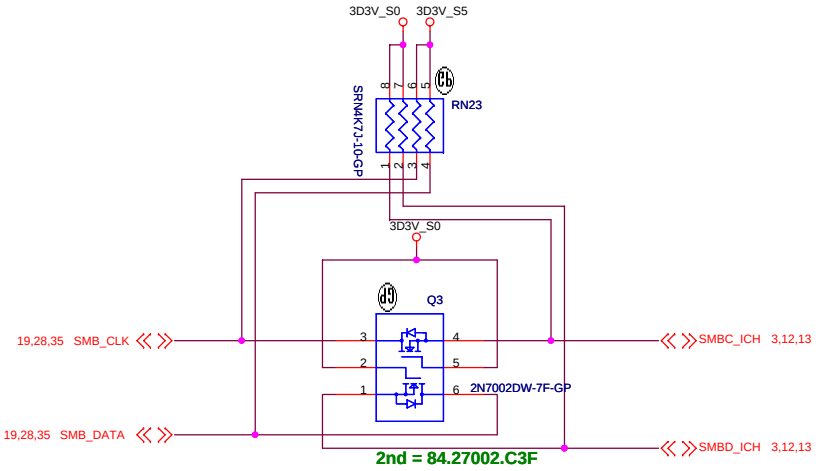
45





緯創資通 **Wistron Corporation**
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Title: *ICH9-M (4 of 4)*

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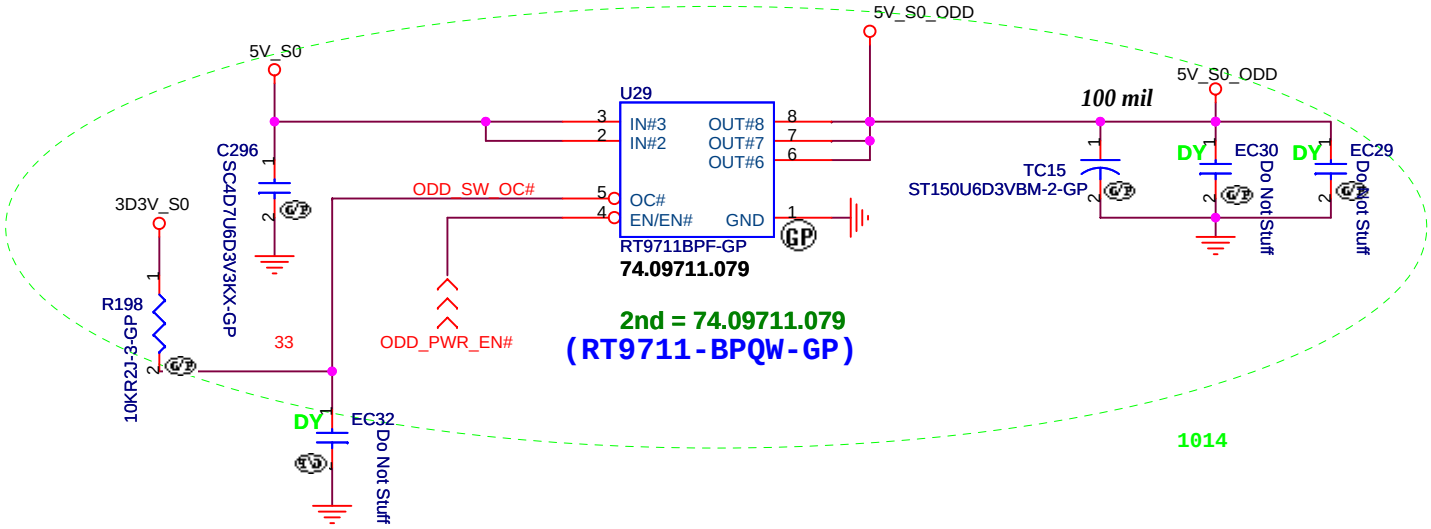
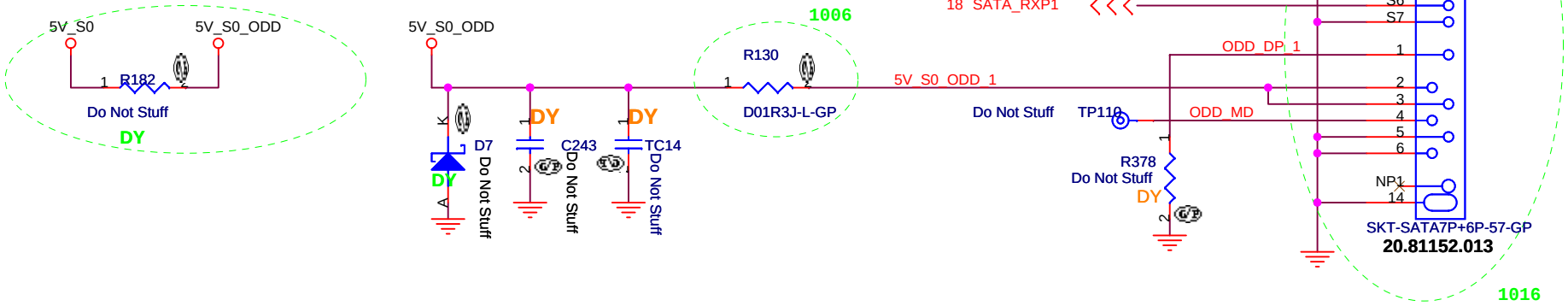
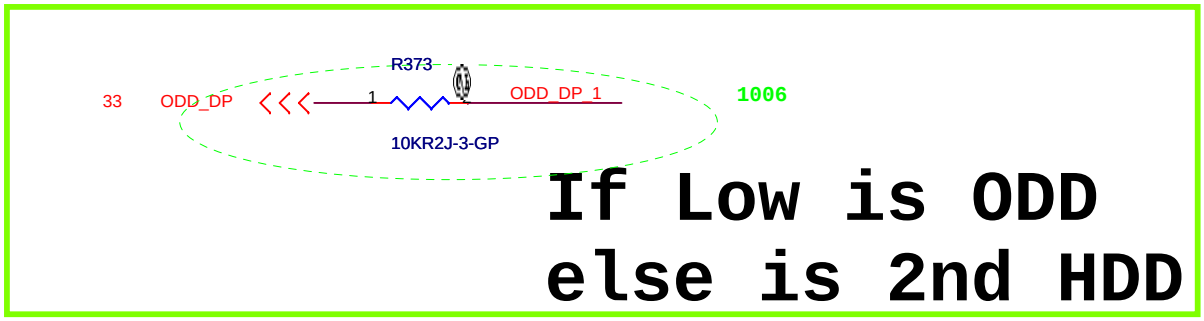
ODD Connector







UMA 2nd

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Title: **ODD**		
Size	Document Number: **SM30**	Rev: SA
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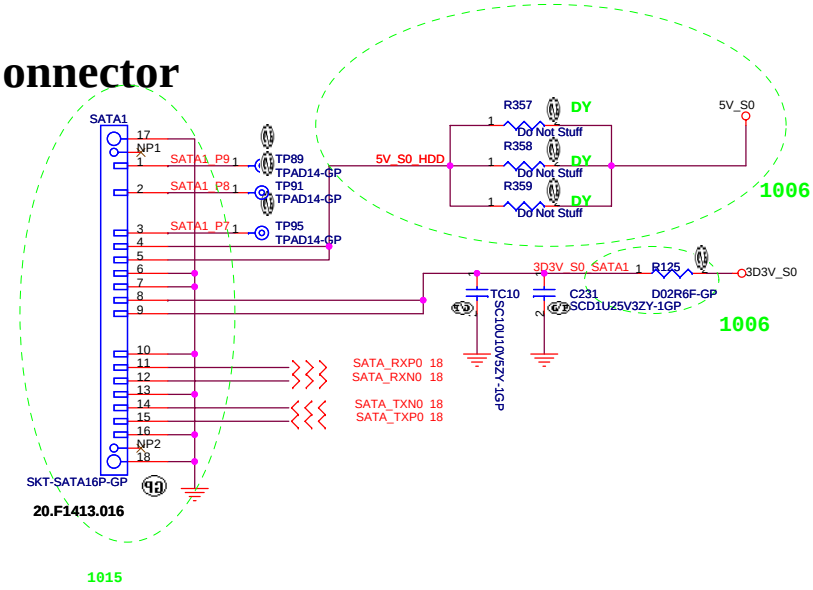
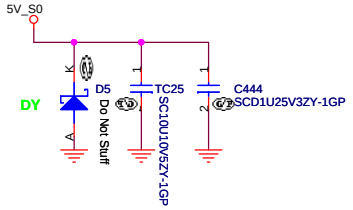
SATA Connector





UMA 2nd

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Title: ***HDD CONN***		
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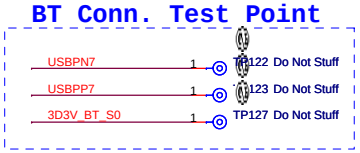
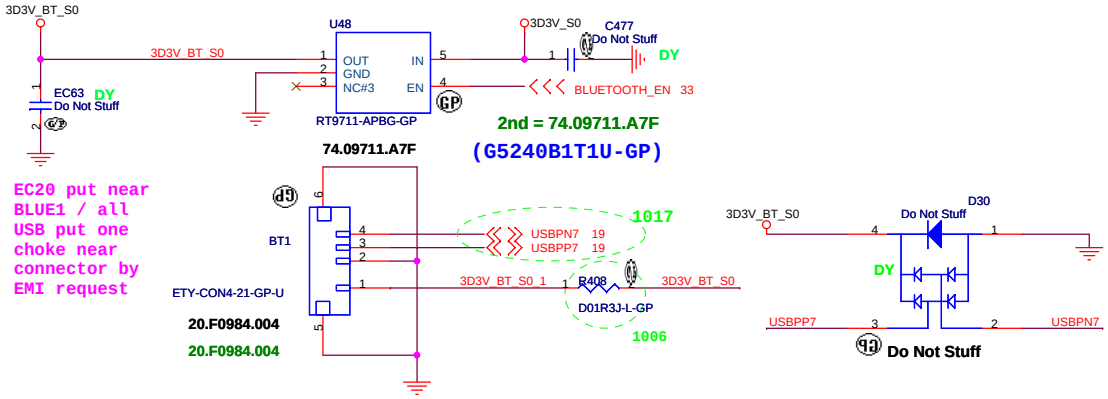
BLUETOOTH MODULE

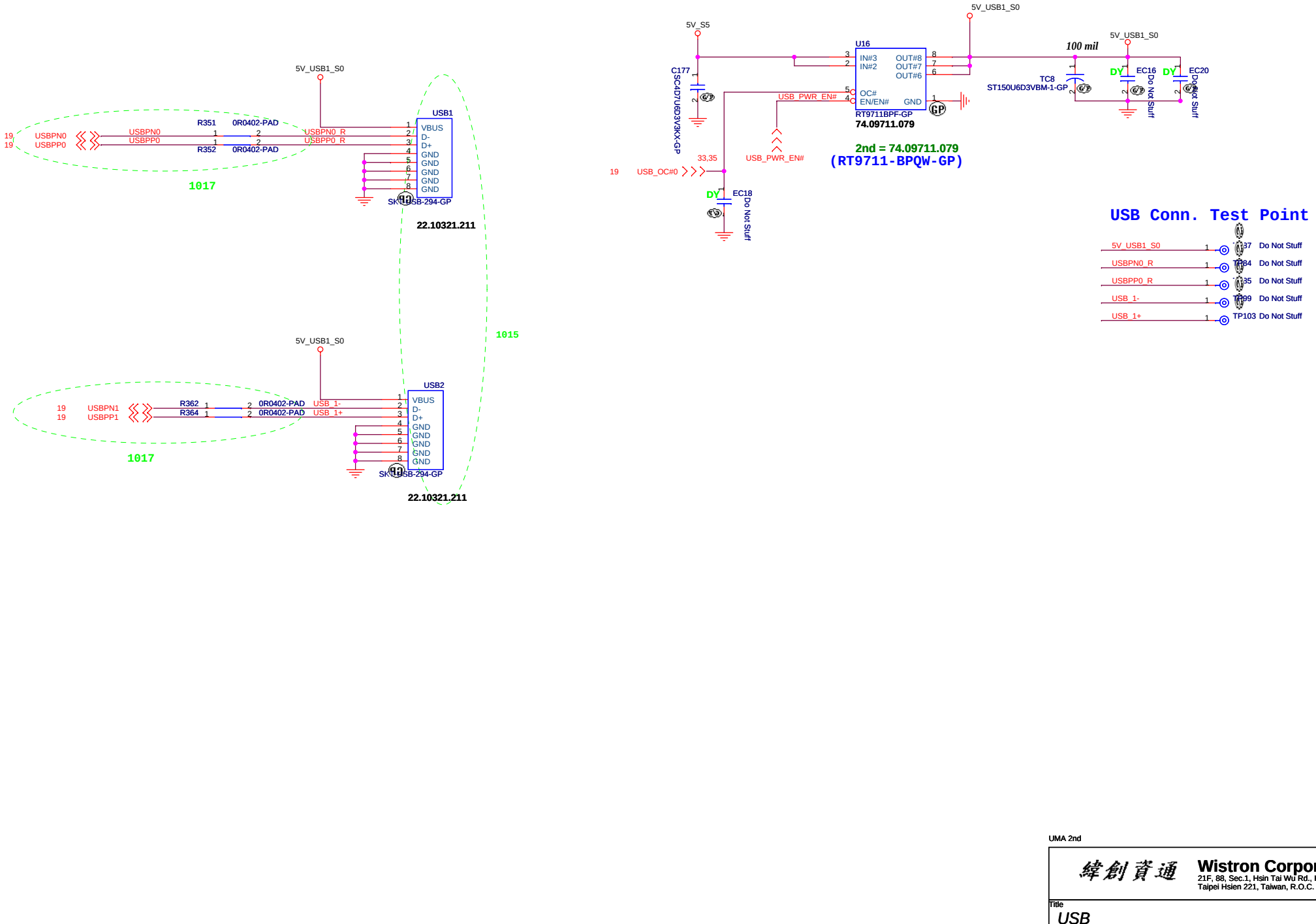




Need check conn.

UMA 2nd

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
Size	Document Number: SM30	Rev: SA
Date: Saturday, October 18, 2008	Sheet 24 of 45	



UMA 2nd

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Title: USB

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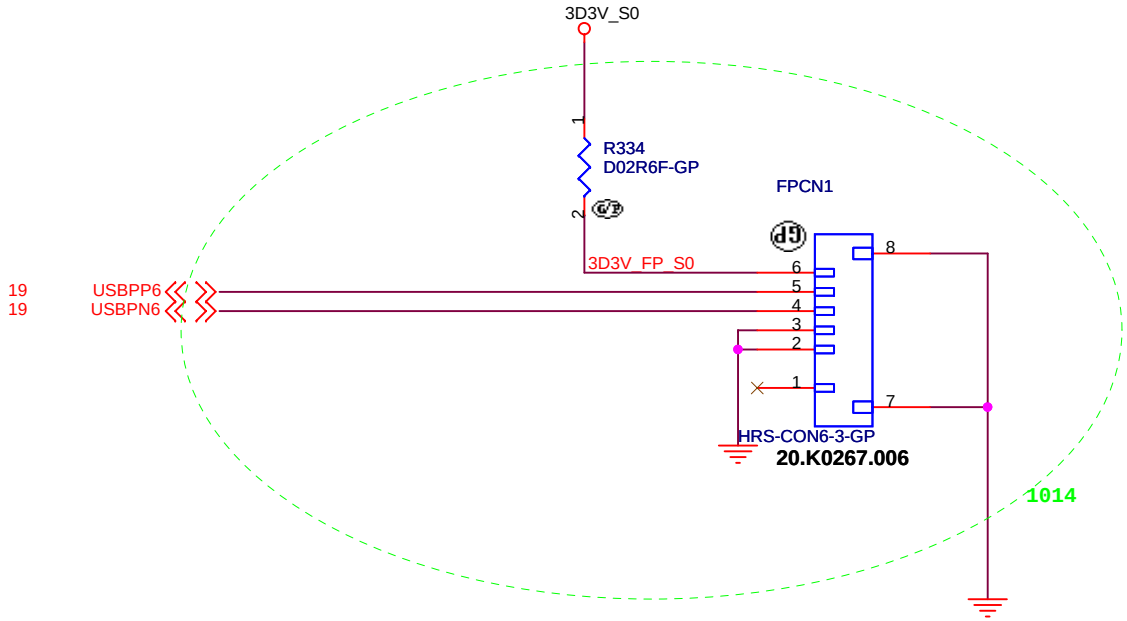
Finger printer

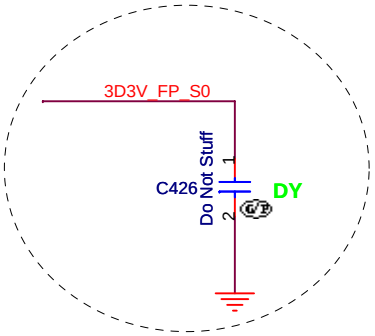
FP Conn. Test Point

3D3V_FP_S0 — 1 — TP148 Do Not Stuff

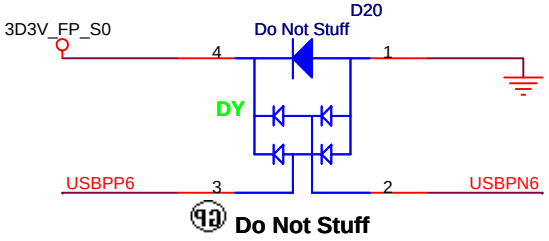
USBPP6 — 1 — TP146 Do Not Stuff

USBPN6 — 1 — TP145 Do Not Stuff





For EMI



Do Not Stuff

UMA 2nd

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Title		
Finger Printer		
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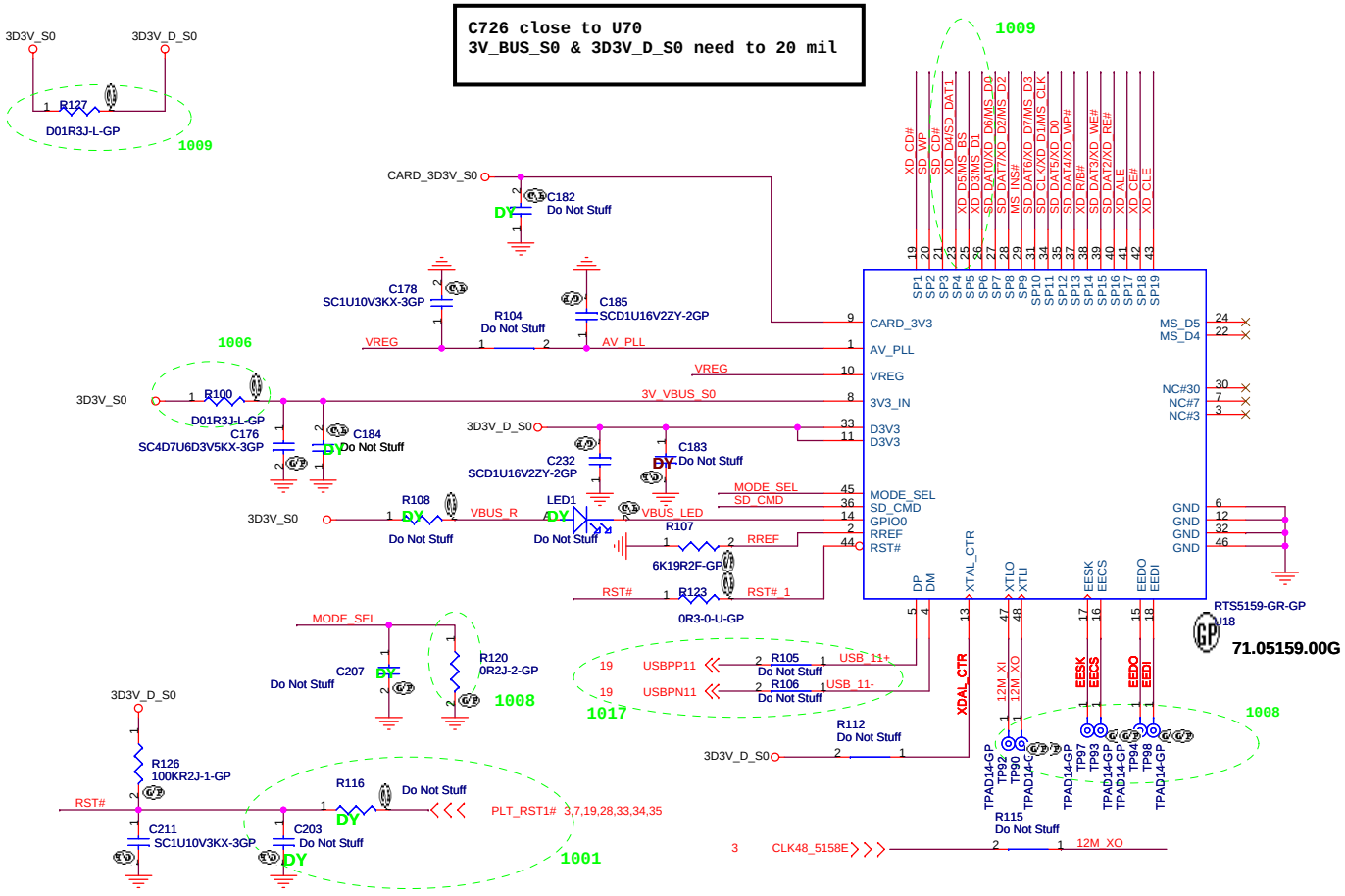
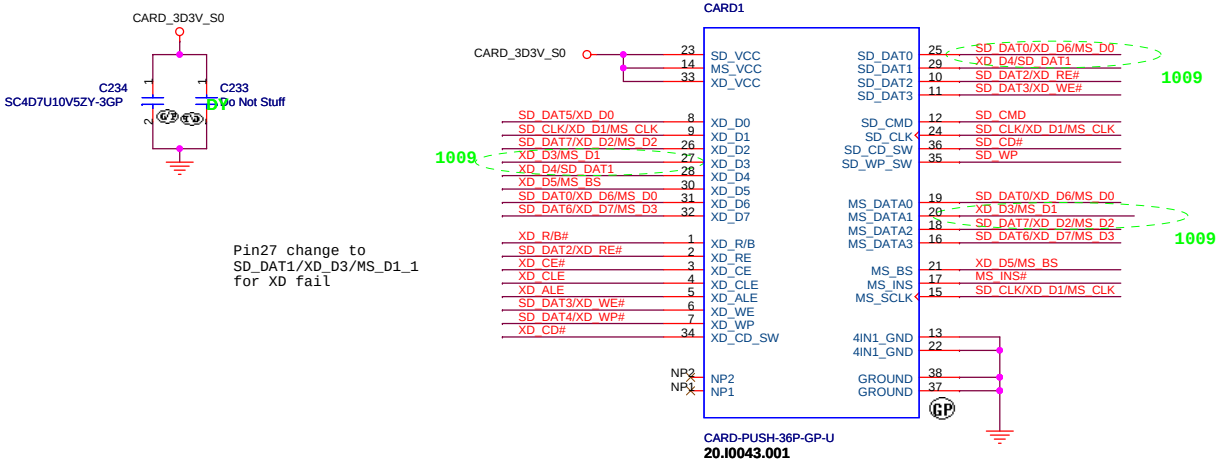
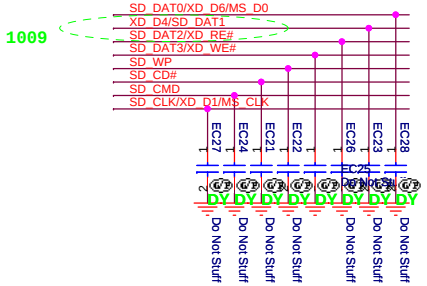
C726 close to U70
3V_BUS_S0 & 3D3V_D_S0 need to 20 mil



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)





UMA 2nd

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARDREADER- RTS5158E**

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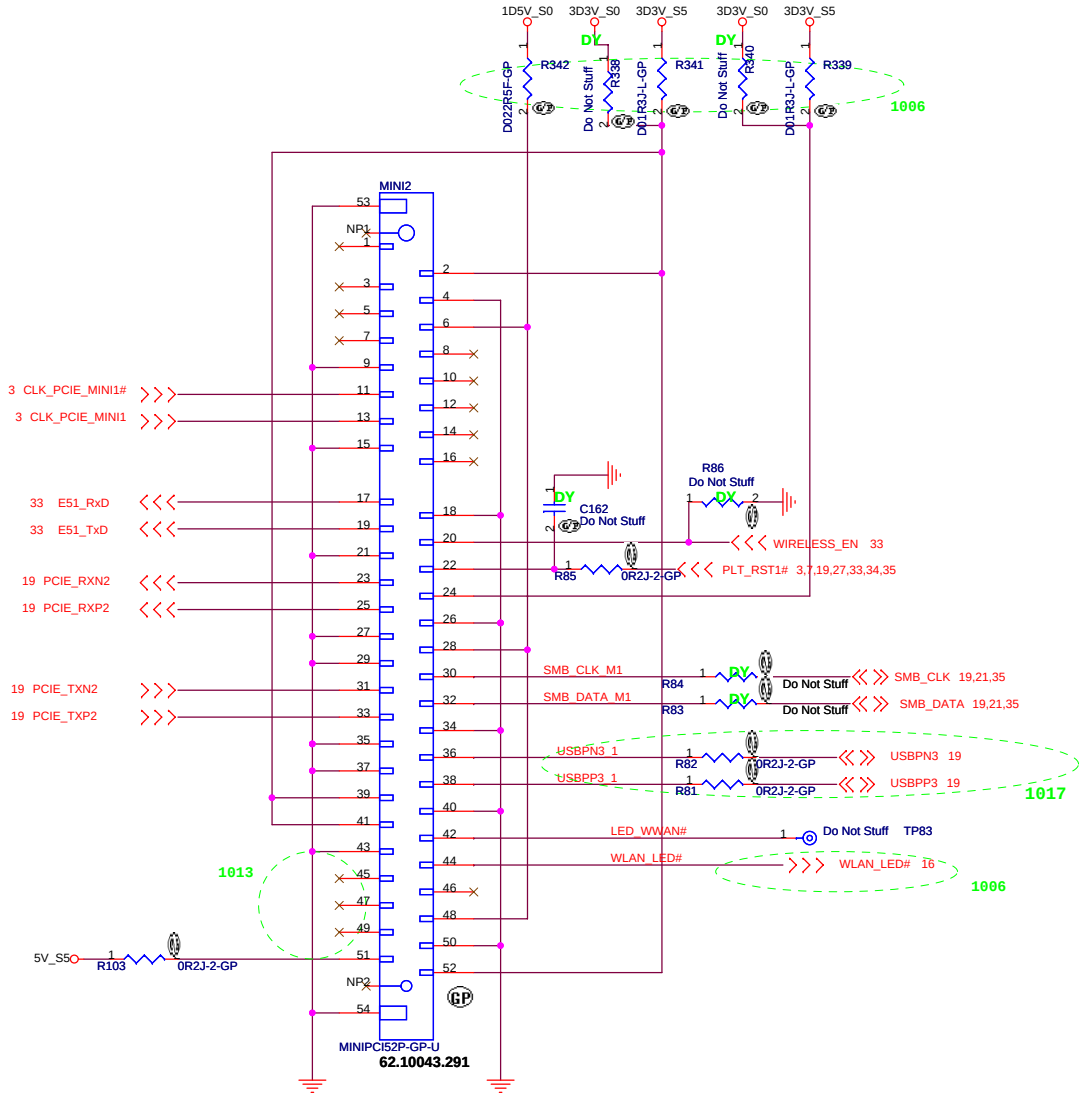
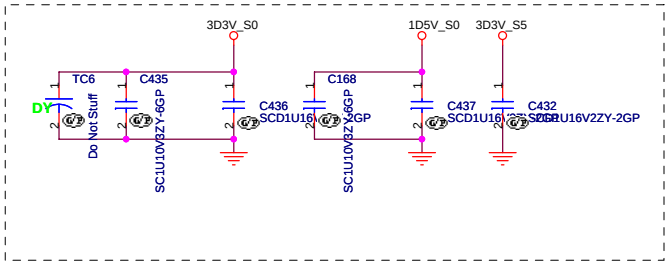
Mini Card Connector(WLAN)



Place near MINIC1



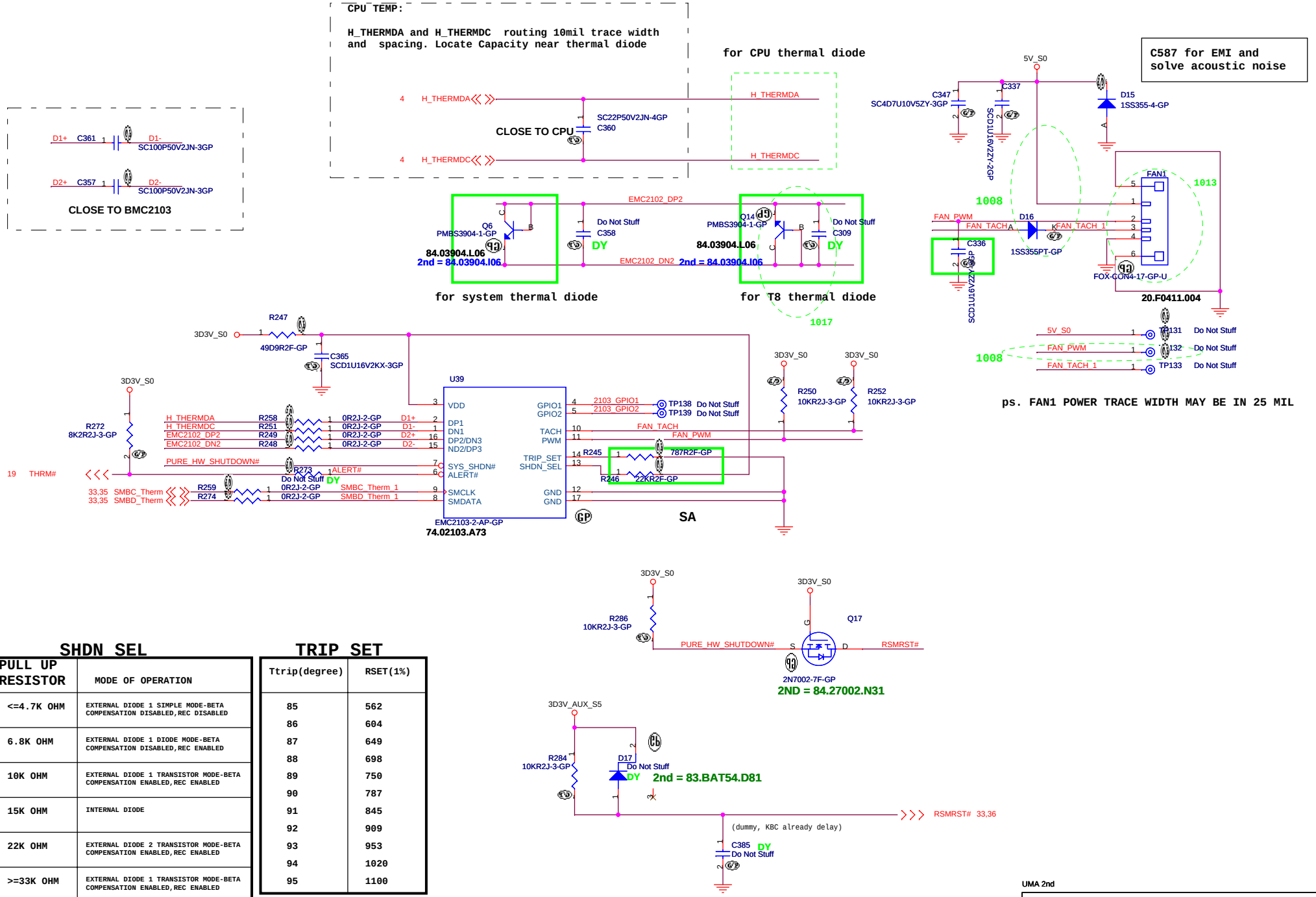
UMA 2nd

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD

Size	Document Number	Rev
A3	SM30	SA

Date: Saturday, October 18, 2008 Sheet 28 of 45



SHDN_SEL

PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED,REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED,REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED

TRIP_SET

Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

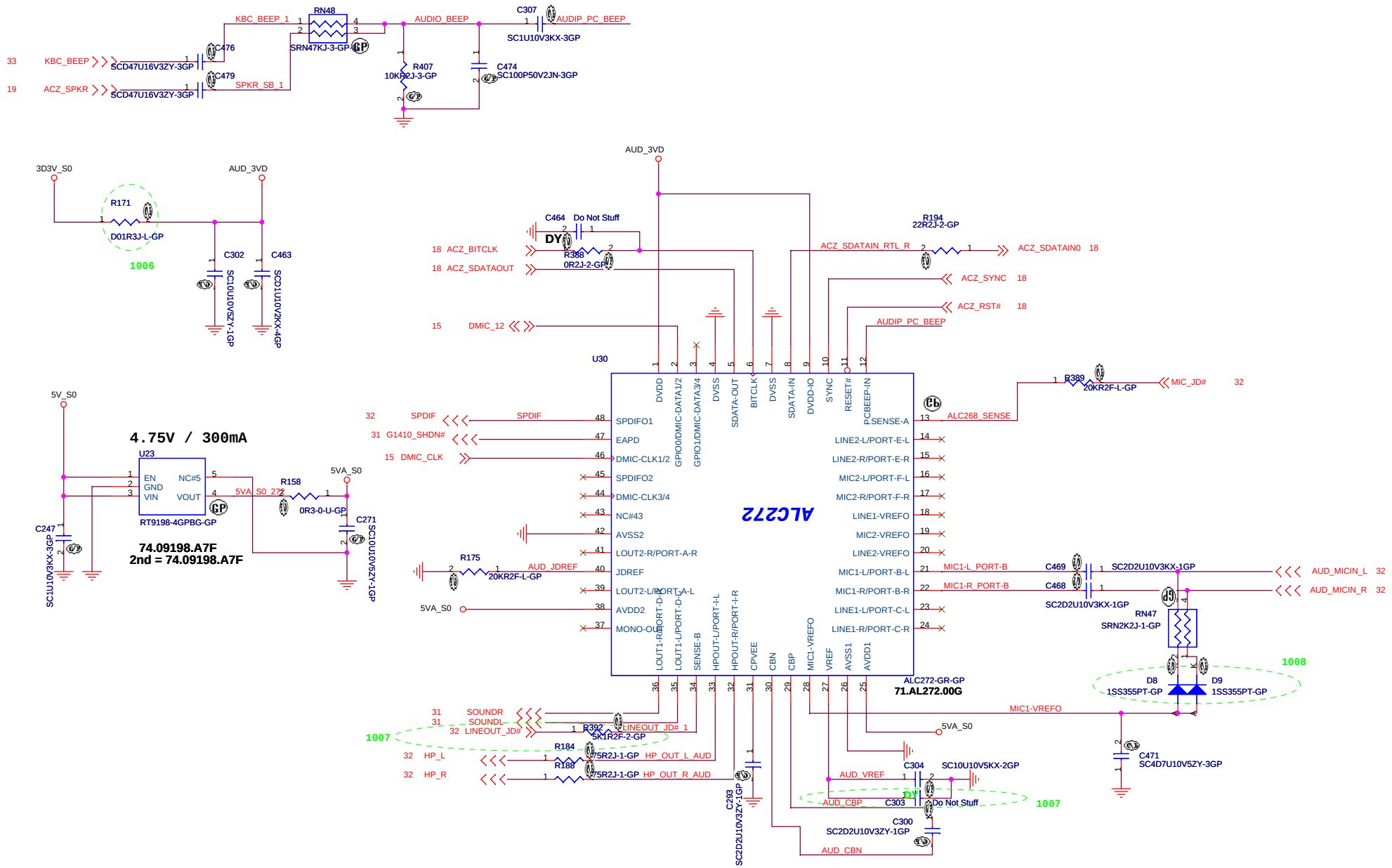
UMA 2nd

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size	Document Number	Rev
	SM30	SA

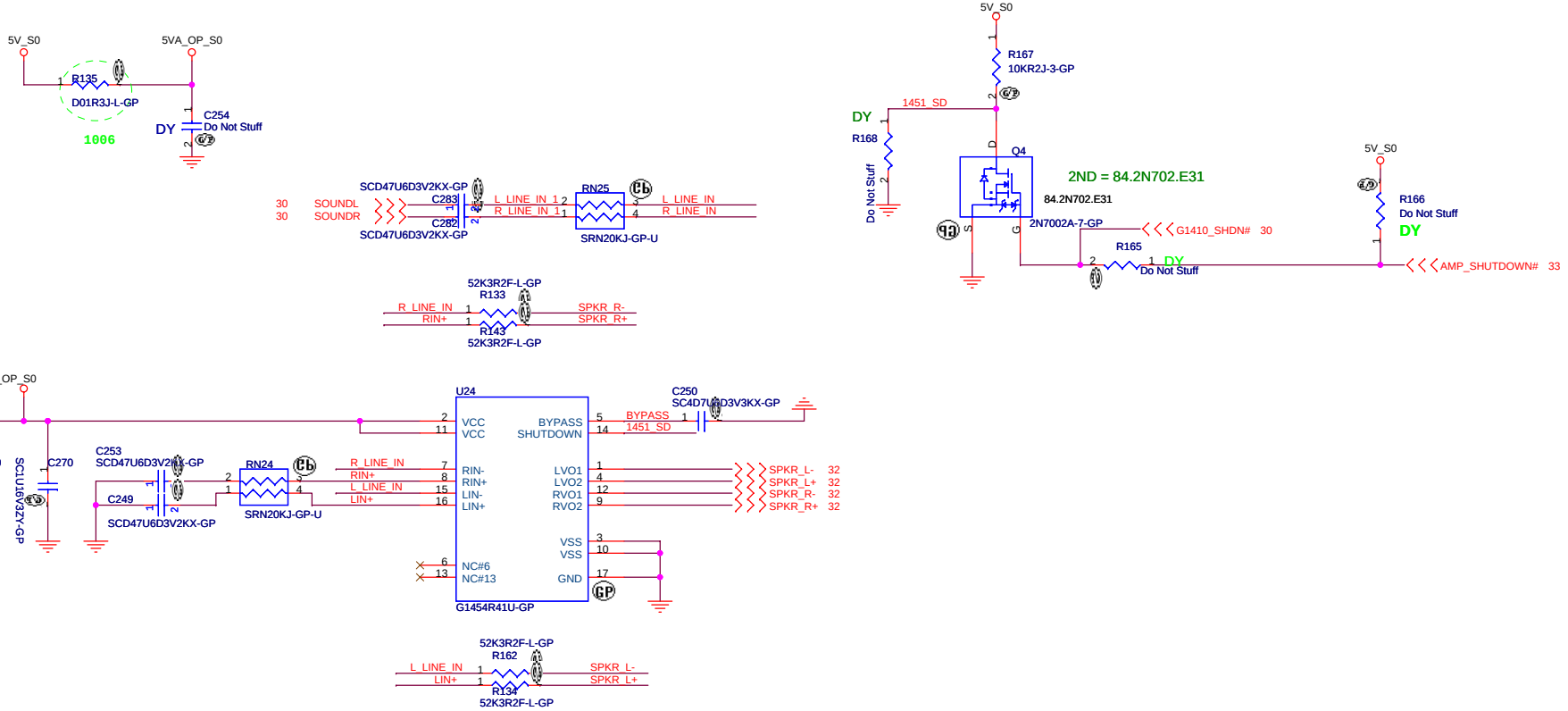
Date: Saturday, October 18, 2008 Sheet 29 of 45



UMA 2nd

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Azalia codec ALC268***		
Size: A3	Document Number: **SM30**	Rev: **SA**
Date: Saturday, October 18, 2008	Sheet 30 of 45	

AUDIO OP AMPLIFIER



UMA 2nd

緯創資通 **Wistron Corporation**
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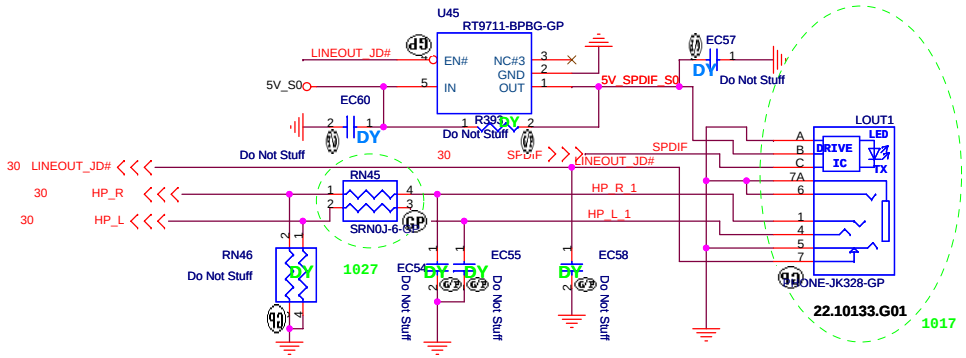
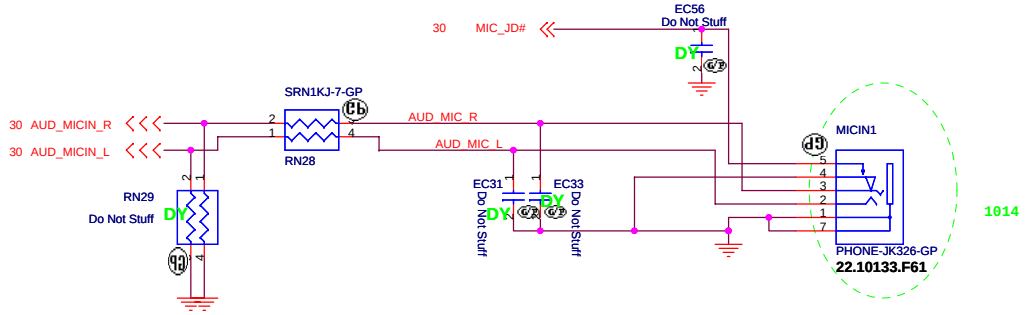
Taipei Hsien 221, Taiwan, R.O.C.

Title	*AUDIO AMP*	
Size	Document Number SM30	Rev SA
Date: Saturday, October 18, 2008	Sheet 31 of 45	

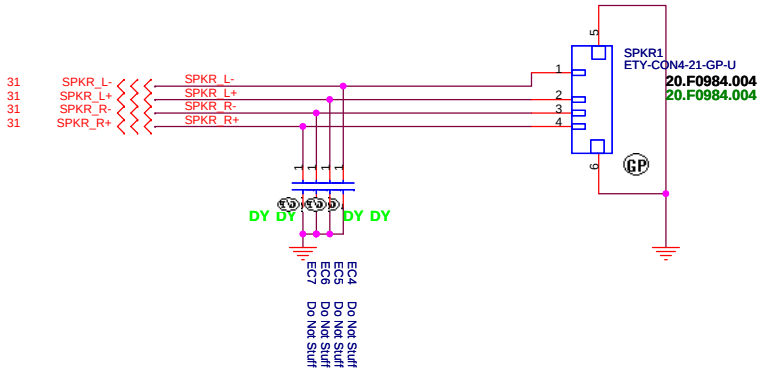
LINE OUT



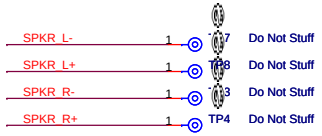
MIC IN



Internal Speaker



SPKR1 Conn. Test Point



UMA 2nd

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
AUDIO JACK		
Size	Document Number	Rev
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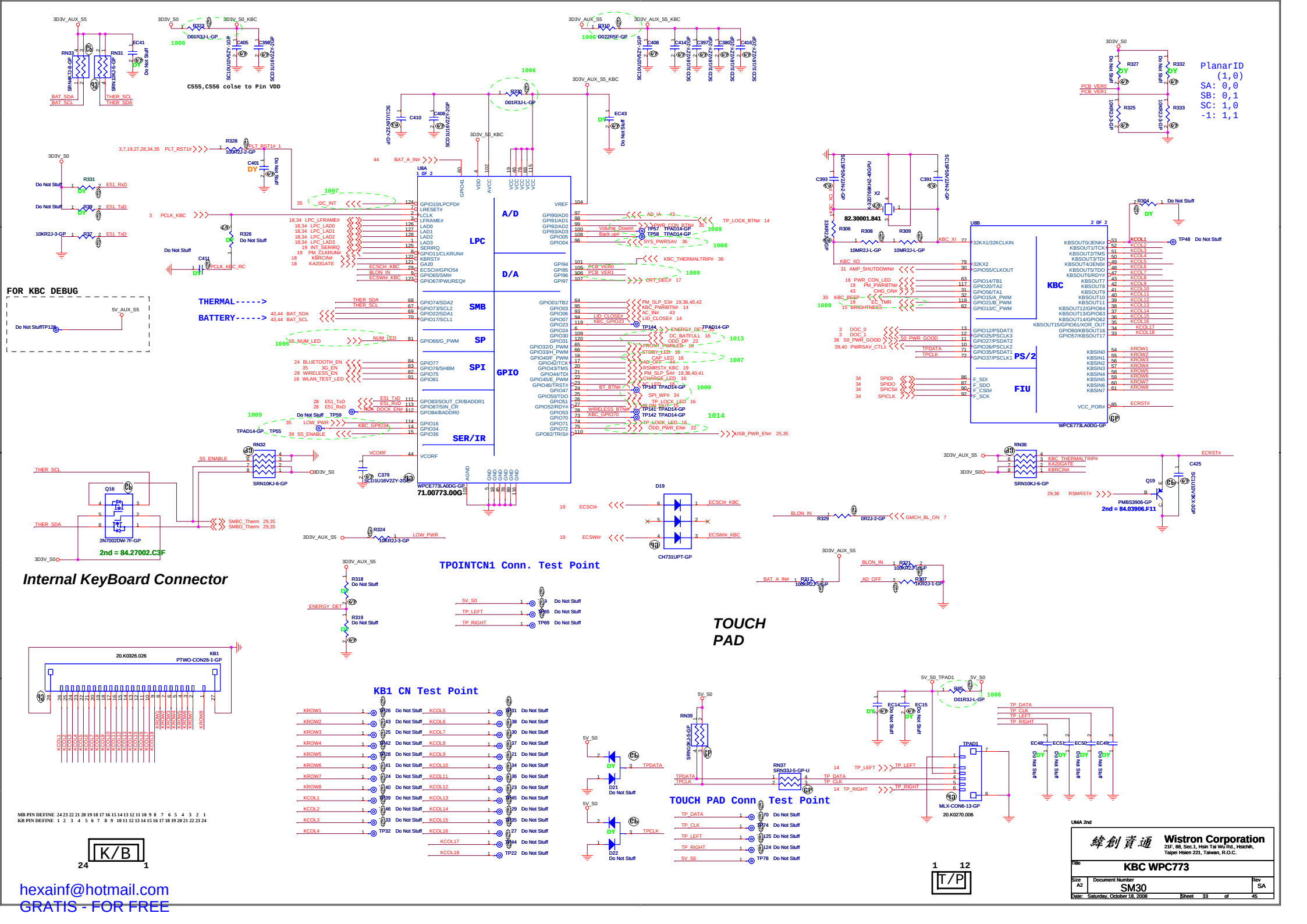
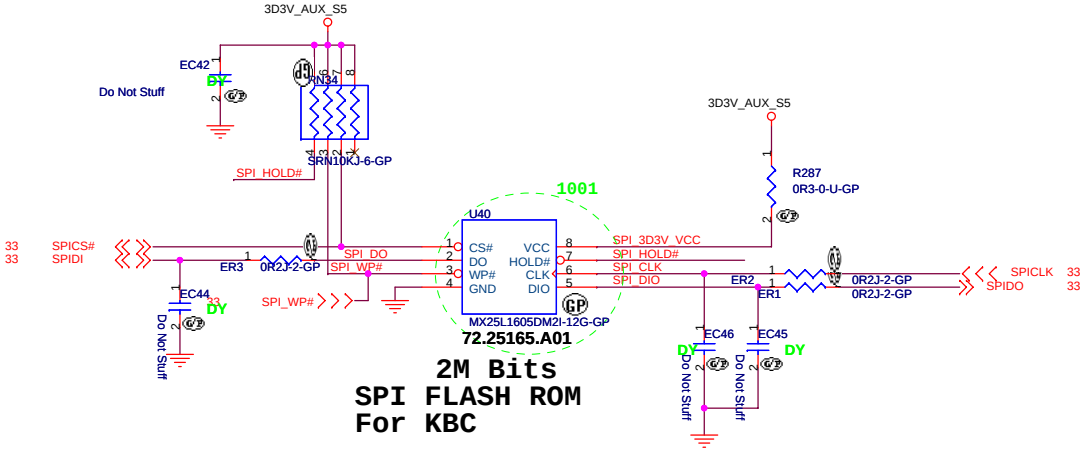
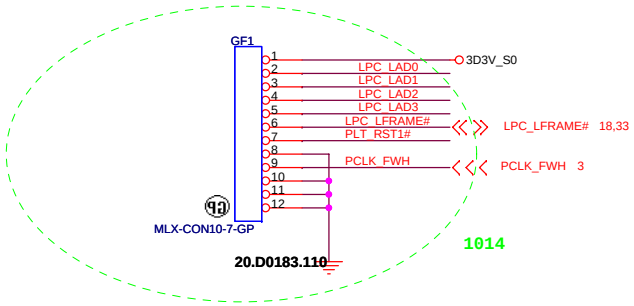
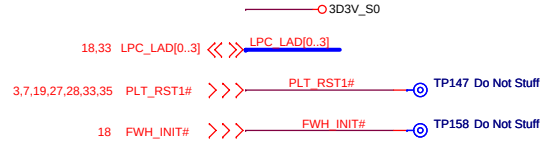
Date: Monday, October 27, 2008	Sheet 32 of 45	


FOR KBC DEBUG
THERMAL----->
BATTERY----->
WPCE773LA0DG-GP
71.00773.00G
LPC
SMB
SPI
SER/IR
A/D
D/A
GPIO
KBC
PS/2
FIU
Internal KeyBoard Connector
TPOINTCN1 Conn. Test Point
TOUCH PAD
KB1 CN Test Point
TOUCH PAD Conn. Test Point
2nd = 84.27002.C3F
2nd = 84.03906.F11
PlanarID (1,0)
SA: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
C555,C556 colse to Pin VDD
20.K0326.026
KB1
PTWO-CON26-1-GP
MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
K/B
24 1
hexainf@hotmail.com
GRATIS - FOR FREE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773
SM30
Saturday, October 18, 2008
33
45





GOLDEN FINGER FOR DEBUG BOARD



TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

UMA 2nd

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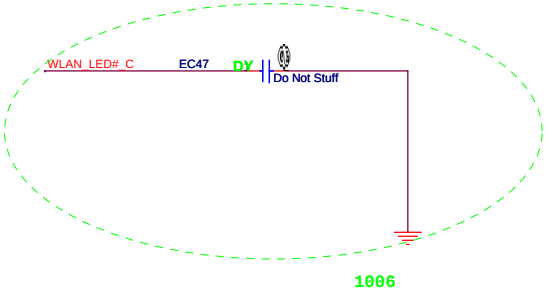
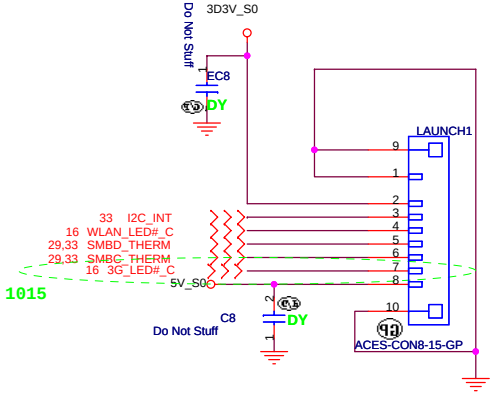
Title: ***BIOS & TPM***

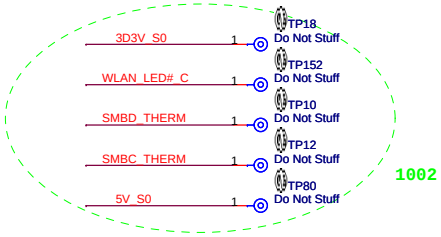
Size	Document Number	Rev
	SM30	SA

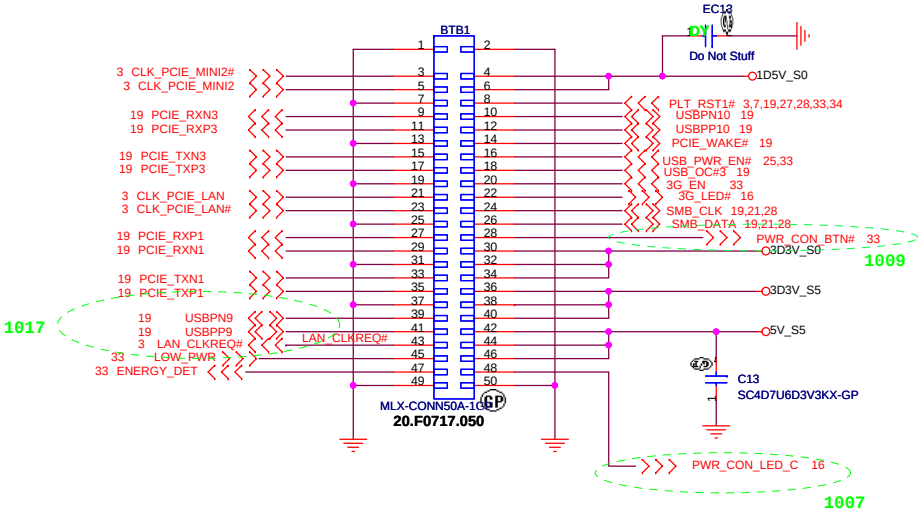
Date: Saturday, October 18, 2008 Sheet 34 of 45

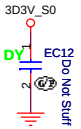


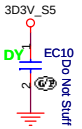


LAUNCH Test Point









UMA 2nd

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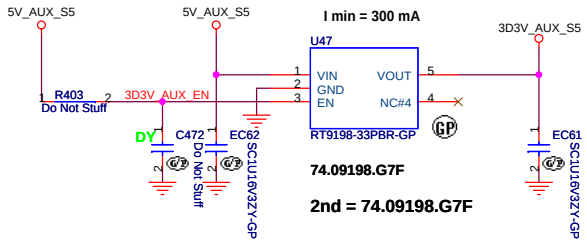
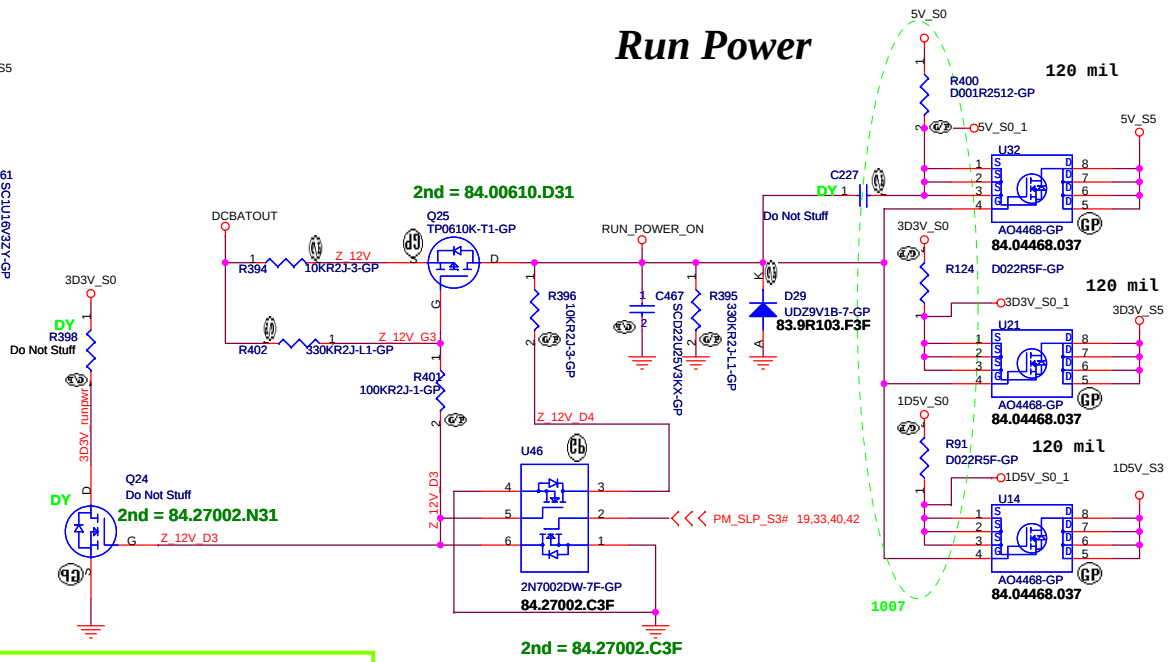
Title: **LAUNCH**		
Size	Document Number: **SM30**	Rev: SA
Date: Saturday, October 18, 2008	Sheet 35 of 45	

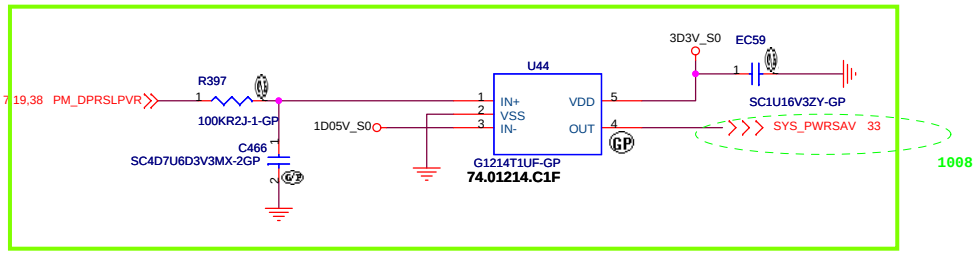
Aux Power

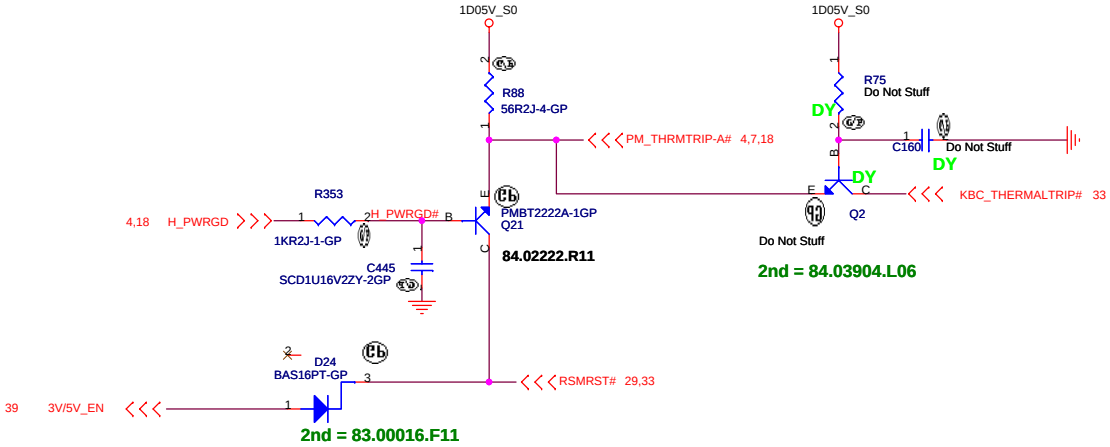
3D3V_AUX_S5

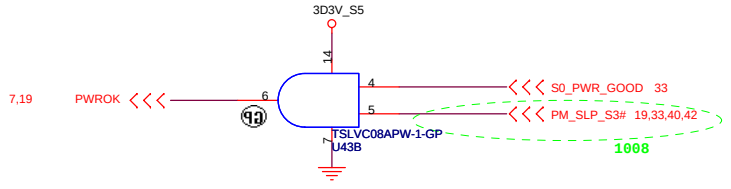


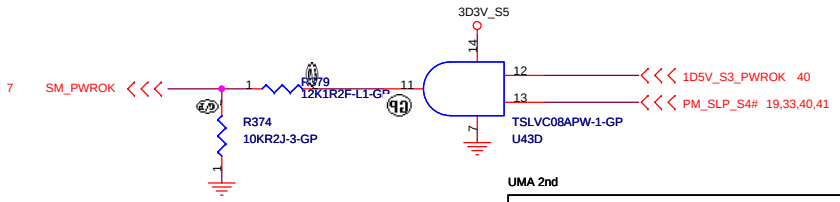
Run Power











UMA 2nd

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and 3D3V_AUX_S5**

Size	Document Number	Rev
	SM30	SA

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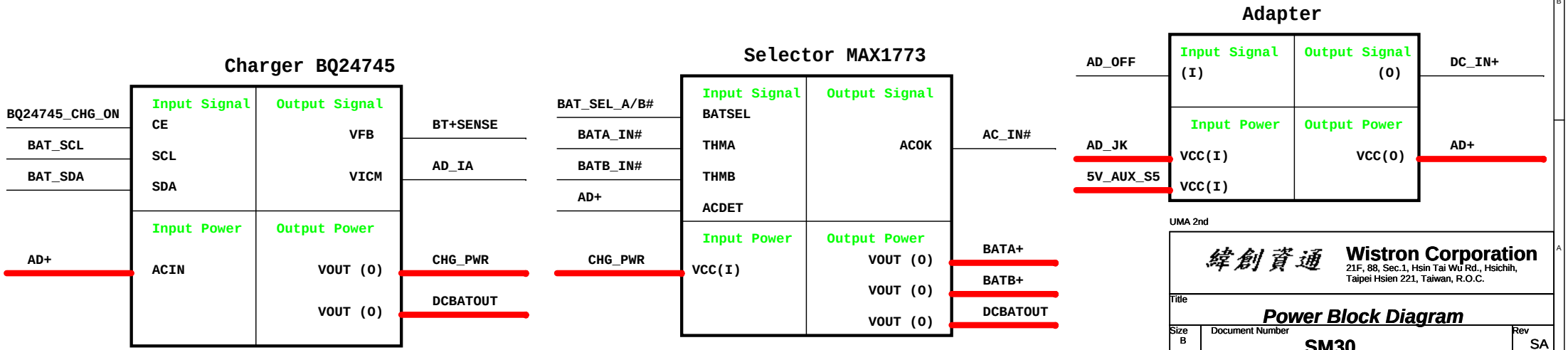

UMA 2nd

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

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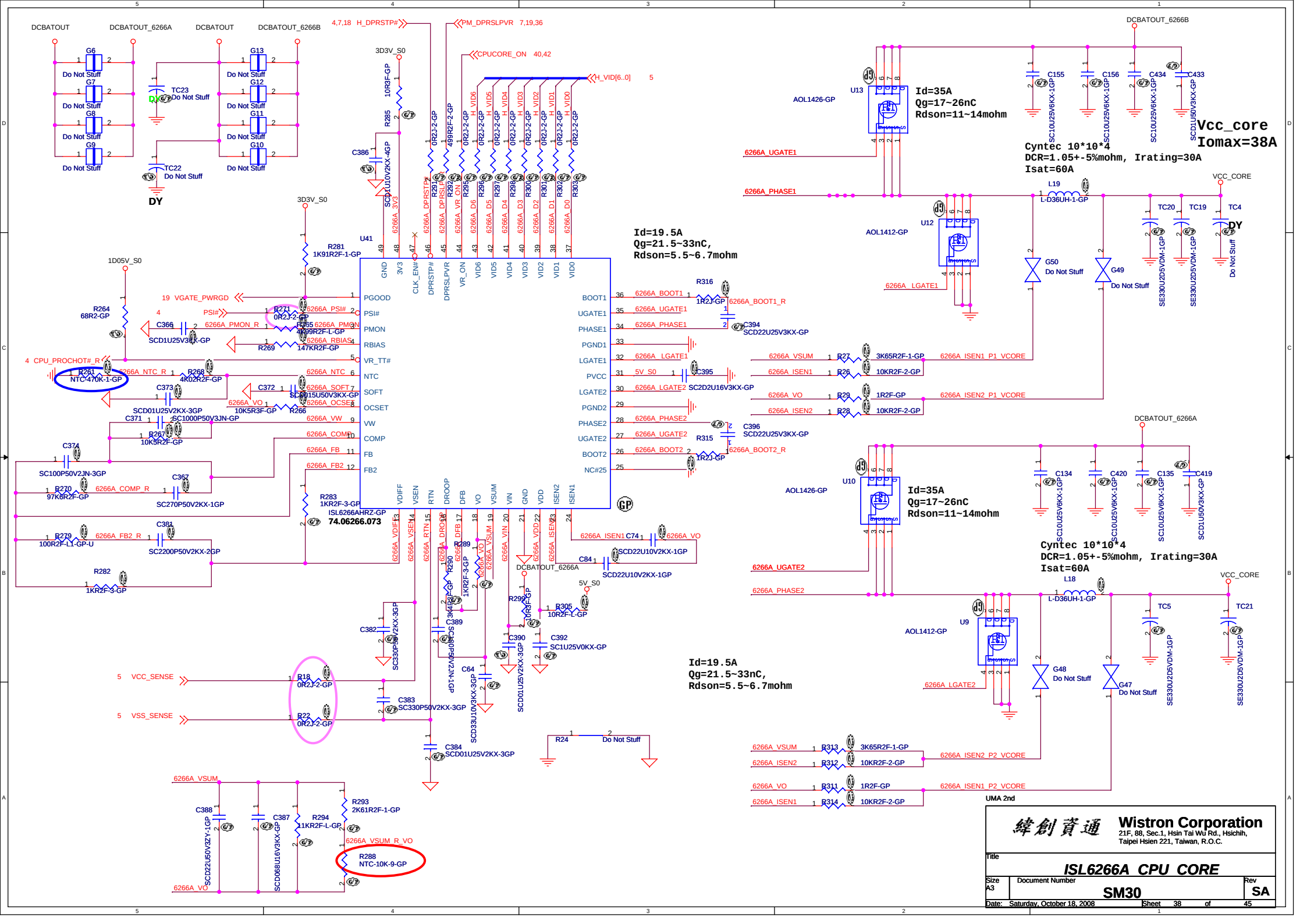
DCBATOUT
DCBATOUT_6266A
DCBATOUT
DCBATOUT_6266B
4,7,18 H_DPRSTP#
PM_DPRSLPVR 7,19,36
CPUCORE_ON 40,42
H_VID[6..0] 5
3D3V_S0
1D05V_S0
5V_S0
DY
ISL6266AHRZ-GP
74.06266.073
U41
PGOOD
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC#25
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
GND
VDD
ISEN2
ISEN1
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Id=35A
Qg=17~26nC
Rdson=11~14mohm
AOL1426-GP
AOL1412-GP
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
VCC_CORE
UMA 2nd
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A_CPU_CORE
Size A3
Document Number SM30
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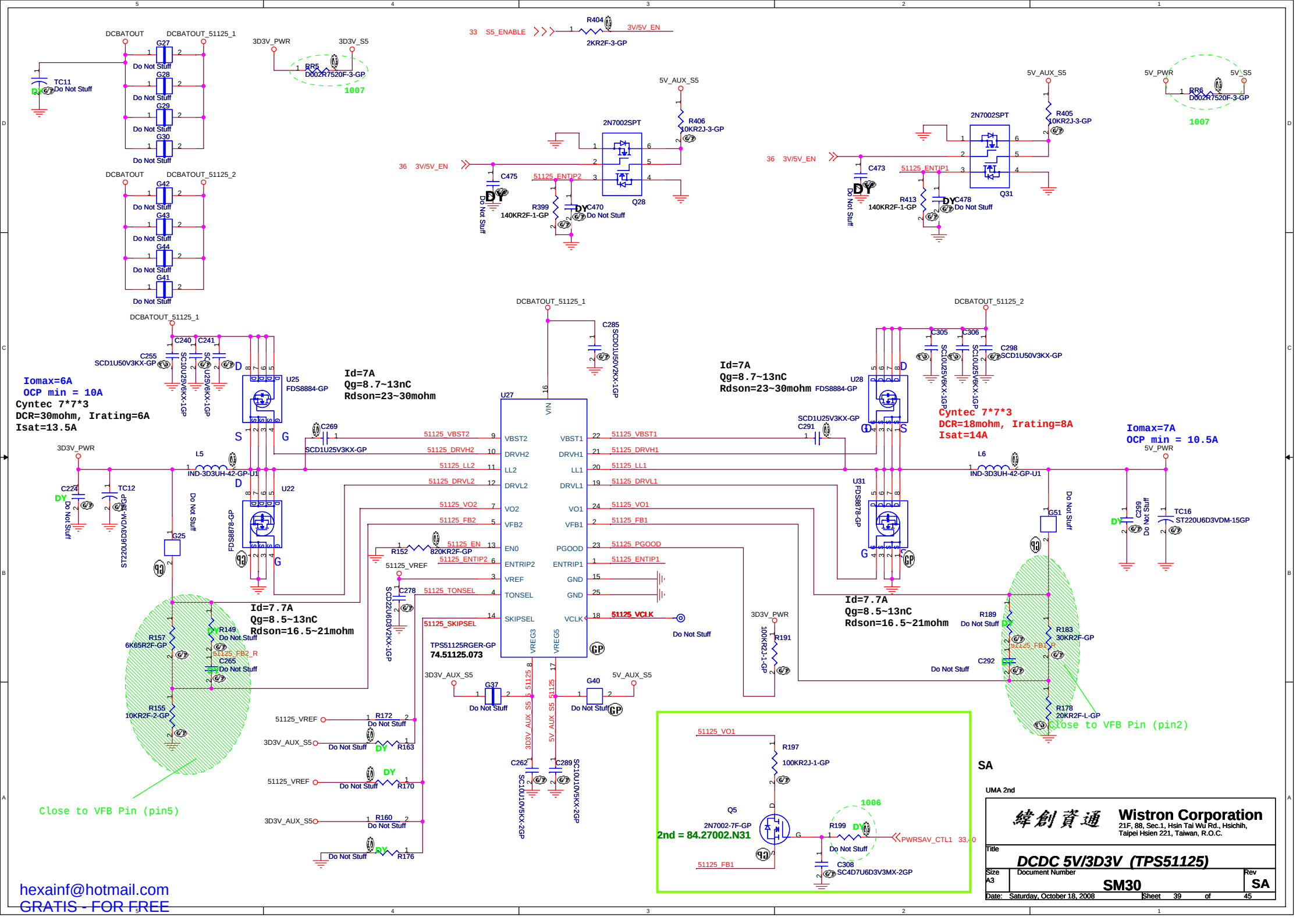
DCBATOUT
DCBATOUT_51125_1
DCBATOUT_51125_2
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
5V_S5
33 S5_ENABLE
36 3V/5V_EN
3V/5V_EN
R404
2KR2F-3-GP
RR5
RR6
D002R7520F-3-GP
1007
2N7002SPT
R405
10KR2J-3-GP
R406
10KR2J-3-GP
C475
C473
C470
C478
R399
140KR2F-1-GP
R413
140KR2F-1-GP
Q28
Q31
51125_ENTIP2
51125_ENTIP1
DY
Do Not Stuff
TC11
G27
G28
G29
G30
G42
G43
G44
G41
C240
C241
C255
SCD1U50V3KX-GP
SC1U25V6KX-1GP
U25
FDS8884-GP
U28
C305
C306
C298
SCD1U50V3KX-GP
SC1U25V6KX-1GP
Iomax=6A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=18mohm, Irating=8A
Isat=14A
Iomax=7A
OCP min = 10.5A
L5
L6
IND-3D3UH-42-GP-U1
C269
SCD1U25V3KX-GP
C291
U22
FDS8878-GP
U31
FDS8878-GP
C224
TC12
ST220U6D3VDM-15GP
TC16
C299
G25
G51
U27
TPS51125RGER-GP
74.51125.073
C285
SCD1U50V2KX-1GP
R152
820KR2F-GP
C278
SCD22U6D3V2KX-1GP
R157
6K65R2F-GP
R149
R155
10KR2F-2-GP
C265
R172
R163
R170
R160
R176
G37
G40
C262
C289
SC10U10V5KX-2GP
R191
100KR2J-1-GP
R189
R183
30KR2F-GP
C292
R178
20KR2F-L-GP
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
VIN
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
ENTRIP1
GND
VCLK
VREG3
VREG5
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_VREF
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_PGOOD
51125_ENTIP1
51125_VCLK
3D3V_AUX_S5
5V_AUX_S5
SA
UMA 2nd
2nd = 84.27002.N31
Q5
2N7002-7F-GP
R197
100KR2J-1-GP
R199
1006
PWRSAV_CTL1
C308
SC4D7U6D3V3MX-2GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Size A3
Document Number SM30
Rev SA
Date: Saturday, October 18, 2008
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hexainf@hotmail.com
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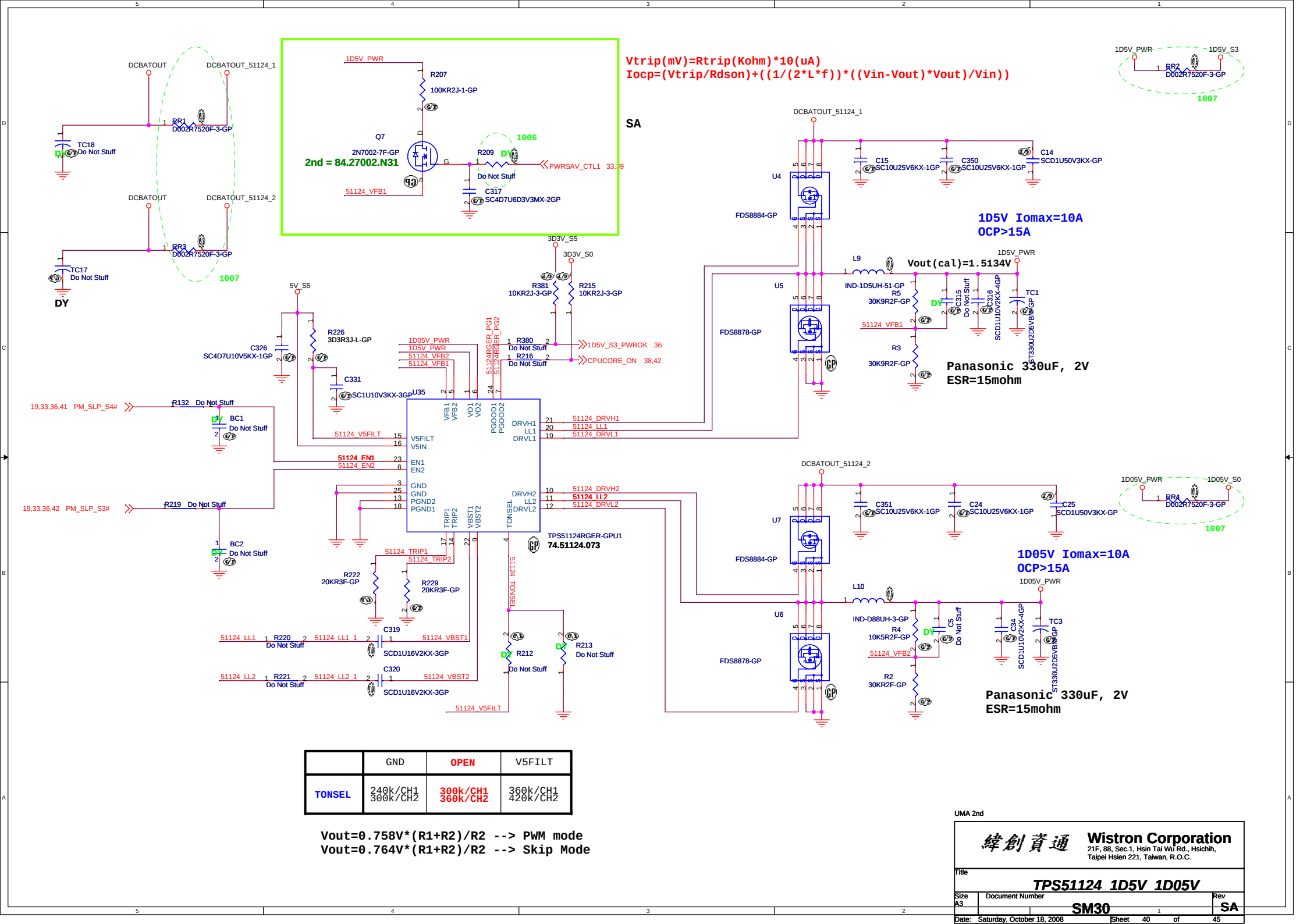
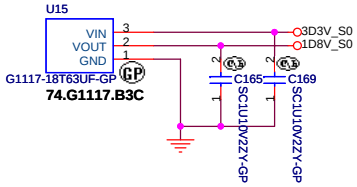
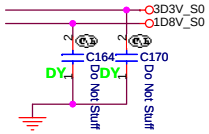
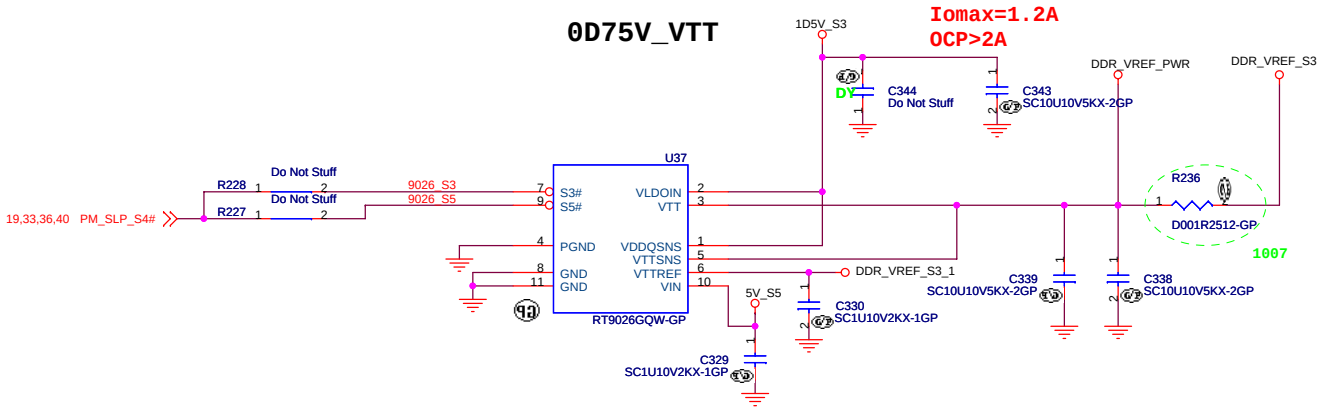


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2







UMA 2nd

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***0D75V & 1D8V***

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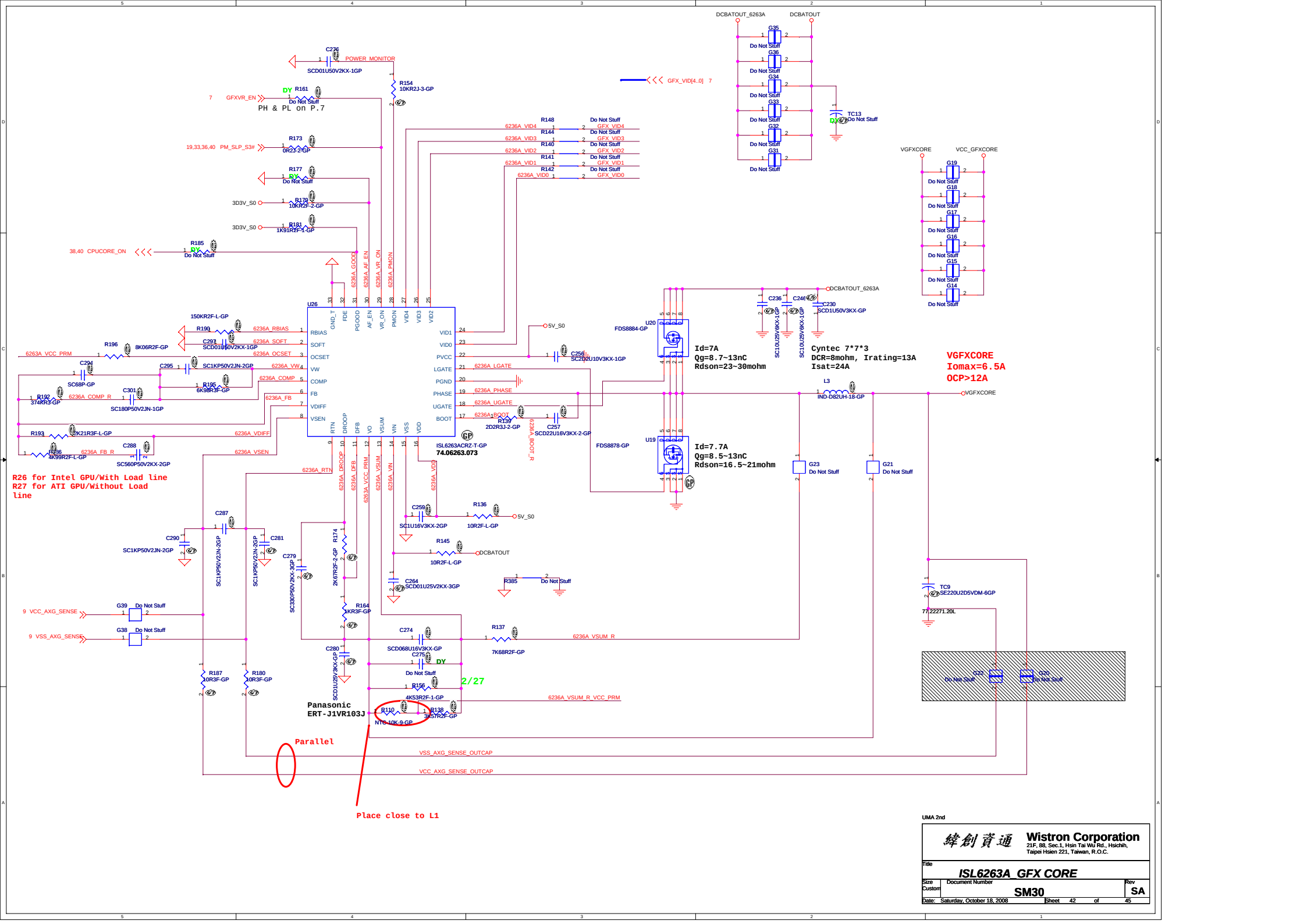
U26
ISL6263ACRZ-T-GP
74.06263.073
U20
FDS8884-GP
U19
FDS8878-GP
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Cyntec 7*7*3
DCR=8mohm, Irating=13A
Isat=24A
VGFXCORE
Iomax=6.5A
OCP>12A
R26 for Intel GPU/With Load line
R27 for ATI GPU/Without Load line
Panasonic
ERT-J1VR103J
Parallel
Place close to L1
2/27
PH & PL on P.7
DCBATOUT_6263A
DCBATOUT
VGFXCORE
VCC_GFXCORE
GFX_VID[4..0]
POWER_MONITOR
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
UMA 2nd
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6263A_GFX CORE
SM30
Saturday, October 18, 2008
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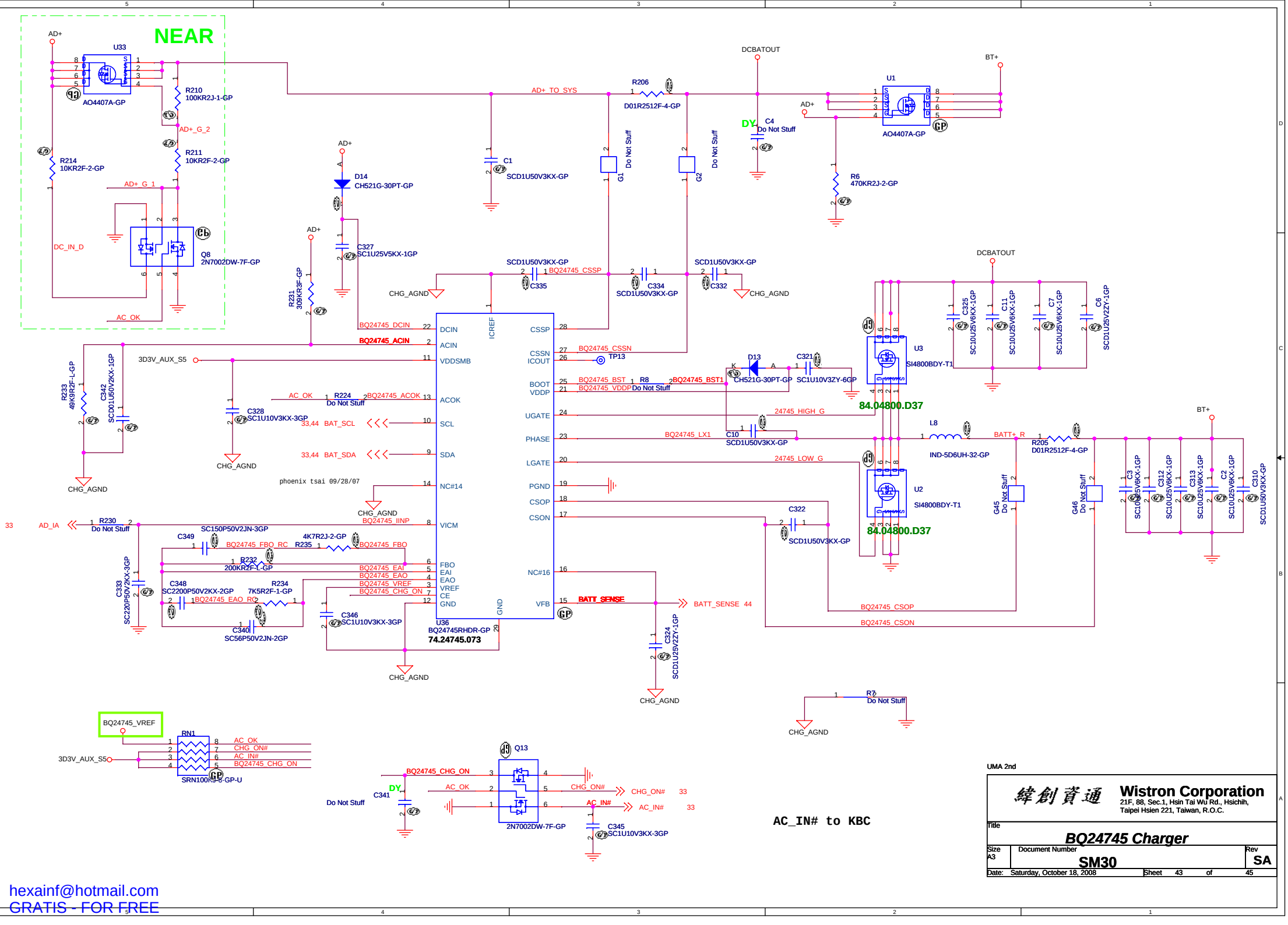
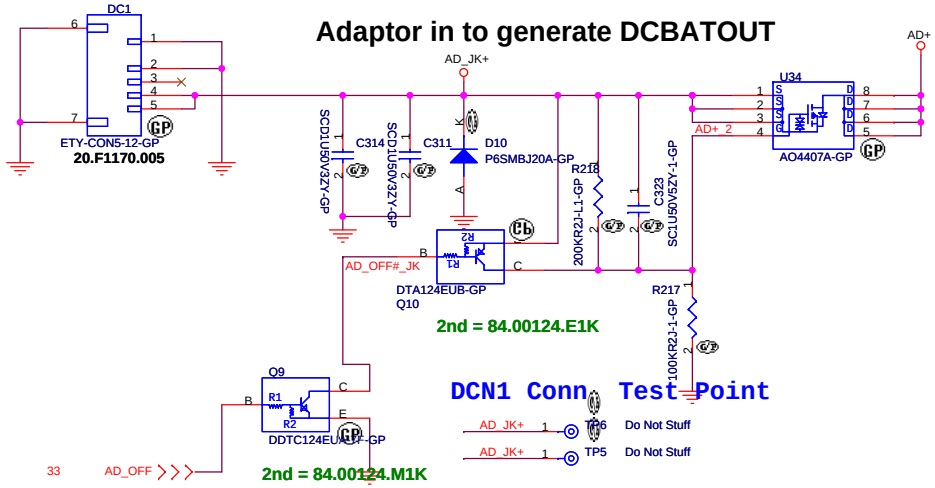
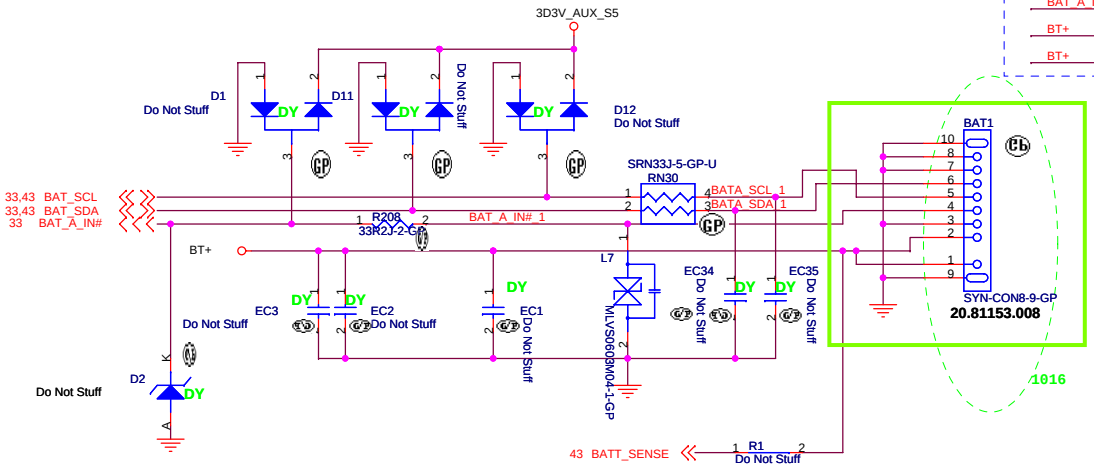


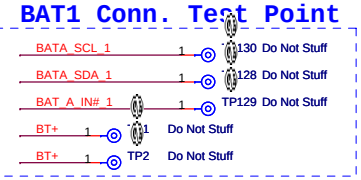
Adaptor in to generate DCBATOUT



MAIN BATTERY CONNECTOR



BAT1 Conn. Test Point



UMA 2nd

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AD&BTY CONNECTER & BTY SWITCH***

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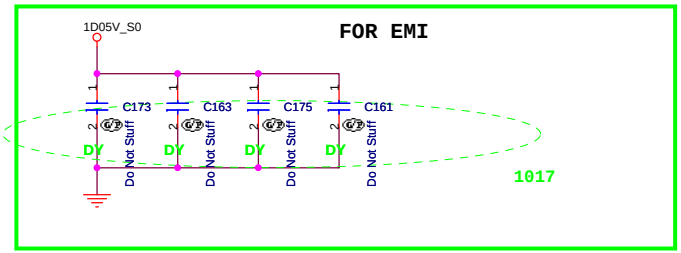
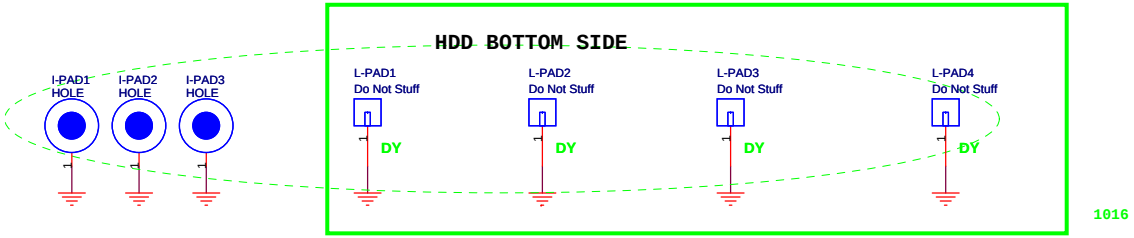
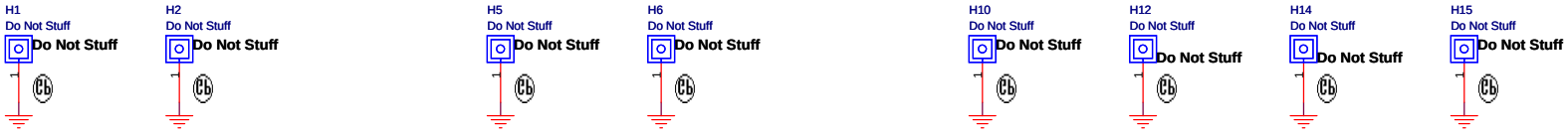
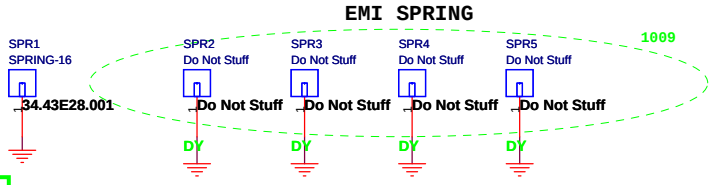
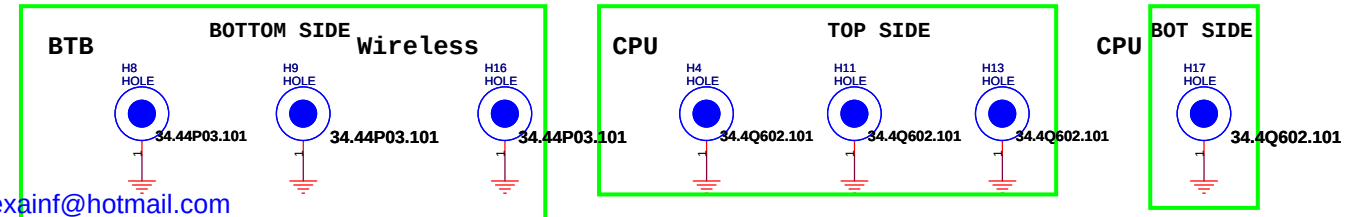








Stand off Location



UMA 2nd

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *EMI/Spring/Boss*

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