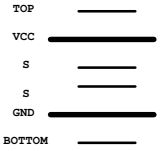
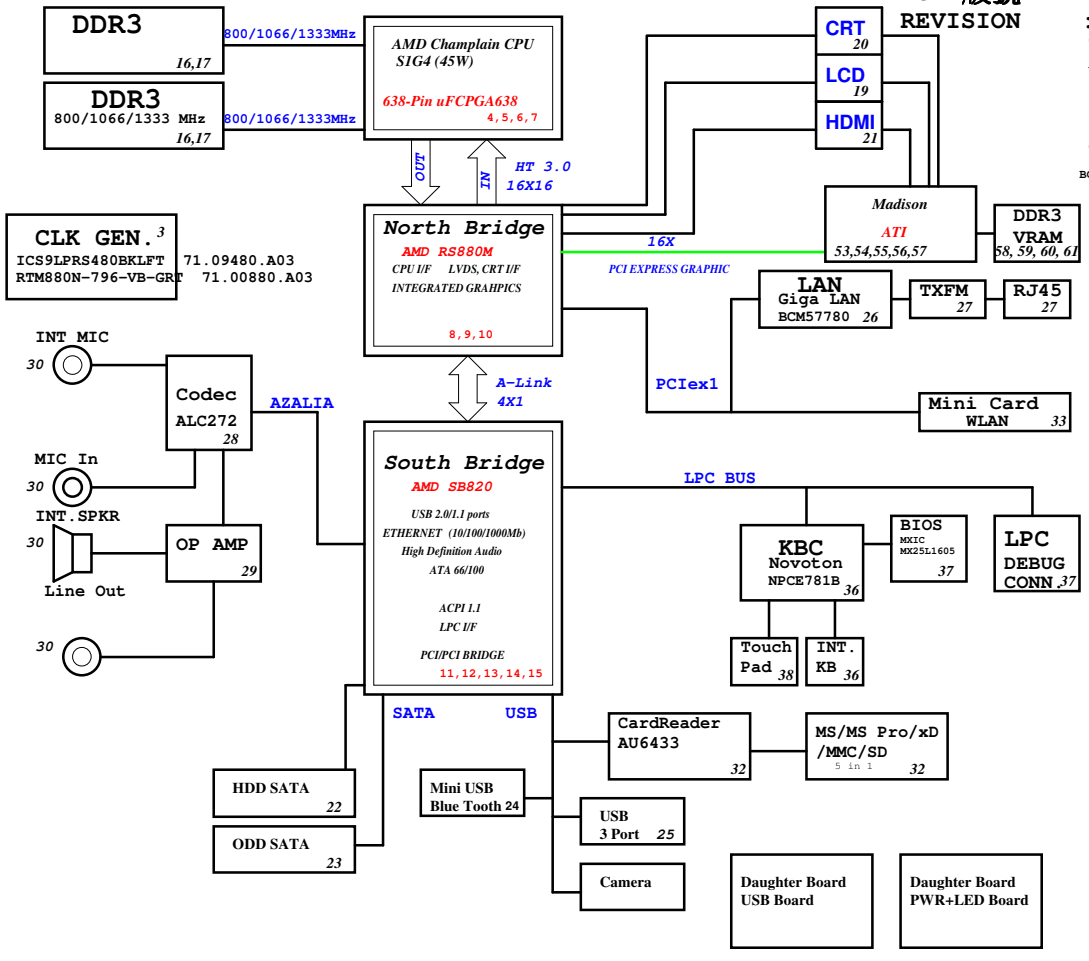
HM42-DN Block Diagram

Project code: 91.4HD01.001
PCB P/N : 48.4GX01.0SA
PCB 版號 : 09919 SA
REVISION : PCB STACKUP





SYSTEM DC/DC RT8223 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5.5A) 3D3V_S5(5A)

SYSTEM DC/DC RT8209E 47	
5V_S5	1D5V_S3(14A)
RT9026 47	
5V_S5	0D75_S3(1.2A)

SYSTEM DC/DC RT8209E 48	
INPUTS	
DCBATOUT	1D1V_S0(11A)
RT9025 48	
3D3V_S5	1D1V_S5(1.4A)

RT9025 49	
5V_S5	1D1V_VGA
RT9161 49	
3D3V_S0	2D5V_S0 (200mA)
RT9025 49	
1D5V_S3	1D05V_S0 (1.4A)

CHARGER BQ24745 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.55V 18A VDDNB 0~1.55V 4A

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 1 of 63

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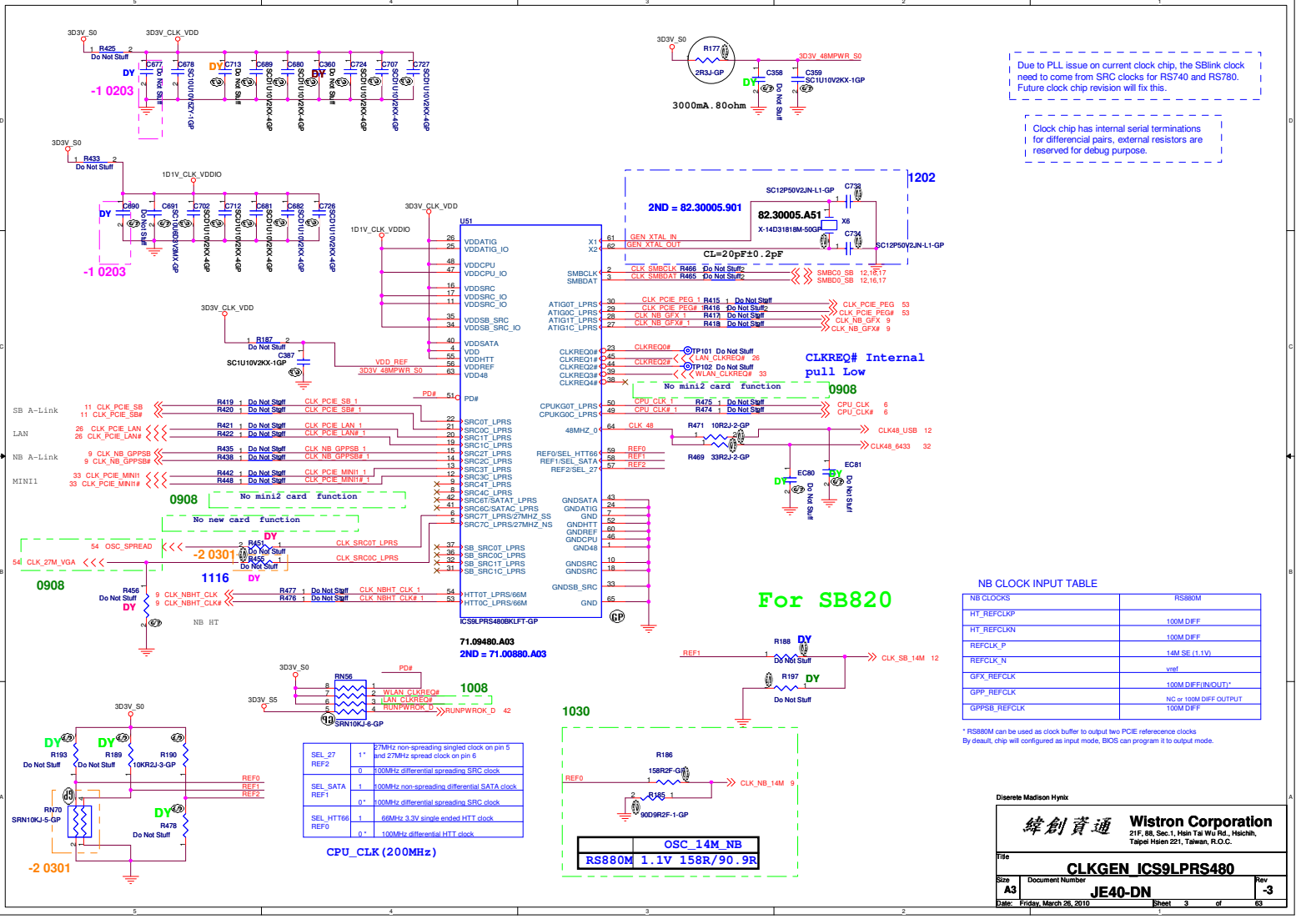
Title: History

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 2 of 63



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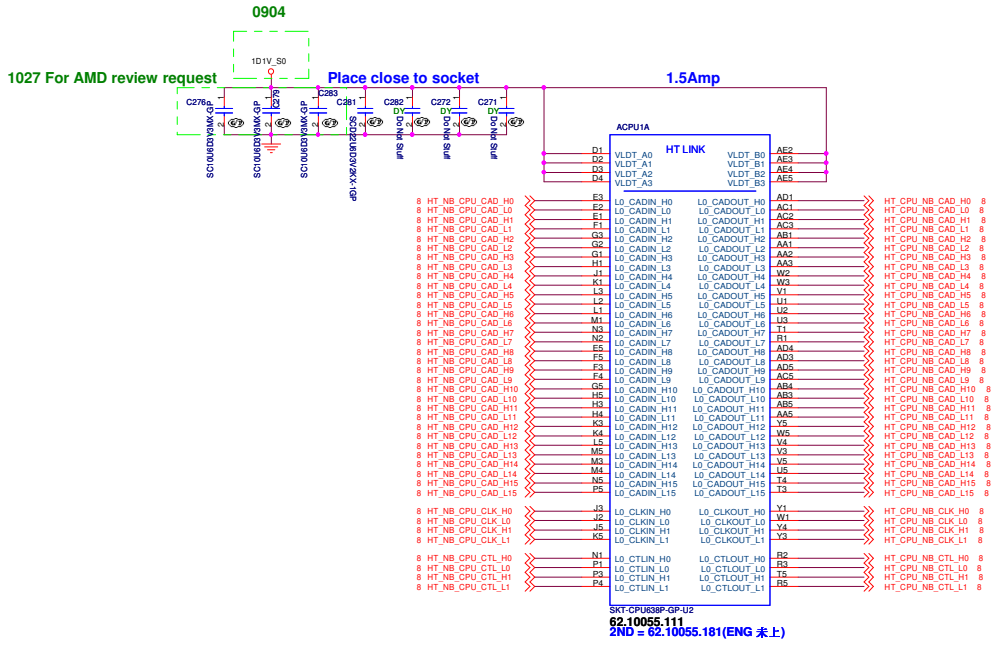

SKT-BGA638H176

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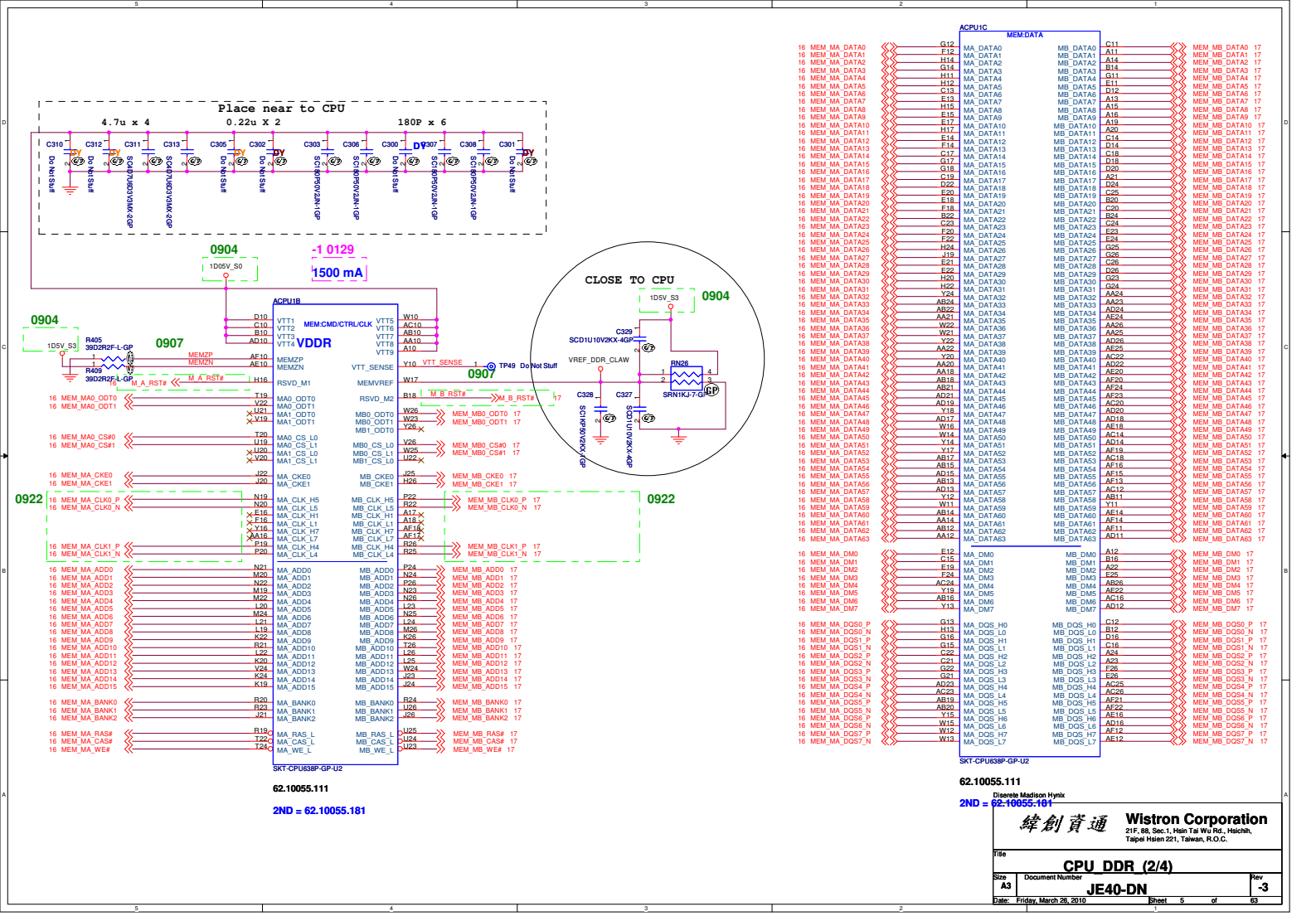
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_HT_LINK I/F_(1/4)**

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 4 of 63



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_DDR_(2/4)**

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 5 of 63

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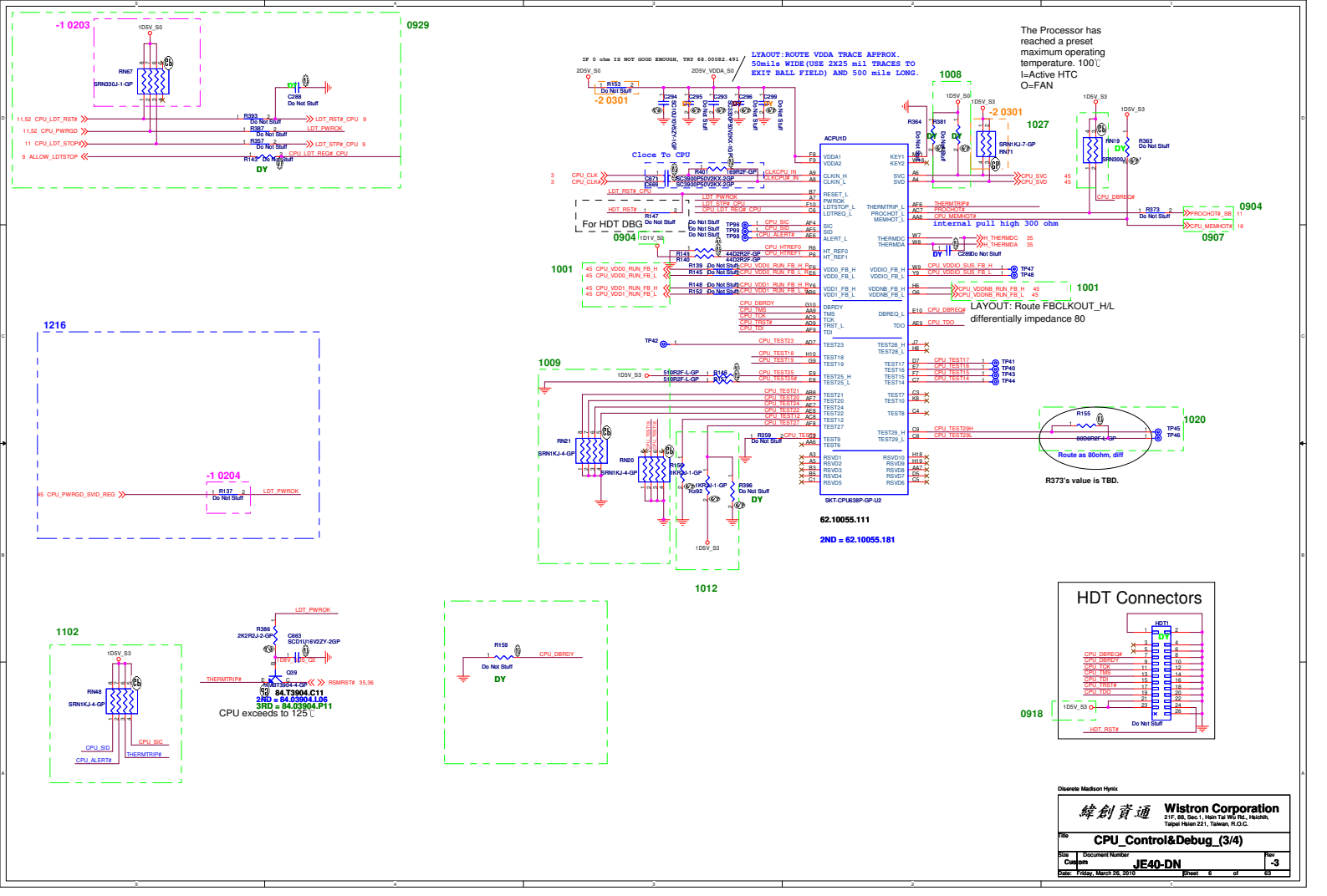
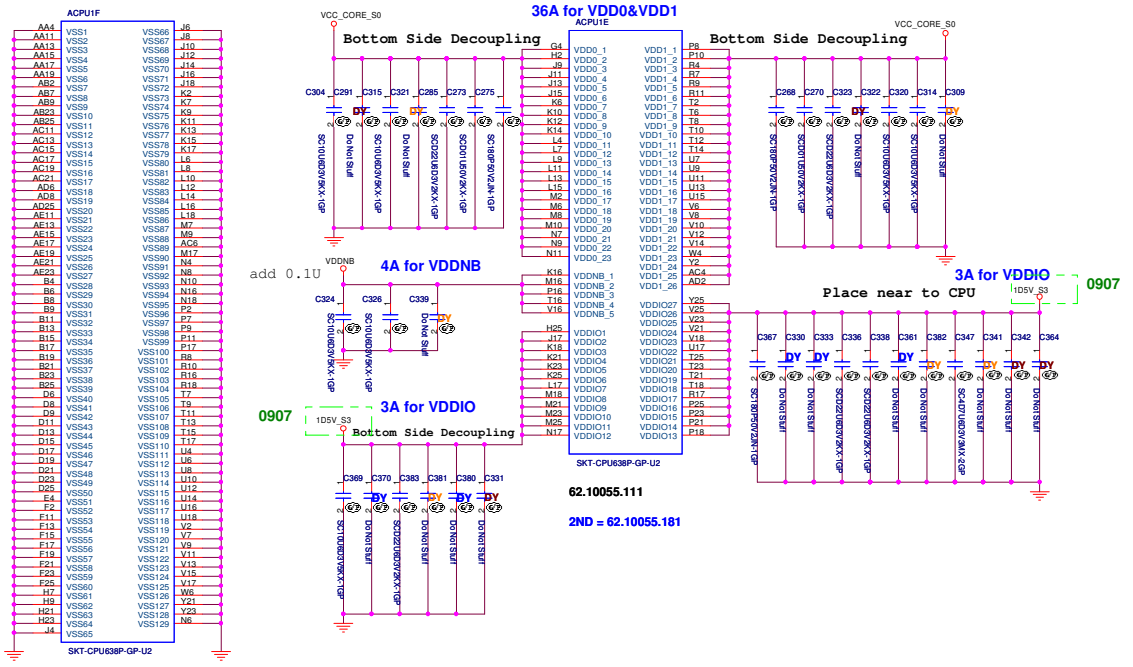


Diserete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU_Control&Debug_(3/4)
Size: Custom	Document Number: JE40-DN
Rev	-3
Date: Friday, March 26, 2010	Sheet 6 of 53



Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU_Power_(4/4)**	
Size A3	Document Number **JE40-DN**	Rev **-3**
Date: Friday, March 26, 2010	Sheet 7 of 63	

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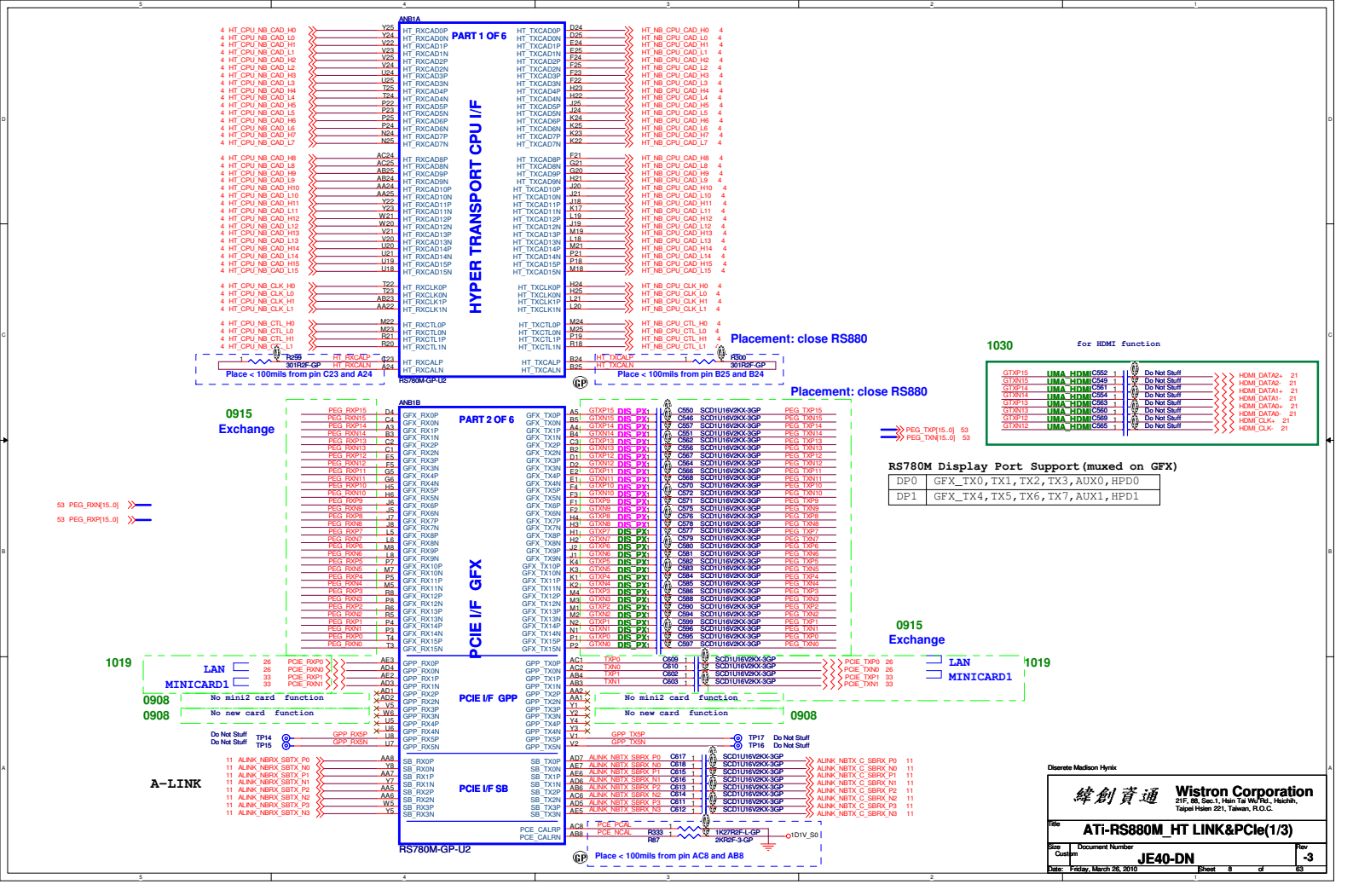

RS780M Display Port Support(muxed on GFX)

DP0	GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1	GFX_TX4,TX5,TX6,TX7,AUX1,HPD1

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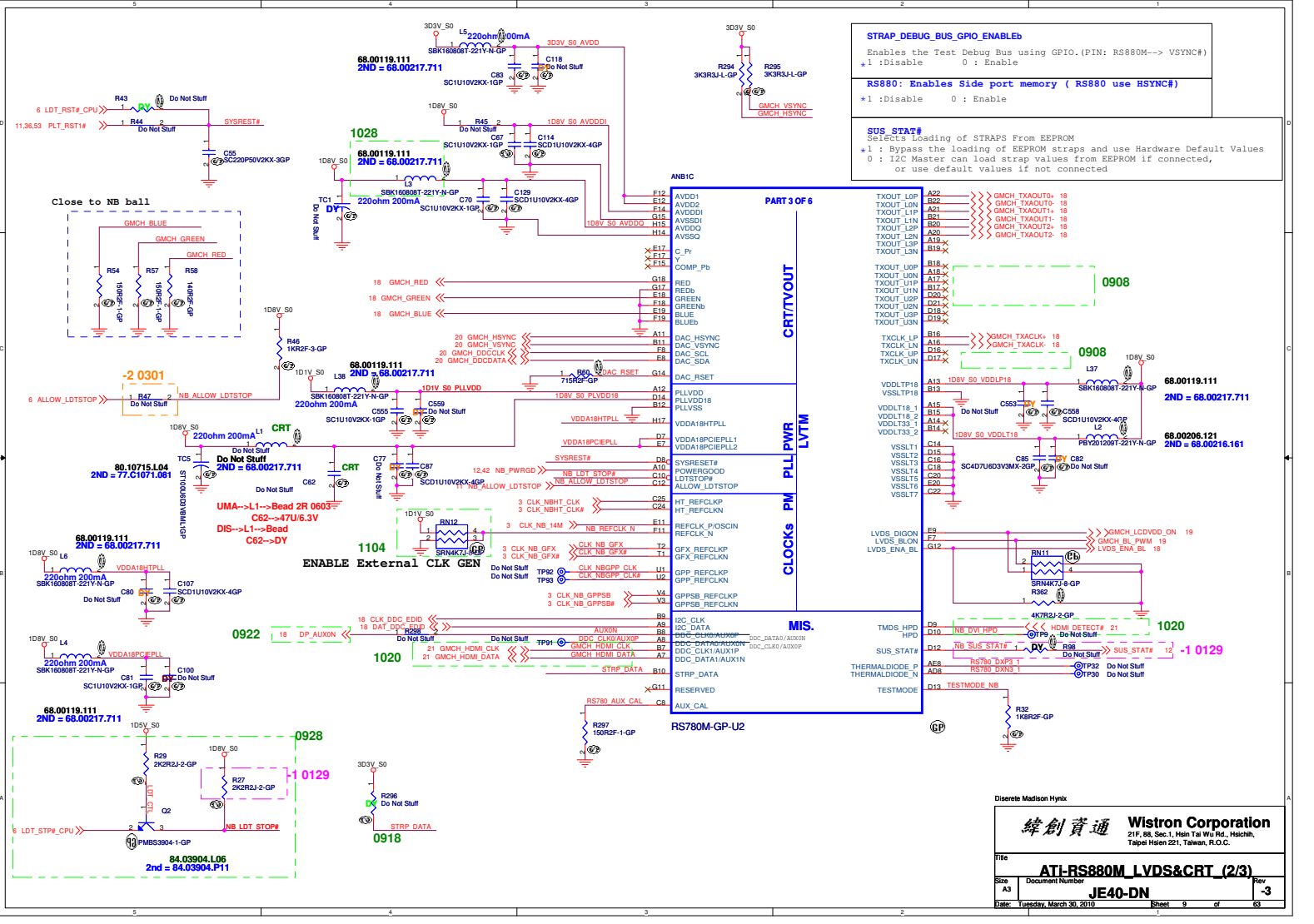
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS880M_HT LINK&PCIe(1/3)

Size: Custom | Document Number: JE40-DN | Rev: -3

Date: Friday, March 26, 2010 | Sheet 8 of 63



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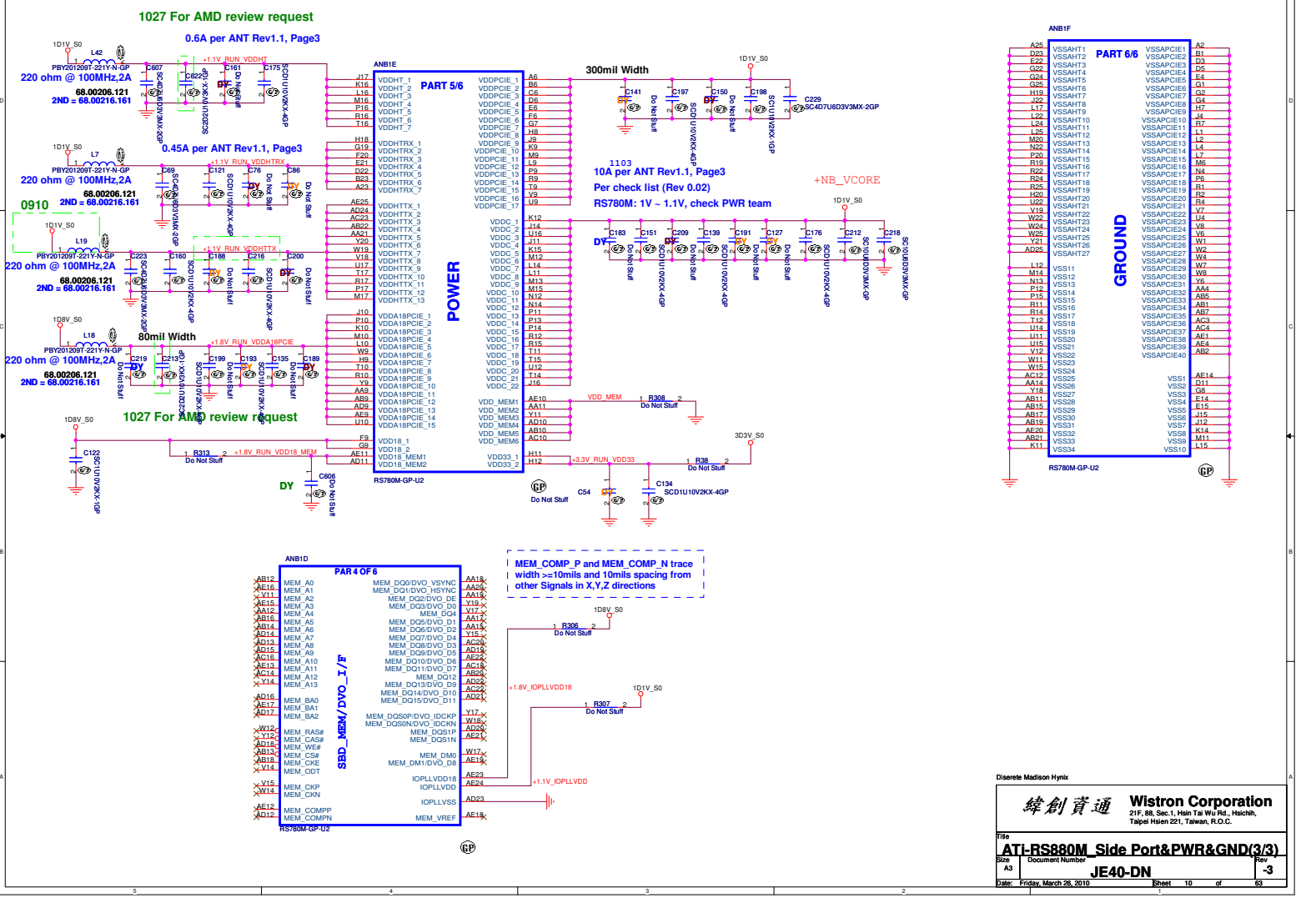


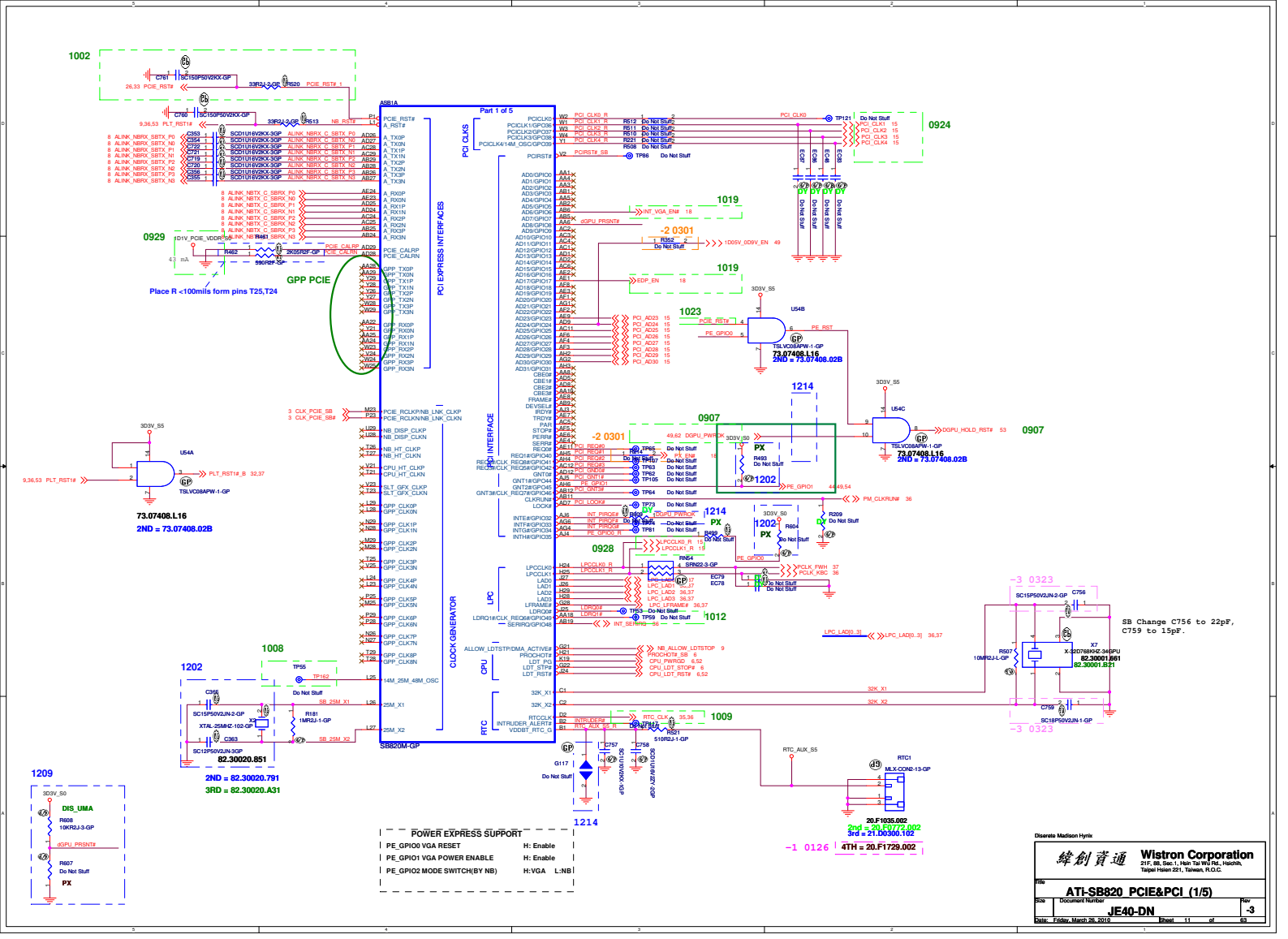
Diserete Madison Hynix

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-RS880M_Side Port&PWR&GND(3/3)

Size: A3 | Document Number: JE40-DN | Rev: -3

Date: Friday, March 26, 2010 | Sheet 10 of 63



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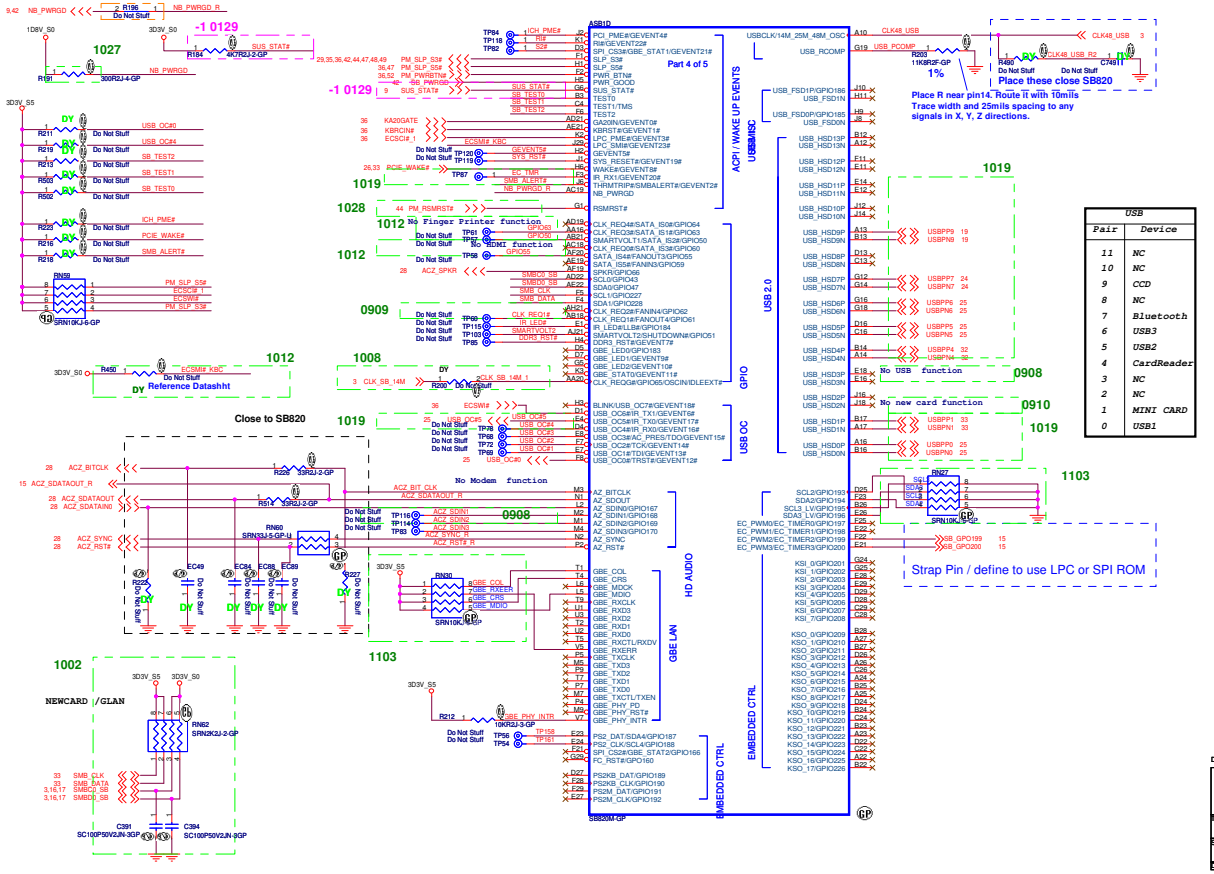

USB	
Pair	Device
11	NC
10	NC
9	CCD
8	NC
7	Bluetooth
6	USB3
5	USB2
4	CardReader
3	NC
2	NC
1	MINI CARD
0	USB1

OCP5#

OCP0#

Discrete Madison Hynix

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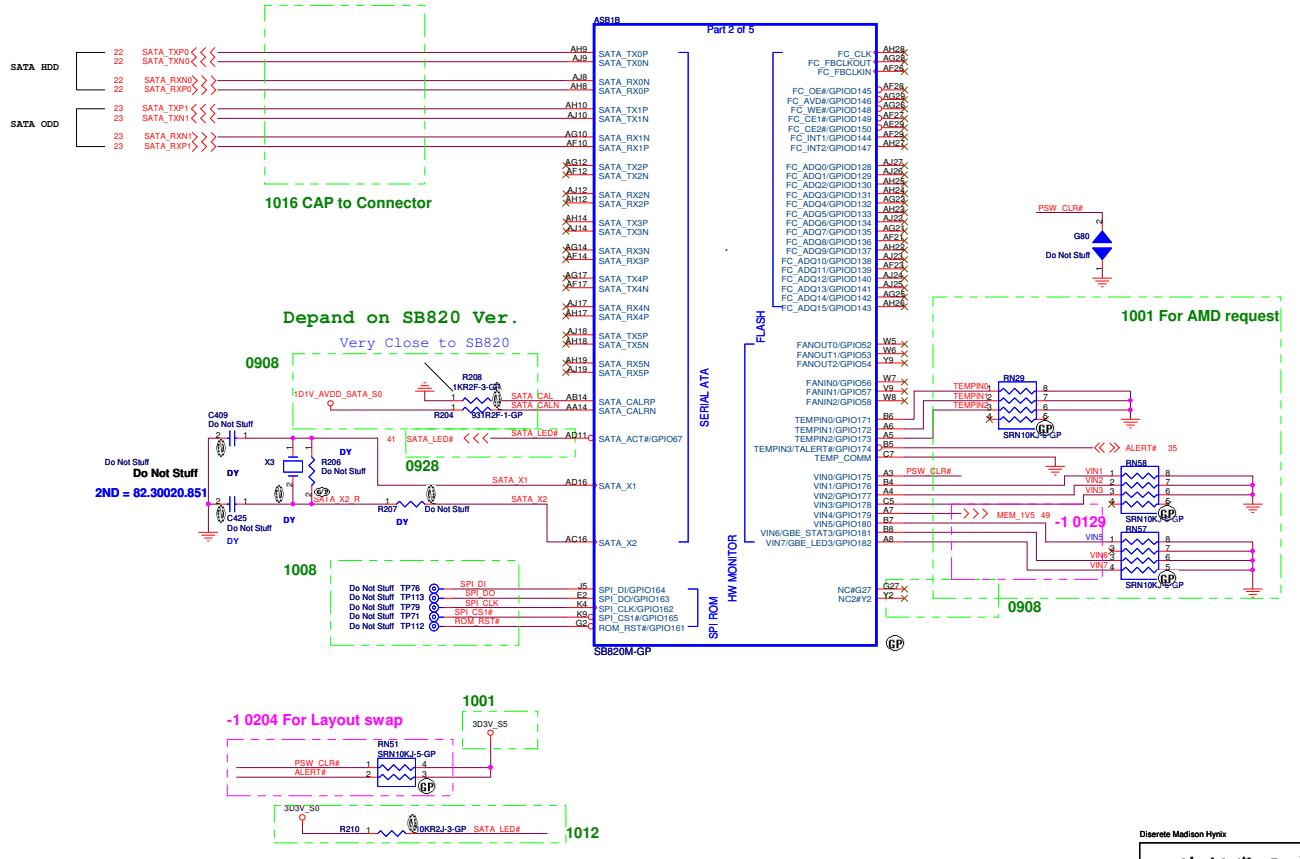
Title: ATI-SB820 USB&GPIO (2/5)

Size: Custom | Document Number: JE40-DN | Rev: -3

Date: Friday, March 26, 2010 | Sheet 12 of 63



Diserete Madison Hynix

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB820 SATA-IDE (3/5)**

Size	Document Number	Rev
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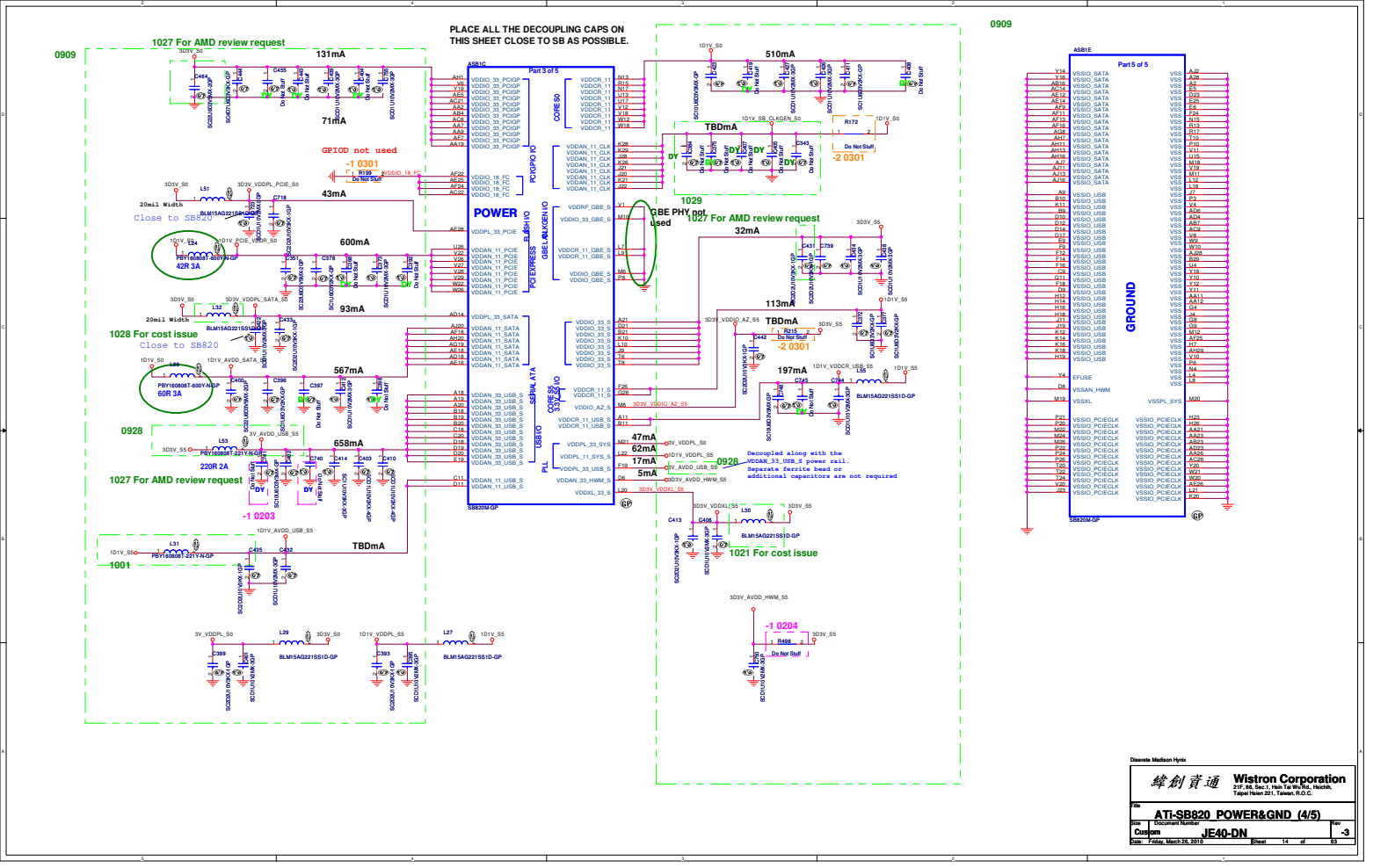
PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.
0909
1027 For AMD review request
131mA
71mA
GPIOD not used
-1 0301
43mA
20mil Width
Close to SB820
600mA
42R 3A
93mA
1028 For cost issue
Close to SB820
567mA
60R 3A
0928
658mA
220R 2A
1027 For AMD review request
-1 0203
TBDmA
1001
510mA
TBDmA
-2 0301
1029
GBE PHY not used
1027 For AMD review request
32mA
113mA
TBDmA
-2 0301
197mA
47mA
62mA
17mA
5mA
0928
Decoupled along with the
VDDAN_33_USB_S power rail.
Separate ferrite bead or
additional capacitors are not required
1021 For cost issue
-1 0204
Part 3 of 5
Part 5 of 5
POWER
GROUND
Discrete Madison Hynix
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATI-SB820 POWER&GND (4/5)
Size
Document Number
Rev
Custom
JE40-DN
-3
Date: Friday, March 26, 2010
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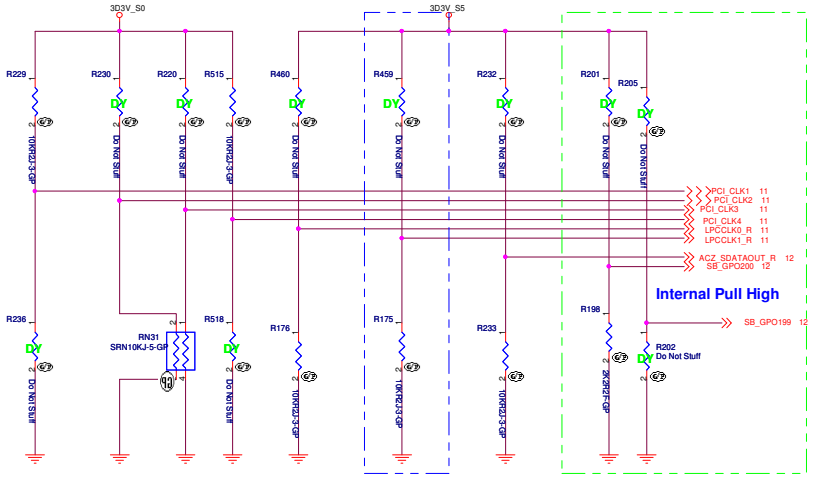
REQUIRED STRAPS

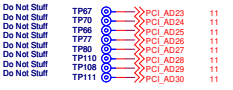
REQUIRED SYSTEM STRAPS

1115



1002

DEBUG STRAPS



	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

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Title: **ATI-SB820 STRAPPING (5/5)**

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 28, 2010 Sheet 15 of 63

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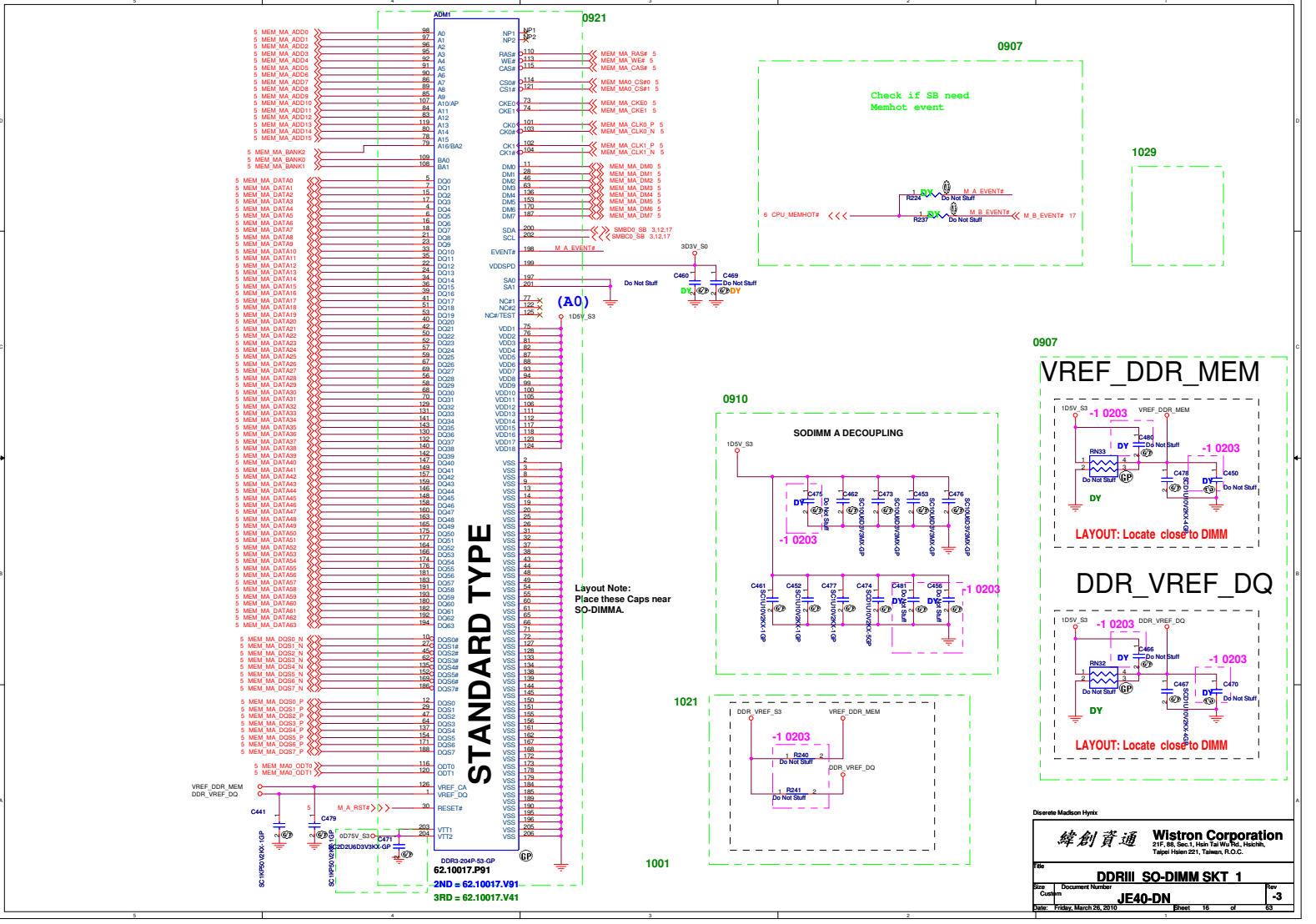

0921
0907
1029
0910
1021
1001
STANDARD TYPE
(A0)
Check if SB need
Memhot event
SODIMM A DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA.
VREF_DDR_MEM
DDR_VREF_DQ
LAYOUT: Locate close to DIMM
DDR3-204P-53-GP
62.10017.P91
2ND = 62.10017.V91
3RD = 62.10017.V41
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Title
DDRIII SO-DIMM SKT 1
Size
Custom
Document Number
JE40-DN
Rev
-3
Date: Friday, March 26, 2010
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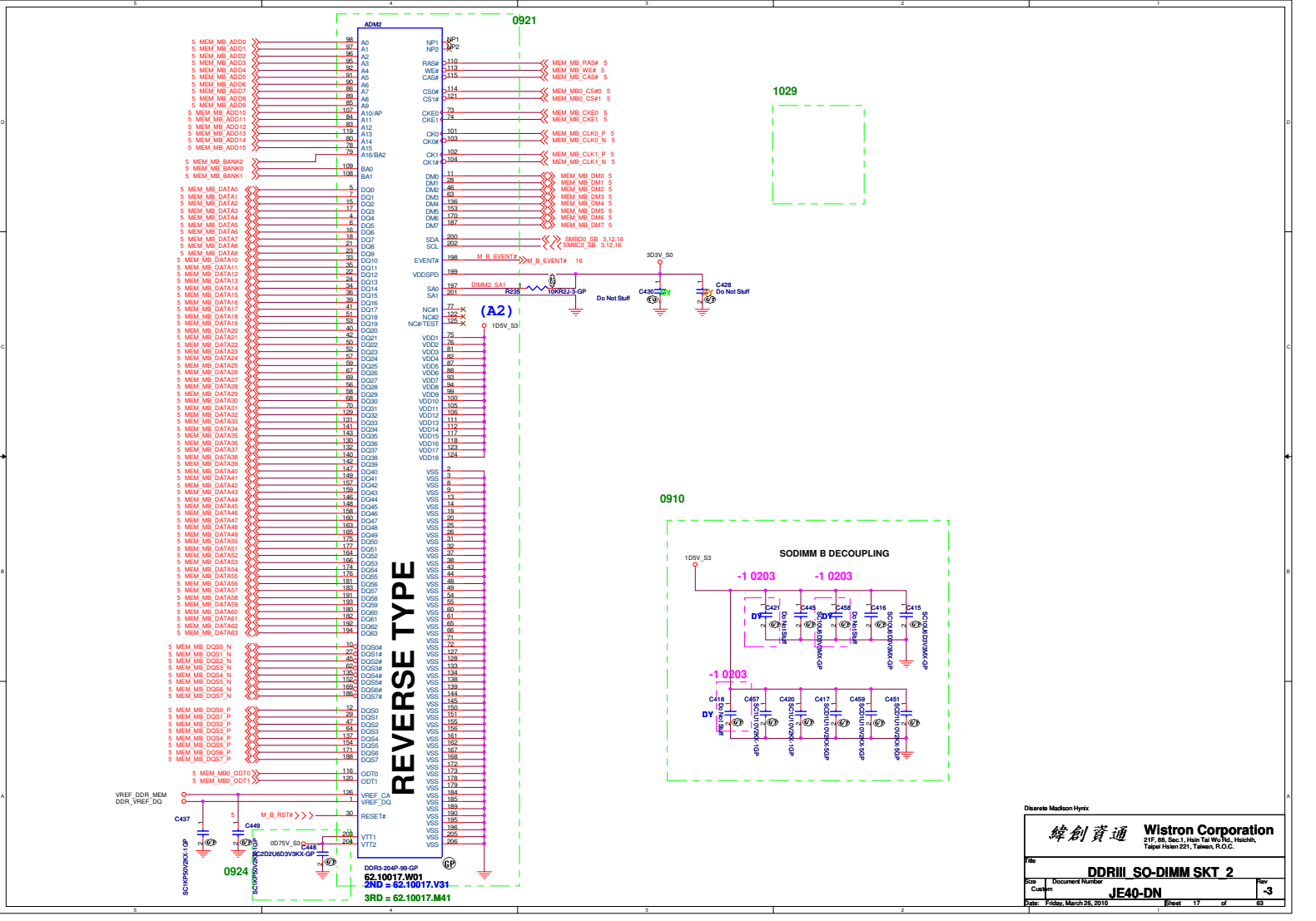

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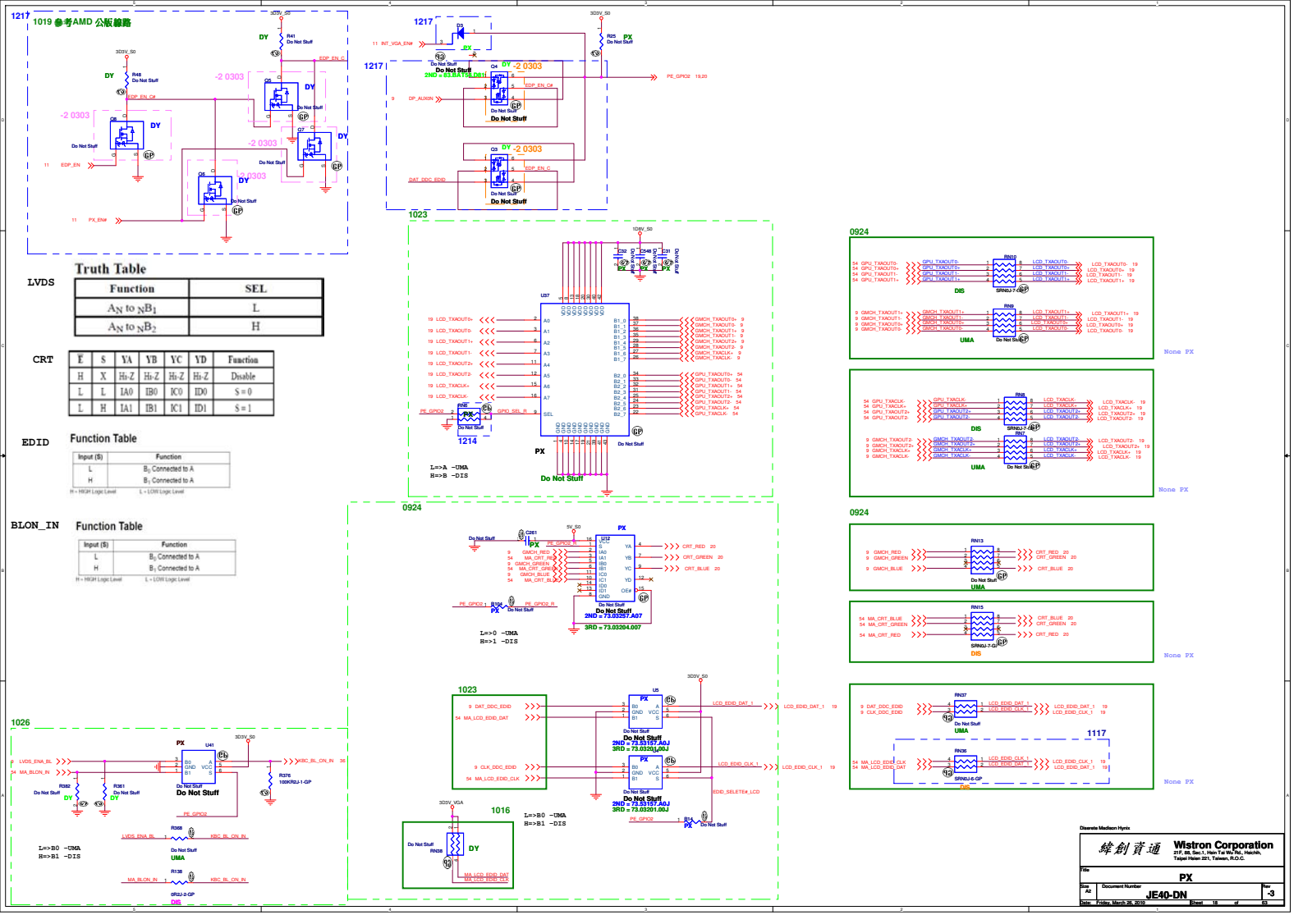

LVDS

Truth Table

Function	SEL
A_N to $_NB_1$	L
A_N to $_NB_2$	H

CRT

E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

EDID

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level

BLON_IN

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level

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Title: PX

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LCD/INVERTER/CCD CONN

1028 for EMC request

0923

LCD1 — PEX/CONN40-2R-GP-U

2ND = 20.F1289.040

JV42_DN SA
20.F1093.040
define same as SJM50-PU,can use SJM50 Cable

DCBATOUT_LCD1 — F1 PCK7SW-1D1A24V-GP-U — DCBATOUT
69.50007.A31
2ND = 69.50007.A41

EC10 DY Not Stuff — C18 SC10U25V6KX-1GP

-1 0125

1005

USBPN9 — EC9 Not Stuff DY
USBPP9 — EC8 Do Not Stuff DY

LCD_EDID_CLK_1 — ECT1 DY Do Not Stuff
LCD_EDID_DAT_1 — ECT2 DY Do Not Stuff

0929 del CCD CON

LCD_TXAOUT0- / LCD_TXAOUT0+ 18
LCD_TXAOUT1- / LCD_TXAOUT1+ 18
LCD_TXAOUT2- / LCD_TXAOUT2+ 18
LCD_TXACLK- / LCD_TXACLK+ 18
LCD_EDID_DAT_1 / LCD_EDID_CLK_1 18

3D3V_S0 — LCDVDD — C14 SCD47U6.3V-Z-GP

3D3V_S0 — SRN2K2J-1-GP RN5 — LCD_EDID_DAT_1 / LCD_EDID_CLK_1

1016

Change PX

0922

3D3V_S0 — R622 Do Not Stuff DY — 36 APS_EN — R623 Do Not Stuff DY

-1 0125

-1 0208

C938 DY Do Not Stuff — C939 DY Do Not Stuff — C940 DY Do Not Stuff — C941 DY Do Not Stuff — C942 DY Do Not Stuff — C943 DY Do Not Stuff — C944 DY Do Not Stuff — C945 DY Do Not Stuff

LCD_TXAOUT0- / LCD_TXAOUT0+ 1
LCD_TXAOUT1- / LCD_TXAOUT1+ 1
LCD_TXAOUT2- / LCD_TXAOUT2+ 1
LCD_TXACLK- / LCD_TXACLK+ 1

1005

JV42_DN SA

UMA — GMCH_LCDVDD_ON — R15 Do Not Stuff — LCDVDD_ON
MA_LCDVDD_ON — R24 1K2J-2-GP DIS — LCDVDD_ON

F2 FUSE-1D1A6V-4GP-U — 3D3V_S0
69.50007.691
2ND = 69.50007.771

CCD_PWR — C21 SC47U6.3V5KX-3GP — C16 DY Do Not Stuff

JV42_DN_PX SA

9 GMCH_LCDVDD_ON — R22 DY Do Not Stuff
54 MA_LCDVDD_ON — R17 DY Do Not Stuff

PX U6 — B0 GND B1 A VCC S — Do Not Stuff — Do Not Stuff
2ND = 73.53157.A0J

3D3V_S0 — LCDVDD_ON — R18 100KR2J-1-GP — 18,20 PE_GPIO2

LCDVDD — C24 DY Not Stuff — C20 SC47U6.3V5KX-GP

Layout 40 mil

U2 — EN IN#5 GND OUT IN#4 — G52851T11U-GP
74.05285.07F
2ND = 74.09724.09F

3D3V_S0 — C9 SC10U6.3V5KX-GP

1026

Reserve direct connector to KBC

-1 0125

UMA_PX

9 GMCH_BL_PWM — R31 Do Not Stuff — L_BKLTCTL_R
36 BRIGHTNESS — R10 DY Do Not Stuff — BRIGHTNESS_DIS
54 ATI_BRIGHTNESS — R12 33R2J-2-GP DIS_PX — BRIGHTNESS_DIS
18,20 PE_GPIO2 — R258 Do Not Stuff PX — PE_GPIO2_C

PX U34 — B0 GND B1 A VCC S — Do Not Stuff — Do Not Stuff

3D3V_S0 — BRIGHTNESS_CN — C497 SC10U25V2JN-GP

L_BKLTCTL_R — R259 Do Not Stuff — BRIGHTNESS_CN
BRIGHTNESS_DIS — R8 0R2J-2-GP UMA — BRIGHTNESS_CN

36 BLON_OUT — 1KR2J-3-GP R19 — R21 100KR2J-1-GP — C23 SC1000P50V2JN-3GP — BLON_OUT_1

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

Size: Custom | Document Number: JE40-DN | Rev: -3

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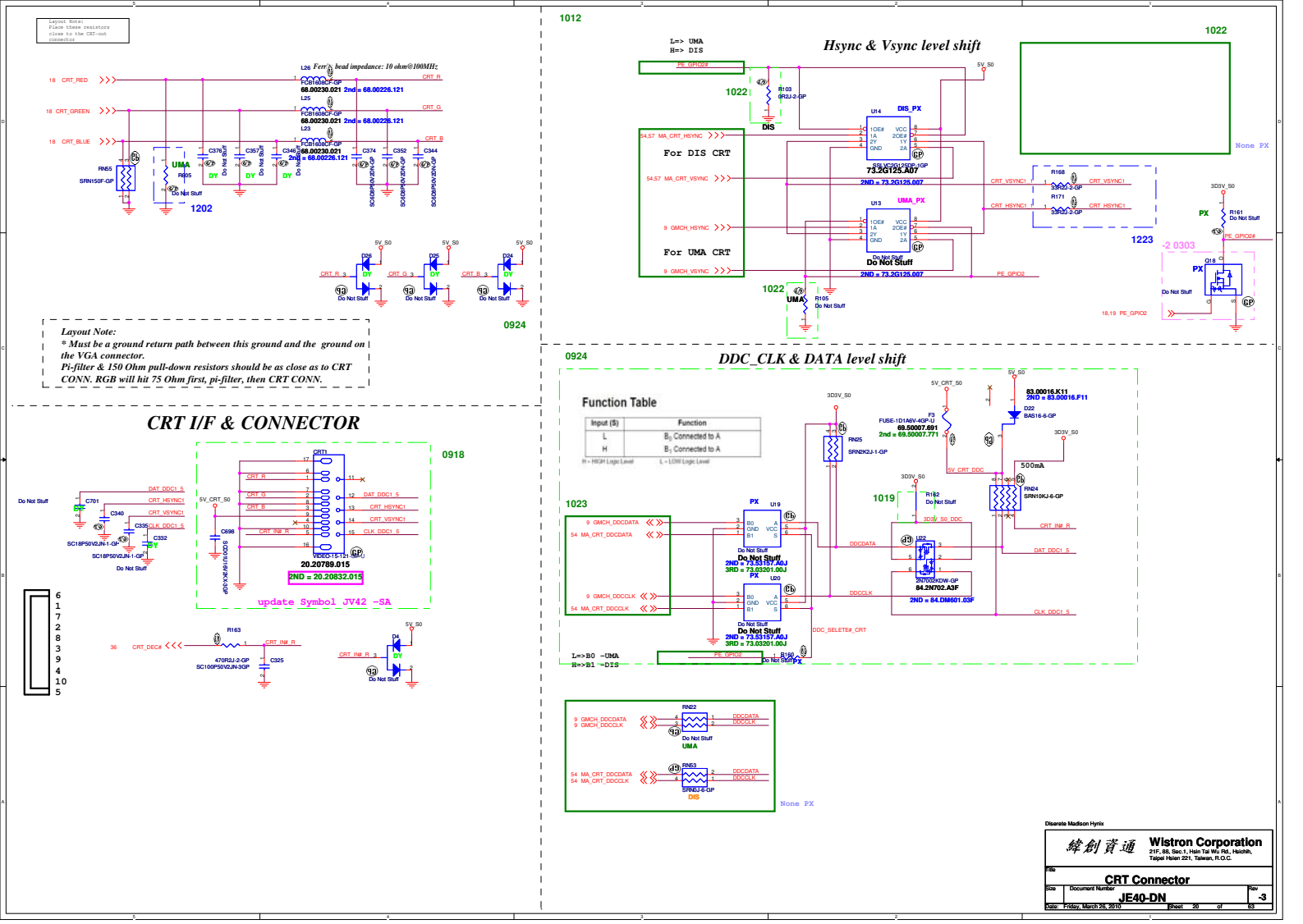

Layout Note:
Place these resistors close to the CRT-out connector
Ferr's bead impedance: 10 ohm@100MHz
18 CRT_RED
18 CRT_GREEN
18 CRT_BLUE
CRT_R
CRT_G
CRT_B
L26 FCB1608CF-GP 68.00230.021 2nd = 68.00226.121
L25 FCB1608CF-GP 68.00230.021 2nd = 68.00226.121
L23 FCB1608CF-GP 68.00230.021 2nd = 68.00226.121
RN55 SRN150F-GP
UMA
R605 Do Not Stuff
1202
C376 C357 C346 C374 C352 C344
SC6DB9P50V2ZN-GP
5V_S0
D26 D25 D24
CRT_R_3 CRT_G_3 CRT_B_3
Do Not Stuff
0924
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.
CRT I/F & CONNECTOR
0918
CRT1
VIDEO-15-121-GP
20.20789.015
2ND = 20.20832.015
update Symbol JV42 -SA
Do Not Stuff
C701 C340 C335 C332
SC18P50V2JN-1-GP
DAT_DDC1_5
CRT_HSYNC1
CRT_VSYNC1
CLK_DDC1_5
5V_CRT_S0
C698
SCD01U16V2KX-GP
CRT_IN#_R
R163 470R2J-2-GP SC100P50V2JN-3GP
C325
CRT_DEC#
D4
1012
Hsync & Vsync level shift
L=> UMA
H=> DIS
PE_GPIO2#
R103 0R2J-2-GP
1022
DIS
U14 DIS_PX
SSLVC2G125DB-1GP
73.2G125.A07
2ND = 73.2G125.007
U13 UMA_PX
Do Not Stuff
2ND = 73.2G125.007
54,57 MA_CRT_HSYNC
54,57 MA_CRT_VSYNC
9 GMCH_HSYNC
9 GMCH_VSYNC
For DIS CRT
For UMA CRT
R105 Do Not Stuff
1022
None PX
R168 33R2J-2-GP
R171 33R2J-2-GP
CRT_VSYNC1
CRT_HSYNC1
1223
3D3V_S0
R161 Do Not Stuff
PX
-2 0303
Q18
18,19 PE_GPIO2
0924
DDC_CLK & DATA level shift
Function Table
Input (S) | Function
L | B0 Connected to A
H | B1 Connected to A
H = HIGH Logic Level L = LOW Logic Level
3D3V_S0
RN25 SRN2K2J-1-GP
5V_CRT_S0
F3 FUSE-1D1A6V-4GP-U 69.50007.691 2nd = 69.50007.771
83.00016.K11 2ND = 83.00016.F11
D22 BAS16-6-GP
500mA
5V_CRT_DDC
RN24 SRN10KJ-6-GP
1023
1019
PX
U19
U20
Do Not Stuff
2ND = 73.53157.A0J
3RD = 73.03201.00J
9 GMCH_DDCDATA
54 MA_CRT_DDCDATA
9 GMCH_DDCCLK
54 MA_CRT_DDCCLK
DDCDATA
DDCCLK
DDC_SELETE#_CRT
U22 2N7002KDW-GP 84.2N702.A3F
2ND = 84.DM601.03F
CRT_IN#_R
DAT_DDC1_5
CLK_DDC1_5
L=>B0 -UMA
H=>B1 -DIS
PE_GPIO2
R160 Do Not Stuff
RN22 Do Not Stuff UMA
RN53 SRN0J-6-GP DIS
None PX
Diserete Madison Hynix
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT Connector
Size
Document Number
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-3
Date: Friday, March 26, 2010
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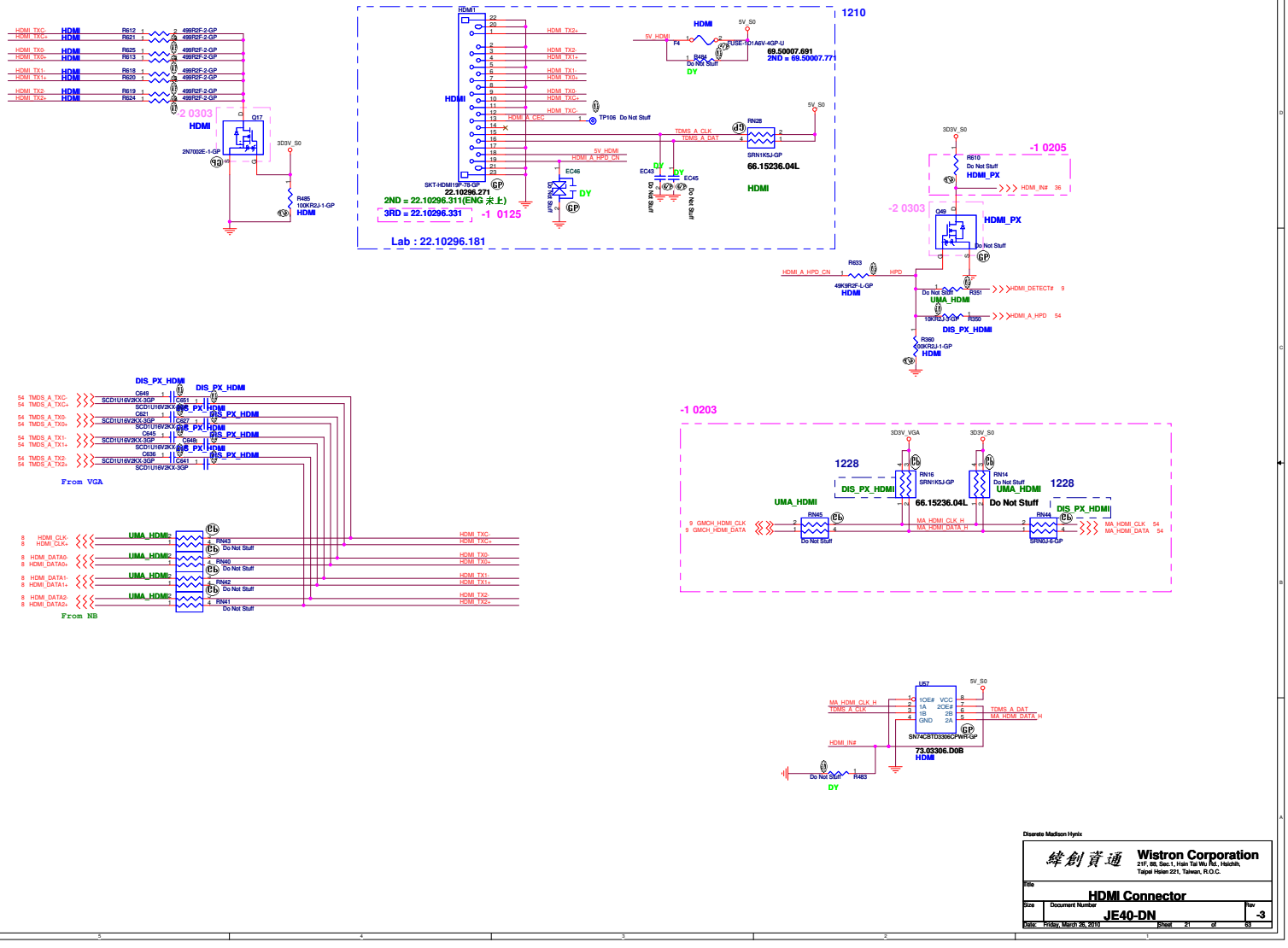

Discrete Madison Hynix

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Title	HDMI Connector	
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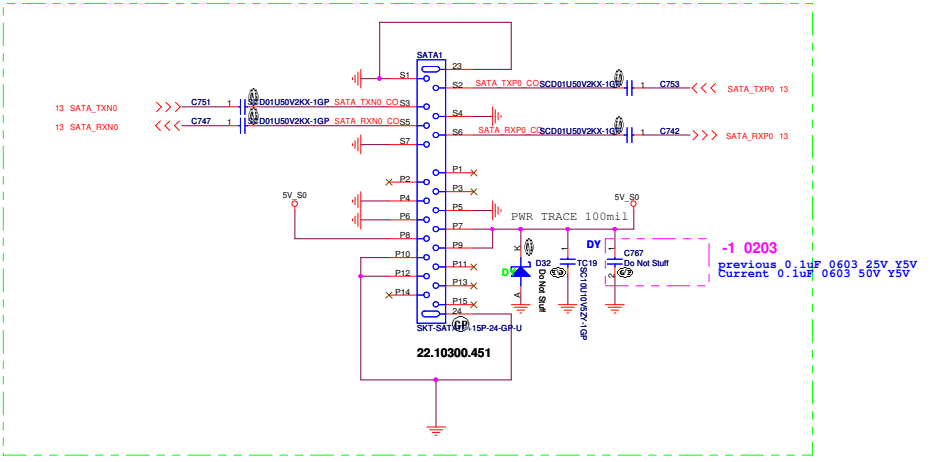
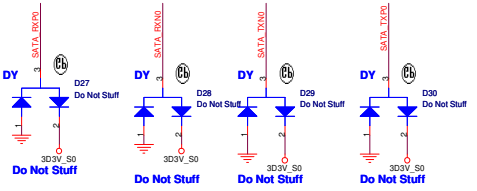
SATA Connector

0923

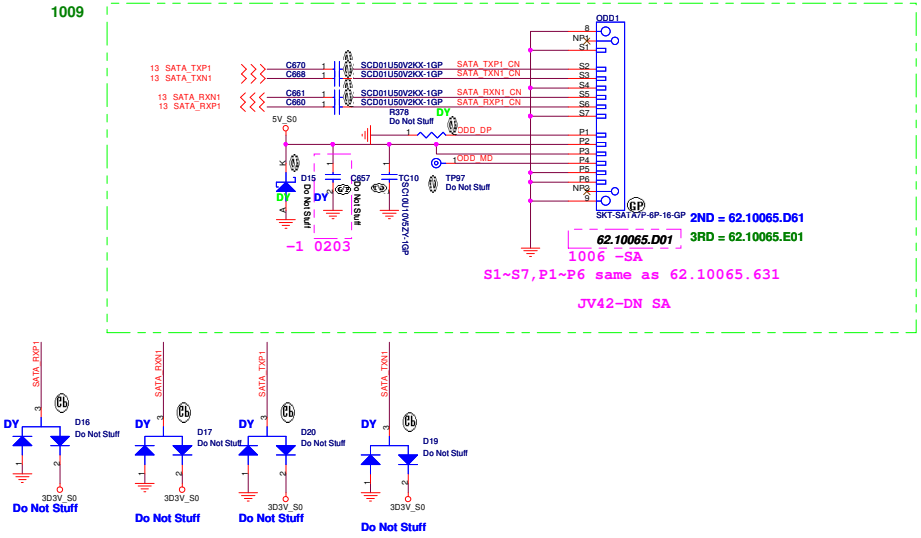




Diserete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD	
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 22 of 63	

ODD Connector



Diserete Madison Hynix

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Title		
ODD		
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Date: Friday, March 26, 2010	Sheet 23 of 63	

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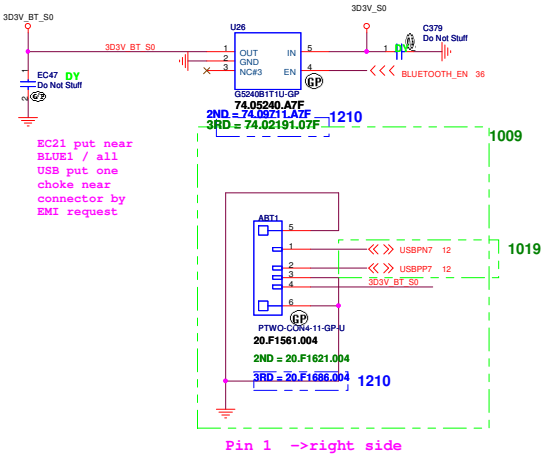
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**BLUETOOTH**	
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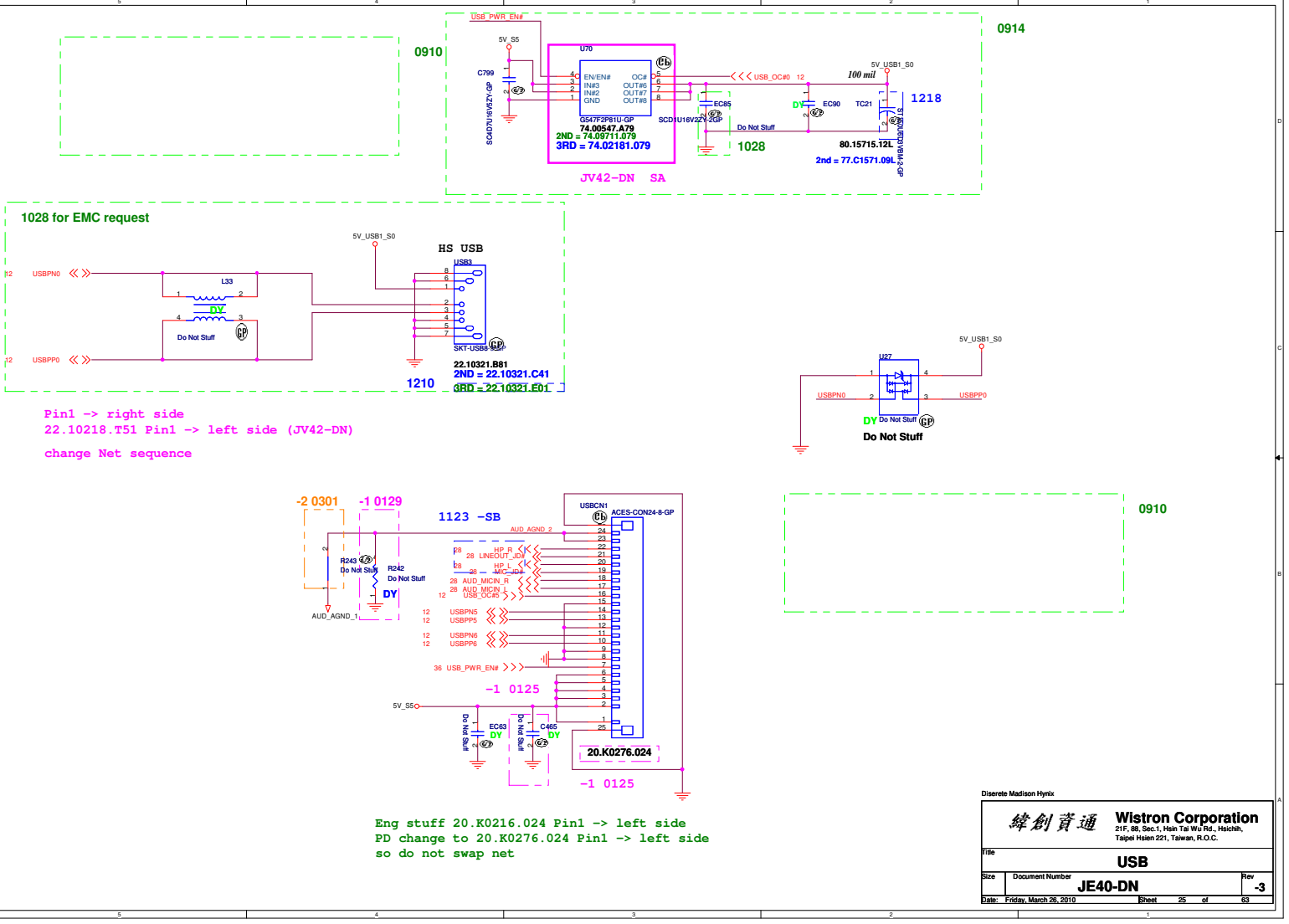

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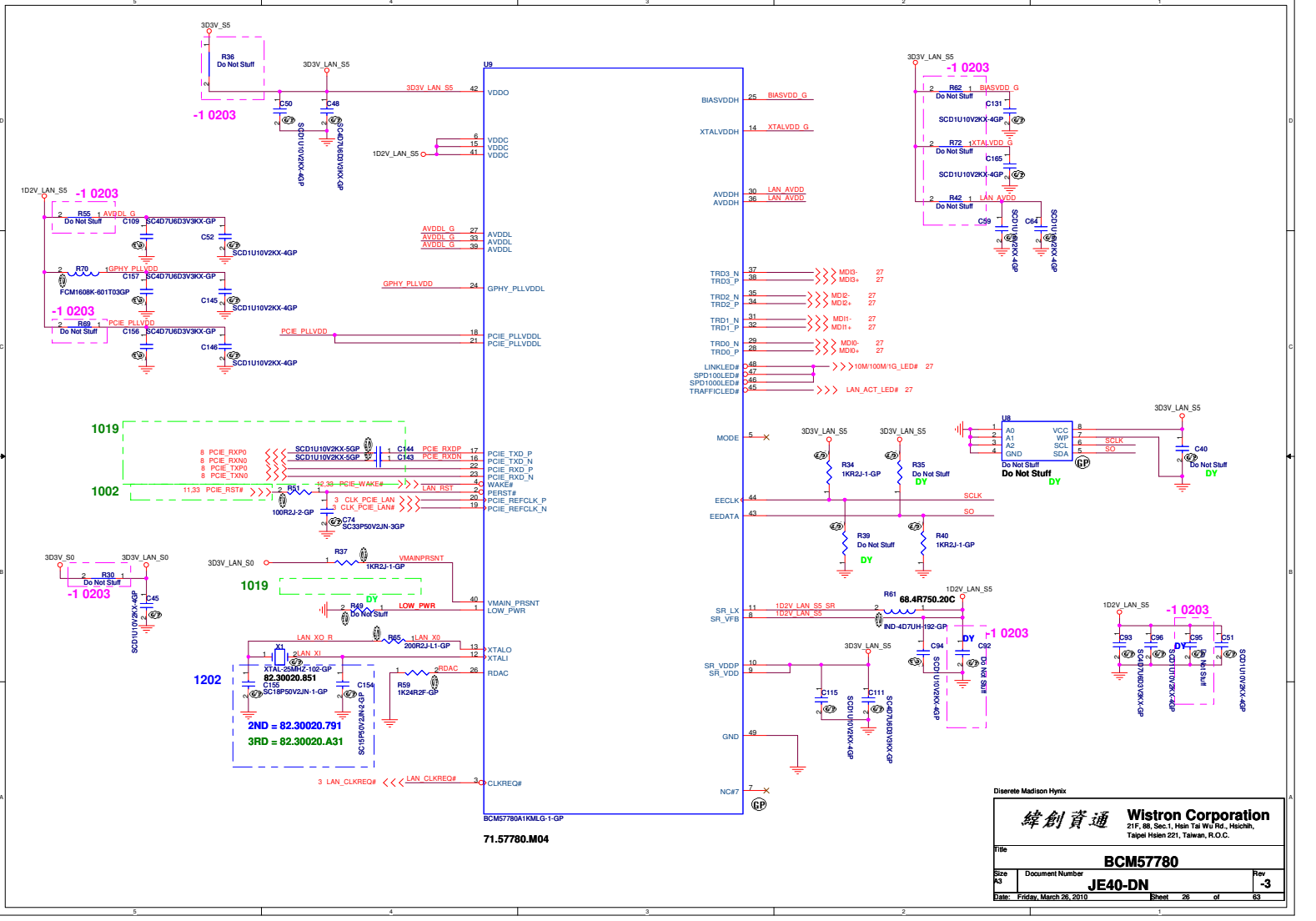

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **BCM57780**

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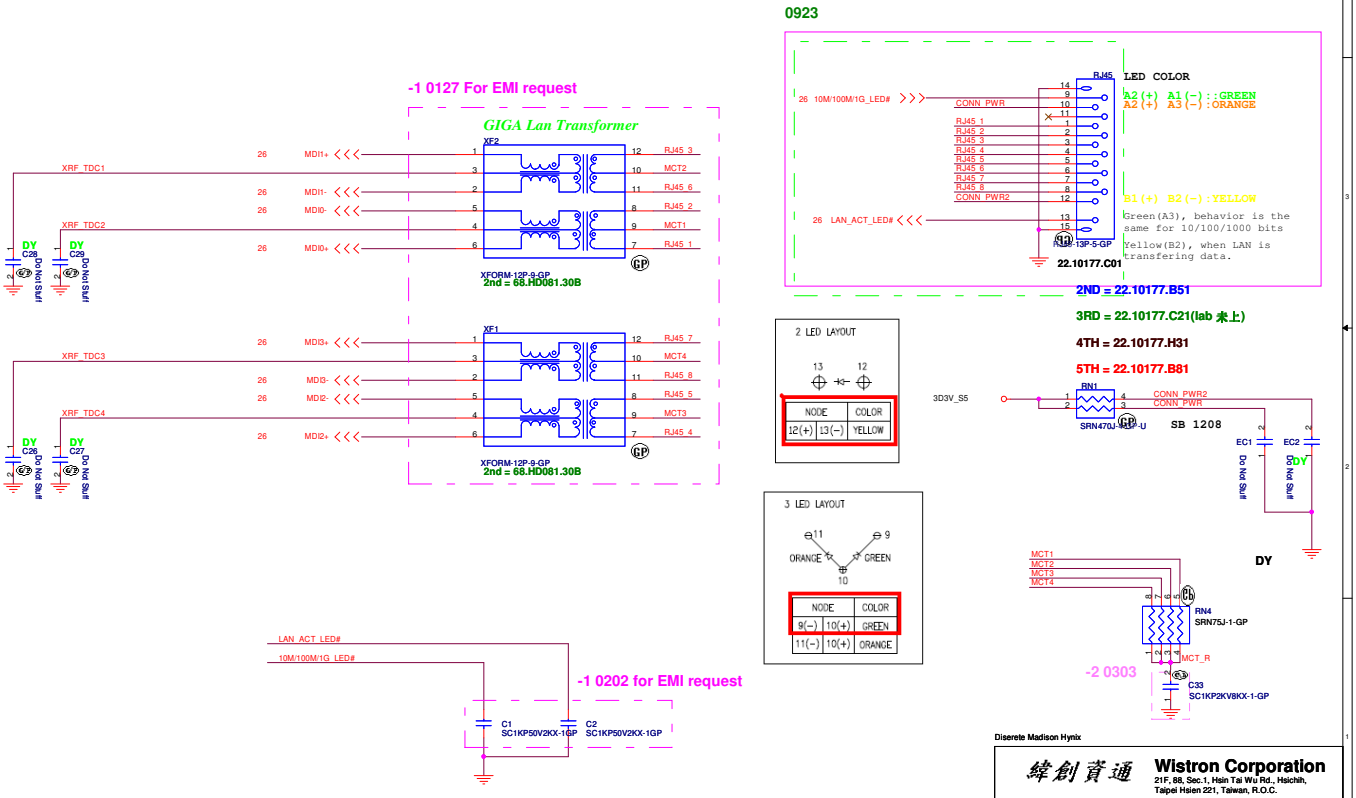
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

LAN Connector



Diserete Madison Hynix

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
	LAN CONN	
Size A3	Document Number JE40-DN	Rev -3
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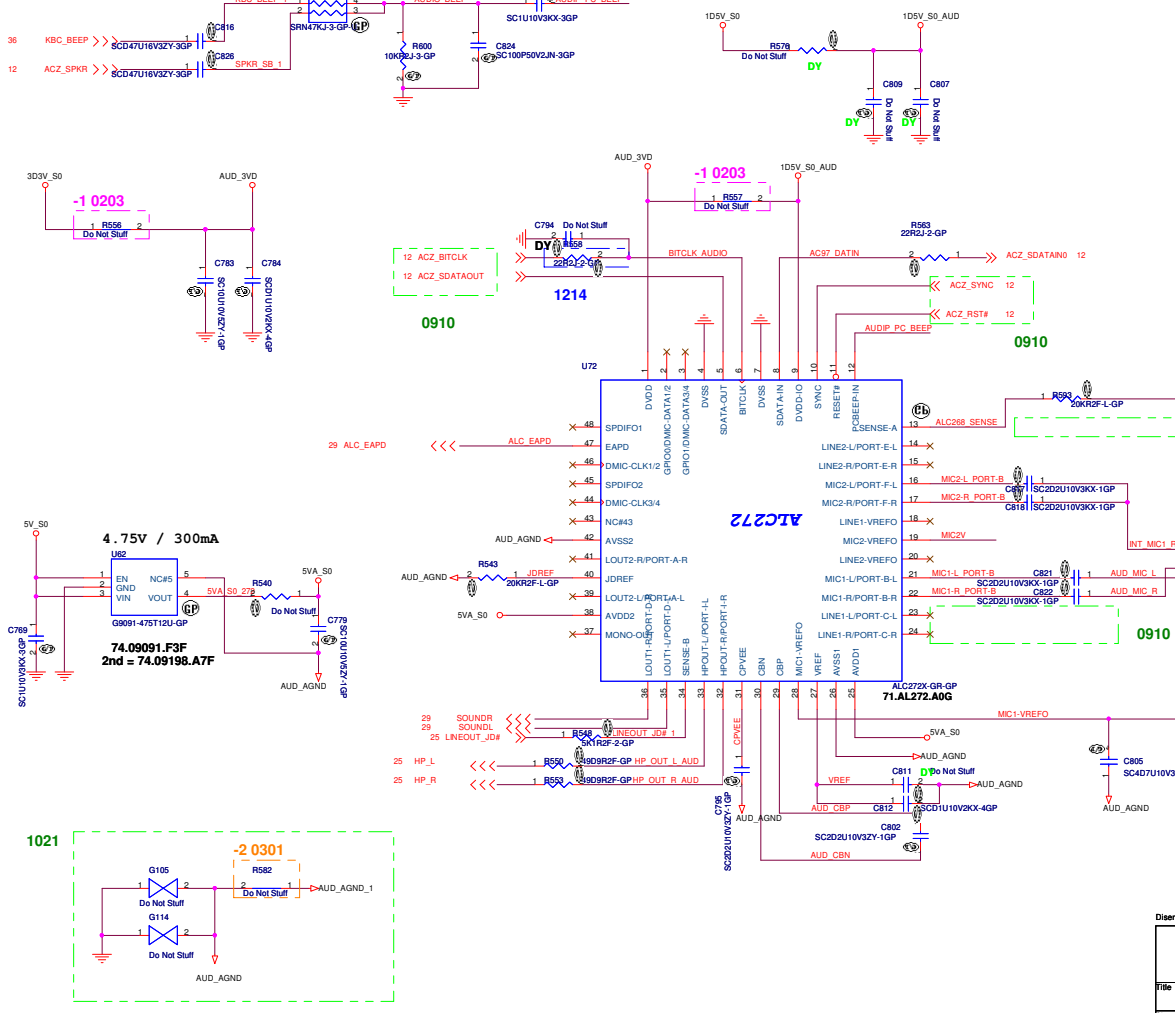

Diserete Madison Hynix

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC272**

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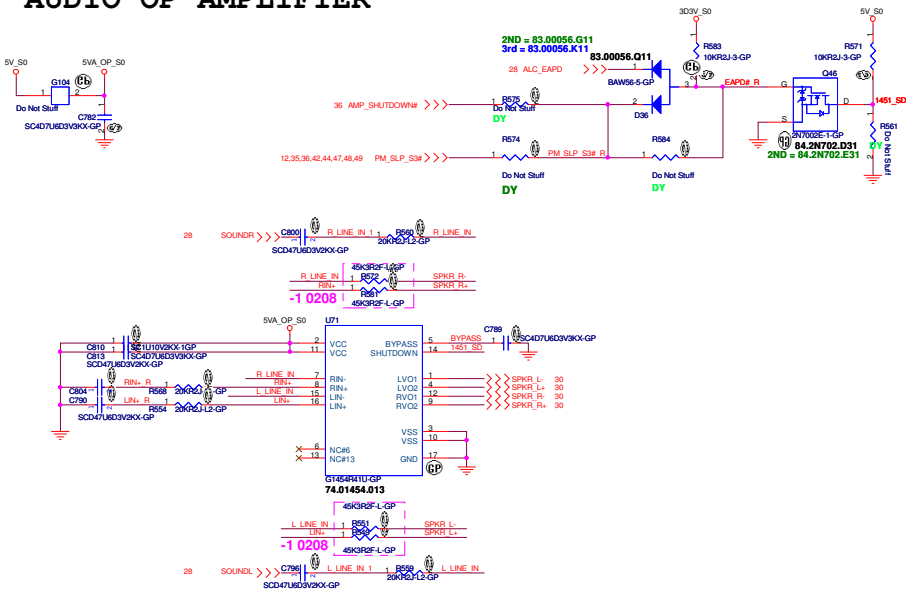
AUDIO OP AMPLIFIER




```
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If  VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W
```

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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO AMP	
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Date: Friday, March 26, 2010	Sheet 29 of 63	

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Internal Speaker

0914

0910

29 SPKR_L-
29 SPKR_L+
29 SPKR_R-
29 SPKR_R+

SPKR_L-
SPKR_L+
SPKR_R-
SPKR_R+

EC15 EC14 EC13 EC12

AZ20125.01H-GP-U
83.02025.0AF

-1 0125 for EMI request

SPKR1

SPKR_L+
SPKR_L-
SPKR_R+
SPKR_R-

PTWO-CON4-11-GP-U
20.F1561.004
2ND = 20.F1621.004
3RD = 20.F1686.004
1210

Plin 1- > right side

JV42-DN SA

0910

LINE OUT

0911

1016

Internal Mic

AAMIC1

28 INT_MIC1

L59
MLVS0603K20-GP

PTWO-CON2-6-GP
20.F1561.002
2ND = 20.F1621.002
3RD = 20.F1686.002
1210

-1 0209 For MIC issue

JV42-DN PX
Pin 1- >right side
20.F1240.002 Pin1->left side

same as JV70-CP

Diserete Madison Hynix

緯創資通 **Wistron Corporation**
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Title: **AUDIO JACK**

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No Modem Function

Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**MDC**
Size / Document Number	**JE40-DN**
Rev	-3
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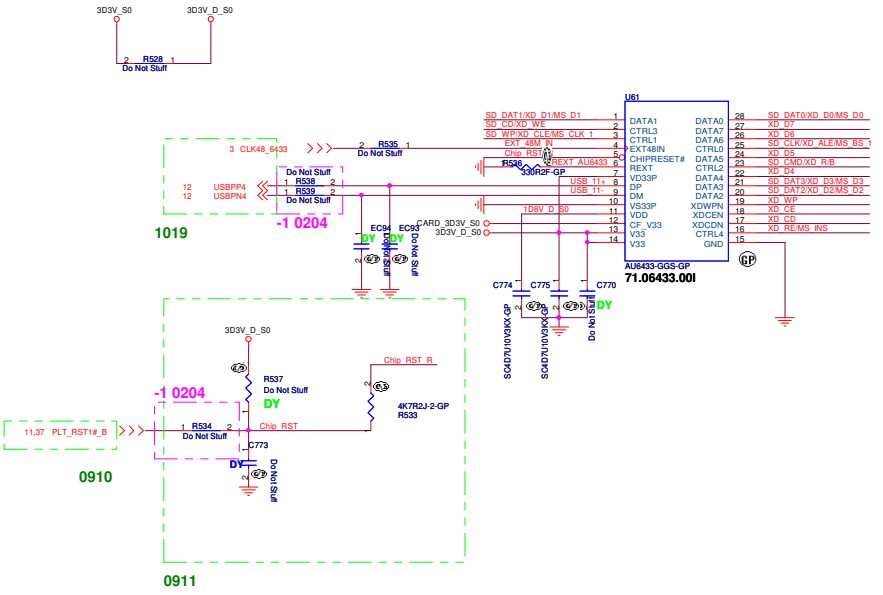
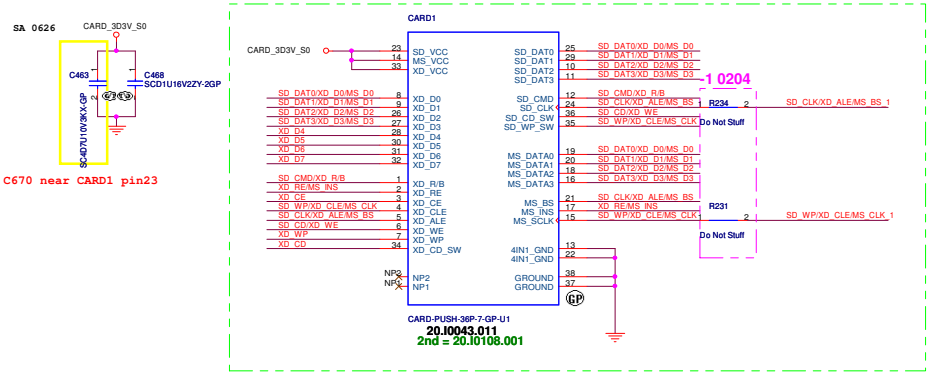
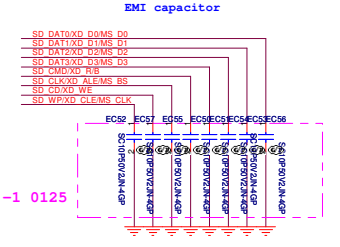


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)





Diserete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CARDREADER	
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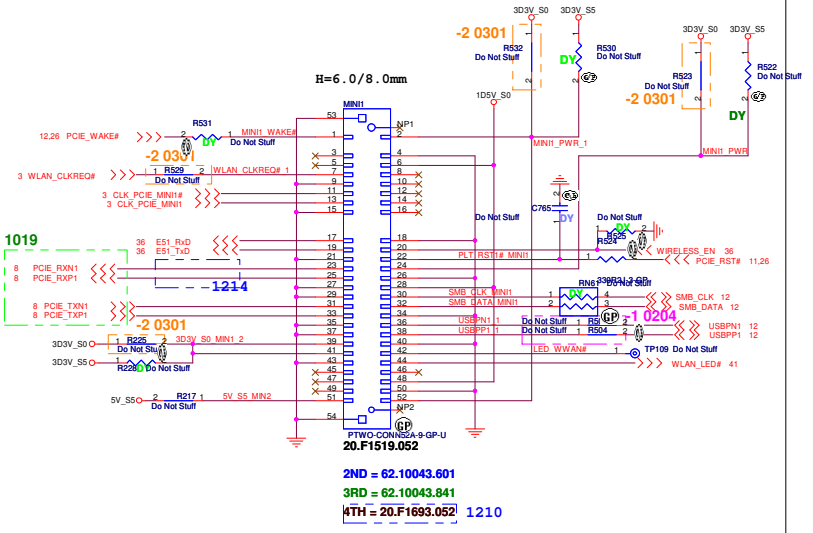
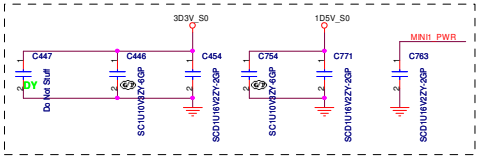
Mini Card Connector(WLAN)

0923



Place near MINI1



No Mini Card Function (Robson2 and 3G)

Diserete Madison Hynix

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Title	MINI CARD	
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No NEWCARD Function

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Taipei Hsien 221, Taiwan, R.O.C.

Title	NEW CARD	
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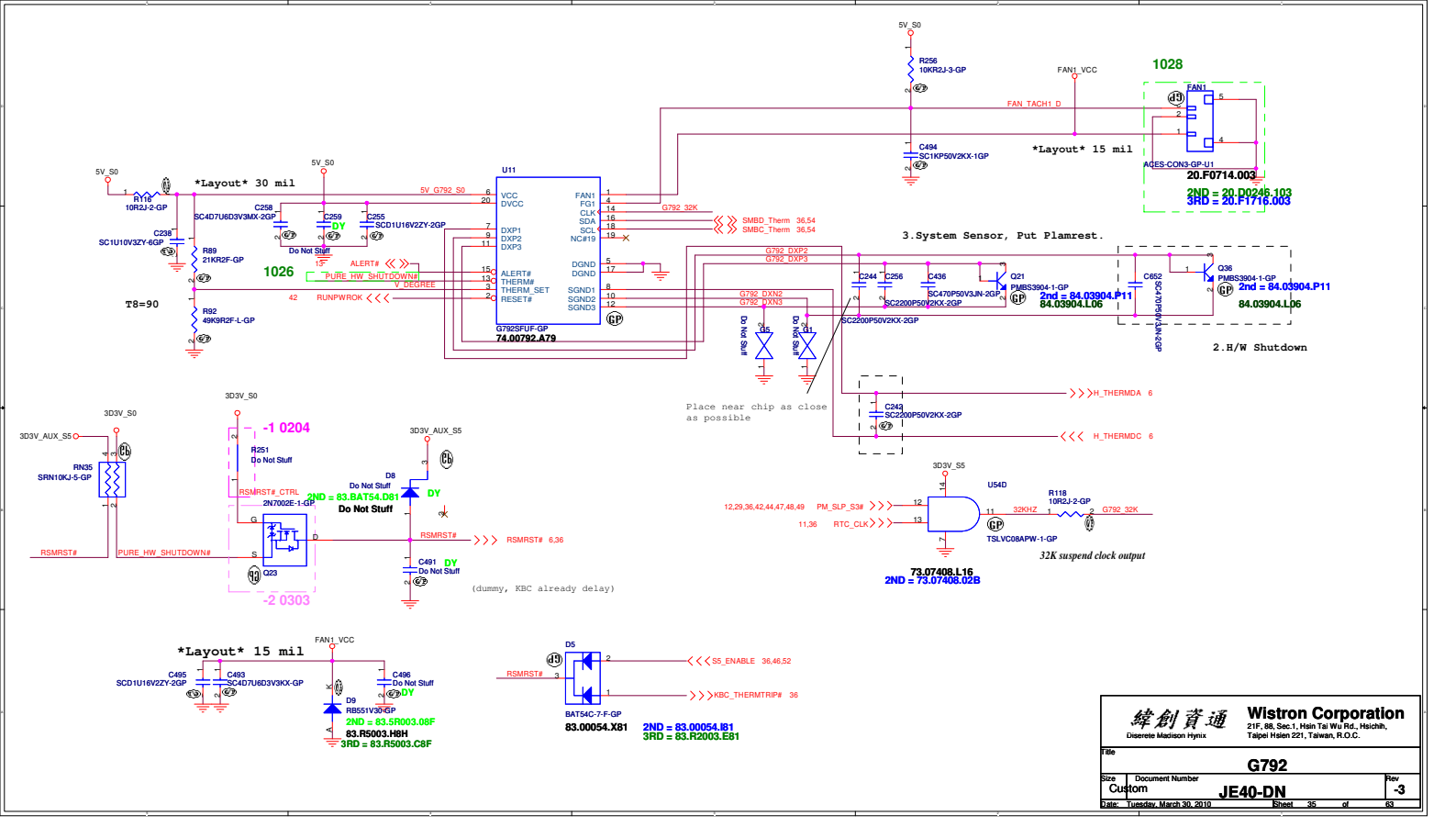

緯創資通
Diserete Madison Hynix

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: G792

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Custom	JE40-DN	-3

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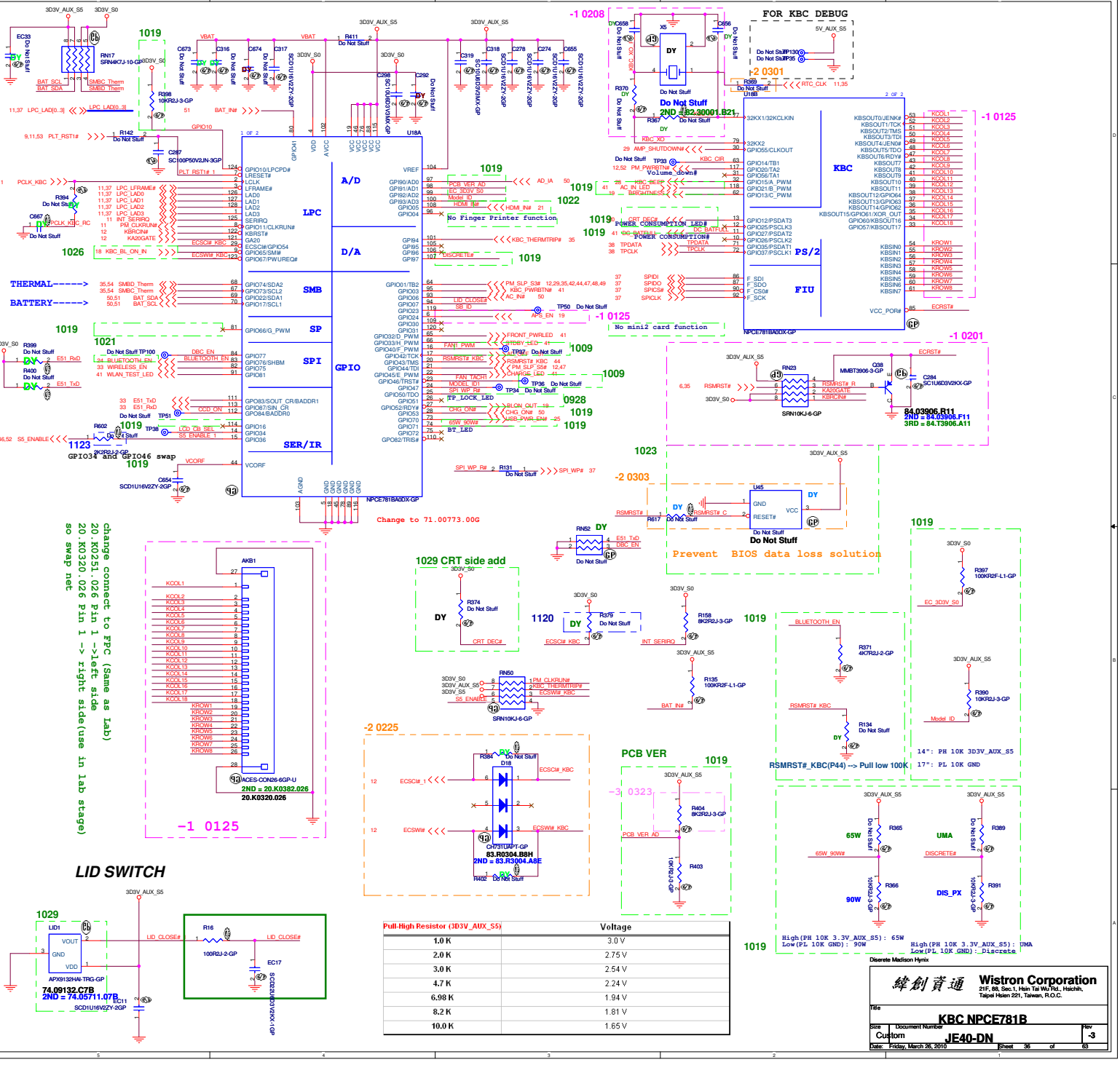
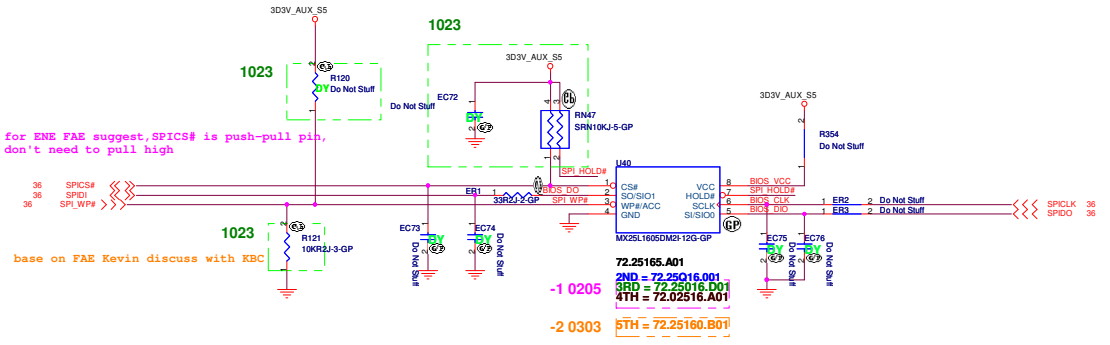


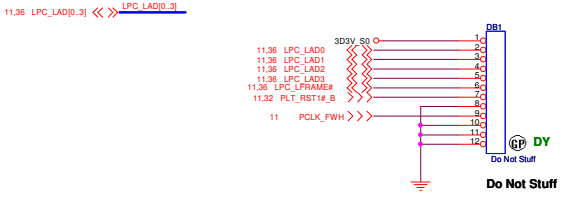
Pull-High Resistor (3D3V_AUX_S5)	Voltage
1.0 K	3.0 V
2.0 K	2.75 V
3.0 K	2.54 V
4.7 K	2.24 V
6.98 K	1.94 V
8.2 K	1.81 V
10.0 K	1.65 V



3rd 4th source LAB ENG未上

16M Bits
SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



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Title	BIOS	
Size A3	Document Number JE40-DN	Rev -3
Date: Friday, March 26, 2010	Sheet 37 of 63	

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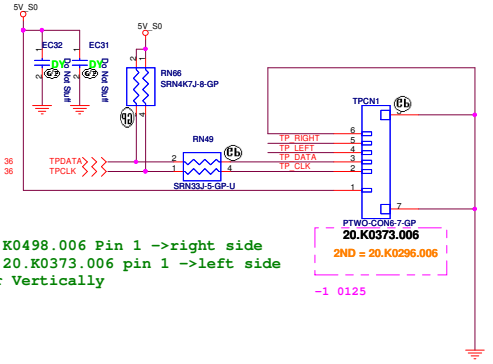
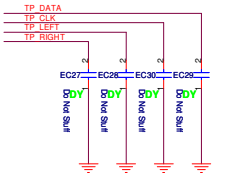
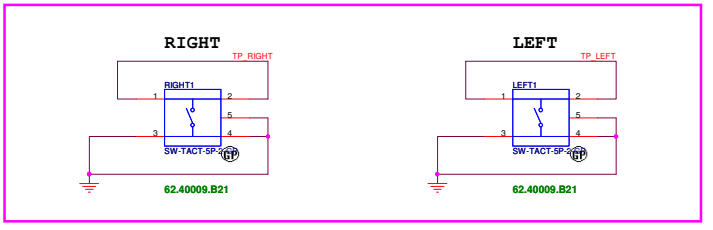


Eng stuff 20.K0498.006 Pin 1 ->right side
PD change to 20.K0373.006 pin 1 ->left side
so net mirror Vertically



-1 0205



No Finger printer Function

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Touch PAD**

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NONE BOARD

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	NONE BOARD	
Size A3	Document Number JE40-DN	Rev -3
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緯創資通 Wistron Corporation
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Title	SWITCH	
Size: A2	Document Number: JE40-DN	Rev: -3
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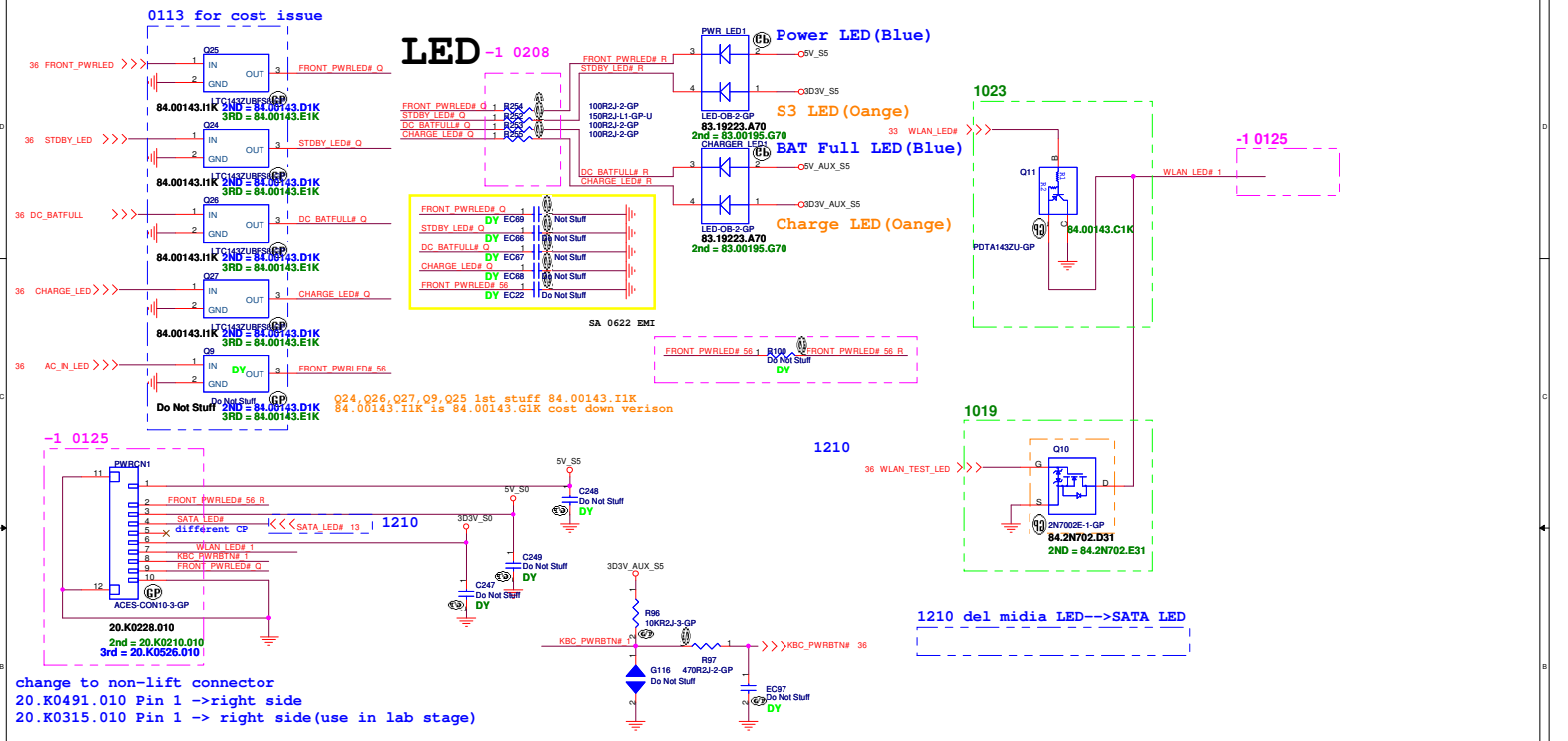

Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	SATA_LED#	HDD
Pin 5	NA	
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LED**

Size: A3 | Document Number: **JE40-DN** | Rev: -3

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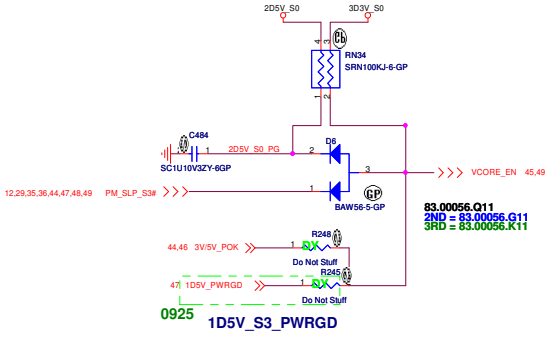
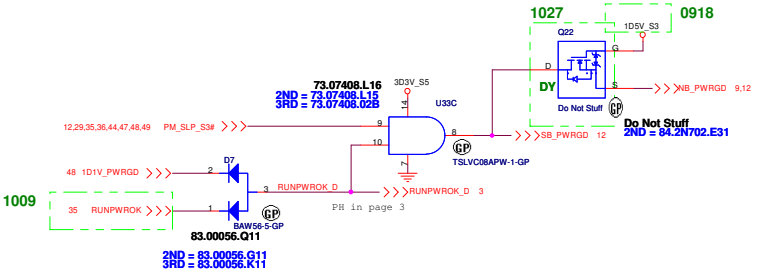


P/H @ 1D8V_S3 PAGE



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**POWER ON LOGIC**	
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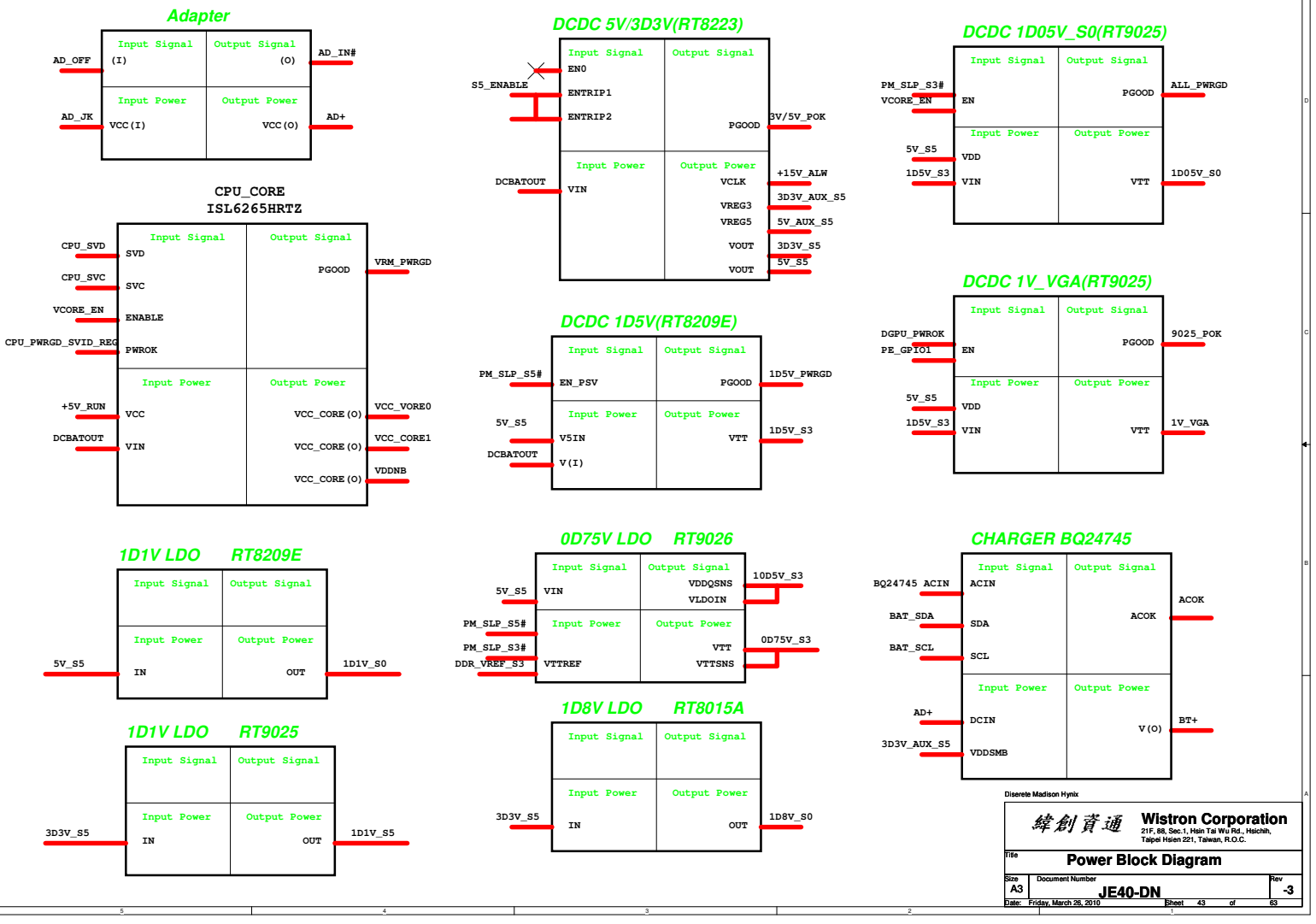

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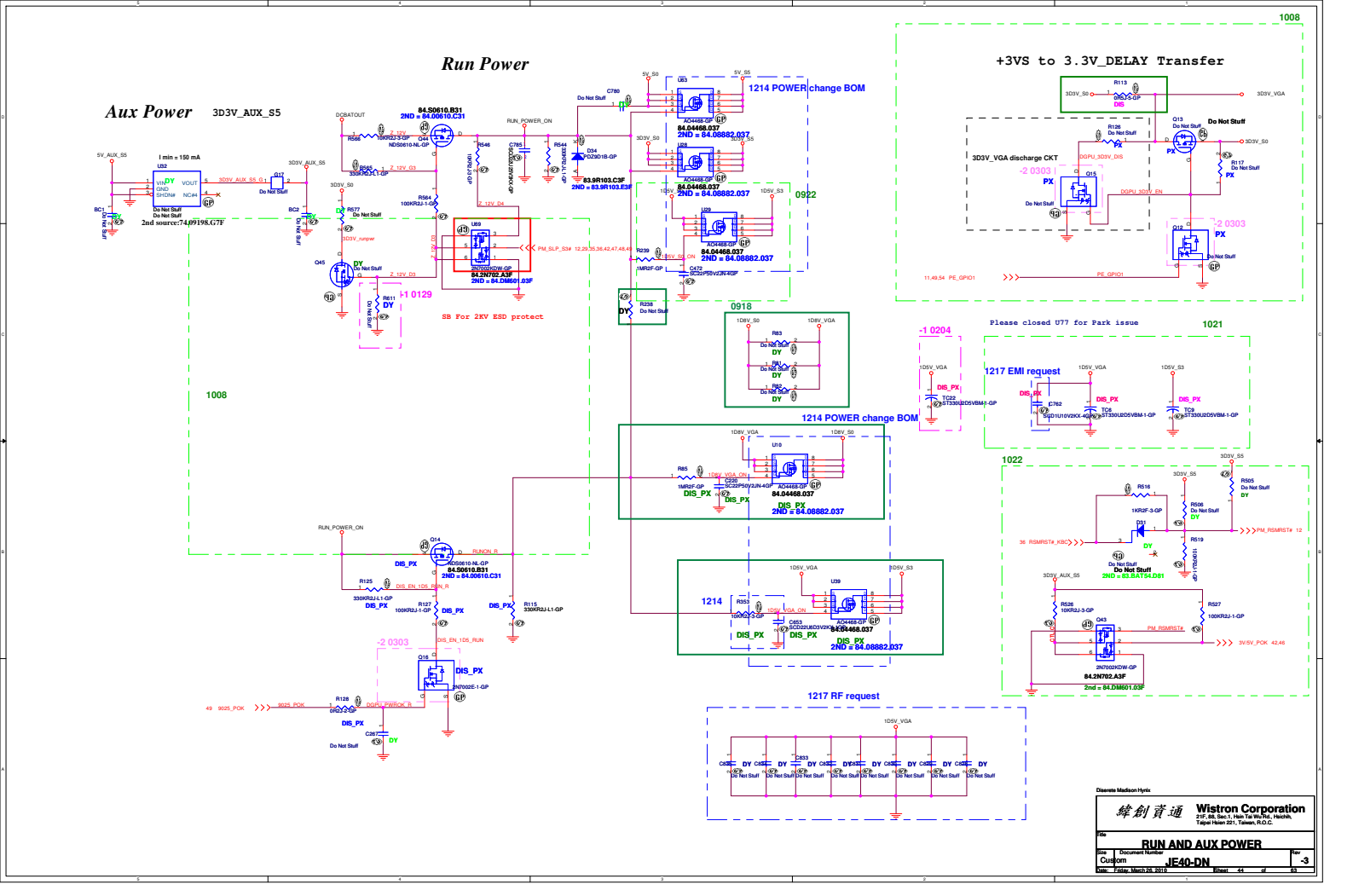
Run Power
Aux Power
3D3V_AUX_S5
+3VS to 3.3V_DELAY Transfer
1008
1214 POWER change BOM
0922
0918
1021
1022
1214
1217 EMI request
1217 RF request
SB For 2KV ESD protect
Please closed U77 for Park issue
3D3V_VGA discharge CKT
I min = 150 mA
2nd source:74.09198.G7F
84.S0610.B31
2ND = 84.00610.C31
84.04468.037
2ND = 84.08882.037
83.9R103.C3F
2ND = 83.9R103.E3F
84.2N702.A3F
2ND = 84.DM601.03F
84.2N702.A3F
2nd = 84.DM601.03F
2ND = 83.BAT54.D81
-1 0129
-1 0204
-2 0303
DIS_PX
DY
PX
Do Not Stuff
Discrete Madison Hynix
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
RUN AND AUX POWER
Size
Custom
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Date: Friday, March 26, 2010
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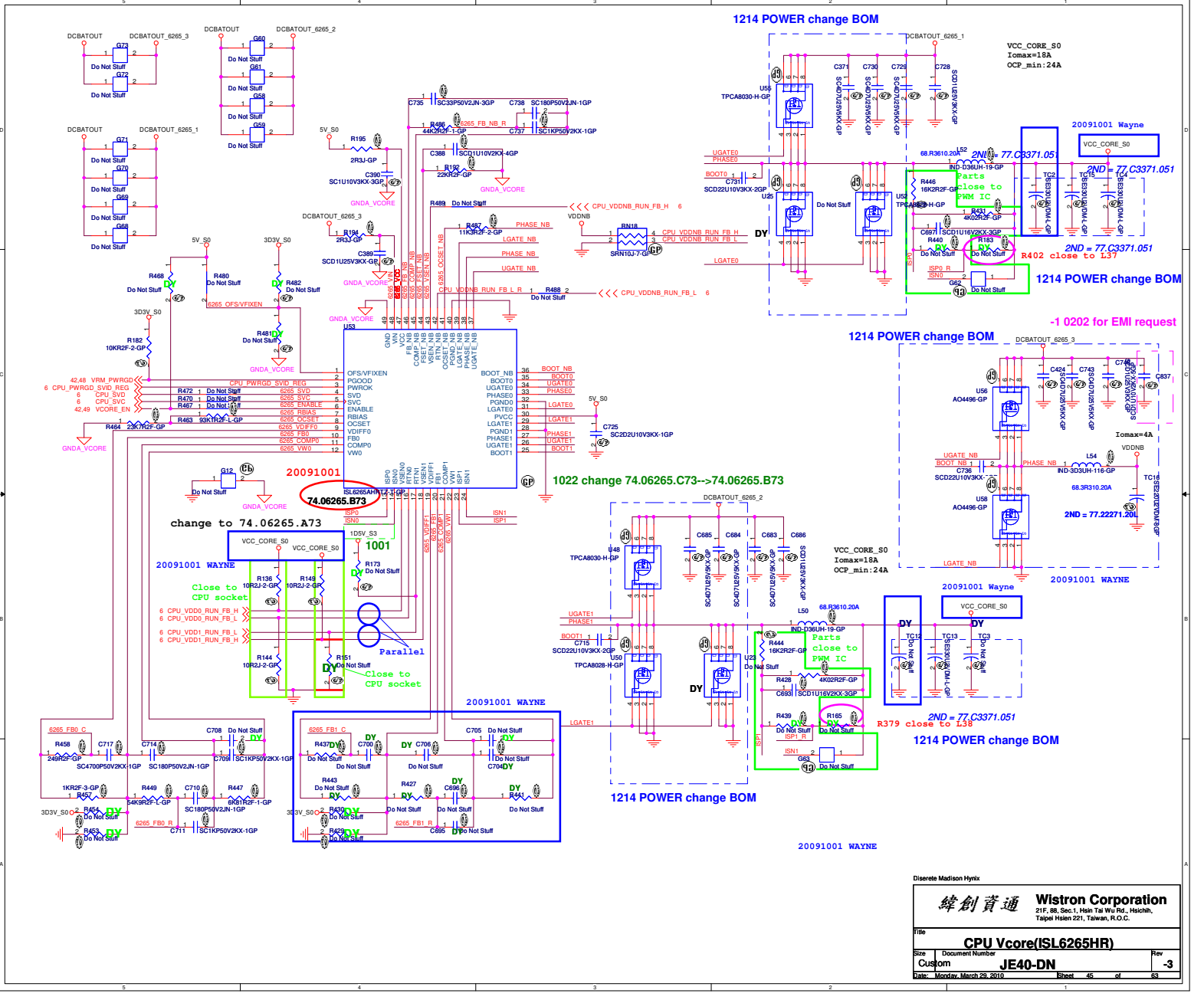

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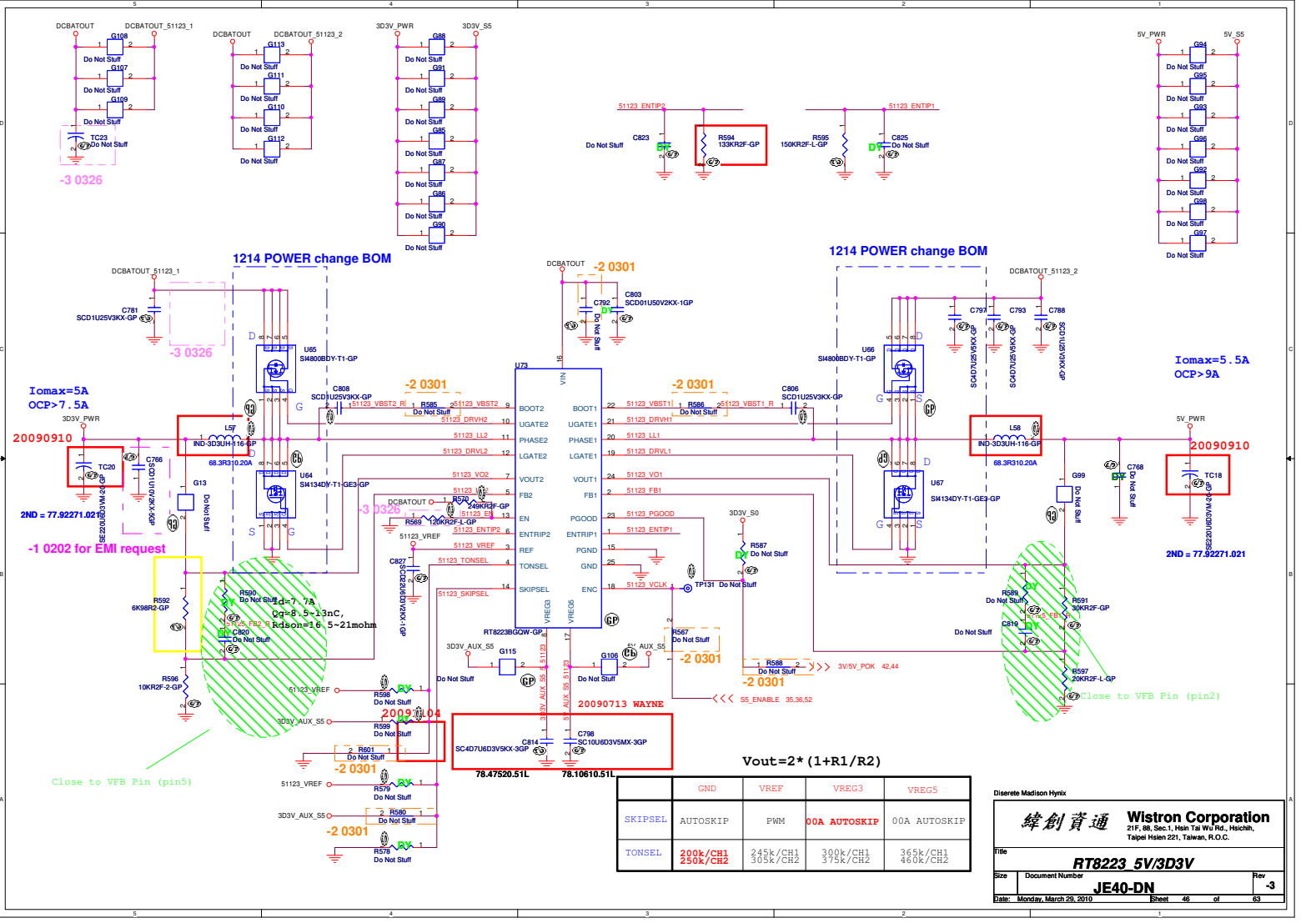
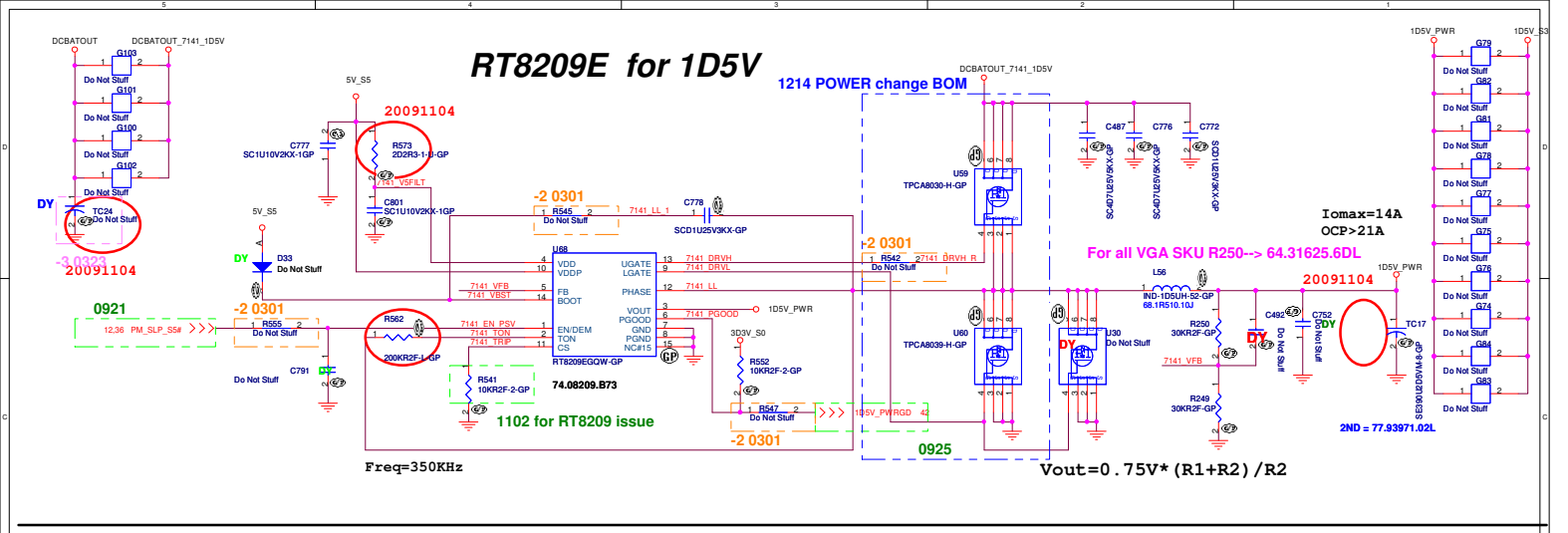
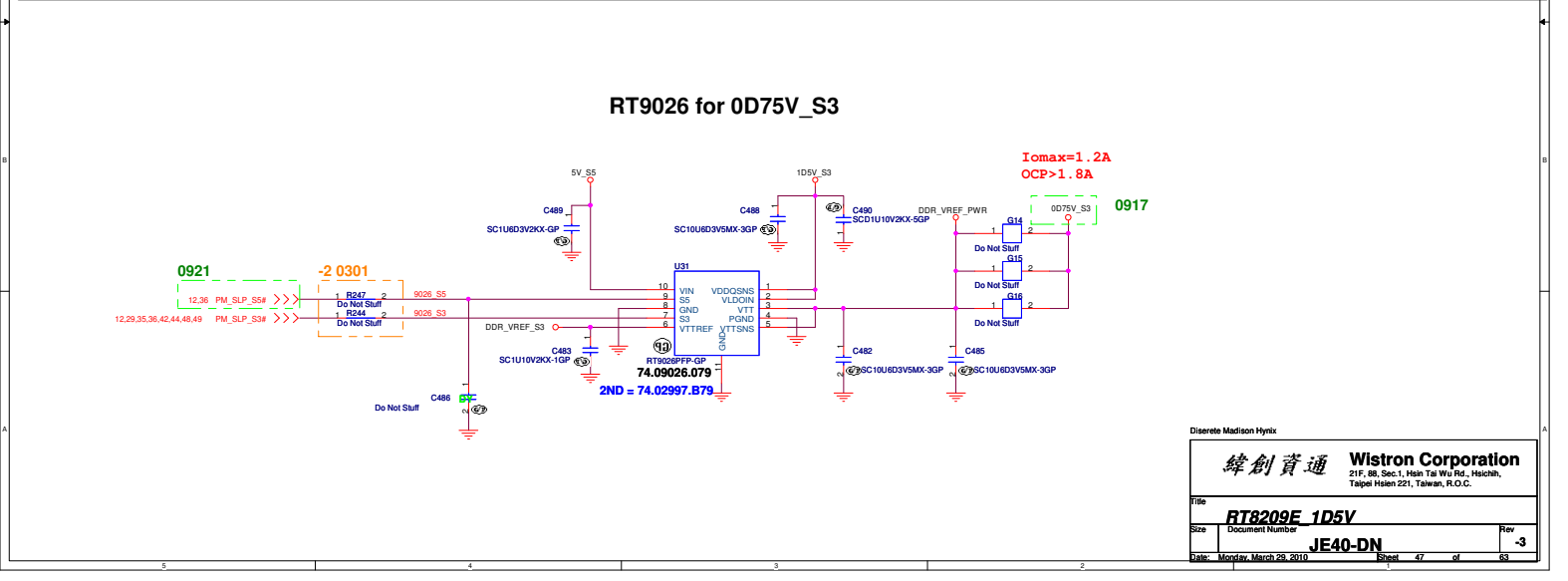


	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2





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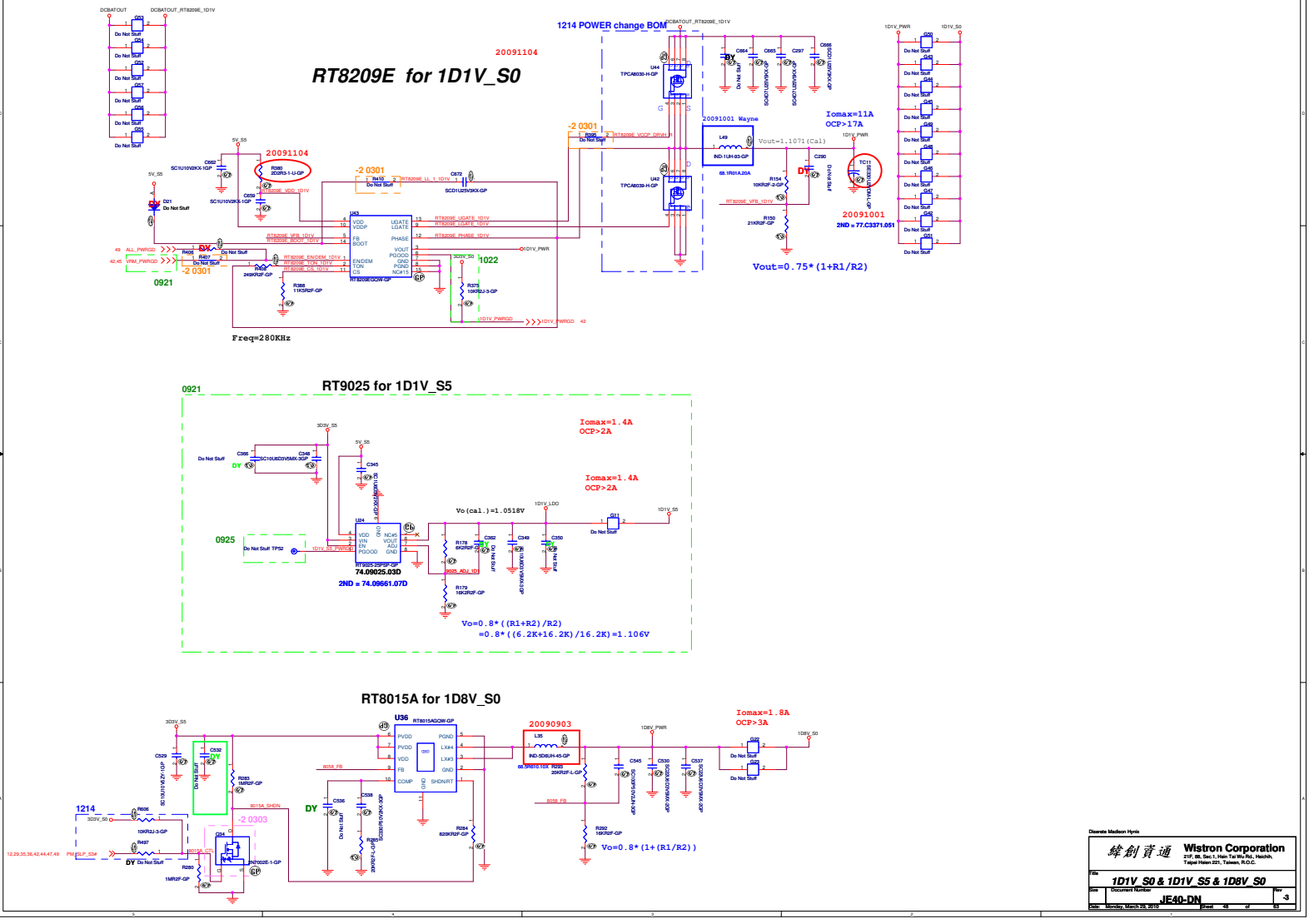
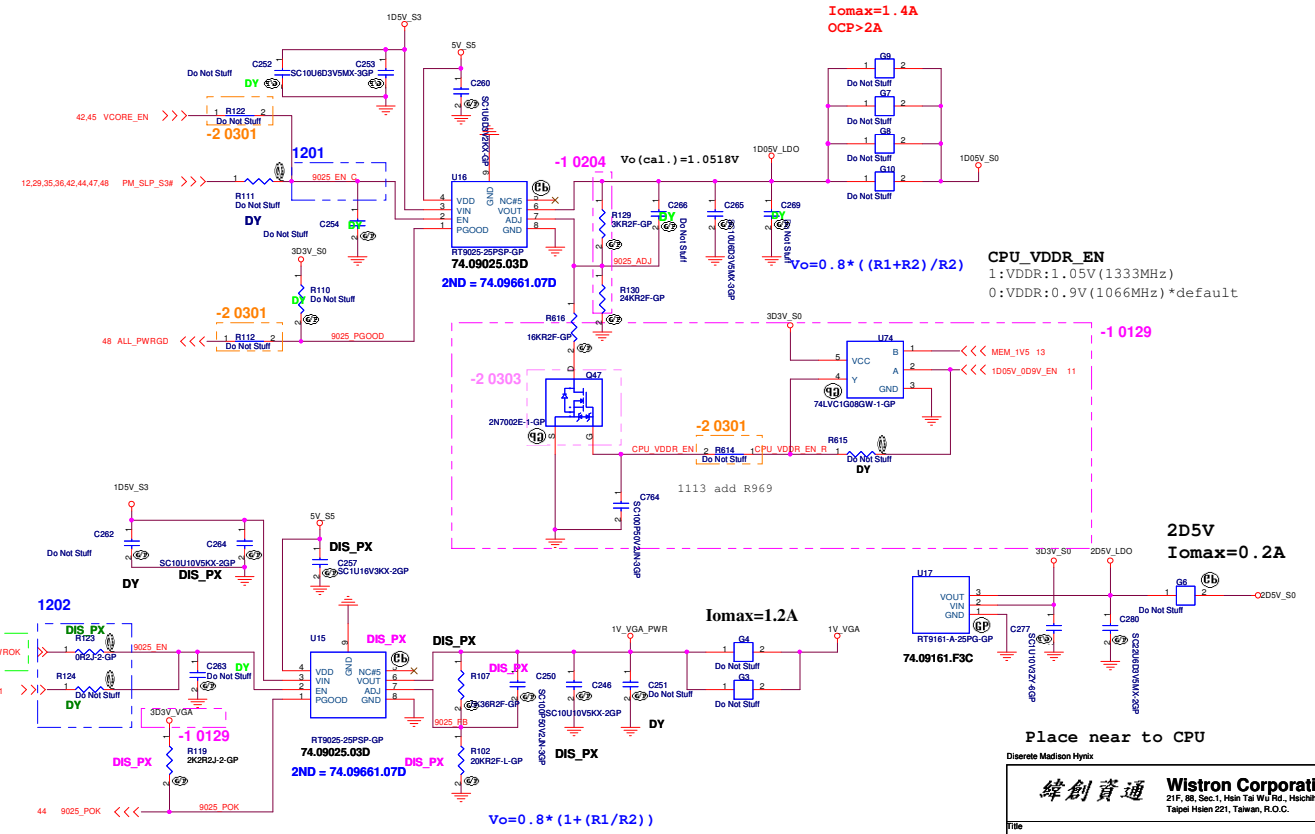

RT8209E for 1D1V_S0
20091104
1214 POWER change BOM
Iomax=11A
OCP>17A
Vout=0.75*(1+R1/R2)
Freq=280KHz
0921
1022
RT9025 for 1D1V_S5
Iomax=1.4A
OCP>2A
Vo(cal.)=1.0518V
Vo=0.8*((R1+R2)/R2)
=0.8*((6.2K+16.2K)/16.2K)=1.106V
2ND = 74.09661.07D
74.09025.03D
0925
RT8015A for 1D8V_S0
Iomax=1.8A
OCP>3A
20090903
Vo=0.8*(1+(R1/R2))
1214
-2 0303
Wistron Corporation
1D1V_S0 & 1D1V_S5 & 1D8V_S0
JE40-DN
Monday, March 29, 2010

RT9025 for 1D05V_S0



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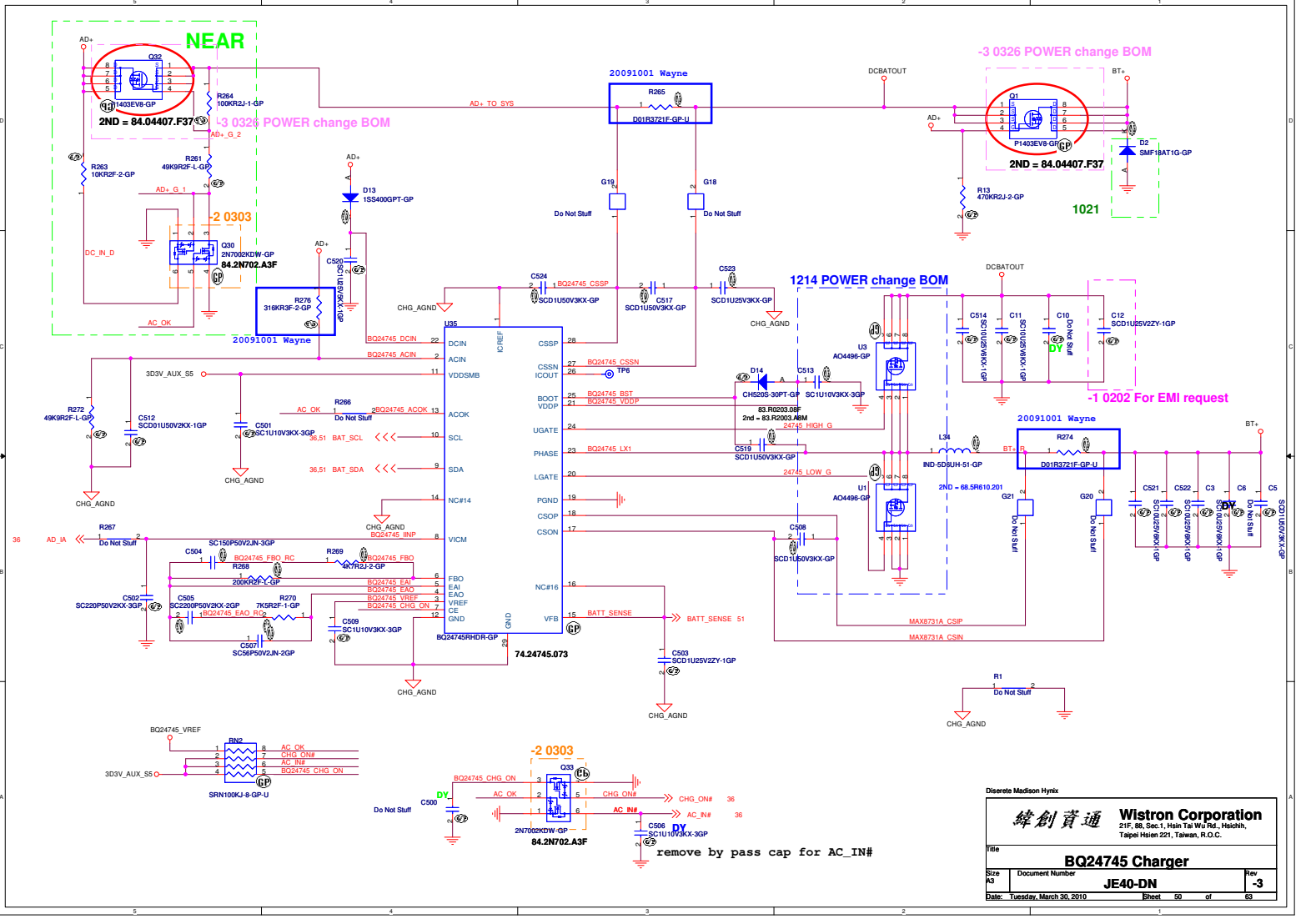

Diserete Madison Hynix

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BQ24745 Charger

Size	Document Number	Rev
A3	JE40-DN	-3

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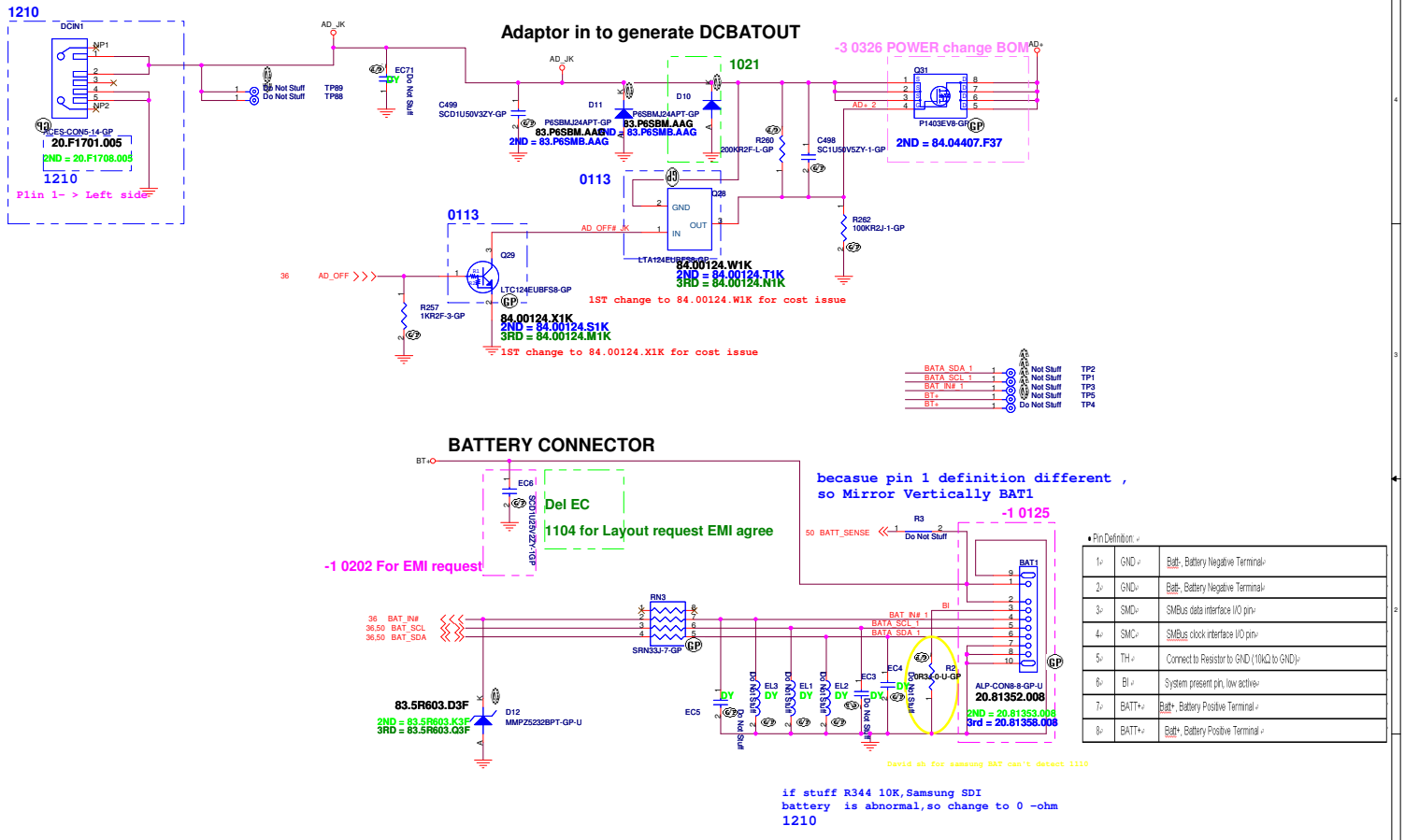

• Pin Definition:

1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

Diserete Madison Hynix

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

Size | Document Number: JE40-DN | Rev: -3

Date: Friday, March 26, 2010 | Sheet 51 of 63

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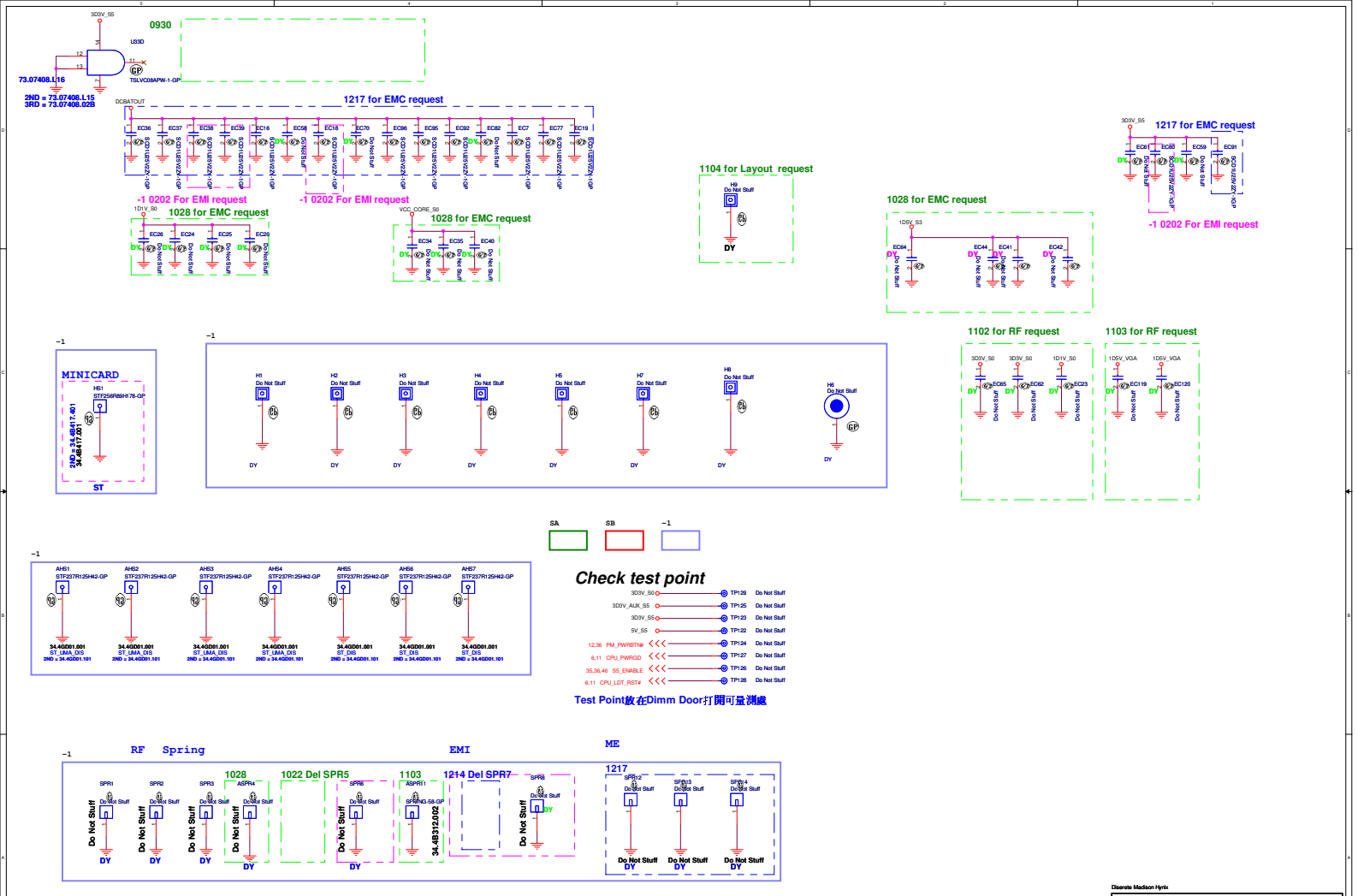

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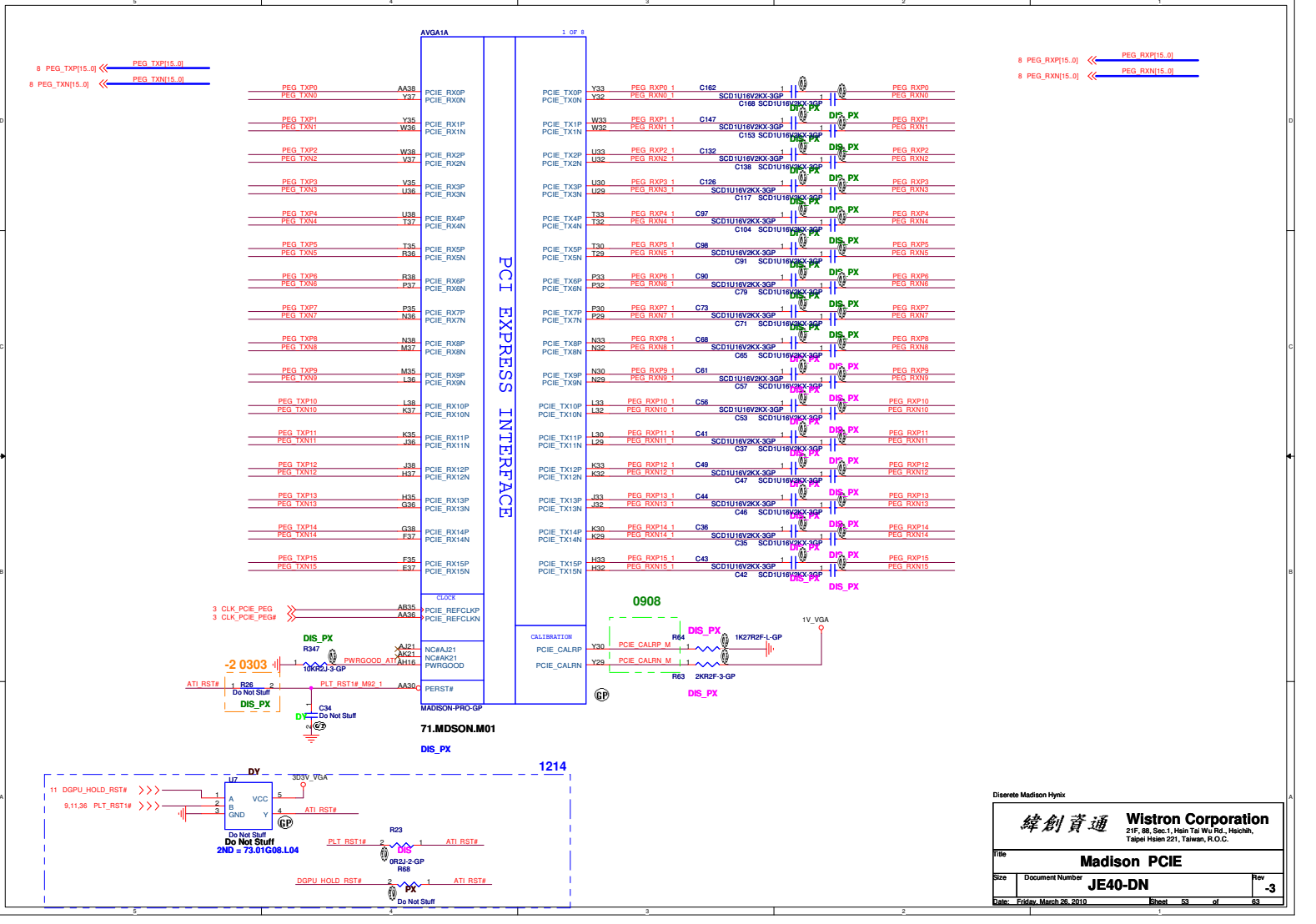
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	EMI/Spring/Boss	
Size	Document Number JE40-DN	Rev -3
Date: Friday, March 26, 2010	Sheet 52 of 63	



Diserete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Madison PCIE	
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 53 of 63	

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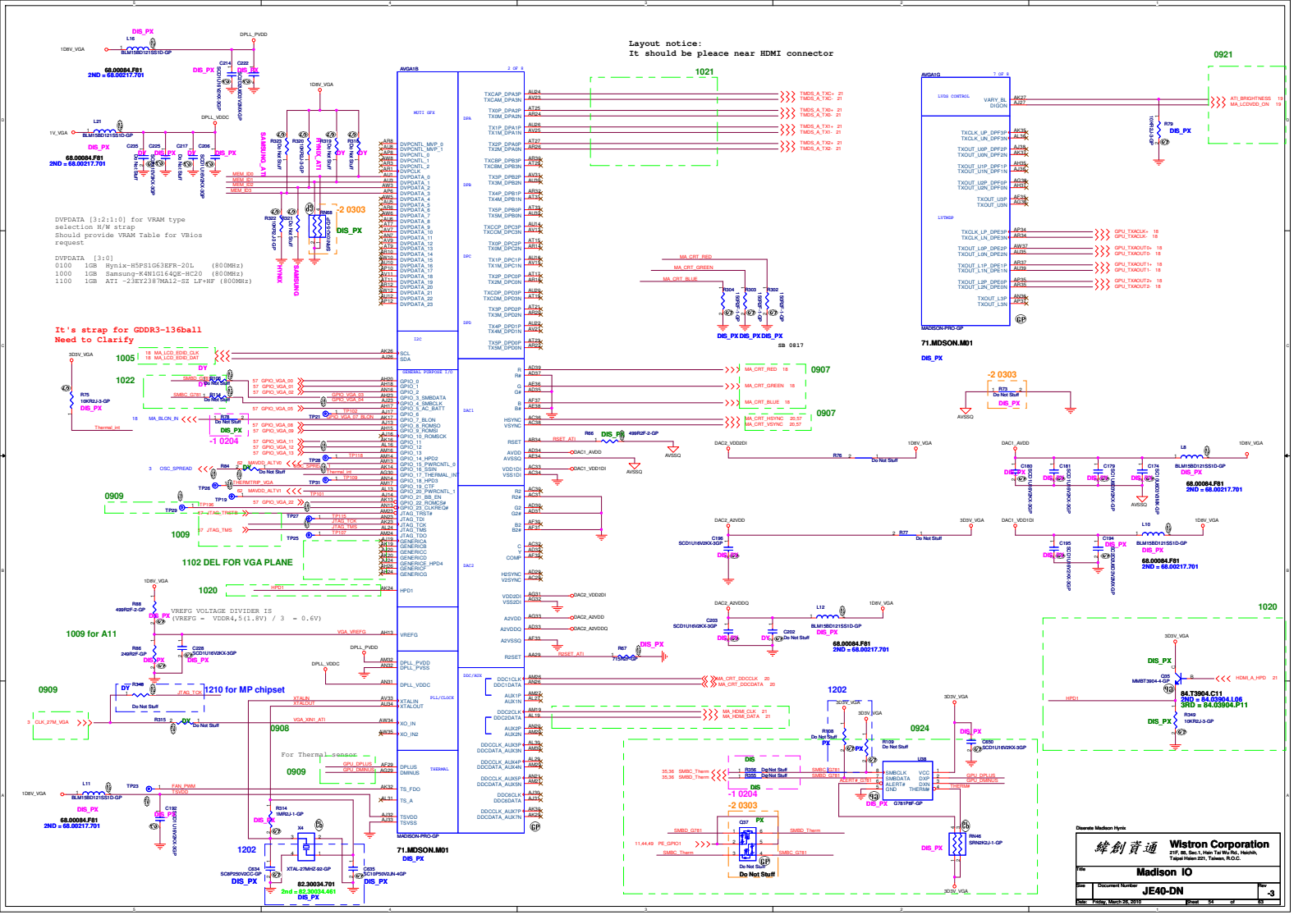
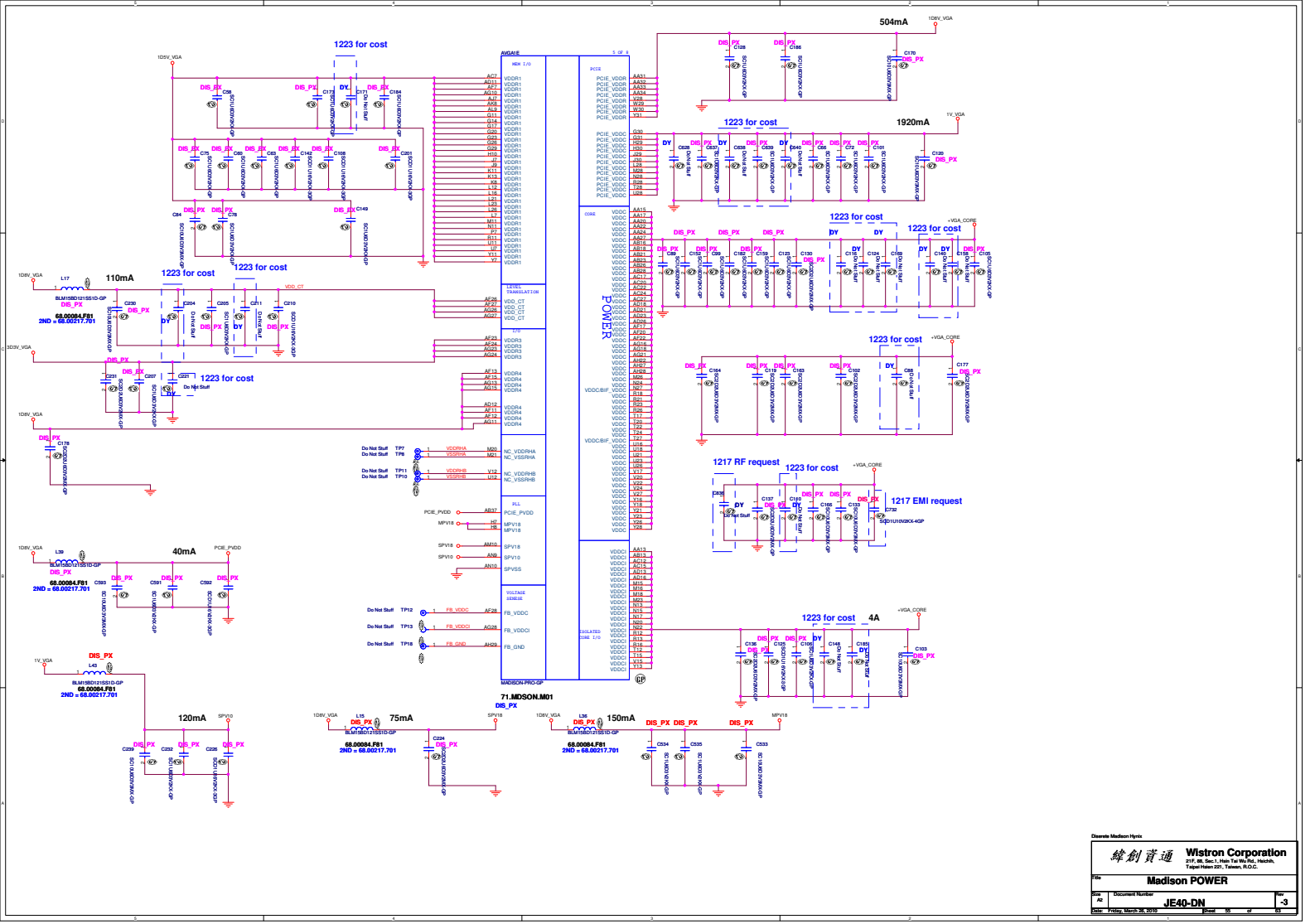

Layout notice:
It should be pleace near HDMI connector
DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0100 1GB Hynix-H5PS1G63EFR-20L (800MHz)
1000 1GB Samsung-K4N1G164QE-HC20 (800MHz)
1100 1GB ATI -23EY2387MA12-SZ LF+HF (800MHz)
It's strap for GDDR3-136ball
Need to Clarify
1102 DEL FOR VGA PLANE
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
1009 for A11
1210 for MP chipset
For Thermal sensor
71.MDSON.M01
Wistron Corporation
Madison IO
JE40-DN
-3



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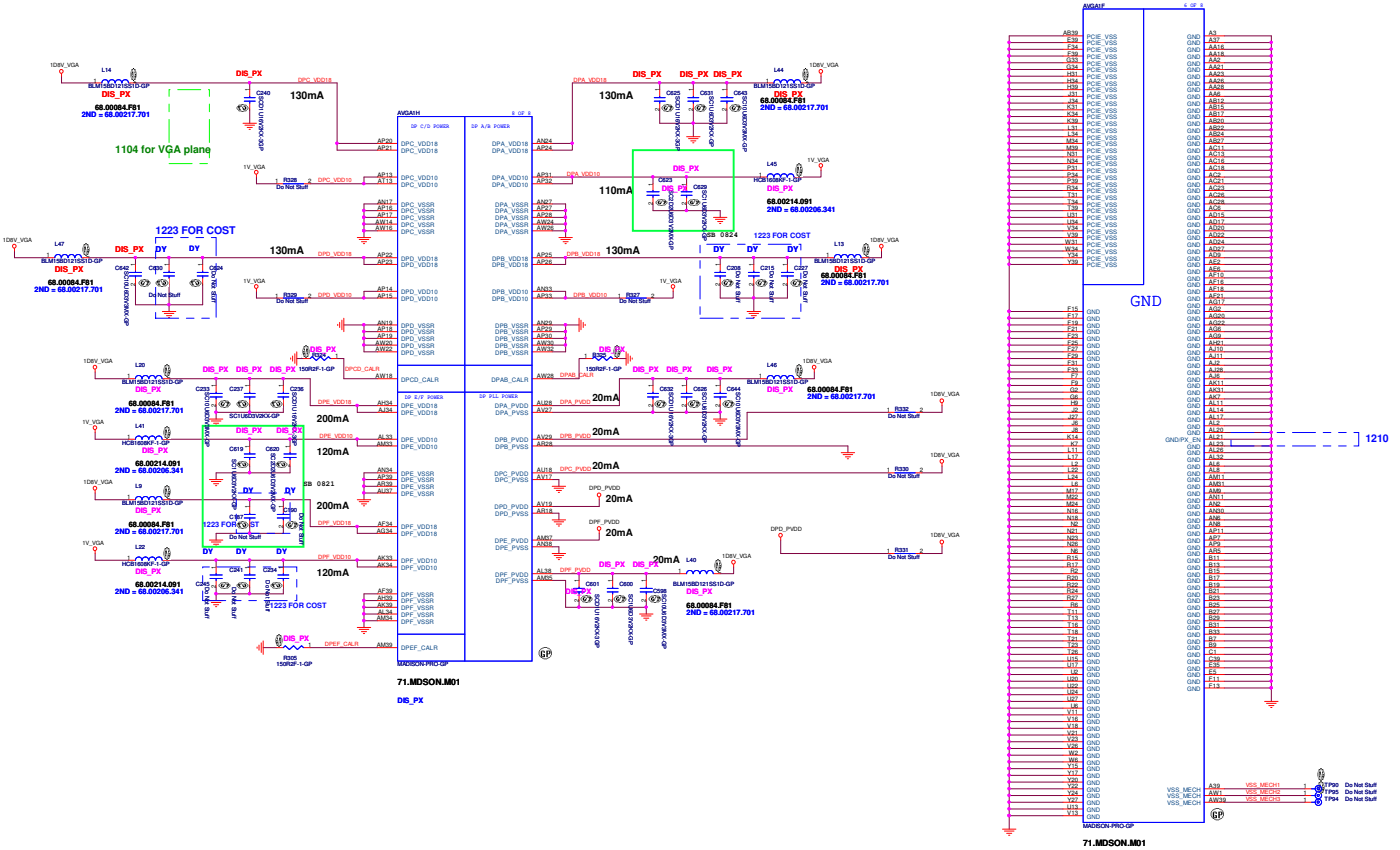
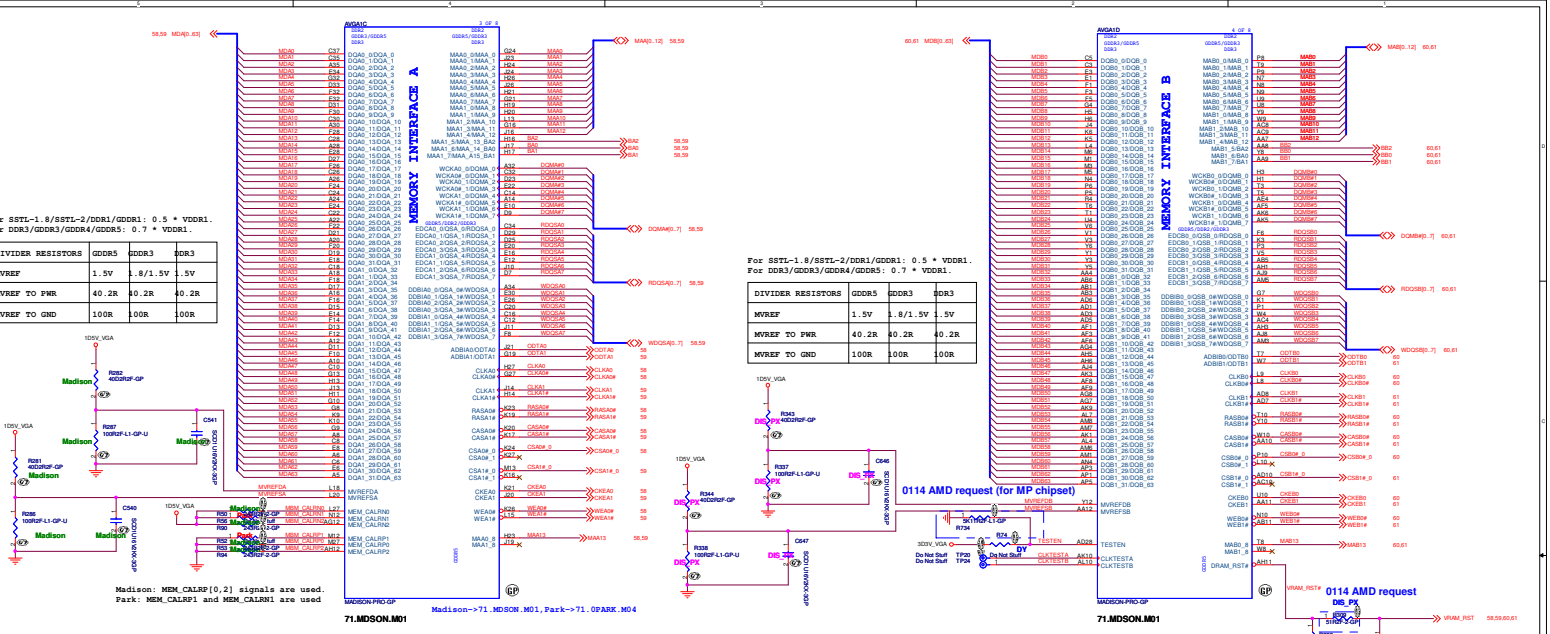


Discrete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DP POWER_GND	
Size: A2	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 56 of 63	



DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

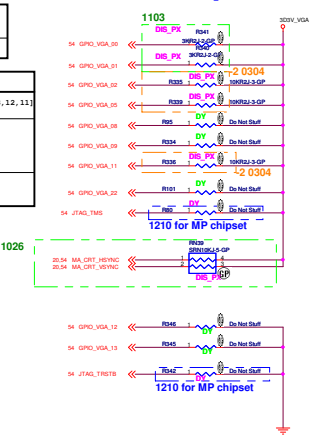
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCE FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory aperture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
V 256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			



Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	51R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

Discrete Madison Hynix

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison Memory / Straps

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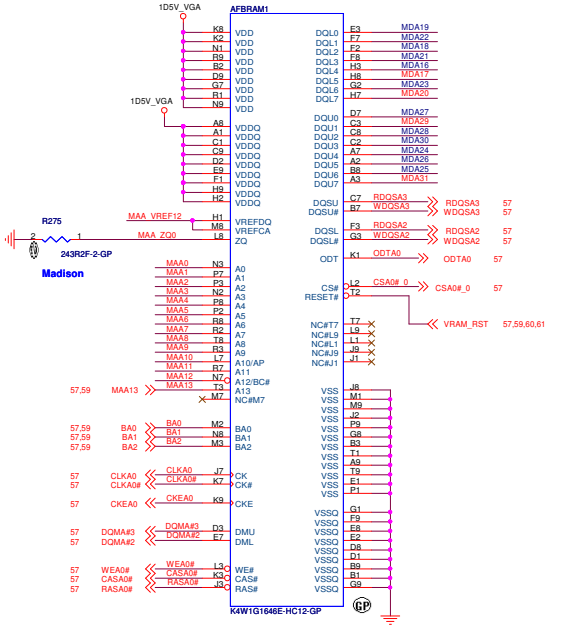
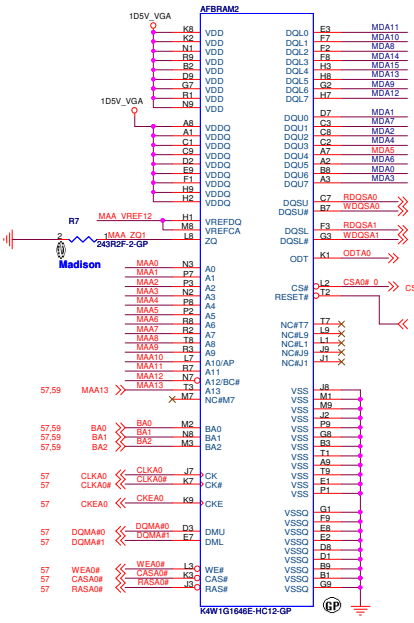
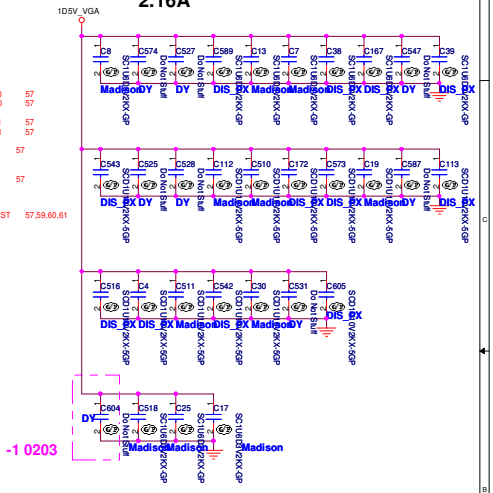
DDR3







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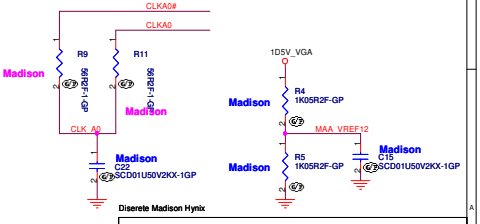
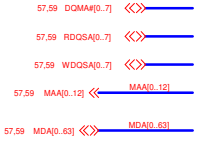
HYNIX: 72.51G63.C0U





緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***VRAM(1/4)***
Size A3 / Document Number	**JE40-DN** / Rev **-3**
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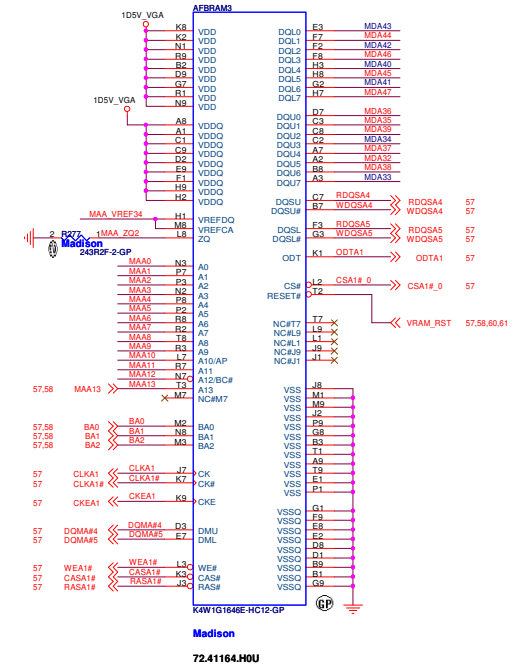
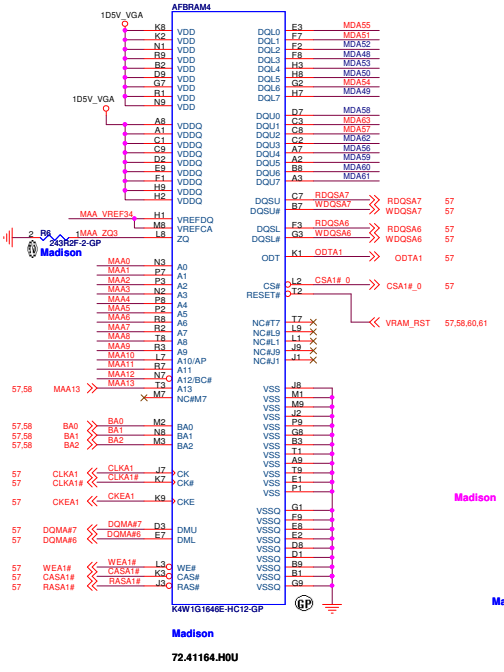
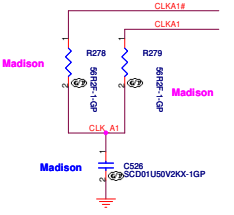
DDR3







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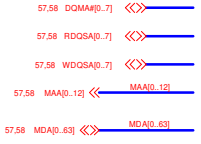

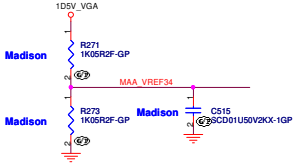

Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(2/4)***	
Size A3	Document Number **JE40-DN**	Rev -3
Date: Friday, March 26, 2010	Sheet 59 of 63	

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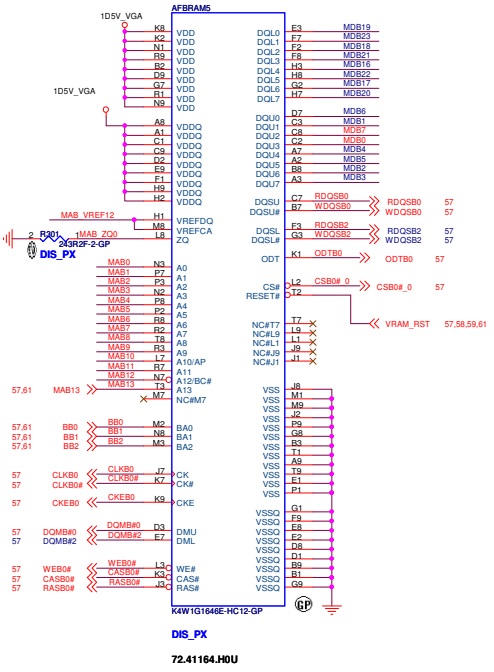
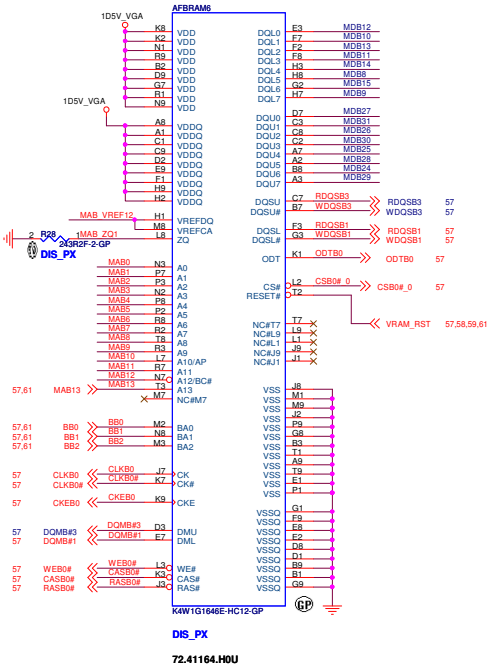
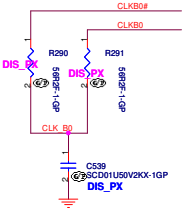
DDR3







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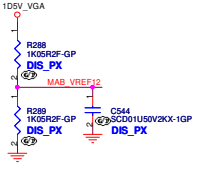

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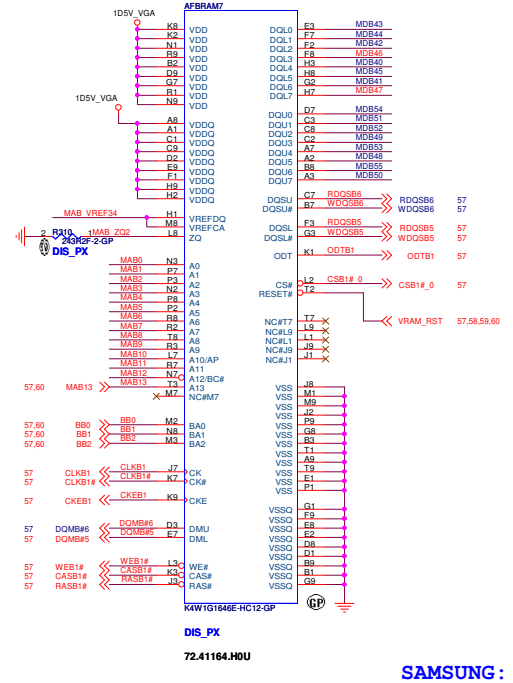
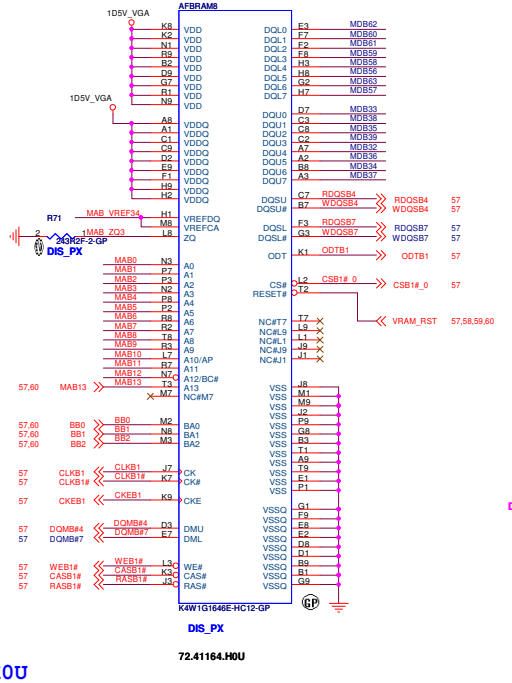
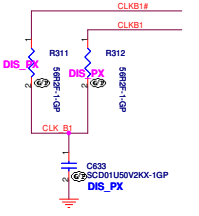
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(3/4)***	
Size A3	Document Number **JE40-DN**	Rev -3
Date: Friday, March 26, 2010	Sheet 60 of 63	

DDR3







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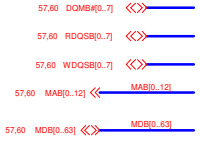

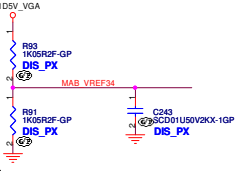

Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(4/4)***	
Size A3	Document Number **JE40-DN**	Rev -3
Date: Friday, March 26, 2010	Sheet 61 of 63	

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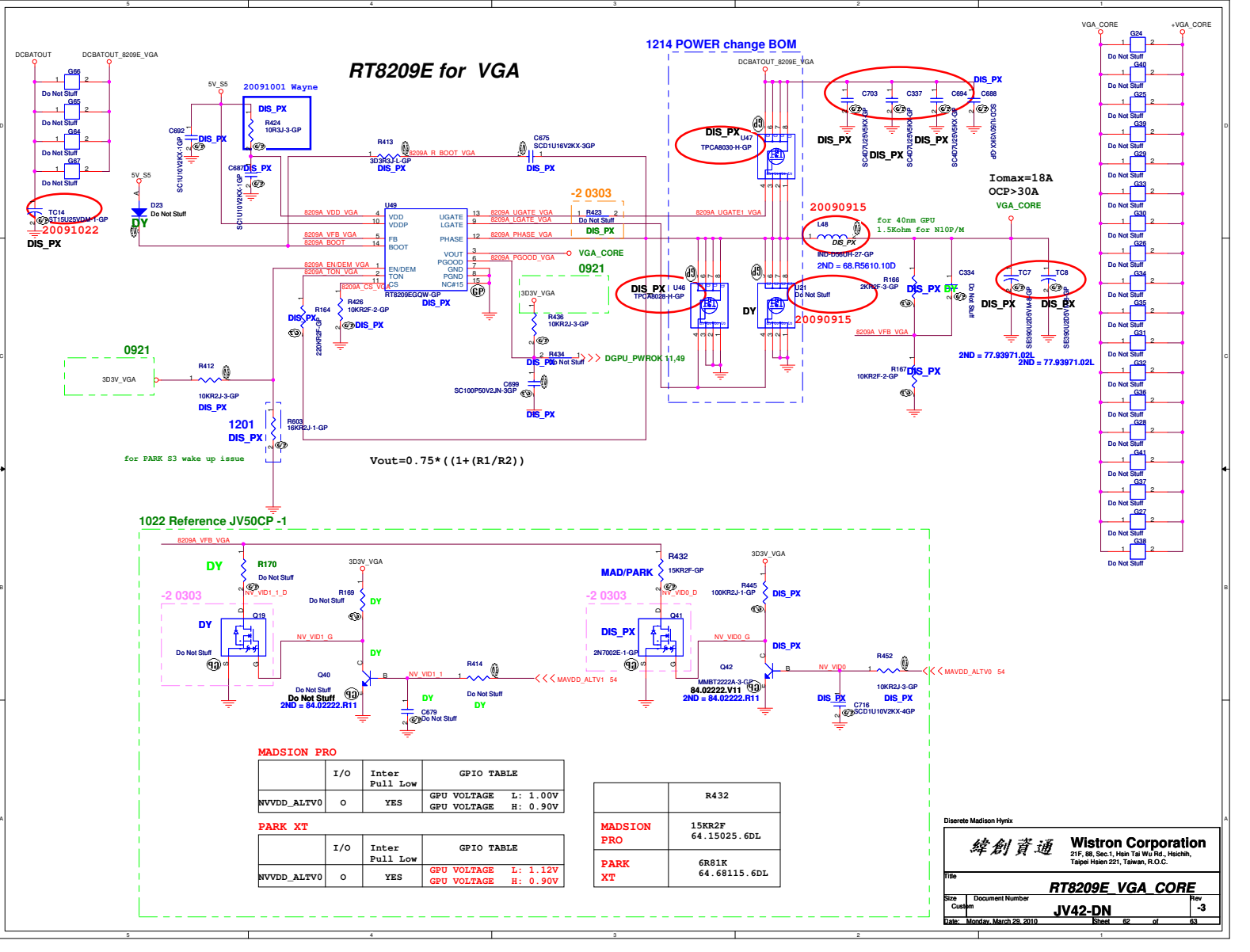
RT8209E for VGA
1214 POWER change BOM
20091001 Wayne
20091022
20090915
-2 0303
0921
1201
1022 Reference JV50CP -1
MADSON PRO
PARK XT
Vout=0.75*((1+(R1/R2))
Iomax=18A
OCP>30A
for PARK S3 wake up issue
for 40nm GPU
1.5Kohm for N10P/M
2ND = 68.R5610.10D
2ND = 77.93971.02L
DGPU_PWROK 11,49
MAVDD_ALTV1 54
MAVDD_ALTV0 54
2ND = 84.02222.R11
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
RT8209E_VGA_CORE
JV42-DN
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NB

RS780-->RS880M

71.RS780.M02-->71.RS880.M02

SB

SB820M-1-GP

71.SB820.00U-->71.SB820.M03

SATA_CALRP

A11: 80歐姆 1% resistor to GND

A12: TBD歐姆 1% resistor to GND

SATA_CALRN

A11:A11: 931歐姆1% resistor to VDDAN_11_SATA

A12: TBD歐姆 1% resistor to VDDAN_11_SATA.

VGA

Madison--> PN:71.MDSON.M01

Park--> PN:71.0PARK.M04

VRAM

Samsung-->VRAM FBRAM1~8 PN:VR.1GB0B.006

Hynix--> VRAM FBRAM1~8 PN:VR.1GB0G.004

ATI--> VRAM FBRAM1~8 PN: VR.1GB0T.002

CRT

UMA-->L1-->2R 0603

C62-->47U/6.3V

DIS-->L1-->Bead(L1 68.00217.711 L1608-UH38 SBK160808T-221Y-N-GP)

C62-->DY

PX--> 133 歐姆 (R58 63.10334.1DL R402H16 133R2F-GP)

R605(MAD/PARK/PX)

Madison-->R605 64.15005.6DL R402H16150R2F-L-GP

Park -->R605 64.15005.6DL R402H16150R2F-L-GP

PX -->R605 64.15005.6DL R402H16150R2F-L-GP

HDMI

UMA -->R612 R613 R618 R619 R620 R621 R624 R625 64.71505.6DL R402H16715R2F-2-GP

R432(MAD/PARK)

Madison-->15KR2F 64.15025.6DL

Park-->R432 64.68115.6DL R402H16 6.81KR2F

BOM

1st -> All SKU

R250

Madison-->R250 64.32425.6DL R402H16 32K4R2F

Park -->R250 64.32425.6DL R402H16 32K4R2F

PX -->R250 64.32425.6DL R402H16 32K4R2F

Diserete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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