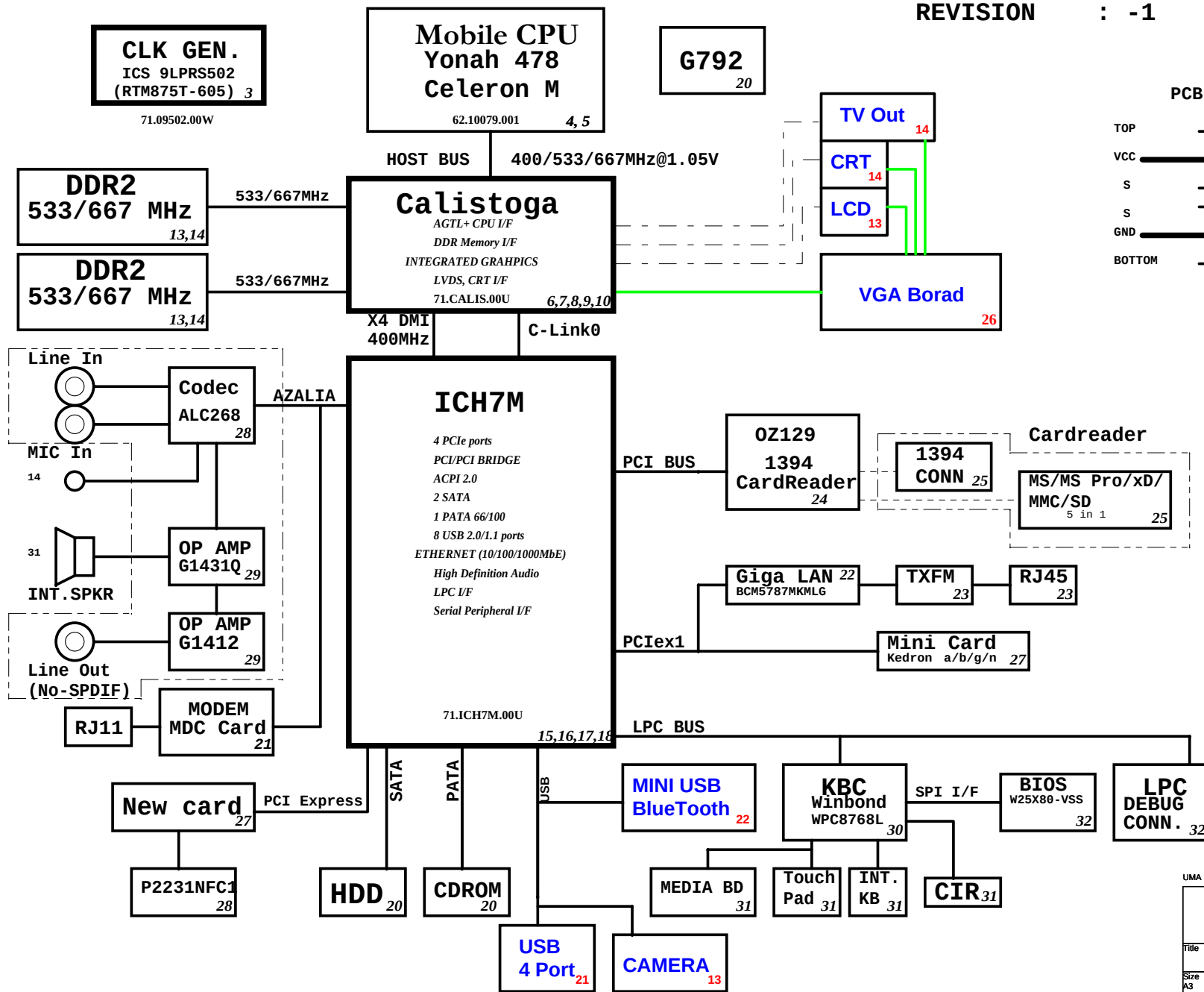


Volvi Block Diagram

Project code: 91.4U701.001
PCB P/N : 07200
REVISION : -1



SYSTEM DC/DC	
MAX8744	36
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5
SYSTEM DC/DC	
MAX8717	37
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D05V_S0
TPS51100	
1D8V_S3	DDR_VREF
APL5312	
3D3V_S0	2D5V_S0
APL5912	
1D8V_S3	1D5V_S0

Intersil CHARGER	
MAX8731 40	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC MAX8770		35
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE 0-1.3V 48A	

ICH7M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/when Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPI020	Reserved	This signal should not be pulled high.
GNT1#/ GPI051	ESi Strap (Server Only) Rising Edge of PWROK	ESi compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH7M IDE Integrated Series
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

PCI Routing

page 16

	IDSEL	INT	REQ	GNT
OZ129	AD22	INT_PIRQ6#	PCI_REQ#0	PCI_GNT#0

ICH7M Integrated Pull-up
and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and
Configuration

Crestline EDS 20954 1.0
page 7

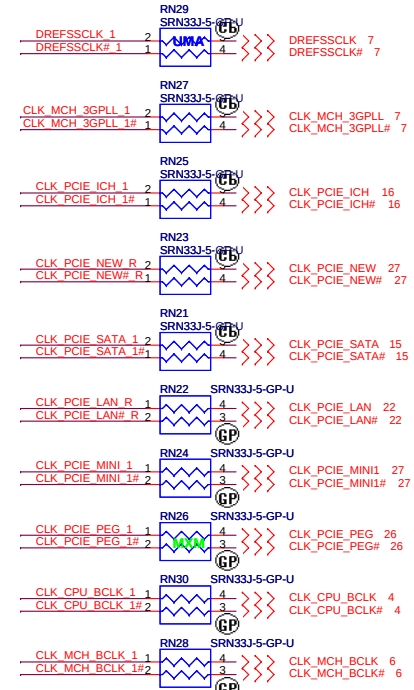
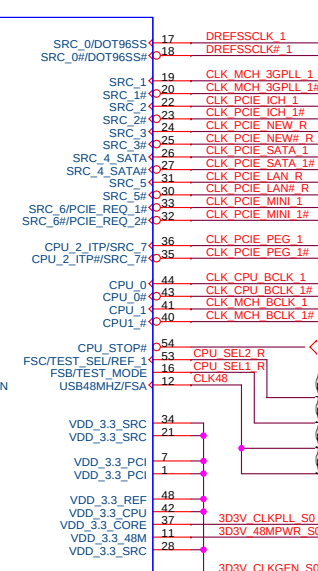
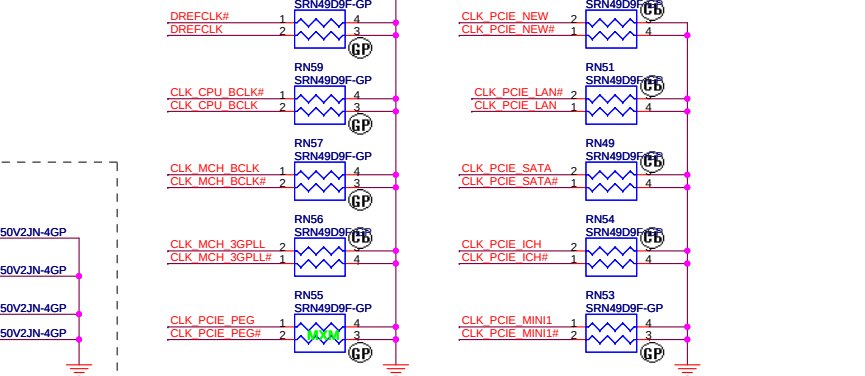
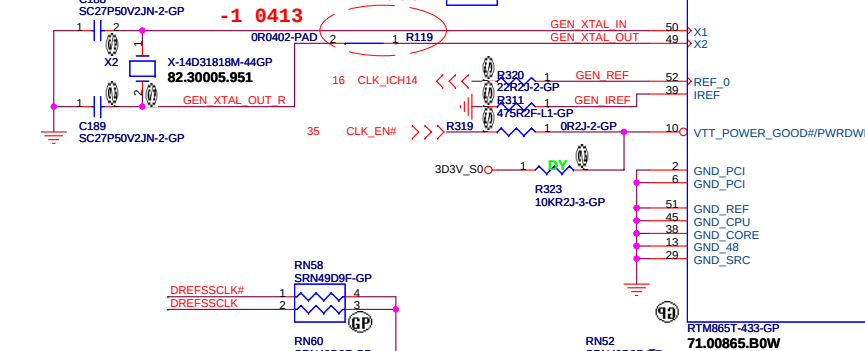
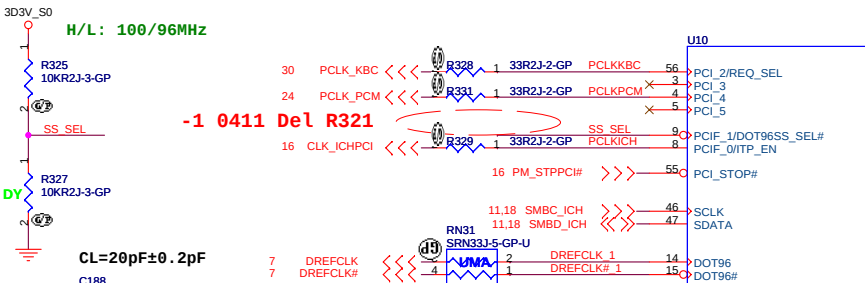
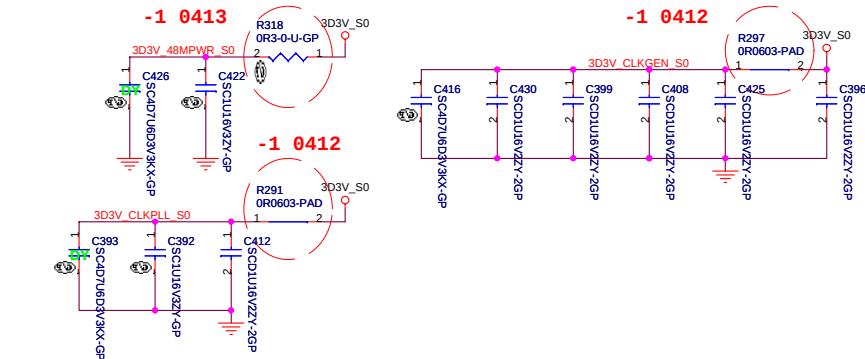
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading
edge of the Crestline GMCH PWORX in signal.

History

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Reference		
Size A3	Document Number Volvi	Rev -1
Date: Wednesday, April 18, 2007	Sheet 2 of	42



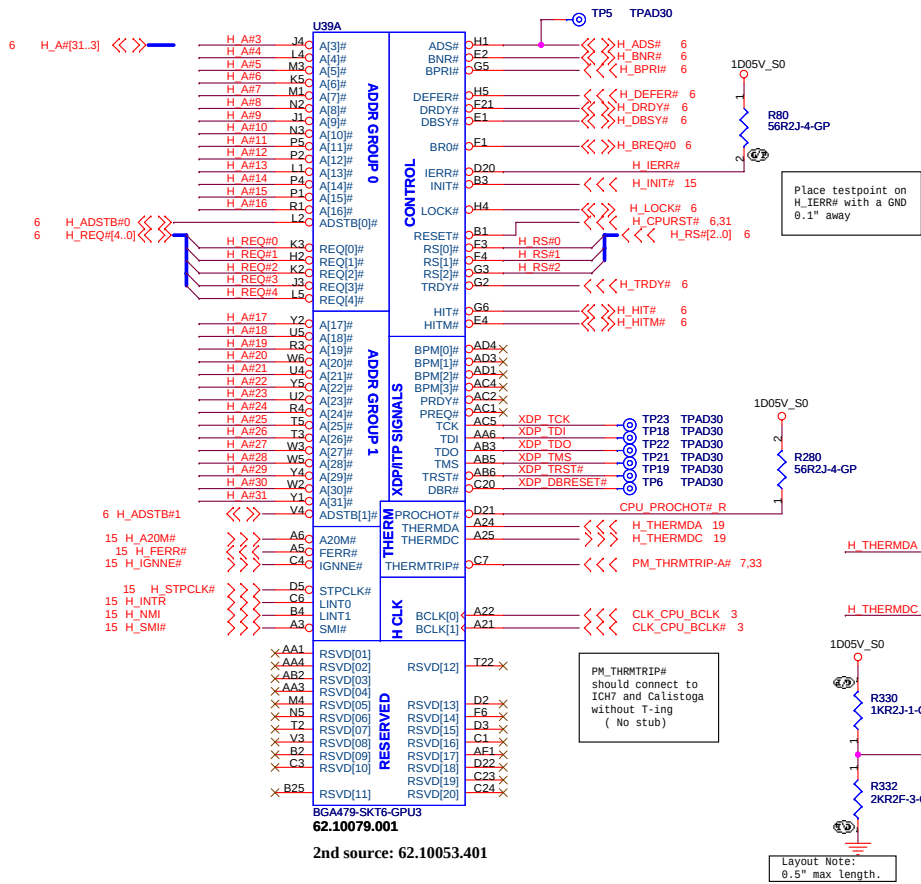
FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

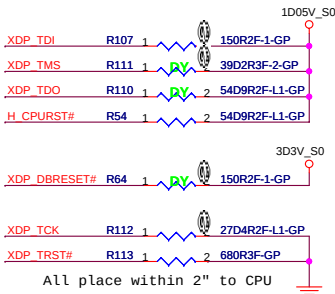
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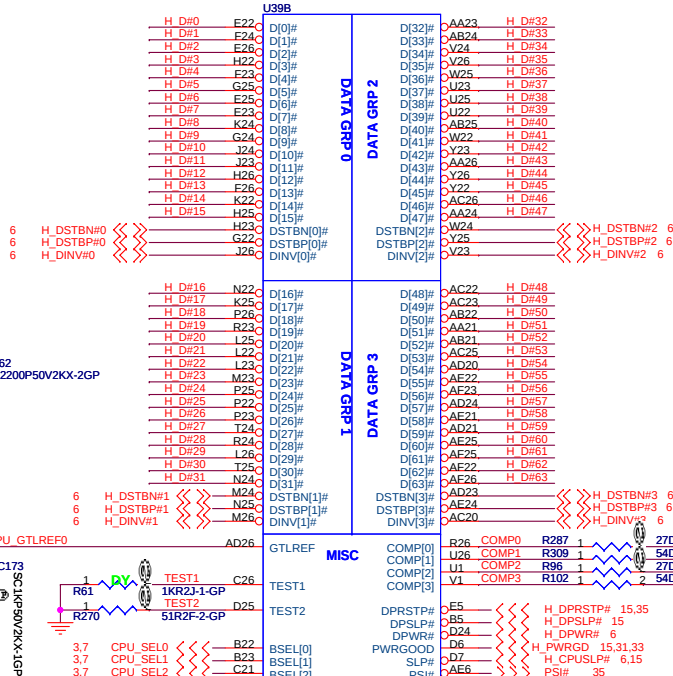
Date: Wednesday, April 18, 2007 Sheet 3 of 42



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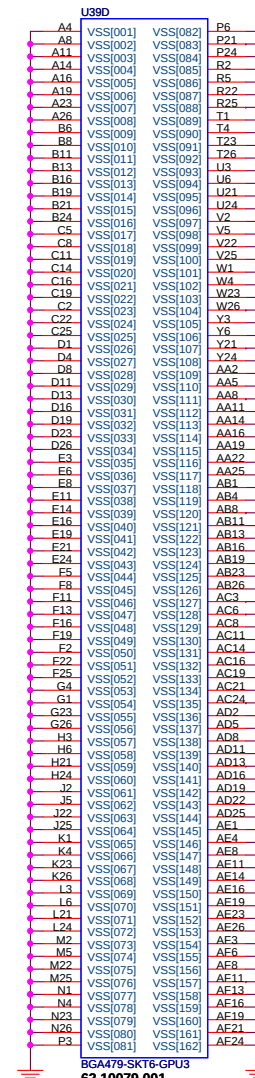


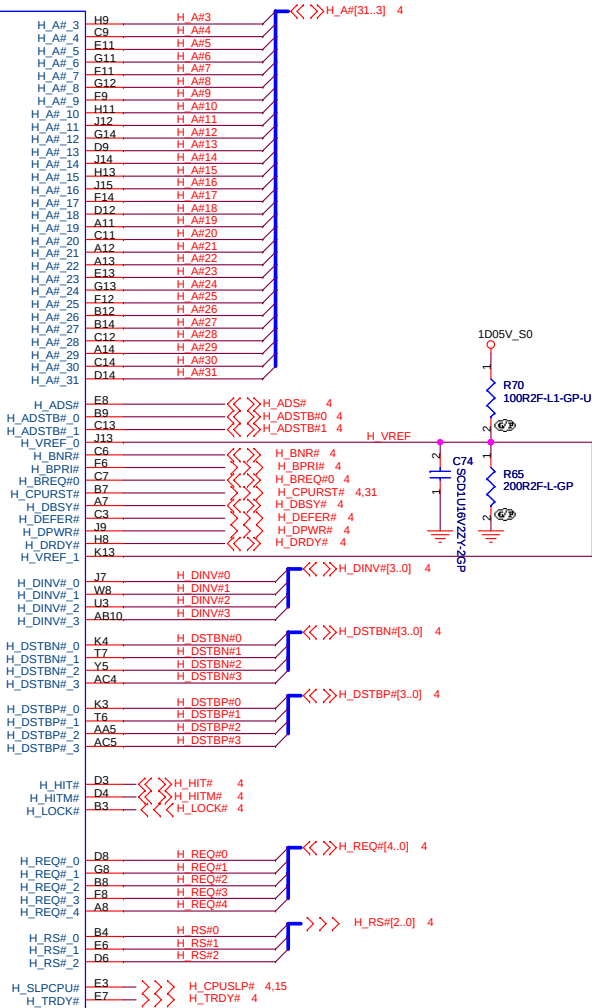
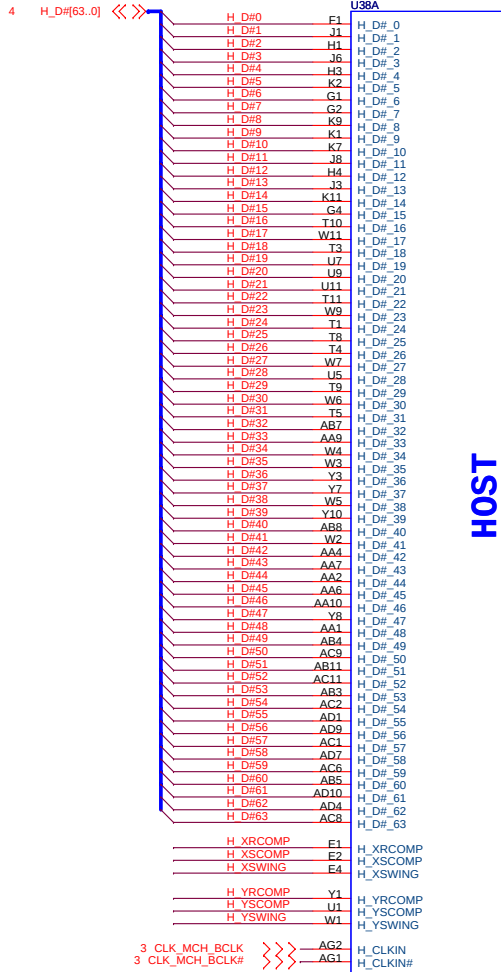
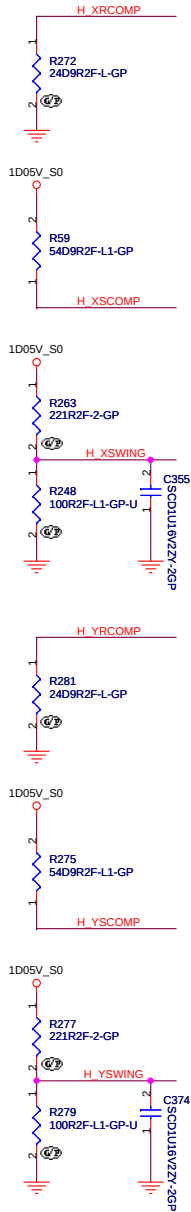
All place within 2" to CPU



2nd source: 62.10053.401

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5"
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"





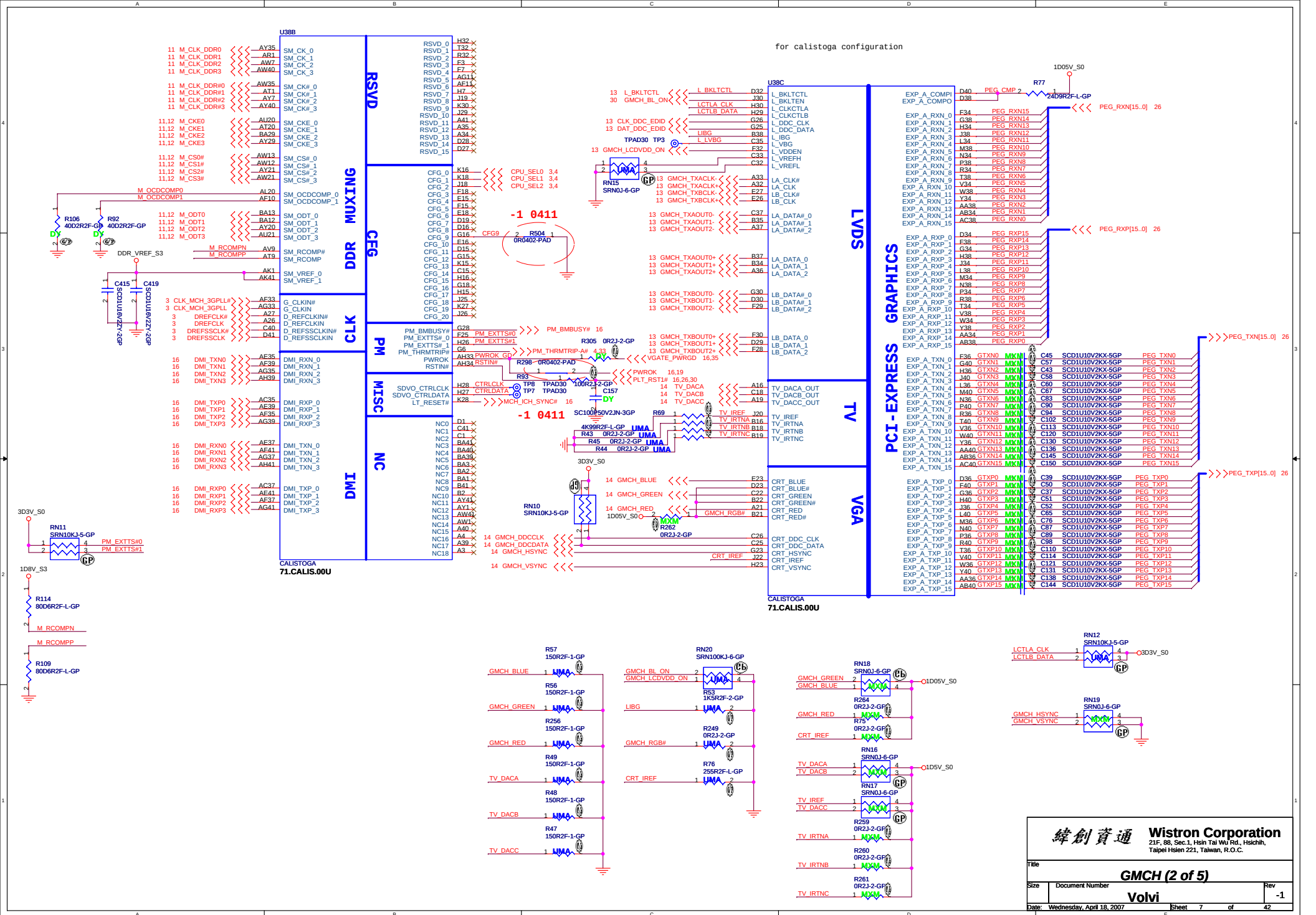
CALISTOGA
71.CALIS.00U

DIS : PM945 KI.94501.006
UMA : GM945 KI.94501.005

Place them near to the chip (< 0.5")

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
GMCH (1 of 5)			
Size	Document Number	Rev	-1
Volvi			
Date: Wednesday, April 18, 2007	Sheet 6	of 42	



11 M_A_DQ[63.0] <<<

U38D
M A DQ0 AJ35 SA_DQ0
M A DQ1 AJ34 SA_DQ1
M A DQ2 AM31 SA_DQ2
M A DQ3 AM33 SA_DQ3
M A DQ4 AJ32 SA_DQ4
M A DQ5 AK35 SA_DQ5
M A DQ6 AH31 SA_DQ6
M A DQ7 AN35 SA_DQ7
M A DQ8 AP33 SA_DQ8
M A DQ9 AR31 SA_DQ9
M A DQ10 AP31 SA_DQ10
M A DQ11 AP31 SA_DQ11
M A DQ12 AN38 SA_DQ12
M A DQ13 AM34 SA_DQ13
M A DQ14 AM36 SA_DQ14
M A DQ15 AN33 SA_DQ15
M A DQ16 AK26 SA_DQ16
M A DQ17 AL27 SA_DQ17
M A DQ18 AM26 SA_DQ18
M A DQ19 AN24 SA_DQ19
M A DQ20 AK28 SA_DQ20
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M A DQ26 AP21 SA_DQ26
M A DQ27 AN20 SA_DQ27
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M A DQ48 AY2 SA_DQ48
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M A DQ52 AY2 SA_DQ52
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M A DQ55 AL2 SA_DQ55
M A DQ56 AG7 SA_DQ56
M A DQ57 AE9 SA_DQ57
M A DQ58 AG4 SA_DQ58
M A DQ59 AE6 SA_DQ59
M A DQ60 AG9 SA_DQ60
M A DQ61 AH6 SA_DQ61
M A DQ62 AE4 SA_DQ62
M A DQ63 AE8 SA_DQ63

DDR SYSTEM MEMORY A

SA_BS_0
SA_BS_1
SA_BS_2
SA_CAS#
SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7
SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7
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SA_DQS#_2
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SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7
SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_RAS#
SA_RCVENIN#
SA_RCVENOUT#
SA_WE#

AU12
AV14
BA20
AY13
AJ33
AM35
AL26
AN22
AM14
AL9
AR3
AH4
AK33
AT33
AN28
AM22
AN12
AN8
AP3
AG5
AK32
AU33
AN27
AM21
AM12
AL8
AN3
AH5
AY16
AU14
AV16
BA16
BA17
AU16
AV17
AU17
AW17
AT16
AU13
AT17
AV20
AV12
AW14
AK23
AK24
AY14

M A BS#0 11.12
M A BS#1 11.12
M A BS#2 11.12
M A CAS# 11.12
M A DM[7.0] 11
M A DQS[7.0] 11
M A DQS#[7.0] 11
M A A[13.0] 11.12
M A RAS# 11.12
M A RCVENIN# 11.12
M A RCVENOUT# 11.12
M A WE# 11.12

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M B DQ1 AJ37 SB_DQ1
M B DQ2 AP38 SB_DQ2
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DDR SYSTEM MEMORY B

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SB_BS_1
SB_BS_2
SB_CAS#
SB_DM_0
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SB_DM_2
SB_DM_3
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SB_WE#

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AR24
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AR38
AT36
BA31
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AH8
BA5
AN4
AM39
AT39
AU35
AR29
AR16
AR10
AR7
ANS
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AU39
AT35
AP29
AP16
AT10
AT7
AP5
AY23
AW24
AY24
AR28
AT27
AT28
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AV28
AW27
AV24
BA27
AY27
AR23
AU23
AK16
AK18
AR27

M B BS#0 11.12
M B BS#1 11.12
M B BS#2 11.12
M B CAS# 11.12
M B DM[7.0] 11
M B DQS[7.0] 11
M B DQS#[7.0] 11
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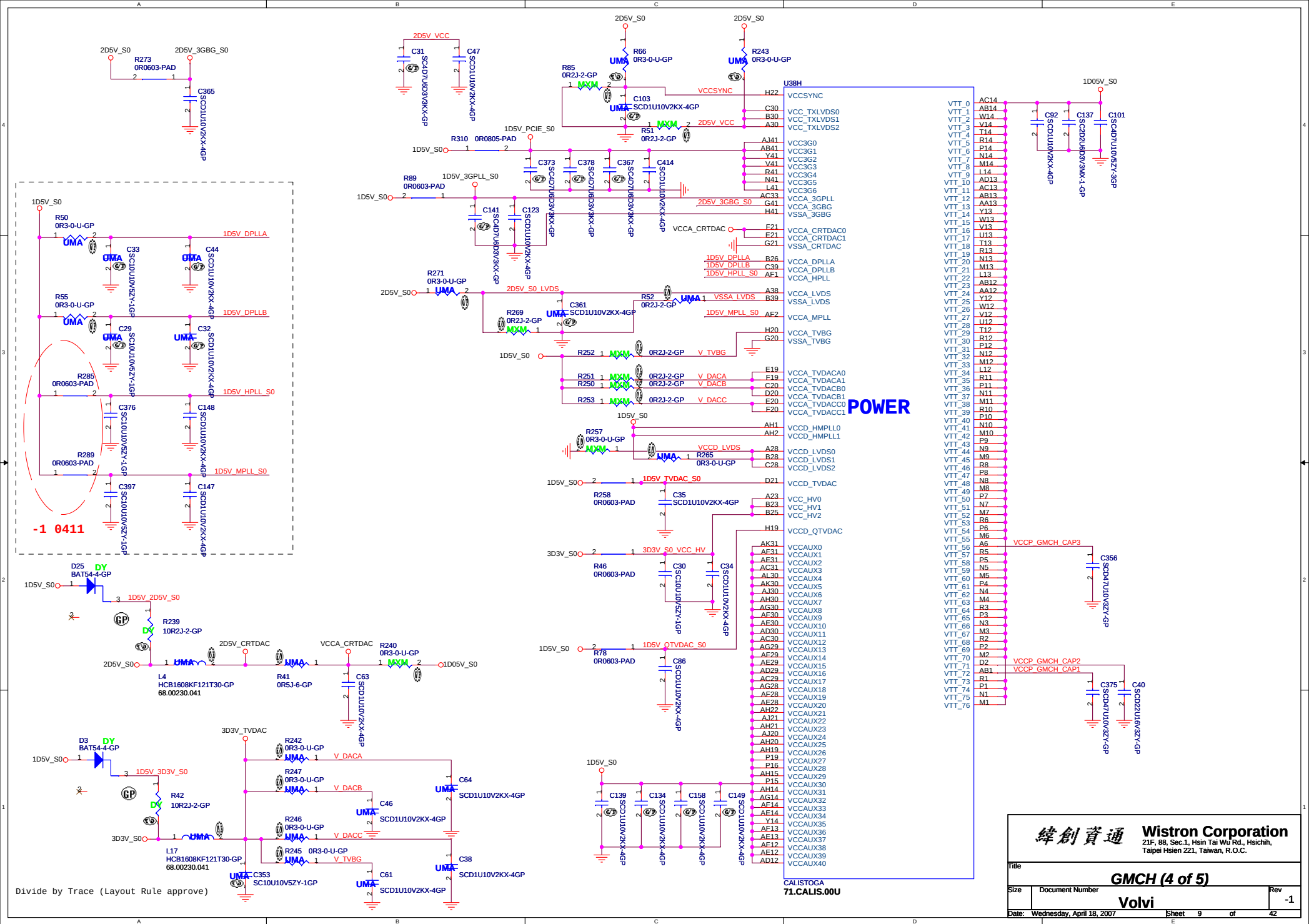
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as could as possible

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71.CALIS.00U

CALISTOGA
71.CALIS.00U

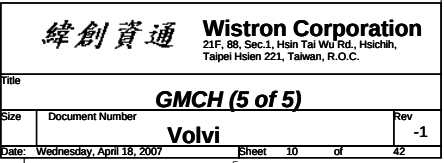
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Taiper Hsien 221, Taiwan, R.O.C.

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Size	Document Number	Rev
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Date: Wednesday, April 18, 2007		
Sheet 8		of 42

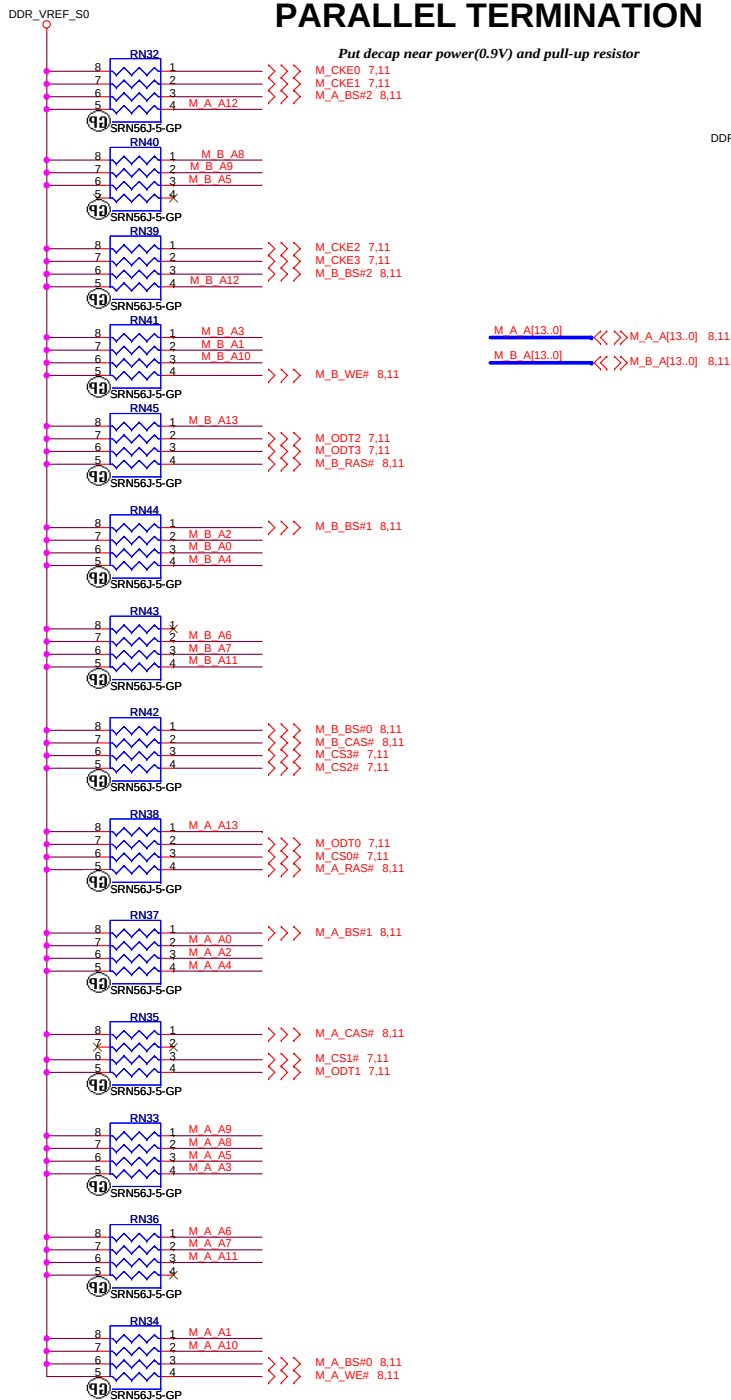


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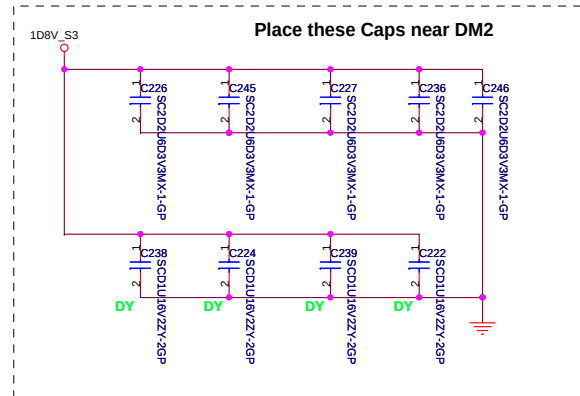
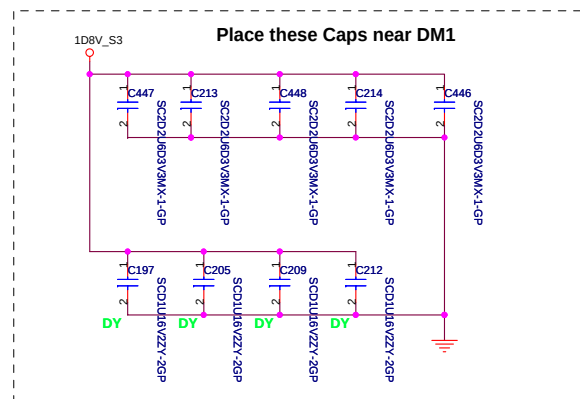
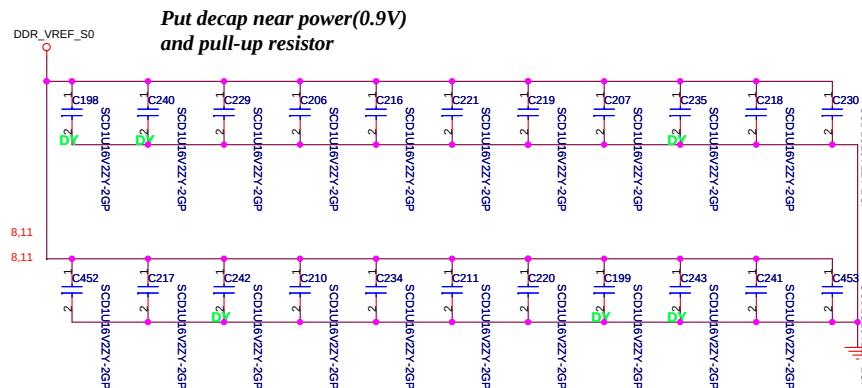
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Size	Document Number			Rev
	Volvi			-1
Date:	Wednesday, April 18, 2007		Sheet 9 of	42



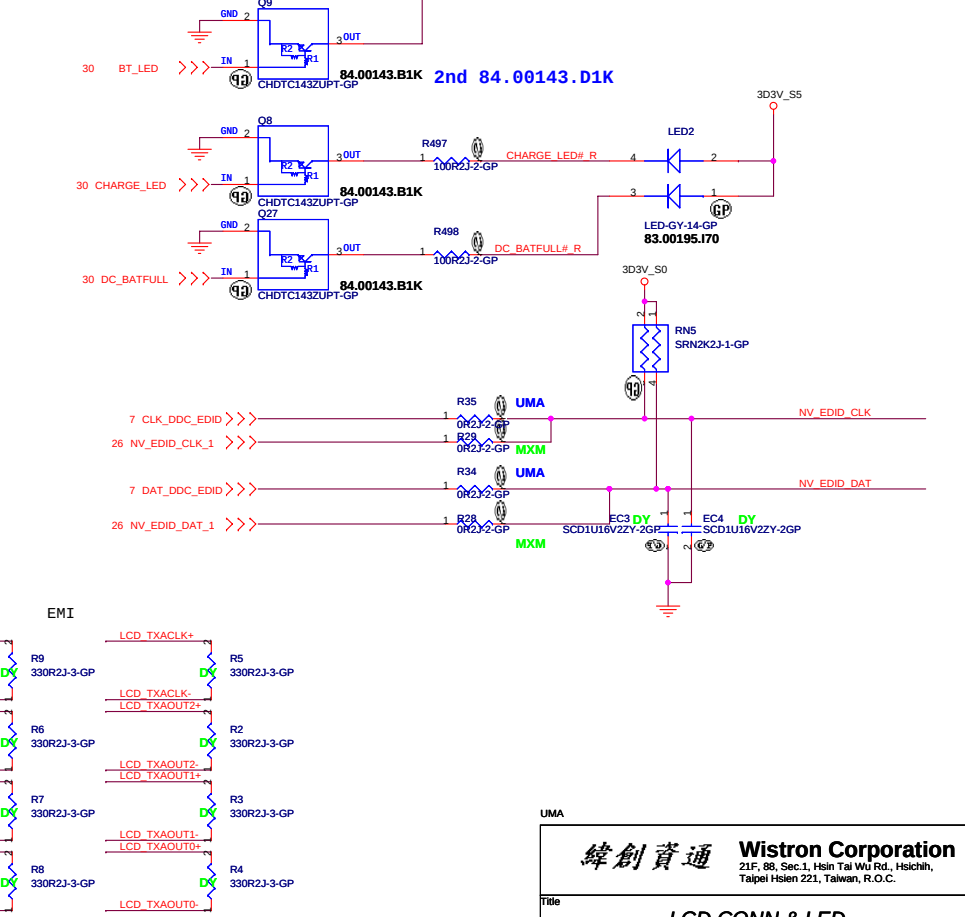
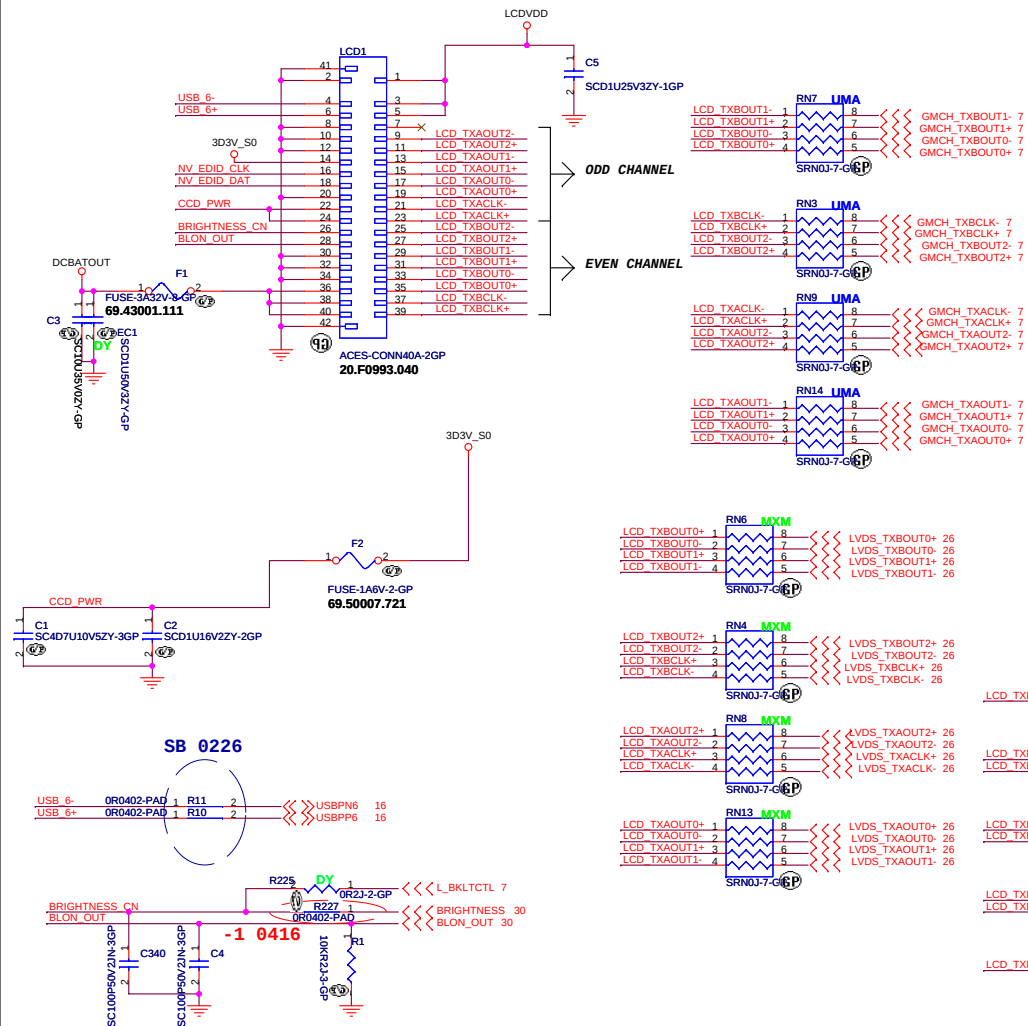
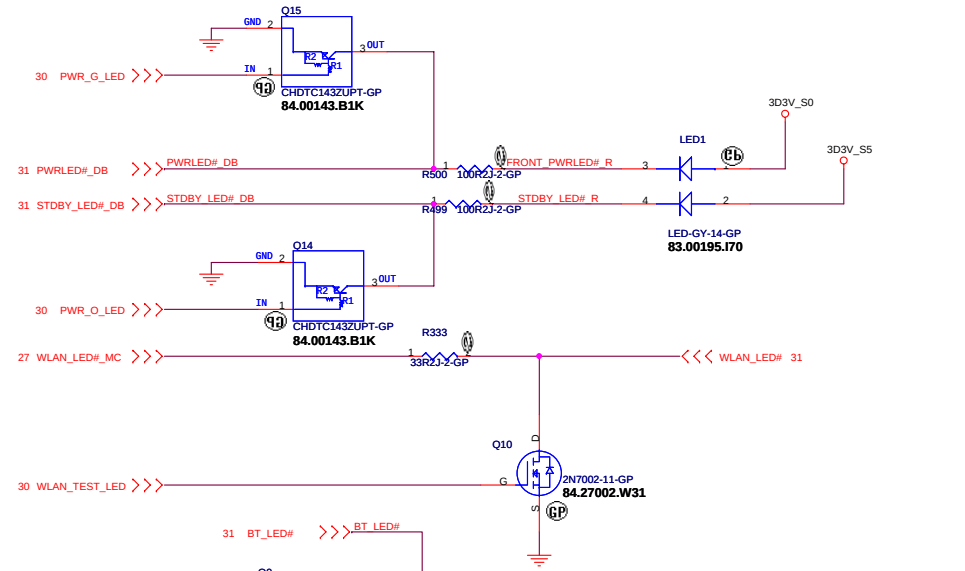
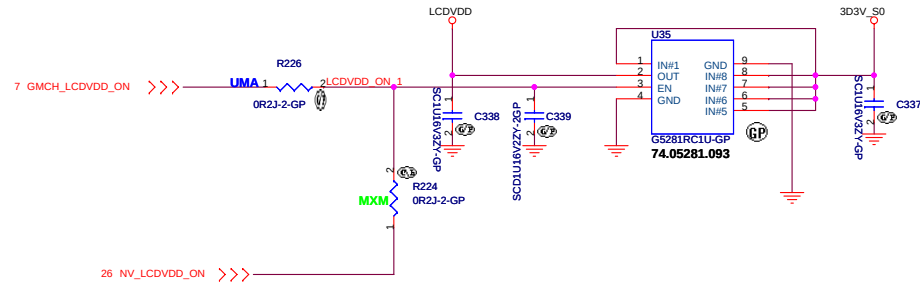
PARALLEL TERMINATION



Decoupling Capacitor



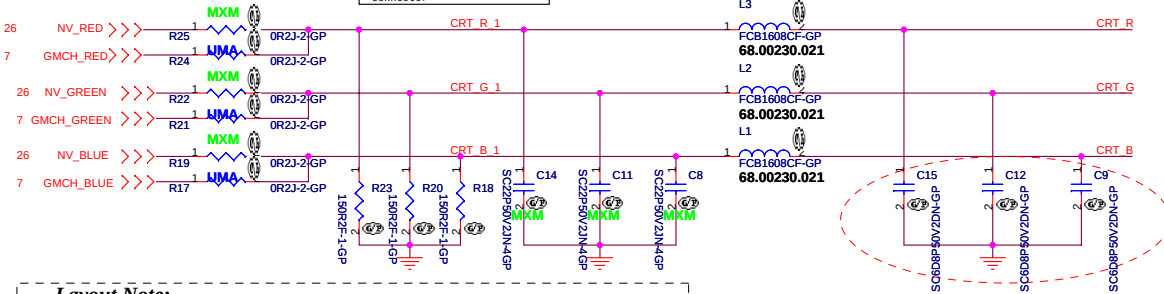
LCD/INVERTER CONN



CRT I/F & CONNECTOR

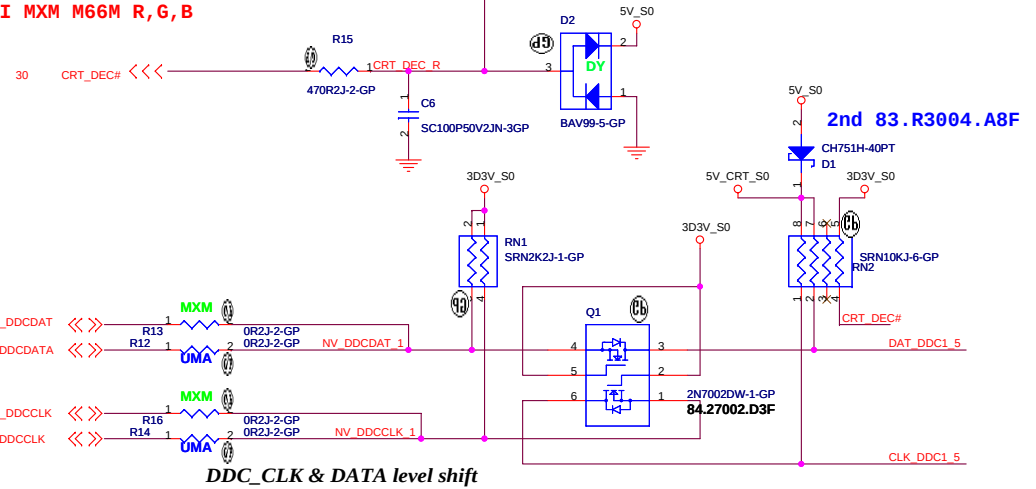
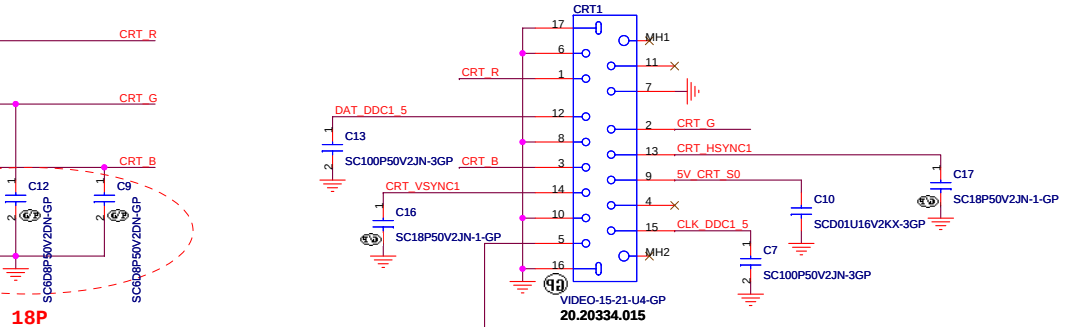
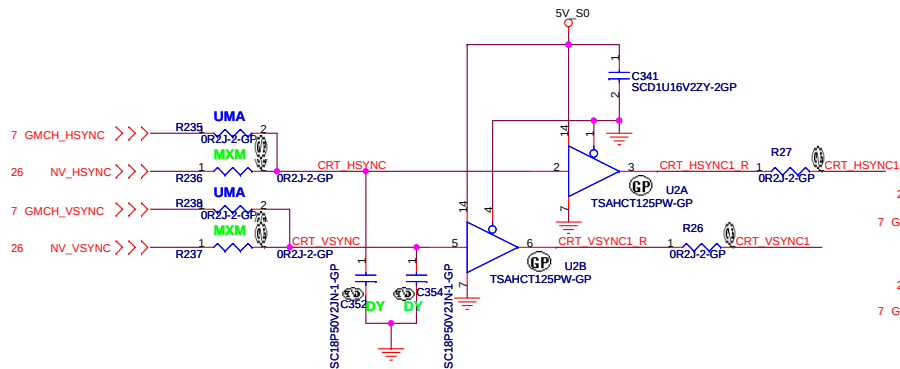
Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 10 ohm@100MHz

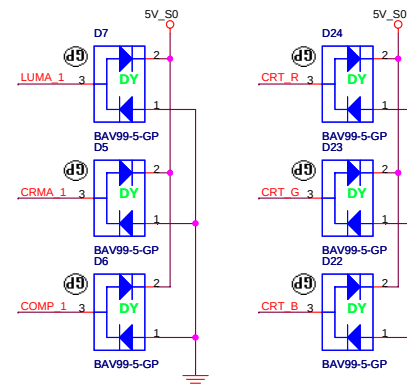
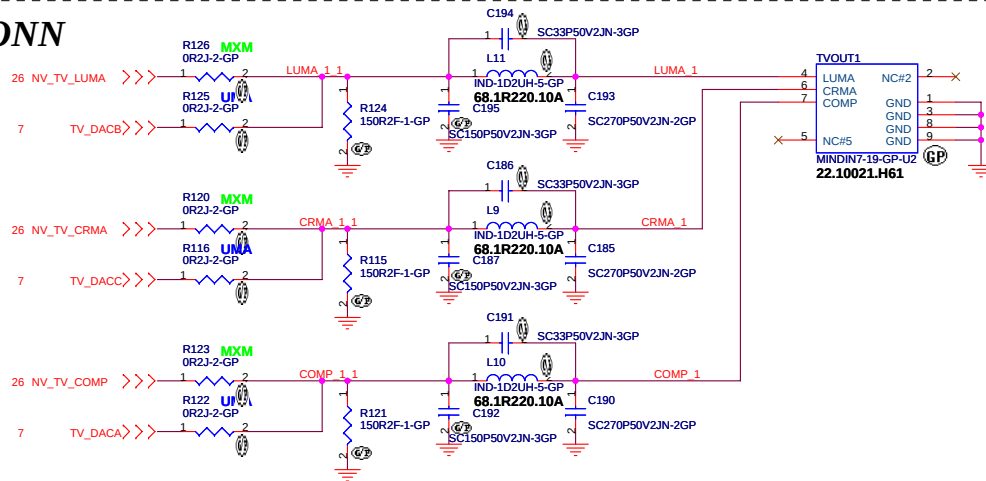


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

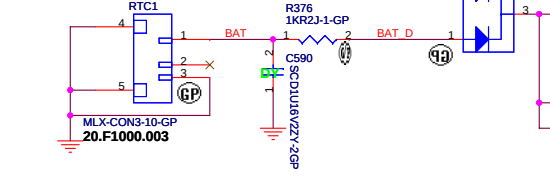


TV CONN

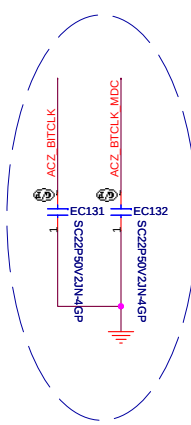


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Title CRT/TV Connector	
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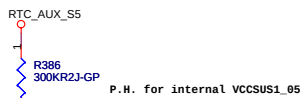
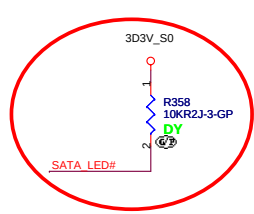
RTC circuitry



SB 0313 for EMI



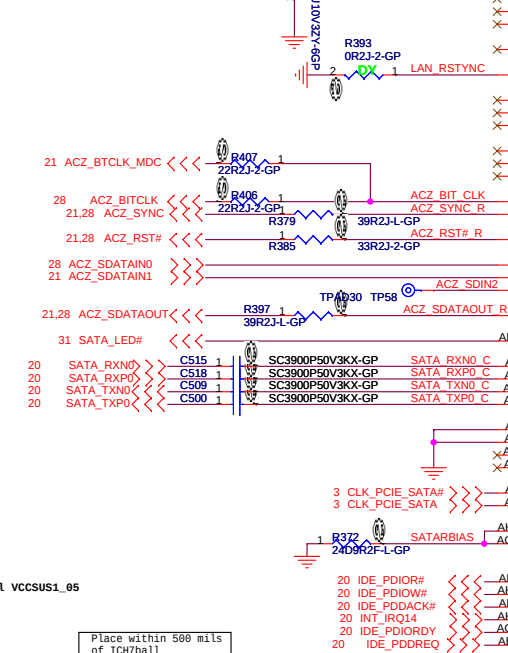
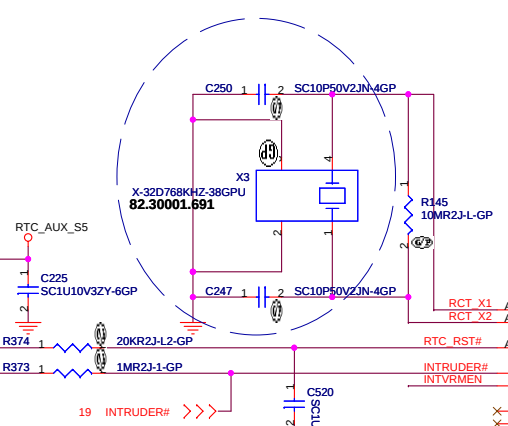
0130



	INTVRMEN
Enable	1
Disable	0

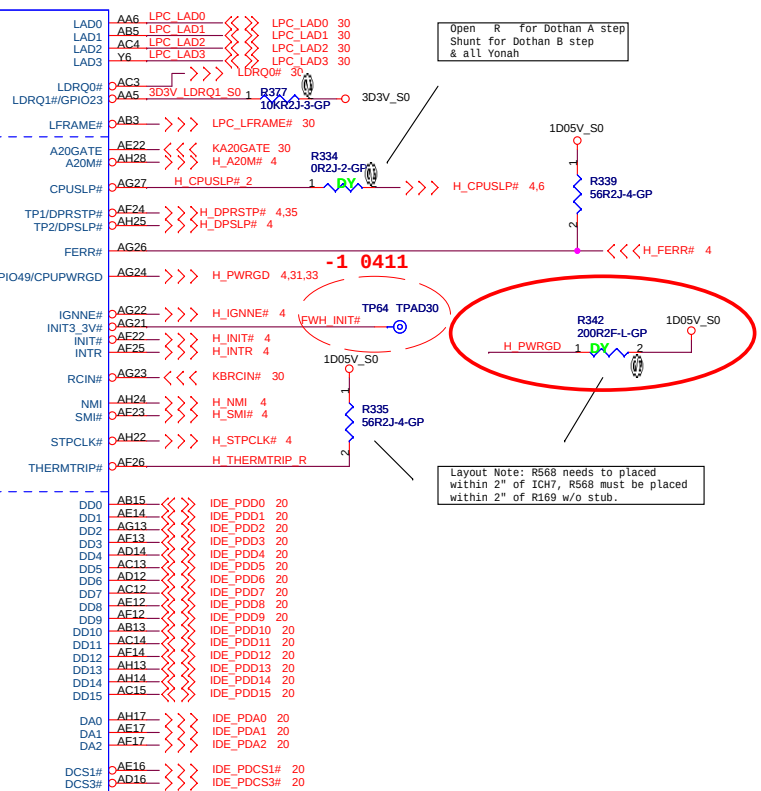
Placement Note:
Distance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.

SB 0305



ICH7-M-GP
71.ICH7M.00U

Change to KI.80101.017



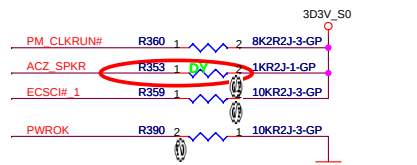
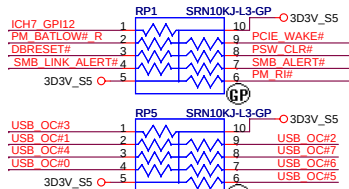
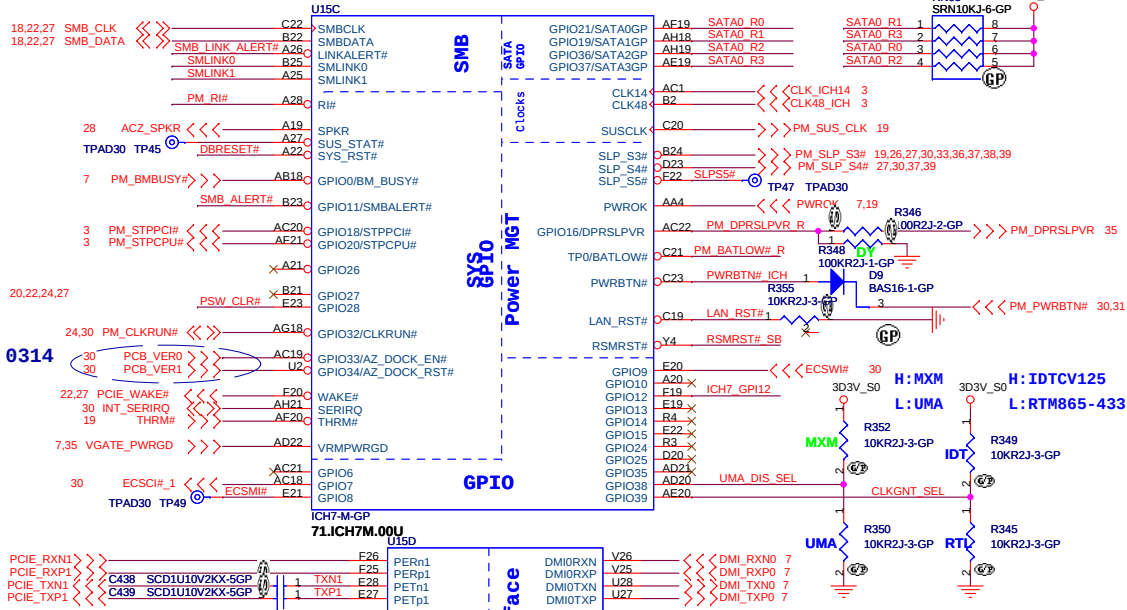
Open R for Dothan A step
Shunt for Dothan B step
& all Yonah

Layout Note: R568 needs to be placed
within 2" of ICH7, R568 must be placed
within 2" of R169 w/o stub.

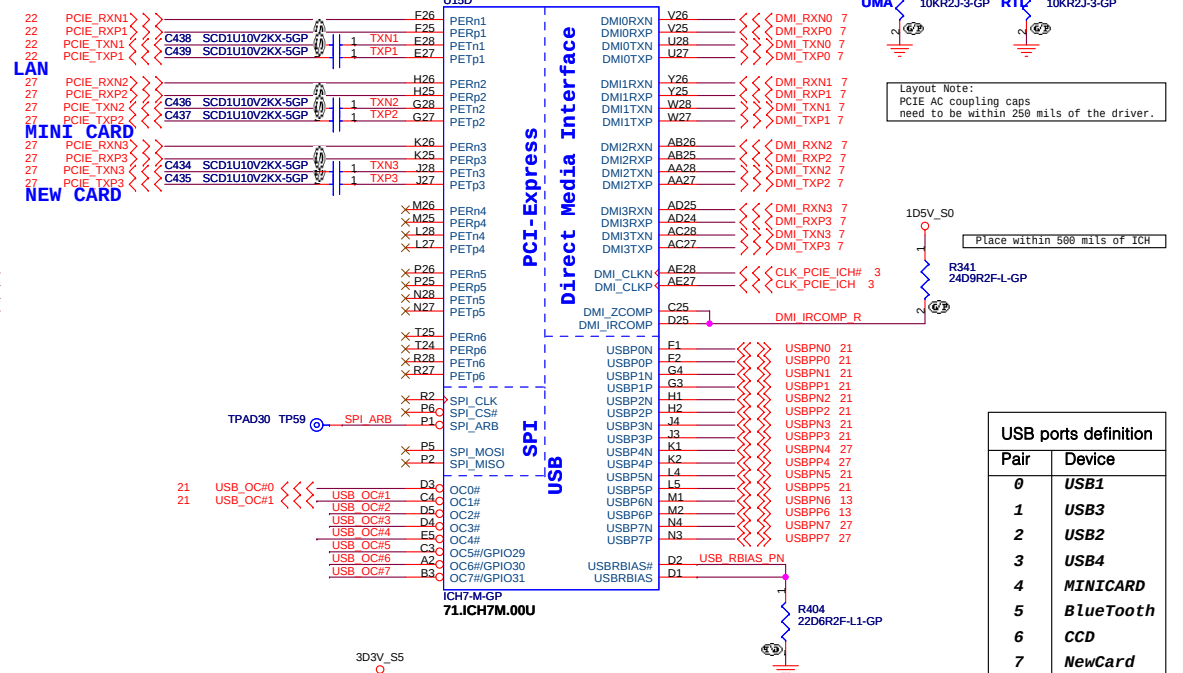
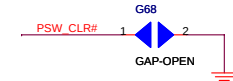
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Title		
ICH7-M (1 of 4)		
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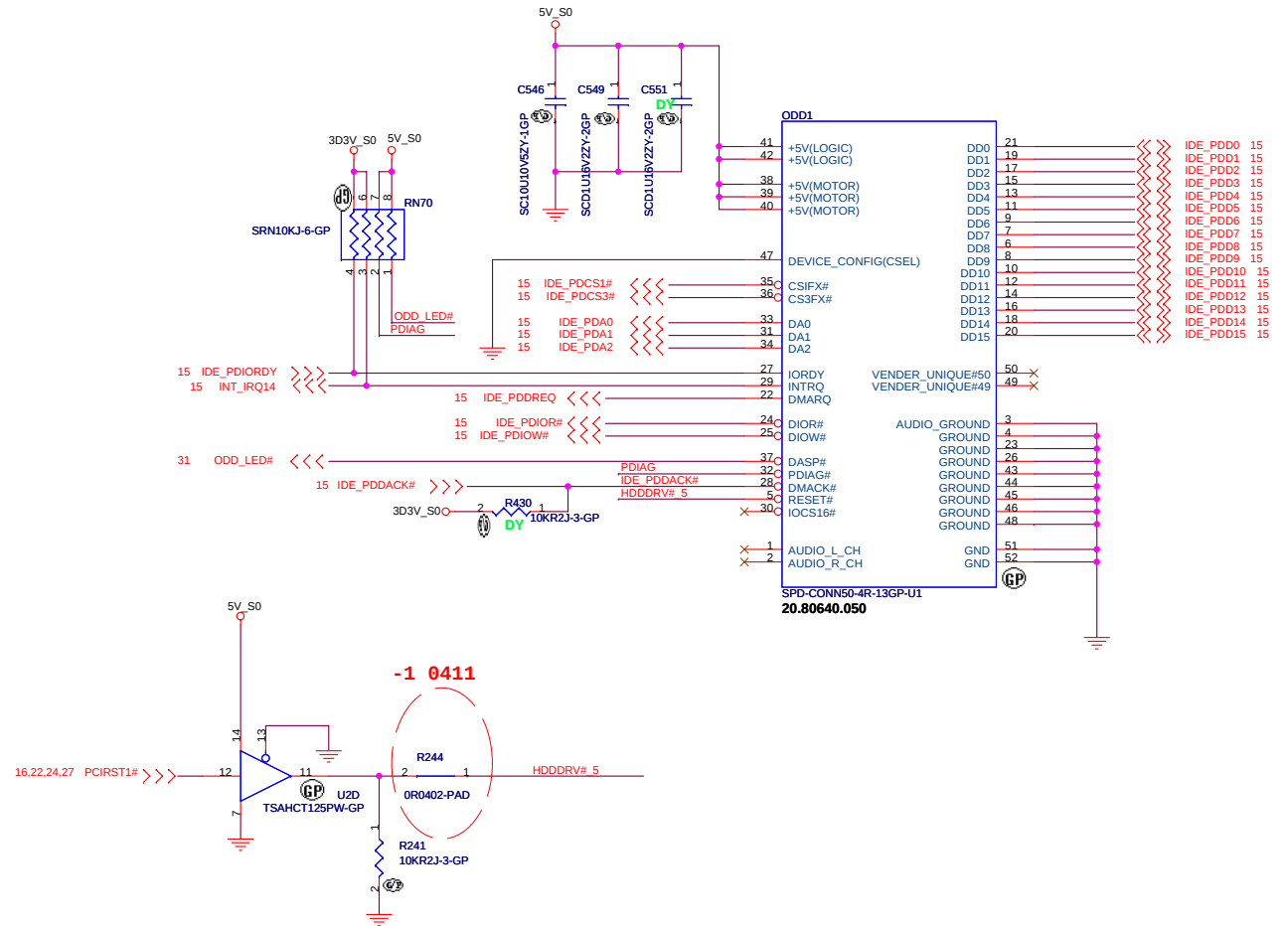


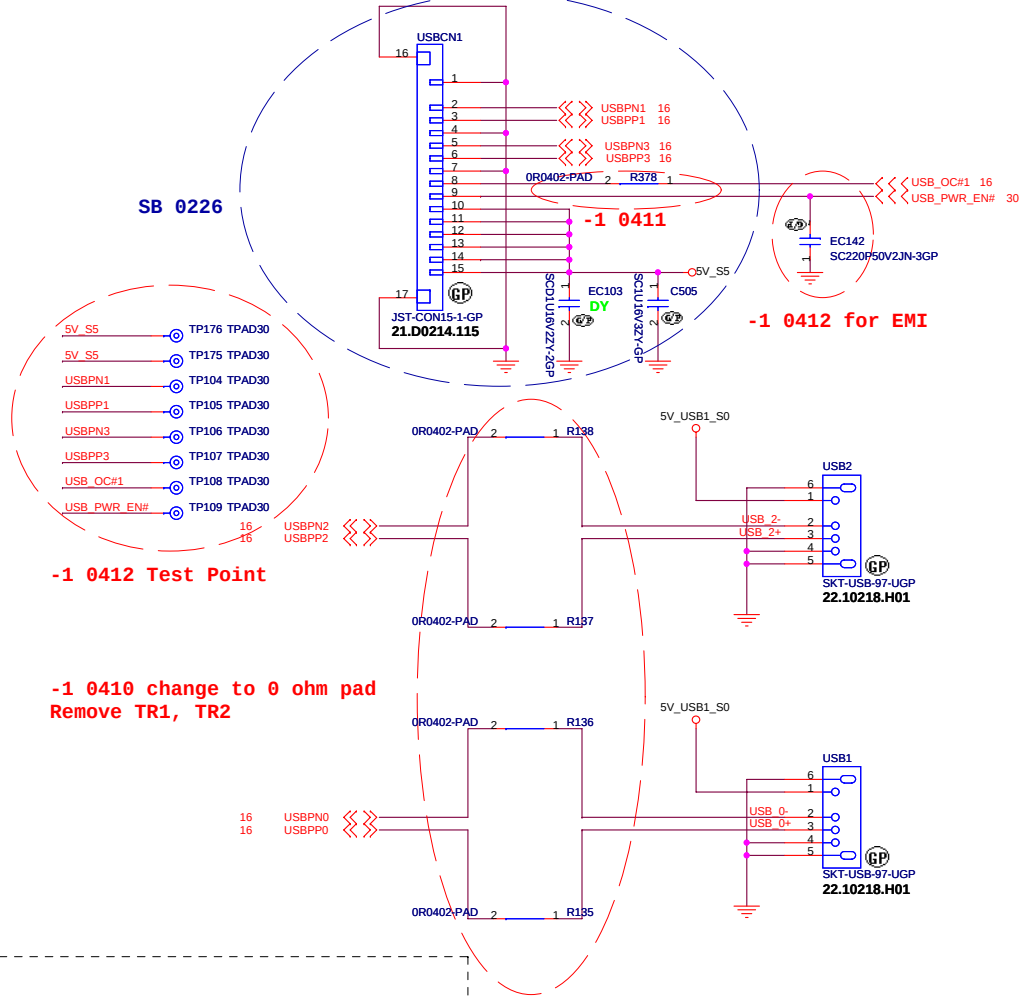
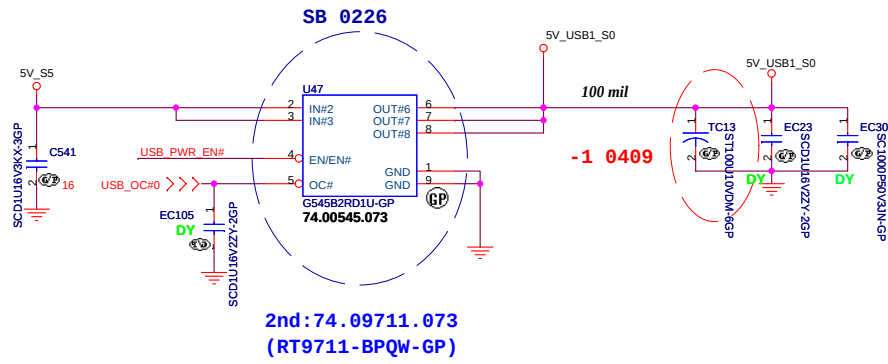
GAP放在Dimm Door打開可量測處



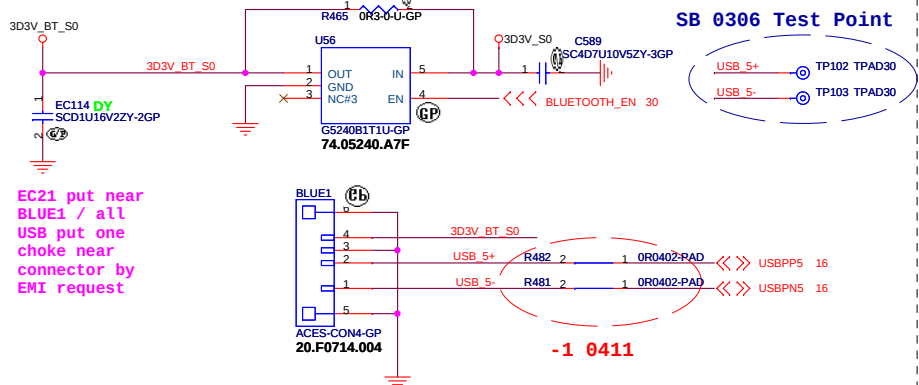
USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

ODD Connector

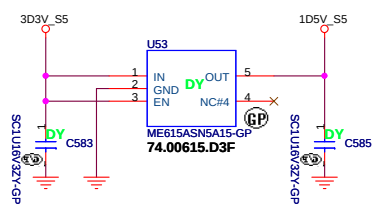
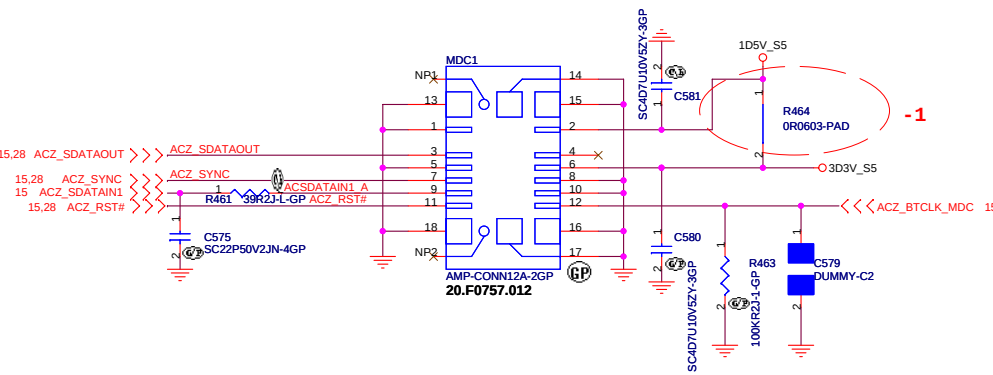


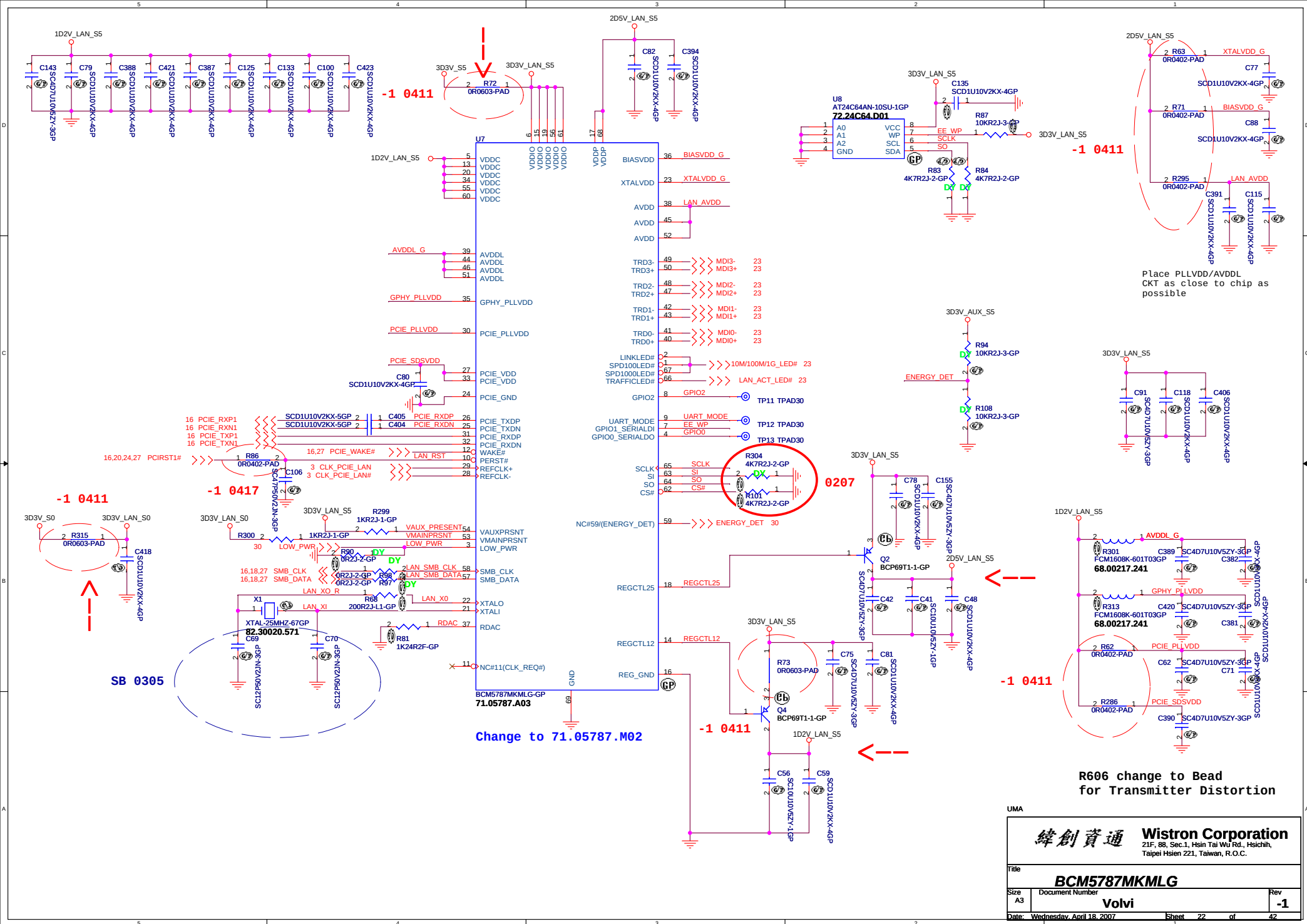


BLUETOOTH MODULE



MDC 1.5 CONN





Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

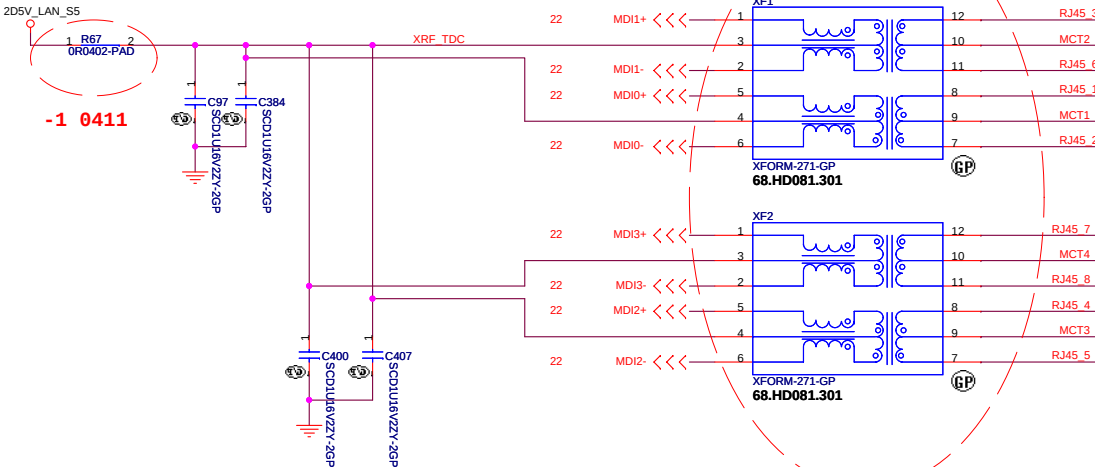
LAN Connector

-1 0331 Test Point



GIGA Lan Transformer

-1 0413



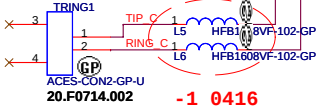
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

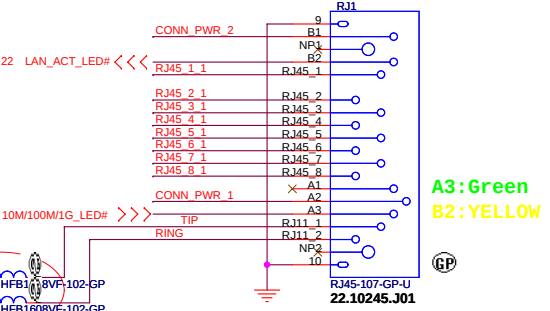
DOC_TIP,DOC_RING,TIP,RING:

W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

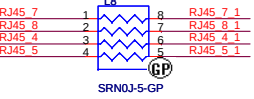
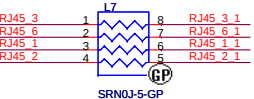


-1 0416

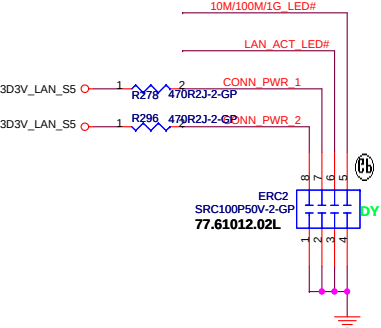


LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

For EMI



Tahoe

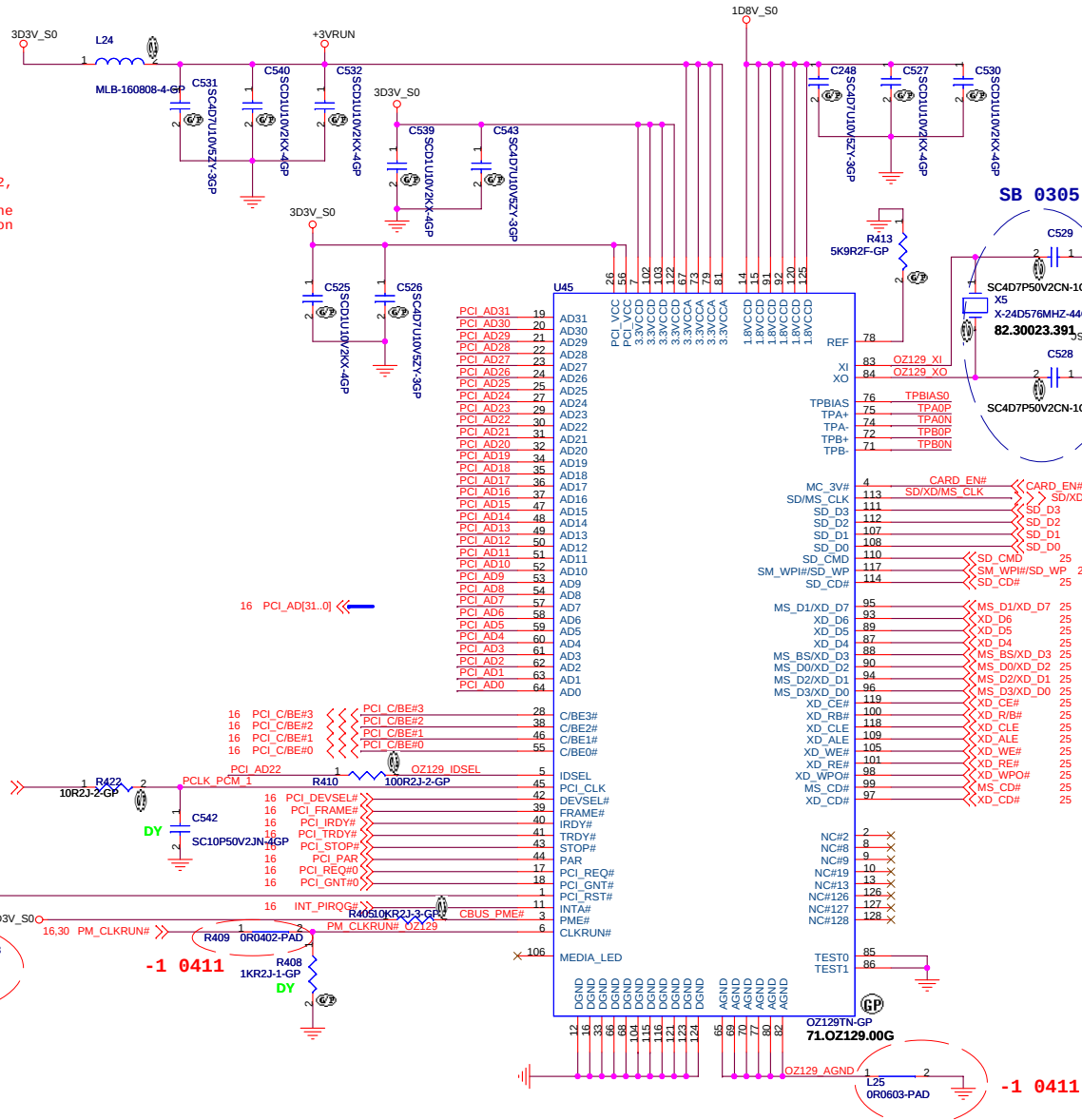


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LAN Connector		
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CLOSE TO TRANSFORMER

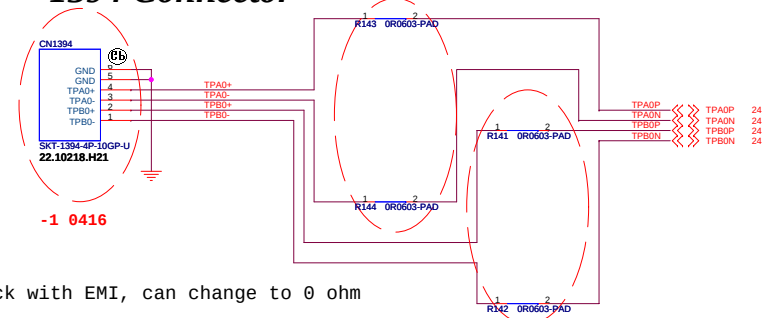


TPBIAS0				
TPA0P	↔	↔	TPA0P	25
TPA0N	↔	↔	TPA0N	25
TPB0P	↔	↔	TPB0P	25
TPB0N	↔	↔	TPB0N	25

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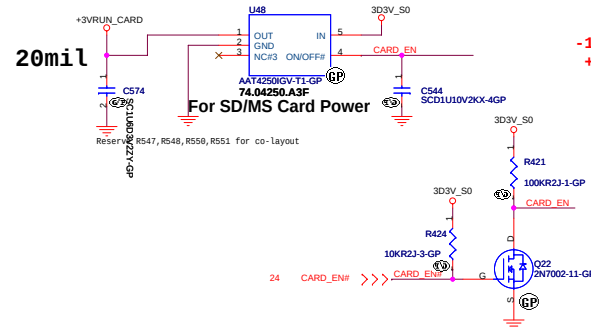
1394 Connector

-1 0411 del L22 and L23



-1 0416

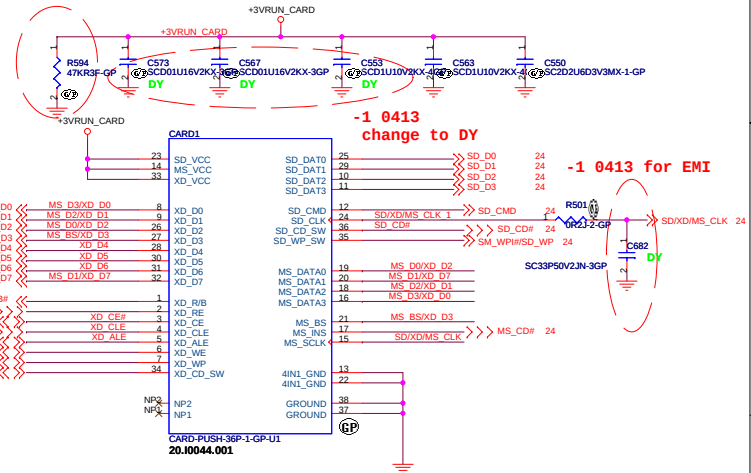
check with EMI, can change to 0 ohm



20mil

For SD/MS Card Power

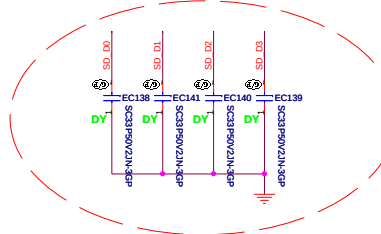
-1 0413
+3VRUN_CARD discharging



-1 0413
change to DY

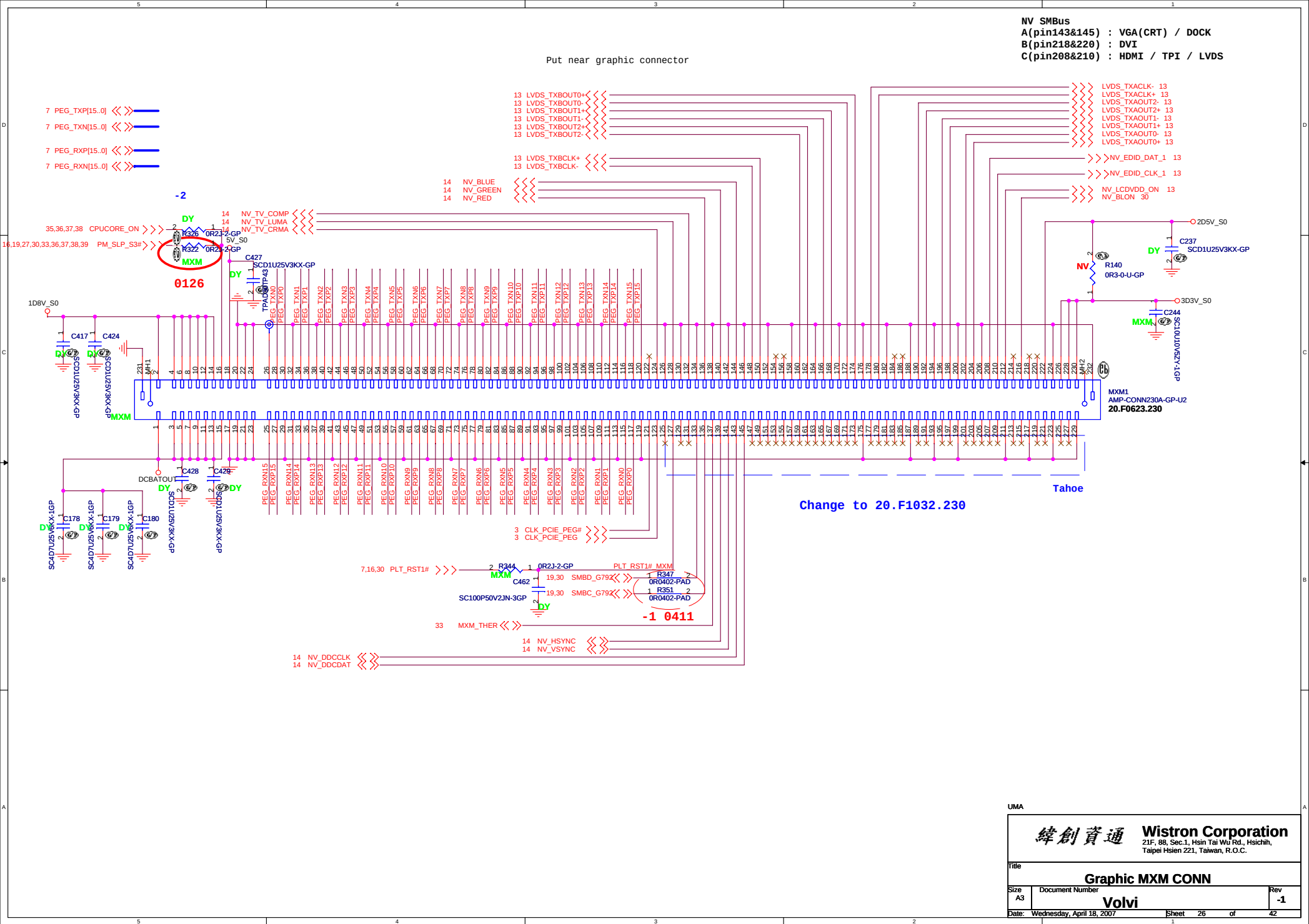
-1 0413 for EMI

-1 0413 for EMI



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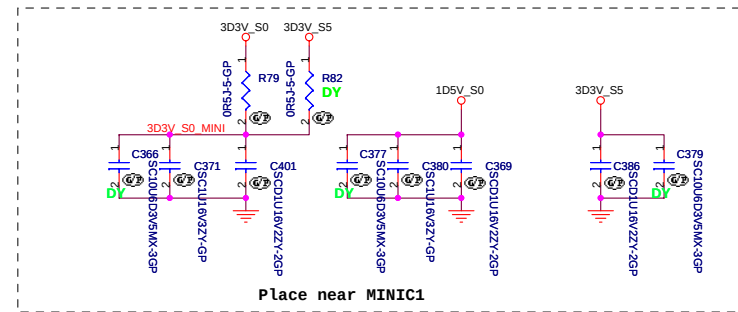
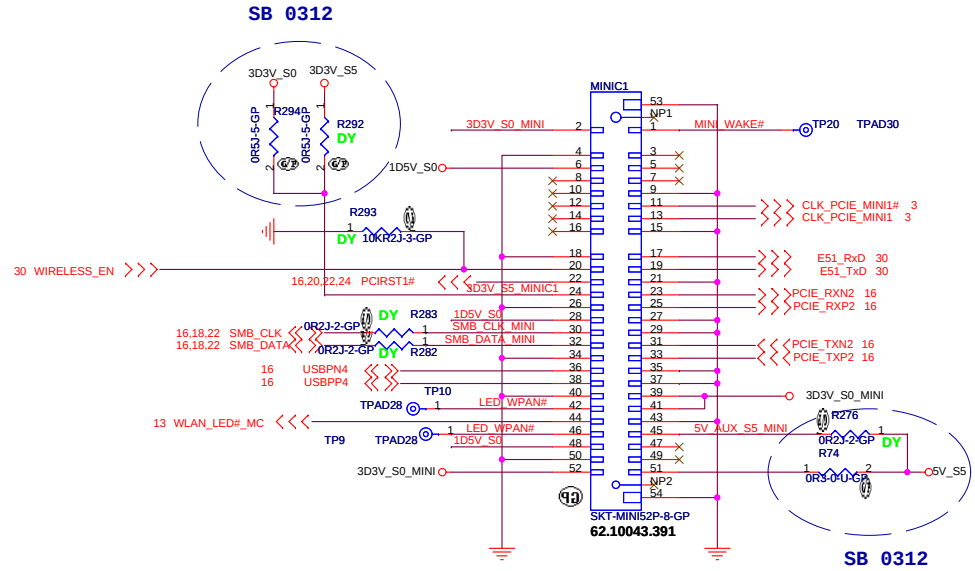
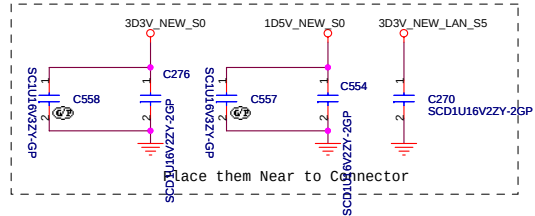
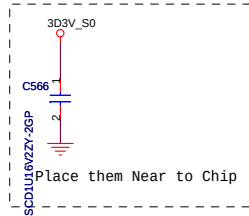
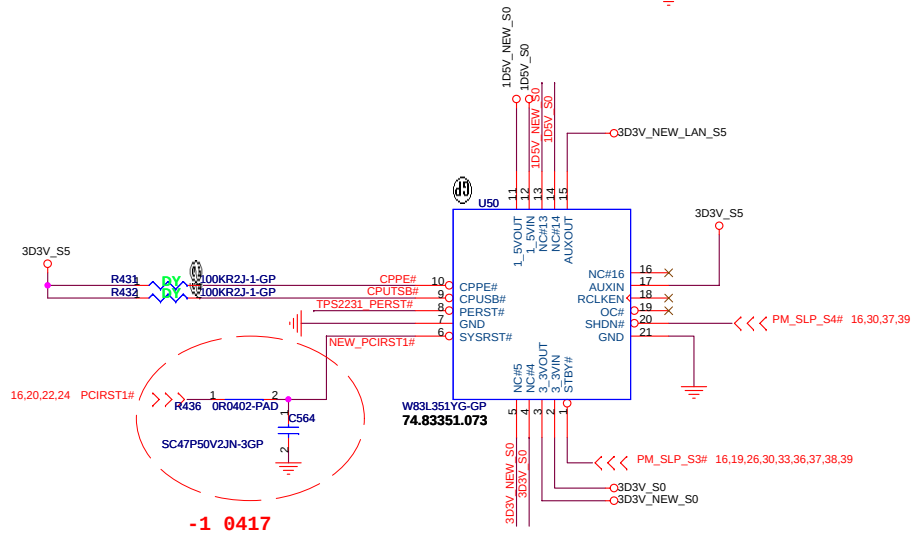
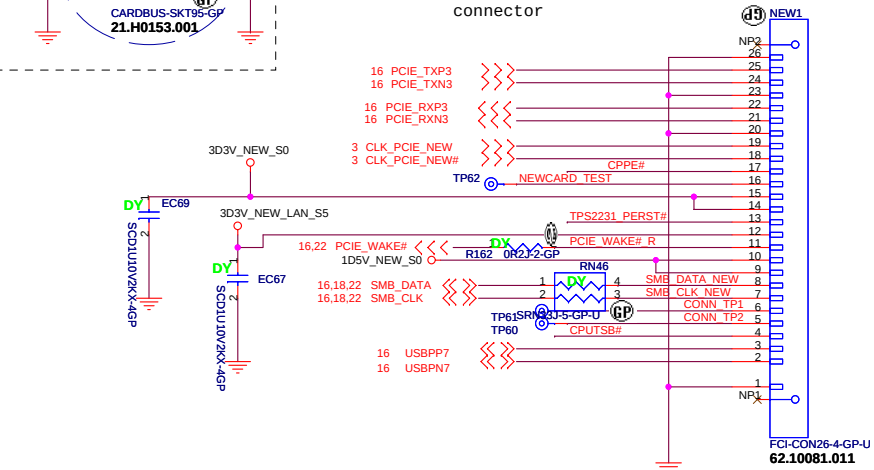
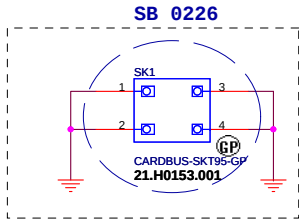
Title			
Graphic MXM CONN			
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Mini Card Connector

NEWCARD Connector

Reserve the symbol
for bottom side
connector



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Title	
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MINI CARD / NEW CARD

Size

Document Number

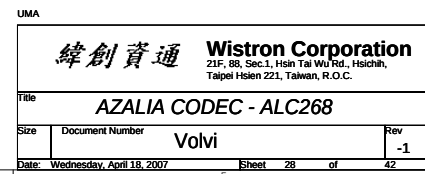
Volvi

Rev

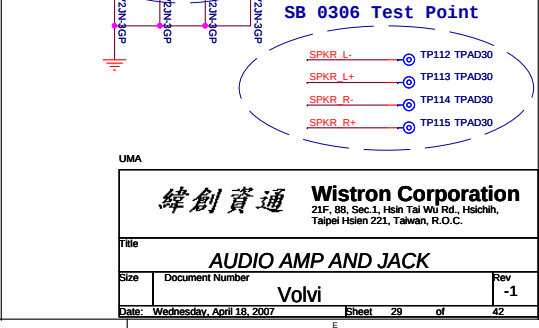
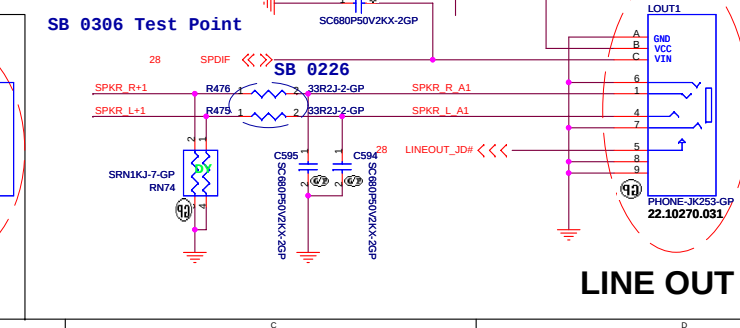
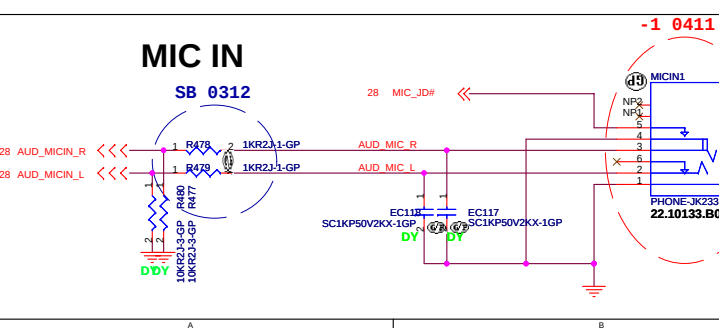
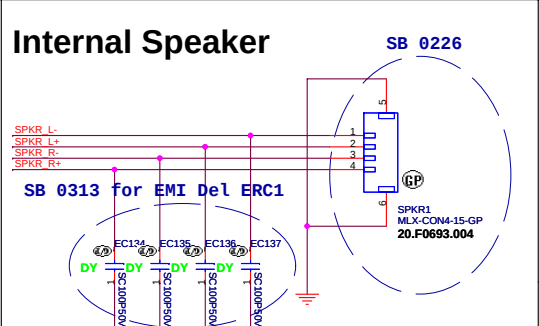
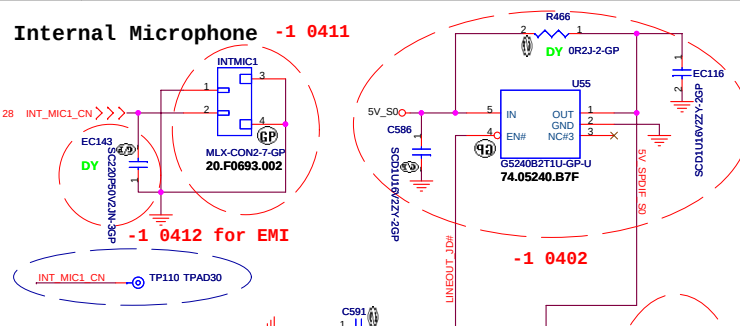
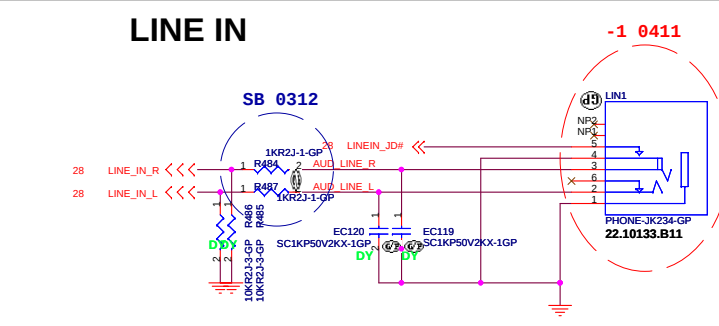
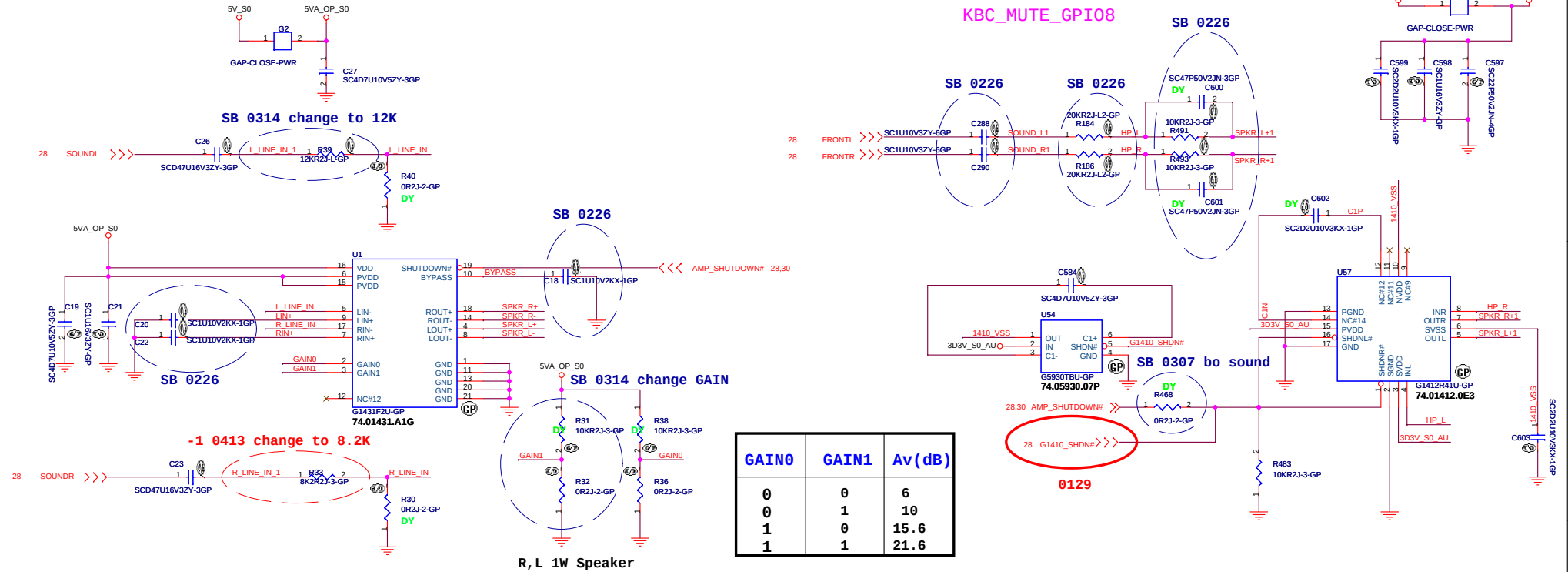
Date: Wednesday, April 18, 2007

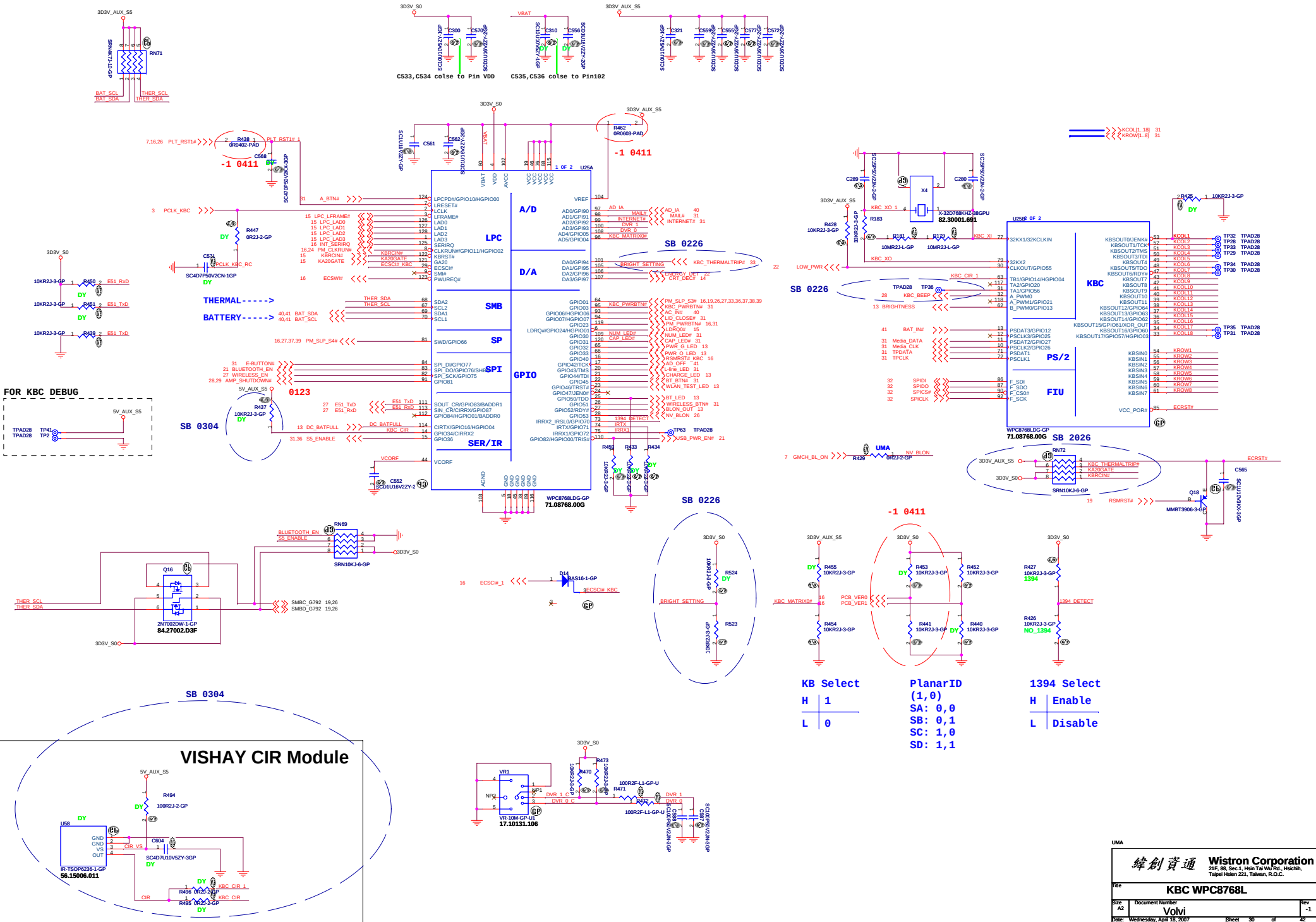
Sheet 27

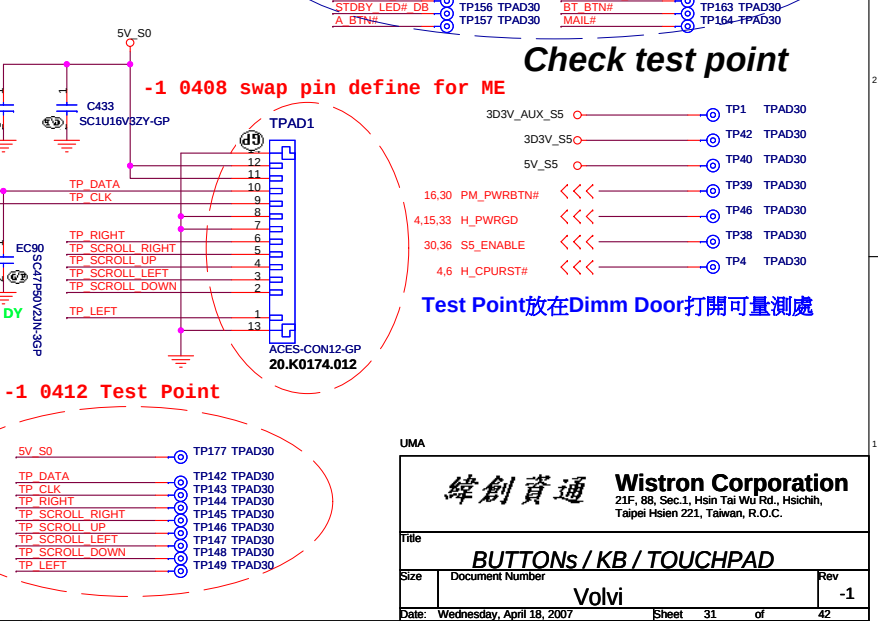
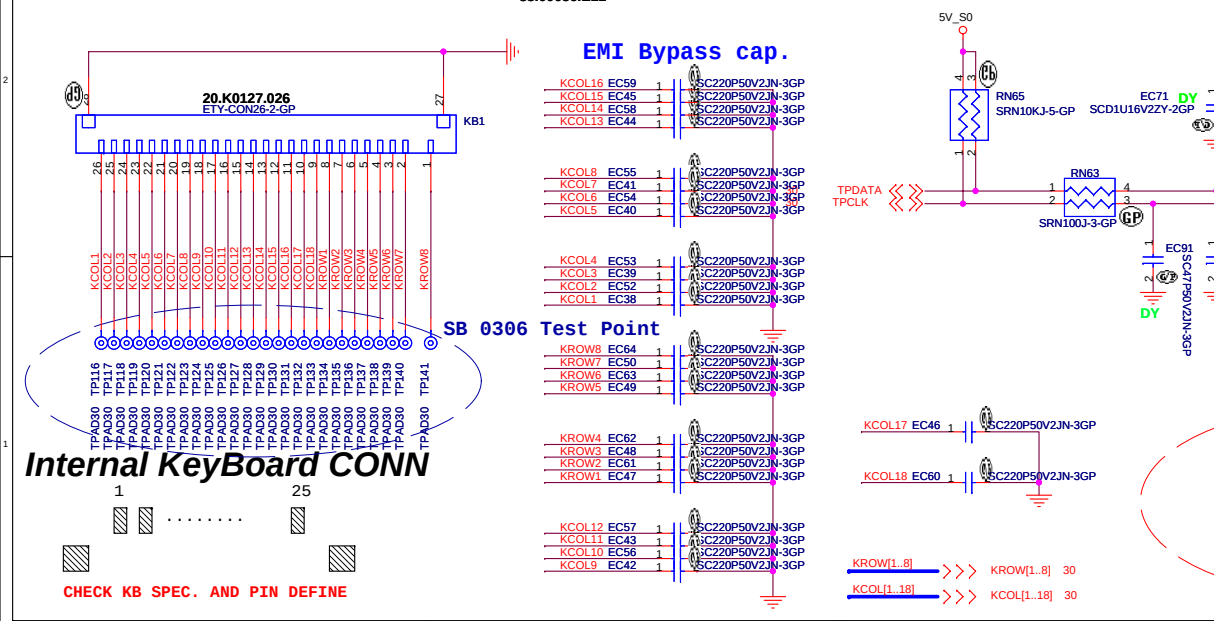
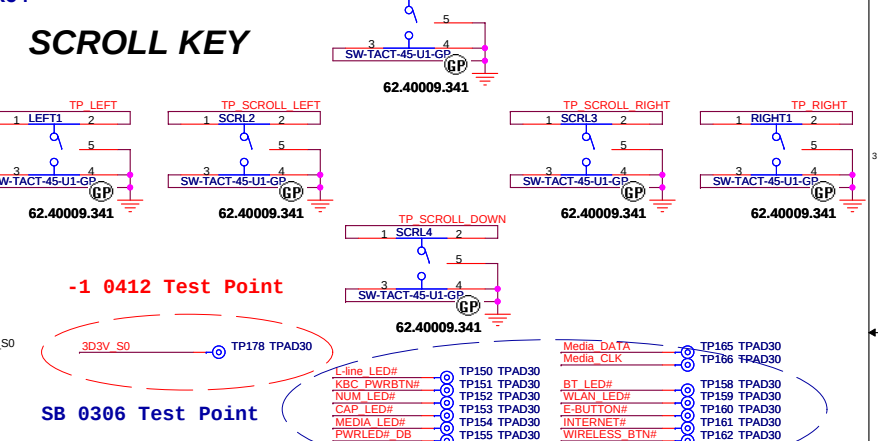
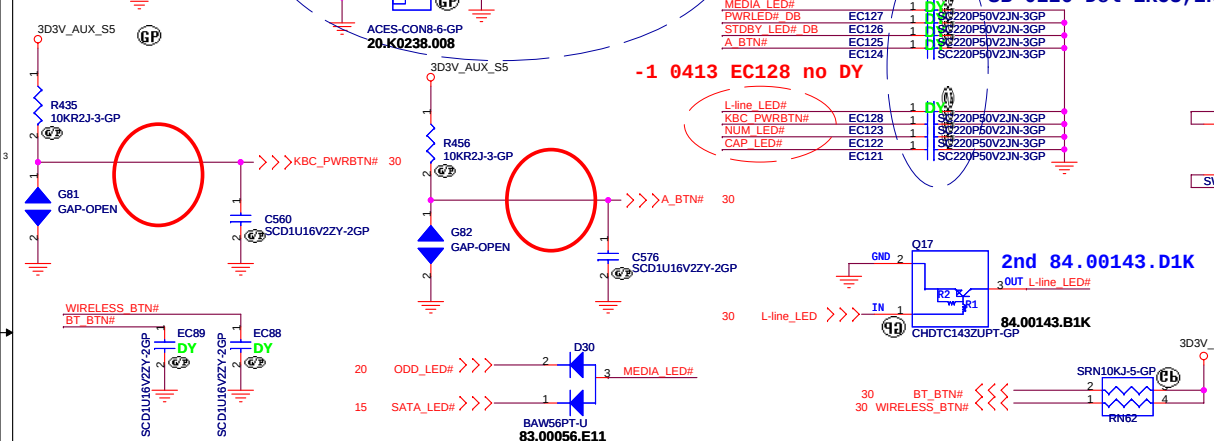
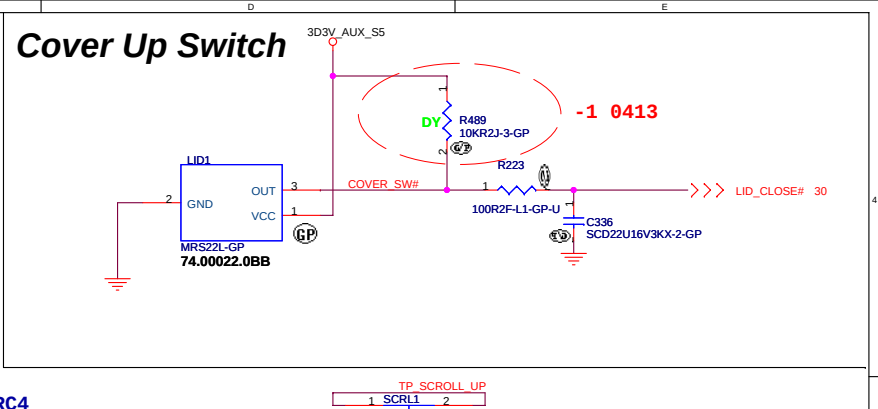
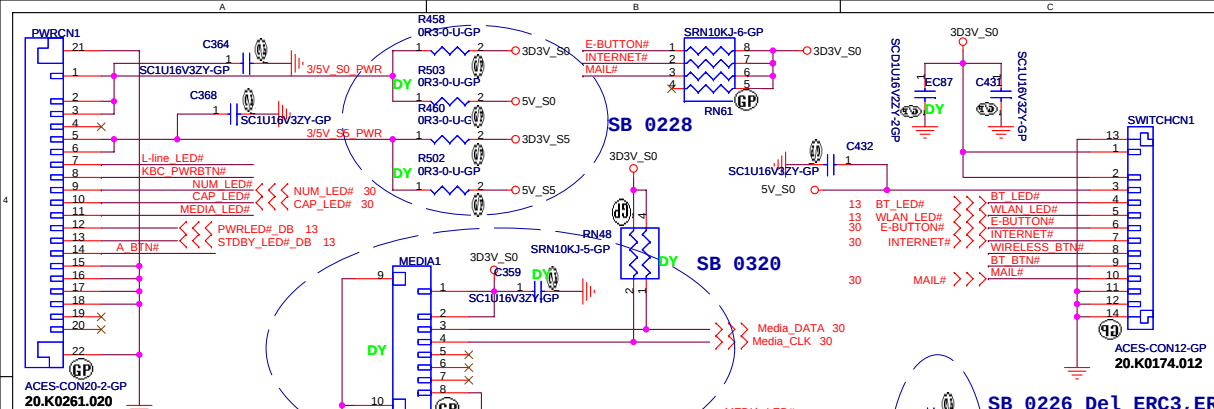
42

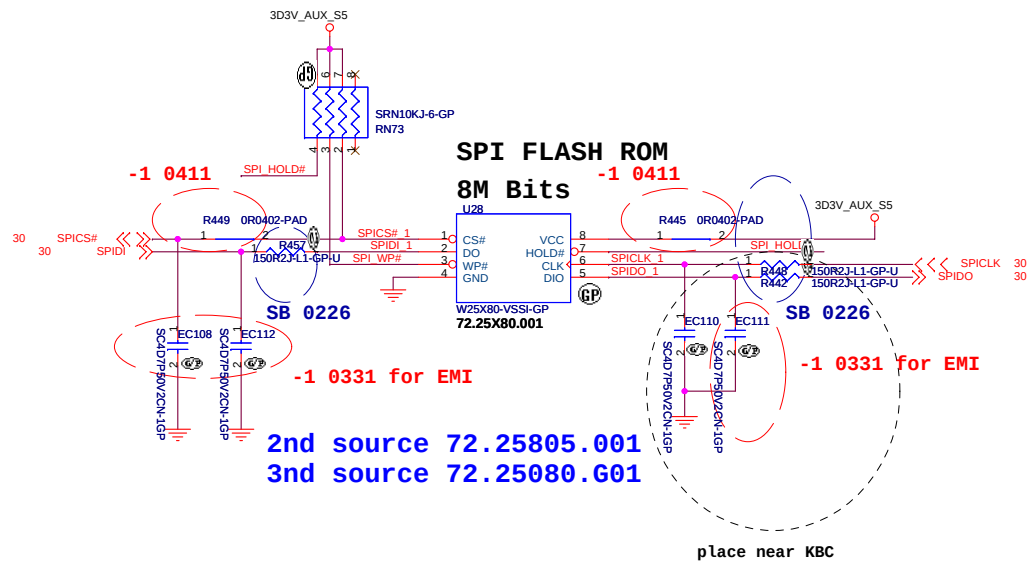


AUDIO OP AMPLIFIER





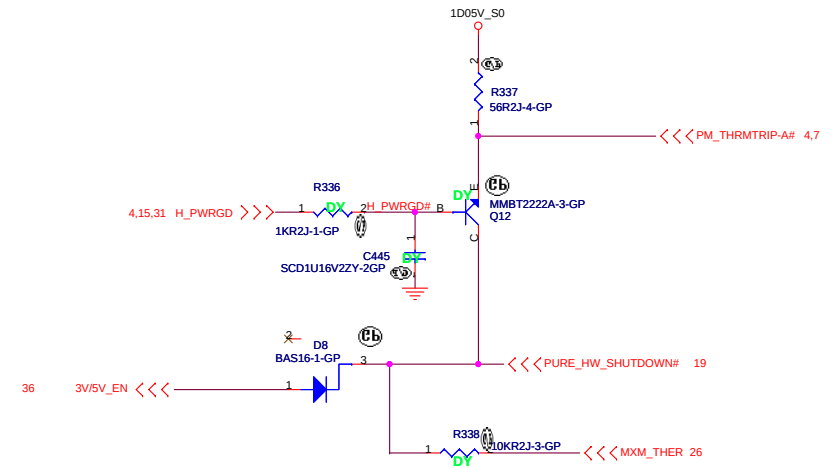




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Title BIOS		
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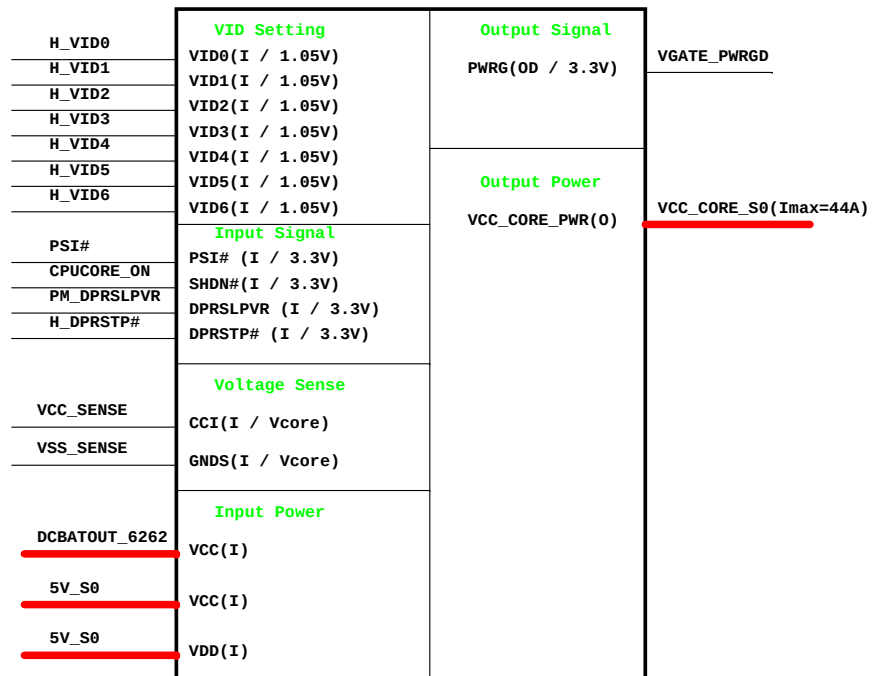
3D3V_AUX_S5



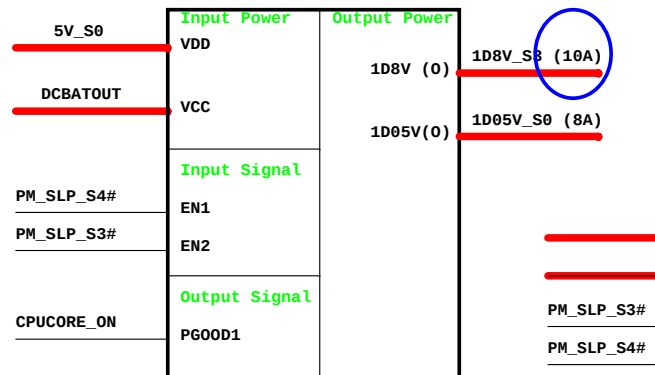
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Title				<i>RUN POWER and 3D3V_AUX_S5</i>			
Size		Document Number				Rev	
		Volvi				-1	
Date: Wednesday, April 18, 2007				Sheet 33 of		42	

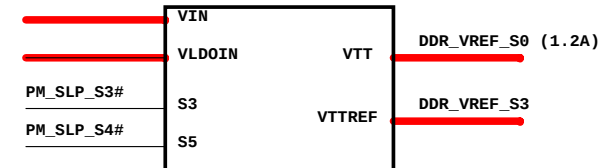
CPU_CORE
MAX8770



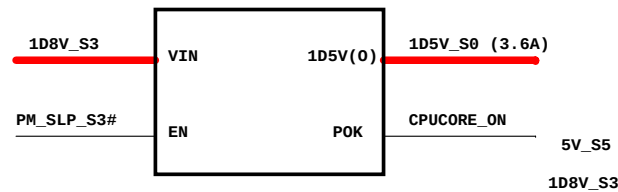
MAX8717
1D8V_S3 / 1D05V_S0



TPS51100
DDR_VREF_S0



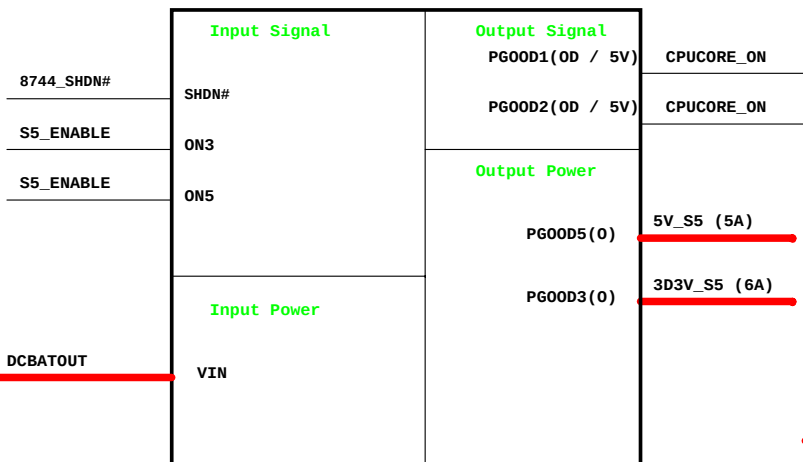
APL5912
1D5V_S0



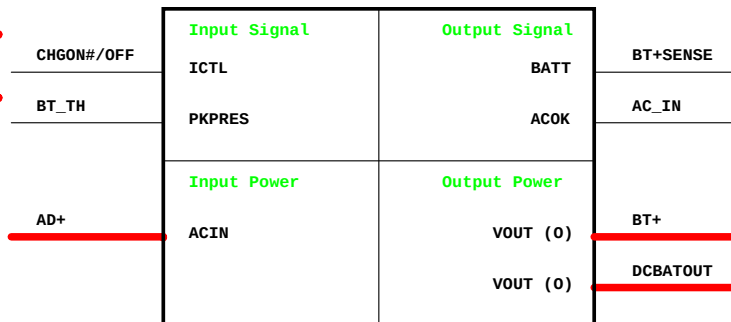
APL5312
2D5V_S0



MAX8744
5V_S5 / 3D3V_S5

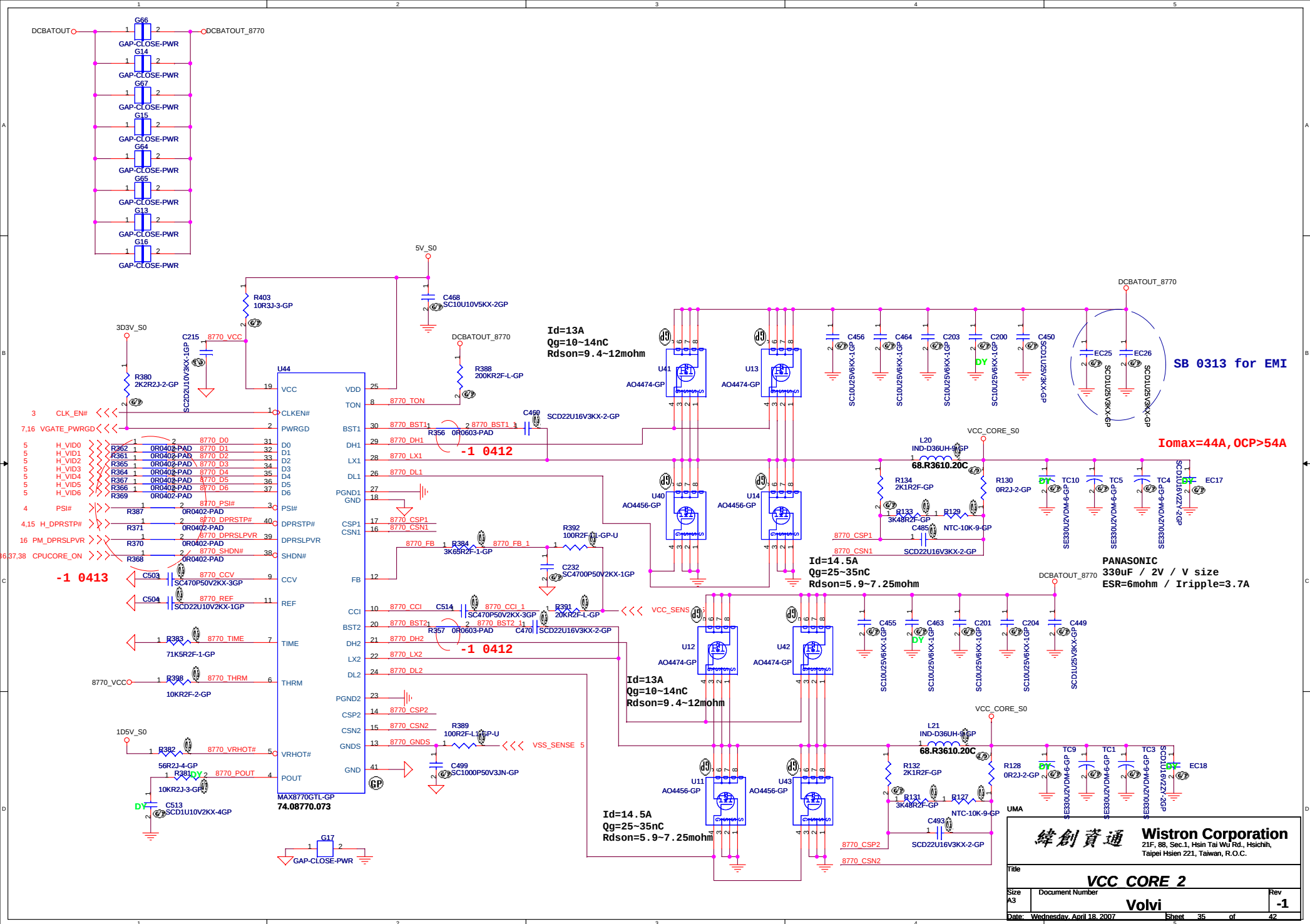


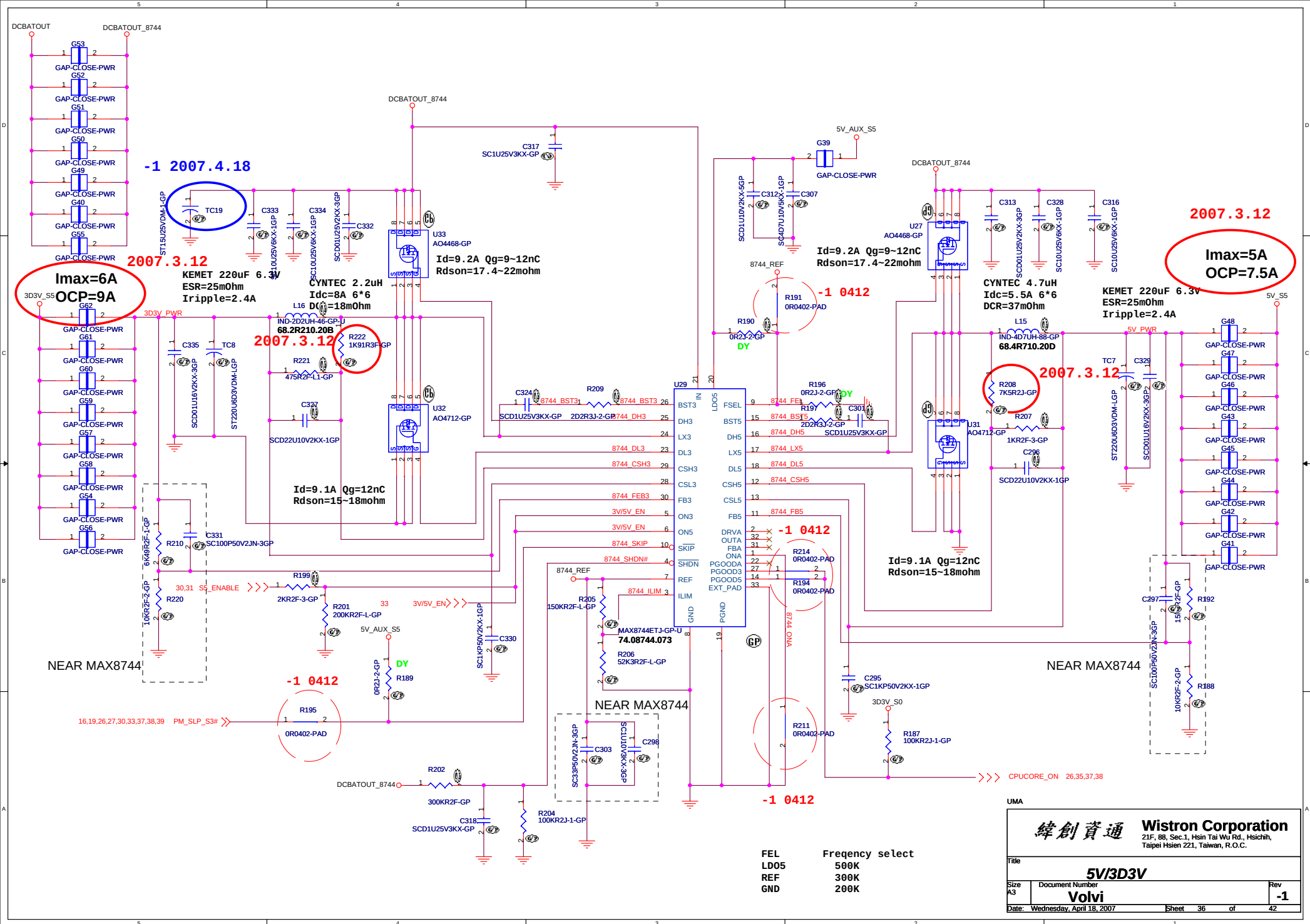
Charger MAX8731A

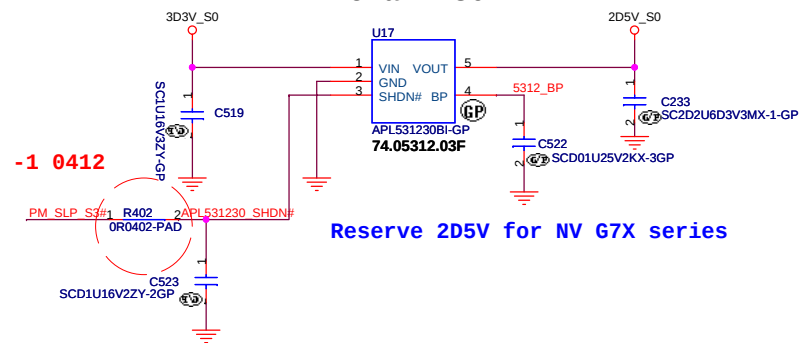
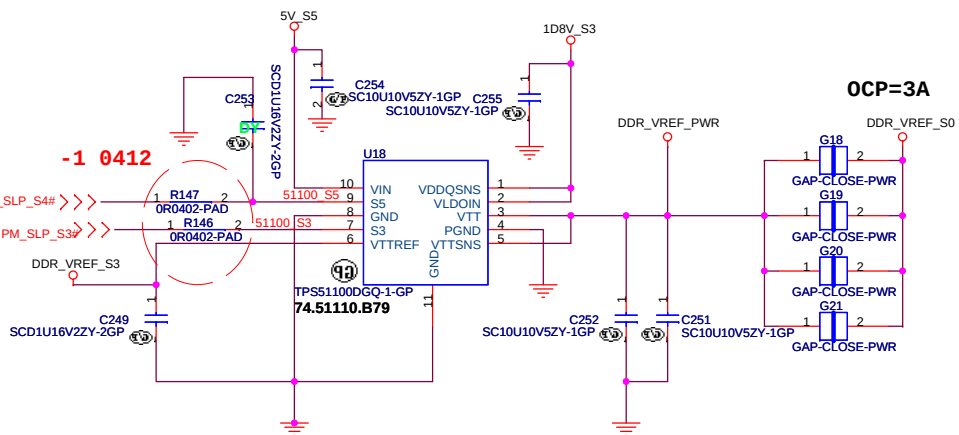


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Title Power Block Diagram	
Size A3	Document Number
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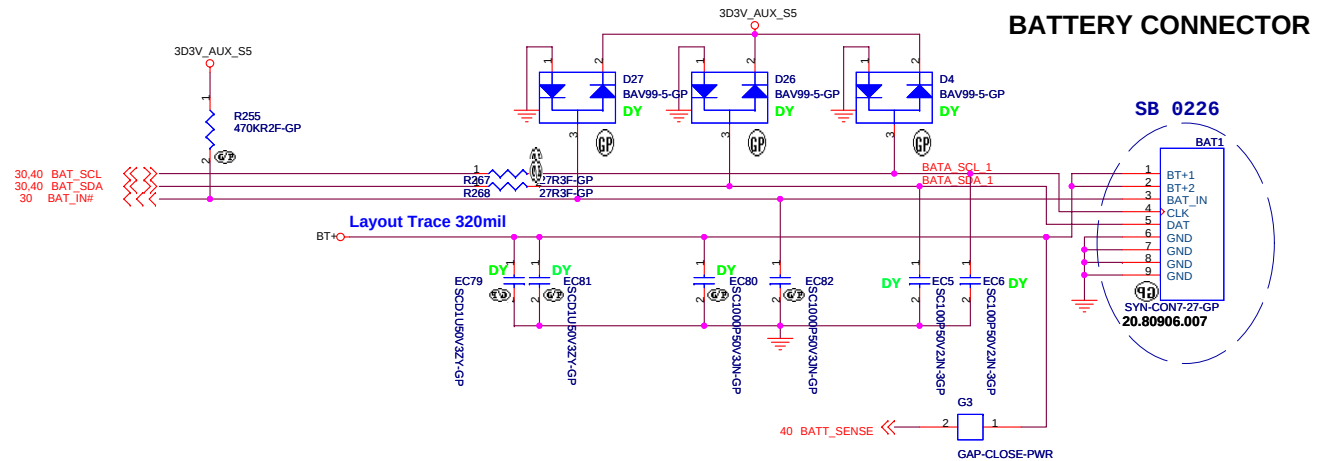
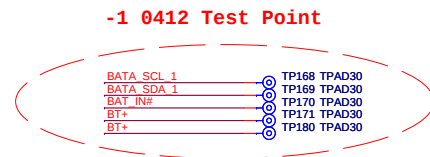
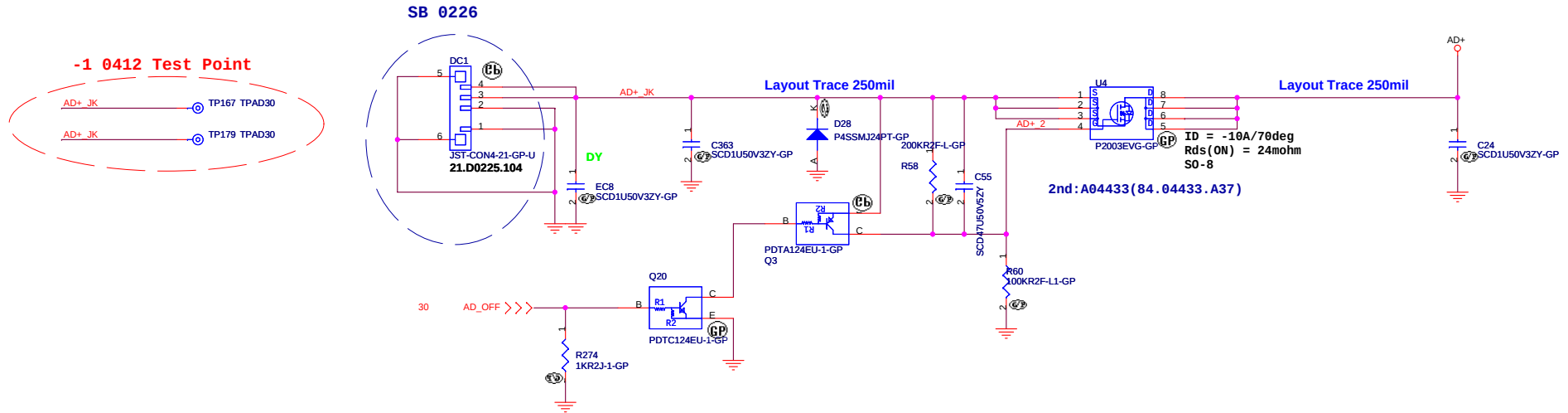






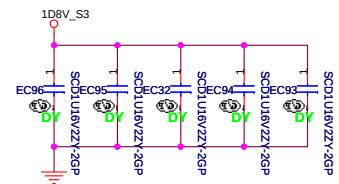
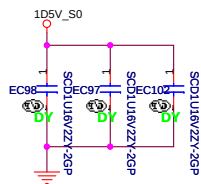
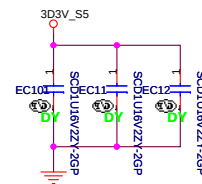
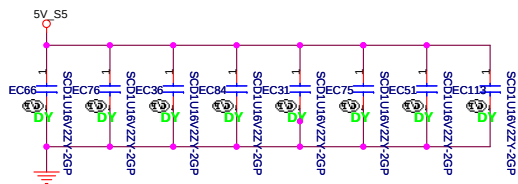
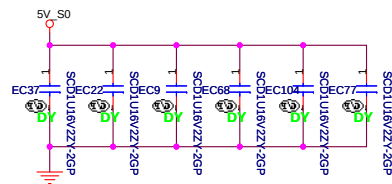
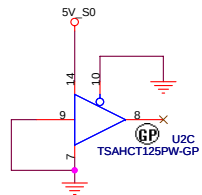
Reserve 2D5V for NV G7X series

Adaptor in to generate DCBATOUT

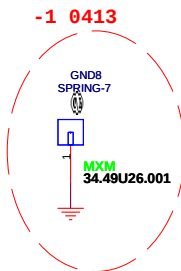
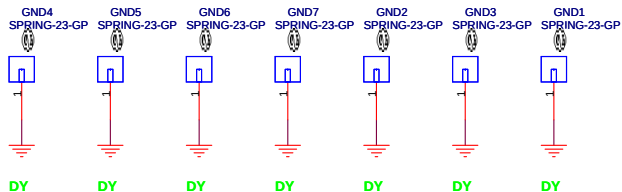
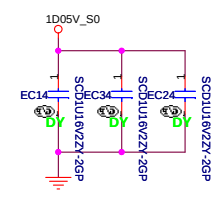
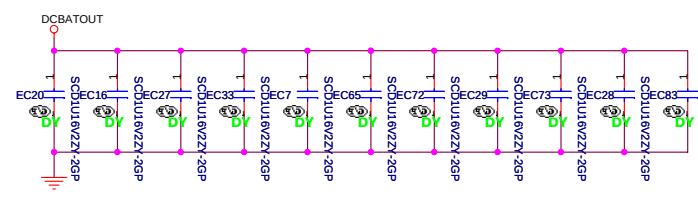
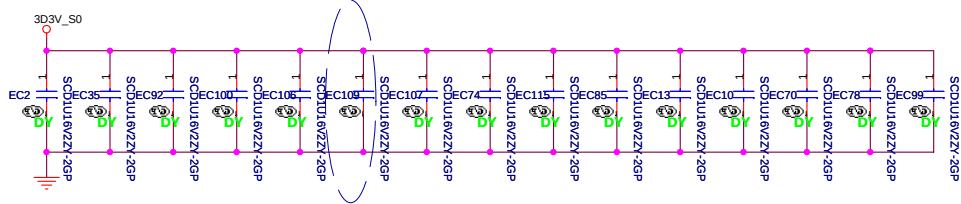


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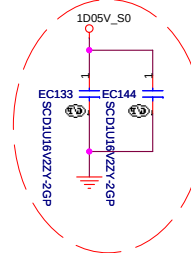
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SB 0312 for EMI

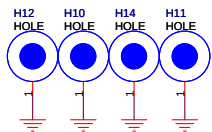


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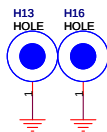


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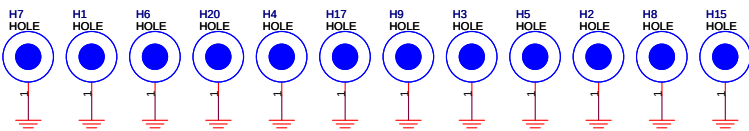
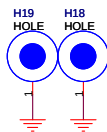
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