Volvi2 Block Diagram

Project code: 91.4X101.001
PCB P/N : 55.4X101.0SA
REVISION : 07220-SA

SA-0606

CLK GEN.
RTM875T-605
(ICS 9LPRS502) 3

Mobile CPU
Merom 479
Celeron M
2.0G : 71.MEROM.A0U
2.33G : 71.MEROM.B0U
4, 5

G792
20

HOST BUS 533/667MHz@1.05V

DDR2
533/667 MHz
12,13

DDR2
533/667 MHz
12,13

533/667MHz

533/667MHz

Intel GL960
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.GL960.00U, SLA5V
6,7,8,9,10,11

SVIDEO/COMP → TVOUT 15

LVDS → 14" WXGA LCD 14

RGB CRT → CRT 15

X4 DMI 400MHz

C-Link0

Audio BD REVISION:07551-SA

MIC In

Codec
ALC268
24

AZALIA

25 INT.MIC

25 INT.SPKR

OP AMP
G1431Q 25

OP AMP
G1412
25

Line Out
(No-SPDIF)

RJ11 22

MODEM
MDC Card
21

ICH8M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
3 SATA
1 PATA 66/100
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)

71.ICH8M.C0U, SLA5Q, B3
16,17,18,19

PCIex1

10/100 LAN
Marvell 88E8039
22

TXFM
22

RJ45
22

Mini Card
abgn/bg 23

New card
23

PWR SW
P2231NFC 23

LPC BUS

KBC
Winbond
WPC8763L 26

SPI I/F

BIOS
W25X80-VSS
27

LPC
DEBUG
CONN. 36

Touch Pad 27

INT. KB 27

SATA

PATA

USB

HDD
21

CDROM
21

USB
1 PORT 21

USB BD
2 PORT
21

REVISION:06628-1

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC
MAX8744 31

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC
TPS51124 32

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(8A) 1D8V_S3(12A)

TPS51100(G2997) 33

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5913 33

1D8V_S3	1D25V_S0 (1.5A)

G909 28

5V_AUX_S5	3D3V_AUX_S5 (100mA)

APL5915 33

1D8V_S3	1D5V_S0 (1.5A)

CHARGER
MAX8731 34

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
MAX8770 30

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	Volvi2	SA

Date: Wednesday, June 06, 2007 Sheet 1 of 36

ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCIE Routing

LANE1	LAN Marvell
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	NC
6	NC
7	MINICARD
8	CCD
9	NEW1

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K ?
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K ?
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

2007/05/02
1 Based on Tahoe to modify schematics.
==========
2007/05/14
1.Page 34:Replace "D25" with "BAS16-1-GP".
2.Page 27:Replace "R485" with "2K7R2j".
3.Page 27:DY:C379"
4.Page 27:Add "C682" D1u capacitor on "LID1.PIN1"
5.Page 27:Replace "R238" with "0R2".
6.Page 25:Replace "INTMIC1" & "SPKR1" with main source follow connector list.
7.Page 5:Add C115, C116, C141, C149, C169, C171 for Colay with TC25.
8.Page 10:Replace "L20" with "68.00217.141".
9.Page 10:Replace "L10" & "L23" with "68.00217.101"
==========

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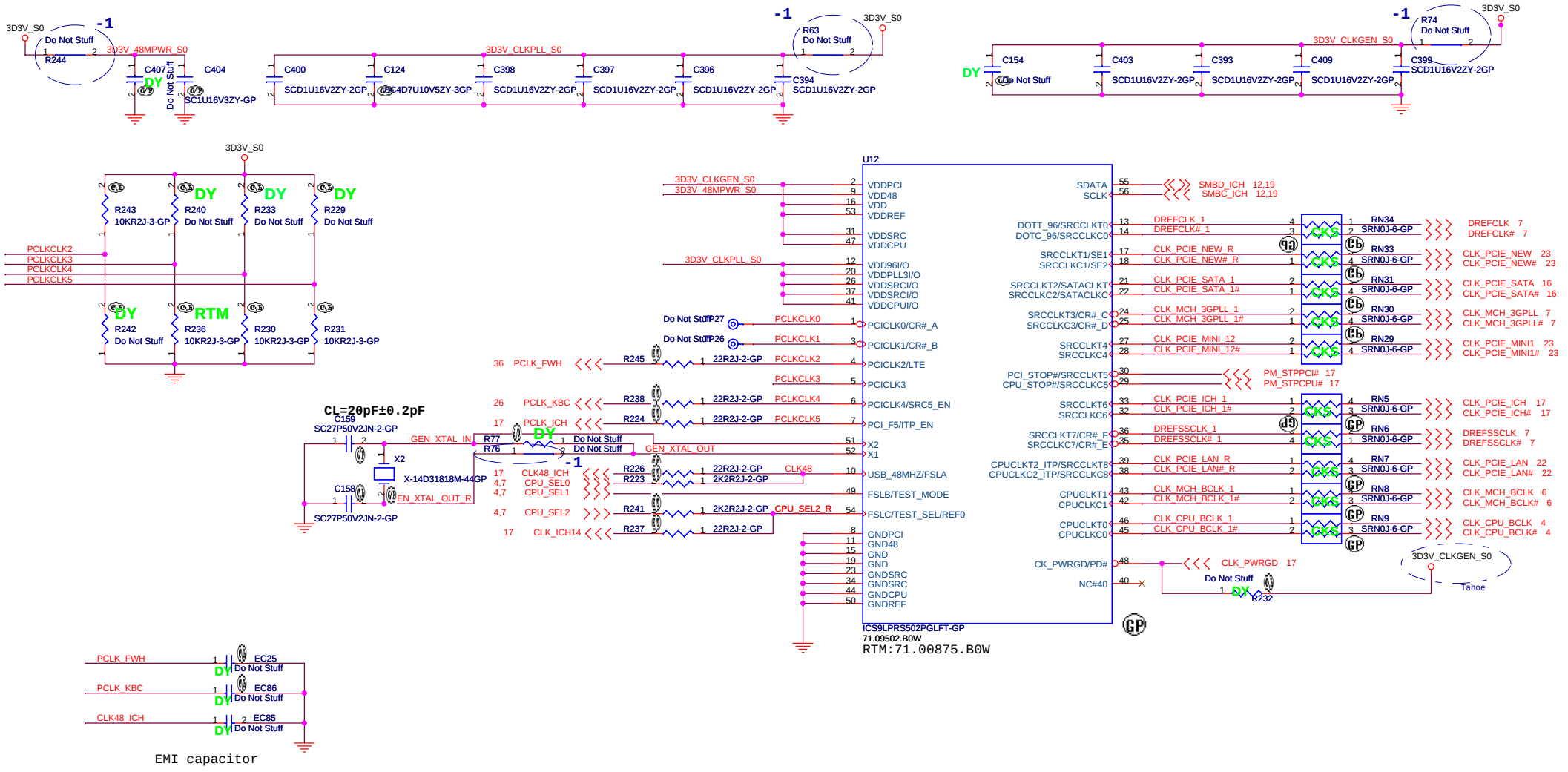
Title: Reference

Size: A3 | Document Number: Volvi2 | Rev: SA

Date: Wednesday, June 06, 2007 | Sheet 2 of 36



ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

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Title: Clock Generator

Size	Document Number	Rev
	Volvi2	SA

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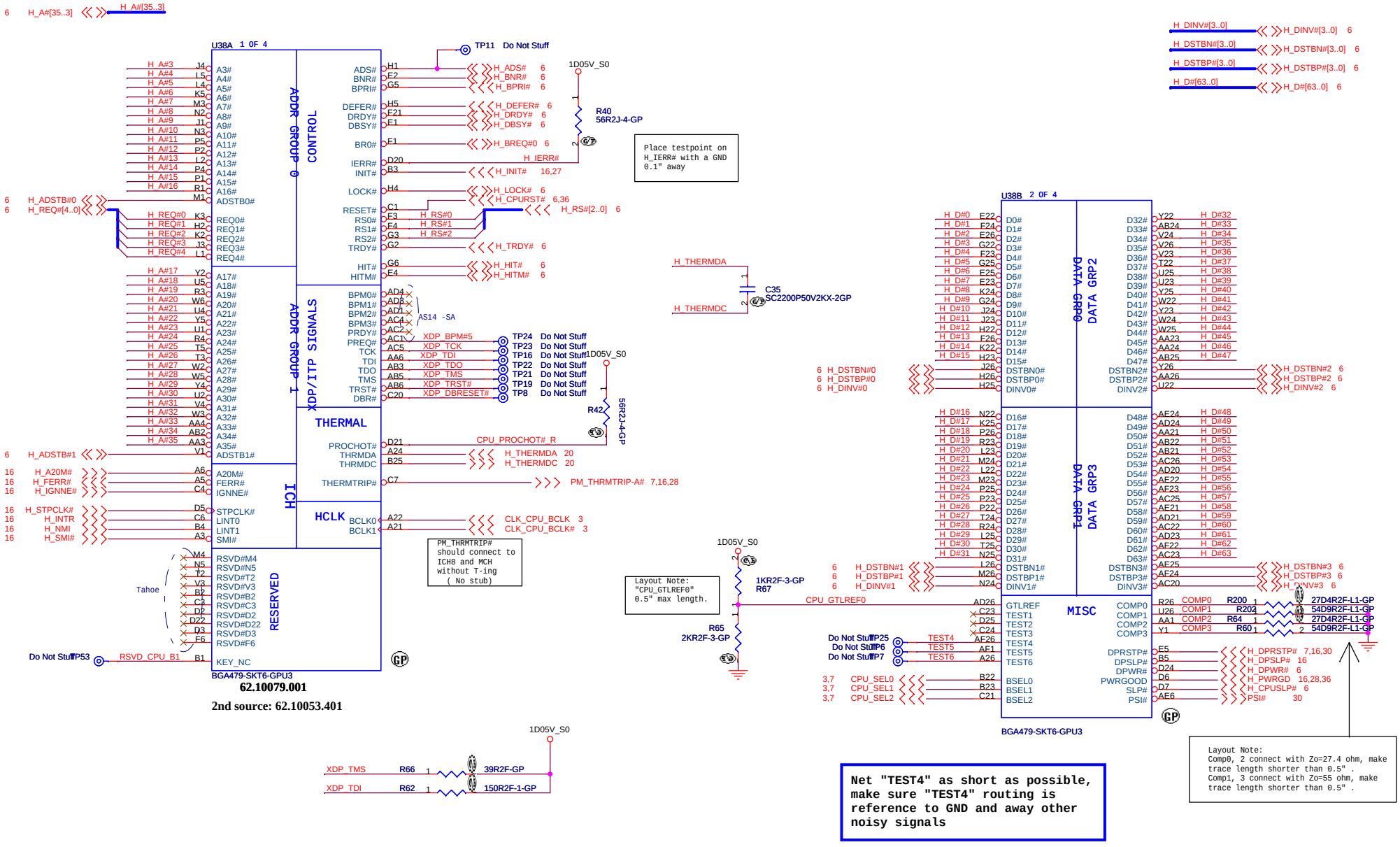

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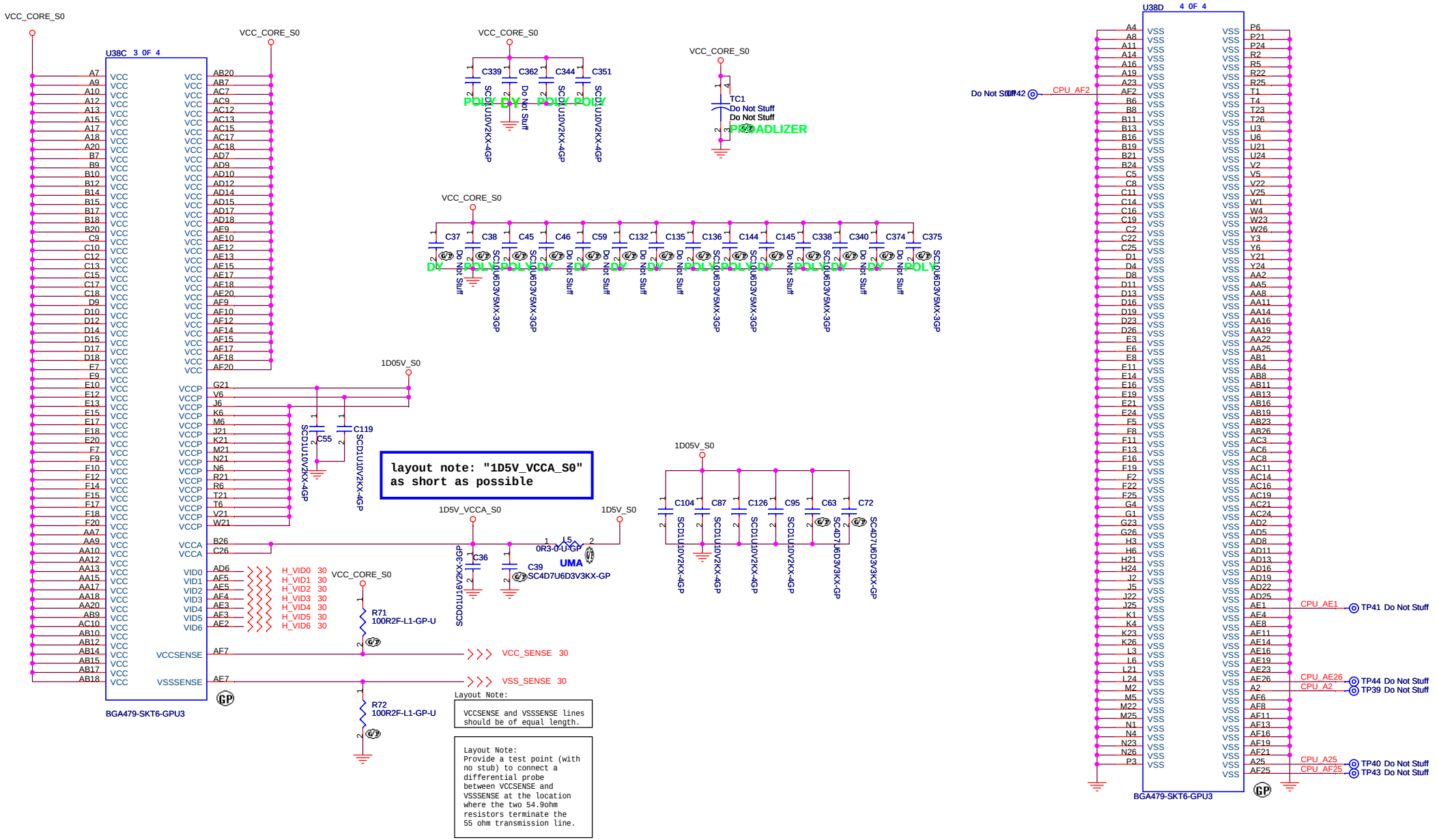
Title: CPU (1 of 2)

Size | Document Number: Volvi2 | Rev: SA

Date: Wednesday, June 06, 2007 | Sheet 4 of 36



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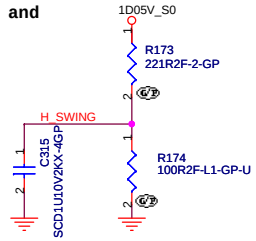
Title	***CPU (2 of 2)***
Size	Document Number: **Volvi2**
Rev	SA
Date:	Wednesday, June 06, 2007
Sheet	5 of 36

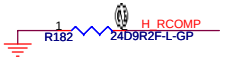
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



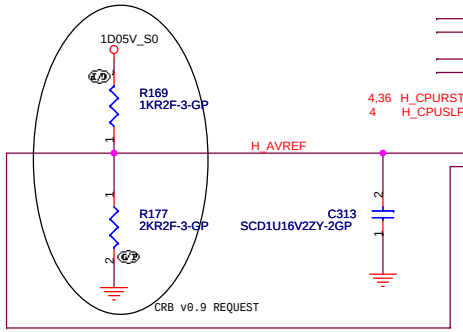
H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

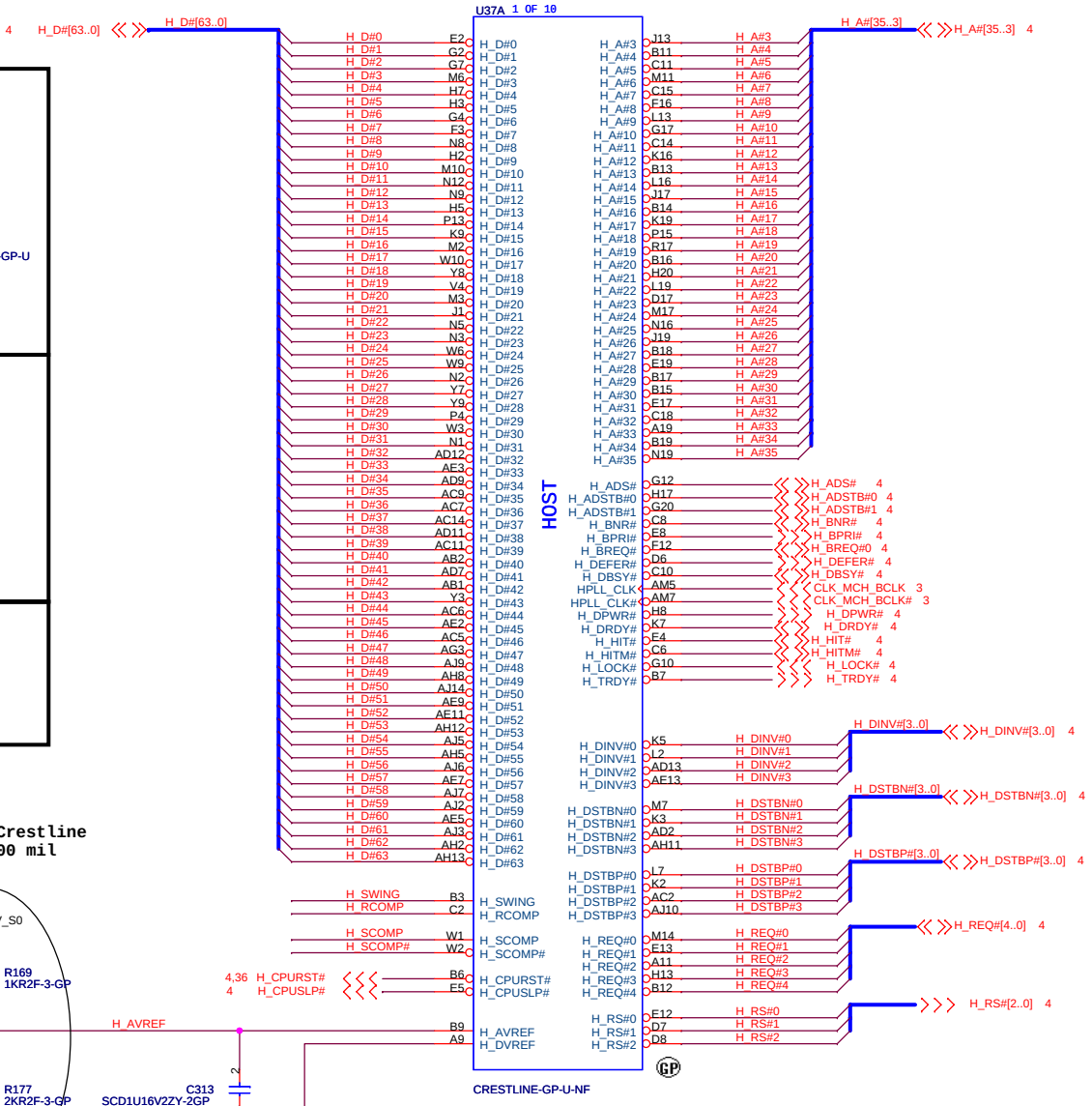
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil





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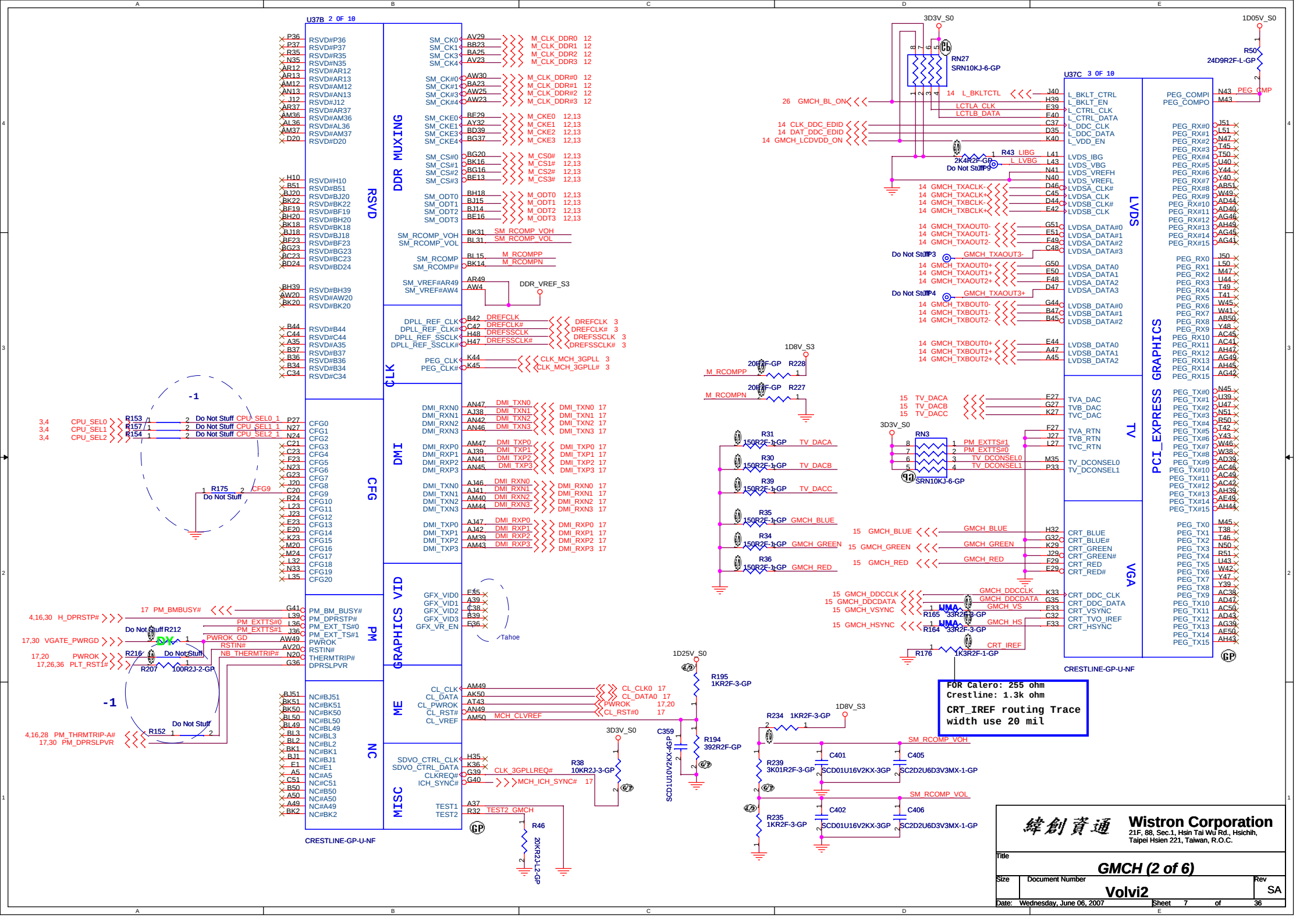
Title	GMCH (1 of 6)	
Size	Document Number: Volvi2	Rev: SA
Date: Wednesday, June 06, 2007	Sheet 6 of 36	


U37B 2 OF 10
RSVD
DDR MUXING
CLK
CFG
DMI
GRAPHICS VID
PM
ME
MISC
NC
CRESTLINE-GP-U-NF
U37C 3 OF 10
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
CRESTLINE-GP-U-NF
Tahoe
RN27 SRN10KJ-6-GP
RN3 SRN10KJ-6-GP
R43 2K4R2F-GP
R50 24D9R2F-L-GP
R31 150R2F-1-GP TV_DACA
R30 150R2F-1-GP TV_DACB
R39 150R2F-1-GP TV_DACC
R35 150R2F-1-GP GMCH_BLUE
R34 150R2F-1-GP GMCH_GREEN
R36 150R2F-1-GP GMCH_RED
R165 33R2F-3-GP
R164 33R2F-3-GP
R176 1K3R2F-1-GP
R195 1KR2F-3-GP
R194 392R2F-GP
R234 1KR2F-3-GP
R239 3K01R2F-3-GP
R235 1KR2F-3-GP
R38 10KR2J-3-GP
R46 20KR2J-L2-GP
C359 SCD1U10V2KX-4GP
C401 SCD01U16V2KX-3GP
C405 SC2D2U6D3V3MX-1-GP
C402 SCD01U16V2KX-3GP
C406 SC2D2U6D3V3MX-1-GP
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
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Title: GMCH (2 of 6)
Size: Document Number: Volvi2
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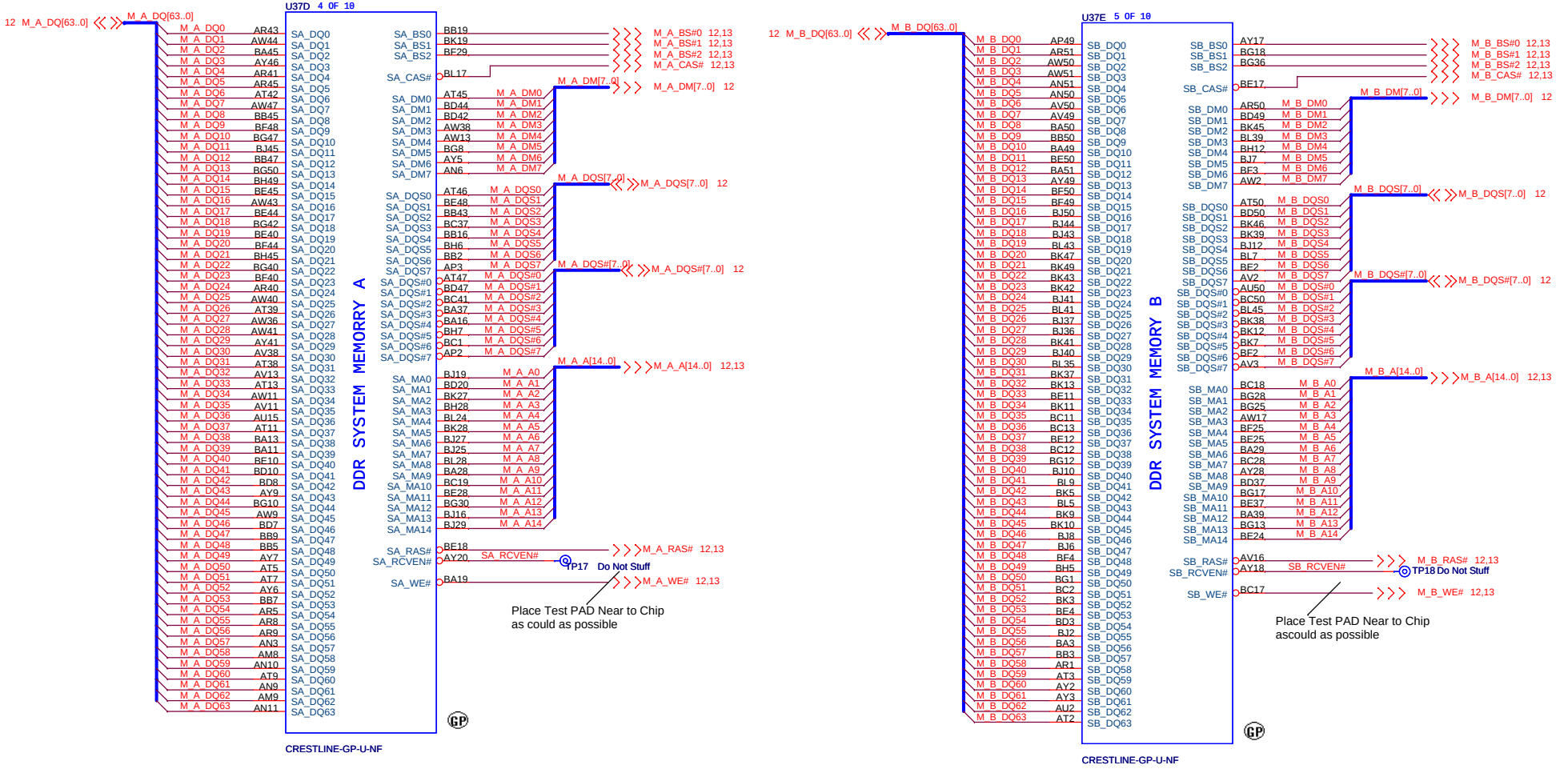

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Title	***GMCH (3 of 6)***	
Size	Document Number **Volvi2**	Rev SA
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VCC_NCTF + VCC=1573mA

FOR VCC CORE

1573mA

1D05V_S0

U37F 6 OF 10

VCC CORE

Coupling CAP 370 mils from the Edge

POWER

1D8V_S3

3138mA

FOR VCC SM

Place CAP where LVDS and DDR2 taps

Place on the Edge

VCC SM

VCC GFX NCTF

VCC_AXG_NCTF + VCC_AXG=7700mA

UMA

VCC GFX

VCC SM LF

CRESTLINE-GP-U-NF

FOR VCC CORE AND VCC NCTF

308 mils from the Edge

Coupling CAP

U37G 7 OF 10

VCC NCTF

VSS NCTF

POWER

VSS SCB

TP84 TP47 TP46 TP45 TP92 TP85 Do Not Stuff

1D05V_S0 Tahoe

VSS AXM

FOR VCC AXM NCTF AND VCC AXM

VCC_AXM_S0

Place on the Edge

Coupling CAP

VCC_AXM_NCTF + VCC_AXM=540mA

VSS AXM NCTF

CRESTLINE-GP-U-NF

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Title: GMCH (4 of 6)

Size: | Document Number: Volvi2 | Rev: SA

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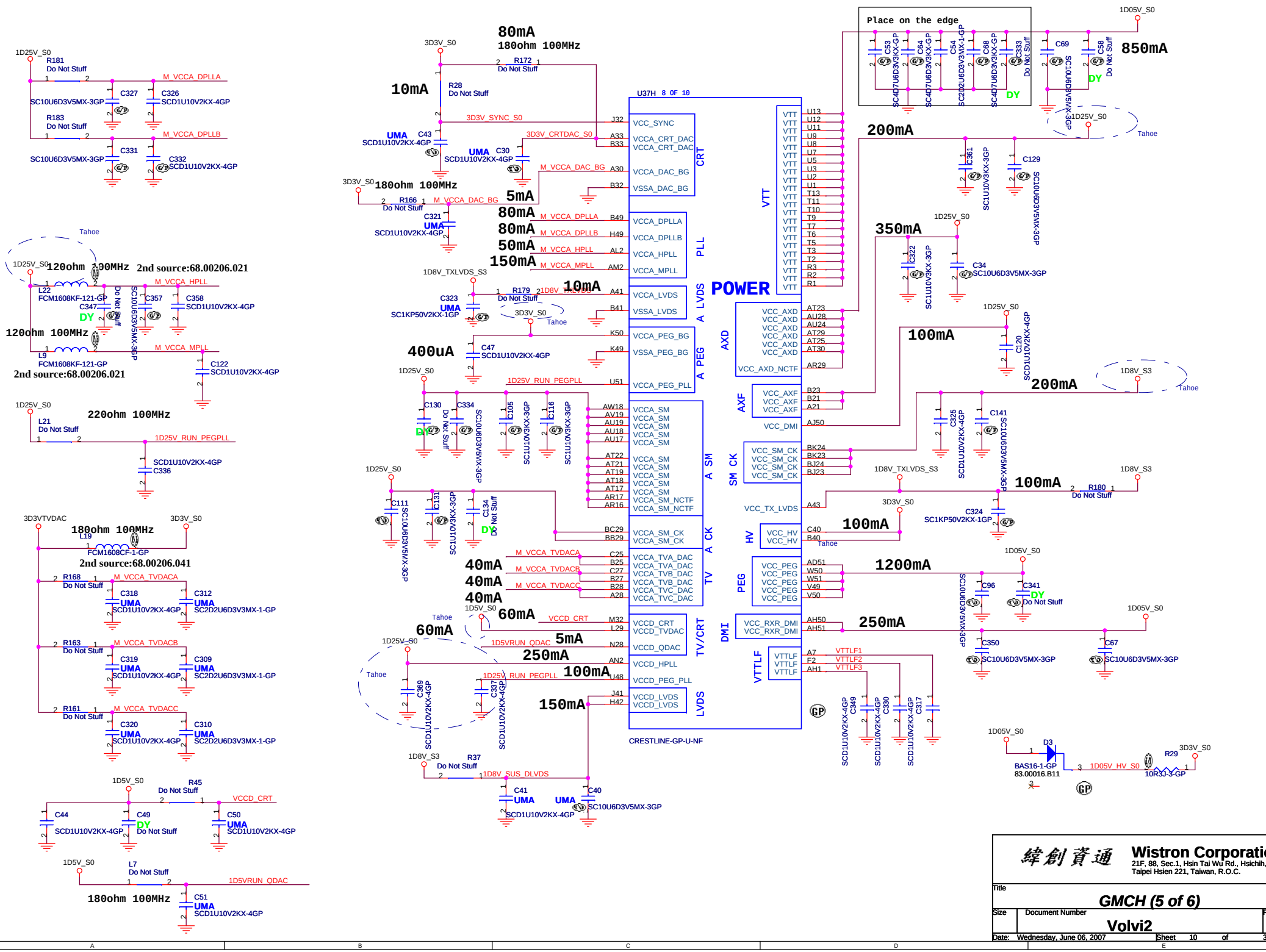

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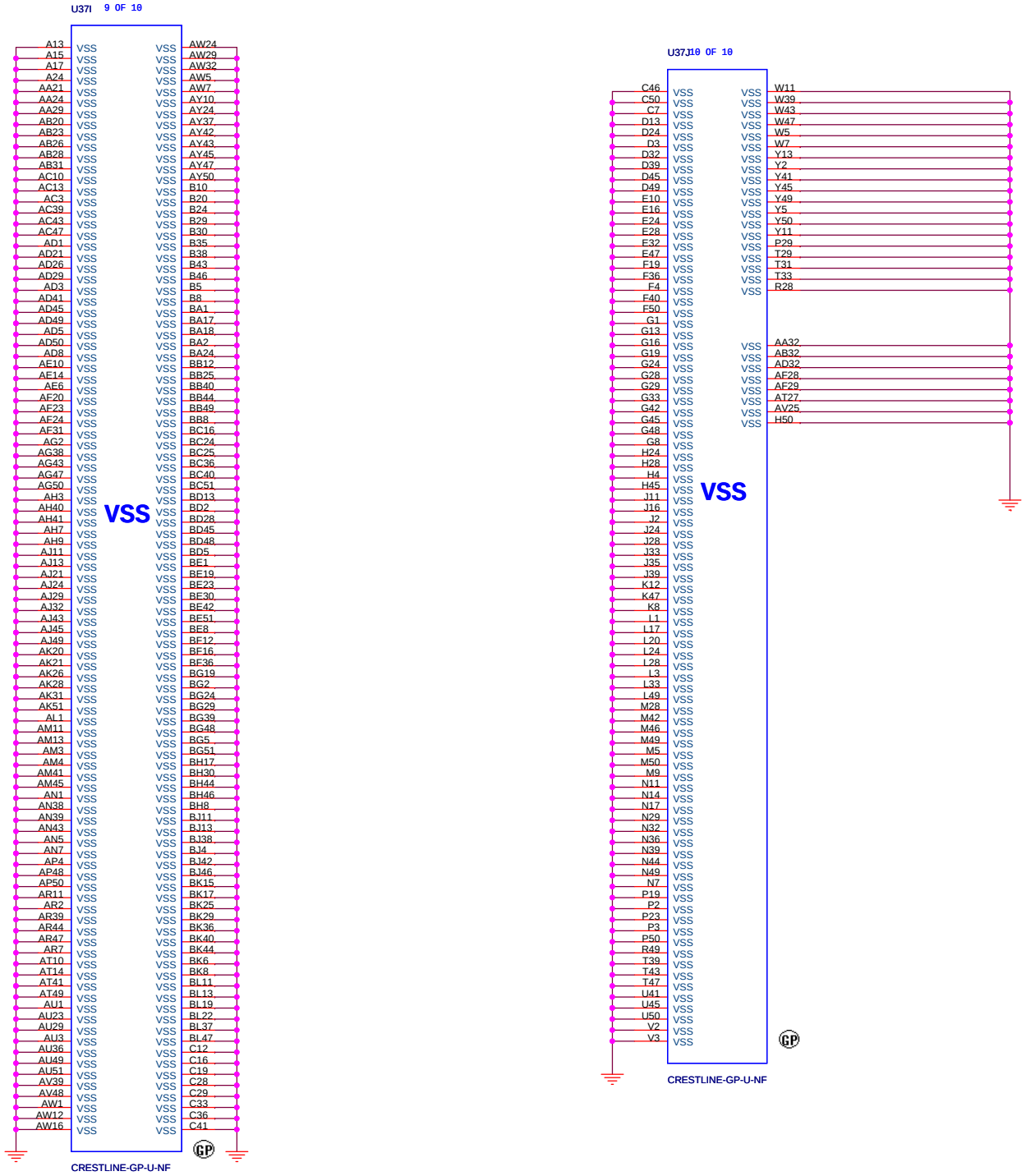
Title	***GMCH (5 of 6)***	
Size	Document Number **Volvi2**	Rev SA
Date: Wednesday, June 06, 2007	Sheet 10 of 36	



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Title: ***GMCH (6 of 6)***

Size	Document Number	Rev
	Volvi2	SA

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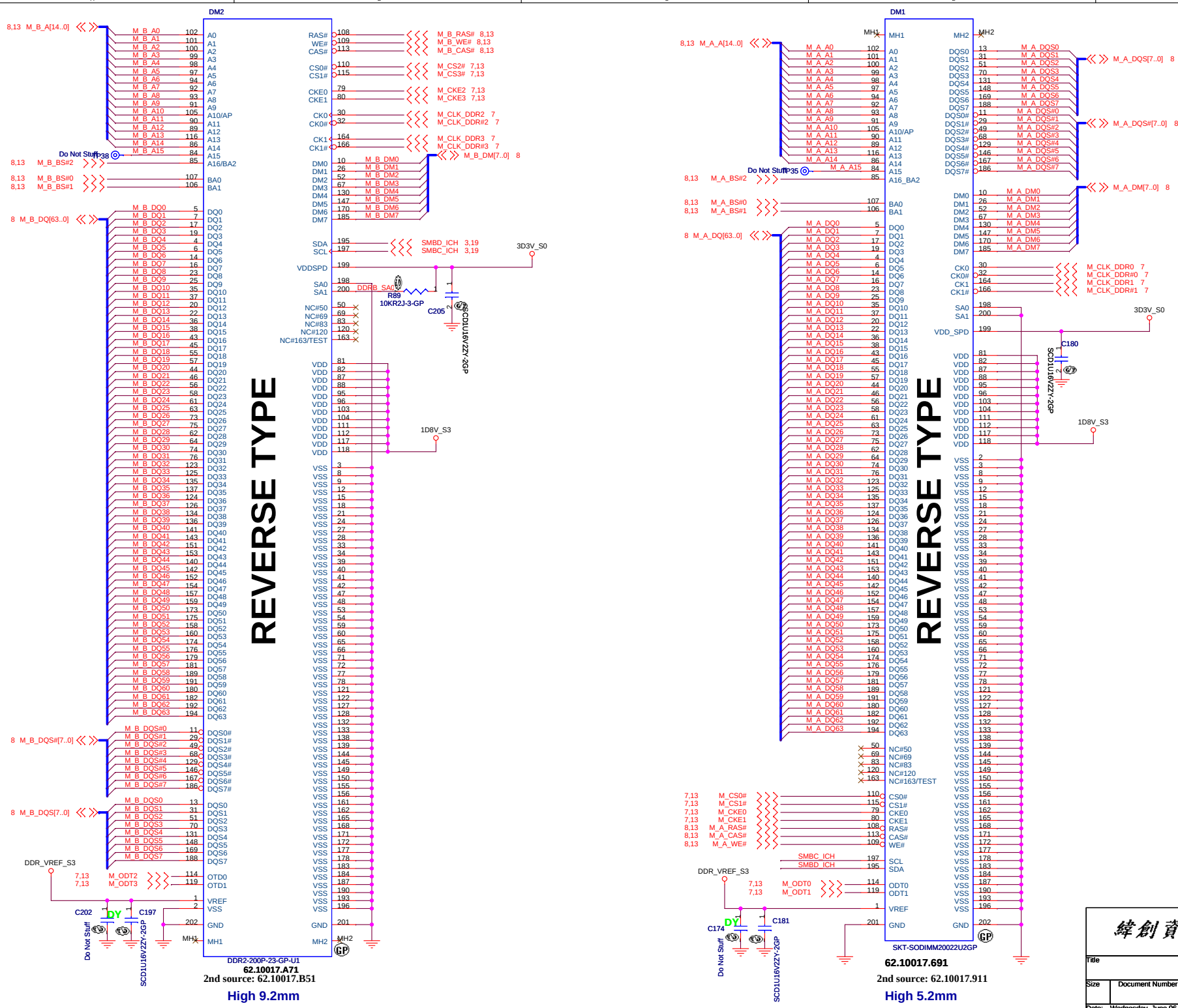

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Title: DDR2 Socket

Size: | Document Number: Volvi2 | Rev: SA

Date: Wednesday, June 06, 2007 | Sheet 12 of 36

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN10 — SRN56J-5-GP
- M_CKE0 7,12
- M_CKE1 7,12
- M_A_BS#2 8,12
- M_A_A12

RN18 — SRN56J-5-GP
- M_B_A8
- M_B_A9
- M_B_A5

RN17 — SRN56J-5-GP
- M_CKE2 7,12
- M_CKE3 7,12
- M_B_BS#2 8,12
- M_B_A12

RN19 — SRN56J-5-GP
- M_B_A3
- M_B_A1
- M_B_A10
- M_B_WE# 8,12

RN23 — SRN56J-5-GP
- M_B_A13
- M_ODT2 7,12
- M_ODT3 7,12
- M_B_RAS# 8,12

RN22 — SRN56J-5-GP
- M_B_BS#1 8,12
- M_B_A2
- M_B_A0
- M_B_A4

RN21 — SRN56J-5-GP
- M_B_A14
- M_B_A6
- M_B_A7
- M_B_A11

RN20 — SRN56J-5-GP
- M_B_BS#0 8,12
- M_B_CAS# 8,12
- M_CS3# 7,12
- M_CS2# 7,12

RN16 — SRN56J-5-GP
- M_A_A13
- M_ODT0 7,12
- M_CS0# 7,12
- M_A_RAS# 8,12

RN15 — SRN56J-5-GP
- M_A_BS#1 8,12
- M_A_A0
- M_A_A2
- M_A_A4

RN13 — SRN56J-5-GP
- M_A_CAS# 8,12
- M_CS1# 7,12
- M_ODT1 7,12

RN11 — SRN56J-5-GP
- M_A_A9
- M_A_A8
- M_A_A5
- M_A_A3

RN14 — SRN56J-5-GP
- M_A_A6
- M_A_A7
- M_A_A11
- M_A_A14

RN12 — SRN56J-5-GP
- M_A_A1
- M_A_A10
- M_A_BS#0 8,12
- M_A_WE# 8,12

M_A_A[14..0] — M_A_A[14..0] 8,12

M_B_A[14..0] — M_B_A[14..0] 8,12

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C166 Do Not Stuff DY
C167 Do Not Stuff DY
C168 SCD1U16V2ZY-2GP
C169 SCD1U16V2ZY-2GP
C178 SCD1U16V2ZY-2GP
C179 Do Not Stuff DY
C183 SCD1U16V2ZY-2GP
C184 SCD1U16V2ZY-2GP
C190 Do Not Stuff DY
C191 SCD1U16V2ZY-2GP
C192 Do Not Stuff DY

C193 SCD1U16V2ZY-2GP
C194 SCD1U16V2ZY-2GP DY
C195 Do Not Stuff DY
C203 Do Not Stuff DY
C204 Do Not Stuff DY
C207 SCD1U16V2ZY-2GP
C208 Do Not Stuff DY
C212 Do Not Stuff DY
C213 SCD1U16V2ZY-2GP
C214 Do Not Stuff DY
C215 Do Not Stuff DY

Place these Caps near DM1

1D8V_S3

C427 SC2D2U6D3V3MX-1-GP
C187 SC2D2U6D3V3MX-1-GP
C428 SC2D2U6D3V3MX-1-GP
C188 SC2D2U6D3V3MX-1-GP
C426 SC2D2U6D3V3MX-1-GP

C165 Do Not Stuff DY
C177 Do Not Stuff DY
C182 Do Not Stuff DY
C185 Do Not Stuff DY

Place these Caps near DM2

1D8V_S3

C199 SC2D2U6D3V3MX-1-GP
C216 SC2D2U6D3V3MX-1-GP
C200 SC2D2U6D3V3MX-1-GP
C209 SC2D2U6D3V3MX-1-GP
C217 SC2D2U6D3V3MX-1-GP

C210 Do Not Stuff DY
C198 Do Not Stuff DY
C211 Do Not Stuff DY
C196 Do Not Stuff DY

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
	Volvi2	SA

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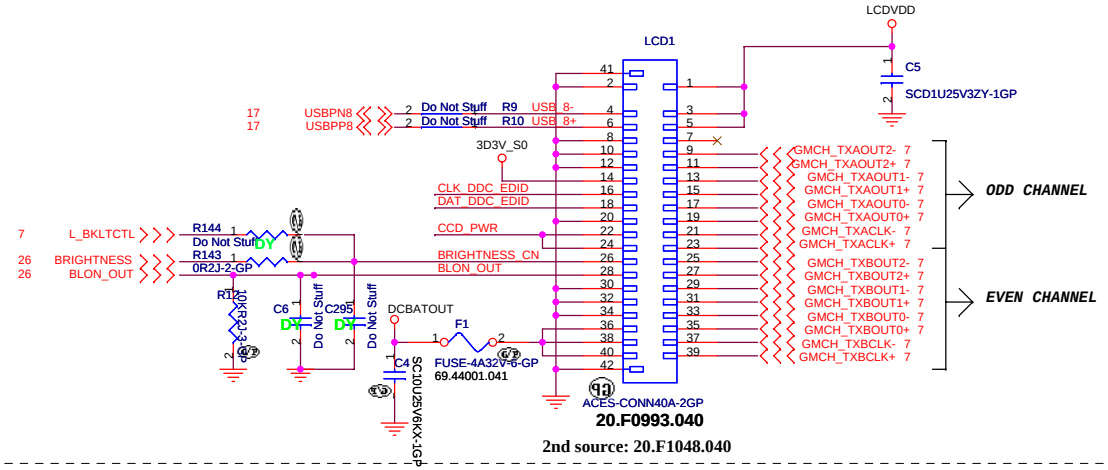
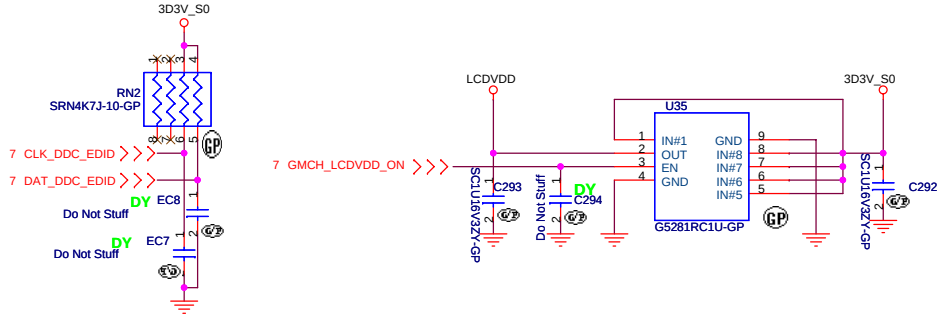
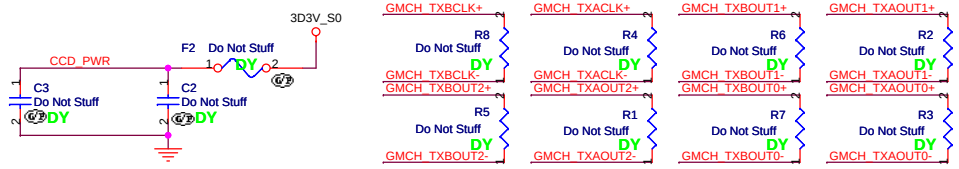
LCD/INVERTER CONN

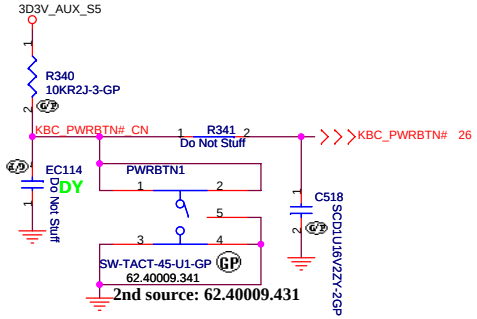


2nd source: 20.F1048.040

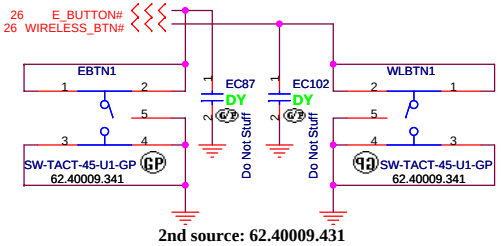




Buttons

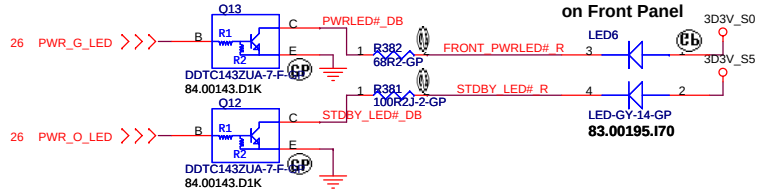


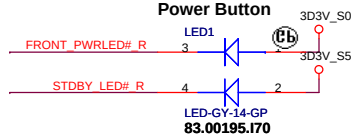
2nd source: 62.40009.431



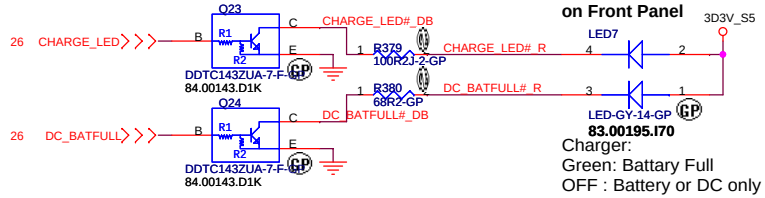
2nd source: 62.40009.431

LED

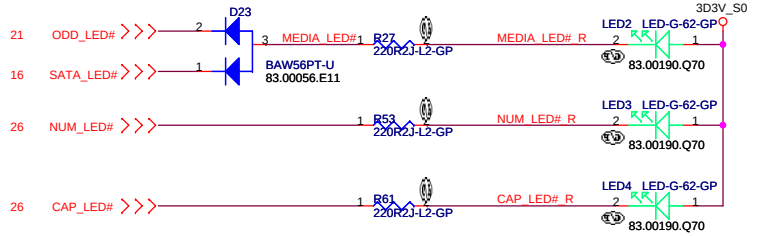


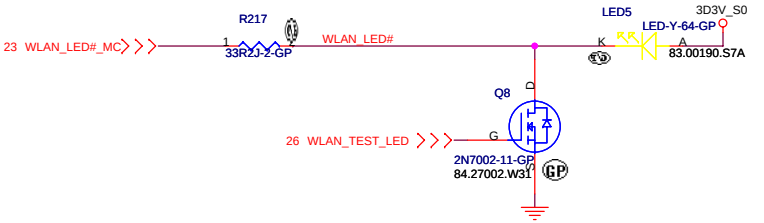


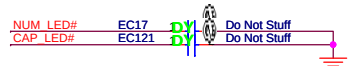
Power:
Green : S0
Orange : S3
Orange Blinking : Enter S4



Charger:
Green: Battary Full
OFF : Battery or DC only
Orange : Charging
Orange Blink : Battery low







RTM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & LED & Buttons

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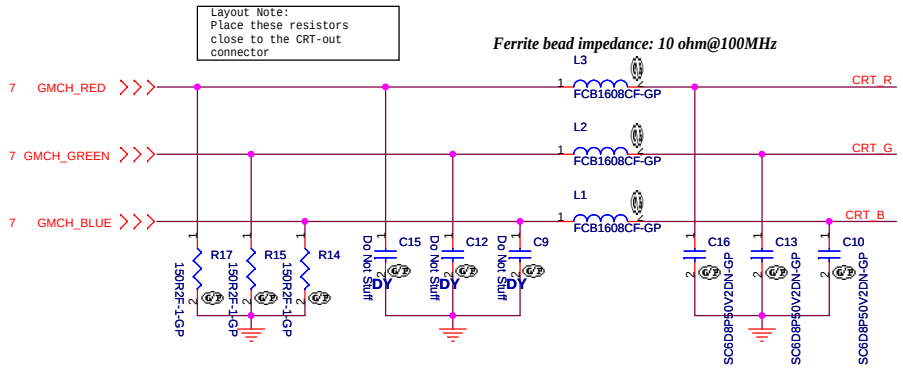
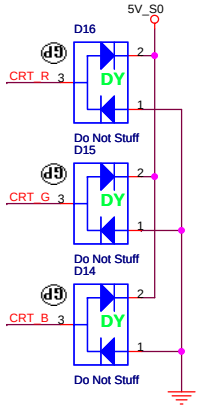
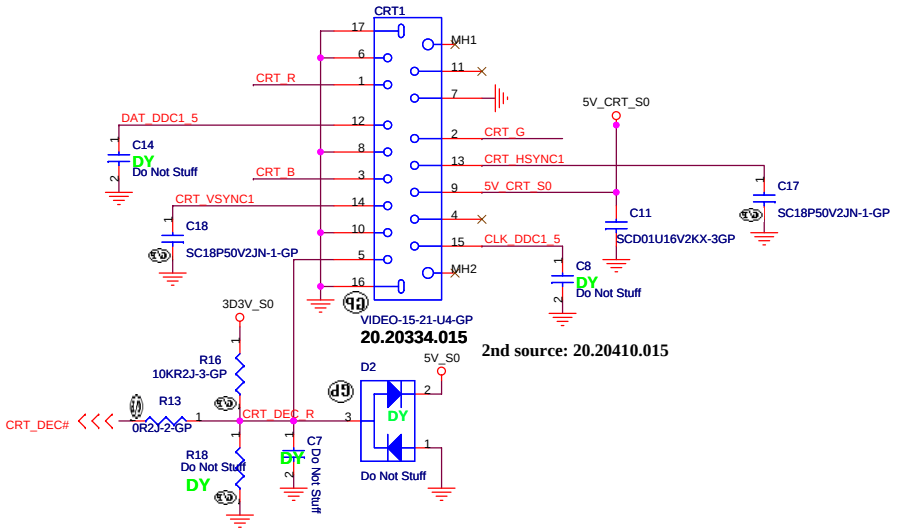
CRT I/F & CONNECTOR

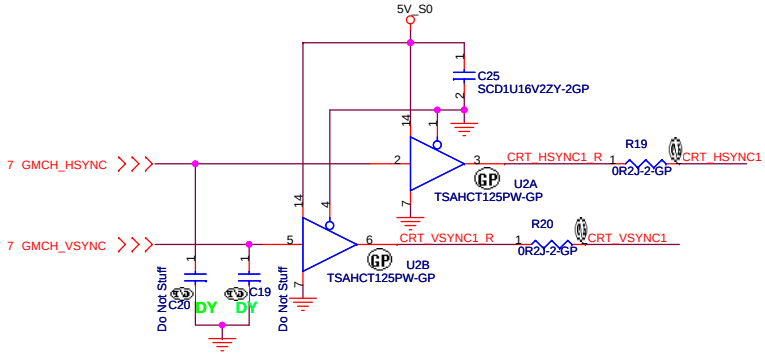


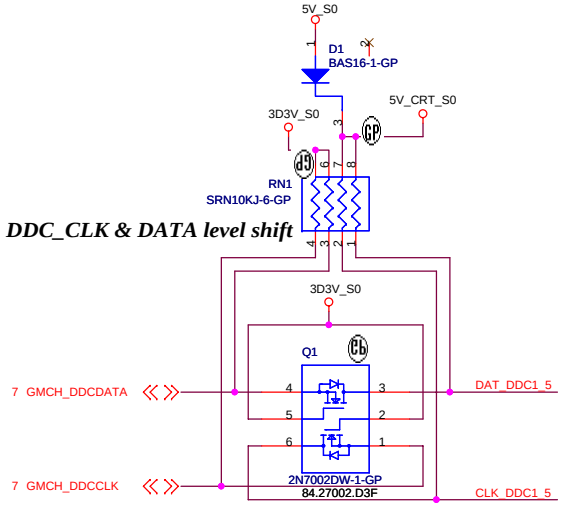




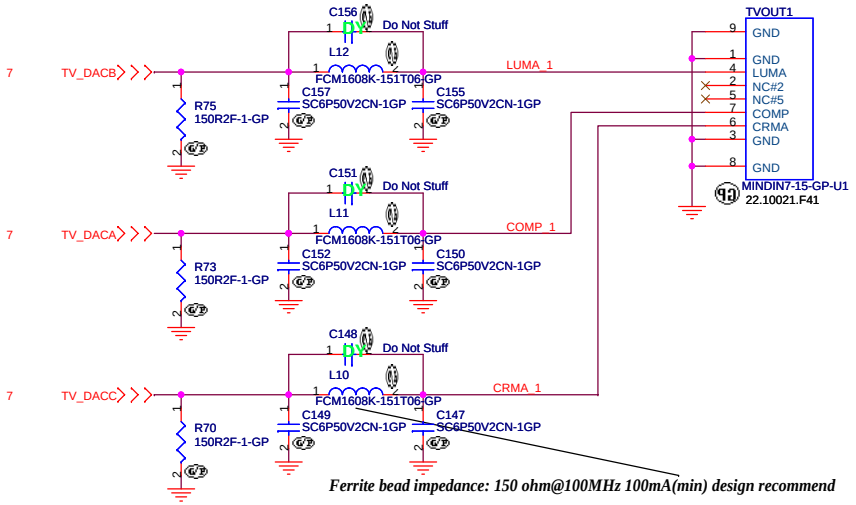
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

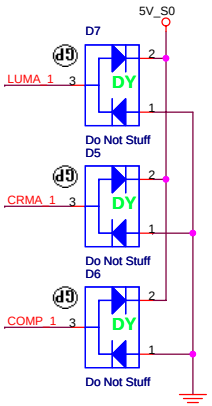
Hsync & Vsync level shift





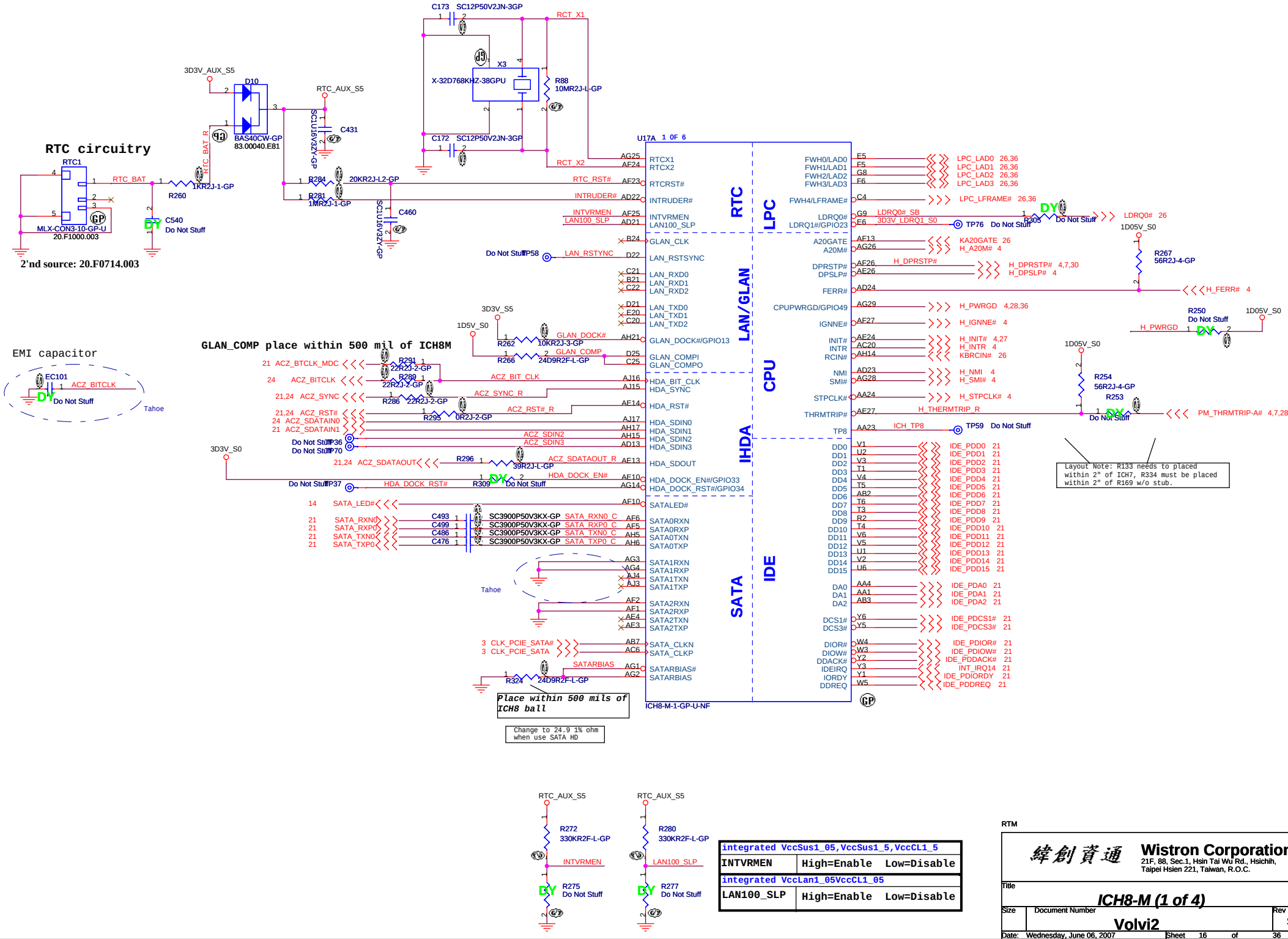
TV CONN





緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT/TV Connector	
Size	Document Number: Volvi2	Rev: SA
Date: Wednesday, June 06, 2007	Sheet 15 of 36	



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Title: **ICH8-M (1 of 4)**

Size	Document Number	Rev
	Volvi2	SA

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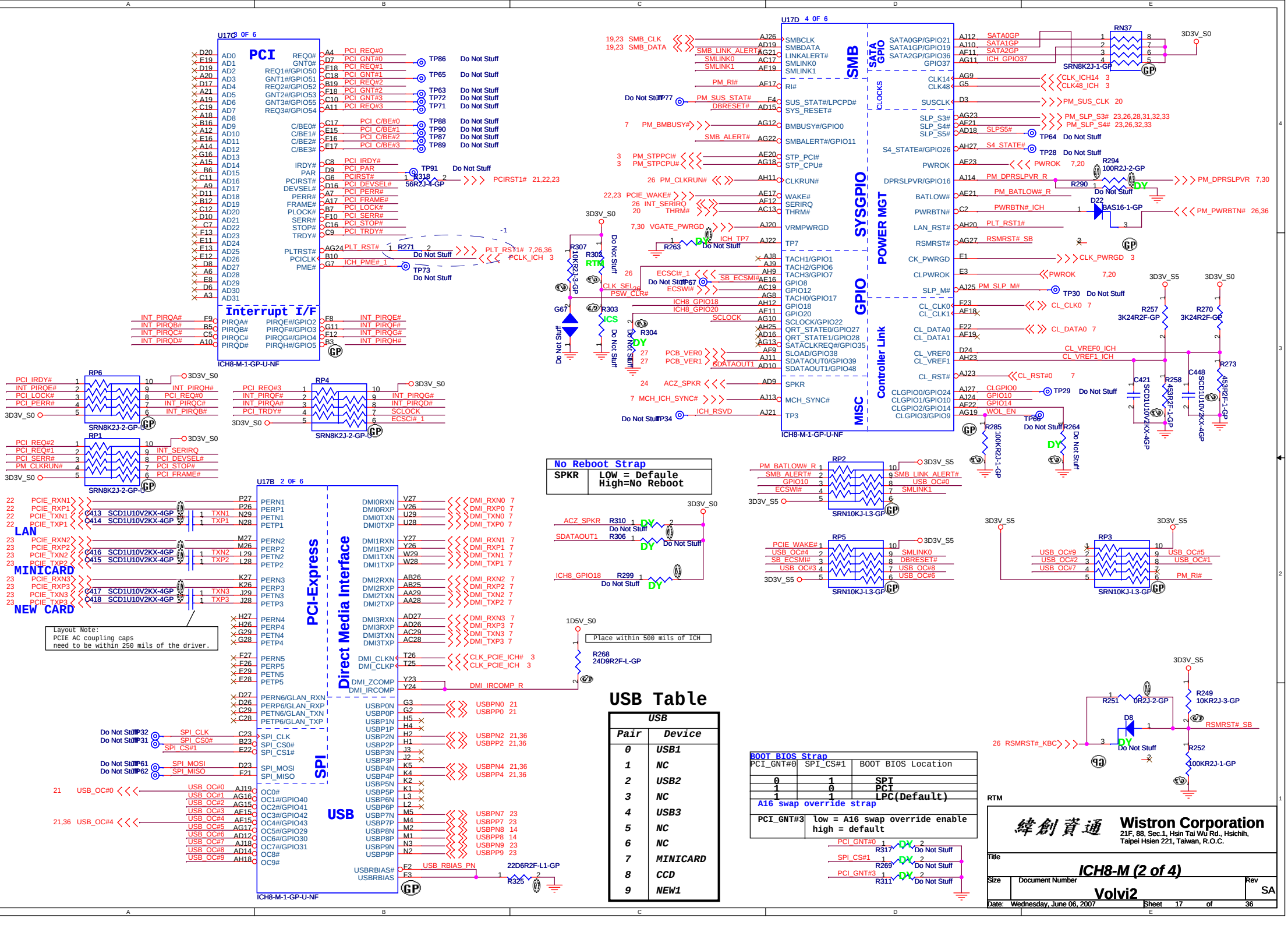
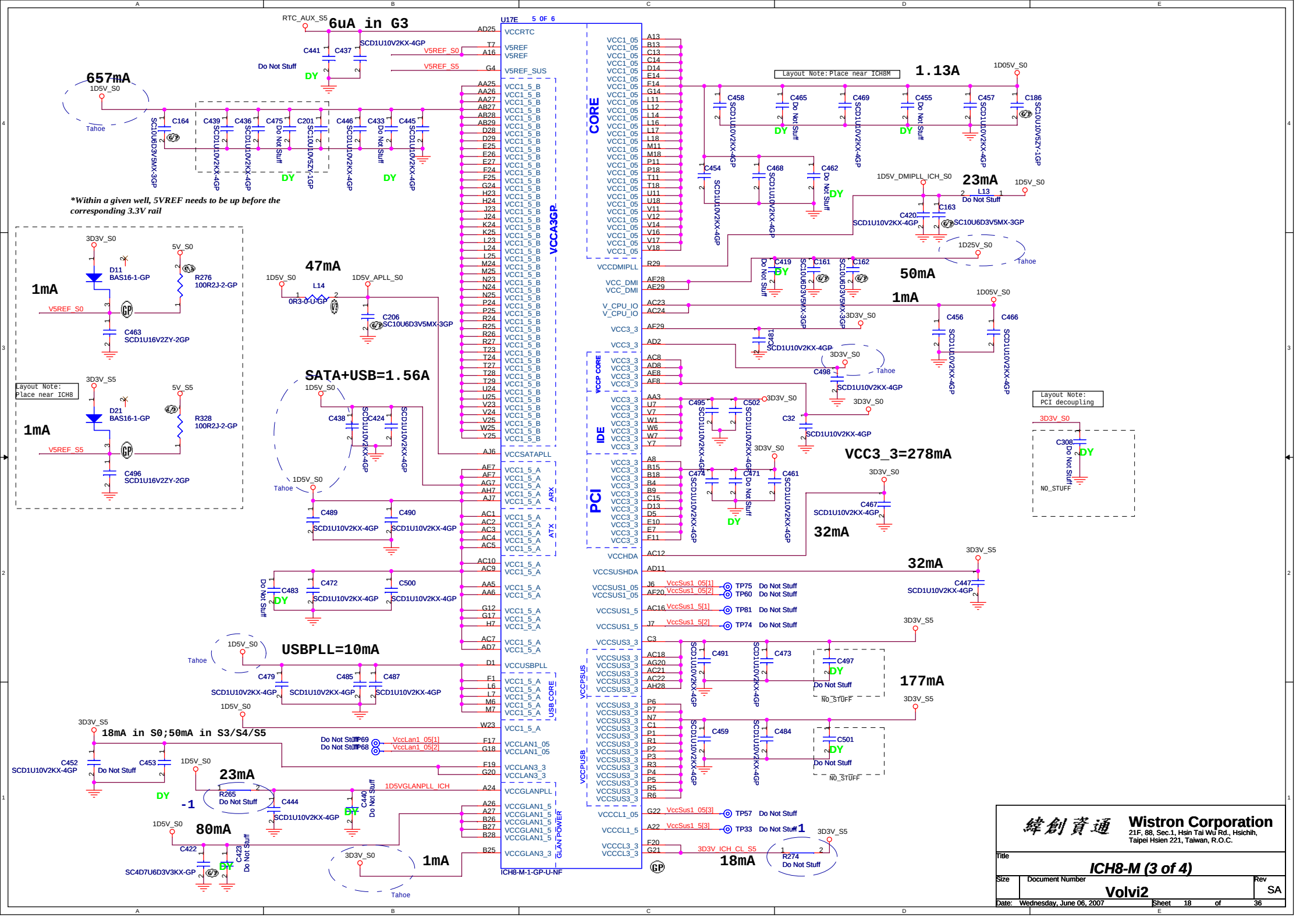

PCI
Interrupt I/F
ICH8-M-1-GP-U-NF
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
ICH8-M-1-GP-U-NF
No Reboot Strap
SPKR LOW = Defaule High=No Reboot
LAN
MINICARD
NEW CARD
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M-1-GP-U-NF
Place within 500 mils of ICH
USB Table
USB
Pair Device
0 USB1
1 NC
2 USB2
3 NC
4 USB3
5 NC
6 NC
7 MINICARD
8 CCD
9 NEW1
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable
high = default
RTM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (2 of 4)
Size Document Number Rev
Volvi2 SA
Date: Wednesday, June 06, 2007 Sheet 17 of 36



緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*ICH8-M (3 of 4)*
Size	Document Number: Volvi2
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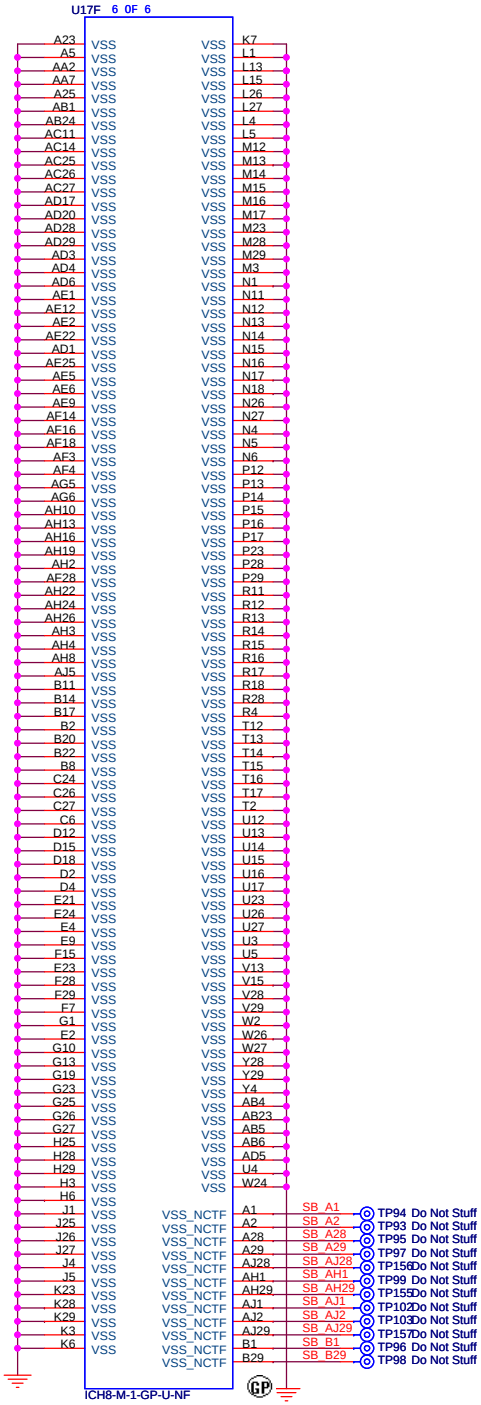
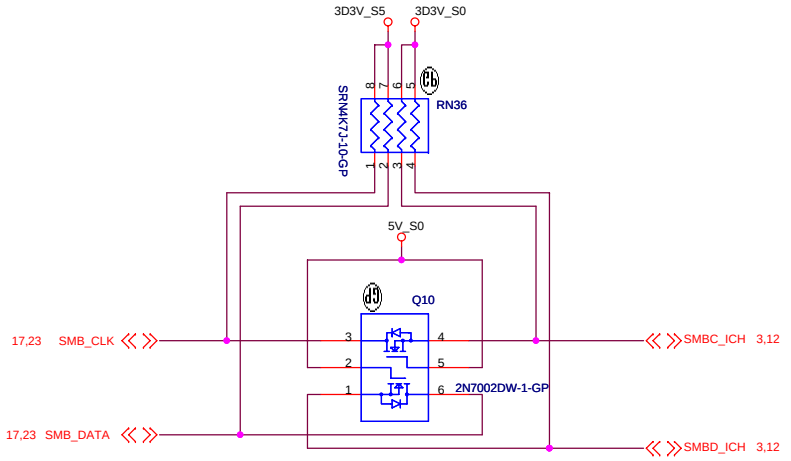
Date: Wednesday, June 06, 2007	Sheet 18 of 36





Q12 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ICH8-M (4 of 4)	
Size	Document Number: Volvi2	Rev: SA
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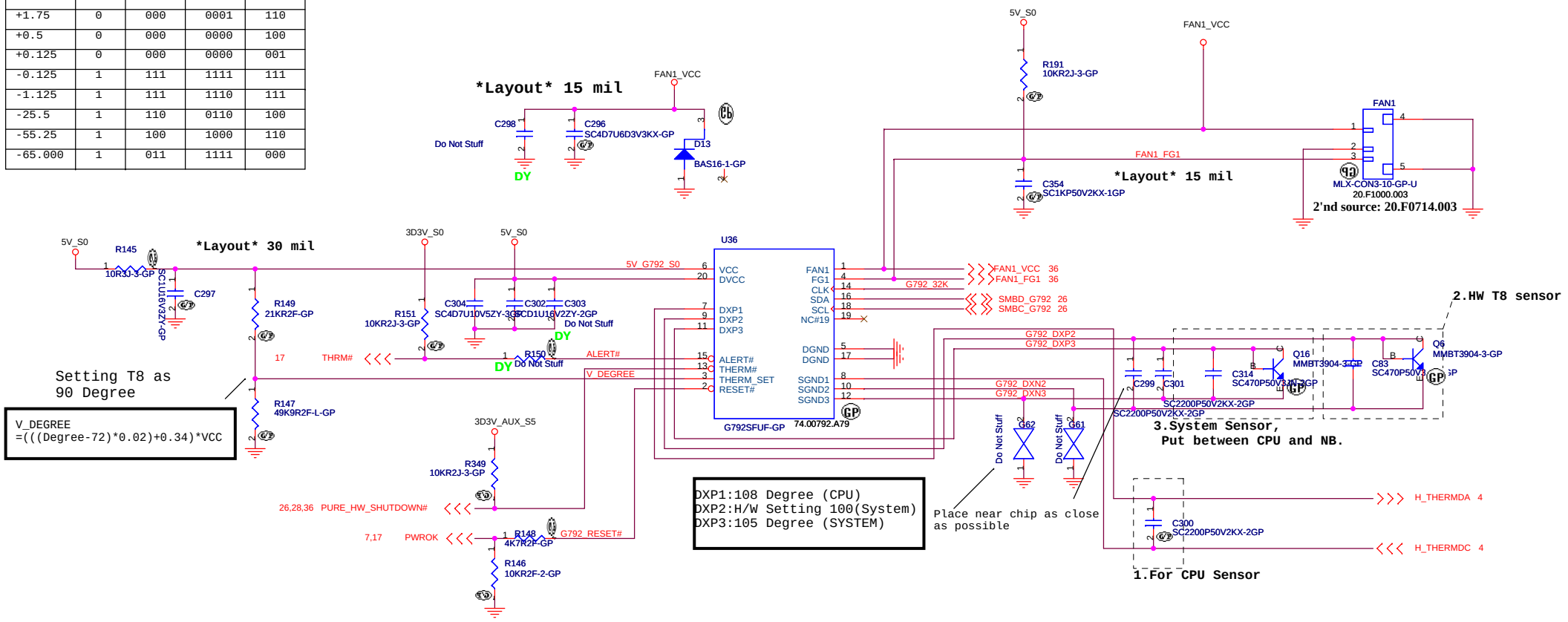
TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal/Fan Controllor**

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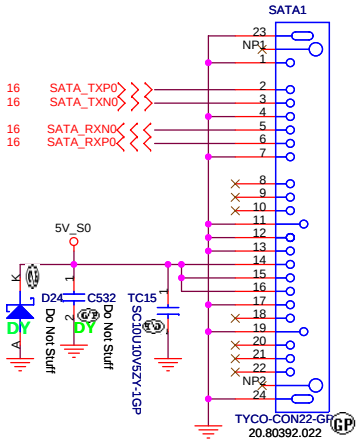
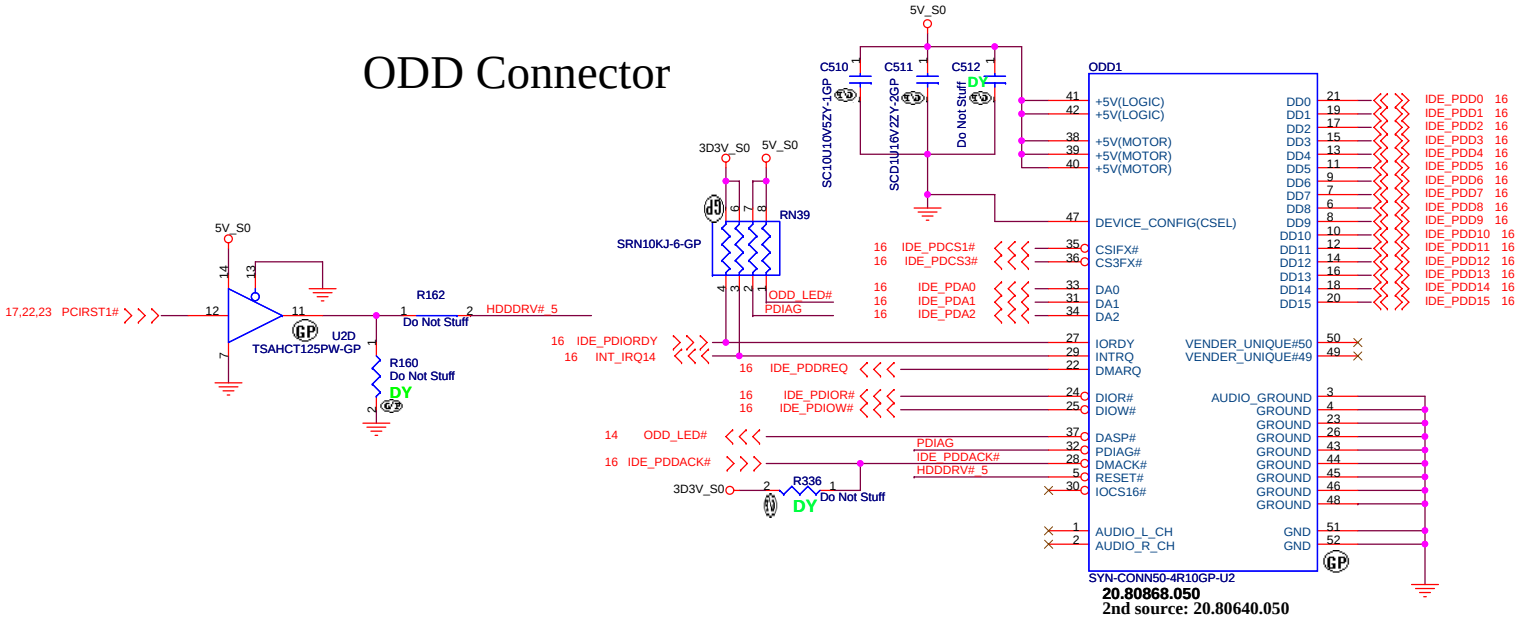
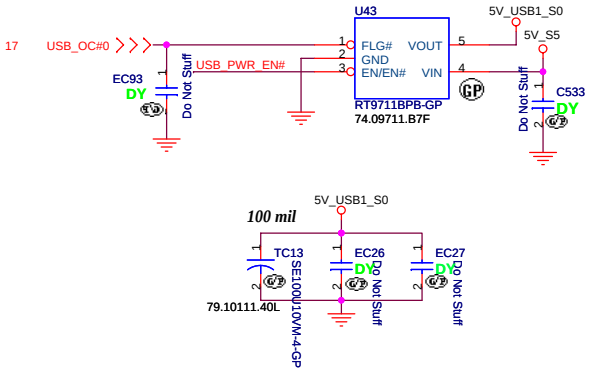
SATA HD Connector

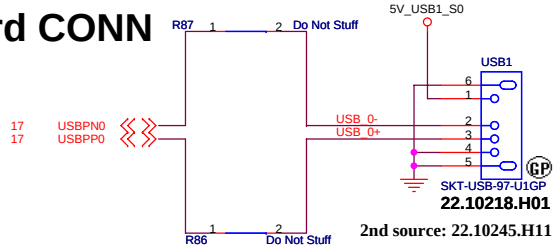


ODD Connector

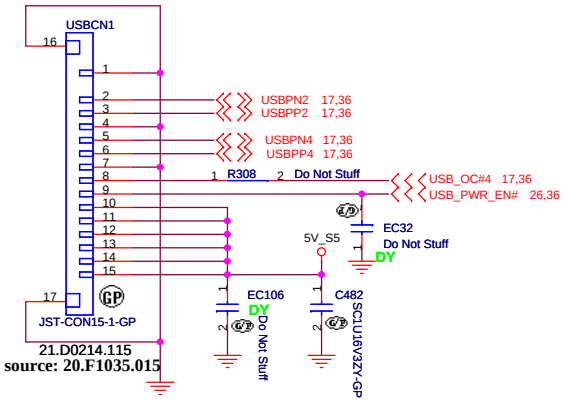




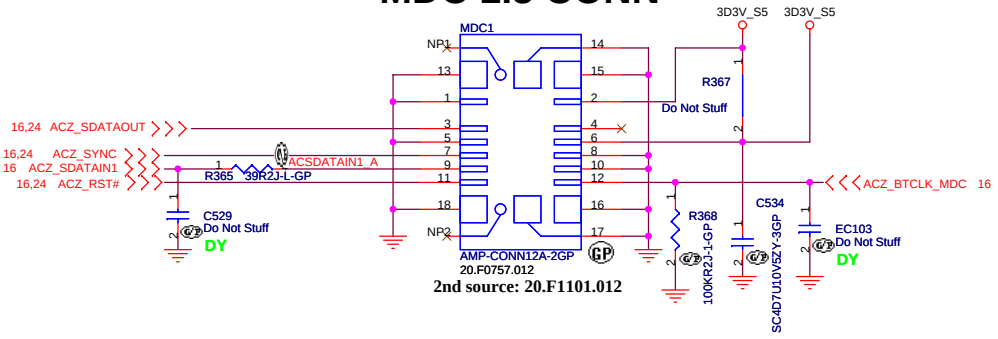
USB On Board CONN



USB ZIF CONN



MDC 1.5 CONN



RTM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD / CDROM / USB / MDC***

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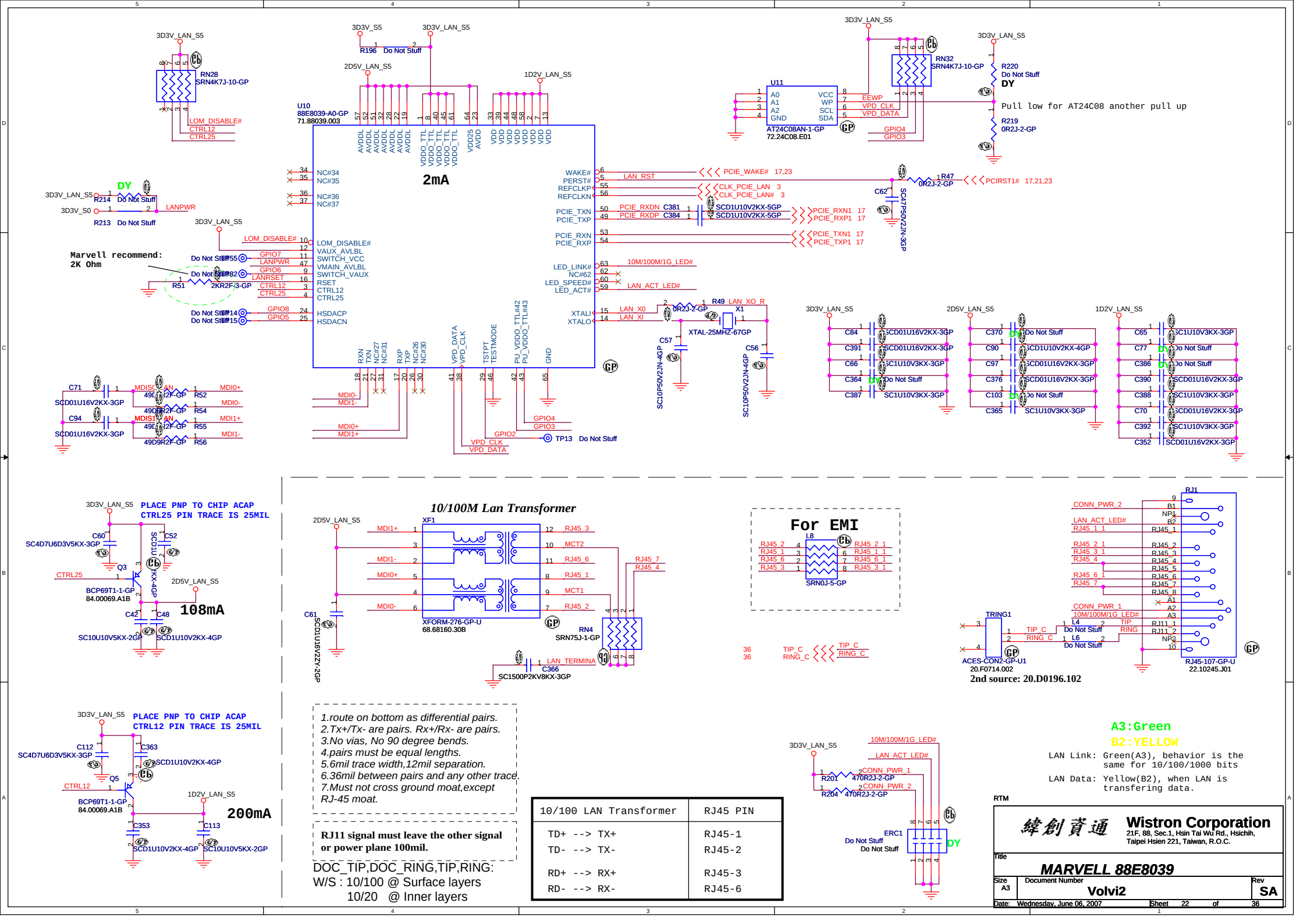
U10
88E8039-A0-GP
71.88039.003
2mA
U11
AT24C08AN-1-GP
72.24C08.E01
RN28
SRN4K7J-10-GP
RN32
SRN4K7J-10-GP
R220
Do Not Stuff
DY
Pull low for AT24C08 another pull up
R219
0R2J-2-GP
R196 Do Not Stuff
R214 Do Not Stuff
R213 Do Not Stuff
LANPWR
Marvell recommend:
2K Ohm
R51
2KR2F-3-GP
R47
0R2J-2-GP
C62
SC47P50V2JN-3GP
PCIE_WAKE# 17,23
CLK_PCIE_LAN 3
CLK_PCIE_LAN# 3
PCIE_RXN1 17
PCIE_RXP1 17
PCIE_TXN1 17
PCIE_TXP1 17
PCIRST1# 17,21,23
10M/100M/1G_LED#
LAN_ACT_LED#
LAN_RST
LAN_XO_R
LAN_XI
XTAL-25MHZ-67GP
X1
C57
C56
SC10P50V2JN-4GP
SC10P50V2JN-4GP
C84
C391
C66
C364
C387
C370
C90
C97
C376
C103
C365
C65
C77
C386
C388
C70
C392
C352
SCD01U16V2KX-3GP
SC1U10V3KX-3GP
SCD01U10V2KX-4GP
Do Not Stuff
C71
C94
SCD01U16V2KX-3GP
MDI0+
MDI0-
MDI1+
MDI1-
TP13 Do Not Stuff
GPIO2
VPD_CLK
VPD_DATA
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
108mA
Q3
BCP69T1-1-GP
84.00069.A1B
C60
C52
C42
C48
SC4D7U6D3V5KX-3GP
SC10U10V5KX-2GP
SCD1U10V2KX-4GP
10/100M Lan Transformer
XF1
XFORM-276-GP-U
68.68160.30B
RN4
SRN75J1-GP
C61
C366
SC1500P2KV8KX-3GP
SCD1U16V2ZX-2GP
LAN_TERMINA
For EMI
L8
SRN0J-5-GP
TRING1
ACES-CON2-GP-U1
20.F0714.002
2nd source: 20.D0196.102
RJ1
RJ45-107-GP-U
22.10245.J01
CONN_PWR_2
LAN_ACT_LED#
CONN_PWR_1
10M/100M/1G_LED#
L4
L6
TIP
RING
TIP_C
RING_C
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
200mA
Q5
BCP69T1-1-GP
84.00069.A1B
C112
C363
C353
C113
SC4D7U6D3V5KX-3GP
SCD1U10V2KX-4GP
SC10U10V5KX-2GP
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width,12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat,except RJ-45 moat.
RJ11 signal must leave the other signal or power plane 100mil.
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers
10/100 LAN Transformer
RJ45 PIN
TD+ --> TX+
TD- --> TX-
RD+ --> RX+
RD- --> RX-
RJ45-1
RJ45-2
RJ45-3
RJ45-6
R201
470R2J-2-GP
R204
470R2J-2-GP
ERC1
Do Not Stuff
A3:Green
B2:YELLOW
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transfering data.
RTM
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MARVELL 88E8039
Size A3
Document Number
Volvi2
Rev SA
Date: Wednesday, June 06, 2007
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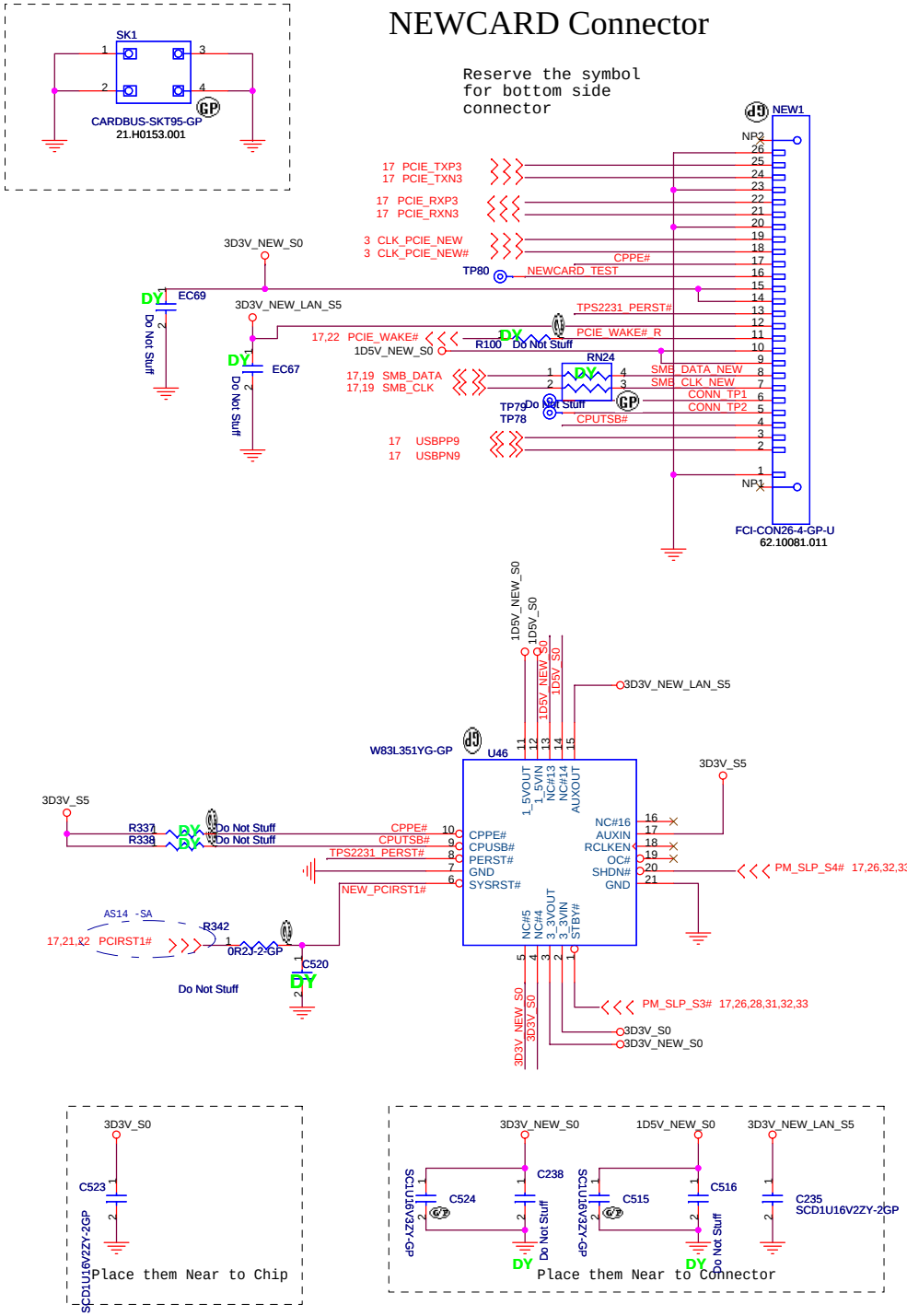
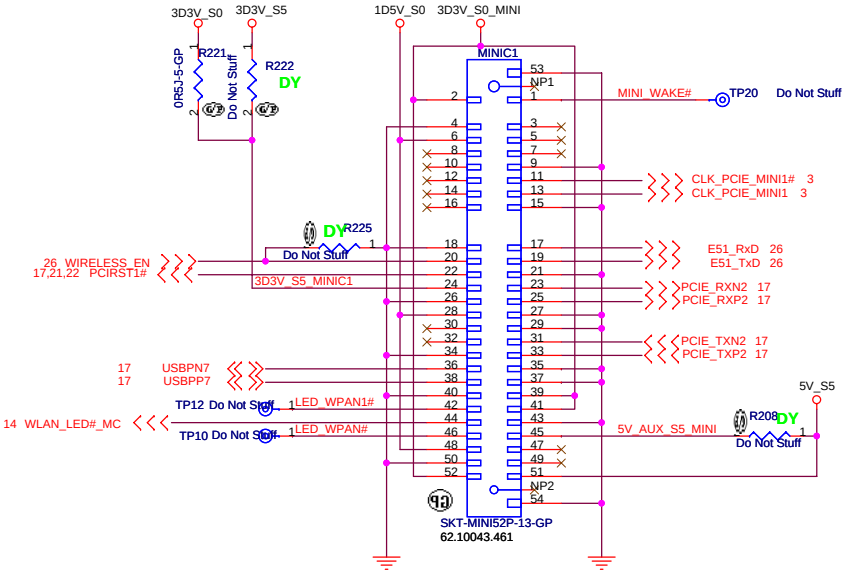
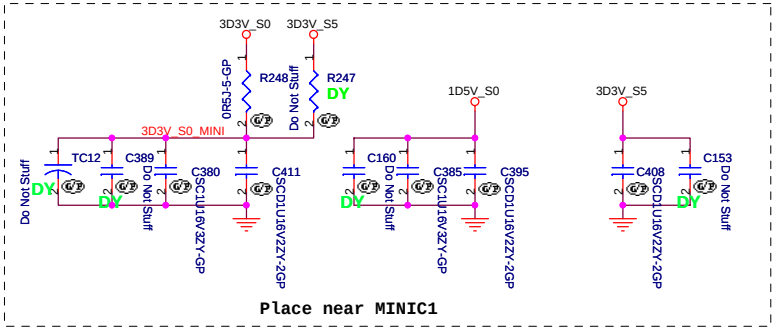
Mini Card Connector

NEWCARD Connector

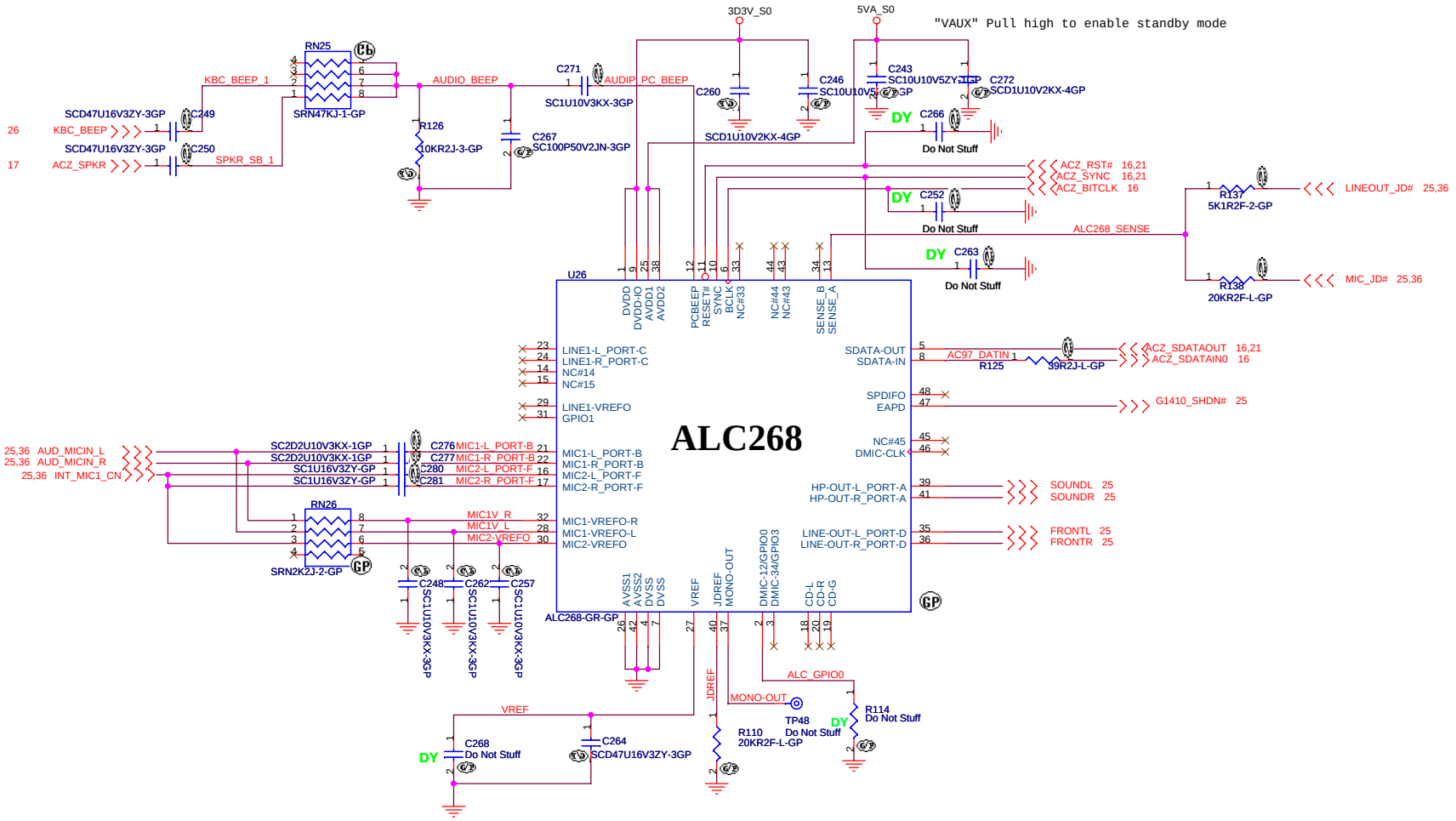






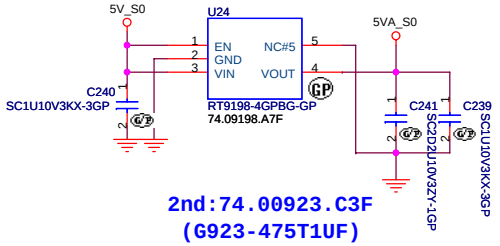
RTM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD / NEW CARD***	
Size	Document Number **Volvi2**	Rev SA
Date: Wednesday, June 06, 2007	Sheet 23 of 36	



POWER GENERATE

Layout
20 mil

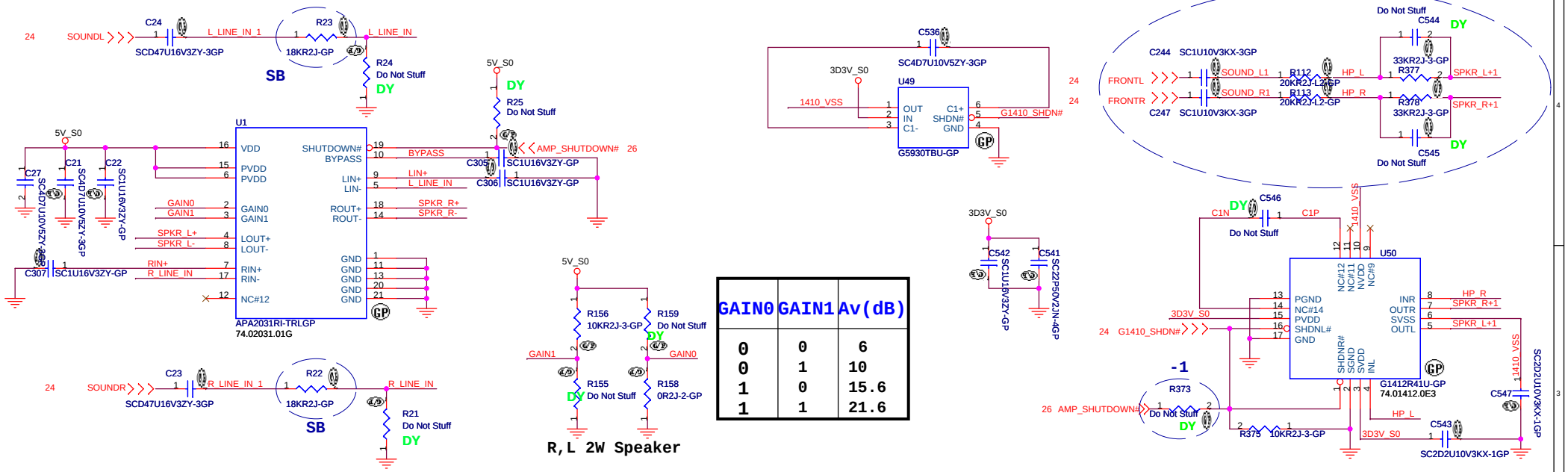


2nd:74.00923.C3F
(G923-475T1UF)

RTM

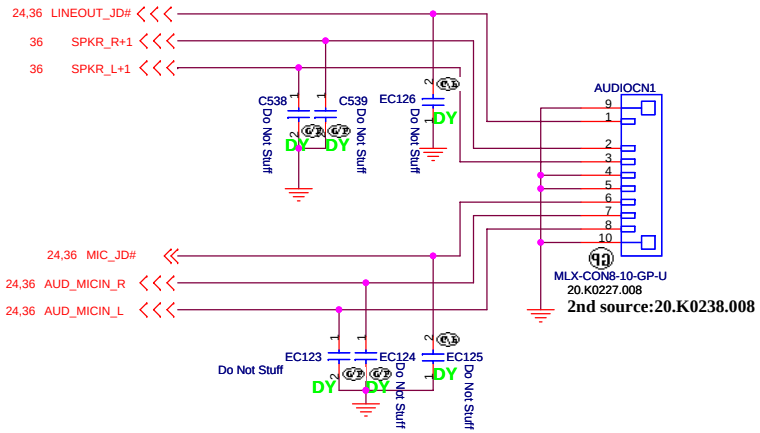
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AZALIA CODEC - ALC268		
Size	Document Number: Volvi2	Rev: SA
Date: Wednesday, June 06, 2007	Sheet 24 of 36	

AUDIO OP AMPLIFIER



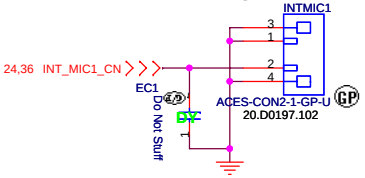
GAIN0	GAIN1	Av(dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

Audio Connector



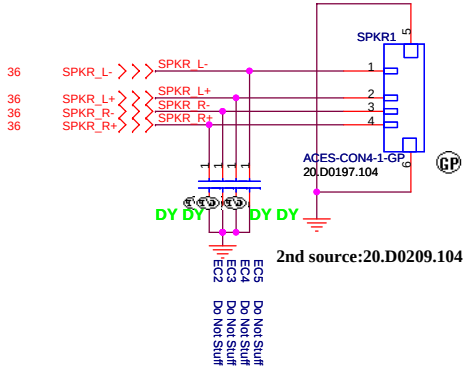
2nd source:20.K0238.008

Internal Microphone



2nd source:20.D0209.102

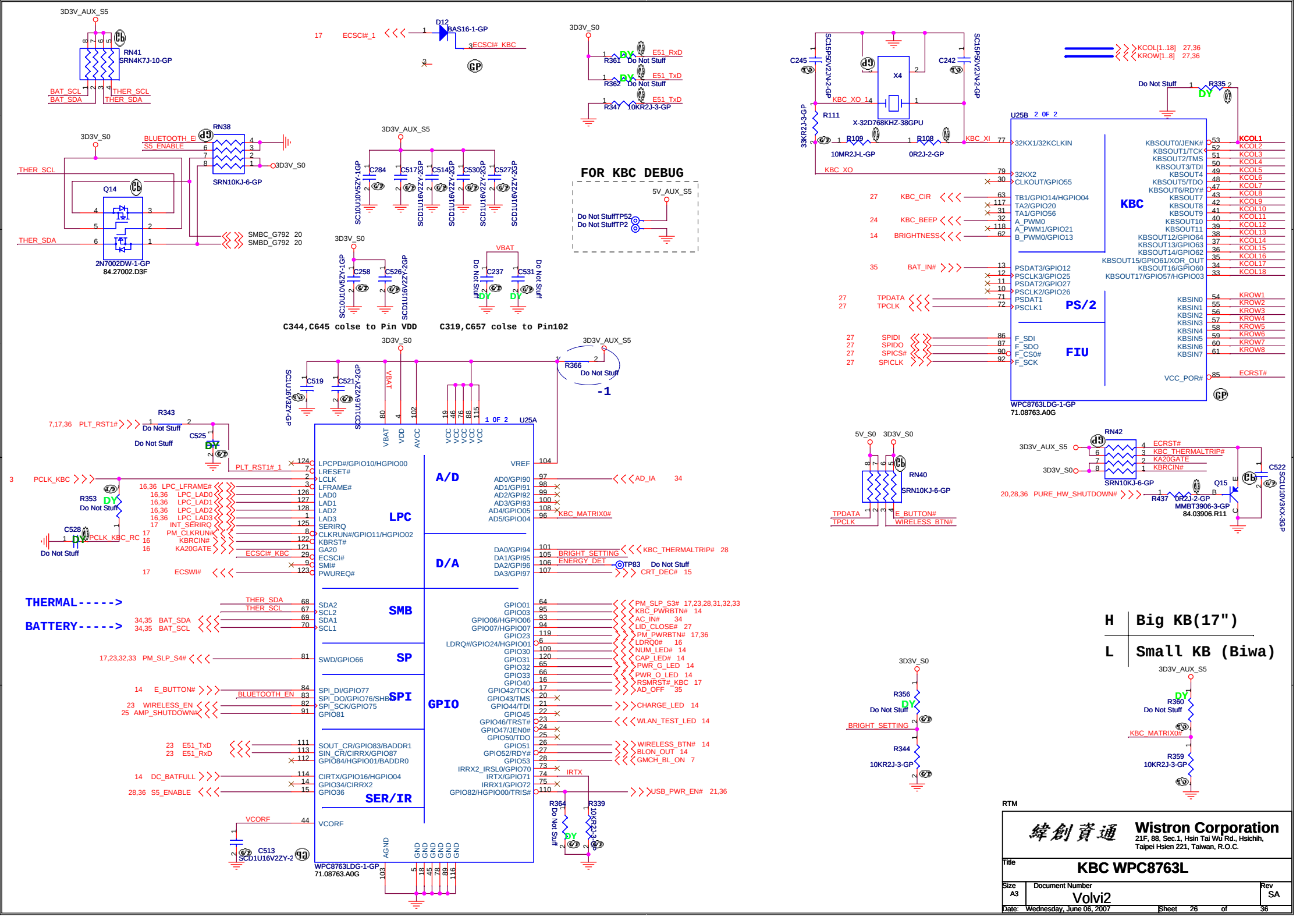
Internal Speaker



2nd source:20.D0209.104

RTM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO AMP AND JACK	
Size	Document Number: Volvi2	Rev: SA
Date: Thursday, June 07, 2007	Sheet 25 of 36	



RTM

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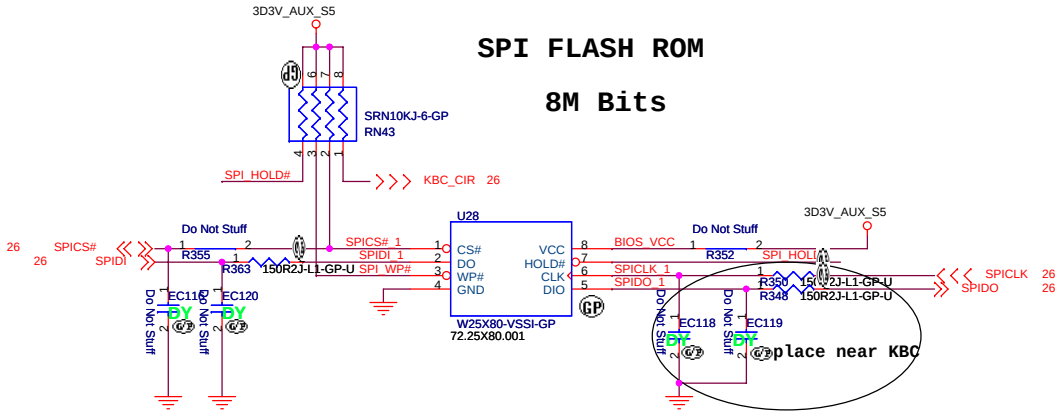
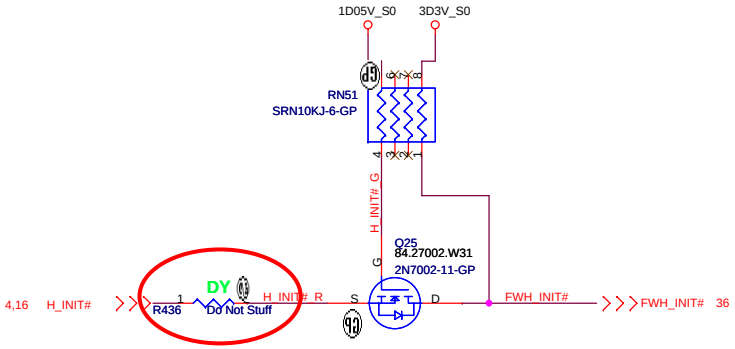
Taipei Hsien 221, Taiwan, R.O.C.

Title	KBC WPC8763L	
Size A3	Document Number Volvi2	Rev SA
Date: Wednesday, June 06, 2007	Sheet 26 of 36	

SPI FLASH ROM

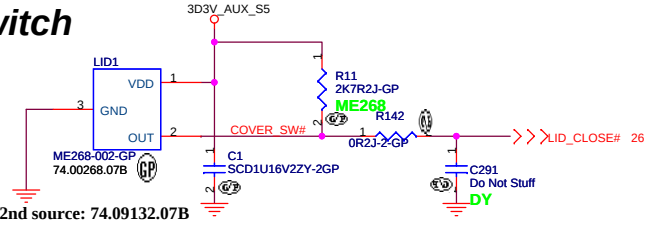
8M Bits



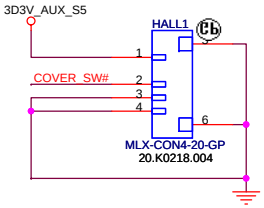


SB modify mount for Debug BD

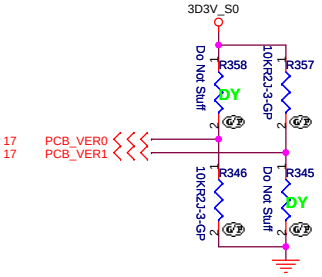
Hall Switch

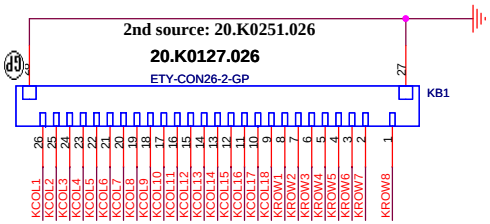


2nd source: 74.09132.07B

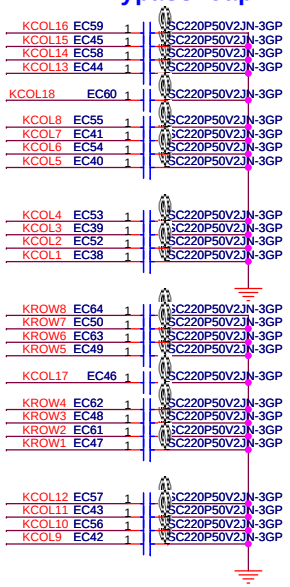


PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
-2: 1,1





EMI Bypass cap.



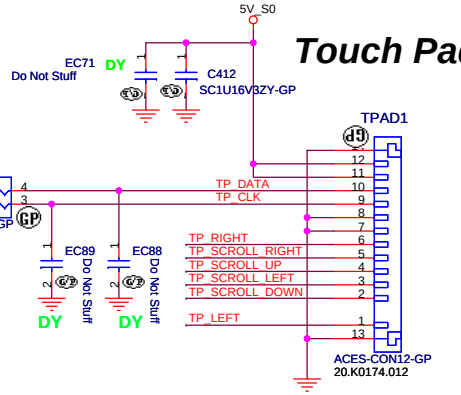
KROW[1..8] KROW[1..8] 26,36
KCOL[1..18] KCOL[1..18] 26,36

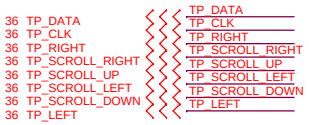
Internal KeyBoard CONN

1 25

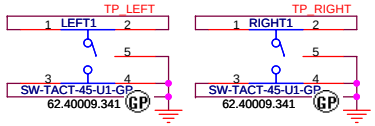
CHECK KB SPEC. AND PIN DEFINE

Touch Pad CONN





Touch Pad Button

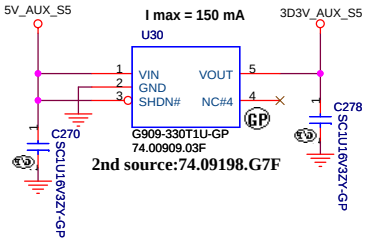


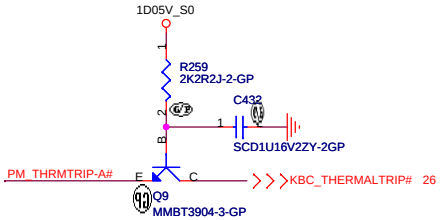
2nd source: 62.40009.431

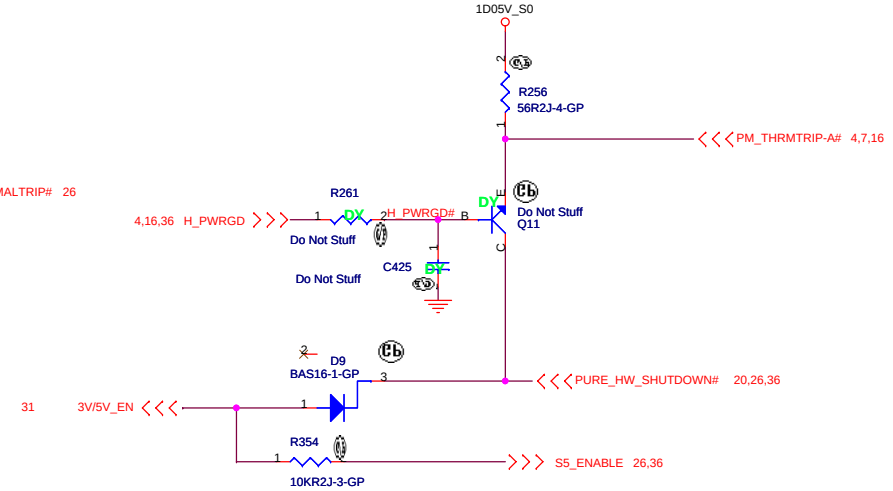
RTM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BUTTONs / KB / TOUCHPAD / BIOS	
Size	Document Number: Volvi2	Rev: SA
Date: Wednesday, June 06, 2007	Sheet 27 of 36	

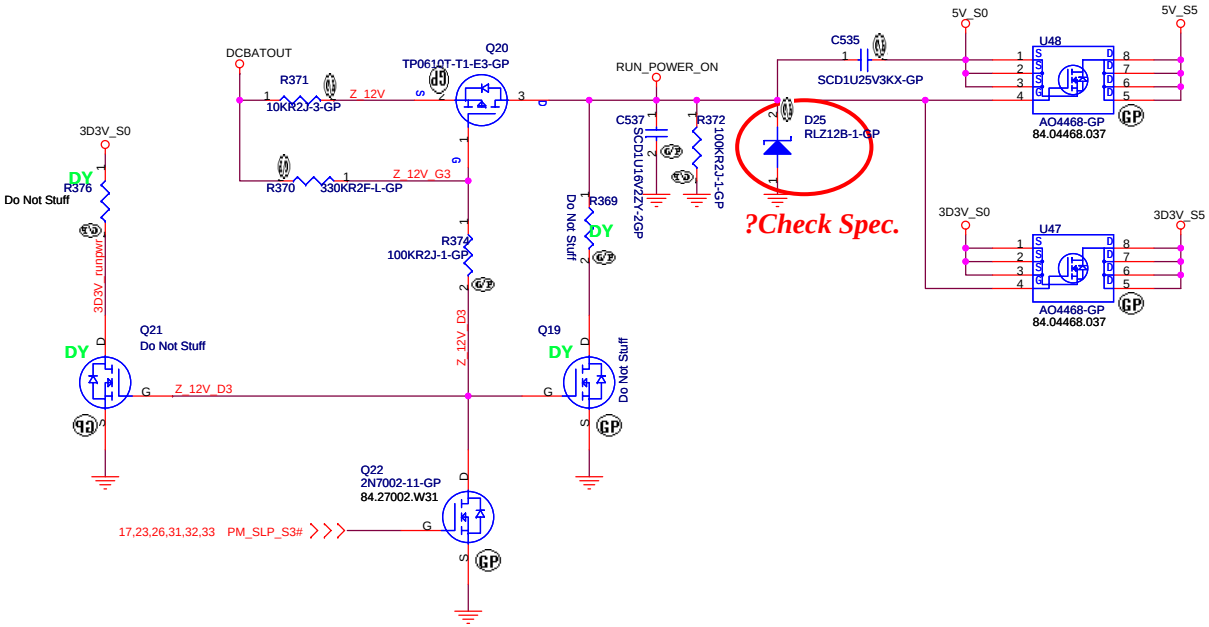
Aux Power 3D3V_AUX_S5







Run Power



RTM

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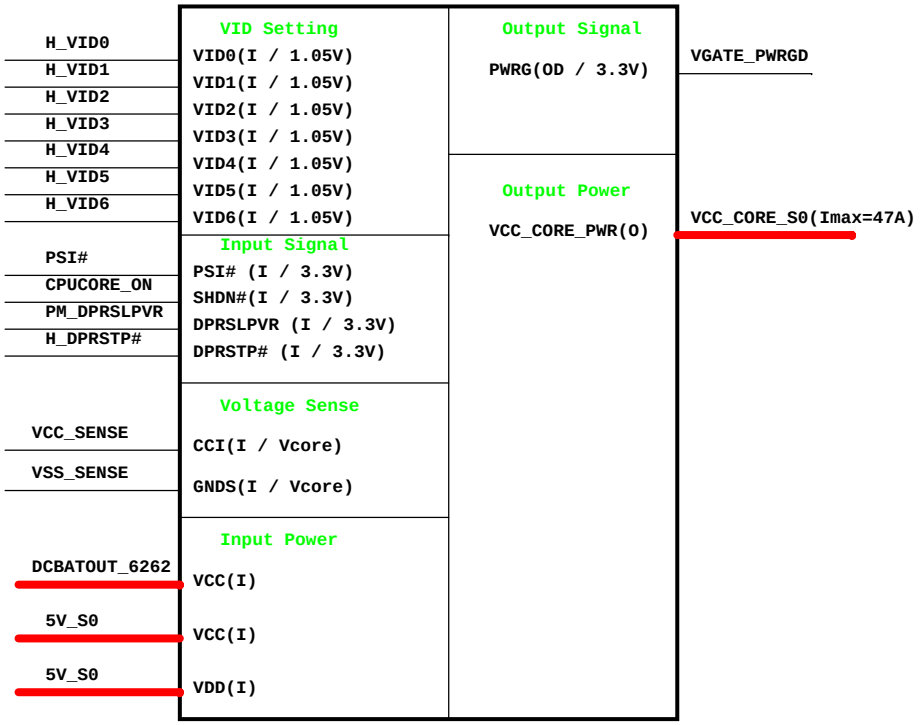
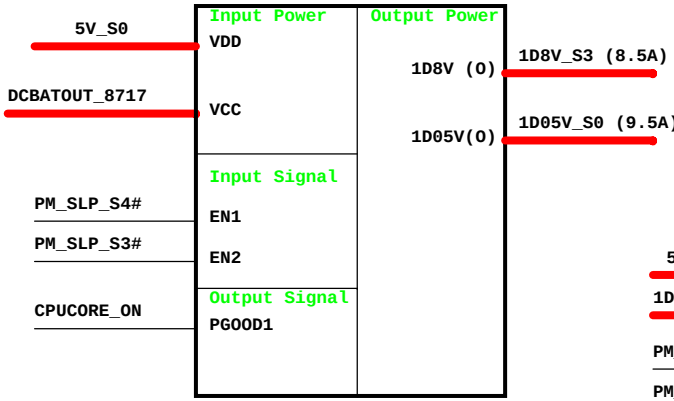
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER and 3D3V_AUX_S5	
Size	Document Number: Volvi2	Rev: SA
Date: Wednesday, June 06, 2007	Sheet 28 of 36	

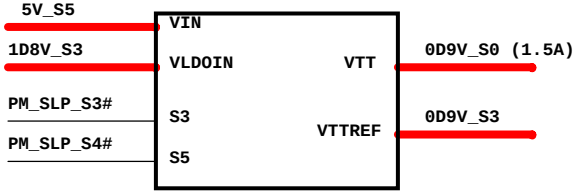
CPU_CORE
MAX8770



TPS51124
1D8V/1D05V

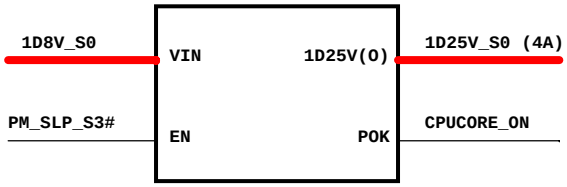


0D9V_S0



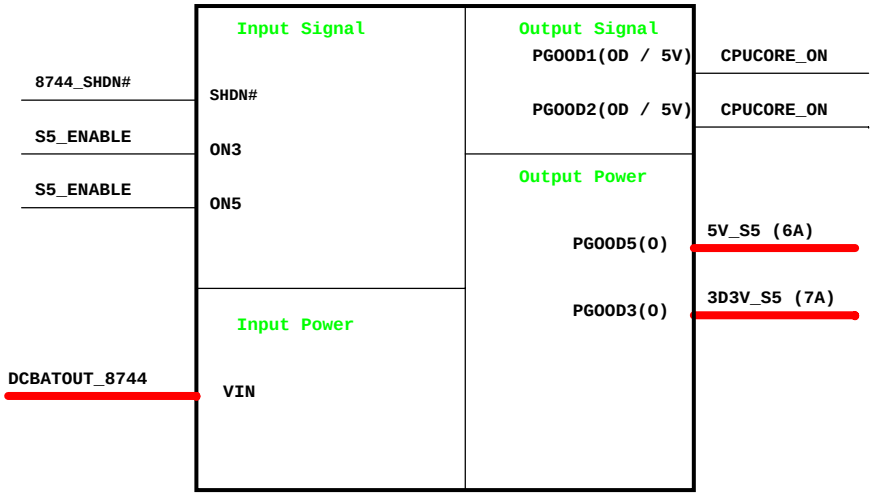
TPS51100

1D25V_S0

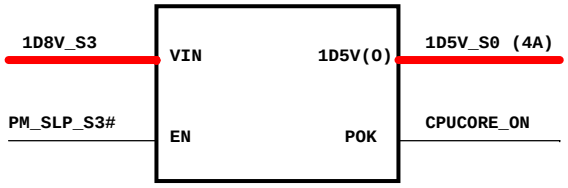


APL5913

MAX8744
5V/3D3V

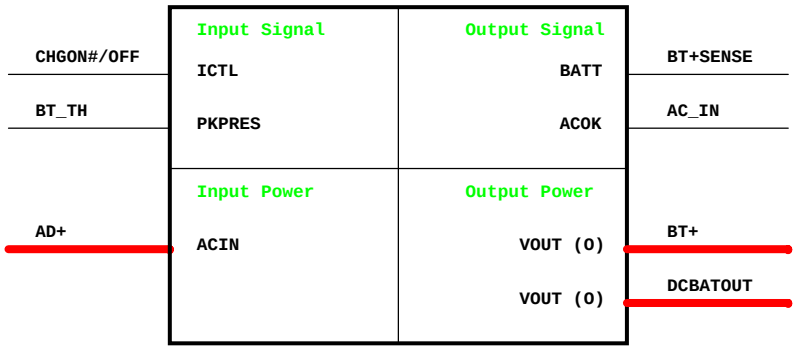


1D5V_S0



APL5915

Charger MAX8731



RTM

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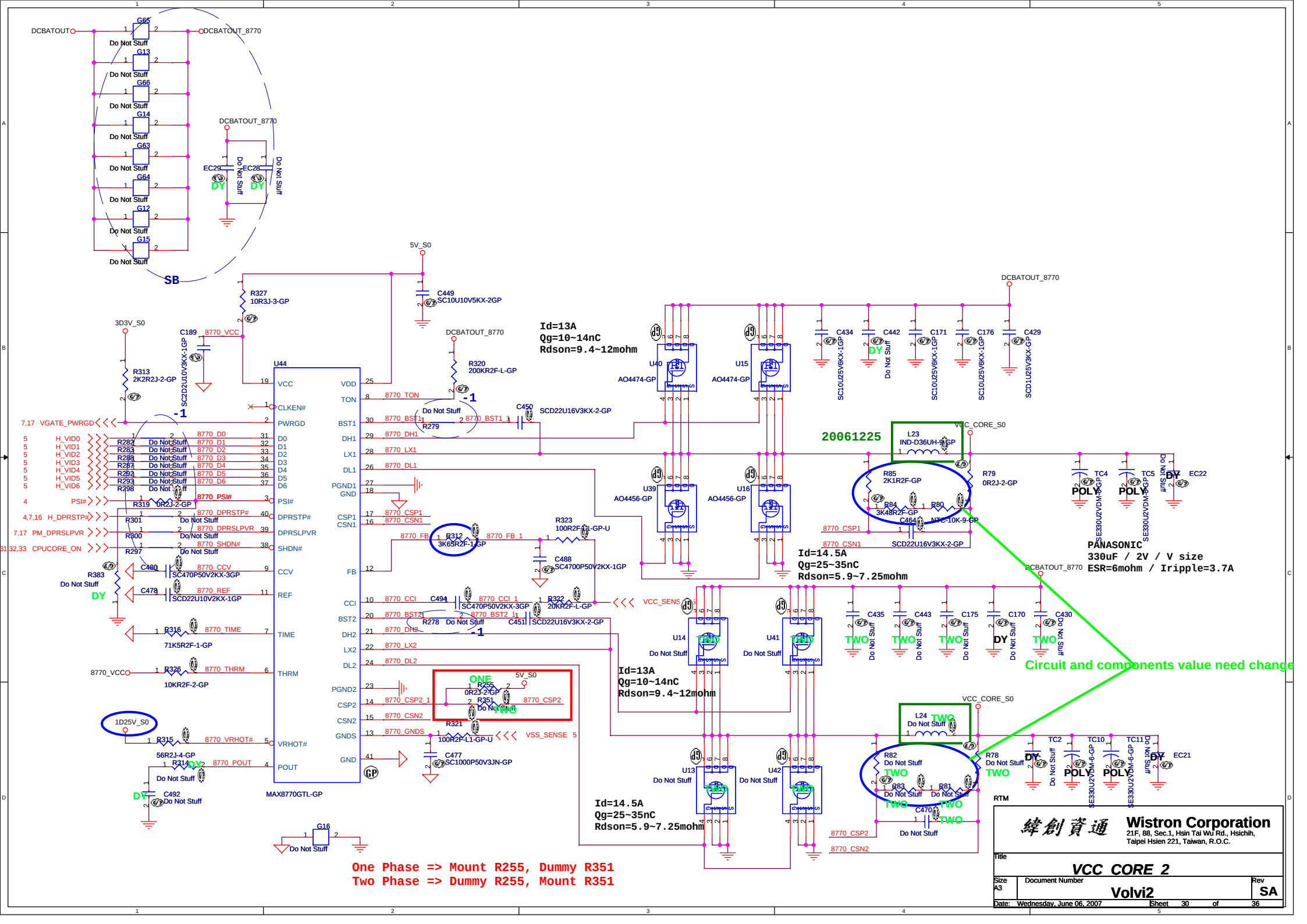
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
A3	Volvi2	SA

Date: Wednesday, June 06, 2007 Sheet 29 of 36


DCBATOUT
DCBATOUT_8770
G65
G13
G66
G14
G63
G64
G12
G15
Do Not Stuff
SB
EC29
EC28
DY
5V_S0
C449
SC10U10V5KX-2GP
R327
10R3J-3-GP
3D3V_S0
C189
8770_VCC
SC2D2U10V3KX-1GP
R313
2K2R2J-2-GP
U44
MAX8770GTL-GP
VCC
CLKEN#
PWRGD
D0
D1
D2
D3
D4
D5
D6
PSI#
DPRSTP#
DPRSLPVR
SHDN#
CCV
REF
TIME
THRM
VRHOT#
POUT
VDD
TON
BST1
DH1
LX1
DL1
PGND1
GND
CSP1
CSN1
FB
CCI
BST2
DH2
LX2
DL2
PGND2
CSP2
CSN2
GNDS
R320
200KR2F-L-GP
C450
SCD22U16V3KX-2GP
R279
R312
3K65R2F-1-GP
R323
100R2F-L1-GP-U
C488
SC4700P50V2KX-1GP
C494
SC470P50V2KX-3GP
R322
20KR2F-L-GP
R278
C451
R321
100R2F-L1-GP-U
C477
SC1000P50V3JN-GP
R255
R351
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
U40
U15
AO4474-GP
U39
U16
AO4456-GP
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
U14
U41
U13
U42
20061225
L23
IND-D36UH-3GP
L24
VCC_CORE_S0
R85
2K1R2F-GP
R84
3K48R2F-GP
R80
NTC-10K-9-GP
C464
R79
0R2J-2-GP
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
Circuit and components value need change
R82
R83
R81
C470
R78
8770_CSP1
8770_CSN1
8770_CSP2
8770_CSN2
VCC_SENS
VSS_SENSE
1D25V_S0
R315
56R2J-4-GP
R314
C492
R316
71K5R2F-1-GP
R326
10KR2F-2-GP
R383
C480
SC470P50V2KX-3GP
C479
SCD22U10V2KX-1GP
G16
One Phase => Mount R255, Dummy R351
Two Phase => Dummy R255, Mount R351
RTM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VCC CORE 2
Size
A3
Document Number
Volvi2
Rev
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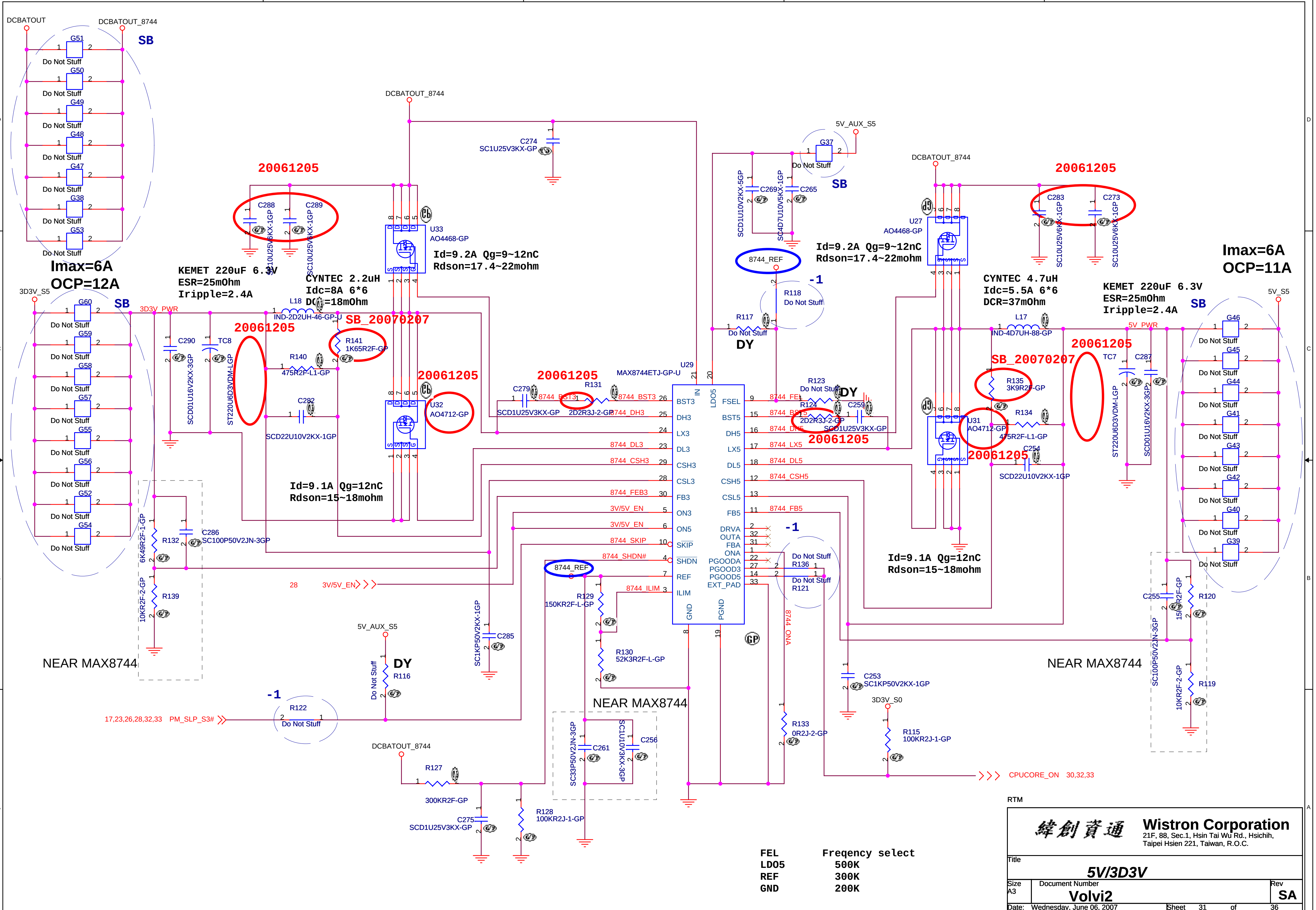

RTM

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Title	5V/3D3V	
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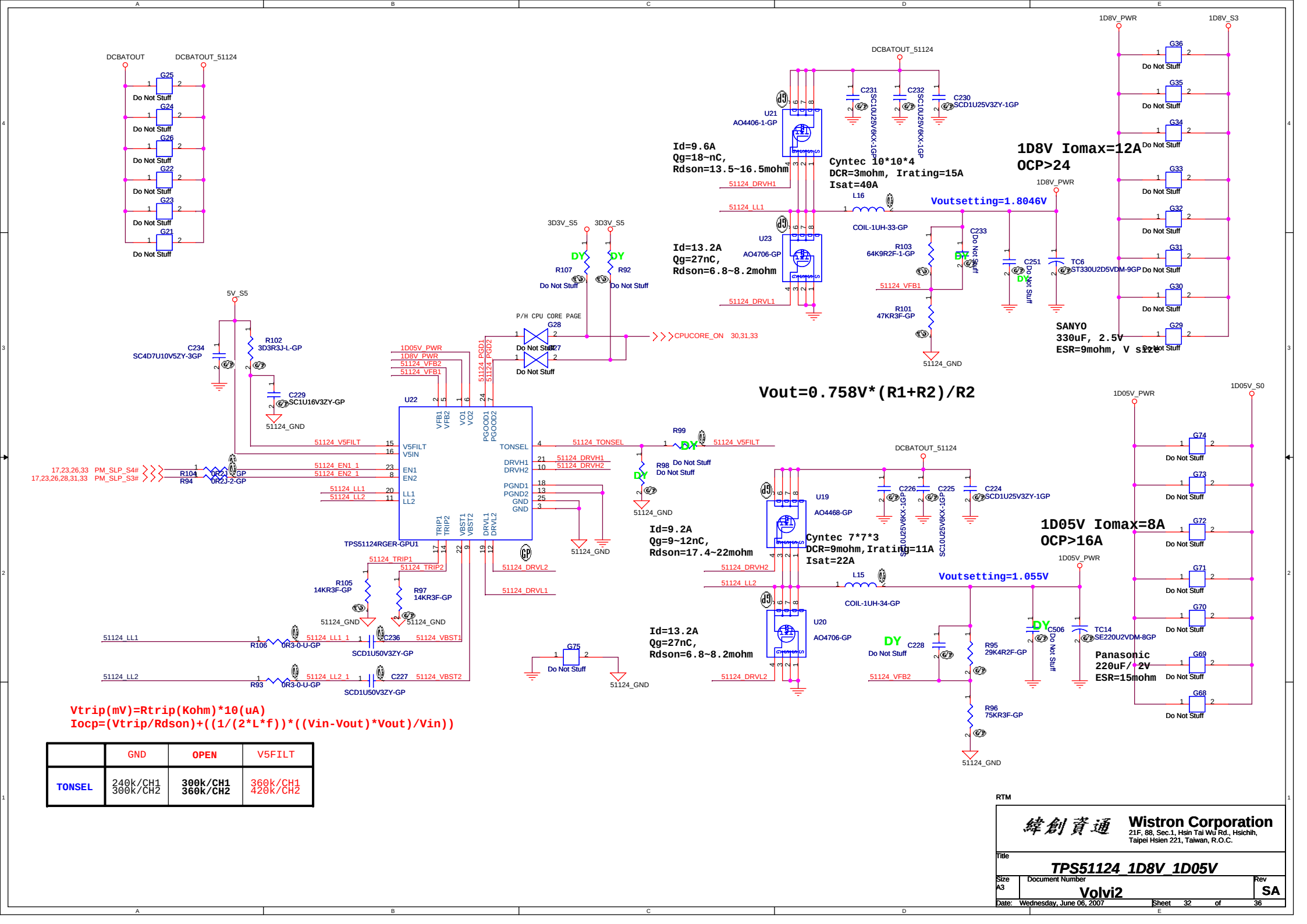
Date: Wednesday, June 06, 2007	Sheet 31 of 36	



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	**300k/CH1** **360k/CH2**	360k/CH1 420k/CH2

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51124_1D8V_1D05V***

Size: A3 | Document Number: **Volvi2** | Rev: **SA**

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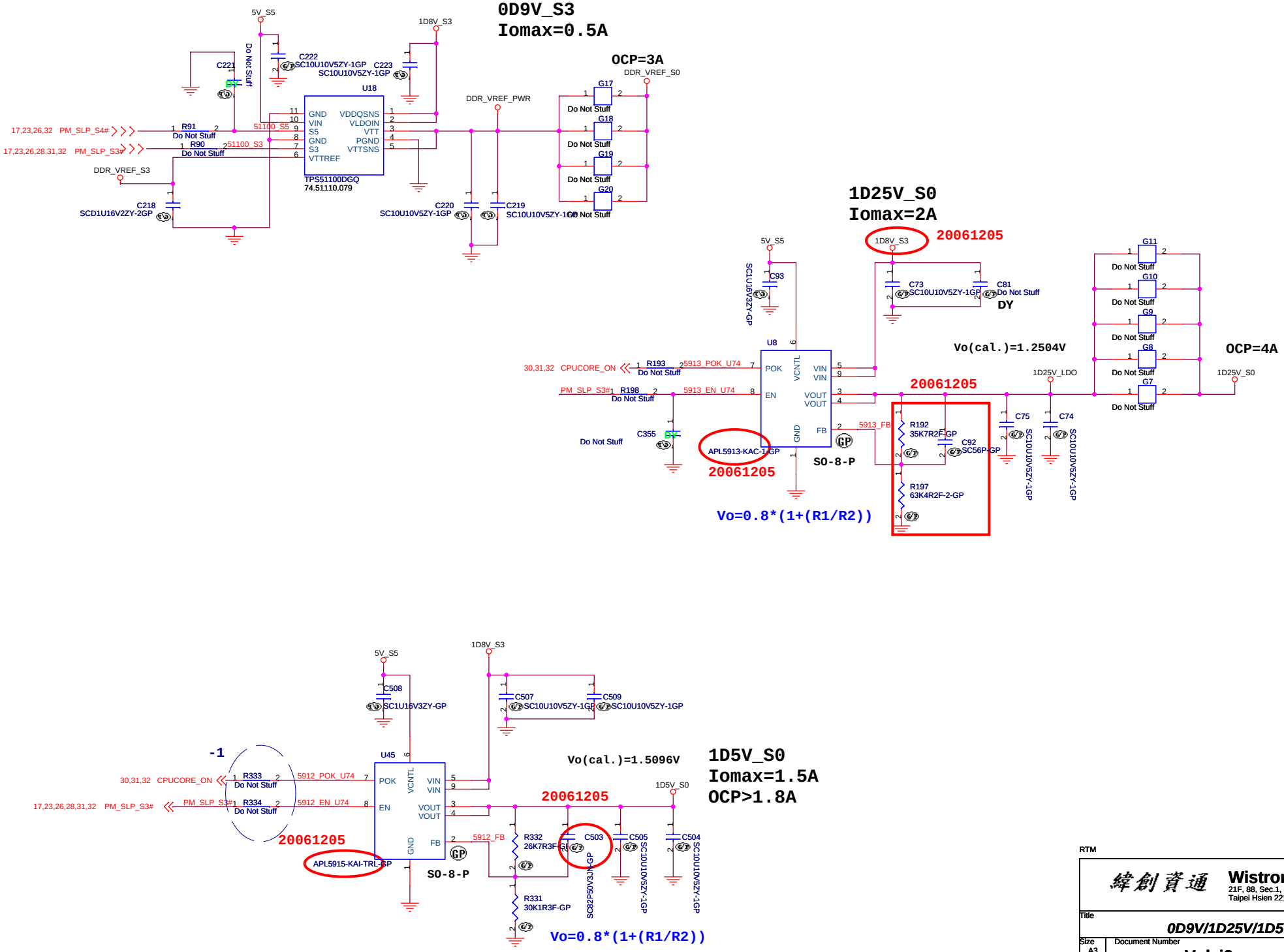

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Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V/1D25V/1D5V

Size	Document Number	Rev
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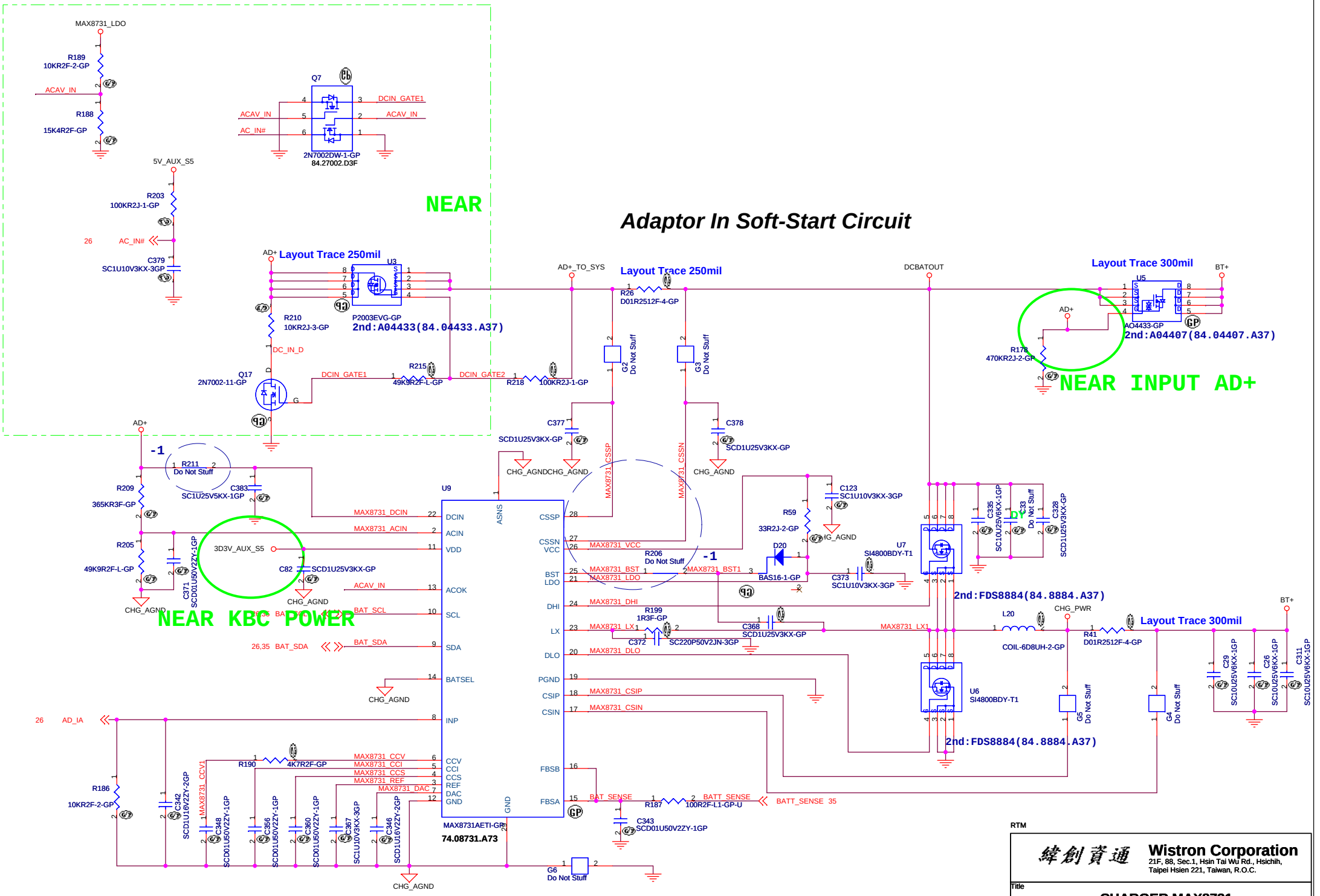
Adaptor In Soft-Start Circuit
NEAR
NEAR INPUT AD+
NEAR KBC POWER
Layout Trace 250mil
Layout Trace 300mil
2nd:A04433(84.04433.A37)
2nd:A04407(84.04407.A37)
2nd:FDS8884(84.8884.A37)
MAX8731_LDO
ACAV_IN
AC_IN#
5V_AUX_S5
3D3V_AUX_S5
AD+
AD+_TO_SYS
DCBATOUT
BT+
CHG_AGND
CHG_PWR
DC_IN_D
DCIN_GATE1
DCIN_GATE2
BAT_SDA
BAT_SCL
BAT_SENSE
BATT_SENSE
MAX8731_DCIN
MAX8731_ACIN
MAX8731_VCC
MAX8731_BST
MAX8731_LDO
MAX8731_DHI
MAX8731_LX
MAX8731_DLO
MAX8731_CSIP
MAX8731_CSIN
MAX8731_CCV
MAX8731_CCI
MAX8731_CCS
MAX8731_REF
MAX8731_DAC
MAX8731_CSSP
MAX8731_CSSN
MAX8731AETI-GP
74.08731.A73
Need Check MAXIM Sming Use MAX8731 or MAX8731A
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8731
Volvi960
SA
Wednesday, June 06, 2007
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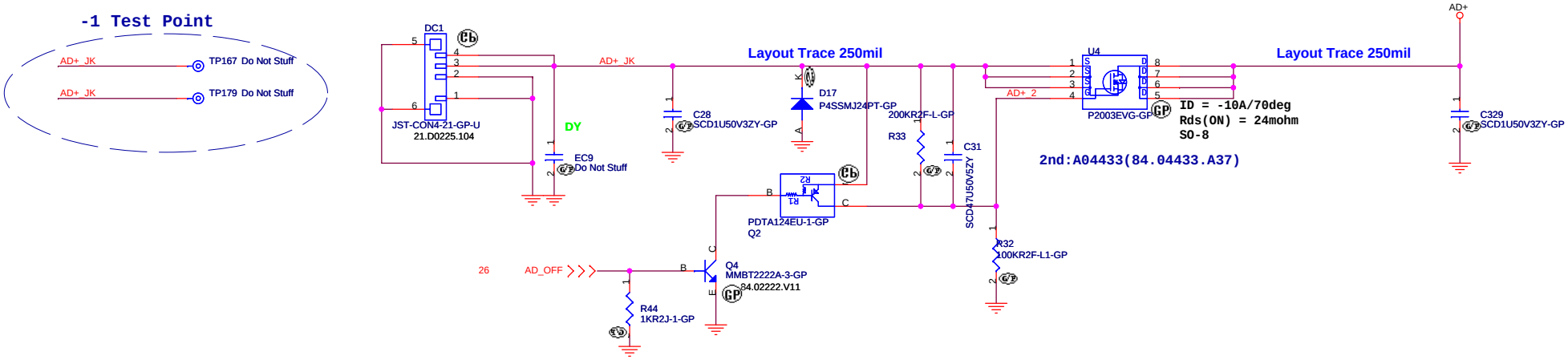
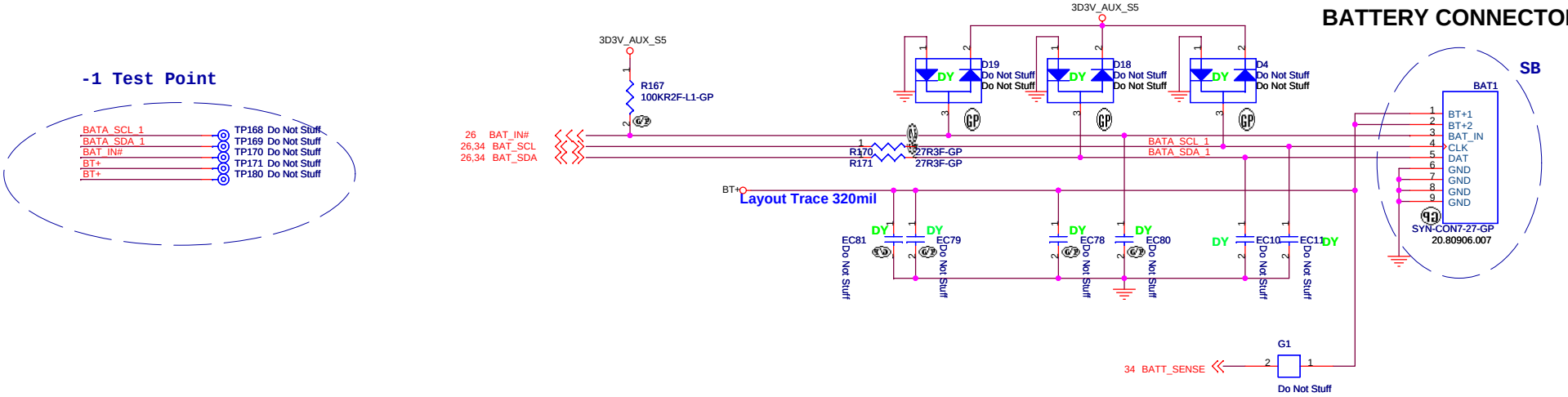
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



RTM

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Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number Volvi2	Rev SA
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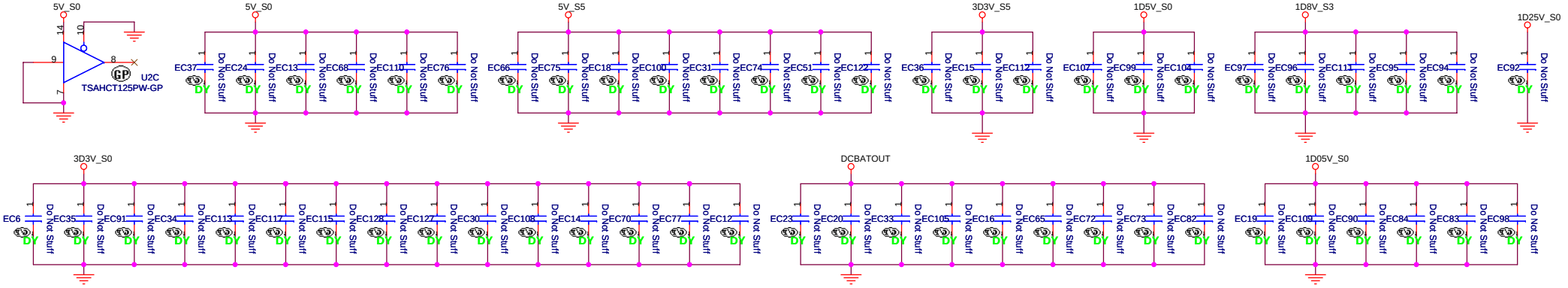
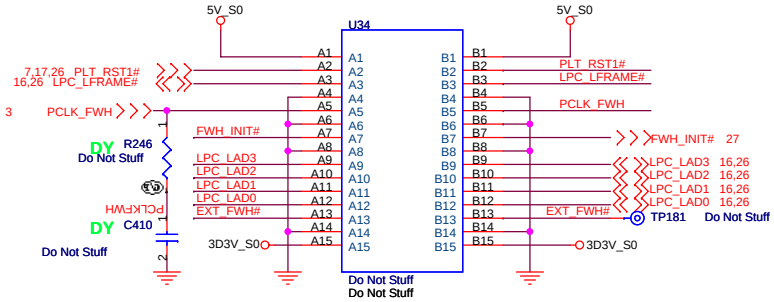
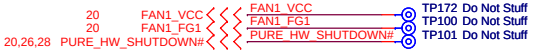
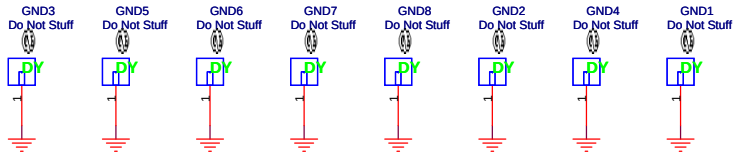


GOLDEN FINGER FOR DEBUG BOARD

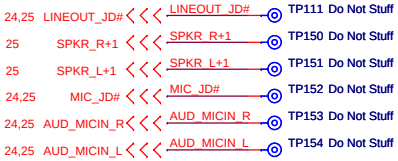


FAN CONN



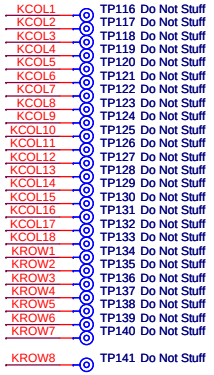


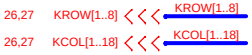
Audio Connector



Internal KeyBoard CONN

Test Point



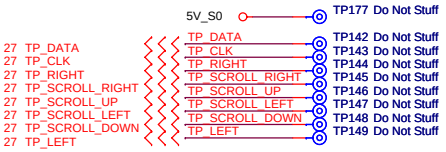


TRING CONN

Test Point

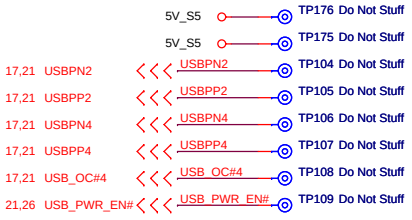
Touch Pad CONN

Test Point near TPAD1



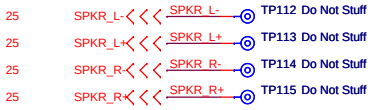
USB ZIF CONN

Test Point

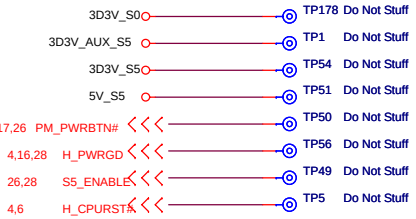


Internal Microphone

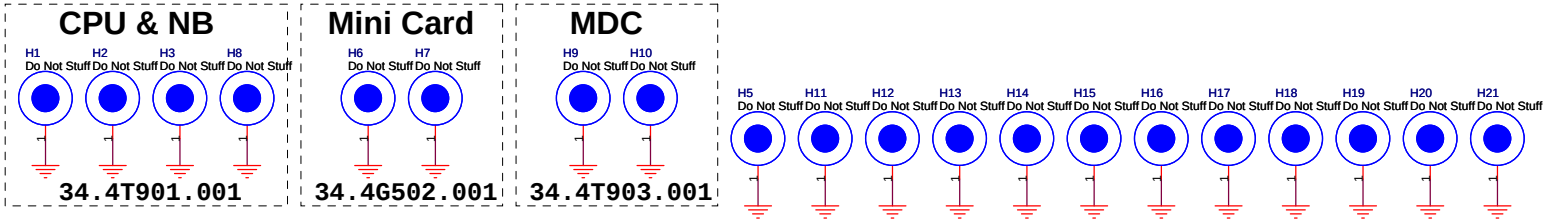
Internal Speaker



Check test point



STAND OFF ON BOTTOM



Test Point放在Dimm Door打開可量測處

RTM

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