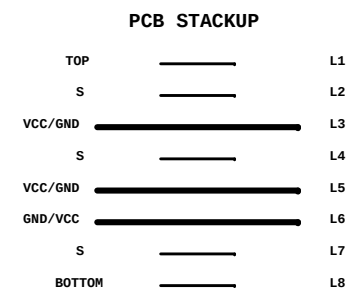


Project code: 91.4CQ01.001  
PCB P/N : 48.4CQ01.0SA  
REVISION : 08274-SA



|                                                                                       |                        |                                                                                                            |           |
|---------------------------------------------------------------------------------------|------------------------|------------------------------------------------------------------------------------------------------------|-----------|
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| Title                                                                                 |                        |                                                                                                            |           |
| <b>BLOCK DIAGRAM</b>                                                                  |                        |                                                                                                            |           |
| Size                                                                                  | Document Number        |                                                                                                            | Rev       |
| Custom                                                                                |                        | <b>JM41 Discrete</b>                                                                                       | <b>SB</b> |
| Date:                                                                                 | Monday, March 02, 2009 | Sheet 1 of                                                                                                 | 48        |

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

| Signal                        | Usage/When Sampled                                                     | Comment                                                                                                                                                                                                          |
|-------------------------------|------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HDA_SDOUT                     | XOR Chain Entrance/<br>PCIE Port Config1 bit1,<br>Rising Edge of PWROK | Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down             |
| HDA_SYNC                      | PCIE config1 bit0,<br>Rising Edge of PWROK.                            | This signal has a weak internal pull-down.<br>Sets bit0 of RPC.PC(Config Registers:Offset 224h)                                                                                                                  |
| GNT2#/<br>GPIO53              | PCIE config2 bit2,<br>Rising Edge of PWROK.                            | This signal has a weak internal pull-up.<br>Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)                                                                                                                  |
| GPIO20                        | Reserved                                                               | This signal should not be pulled high.                                                                                                                                                                           |
| GNT1#/<br>GPIO51              | ESI Strap (Server Only)<br>Rising Edge of PWROK                        | ESI compatible mode is for server platforms only.<br>This signal should not be pulled low for desttop and mobile.                                                                                                |
| GNT3#/<br>GPIO55              | Top-Block<br>Swap Override.<br>Rising Edge of PWROK.                   | Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space).<br>Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT0#:<br>SPI_CS1#/<br>GPIO58 | Boot BIOS Destination<br>Selection 0:1.<br>Rising Edge of PWROK.       | Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10).<br>GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.                                                                                   |
| SPI_MOSI                      | Integrated TPM Enable,<br>Rising Edge of CLPWROK                       | Sample low: the Integrated TPM will be disabled.<br>Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.                                    |
| GPIO49                        | DMI Termination Voltage,<br>Rising Edge of PWROK.                      | The signal is required to be low for desktop applications and required to be high for mobile applications.                                                                                                       |
| SATALED#                      | PCI Express Lane<br>Reversal. Rising Edge<br>of PWROK.                 | Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)                                                                                                                          |
| SPKR                          | No Reboot.<br>Rising Edge of PWROK.                                    | If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.                                            |
| TP3                           | XOR Chain Entrance.<br>Rising Edge of PWROK.                           | This signal should not be pull low unless using XOR Chain testing.                                                                                                                                               |
| GPIO33/<br>HDA_DOCK<br>_EN#   | Flash Descriptor<br>Security Override Strap<br>Rising Edge of PWROK    | Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.      |

ICH9M Integrated Pull-up  
and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

| SIGNAL                     | Resistor Type/Value                                                                                                      |
|----------------------------|--------------------------------------------------------------------------------------------------------------------------|
| CL_CLK[1:0]                | PULL-UP 20K                                                                                                              |
| CL_DATA[1:0]               | PULL-UP 20K                                                                                                              |
| CL_RST0#                   | PULL-UP 20K                                                                                                              |
| DPRSLPVR/GPIO16            | PULL-DOWN 20K                                                                                                            |
| ENERGY_DETECT              | PULL-UP 20K                                                                                                              |
| HDA_BIT_CLK                | PULL-DOWN 20K                                                                                                            |
| HDA_DOCK_EN#/GPIO33        | PULL-UP 20K                                                                                                              |
| HDA_RST#                   | PULL-DOWN 20K                                                                                                            |
| HDA_SDIN[3:0]              | PULL-DOWN 20K                                                                                                            |
| HDA_SDOUT                  | PULL-DOWN 20K                                                                                                            |
| HDA_SYNC                   | PULL-DOWN 20K                                                                                                            |
| GLAN_DOCK#                 | The pull-up or pull-down active when configured for native LAN controller functionality and determined by LAN controller |
| GNT[3:0]#/GPIO[55, 53, 51] | PULL-UP 20K                                                                                                              |
| GPIO[20]                   | PULL-DOWN 20K                                                                                                            |
| GPIO[49]                   | PULL-UP 20K                                                                                                              |
| LDA[3:0]#/FWH[3:0]#        | PULL-UP 20K                                                                                                              |
| LAN_RXD[2:0]               | PULL-UP 20K                                                                                                              |
| LDRQ[0]                    | PULL-UP 20K                                                                                                              |
| LDRQ[1]/GPIO23             | PULL-UP 20K                                                                                                              |
| PME#                       | PULL-UP 20K                                                                                                              |
| PWRBTN#                    | PULL-UP 20K                                                                                                              |
| SATALED#                   | PULL-UP 15K                                                                                                              |
| SPI_CS1#/GPIO58/CLGPIO6    | PULL-UP 20K                                                                                                              |
| SPI_MOSI                   | PULL-DOWN 20K                                                                                                            |
| SPI_MISO                   | PULL-UP 20K                                                                                                              |
| SPKR                       | PULL-DOWN 20K                                                                                                            |
| TACH_[3:0]                 | PULL-UP 20K                                                                                                              |
| TP[3]                      | PULL-UP 20K                                                                                                              |
| USB[11:0][P,N]             | PULL-DOWN 15K                                                                                                            |

Cantiga chipset and ICH9M I/O controller  
Hub strapping configuration

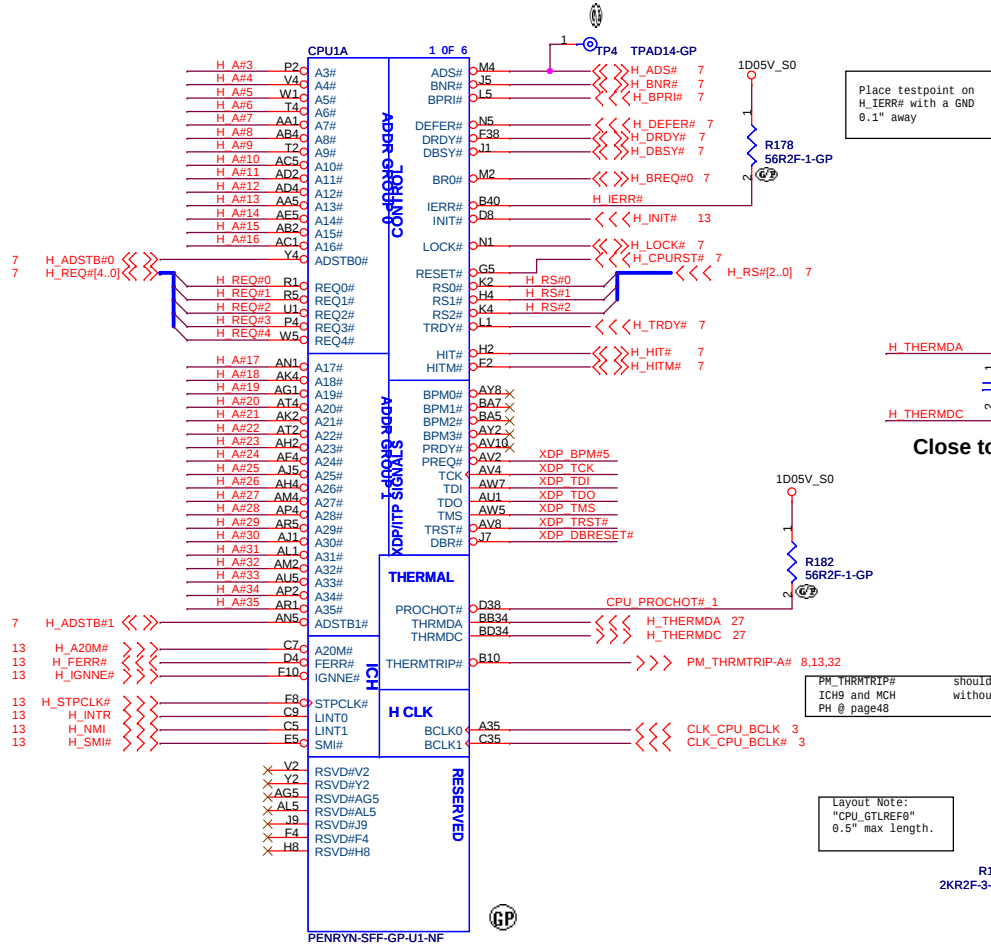
Montevina Platform Design guide 22339 0.5  
page 218

| Pin Name                                     | Strap Description                                            | Configuration                                                                                                                                                                 |
|----------------------------------------------|--------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG[2:0]                                     | FSB Frequency Select                                         | 000 = FSB1067<br>011 = FSB667<br>010 = FSB800<br>others = Reserved                                                                                                            |
| CFG[4:3]<br>CFG8<br>CFG[15:14]<br>CFG[18:17] | Reserved                                                     |                                                                                                                                                                               |
| CFG5                                         | DMI x2 Select                                                | 0 = DMI x2<br>1 = DMI x4 (Default)                                                                                                                                            |
| CFG6                                         | iTPM Host Interface                                          | 0= The iTPM Host Interface is enabled(Note2)<br>1=The iTPM Host Interface is disalbed(default)                                                                                |
| CFG7                                         | Intel Management<br>engine Crypto strap                      | 0 = Transport Layer Security (TLS) cipher suite with no confidentiality<br>1 = TLS cipher suite with confidentiality (default)                                                |
| CFG9                                         | PCIE Graphics Lane                                           | 0 = Reverse Lanes,15->0,14->1 ect..<br>1= Normal operation(Default):Lane Numbered in order                                                                                    |
| CFG10                                        | PCIE Loopback enable                                         | 0 = Enable (Note 3)<br>1= Disabled (default)                                                                                                                                  |
| CFG[13:12]                                   | XOR/ALL                                                      | 00 = Reserve<br>10 = XOR mode Enabled<br>01 = ALLZ mode Enabled (Note 3)<br>11 = Disabled (default)                                                                           |
| CFG16                                        | FSB Dynamic ODT                                              | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled (Default)                                                                                                                 |
| CFG19                                        | DMI Lane Reversal                                            | 0 = Normal operation(Default):<br>Lane Numbered in Order<br>1 = Reverse Lanes<br>x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3)<br>DMI<br>DMI<br>x2 mode[MCH -> ICH]:(3->0,2->1) |
| CFG20                                        | Digital Display Port (SDVO/DP/iHDMI)<br>Concurrent with PCIE | 0 = Only Digital Display Port or PCIE is operational (Default)<br>1 = Digital display port and PCie are operating simulatanuously via the PEG port                            |
| SDVO_CTRLDATA                                | SDVO Present                                                 | 0 =No SDVO Card Present (Default)<br>1 = SDVO Card Present                                                                                                                    |
| L_DDC_DATA                                   | Local Flat Panel (LFP) Present                               | 0 = LFP Disabled (Default)<br>1= LFP Card Present; PCIE disabled                                                                                                              |

NOTE:  
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.  
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.  
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.



7 H\_A#(35..3) <<< H\_A#(35..3)



H\_DINV#(3..0) <<>> H\_DINV#(3..0) 7  
H\_DSTBN#(3..0) <<>> H\_DSTBN#(3..0) 7  
H\_DSTBP#(3..0) <<>> H\_DSTBP#(3..0) 7  
H\_D#(63..0) <<>> H\_D#(63..0) 7

7 H\_A#(35..3) <<< H\_A#(35..3)  
13 H\_A20M# <<< H\_A20M#  
13 H\_FERR# <<< H\_FERR#  
13 H\_IGNNE# <<< H\_IGNNE#  
13 H\_STPCLK# <<< H\_STPCLK#  
13 H\_INTR# <<< H\_INTR#  
13 H\_NMI# <<< H\_NMI#  
13 H\_SMI# <<< H\_SMI#

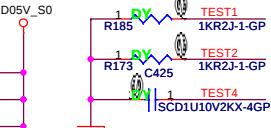
H\_FERR# C442  
H\_STPCLK# C97  
H\_IGNNE# C436  
H\_INTR# C439  
H\_PWVRGD# C437  
H\_A20M# C429  
H\_SMI# C435  
H\_NMI# C430  
H\_INIT# C431  
C428

XDP TMS R140  
XDP TDI R141  
XDP BPM#5 R143  
XDP TDO R142

XDP DBRESET# R37  
XDP TCK R145  
XDP TRST# R144

All place within 2" to CPU

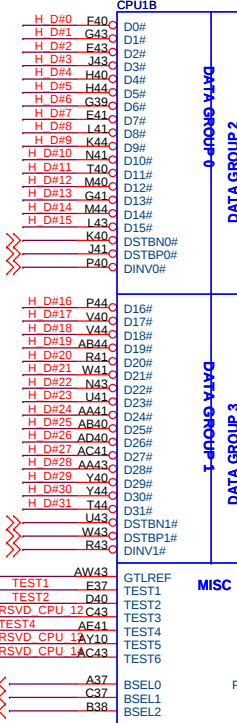
Layout Note:  
"CPU\_GTLREF#"  
0.5" max length.



Net "TEST4" as short as possible,  
make sure "TEST4" routing is  
reference to GND and away other  
noisy signals

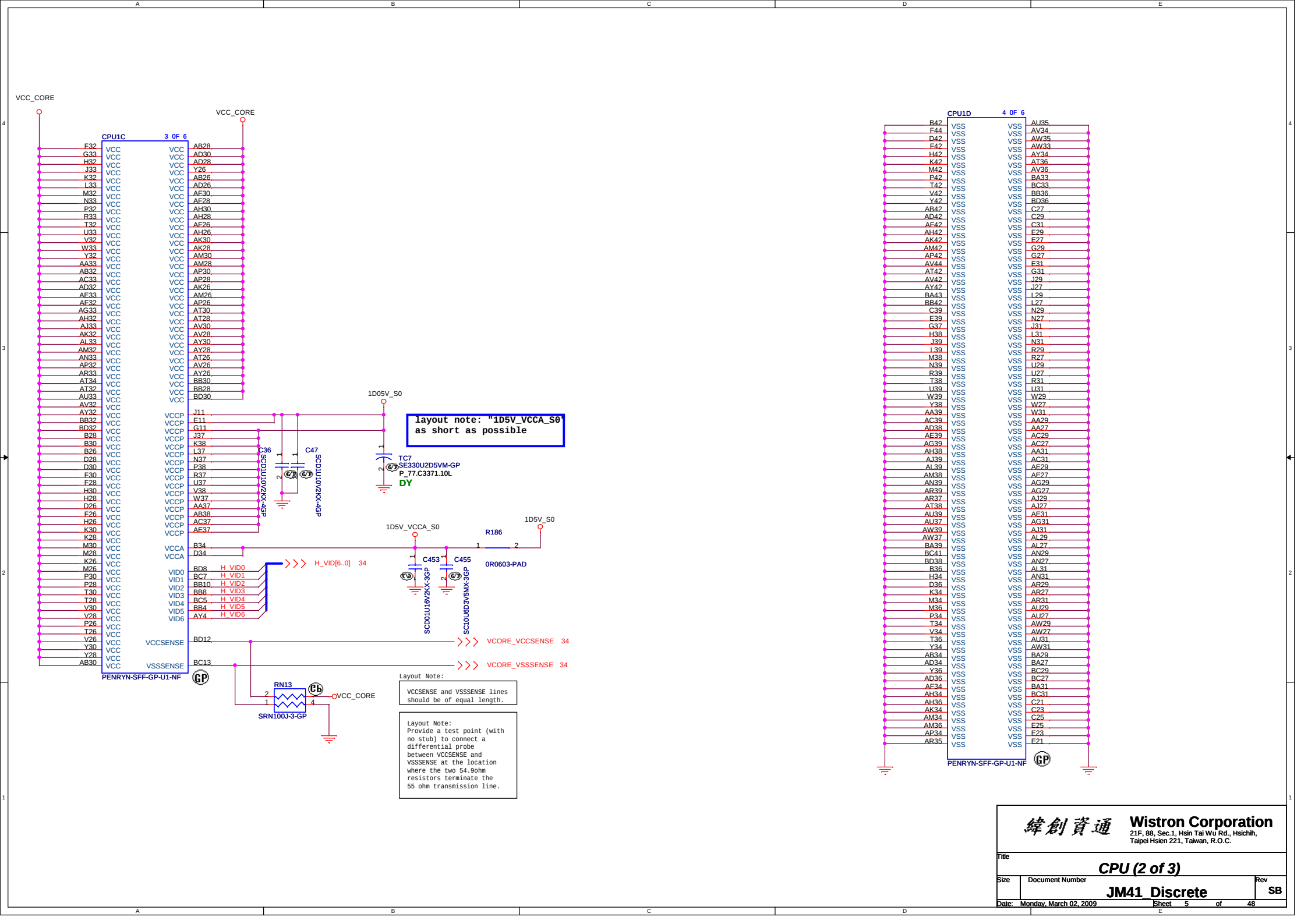
H\_DPRSTP# TP10  
H\_DPSP# TP69  
H\_DPWR# TP62  
H\_PWVRGD# TP12  
H\_CPUSLP# TP68  
H\_INIT# TP13  
H\_CPURST# TP9

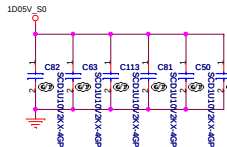
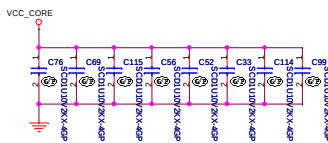
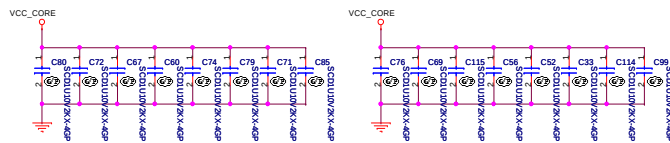
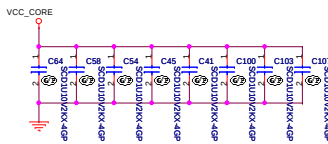
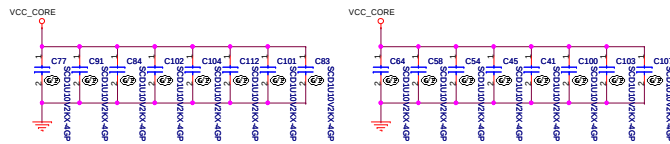
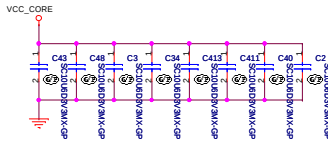
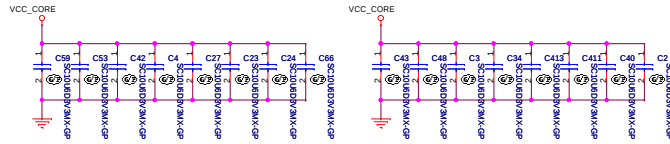
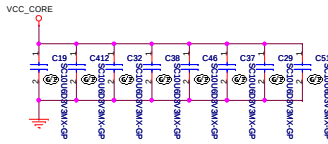
Place these TP on button-side,  
easy to measure.



Layout Note:  
Comp0, 2 connect with Zo=27.4 ohm, make  
trace length shorter than 0.5"  
Comp1, 3 connect with Zo=55 ohm, make  
trace length shorter than 0.5"

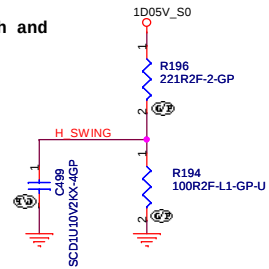
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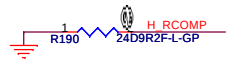


H\_SWING routing Trace width and Spacing use 10 / 20 mil

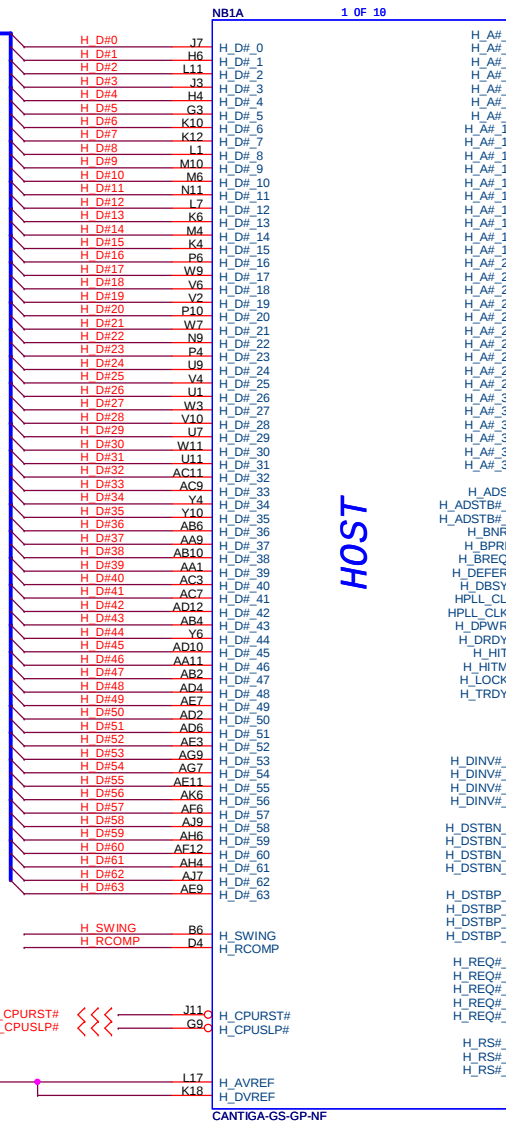
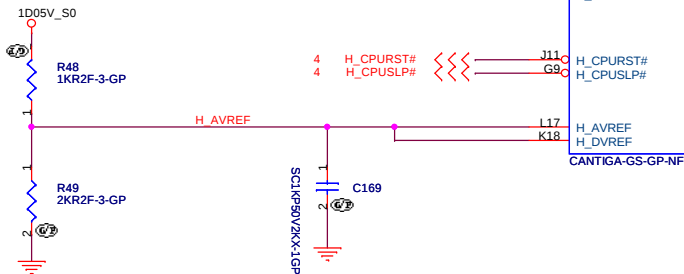
H\_SWING Resistors and Capacitors close MCH 500 mil ( MAX )



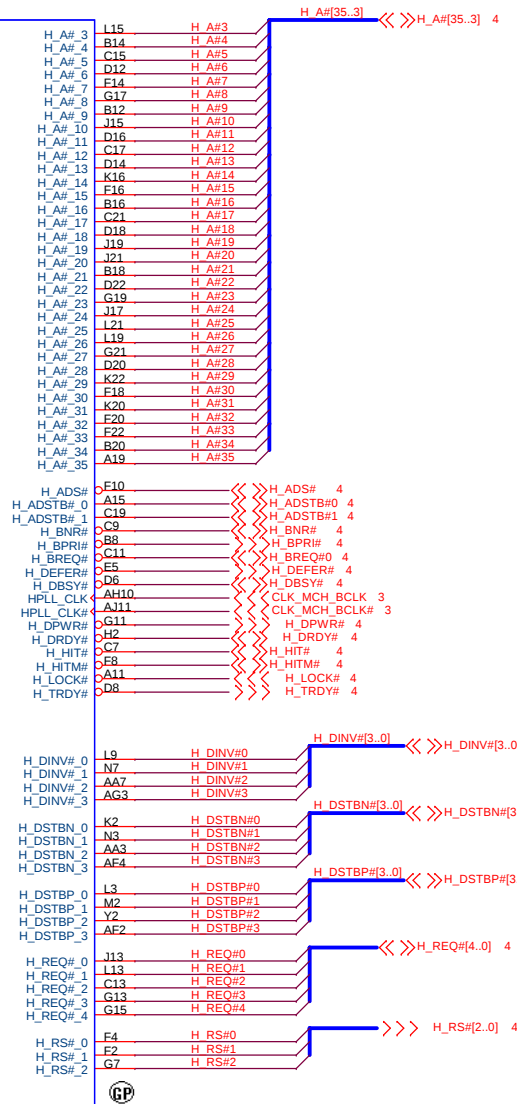
H\_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip ( < 0.5"

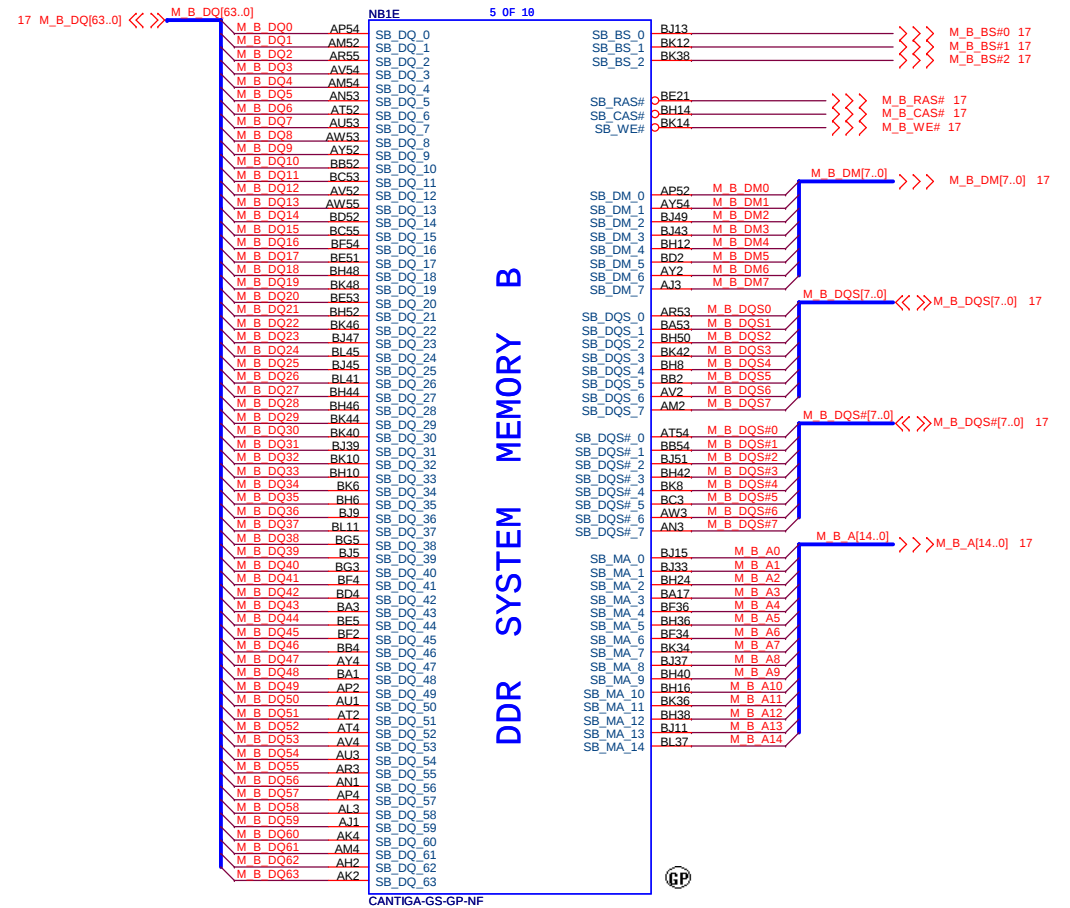
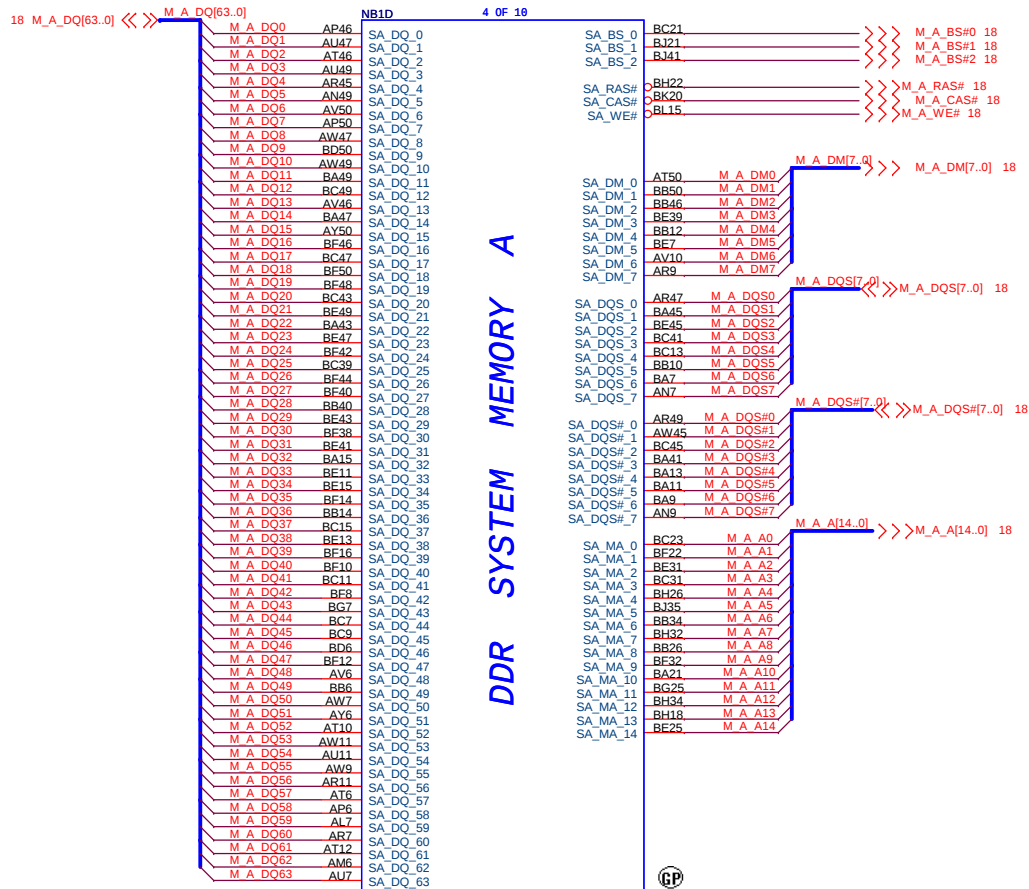


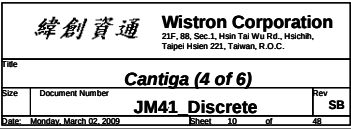
HOST

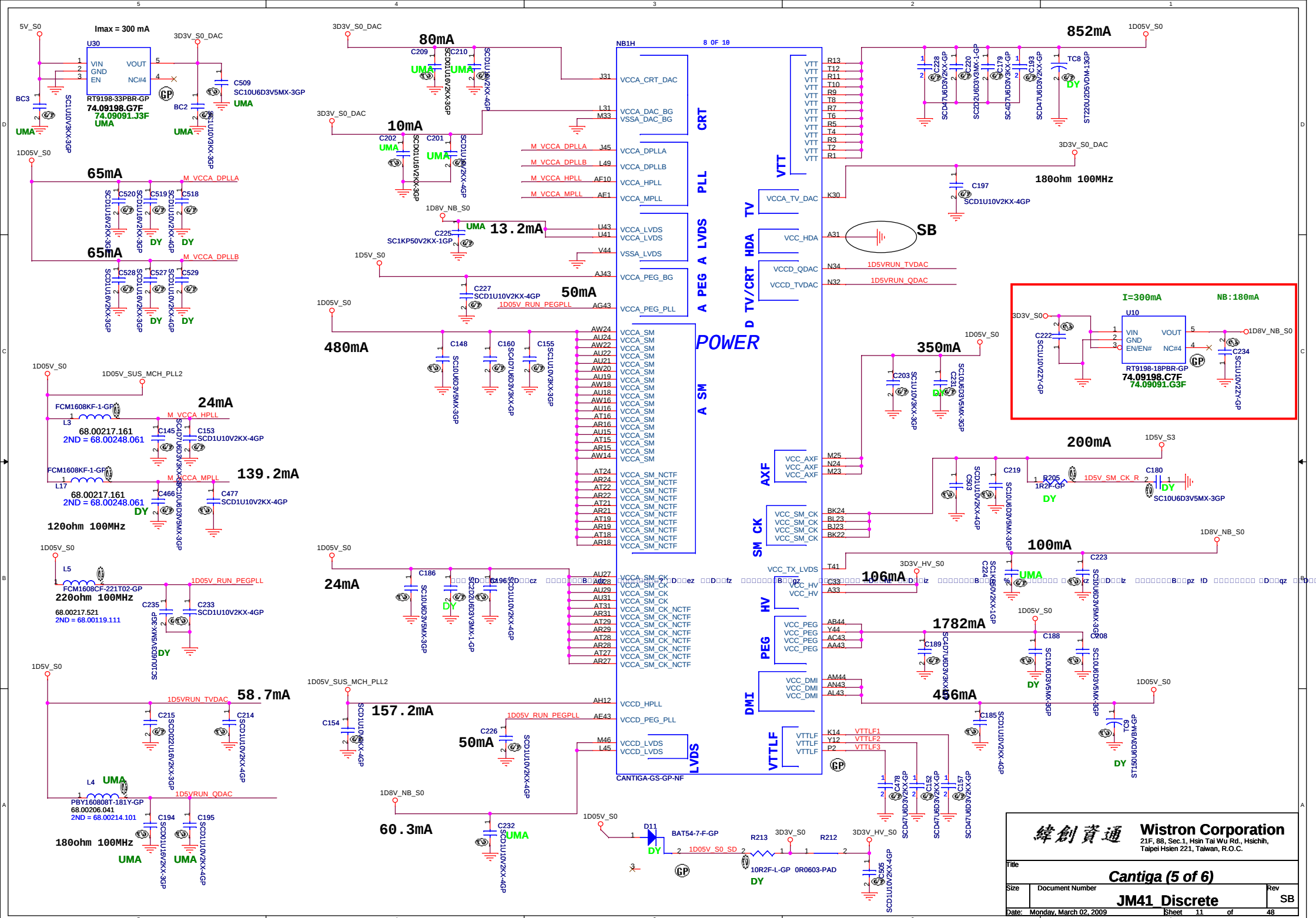


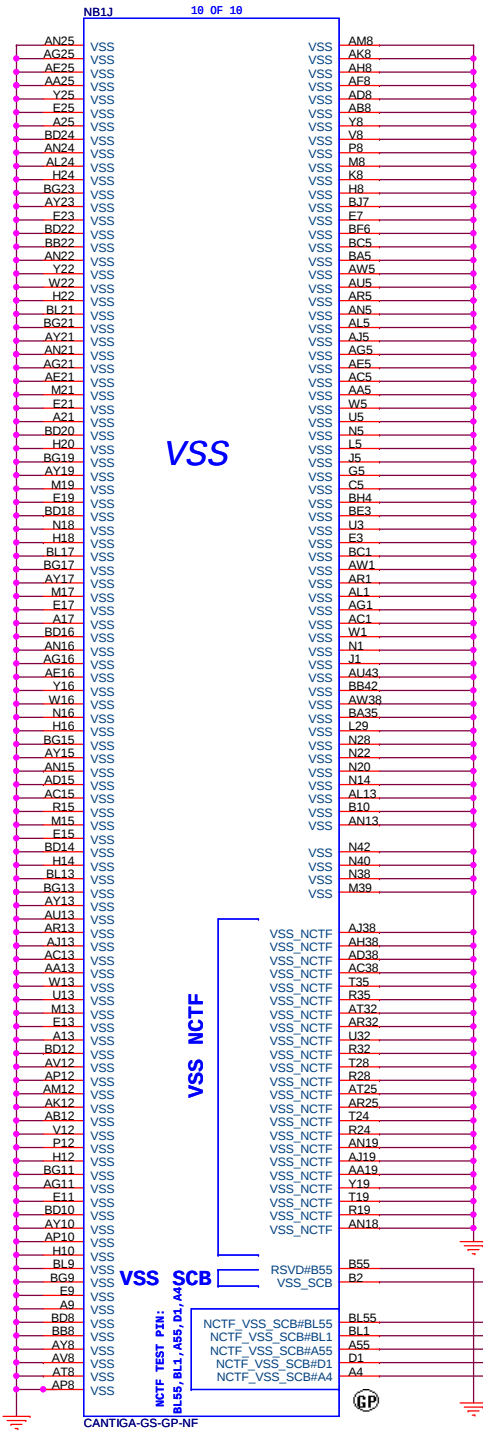
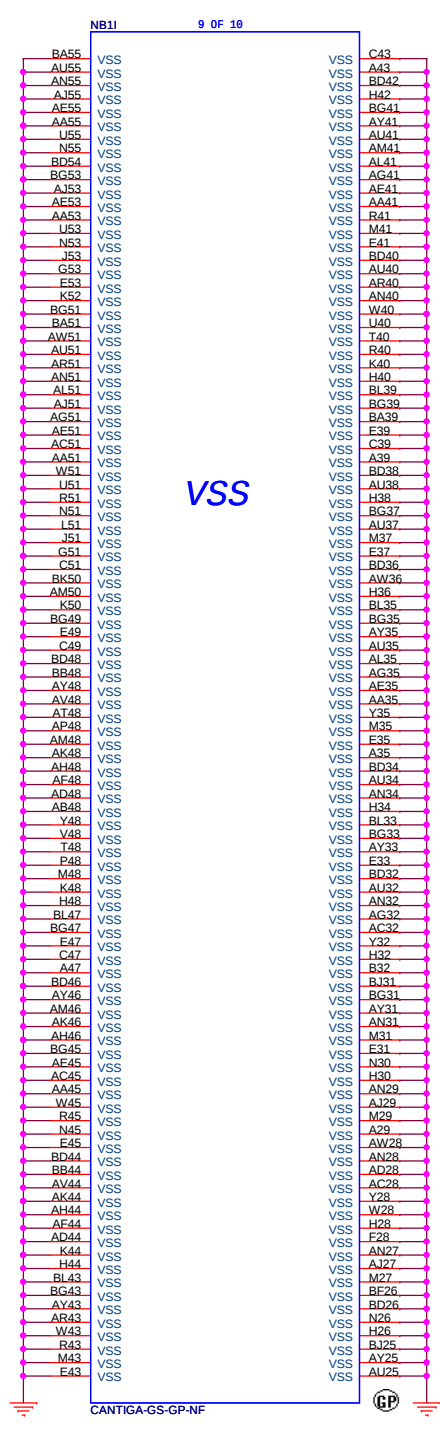
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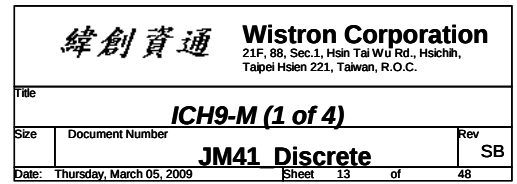


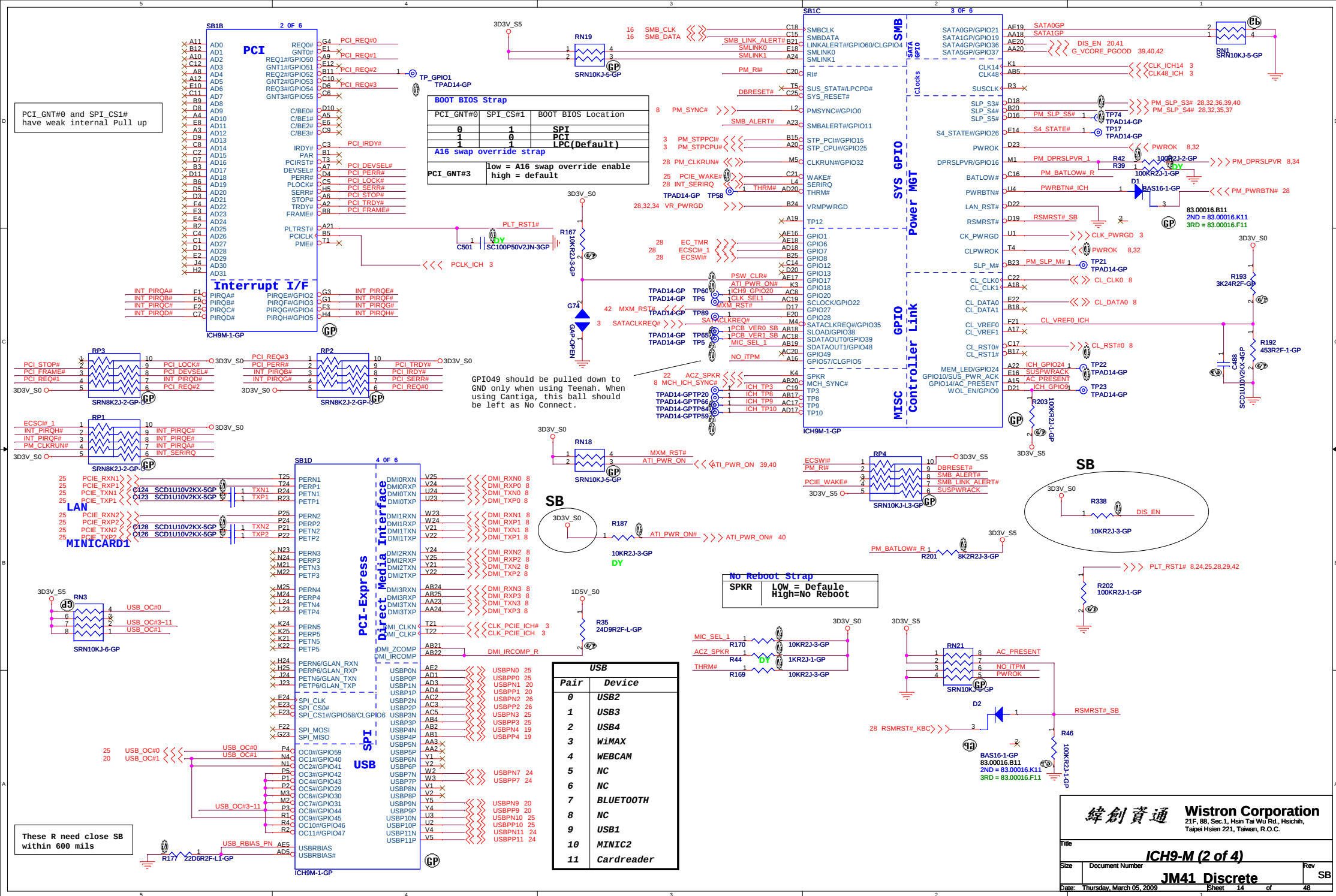
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Title  
**Cantiga (6 of 6)**

Size Document Number Rev  
**JM41 Discrete** SB

Date: Monday, March 02, 2009 Sheet 12 of 48





657mA

6uA in G3

1.13A

23mA

50mA

1mA

VCC3\_3=278mA

32mA

32mA

177mA

18mA

47mA

SATA+USB=1.56A

USBPLL=10mA

23mA

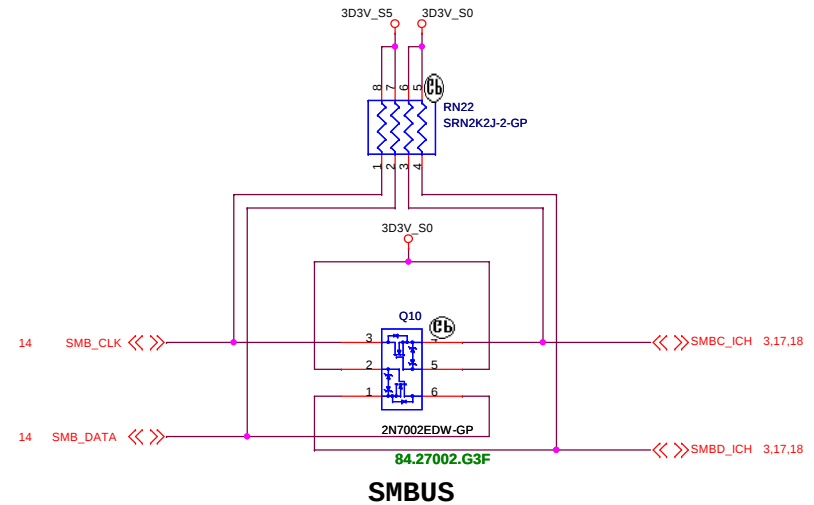
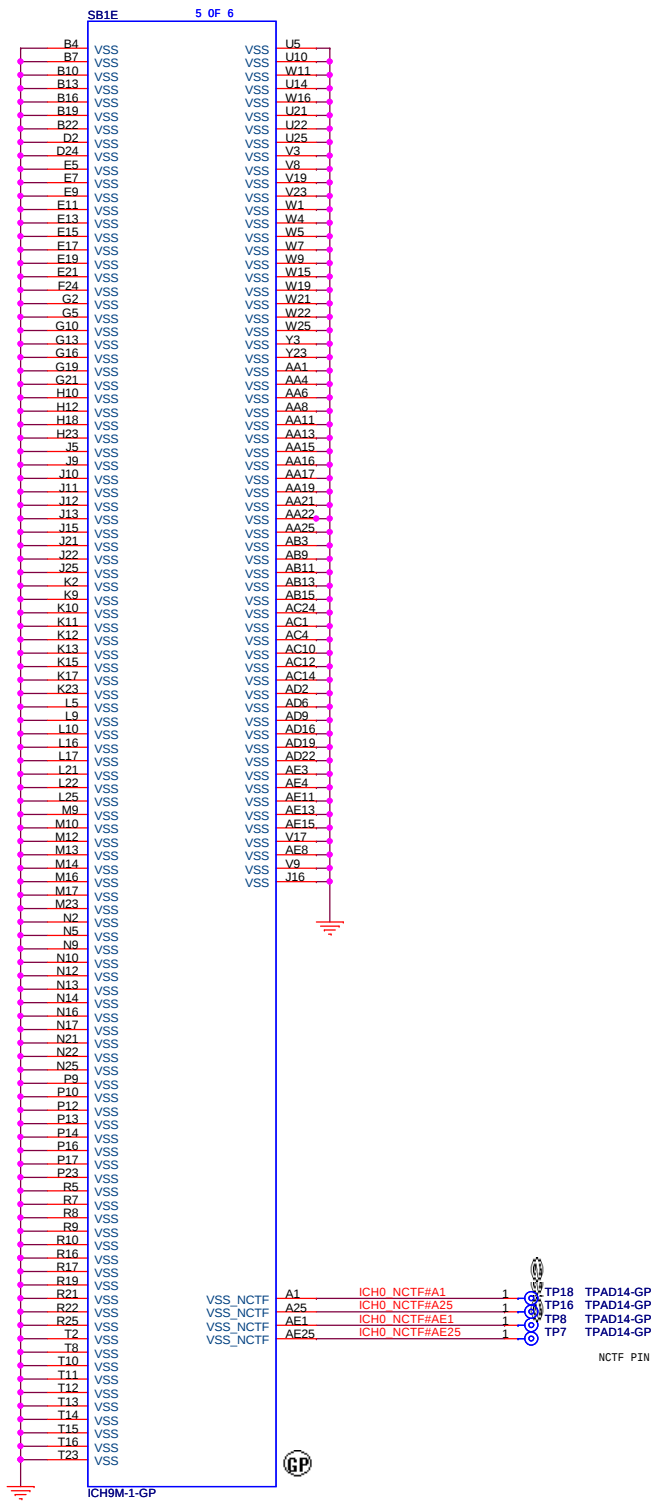
80mA

1mA

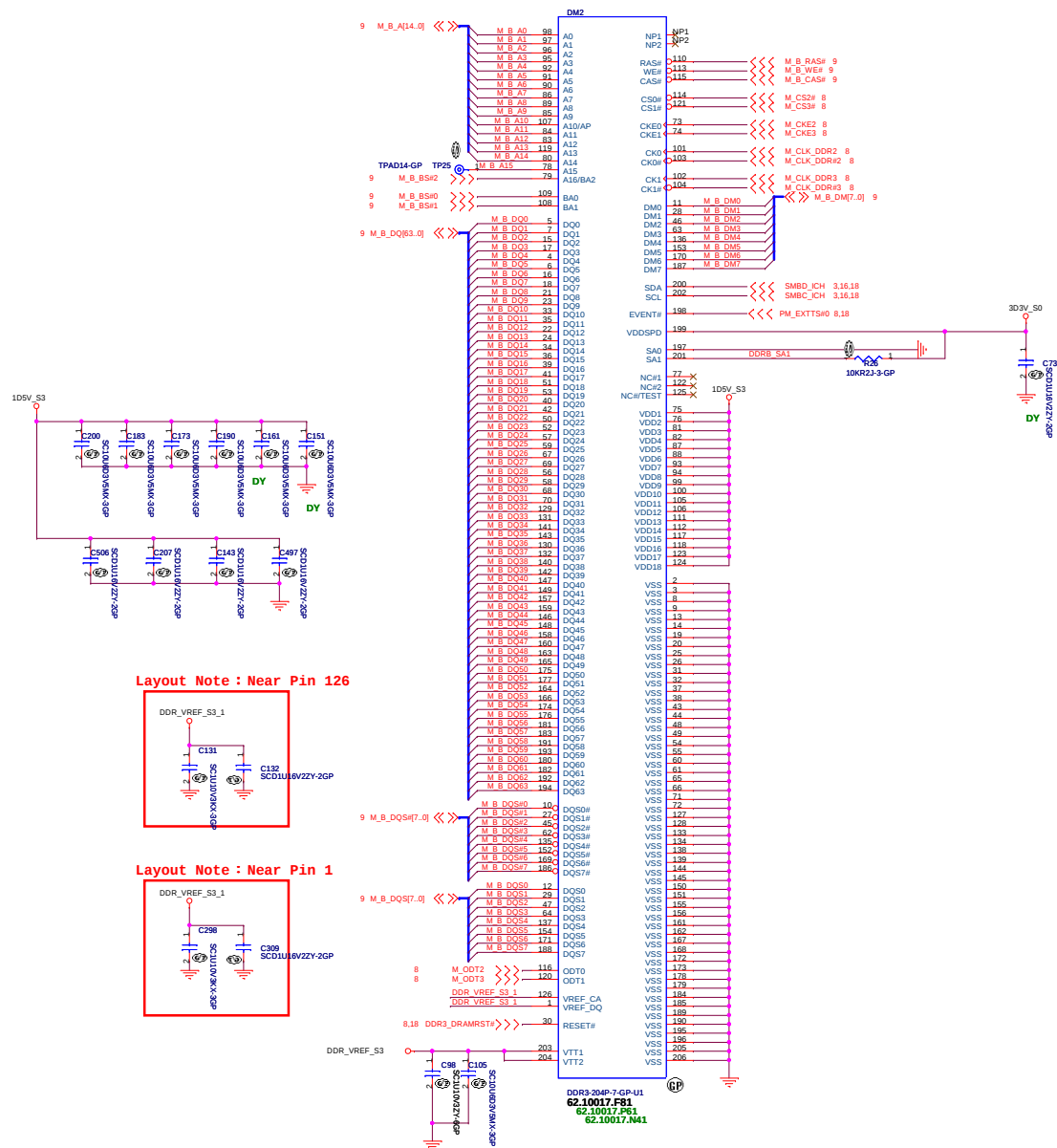
\*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

2mA

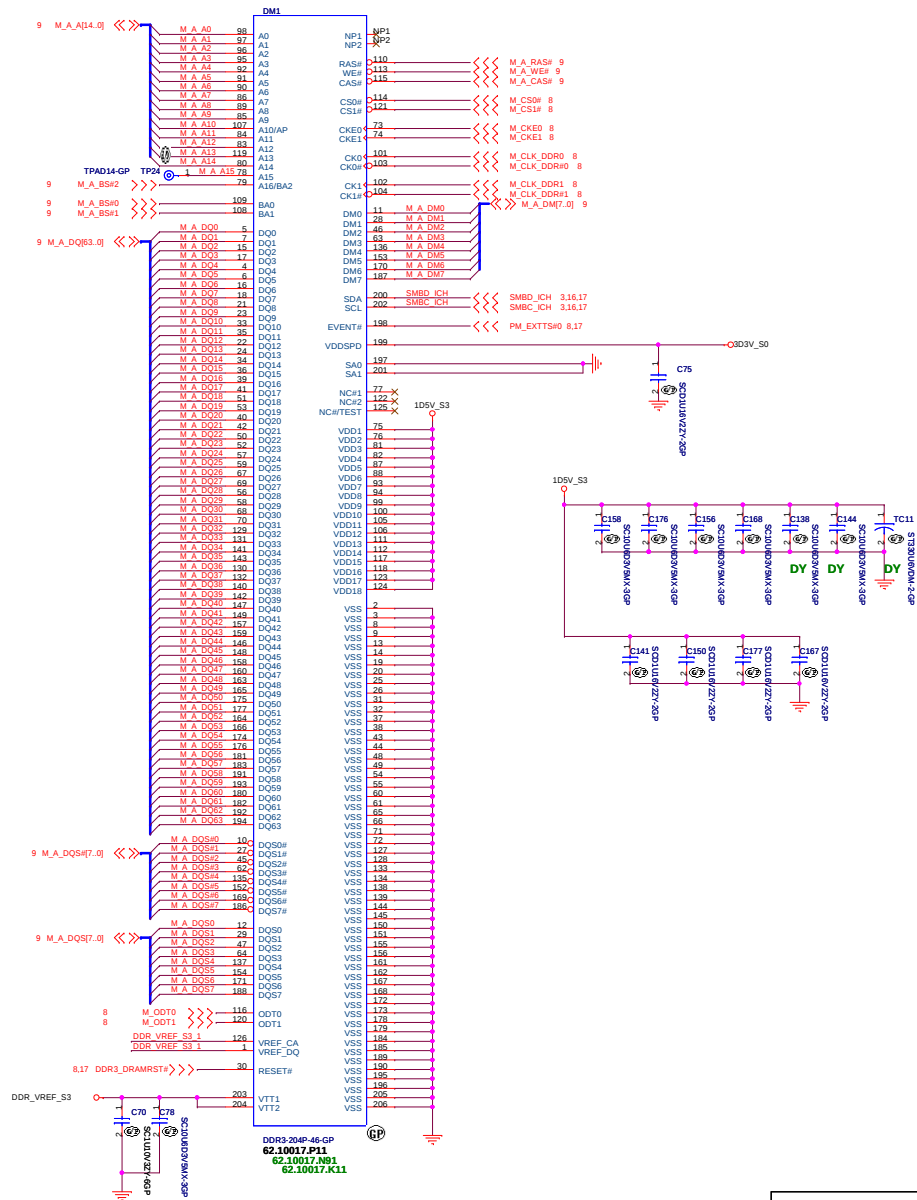
2mA



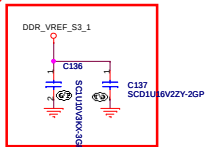
## DDR3 SOCKET\_1



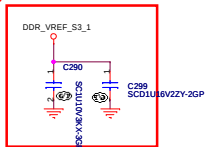
## DDR3 SOCKET\_2



**Layout Note : Near Pin 126**

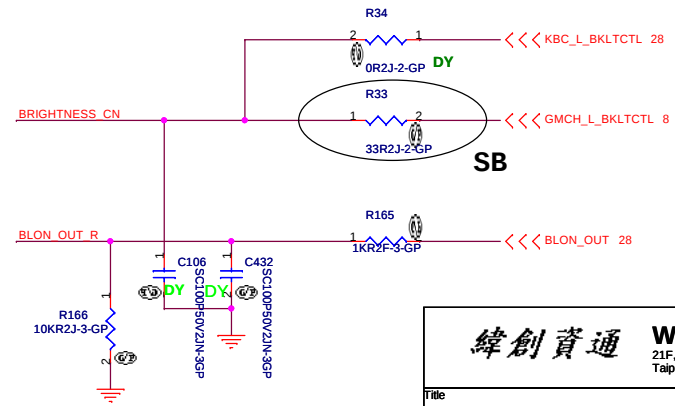
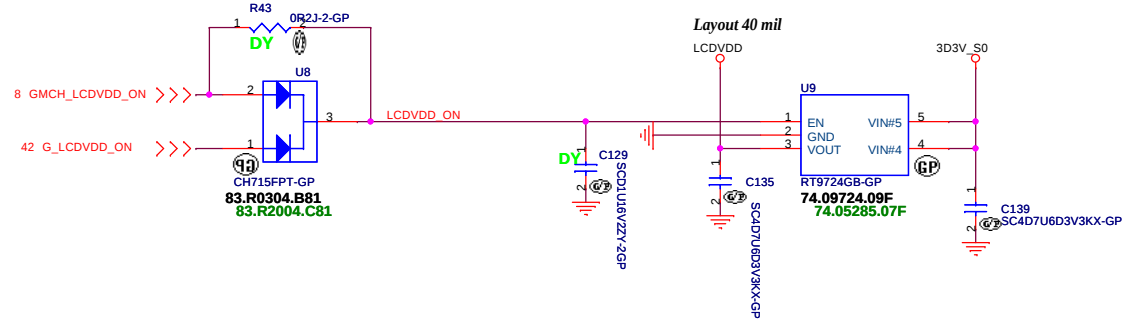
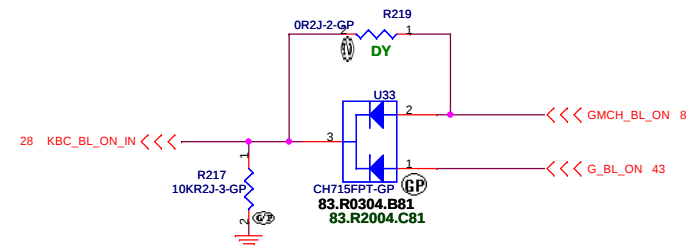
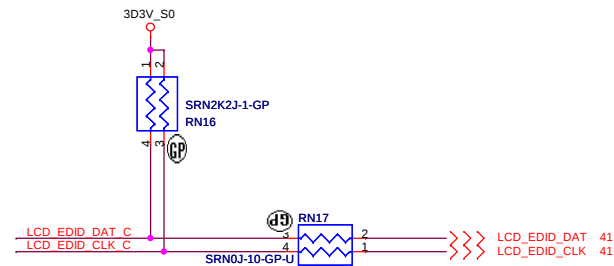
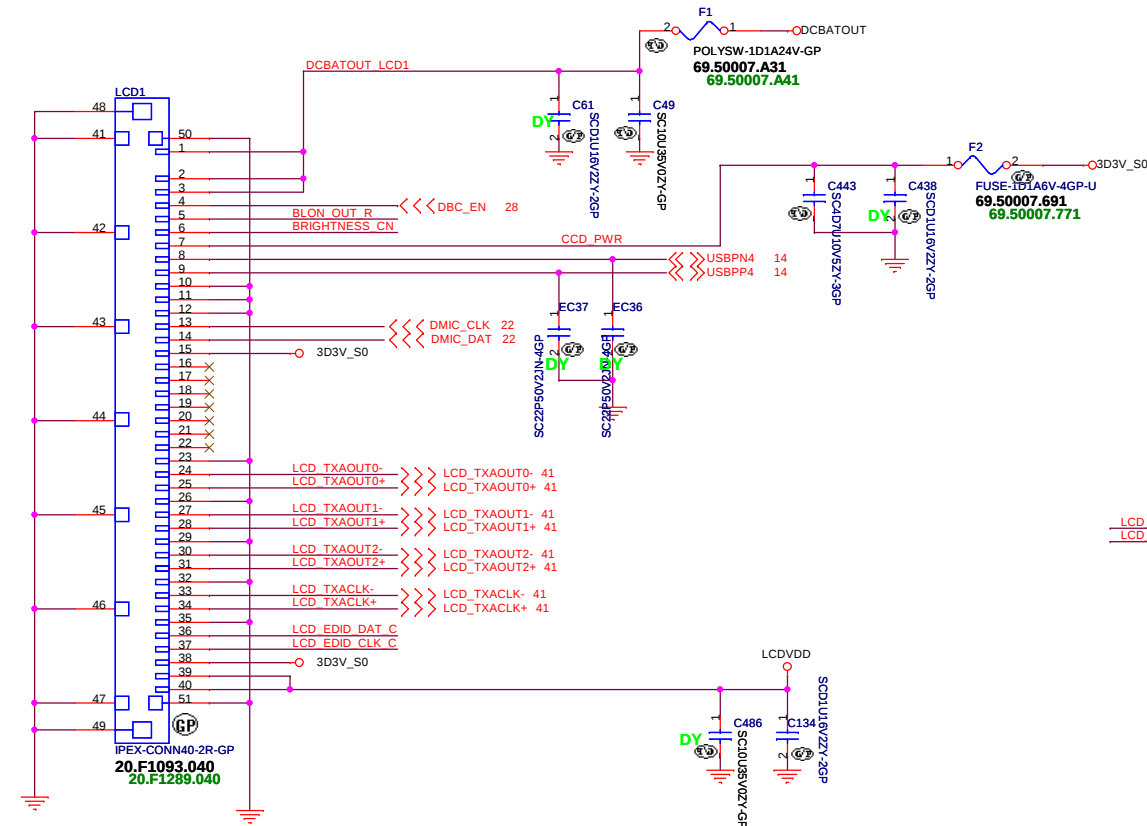


**Layout Note : Near Pin 1**



# LCD/CCD CONN

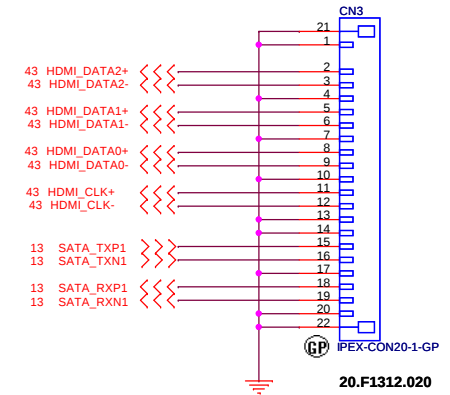
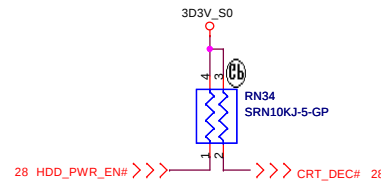
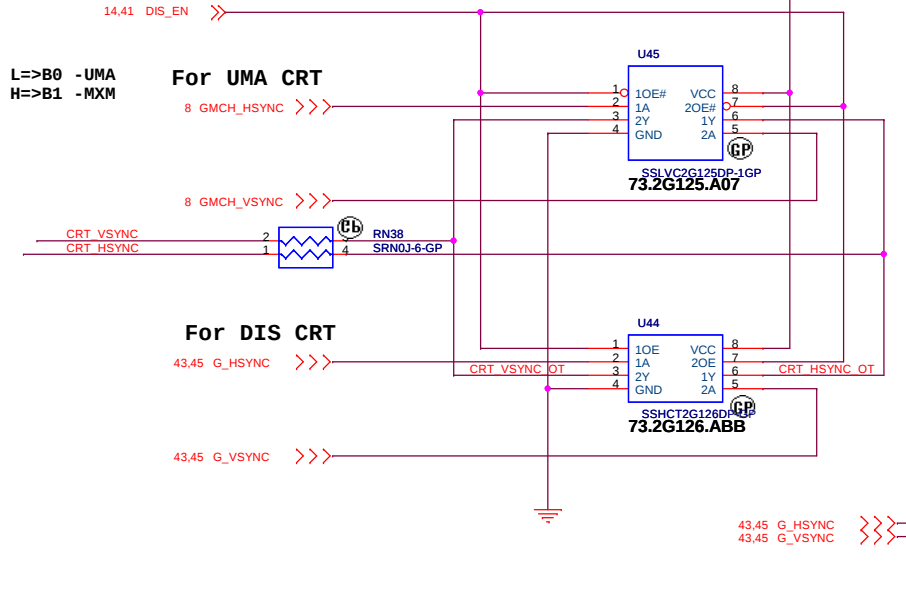
# Internal MIC



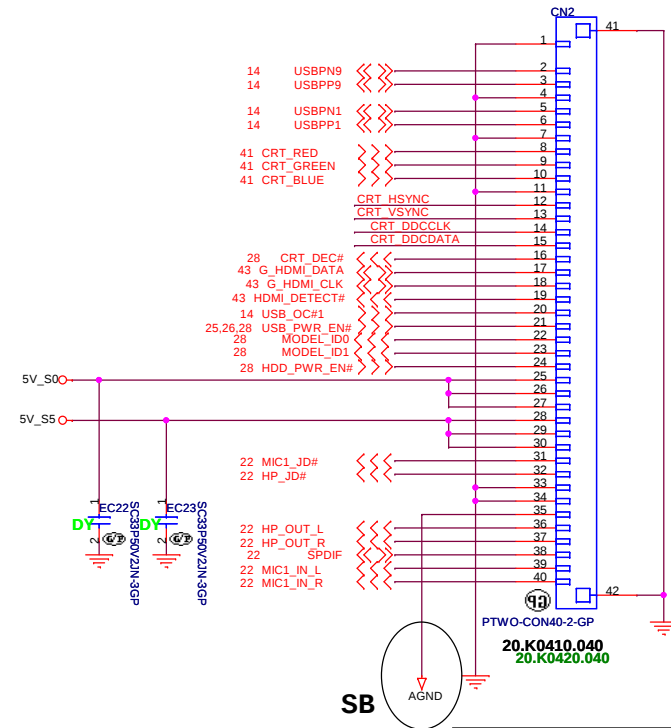
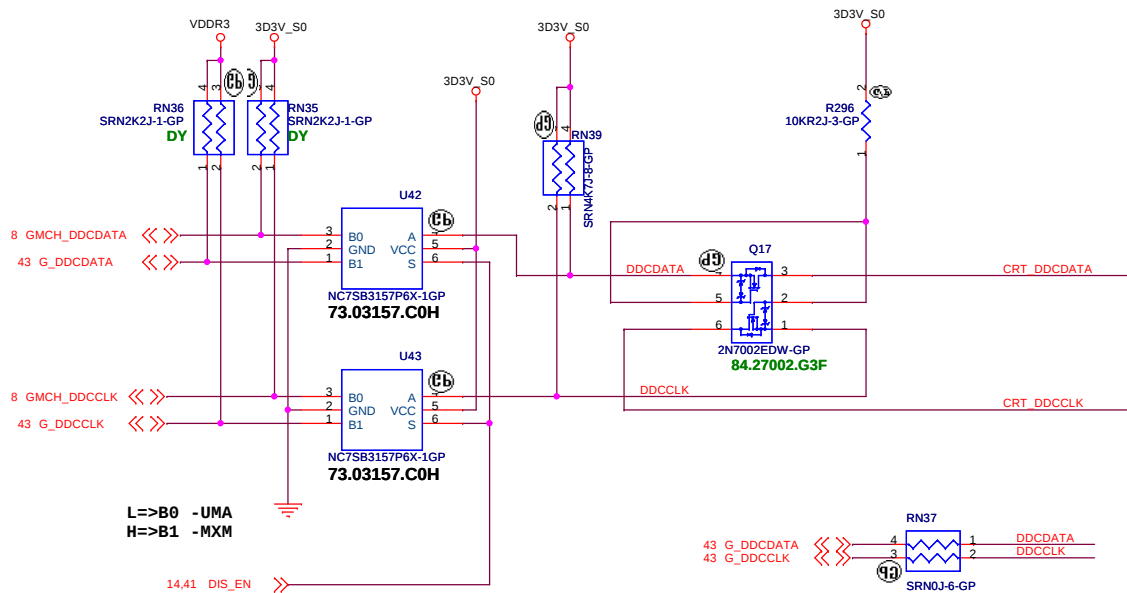
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|                              |                 |     |               |
|------------------------------|-----------------|-----|---------------|
| Title                        |                 |     | LCD CONN      |
| Size                         | Document Number | Rev | SB            |
| Date: Monday, March 02, 2009 |                 |     | JM41 Discrete |
| Sheet                        | 19              | of  | 48            |

# Hsync & Vsync level shift



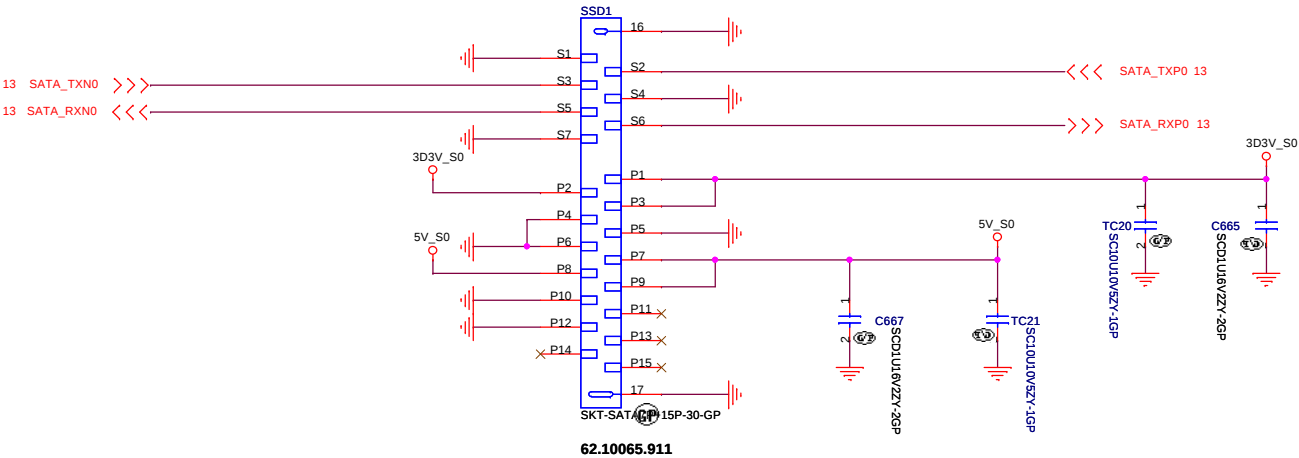
# DDC\_CLK & DATA level shift



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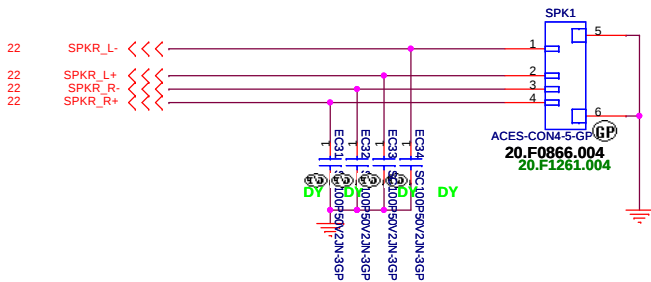
|       |                        |       |               |       |
|-------|------------------------|-------|---------------|-------|
| Title |                        |       | CRT BD CONN   |       |
| Size  | Document Number        |       | Rev           |       |
|       |                        |       | JM41 Discrete |       |
| Date: | Monday, March 02, 2009 | Sheet | 20            | of 48 |

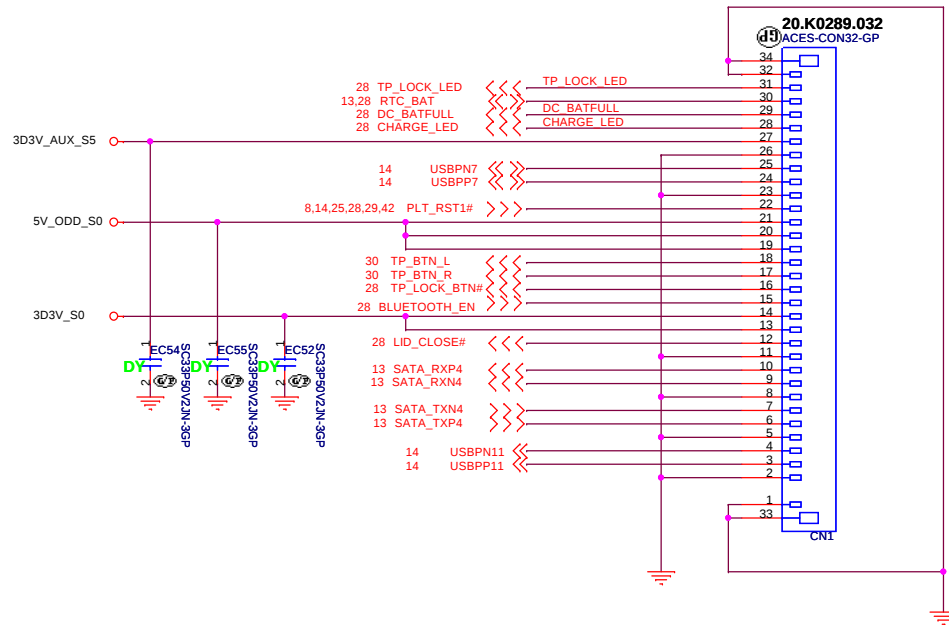
SSD SATA Connector

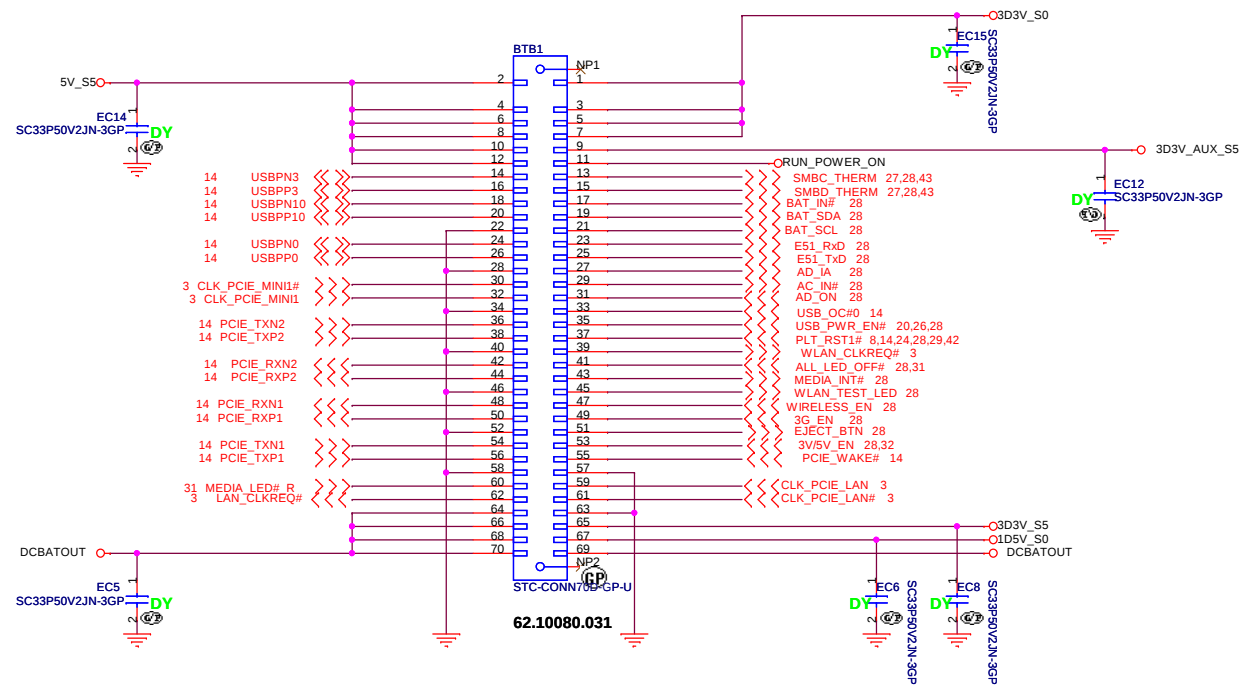




Internal Speaker

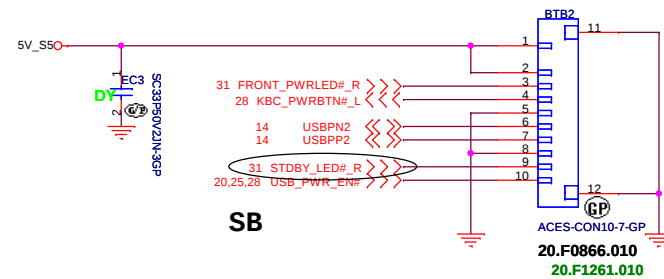


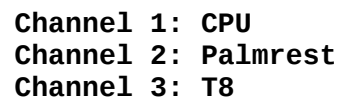
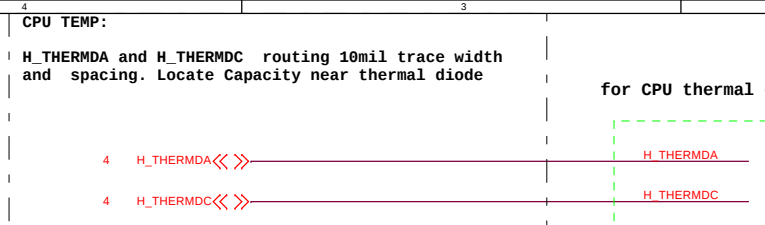




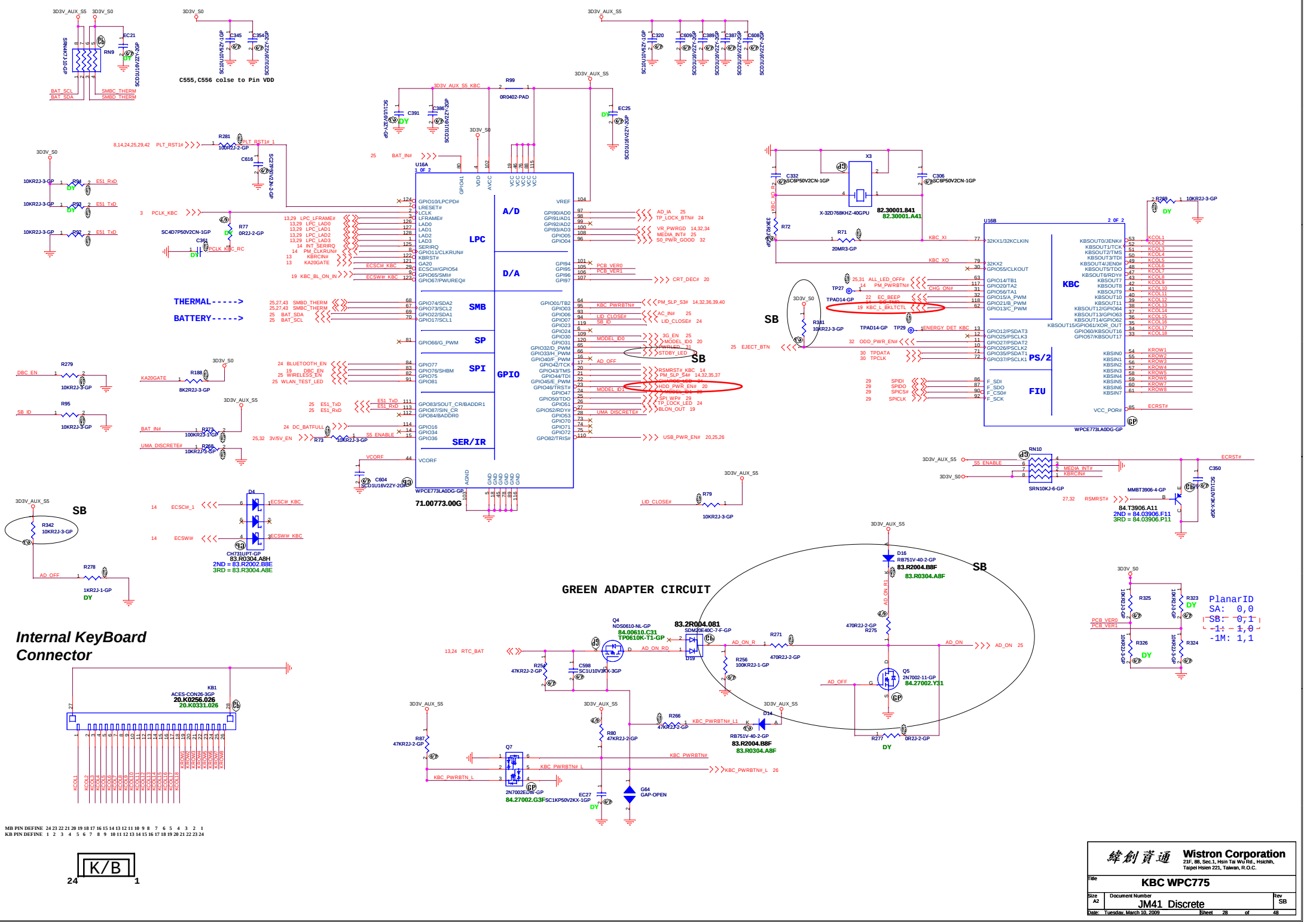
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|              |                         |                |
|--------------|-------------------------|----------------|
| Title        |                         |                |
| MINI BD CONN |                         |                |
| Size         | Document Number         | Rev            |
| A3           | JM41_Discrete           | SB             |
| Date:        | Tuesday, March 03, 2009 | Sheet 25 of 48 |





| SHDN SEL         |                                                                         | TRIP SET      |          |
|------------------|-------------------------------------------------------------------------|---------------|----------|
| PULL UP RESISTOR | MODE OF OPERATION                                                       | Ttrip(degree) | RSET(1%) |
| <=4.7K OHM       | EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED, REC DISABLED   | 85            | 562      |
|                  |                                                                         | 86            | 604      |
|                  |                                                                         | 87            | 649      |
|                  |                                                                         | 88            | 698      |
| 6.8K OHM         | EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED, REC ENABLED     | 89            | 750      |
|                  |                                                                         | 90            | 787      |
|                  |                                                                         | 91            | 845      |
|                  |                                                                         | 92            | 909      |
| 10K OHM          | EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED | 93            | 953      |
|                  |                                                                         | 94            | 1020     |
|                  |                                                                         | 95            | 1100     |
|                  |                                                                         |               |          |
| 15K OHM          | INTERNAL DIODE                                                          |               |          |
|                  |                                                                         |               |          |
|                  |                                                                         |               |          |
|                  |                                                                         |               |          |
| 22K OHM          | EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED |               |          |
|                  |                                                                         |               |          |
|                  |                                                                         |               |          |
|                  |                                                                         |               |          |
| >=33K OHM        | EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED |               |          |
|                  |                                                                         |               |          |
|                  |                                                                         |               |          |
|                  |                                                                         |               |          |

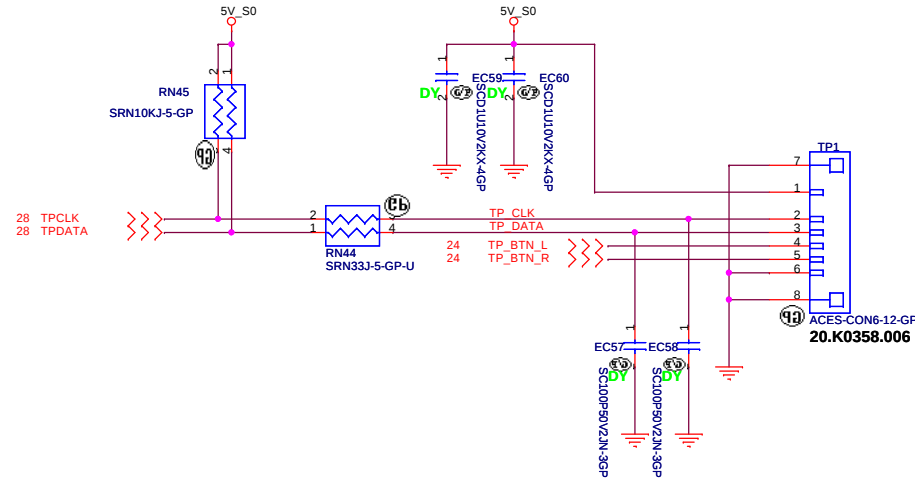


MB PIN DEFINE: 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1  
KB PIN DEFINE: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

24 **K/B** 1

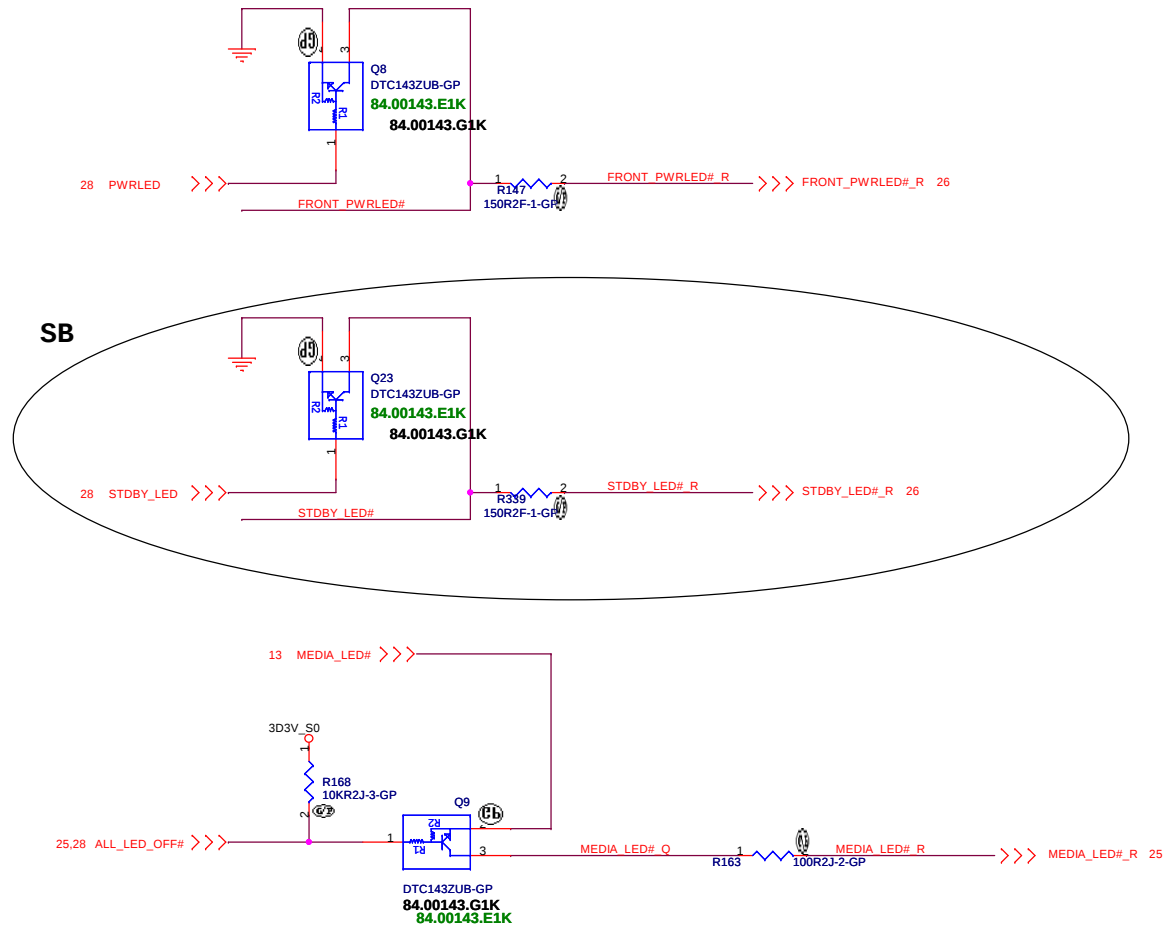


# TOUCH PAD

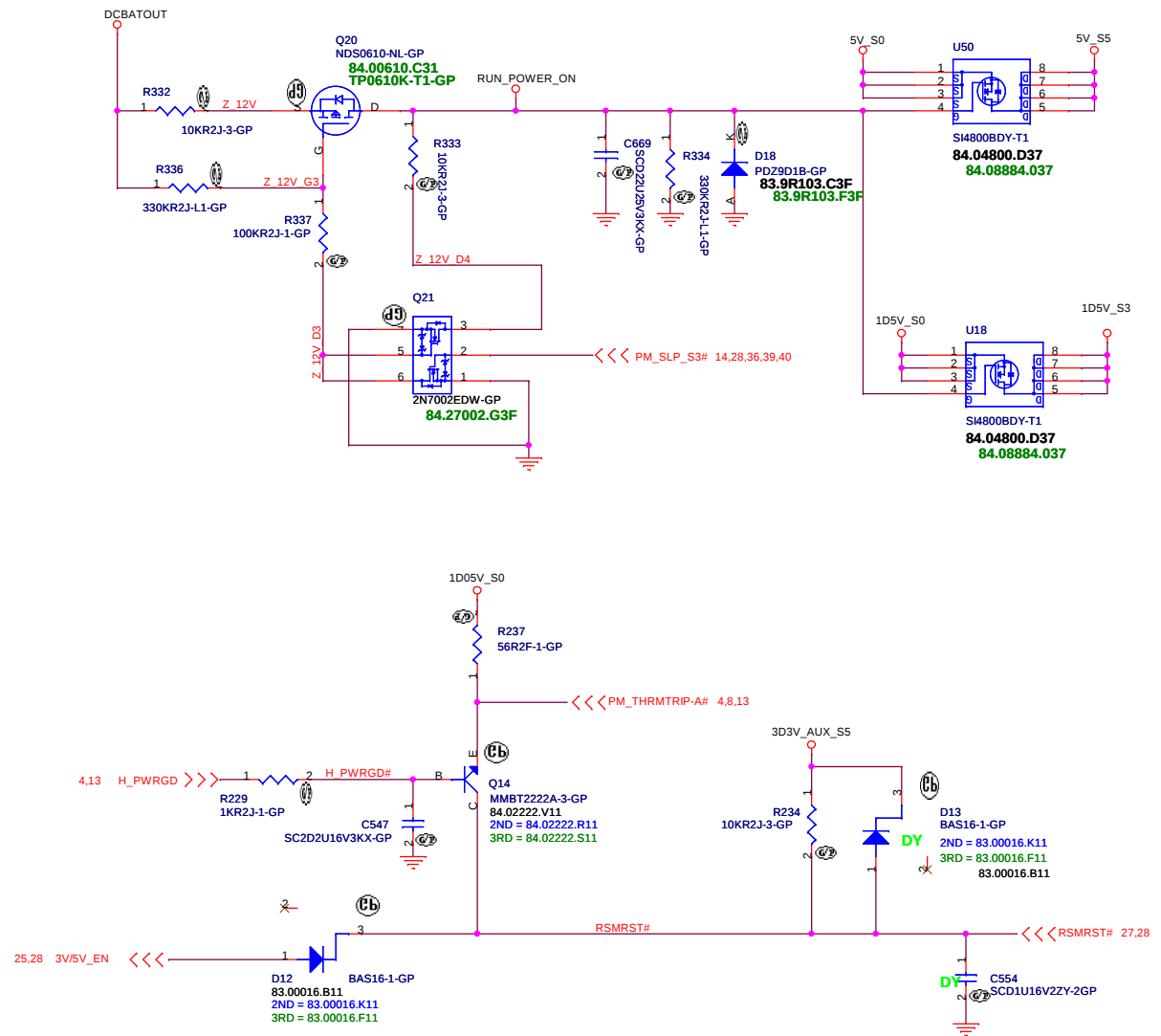


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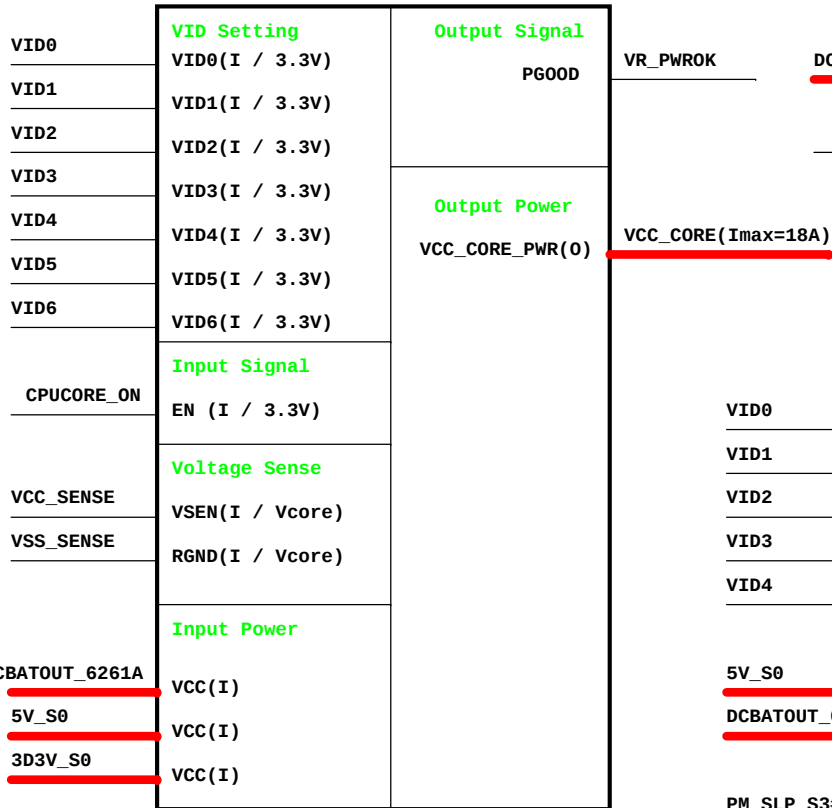
|           |                        |  |       |          |
|-----------|------------------------|--|-------|----------|
| Title     |                        |  |       |          |
| Touch PAD |                        |  |       |          |
| Size      | Document Number        |  |       | Rev      |
|           | JM41 Discrete          |  |       | SB       |
| Date:     | Monday, March 02, 2009 |  | Sheet | 30 of 48 |



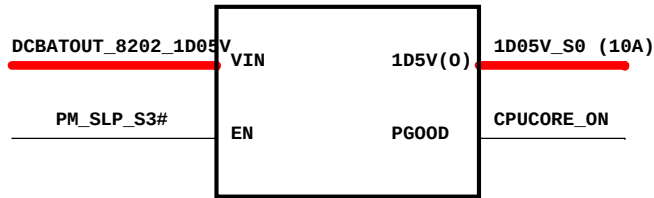
## Run Power



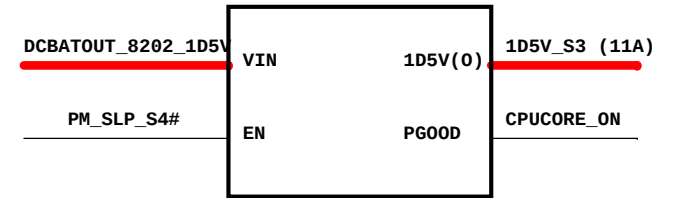
CPU\_CORE  
ISL6261A



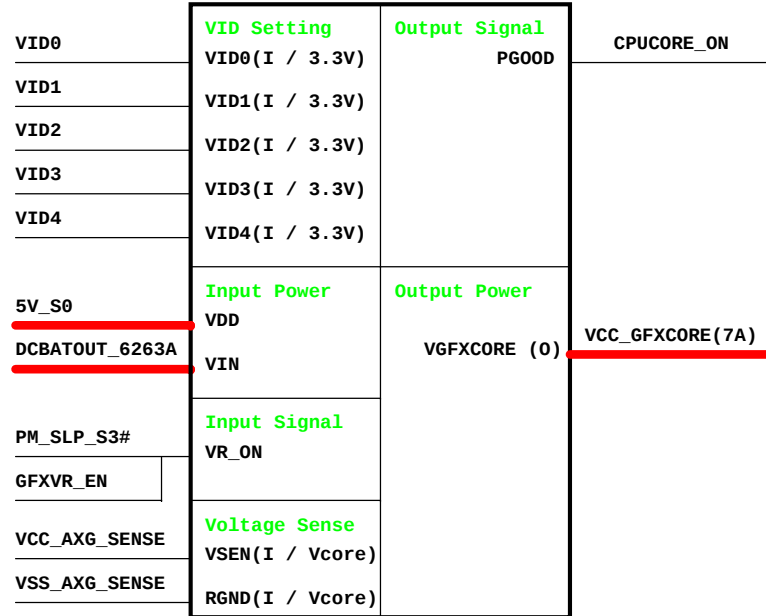
RT8202 1D05V\_S0



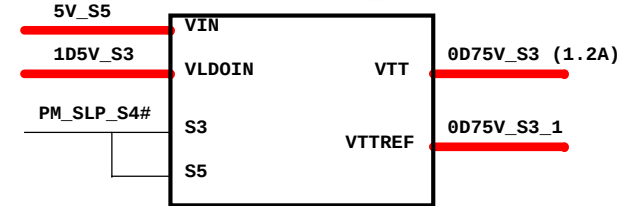
RT8202 1D5V\_S3



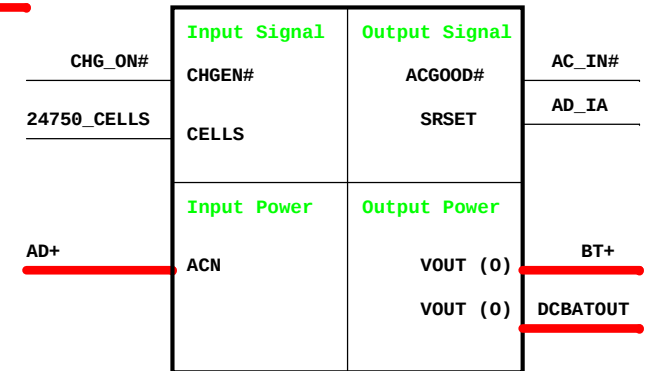
GFX\_CORE  
ISL6263A



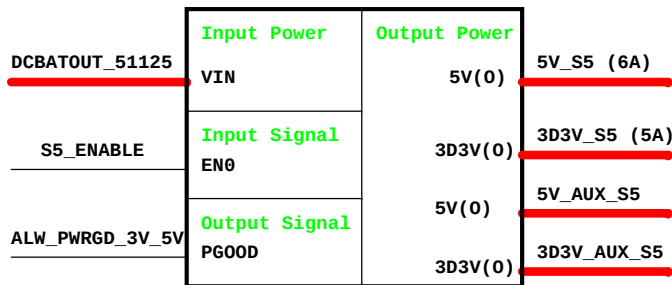
RT9026 0D9V\_S0



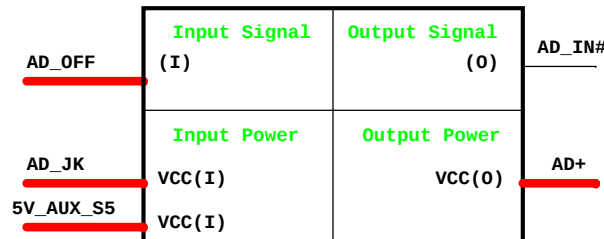
Charger MAX8731A



TPS51125  
5V/3D3V



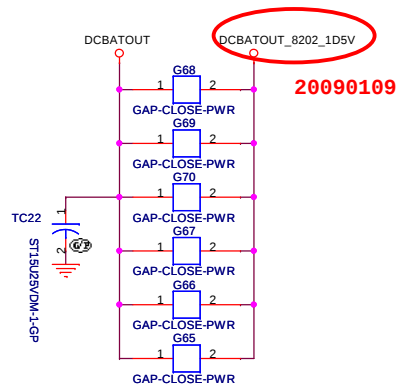
Adapter



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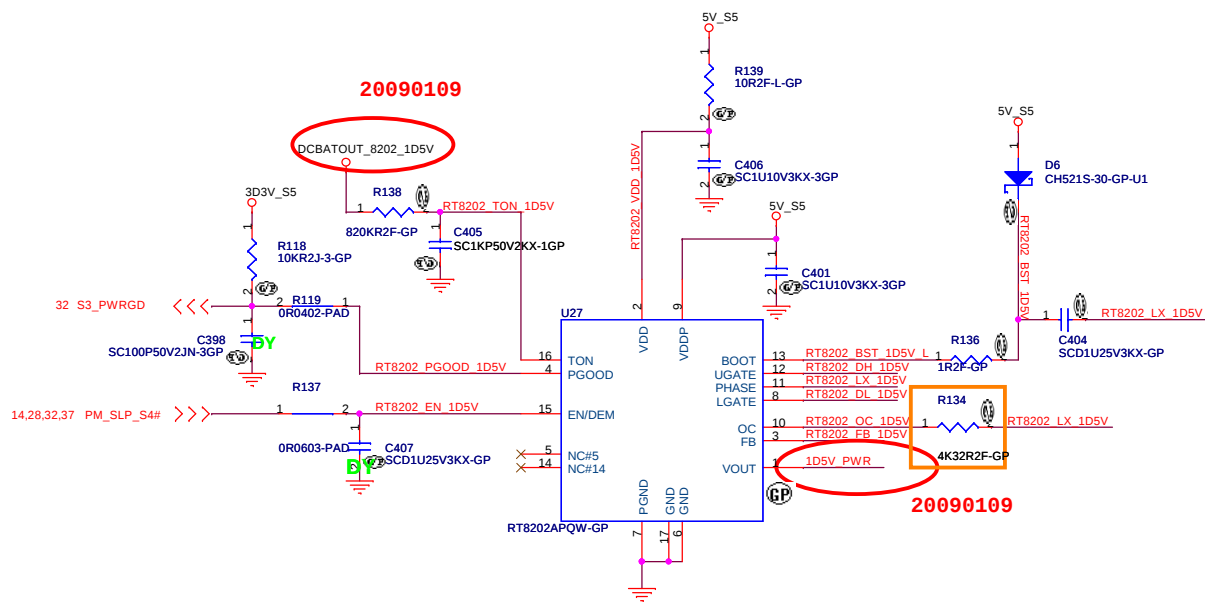
|                              |                 |     |
|------------------------------|-----------------|-----|
| Title                        |                 |     |
| Power Sequence Logic         |                 |     |
| Size B                       | Document Number | Rev |
|                              | JM41 Discrete   | SB  |
| Date: Monday, March 02, 2009 | Sheet 33 of 48  |     |



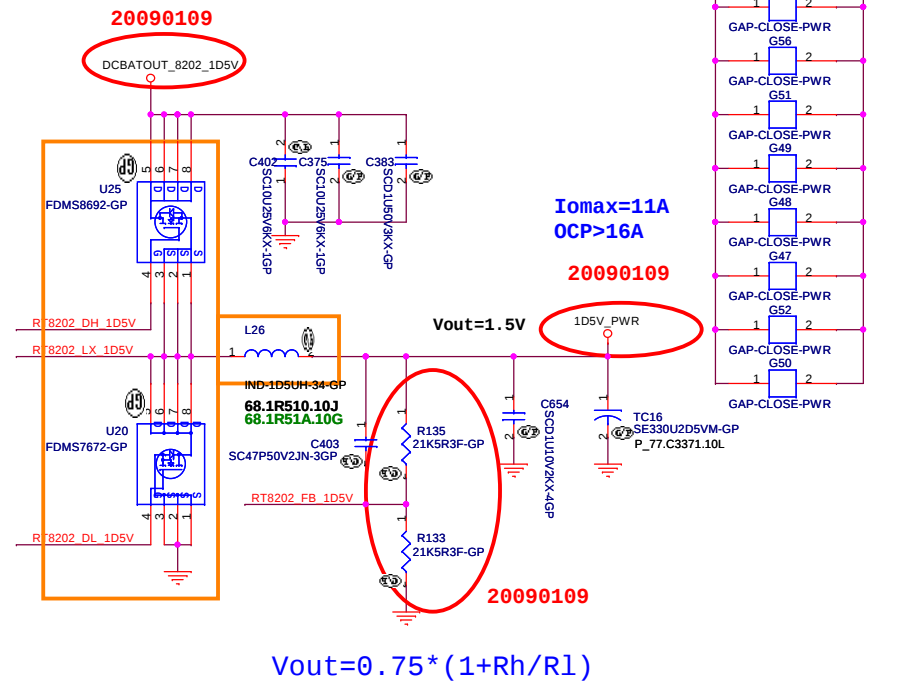


20090109

20090109



20090109



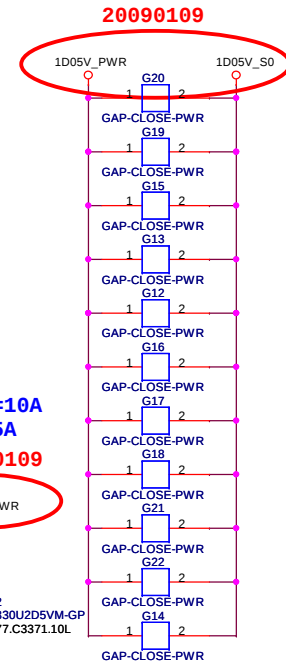
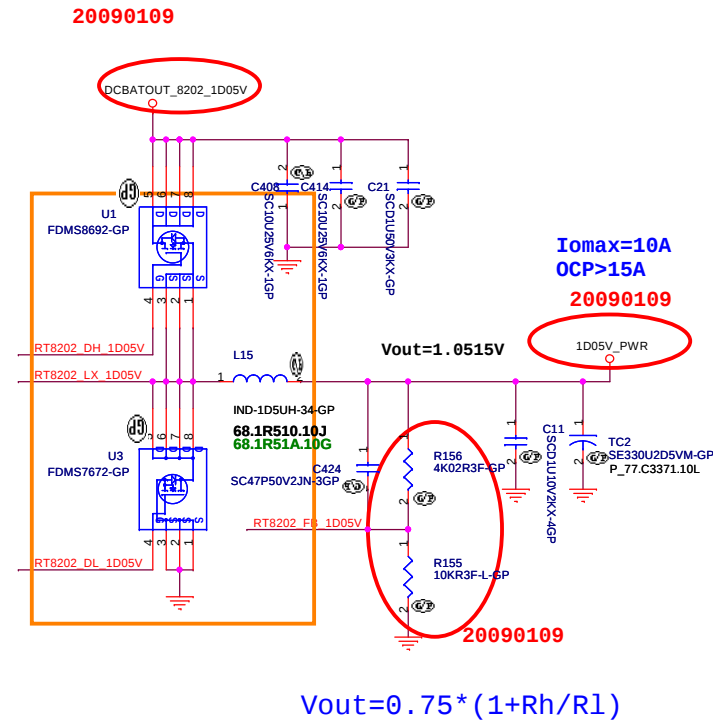
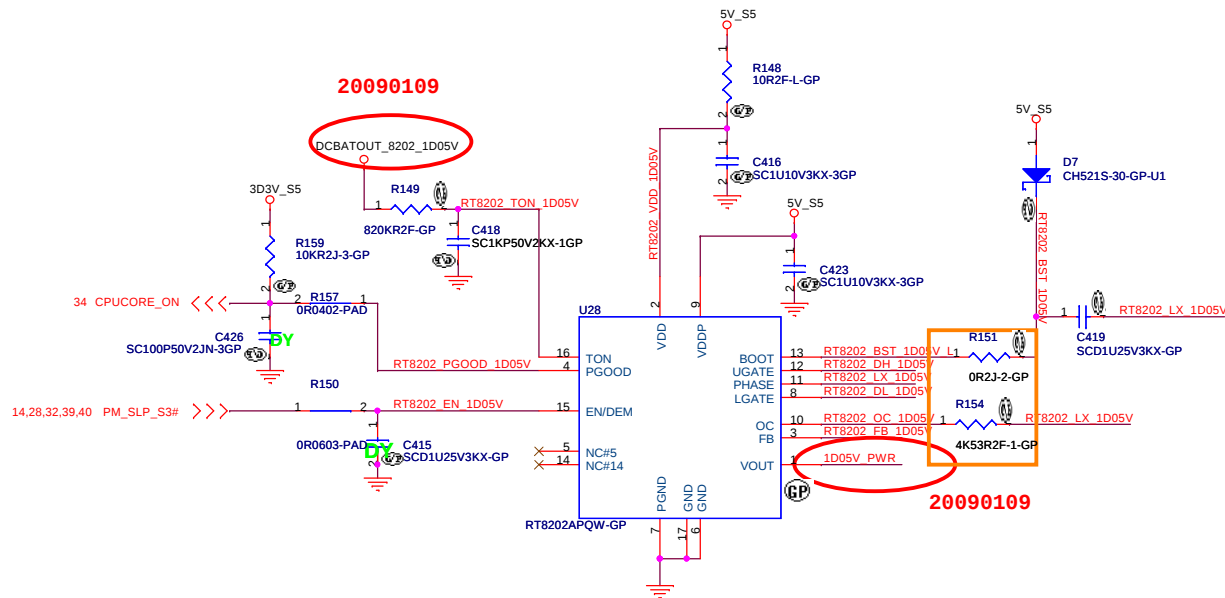
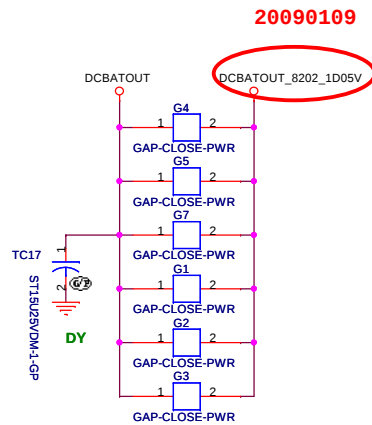
$I_{omax}=11A$   
 $OCP>16A$

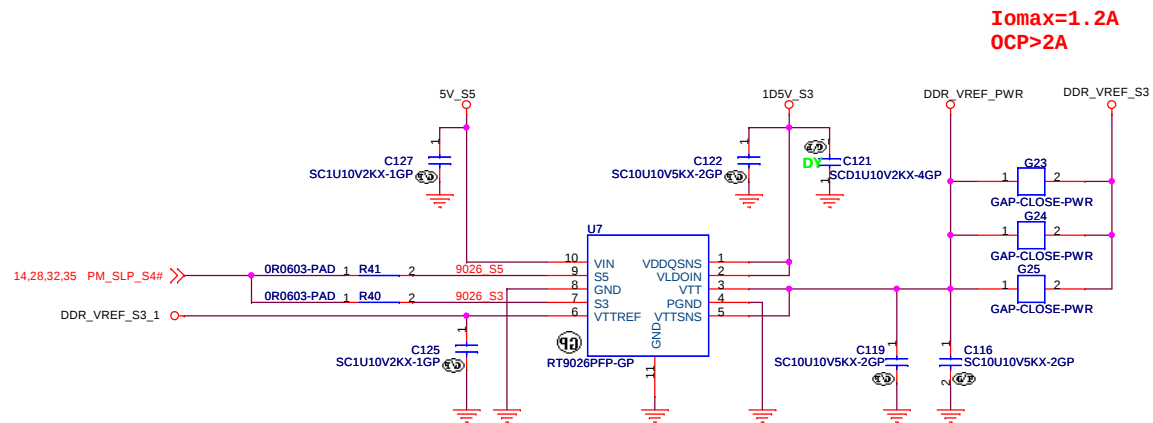
20090109

$$V_{out}=0.75*(1+R_h/R_l)$$

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|       |                          |               |             |       |
|-------|--------------------------|---------------|-------------|-------|
| Title |                          |               | RT8202 1D5V |       |
| Size  | Document Number          | JM41 Discrete |             | Rev   |
| A3    |                          |               |             | SB    |
| Date: | Thursday, March 05, 2009 | Sheet         | 35          | of 48 |

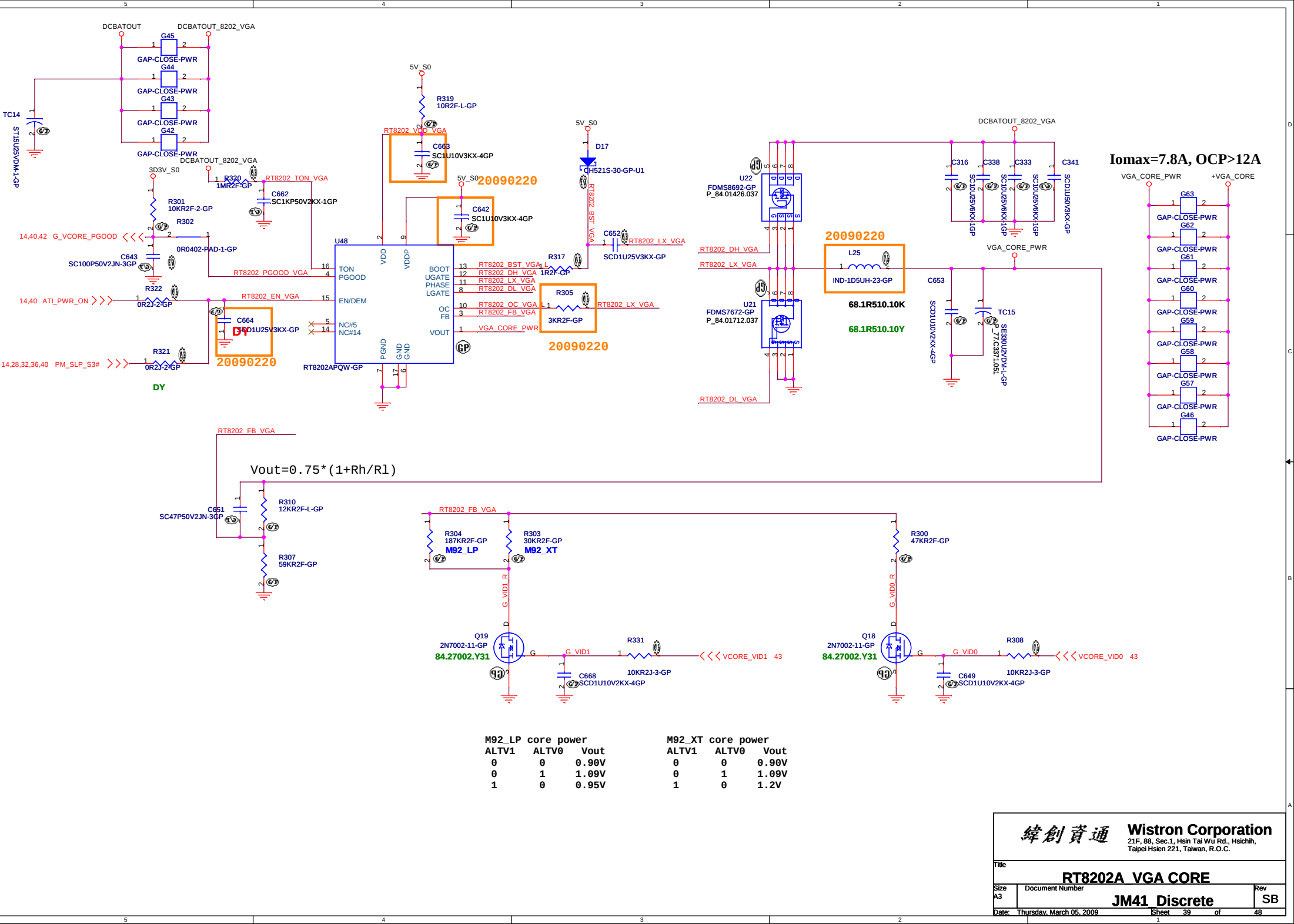




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|       |                        |               |              |       |
|-------|------------------------|---------------|--------------|-------|
| Title |                        |               | RT9026 0D75V |       |
| Size  | Document Number        | JM41 Discrete |              | Rev   |
| A3    |                        |               |              | SB    |
| Date: | Monday, March 02, 2009 | Sheet         | 37           | of 48 |



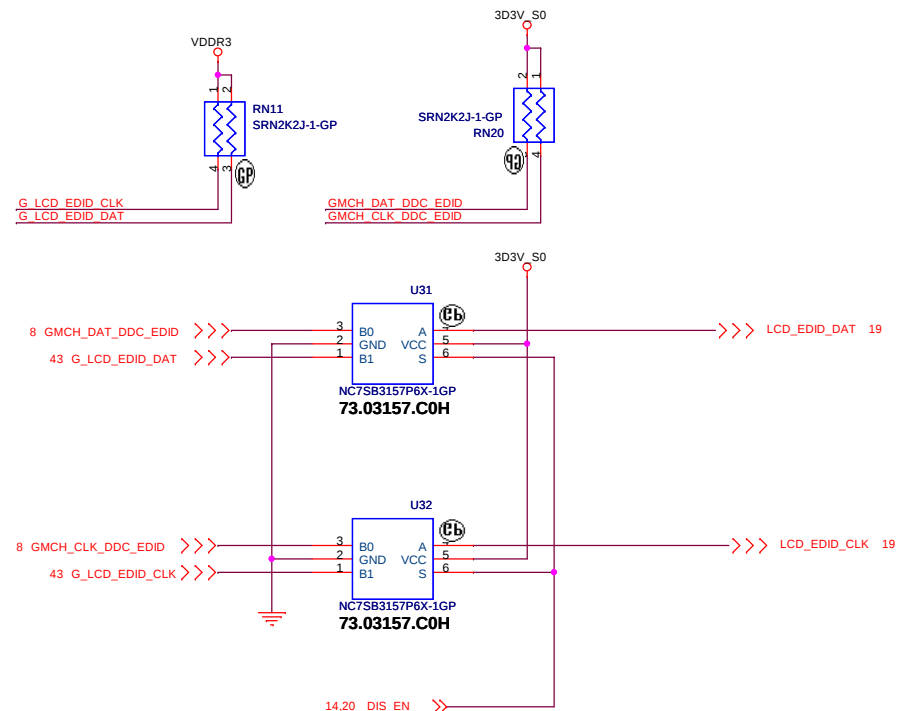


$$V_{out} = 0.75 * (1 + R_h / R_l)$$

| M92_LP core power |       |       |
|-------------------|-------|-------|
| ALTV1             | ALTV0 | Vout  |
| 0                 | 0     | 0.90V |
| 0                 | 1     | 1.09V |
| 1                 | 0     | 0.95V |

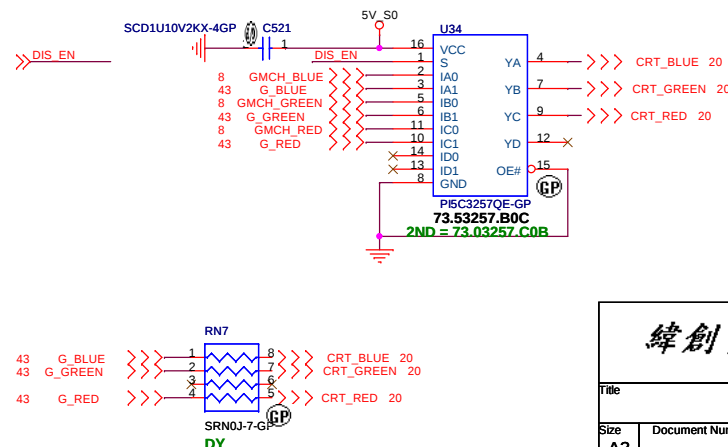
| M92_XT core power |       |       |
|-------------------|-------|-------|
| ALTV1             | ALTV0 | Vout  |
| 0                 | 0     | 0.90V |
| 0                 | 1     | 1.09V |
| 1                 | 0     | 1.2V  |



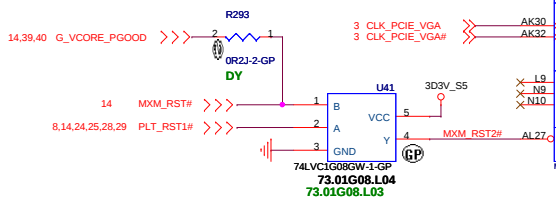
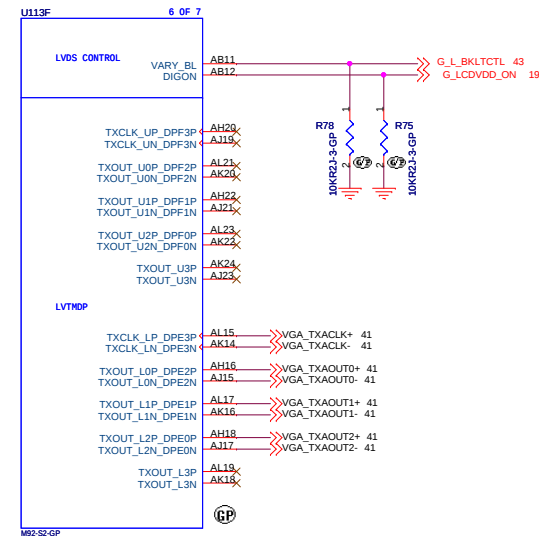
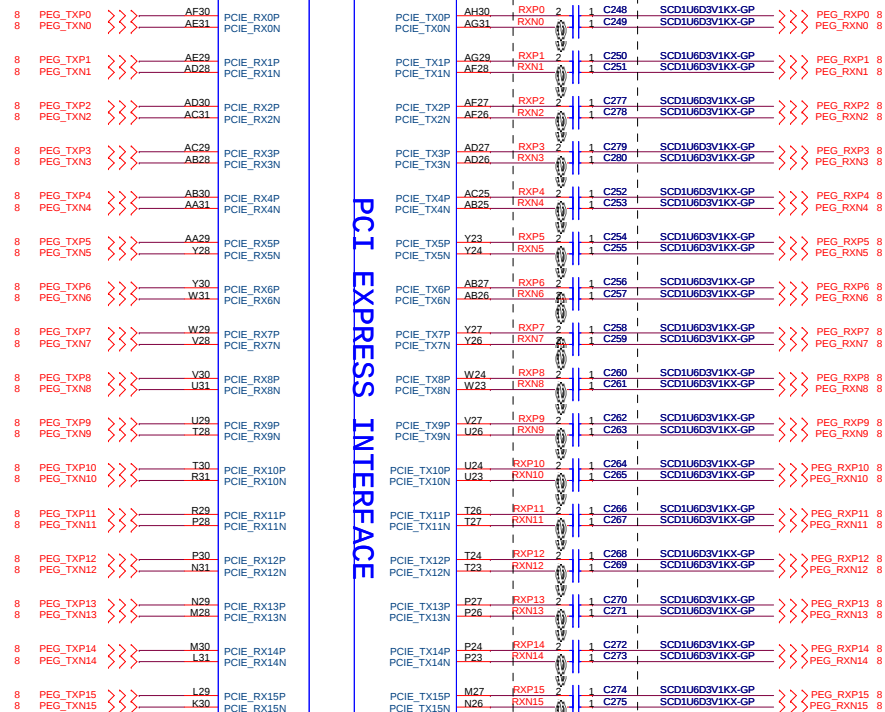


| $\bar{E}$ | S | YA   | YB   | YC   | YD   | Function |
|-----------|---|------|------|------|------|----------|
| H         | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Disable  |
| L         | L | IA0  | IB0  | IC0  | ID0  | S = 0    |
| L         | H | IA1  | IB1  | IC1  | ID1  | S = 1    |

| SEL | FUNCTION                                                                                                                                                                                                 | OUTPUT                                   |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|
| L   | TMDSn+ = ATMDSn+<br>TMDSn- = ATMDSn-<br>TMDSCLK+ = ATMDSCLK+<br>TMDSCLK- = ATMDSCLK-<br>BTMDSn+ = High Impedance<br>BTMDSn- = High Impedance<br>BTMDSCLK+ = High Impedance<br>BTMDSCLK- = High Impedance | TMDSn+<br>TMDSn-<br>TMDSCLK+<br>TMDSCLK- |
| H   | TMDSn+ = BTMDSn+<br>TMDSn- = BTMDSn-<br>TMDSCLK+ = BTMDSCLK+<br>TMDSCLK- = BTMDSCLK-<br>ATMDSn+ = High Impedance<br>ATMDSn- = High Impedance<br>ATMDSCLK+ = High Impedance<br>ATMDSCLK- = High Impedance | TMDSn+<br>TMDSn-<br>TMDSCLK+<br>TMDSCLK- |



SSID = VIDEO

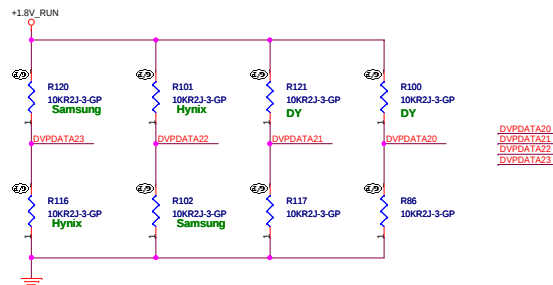


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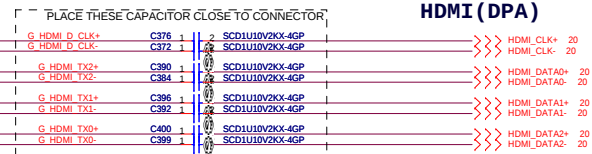
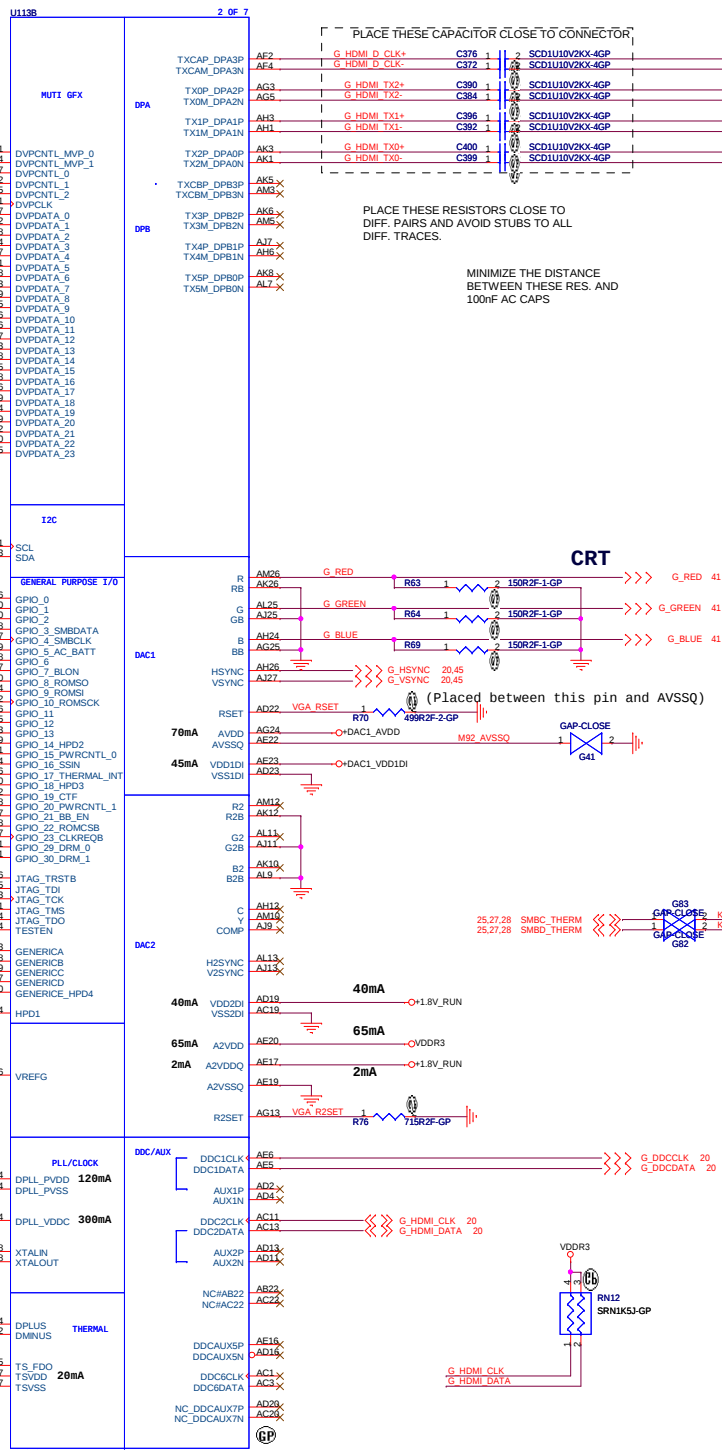
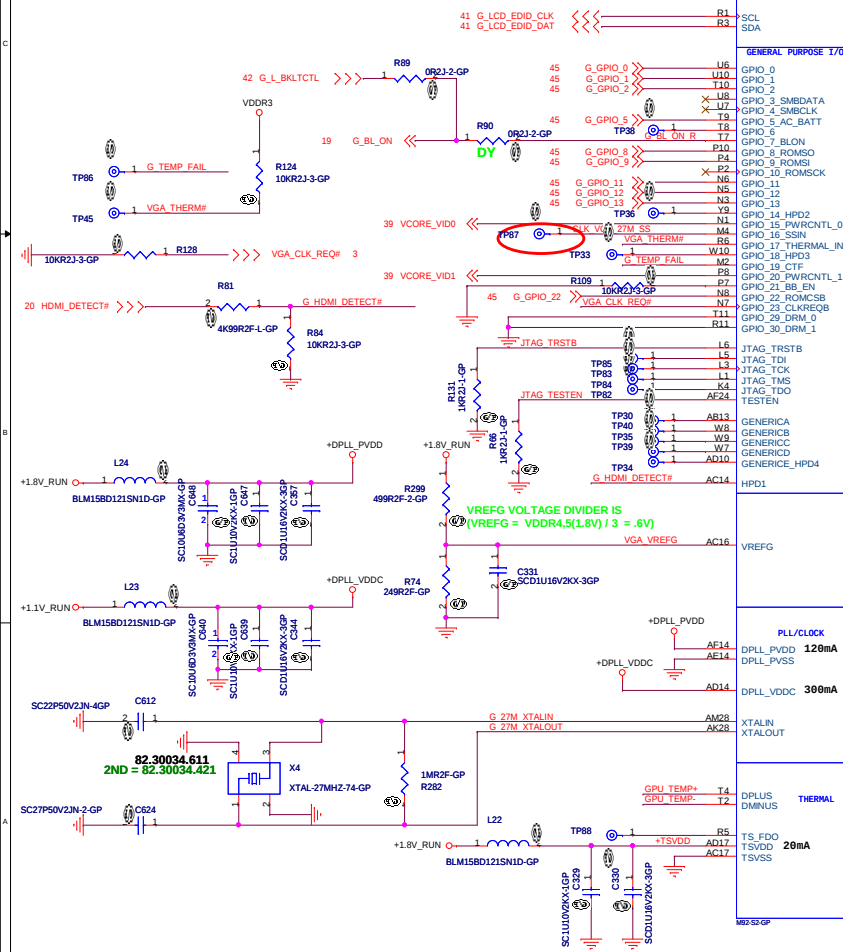
|        |                        |       |                    |
|--------|------------------------|-------|--------------------|
| Title  |                        |       | VGA-PCIE/LVDS(1/4) |
| Size   | Document Number        | Rev   | SB                 |
| Custom | JM41 Discrete          |       |                    |
| Date:  | Monday, March 02, 2009 | Sheet | 42 of 48           |

**SSID = VIDEO**

```
DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung
```

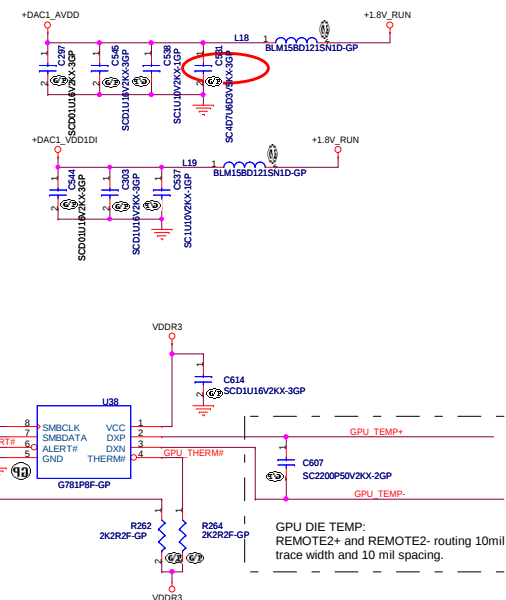
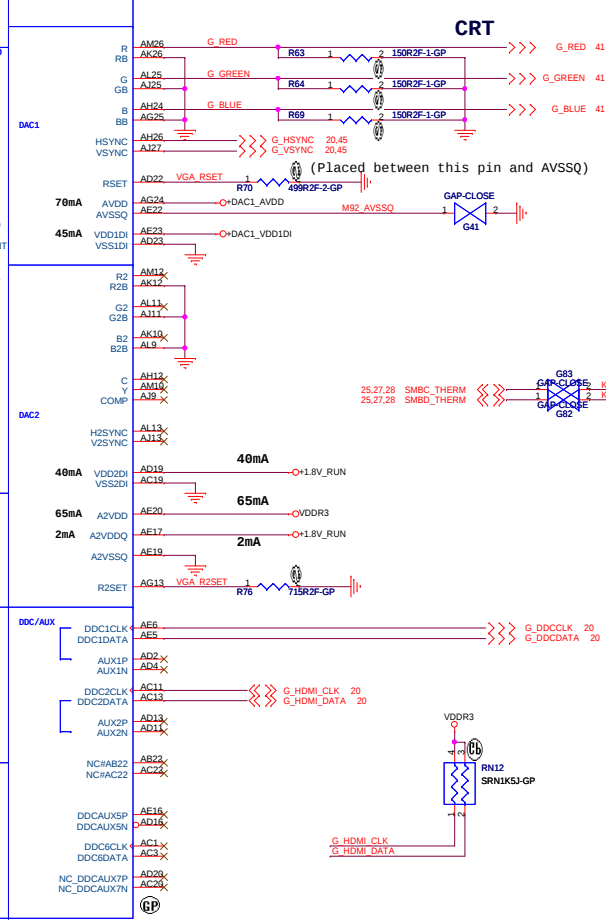


| STRAPS   | PIN                             | DESCRIPTION                                                                                                                                               |
|----------|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| MEM_TYPE | DVPDATA(23:20)<br>(Internal PD) | MEMORY TYPE, MAKE AND SIZE INFO<br>0000 - GDDR3 16Mx32 Qimonda<br>0001 - GDDR3 32Mx32 Hynix<br>0010 - GDDR3 32Mx32 Qimonda<br>0011 - GDDR3 32Mx32 Samsung |

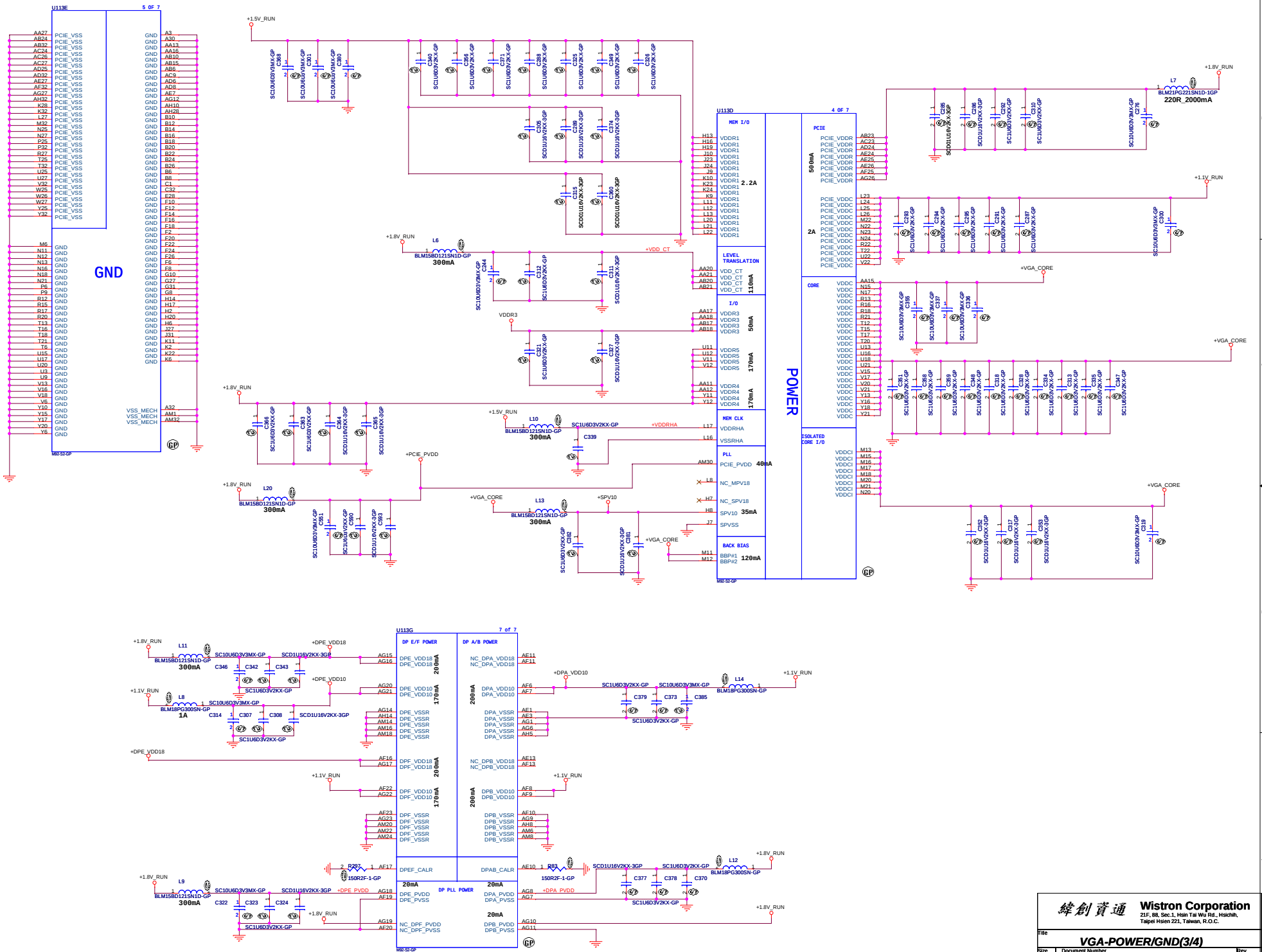


PLACE THESE RESISTORS CLOSE TO  
DIFF. PAIRS AND AVOID STUBS TO ALL  
DIFF. TRACES.

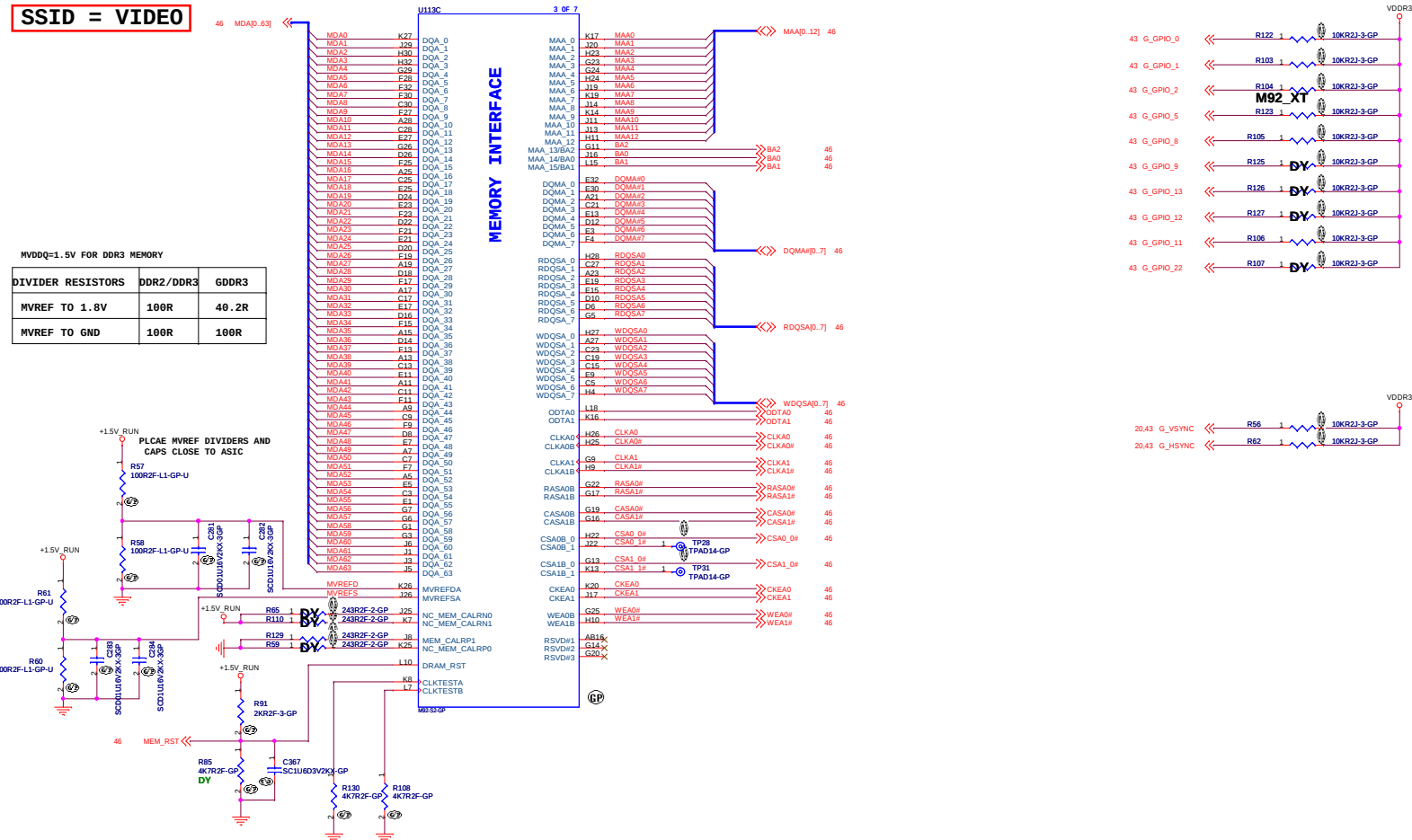
MINIMIZE THE DISTANCE  
BETWEEN THESE RES. AND  
100nF AC CAPS



SSID = VIDEO



**SSID = VIDEO**



FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED  
THEY MUST NOT CONFLICT DURING RESE

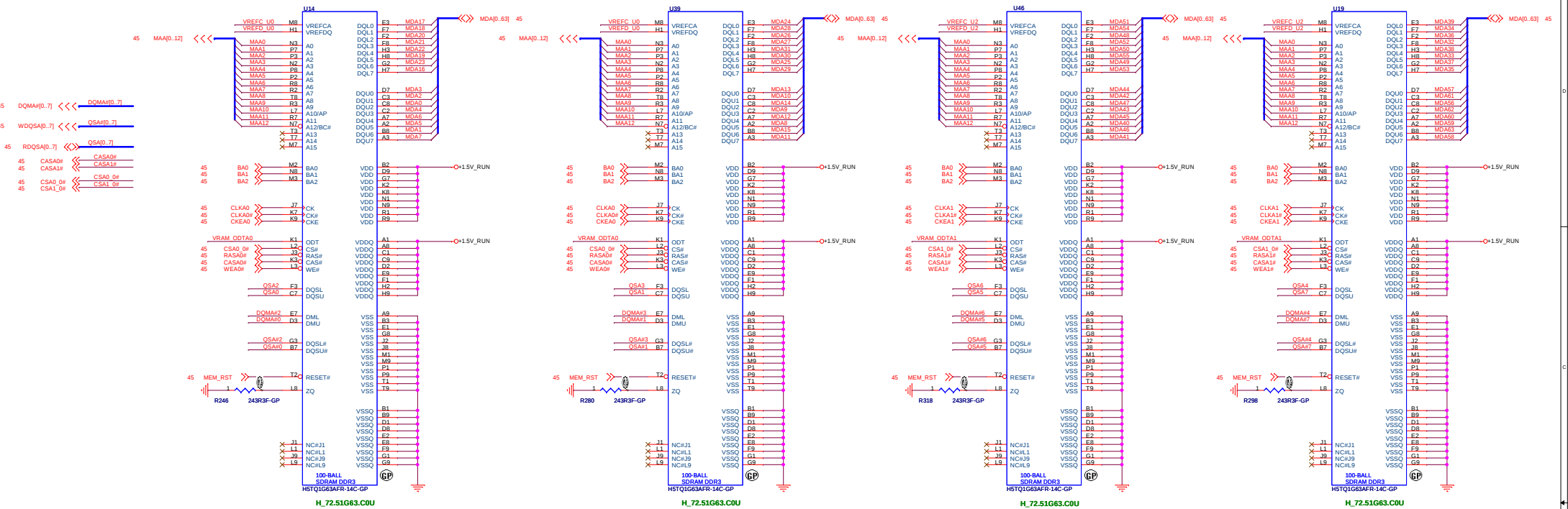
GPI03 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED,  
THEY MUST NOT CONFLICT DURING RESET

| If BIOS_ROM_EN (GPIO22) = 0          |                  | If BIOS_ROM_EN (GPIO22) = 1 |                           |                |      |
|--------------------------------------|------------------|-----------------------------|---------------------------|----------------|------|
| Size of the primary memory apertures | GPIO[9,13,12,11] | Manufacturer                | Part Number               | GPIO[13,12,11] |      |
| V                                    | 128MB            | x000                        | ST<br>Microelectronics    | M25P05A        | 0100 |
|                                      | 256MB            | x001                        |                           | M25P10A        | 0101 |
|                                      | 64MB             | x010                        |                           | M25P20         | 0101 |
|                                      | 32MB             | x                           |                           | M25P40         | 0101 |
|                                      | 512MB            | x                           |                           | M25P80         | 0101 |
|                                      | 1GB              | x                           | Chingis<br>(formerly PMC) | Pm25LV512A     | 0100 |
|                                      | 2GB              | x                           |                           | Pm25LV810A     | 0101 |
| 4GB                                  | x                |                             |                           |                |      |

| STRAPS                            | PIN                    | DESCRIPTION                                                                                                                                                                    |
|-----------------------------------|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TX_PWRS_ENB<br>(Internal PD)      | GPI08                  | Transmitter Power Savings Enable<br>0= 50% Tx output swing<br>1= Full Tx output swing<br>✓                                                                                     |
| TX_DEEMPH_EN<br>(Internal PD)     | GPI01                  | Transmitter De-emphasis Enable<br>0= Tx de-emphasis disabled<br>1= Tx de-emphasis enabled<br>✓                                                                                 |
| BIF_GEN2_EN_A                     | GPI02                  | ✓ 0 = Advertises the PCI-E device as 2.5GT/s<br>1 = Advertises the PCI-E device as 5GT/s                                                                                       |
| BIF_CLK_PM_EN                     | GPI08                  | 0= Disable CLKREQ#power management capability<br>1= Enable CLKREQ# power management capability<br>✓                                                                            |
| ROMIDCFG[3:0]<br>(Internal PD)    | GPI0[13,12,11]         | if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type<br>if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size                                         |
| BIOS_ROM_EN<br>(Internal PD)      | GPI0_22_ROMCSB         | ✓ Enable external BIOS ROM device<br>0= Disable external BIOS ROM device<br>1= Enable external BIOS ROM device                                                                 |
| AUD[1]<br>AUD[0]<br>(Internal PD) | VGA_HSYNC<br>VGA_VSYNC | AUD[1:0]<br>00:No audio function<br>01:Audio for DisplayPort and HDMI (if adapter is detected)<br>10:Audio for DisplayPort only<br>11:Audio for both DisplayPort and HDMI<br>✓ |

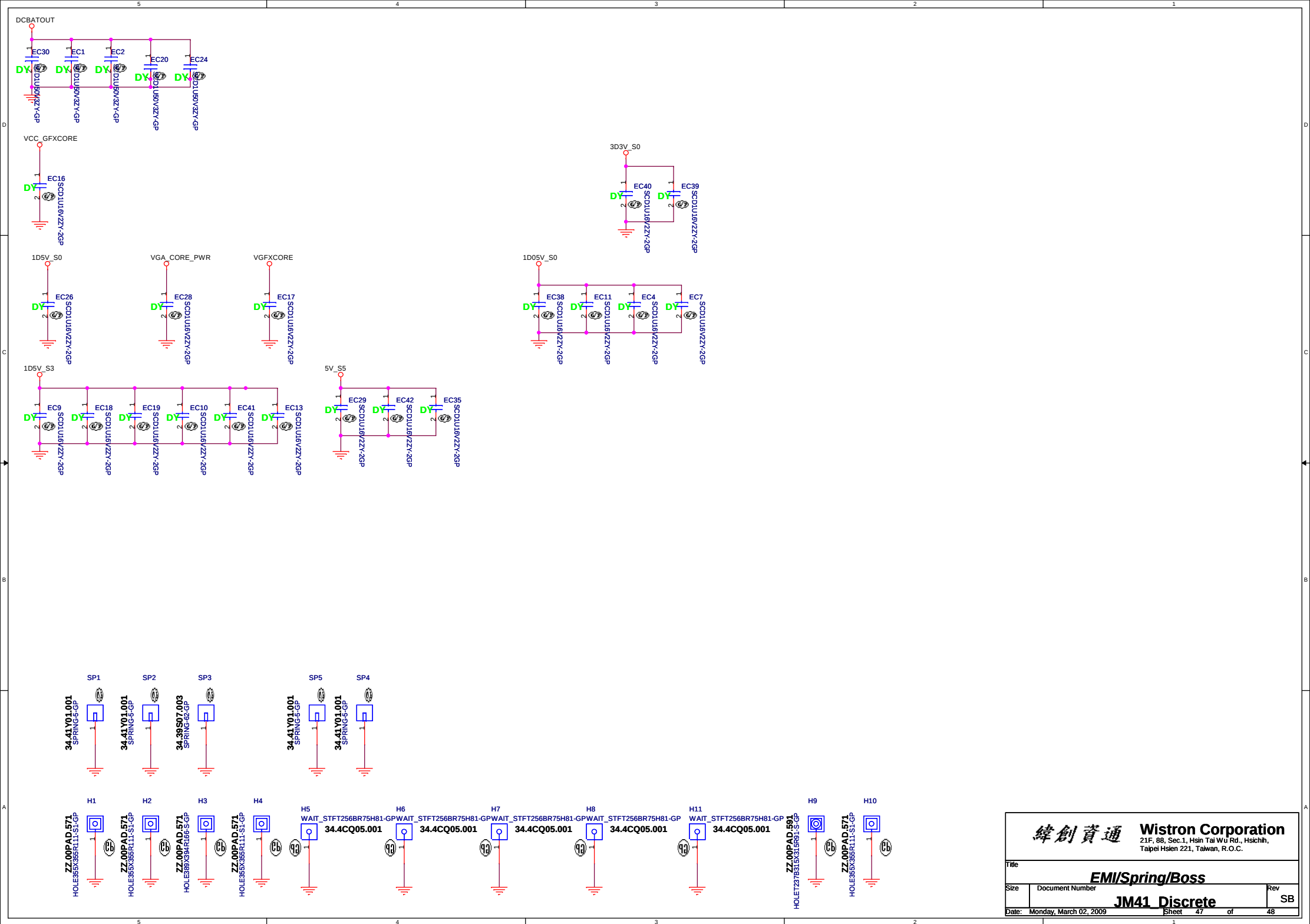
# 512MB DDR3

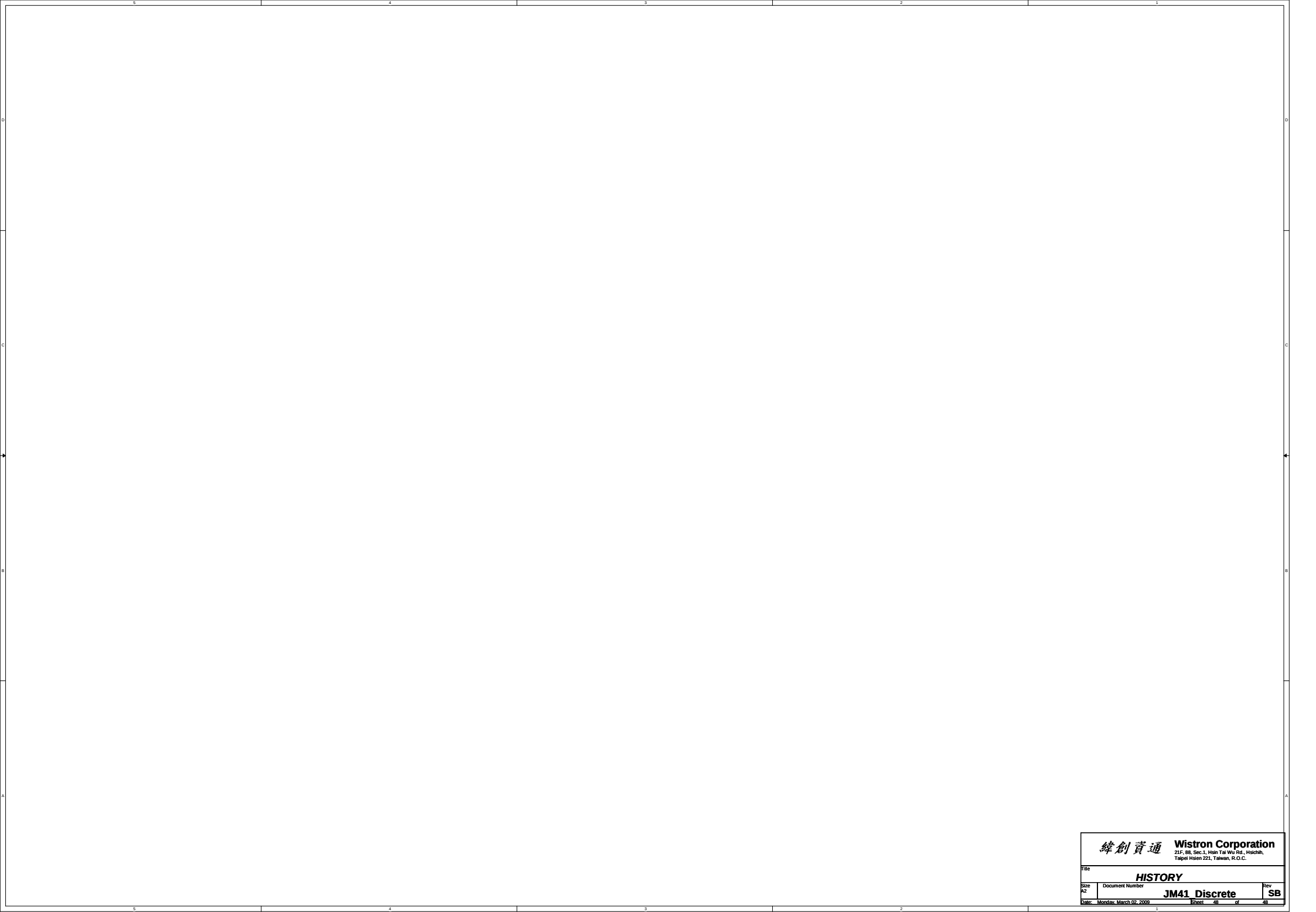


Samsung : K4W1G1646E-EC12

Hynix : H5TQ1G63BFR-12C







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Title

HISTORY

Size  
A2

Document Number  
JM41\_Discrete

Rev  
SB

Date: Monday, March 02, 2009

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