

HM40-MV Block Diagram

Project code: 91.4BW01.001
PCB P/N : 48.4BW01.0SB
REVISION : 08242-SB

CLK GEN.
ICS 9LPRS365BKLFT (71.09365.A03)
SILEGO SLG8SP513VTR (71.08513.003)
3

Mobile CPU
Penryn 479
4.5

THERMAL EMC2102
32

DDR2 DIMM1
667/800 MHz
16

DDR2 DIMM2
667/800 MHz
17

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAPHICS
LVDS, CRT I/F
6,7,8,9,10,11

CRT
19

LCD
18

Codec
CX20561
26

MIC In
28

OP AMP
G1454
27

INT. SPKR

Line Out
(NO SPDIF)
28

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
12,13,14,15

HDD SATA
20

ODD SATA
21

Blue Tooth
(USB)
22

Camera
(USB)
18

Touch
Pad
35

INT.
KB
33

CardReader
Realtek
RTS5159
30

MS/MS Pro/xD
/MMC/SD
5 in 1
30

KBC
KBC773L
33

BIOS
Winbond
W25X16
16M Bits
34

LPC
DEBUG
CONN
34

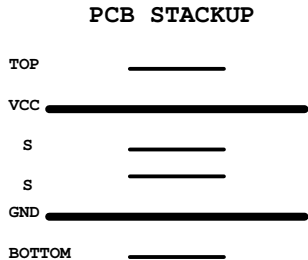
LAN
Atheros
AR8114
AR8132
24

TXFM
25

RJ45
25

Mini Card
Kedron a/b/g/n
31

Power Board
36



SYSTEM DC/DC TPS51125 42

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 44

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
RT9026	43
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A	43
1D8V_S3	1D5V_S0

CPU DC/DC ISL6266A 41

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER BQ24745 46

INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

UMA Two Phase 2

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Title BLOCK DIAGRAM

Size A3 Document Number HM40-MV Rev SB

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLFVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]: (3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]: (3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
- Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

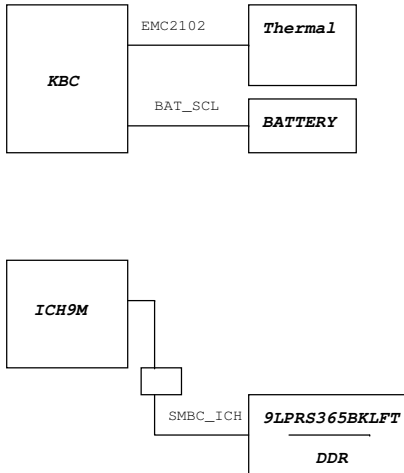
PCIE Routing

LANE1	LAN Atheros AR8114A
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NC
LANE6	NC

USB Table

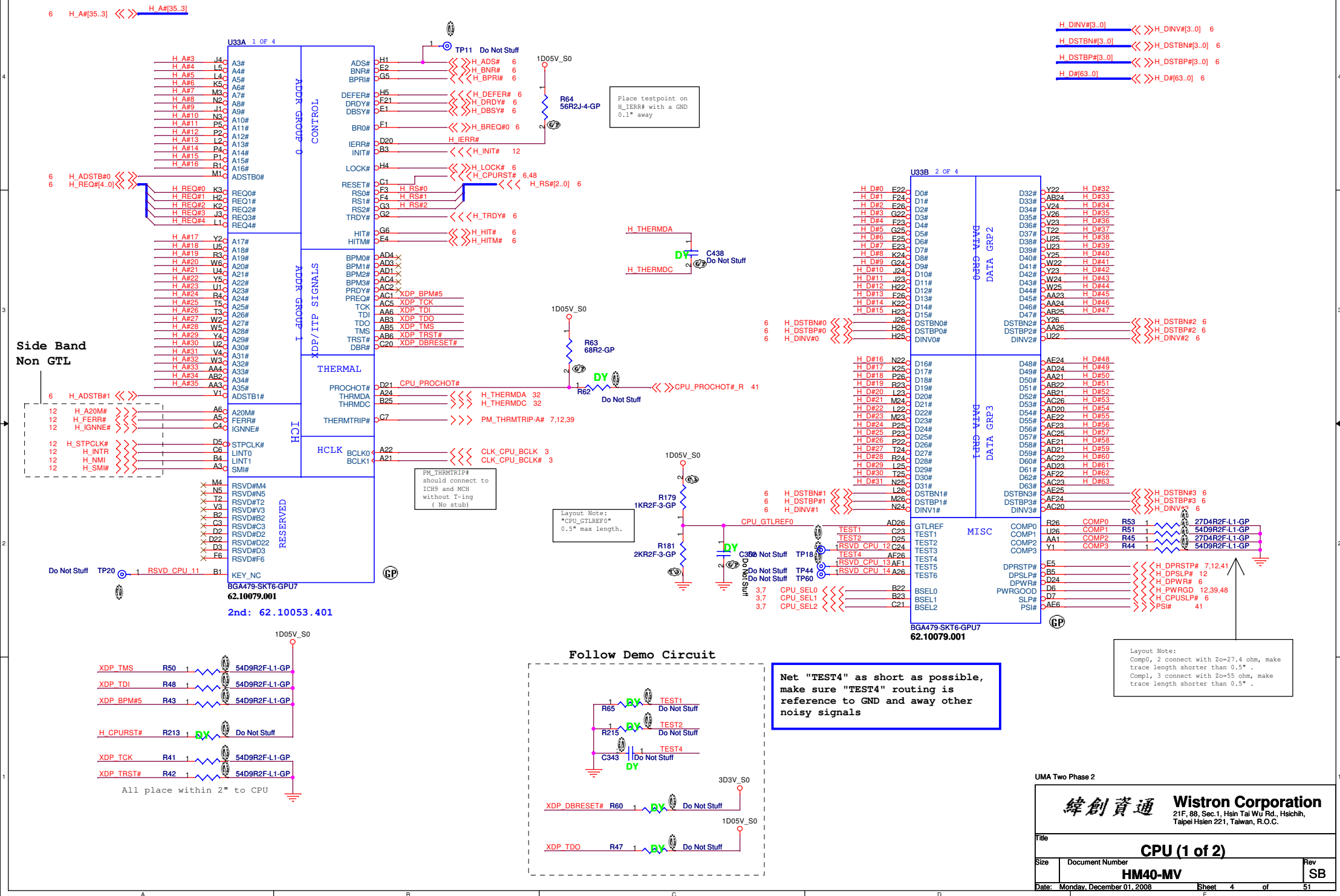
USB	
Pair	Device
0	USB1
1	NC
2	NC
3	MINIC1
4	WEBCAM
5	NC
6	NC
7	Bluetooth
8	NC
9	USB2 (High speed)
10	NC
11	CardReader

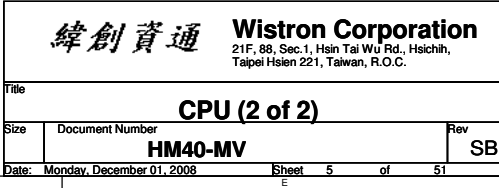
SMBus



UMA Two Phase 2

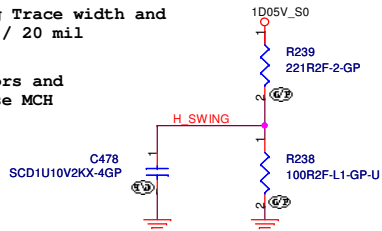
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Title			
Reference			
Size A3	Document Number	Rev	SB
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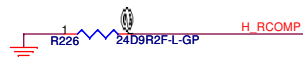


H_SWING routing Trace width and Spacing use 10 / 20 mil

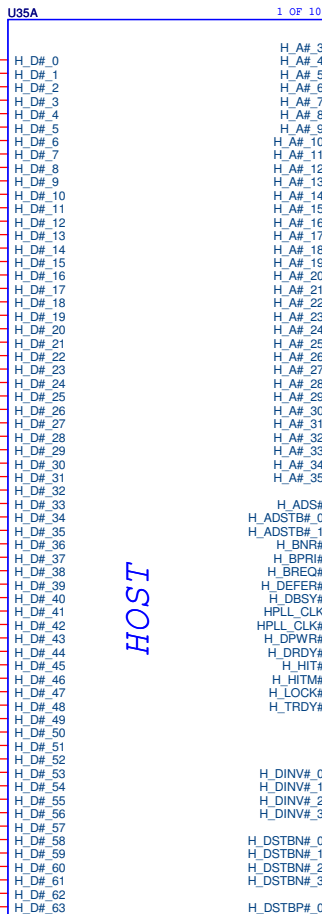
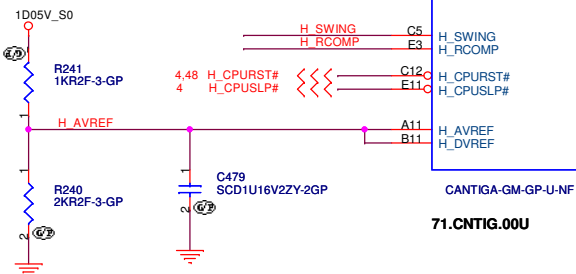
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



HOST

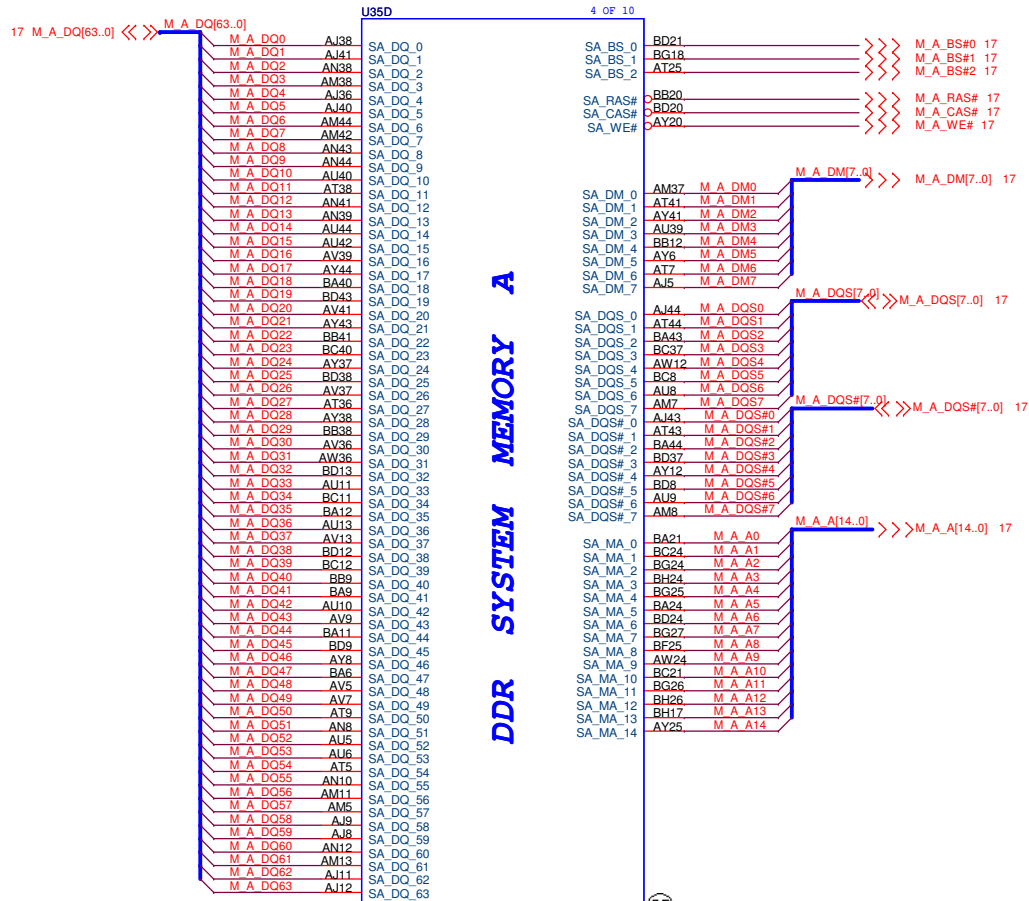
UMA Two Phase 2

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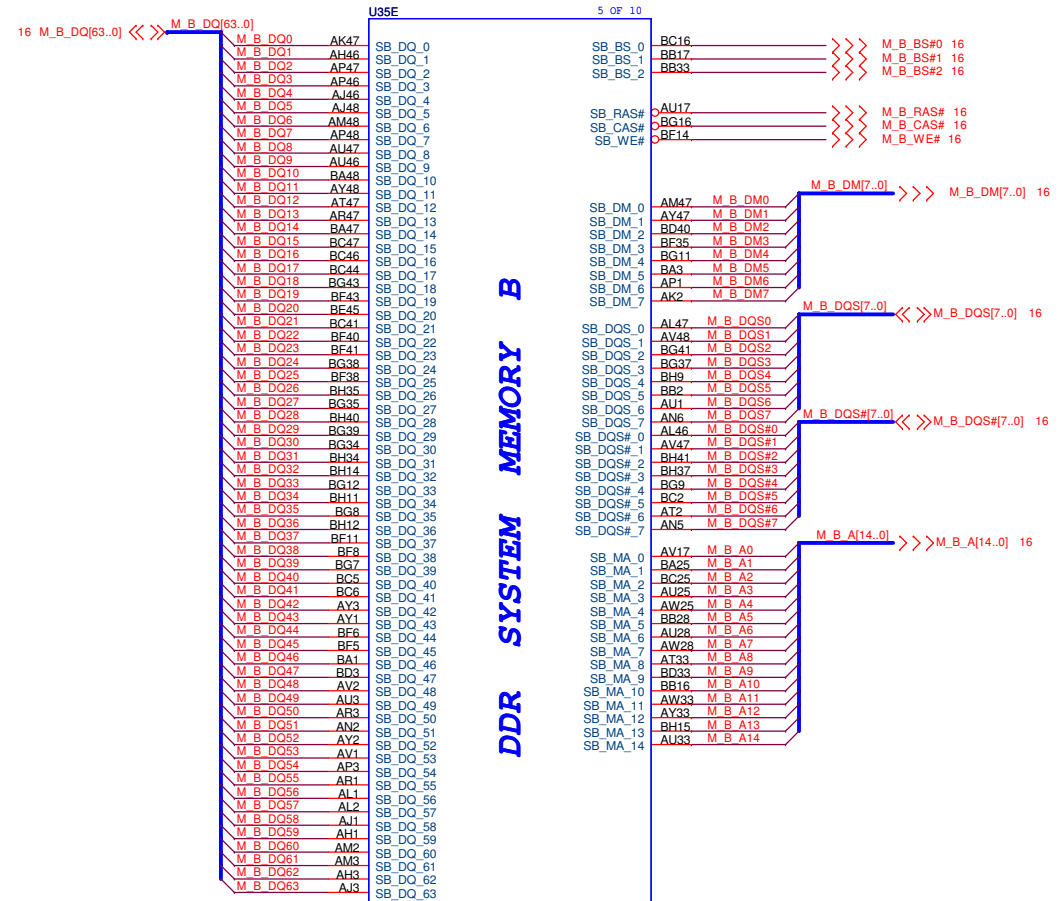
Cantiga (1 of 6)_HOST
HM40-MV

Rev
SB



CANTIGA-GM-GP-U-NF

71.CNTIG.00U



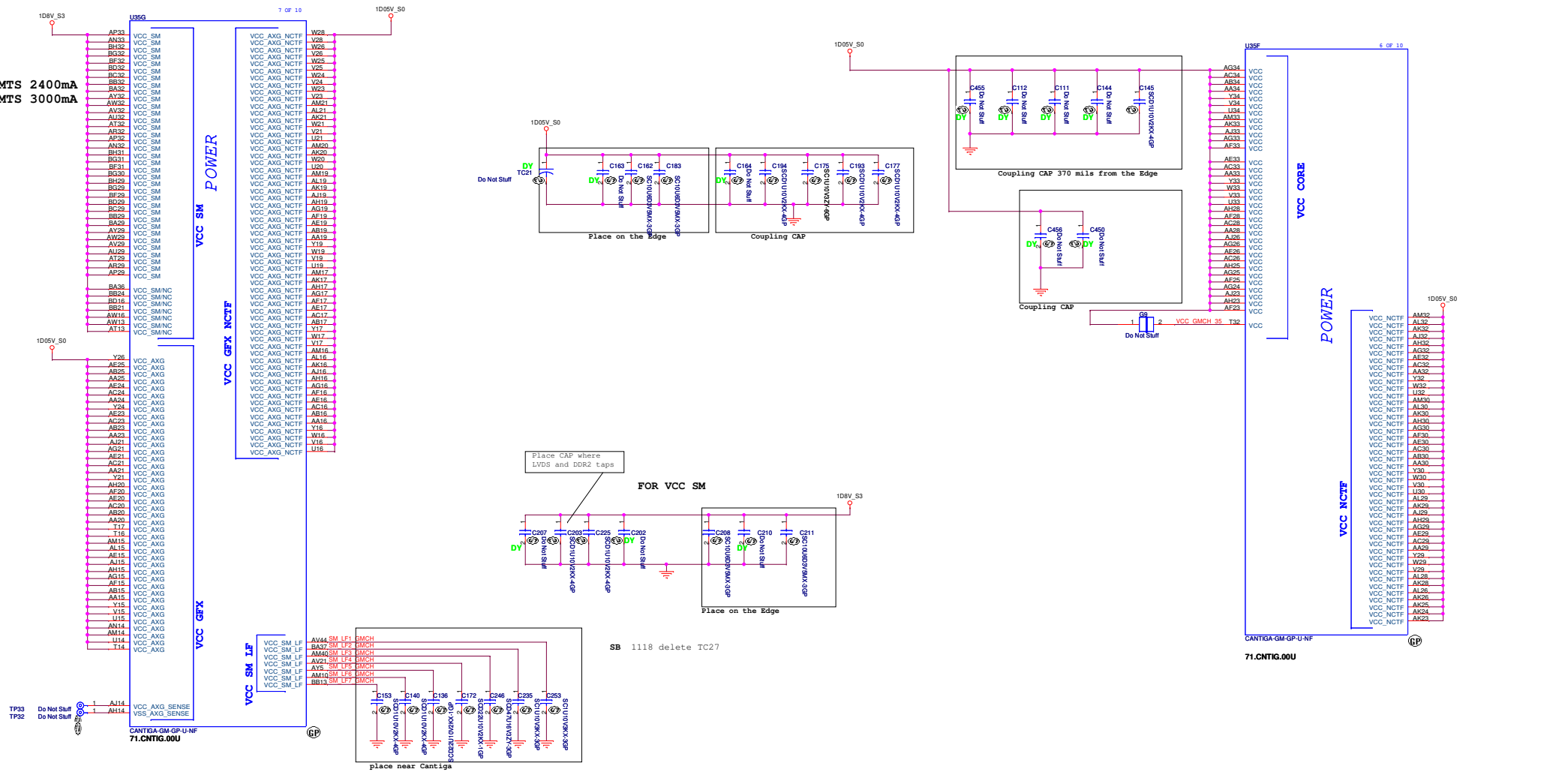
CANTIGA-GM-GP-U-NF

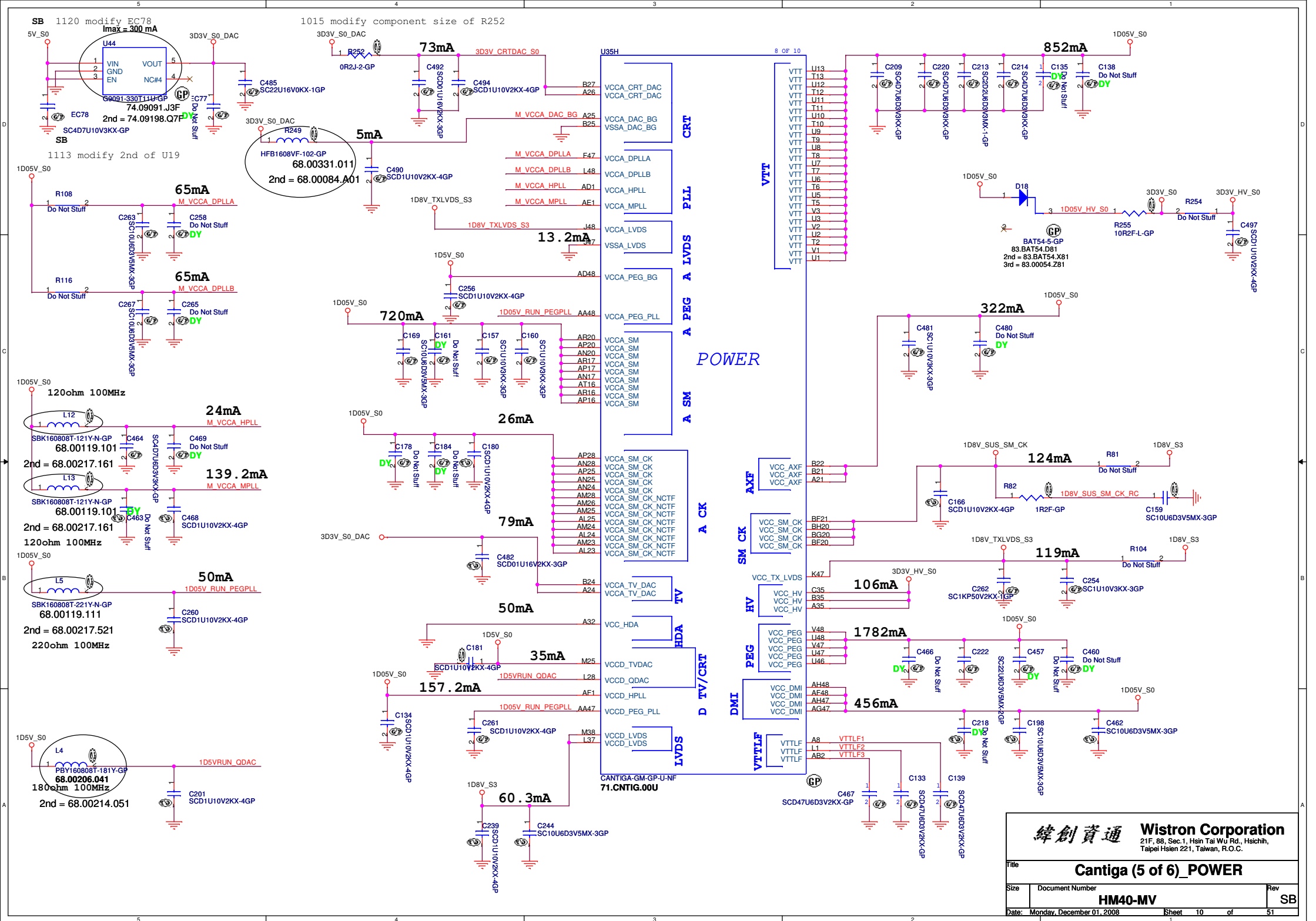
71.CNTIG.00U

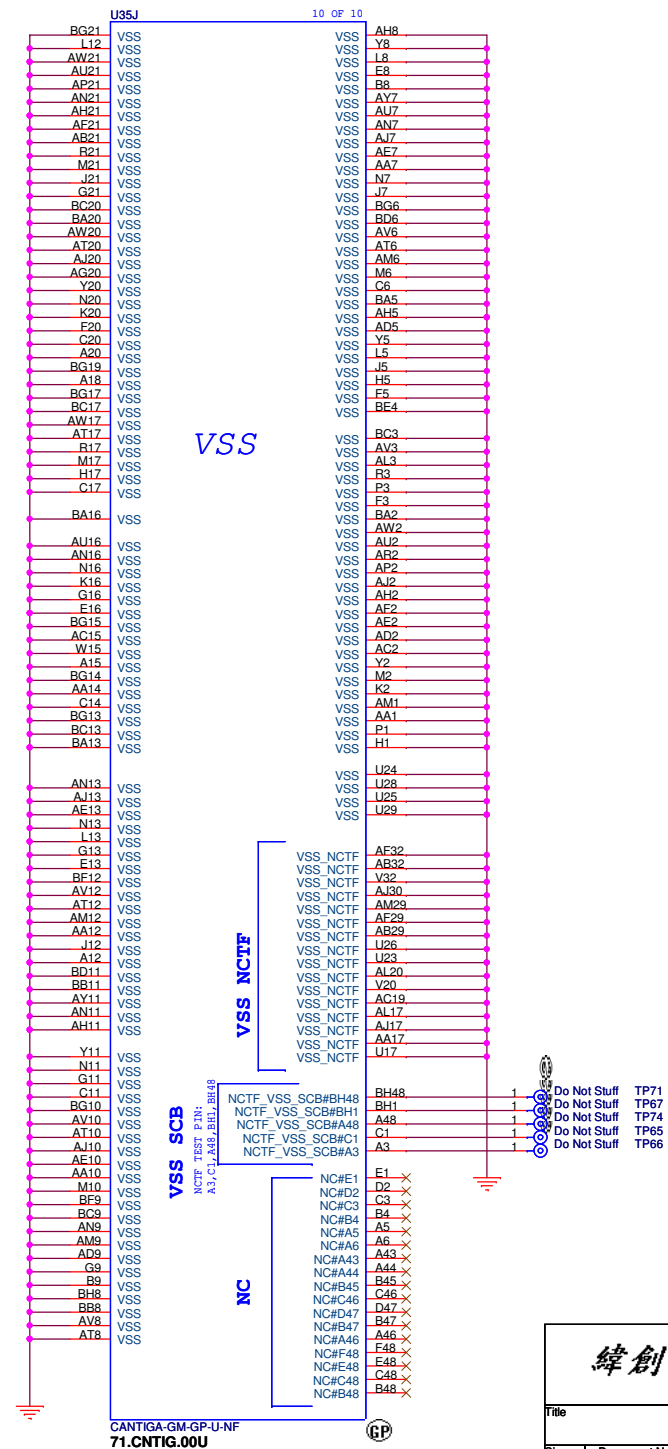
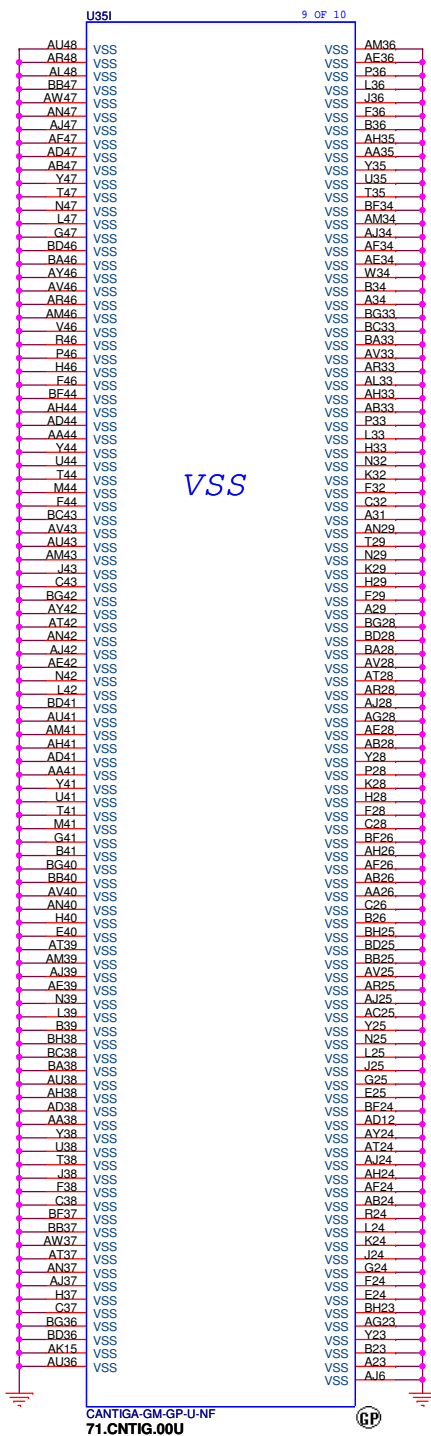
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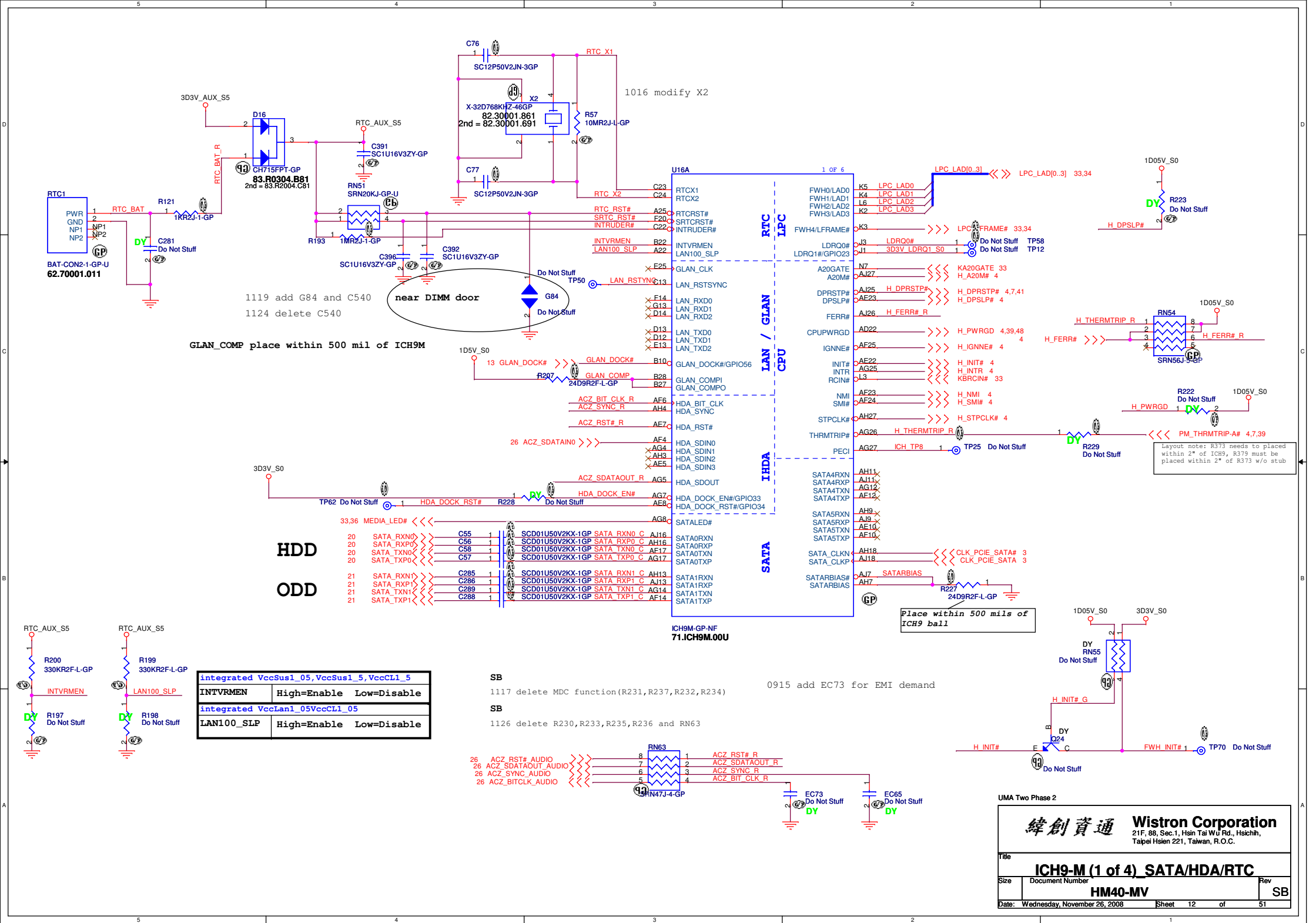
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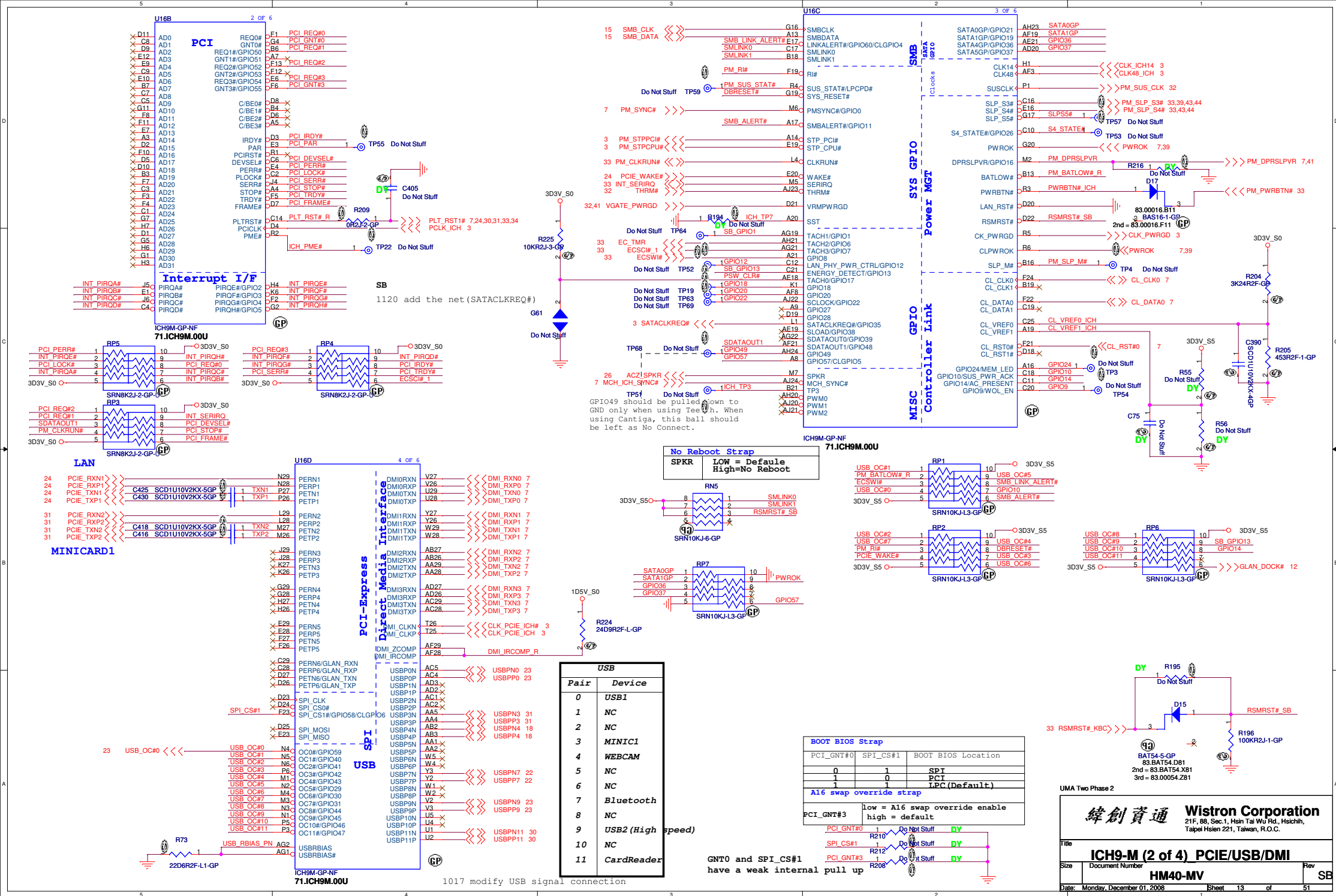
667MTS 2400mA
800MTS 3000mA

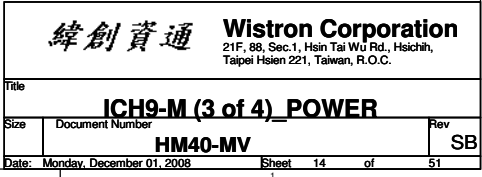


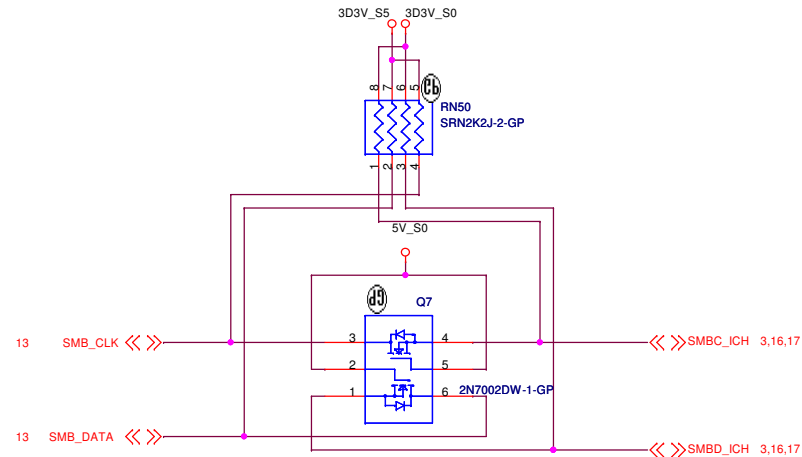
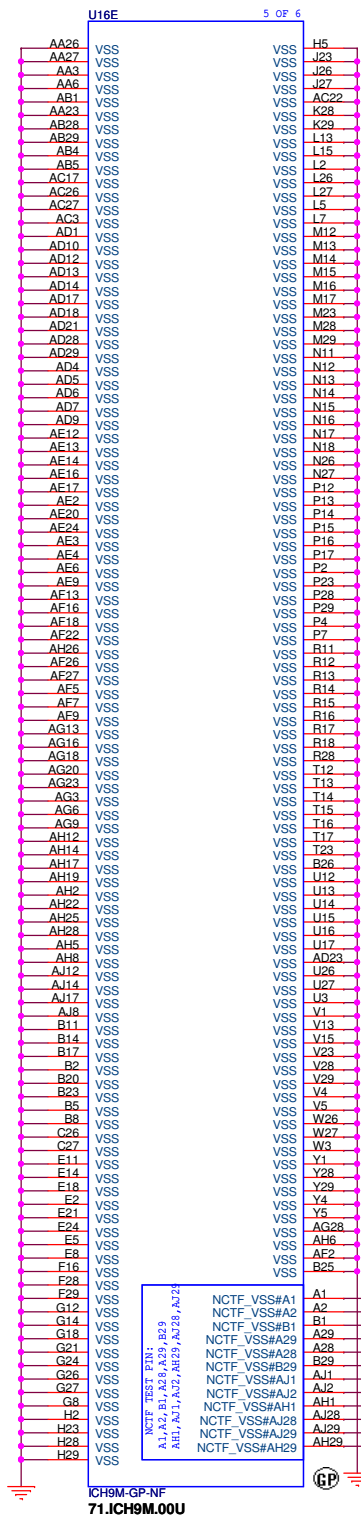






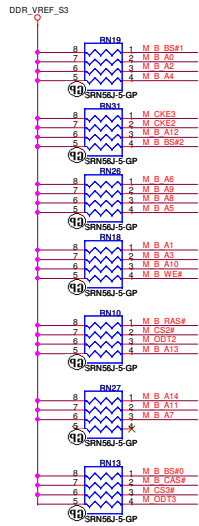






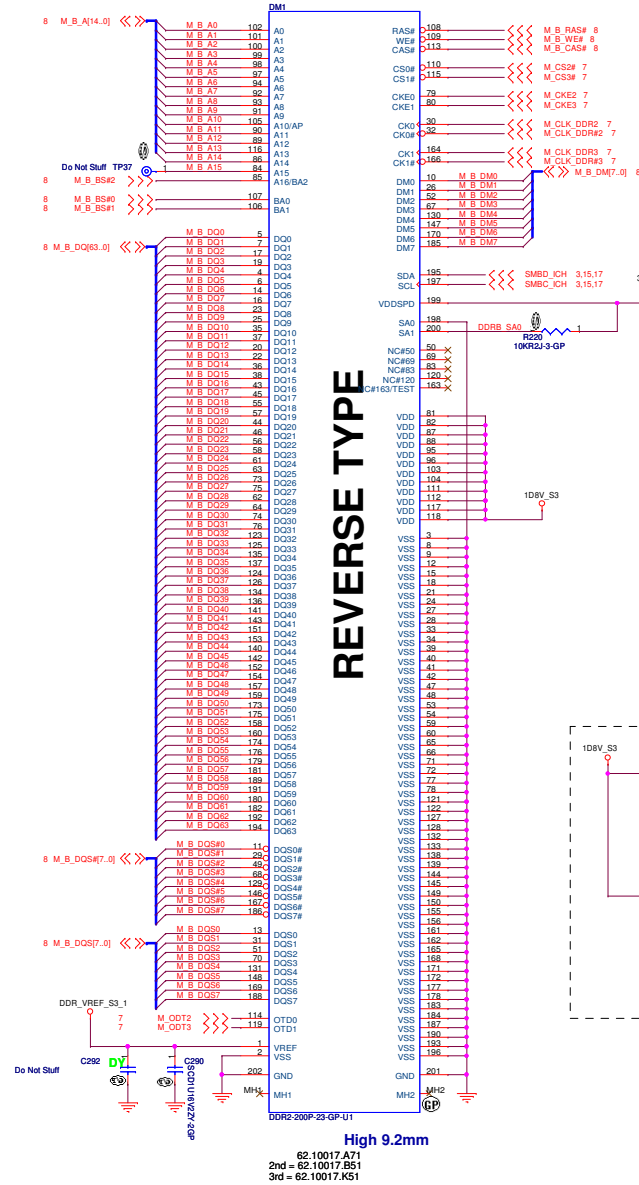
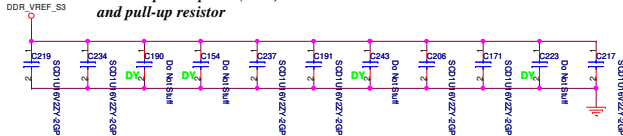
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

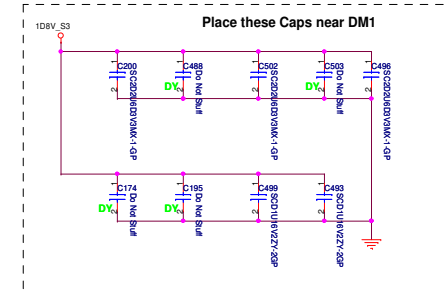


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

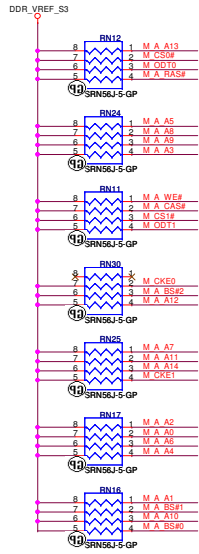


REVERSE TYPE



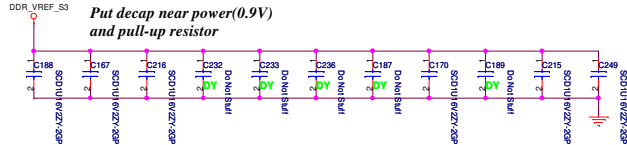
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

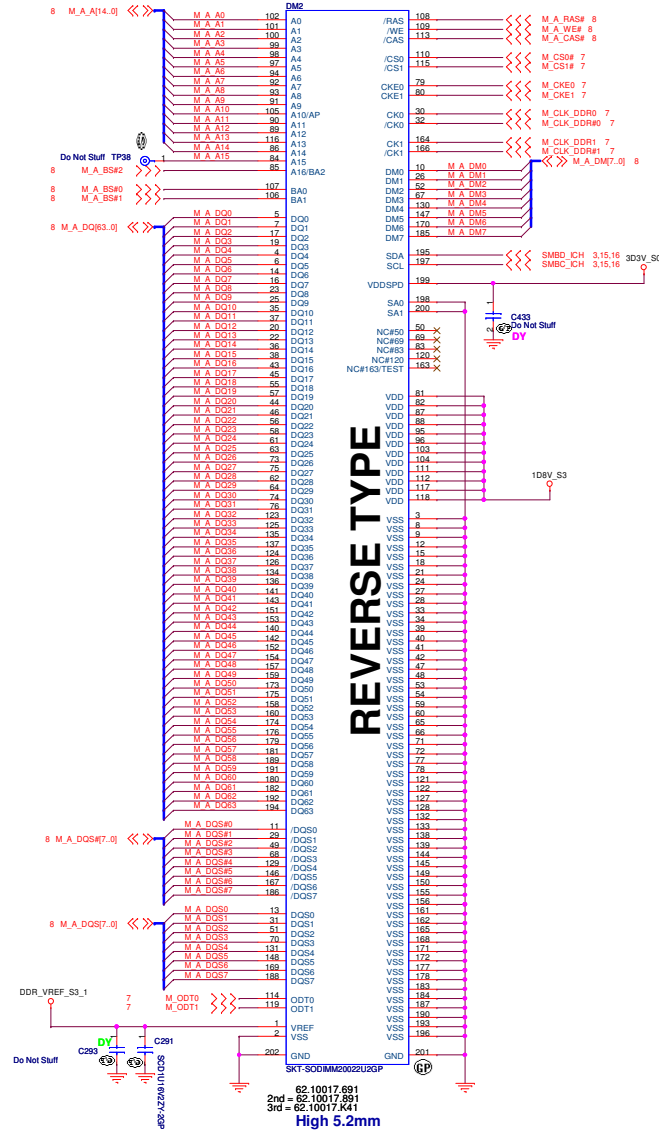
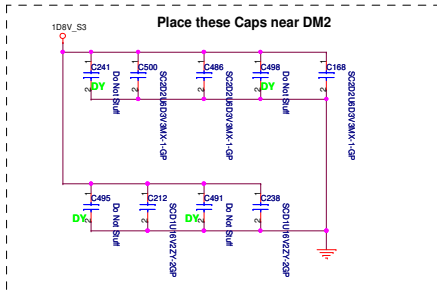


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



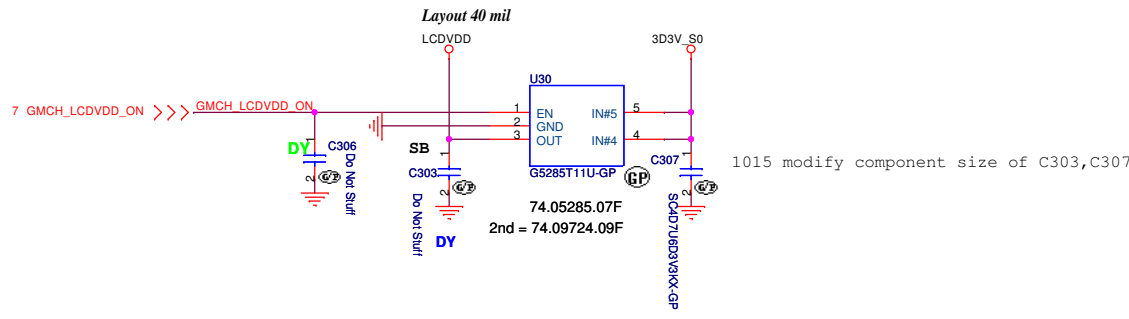
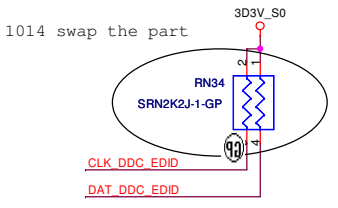
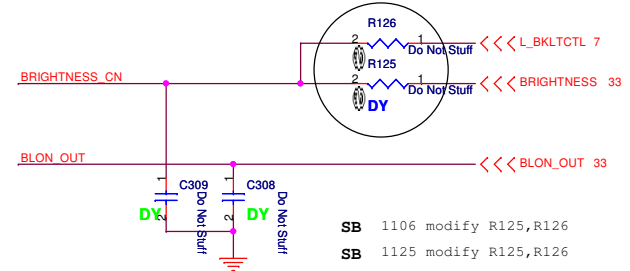
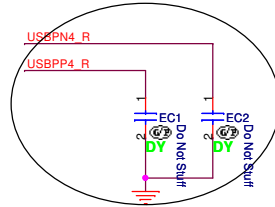
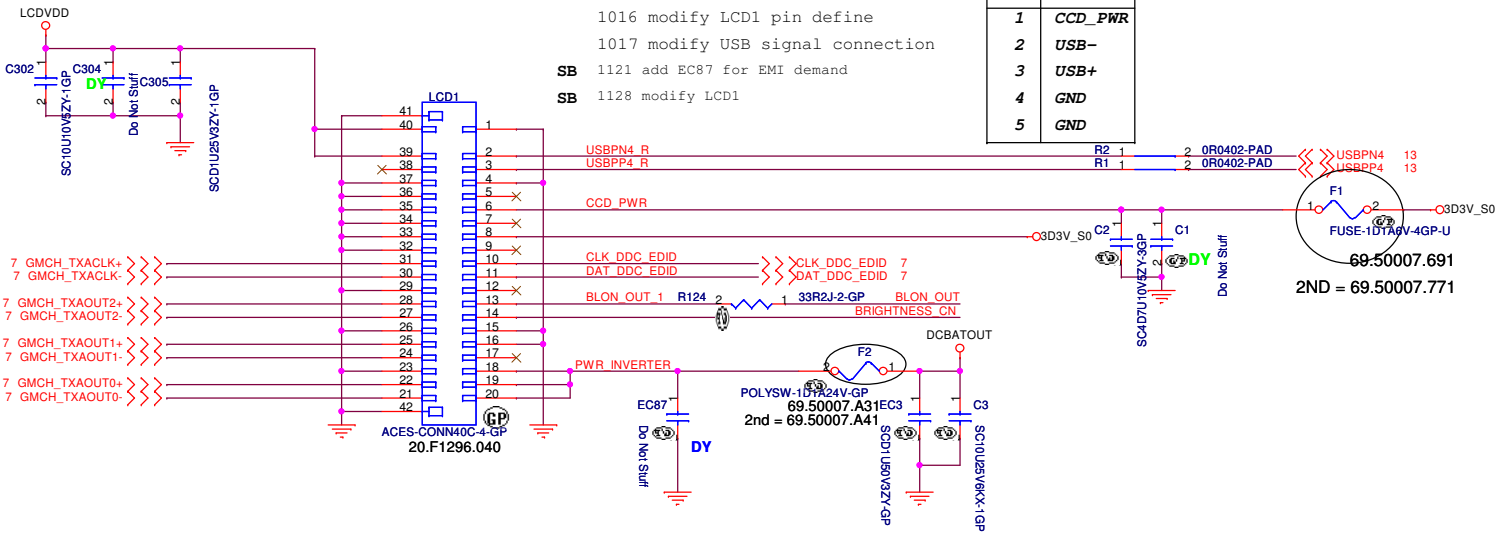
Place these Caps near DM2



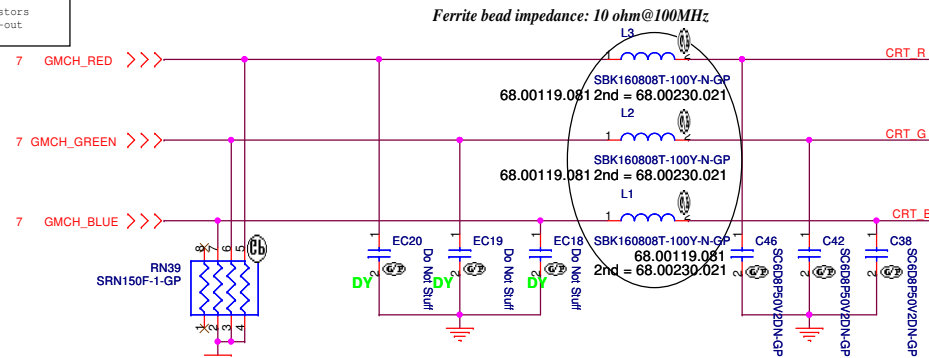
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Title			
DDR2 Socket 1 (DM2)			
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LCD/CCD CONN



Layout Note:
Place these resistors
close to the CRT-out
connector



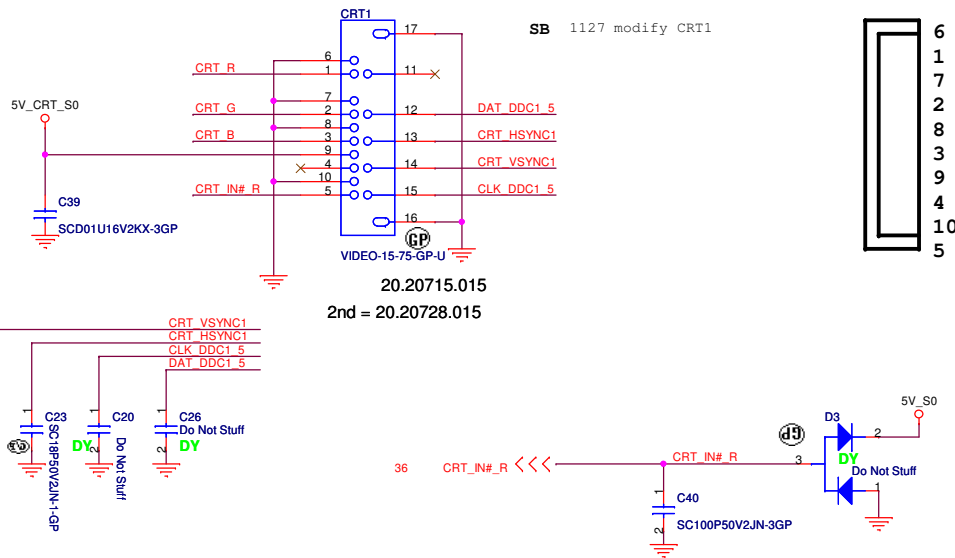
1016 modify L1, L2 and L3

Layout Note:

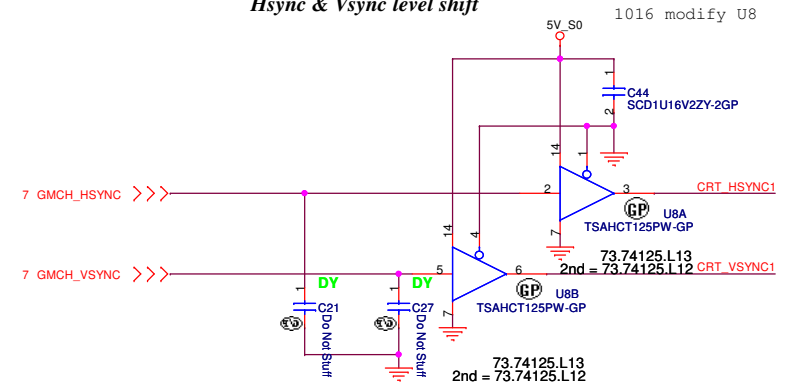
* Must be a ground return path between this ground and the ground on the VGA connector.

Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

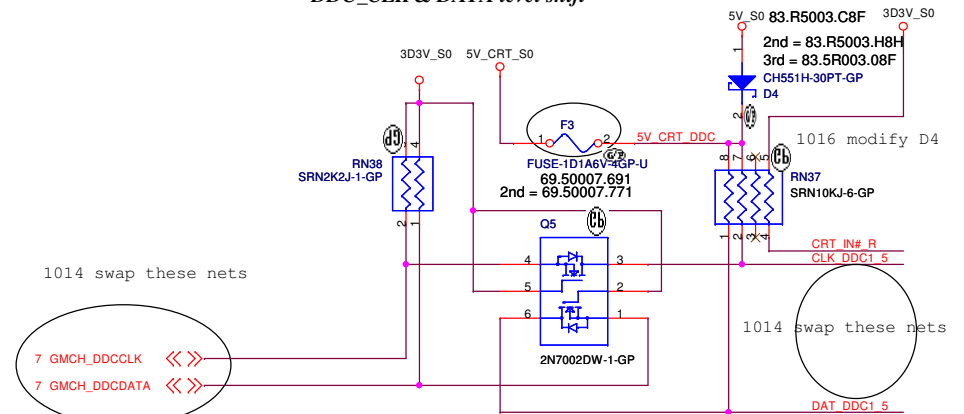
CRT I/F & CONNECTOR



Hsync & Vsync level shift



DDC_CLK & DATA level shift



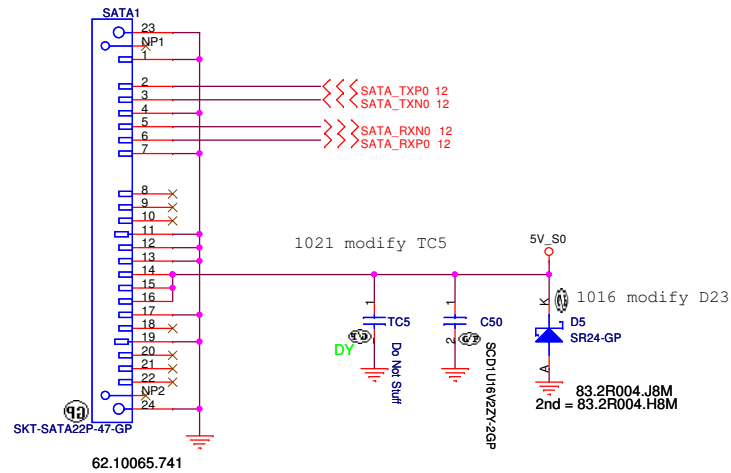
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CRT Connector		
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SATA Connector

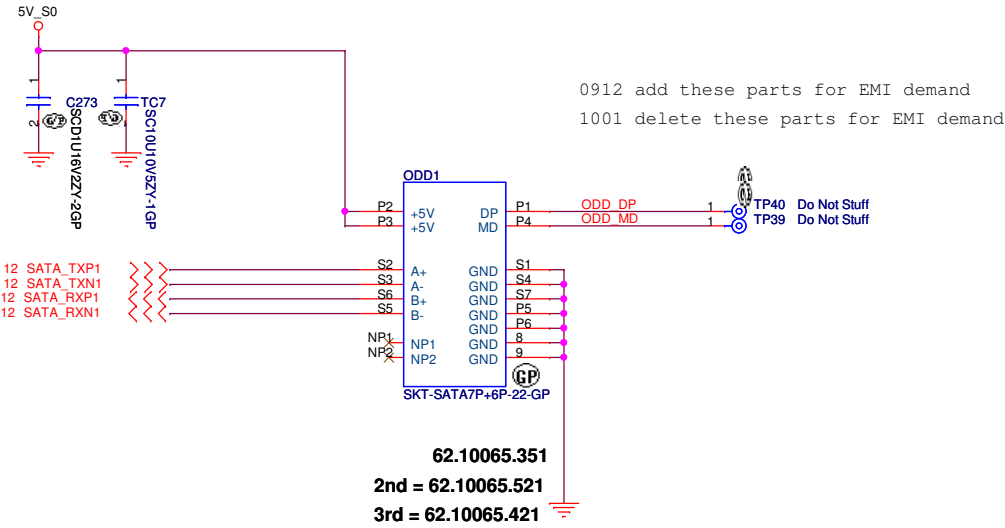
0912 add these parts for EMI demand
1001 delete these parts for EMI demand
1021 modify SATA1



UMA Two Phase 2

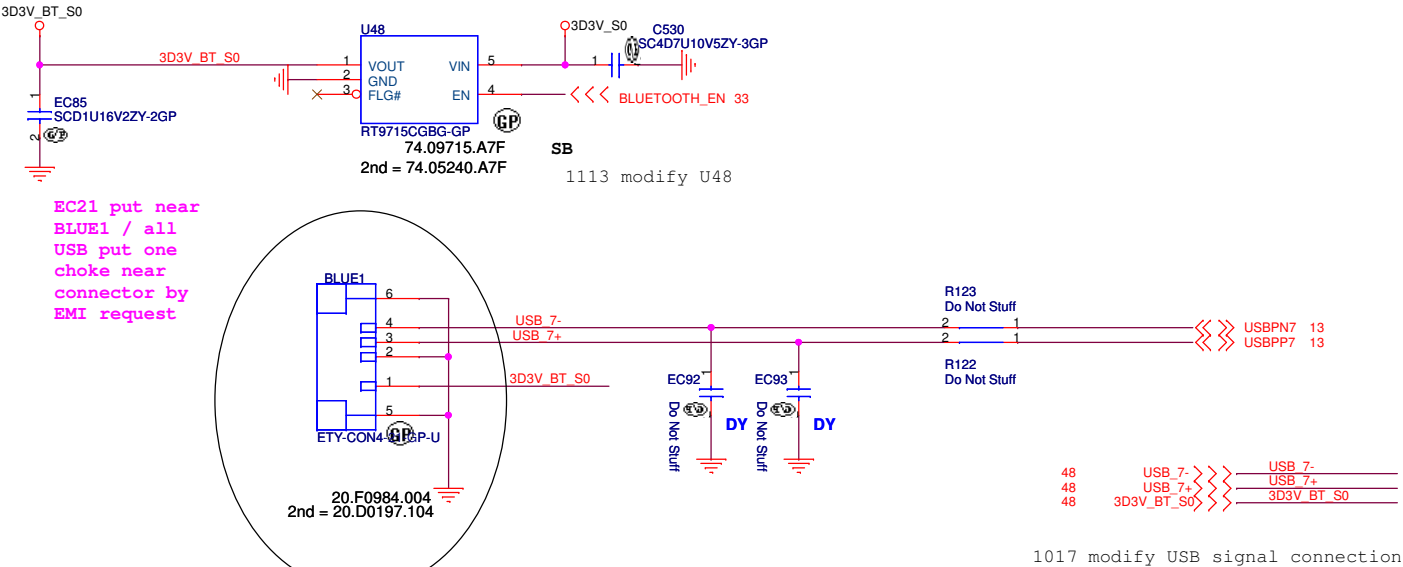
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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HDD			
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SATA ODD Connector



BLUETOOTH MODULE

1.5A / High Active Voltage 2V



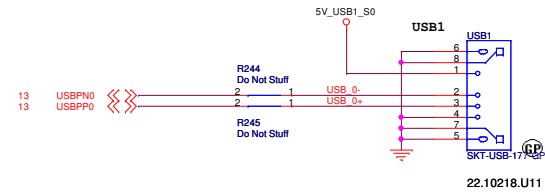
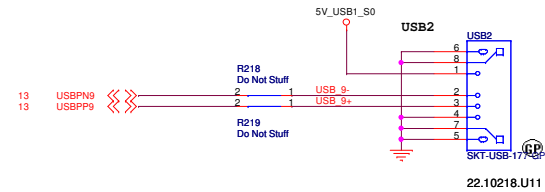
EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

20.F0984.004
2nd = 20.D0197.104

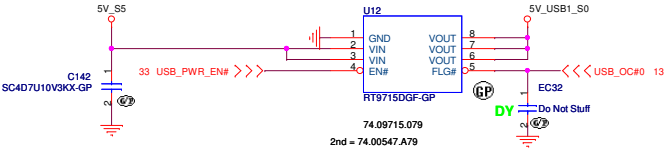
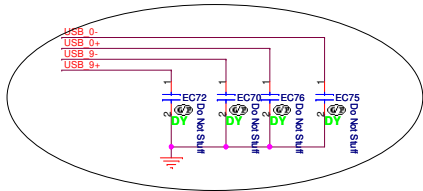
SB 1125 add EC92 and EC93

1017 modify USB signal connection

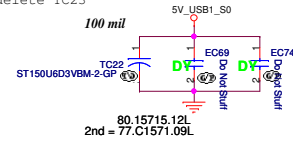
1017 modify USB signal connection
1021 modify and swap these parts(USB1 and USB2)

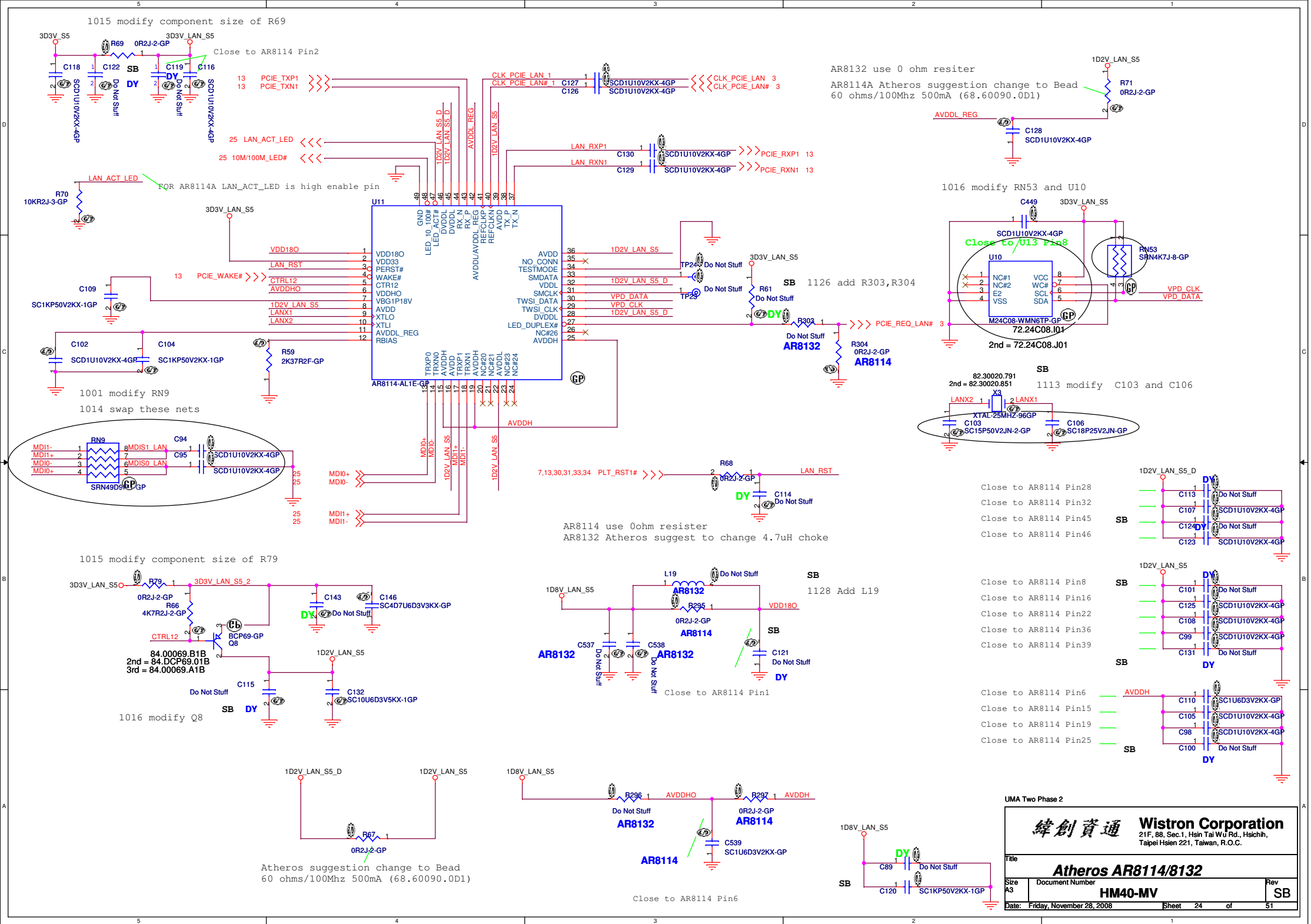


0912 add these parts for EMI demand

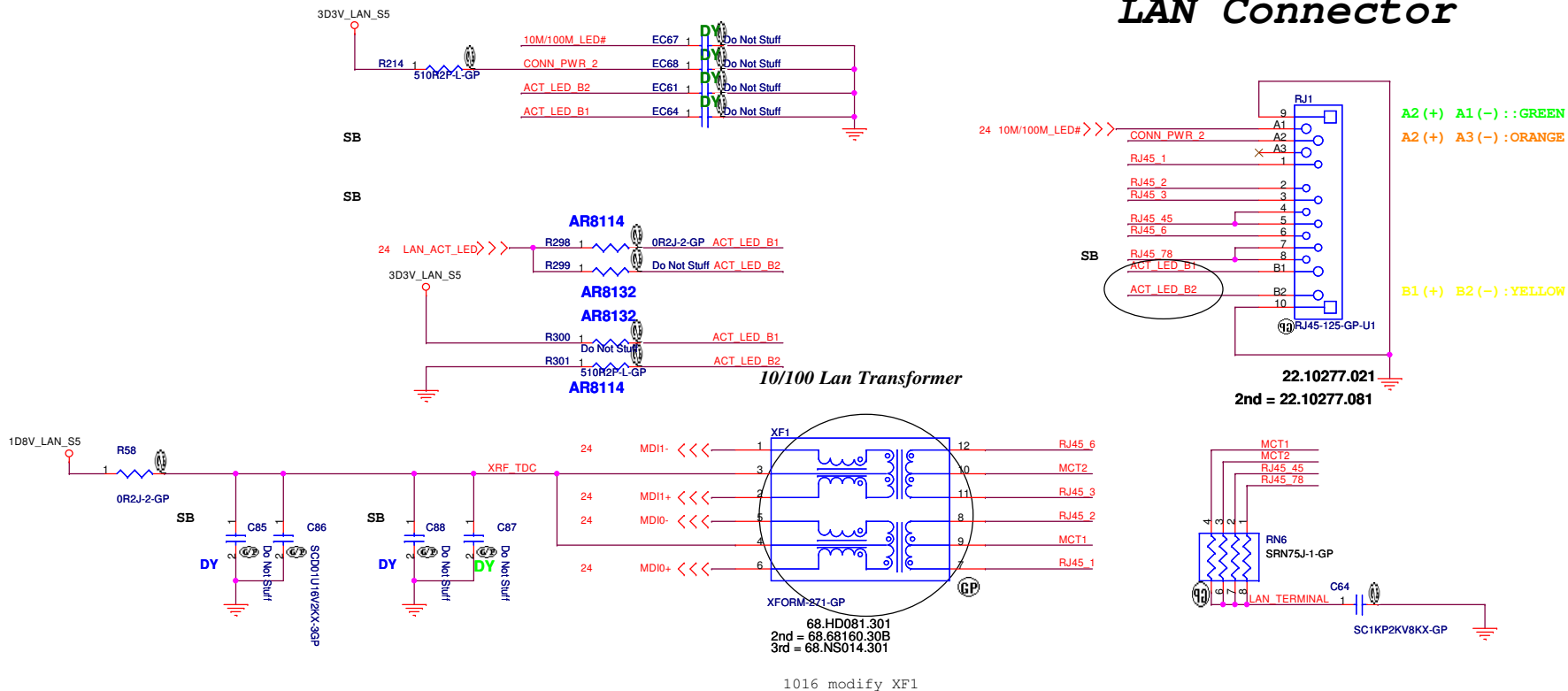


1021 delete TC23





LAN Connector



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP, DOC_RING, TIP, RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

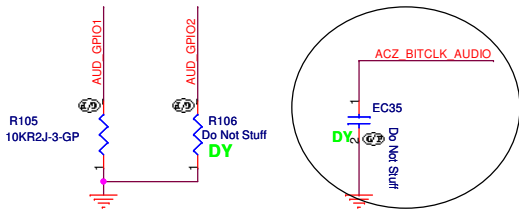
UMA Two Phase 2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LAN Connector	
Size: A3	Document Number: HM40-MV
Date: Monday, December 01, 2008	Rev: SB
Sheet 25 of 51	

PC BEEP GAIN CONTROL

Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.

0912 add the part for EMI demand



GAIN	10K GPIO RESISTORS	
	R615	R614
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-18dB	Omit	Populate

SB 1118 delete C245 and C270

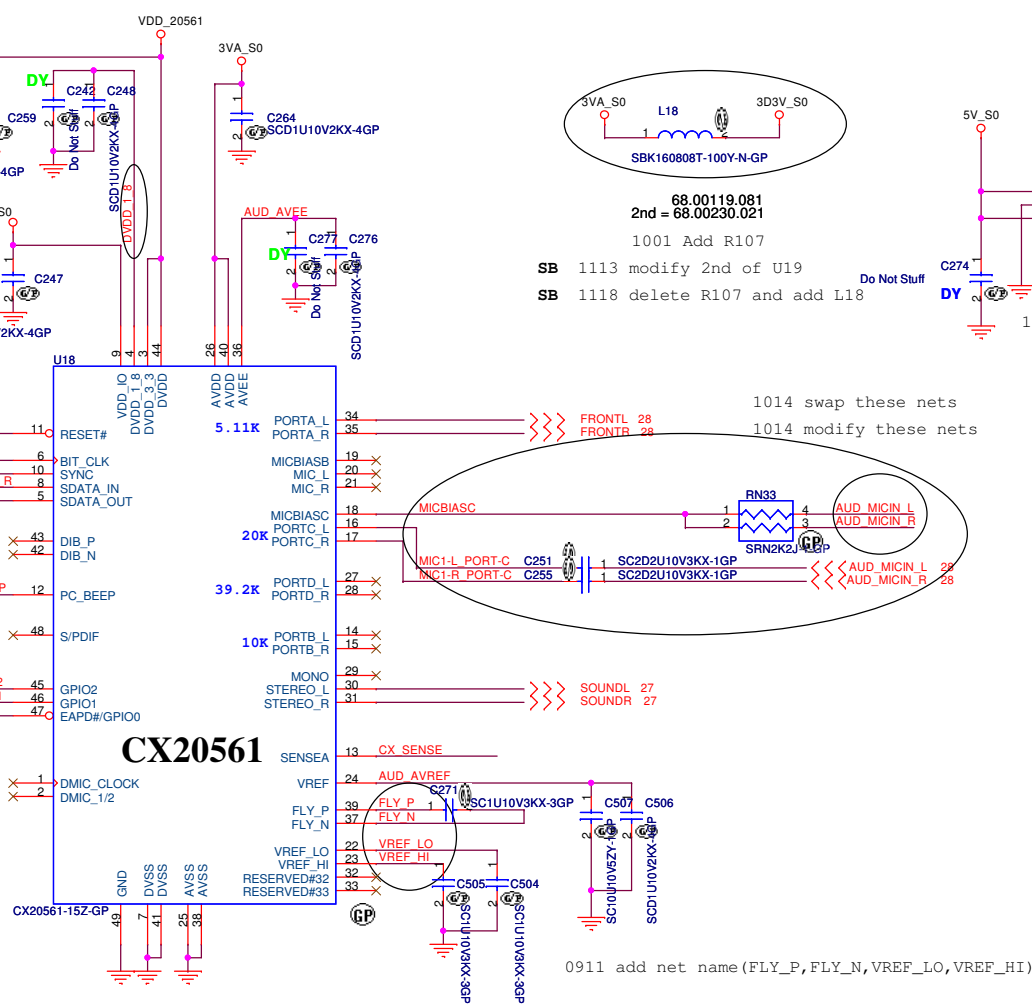
0911 add net name(DVDD_1_8)

0911 add net name(ACZ_SDATAIN0_R)

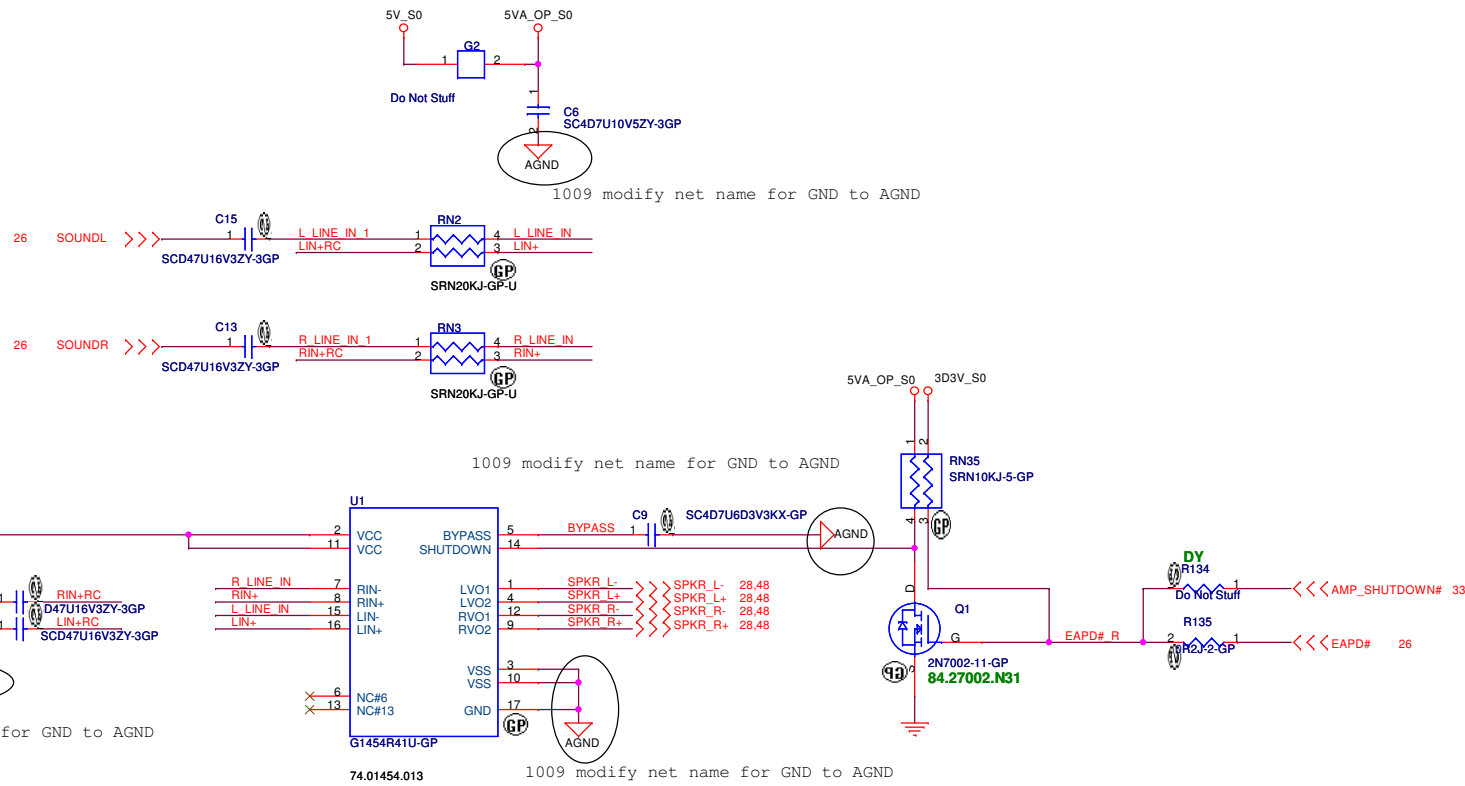
12 ACZ_RST#_AUDIO >>>
12 ACZ_BITCLK_AUDIO >>>
12 ACZ_SYNC_AUDIO >>>
12 ACZ_SDATAIN0 >>>
12 ACZ_SDATAOUT_AUDIO >>>

SB 1126 add C541 and modify R101

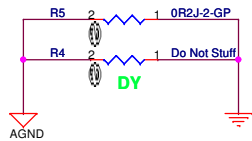
27 EAPD# <<<



AUDIO OP AMPLIFIER



AC decoupling

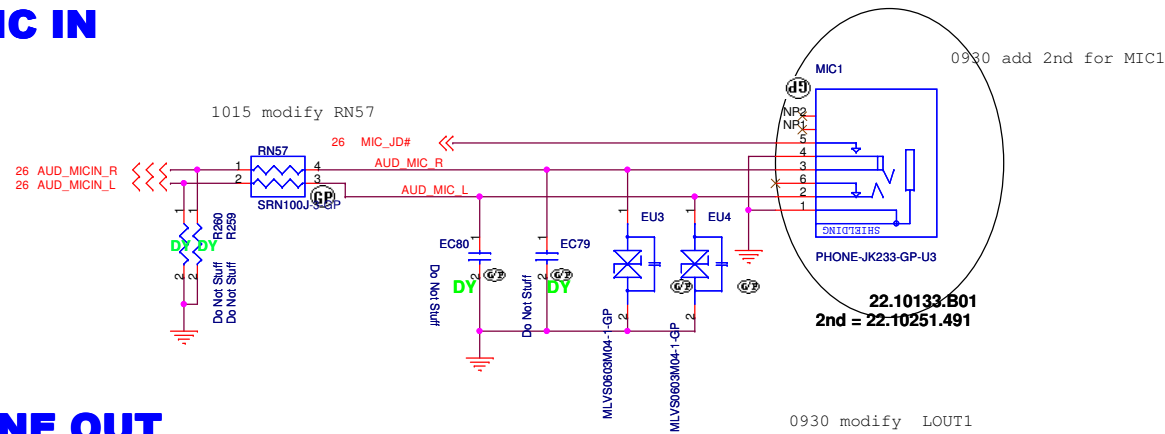


UMA Two Phase 2

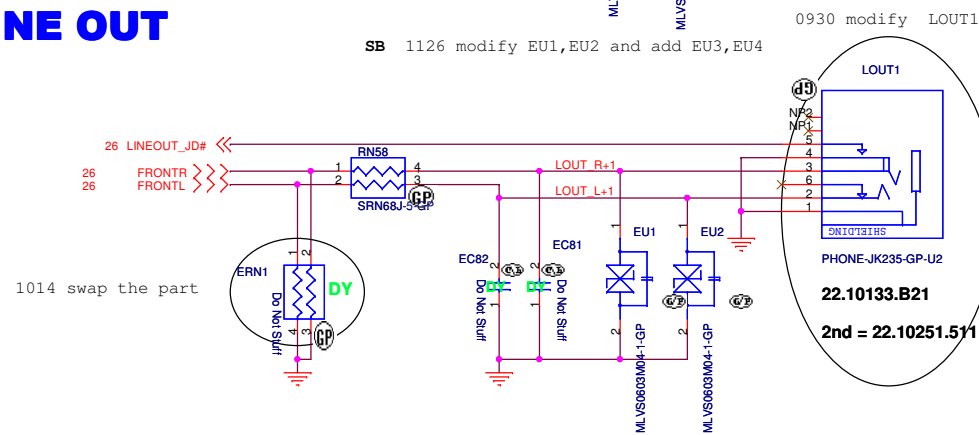
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				
AUDIO AMP				
Size	Document Number			Rev
	HM40-MV			SB
Date:	Monday, December 01, 2008		Sheet 27 of	51

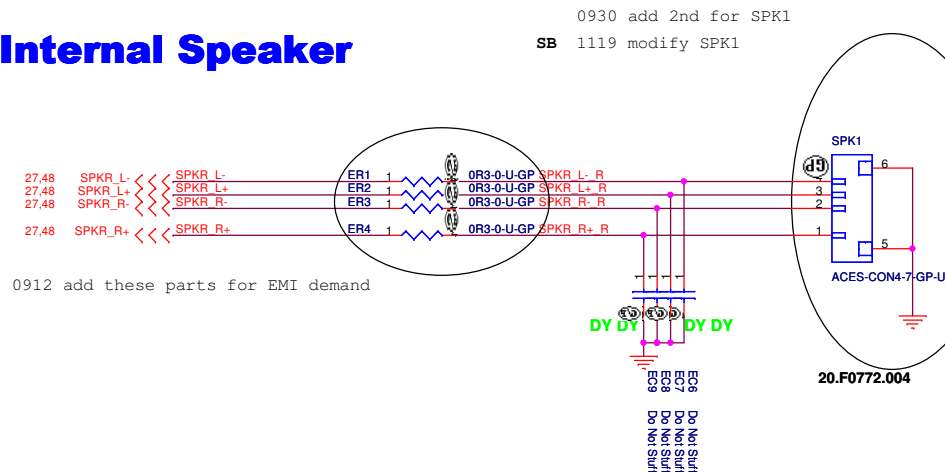
MIC IN



LINE OUT



Internal Speaker



UMA Two Phase 2

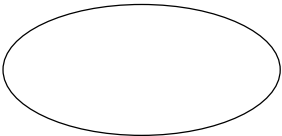
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AUDIO JACK			
Size	Document Number	Rev	
	HM40-MV	SB	
Date:	Monday, December 01, 2008	Sheet	28 of 51

MDC 1.5 CONN

0912 add the part for EMI demand

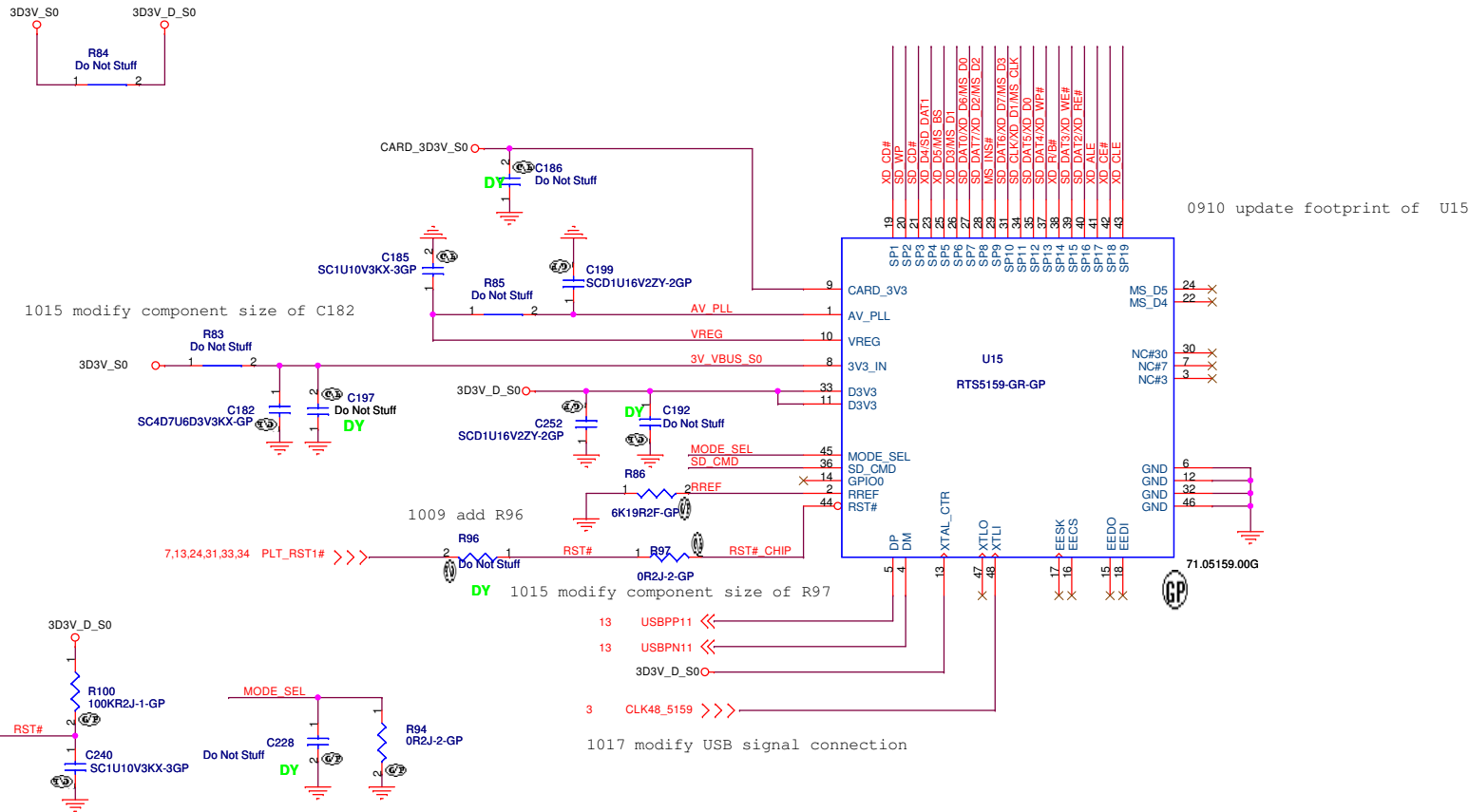
1002 modify MDC1

SB
1112 delete MDC function

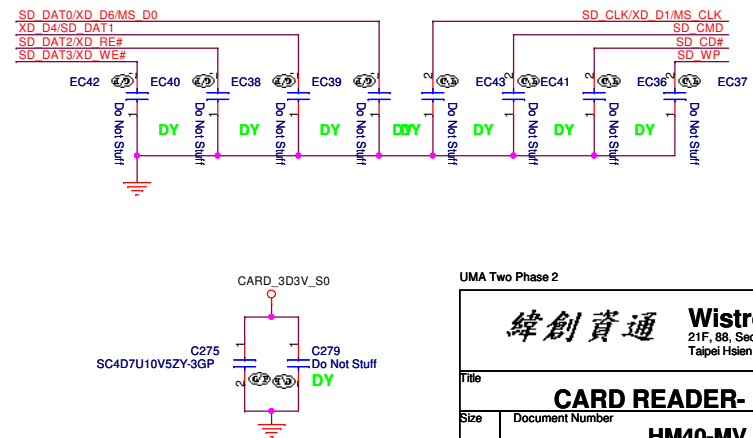
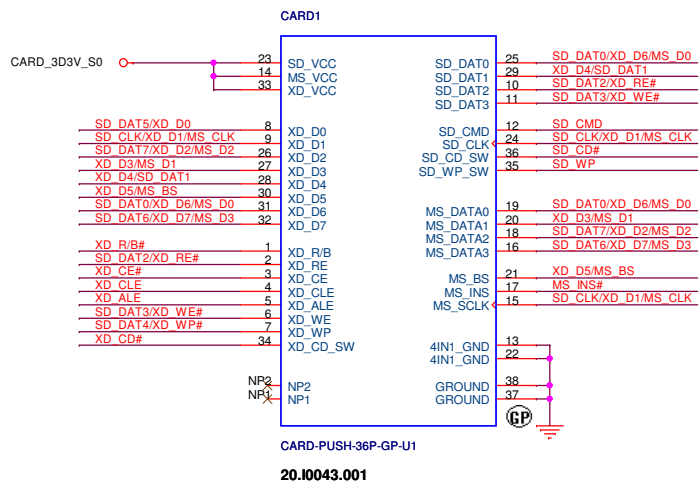


UMA Two Phase 2

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wuj Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MDC			
Size	Document Number		Rev
	HM40-MV		SB
Date:	Monday, November 24, 2008	Sheet	29 of 51



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)

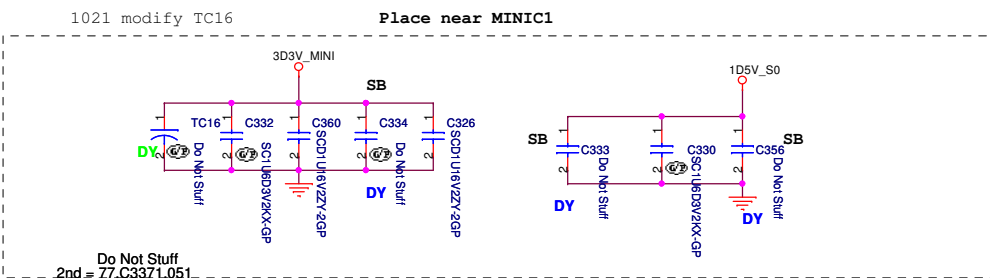
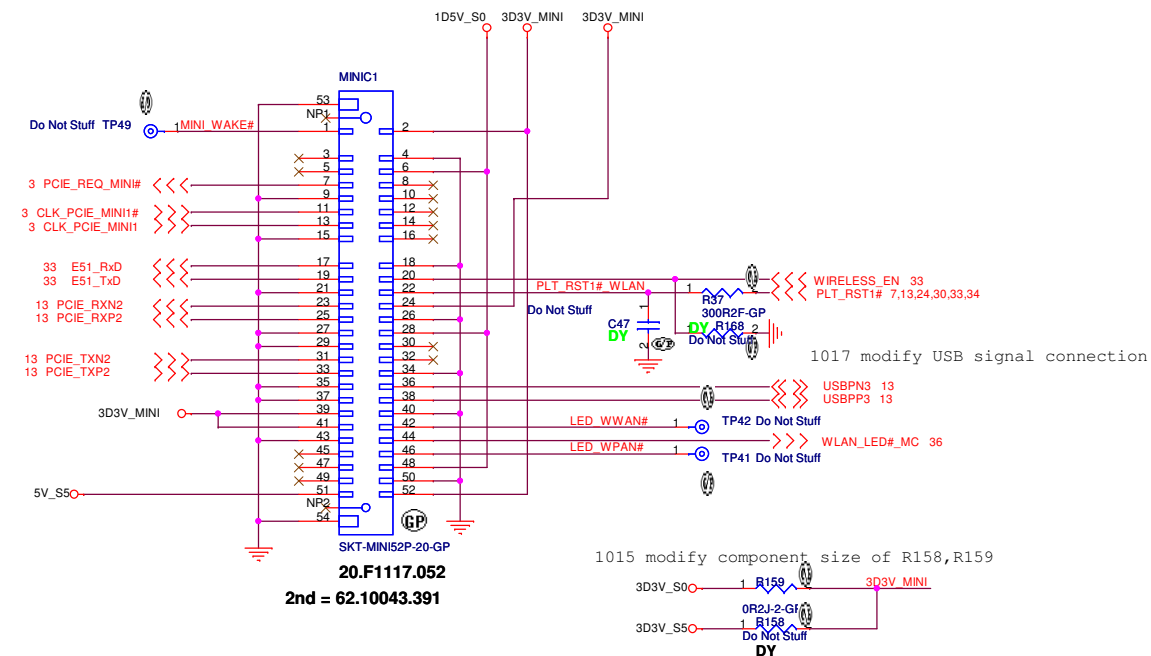


UMA Two Phase 2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

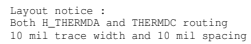
CARD READER- RTS5159		
Size	Document Number	Rev
	HM40-MV	SB
Date: Monday, December 01, 2008	Sheet 30 of 51	

Mini Card Connector(WLAN)



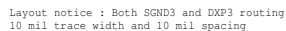
UMA Two Phase 2

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MINI CARD			
Size	Document Number	Rev	
	HM40-MV	SB	
Date:	Monday, December 01, 2008	Sheet	31 of 51



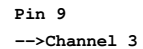
C373 must be near EMC2102

Layout notice : Both SGND2 and DXP2 routing
10 mil trace width and 10 mil spacing

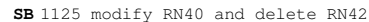
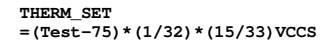


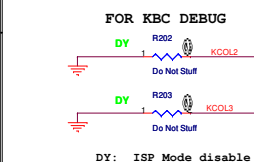
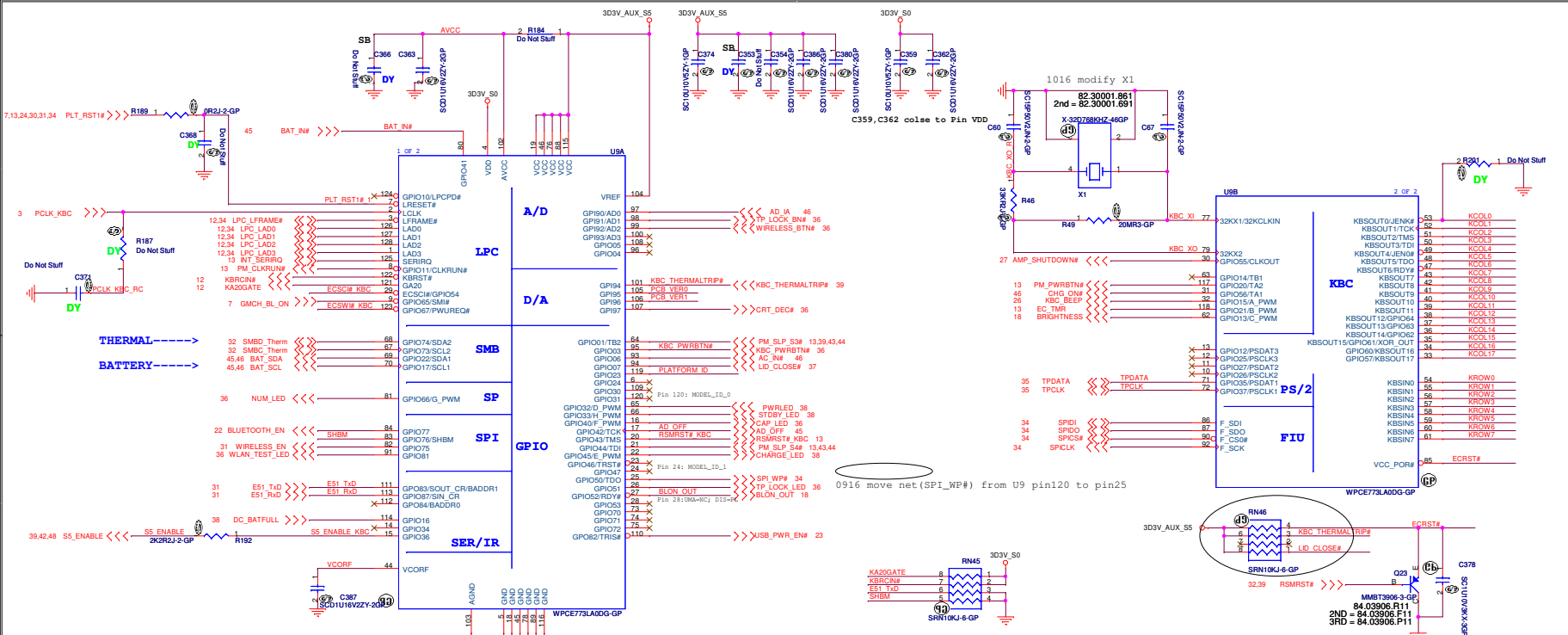
C372 must be near EMC2102

C375 must be near Q8

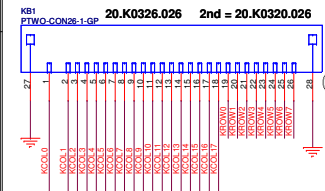


```
Pin 10
--> Fan is OFF
```



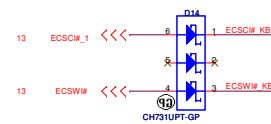
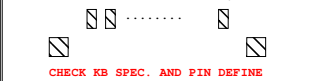


Internal Keyboard Connector

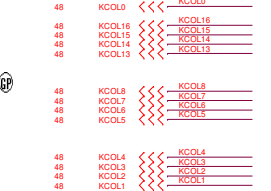


0930 modify KB1

Internal Keyboard CONN

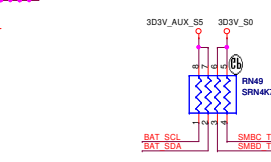


Internal Keyboard Connector

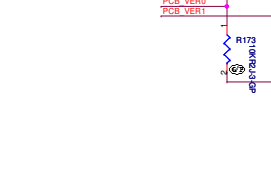


0930 modify KB1

Internal Keyboard CONN

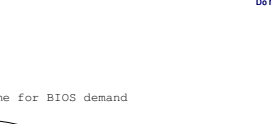


Internal Keyboard Connector

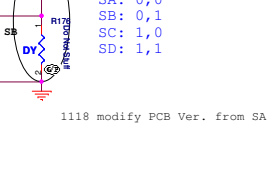


0930 modify KB1

Internal Keyboard CONN

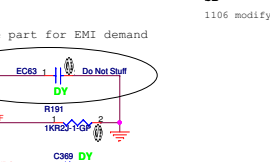


Internal Keyboard Connector

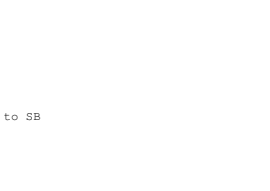


0930 modify KB1

Internal Keyboard CONN

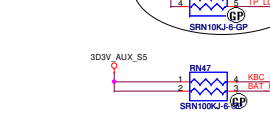
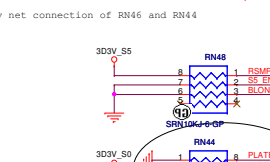


Internal Keyboard Connector



0930 modify KB1

Internal Keyboard CONN

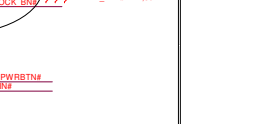
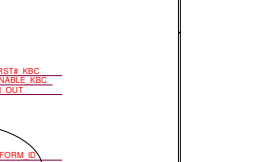
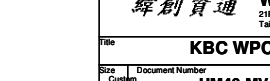


Internal Keyboard Connector

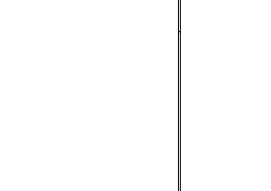


0930 modify KB1

Internal Keyboard CONN

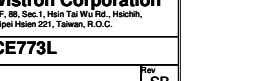


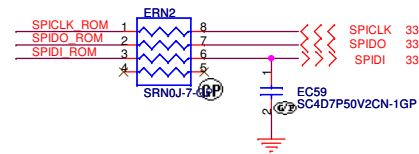
Internal Keyboard Connector



0930 modify KB1

Internal Keyboard CONN





SB

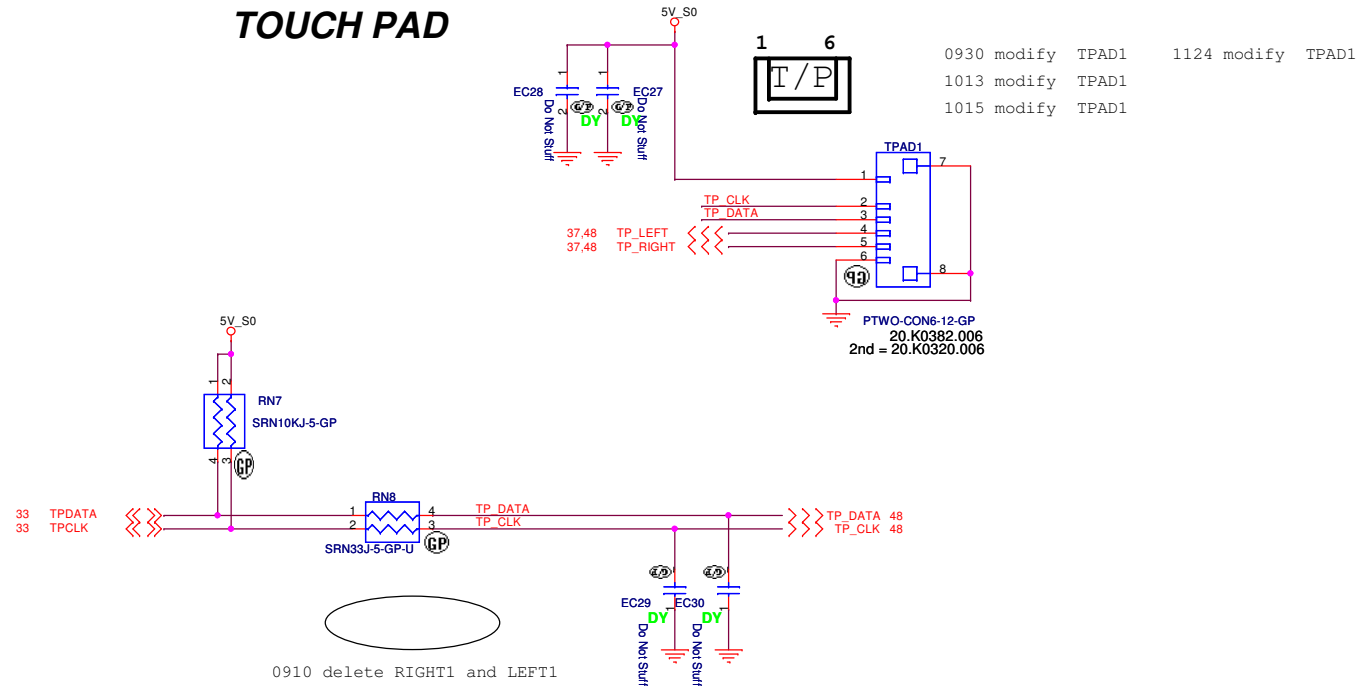
Pin	Signal	Direction / Value
1	LPC_LAD0	<< >> LPC_LAD[0.3] 12,33
2	LPC_LAD1	
3	LPC_LAD2	
4	LPC_LAD3	
5	LPC_LAD4	
6	LPC_LFRAME#	<< >> LPC_LFRAME# 12,33
7	PLT_RST1#	<< >> PLT_RST1# 7,13,24,30,31,33
8	PCLK_FWH	<< >> PCLK_FWH 3
9	PCLK_FWH	
10	GND	
11	GND	
12	GND	

DY Do Not Stuff

EC26 Do Not Stuff

The diagram shows a circuit for the **SPI_HOLD#EC56** pin. The pin is labeled **Do Not Stuff**. It is connected to ground through a resistor labeled **DY**. The pin is also connected to a signal line.

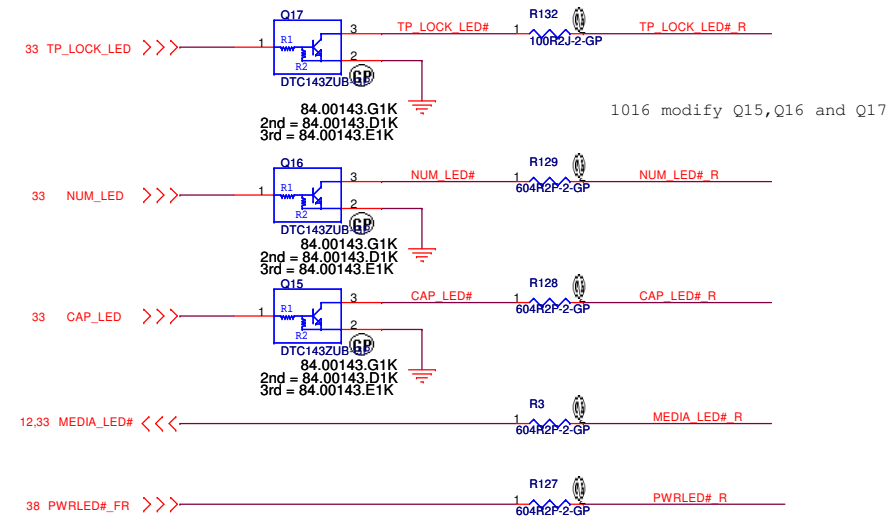
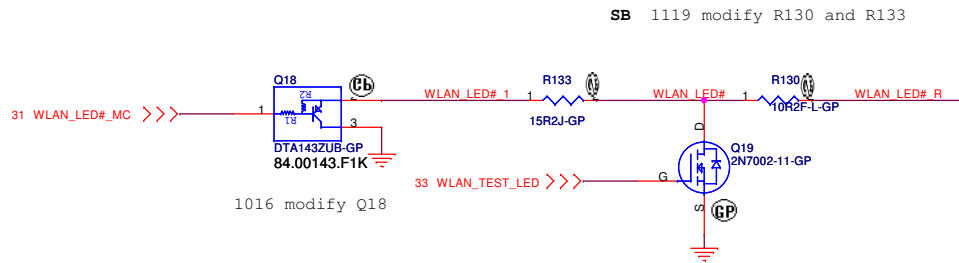
TOUCH PAD



UMA Two Phase 2

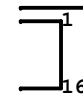
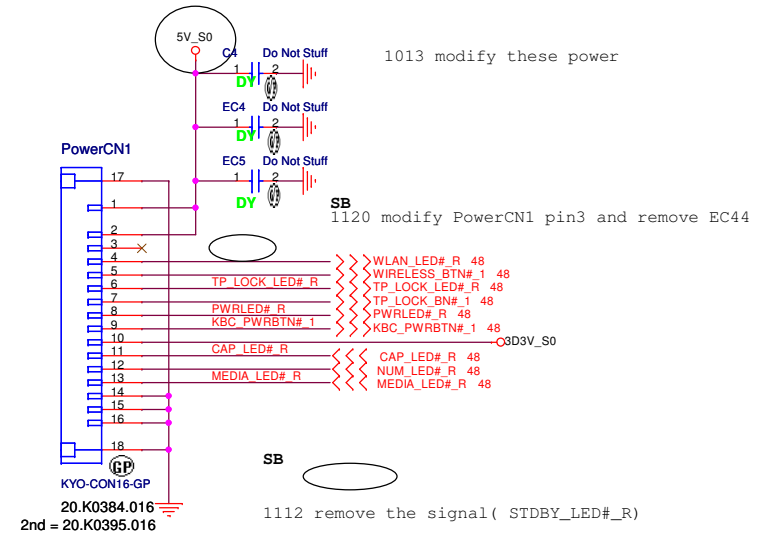
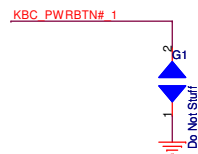
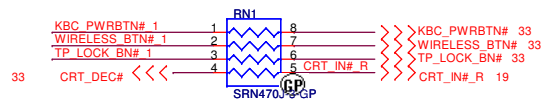
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Touch pad	
Size	Document Number	HM40-MV		Rev
				SB
Date:	Monday, December 01, 2008	Sheet	35	of 51



SB

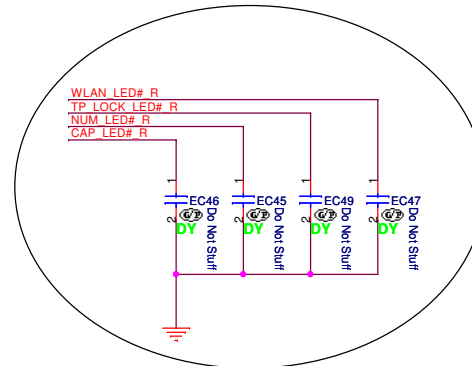
1112 remove these signals(STDBY_LED#_FR and STDBY_LED#_R) and R131



SB

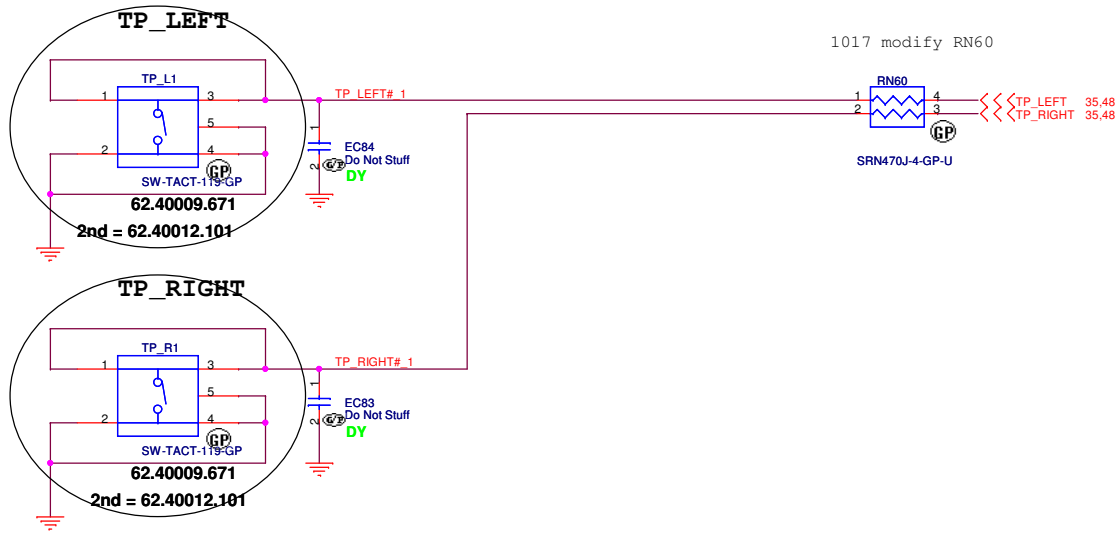
1112 remove the signal(STDBY_LED#_R)

0912 add these parts for EMI demand

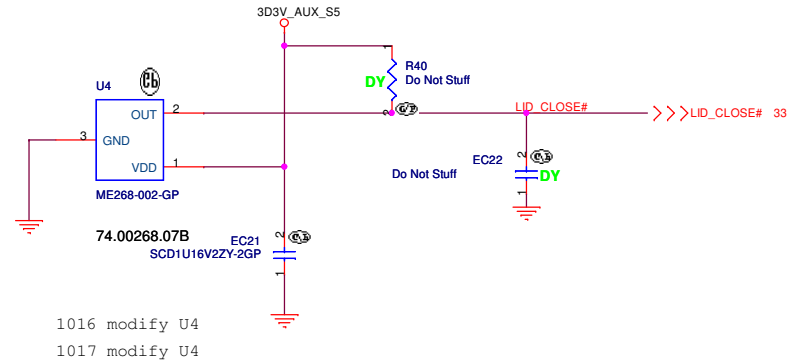


UMA Two Phase 2

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Power Board			
Size	Document Number	Rev	
	HM40-MV	SB	
Date: Wednesday, November 26, 2008	Sheet 36	of 51	

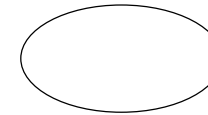


Cover Up Switch



1017 add U61,R52,EC24 and EC23

1020 delete U61,R52,EC24 and EC23

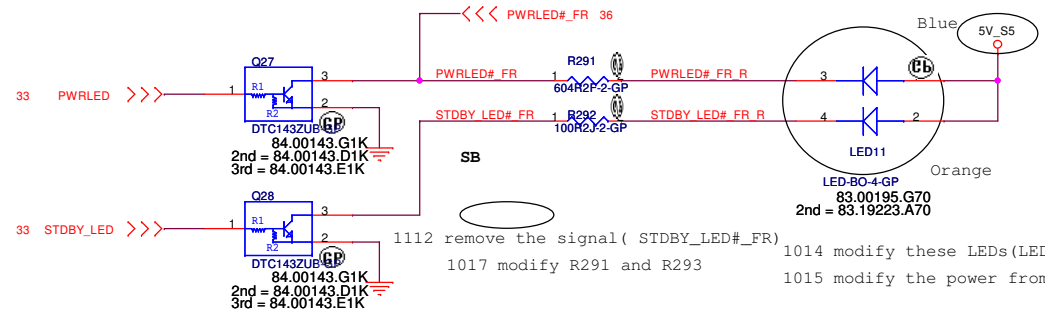


UMA Two Phase 2

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
SWITCHS			
Size	Document Number		Rev
	HM40-MV		SB
Date:	Monday, December 01, 2008	Sheet 37 of	51

1015 modify the power from 3D3V_S5 to 5V_S5

SB 1106 modify LED11

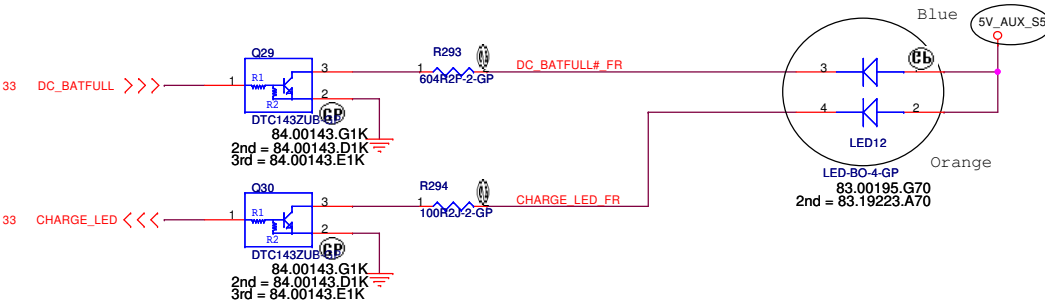


1014 modify these LEDs(LED11,LED12)

1015 modify the power from 3D3V_S5 to 5V_S5

SB 1106 modify LED12

1106 modify LED power from 5V_S5 to 5V_AUX_S5



1016 modify Q27~Q30

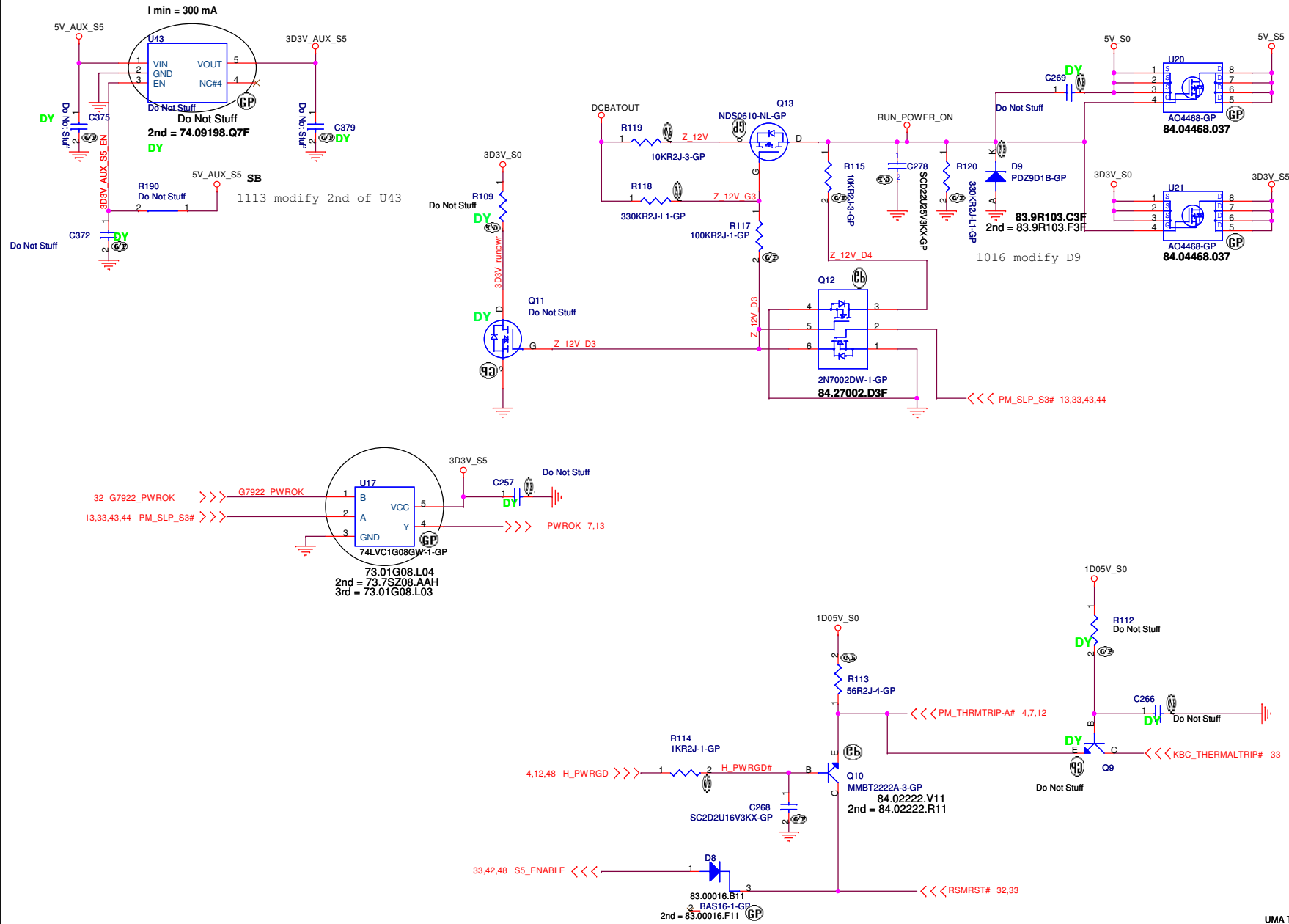
UMA Two Phase 2

緯創資通 Wistron Corporation
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Title		
LED		
Size	Document Number	Rev
	HM40-MV	SB
Date: Wednesday, November 26, 2008		
Sheet 38 of 51		

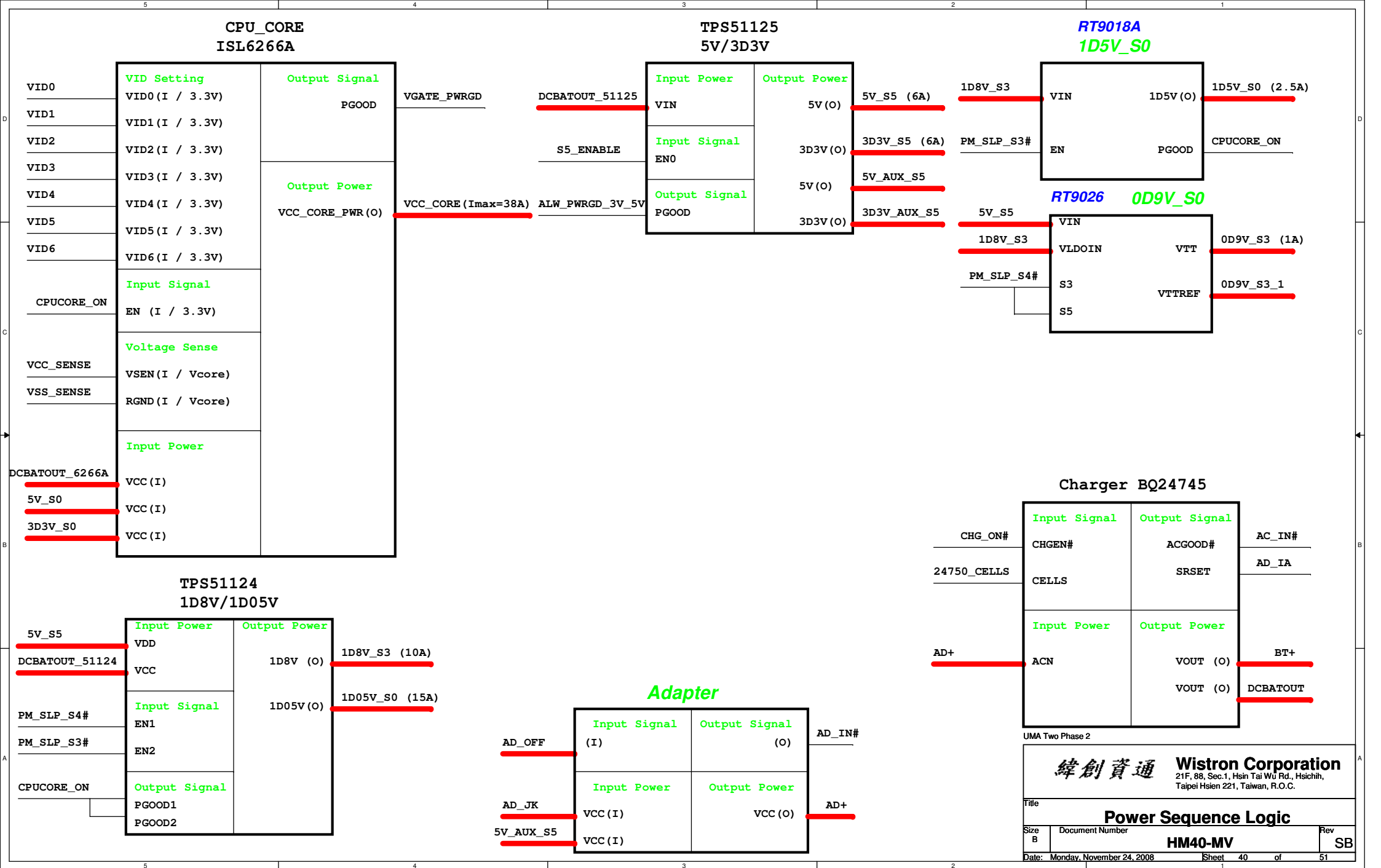
3D3V_AUX_S5

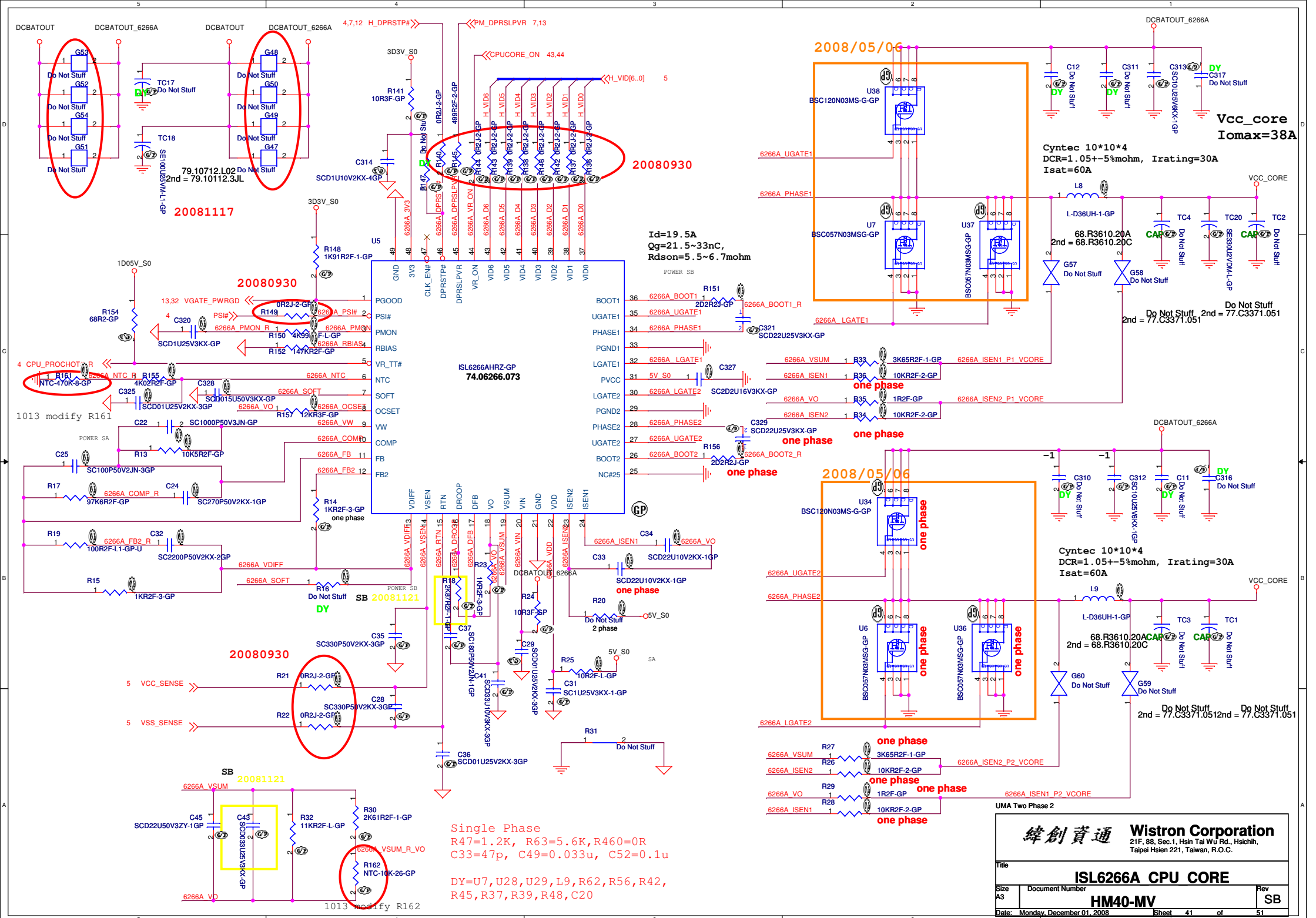
Run Power

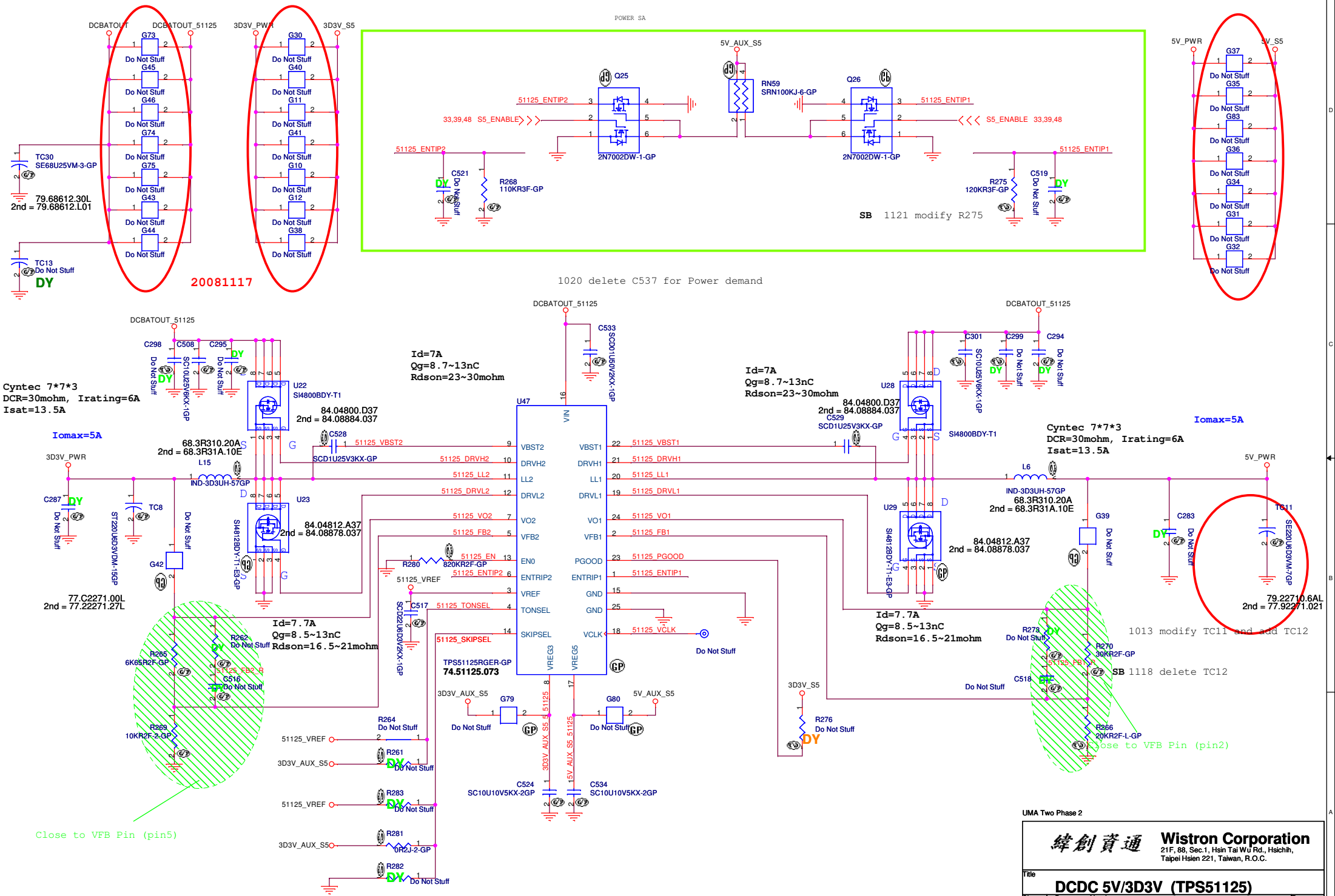


UMA Two Phase 2

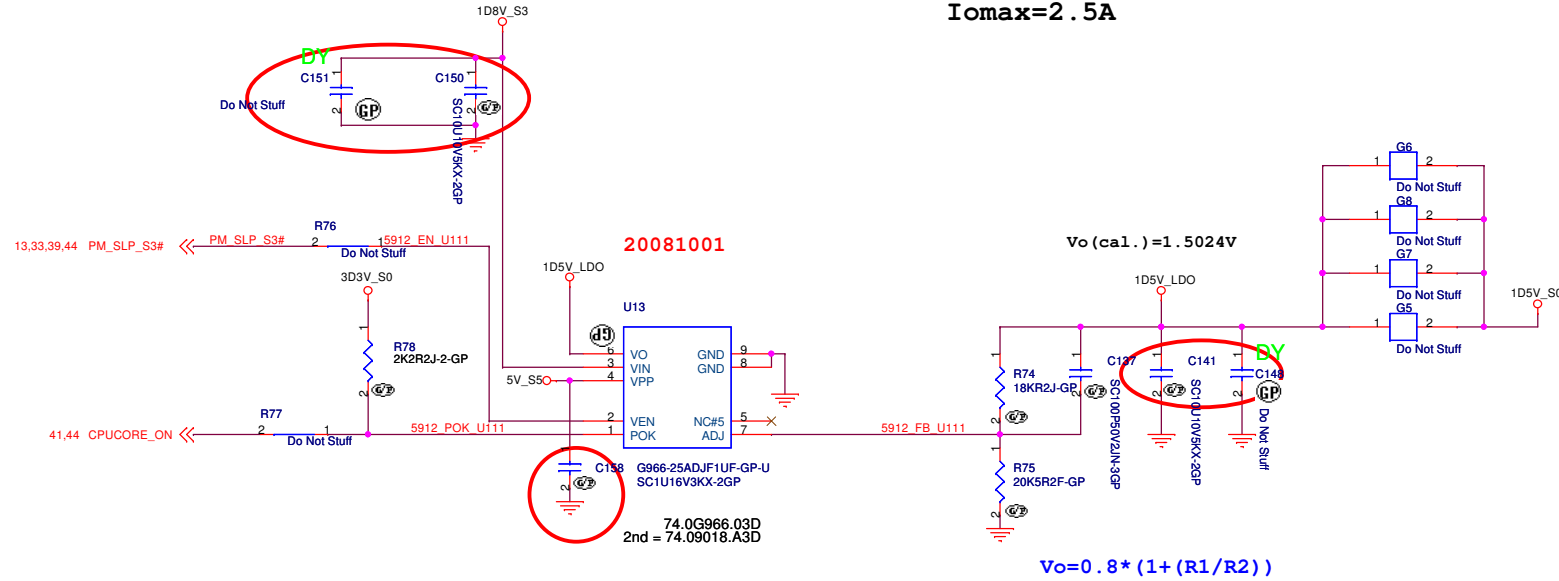
Title				RUN POWER and 3D3V_AUX_S5			
Size		Document Number				Rev	
		HM40-MV				SB	
Date: Monday, December 01, 2008				Sheet 39 of 51			





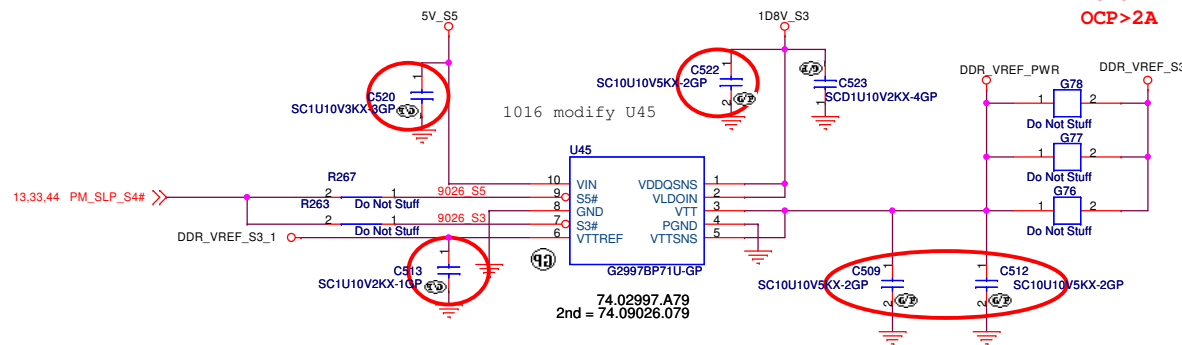


1D5V_S0
I_{omax}=2.5A



20081001

I_{omax}=1A
OCP>2A

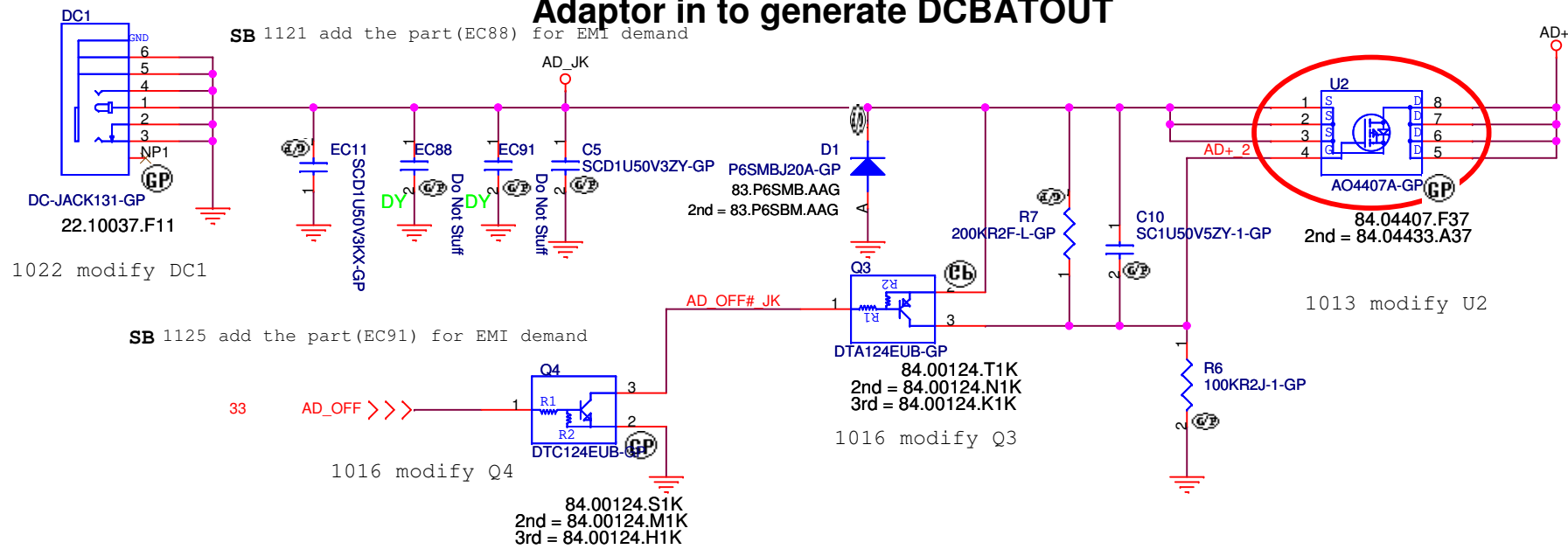


UMA Two Phase 2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

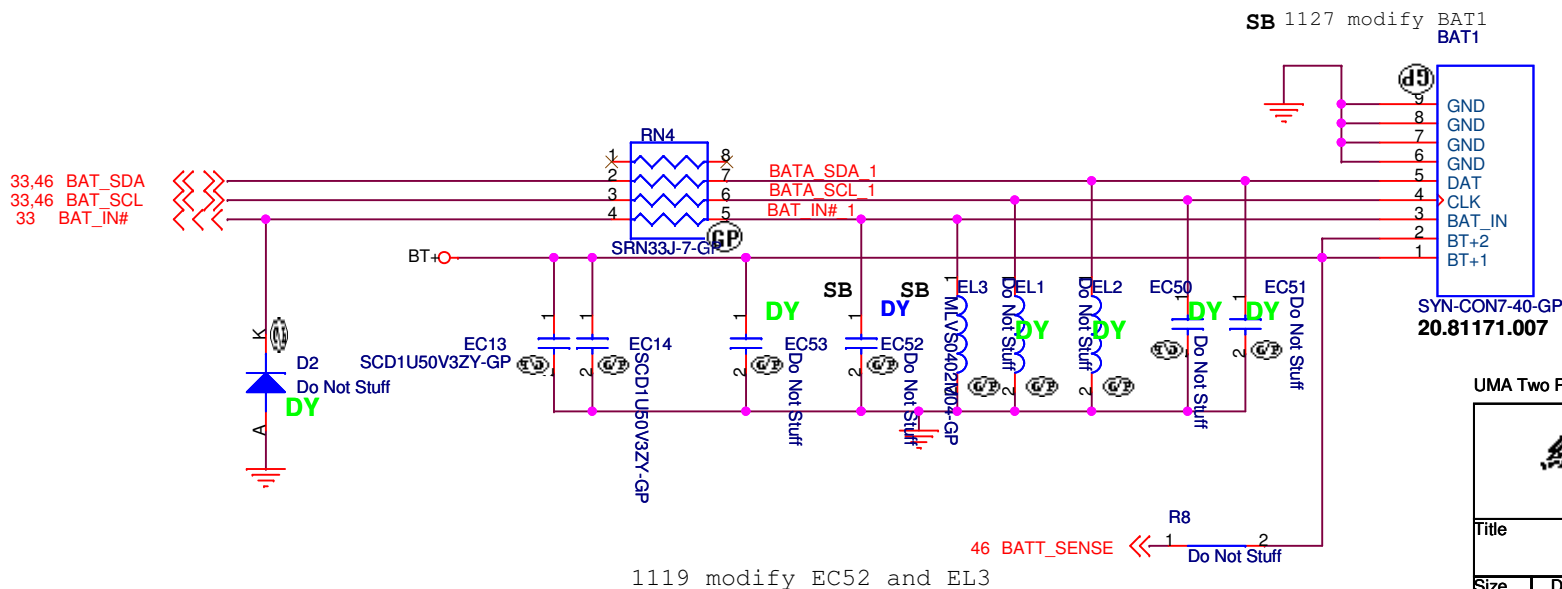
Title		
1D5V & 0D9V		
Size	Document Number	Rev
A3	HM40-MV	SB
Date:	Monday, December 01, 2008	Sheet 43 of 51

Adaptor in to generate DCBATOUT



BATA_SDA_1 48
BATA_SCL_1 48
BAT_IN#_1 48

BATTERY CONNECTOR



UMA Two Phase 2

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

AD/BATT CONN

Size

Document Number

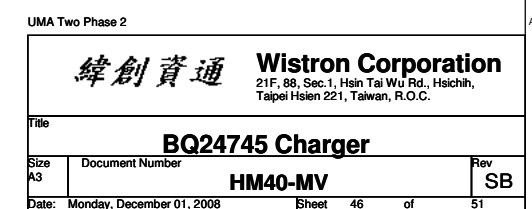
HM40-MV

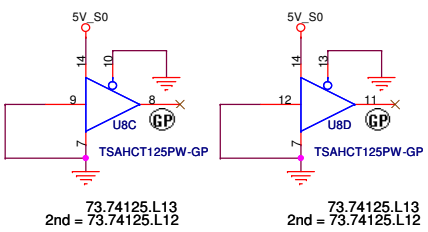
Rev

SB

Date: Monday, December 01, 2008

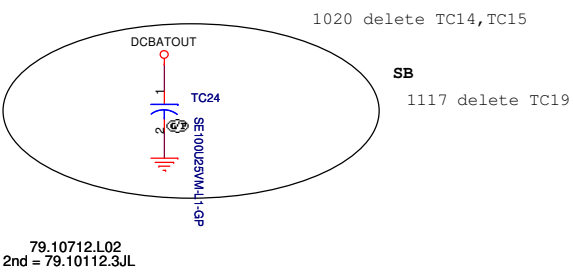
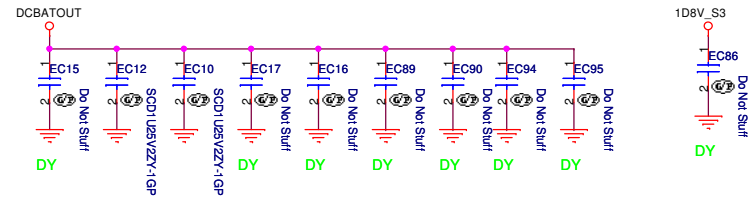
Sheet 45 of 51



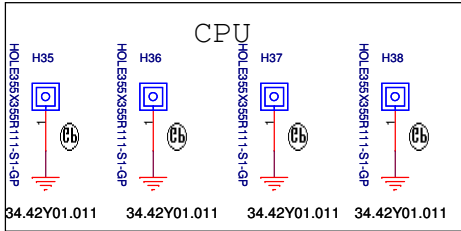


1016 modify U32

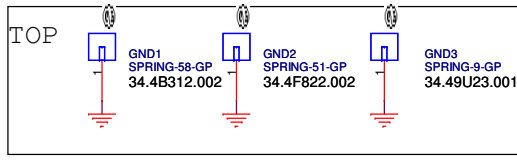
1017 add these parts(EC10,EC12,EC15~EC17,EC86) for EMI demand
1020 add the part(EC86) for EMI demand 1125 add the part(EC90) for EMI demand
SB 1121 add the part(EC89) for EMI demand 1128 add EC94,EC95 for EMI demand



1016 add GND1 and GND2 for EMI demand
1017 add GND3 and modify GND2 for EMI demand

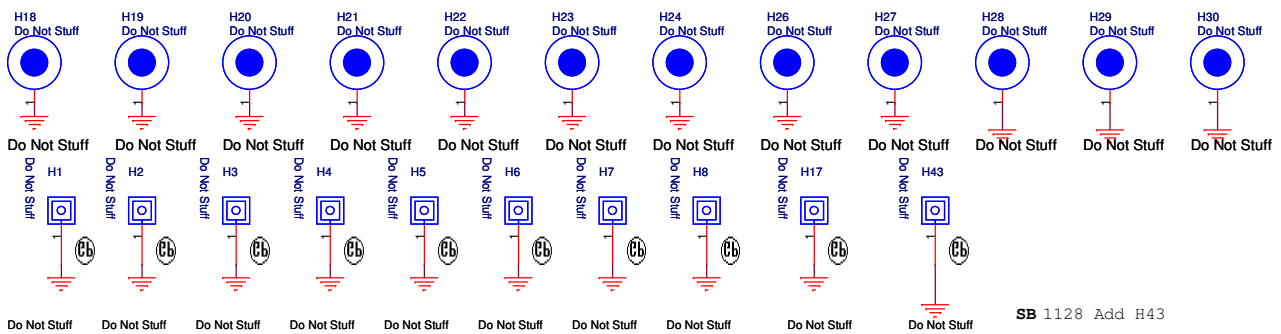


1016 modify H35~H38
1016 delete H9~H12



SB 1128 Add GND4,GND7,GND8

1016 modify H31 and H32
SB 1120 remove H31and H32



SB 1128 Add H43

Speaker



Touch pad



Keyboard

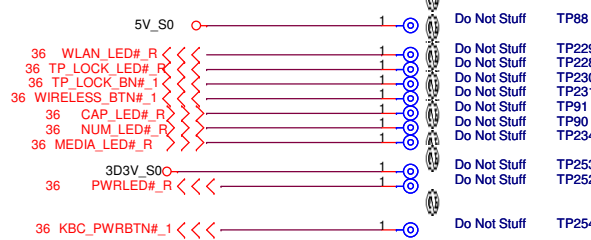


Bluetooth



1017 modify USB signal connection

LED



SB

1112 remove the signal(STDBY_LED#_R)

Battery



Check test point



Test Point放在Dimm Door打開可量測處

FAN



UMA Two Phase 2

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

AFTE test point

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0910 delete F4(Page 18)
0910 update footprint of U15(Page 30)
0910 delete RIGHT1 and LEFT1(Page 33)
0910 modify net names of TP_LEFT and TP_RIGHT(Page 36)
0910 modify test points of AFTE and TPAD
0911 modify net name from LPC_RST to PLT_RST1#(Page 24)
0911 add net name(RBIAS,LED_DUPLEX#,SMDATA,SMCLK) (Page 24)
0911 add net name(DVDD_1_8,ACZ_SDATAIN0_R,FLY_P,FLY_N,VREF_LO,VREF_HI) (Page 26)
0911 add net name(EAPD#_R) (Page 27)
0912 modify the schematic of Page 33
0912 delete GMCH_TXB*(Page 7& 18)
0912 add these parts for EMI demand(page 7,18,20,21,23,26,28,29,30,32,33,34,35)
0915 modify net name from 10M/100M/1G_LED# to 10M/100M_LED#(page24,25)
0915 delete these parts for EMI demand(page 30)
0915 add EC34 for EMI demand(page3)
0915 add EC73 for EMI demand(page 12)
0915 modify LEDs port
0916 move net(SPI_WP#) from U9 pin120 to pin25(page33)
0930 modify BLUE1(page22)
0930 add 2nd for SPK1, MIC1 and modify LOUT1 (page28)
0930 modify FAN1(page32)
0930 modify TPAD1(page35)
0930 modify KB1(page33)
0930 modify net name for BIOS demand(page33)
1001 delete these parts for EMI demand(ED1~8)
1009 modify net name for GND to AGND(page27)
1009 add R4,R5 for AC decoupling(page27)
1009 add R96(page30)
1013 modify TPAD1(page35)
1013 modify U40 from 72.25X16.001 to 72.25X16.A01(page 34)
1013 modify TC11 and add TC12(page42)
1013 modify TC10 and add TC26(page44)
1013 modify U2(page45)
1013 modify U3 and U31(page 46)
1013 modify R161 and R162(page41)
1013 modify card1(page 30)
1014 modify these LEDs(LED11,LED12) (page38)
1014 modify these nets(page 26)
1014 modify R258 from 10k to 20k ohm(page26)
1014 add ER5 for EMI deamnd(page3)
1015 modify LCD1 pin define(page 18)
1015 modify the power from 3D3V_S5 to 5V_S5(page38)
1015 modify TPAD1(page35)
1015 modify RN57(page28)
1015 modify F1(page18)

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1016 modify L1,L2 and L3(page 19)
1016 modify XF1(page 25)
1016 modify RN53 and U10(page 24)
1016 modify U8(page19,47)
1016 modify U4(page 37)
1016 modify U23(page 43)
1016 modify X2(page12)
1016 modify X1(page 33)
1016 modify X3(page 3)
1016 modify D13(page 46)
1016 modify D23(page 20)
1016 modify D9(page 39)
1016 modify D4(page 19)
1016 modify Q3 and Q4(page45)
1016 modify Q18(page 36)
1016 modify Q15~Q17(page 36)
1016 modify Q27~Q30(page38)
1016 modify Q6 and Q14(page 32)
1016 modify Q8(PAGE 24)
1016 add GND1 nad GND2 for EMI demand(page 47)
1016 modify LCD1 pin define(page 18)
1016 delete H9~H12 and modify H35~H38,H31,H32(page 47)
1017 add these parts for EMI demand(page 47)
1017 delete these parts(EC208~EC210) (page 7)
1017 modify BLUE1(page 22)
1017 modify FAN1(page 32)
1017 modify R291 and R293(page 38)
1017 add U61,R52,EC23 and EC24(page 37)
1017 modify RN60(page37)
1017 add TC25(page 44)
1017 add GND3 and modify GND2 for EMI demand(page 47)
1017 modify USB signal connection(page13,18,22,23,30,31,48)
1020 delete C537 for Power demand(page42)
1020 add the part(EC86) for EMI demand(page 47)
1020 delete U61,R52,EC24 and EC23(page 37)
1020 delete TC14,TC15(page 47)
1021 modify TC16(page 31)
1021 delete TC23(page 23)
1021 modify TC5(page 20)
1021 modify and swap these parts(USB1 and USB2) (page 23)
1021 modify SATA1(page 20)
1022 modify DC1(page 45)

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SA to SB

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1127 modify C377(page32) for thermal function
1128 Add H43,GND4,GND7,GND8(page47) for EMI demand
1128 modify LCD1(page18) for cost down
1128 Add L19(page24) for vender demand
1128 add EC94,EC95 for EMI demand(page47)
r demand

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