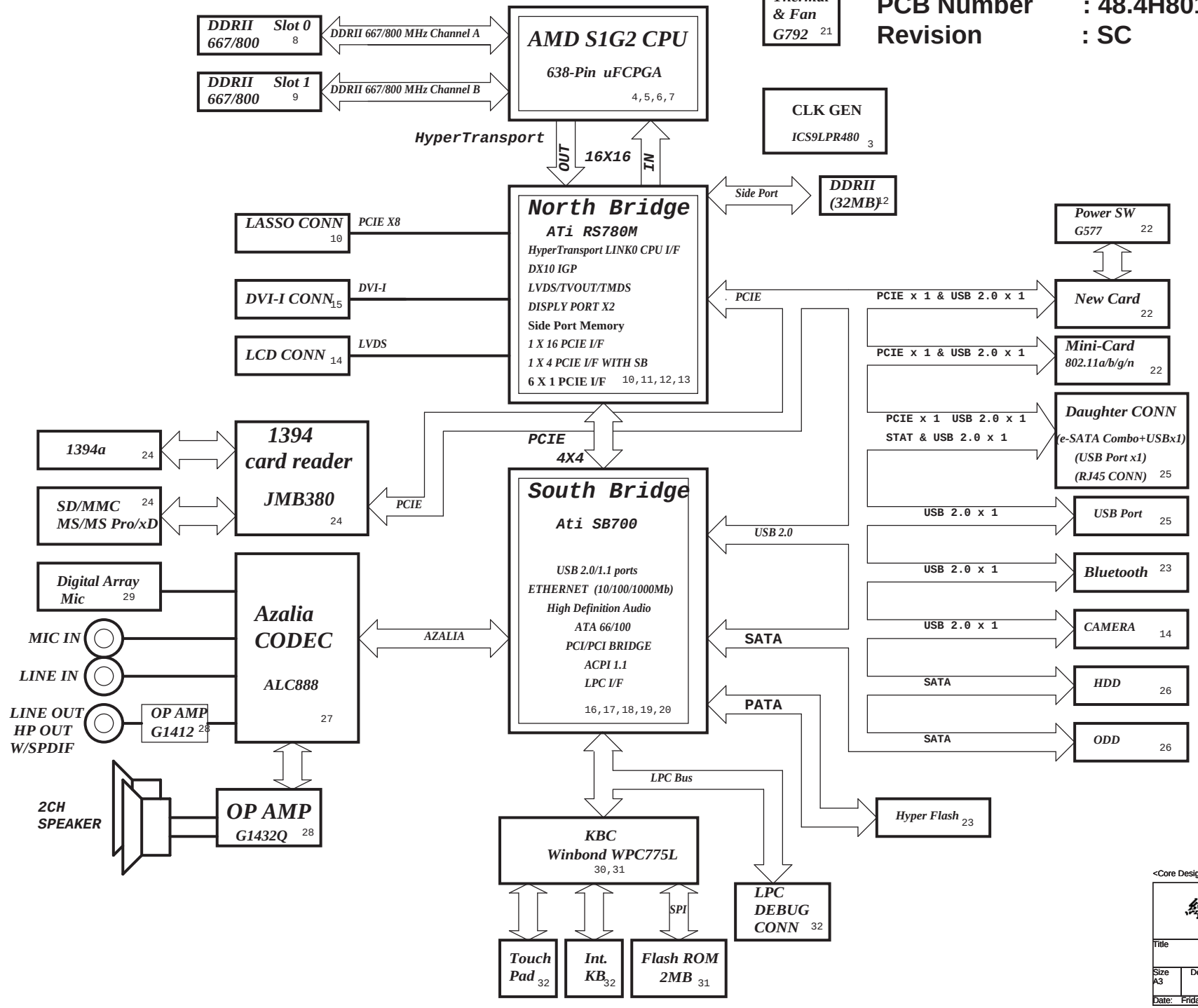
S13 Block Diagram

Project code : 91.4H801.001
PCB Number : 48.4H801.0SC
Revision : SC



CPU V_CORE	ISL6265	34,35
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	

SYSTEM DC/DC	TPS51124	37
INPUTS	OUTPUTS	
DCBATOUT	1D8V_S3 1D2V_S0	

SYSTEM DC/DC	TPS51125	36
INPUTS	OUTPUTS	
DCBATOUT	5V_S5 3D3V_S5	

SYSTEM DC/DC	LDO	39
INPUTS	OUTPUTS	
5V_S5 3D3V_S0	0D9V_S3 1D5V_S0	

SYSTEM DC/DC	LDO	39
INPUTS	OUTPUTS	
3D3V_S5 3D3V_S0	1D2V_S5 2D5V_S0	

SYSTEM DC/DC	TPS51125	36
INPUTS	OUTPUTS	
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5	

MAXIM CHARGER	BQ24745	41
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: System Block Diagram

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 1 of 44

		USB PORT#	DESTINATION
SB700	2.0	0	USB1
		1	CAMERA
		2	Combo(ESATA/USB)
		3	NEW CARD
		4	USB2
		5	Bluetooth
		6	NC
		7	WLAN
		8	NC
		9	NC
		10	NC
		11	NC
	1.1	12	NC
		13	NC

PCI EXPRESS	DESTINATION
Lane 0	NEW CARD
Lane 1	WLAN
Lane 2	LAN
Lane 3	CARD READER&1394
Lane 4	NC
Lane 5	NC

RS780M Functional Strap Definitions

STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC)
0 : Enable * 1 : Disable

RS780: Enables Side port memory (RS780 use HSYNC)

* 0 : Enable 1 : Disable

SUS_STAT#

Selects Loading of STRAPS From EEPROM
* 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

SB700 Functional Strap Definitions

		PULL HIGH	PULL LOW
CLK_PCI_2	WatchDOG (NB_PWRGD)	ENABLED	DISABLED DEFAULT
CLK_PCI_3	DEBUG STRAPS	USB	IGNORE DEFAULT
CLK_PCI_1 CLK_PCI_4	RESERVED		
LPCCLK0	PCI MEM BOOT	ENABLED	DISABLED DEFAULT
LPCCLK1	INTERNAL CLK GEN	ENABLED	DISABLED DEFAULT
RTCCLK	INTERNAL RTC	ENABLED DEFAULT	DISABLED
AZ_RST#	IMC	ENABLED	DISABLED DEFAULT
SB_GPO17 SB_GPO16	ROM TYPE	H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	

<Core Design>

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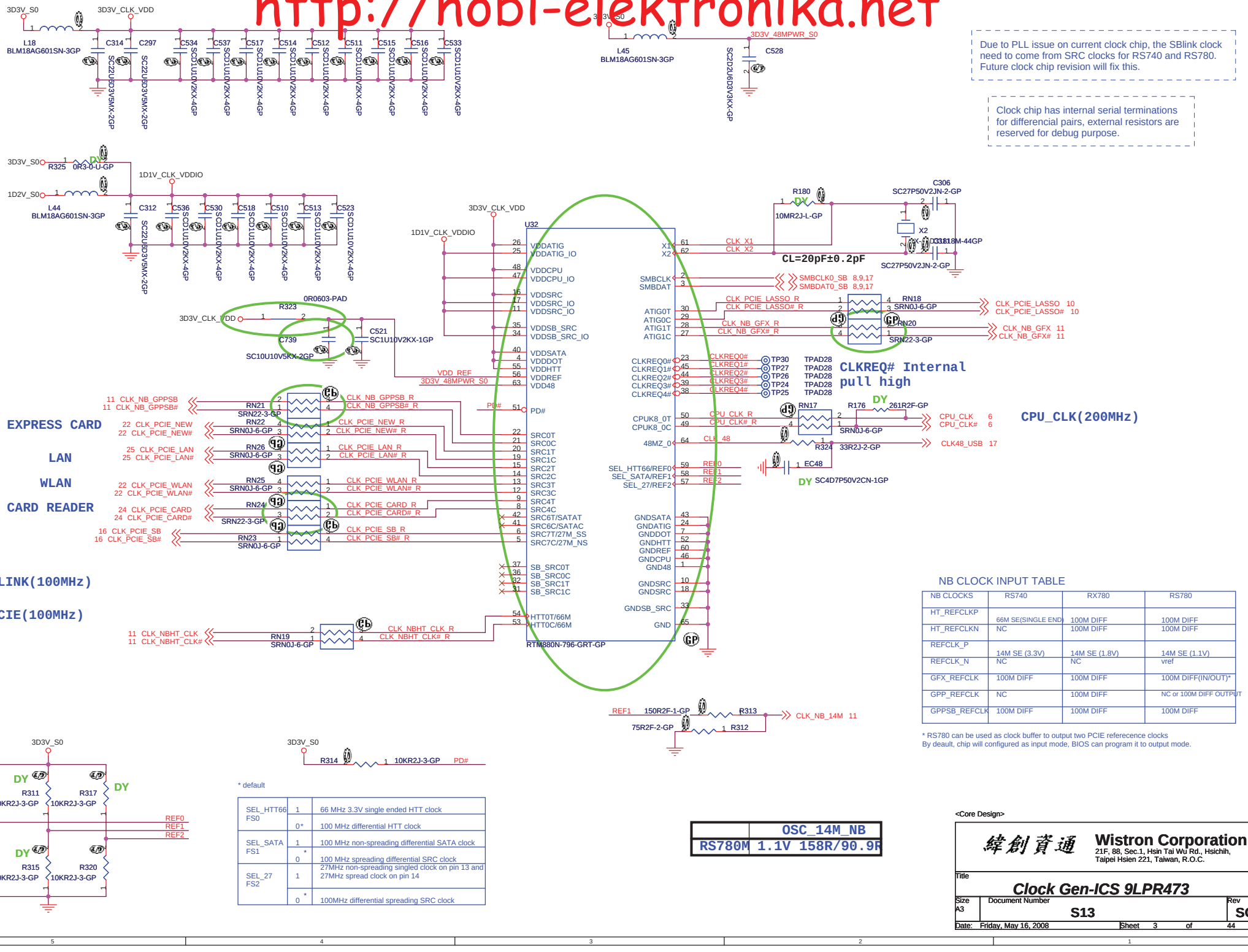
Title: Table of Content

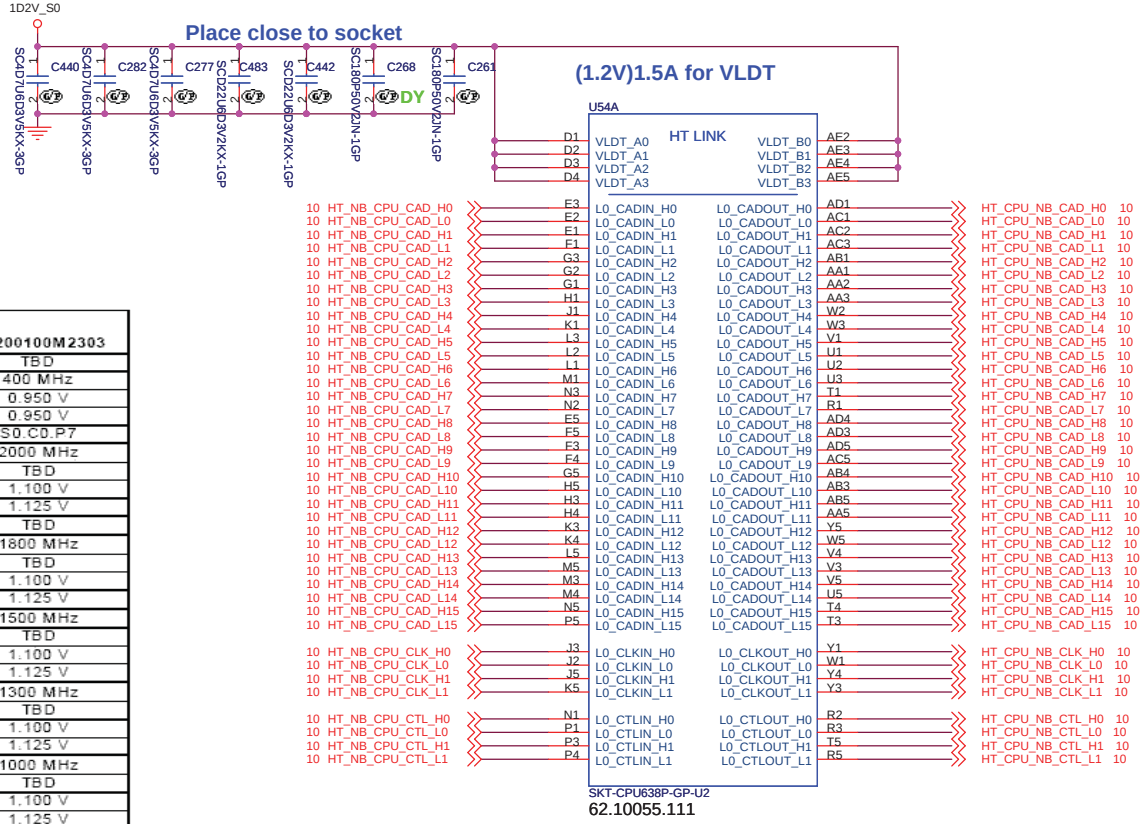
Size: A3 | Document Number: S13 | Rev: SC

Date: Friday, May 16, 2008 | Sheet 2 of 44



NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66 FS0	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA FS1	1	100 MHz non-spreading differential SATA clock
	0*	100 MHz spreading differential SRC clock
SEL_27 FS2	1	27MHz non-spreading singled clock on pin 13 and 27MHz spread clock on pin 14
	0*	100MHz differential spreading SRC clock



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

緯創資通 Wistron Corporation
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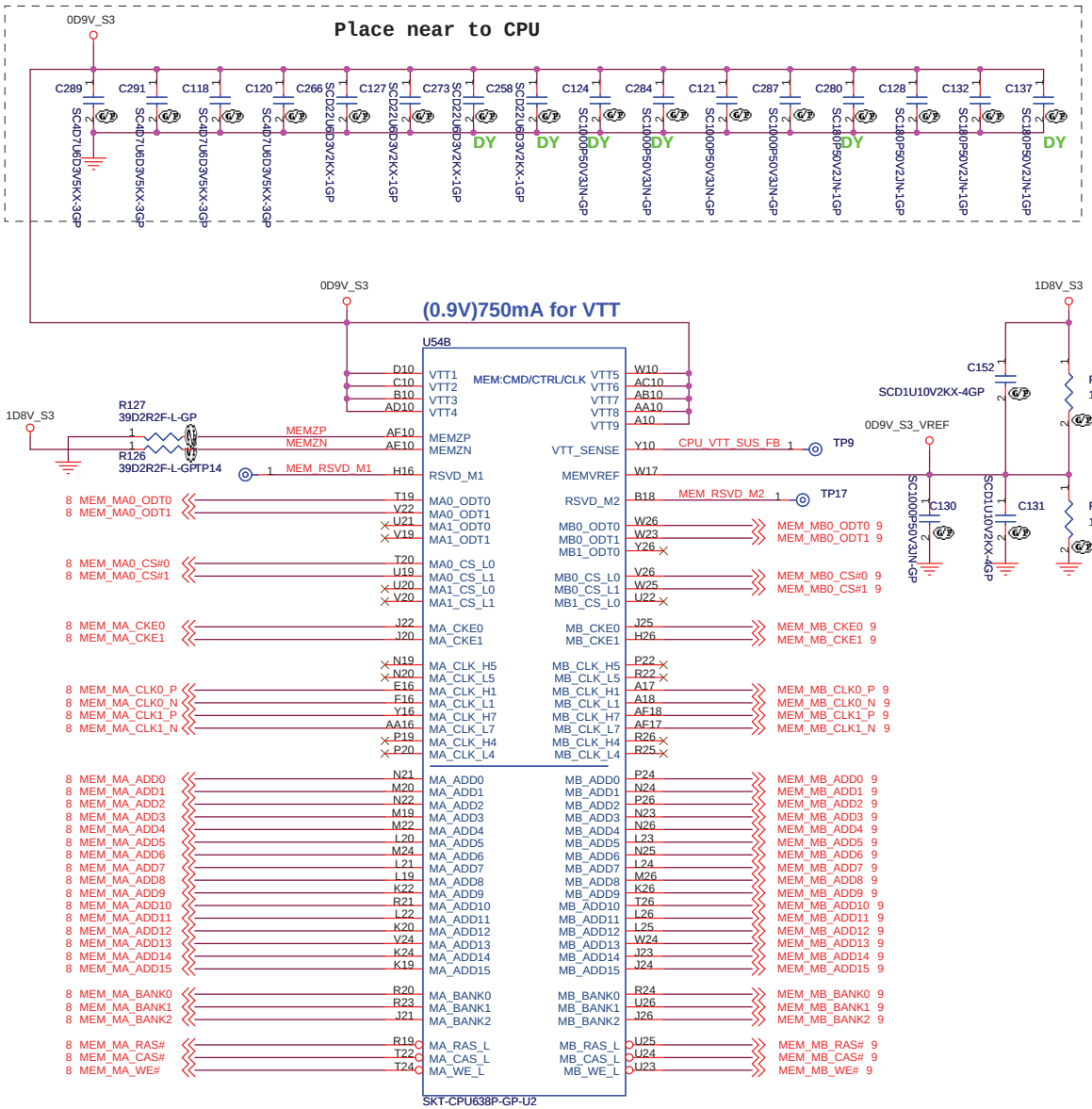
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_HT_LINK I/F_(1/4)

Size: A3 | Document Number: S13 | Rev: SC

Date: Friday, May 16, 2008 | Sheet 4 of 44



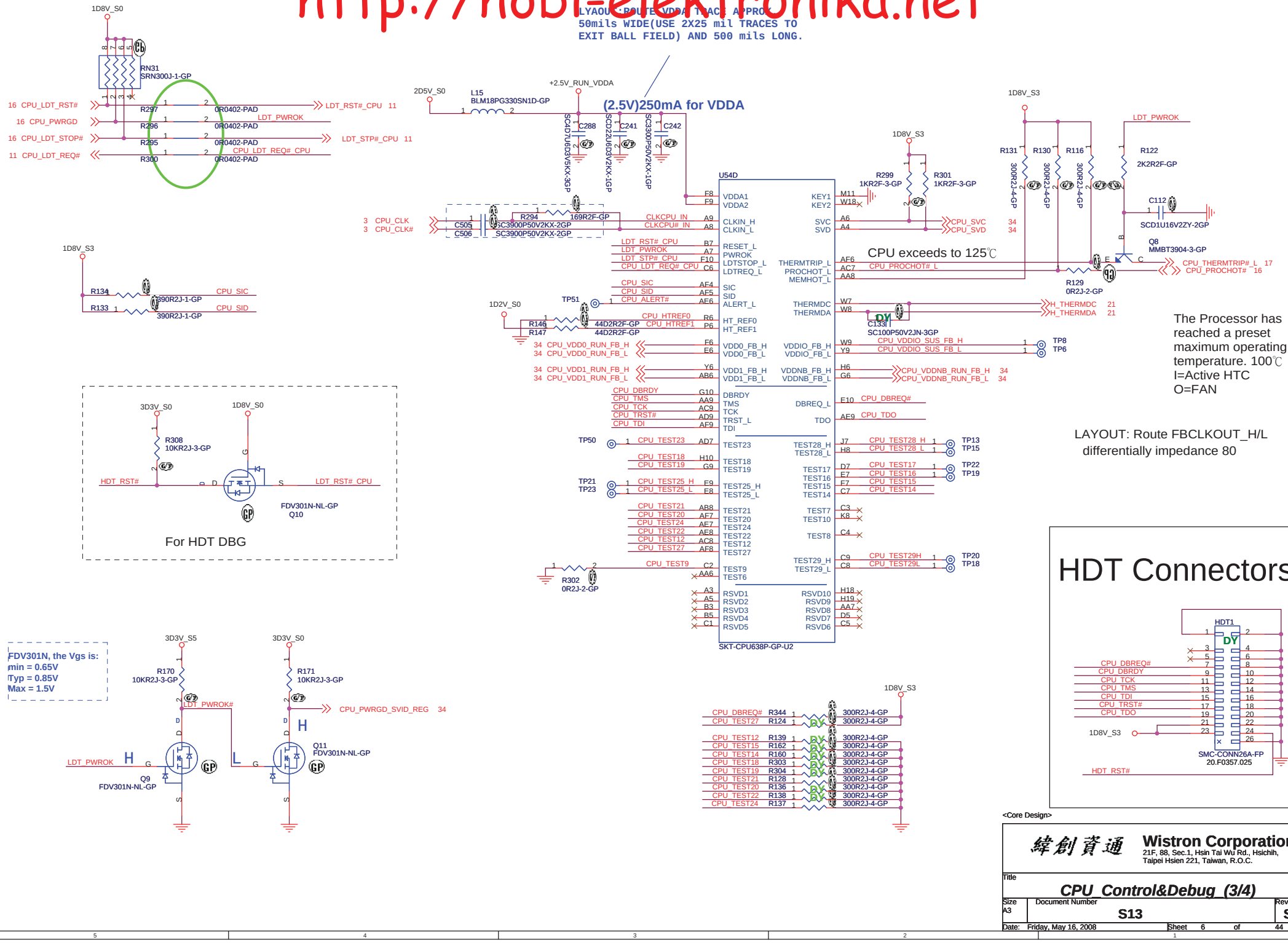
<Core Design>

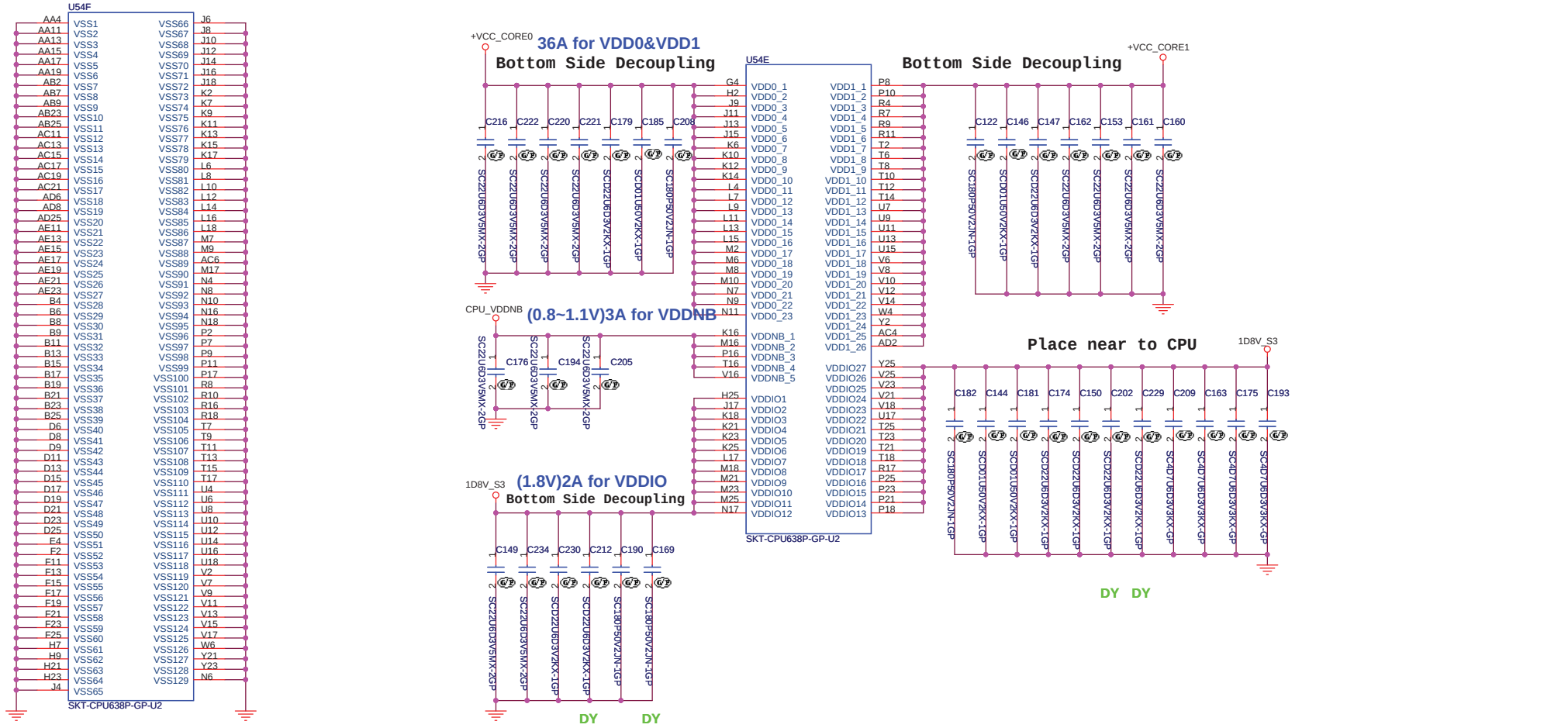
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 5 of 44





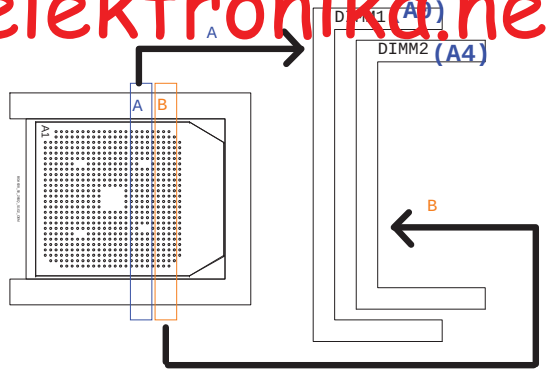
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Power_(4/4)

Size: A3 | Document Number: S13 | Rev: SC

Date: Friday, May 16, 2008 | Sheet 7 of 44



CN10

REVERSE TYPE

DDR2-200P-22-GP-U2

(A0)

Decoupling Capacitor

Place these Caps near DM1

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT

DY

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

Do not share the Term resistor between the DDR addess and Control Signals.

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

DDR_VREF

LAYOUT: Locate close to DIMM

Place C2.2uF and 0.1uF < 500mils from DDR connector

HI 9.2mm

<Core Design>

Wistron Corporation
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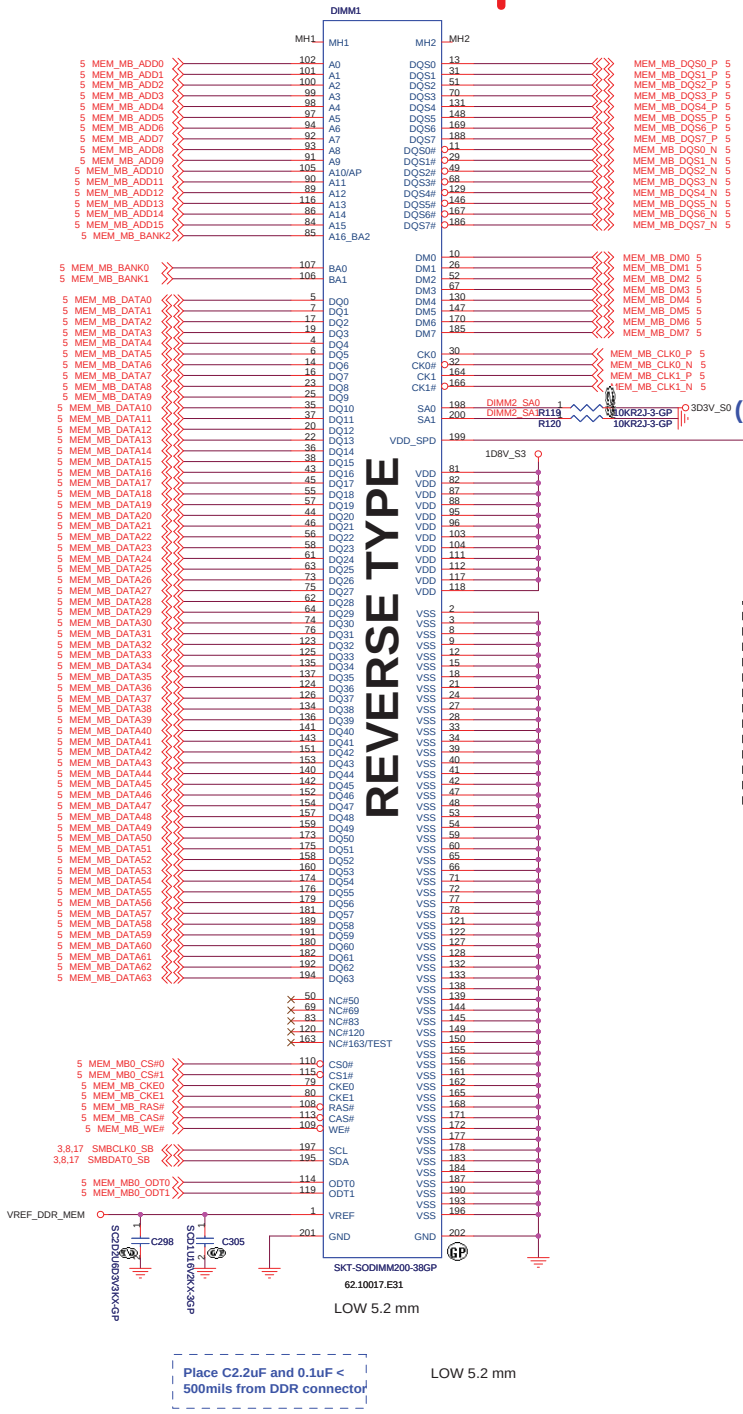
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_DIMM1

Size: Custom | Document Number: S13 | Rev: SC

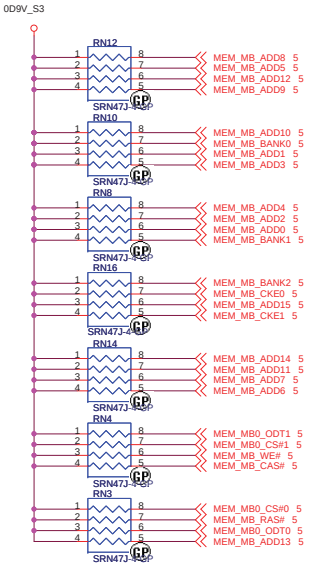
Date: Friday, May 16, 2008 | Sheet 8 of 44

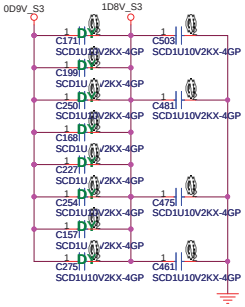


PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

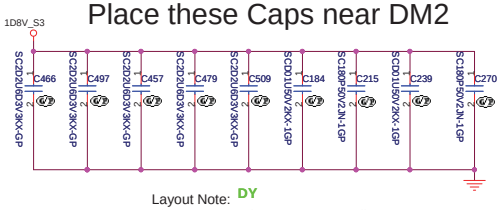
Do not share the Term resistor between the DDR addess and Control Signals.



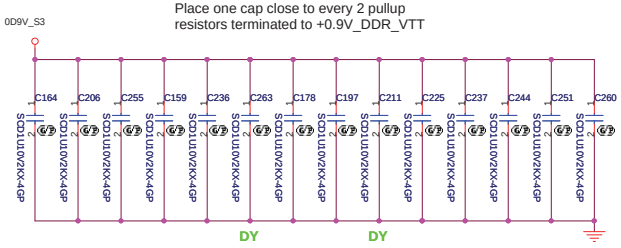


Decoupling Capacitor

Place these Caps near DM2



Layout Note: DY
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



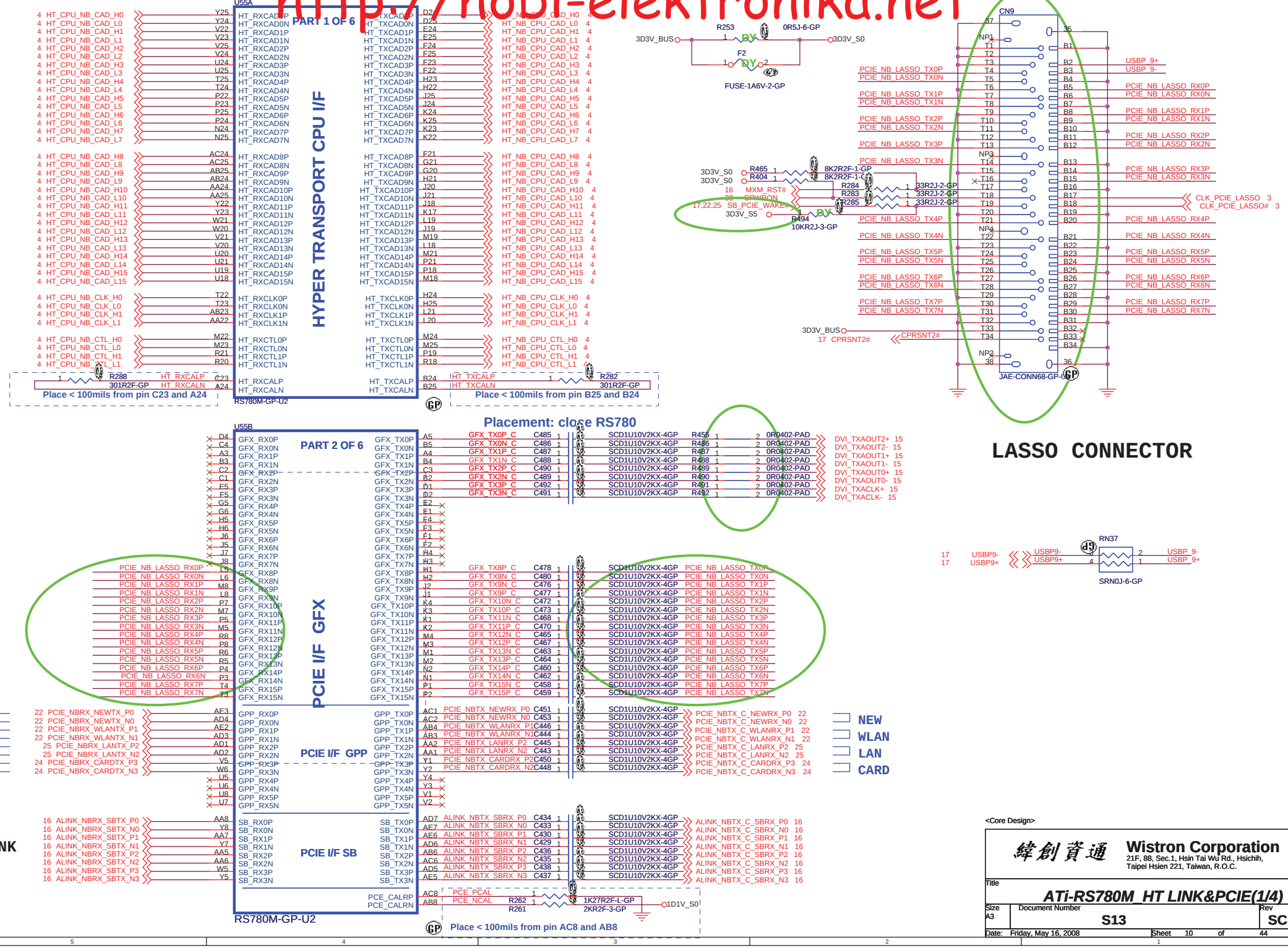
<Core Design>

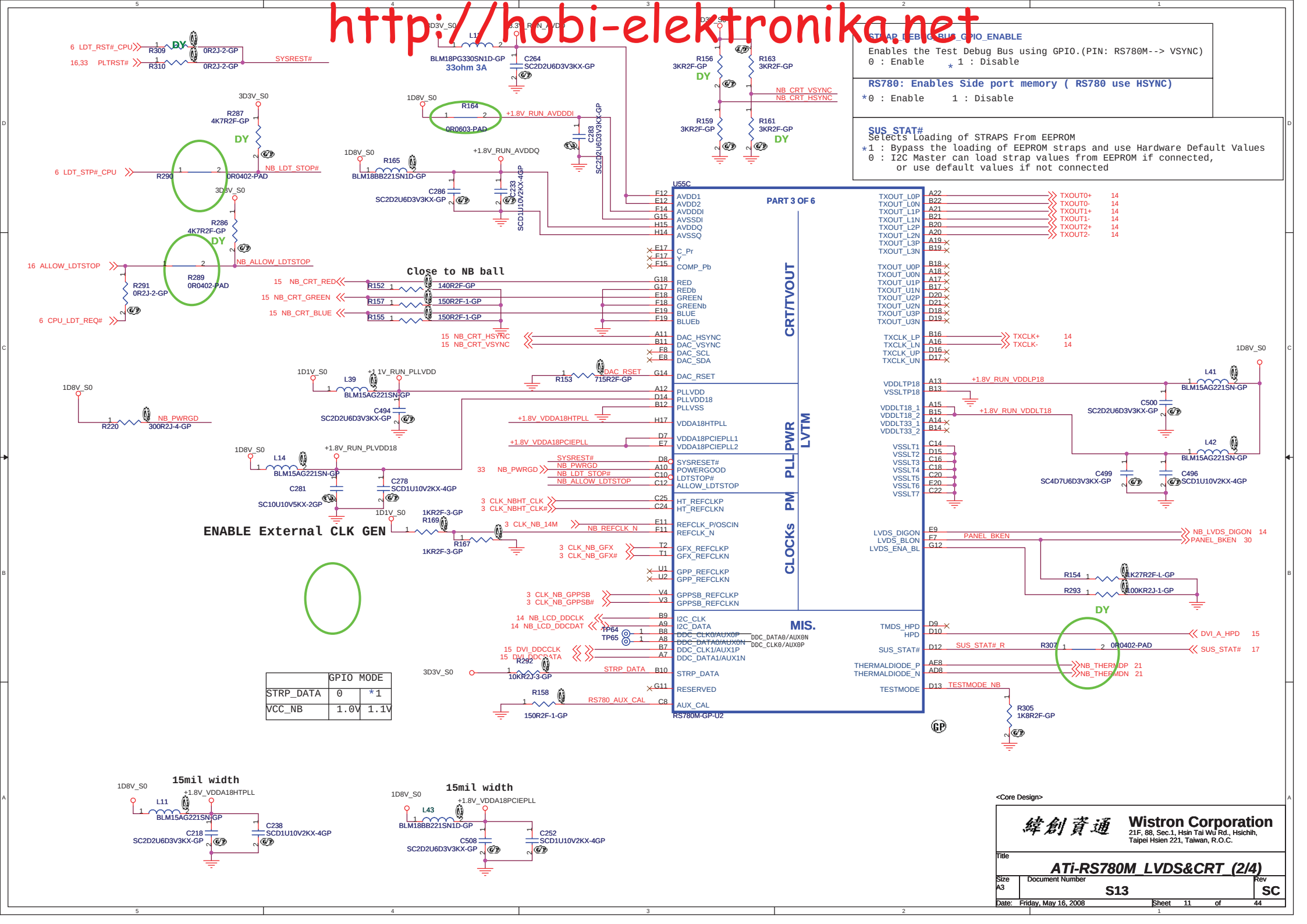
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

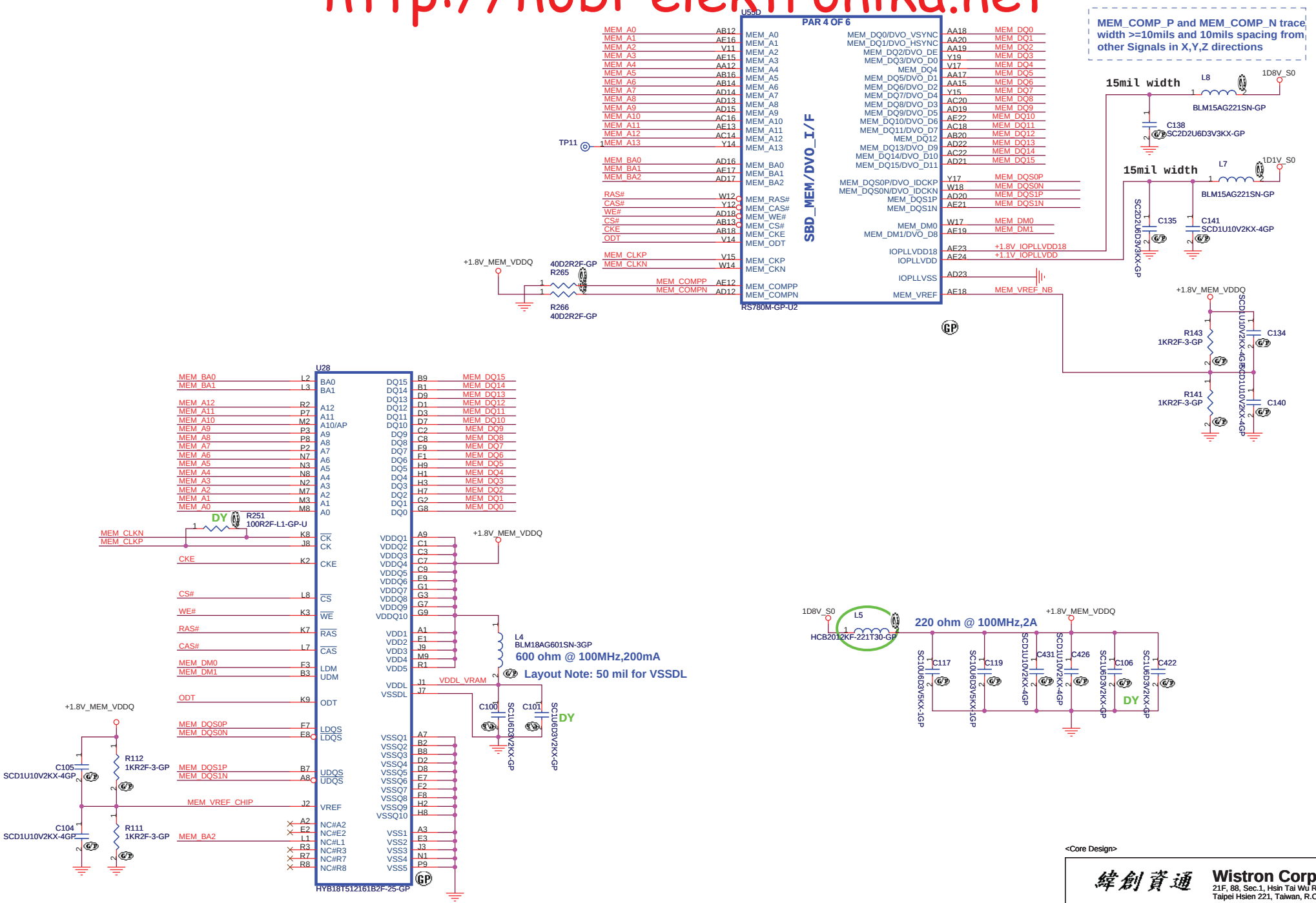
Title: DDR_DIMM2

Size	Document Number	Rev
Custom	S13	SC

Date: Friday, May 16, 2008 Sheet 9 of 44

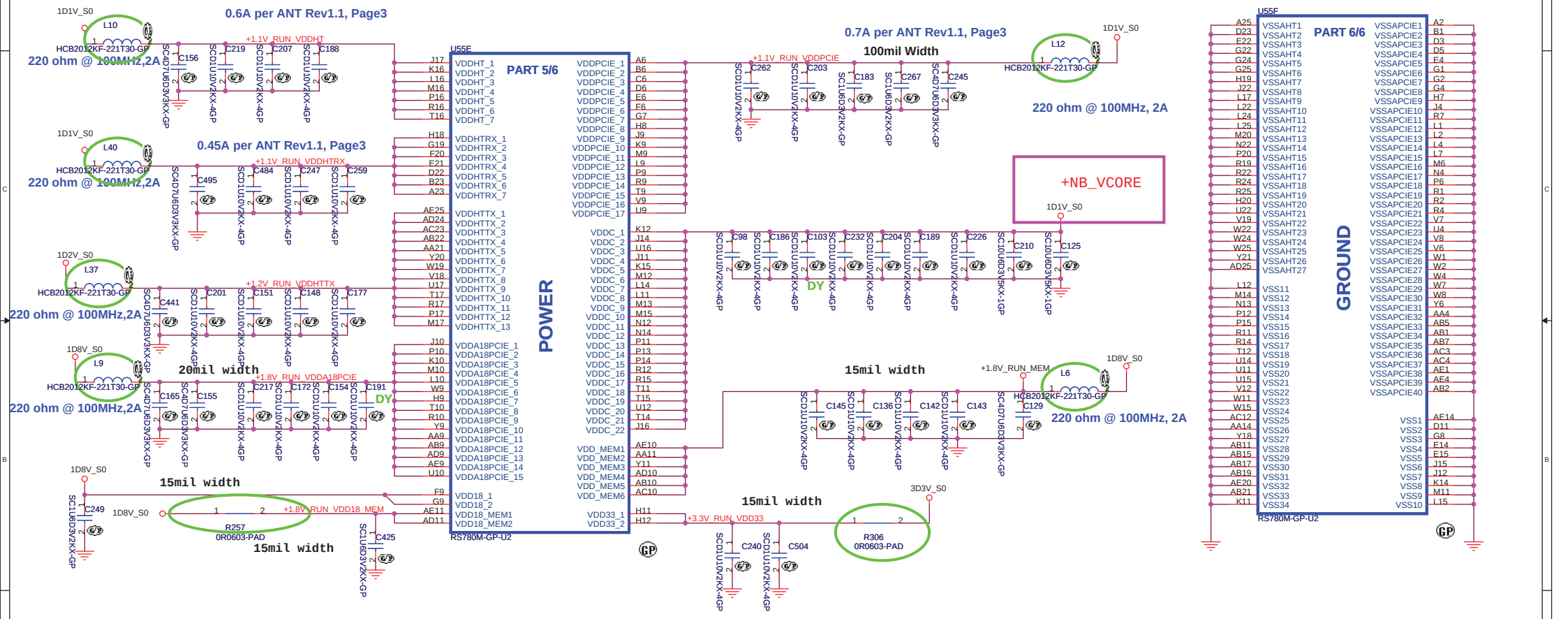






<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***ATi-RS780M_SidePort_(3/4)***
Size: A3	Document Number: **S13** — Rev: **SC**
Date: Friday, May 16, 2008	Sheet 12 of 44



<Core Design>

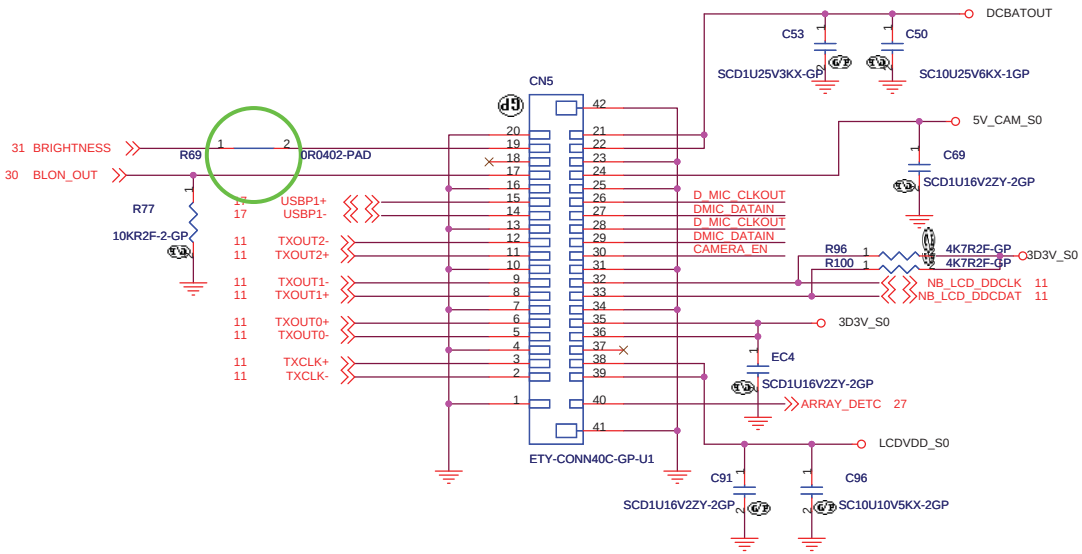
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_PWR&GD_(4/4)

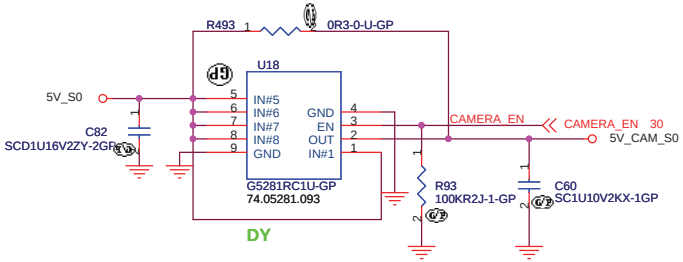
Size	Document Number	Rev
A3	S13	SC

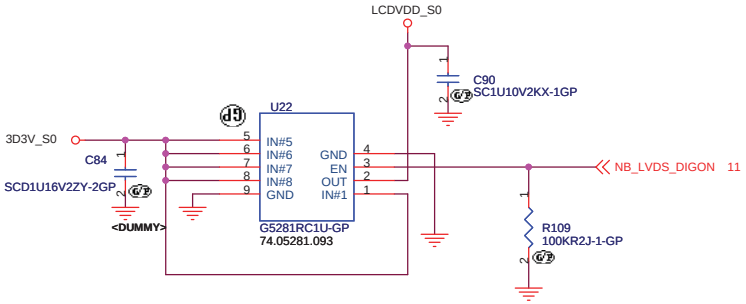
Date: Friday, May 16, 2008 Sheet 13 of 44

LCD CONNECTOR

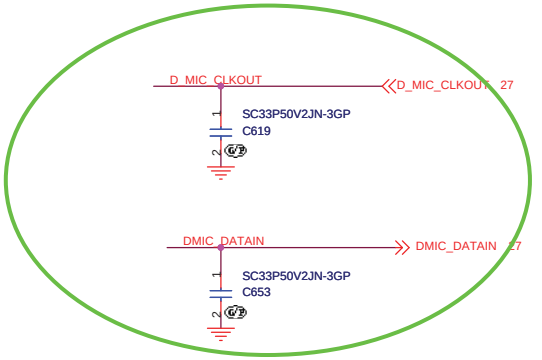


CAMERA POWER





TOP VIEW



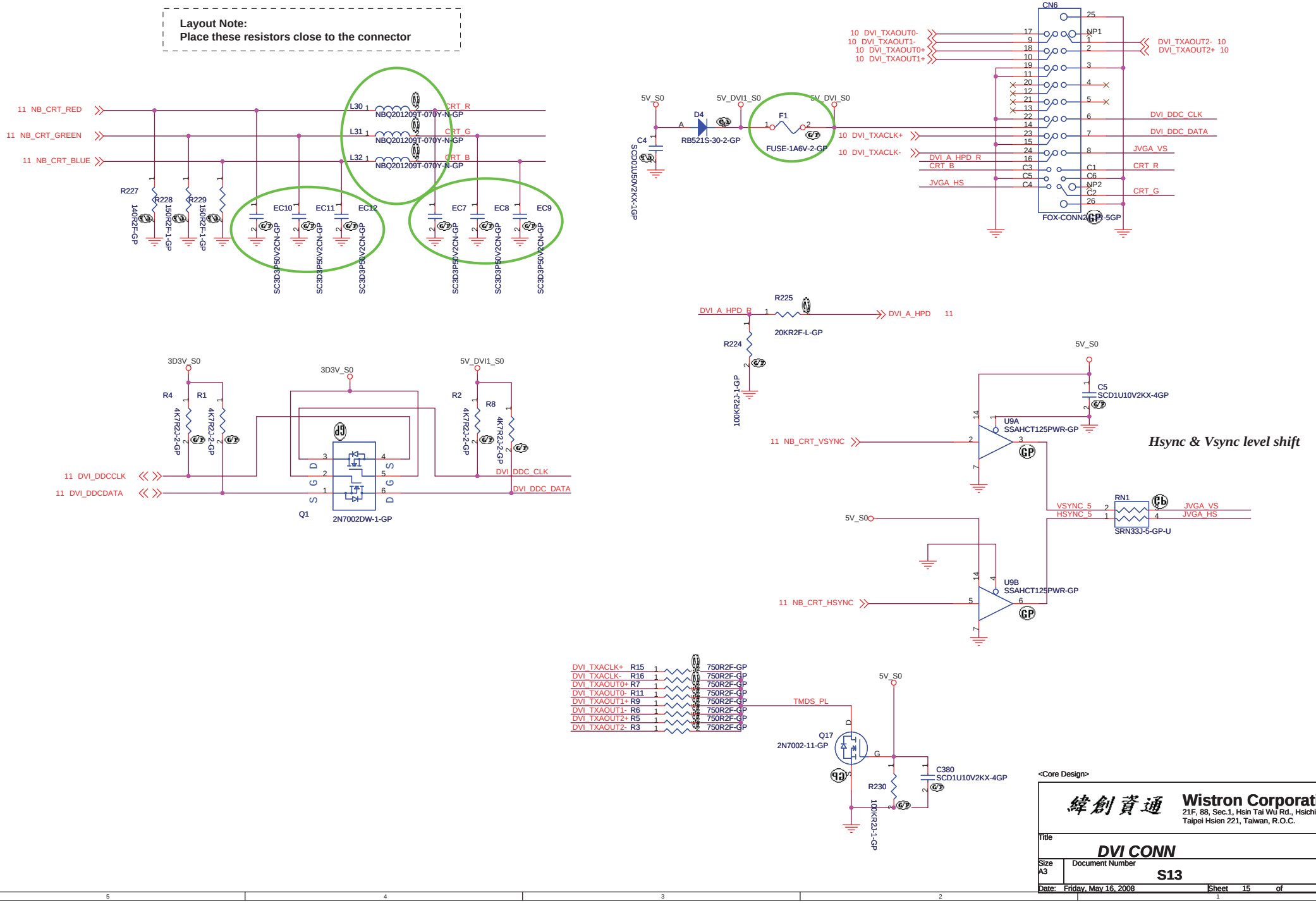
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN/CAMERA

Size: A3 | Document Number: S13 | Rev: SC

Date: Friday, May 16, 2008 | Sheet 14 of 44



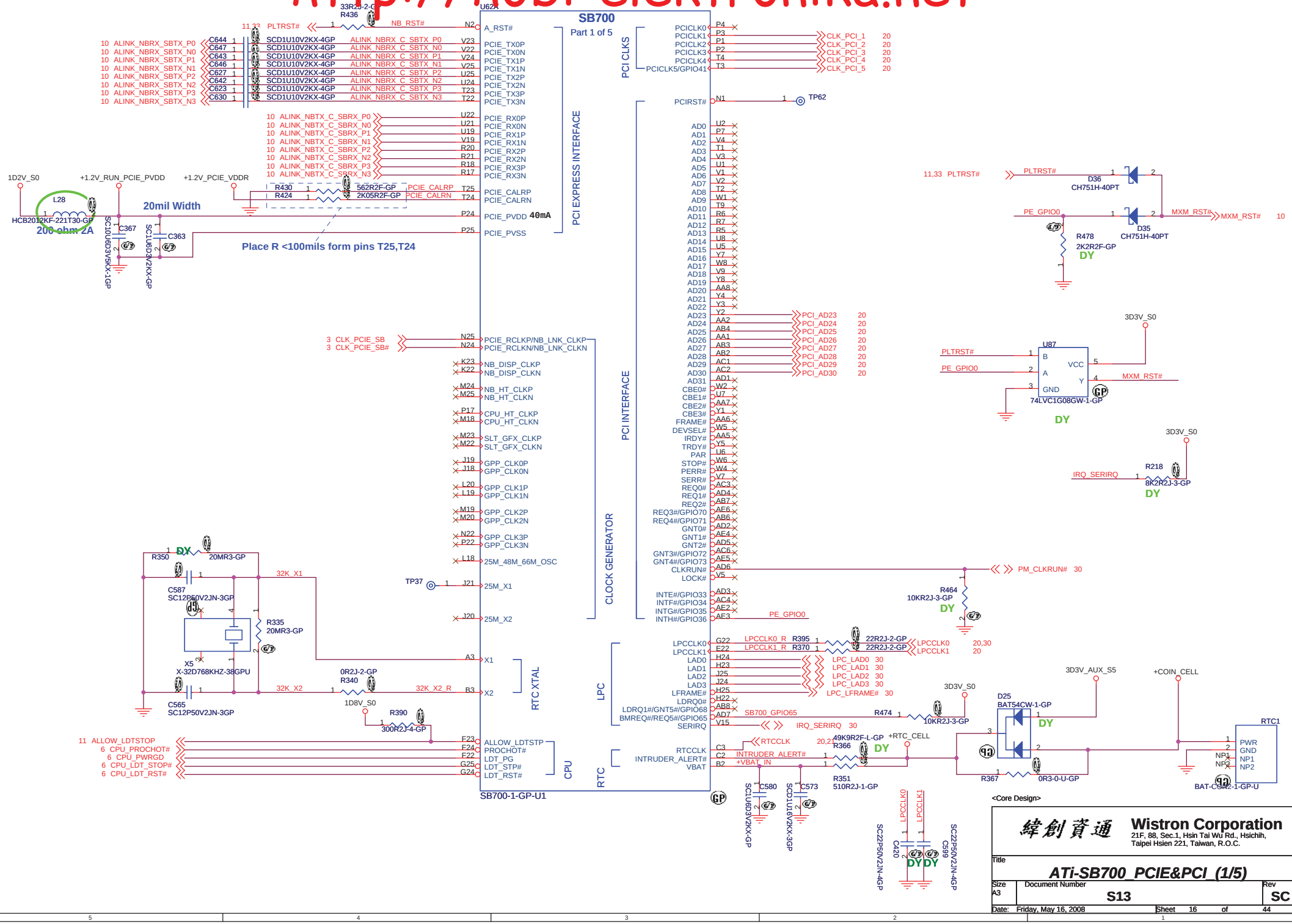
<Core Design>

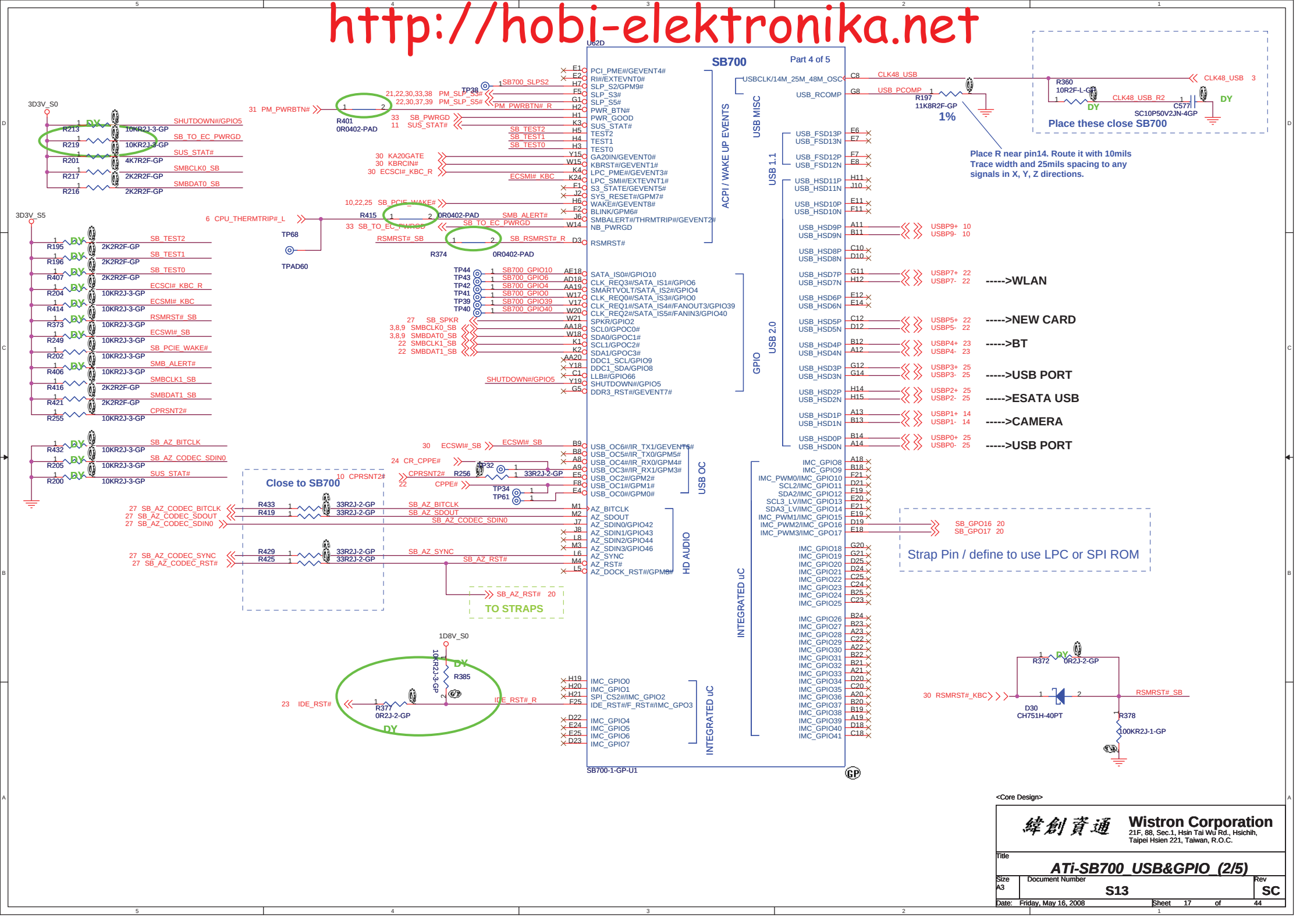
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

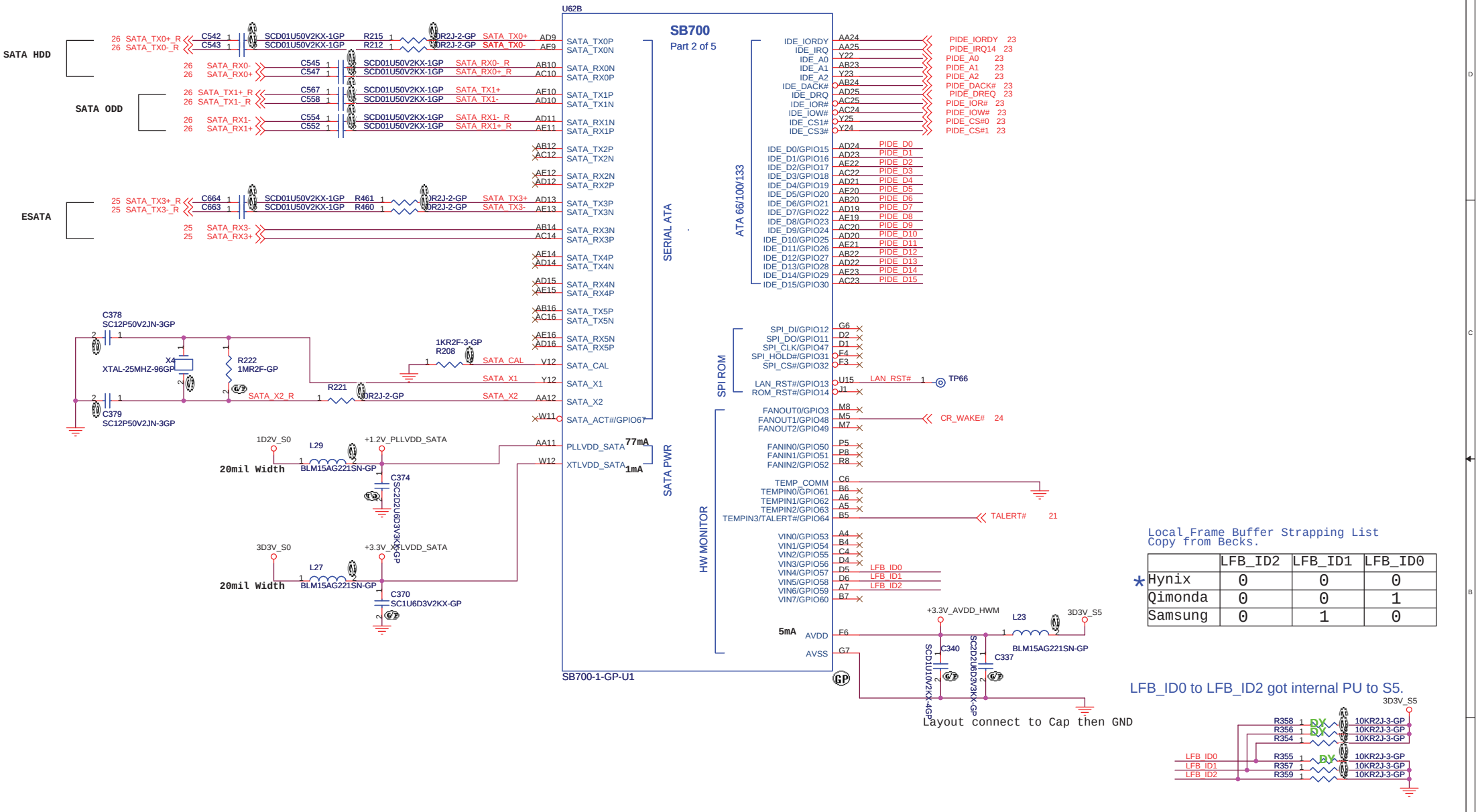
Title: **DVI CONN**

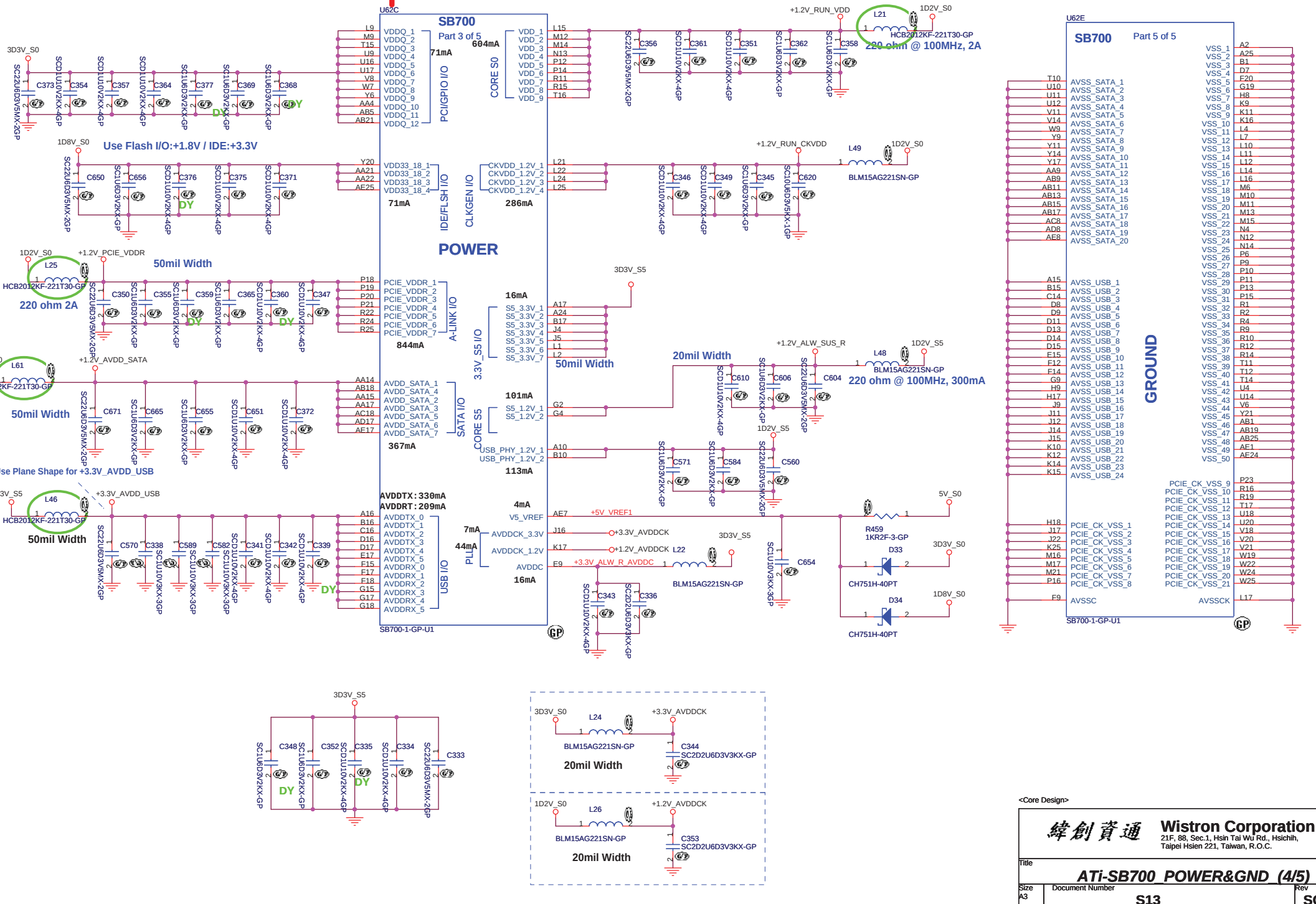
Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 15 of 44









<Core Design>

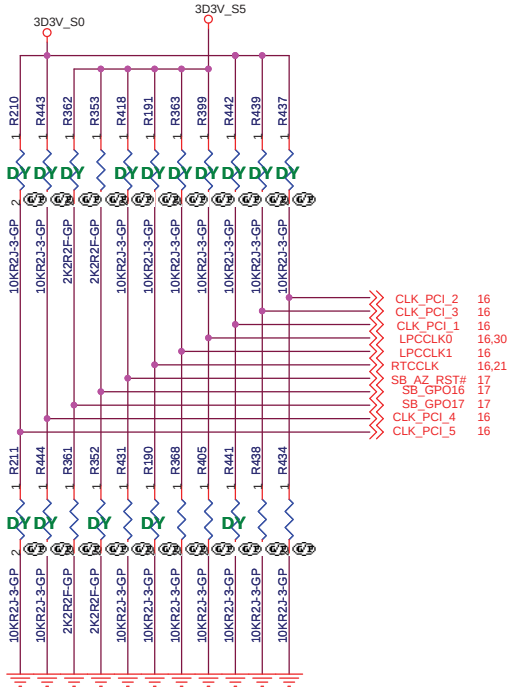
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_POWER&GND_(4/5)

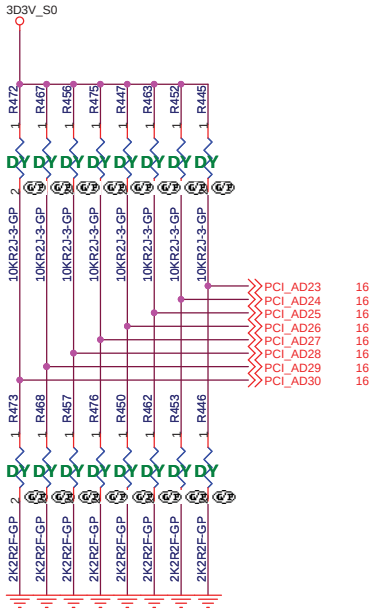
Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 19 of 44

REQUIRED STRAPS



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

	CLK_PCI_2	CLK_PCI_3	CLK_PCI_4 CLK_PCI_5	LPCCLK0	LPCCLK1	RTCCLK	AZ_RST#	SB_GPO17 , SBGPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	IMC DISABLED DEFAULT	

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

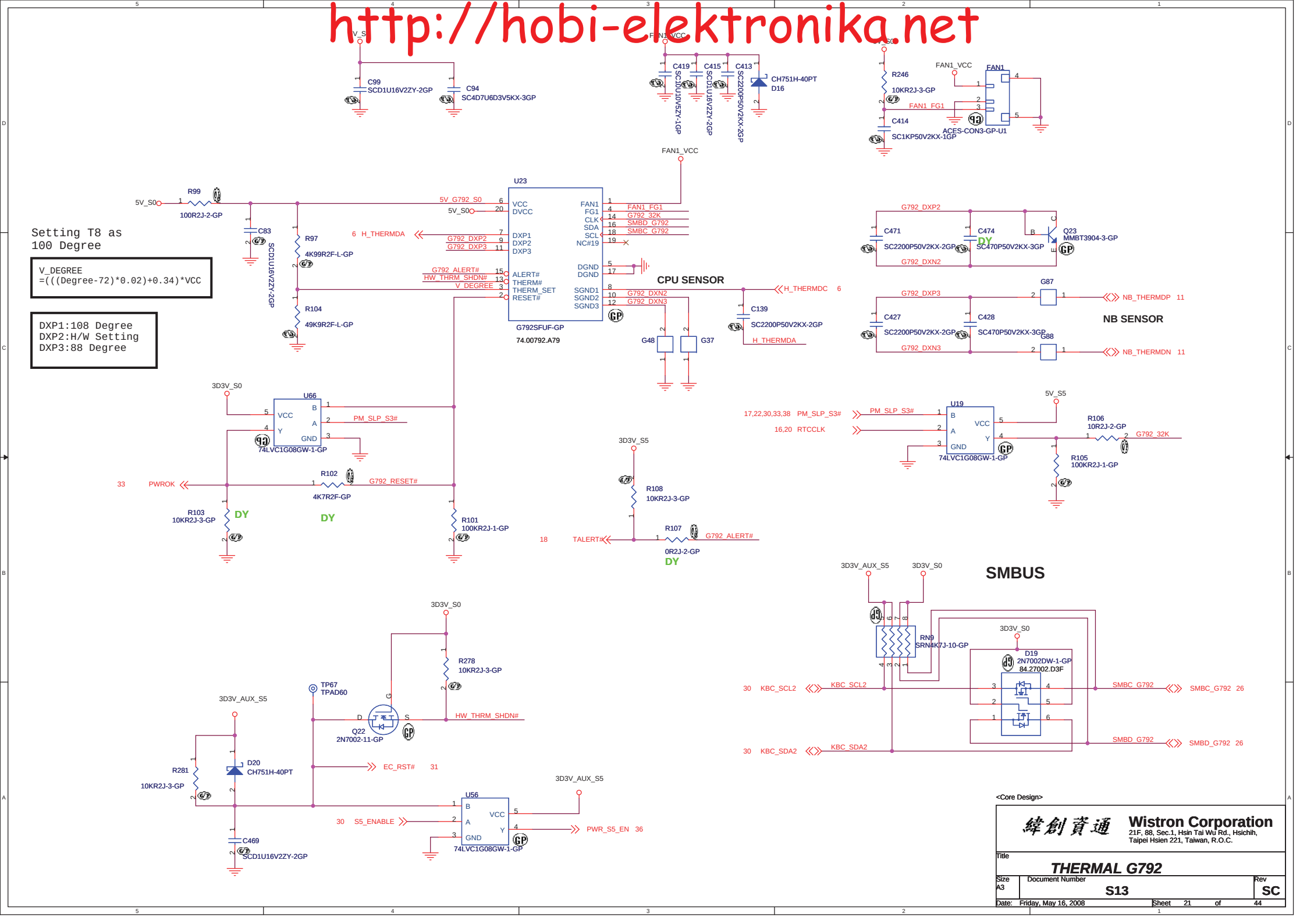
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: S13 | Rev: SC

Date: Friday, May 16, 2008 | Sheet 20 of 44



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

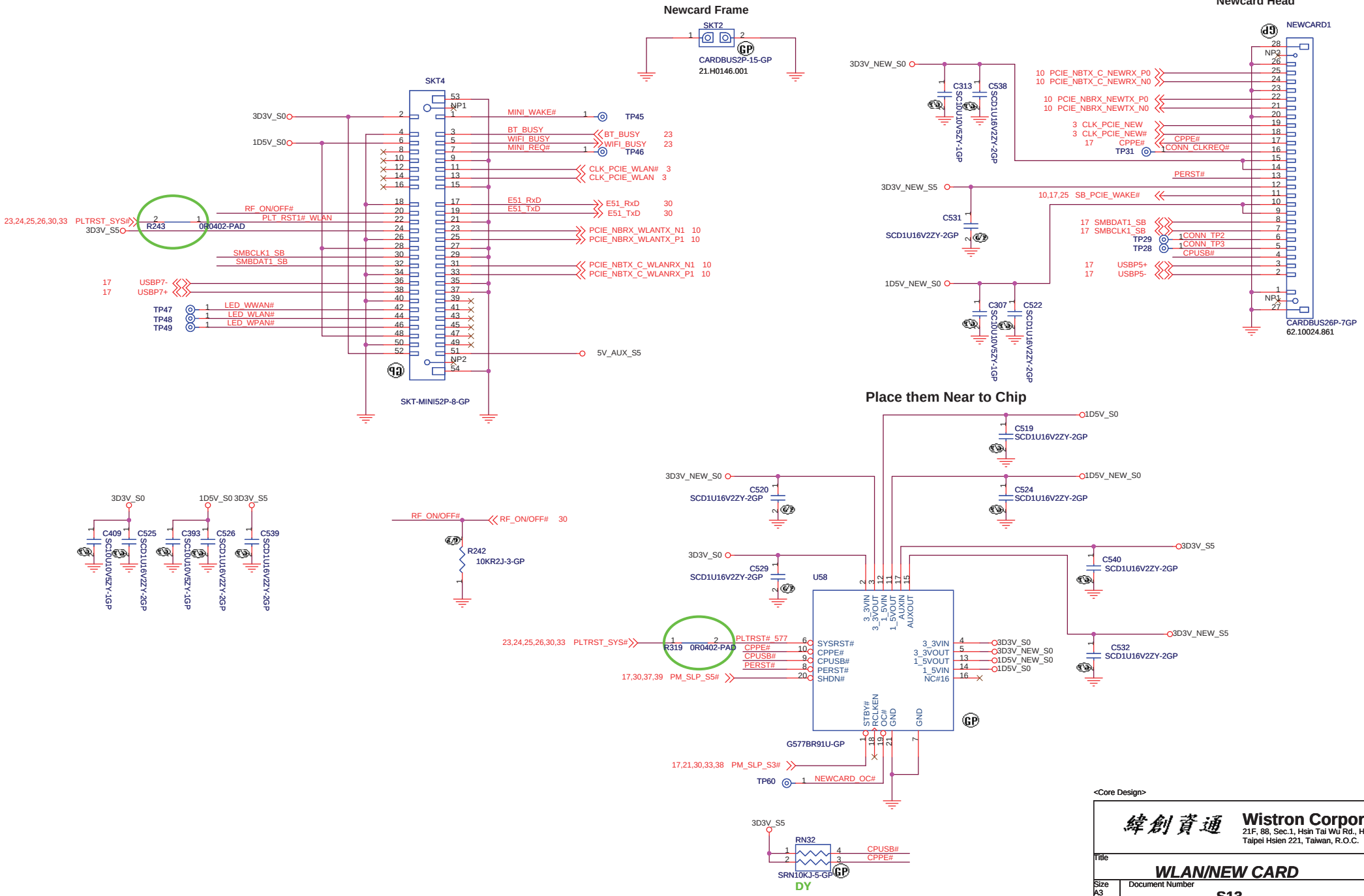
Title: **THERMAL G792**

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 21 of 44

NEWCARD Connector

WLAN Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

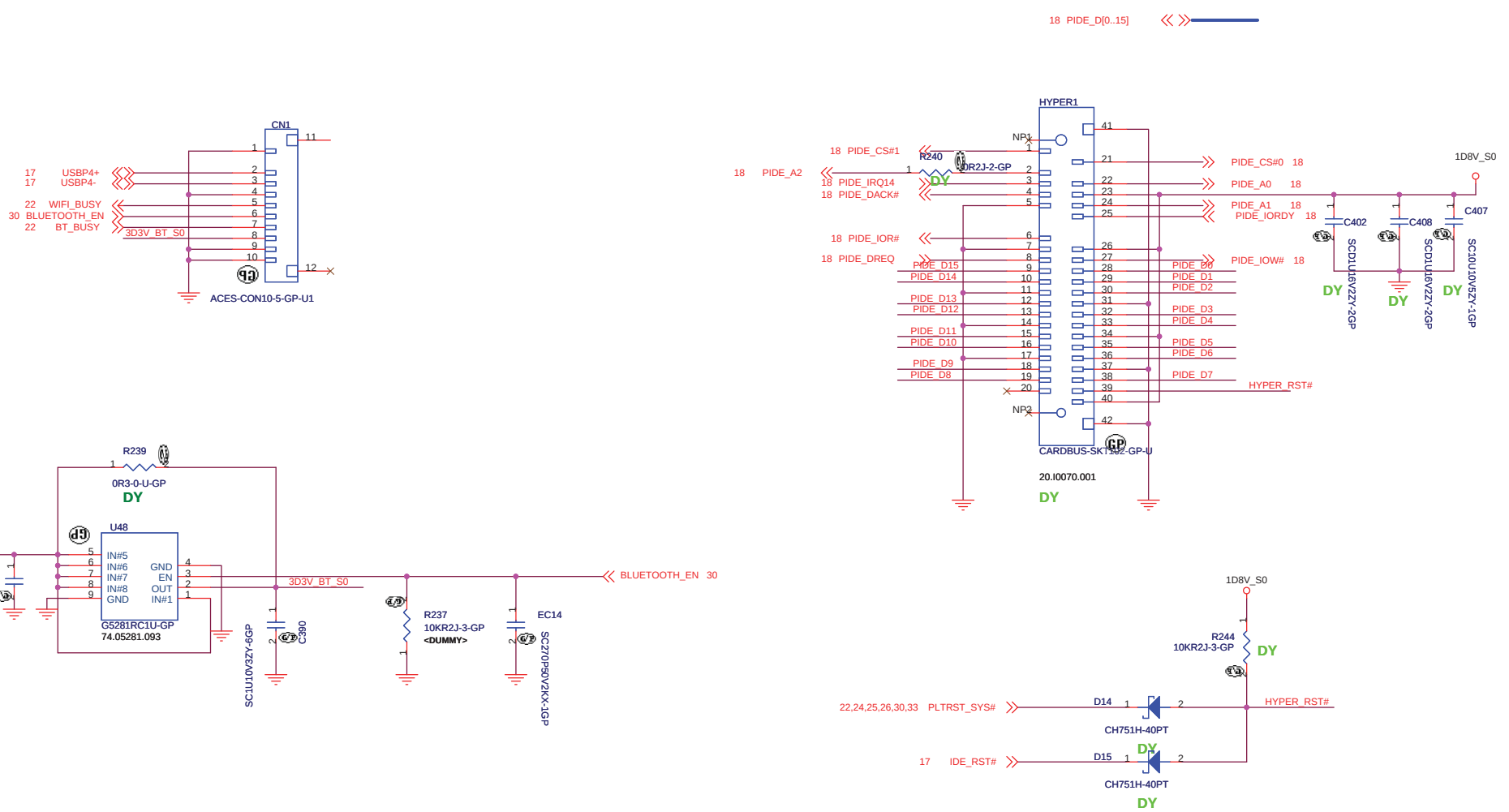
Title: WLAN/NEW CARD

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 22 of 44

Bluetooth

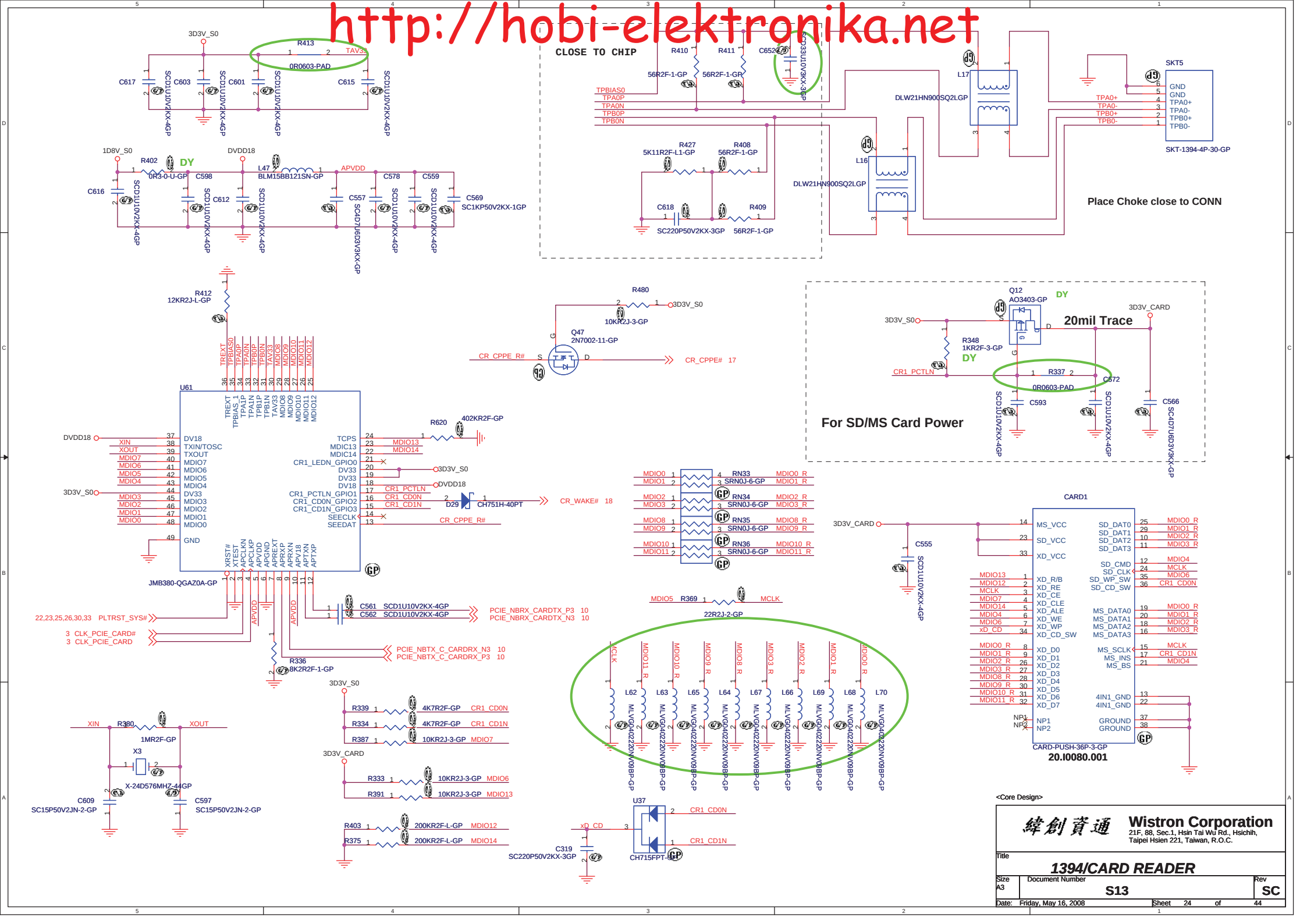
HYPER FLASH



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HYPER FLASH/BT***	
Size A3	Document Number **S13**	Rev **SC**
Date: Friday, May 16, 2008	Sheet 23 of 44	

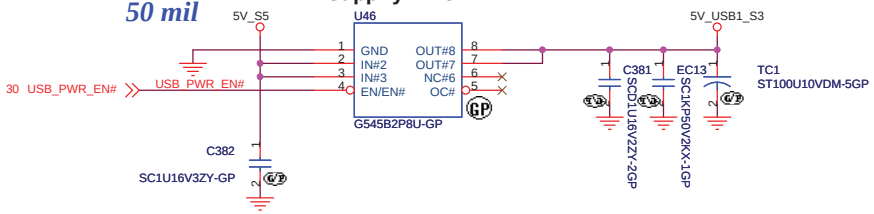


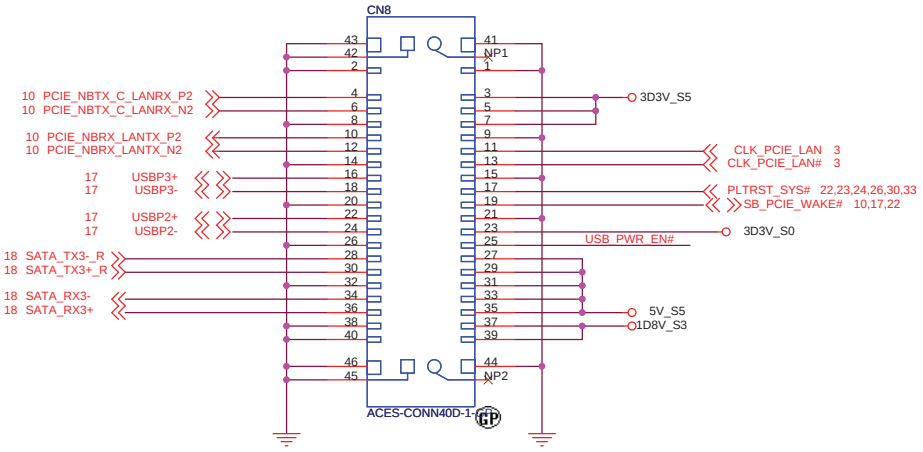
USB PORT

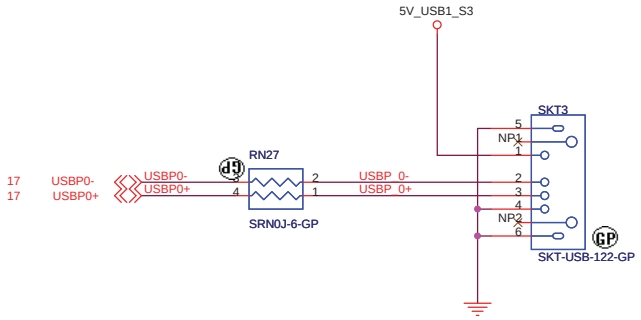
50 mil

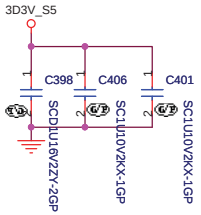
400uS rise time
Supply 1.5~1.1A

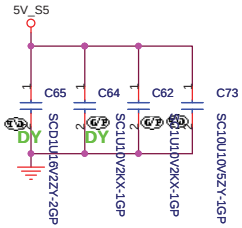
50 mil

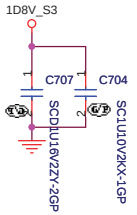


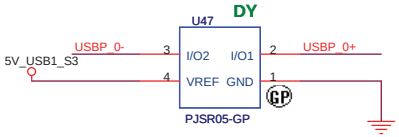








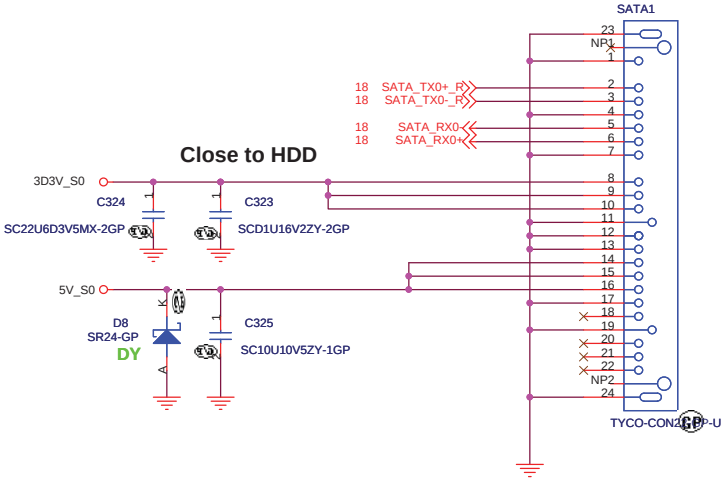




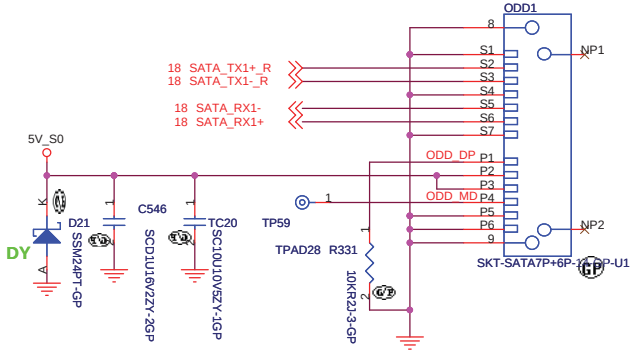
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB & DAUGHTER CONN		
Size: A3	Document Number: S13	Rev: SC
Date: Friday, May 16, 2008	Sheet 25 of 44	

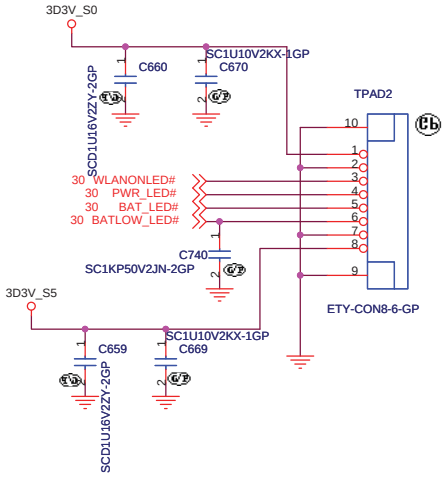
SATA HDD Connector



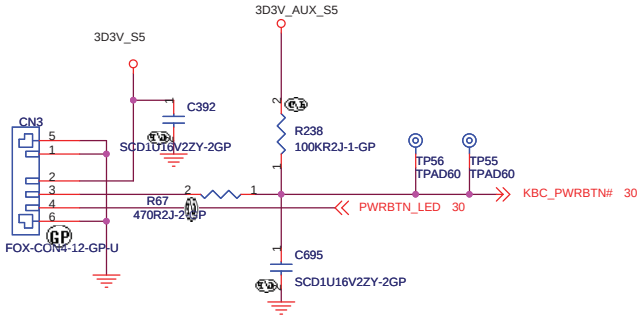
SATA ODD Connector



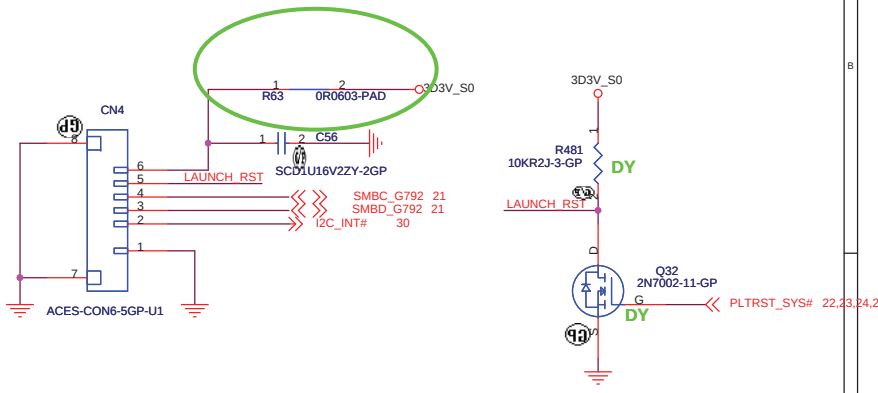
LED BD CONN



PWRBTN BD CONN



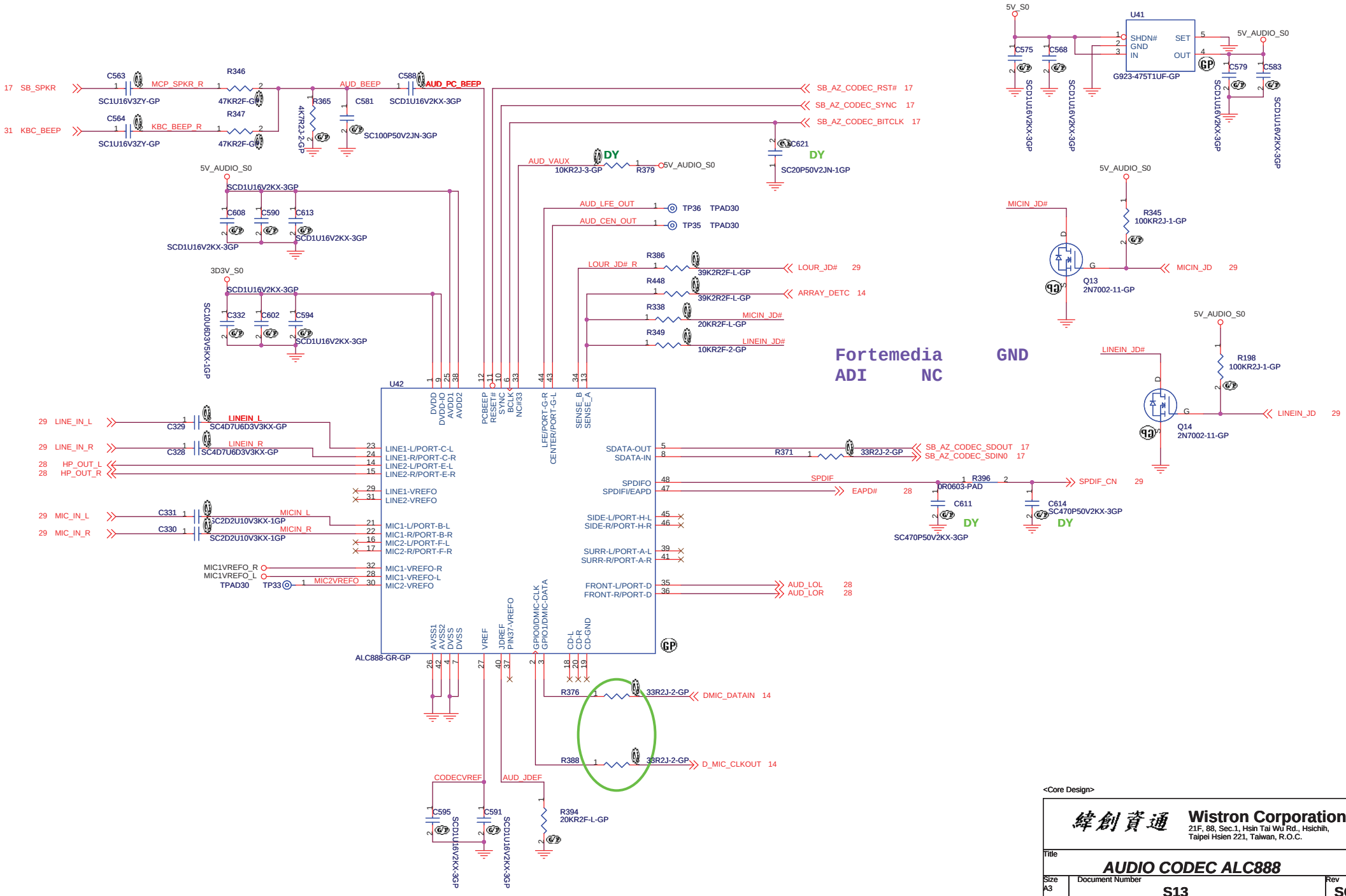
LAUNCH BD CONN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

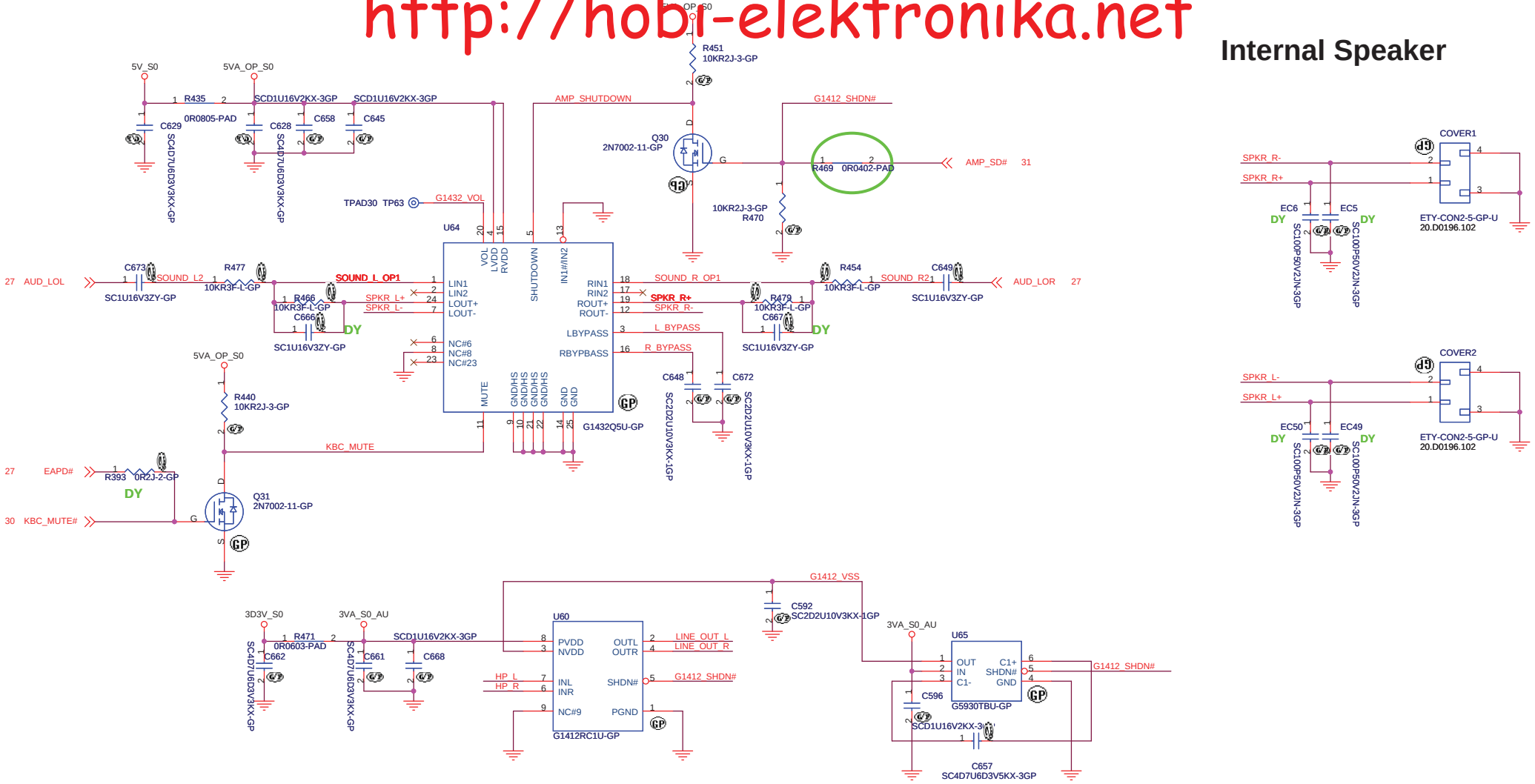
Title	HDD/CDROM/LED/LAUNCH	
Size A3	Document Number S13	Rev SC
Date: Friday, May 16, 2008	Sheet 26 of 44	



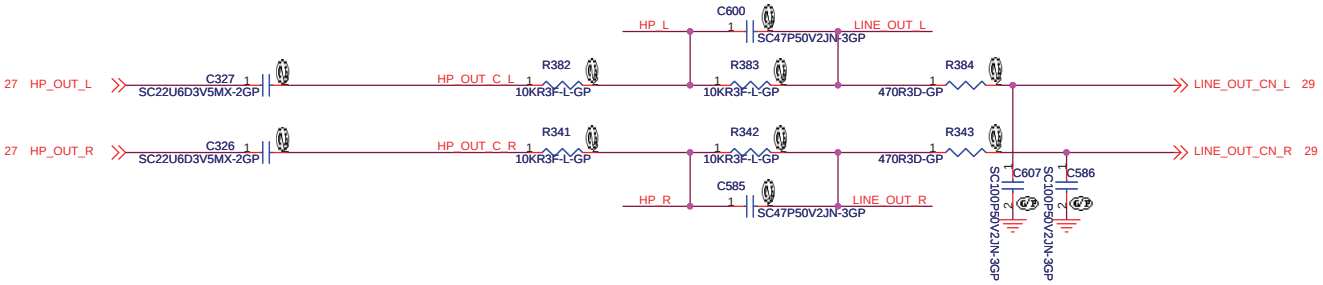
<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO CODEC ALC888	
Size A3	Document Number S13	Rev SC
Date: Friday, May 16, 2008	Sheet 27 of 44	

Internal Speaker



LINE Out



<Core Design>

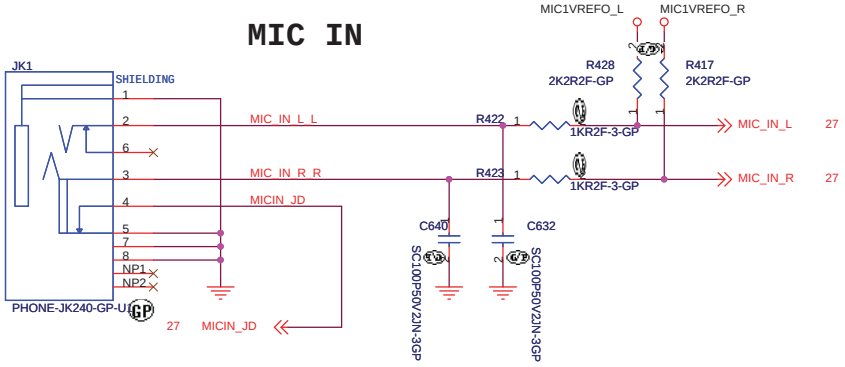
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO AMP/Speaker***

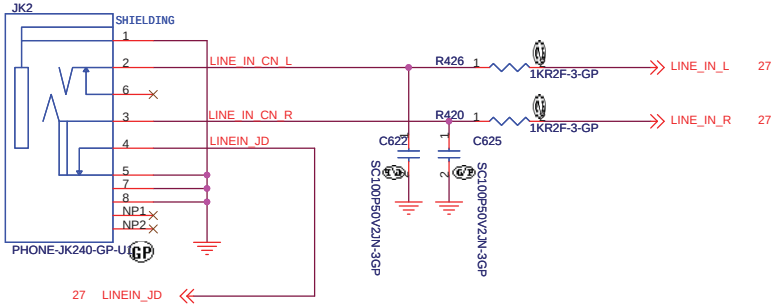
Size	Document Number	Rev
A3	S13	SC

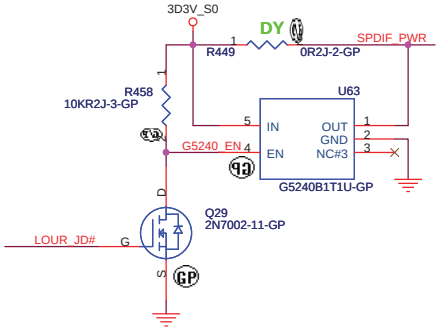
Date: Friday, May 16, 2008 Sheet 28 of 44

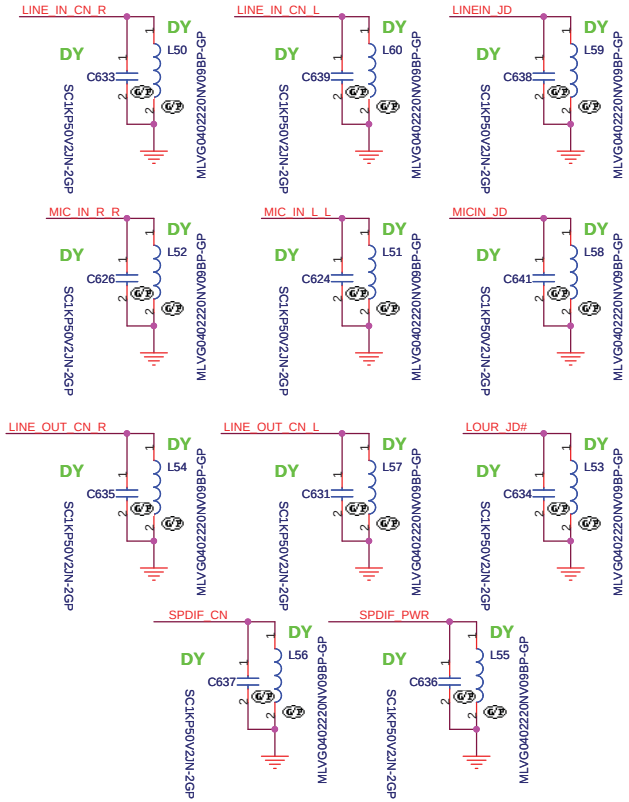
MIC IN



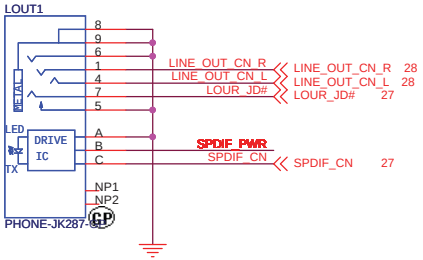
LINE IN





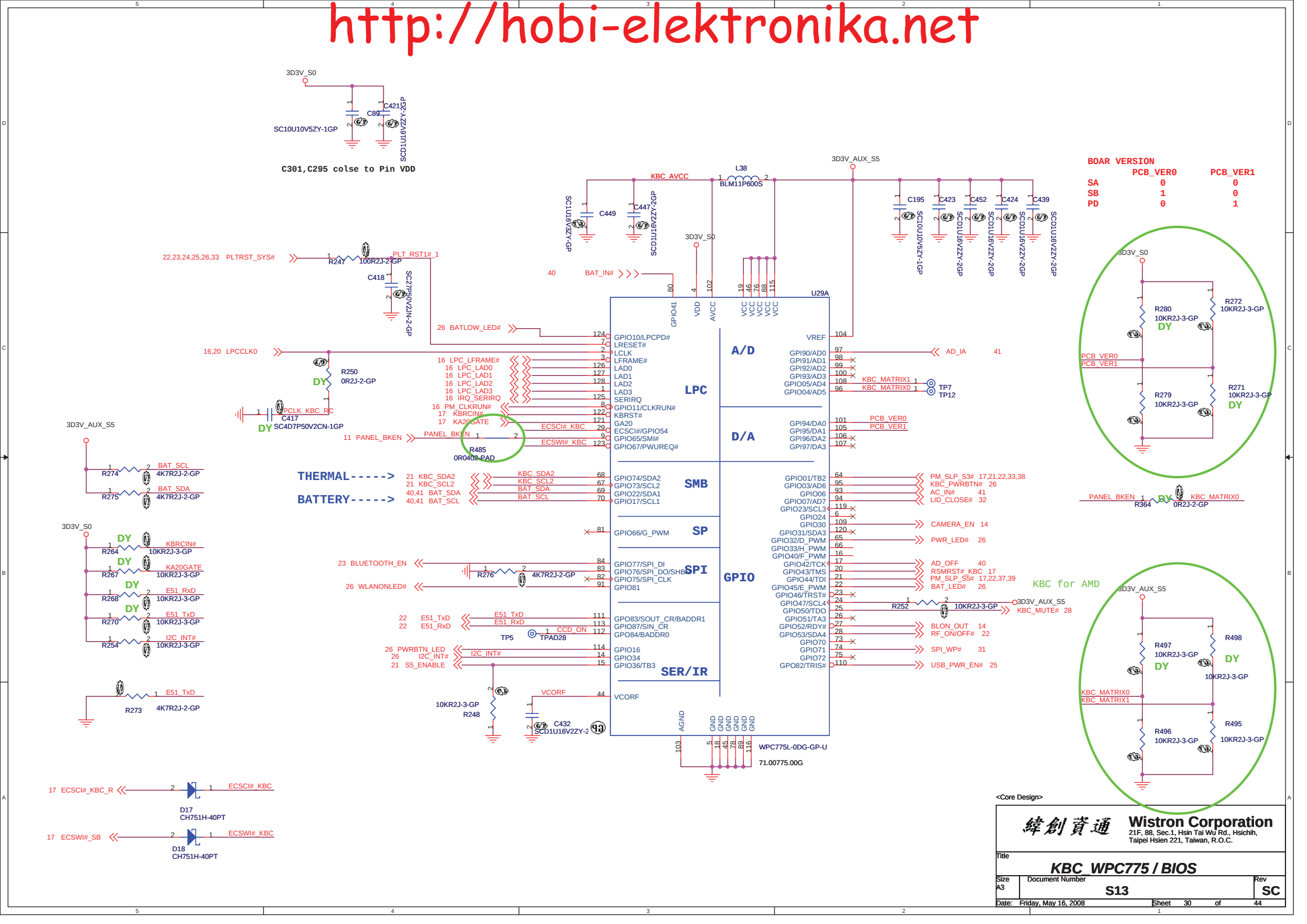


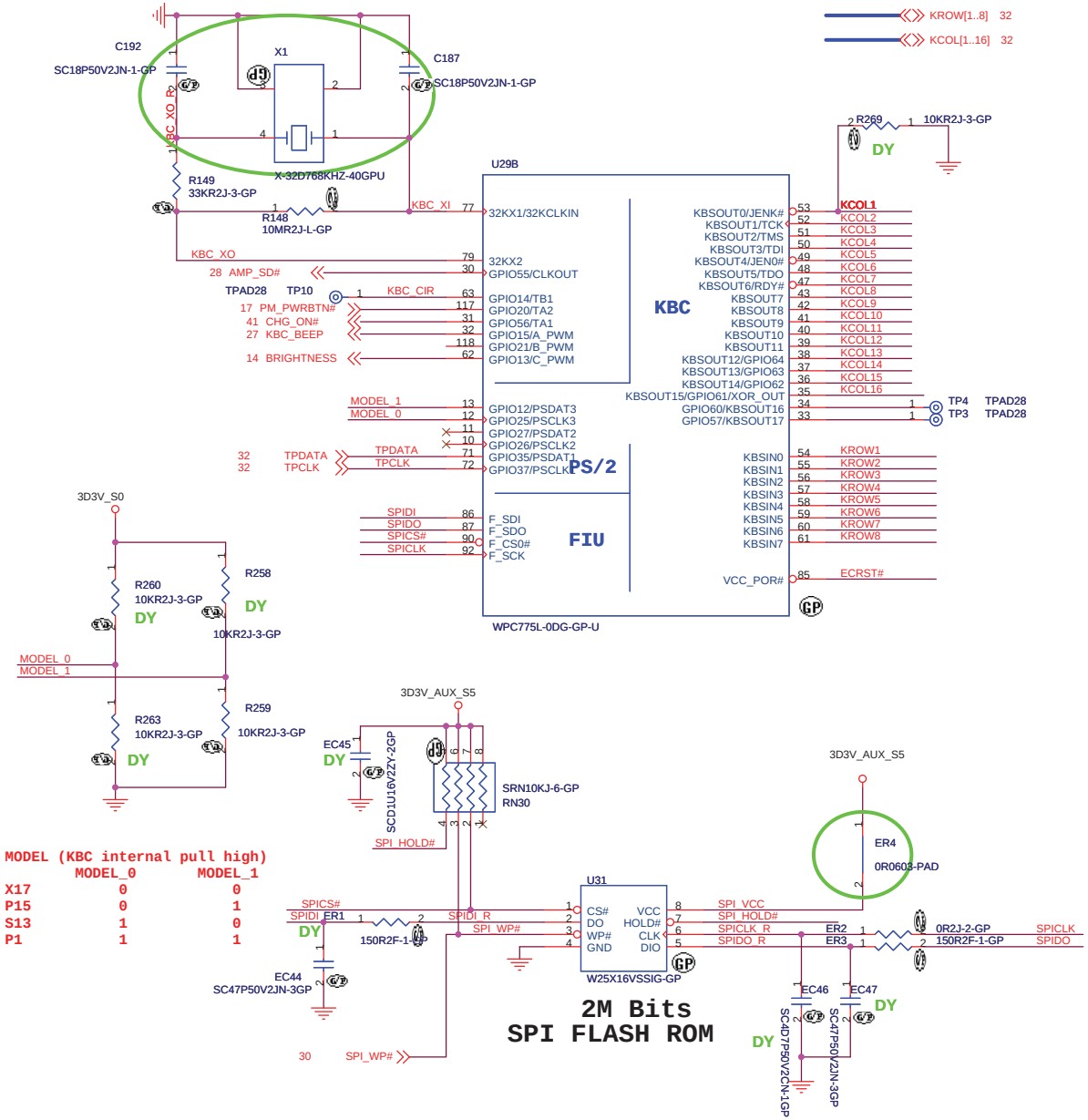
SPDIF / LINE OUT



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***AUDIO CONN/SUBWOOFER***
Size: A3	Document Number: S13 — Rev: SC
Date: Friday, May 16, 2008	Sheet 29 of 44





<Core Design>

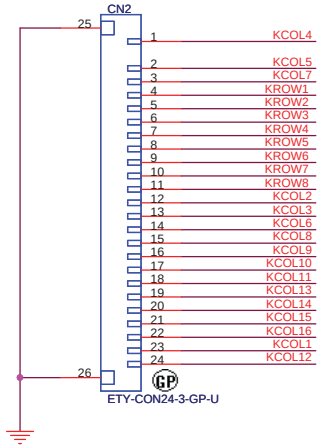
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

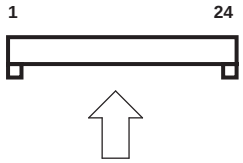
Title: KBC_WPC775 / BIOS(2/2)

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 31 of 44

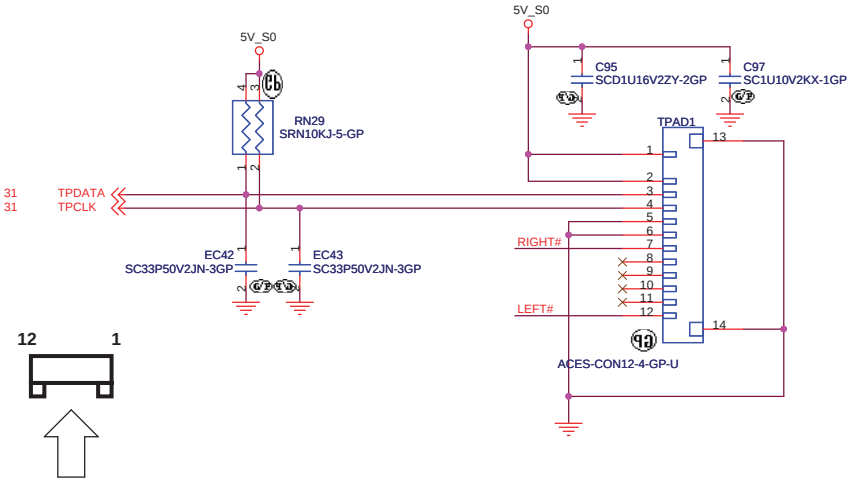
Internal KeyBoard Connector



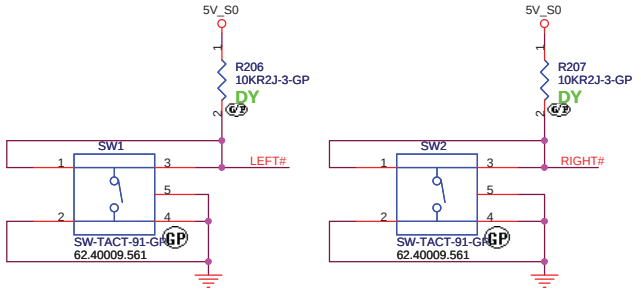


GOLDEN FINGER FOR DEBUG BOARD

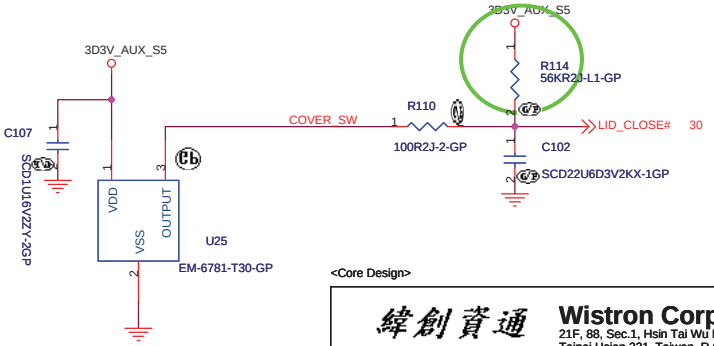
TouchPad Connector



TOUCHPAD BUTTON SWITCH



COVER SWITCH



<Core Design>

緯創資通 **Wistron Corporation**
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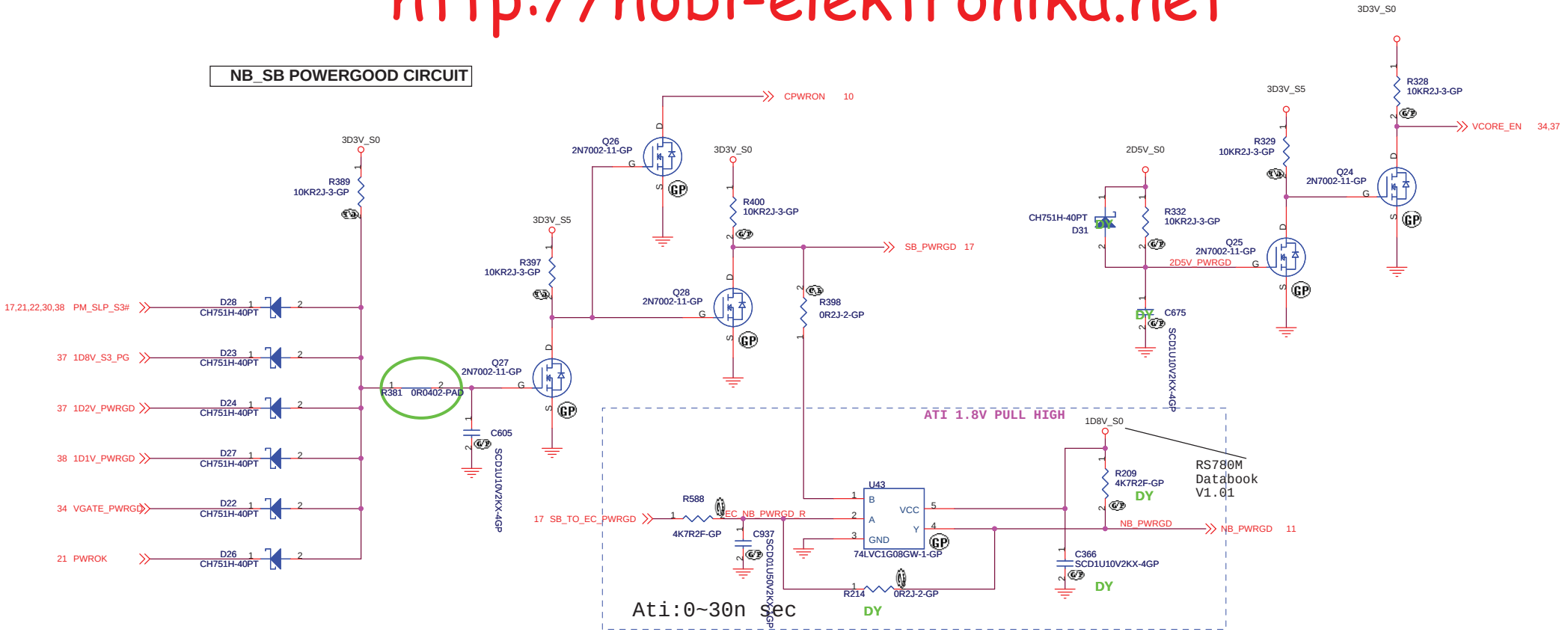
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***KEYBOARD/TPAD/DEBUG/LID***

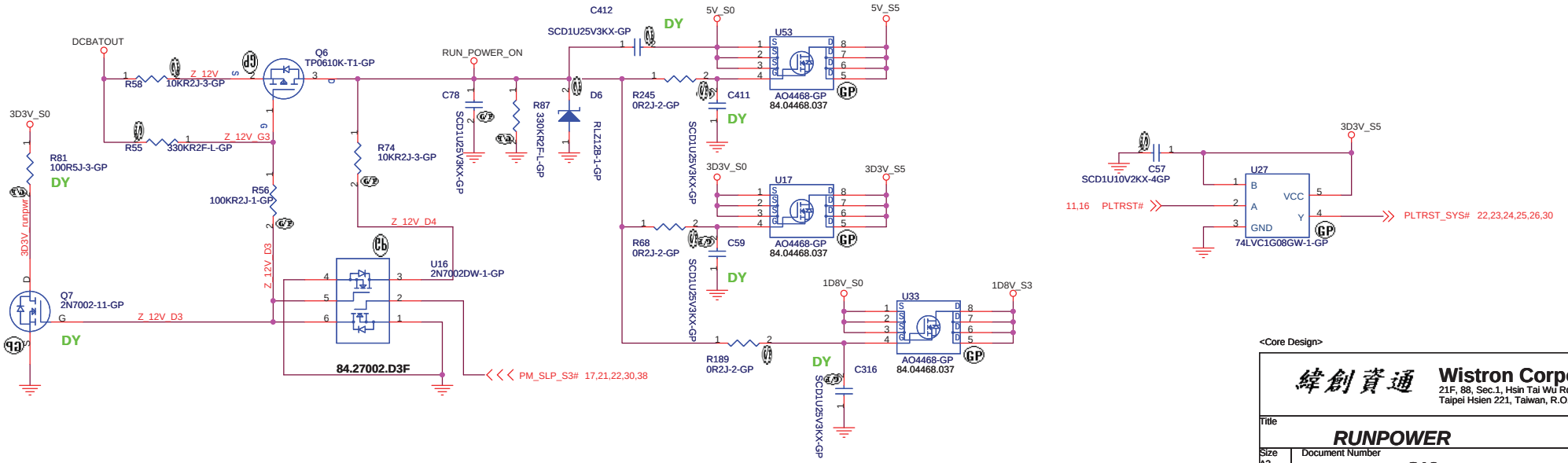
Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 32 of 44

NB_SB POWERGOOD CIRCUIT

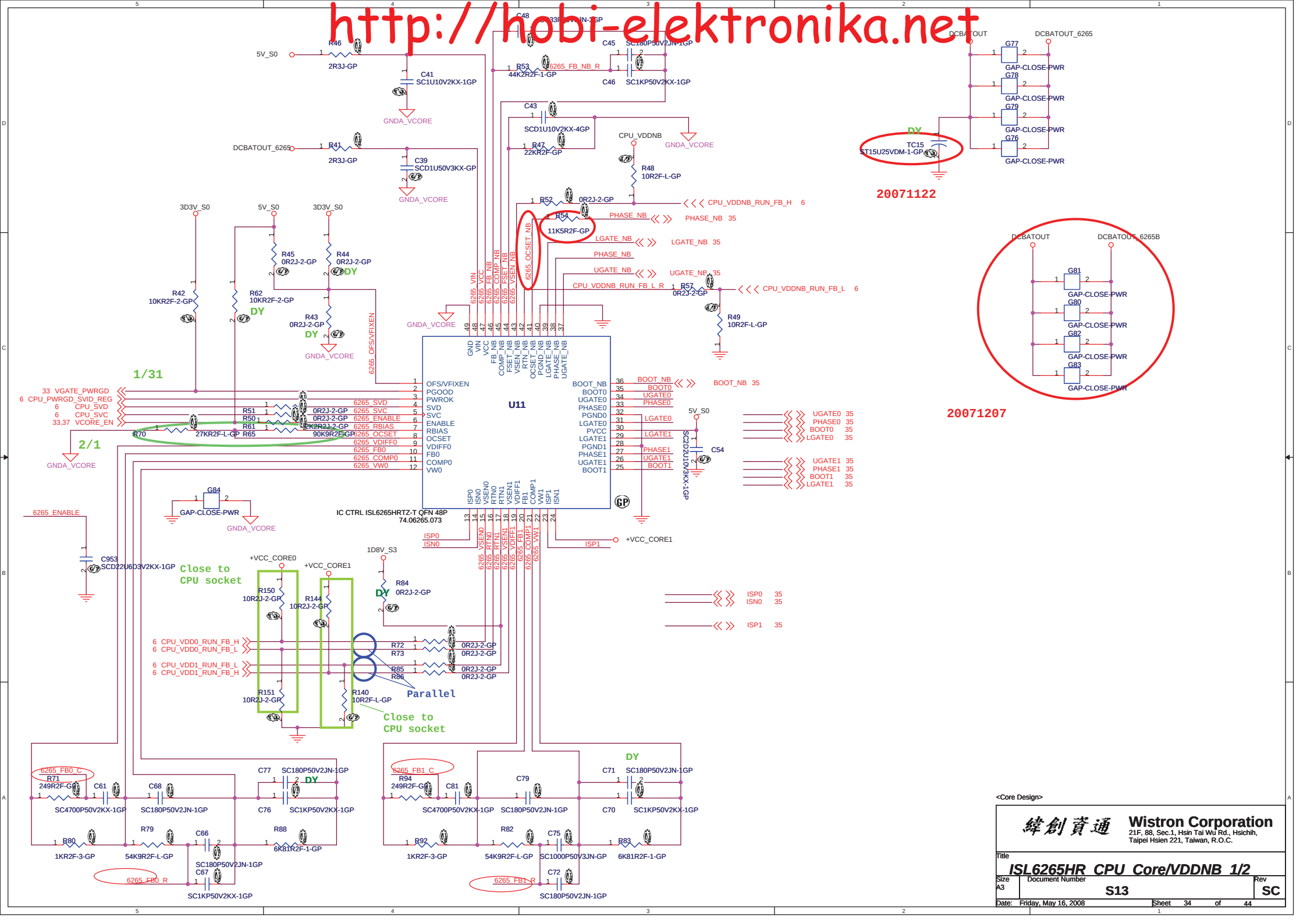


Run Power



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **RUNPOWER**		
Size: A3	Document Number: **S13**	Rev: **SC**
Date: Friday, May 16, 2008	Sheet 33 of 44	



<Core Design>

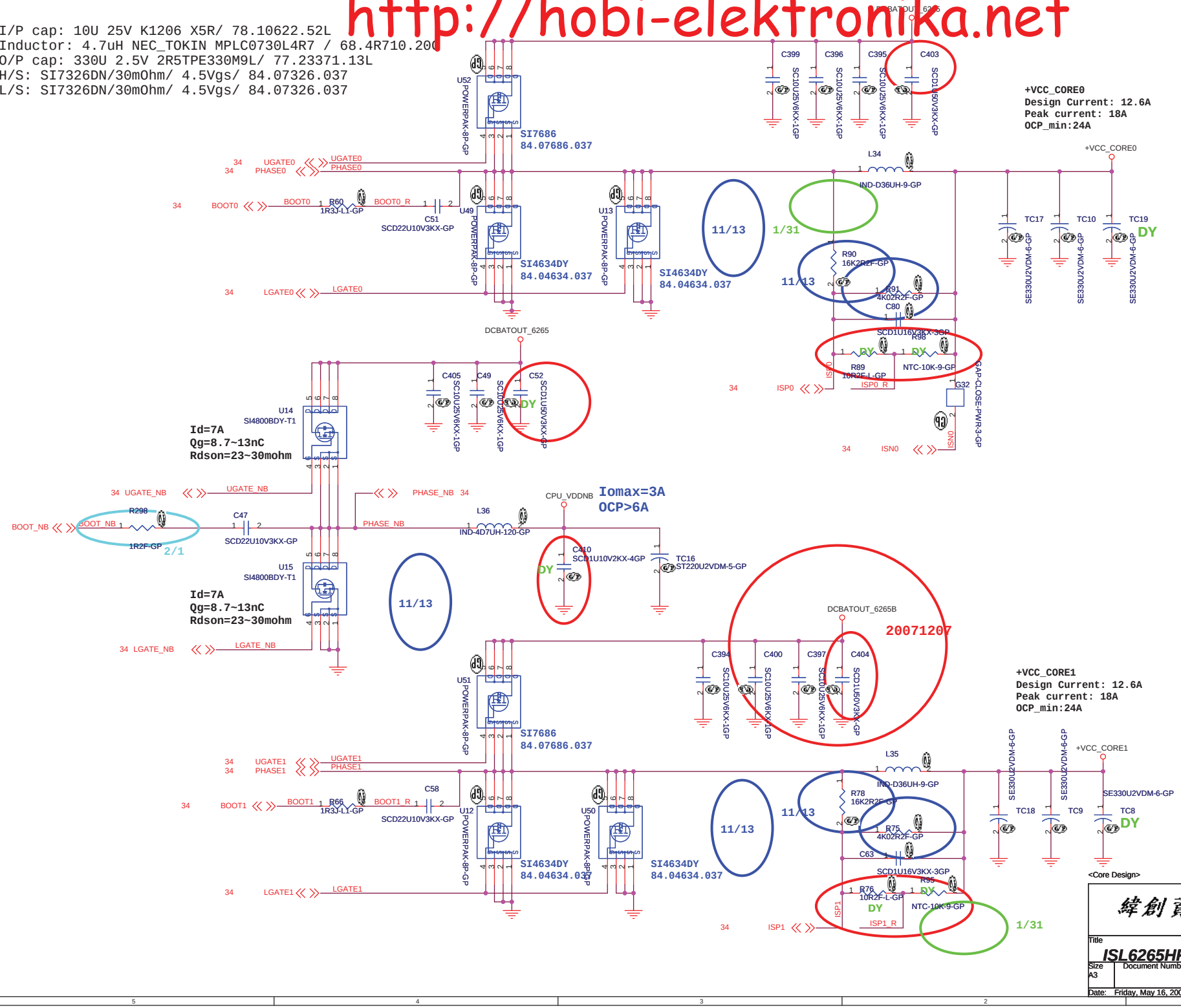
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6265HR CPU Core/VDDNB 1/2

Size	Document Number	Rev
A3	S13	SC

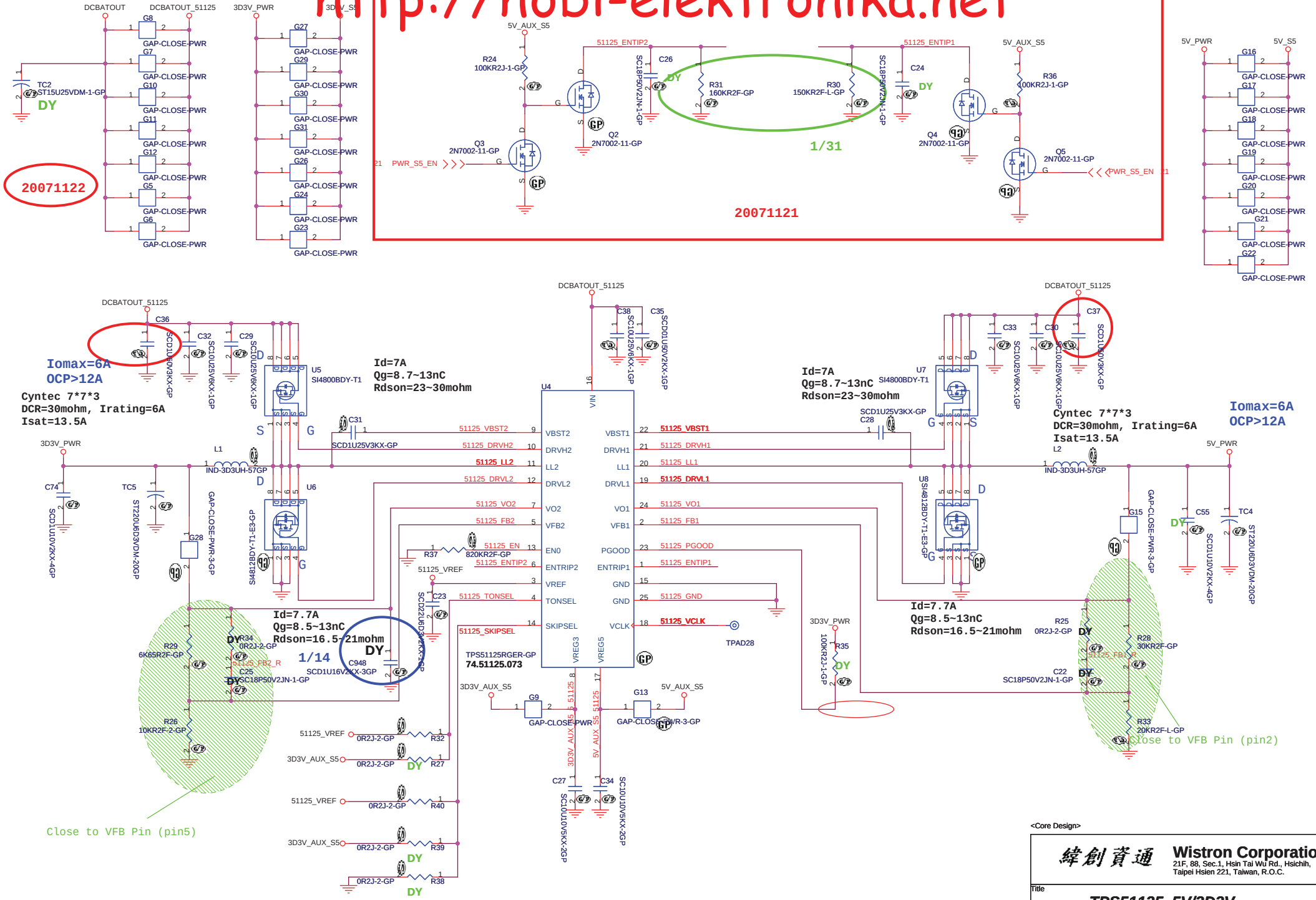
Date: Friday, May 16, 2008 Sheet 34 of 44

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 4.7uH NEC_TOKIN MPLC0730L4R7 / 68.4R710.20C
O/P cap: 330U 2.5V 2R5TPE330M9L/ 77.23371.13L
H/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037
L/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6265HR CPU Core/VDDNB 2/2
Size: A3 | Document Number: S13 | Rev: SC
Date: Friday, May 16, 2008 | Sheet 35 of 44



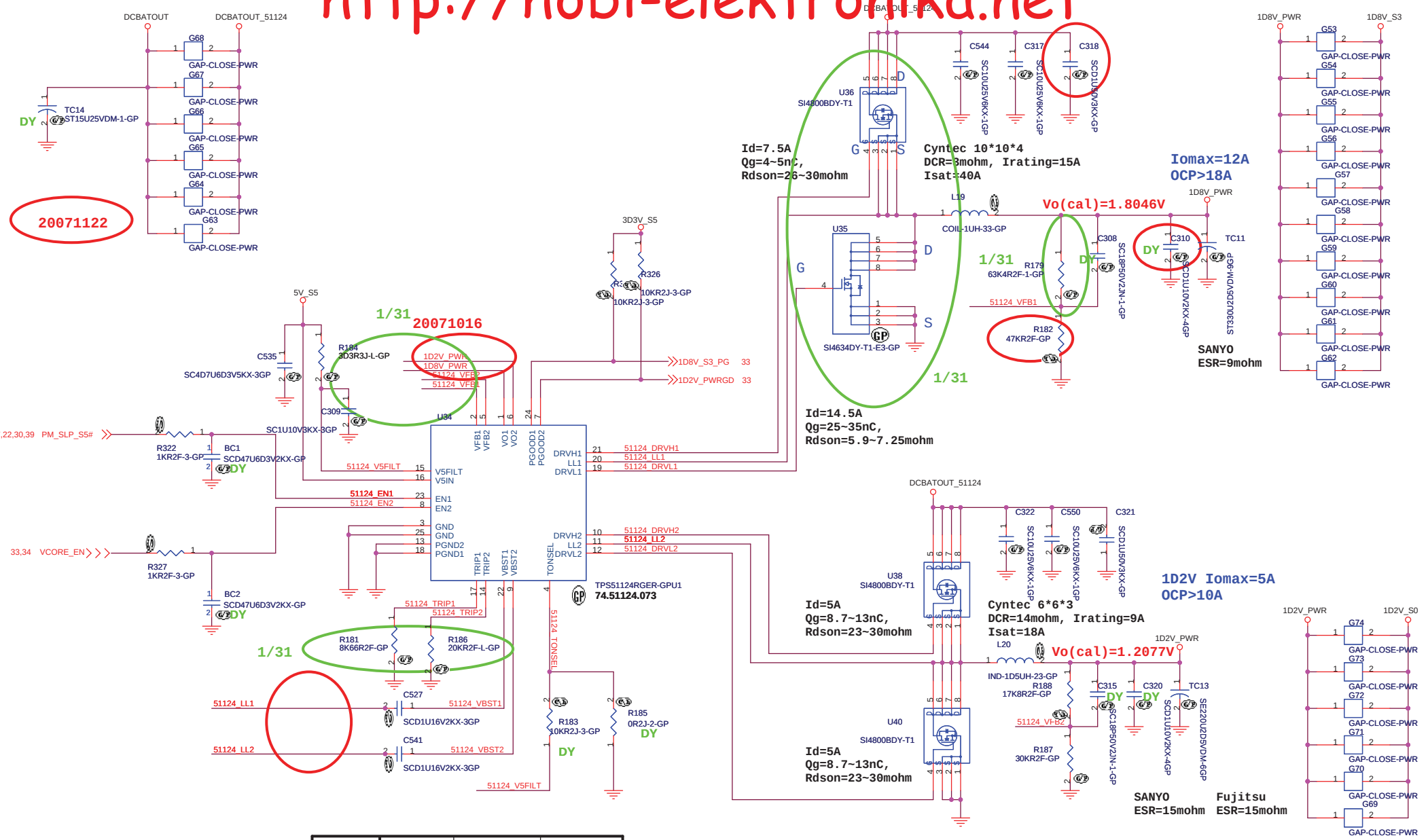
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51125_5V/3D3V**

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 36 of 44



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

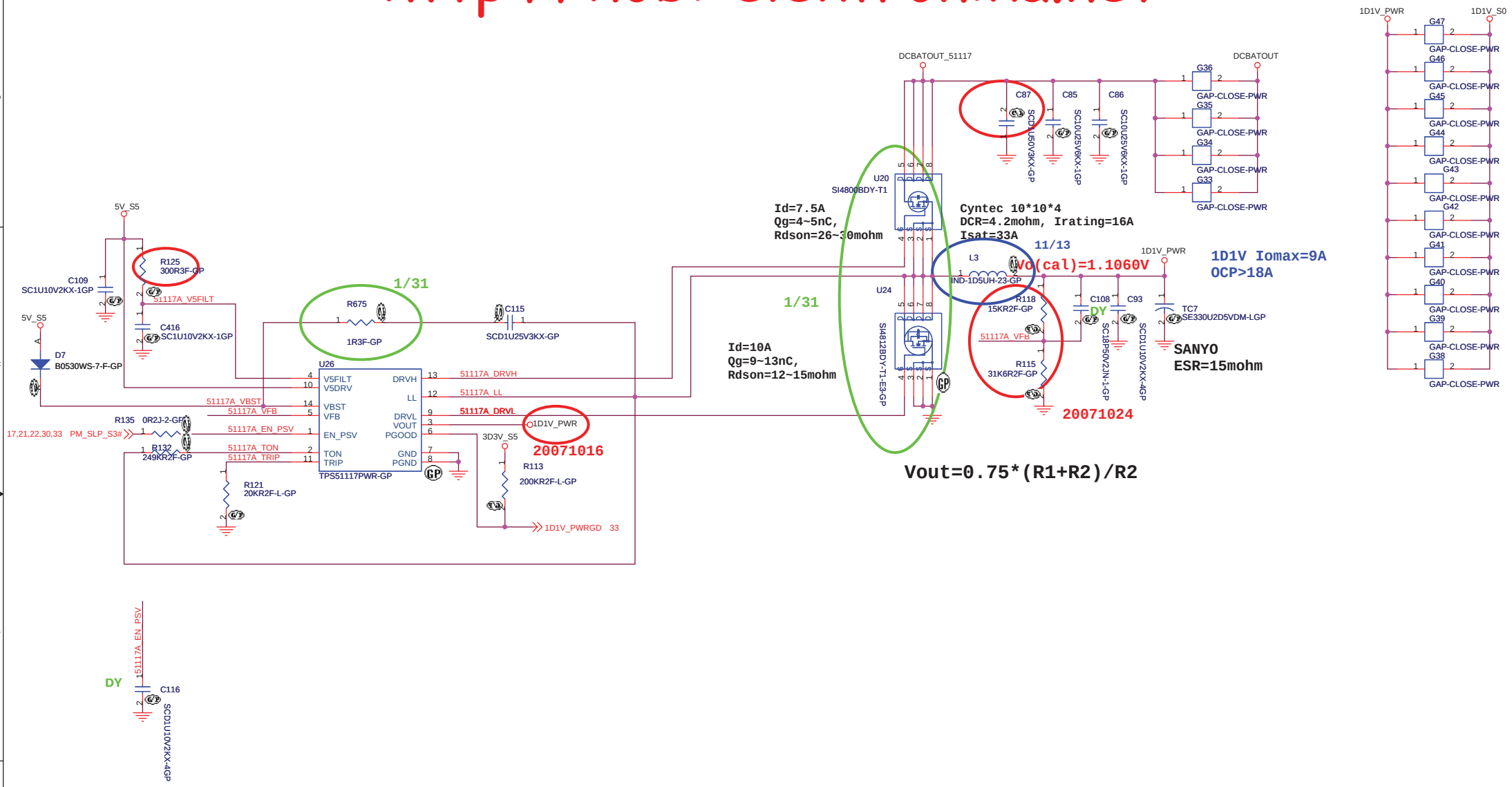
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V/1D2V

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 37 of 44



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51117_1D1V	
Size A3	Document Number S13	Rev SC
Date: Friday, May 16, 2008	Sheet 38 of 44	

1D2V_S5
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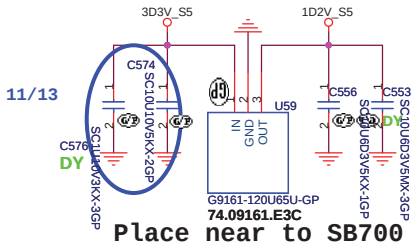

Place near to SB700

G957
1D5V_S0
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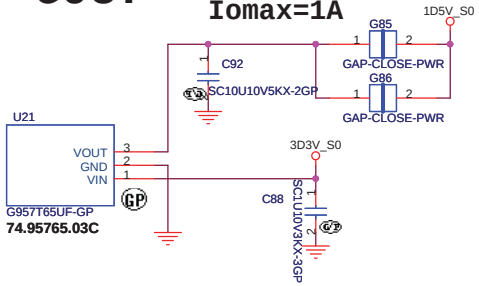

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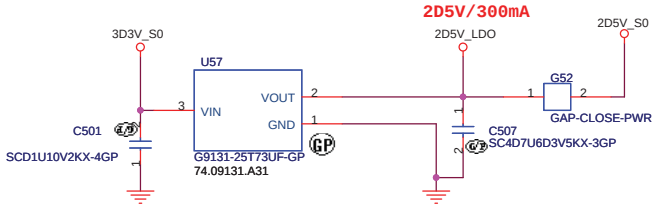

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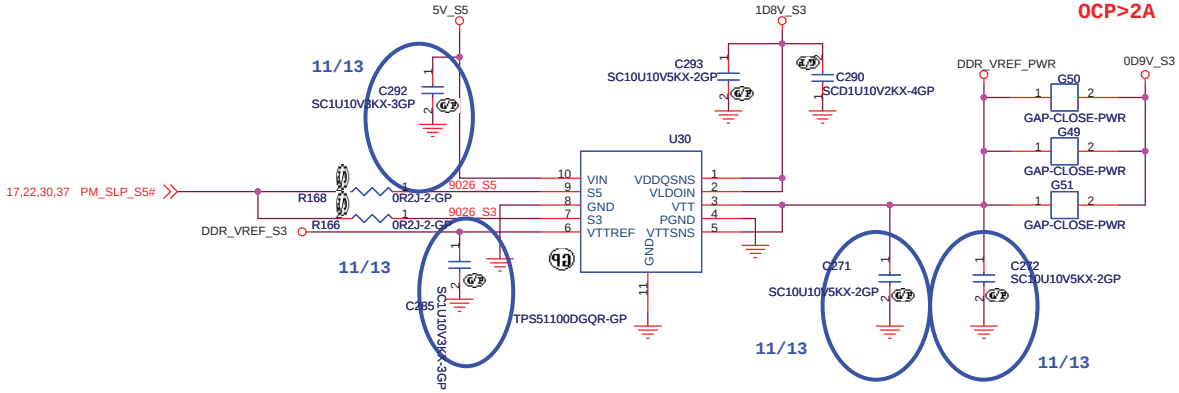
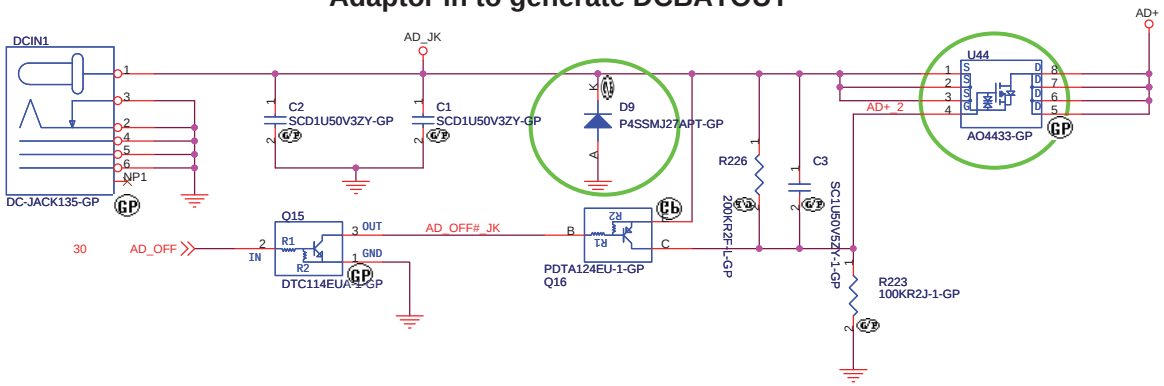


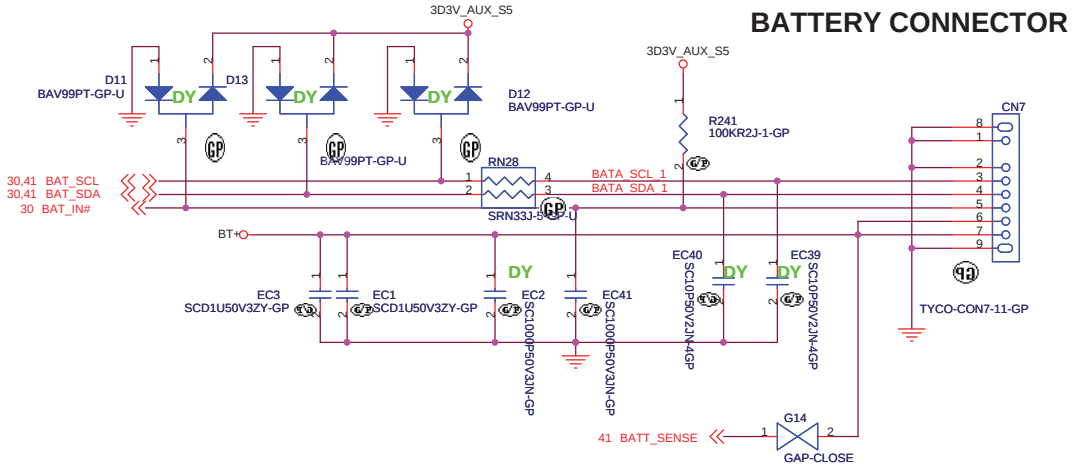
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 0D9V&2D5V&1D25V&1D5V		
Size: A3	Document Number: S13	Rev: SC
Date: Friday, May 16, 2008	Sheet 39 of 44	

Adaptor in to generate DCBATOUT

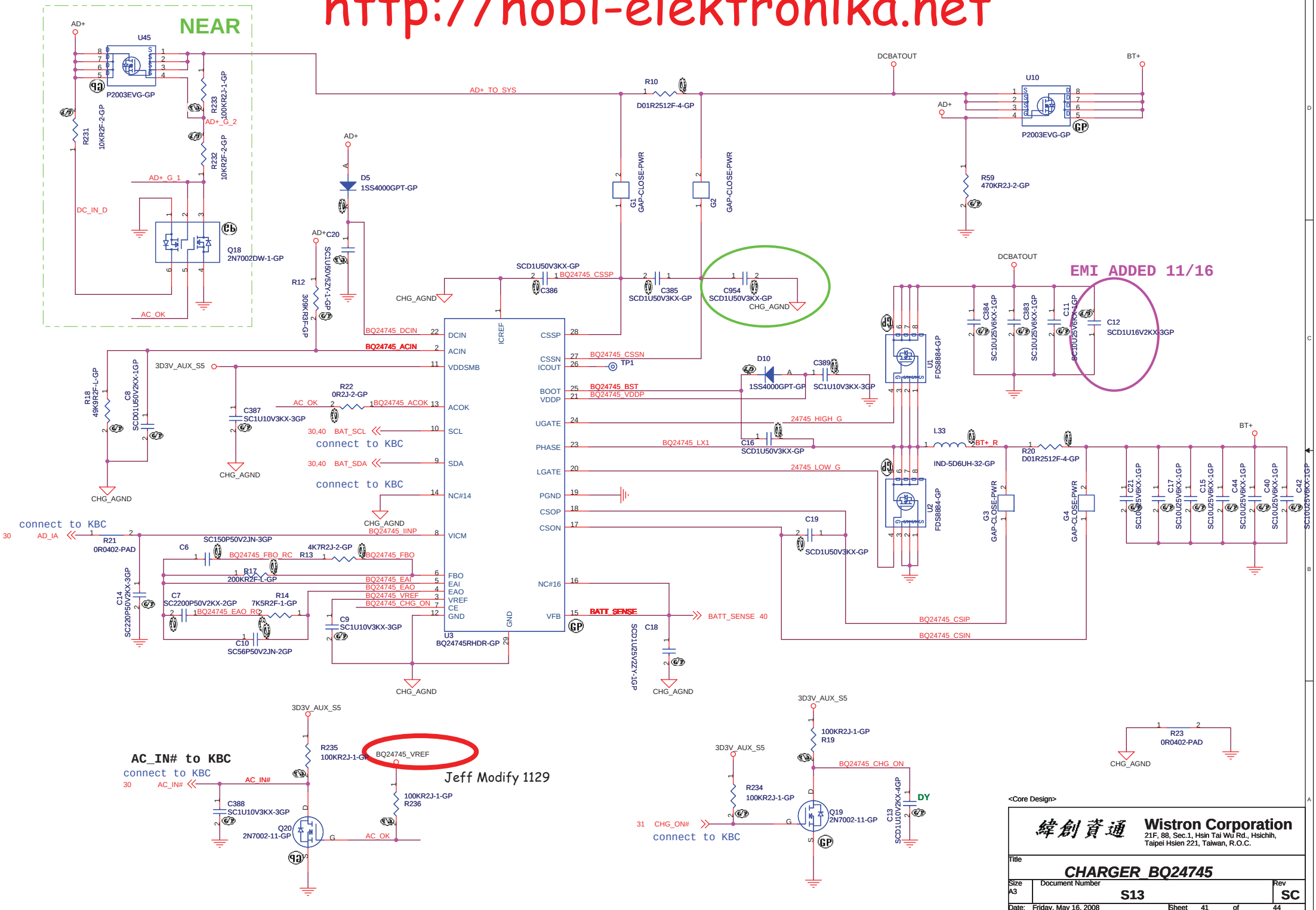


BATTERY CONNECTOR



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***AD_IN/ BTY SWITCH/GPURUN***
Size: A3	Document Number: **S13** — Rev: **SC**
Date: Friday, May 16, 2008	Sheet 40 of 44



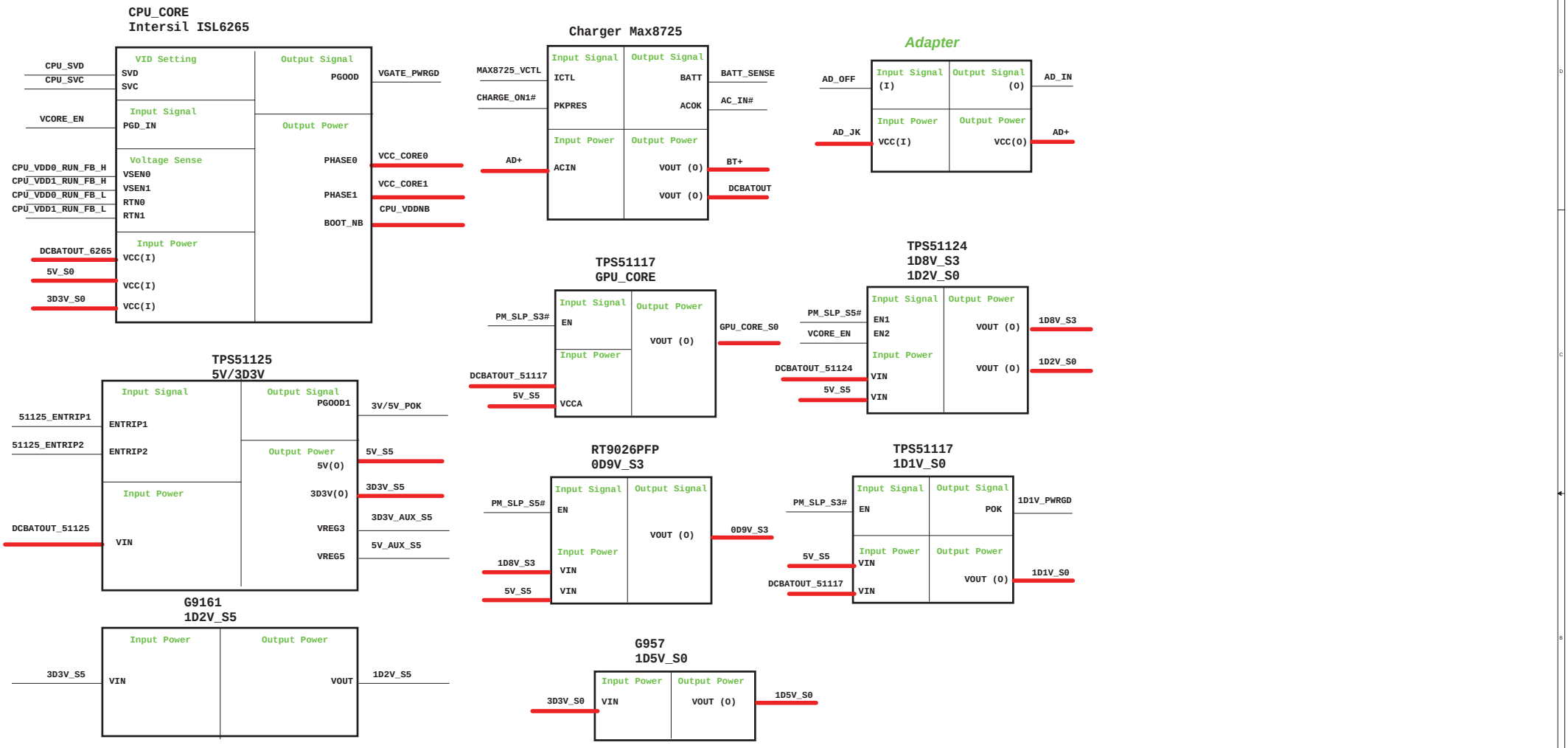
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER_BQ24745

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 41 of 44



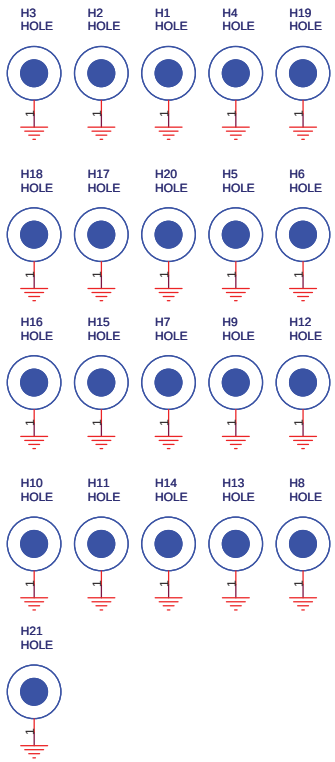
<Core Design>

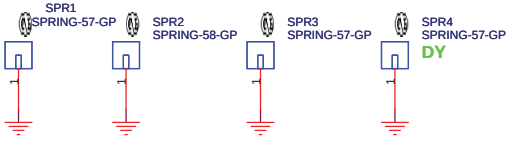
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

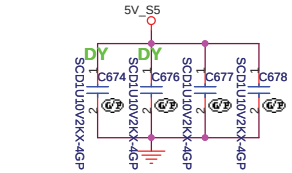
Title: Power Block Diagram

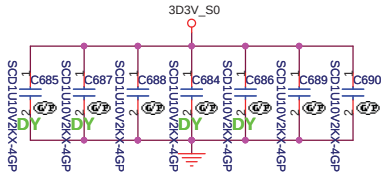
Size	Document Number	Rev
A2	S13	SC

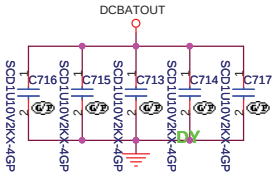
Date: Friday, May 16, 2008 Sheet 42 of 44

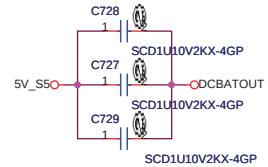


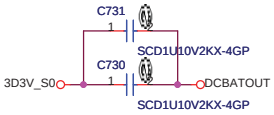


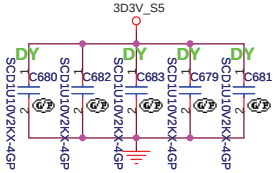


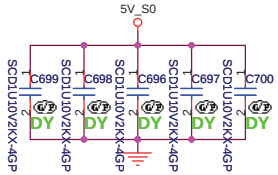


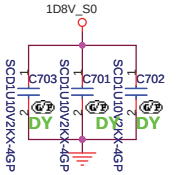


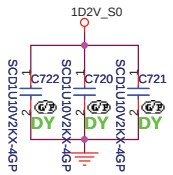


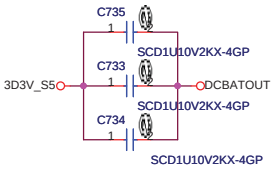


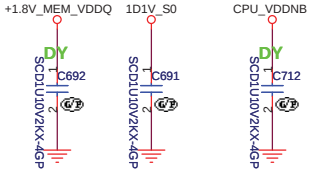


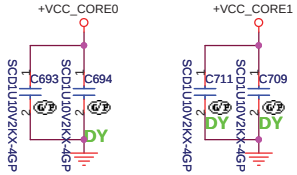


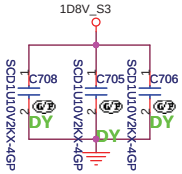


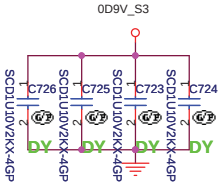


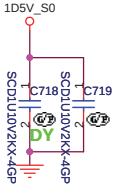


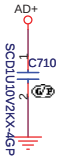


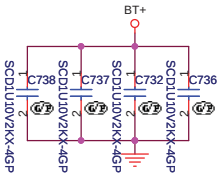


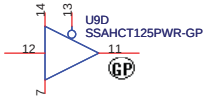


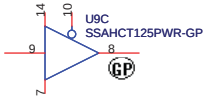












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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MISC
Size: A3
Document Number: S13
Rev: SC
Date: Friday, May 16, 2008
Sheet 43 of 44

NOTICE

Change List

Common Part

1.RS780M_A12 U55 71.RS780.M12
2.SB700_A12 U62 71.SB700.M06
3.KBC U29 71.00773.00G
4.CLKGEN U32 71.09480.A03
5.SIDE PORT U28 72.18512.M0U
6.MOSFET U52,U51 84.07686.037
7.MOSFET U13,U12,U49,U50 84.04634.037
8.H18,H19 34.4H802.001
9.CARD1 20.I0043.001
10.U61 71.00380.003
11. U11 74.06265.A73
12. U42 71.00888.E0G
13. U31 72.25X16.A01

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHANGE LIST
Size: A3 | Document Number: S13 | Rev: SC
Date: Friday, May 16, 2008 | Sheet 44 of 44