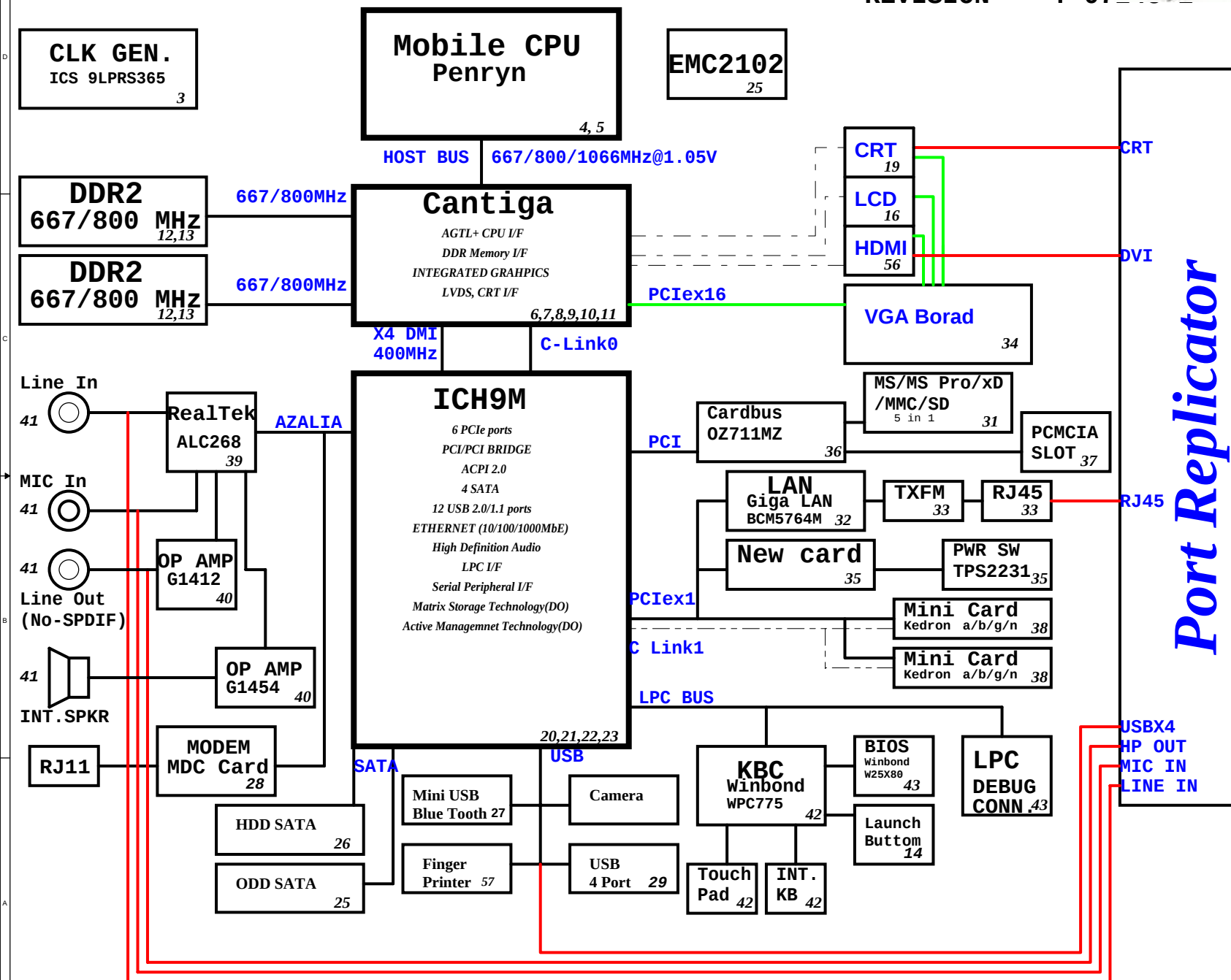


Homa (TM15") Block Diagram

Project code: 91
PCB P/N : 48
REVISION : 07



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Port Replicator

PCB STACKUP	
TOP	
VCC	
S	
S	
GND	
BOTTOM	

DCBATOUT	5V_S5(7A) 3D3V_S5(7A)
SYSTEM DC/DC TPS51124 51	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(16A) 1D8V_S3(16A)
TPS51100 50	
5V_S5	DDR_VREF_S3(1.5A) DDR_VREF_S3_1
G9131	
3D3V_S0	2D5V_S0(300mA)
APL5912 50	
1D8V_S3	1D5V_S0(2.5A)
CHARGER BQ24750 53	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA
CPU DC/DC ISL6266A 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 38A
GFX DC/DC ISL6263 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 5.5A

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config 1bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config 1 bit 0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved, Rising Edge of PWROK.	This signal has a weak internal pull-down. This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	Tying this strap low configures DMI for ESI-compatible operation. This signal has a weak internal pull up. ESI compatible mode is for server platforms only.This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing. It has a weak internal pull up.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

PCI Routing

page 31

	IDSEL	INT	REQ	GNT
RTS5158	AD25	6: CARDBUS	0	0

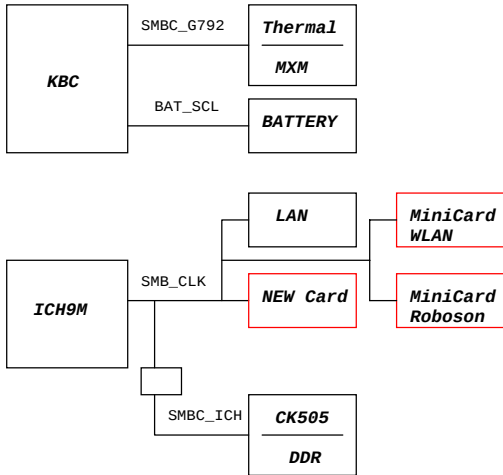
PCIE Routing

LANE1	LAN BCM5764MKMLG
LANE2	MiniCard WLAN
LANE3	MiniCard Roboson
LANE4	NewCard

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	DOCK USB
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

SMBus



ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5 page 97

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for nativeCFG9 GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LAD[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1066 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG12	ALLZ	0 = ALLZ mode enabled (Note 3) 1 = Disabled (default)
CFG13	XOR	0 = XOR mode enabled (Note 3) 1 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 =Digital display Port and PCie are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

- NOTE:
- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
 - iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.
 - Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

970

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Title	
Reference	
Size A3	Document Number
Homa	
Date: Thursday, April 03, 2008	Sheet 2 of 57
Rev -1	

6 H_A#(35..3) <<>> H_A#(35..3)

U29A 1 OF 4

H_A#3 J4 A3#
H_A#4 L5 A4#
H_A#5 L4 A5#
H_A#6 K5 A6#
H_A#7 M3 A7#
H_A#8 N2 A8#
H_A#9 J1 A9#
H_A#10 N3 A10#
H_A#11 P5 A11#
H_A#12 L2 A12#
H_A#13 L2 A13#
H_A#14 P4 A14#
H_A#15 P1 A15#
H_A#16 R1 A16#

ADDR GROUP 0
CONTROL

ADS# H1 <>> H_ADS# 6
BNR# E2 <>> H_BNR# 6
BPR# G5 <>> H_BPR# 6
DEFER# H5 <>> H_DEFER# 6
DRDY# F21 <>> H_DRDY# 6
DBSY# E1 <>> H_DBSY# 6
BR0# F1 <>> H_BRQ# 6
D20 <>> H_IERR#
B3 <<< H_INIT# 21
LOCK# H4 <>> H_LOCK# 6
H_CPURST# 6.55
RESET# C1 <>> H_RS#0
RS0# E4 <>> H_RS#1
RS1# G3 <>> H_RS#2
RS2# G2 <<< H_TRDY# 6
TRDY# G2 <<< H_HIT# 6
H_HITM# 6

6 H_ADSTB#0 <<>> H_REQ#(4..0)
6 H_REQ#(4..0)

H_REQ#0 K3 REQ#0
H_REQ#1 H2 REQ#1
H_REQ#2 K2 REQ#2
H_REQ#3 J3 REQ#3
H_REQ#4 L1 REQ#4

ADDR GROUP 1
STATUS I/O

BPM0# AD4 XDP BPM#0
BPM1# AD3 XDP BPM#1
BPM2# AD1 XDP BPM#2
BPM3# AC4 XDP BPM#3
PRDY# AC2 XDP BPM#4
PREQ# AC1 XDP BPM#5
TCK AA6 XDP TCK
TDI AA6 XDP TDI
TDO AB3 XDP TDO
TMS AB5 XDP TMS
TRST# AB6 XDP TRST#
DBR# C20 XDP DBRESET#

H_A#17 Y2 A17#
H_A#18 U6 A18#
H_A#19 P3 A19#
H_A#20 W6 A20#
H_A#21 U4 A21#
H_A#22 Y5 A22#
H_A#23 U1 A23#
H_A#24 R4 A24#
H_A#25 T3 A25#
H_A#26 T3 A26#
H_A#27 W2 A27#
H_A#28 W5 A28#
H_A#29 Y4 A29#
H_A#30 U2 A30#
H_A#31 V4 A31#
H_A#32 W3 A32#
H_A#33 AA4 A33#
H_A#34 AB2 A34#
H_A#35 AA3 A35#

ICL

PROCHOT# D21 CPU_PROCHOT#
A24 <>> H_THERMDA 25
B25 <>> H_THERMDC 25
THERMTRIP# C7 THERMTRIP#
1 R104
Do Not Stuff
PM_THRMTRIP-A# 7,21,46

6 H_ADSTB#1 <<>> H_A20M#
21 H_A20M# <<>> H_FERR#
21 H_FERR# <<>> H_IGNNE#
21 H_IGNNE# <<>> H_STPCLK#
21 H_STPCLK# <<>> H_INTR#
21 H_INTR# <<>> H_NMI#
21 H_NMI# <<>> H_SMI#

RESERVED

HCLK
BCLK0 A22 <>> CLK_CPU_BCLK 3
BCLK1 A21 <>> CLK_CPU_BCLK 3

RSVD#M4 M4
RSVD#N5 N5
RSVD#T2 T2
RSVD#V3 V3
RSVD#B2 B2
RSVD#C3 C3
RSVD#D2 D2
RSVD#D22 D22
RSVD#D3 D3
RSVD#F6 F6
KEY_NC B1

BGA479-SKT6-GPU6
62.10079.001
1ST = 62.10053.401

XDP TMS R51 1 54D9R2F-L1-GP
XDP TDI R52 1 54D9R2F-L1-GP
XDP BPM#5 R43 1 54D9R2F-L1-GP
H_CPURST# R401 1 Do Not Stuff
XDP DBRESET# R109 1 Do Not Stuff
XDP TCK R42 1 54D9R2F-L1-GP
XDP TRST# R53 1 54D9R2F-L1-GP

All place within 2" to CPU

TP15 Do Not Stuff

1D05V_S0

R86 56R2J-4-GP

Place testpoint on H_IERR# with a GND 0.1" away

TP17 Do Not Stuff

H_THERMDA

H_THERMDC

C97 Do Not Stuff

DY

1D05V_S0

R82 68R2-GP

R75 Do Not Stuff

DY

CPU_PROCHOT#_R 48

PM_THRMTRIP-A# 7,21,46

1D05V_S0

R41 1KR2F-3-GP

CPU_GTLREF0

TEST1 C23

TEST2 D25

TEST4 AF26

RSVD CPU 12 C24

RSVD CPU 13 AE1

RSVD CPU 14 A26

Do Not Stuff P16

Do Not Stuff P21

CPU_SEL0 B22

CPU_SEL1 B23

CPU_SEL2 C21

2KR2F-3-GP

R34

Do Not Stuff

C25

Do Not Stuff

DY

Do Not Stuff

Do Not Stuff

Do Not Stuff

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Do Not Stuff

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Do Not Stuff



Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

H_DINV#(3..0) <<>> H_DINV#(3..0) 6
H_DSTBN#(3..0) <<>> H_DSTBN#(3..0) 6
H_DSTBP#(3..0) <<>> H_DSTBP#(3..0) 6
H_D#(63..0) <<>> H_D#(63..0) 6

U29B 2 OF 4

H_D#0 E22 D0#
H_D#1 E24 D1#
H_D#2 E26 D2#
H_D#3 G22 D3#
H_D#4 E23 D4#
H_D#5 G25 D5#
H_D#6 E25 D6#
H_D#7 E23 D7#
H_D#8 K24 D8#
H_D#9 G24 D9#
H_D#10 J24 D10#
H_D#11 J23 D11#
H_D#12 H22 D12#
H_D#13 F26 D13#
H_D#14 K22 D14#
H_D#15 H23 D15#

DATA GRP0
DATA

Y22 H_D#32
AB24 H_D#33
V24 H_D#34
V26 H_D#35
V23 H_D#36
T22 H_D#37
U25 H_D#38
U23 H_D#39
V25 H_D#40
W22 H_D#41
Y23 H_D#42
W24 H_D#43
U25 H_D#44
AA23 H_D#45
AA24 H_D#46
AB25 H_D#47
Y26 H_D#48
AA26 H_D#49
U22 H_D#50

6 H_DSTBN#0 <<>> H_DSTBN#0
6 H_DSTBP#0 <<>> H_DSTBP#0
6 H_DINV#0 <<>> H_DINV#0

DATA GRP1
DATA

DSTBN#0
DSTBP#0
DINV#0

H_D#16 N22 D16#
H_D#17 K22 D17#
H_D#18 P26 D18#
H_D#19 R23 D19#
H_D#20 L23 D20#
H_D#21 M24 D21#
H_D#22 L22 D22#
H_D#23 M25 D23#
H_D#24 P25 D24#
H_D#25 P23 D25#
H_D#26 P22 D26#
H_D#27 T24 D27#
H_D#28 R24 D28#
H_D#29 L25 D29#
H_D#30 T25 D30#
H_D#31 N25 D31#

DATA GRP2
DATA

AE24 H_D#48
AD24 H_D#49
AA21 H_D#50
AB22 H_D#51
AB21 H_D#52
AC26 H_D#53
AD20 H_D#54
AE22 H_D#55
AE23 H_D#56
AC25 H_D#57
AE21 H_D#58
AD21 H_D#59
AC22 H_D#60
AD23 H_D#61
AE22 H_D#62
AC23 H_D#63
AE25 H_D#64
AE24 H_D#65
AC20 H_D#66

6 H_DSTBN#1 <<>> H_DSTBN#1
6 H_DSTBP#1 <<>> H_DSTBP#1
6 H_DINV#1 <<>> H_DINV#1

DATA GRP3
DATA

DSTBN#1
DSTBP#1
DINV#1

AD26
TEST1 C23
TEST2 D25
TEST3
TEST4
TEST5
TEST6

MISC

COMP0 R26 COMP0 R66 1 27D4R2F-L1-GP
COMP1 U26 COMP1 R59 1 54D9R2F-L1-GP
COMP2 AA1 COMP2 R48 1 27D4R2F-L1-GP
COMP3 Y1 COMP3 R54 1 54D9R2F-L1-GP

3.7 CPU_SEL0 <<< B22
3.7 CPU_SEL1 <<< B23
3.7 CPU_SEL2 <<< C21

DATA GRP4
DATA

DPRSTP# B5 <<< H_DPRSTP# 7,21,48
DPSLP# D24 <<< H_DPSLP# 6
DPWR# D6 <<< H_DPWR# 6
PWRGOOD D7 <<< H_PWRGD 21,46,55
SLP# D7 <<< H_CPUSLP# 6
PSI# AE6 <<< PSI# 48

BGA479-SKT6-GPU6
1ST = 62.10053.401

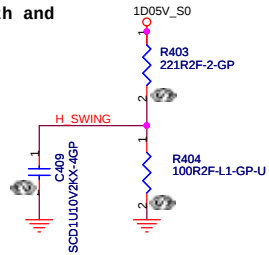
Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5"
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"

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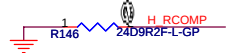
Title		CPU (1 of 2)	
Size	Document Number	Rev	-1
Date: Thursday, April 03, 2008		Sheet 4 of 57	

H_SWING routing Trace width and Spacing use 10 / 20 mil

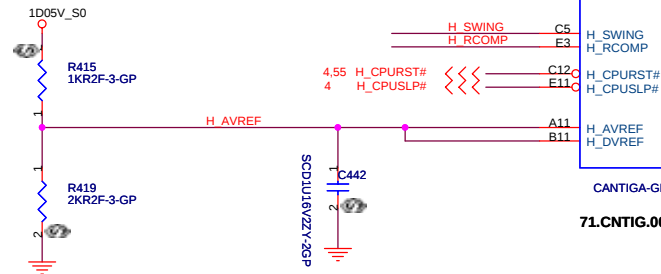
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

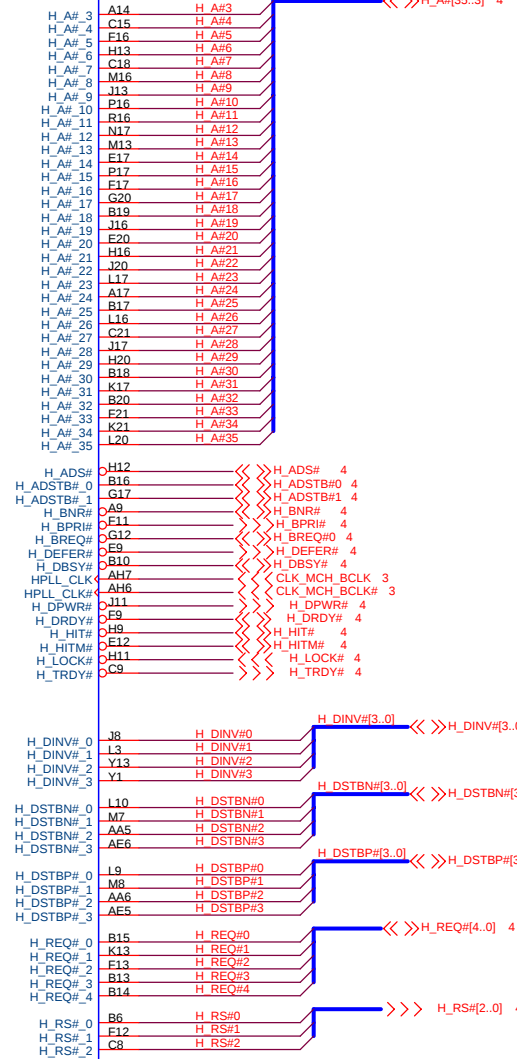


Place them near to the chip (< 0.5")



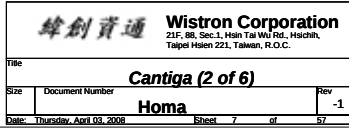
U37A 1 OF 10

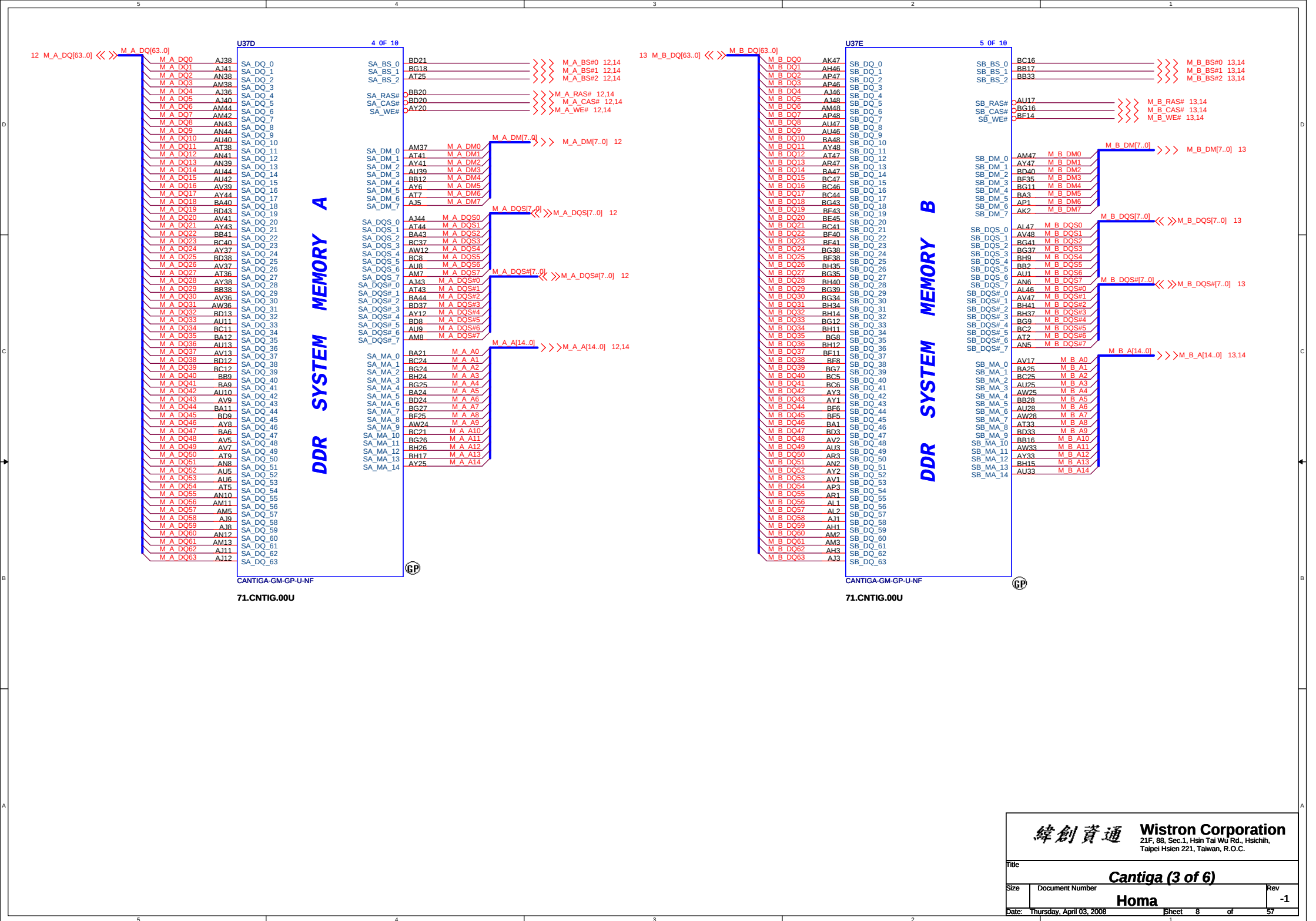
HOST

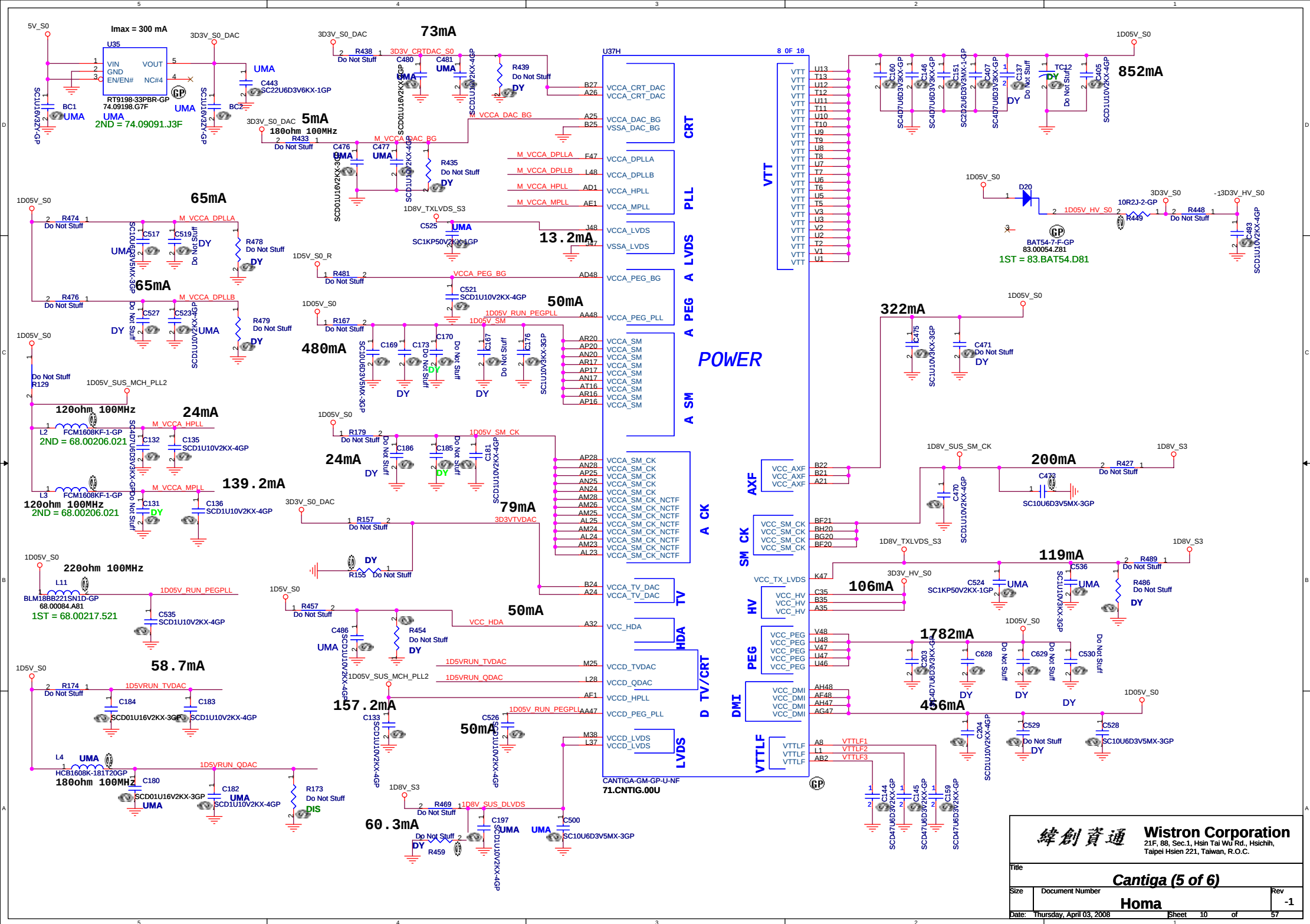


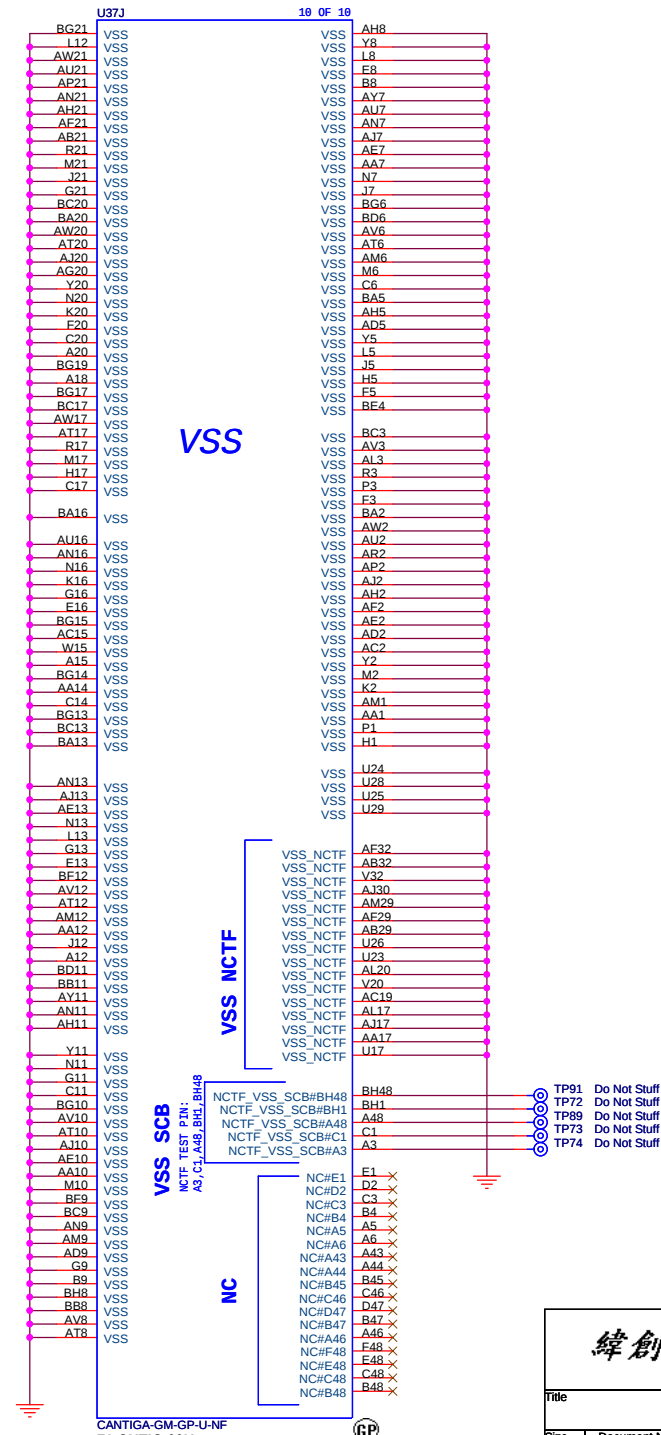
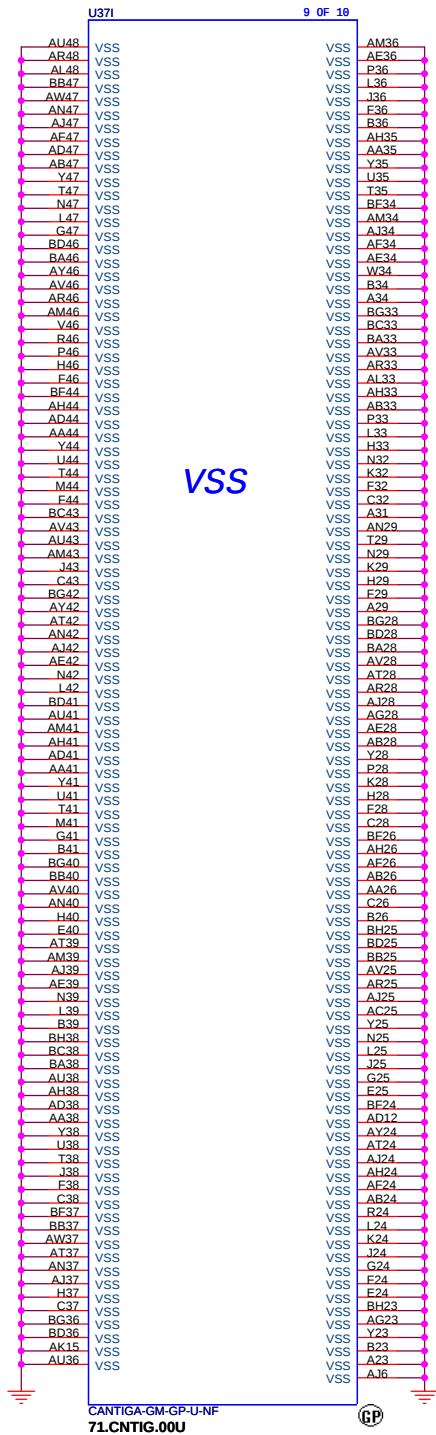
970

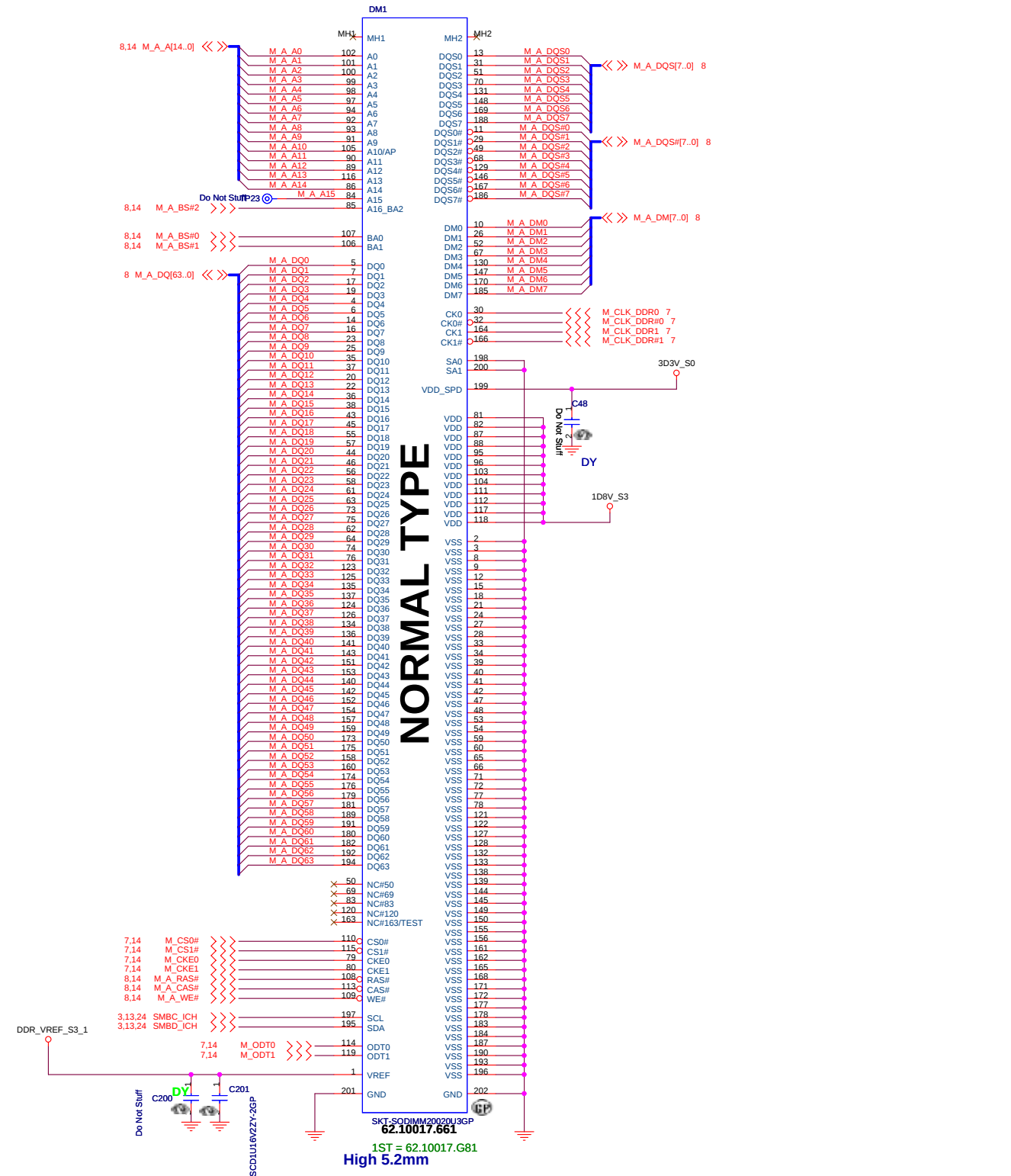
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Taipei Hsien 221, Taiwan, R.O.C.







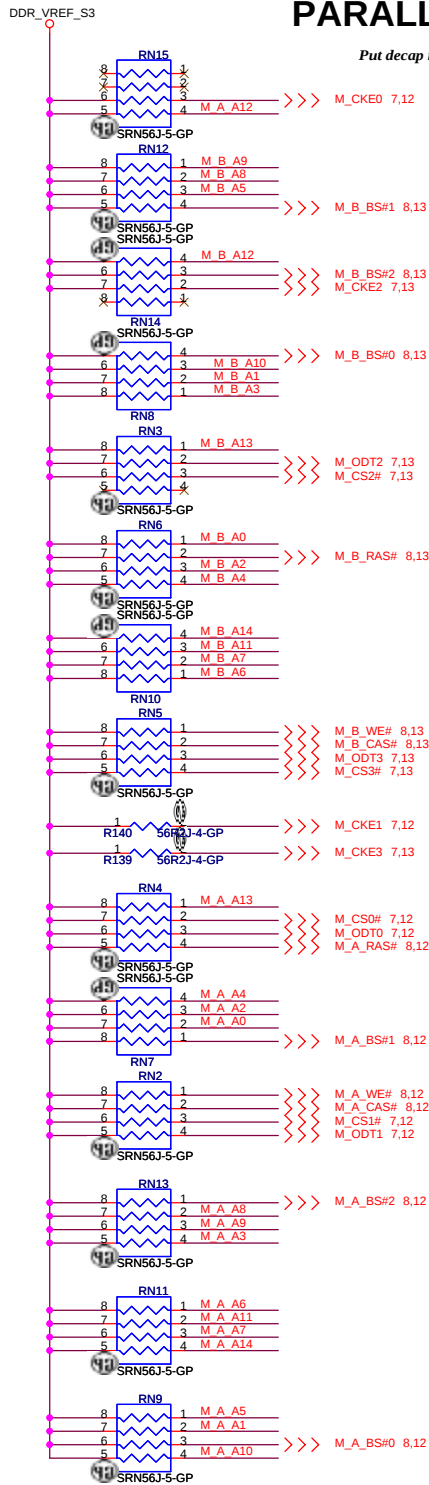






PARALLEL TERMINATION

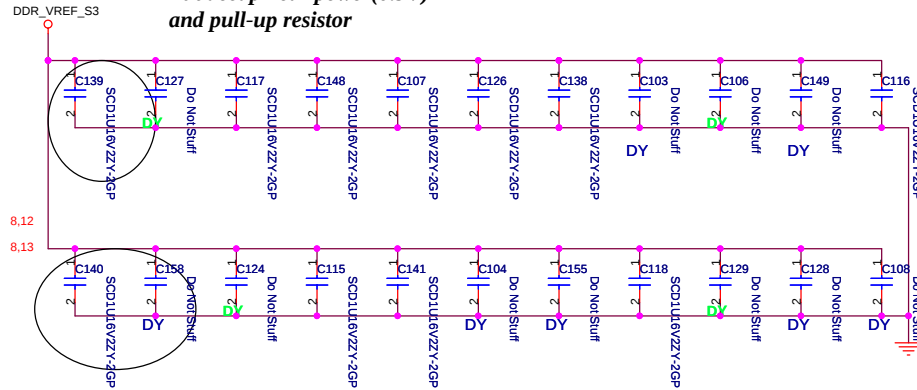
Put decap near power(0.9V) and pull-up resistor



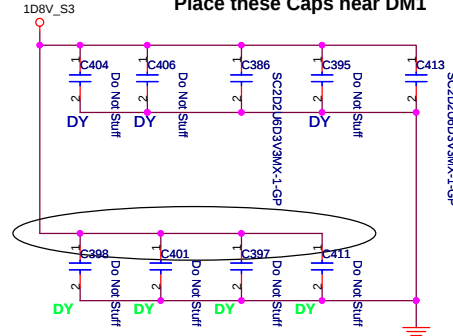
M_A_A[14..0] << M_A_A[14..0] 8,12
M_B_A[14..0] << M_B_A[14..0] 8,13

Decoupling Capacitor

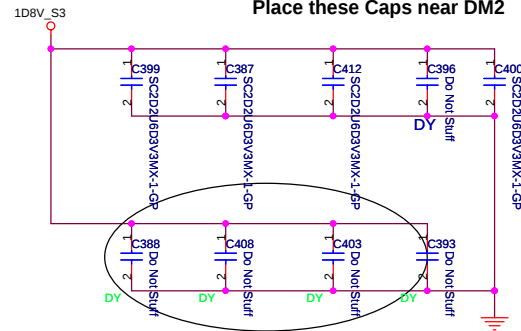
Put decap near power(0.9V) and pull-up resistor



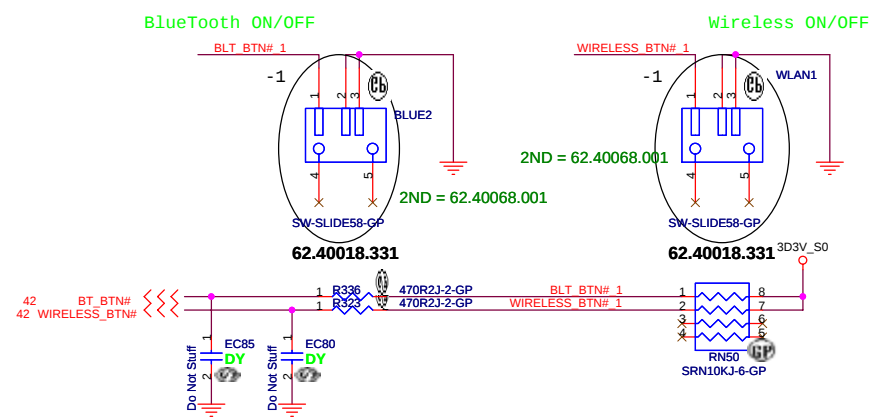
Place these Caps near DM1



Place these Caps near DM2

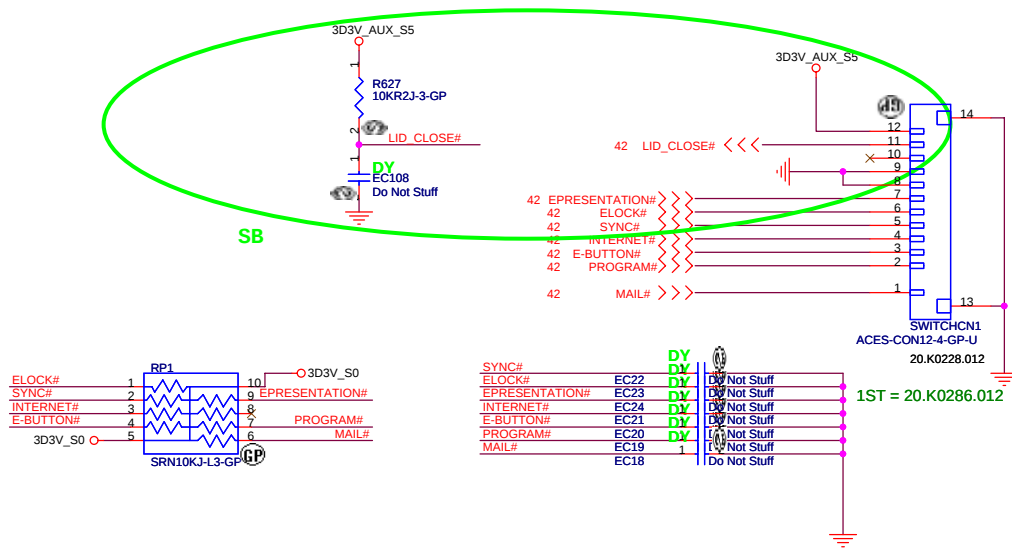


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970

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
SWITCH			
Size	Document Number		Rev
	Homa		-1
Date:	Thursday, April 03, 2008	Sheet 15 of	57

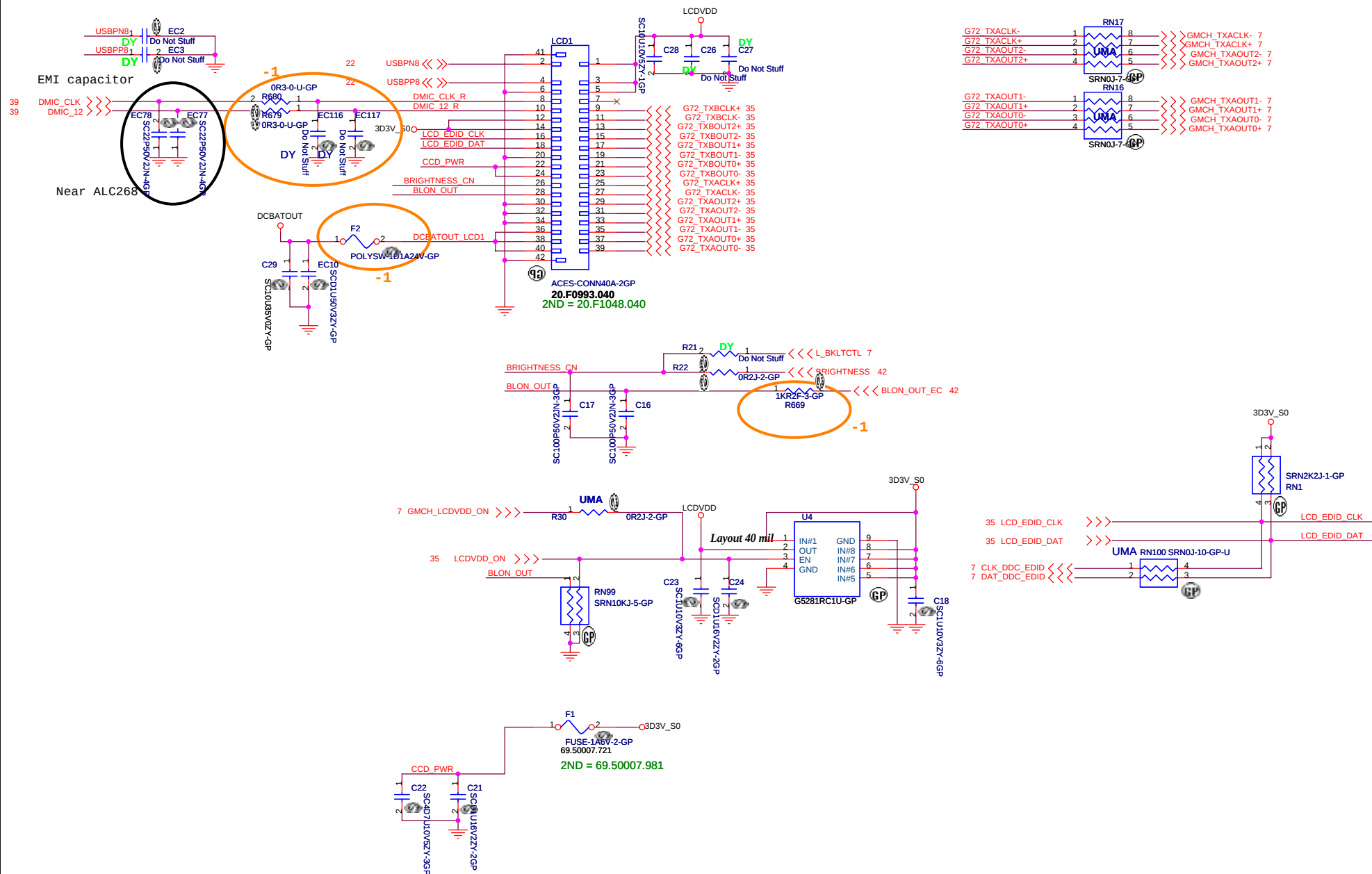


3D3V_AUX_S5	1	TP118	Do Not Stuff
LID_CLOSE#	1	TP121	Do Not Stuff
SYNC#	1	TP120	Do Not Stuff
ELOCK#	1	TP122	Do Not Stuff
EPRESENTATION#	1	TP124	Do Not Stuff
INTERNET#	1	TP123	Do Not Stuff
E-BUTTON#	1	TP126	Do Not Stuff
PROGRAM#	1	TP125	Do Not Stuff
MAIL#	1	TP127	Do Not Stuff

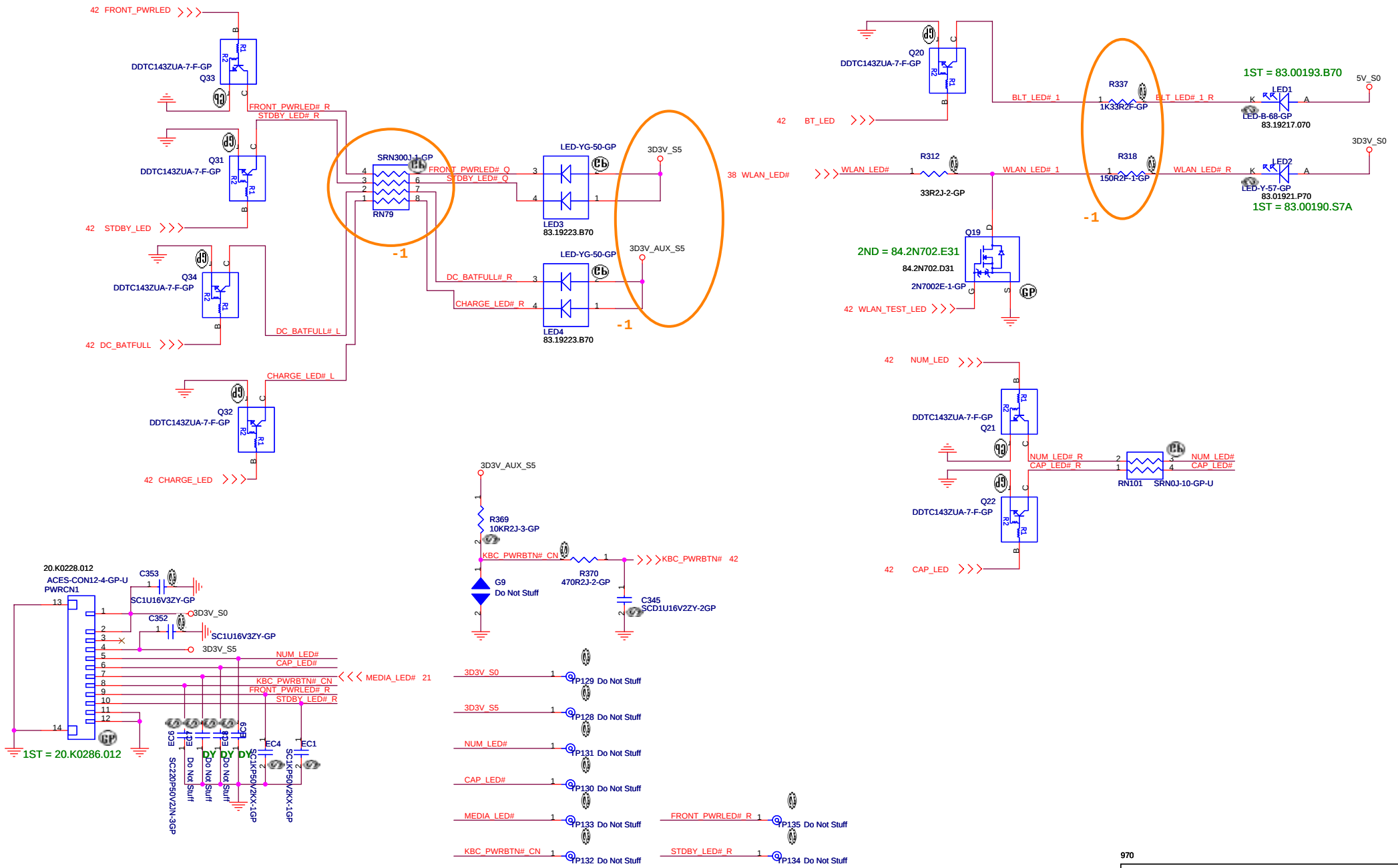
SYNC#	DY	Do Not Stuff
ELOCK#	EC22	Do Not Stuff
EPRESENTATION#	EC23	Do Not Stuff
INTERNET#	EC24	Do Not Stuff
E-BUTTON#	EC21	Do Not Stuff
PROGRAM#	EC20	Do Not Stuff
MAIL#	EC19	Do Not Stuff
	EC18	Do Not Stuff

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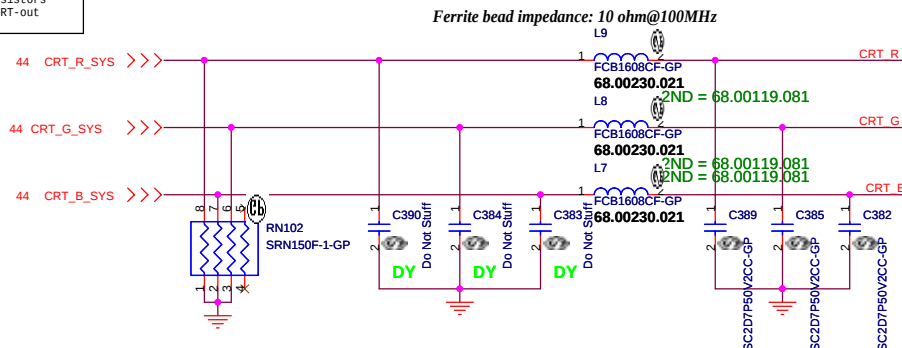
LCD/INVERTER/CCD CONN



LED

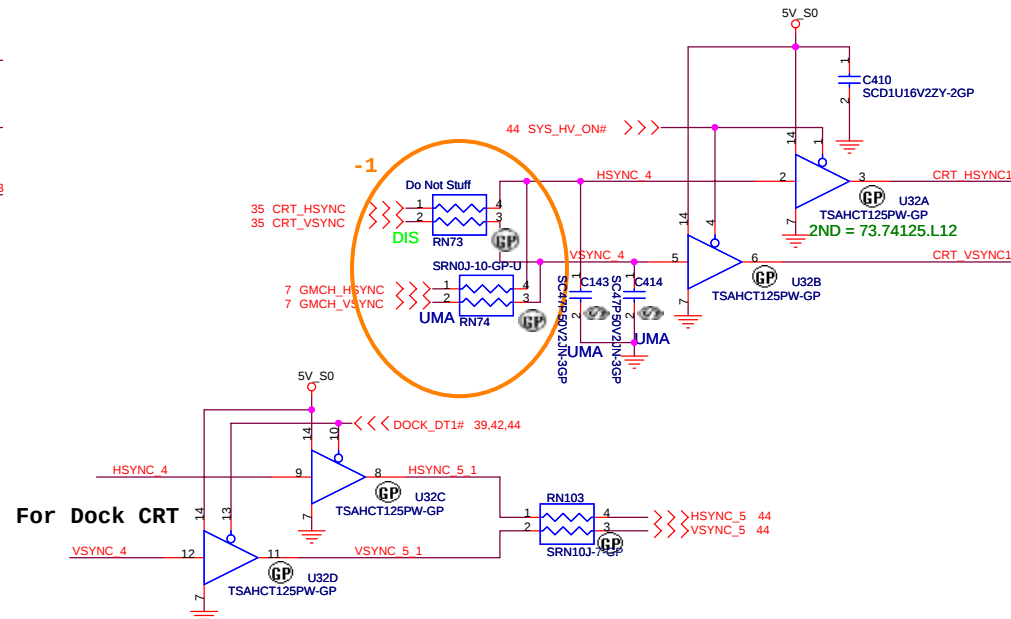


Layout Note:
Place these resistors
close to the CRT-out
connector

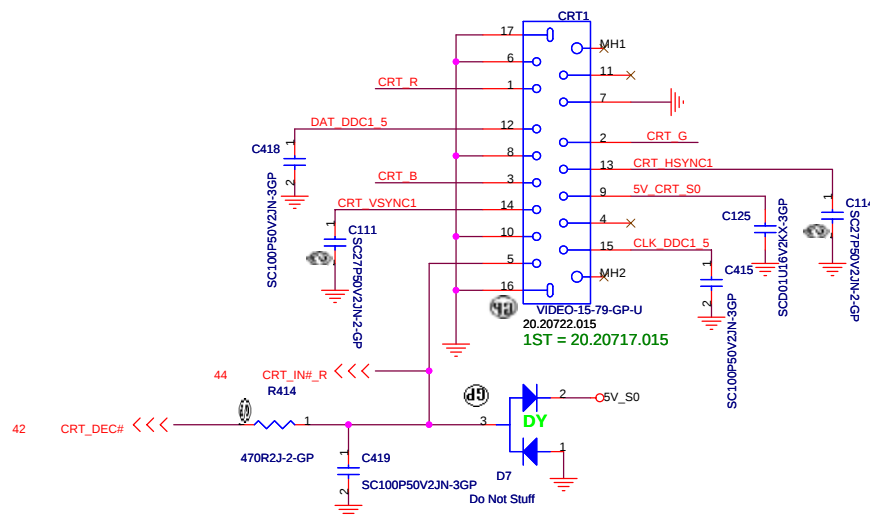


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

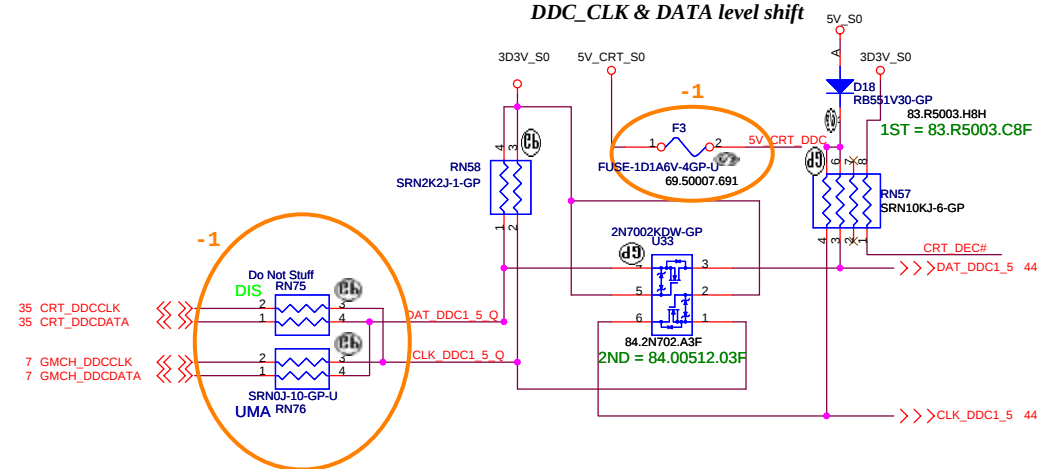
Hsync & Vsync level shift



CRT I/F & CONNECTOR



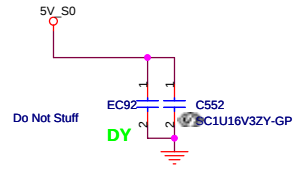
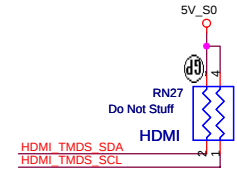
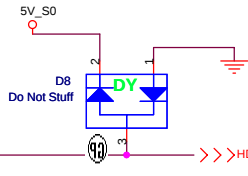
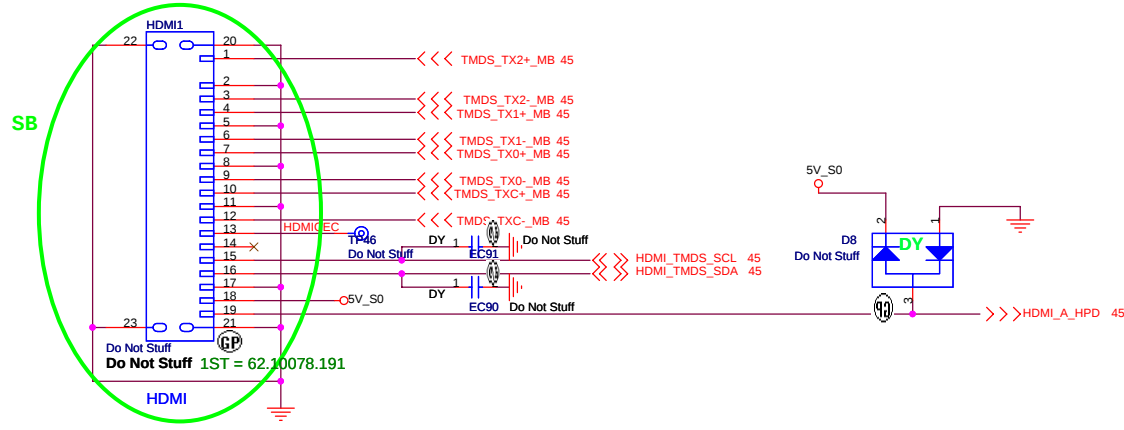
DDC_CLK & DATA level shift

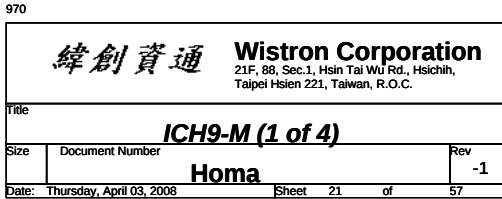


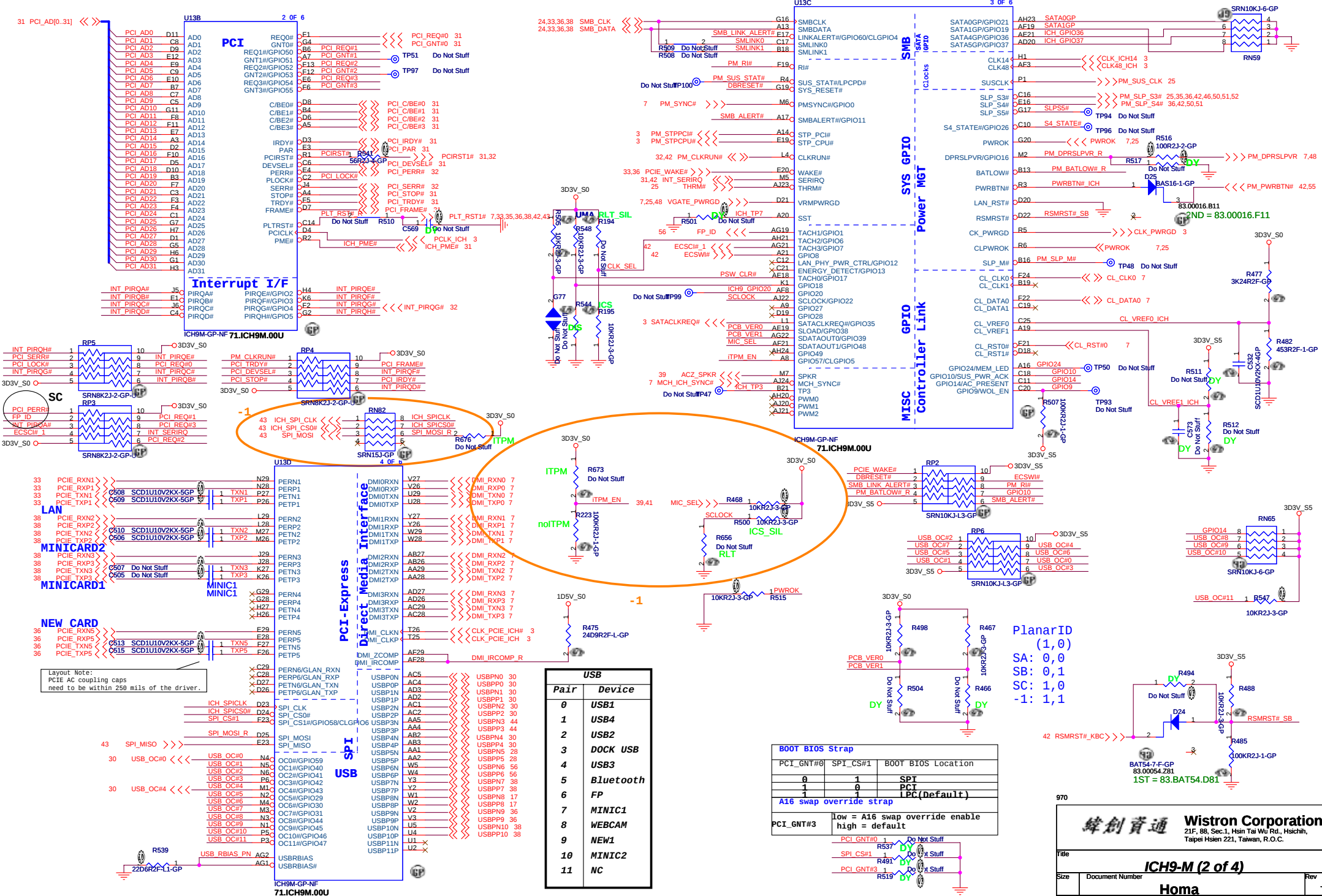
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		CRT Connector	
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USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	DOCK USB
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCI
1	1	LPC(default)
A16 swap override strap		
PCI_GNT#3	Low = A16 swap override enable high = default	

PlanarID
(1,0)
SA: 0,0
SB: 0,1
SC: 1,0
-1: 1,1

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

ICH9-M (2 of 4)

Homa

Title

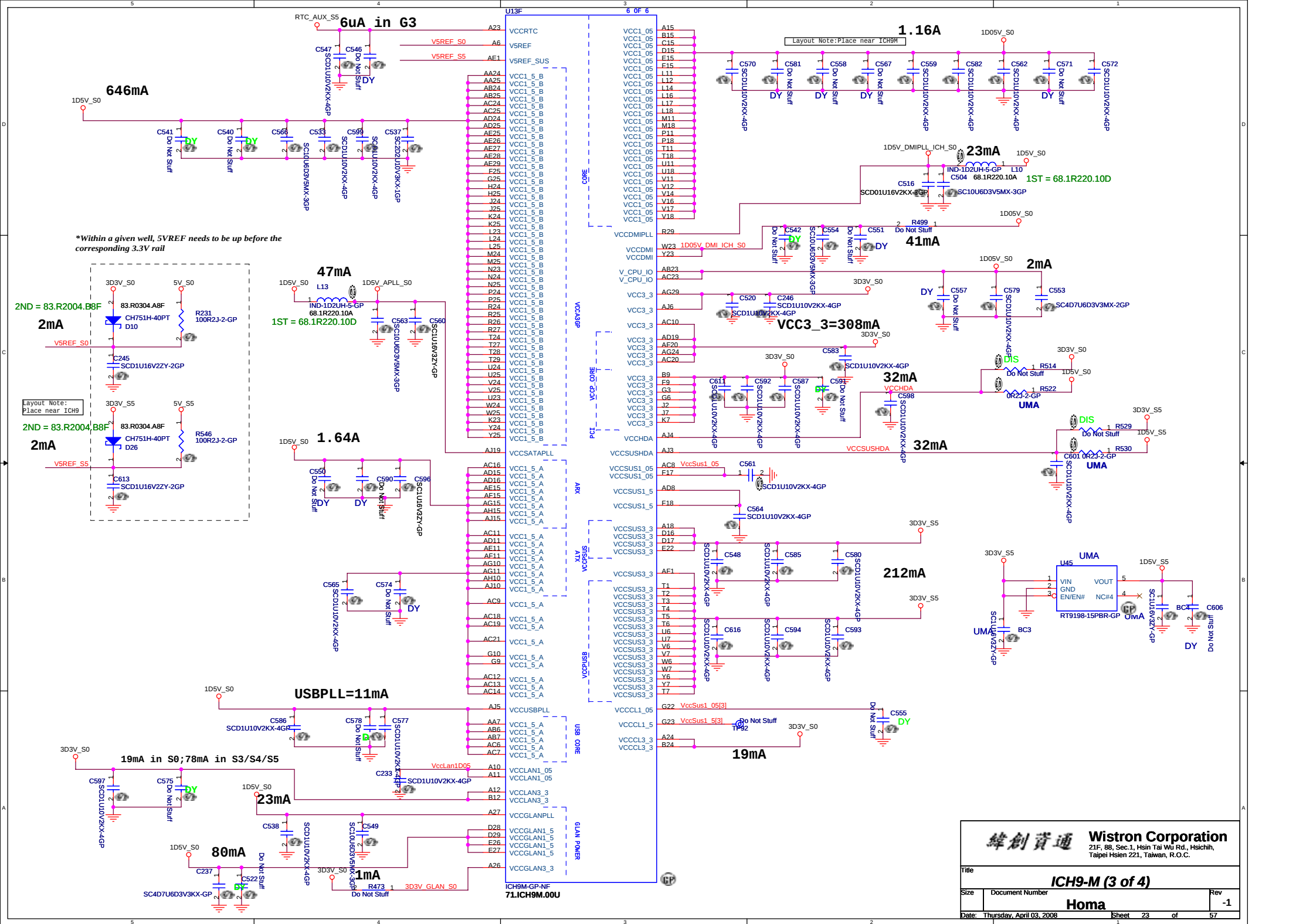
Size

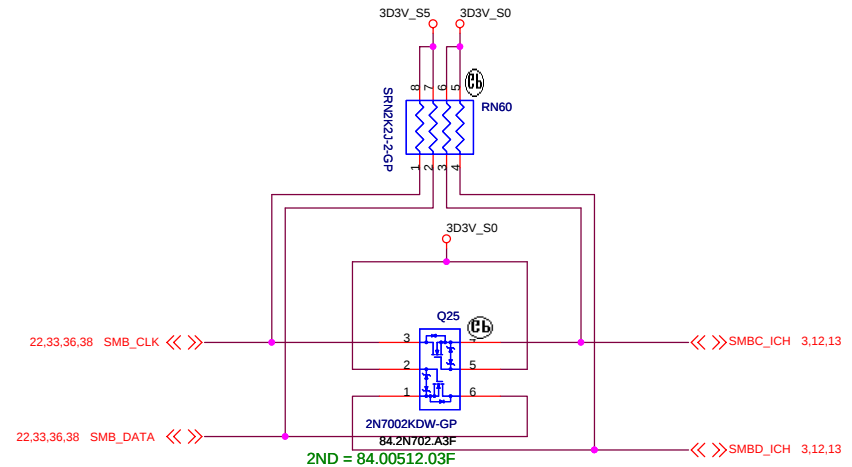
Document Number

Date: Thursday, April 03, 2008

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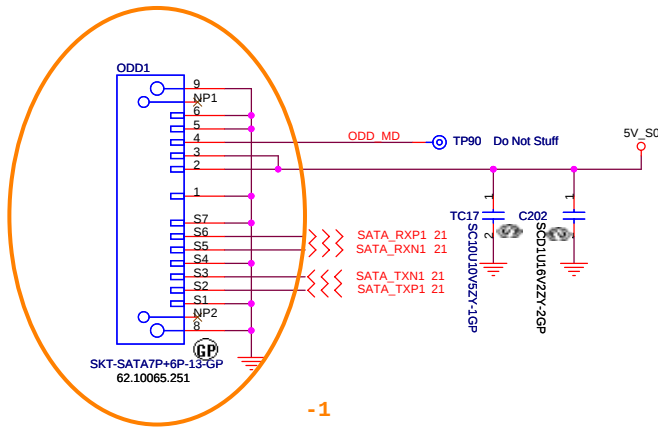
Rev -1





SMBUS

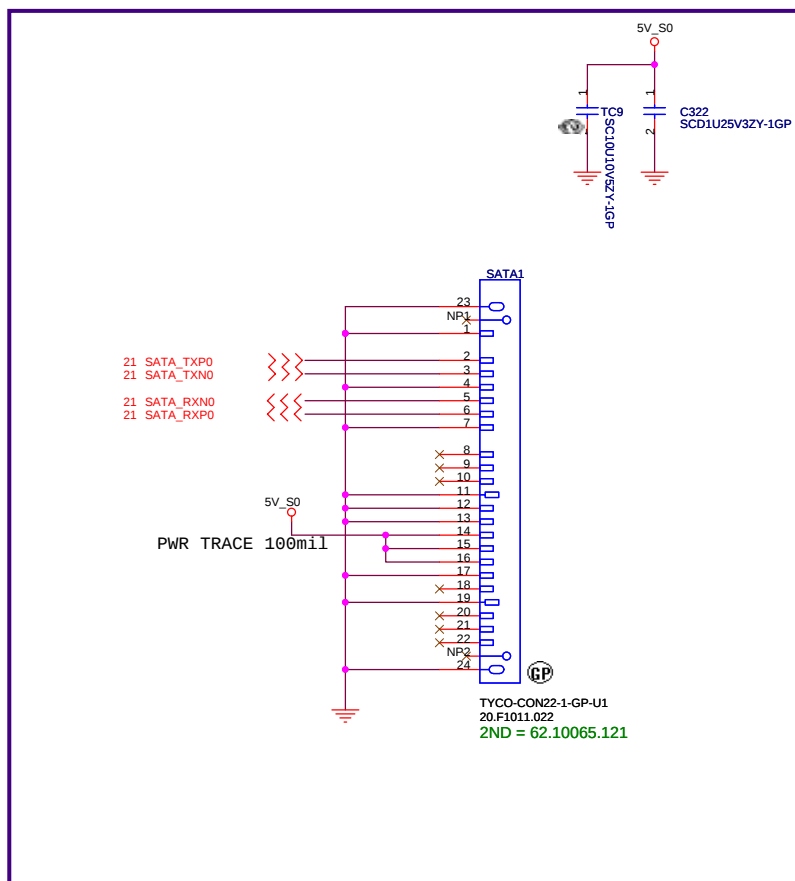
ODD Connector



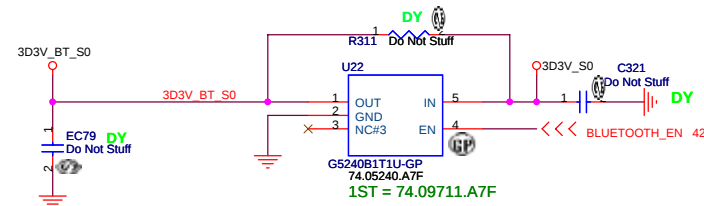
-1

970

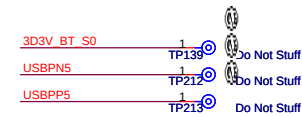
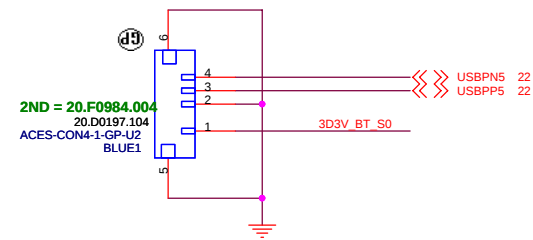
SATA Connector



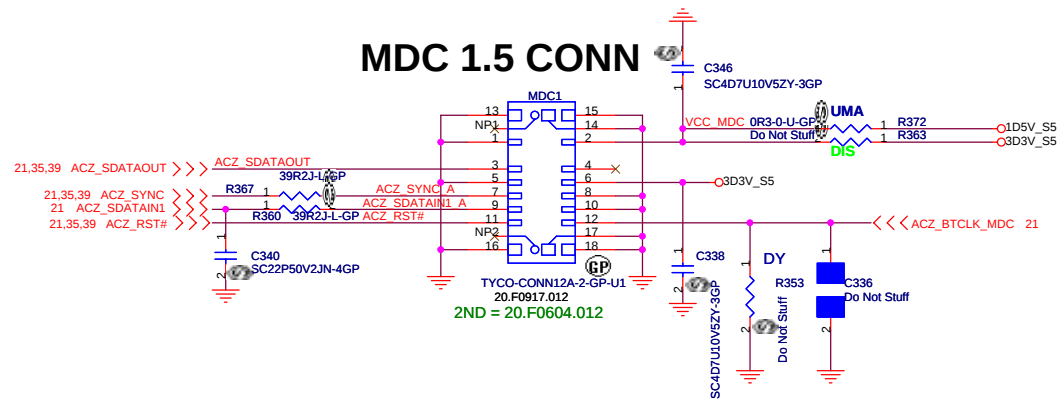
BLUETOOTH MODULE



EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

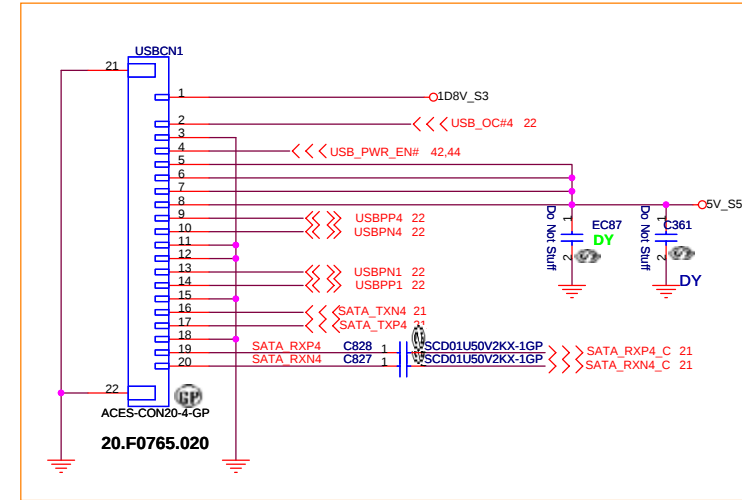
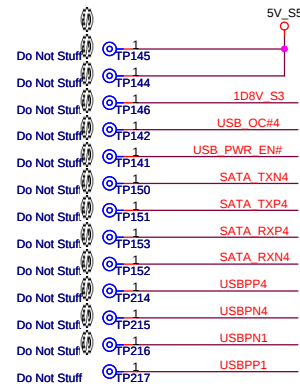
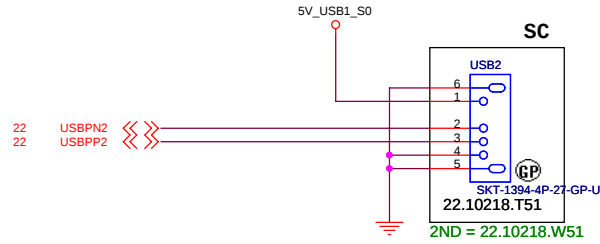
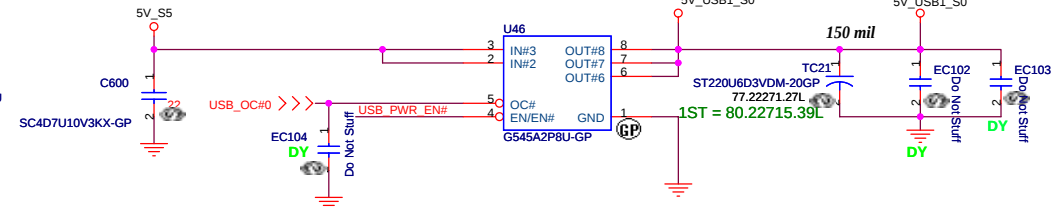
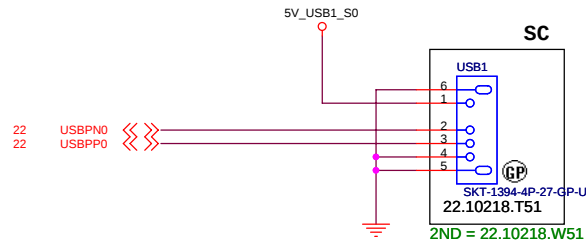


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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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MDC			
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22 PCI_AD[0..31]

<<<

- PCI_AD0 64
- PCI_AD1 63
- PCI_AD2 62
- PCI_AD3 61
- PCI_AD4 60
- PCI_AD5 59
- PCI_AD6 58
- PCI_AD7 57
- PCI_AD8 54
- PCI_AD9 53
- PCI_AD10 52
- PCI_AD11 51
- PCI_AD12 50
- PCI_AD13 49
- PCI_AD14 47
- PCI_AD15 46
- PCI_AD16 37
- PCI_AD17 36
- PCI_AD18 35
- PCI_AD19 34
- PCI_AD20 32
- PCI_AD21 31
- PCI_AD22 30
- PCI_AD23 29
- PCI_AD24 27
- PCI_AD25 25
- PCI_AD26 24
- PCI_AD27 23
- PCI_AD28 22
- PCI_AD29 21
- PCI_AD30 20
- PCI_AD31 19

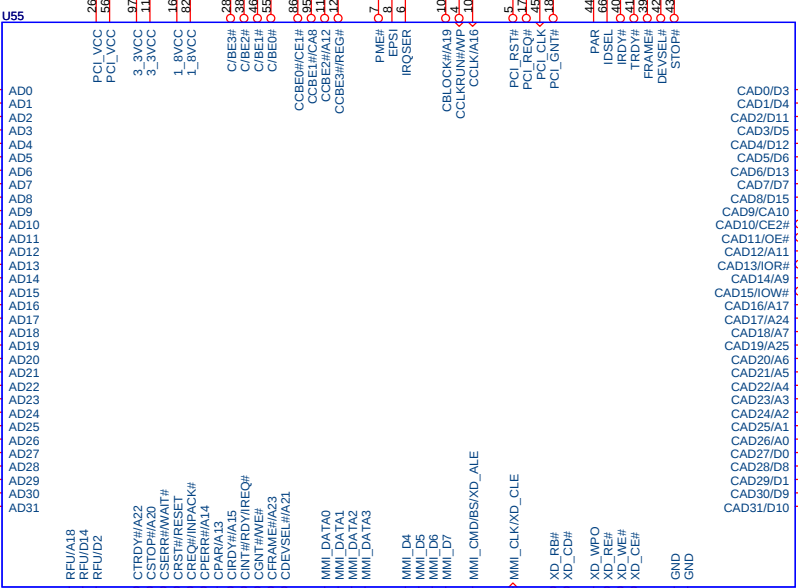
OZ711MZ0TN-GP-U1
71.00711.A0G

37 CBB_A18

37 CBB_D14

37 CBB_D2

- CBB_A22 37
- CBB_A20 37
- CBB_WAIT# 37
- CBB_RESET 37
- CBB_INPACK# 37
- CBB_A14 37
- CBB_A13 37
- CBB_A15 37
- CBB_RDY 37
- CBB_WE# 37
- CBB_A23 37
- CBB_A21 37
- MMI_D0 32
- MMI_D1 32
- MMI_D2 32
- MMI_D3 32

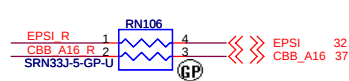


- CAD0/D3 76
- CAD1/D4 77
- CAD2/D11 78
- CAD3/D5 79
- CAD4/D12 80
- CAD5/D6 81
- CAD6/D13 83
- CAD7/D7 84
- CAD8/D15 87
- CAD9/CA10 88
- CAD10/CE2# 89
- CAD11/OE# 90
- CAD12/A11 91
- CAD13/IOR# 92
- CAD14/A9 93
- CAD15/IOW# 94
- CAD16/A17 96
- CAD17/A24 112
- CAD18/A7 113
- CAD19/A25 114
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- CAD21/A5 116
- CAD22/A4 118
- CAD23/A3 120
- CAD24/A2 122
- CAD25/A1 124
- CAD26/A0 125
- CAD27/D0 126
- CAD28/D8 127
- CAD29/D1 128
- CAD30/D9 1
- CAD31/D10 3

- CBB_D3 37
- CBB_D4 37
- CBB_D11 37
- CBB_D5 37
- CBB_D12 37
- CBB_D6 37
- CBB_D13 37
- CBB_D7 37
- CBB_D15 37
- CBB_A10 37
- CBB_CE2# 37
- CBB_OE# 37
- CBB_A11 37
- CBB_IORD# 37
- CBB_A9 37
- CBB_IOWR# 37
- CBB_A17 37
- CBB_A24 37
- CBB_A7 37
- CBB_A25 37
- CBB_A6 37
- CBB_A5 37
- CBB_A4 37
- CBB_A3 37
- CBB_A2 37
- CBB_A1 37
- CBB_A0 37
- CBB_D0 37
- CBB_D8 37
- CBB_D1 37
- CBB_D9 37
- CBB_D10 37

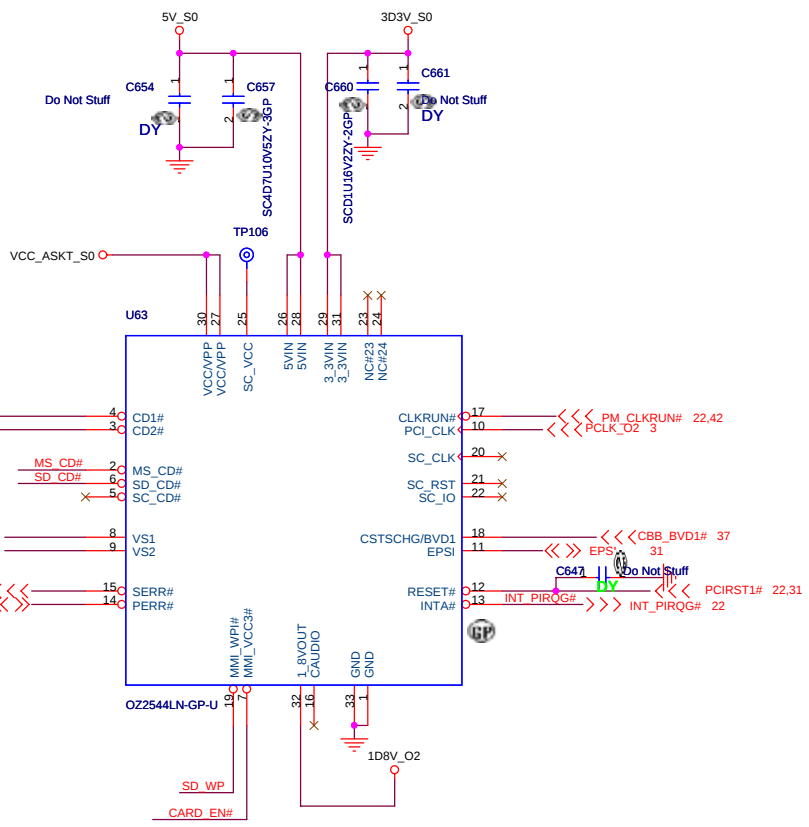
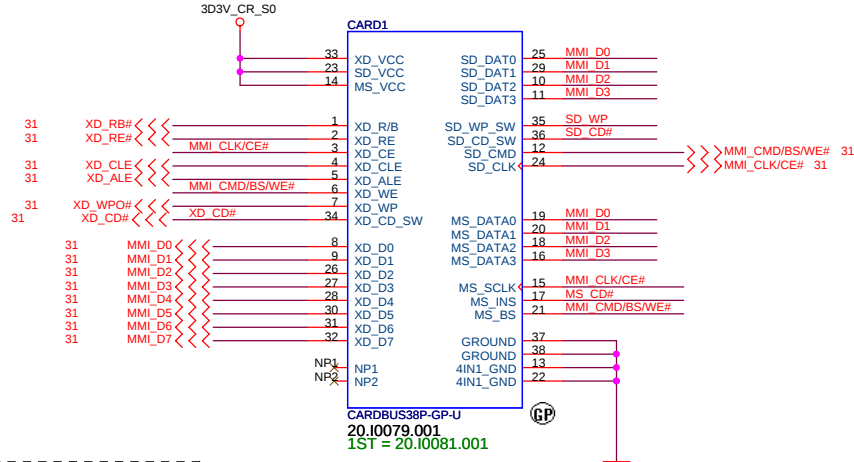
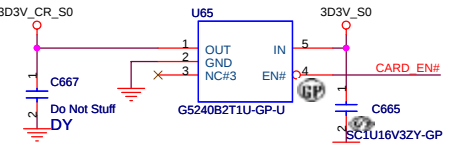
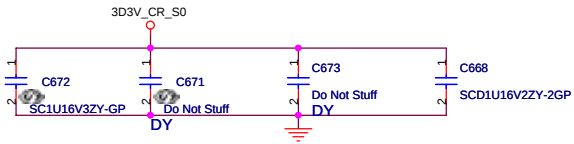
- MMI_DATA0 9
- MMI_DATA1 10
- MMI_DATA2 12
- MMI_DATA3 13
- MMI_D4 75
- MMI_D5 74
- MMI_D6 73
- MMI_D7 72
- MMI_CMD/BS/XD_ALE 14
- MMI_CLK/XD_CLE 15
- XD_RE# 68
- XD_CD# 66
- XD_WPO# 67
- XD_RE# 69
- XD_WE# 70
- XD_CE# 71
- GND 108
- GND 33

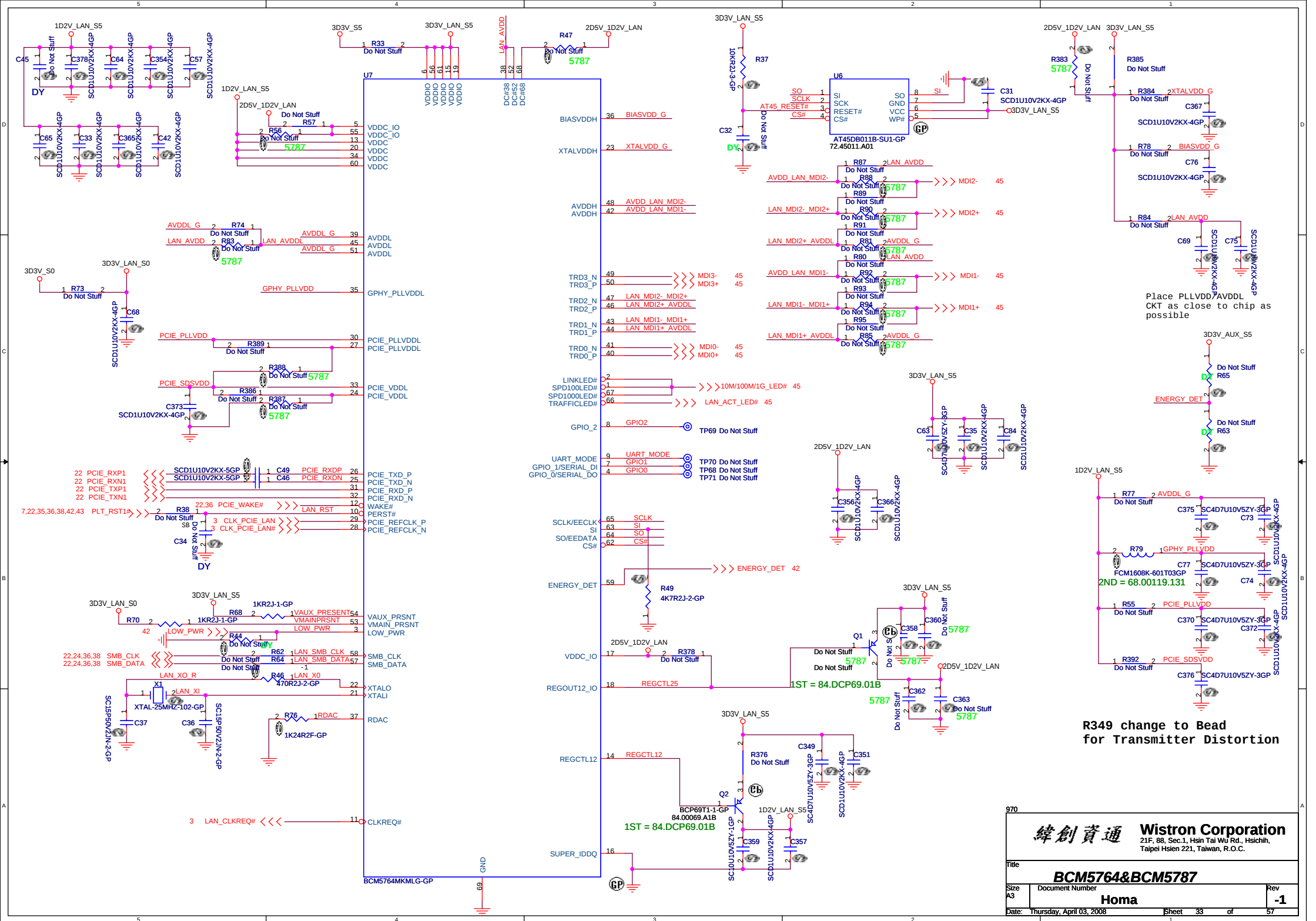
- <<< XD_ALE 32
- <<< XD_CLE 32
- <<< XD_RE# 32
- <<< XD_WPO# 32
- <<< XD_CD# 32
- <<< XD_RB# 32
- <<< MMI_CLK/CE# 32
- <<< MMI_CMD/BS/WE# 32
- <<< MMI_D7 32
- <<< MMI_D6 32
- <<< MMI_D5 32
- <<< MMI_D4 32



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XD
MS / MS PRO
SD / SD IO / MMC



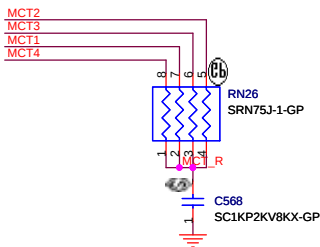
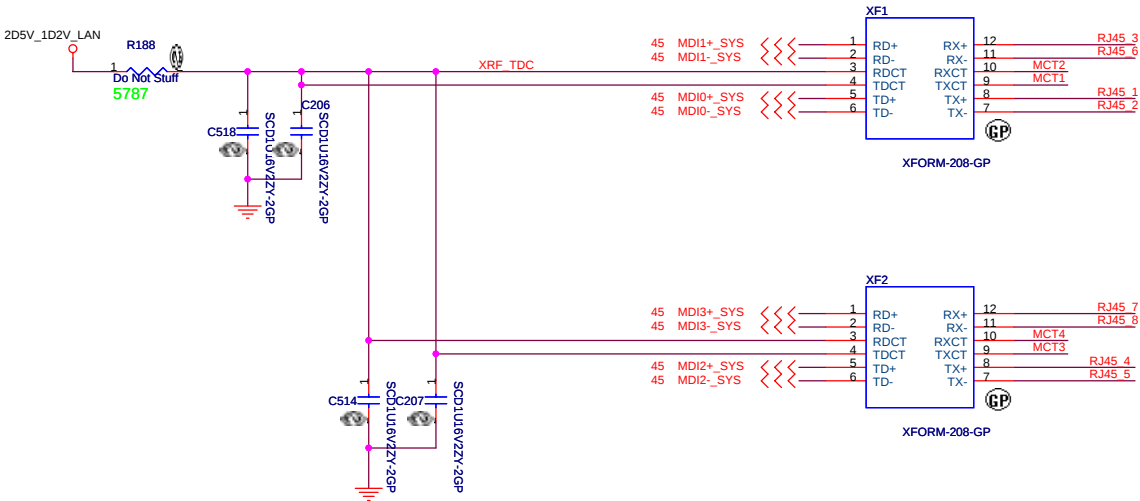


R349 change to Bead
for Transmitter Distortion

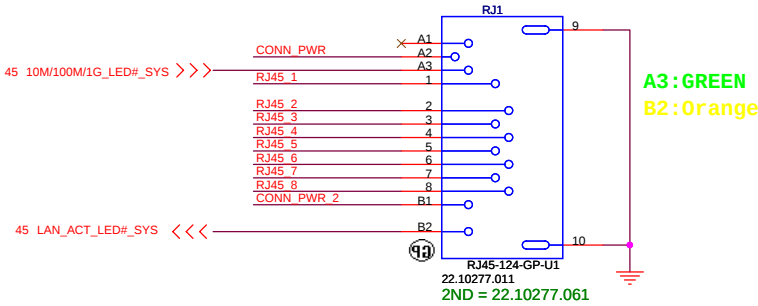
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

GIGA Lan Transformer

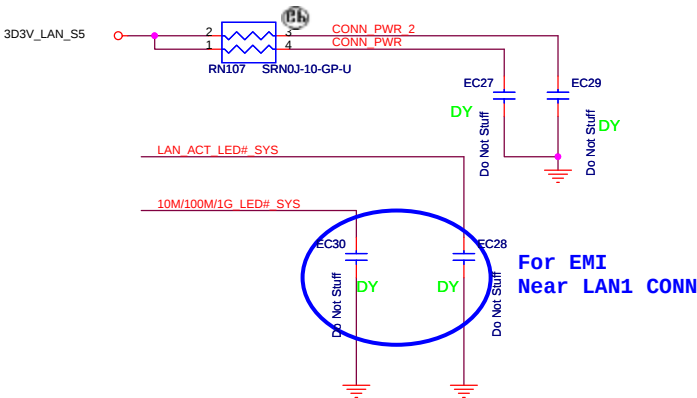


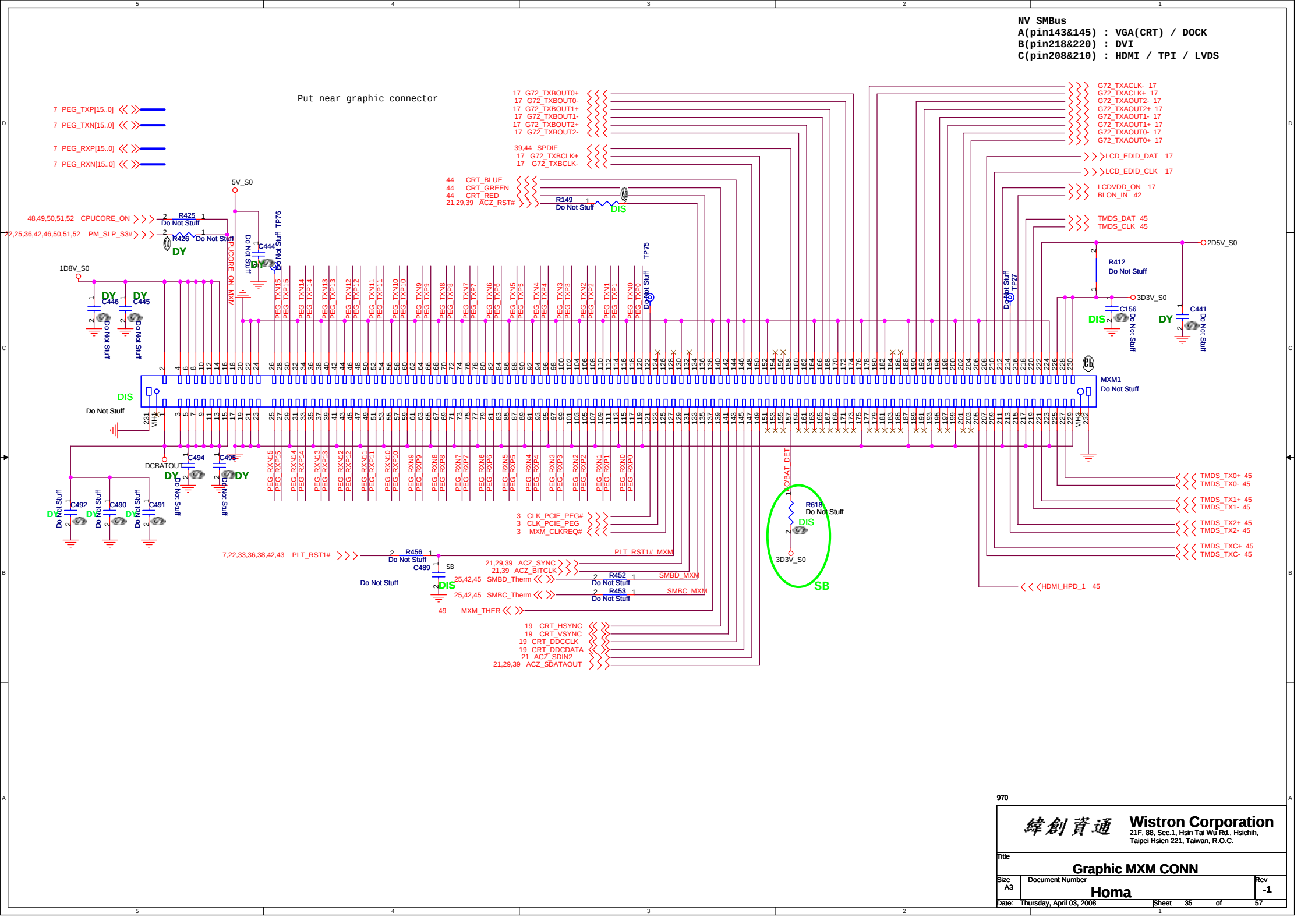
LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

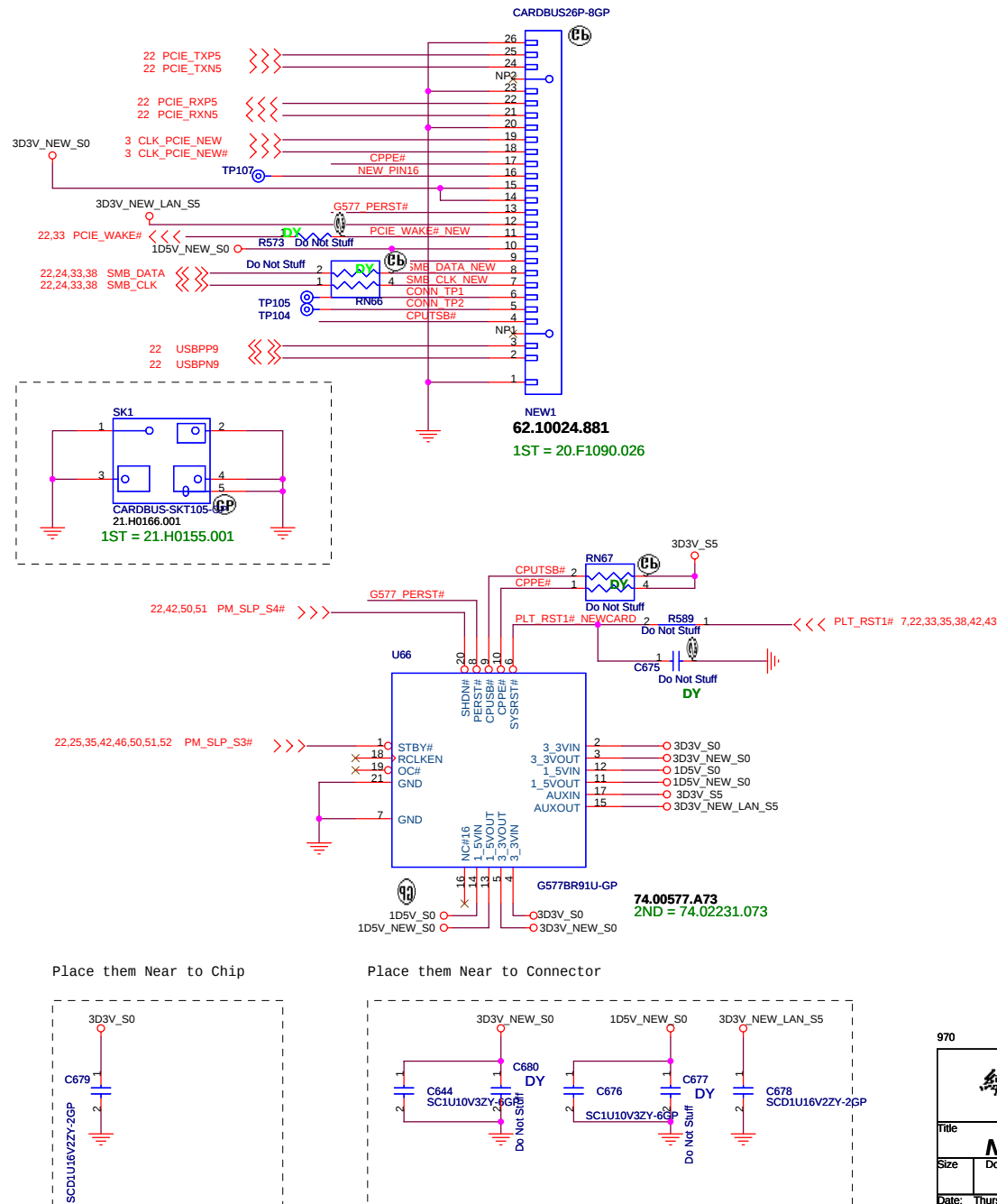




NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

NEWCARD Connector

Reserve the symbol
for bottom side
connector

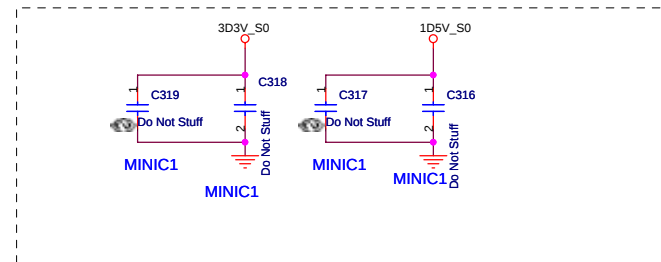
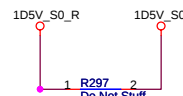


970

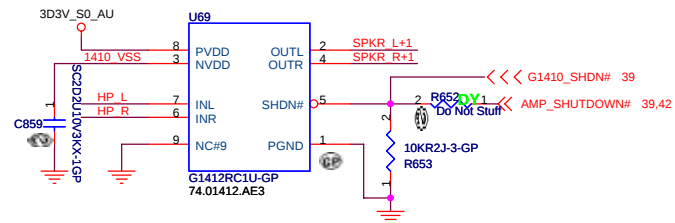
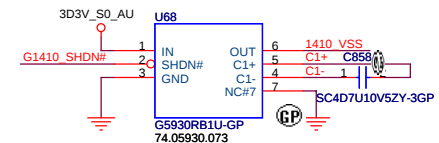
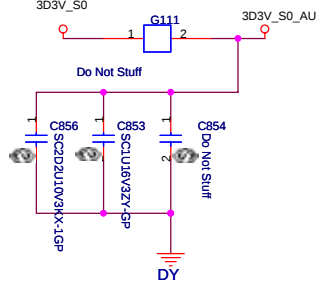
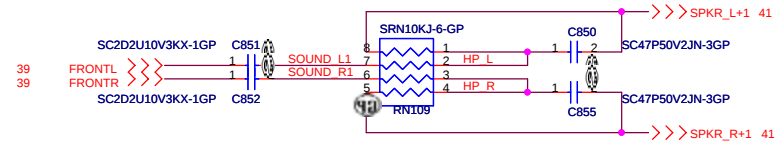
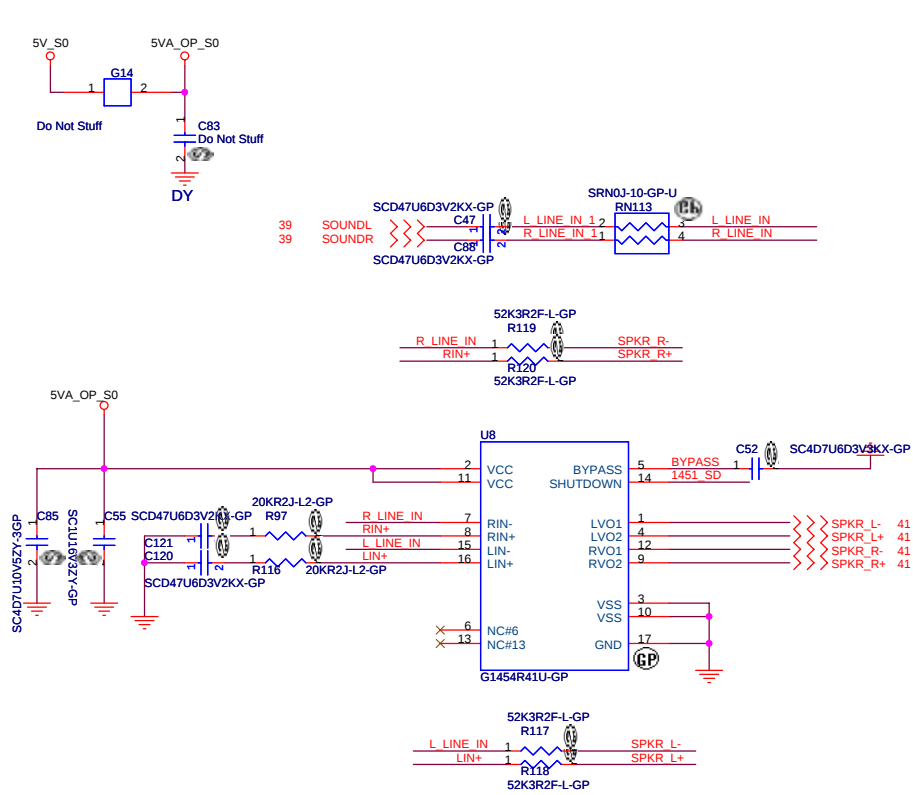
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

NEW CARD		
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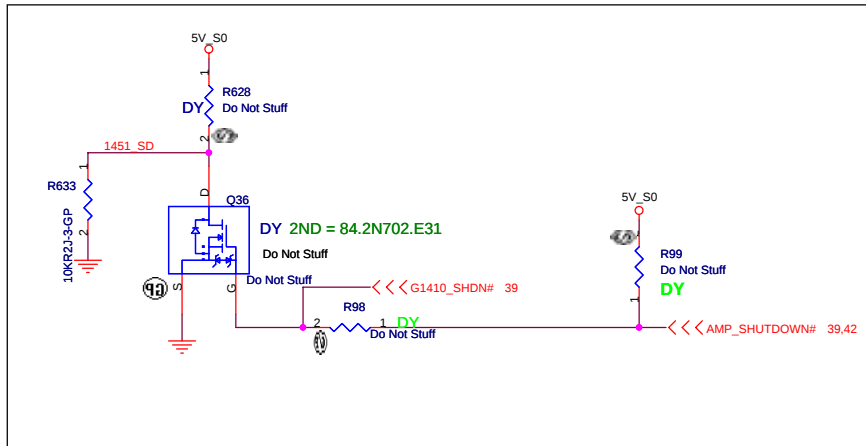
Mini Card Connector



AUDIO OP AMPLIFIER

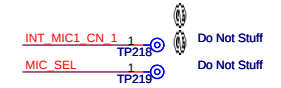
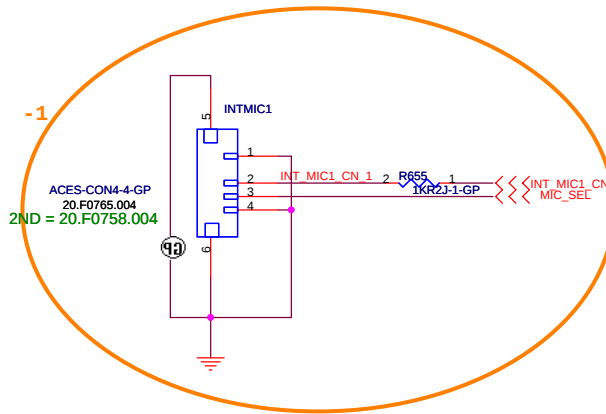
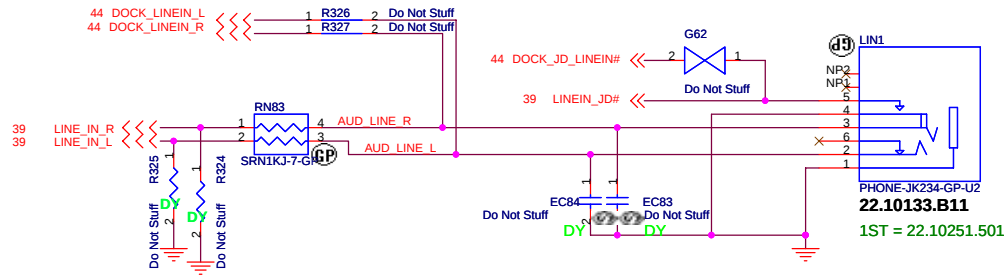


SC

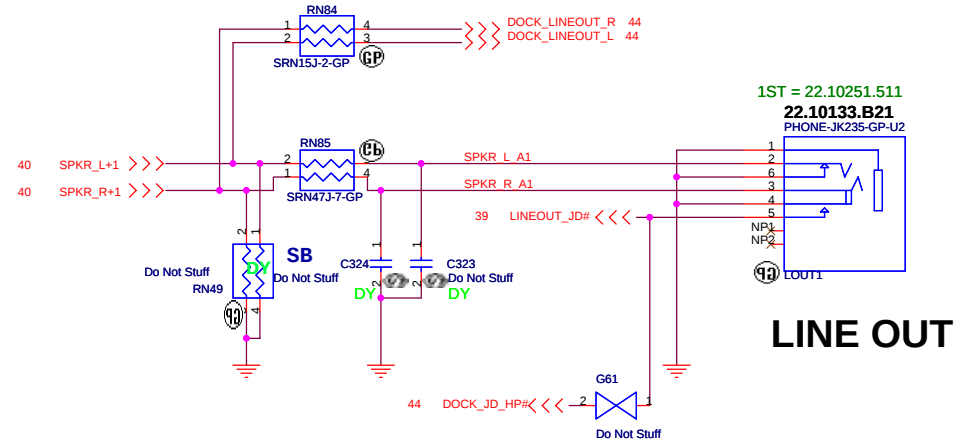
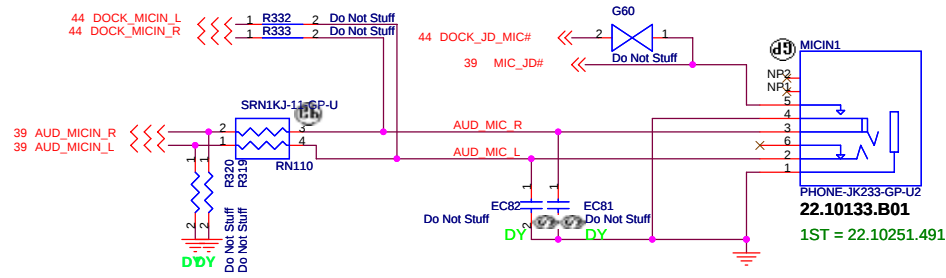


970

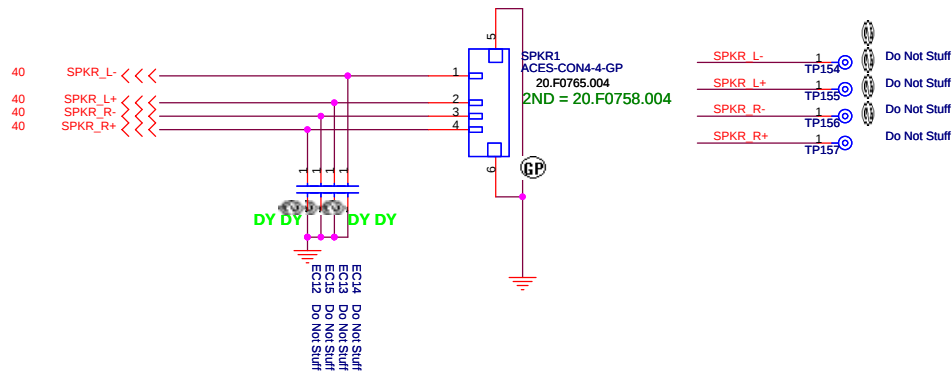
LINE IN



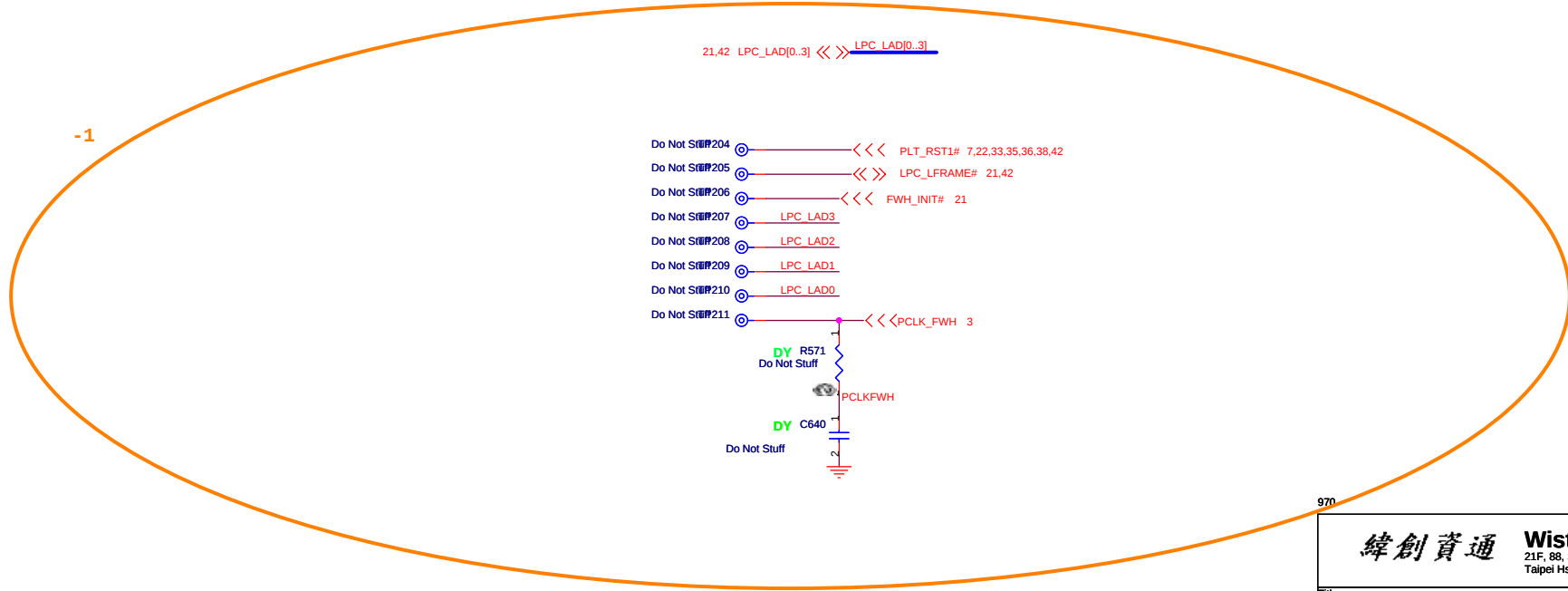
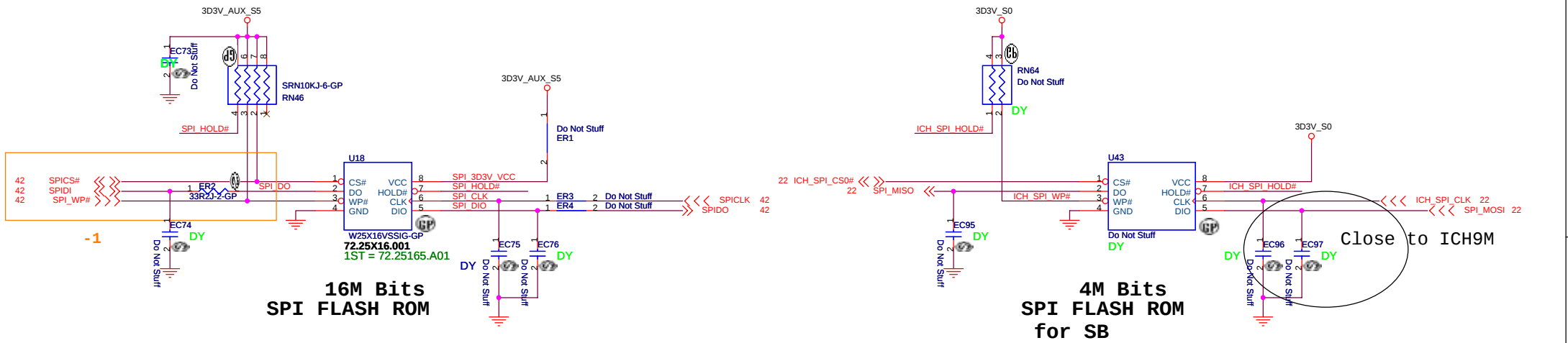
MIC IN



Internal Speaker

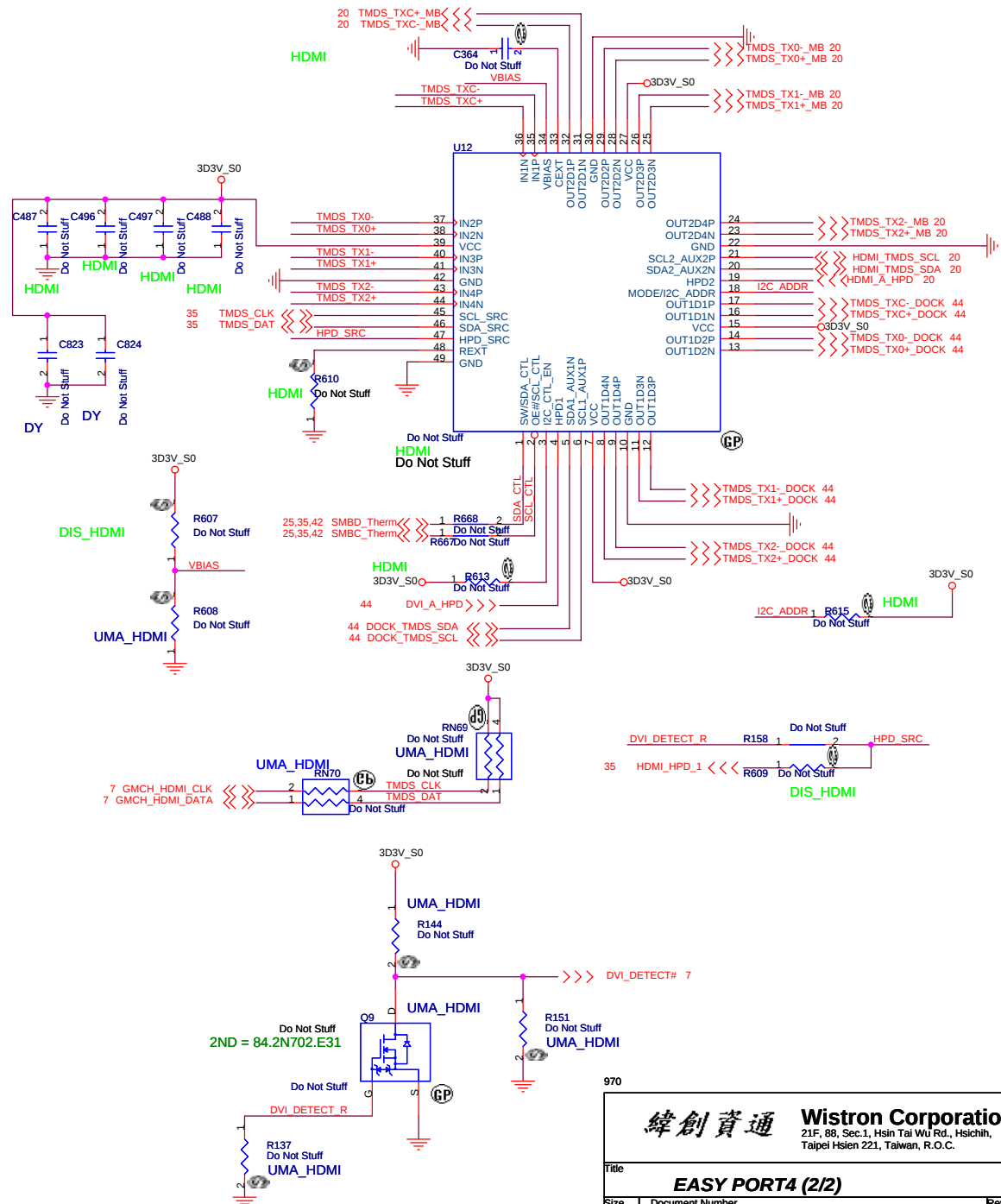
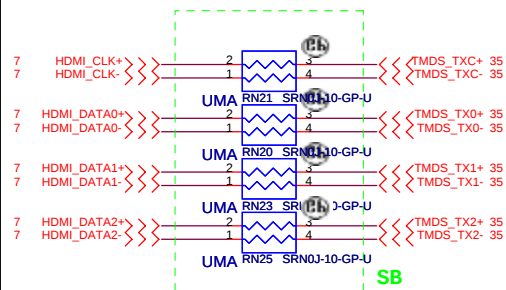
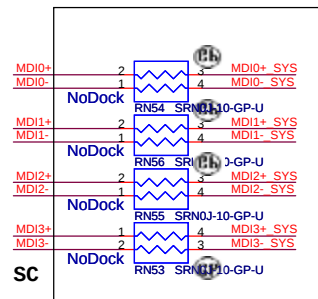
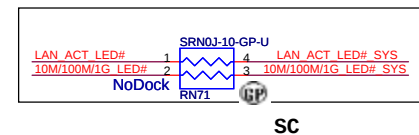
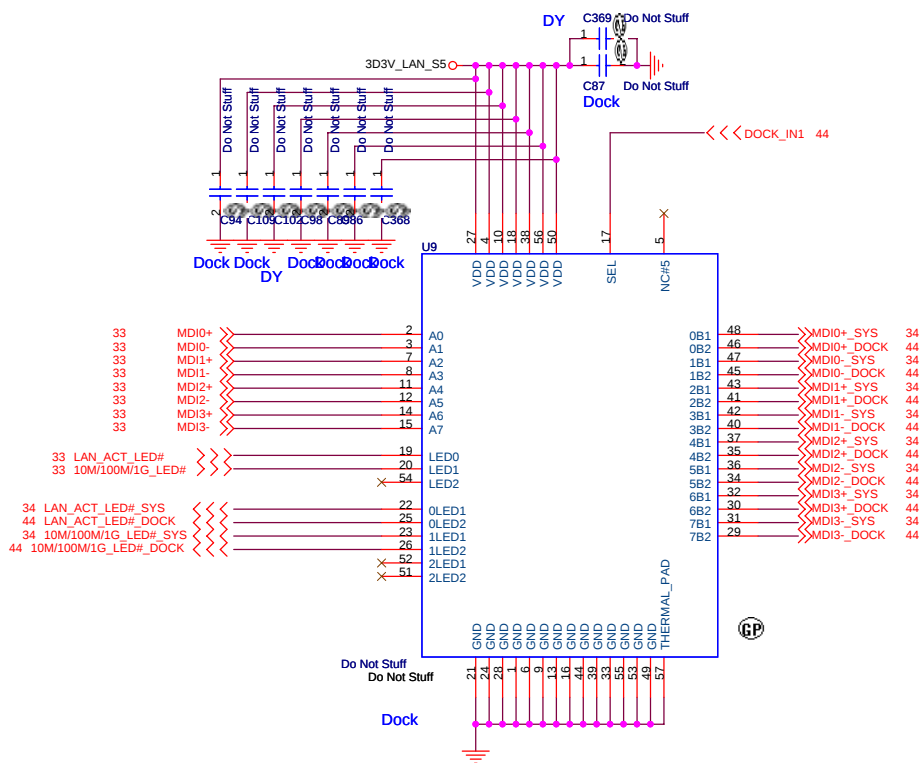


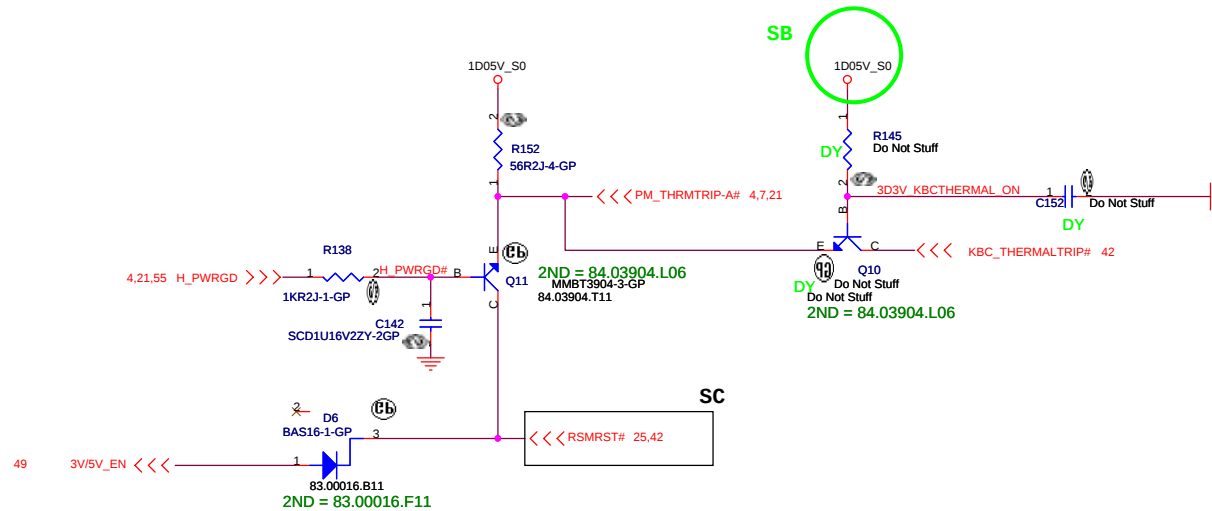
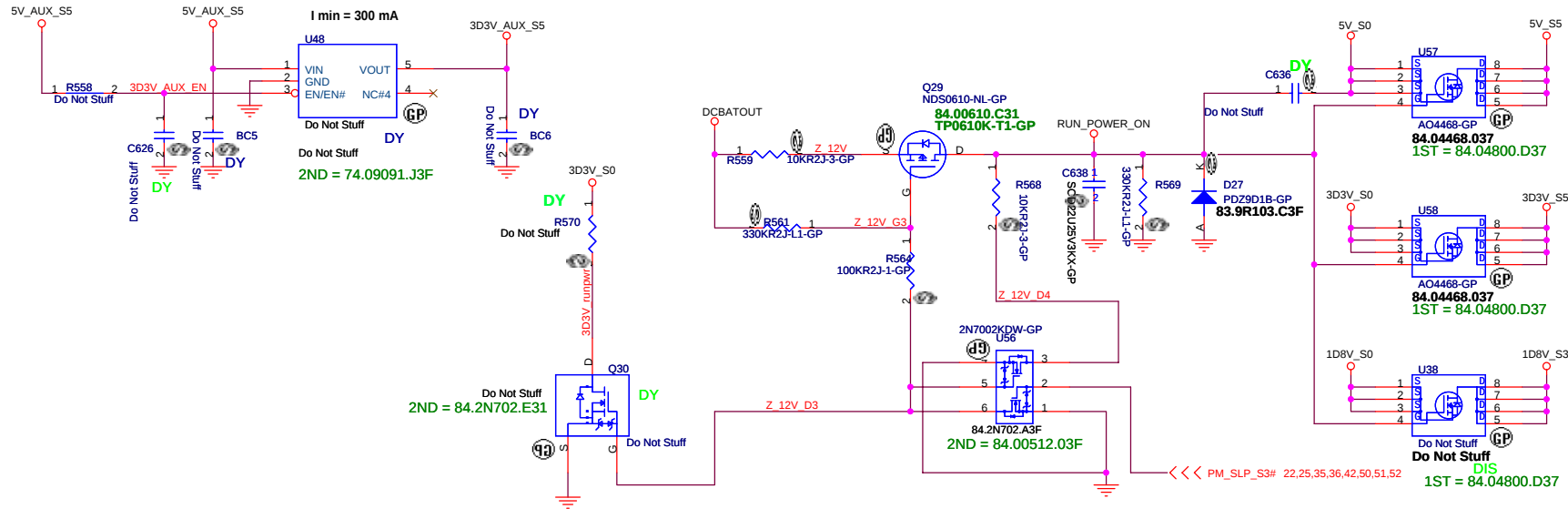
970





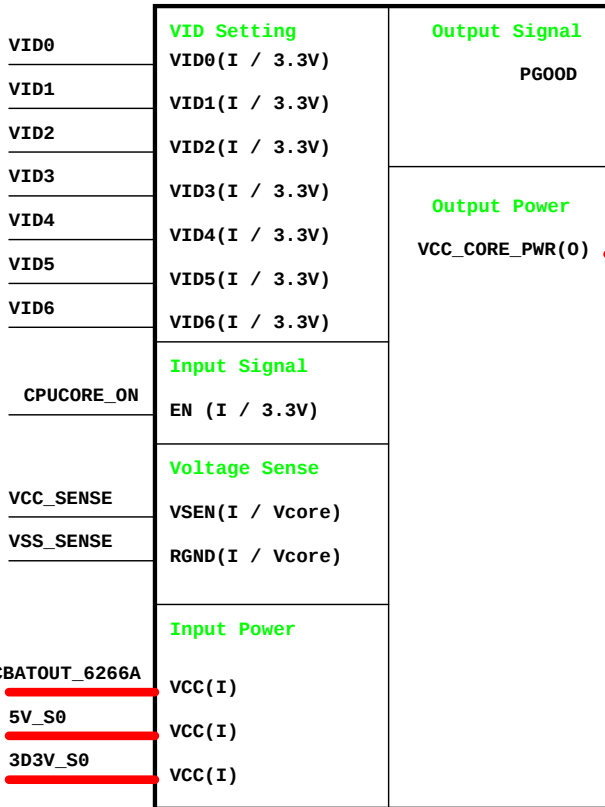
LAN switch



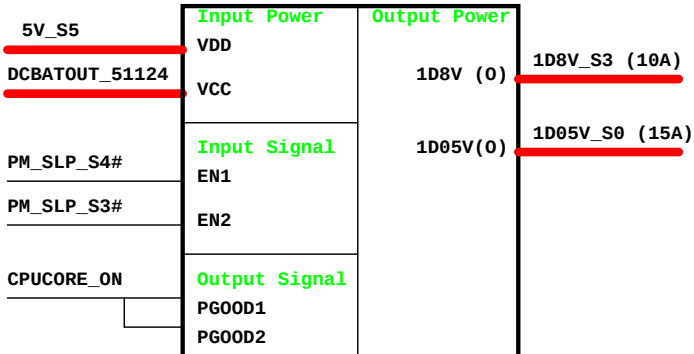


970

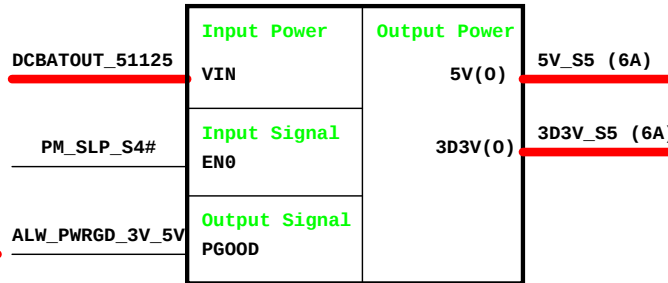
CPU_CORE
ISL6266A



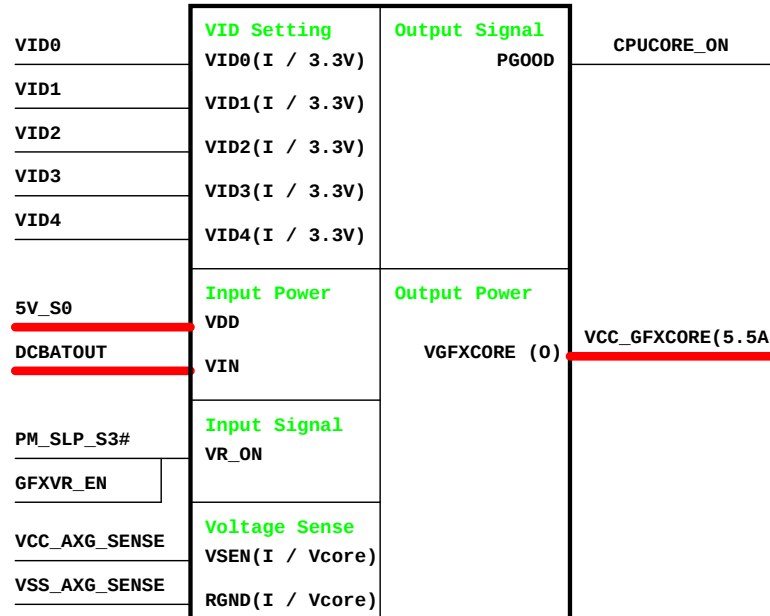
TPS51124
1D8V/1D05V



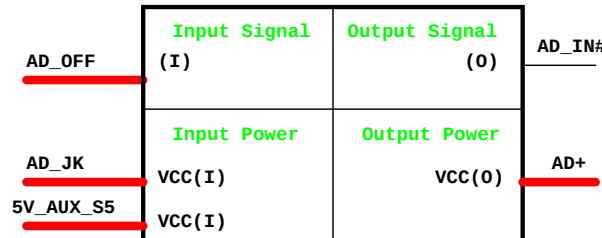
TPS51125
5V/3D3V



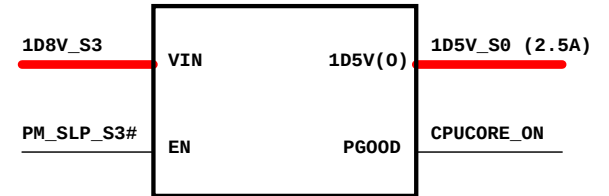
GFX_CORE
ISL6263A



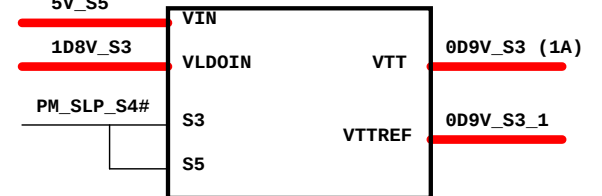
Adapter



RT9018A
1D5V_S0



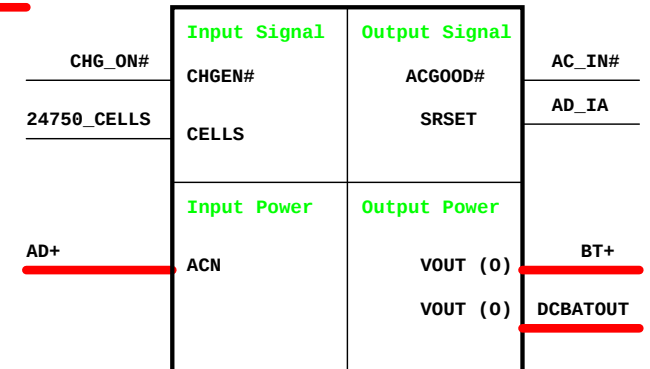
RT9026 0D9V_S0

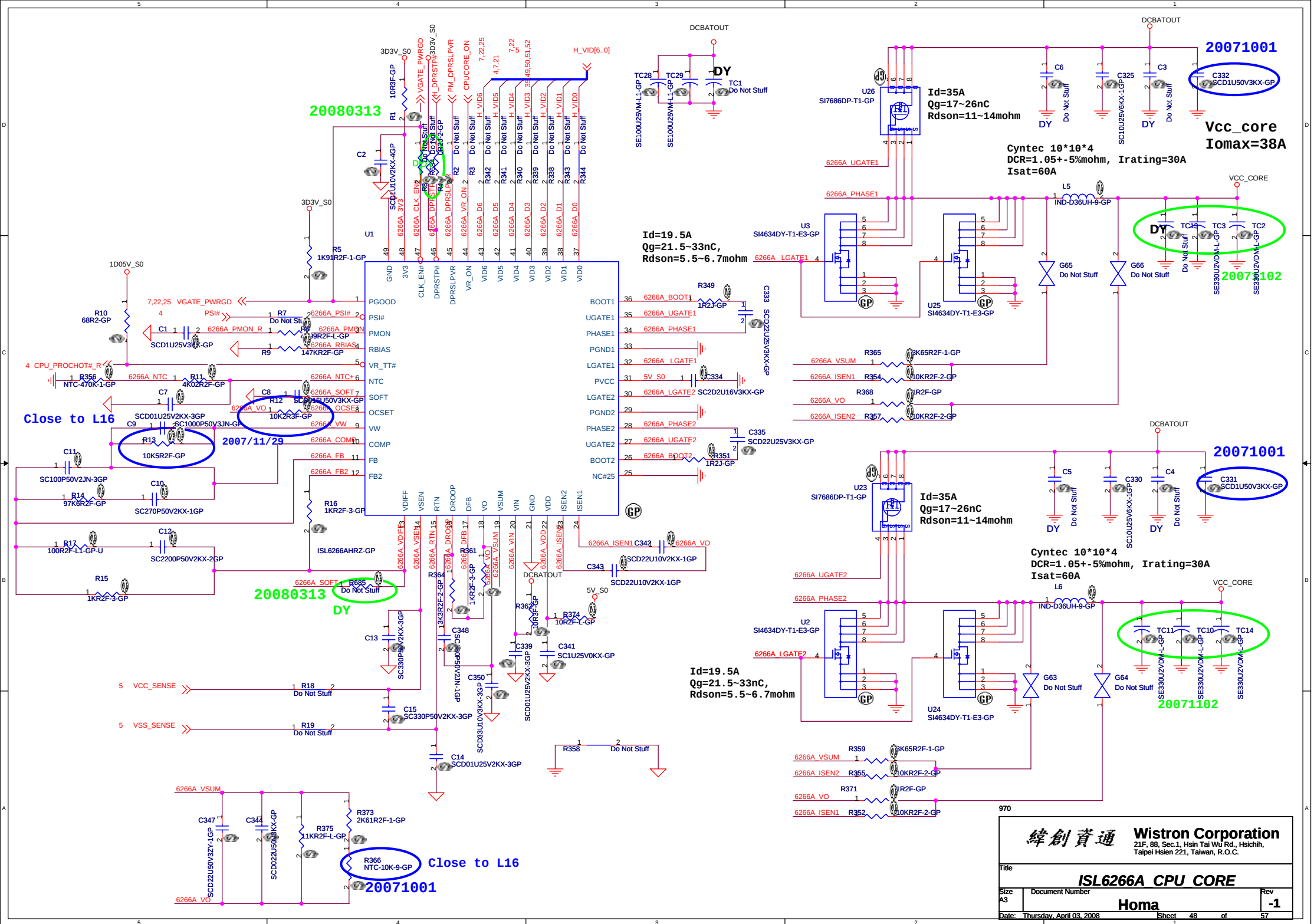


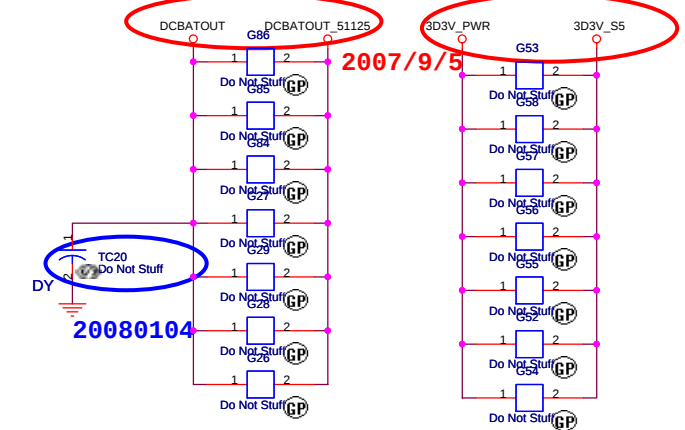
G9131 2D5V_S0



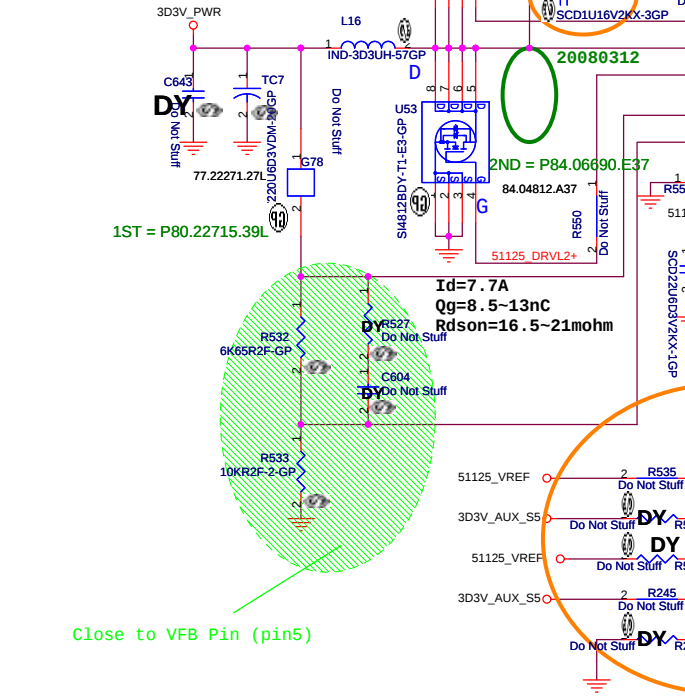
Charger BQ24750







Design Current = 6A
 Max Current = 7A
 OCP min = 10A
 Cyntec 7*7*3
 DCR=30mohm, Irating=6A
 Isat=13.5A

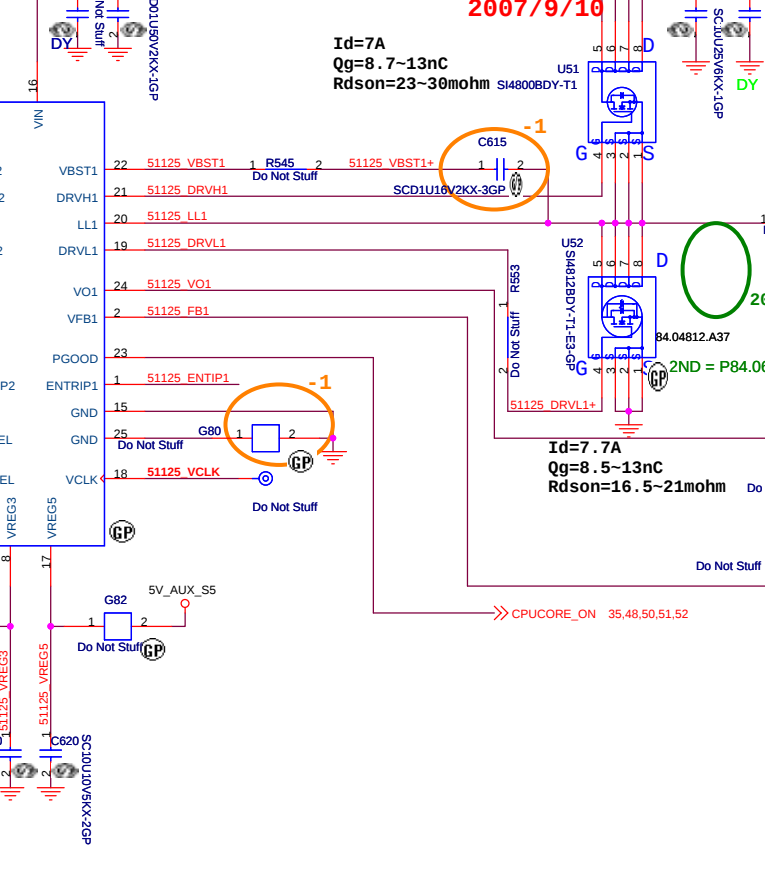
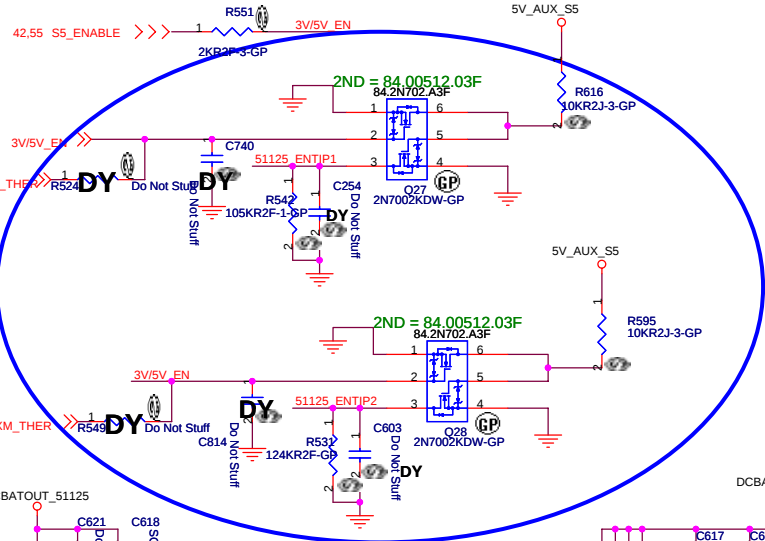


Close to VFB Pin (pin5)

2007/1/2

2007/9/10

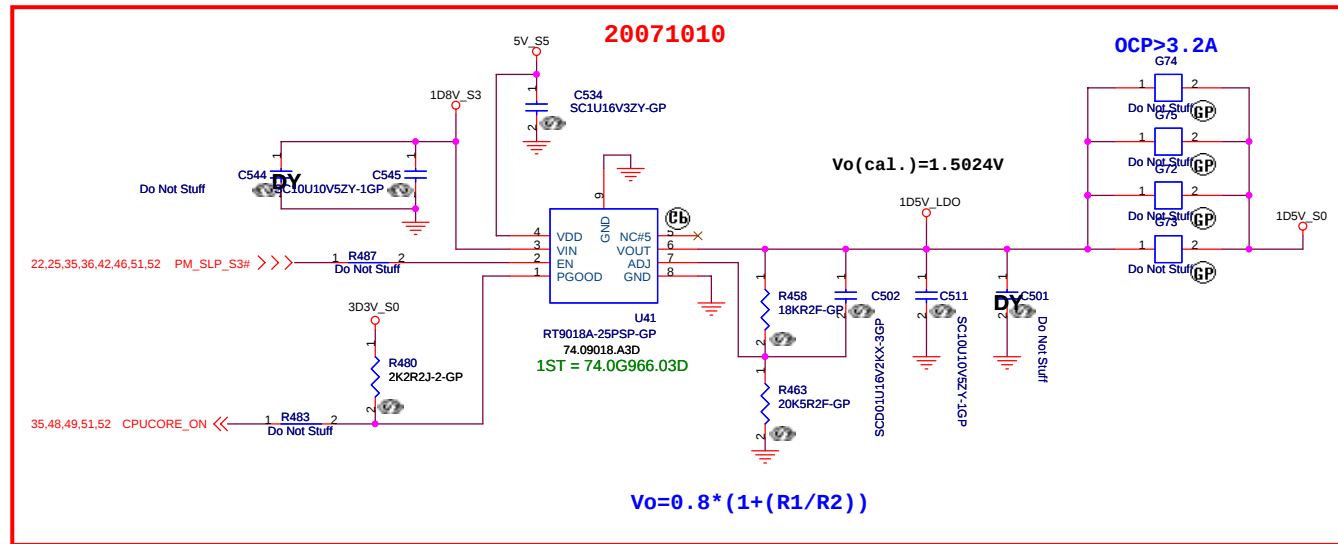
-1



Close to VFB Pin (pin2)

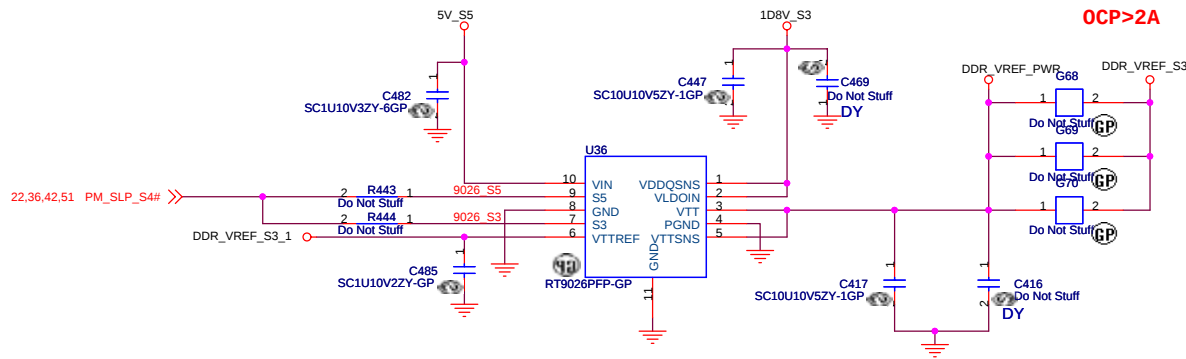
970

1D5V_S0 Iomax=2.5A

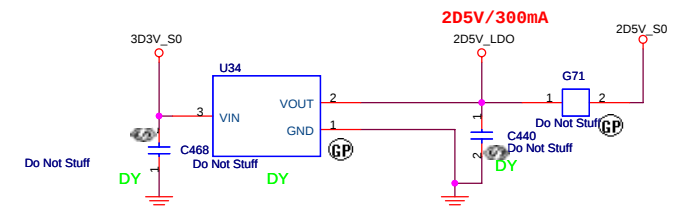


20071001

Iomax=1A
OCP>2A



2D5V_S0 Iomax=0.3A



970

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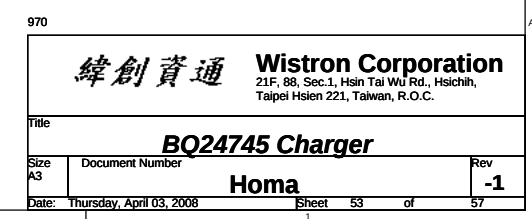
Title			1D5V & 0D9V & 2D5V
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$V_{trip}(mV) = R_{trip}(Kohm) * I_{ua}$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

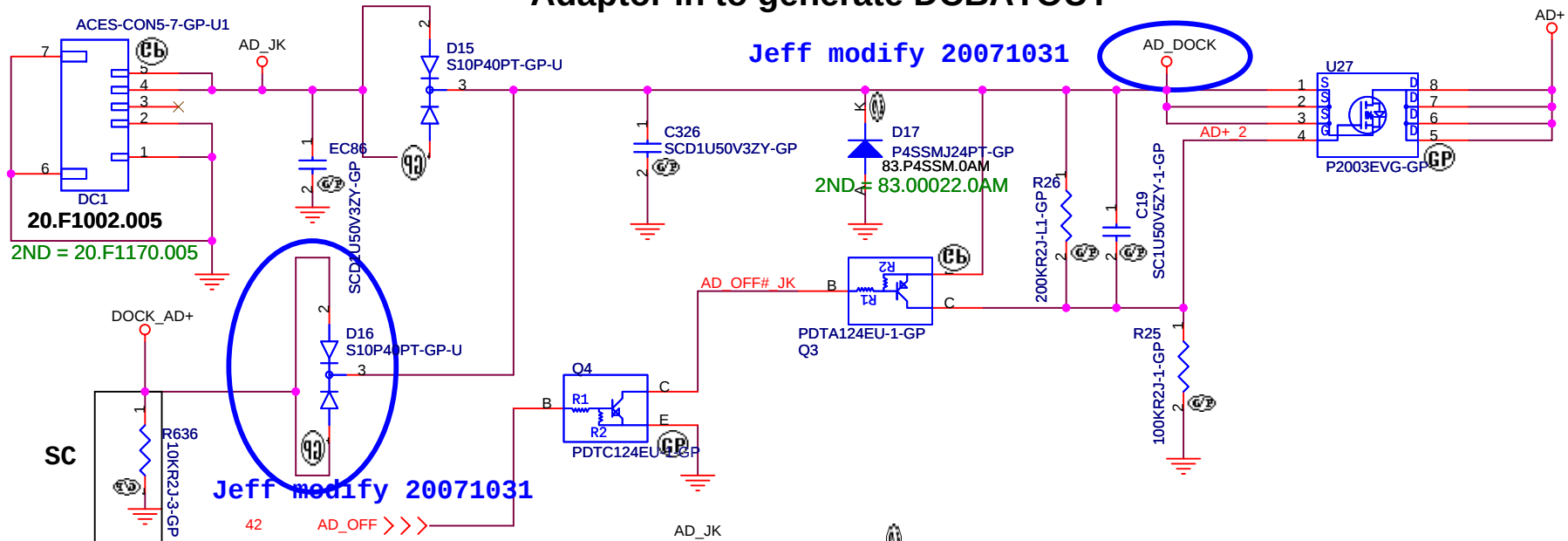
$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode

970

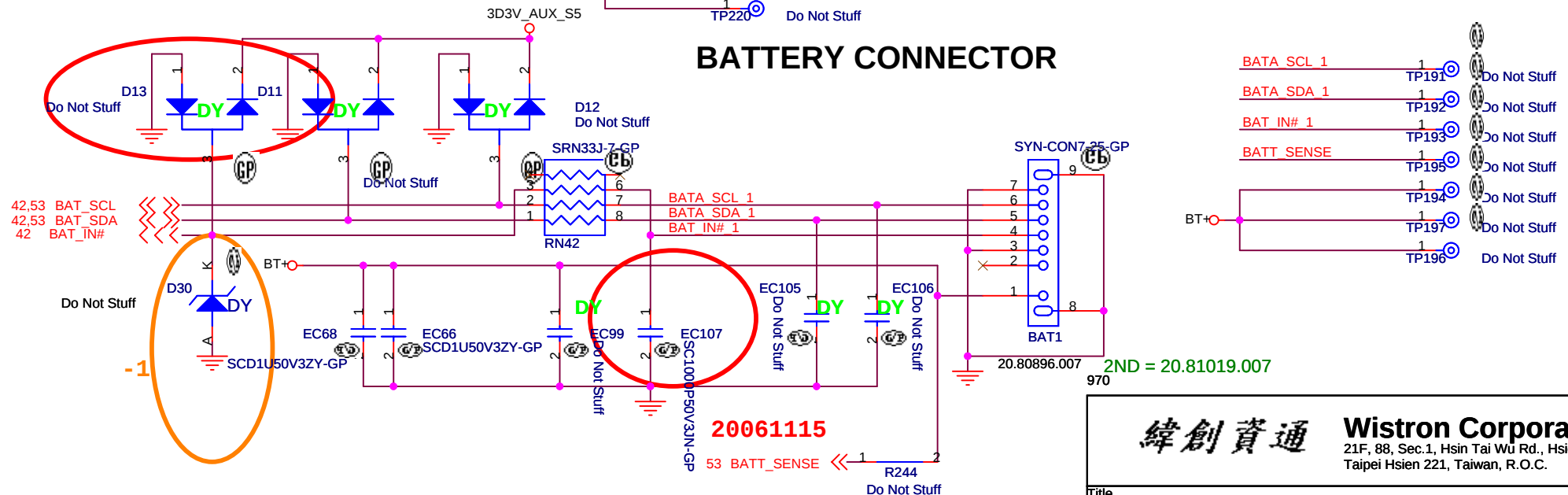


Adaptor in to generate DCBATOUT

Jeff modify 20071031



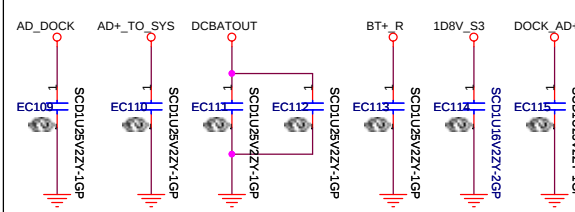
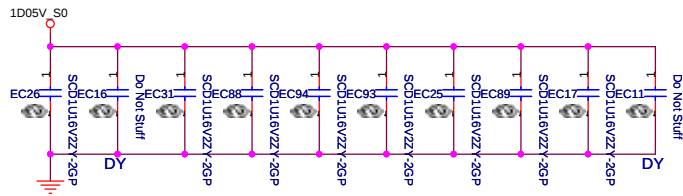
BATTERY CONNECTOR



緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title				
AD/BATT CONN				
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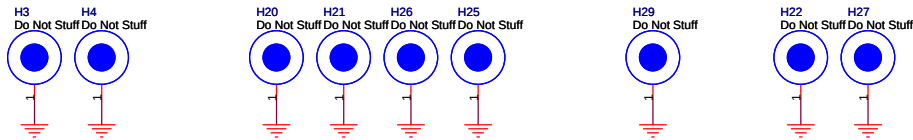
Check test point

- 3D3V_S0 <<< TP110 Do Not Stuff
- 3D3V_AUX_S5 <<< TP111 Do Not Stuff
- 3D3V_S5 <<< TP112 Do Not Stuff
- 5V_S5 <<< TP113 Do Not Stuff
- 22.42 PM_PWRBTN# <<< TP114 Do Not Stuff
- 4.21.46 H_PWRGD <<< TP115 Do Not Stuff
- 42.49 SS_ENABLE <<< TP116 Do Not Stuff
- 4.6 H_CPURST# <<< TP117 Do Not Stuff

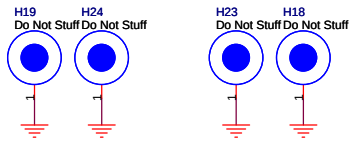
Test Point 放在 Dimm Door 打開可量測處

Stand off Location

34.42Y01.031



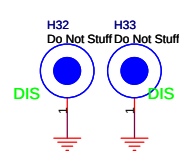
34.46502.021



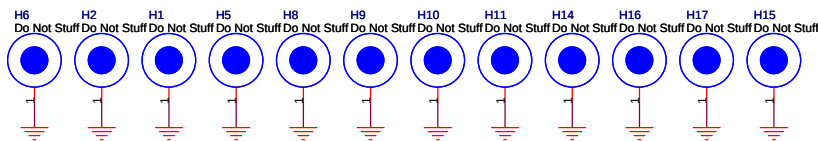
34.4Z402.011



34.4Z401.011



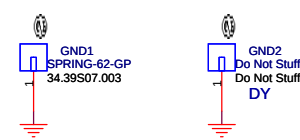
**DELETE MXM
STAND-OFF
H7;H28;H30;H31**



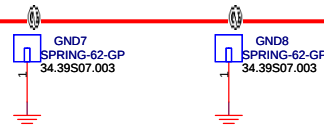
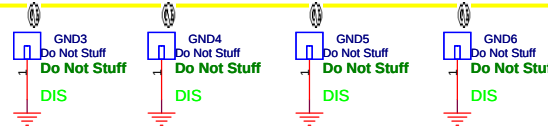
SC

SPRING ON BOTTOM

DIMM Heat Sink



MXM SPRING -1 20080307



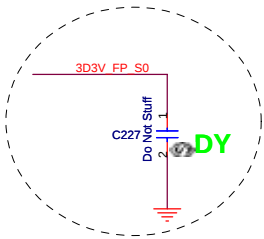
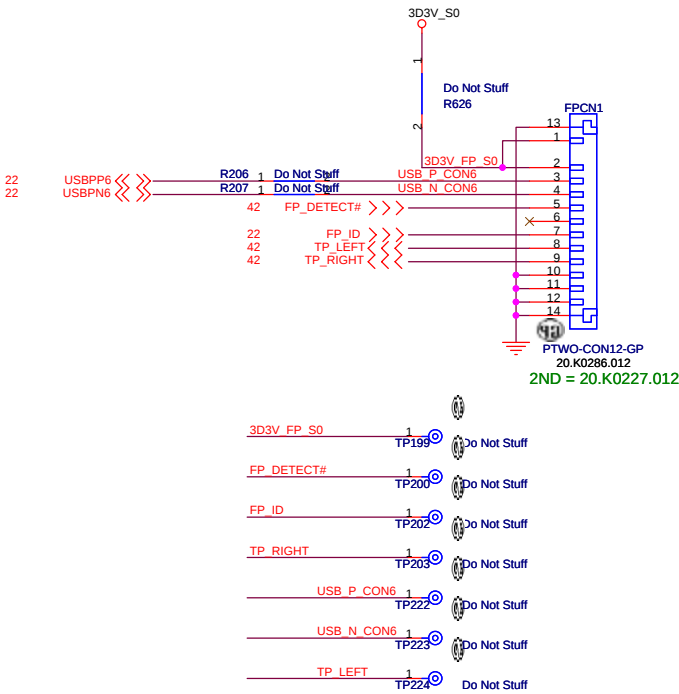
SC

970

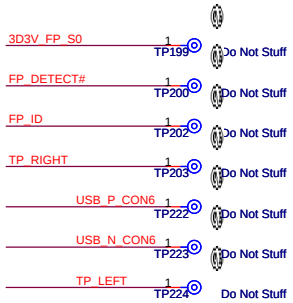
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Taipei Hsien 221, Taiwan, R.O.C.

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EMI/Spring/Boss		
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Finger printer



For EMI



SA --> SB

- 1.page25,Change Q24 and Q5 Pin_C and Pin_E net, Swap H_THERMDA and H_THERMDC(only close to C95)
- 2.page46,Change R145_Pin1 pull hige power to 1D05V_S0
- 3.page42,Add the Net let link U17_Pin101 and RN45_Pin3
- 4.page16,SWITCHCN1 pin12 connect to 3D3V_AUX_S5 and pin 11 connect to LID_CLOSE#
- 5.page20,HDMI1 change to 62.10078.171
- 6.page44,DOCK1 pin51 connect to CRT_DEC#
- 7.page53,R214 change to connect BQ24745_VREF as charger modify
- 8.page26,change ODD1 to 22.10300.141
- 9.page45,change U12 to PS8122QFN48G-GP and add some components
- 10.page44,Del U5
- 11.page20,Del U11,U42,Q9...
- 12.del G1-G8
- 13.page45,R614 changed to "DOCK_DT1#" and U12 output port1 and port2 swap,RN68 pin1&2 change to KBC SMBUS, RN69 pin3&4 change to connect"3D3V_S0",R615 change to 4K7R2F-GP
- 14.page49,change Q27&Q28 to 2N7002SPT ,add R595 R616
- 15.page48,change R12 to 10K2R3F-GP ,R13 to 16K5R2F-1-GP
- 16.page51,R578 change to 22K1R3-GP
- 17.page52,R257 change to 2K87R2F-1-GP ,C259 change to SCD033U50V
- 18.page40,change U8 to G1454R41U-GP
- 19.page42,Del R29 R27 C20 EC5
- 20.page41,LID1 change to INTMIC1 and connect to "MIC_L_CN"&"MIC_R_CN"
- 21.page39,add R619 C815 R621 R620 C816 C817
- 22.page38,Del C355 C320
- 23.page56,Del F4 addR626
- 24.page3,R204 change to connect"3D3V_CLKPLL_S0"
- 25.page52,add R622-R625
- 26.page44,add C818-C822 and L19 L20 L21
- 27.page35,Del TP77-TP82 TP84 TP86 TP87 TP24 TP25 TP26 TP28,add R618 pull up to 3D3V_S0
- 28.page25,add R617 Q35 del R115
- 29.page30,change C600 to 4.7U10V
- 30.page45, swap U12 output port1&pot2
- 31.page48-52, change power GAPS to close GAPS
- 32.page49,L15 change to 1ND-3D3UH by power modify
- 33.page16,add R627 EC108
- 34.page45,add C823 C824 and R144 R151 Q9 R137

970



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Change list