# Wistron Confidential

# SI2

2009/09/10 REV :SI2-01

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Title: NORN 3.0

| Size | Document Number | Rev |
|---|---|---|
| A3 | NORN 3.0 | SE |

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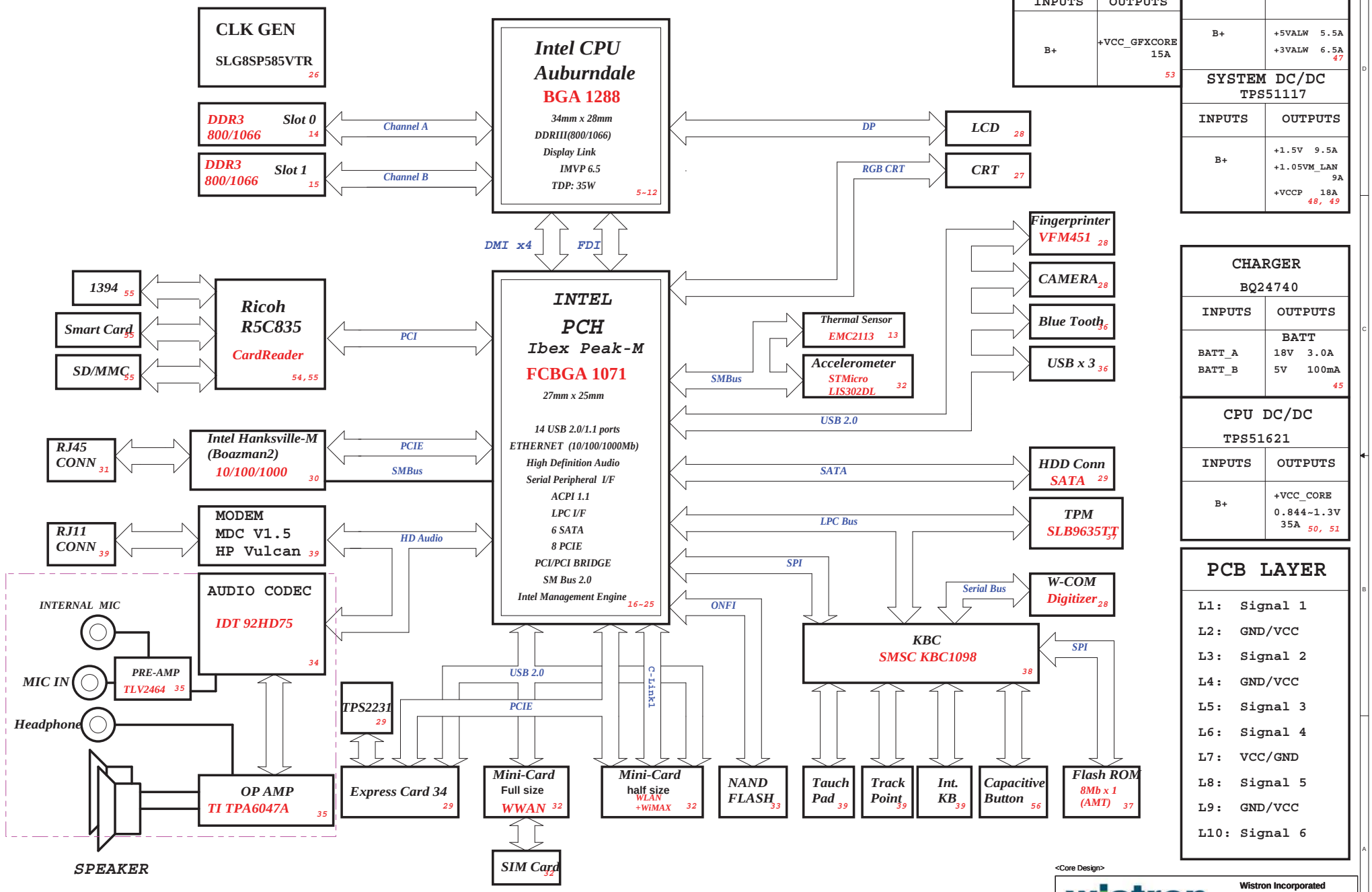
# Norn3.0 BLOCK DIAGRAM




**VGA**
TPS51611

| INPUTS | OUTPUTS |
|---|---|
| B+ | +VCC_GFXCORE 15A 53 |

**SYSTEM DC/DC**
TPS51125

| INPUTS | OUTPUTS |
|---|---|
| B+ | +5VALW 5.5A<br>+3VALW 6.5A 47 |

**SYSTEM DC/DC**
TPS51117

| INPUTS | OUTPUTS |
|---|---|
| B+ | +1.5V 9.5A<br>+1.05VM_LAN 9A<br>+VCCP 18A 48, 49 |

**CHARGER**
BQ24740

| INPUTS | OUTPUTS |
|---|---|
| | BATT |
| BATT_A | 18V 3.0A |
| BATT_B | 5V 100mA 45 |

**CPU DC/DC**
TPS51621

| INPUTS | OUTPUTS |
|---|---|
| B+ | +VCC_CORE 0.844~1.3V 35A 50, 51 |

**PCB LAYER**

| | |
|---|---|
| L1: | Signal 1 |
| L2: | GND/VCC |
| L3: | Signal 2 |
| L4: | GND/VCC |
| L5: | Signal 3 |
| L6: | Signal 4 |
| L7: | VCC/GND |
| L8: | Signal 5 |
| L9: | GND/VCC |
| L10: | Signal 6 |

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*Change Notes List*

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## Voltage Rails

o MEANS ON  x MEANS OFF

| State \ power plane | +3VL<br>VL | +3VALW<br>+5VALW | +1.5V<br>+0.75VS | +5VS<br>+3VS<br>+1.8VS<br>+1.5VS<br>+VCCP<br>+1.05VS<br>+VCC_CORE<br>+VCC_GFXCORE | +3VM<br>+1.05VM | CLOCK |
|---|---|---|---|---|---|---|
| S0 | O | O | O | O | O | O |
| S3/M1 | O | O | O | X | O | O |
| S3 | O | O | O | X | O | O |
| S5 S4/AC | O | O | X | X | X | O |
| S5 S4/Battery only | O | X | X | X | X | X |
| S5 S4/AC & Battery don't exist | X | X | X | X | X | X |

## PCI Devices

| EETERNAL | IDSEL# | REQ/GNT# | PIRQ |
|---|---|---|---|
| Cardreader & 1394 | AD22 | 2 | G,E |

| DMA Channel | Device |
|---|---|
| DMA0 | Modem/LAN |
| DMA1 | ECP |
| DMA2 | ~~Floppy Disk~~ |
| DMA3 | Audio |
| DMA4 | (Cascade) |
| DMA5 | Unused |
| DMA6 | Unused |
| DMA7 | Unused |

| USB PORT# | Destination |
|---|---|
| 0 | Walk-up1 (Right Side) |
| 1 | Walk-up2 (Right Side) |
| 2 | Walk-up3 (Left Side) |
| 3 | Free |
| 4 | EXPRESS SLOT |
| 5 | Free |
| 6 | WLAN |
| 7 | Free |
| 8 | Bluetooth |
| 9 | WWAN |
| 10 | Fingerprint |
| 11 | Dock1 (HUB) |
| 12 | Webcam |
| 13 | Dock2 (IDE) |

| Symbols | Description |
|---|---|
| DY/DUMMY | No install |
| 1KR2J | Resistor 1K ohm ,Size 0402 ,5% |
| 1KR3F | Resistor 1K ohm ,Size 0603 ,1% |
| GP | ROHS parts |
| NC | Pin no connect to anything |
| | |
| | |

| IRQ | Device |
|---|---|
| 0 | System Timer |
| 1 | Keyboard |
| 2 | N/A |
| 3 | Serial port (COM2) ,LAN/Modem |
| 4 | Serial port (COM1) |
| 5 | Audio/VGA |
| 6 | ~~Floppy~~ |
| 7 | Parallel port |
| 8 | System CMOS/Real-time clock |
| 9 | Microsoft ACPI |
| 10 | N/A,Modem,LAN |
| 11 | Mass storage control/PCI simple communication control |
| 12 | synactic PS2 port GlidePAD |
| 13 | Numeric Data Process |
| 14 | Primary IDE interface ,HDD |
| 15 | Secondary IDE interface ,CD-ROM |
| 16 | Mobile Intel Crestline Express Chipset Family<br>Microsoft UAA Bus Drive for High Definition Audio<br>Intel 82801H (ICH8 Family) PCI Express Root Port -27D0<br>Broadcom NetXtreme Gigabit Ethernet |
| 17 | Intel 82801H (ICH8 Family) PCI Express Root Port -27D2<br>Broadcom 802.11b/g WLAN<br>Intel 82801H (ICH8 Family) USB Universal Host Control |
| 18 | Intel 82801H (ICH8 Family) USB Universal Host Control<br><br>Richo R5C853 Integrates FlashMedia Control<br>Richo R5C853 Gemcore based SmartCard Control |
| 19 | Intel 82801H (ICH8 Family) PCI Express Root Port -27D6<br>Intel 82801H (ICH8 Family) USB Universal Host Control |
| 20 | Intel 82801H (ICH8 Family) USB Universal Host Control<br>Intel 82801H (ICH8 Family) USB2 Enhanced Host Control |
| 21 | Intel 82801H (ICH8 Family) USB Universal Host Control |
| 22 | SDA Standard Compliant SD Host Control |
| 23 | HP Mobile Data Protection Sensor |

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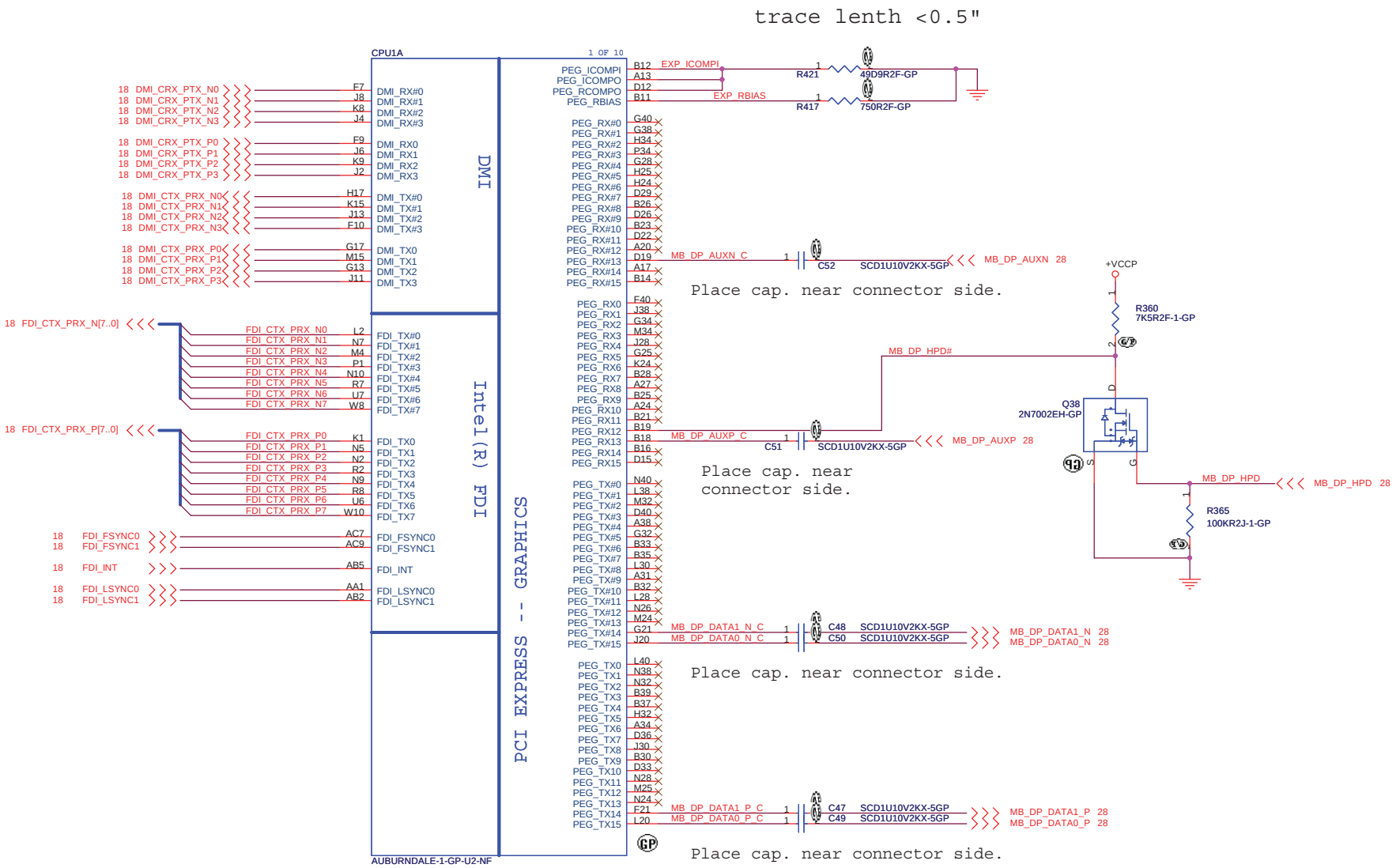


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Title: Auburndale(1/8)-DMI+PEG+FDI

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## Processor Pullups

+VCCP
R121 49D9R2F-GP H_CATERR#
R494 68R2-GP H_PROCHOT#_D
R492 DY 68R2-GP H_CPURST#_R

## Processor Compensation Signals

R148 20R2F-GP COMP3 AD71
R147 20R2F-GP COMP2 AC70
R153 49D9R2F-GP COMP1 AD69
R154 49D9R2F-GP COMP0 AE66

## closed to CPU

### DDR3 Compensation Signals

SM_RCOMP0 R442 100R2F-L1-GP-U
SM_RCOMP1 R443 24D9R2F-L-GP
SM_RCOMP2 R444 130R2F-1-GP

## CPU1B

### Misc

COMP3 COMP2 COMP1 COMP0
TP29 TP_SKTOCC# M71
PROC_DETECT

### Thermal

H_CATERR# N61 CATERR#
21 H_PECI R353 0R2J-2-GP H_PECI_ISO N19 PECI
50 H_PROCHOT# R496 0R2J-2-GP H_PROCHOT#_D N67 PROCHOT#
13,21 H_THRMTRIP# R358 0R2J-2-GP H_THRMTRIP#_R N17 THERMTRIP#

### Power Management

H_CPURST# R485 0R2J-2-GP H_CPURST#_R N70 RESET_OBS#
18 H_PM_SYNC R359 0R2J-2-GP H_PM_SYNC_R M17 PM_SYNC
TP103 SYS_AGENT_PWROK AM7 VCCPWRGOOD_1
TP134 R354 0R2J-2-GP
21 H_CPUPWRGD R355 0R2J-2-GP TP104 VCCPWRGOOD_0 Y67 VCCPWRGOOD_0
18 PM_DRAM_PWRGD R350 0R2J-2-GP VDDPWRGOOD_R AM5 SM_DRAMPWROK
TP105 VTTPWRGOOD H15 VTTPWRGOOD
0708 SI1-R 0712 SI1-R
42 VTTPWRGOOD
VCCP_1.5VSPWRGD 42 R352 1K5R2F-2-GP
H_PWRGD_XDP R146 0R2J-2-GP H_PWRGD_XDP_R Y70 TAPPWRGOOD
20 BUF_PLT_RST# R372 1K5R2F-2-GP PLT_RST#_R G3 RSTIN#
TP106 R373 750R2F-GP
VDDPWRGOOD_R R351 750R2F-GP

AUBURNDALE-1-GP-U2-NF

### Clocks

BCLK AK7 AK8 BCLK# CLK_CPU_BCLK 21 CLK_CPU_BCLK# 21
BCLK_ITP K71 CLK_CPU_XDP BCLK_ITP# J70 CLK_CPU_XDP#
PEG_CLK L21 CLK_EXP 17 PEG_CLK# J21 CLK_EXP# 17
DPLL_REF_SSCLK Y2 CLK_DP 17 DPLL_REF_SSCLK# W4 CLK_DP# 17

### DDR3 Misc

TP102 SM_DRAMRST#
SM_DRAMRST# BJ12
SM_RCOMP0 BV33 SM_RCOMP0
SM_RCOMP1 BP39 SM_RCOMP1
SM_RCOMP2 BV40 SM_RCOMP2
PM_EXT_TS#0 AV66 PM_EXTTS#0
PM_EXT_TS#1 AV64 PM_EXTTS#1
RN5 SRN10KJ-5-GP +VCCP
R127 0R2J-2-GP TP8 PM_EXTTS#1_R 14,15

0708 SI1-R 0712 SI1-R 0718 SI1-R 0821 SI2
R1255 100KR2J-1-GP
+1.5V R1253 1KR2J-1-GP
Q86 BSS138-7-F-GP
DRAMRST# 14,15
0712 SI1-R PCH_DDR_RST 21
+3VALW R1254 10KR2J-3-GP 0713 SI1-R

### JTAG & MBP

PRDY# U71 XDP_PRDY# PREQ# U69 XDP_PREQ#
TCK T67 XDP_TCK
TMS N65 XDP_TMS
TRST# P69 XDP_TRST#
TDI T69 XDP_TDI
TDO T71 XDP_TDO
TDI_M P71 XDP_TDI_TDO_M
TDO_M T70
DBR# W71 XDP_DBRESET#
BPM#0 J69 XDP_BPM#0
BPM#1 J67 XDP_BPM#1
BPM#2 J62 XDP_BPM#2
BPM#3 K65 XDP_BPM#3
BPM#4 K62 XDP_BPM#4_R R120 0R2J-2-GP XDP_BPM#4
BPM#5 J64 XDP_BPM#5_R R122 0R2J-2-GP XDP_BPM#5
BPM#6 K69 XDP_BPM#6_R R129 0R2J-2-GP XDP_BPM#6
BPM#7 M69 XDP_BPM#7_R R130 0R2J-2-GP XDP_BPM#7

Place resistors close to pin of CPU.

**Layout Notes:**

Make sure that the stubs to the test points(SYS_AGENT_PWROK, PLT_RST#_R, CLK_CPU_BCLK, CLK_CPU_BCLK#, DRAMRST#, VTTPWRGOOD, VCCPWRGOOD_0, H_CPUPWRGD) in the layout are as short as possible on the high speed signals.

+VCCP R89 DY 1KR2J-1-GP PM_PWRBTN#_R

0622 SI1 XDP1 DY

XDP_BPM#0 XR4 XDP_BPM#1 XR5 XDP_BPM#2 XR6 XDP_BPM#3 XR8 XR9 XR10 XR11 0R2J-2-GP
CFG12 CFG13 CFG14 CFG15 11
XDP_PREQ# XDP_PRDY# XDP_9 XDP_11 XDP_15 XDP_17
CFG17 CFG16 11
XDP_BPM#4 XDP_BPM#5 XDP_BPM#6 XDP_BPM#7
H_CPUPWRGD XR13 1KR2J-1-GP H_CPUPWRGD_R
18,25 PM_PWRBTN#_R
H_PWRGD_XDP XR12 0R2J-2-GP H_PWRGD_XDP_L
+VCCP XC1 SCD1U16V2ZY-2GP
TP5 TP6 XDP_TP_51 XDP_TP_53 XDP_TCK

CFG8 CFG9 CFG0 CFG1 CFG2 CFG3 CFG10 CFG11 CFG4 CFG5 CFG6 CFG7 11
CLK_CPU_XDP CLK_CPU_XDP#
XDP_RST#_R XR1 XDP_DBRESET#_R XR3 1KR2J-1-GP H_CPURST# 0R2J-2-GP
XDP_TRST# XDP_TDI XDP_TMS
XDP_RST#_R XR2 0R2J-2-GP PLT_RST# 20,25,29,30,32,35,37

STC-CONN60A-GP
20.F0971.060

closed to XDP

XDP_TRST# R63 51R2J-2-GP

+VCCP R62 51R2J-2-GP
+3VS R51 1KR2J-1-GP
XDP_TDO
XDP_DBRESET# 18,25

Place those AFTP at bottom side.

XDP_TDO AFTP72
XDP_TRST# AFTP73
XDP_TDI AFTP74
XDP_TMS AFTP75
XDP_TCK AFTP76

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Title: Auburndale(2/8)-CLK+MISC+JTAG
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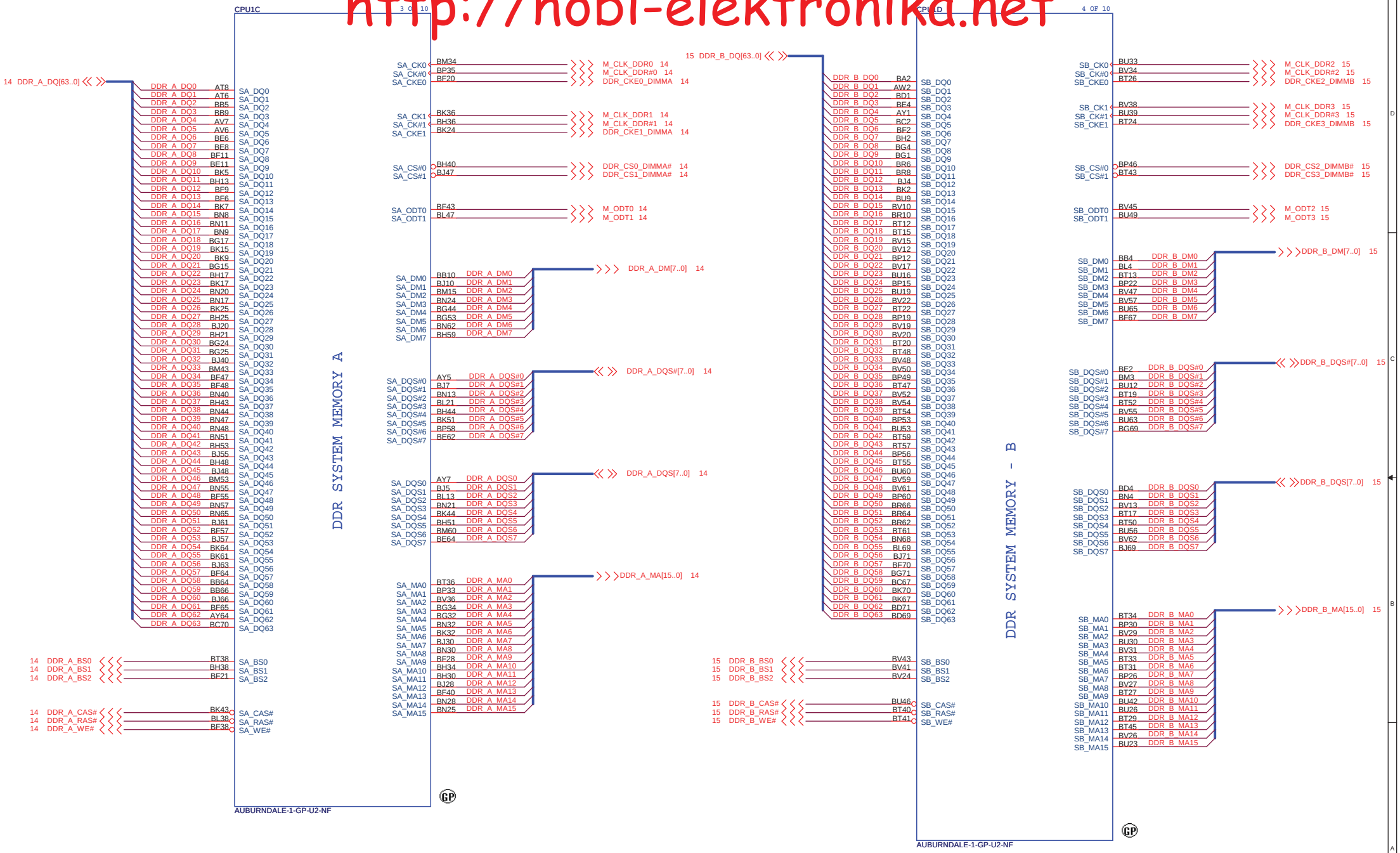


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| | |
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| Title | Auburndale(3/8)-DDR3 |
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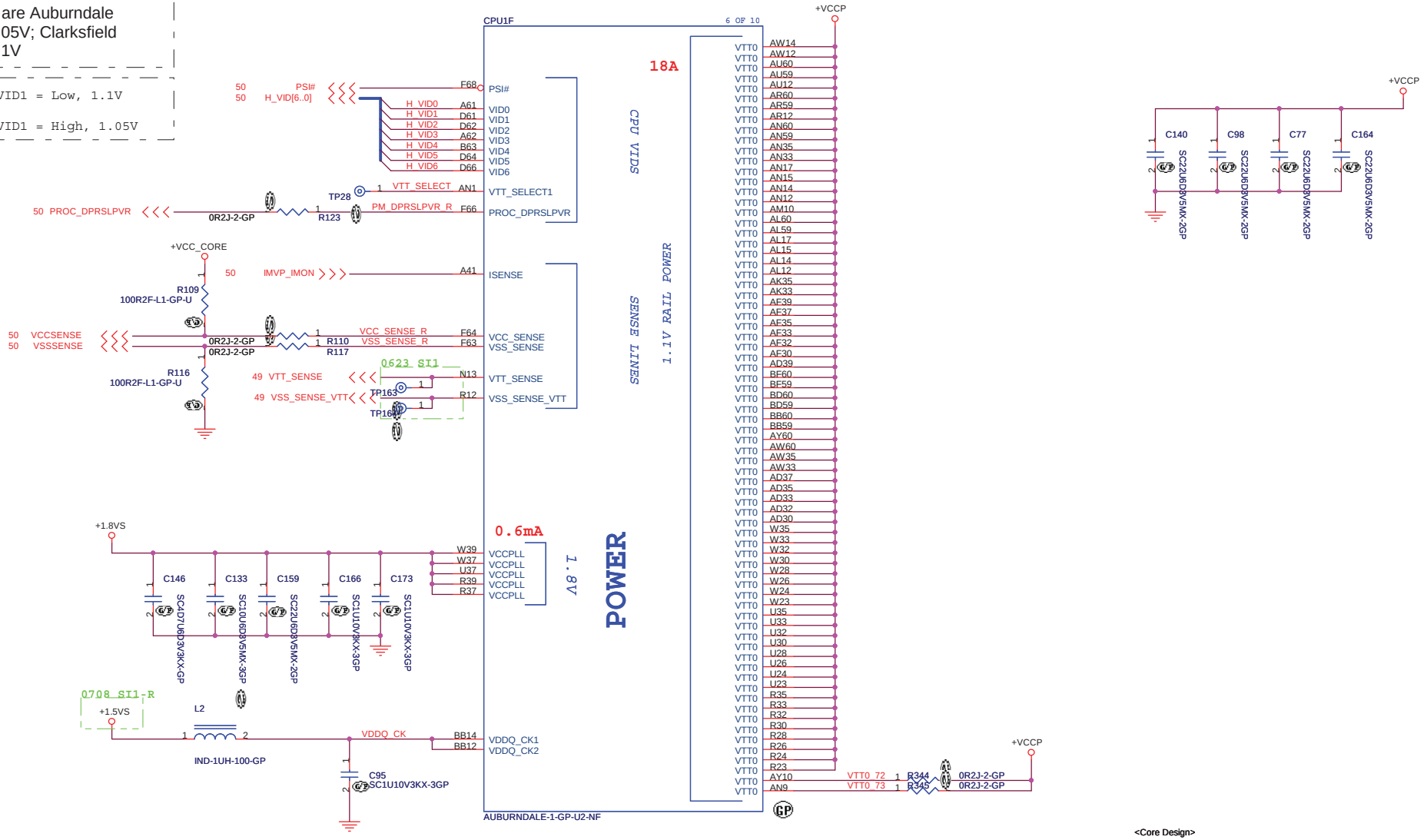
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

H_VTTVID1 = Low, 1.1V

H_VTTVID1 = High, 1.05V

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Title: Auburndale(4/8)-POWER

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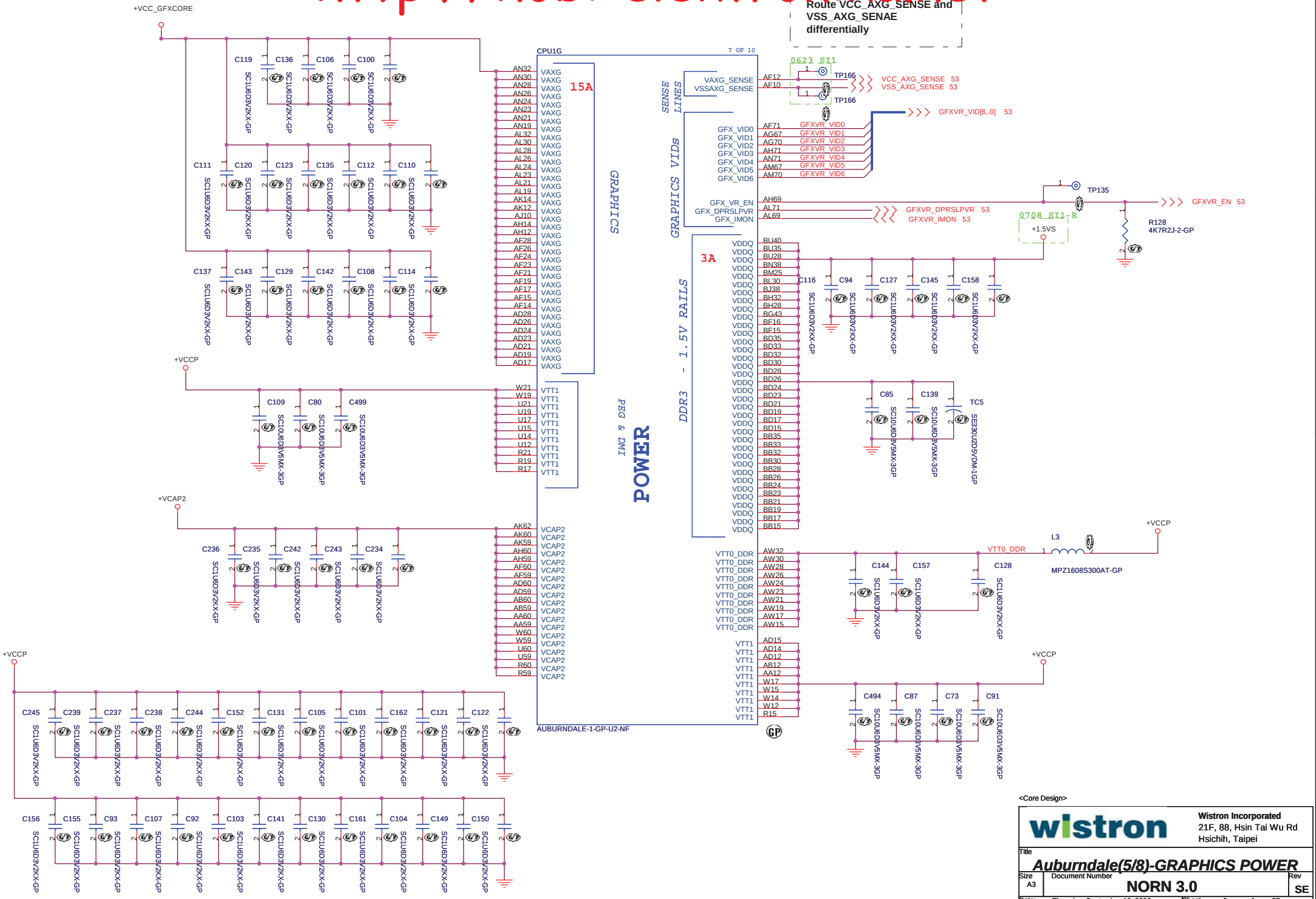



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Title: Auburndale(5/8)-GRAPHICS POWER

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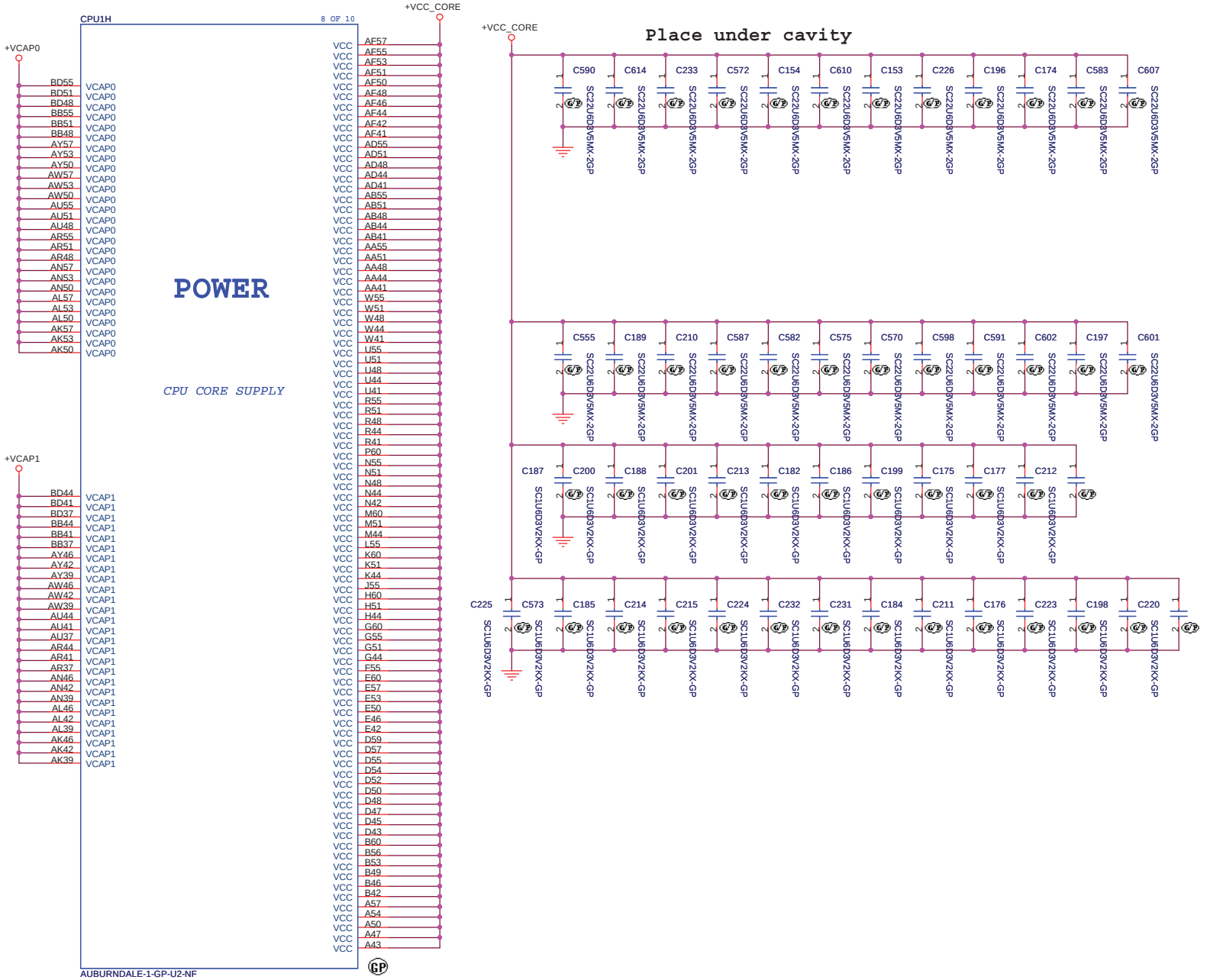



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Title: *Auburndale(6/8)-GND*

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## CFG Straps for Processor

CFG0 — R346 3K01R2F-3-GP (DY)

| PCI-Express Configuration Select | |
|---|---|
| CFG0 | 1:Single PEG<br>0:Bifurcation enabled |

CFG3 — R347 3K01R2F-3-GP (DY)

| CFG3 - PCI-Express Static Lane Reversal | |
|---|---|
| CFG3 | 1 :Normal Operation<br>0 :Lane Numbers Reversed<br>15 -> 0, 14 -> 1, ... |

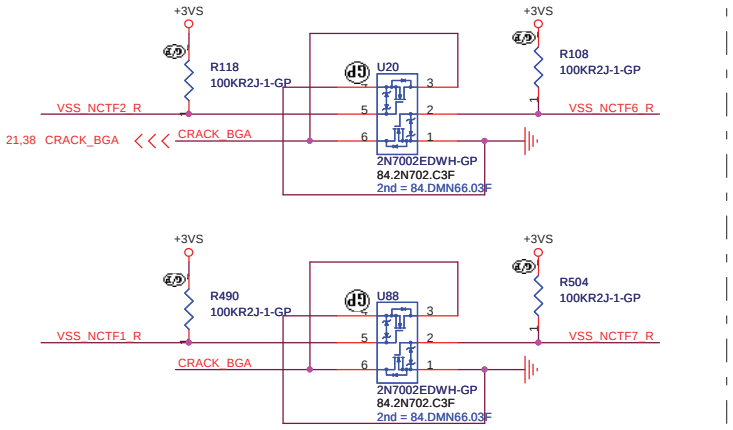
CFG4 — R348 3K3R2J-3-GP (0623 SI1)

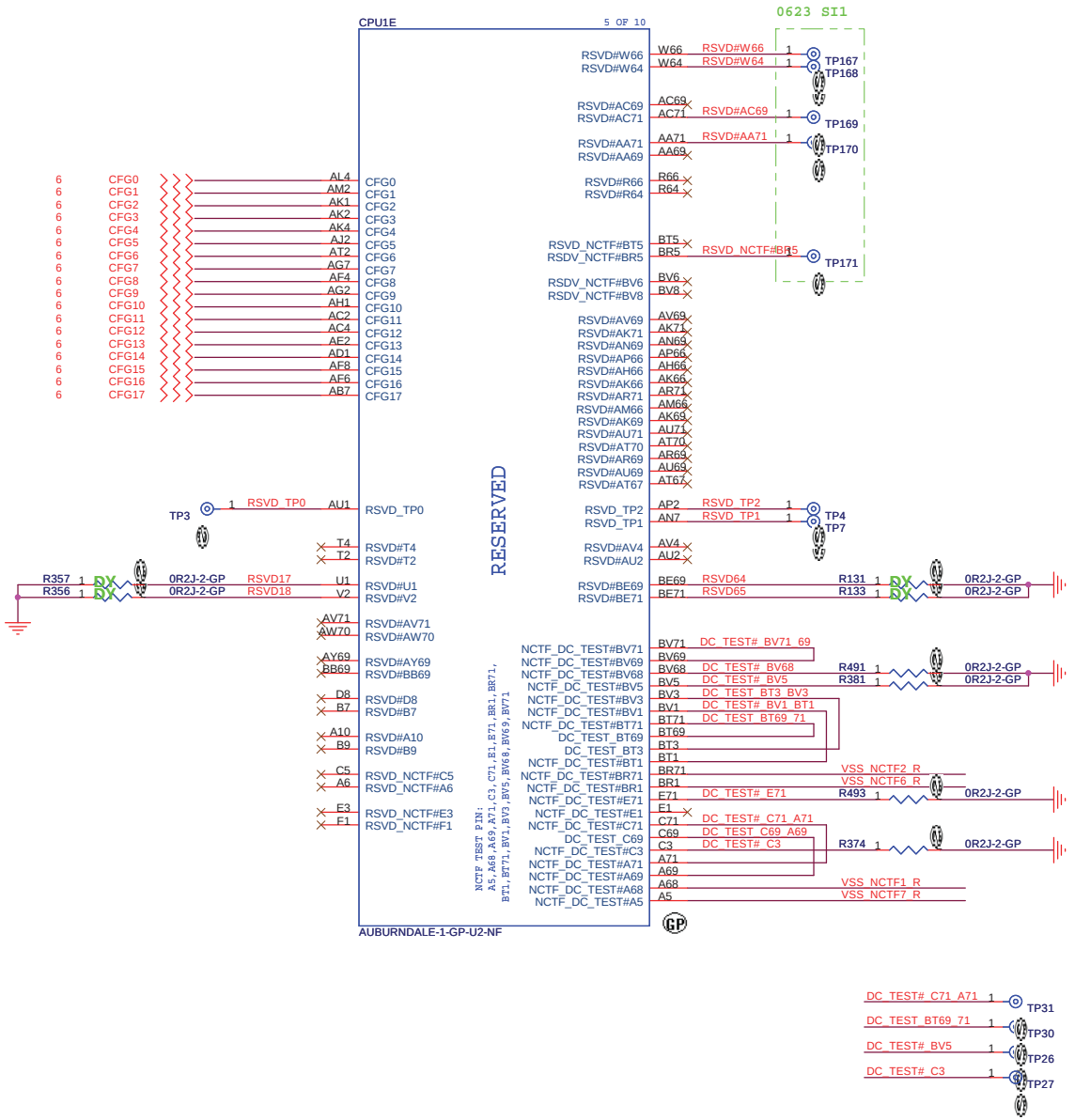
| CFG4 - Display Port Presence | |
|---|---|
| CFG4 | 1:Disabled; No Physical Display Port attached to Embedded Display Port<br>0:Enabled; An external Display Port device is connected to the Embedded Display Port |

Only temporary for early CFD samples (rPGA/BGA)

CFG7 — R349 3K01R2F-3-GP (DY)

## BGA Ball Cracking Prevention and Detection

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Title: Auburndale(7/8)-RESERVED

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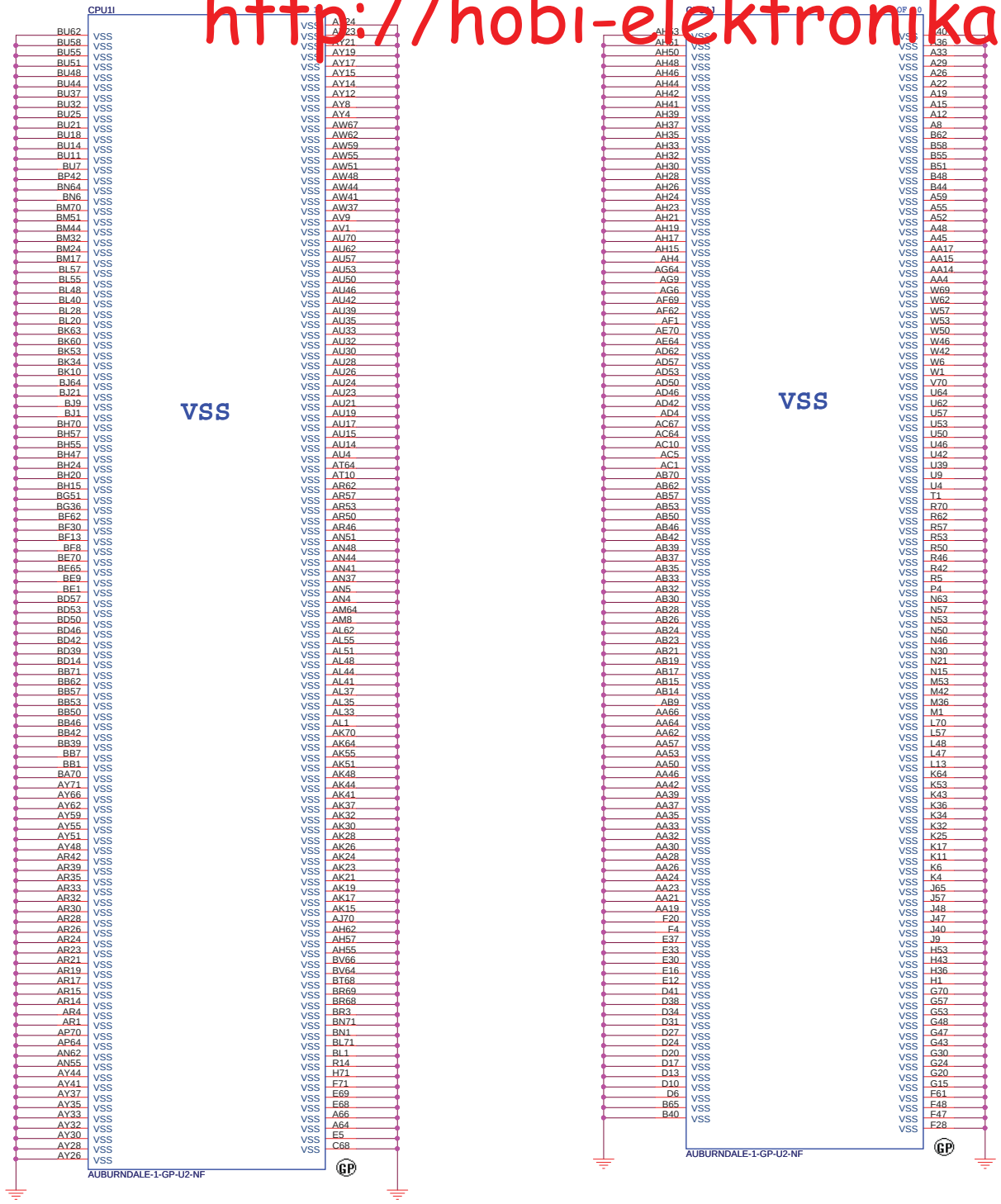


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Title: *Auburndale(8/8)-VSS*

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CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

H_THERMDA
C290
SC2200P50V2KX-2GP
H_THERMDC

REMOTE2-
Q10
MMBT3904WT1G-1-GP
84.M3904.D11
2nd = 84.03904.Y11
C202
SC2200P50V2KX-2GP
REMOTE2+

AMBIENT TEMP: Q24 used for GPU

REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing. Lacate Cap near thermal diode .

# 4 WIRE PWM Fan Control circuit

+5VS
D10
1SS355GP-GP
83.00355.F1F
2nd = 83.00355.F1F
C291
SCD1U16V2ZY2GP
R516
10KR2J-3-GP

FAN1
MLX-CON4-28-GP
20.F1035.004

+3VS
R166
10KR2J-3-GP
6,21 H_THRMTRIP#
R173
0R2J-2-GP
SYS_SHDN#

+3VS
R159
68R2-GP
C289
SCD1U10V2KX-4GP
+3VS_THER
R1219
10KR2J-3-GP

0630 SI1
FAN_PWM-R
FAN_PWM-R 38
C292
SCD1U16V2KX-3GP

FAN_PWM
FAN_TACH
R515
0R2J-2-GP
FAN_PWM_C

RN12
+3VS
SRN10KJ-5-GP

U32
EMC2113-1-AP-TR-GP
VDD
DP1
DN1
DP2/DN3
ND2/DP3
SYS_SHDN#
ALERT#
SMCLK
SMDATA
PWM_IN
ADDR_SEL
TACH
PWM
TRIP_SET
SHDN_SEL
GND
GND

H_THERMDA
H_THERMDC
REMOTE2+
REMOTE2-
21 THERM_SCI#
R165
0R2J-2-GP
SYS_SHDN#
THERM_SCI#_R
14,15,17,26,32 SMB_CLK_S3
14,15,17,26,32 SMB_DATA_S3
FAN_PWM-R
ADDR_SEL
FAN_TACH
FAN_PWM
TRIP_SET R164
2K05R2F-GP
SHDN_SEL

+3VS
R170
15KR2J-1-GP
SHDN_SEL

+5VS
AFTP43
FAN_PWM_C
AFTP39
FAN_TACH
AFTP40
AFTP41

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Title: SMSC2113 Thermal Sensor
Size: A3
Document Number: NORN 3.0
Rev: SE
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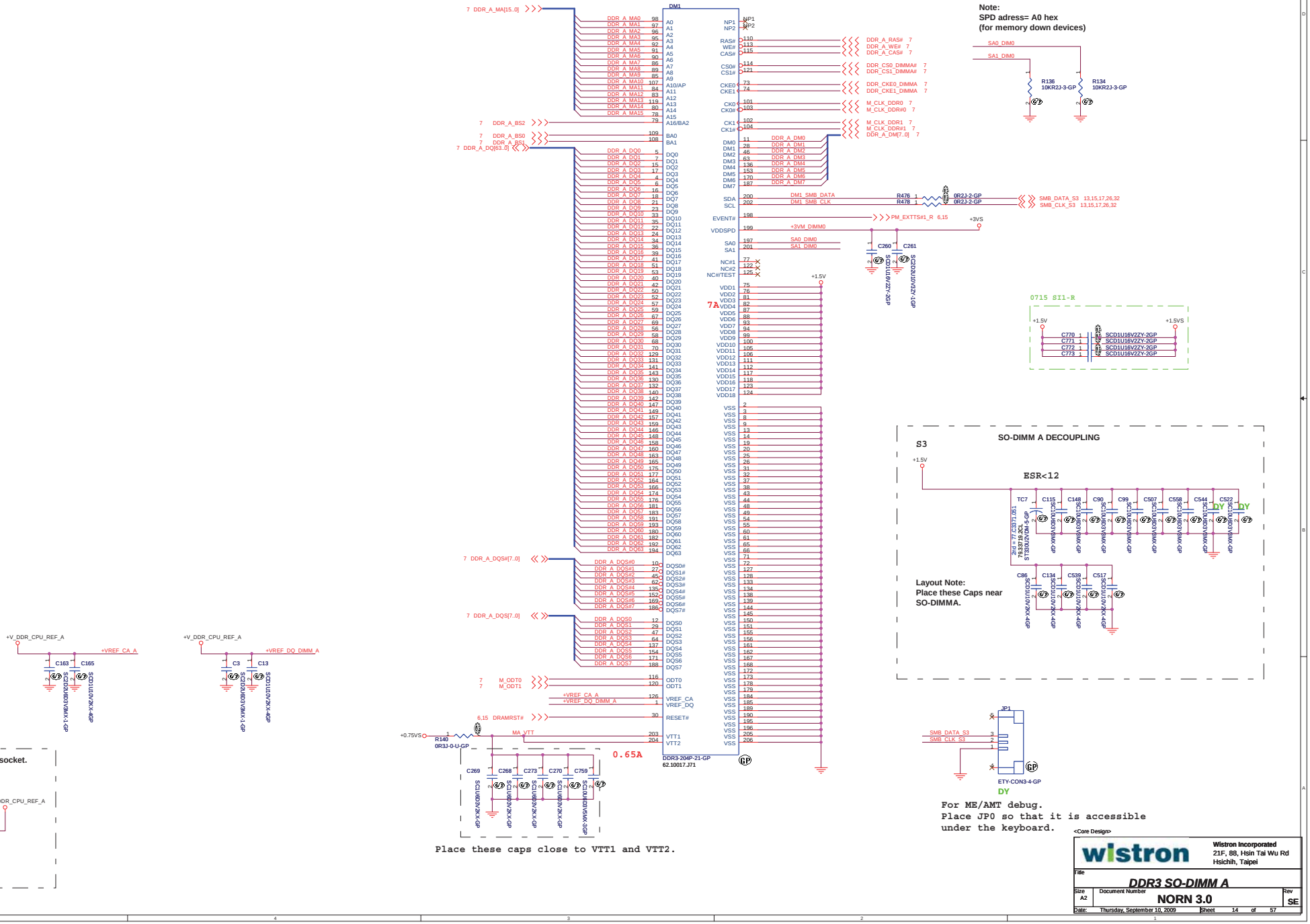

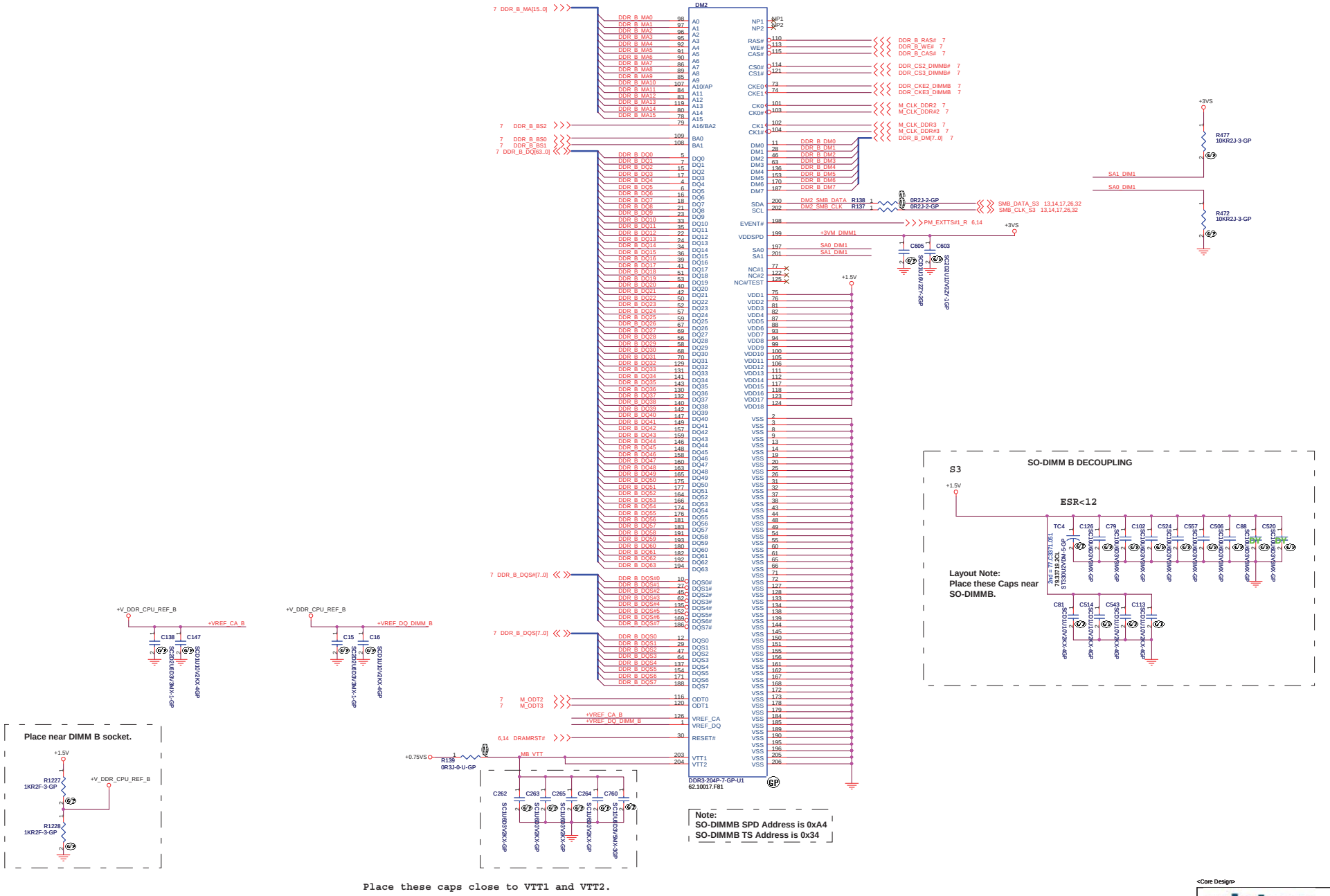


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Title: DDR3 SO-DIMM B

Size: A2 | Document Number: NORN 3.0 | Rev: SE

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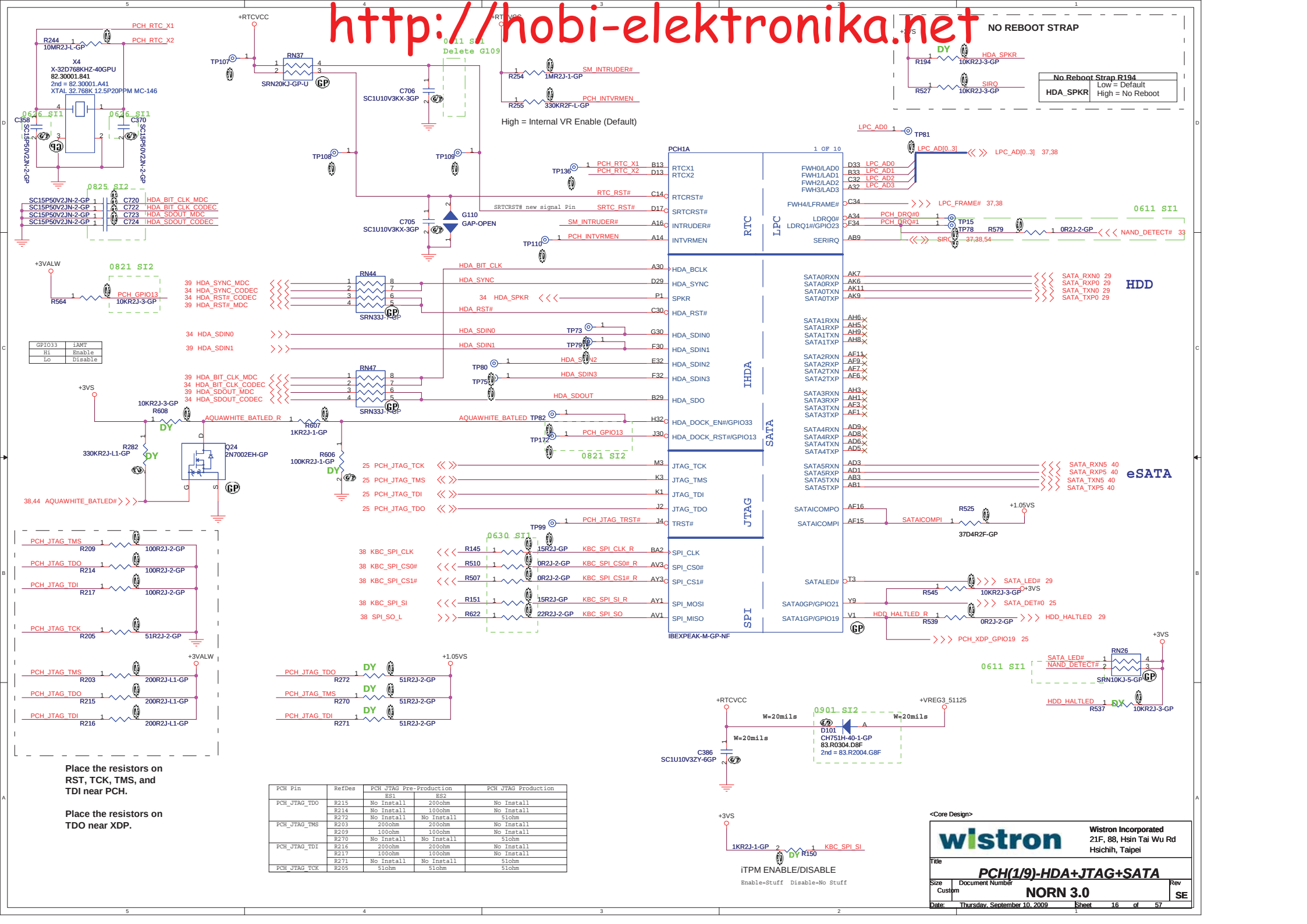


| PCH Pin | RefDes | PCH JTAG Pre-Production | | PCH JTAG Production |
|---|---|---|---|---|
| | | ES1 | ES2 | |
| PCH_JTAG_TDO | R215 | No Install | 200ohm | No Install |
| | R214 | No Install | 100ohm | No Install |
| | R272 | No Install | No Install | 51ohm |
| PCH_JTAG_TMS | R203 | 200ohm | 200ohm | No Install |
| | R209 | 100ohm | 100ohm | No Install |
| | R270 | No Install | No Install | 51ohm |
| PCH_JTAG_TDI | R216 | 200ohm | 200ohm | No Install |
| | R217 | 100ohm | 100ohm | No Install |
| | R271 | No Install | No Install | 51ohm |
| PCH_JTAG_TCK | R205 | 51ohm | 51ohm | 51ohm |

| GPIO33 | iAMT |
|---|---|
| Hi | Enable |
| Lo | Disable |

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Title: PCH(1/9)-HDA+JTAG+SATA

Size: Custom | Document Number: NORN 3.0 | Rev: SE

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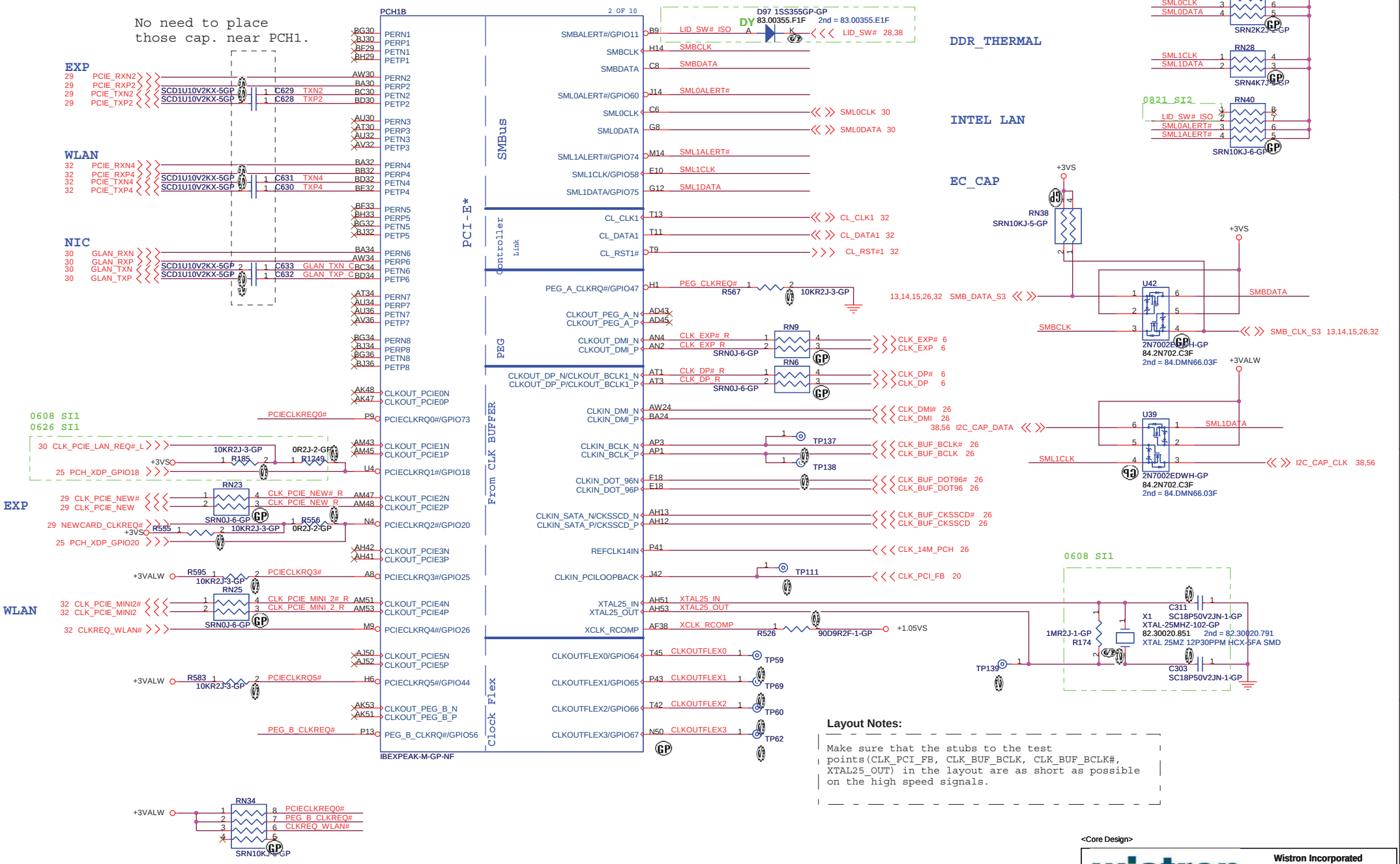

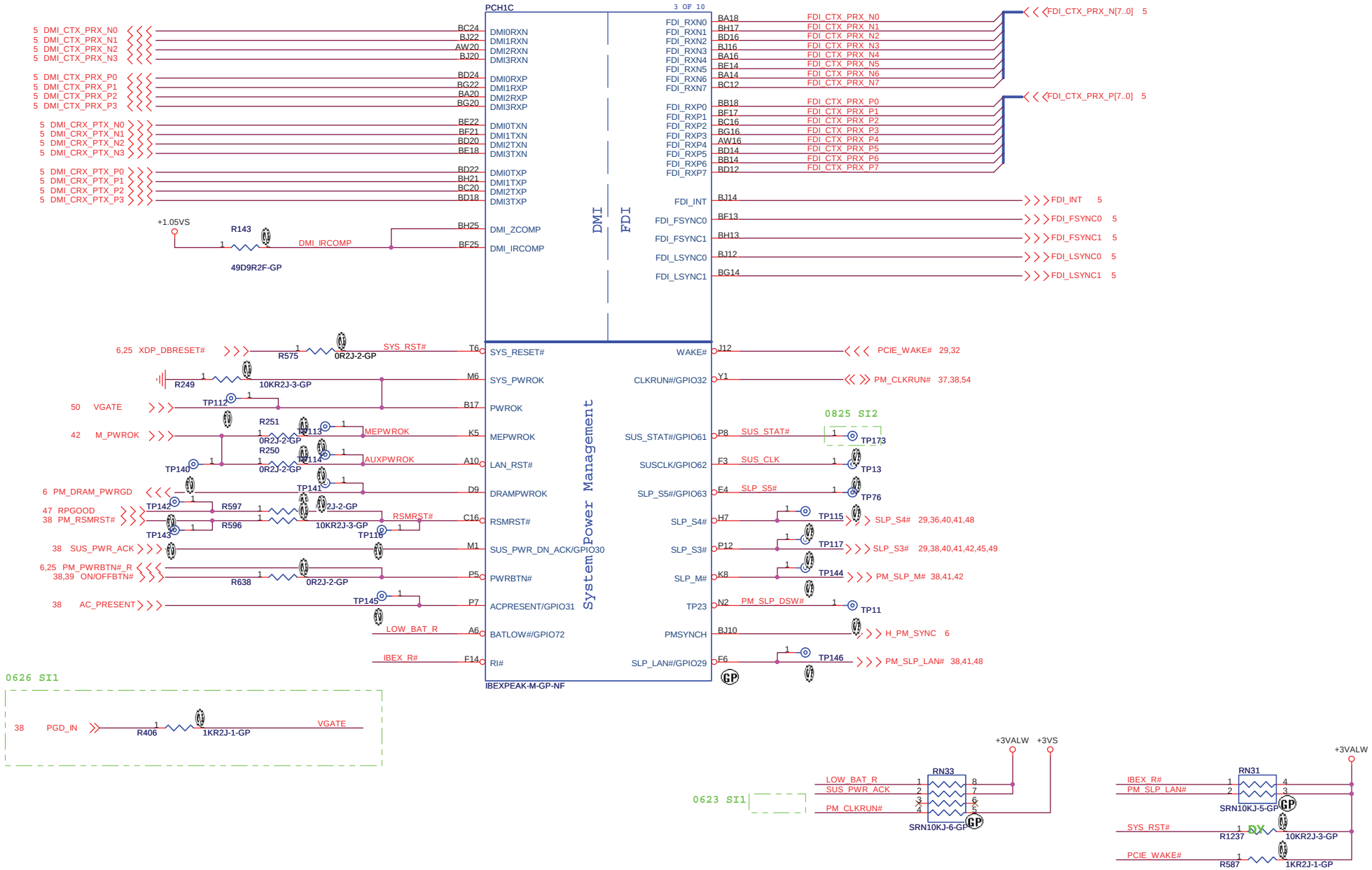



<Core Design>

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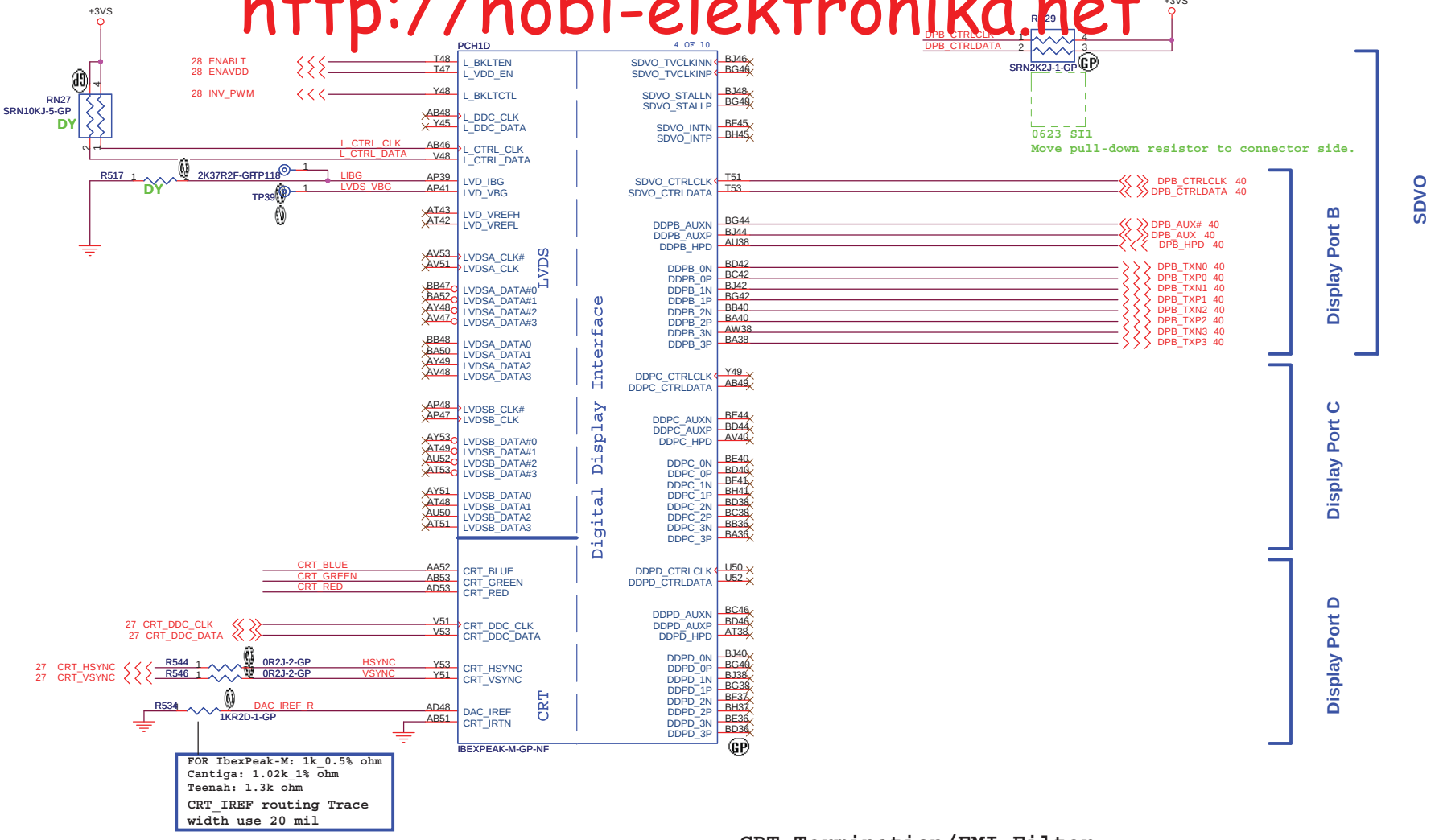
Title: PCH(3/9)-DMI+FDI+GPIO

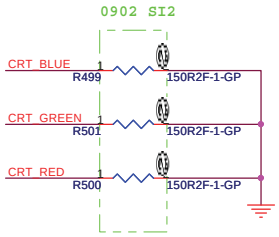
Size: A3 | Document Number: NORN 3.0 | Rev: SE

Date: Thursday, September 10, 2009 | Sheet 18 of 57

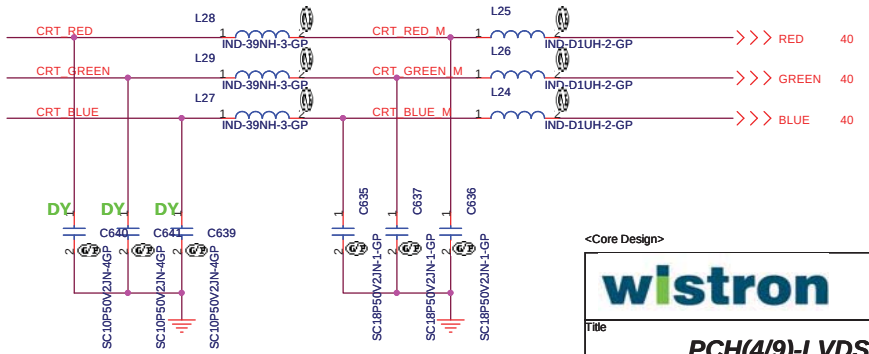



FOR IbexPeak-M: 1k_0.5% ohm
Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil

## Place Close IbexPeak-M




## CRT Termination/EMI Filter
## T-Filter network should be placed near IbexPeak-M.

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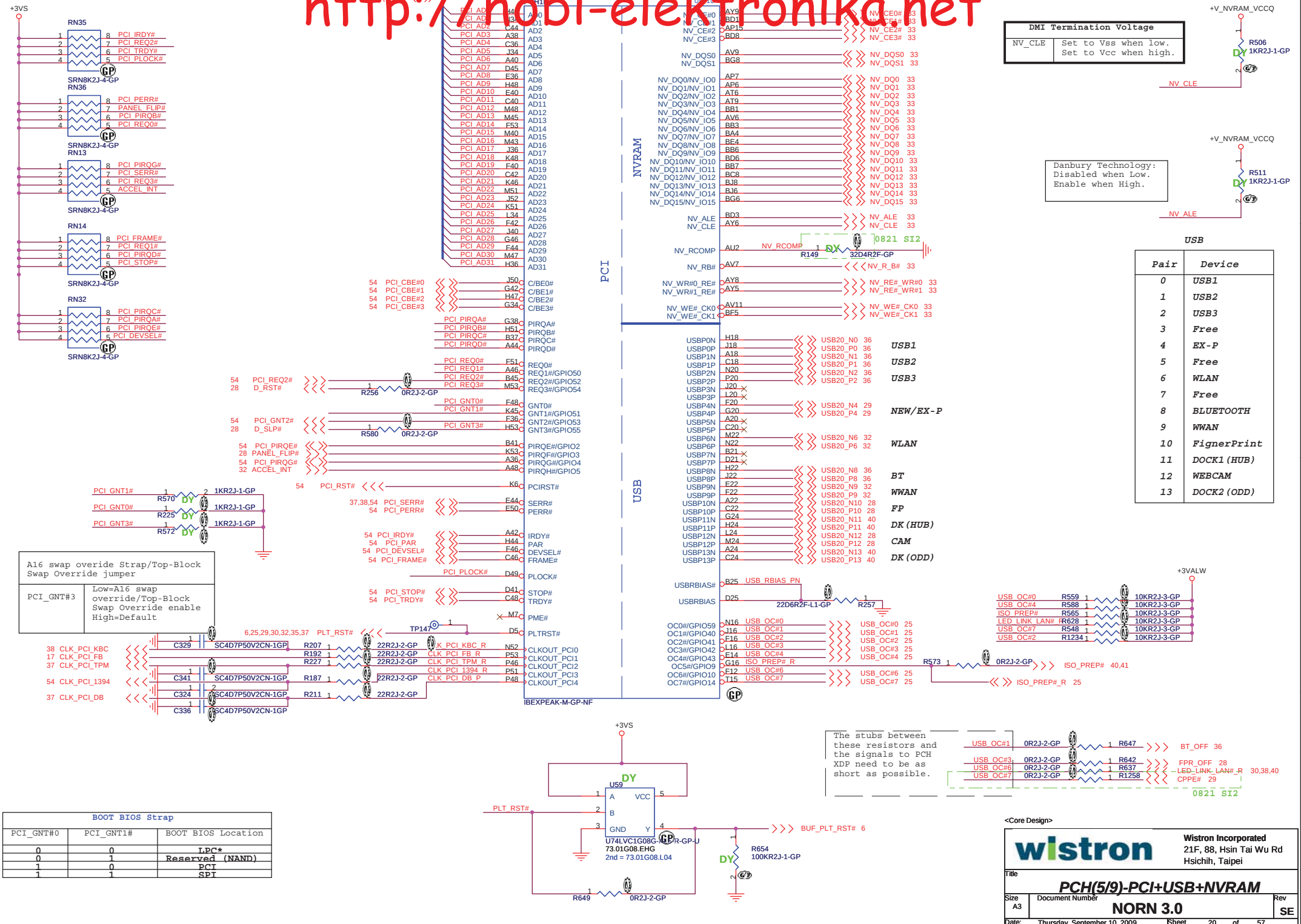
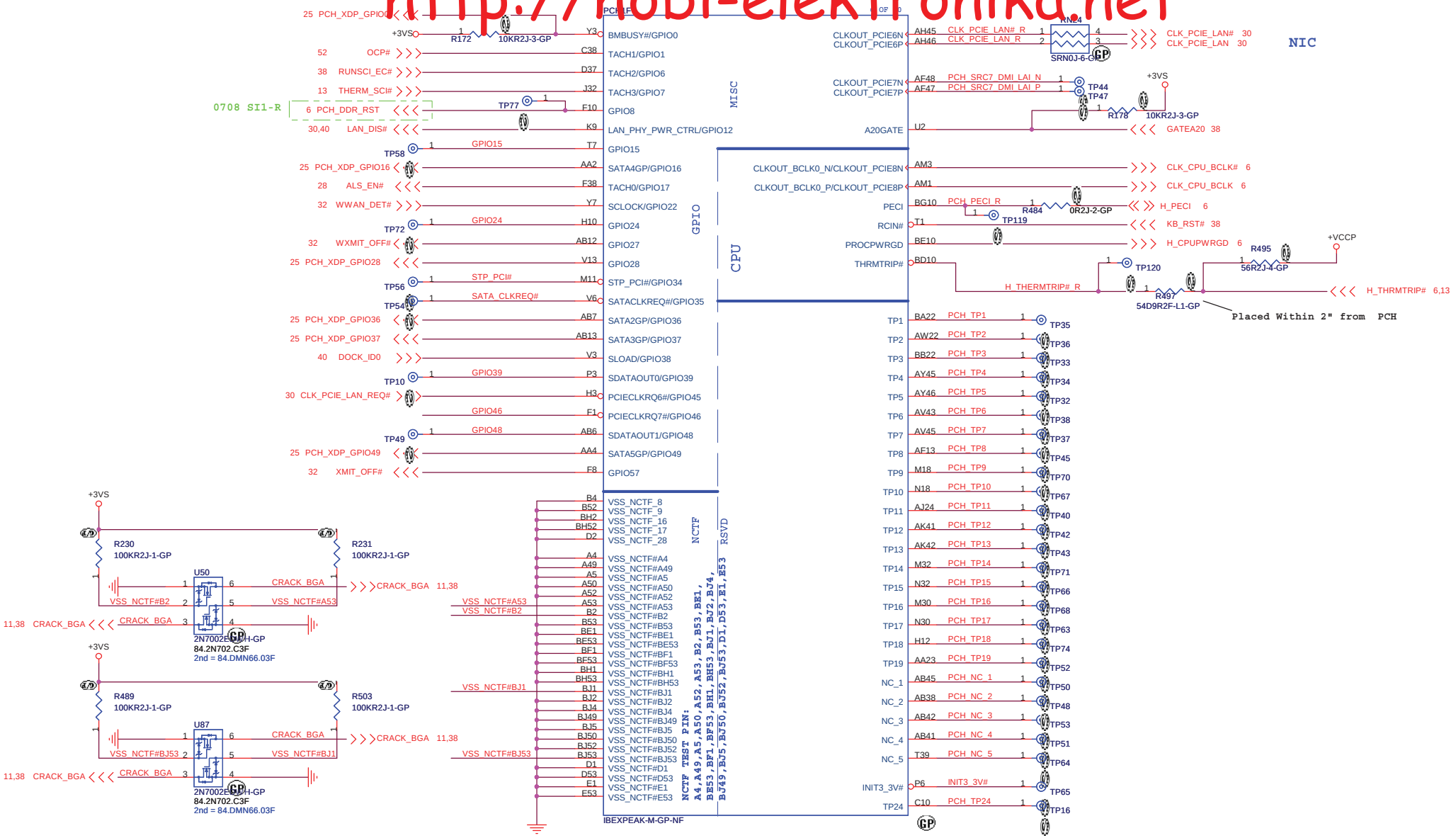
Title: PCH(4/9)-LVDS+DDI

Size: A3 | Document Number: NORN 3.0 | Rev: SE

Date: Thursday, September 10, 2009 | Sheet 19 of 57







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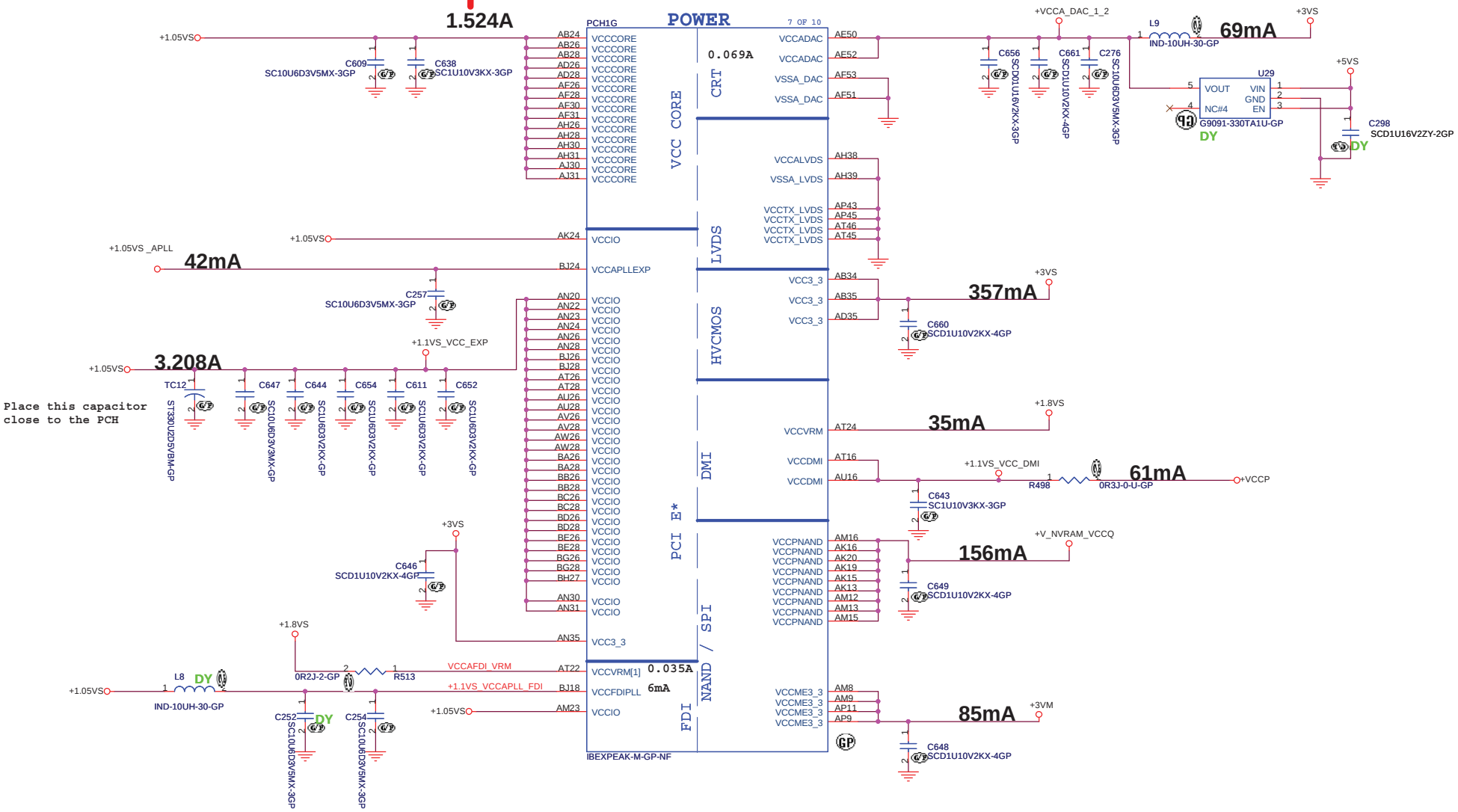
Title: PCH(6/9)-GPIO+VSS_NCTF+RSVD

| Size | Document Number | Rev |
|---|---|---|
| A3 | NORN 3.0 | SE |

Date: Thursday, September 10, 2009 Sheet 21 of 57




<Core Design>

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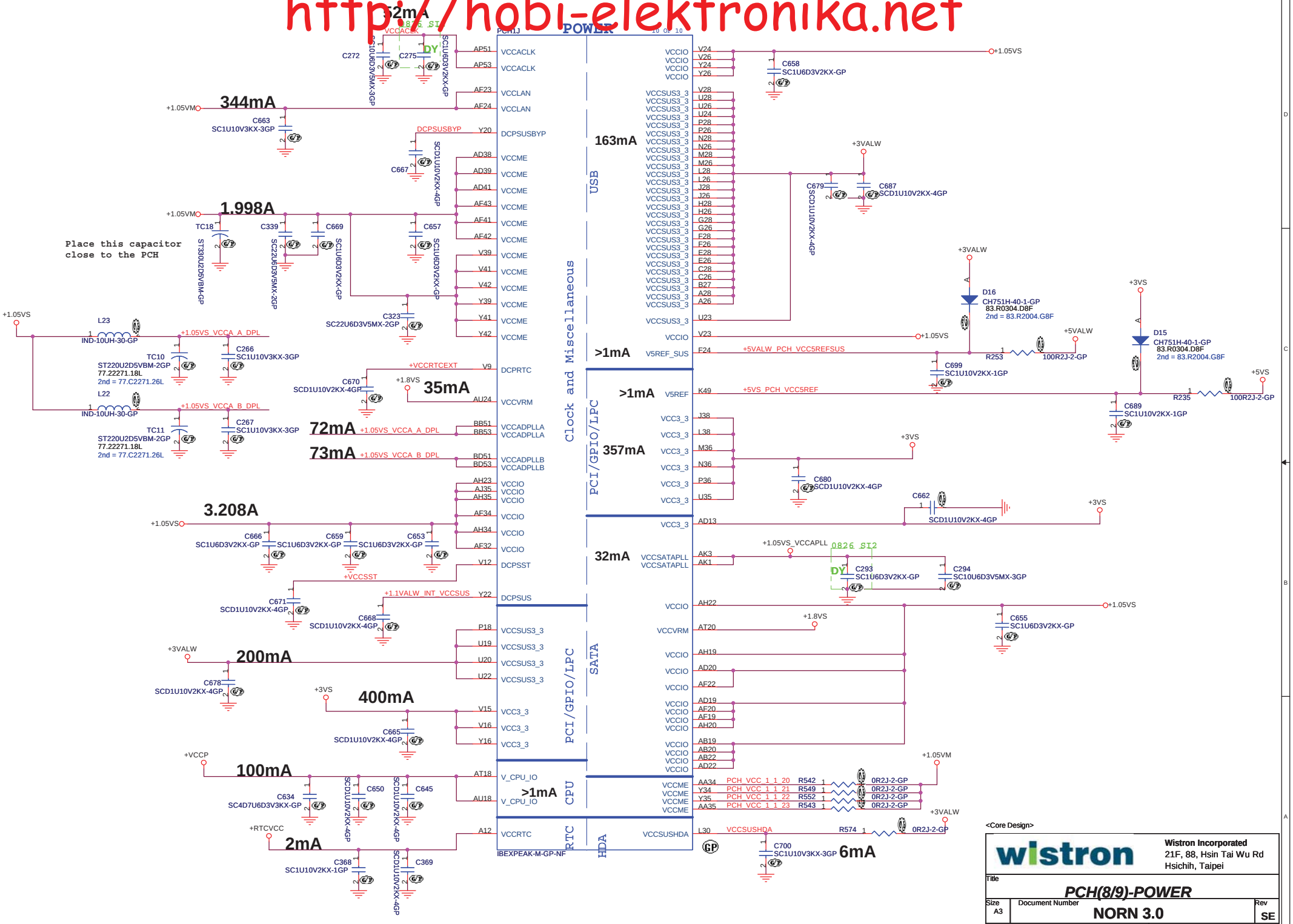
Hsichih, Taipei

Title: PCH(7/9)-POWER

| Size | Document Number | Rev |
|---|---|---|
| A3 | NORN 3.0 | SE |

Date: Monday, August 17, 2009 Sheet 22 of 57





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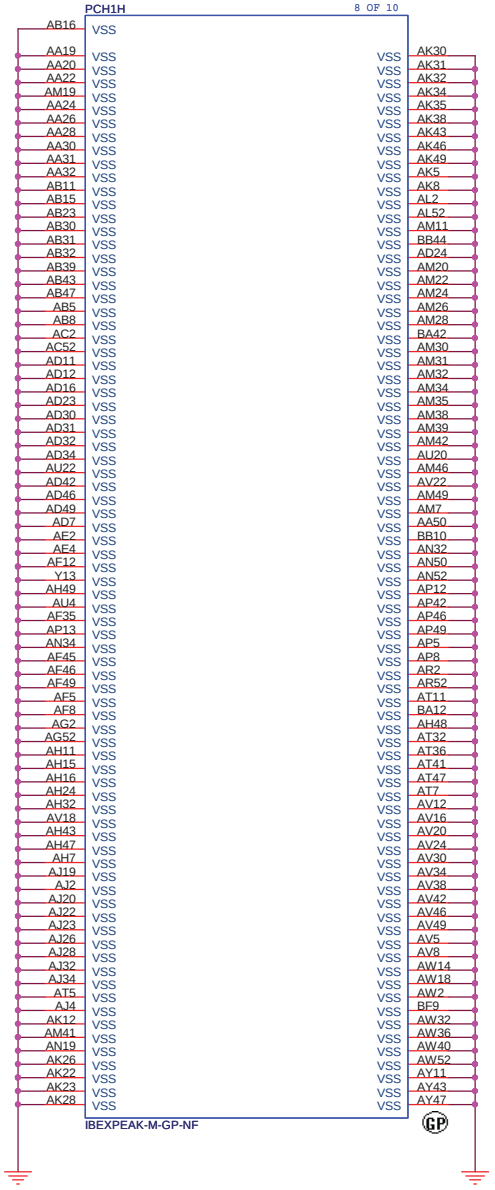
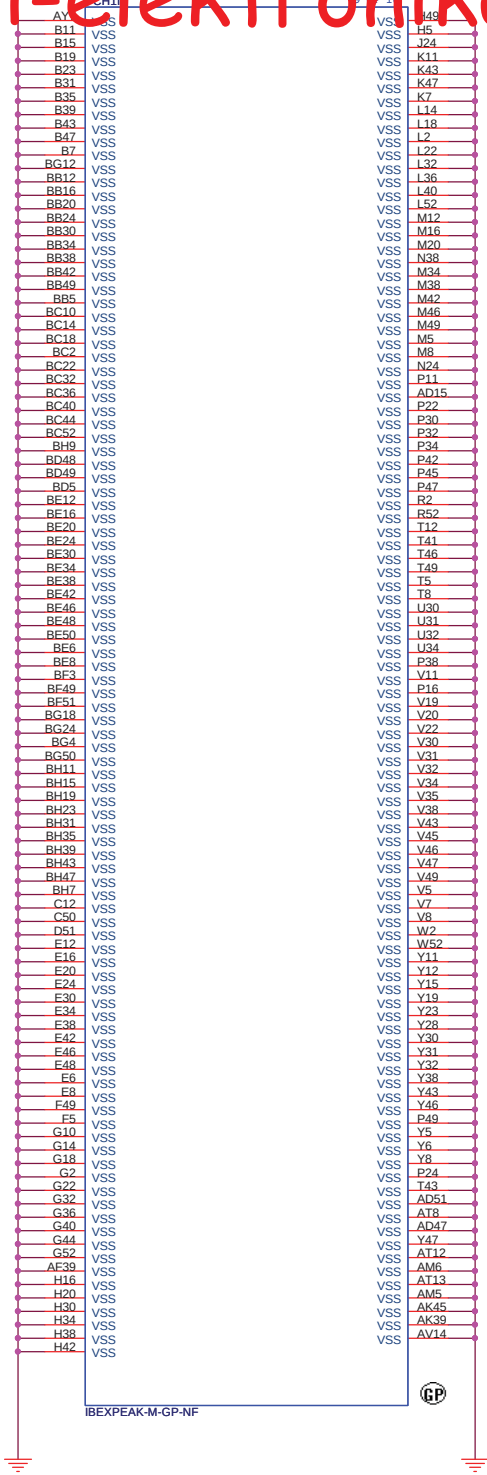
Title: PCH(8/9)-POWER
Size: A3
Document Number: NORN 3.0
Rev: SE
Date: Wednesday, August 26, 2009
Sheet 23 of 57

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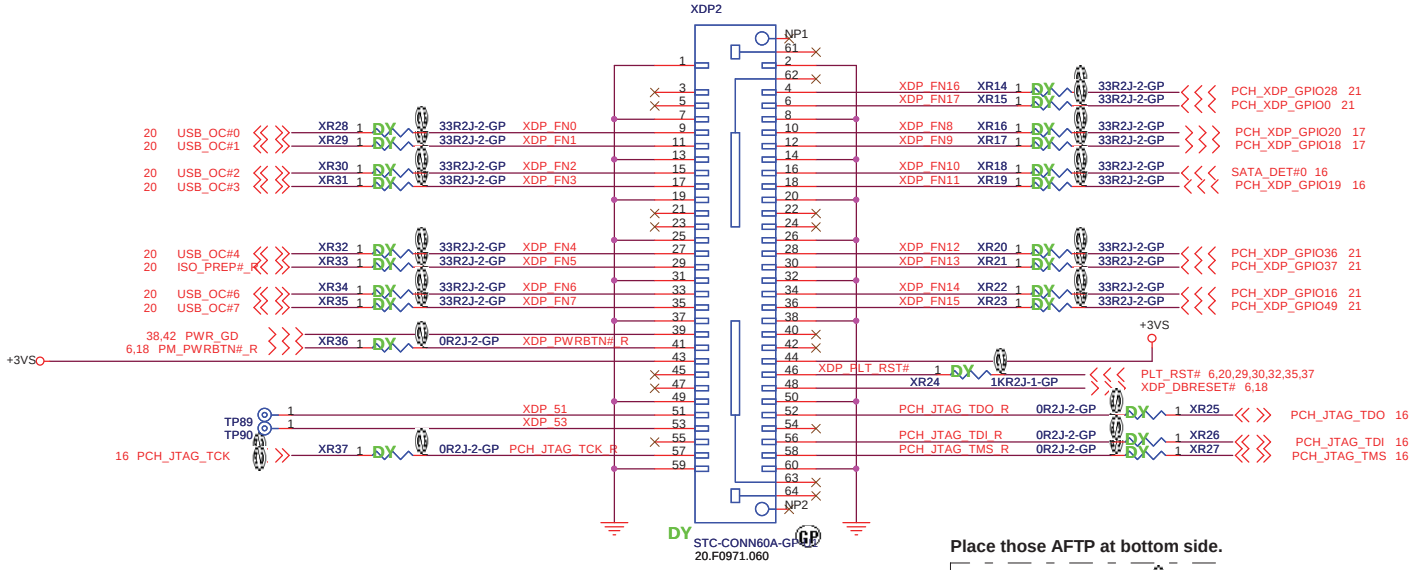
Title: PCH(9/9)-GND

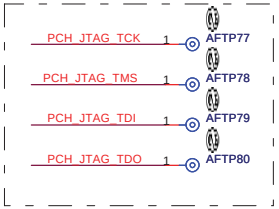
| Size | Document Number | Rev |
|---|---|---|
| A3 | NORN 3.0 | SE |

Date: Monday, August 17, 2009 Sheet 24 of 57

0626 SI1
Remove XDP2 and relative circuits.
0711 SI1-R
Add back.




**Place those AFTP at bottom side.**

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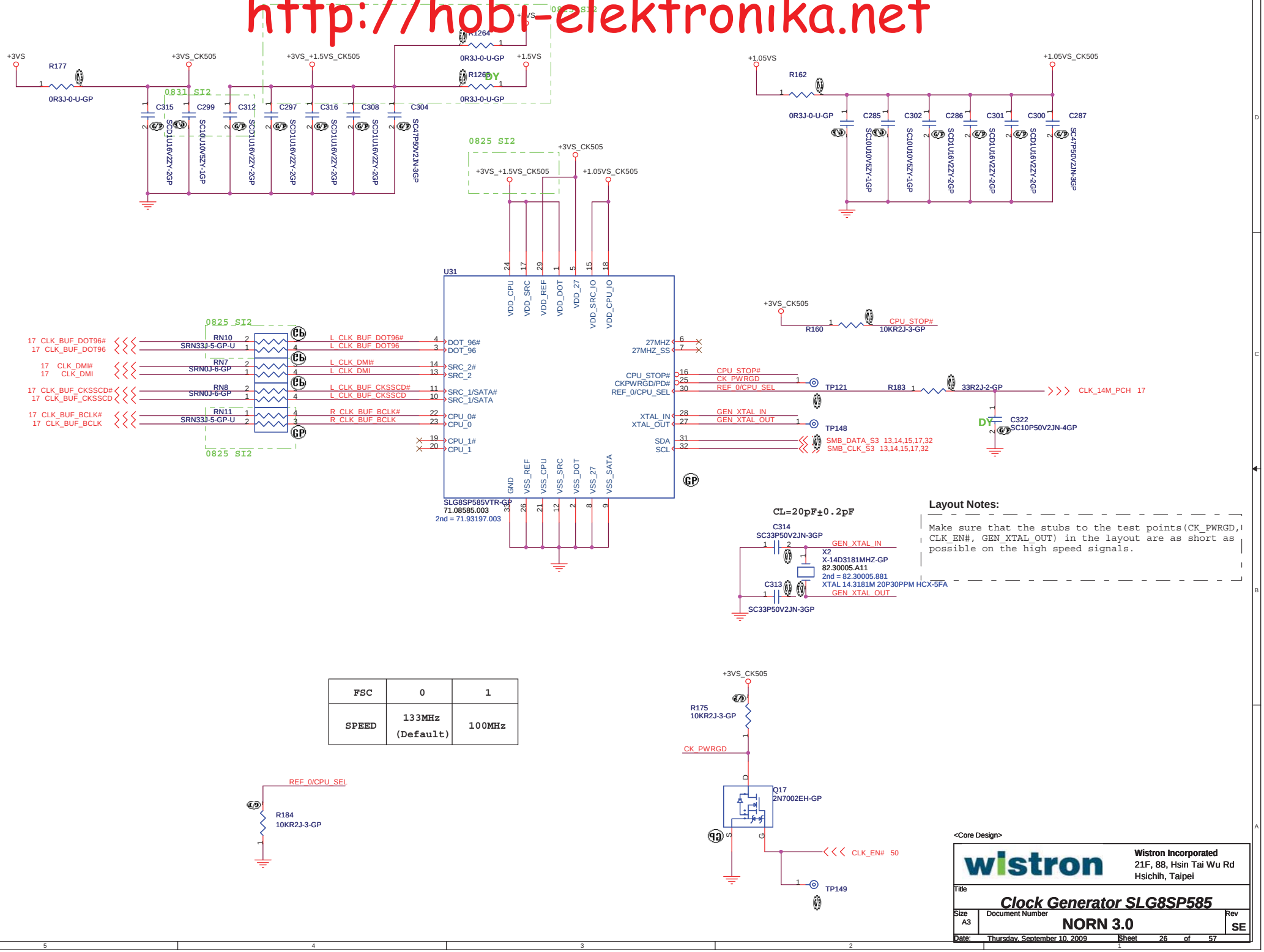
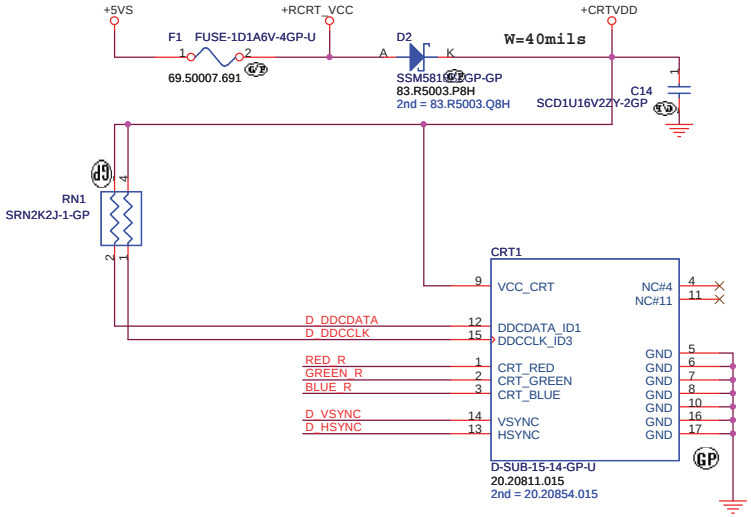
Title: PCH XDP

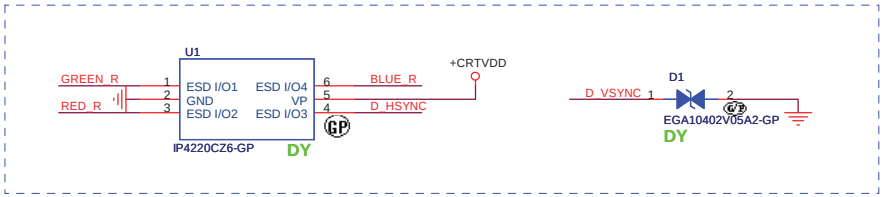
| Size | Document Number | Rev |
|---|---|---|
| A3 | NORN 3.0 | SE |

Date: Thursday, September 10, 2009 Sheet 25 of 57

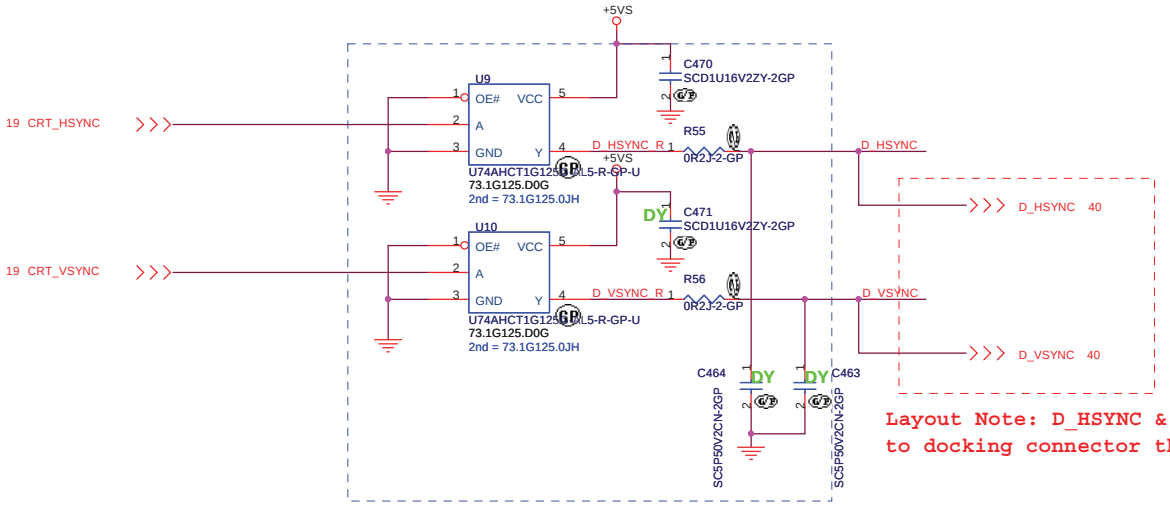


# CRT connector

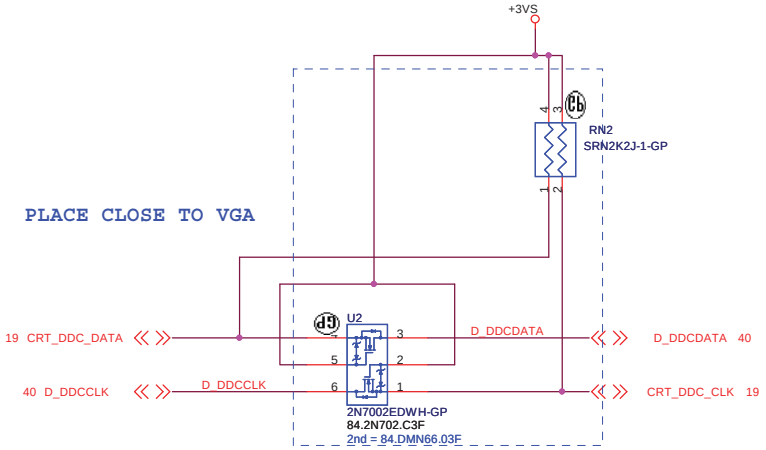




Place near the CRT connector




PLACE CLOSE TO VGA

Layout Note: D_HSYNC & D_VSYNC should be routed to docking connector then to VGA connector

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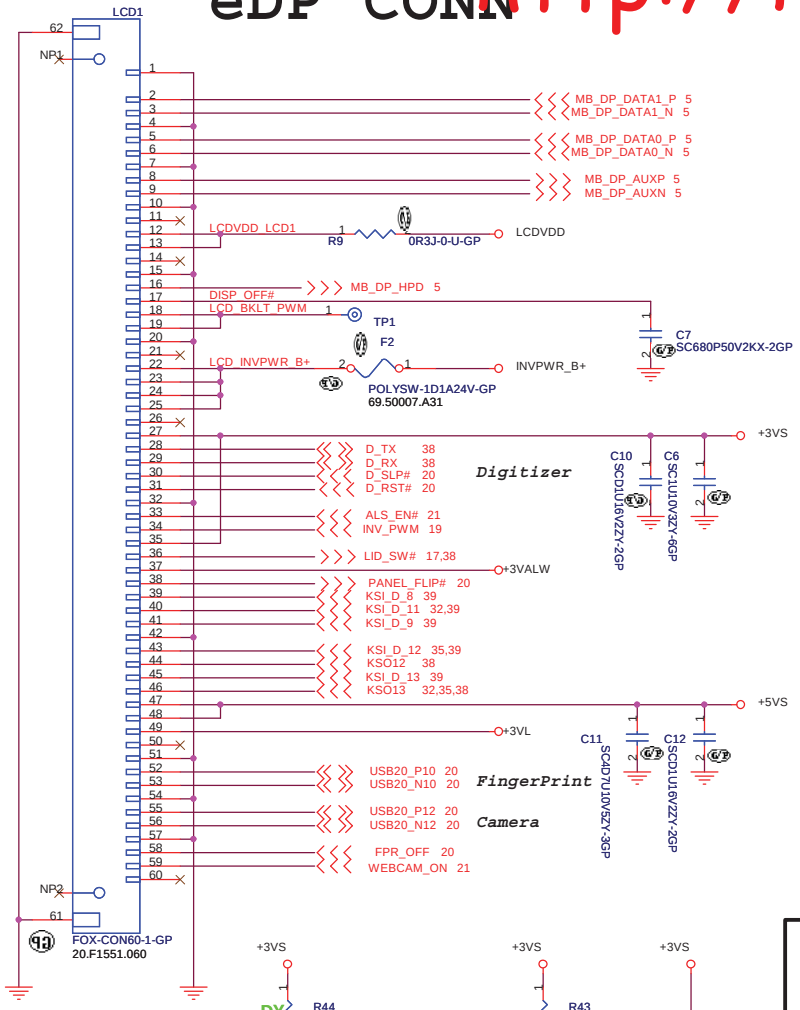
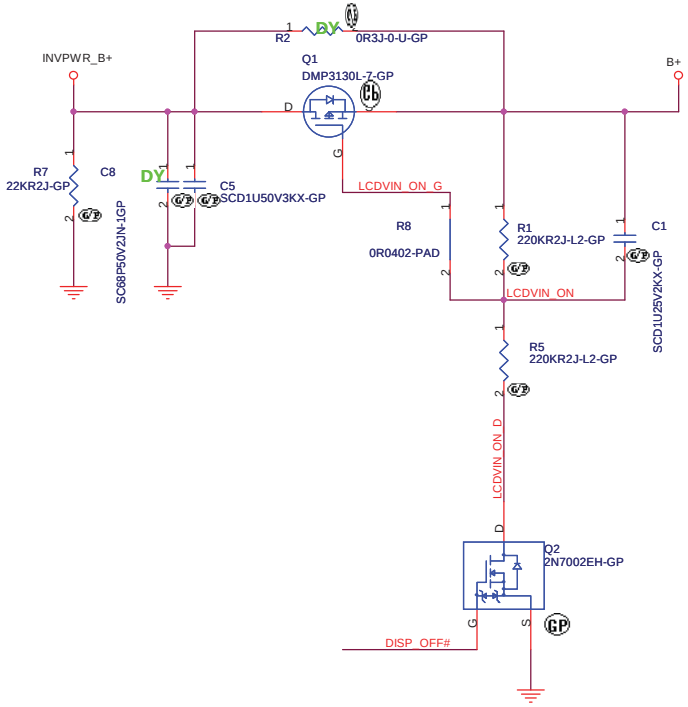
Title: CRT/TV CONNECTOR

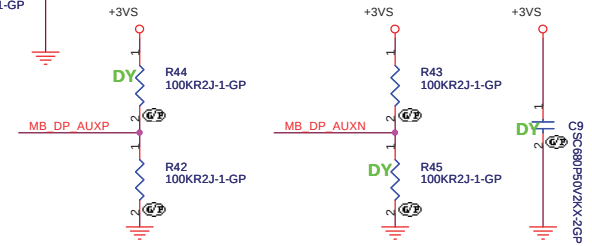
Size: A3 | Document Number: NORN 3.0 | Rev: SE

Date: Thursday, September 10, 2009 | Sheet 27 of 57

# eDP CONN

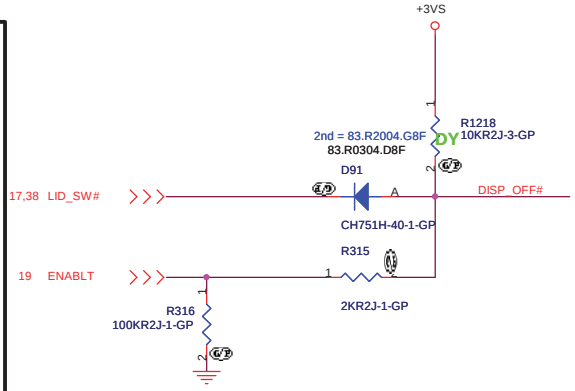



# LCD POWER CIRCUIT

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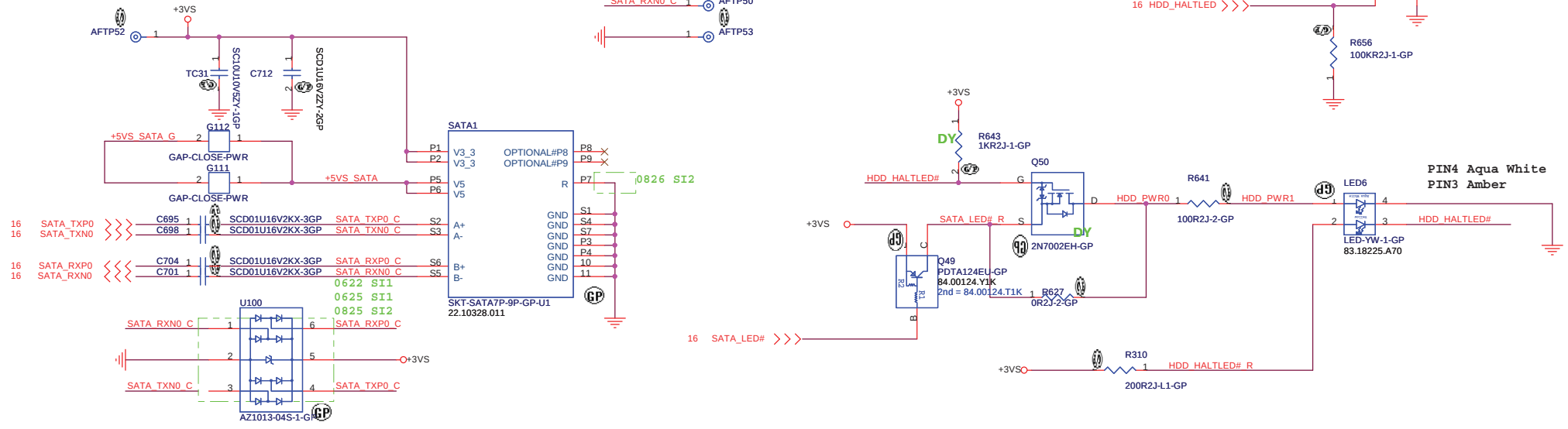
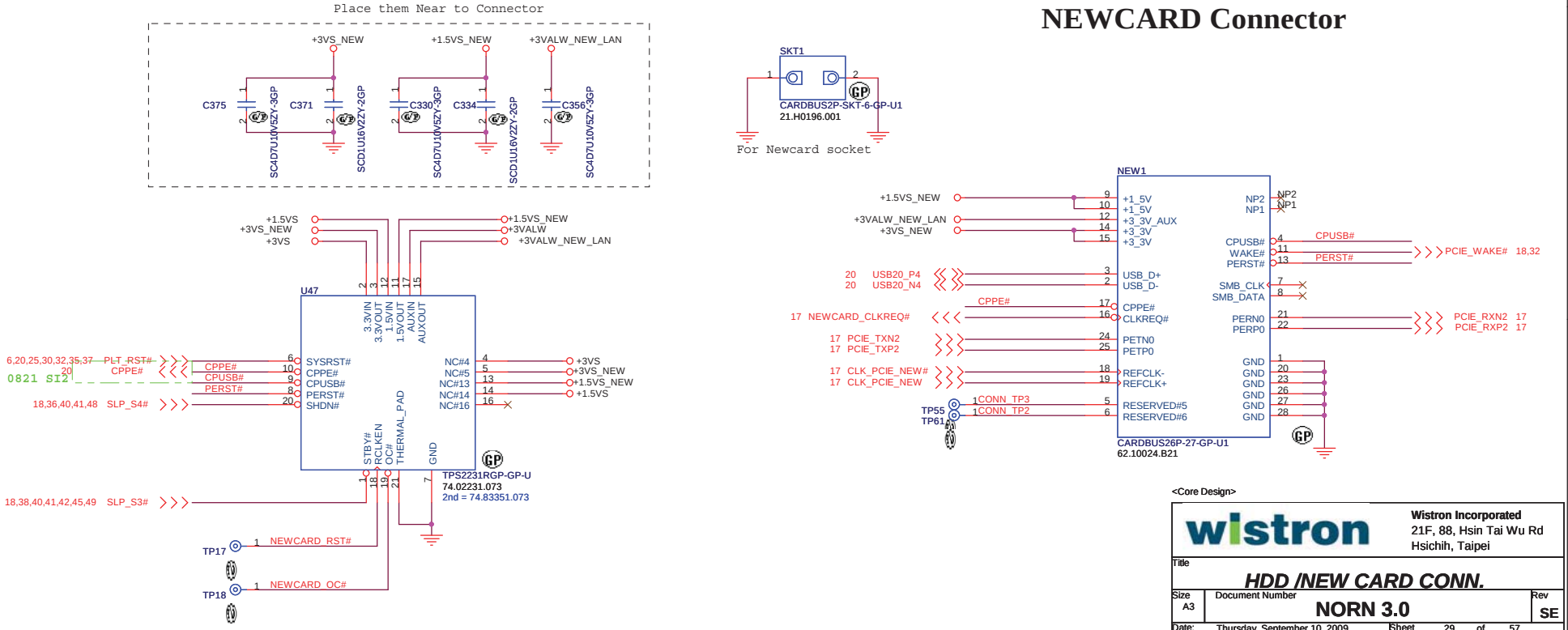
| Title | | |
|---|---|---|
| LCD CONN. | | |
| Size A3 | Document Number NORN 3.0 | Rev SE |
| Date: Thursday, September 10, 2009 | Sheet 28 of 57 | |

# SATA HDD




# NEWCARD Connector

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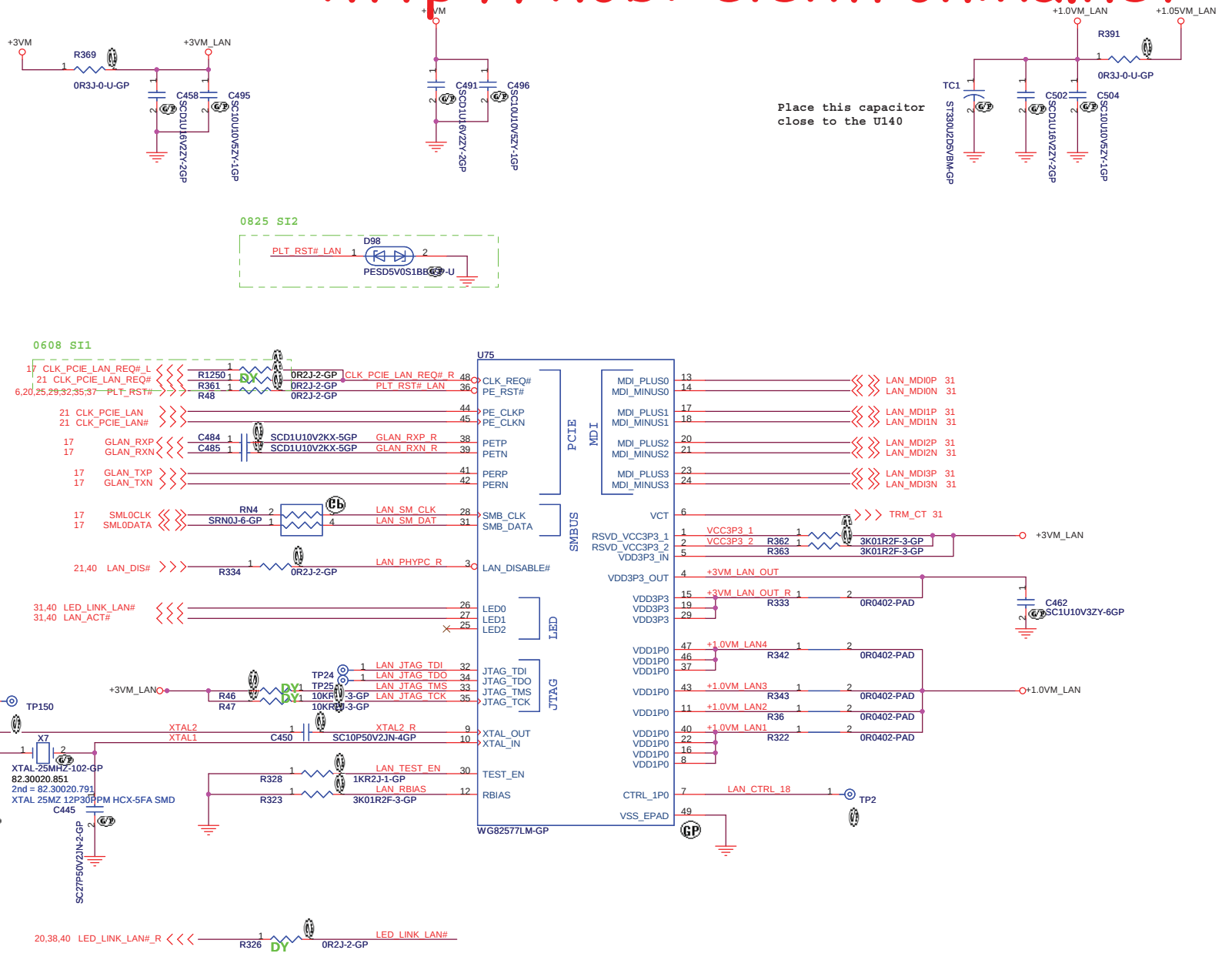
Title: HDD /NEW CARD CONN.

Size: A3 | Document Number: NORN 3.0 | Rev: SE

Date: Thursday, September 10, 2009 | Sheet 29 of 57

From Power




**Layout Notes:**

Make sure that the stubs to the test points(XTAL2) in the layout are as short as possible on the high speed signals.

<Core Design>

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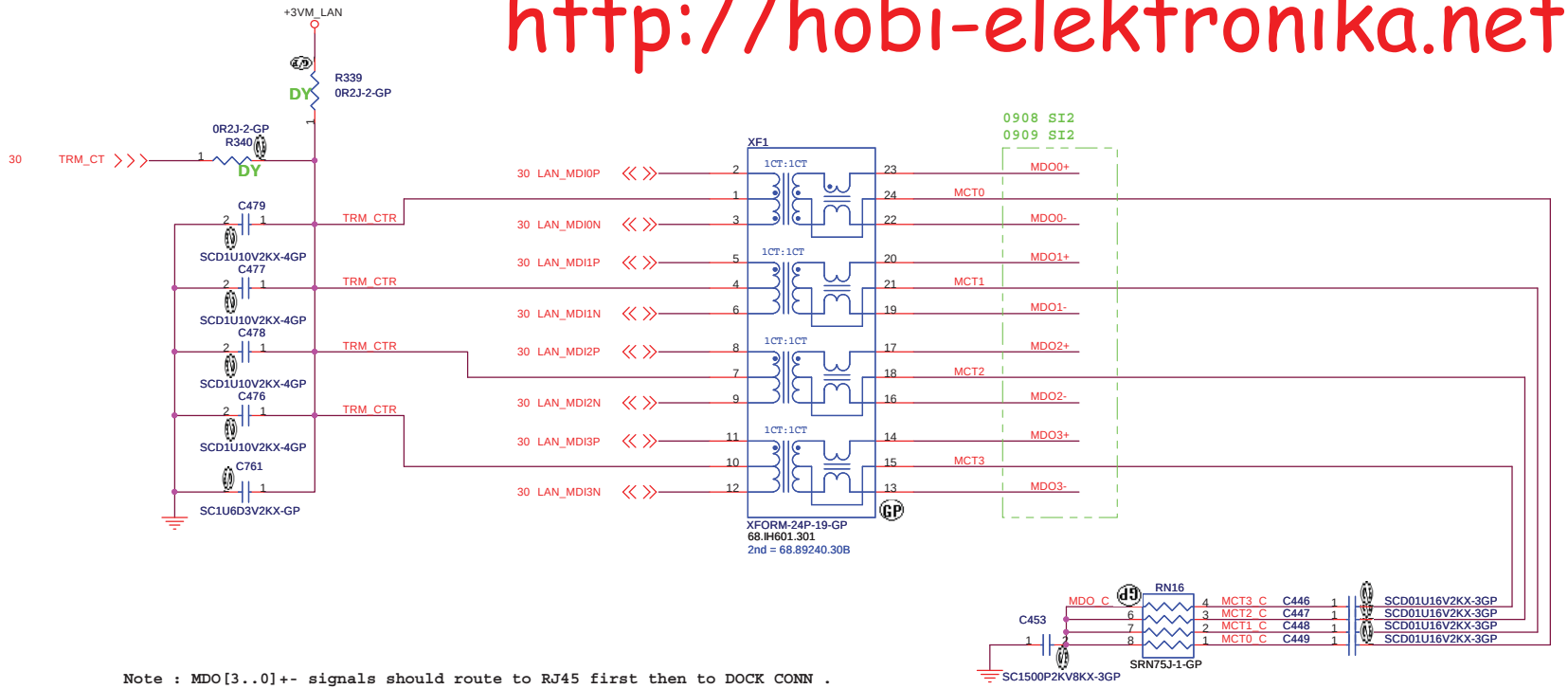
Hsichih, Taipei

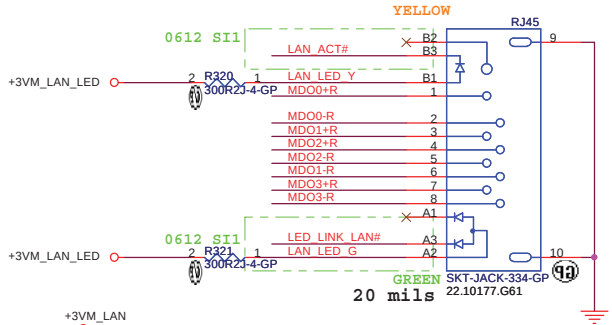
Title: *Intel 82577 Bavoz*

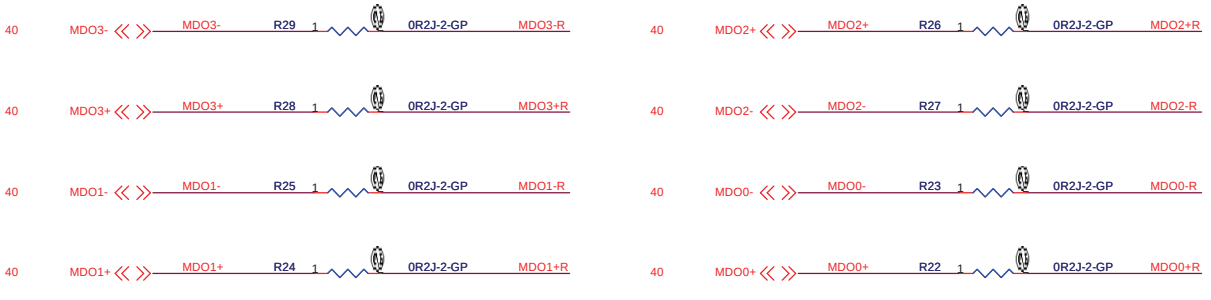
Size: A3 | Document Number: NORN 3.0 | Rev: SE

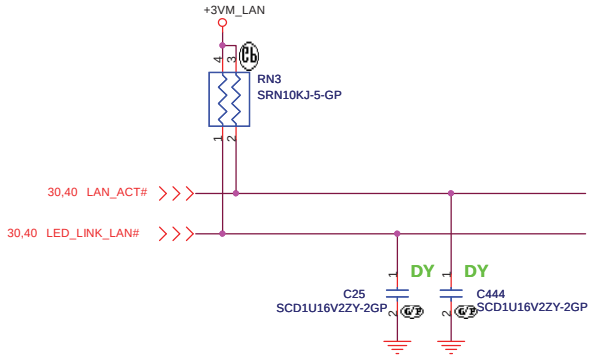
Date: Thursday, September 10, 2009 | Sheet 30 of 57

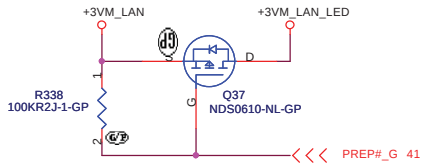



Note : MDO[3..0]+- signals should route to RJ45 first then to DOCK CONN .

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Title: Magnetic & RJ45

| Size | Document Number | Rev |
|---|---|---|
| A3 | NORN 3.0 | SE |

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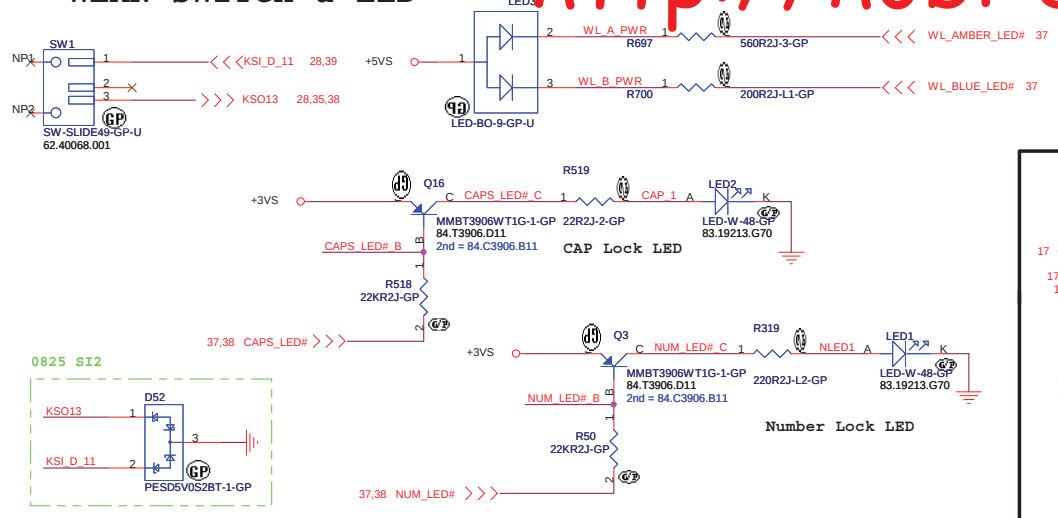
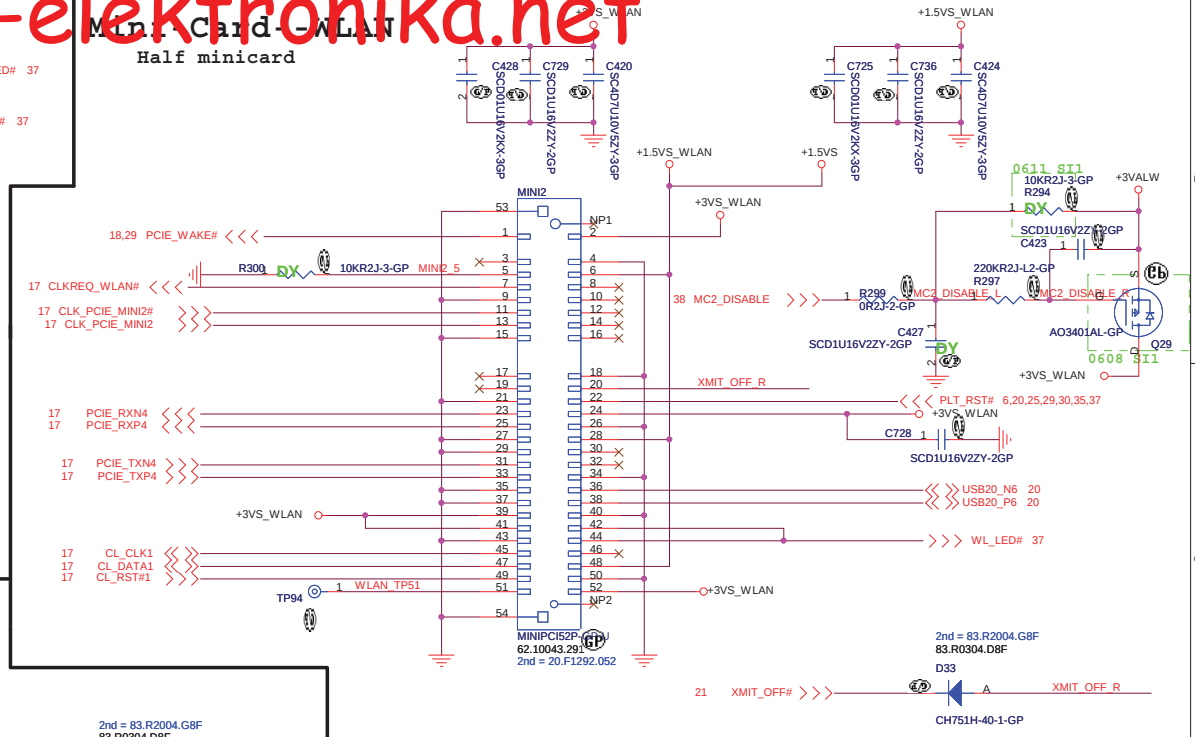
# WLAN SWITCH & LED



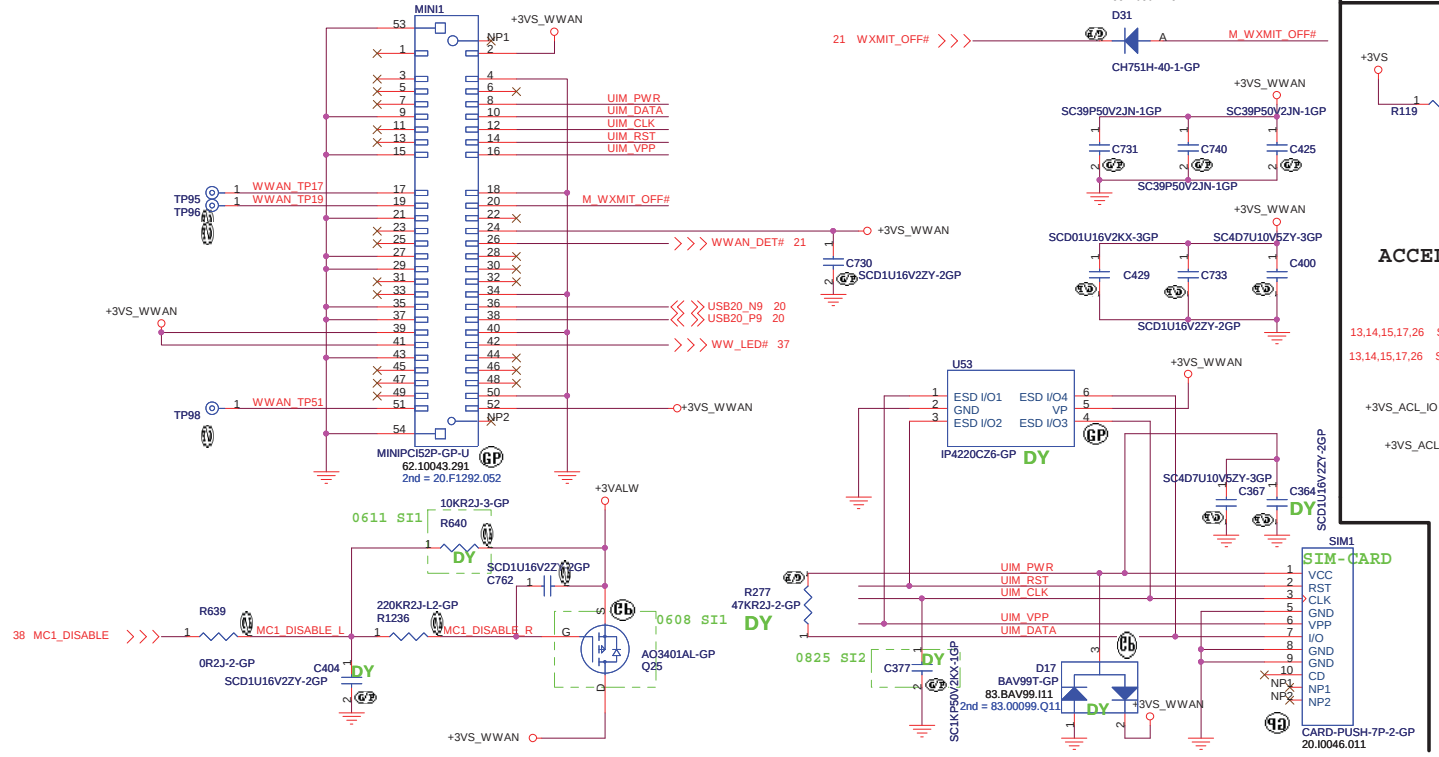

# Mini-Card--WLAN

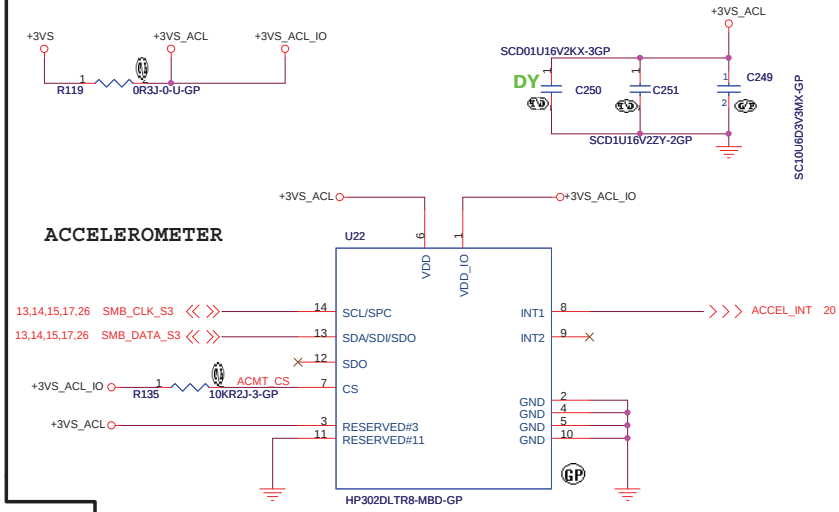
Half minicard




# Mini-Card--WWAN

Full minicard

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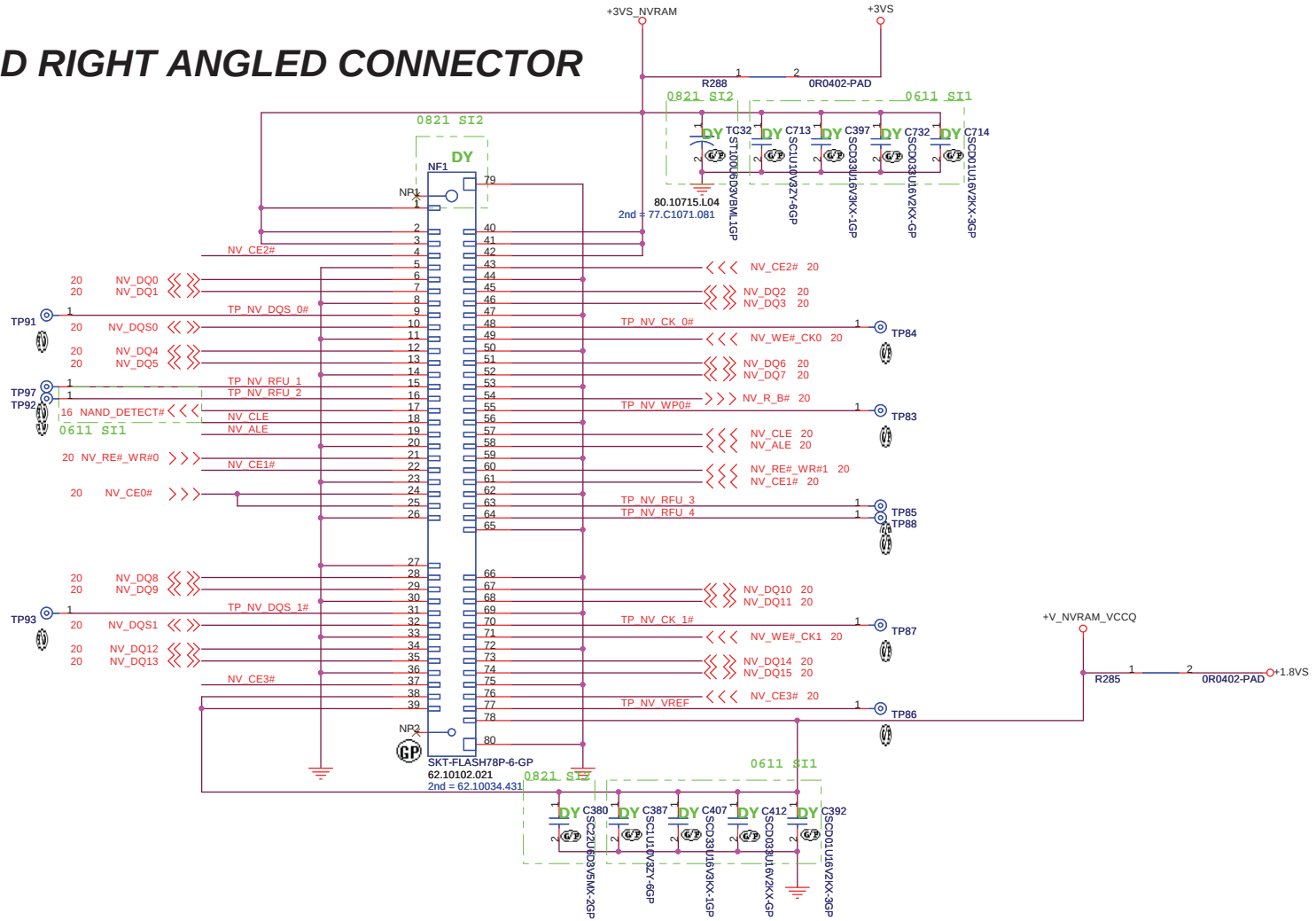
Title: Mini-Card/Accelerometer

Size: Custom | Document Number: NORN 3.0 | Rev: SE

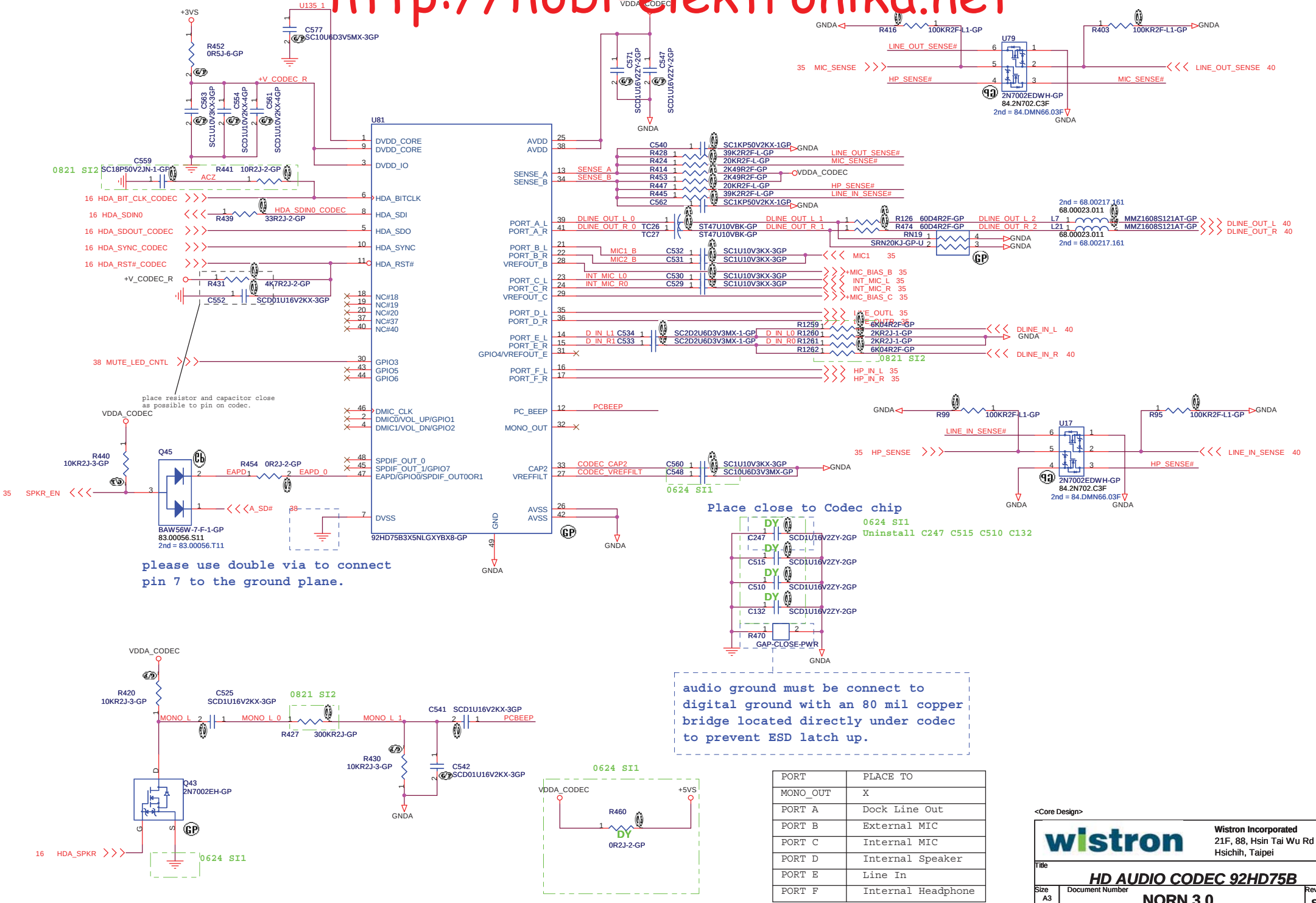
Date: Thursday, September 10, 2009 | Sheet 32 of 57

# BRAIDWOOD RIGHT ANGLED CONNECTOR




<Core Design>

| | |
|---|---|
| wistron | Wistron Incorporated<br>21F, 88, Hsin Tai Wu Rd<br>Hsichih, Taipei |
| Title | NAND FLASH CONN |
| Size A3 | Document Number NORN 3.0 Rev SE |
| Date: Thursday, September 10, 2009 | Sheet 33 of 57 |




| PORT | PLACE TO |
|---|---|
| MONO_OUT | X |
| PORT A | Dock Line Out |
| PORT B | External MIC |
| PORT C | Internal MIC |
| PORT D | Internal Speaker |
| PORT E | Line In |
| PORT F | Internal Headphone |

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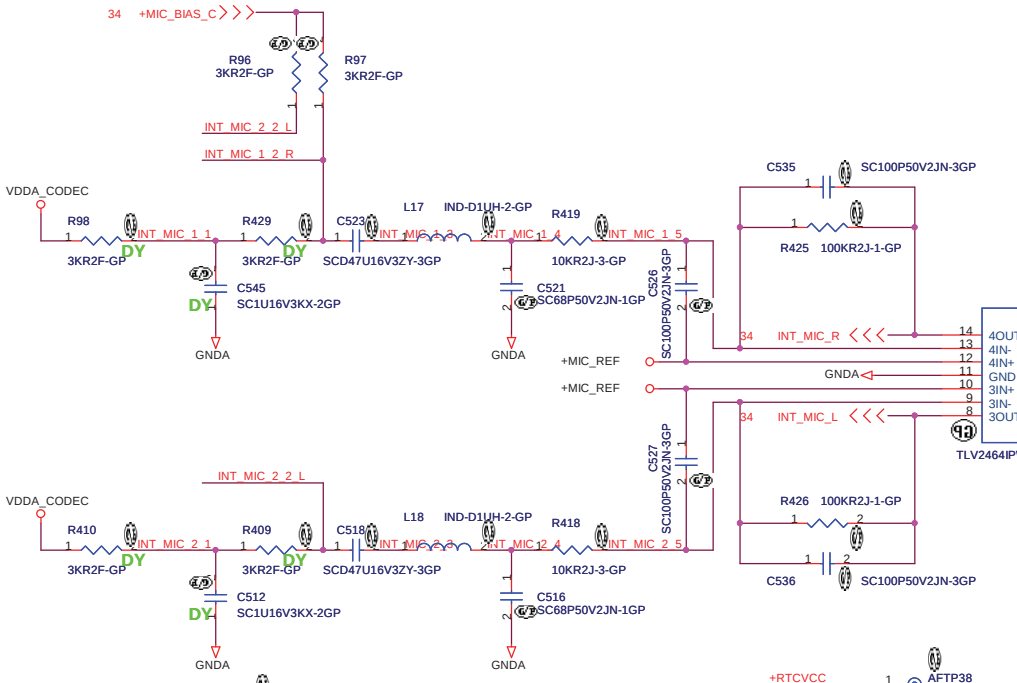
Title: HD AUDIO CODEC 92HD75B

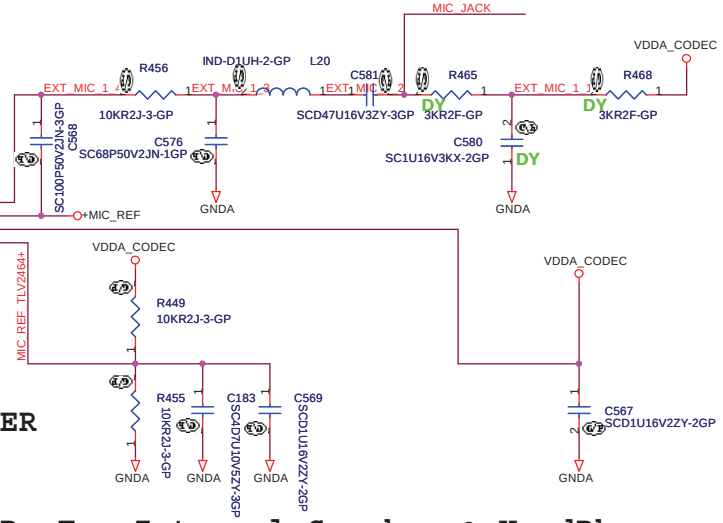
Size: A3 | Document Number: NORN 3.0 | Rev: SE

Date: Thursday, September 10, 2009 | Sheet 34 of 57

AMP. for Internal Microphone

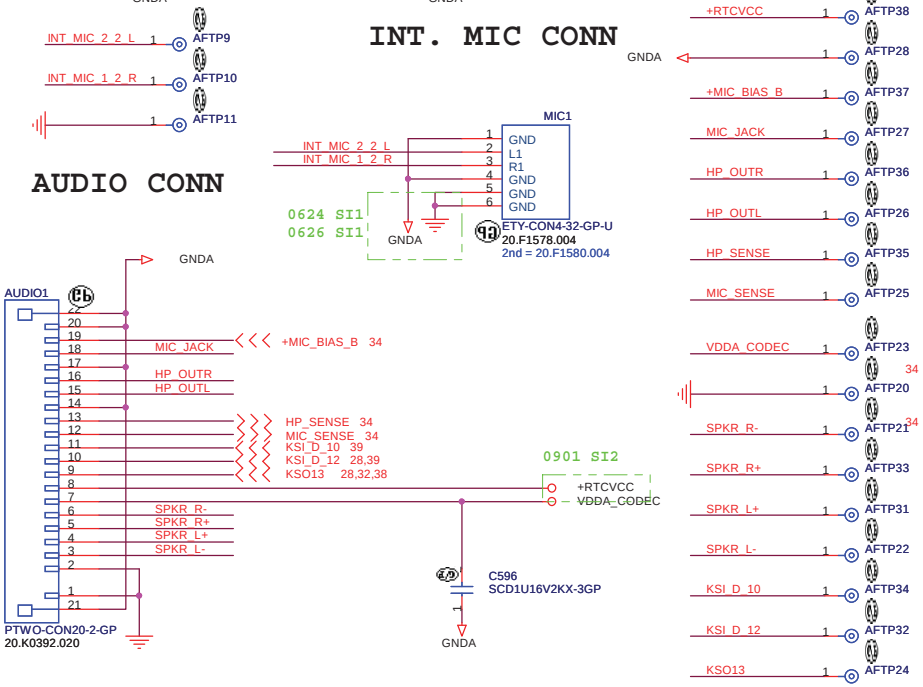
AMP. for External Microphone




VREF BUFFER

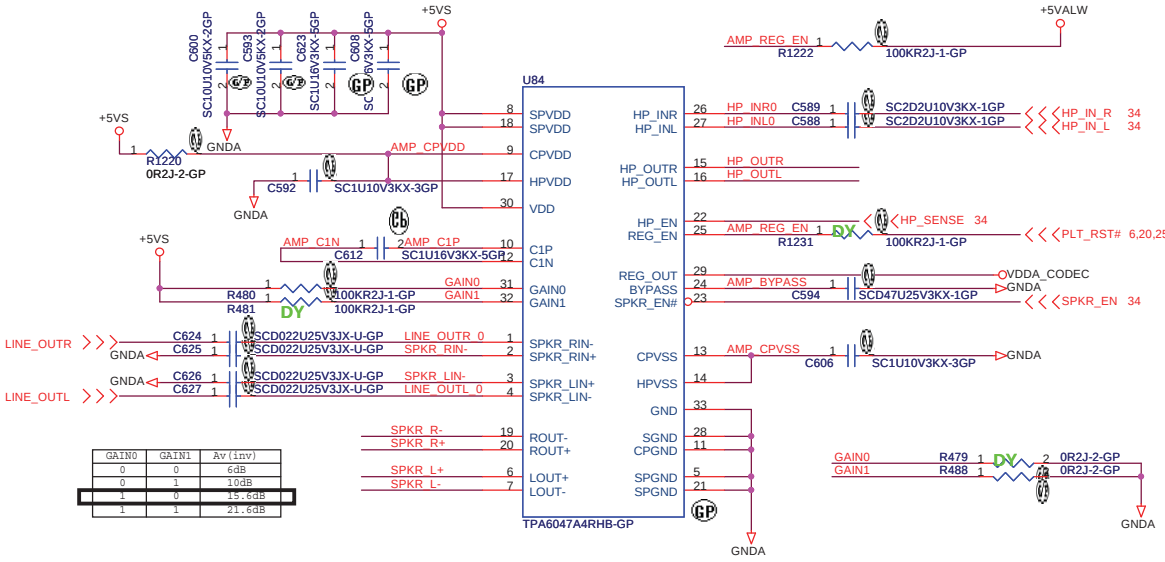
INT. MIC CONN




AUDIO CONN




AMP. For Internal Speaker & HeadPhone.




| GAIN0 | GAIN1 | Av(inv) |
|---|---|---|
| 0 | 0 | 6dB |
| 0 | 1 | 10dB |
| 1 | 0 | 15.6dB |
| 1 | 1 | 21.6dB |

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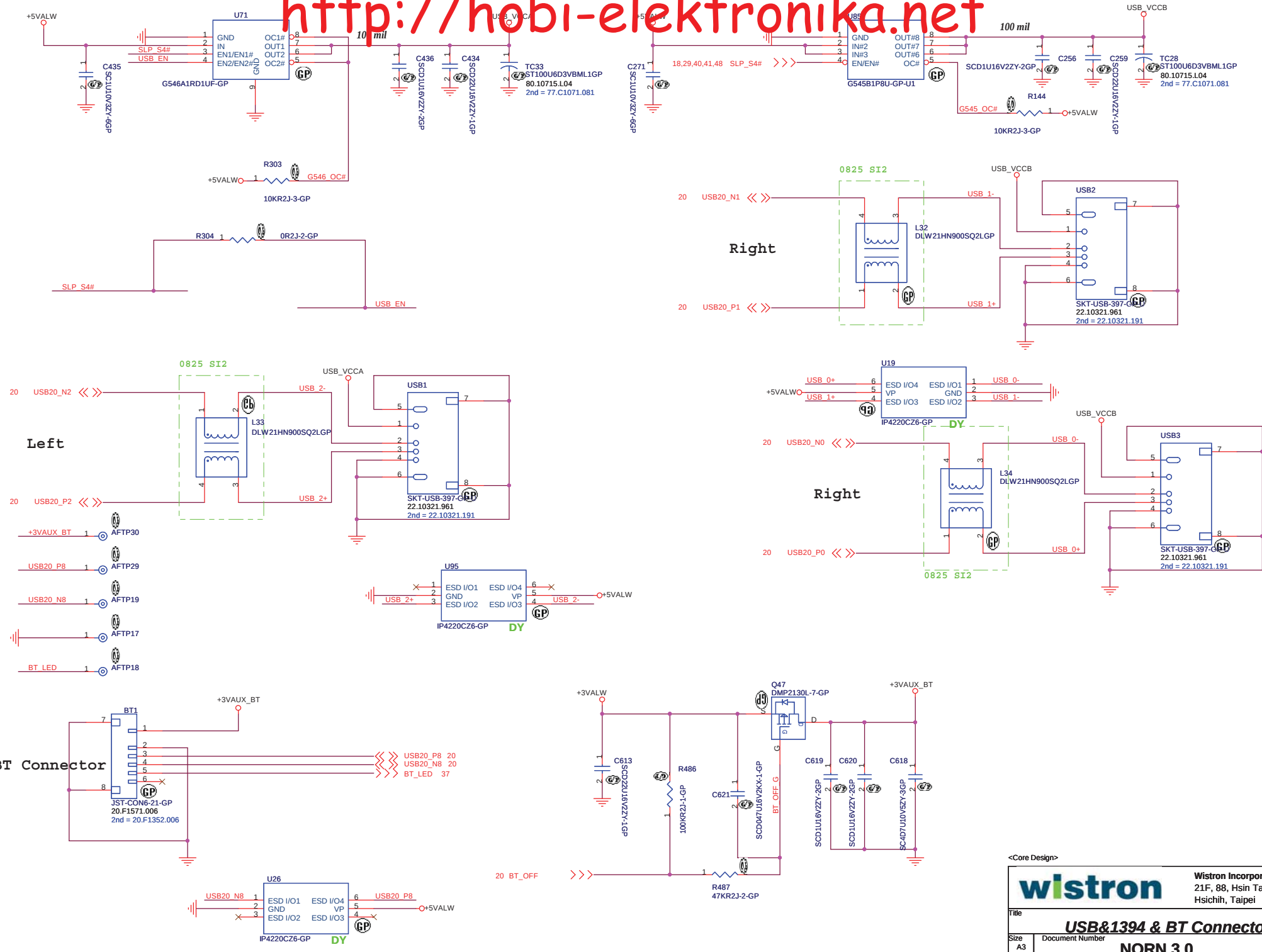
Hsichih, Taipei

Title: AMP & Audio Conn.

Size: A3 | Document Number: NORN 3.0 | Rev: SE

Date: Thursday, September 10, 2009 | Sheet 35 of 57




<Core Design>

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Hsichih, Taipei

Title: USB&1394 & BT Connector

| Size | Document Number | Rev |
|---|---|---|
| A3 | NORN 3.0 | SE |

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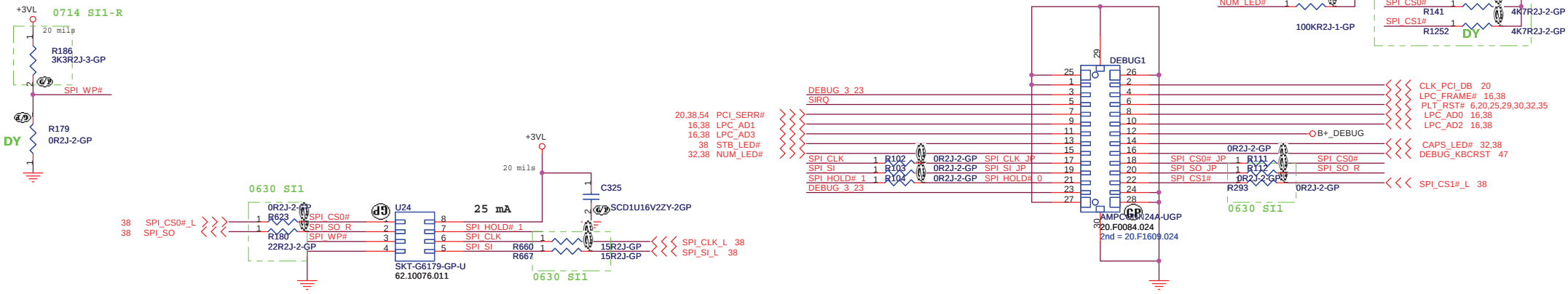
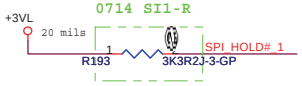
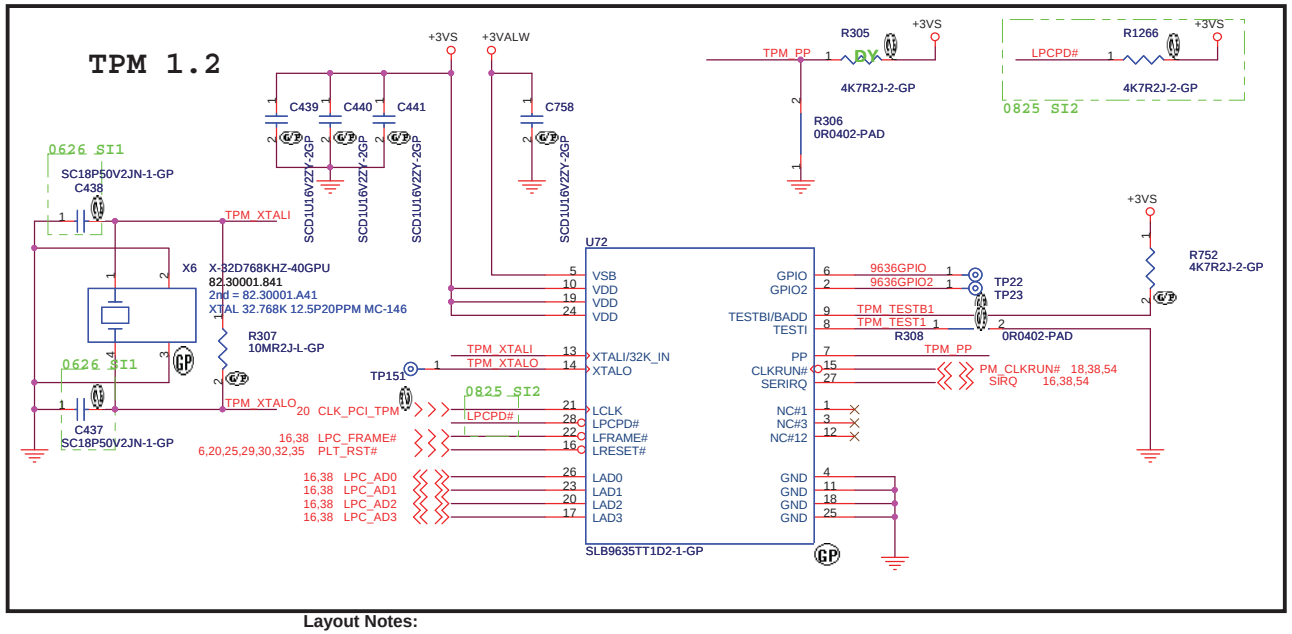
# LPC Debug Port



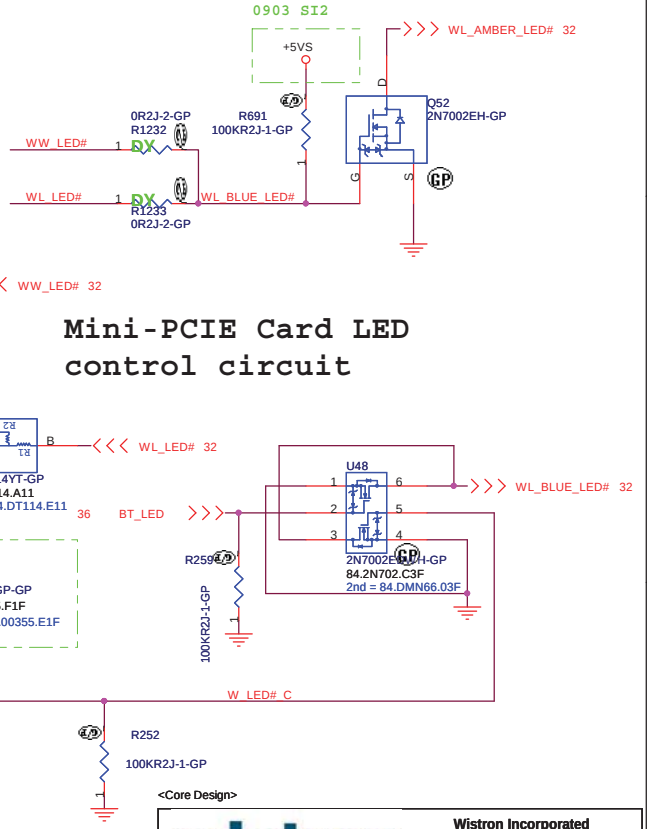

8M SPI
>72.25644.001 MX25L6445EM2I-10G 8-SOP
>72.25Q64.001 W25Q64BVSSIG SOIC-8




Layout Notes:

Make sure that the stubs to the test points(TPM_XTALO) in the layout are as short as possible on the high speed signals.

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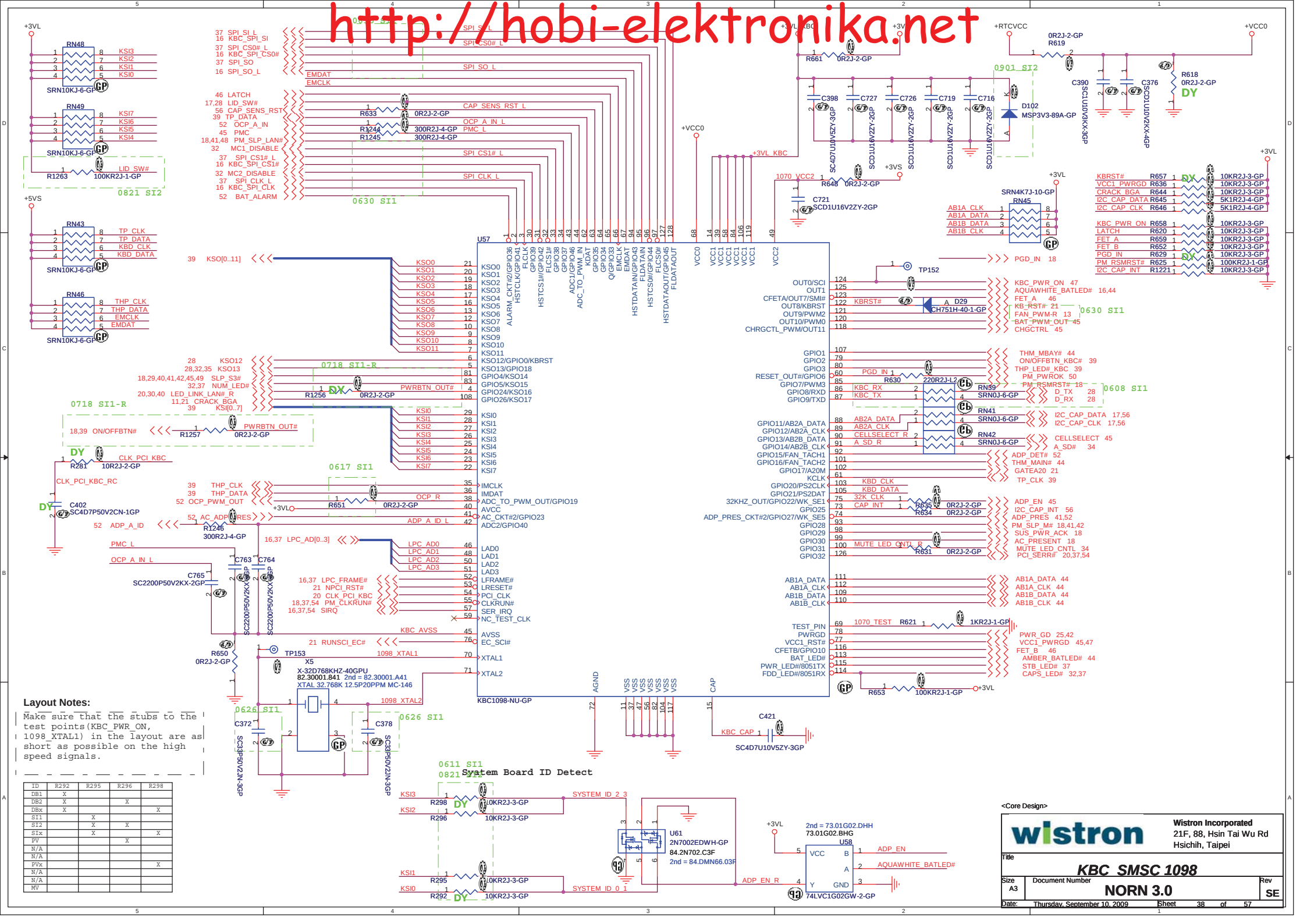
Hsichih, Taipei

Title: TPM/BIOS/24 DEBUG PORT

| Size | Document Number | Rev |
|---|---|---|
| A3 | NORN 3.0 | SE |

Date: Thursday, September 10, 2009 Sheet 37 of 57




**Layout Notes:**

Make sure that the stubs to the test points(KBC_PWR_ON, 1098_XTAL1) in the layout are as short as possible on the high speed signals.

| ID | R292 | R295 | R296 | R298 |
|---|---|---|---|---|
| DB1 | X | | | |
| DB2 | X | | X | |
| DBx | X | | | X |
| SI1 | | X | | |
| SI2 | | X | X | |
| SIx | | X | | X |
| PV | | | X | |
| N/A | | | | |
| N/A | | | | |
| PVx | | | | X |
| N/A | | | | |
| N/A | | | | |
| MV | | | | |

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Title: KBC SMSC 1098

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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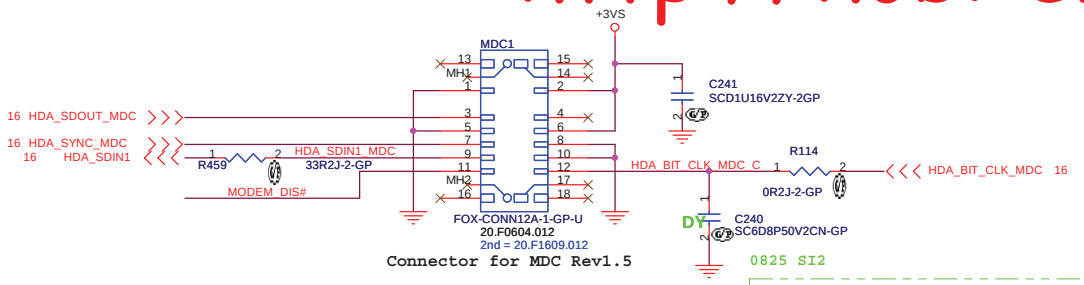
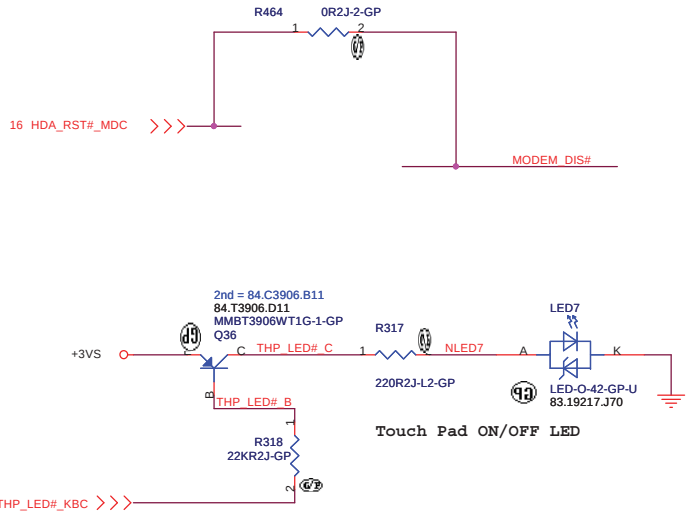
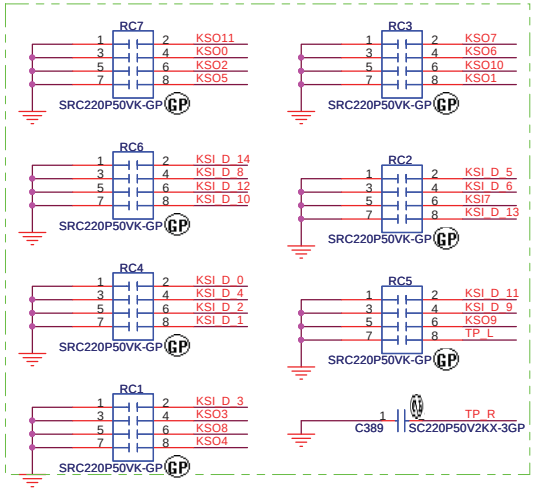
## MDC 1.5 Conn.



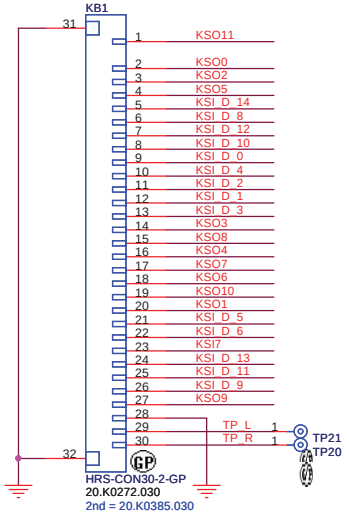

Connector for MDC Rev1.5



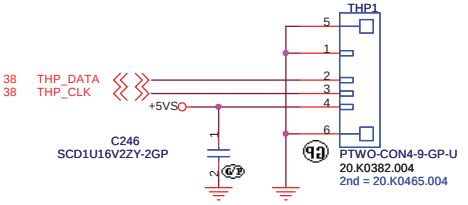

Touch Pad ON/OFF LED



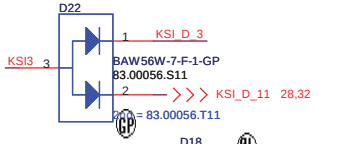

## INT_KBD CONN.

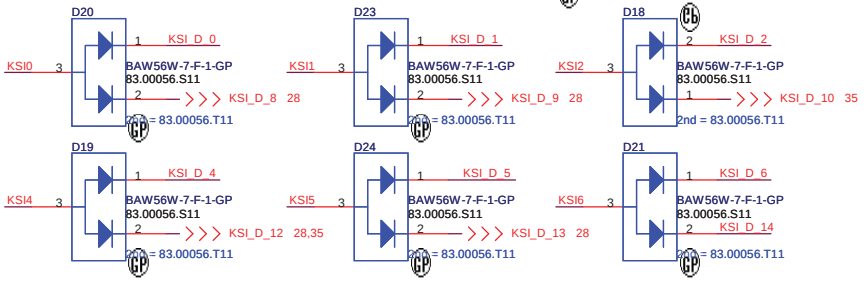




## Touch_Pad CONN.

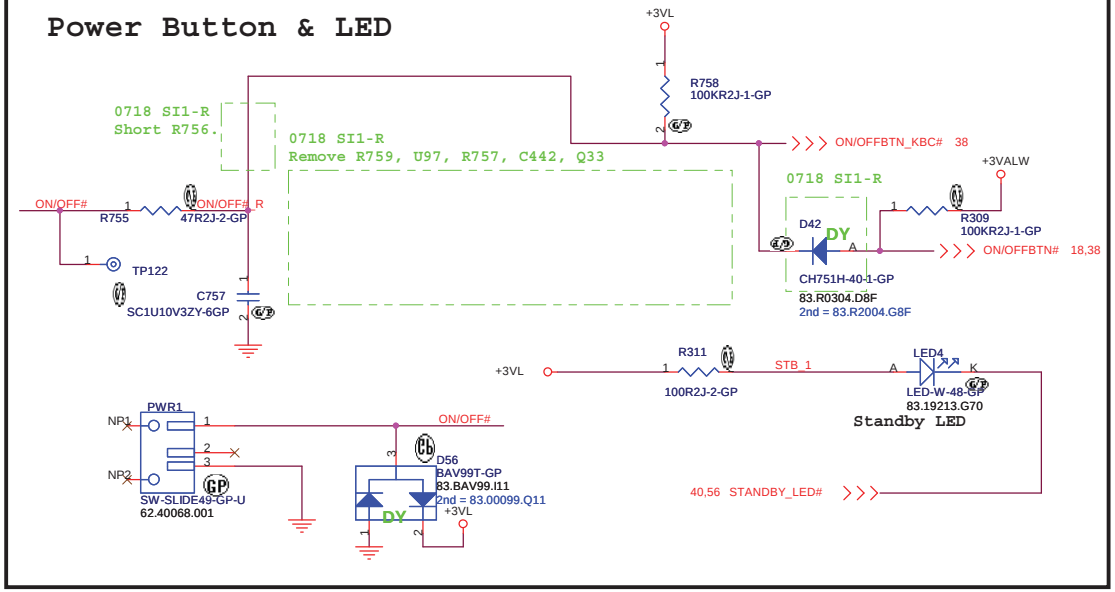




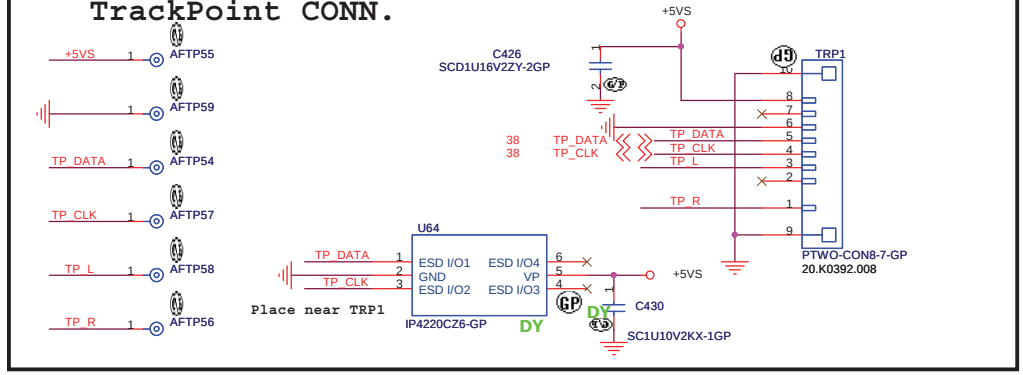


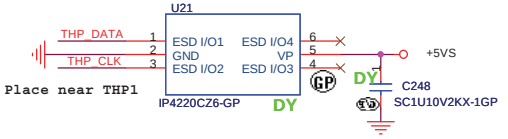




## Power Button & LED




## TrackPoint CONN.





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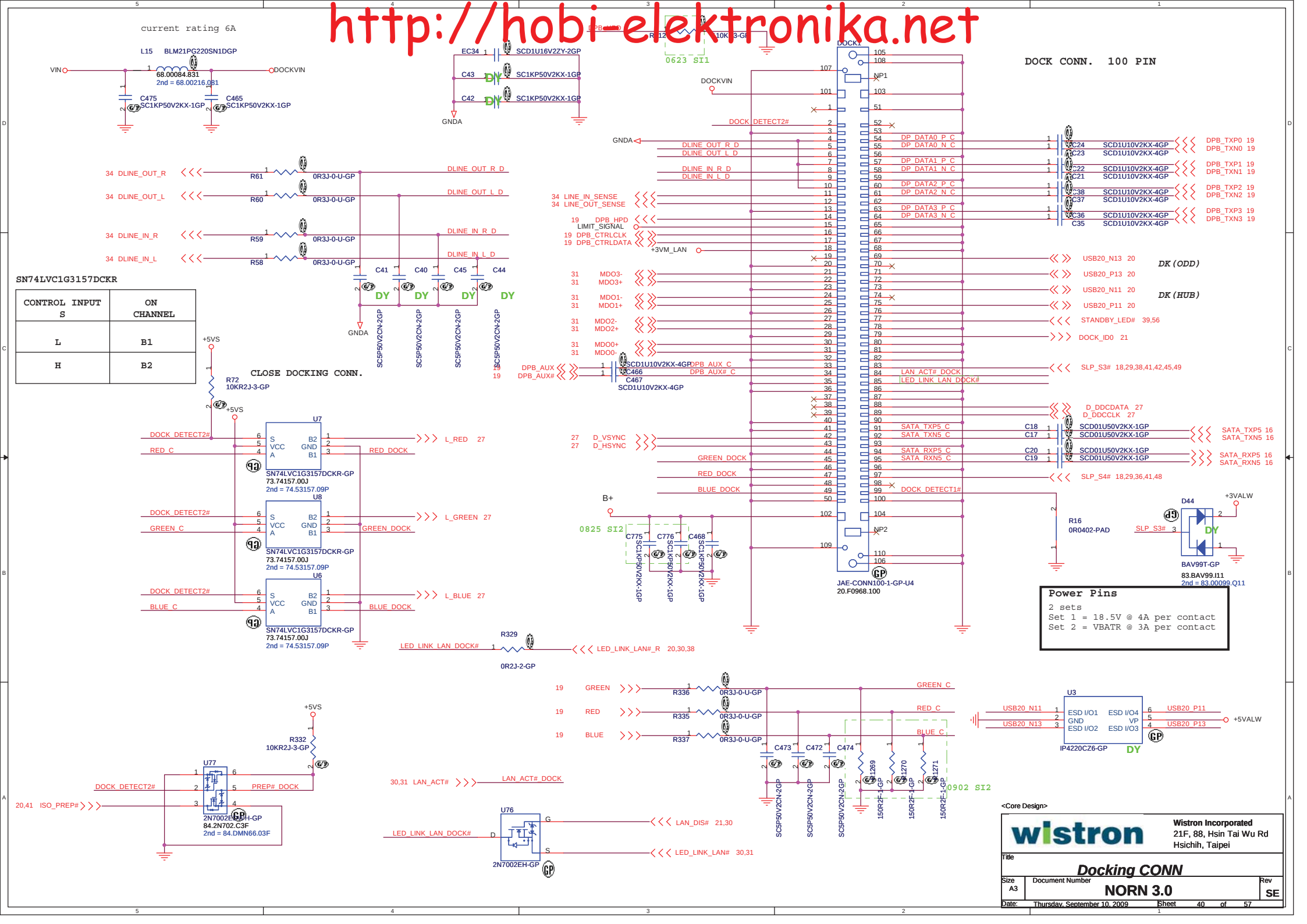


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Title: Docking CONN

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|---|---|---|
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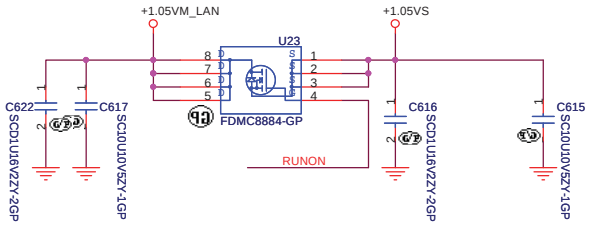
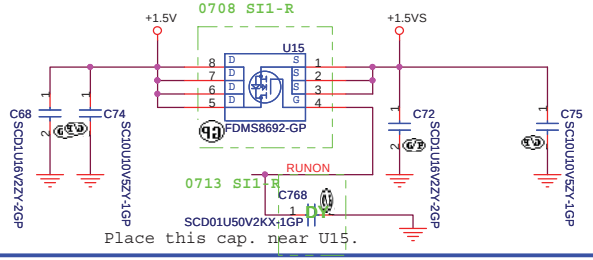
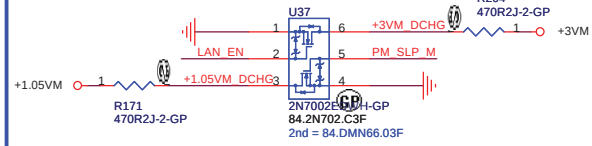
## +1.05VM_LAN to +1.05VS Transfer



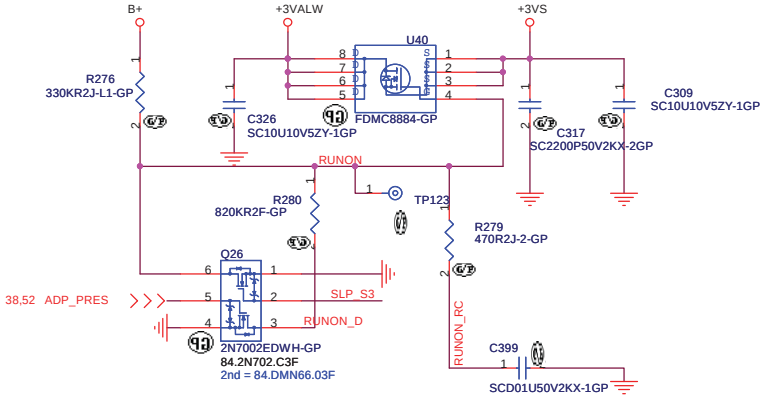

## +1.5V to +1.5VS Transfer



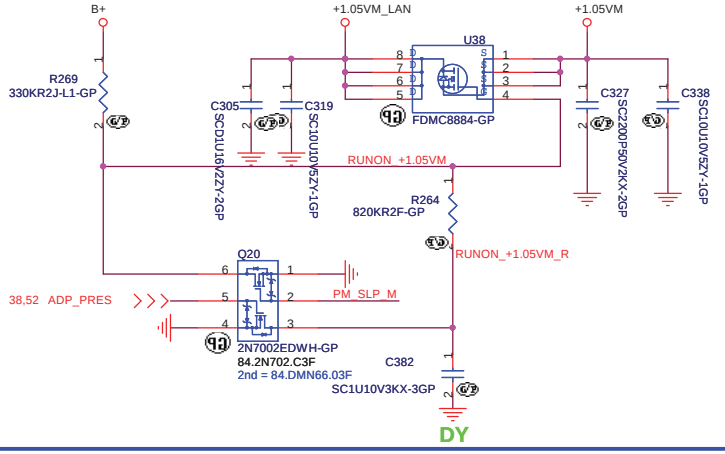

## Discharge circuit-2 fot V-M



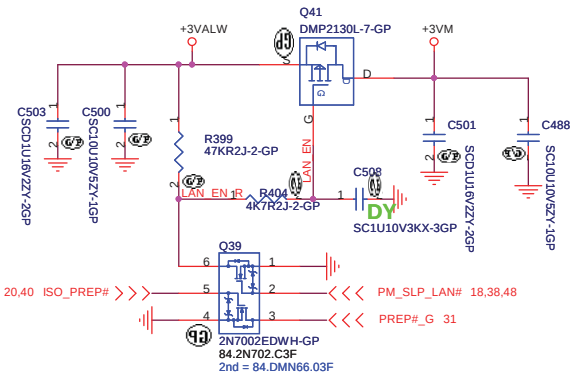

## +3VALW to +3VS Transfer



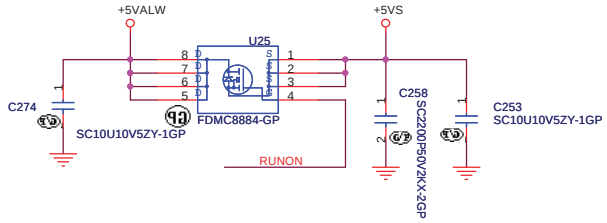

## +1.05VM_LAN to +1.05VM Transfer

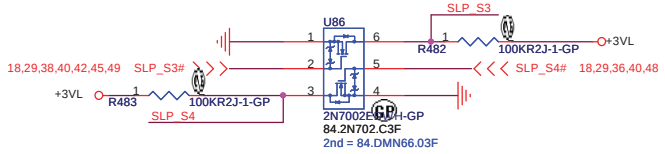


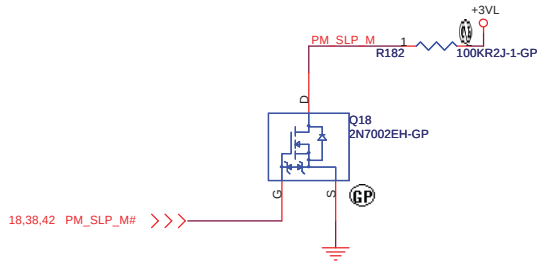

## +3VALW to +3VM Transfer



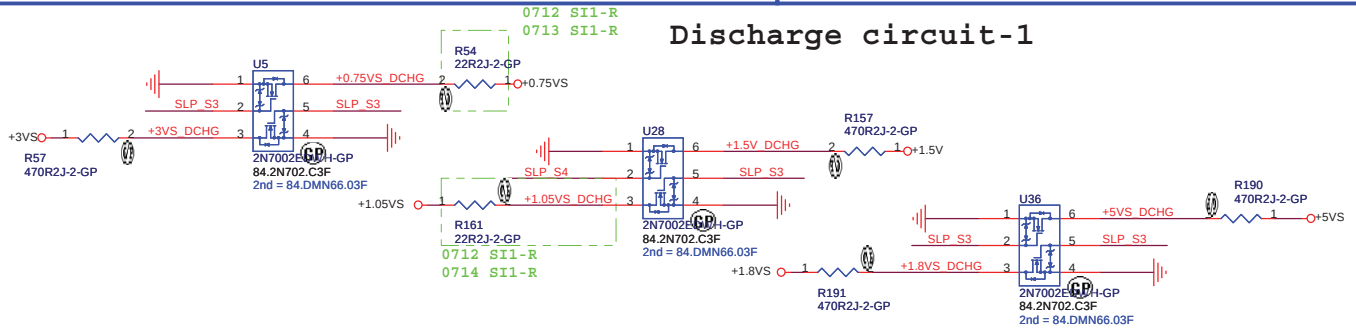

## +5VALW to +5VS Transfer

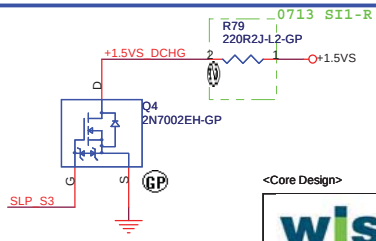



## Discharge circuit-1





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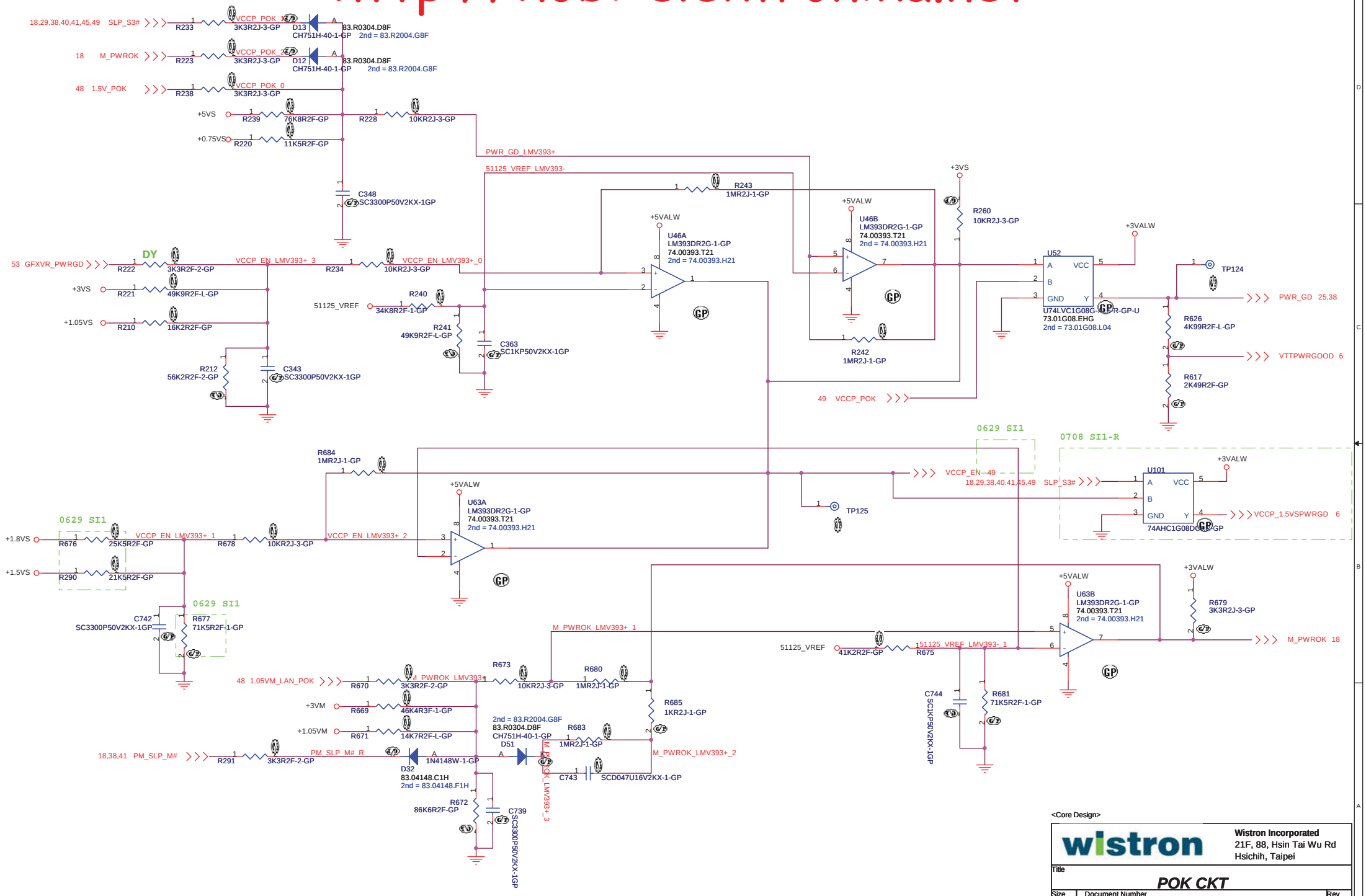


<Core Design>

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Title: POK CKT

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|---|---|---|
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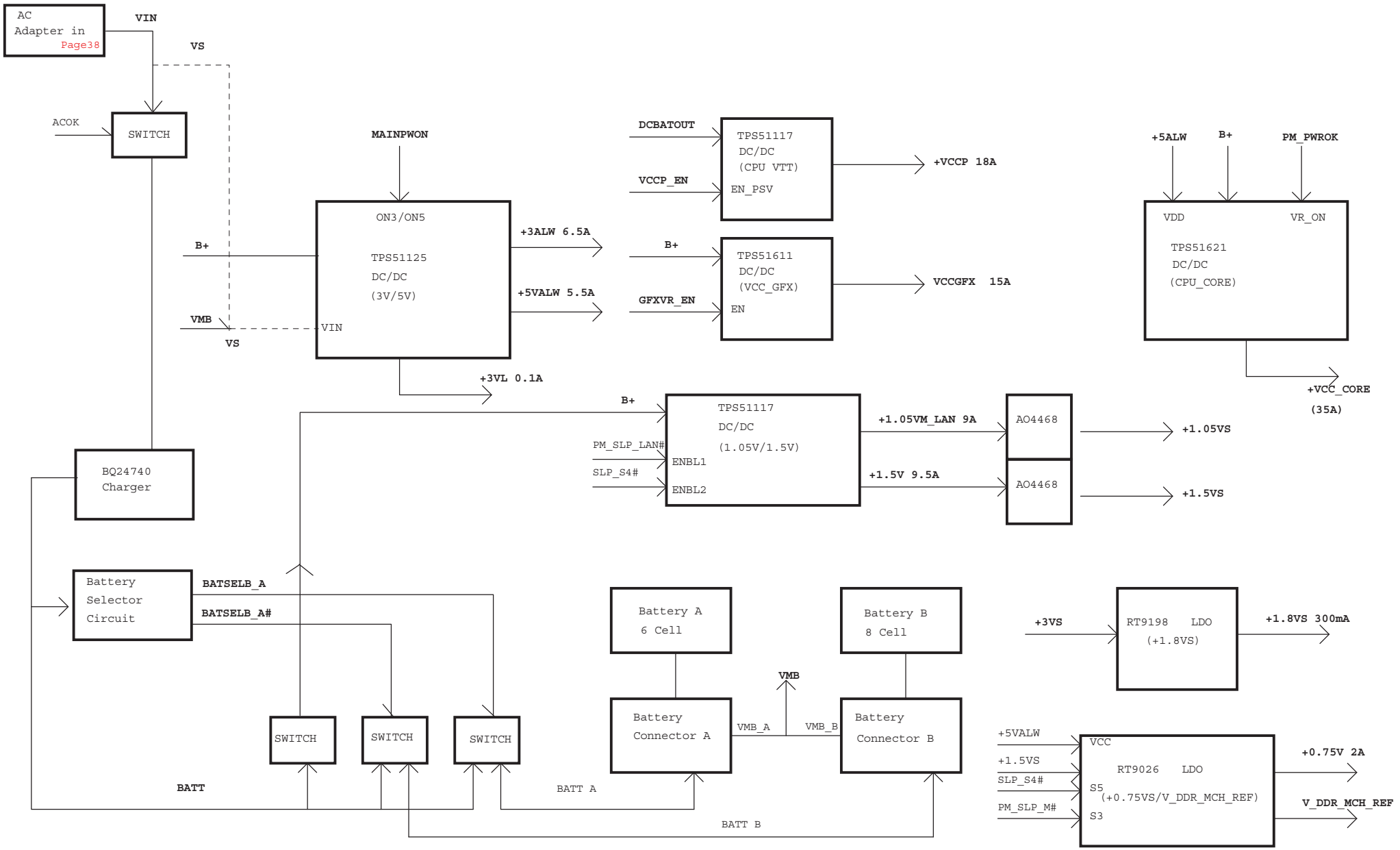


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Title: Power Block Diagram

| Size | Document Number | Rev |
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# Adaptor in to generate DCBATOUT

Current Rating 6 A

0825_SI2

ADPIN — AFTP81
LIMIT_SIGNAL — AFTP82
AFTP83

DCIN1
SKT-JACK-329-GP
22.10037.I11
2nd = 22.10037.I71

LIMIT_SIGNAL
EC22 SC1KP50V2KX-1GP
D3 P6SMBJ24A-H-GP
C443 SCD1U25V3KX-GP
C27 SC1KP50V2KX-1GP
C33 SC100P50V2JN-3GP
C30 SC1KP50V2KX-1GP
ADPIN
L14 BLM21PG220SN1DGP
68.00084.831
2nd = 68.00216.081
R33 15KR2J-1-GP
VIN
TP126

D25 BAV99DGP-GP
83.BAV99.AAE
2nd = 83.BAV99.BAE
AB1A_DATA
AB1A_CLK
+3VLO

THM_MAIN#
BAV99T-GP
83.BAV99.I11
2nd = 83.00099.Q11
C391 SCD1U16V2ZY-2GP
+3VL

D35
THM_MBAY#
BAV99T-GP
83.BAV99.I11
2nd = 83.00099.Q11
C433 SCD1U16V2ZY-2GP

D34 BAV99DGP-GP
83.BAV99.AAE
2nd = 83.BAV99.BAE
AB1B_DATA
AB1B_CLK

## MAIN BATTERY CONNECTOR

Current Rating 6 A

VMB_A
L13 BLM21PG220SN1DGP
68.00084.831
2nd = 68.00216.081
C735 SC1KP50V2KX-1GP
BATT_A 0825_SI2
TP174
C418 SC1KP50V2KX-1GP
EC35 SCD1U25V2KX-GP

BAT1
SYN-CON6-GP-U
20.81232.006
2nd = 20.81265.006

AB1A_DATA_C
AB1A_CLK_C
FBK_A_C
THM_MAIN#_C

R663 100R2J-2-GP — AB1A_DATA 38
R666 100R2J-2-GP — AB1A_CLK 38
R668 1KR2J-1-GP — AFTP64

C734 SC100P50V2JN-3GP
C738 SC100P50V2JN-3GP
C737 SC100P50V2JN-3GP

Route the GND of Caps all to BAT1 GND.

VMB_A — AFTP63
AB1A_DATA_C — AFTP62
AB1A_CLK_C — AFTP61

THM_MAIN#_C — AFTP60, AFTP65

R273 210KR2F-GP
+3VL
THM_MAIN# 38

R312 200R2J-L1-GP
BAT_AM_0 — BAT_AM_1
Q56 PDTA124EU-GP
84.00124.Y1K
2nd = 84.00124.T1K
38 AMBER_BATLED#

PIN3 Amber
PIN4 Aqua White

LED5 LED-YW-1-GP
83.18225.A70
BAT_AM_1
BATGRN_1

Layout Note:
Place R663, R666, R668,
C734, C738, and C737 close to BAT1.

## BAY BATTERY CONNECTOR

Current Rating 6 A

VMB_B
L31 BLM21PG220SN1DGP
68.00084.831
2nd = 68.00216.081
EC36 SCD1U25V2KX-GP
C746 SC1KP50V2KX-1GP
BATT_B 0825_SI2
TP175
C751 SCD01U50V2KX-1GP

BAT2
SYN-CON4-GP
20.81259.006
2nd = 20.81267.006

AB1B_DATA_C
AB1B_CLK_C
FBK_B_C
THM_MBAY#_C

R715 100R2J-2-GP — AB1B_DATA 38
R716 100R2J-2-GP — AB1B_CLK 38
R717 1KR2J-1-GP — AFTP68

C749 SC100P50V2JN-3GP
C748 SC100P50V2JN-3GP
C747 SC100P50V2JN-3GP

Route the GND of Caps all to BAT2 GND.

VMB_B — AFTP71
AB1B_DATA_C — AFTP70
AB1B_CLK_C — AFTP69

THM_MBAY#_C — AFTP67, AFTP66

R713 210KR2F-GP
+3VL
THM_MBAY# 38

R301 100R2J-2-GP
BATGRN_0 — BATGRN_1
Q31 PDTA124EU-GP
84.00124.Y1K
2nd = 84.00124.T1K
16,38 AQUAWHITE_BATLED#

Layout Note:
Place R715, R716, R717,
C749, C748, and C747 close to BAT2.

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Title: DC & BATTERT CONN.
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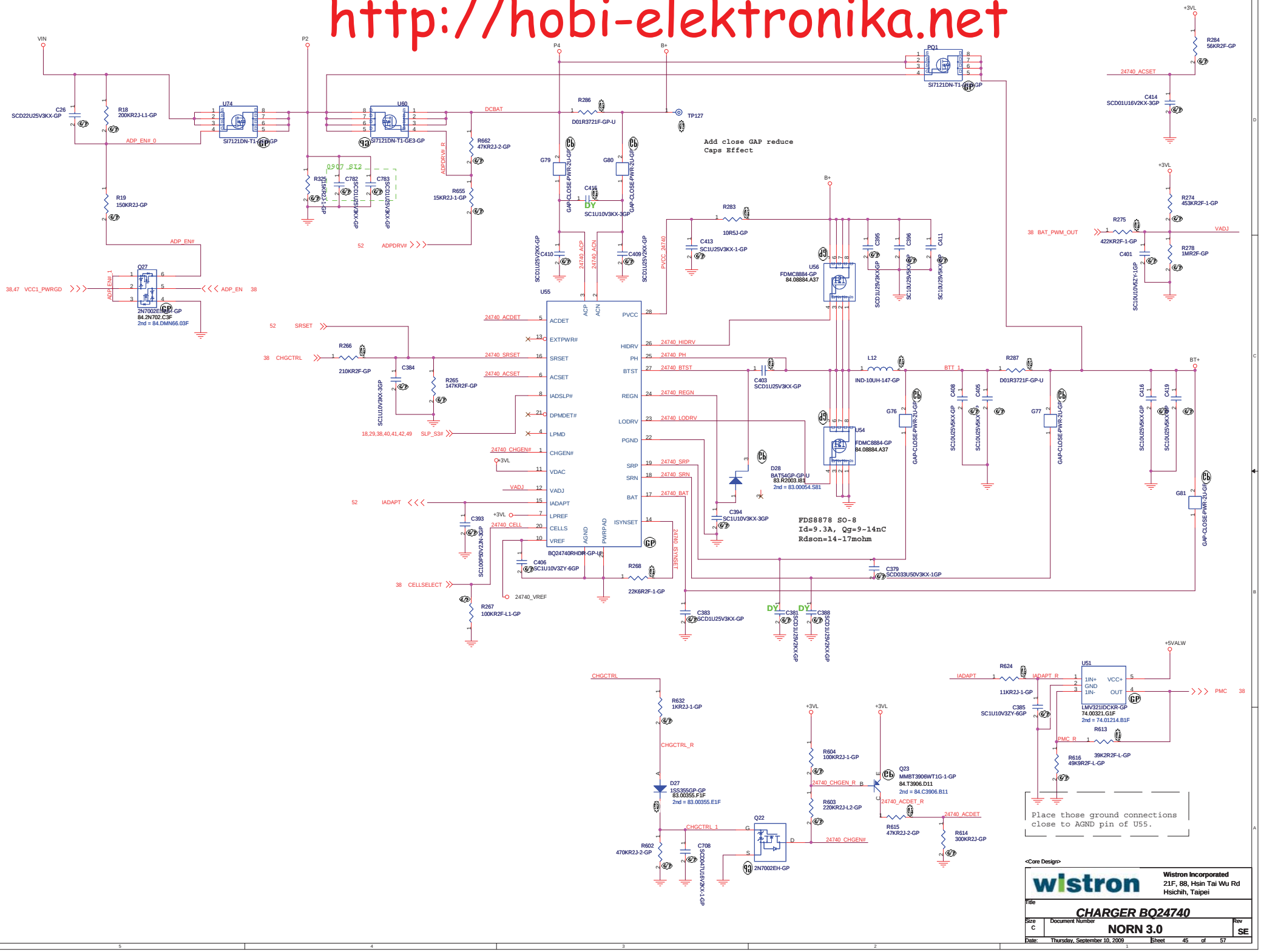


<Core Design>

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Title: CHARGER BQ24740

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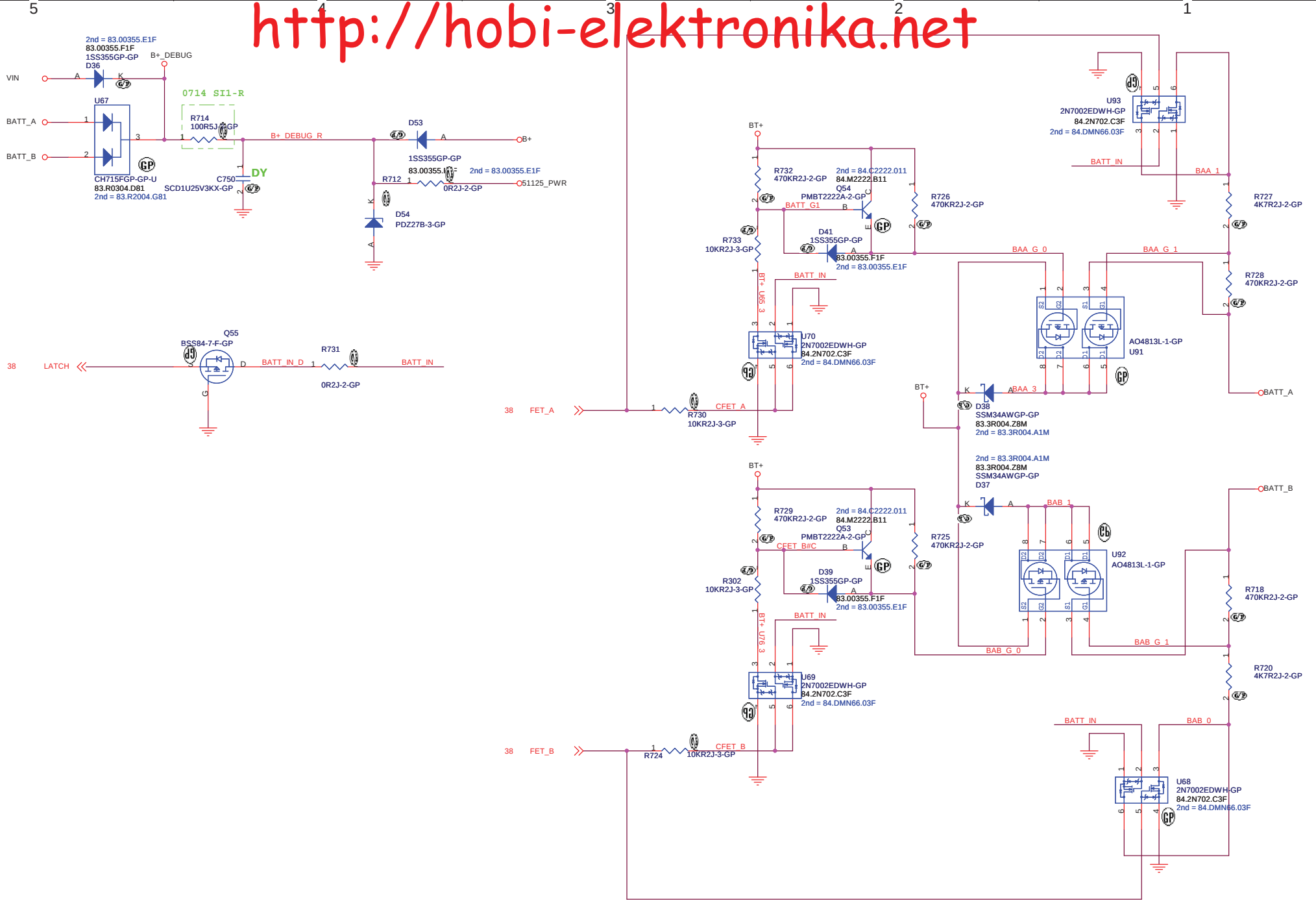


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|---|---|---|
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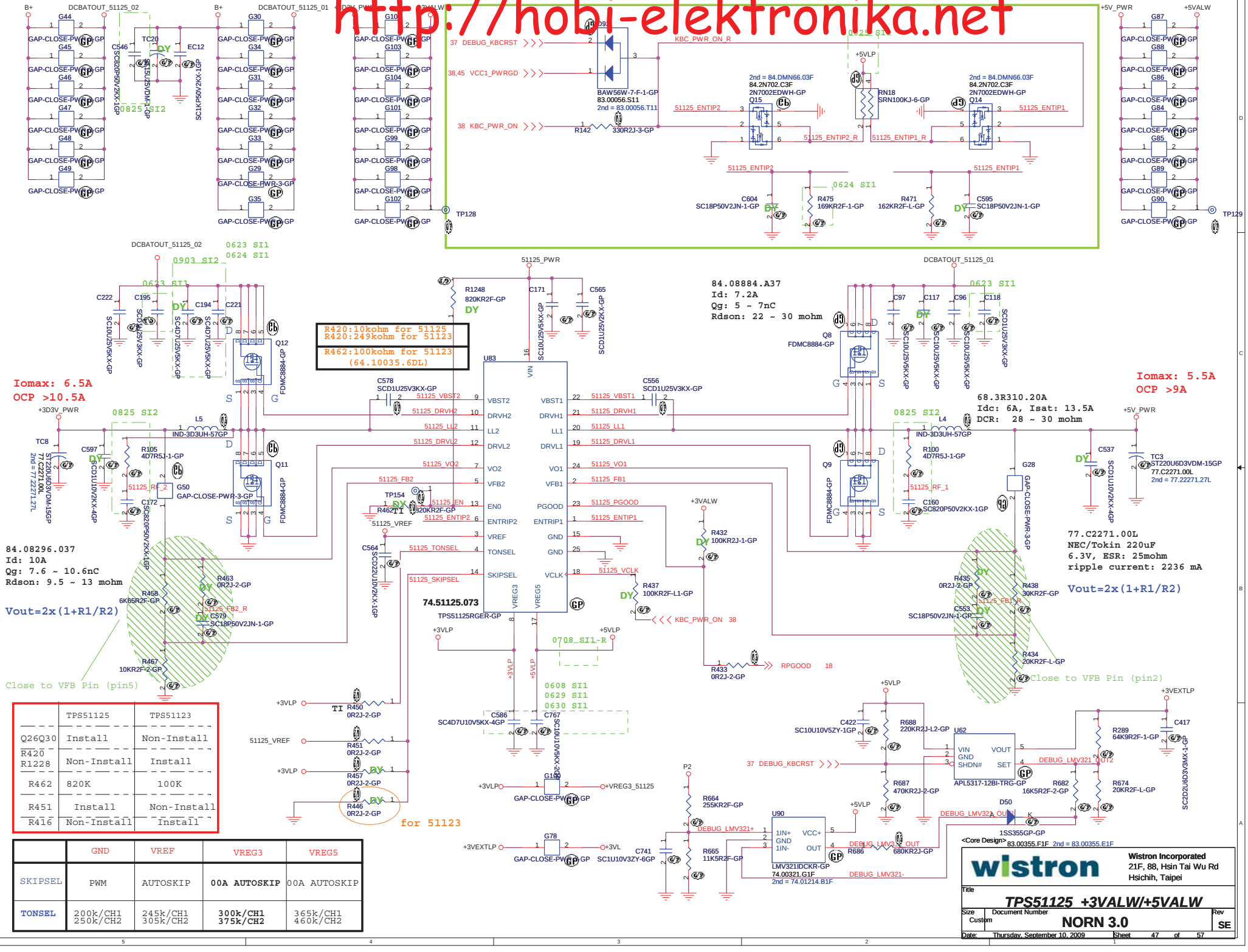


| | TPS51125 | TPS51123 |
|---|---|---|
| Q26Q30 | Install | Non-Install |
| R420 / R1228 | Non-Install | Install |
| R462 | 820K | 100K |
| R451 / R416 | Install / Non-Install | Non-Install / Install |

| | GND | VREF | VREG3 | VREG5 |
|---|---|---|---|---|
| SKIPSEL | PWM | AUTOSKIP | **00A AUTOSKIP** | 00A AUTOSKIP |
| TONSEL | 200k/CH1<br>250k/CH2 | 245k/CH1<br>305k/CH2 | **300k/CH1**<br>**375k/CH2** | 365k/CH1<br>460k/CH2 |

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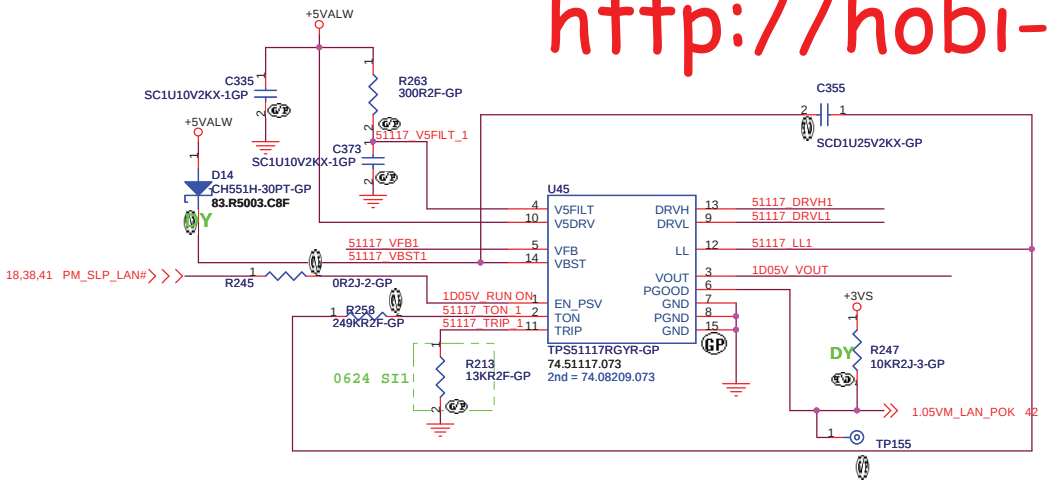
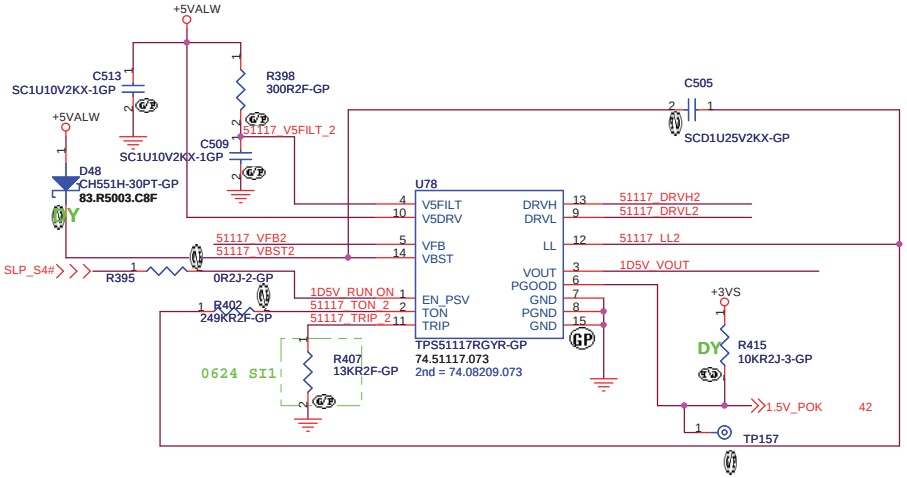
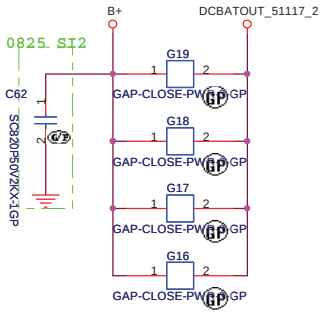
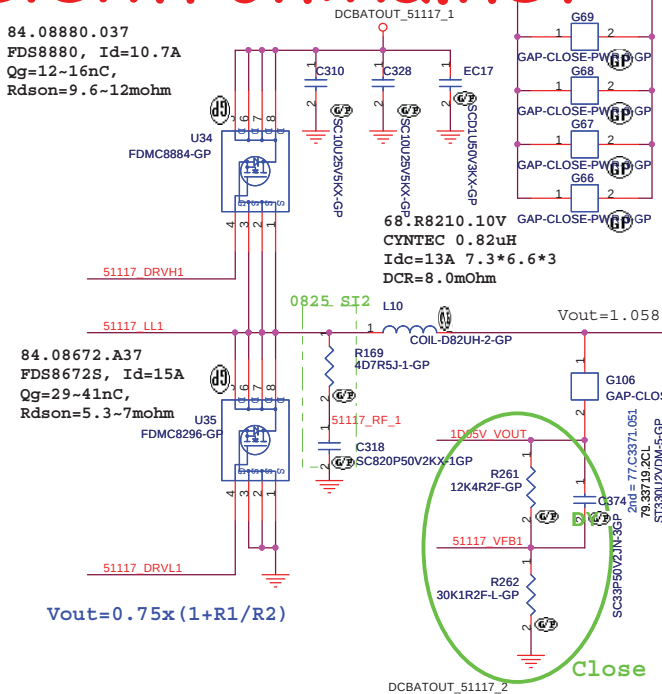
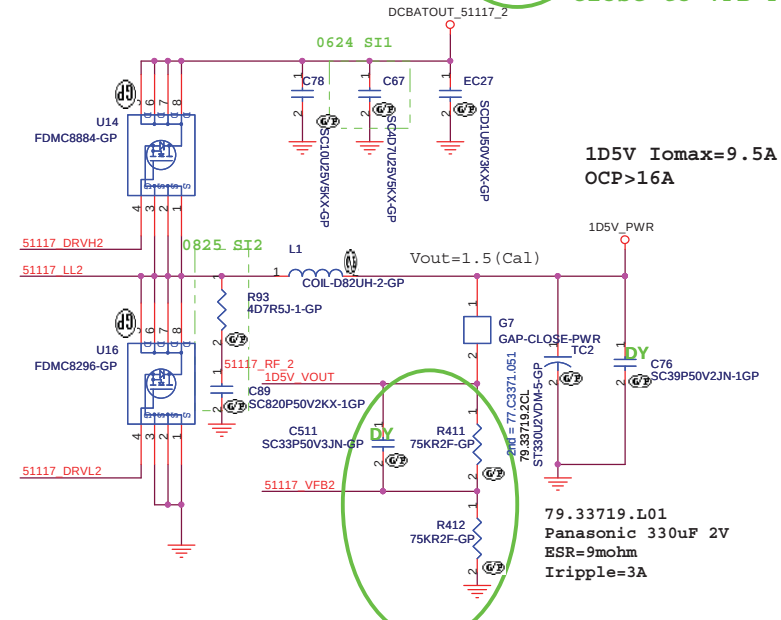



| | GND | OPEN | V5FILT |
|---|---|---|---|
| TONSEL | 240k/CH1<br>300k/CH2 | 300k/CH1<br>360k/CH2 | 360k/CH1<br>420k/CH2 |





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Title: TPS51117_+1.05VM_LAN / +1.5V

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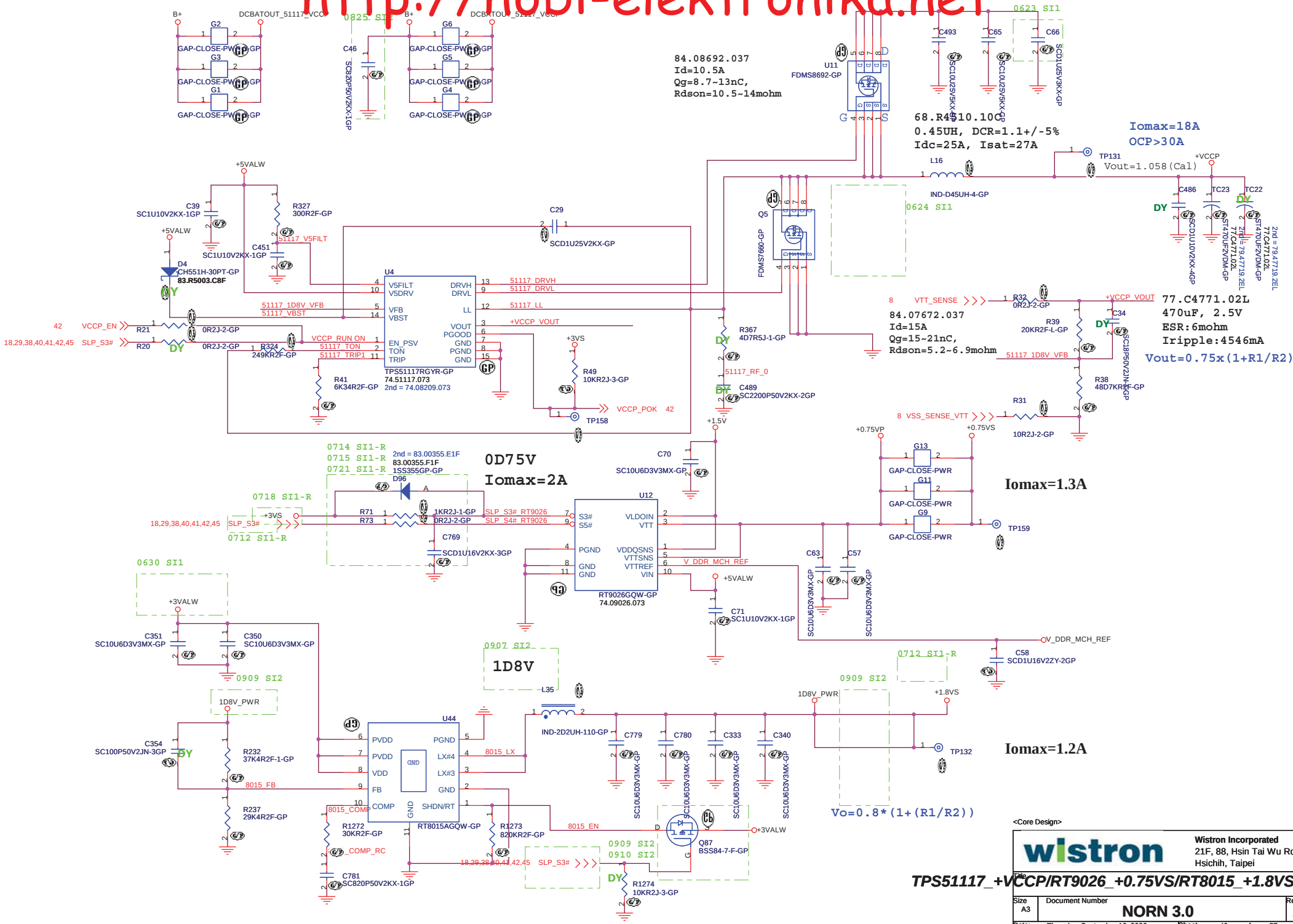

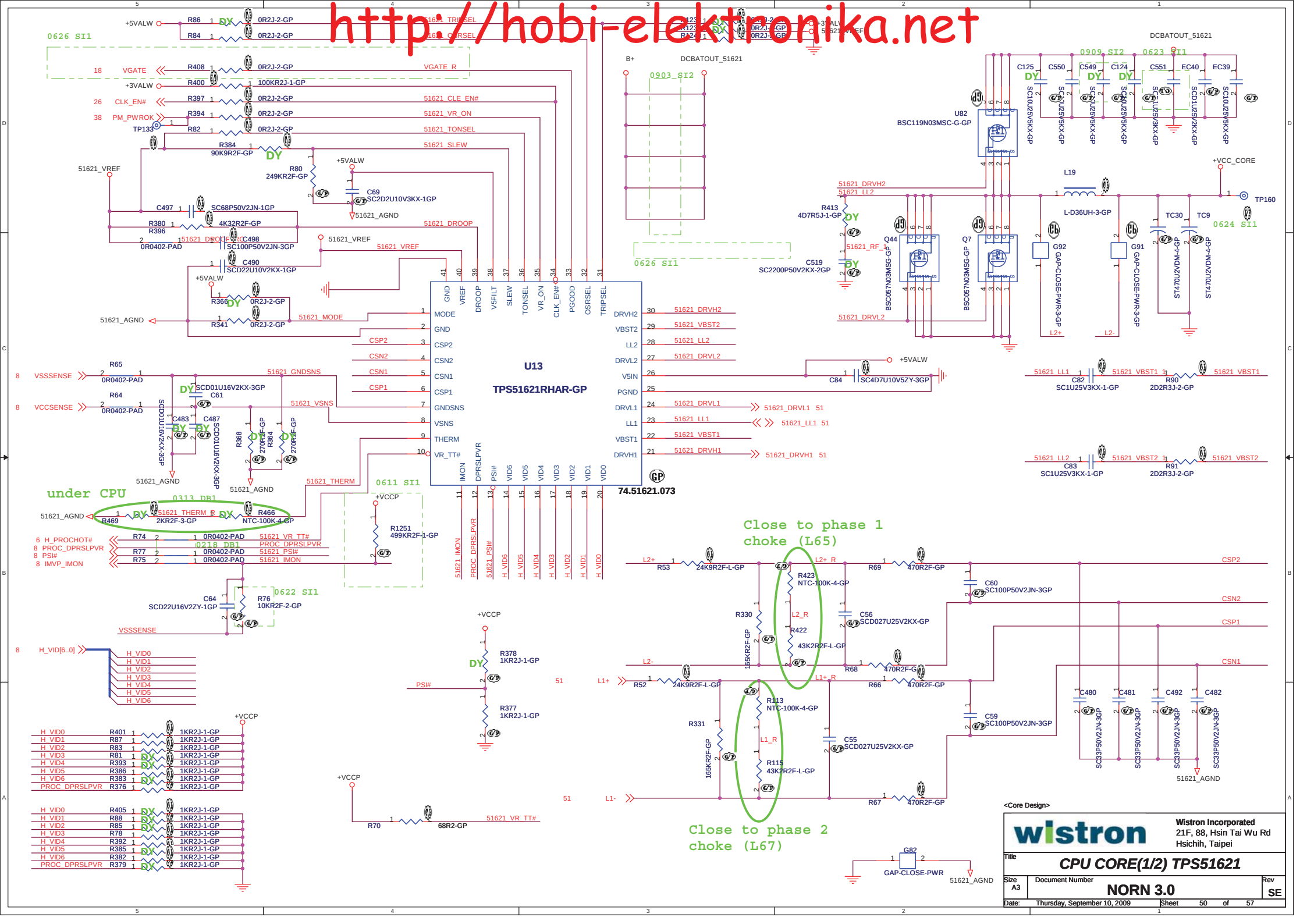

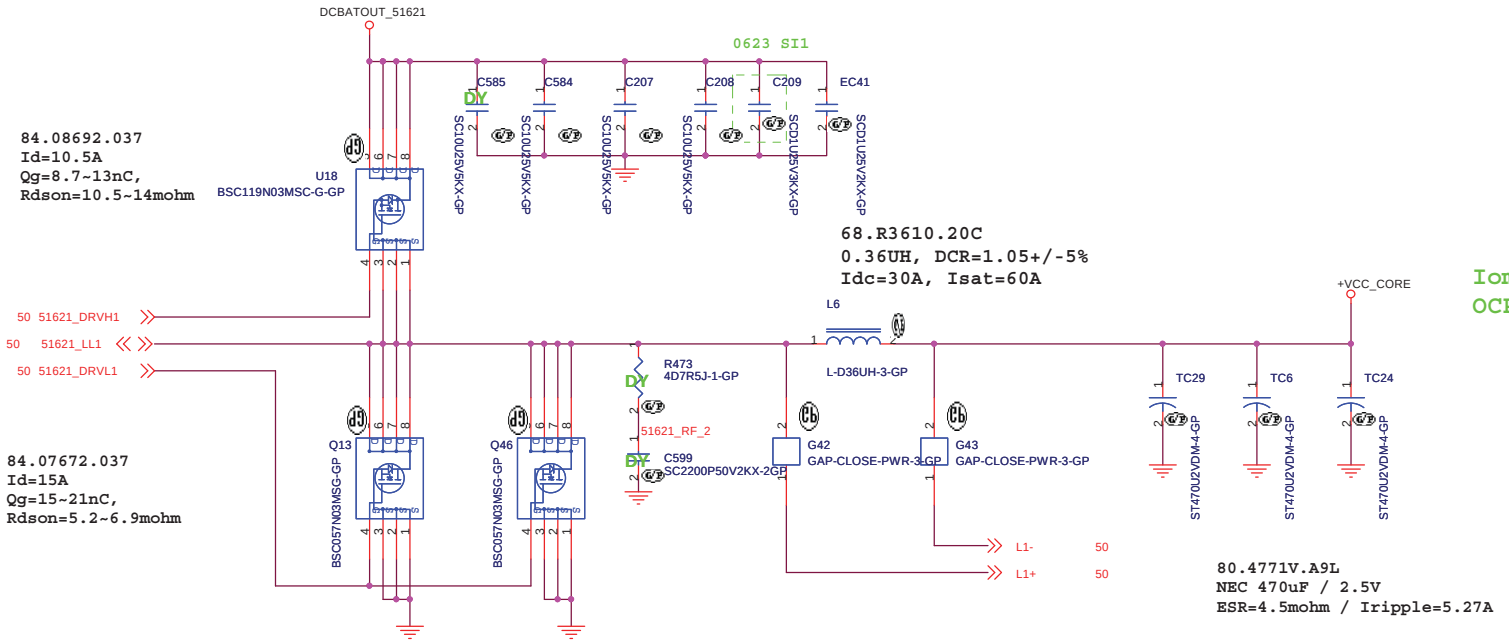


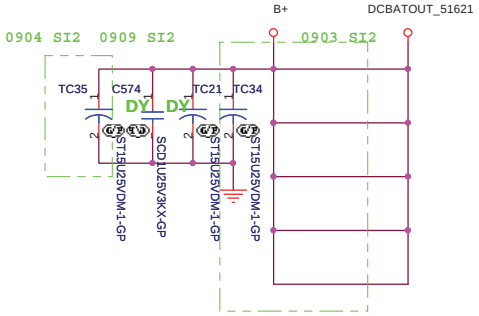

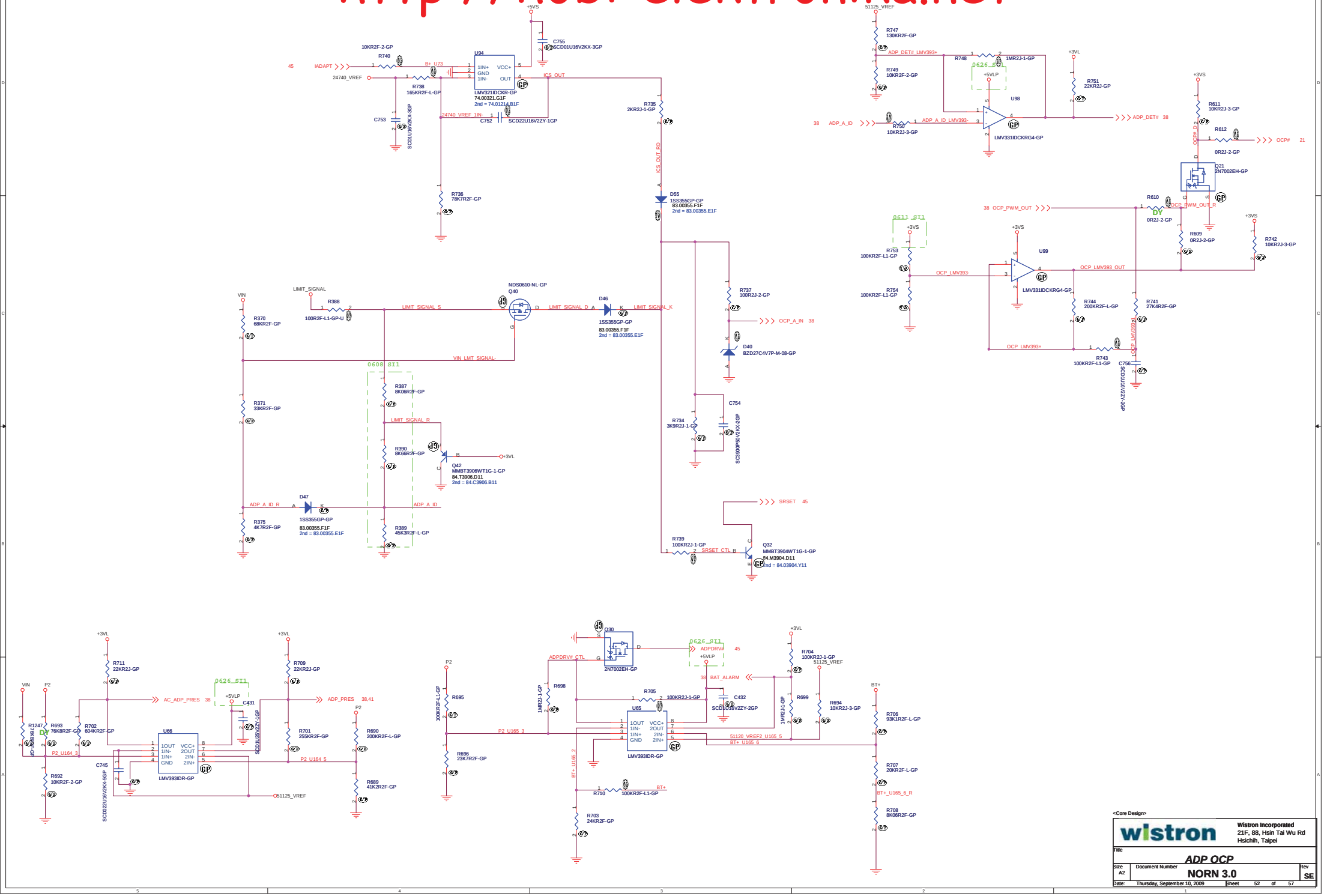


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Title: ADP OCP

Size: A2 | Document Number: NORN 3.0 | Rev: SE

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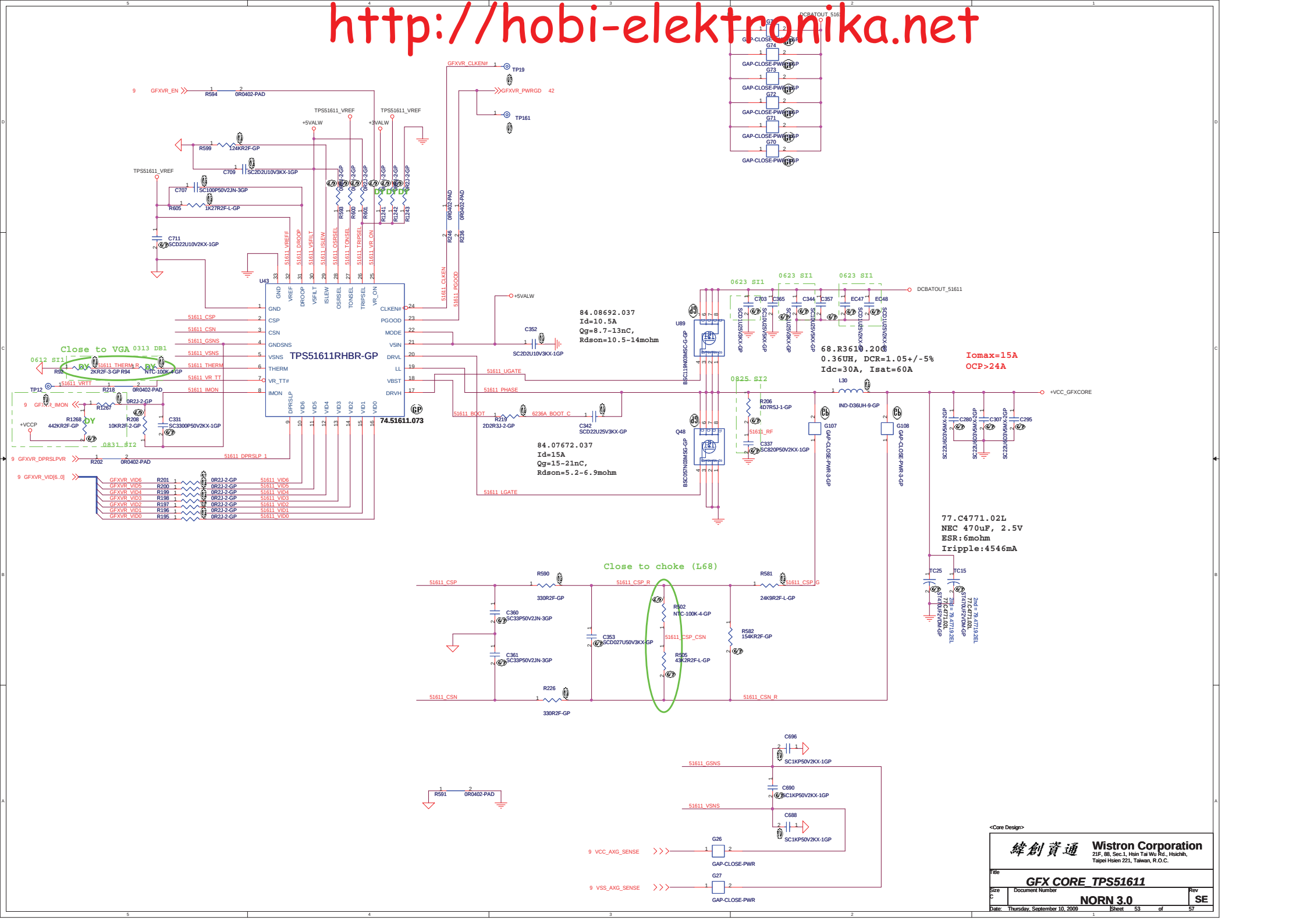

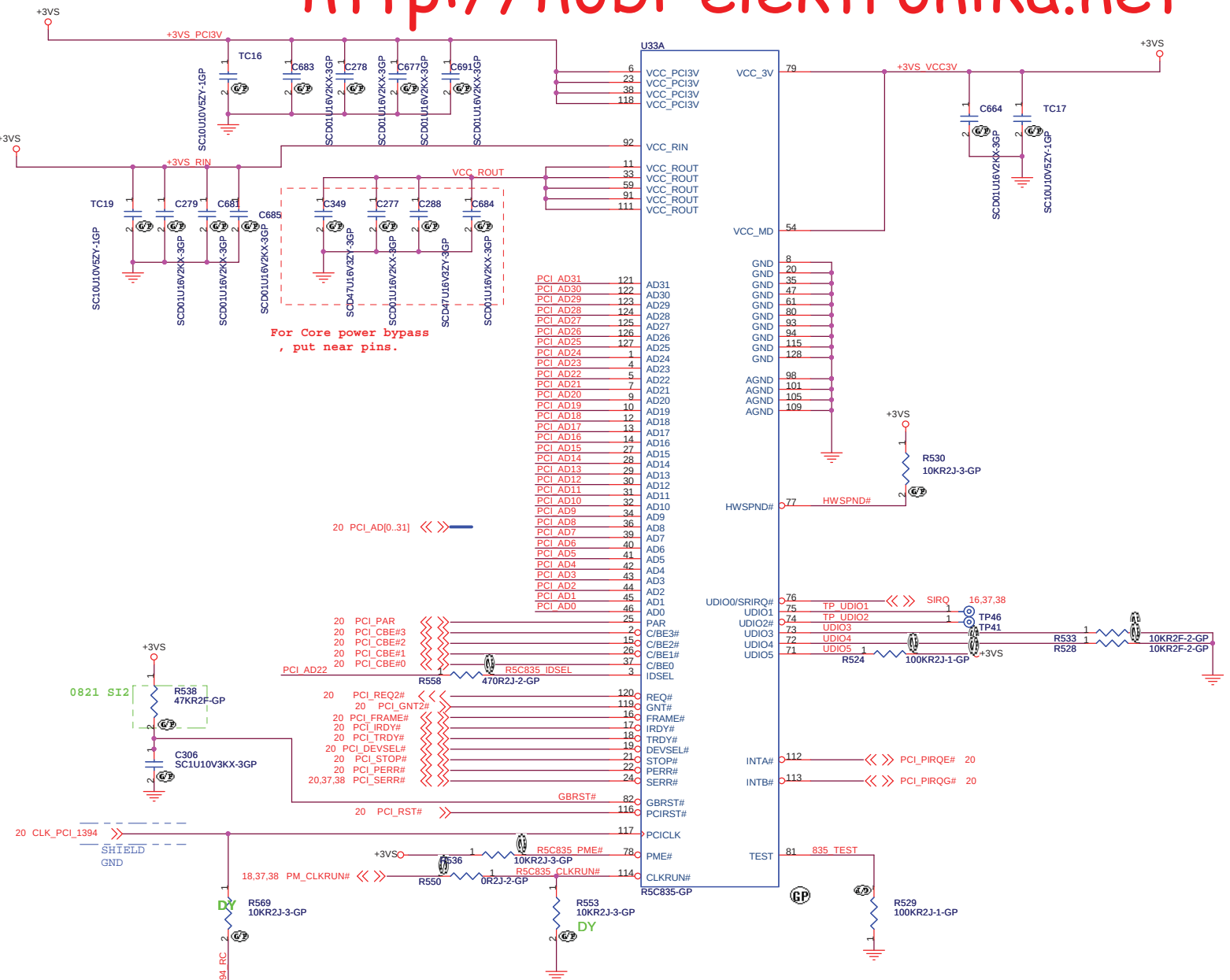

Place C345 and C346, and X3 as close to R5C835 as possible.

GUARD GND

C345 SC15P50V2JN-2-GP 1394_XI

X3 should be 50 ppm or better.

X3 X-24D576MHZ-62GP 82.30023.511 2nd = 82.30023.611 XTAL 24.576M 12P30PPM HCX-5FA 1394_XO

C346 SC15P50V2JN-2-GP

TP162

Place R576 and C693 as close to R5C835 as possible.

R576 10KR2F-2-GP RICHO_REXT

C693 SCD01U16V2KX-3GP RICHO_VREF

GUARD GND

+VCC_SC

C320 SC10U10V5ZY-1GP C672 SCD01U16V2KX-3GP

Layout notes :
external parts for VREF, REXT and FIL0 as close as possible to R5C835.

Layout Notes:

Make sure that the stubs to the test points(1394_XO) in the layout are as short as possible on the high speed signals.

U33B

R5C835-GP

AVCC_PHY3V AVCC_PHY3V AVCC_PHY3V

+3V_PH

L11 FCM1608KF-3-GP 69.00133.001 2nd = 68.00206.191

C362 SC10U10V5ZY-1GP C694 SC1KP50V2KX-1GP C347 SCD01U16V2KX-3GP

Layout note :
Place these Caps
Close to R5C835

TPBIAS0 R560 56R2F-1-GP R561 56R2F-1-GP C675 SCD01U16V2KX-3GP C674 SCD33U10V2ZY-GP

TPB0N TPB0P TPA0N TPA0P

R563 56R2F-1-GP R562 56R2F-1-GP

1394_TPB1_R C676 SC270P50V2JN-2GP R554 5K1R2F-2-GP

CLOSE TO CHIP R5C835

MDIO19 MDIO18 MDIO17 MDIO16 MDIO15 MDIO14 MDIO13 MDIO12 MDIO11 MDIO10 MDIO09 MDIO08 MDIO06 MDIO05 MDIO04 MDIO03 MDIO02 MDIO01 MDIO00 MDIO07

SD_DATA7 SD_DATA6 SD_DATA5 SD_DATA4 SD_DATA3 SD_DATA2 SD_DATA1 SD_DATA0 SD_CLK SD_CMD SD_EN SD_WP# SD_CD#

MDIO06 TP9

+5VSCEN# +3VSCEN# SCSENSE SC_CD# SC_DATA SC_CLK_R SC_RST

SCVCC5EN# SCVCC3EN# SCSENSE SCCD# SCIO SCCLK SCRST

SC_CLK 33R2J-2-GP R551 SHIELD GND

SD_CLK SHIELD GND

The shield GND is needed for SD_CLK(MDIO09).
Also, the wide-width (more than 0.02inch) trace for MDIO09 should be used.

Layout Note: Add guard GND around SD_CLK
Change +3VS_CARD to 40mils

Please ensure that TPA+/- and TPB+/- are routed the same wire length.

IEEE1 SKT-1394-4P-48-GP 62.10027.B31

TPB0- R723 0R2J-2-GP TPB0N
TPB0+ R722 0R2J-2-GP TPB0P
TPA0- R721 0R2J-2-GP TPA0N
TPA0+ R719 0R2J-2-GP TPA0P

Place C741 within 4mils of the card connector

+3VS_CARD

R598 10KR2J-3-GP C366 SC1U10V3ZY-6GP

U U5240D1T1U-GP-U 74.05240.D7F

+3VS C321 SCD1U16V2ZY-2GP SD_EN

For SD Card Power

Layout notes :
1394
GND
TPB0-
TPB0+
GND
TPA0-
TPA0+
GND

SD_DATA0_1 C682 SC22P50V2JN-4GP
SD_DATA1_1 C673 SC22P50V2JN-4GP
SD_DATA2_1 C718 SC22P50V2JN-4GP
SD_DATA3_1 C717 SC22P50V2JN-4GP
SD_DATA4_1 C715 SC22P50V2JN-4GP
SD_DATA5_1 C710 SC22P50V2JN-4GP
SD_DATA6_1 C697 SC22P50V2JN-4GP
SD_DATA7_1 C686 SC22P50V2JN-4GP

+3VS_CARD C359 SCD1U16V2ZY-2GP

SD_CD# D11 1SS355GP-GP 83.00355.F1F 2nd = 83.00355.E1F

SD_CLK need to 25mil

CARD1

VDD CLK CMD WP CD NP1 NP2 DAT0 DAT1 DAT2 DAT3 DAT4 DAT5 DAT6 DAT7 VSS1 VSS2 GND GND

SD_CLK_1 SD_CMD_1 SD_WP# SD_CD#_CARD

SD_DATA0_1 SD_DATA1_1 SD_DATA2_1 SD_DATA3_1 SD_DATA4_1 SD_DATA5_1 SD_DATA6_1 SD_DATA7_1

CARD-PUSH-15P-1-GP 20.I0107.011

SD_CLK_1 R578 22R2J-2-GP SD_CLK_1_RC C702 SC22P50V2JN-4GP

+3VS_CARD R592 150KR2J-GP

Place resistor close to CARD1

+3VS C651 SCD1U16V2ZY-2GP

+VCC_SC U30 G552A1TA1U-GP

VOUT VIN GND FLAG# ON/ON#

U204_3

R514 10KR2J-3-GP +3VS

+3VS_PHY R521 100KR2J-1-GP +3VSCEN#

RN22 SRN33J-7-GP

SD_DATA3 SD_DATA2 SD_DATA1 SD_DATA0 SD_DATA3_1 SD_DATA2_1 SD_DATA1_1 SD_DATA0_1

RN21 SRN33J-7-GP

SD_DATA7 SD_DATA6 SD_DATA5 SD_DATA4 SD_DATA7_1 SD_DATA6_1 SD_DATA5_1 SD_DATA4_1

RN20 SRN33J-5-GP-U

SD_CMD SD_CLK SD_CMD_1 SD_CLK_1

SCSENSE R155 10KR2J-3-GP

R152 15KR2J-1-GP R156 15KR2J-1-GP R158 15KR2J-1-GP D9 CH731UA-GP

SC_DATA SC_CLK SC_RST

C282 SC12P50V2JN-3GP C283 SC12P50V2JN-3GP C284 SC12P50V2JN-3GP

+VCC_SC C281 SCD1U16V2ZY-2GP

J9 SMART1 PTWO-CON10-4-GP 20.K0382.010 2nd = 20.K0465.010

SC_CD# SC_DATA SC_CLK SC_RST +VCC_SC

AFTP46 AFTP47 AFTP44 AFTP42 AFTP45 AFTP84

0825 SI2

+5VS C642 SCD1U16V2ZY-2GP

+VCC_SC U27 G552A1TA1U-GP

VOUT VIN GND FLAG# ON/ON#

U205_3

R508 10KR2J-3-GP +3VS

+3VS_PHY R509 100KR2J-1-GP +5VSCEN#

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: R5C835/IEEE1394/SD/Smart(2/2)

Size: Custom | Document Number: NORN 3.0 | Rev: SE

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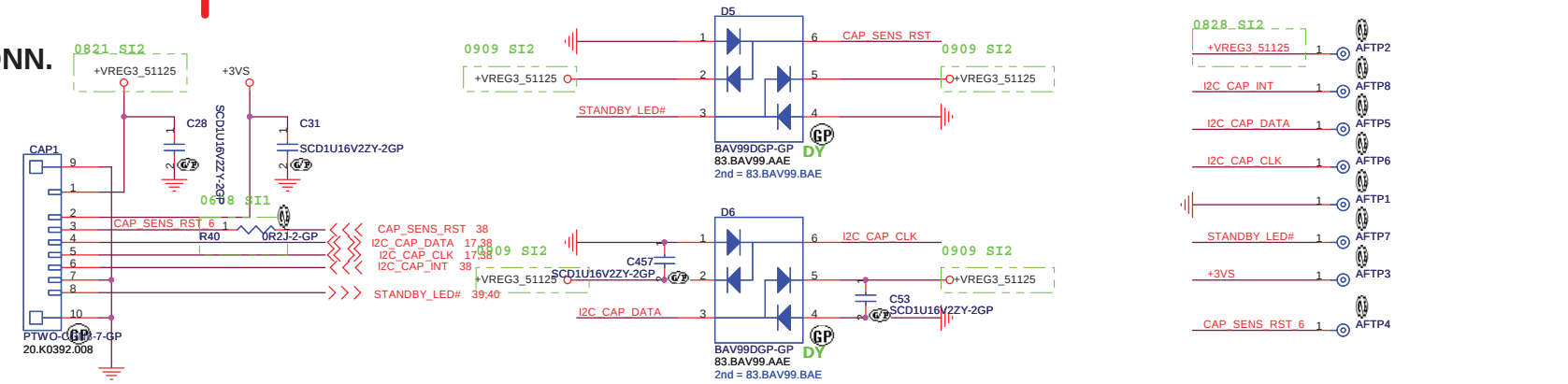
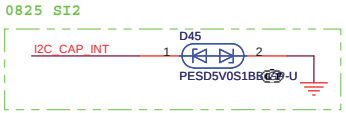
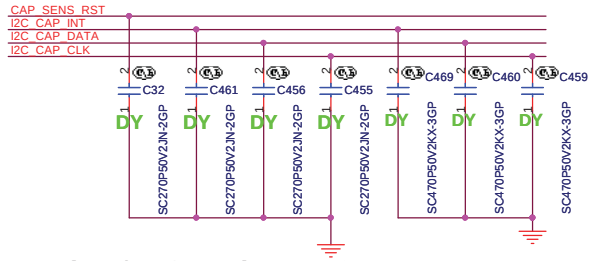
# CAP BD CONN.




Vol up , Vol down , Mute ,Presentation




Place these 4 Caps close to CAP1.

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Hsichih, Taipei

Title: CAP CONN.

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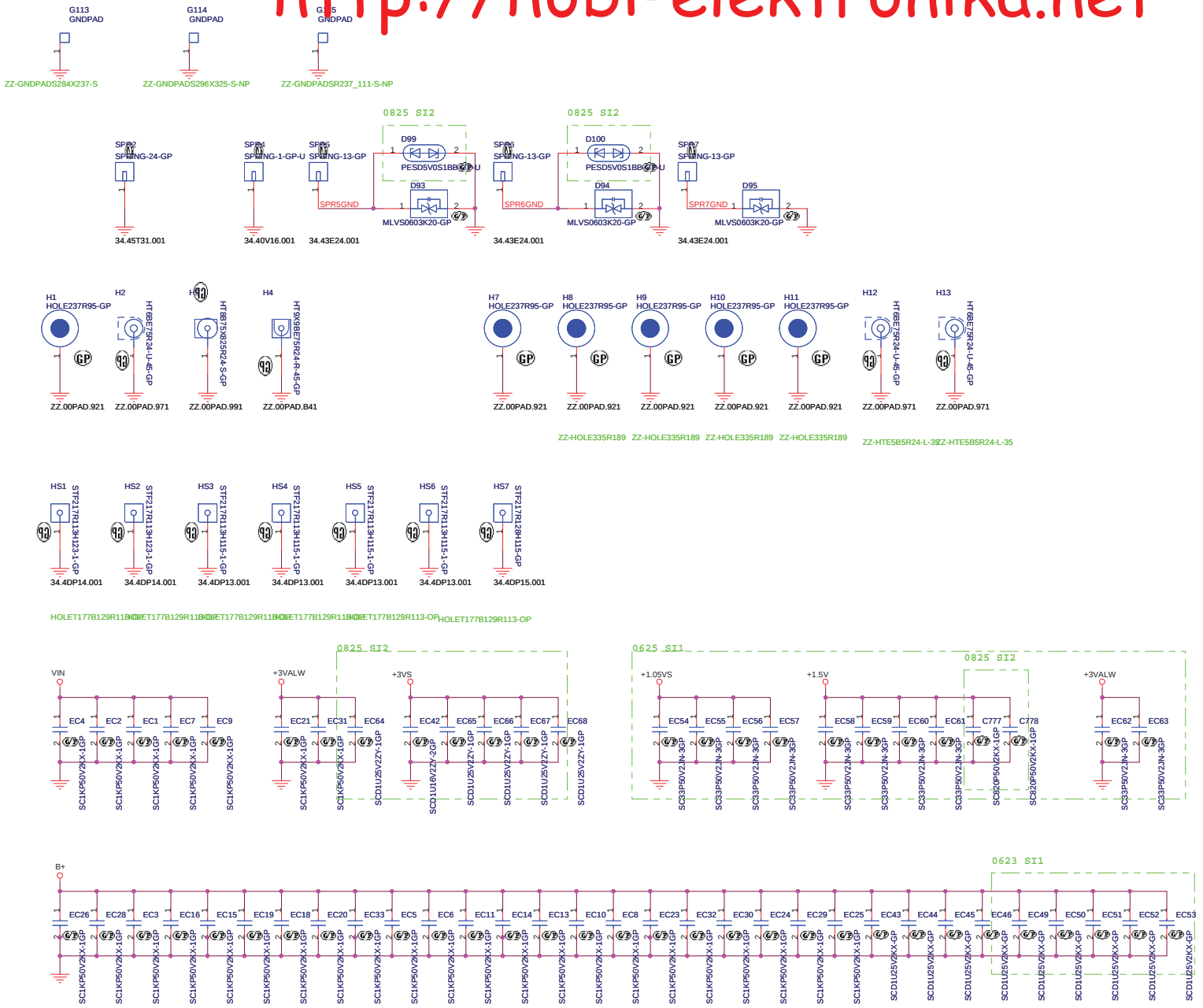


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Hsichih, Taipei

Title: UNUSED PARTS/EMI Capacitors

| Size | Document Number | Rev |
|---|---|---|
| Custom | NORN 3.0 | SE |

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