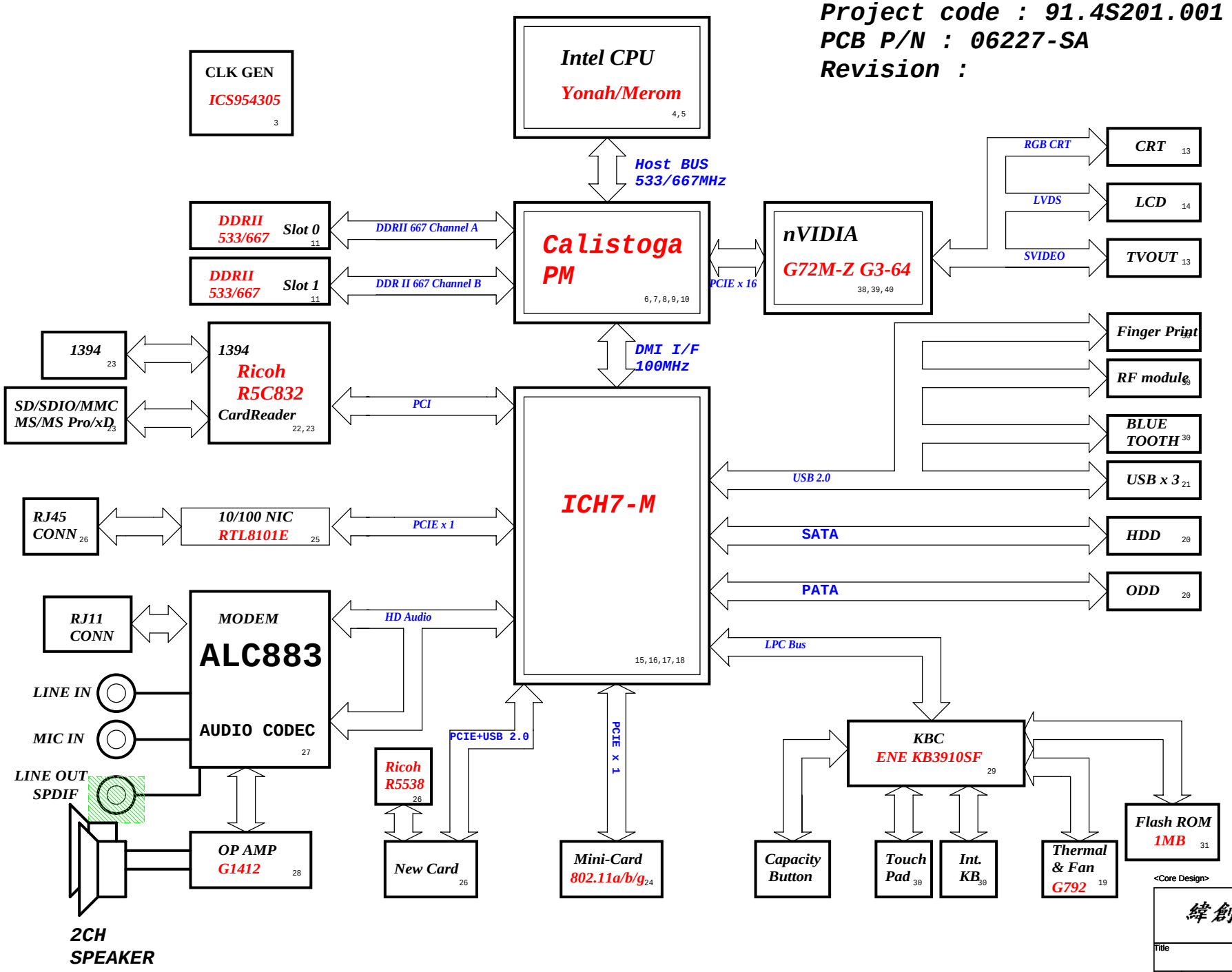
MB3 Block Diagram

Project code : 91.4S201.001
PCB P/N : 06227-SA
Revision :



SYSTEM DC/DC
TPS51120

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC
MAX8743

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

MAXIM CHARGER
MAX8725

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC
MAX8736ETL

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4
L7: GND
L8: Signal 5

<Core Design>

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Title: Block Diagram

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Date: Thursday, August 17, 2006 Sheet 1 of 44

Calistoga Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6		0=Moby Dick 1=Calistoga
CFG7	CPU Strap	0 = Reserved **1 =Mobile CPU(Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	Reserved	
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable **1 = Normal Operation (Default)**
CFG18	VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

ICS954305 Spread Spectrum Select

page 3

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.5
0	0	0	1	-1.0
0	0	1	0	-1.5
0	0	1	1	-2.0
0	1	0	0	-0.75
0	1	0	1	-1.25
0	1	1	0	-1.75
0	1	1	1	-2.25
1	0	0	0	+/-0.25
1	0	0	1	+/-0.5
1	0	1	0	+/-0.75
1	0	1	1	+/-1.0
1	1	0	0	+/-0.25
1	1	0	1	+/-0.5
1	1	1	0	+/-0.75
1	1	1	1	+/-1.0

PCI Routing

	IDSEL	IRQ	REQ/GNT
R5C832	25		0

ICH7M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

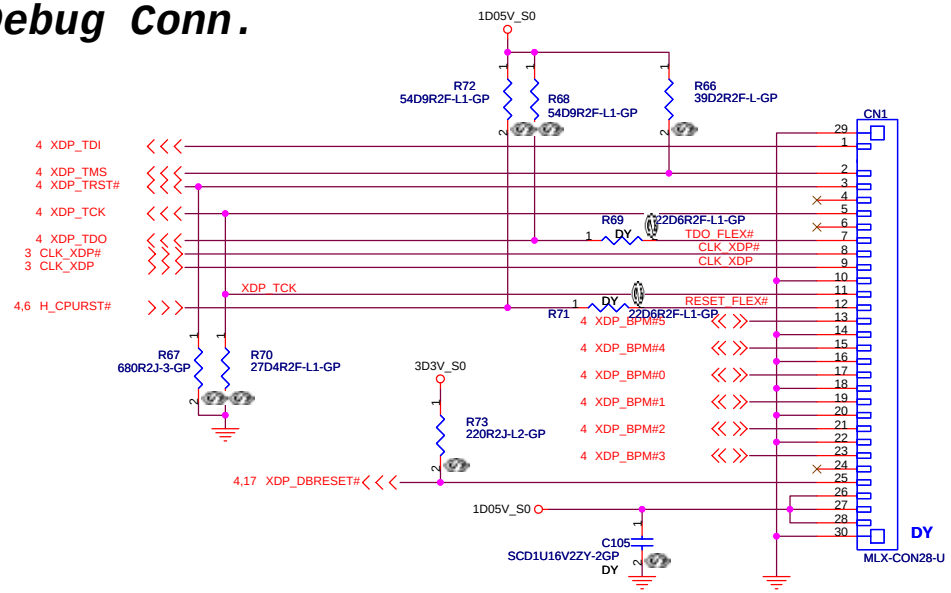
ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

History

U19---->71.945PM.B0U
U27---->71.ICH7M.C0U
CHECK NEW CARD p/n for BOM

ITP Debug Conn.



<Core Design>

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Title		
	ITP	
Size A3	Document Number MB3	Rev SA
Date: Thursday, August 24, 2006	Sheet 2 of 44	

IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z

H/L : CPU_ITP/SRC10

H/L: 27MHz/96MHz

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

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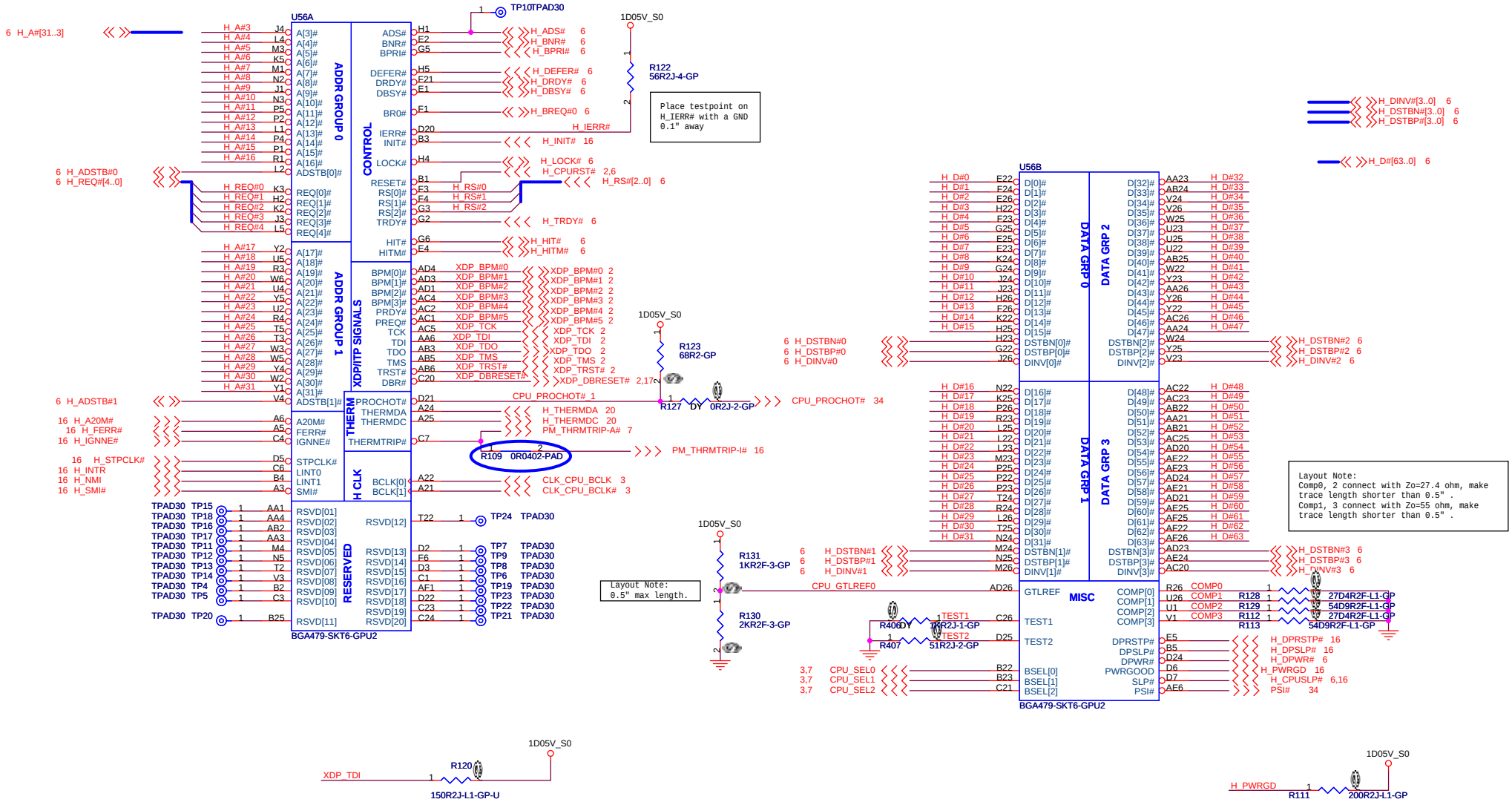
Title: Clock Generator

Size: A3 | Document Number: MB3 | Rev: SA

Date: Thursday, August 24, 2006 | Sheet 3 of 44



<Core Design>

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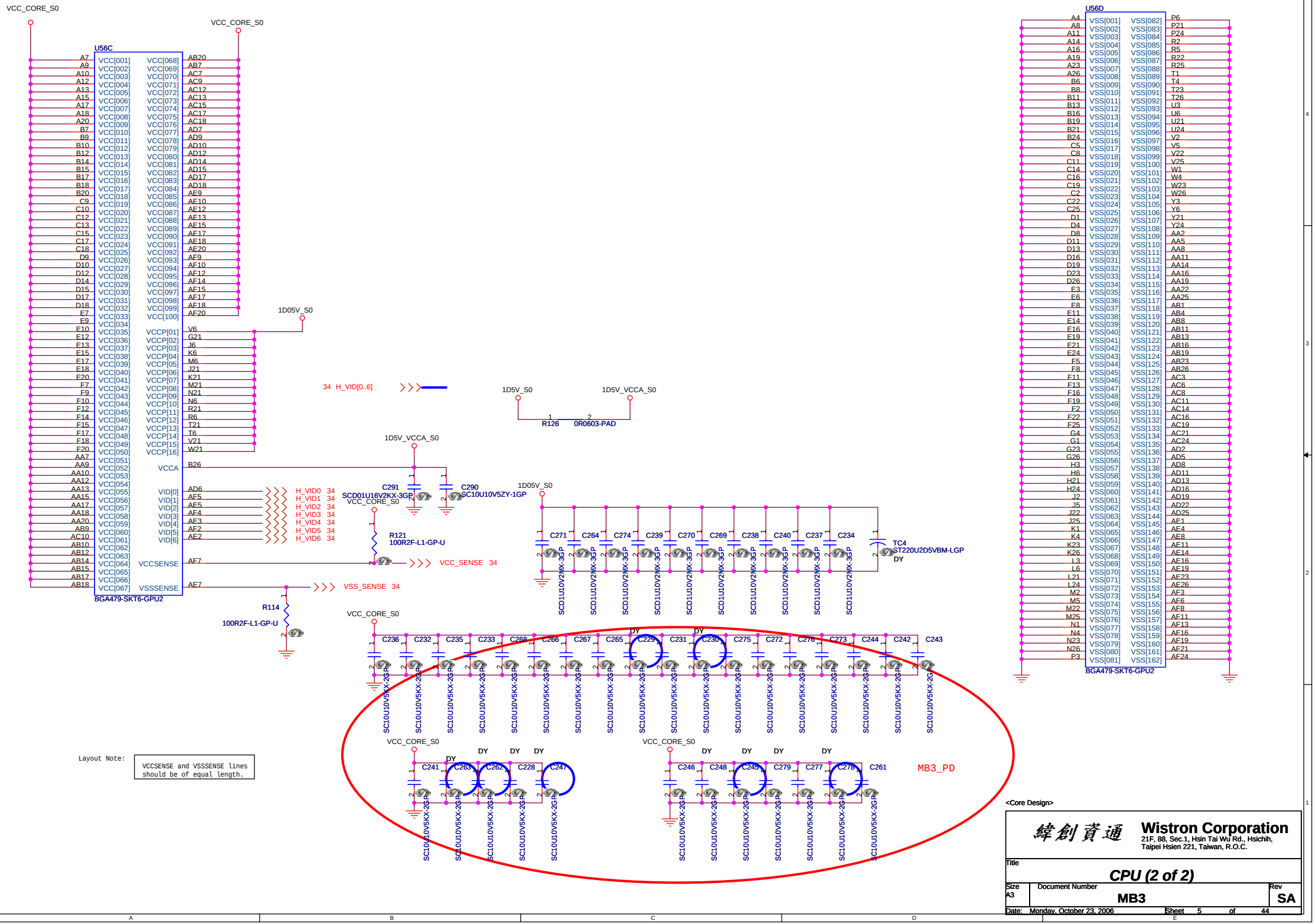
Title: CPU (1 of 2)

Size: A3 | Document Number: MB3 | Rev: SA

Date: Thursday, August 24, 2006 | Sheet 4 of 44



Layout Note:

VCCSENSE and VSSSENSE lines should be of equal length.

<Core Design>

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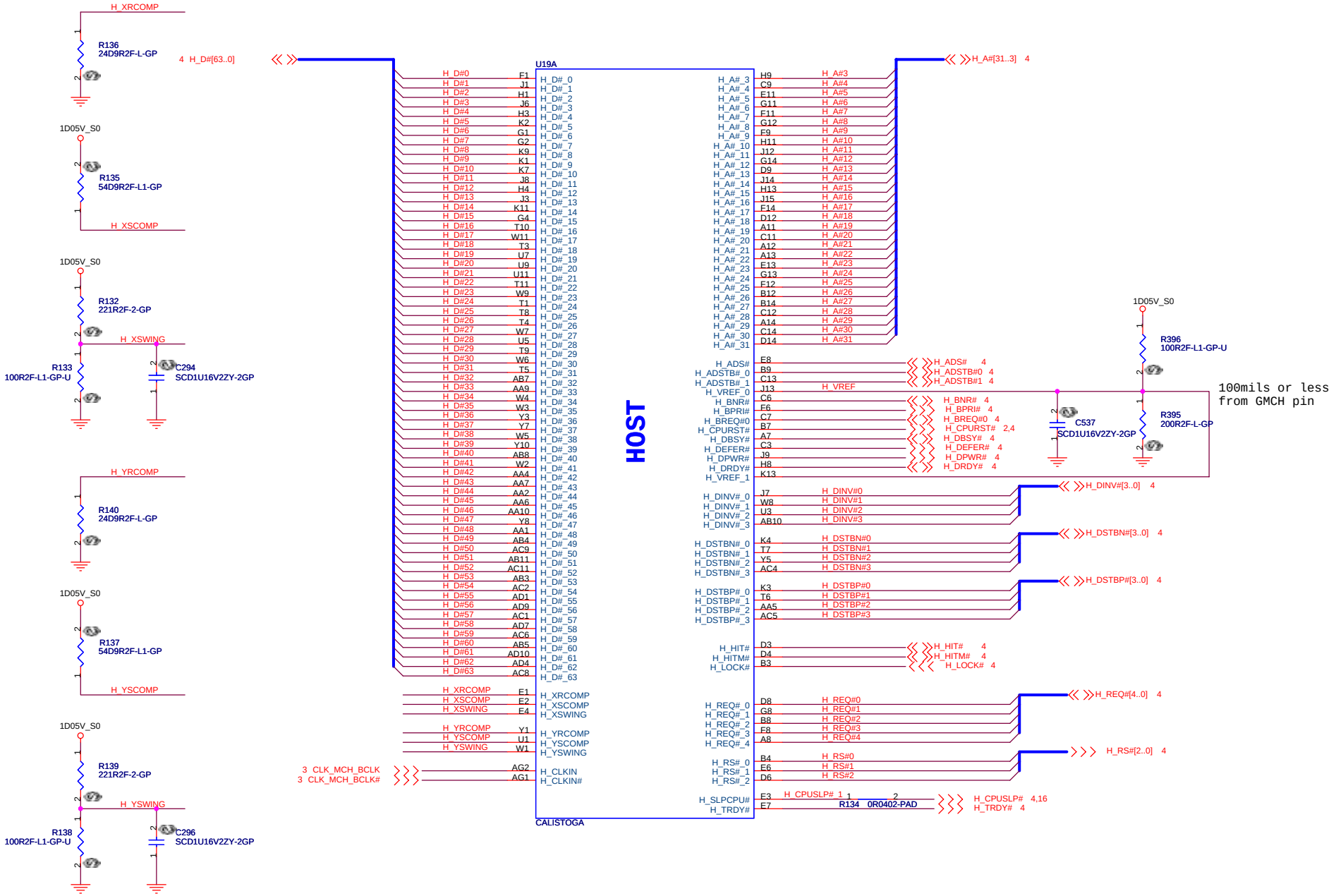
Title: CPU (2 of 2)

Size: A3 | Document Number: MB3 | Rev: SA

Date: Monday, October 23, 2006 | Sheet 5 of 44



Place them near to the chip

<Core Design>

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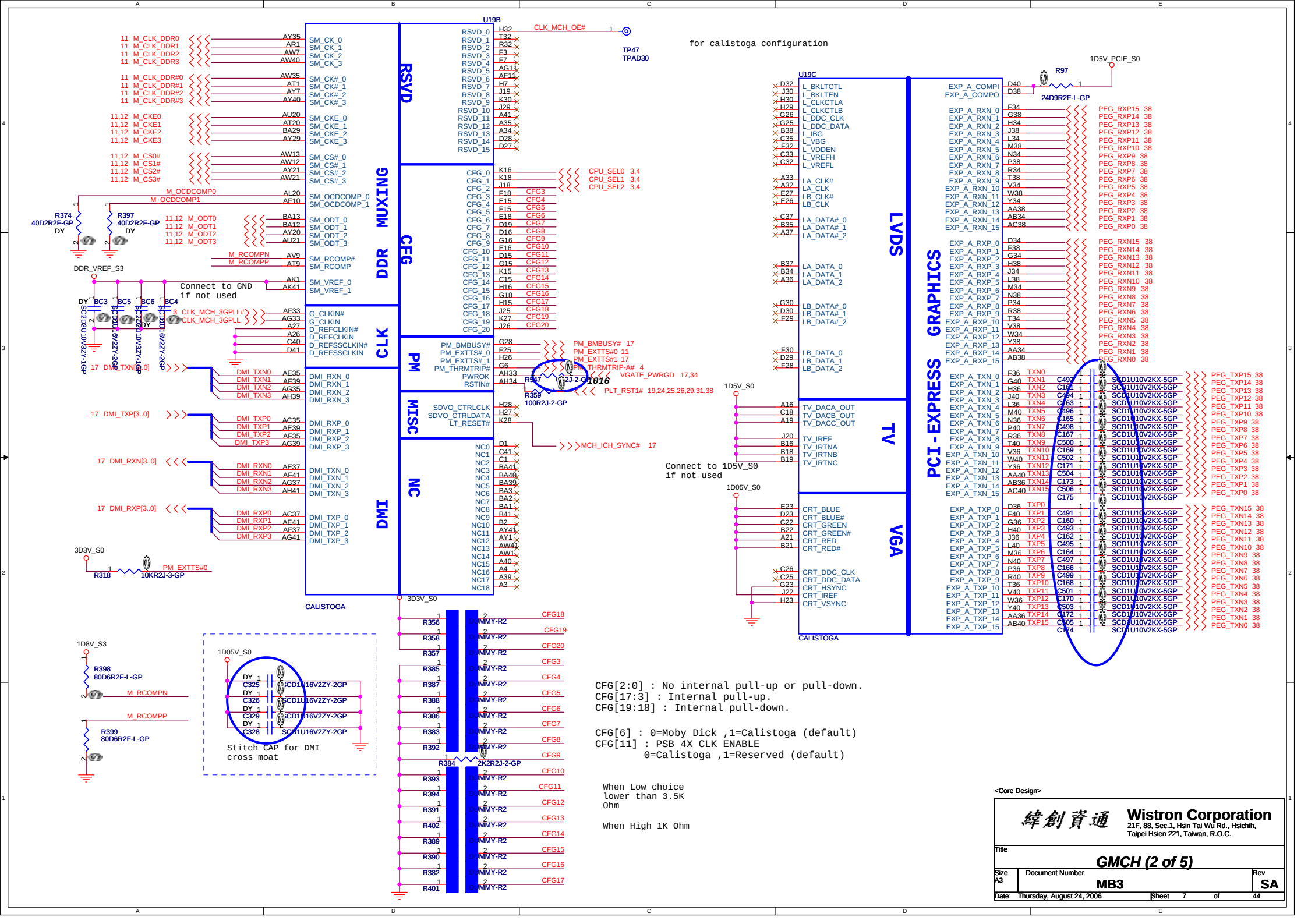
Title: GMCH (1 of 5)

Size	Document Number	Rev
A3	MB3	SA

Date: Thursday, August 24, 2006 Sheet 6 of 44


U19B
RSVD
CFG
MUXING
DDR
CLK
PM
MISC
NC
DMI
CALISTOGA
for calistoga configuration
U19C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA
Connect to GND if not used
Connect to 1D5V_S0 if not used
Stitch CAP for DMI cross moat
CFG[2:0] : No internal pull-up or pull-down.
CFG[17:3] : Internal pull-up.
CFG[19:18] : Internal pull-down.
CFG[6] : 0=Moby Dick ,1=Calistoga (default)
CFG[11] : PSB 4X CLK ENABLE
0=Calistoga ,1=Reserved (default)
When Low choice lower than 3.5K Ohm
When High 1K Ohm
<Core Design>
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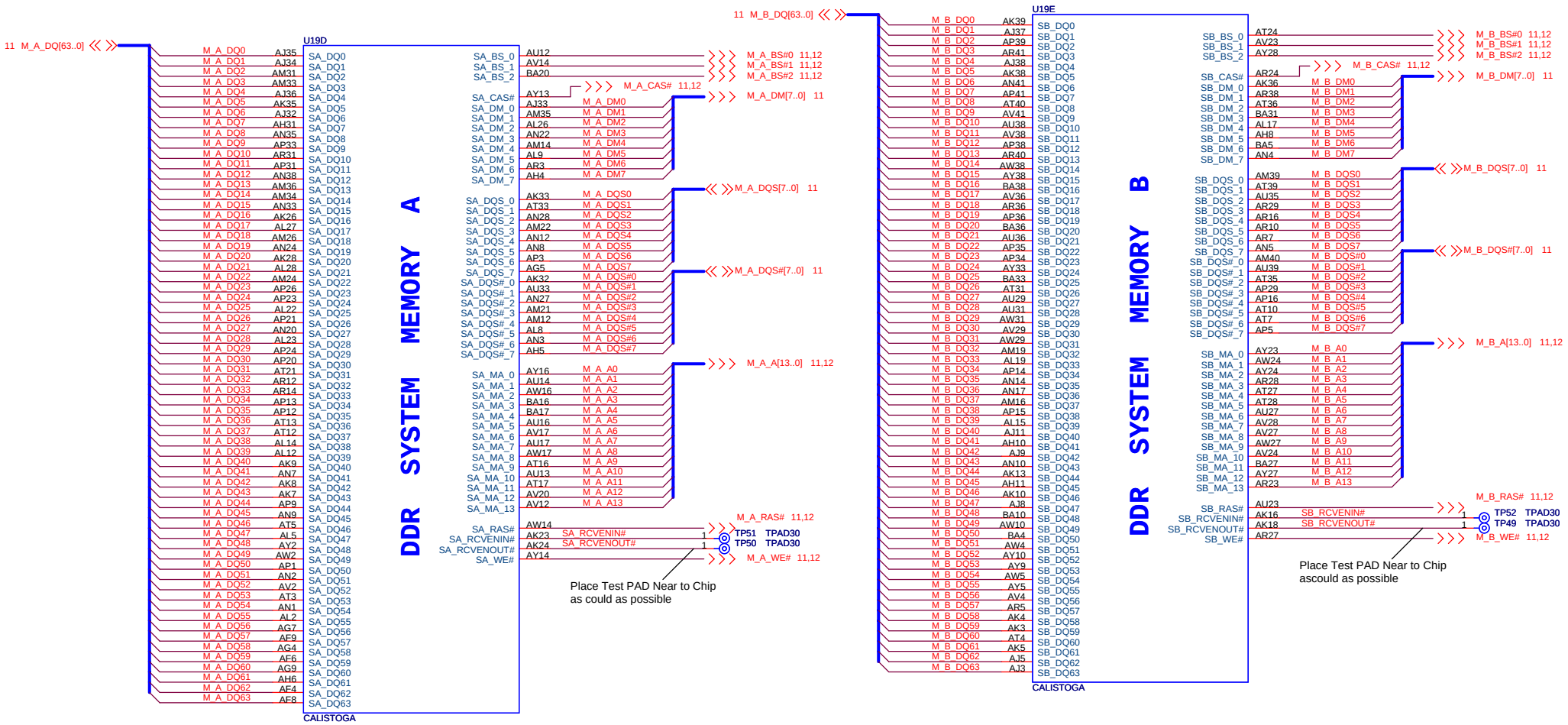
Title
GMCH (2 of 5)
Size A3
Document Number MB3
Rev SA
Date: Thursday, August 24, 2006
Sheet 7 of 44



<Core Design>

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Title: ***GMCH (3 of 5)***

Size	Document Number	Rev
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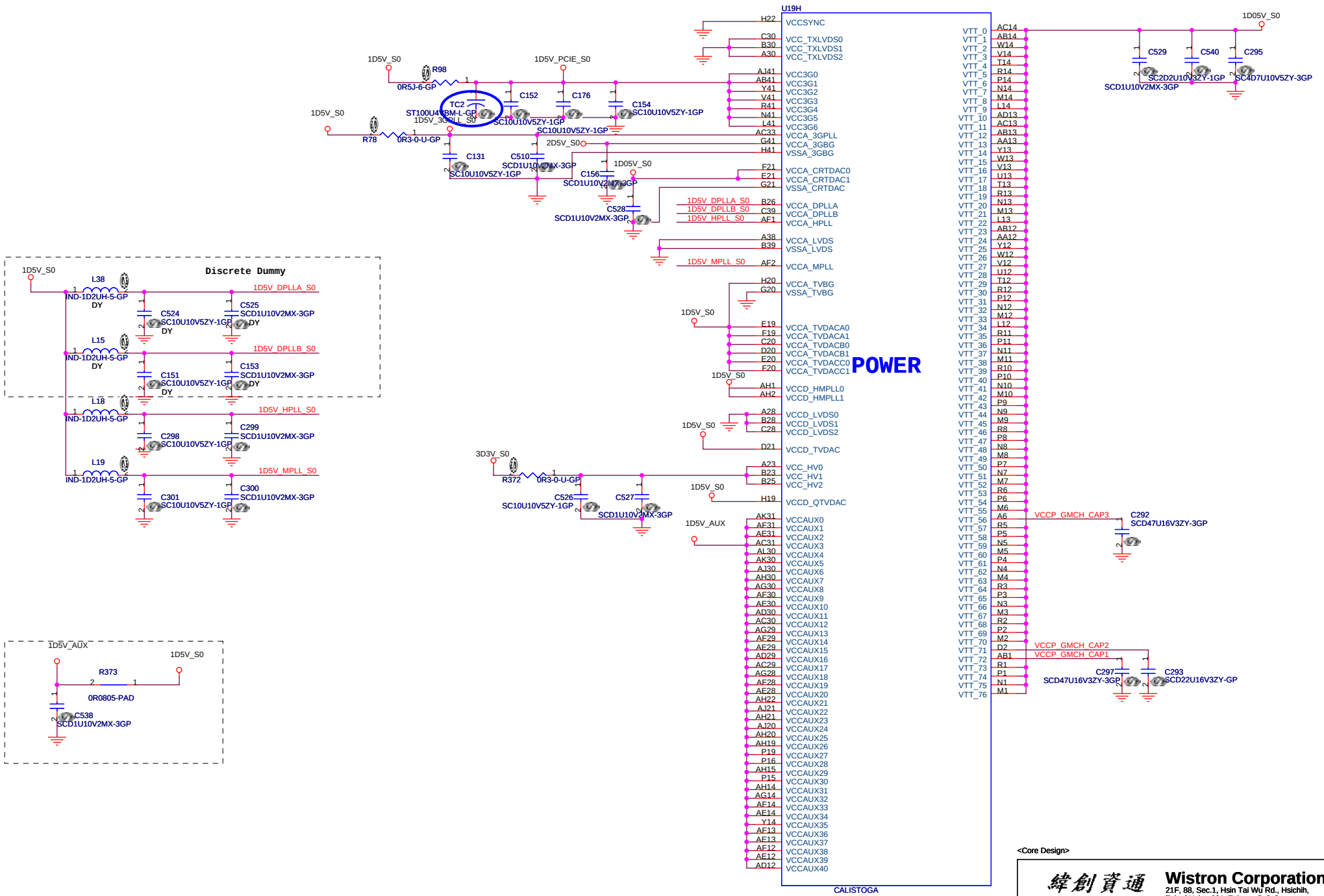
Date: Thursday, August 24, 2006 Sheet 8 of 44



<Core Design>

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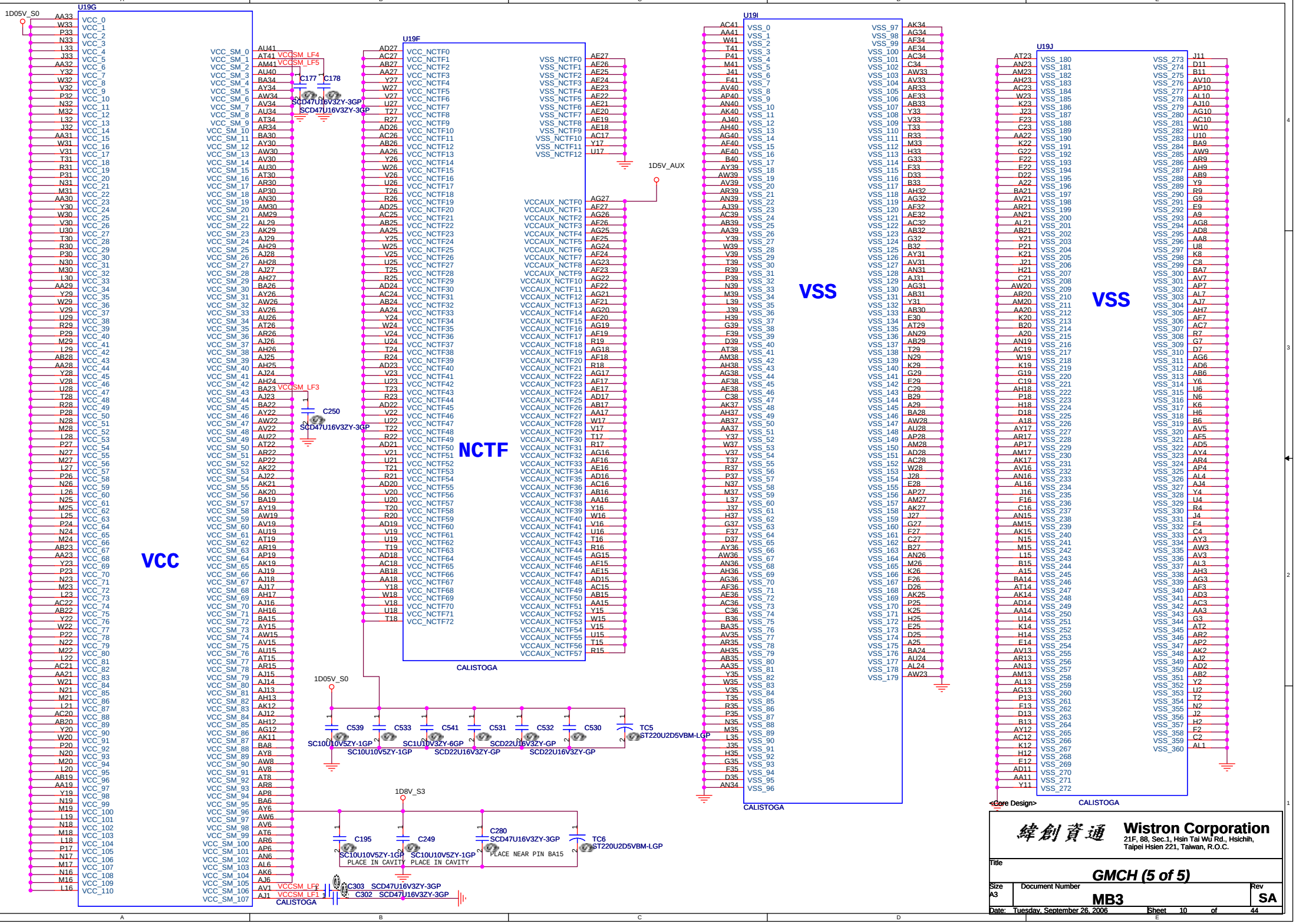
Title: ***GMCH (4 of 5)***

Size	Document Number	Rev
A3	MB3	SA

Date: Thursday, August 17, 2006 Sheet 9 of 44



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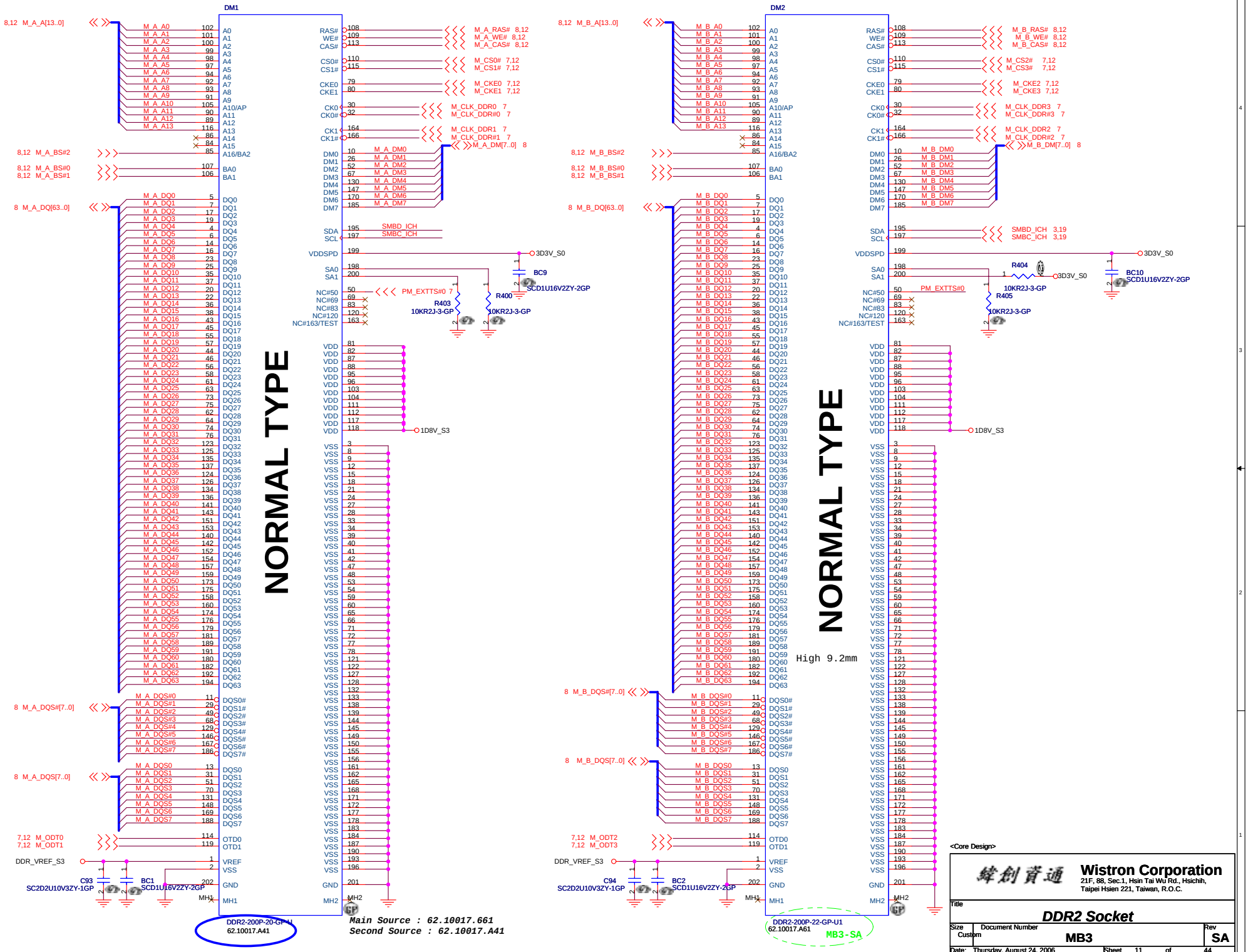
Title: GMCH (5 of 5)

Size: A3 | Document Number: MB3 | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 10 of 44


DM1
NORMAL TYPE
DDR2-200P-20-GP-U
62.10017.A41
Main Source : 62.10017.661
Second Source : 62.10017.A41
DM2
NORMAL TYPE
High 9.2mm
DDR2-200P-22-GP-U1
62.10017.A61
MB3-SA
<Core Design>
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Title
DDR2 Socket
Size
Custom
Document Number
MB3
Rev
SA
Date: Thursday, August 24, 2006
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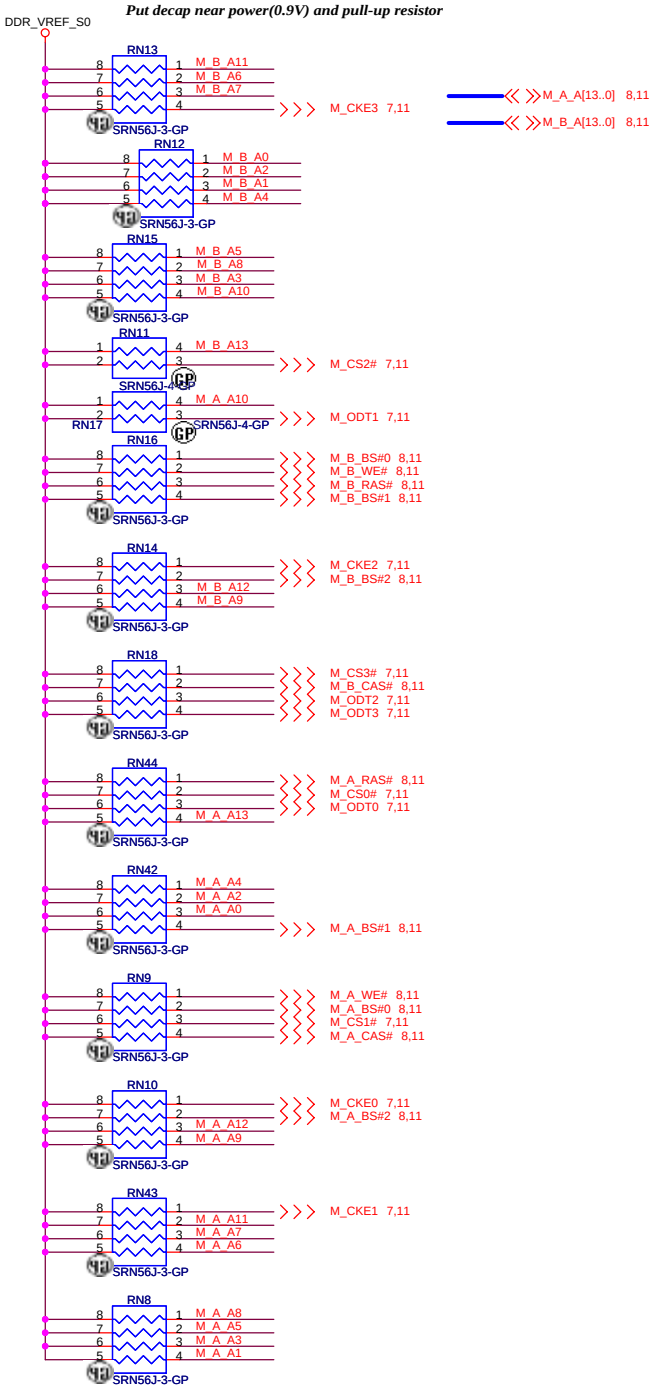
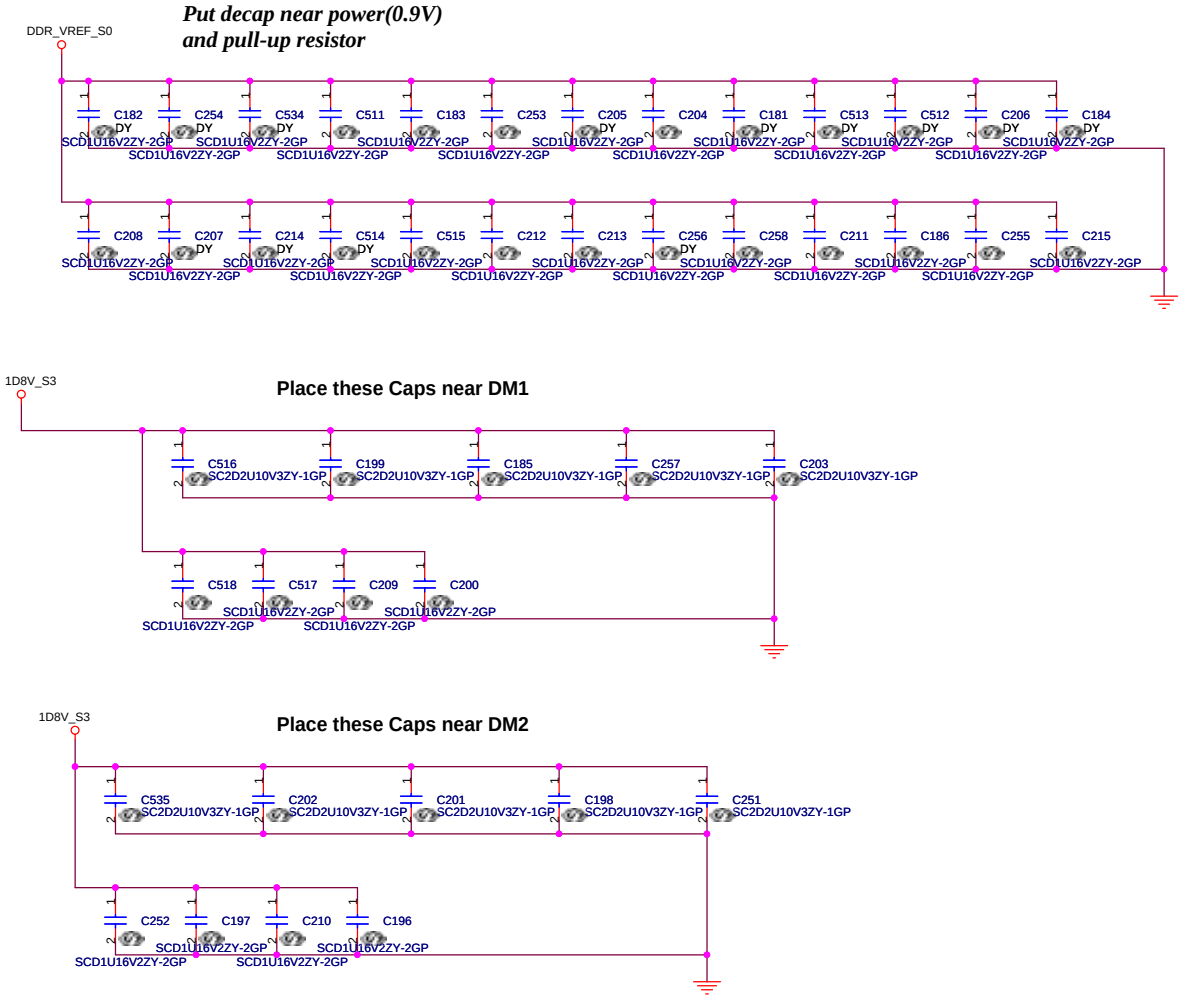
PARALLEL TERMINATION



Decoupling Capacitor



<Core Design>

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Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
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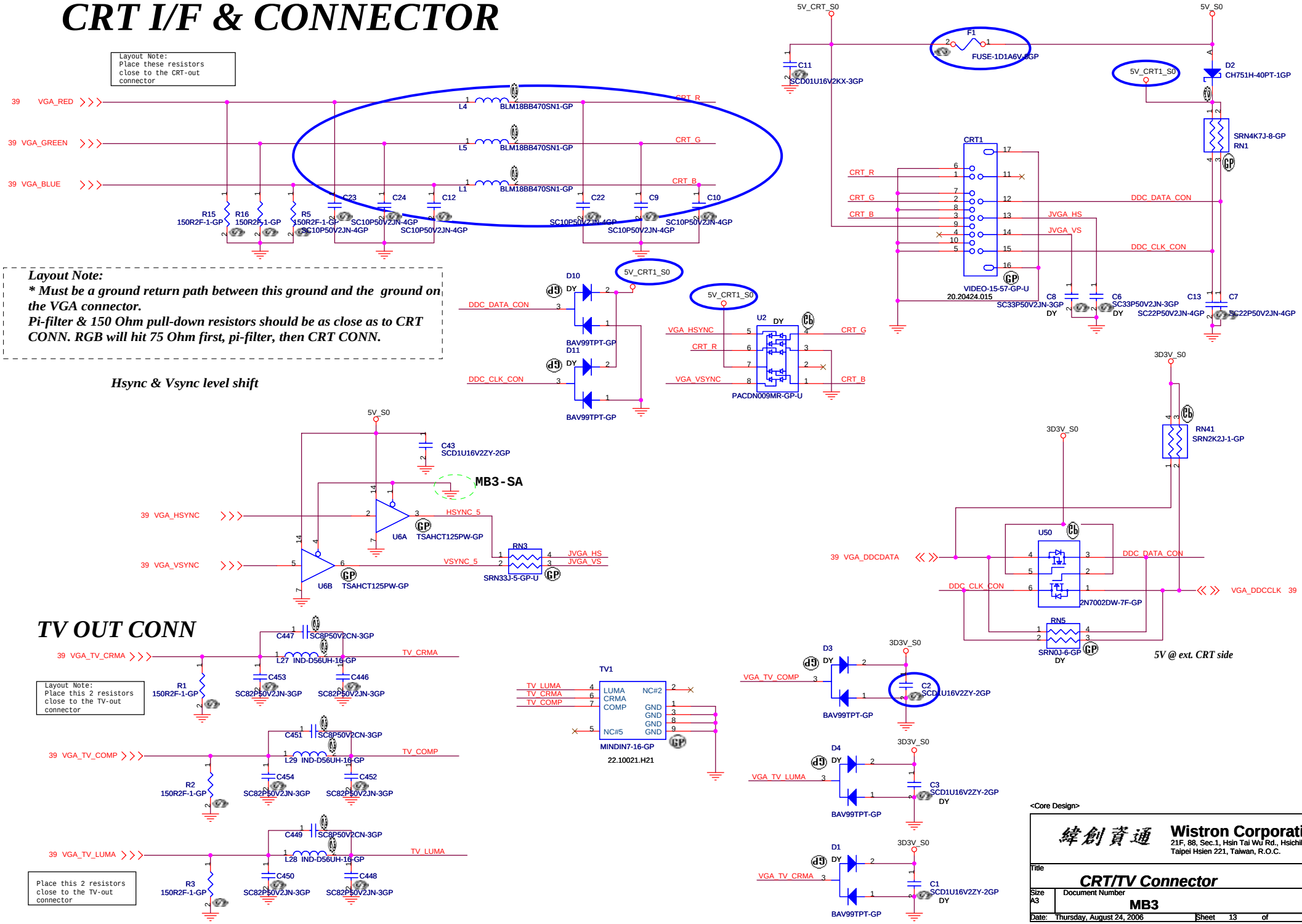
CRT I/F & CONNECTOR



<Core Design>

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Title: **CRT/TV Connector**

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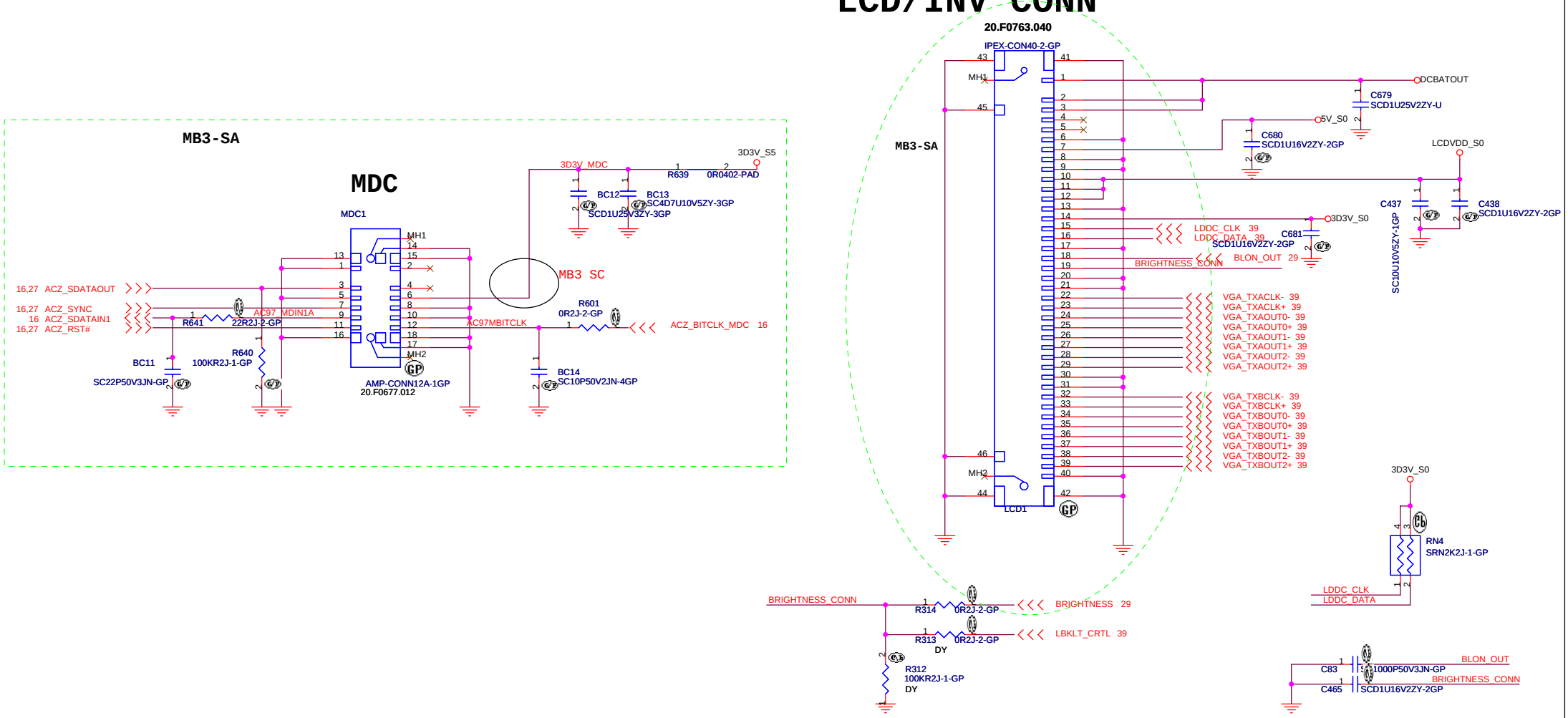
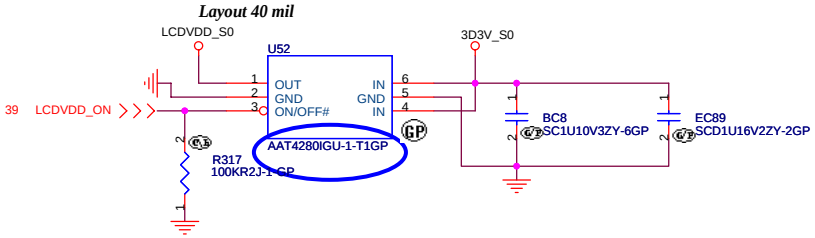
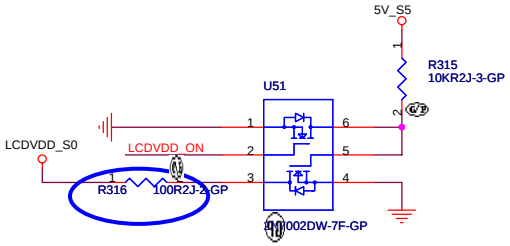
LED / INVERTER INTERFACE

LCD/INV CONN







Discharge circuit

<Core Design>

緯創資通 **Wistron Corporation**
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Title: **LCD/Inverter Connector**

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Custom	MB3	SA

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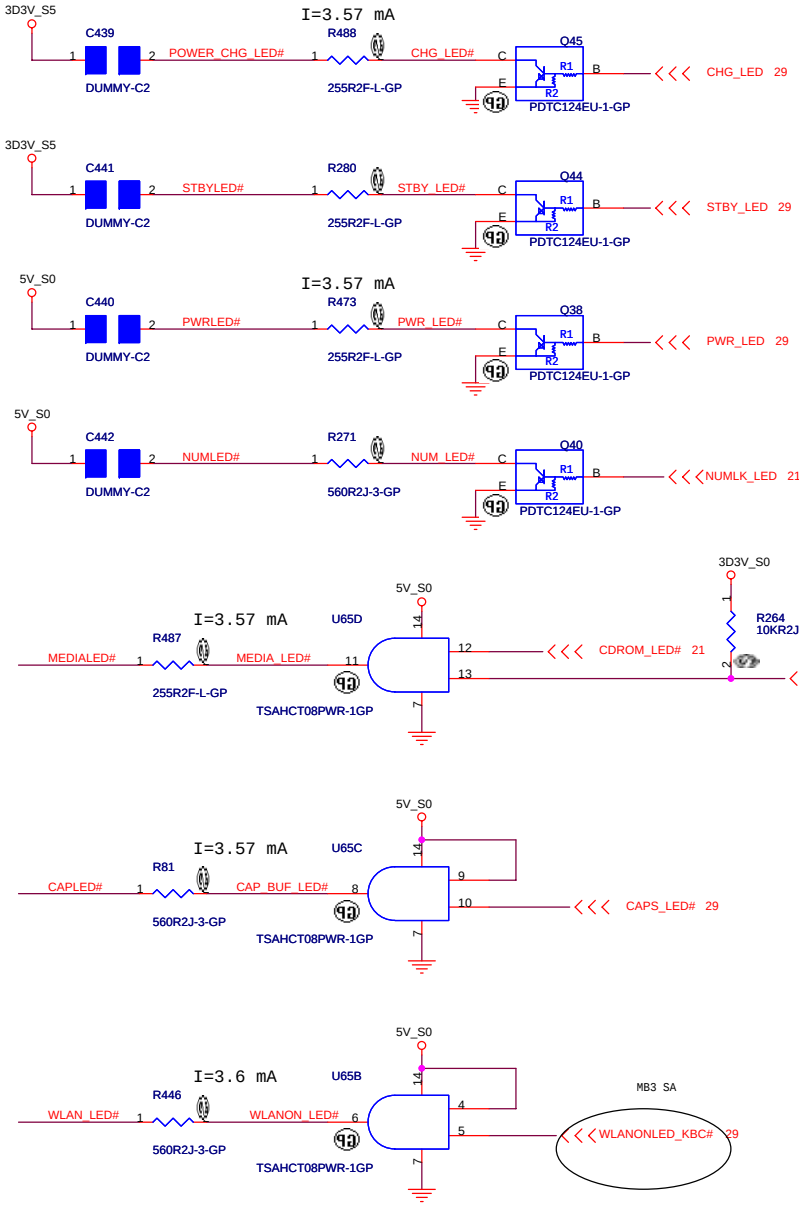
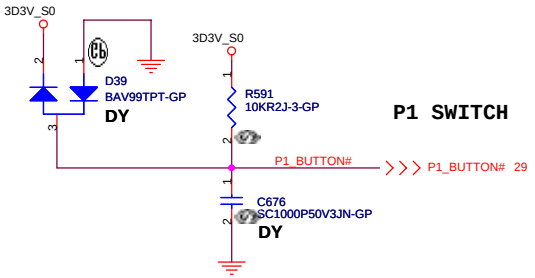
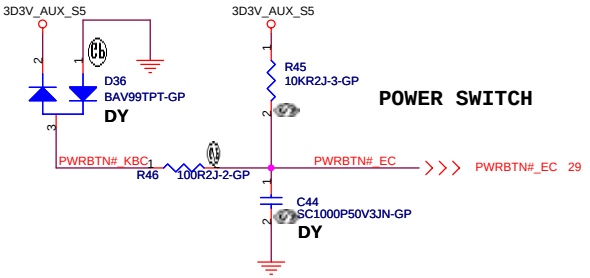
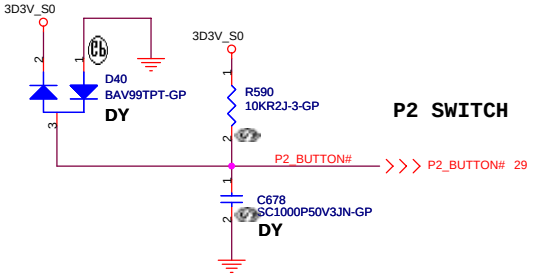
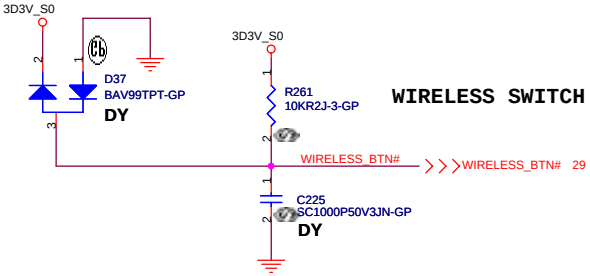
all page is for MB3-SA



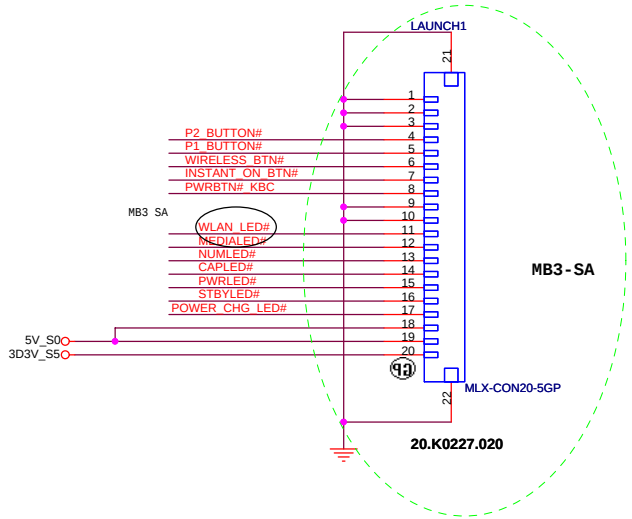


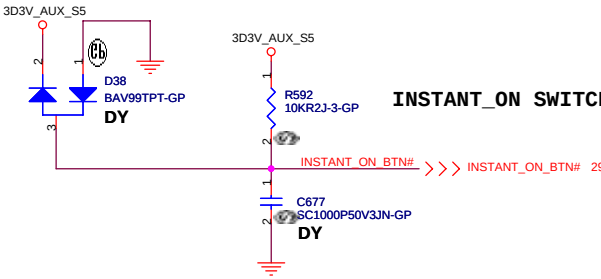






Launch Board CNN





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Title: Board to board conn/ Docking

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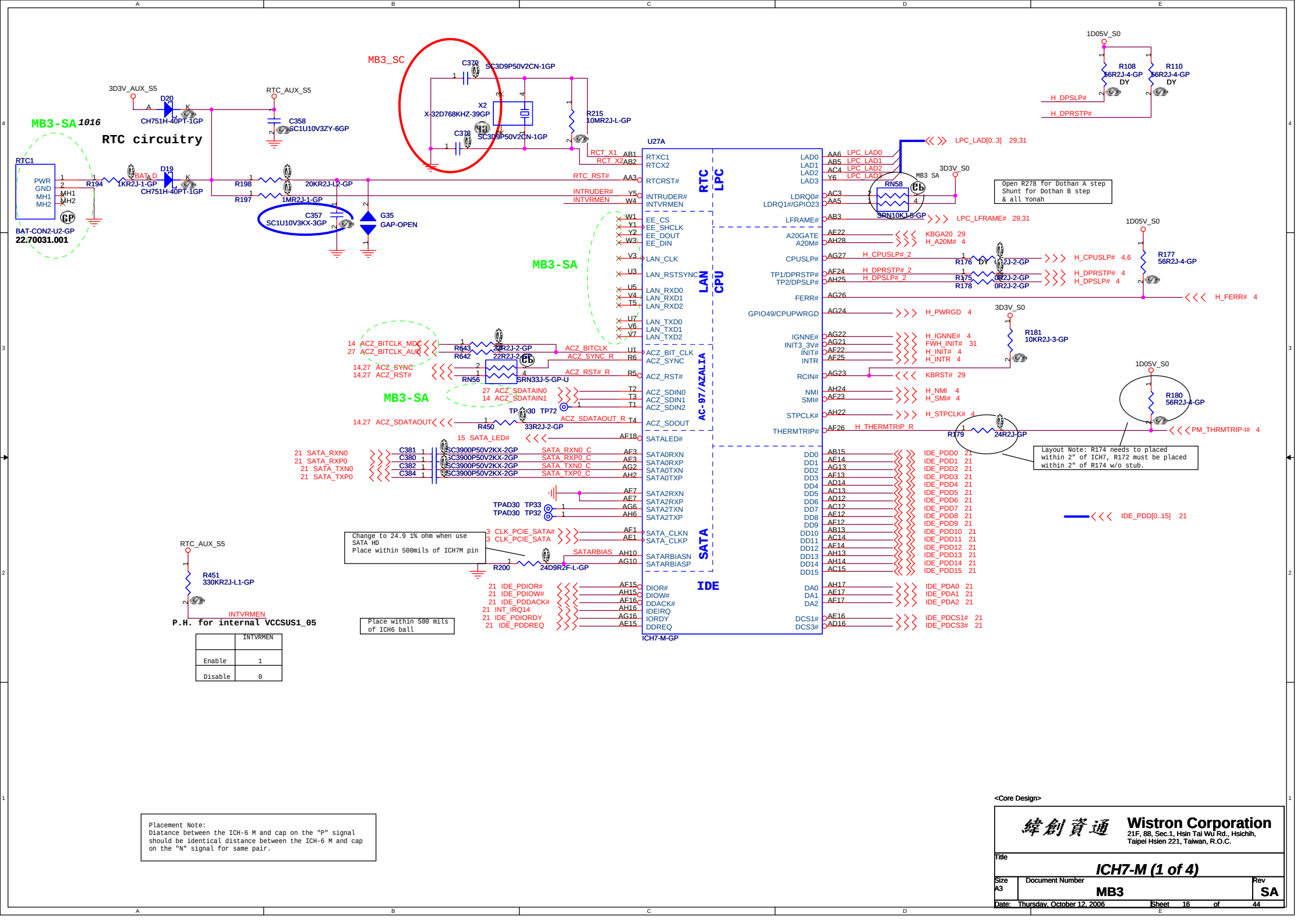
Date: Thursday, August 24, 2006 Sheet 15 of 44


MB3-SA 1016
RTC circuitry
MB3_SC
MB3-SA
MB3-SA
U27A
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
ICH7-M-GP
RTC1
BAT-CON2-U2-GP
22.70031.001
3D3V_AUX_S5
RTC_AUX_S5
CH751H-40PT-1GP
SC1U10V3ZY-6GP
X2
X-32D768KHZ-39GP
SC3D9P50V2CN-1GP
10MR2J-L-GP
20KR2J-L2-GP
1MR2J-1-GP
SC1U10V3KX-3GP
GAP-OPEN
1KR2J-1-GP
RTC_RST#
INTRUDER#
INTVRMEN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
SRN10KJ-6-GP
SRN33J-5-GP-U
24D9R2F-L-GP
33R2J-2-GP
24R2J-GP
10KR2J-3-GP
56R2J-4-GP
0R2J-2-GP
Open R278 for Dothan A step
Shunt for Dothan B step
& all Yonah
Layout Note: R174 needs to placed within 2" of ICH7, R172 must be placed within 2" of R174 w/o stub.
Change to 24.9 1% ohm when use SATA HD
Place within 500mils of ICH7M pin
Place within 500 mils of ICH6 ball
P.H. for internal VCCSUS1_05
INTVRMEN
Enable 1
Disable 0
Placement Note:
Diatance between the ICH-6 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
ICH7-M (1 of 4)
Size A3
Document Number MB3
Rev SA
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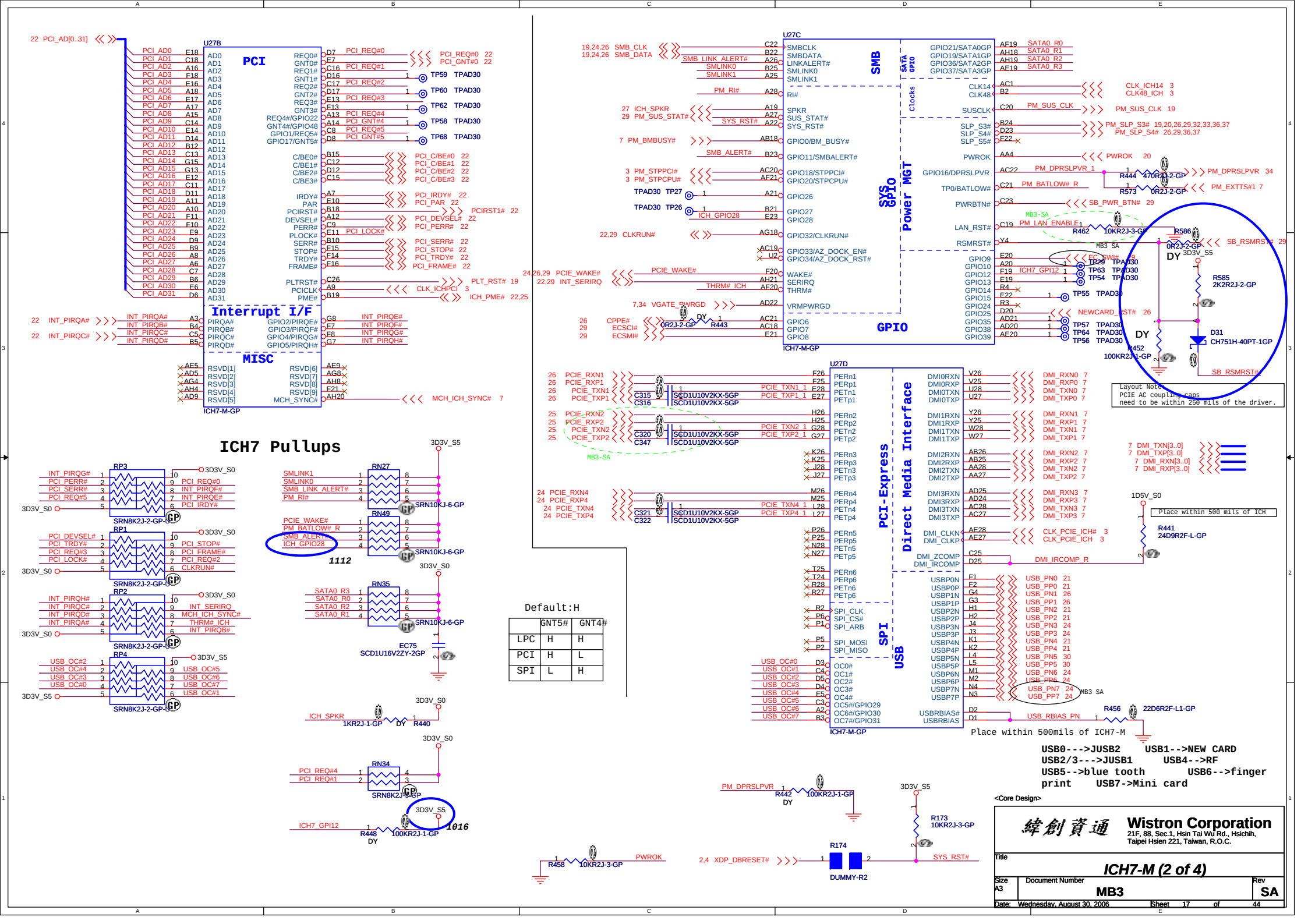
U27B
PCI
Interrupt I/F
MISC
ICH7-M-GP
U27C
SMB
SYS GPIO
Power MGT
GPIO
Clocks
ICH7-M-GP
U27D
PCI-Express
Direct Media Interface
SPI
USB
ICH7-M-GP
ICH7 Pullups
Default:H
GNT5# GNT4#
LPC H H
PCI H L
SPI L H
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
Place within 500mils of ICH7-M
USB0--->JUSB2 USB1-->NEW CARD
USB2/3--->JUSB1 USB4-->RF
USB5-->blue tooth USB6-->finger
print USB7->Mini card
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
Size A3
Document Number MB3
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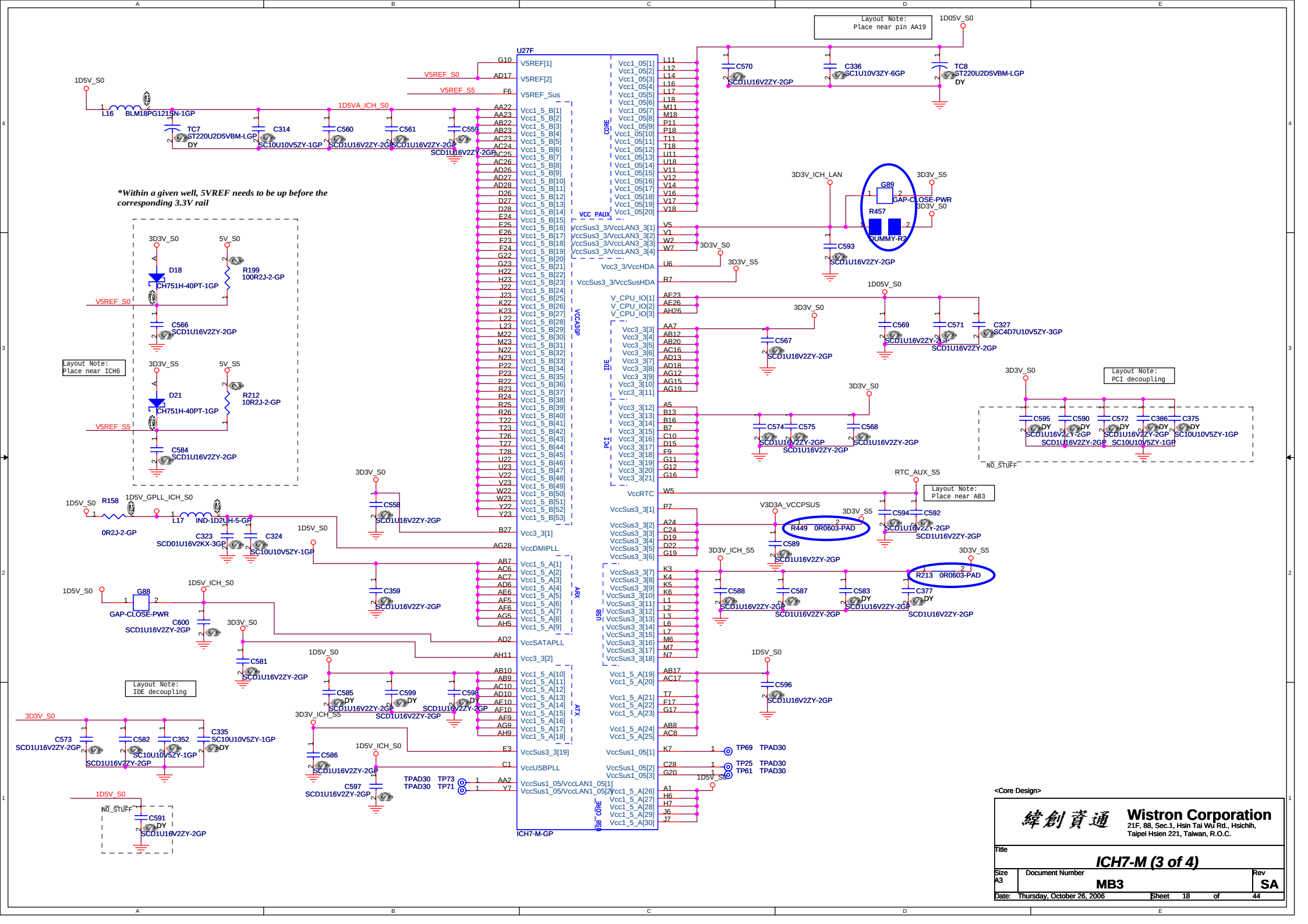
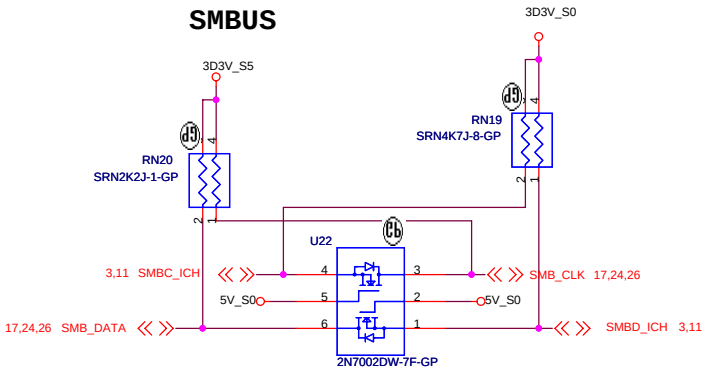
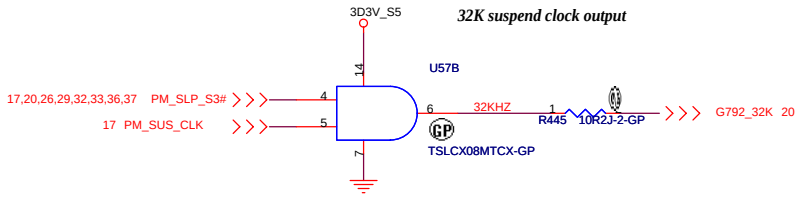
Date: Wednesday, August 30, 2006
Sheet 17 of 44

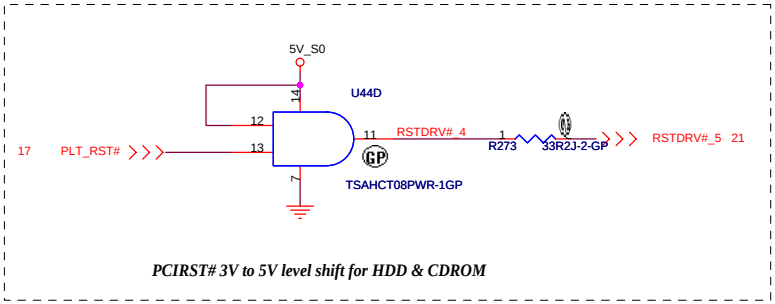

U27F
ICH7-M-GP
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH6
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Layout Note: Place near AB3
NO_STUFF
GAP-CLOSE-PWR
DUMMY-R3
0R2J-2-GP
IND-1D2UH-5-GP
TPAD30
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size A3
Document Number
MB3
Rev
SA
Date: Thursday, October 26, 2006
Sheet 18 of 44

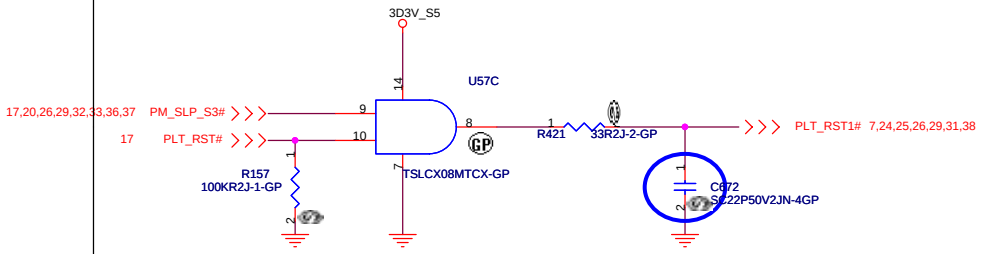
SMBUS

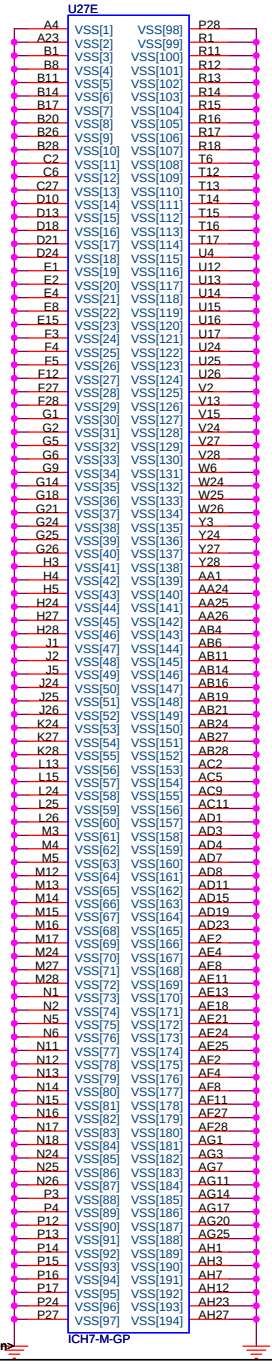


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance









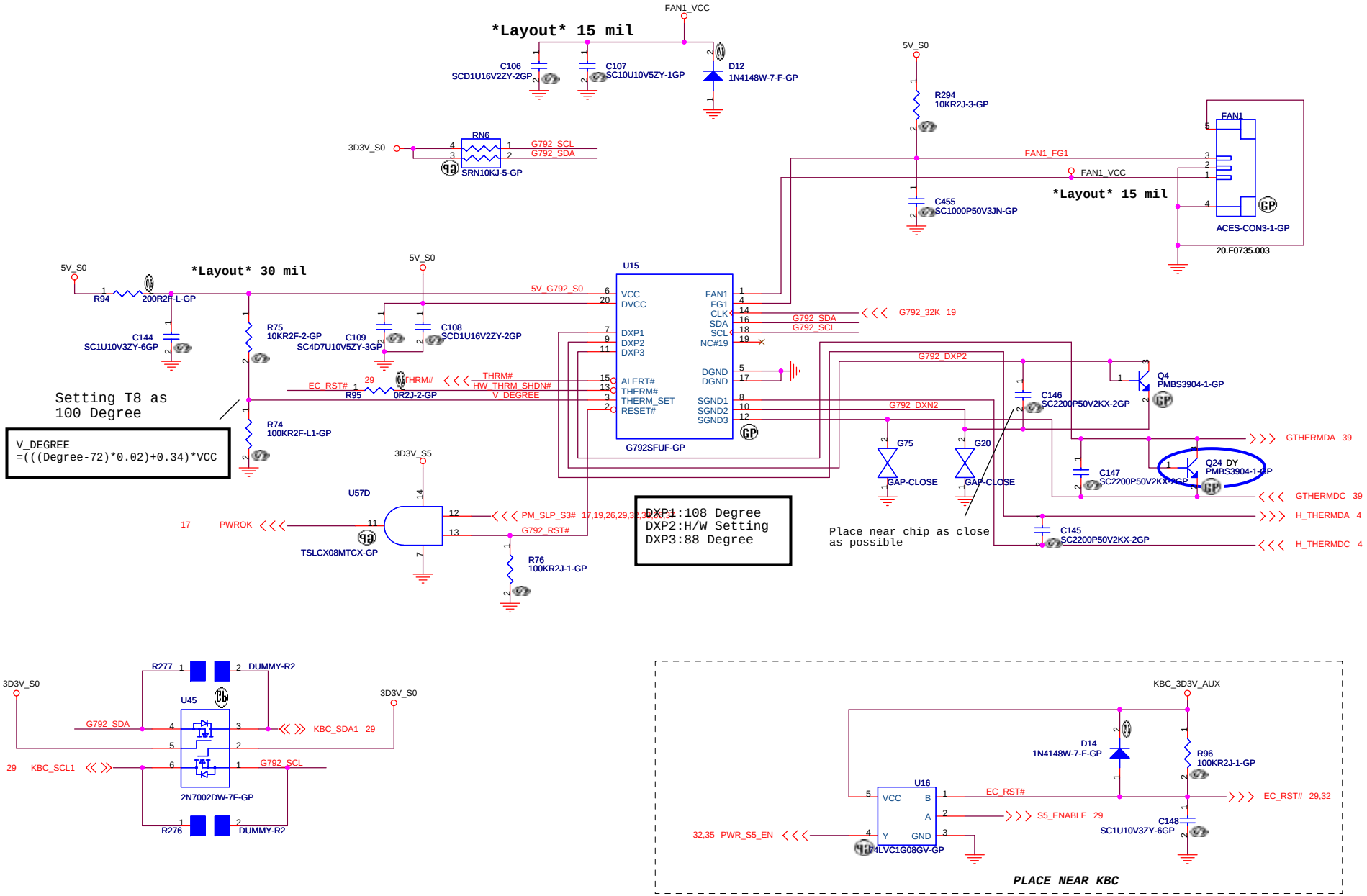
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH7-M (4 of 4)**

Size	Document Number	Rev
A3	MB3	SA

Date: Thursday, August 24, 2006 Sheet 19 of 44



<Core Design>

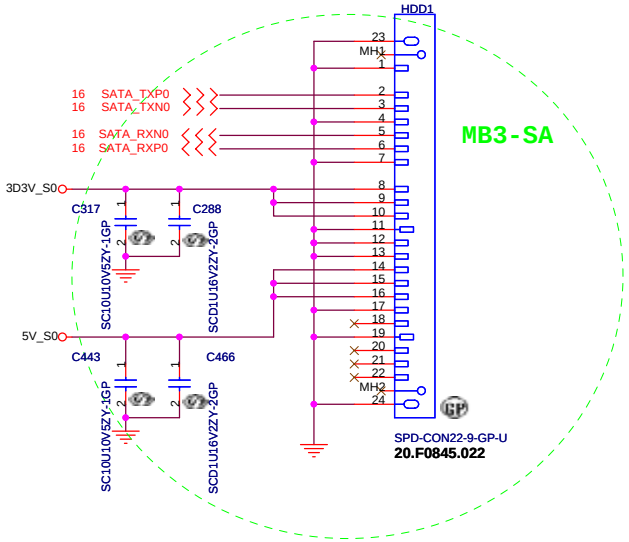
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

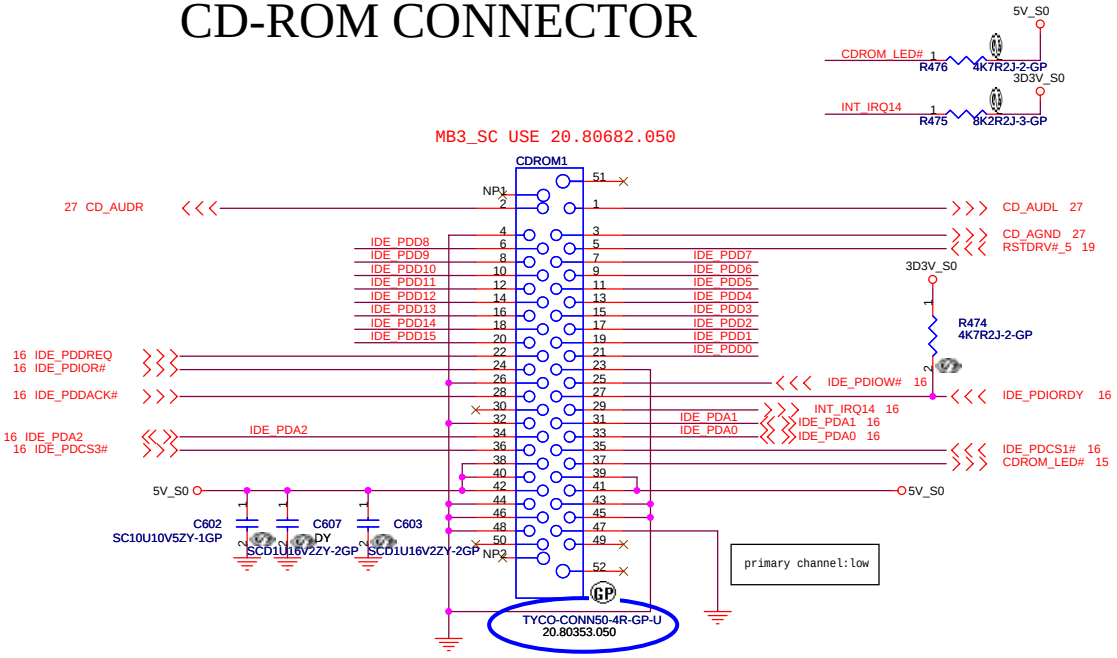
Size	Document Number	Rev
Custom	MB3	SA

Date: Wednesday, October 18, 2006 Sheet 20 of 44

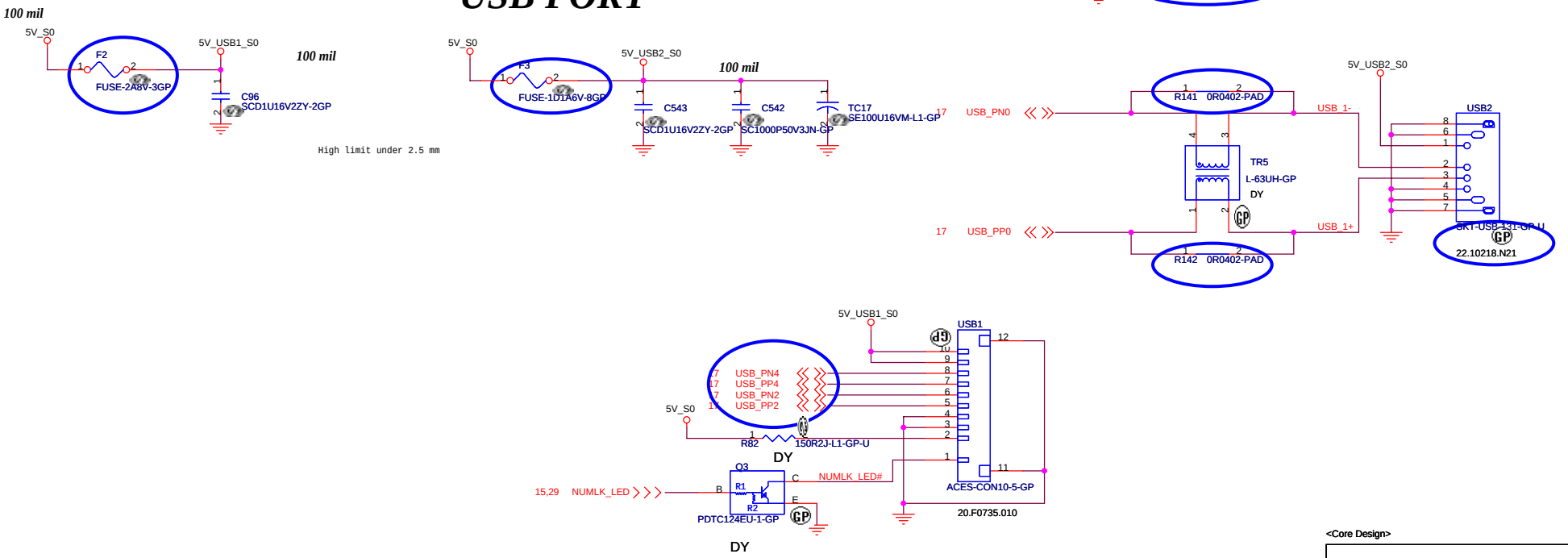
SATA HD Connector



CD-ROM CONNECTOR



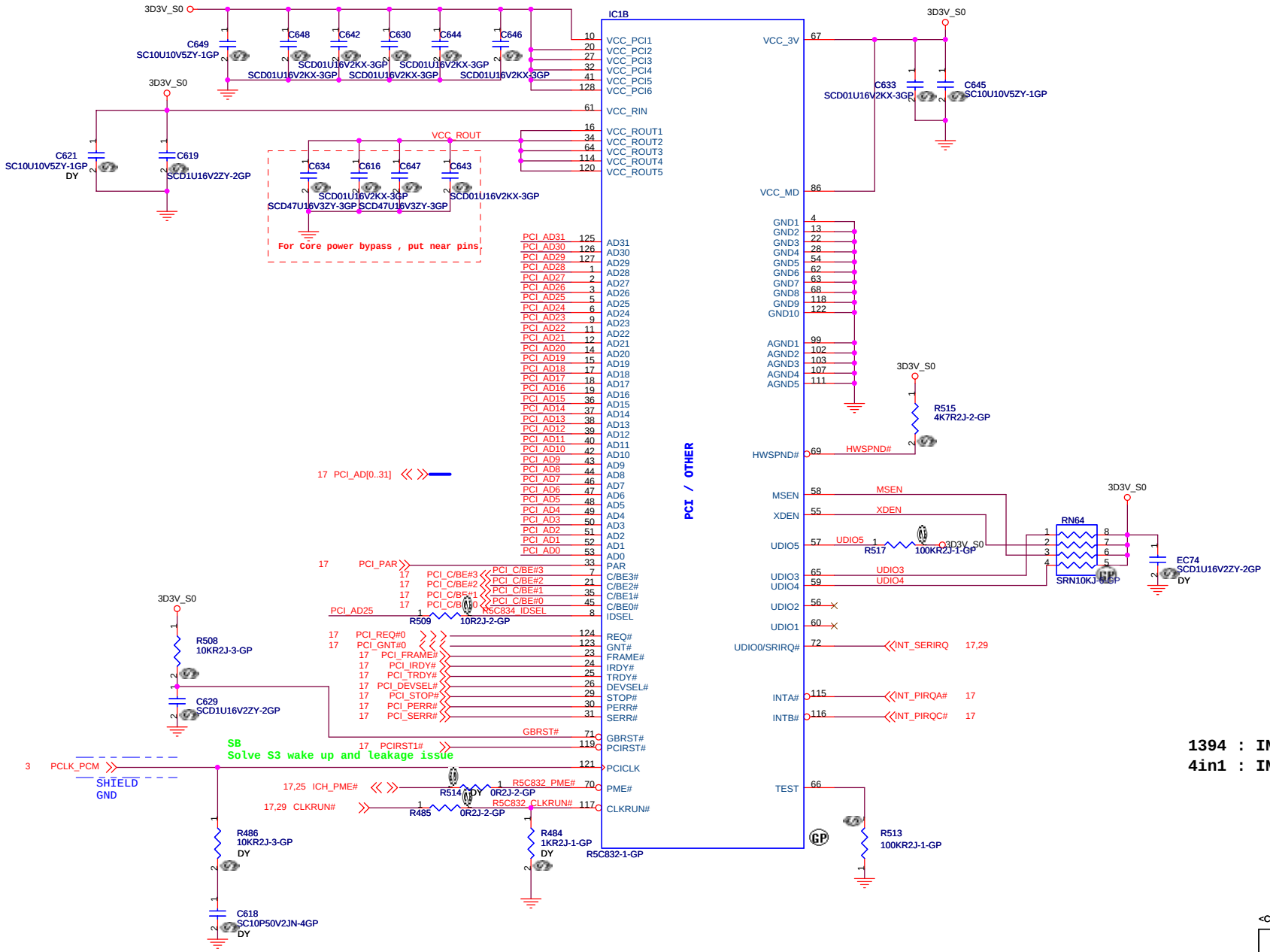
USB PORT



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HD/CDROM***	
Size A3	Document Number **MB3**	Rev **SA**
Date: Friday, October 13, 2006	Sheet 21 of 44	



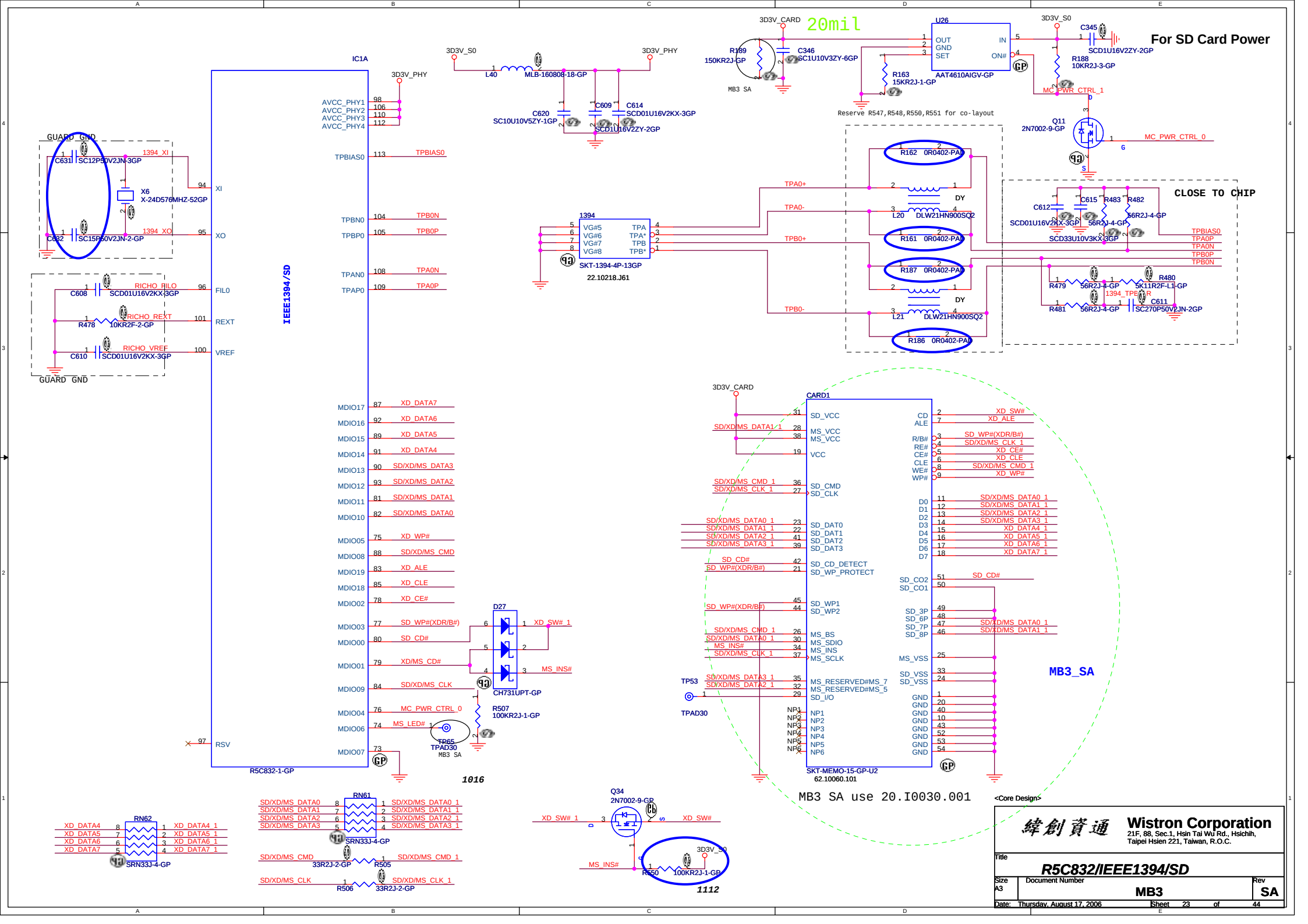
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

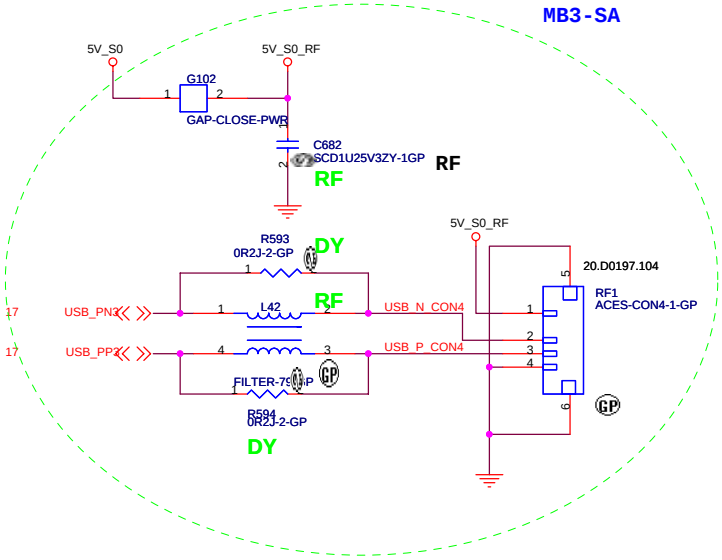
Title: R5C832/PCI

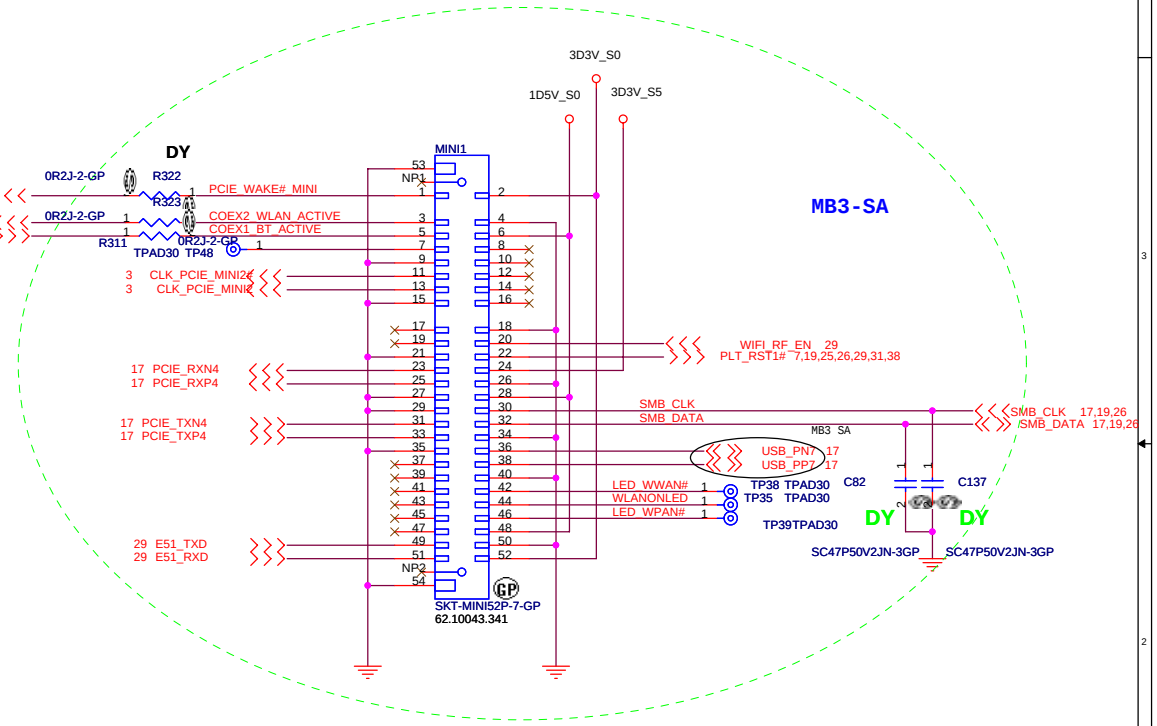
Size	Document Number	Rev
A3	MB3	SA

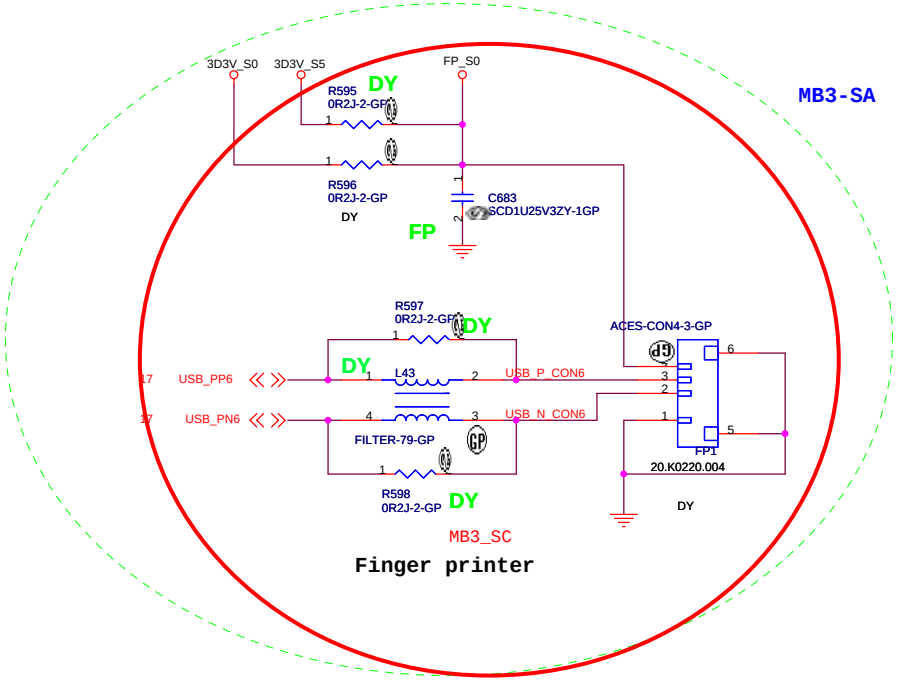
Date: Thursday, August 24, 2006 Sheet 22 of 44

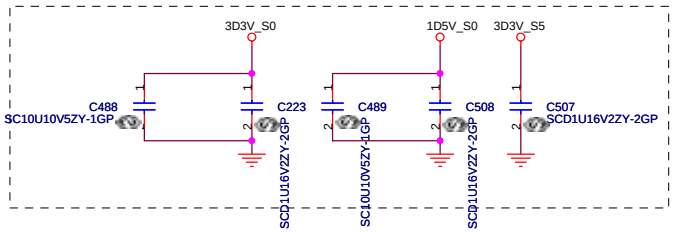

For SD Card Power
20mil
IC1A
IEEE1394/SD
R5C832-1-GP
CARD1
SKT-MEMO-15-GP-U2
62.10060.101
MB3_SA
MB3 SA use 20.I0030.001
CLOSE TO CHIP
Reserve R547,R548,R550,R551 for co-layout
1016
1112
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C832/IEEE1394/SD
MB3
SA
Thursday, August 17, 2006
23
44

Mini Card Connector 1



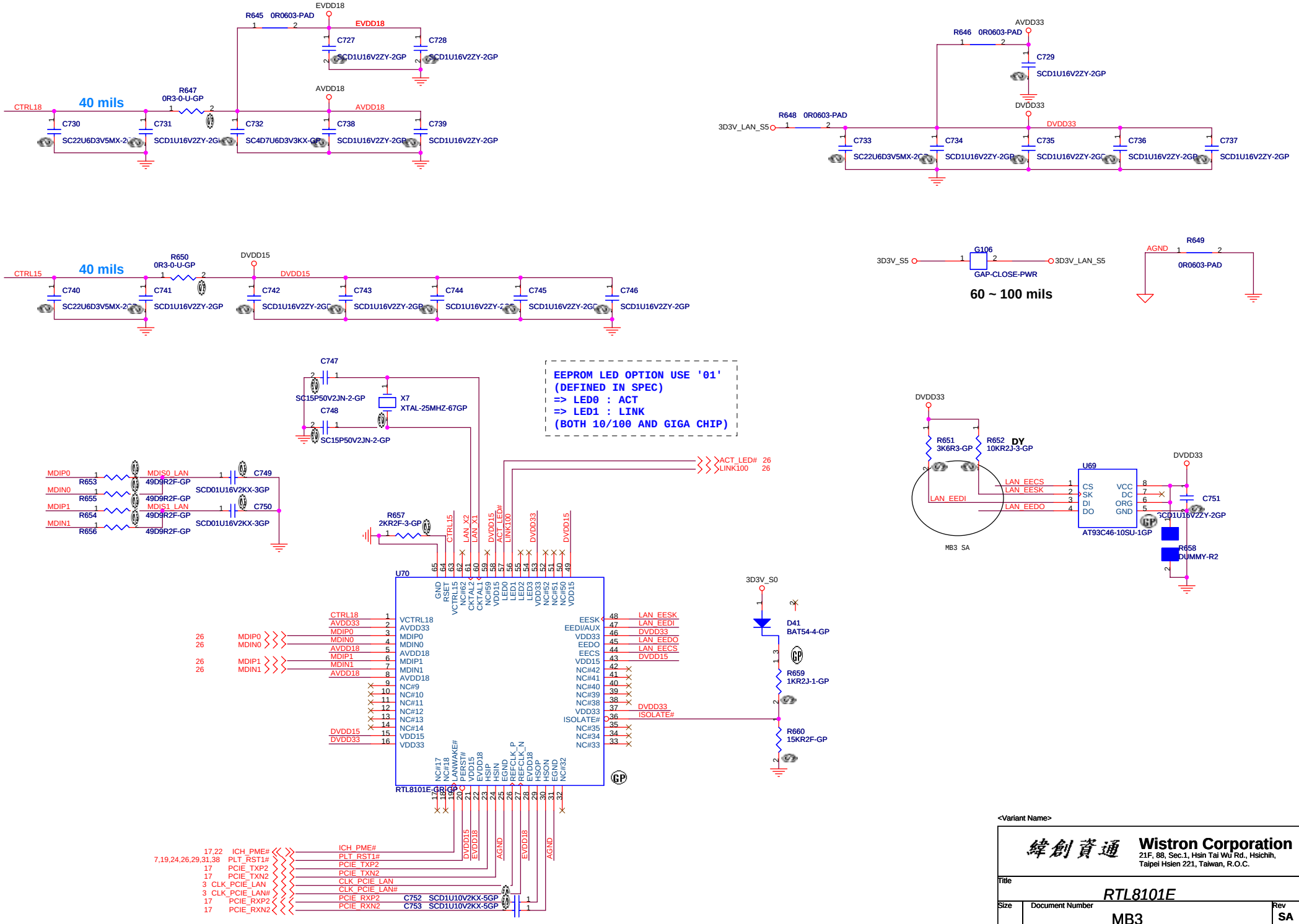






<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD CONN .		
Size: A3	Document Number: MB3	Rev: SA
Date: Wednesday, September 27, 2006	Sheet 24 of 44	



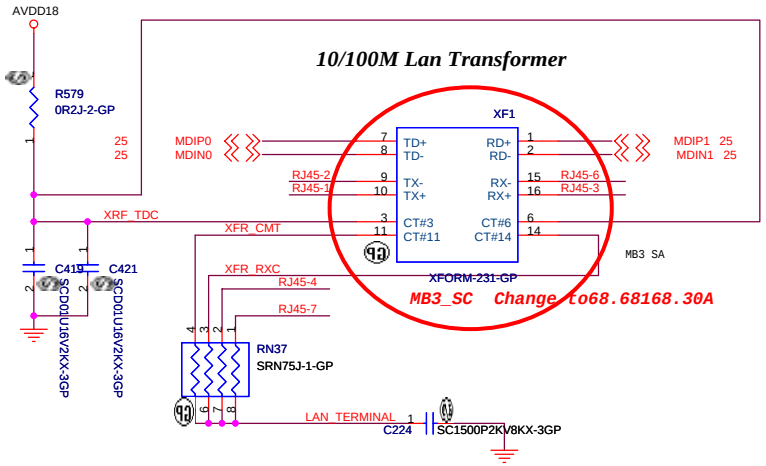
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

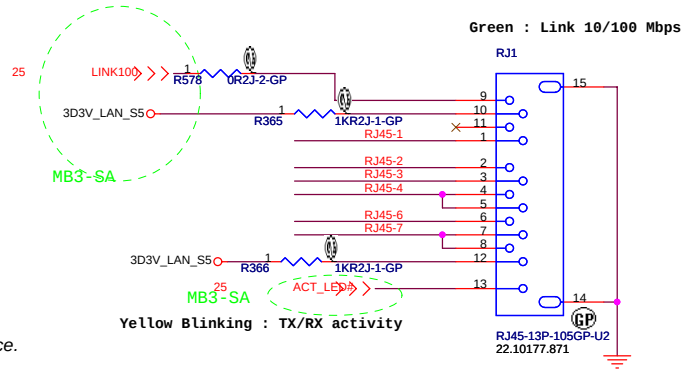
Title: *RTL8101E*

Size	Document Number	Rev
	MB3	SA

Date: Thursday, August 24, 2006 Sheet 25 of 44



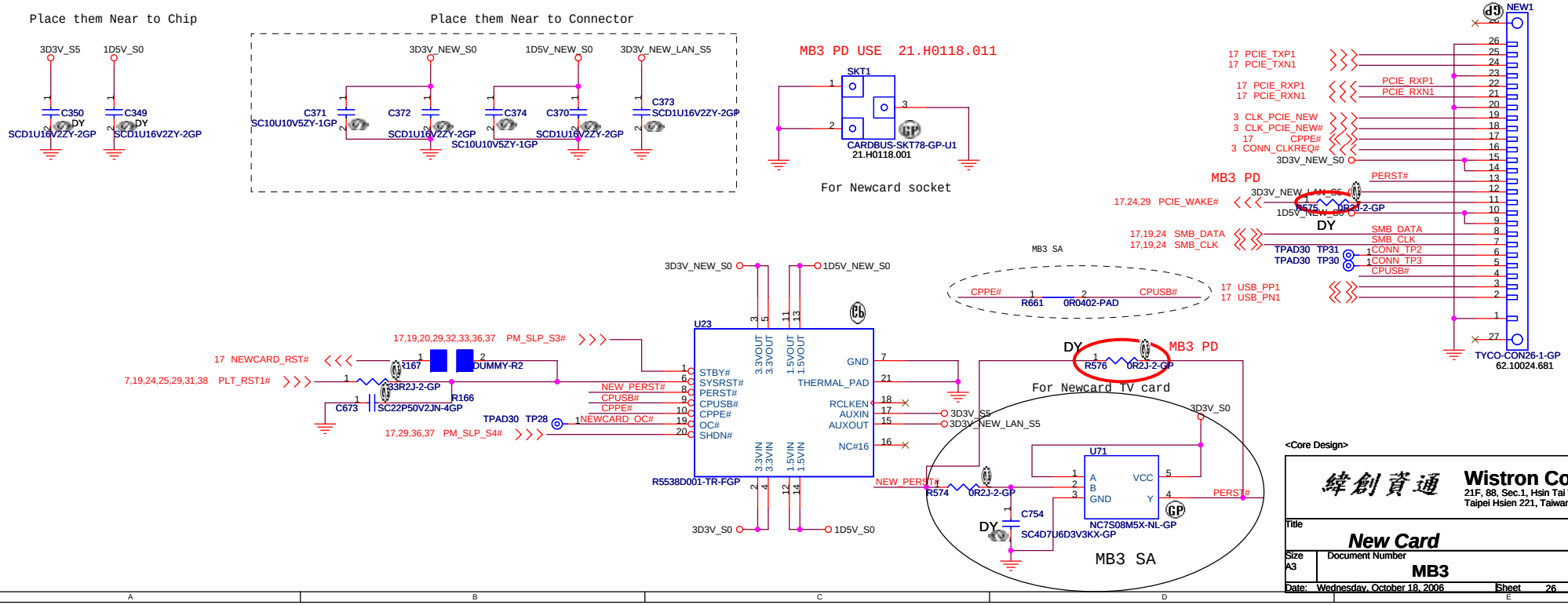
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



Pin10(+)Pin9(-) Green
Pin10(+)Pin11(-) Orange
Pin12(+) Pin13(-) Yellow

PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

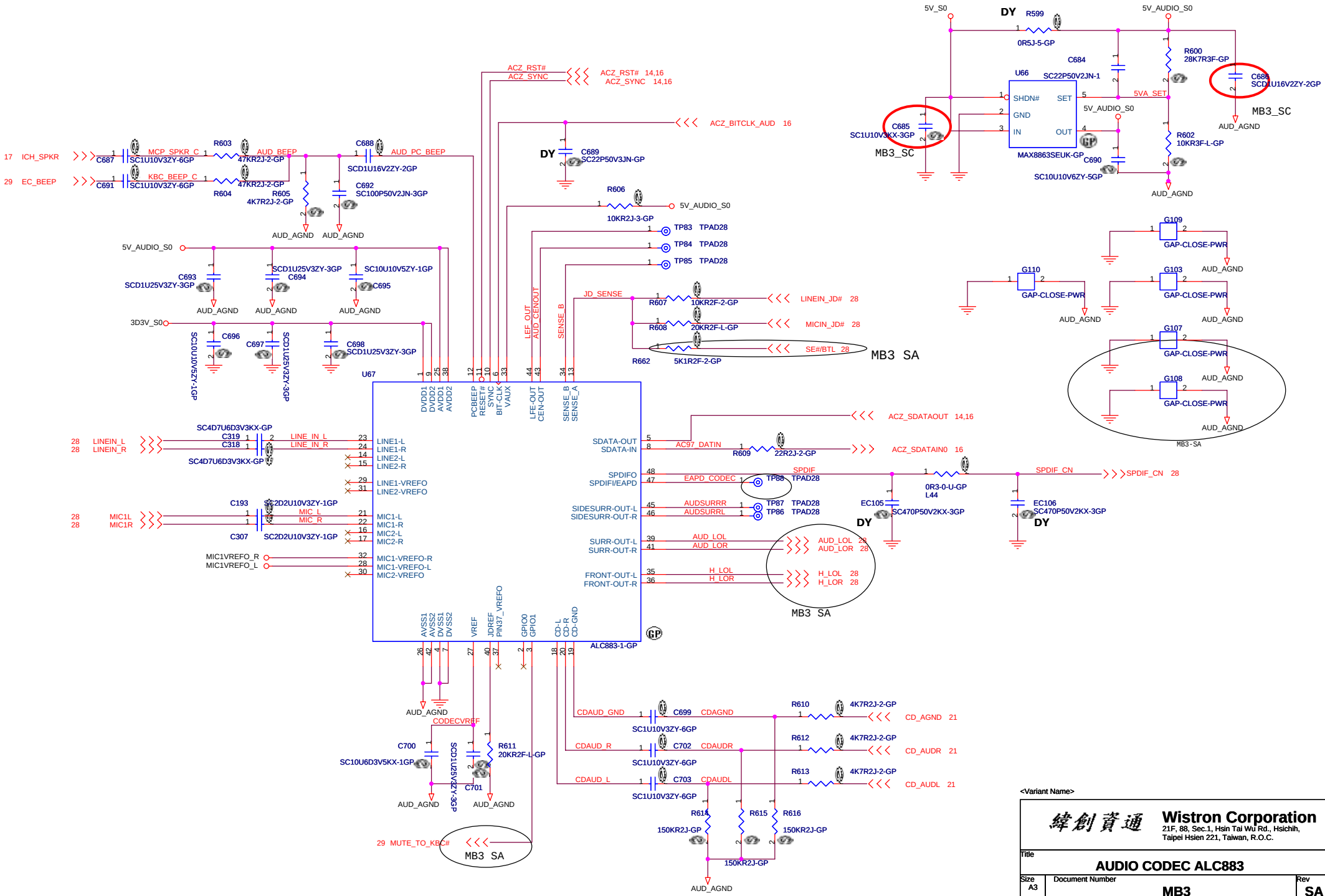
NEWCARD Connector

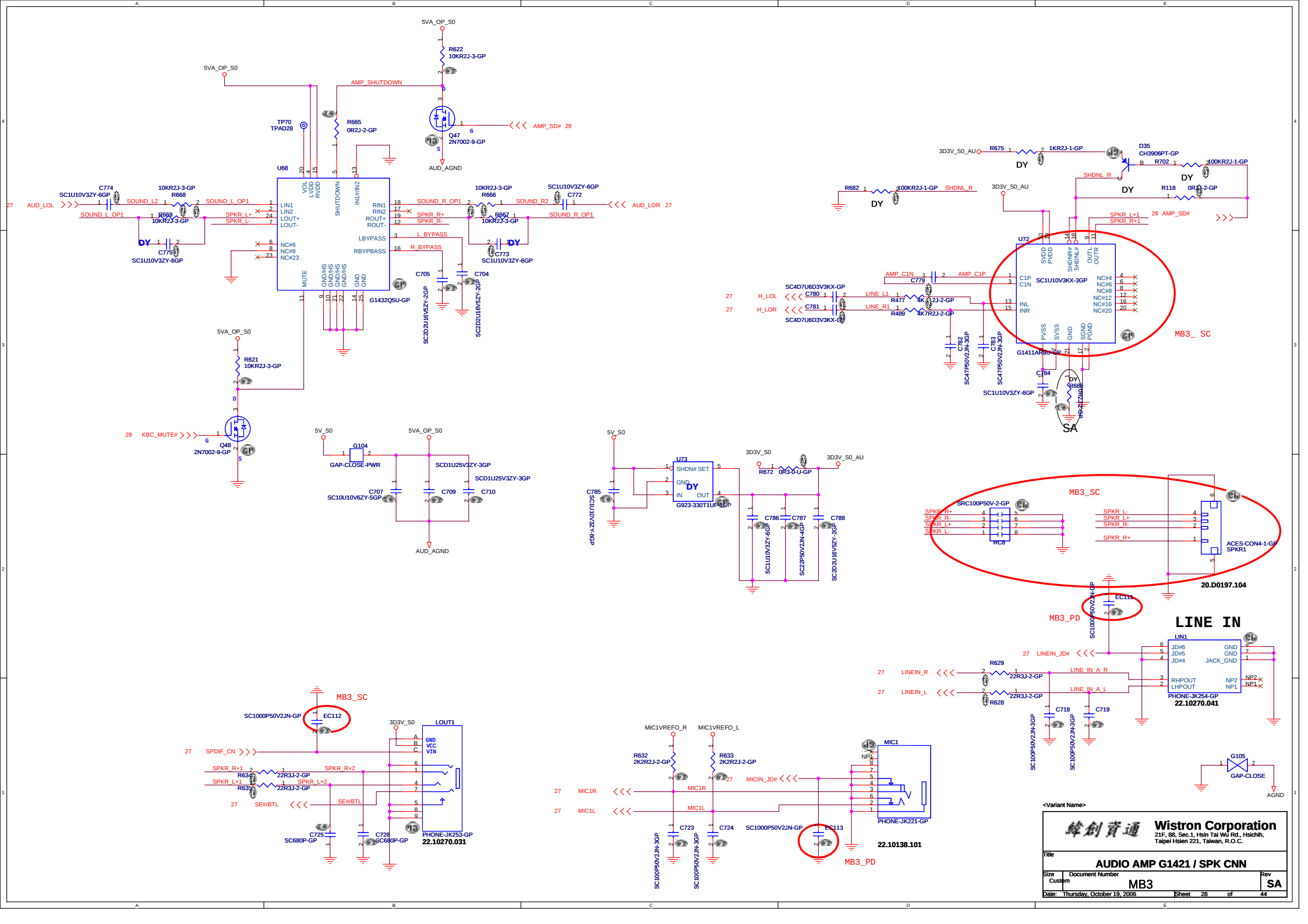


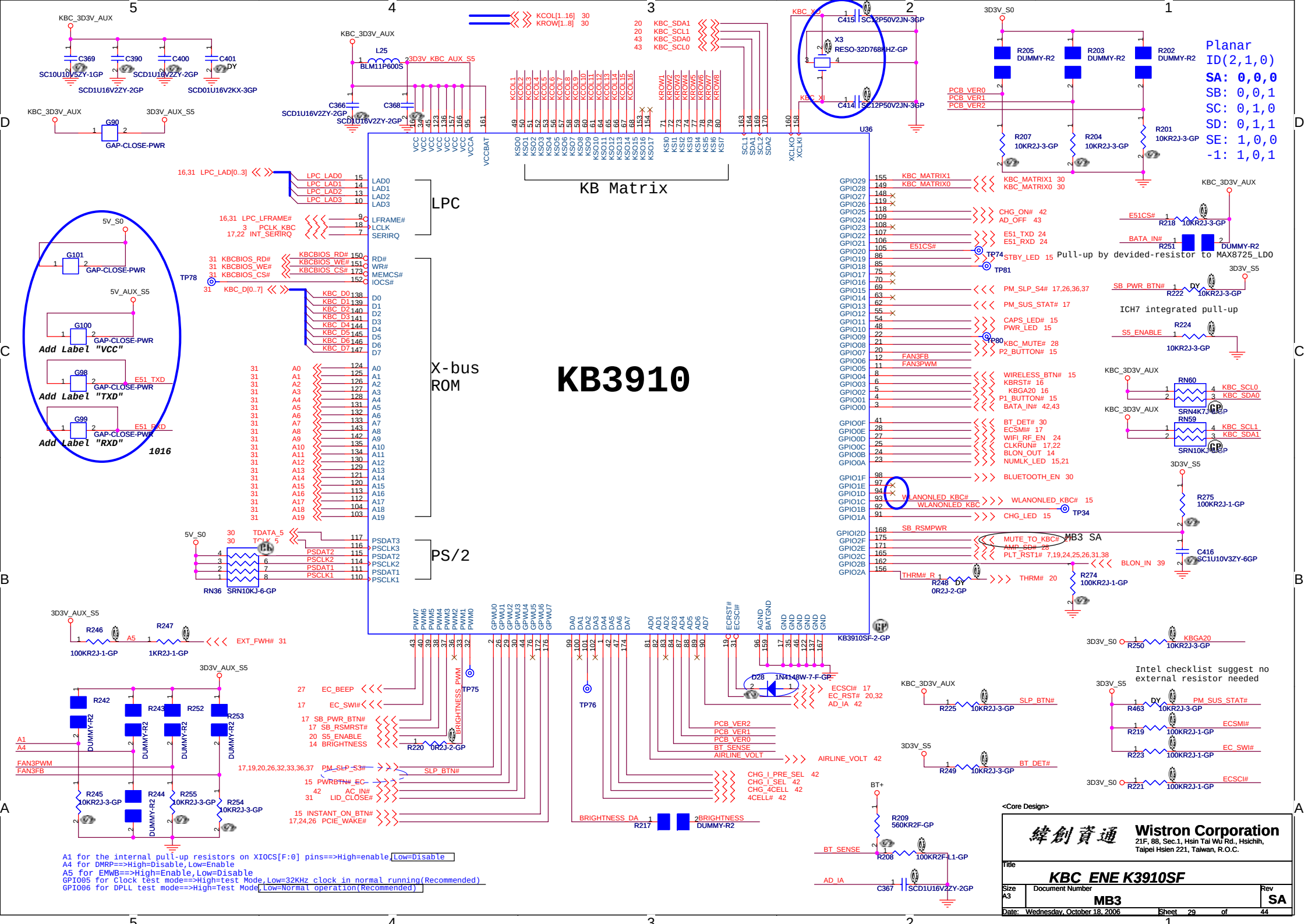
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card
Size: A3
Document Number: MB3
Rev: SA
Date: Wednesday, October 18, 2006
Sheet 26 of 44


5V_S0
DY
R599
0R5J-5-GP
5V_AUDIO_S0
C684
U66
SC22P50V2JN-1
SHDN#
GND
IN
SET
OUT
5VA_SET
R600
28K7R3F-GP
C686
SCD1U16V2ZY-2GP
MB3_SC
AUD_AGND
C685
SC1U10V3KX-3GP
MAX8863SEUK-GP
R602
10KR3F-L-GP
C690
SC10U10V6ZY-5GP
ACZ_RST#
ACZ_SYNC
ACZ_RST# 14,16
ACZ_SYNC 14,16
ACZ_BITCLK_AUD 16
17 ICH_SPKR
29 EC_BEEP
C687
SC1U10V3ZY-6GP
MCP_SPKR_C
R603
47KR2J-2-GP
AUD_BEEP
C688
AUD_PC_BEEP
SCD1U16V2ZY-2GP
KBC_BEEP_C
C691
R604
R605
4K7R2J-2-GP
C692
SC100P50V2JN-3GP
C689
SC22P50V3JN-GP
R606
10KR2J-3-GP
TP83 TPAD28
TP84 TPAD28
TP85 TPAD28
3D3V_S0
C693
SCD1U25V3ZY-3GP
C694
SC10U10V5ZY-1GP
C695
C696
C697
C698
SCD1U25V3ZY-3GP
JD_SENSE
R607
10KR2F-2-GP
LINEIN_JD# 28
R608
20KR2F-L-GP
MICIN_JD# 28
R662
5K1R2F-2-GP
SE#/BTL 28
MB3 SA
U67
DVDD1
DVDD2
AVDD1
AVDD2
PCBEEP
RESET#
SYNC
BIT-CLK
VAUX
LFE-OUT
CEN-OUT
SENSE_B
SENSE_A
LEF_OUT
AUD_CENOUT
SC4D7U6D3V3KX-GP
28 LINEIN_L
28 LINEIN_R
C319
C318
LINE_IN_L
LINE_IN_R
LINE1-L
LINE1-R
LINE2-L
LINE2-R
LINE1-VREFO
LINE2-VREFO
C193
SC2D2U10V3ZY-1GP
28 MIC1L
28 MIC1R
MIC_L
MIC_R
C307
MIC1-L
MIC1-R
MIC2-L
MIC2-R
MIC1VREFO_R
MIC1VREFO_L
MIC1-VREFO-R
MIC1-VREFO-L
MIC2-VREFO
SDATA-OUT
SDATA-IN
ACZ_SDATAOUT 14,16
AC97_DATIN
R609
22R2J-2-GP
ACZ_SDATAIN0 16
SPDIFO
SPDIFI/EAPD
EAPD_CODEC
TP88 TPAD28
SPDIF
0R3-0-U-GP
L44
SPDIF_CN
SPDIF_CN 28
EC105
SC470P50V2KX-3GP
EC106
SIDESURR-OUT-L
SIDESURR-OUT-R
AUDSURRR
AUDSURRL
TP87 TPAD28
TP86 TPAD28
SURR-OUT-L
SURR-OUT-R
AUD_LOL
AUD_LOR
AUD_LOL 28
AUD_LOR 28
FRONT-OUT-L
FRONT-OUT-R
H_LOL
H_LOR
H_LOL 28
H_LOR 28
MB3 SA
AVSS1
AVSS2
DVSS1
DVSS2
VREF
JDREF
PIN37_VREFO
GPIO0
GPIO1
CD-L
CD-R
CD-GND
ALC883-1-GP
CODECVREF
C700
SC10U6D3V5KX-1GP
C701
SCD1U25V3ZY-3GP
R611
20KR2F-L-GP
29 MUTE_TO_KBC#
CDAUD_GND
CDAUD_R
CDAUD_L
C699
CDAGND
C702
CDAUDR
C703
CDAUDL
SC1U10V3ZY-6GP
R610
R612
R613
4K7R2J-2-GP
CD_AGND 21
CD_AUDR 21
CD_AUDL 21
R614
R615
R616
150KR2J-GP
G109
GAP-CLOSE-PWR
G110
G103
G107
G108
MB3-SA
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC ALC883
Size
A3
Document Number
MB3
Rev
SA
Date: Friday, October 20, 2006
Sheet 27 of 44


5VA_OP_S0
R622
10KR2J-3-GP
AMP_SHUTDOWN
TP70
TPAD28
R665
0R2J-2-GP
Q47
2N7002-9-GP
AMP_SD# 29
AUD_AGND
U68
C774
SC1U10V3ZY-6GP
10KR2J-3-GP
R668
SOUND_L_OP1
R669
10KR2J-3-GP
DY
C775
SC1U10V3ZY-6GP
AUD_LOL
LIN1
LIN2
LOUT+
LOUT-
SPKR_L+
SPKR_L-
NC#6
NC#8
NC#23
MUTE
VOL
LVDD
RVDD
SHUTDOWN
IN1#/IN2
RIN1
RIN2
ROUT+
ROUT-
SPKR_R+
SPKR_R-
LBYPASS
RBYPASS
L_BYPASS
R_BYPASS
GND/HS
GND
G1432Q5U-GP
SOUND_R_OP1
R666
R667
C772
SC1U10V3ZY-6GP
SOUND_R2
AUD_LOR 27
C773
C705
C704
SC2D2U16V5ZY-2GP
R621
10KR2J-3-GP
Q48
2N7002-9-GP
29 KBC_MUTE#
G104
GAP-CLOSE-PWR
5V_S0
SCD1U25V3ZY-3GP
C707
SC10U10V6ZY-5GP
C709
C710
AUD_AGND
R675
1KR2J-1-GP
D35
CH3906PT-GP
R702
100KR2J-1-GP
R682
SHDNL_R
3D3V_S0_AU
R118
0R2J-2-GP
SPKR_L+1
SPKR_R+1
29 AMP_SD#
U72
SVDD
PVDD
SHDNR#
SHDNL#
OUTL
OUTR
SC1U10V3KX-3GP
AMP_C1N
AMP_C1P
C779
H_LOL
H_LOR
C780
C781
SC4D7U6D3V3KX-GP
LINE_L1
LINE_R1
R477
R489
4K7R2J-2-GP
C782
C783
SC47P50V2JN-3GP
PVSS
SVSS
GND
SGND
PGND
G1411AR3U-GP
C784
R688
0R2J-2-GP
SC1U10V3ZY-6GP
MB3_ SC
SA
U73
SHDN# SET
IN
OUT
G923-330T1UF-GP
R672
0R3-0-U-GP
C785
C786
C787
C788
SC1U10V3ZY-6GP
SC22P50V2JN-4GP
SC2D2U16V5ZY-2GP
MB3_SC
SRC100P50V-2-GP
RC8
SPKR_R+
SPKR_R-
SPKR_L+
SPKR_L-
ACES-CON4-1-GP
SPKR1
20.D0197.104
EC111
SC100P50V2JN-4GP
MB3_PD
LINE IN
LIN1
JD#6
JD#5
JD#4
GND
JACK_GND
RHPOUT
LHPOUT
NP2
NP1
PHONE-JK254-GP
22.10270.041
27 LINEIN_JD#
27 LINEIN_R
27 LINEIN_L
R629
R628
22R3J-2-GP
LINE_IN_A_R
LINE_IN_A_L
C718
C719
SC100P50V2JN-3GP
G105
GAP-CLOSE
AGND
MB3_SC
SC1000P50V2JN-GP
EC112
3D3V_S0
LOUT1
GND
VCC
VIN
27 SPDIF_CN
SPKR_R+1
SPKR_L+1
R634
R635
22R3J-2-GP
SPKR_R+2
SPKR_L+2
27 SE#/BTL
SE#/BTL
C725
SC680P-GP
C726
SC680P-GP
PHONE-JK253-GP
22.10270.031
MIC1VREFO_R
MIC1VREFO_L
R632
R633
2K2R2J-2-GP
MIC1
NP1
NP2
MICIN_JD#
27 MIC1R
27 MIC1L
C723
C724
SC1000P50V2JN-GP
EC113
PHONE-JK221-GP
22.10138.101
MB3_PD
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO AMP G1421 / SPK CNN
Size
Custom
Document Number
MB3
Rev
SA
Date: Thursday, October 19, 2006
Sheet 28 of 44


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U36
KB3910SF-2-GP
Planar ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
SE: 1,0,0
-1: 1,0,1
Add Label "VCC"
Add Label "TXD"
Add Label "RXD"
1016
MB3 SA
Pull-up by devided-resistor to MAX8725_LDO
ICH7 integrated pull-up
Intel checklist suggest no external resistor needed
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC_ENE K3910SF
MB3
SA
Wednesday, October 18, 2006
29
44

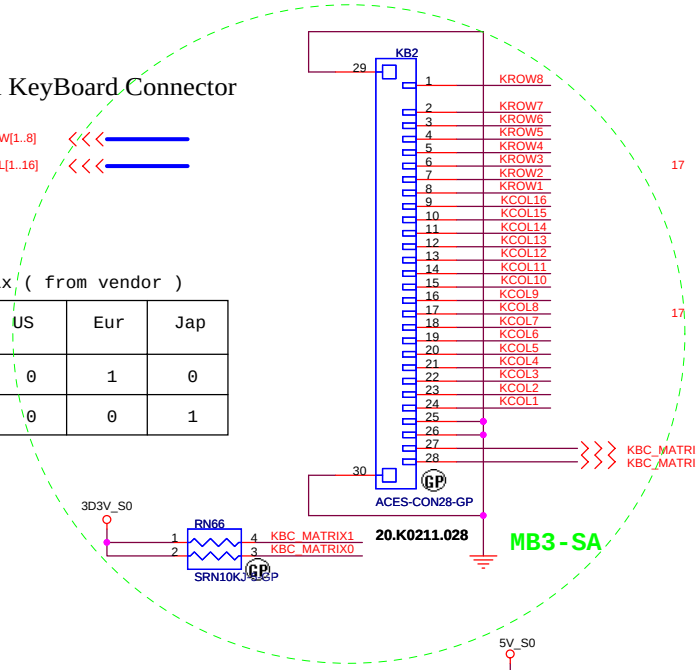
Internal KeyBoard Connector

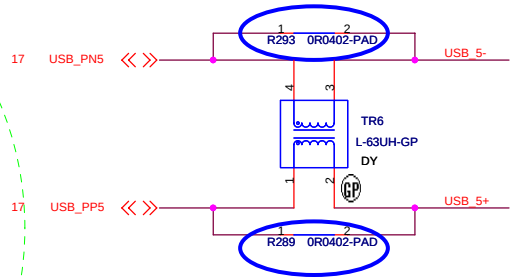
Internal KeyBoard Connector

29 KROW[1..8]
29 KCOL[1..16]

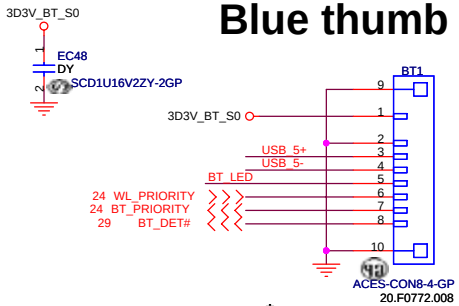
Keyboard matrix (from vendor)

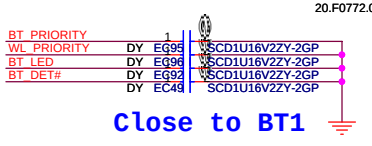
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



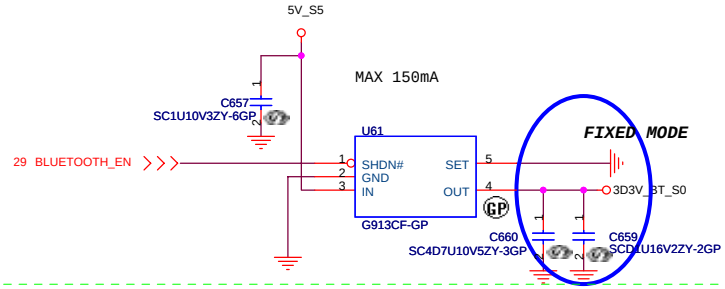


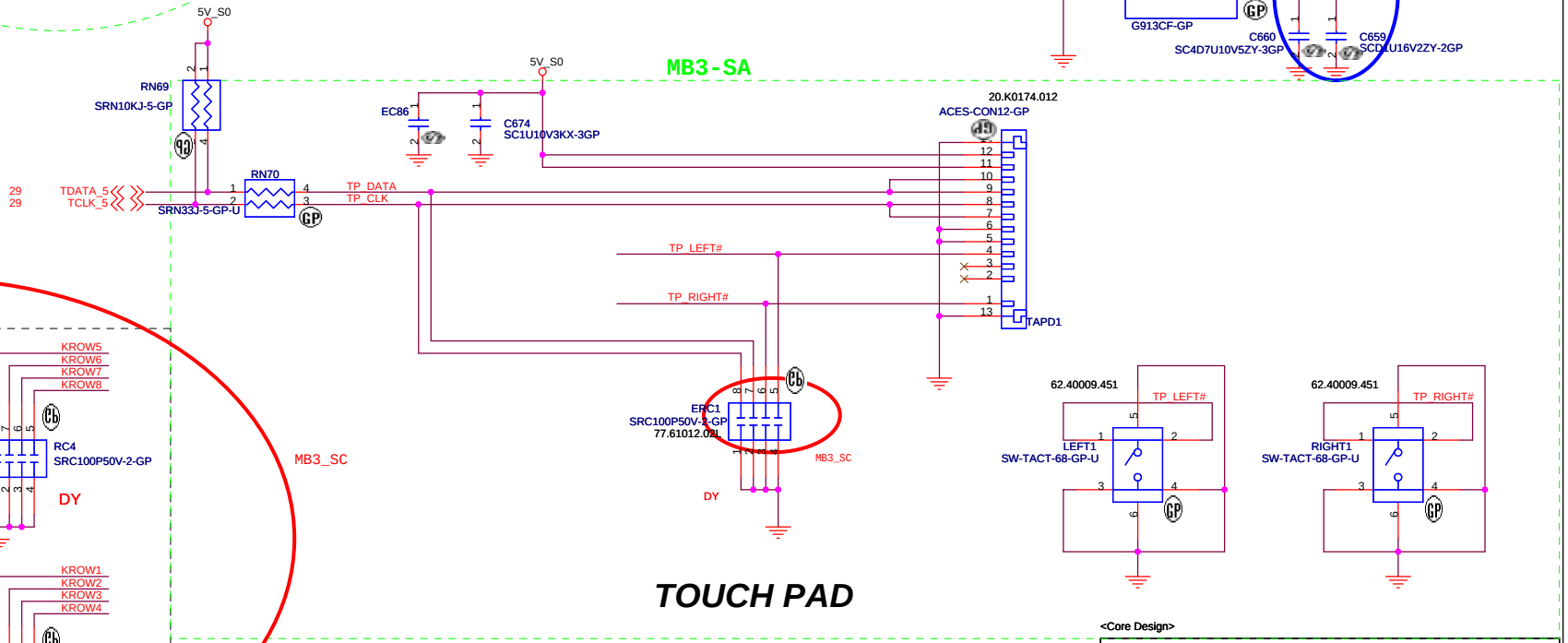
Blue thumb

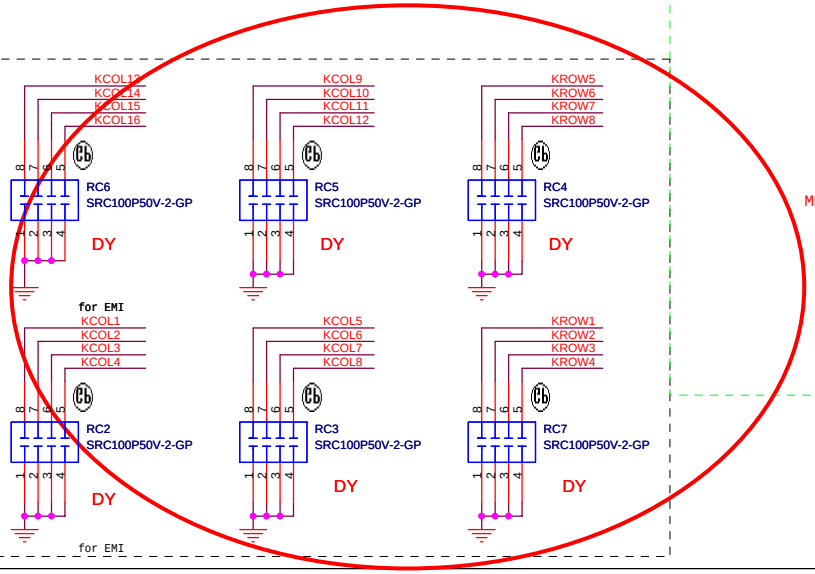




Close to BT1







<Core Design>

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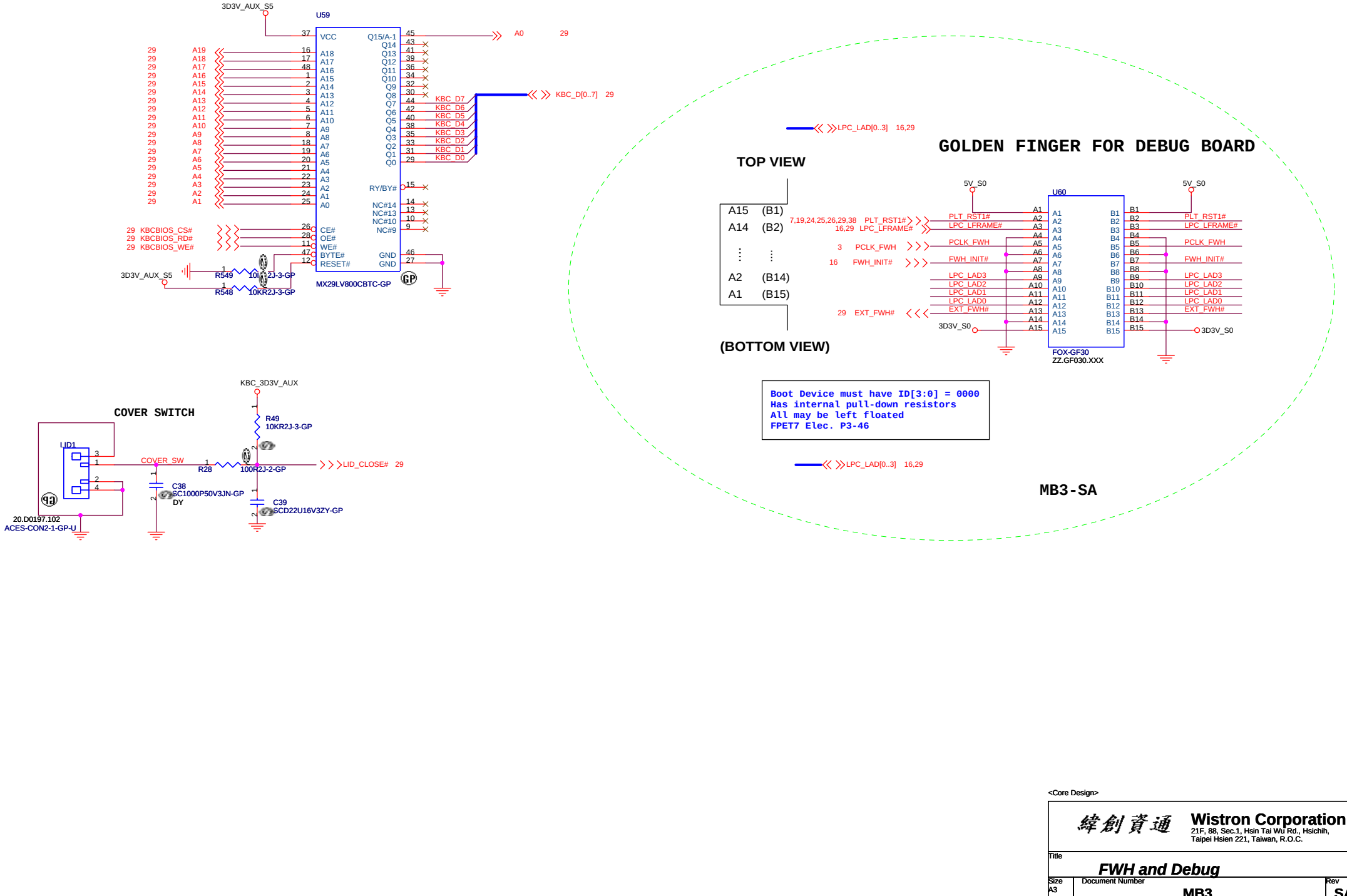
Taipei Hsien 221, Taiwan, R.O.C.

Title: **KeyBoard-CONN**

Size	Document Number	Rev
A3	MB3	SA

Date: Friday, October 20, 2006 Sheet 30 of 44



<Core Design>

Wistron Corporation
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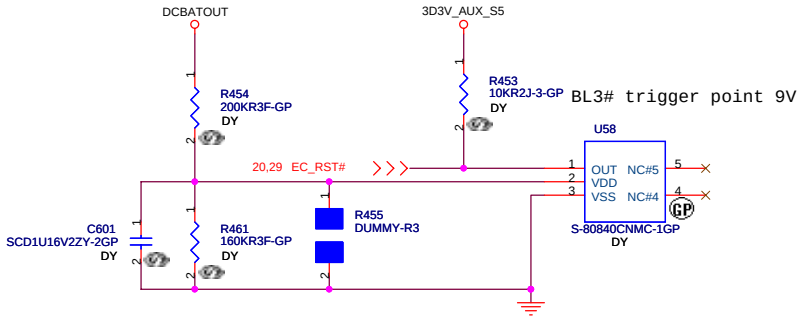
Taipei Hsien 221, Taiwan, R.O.C.

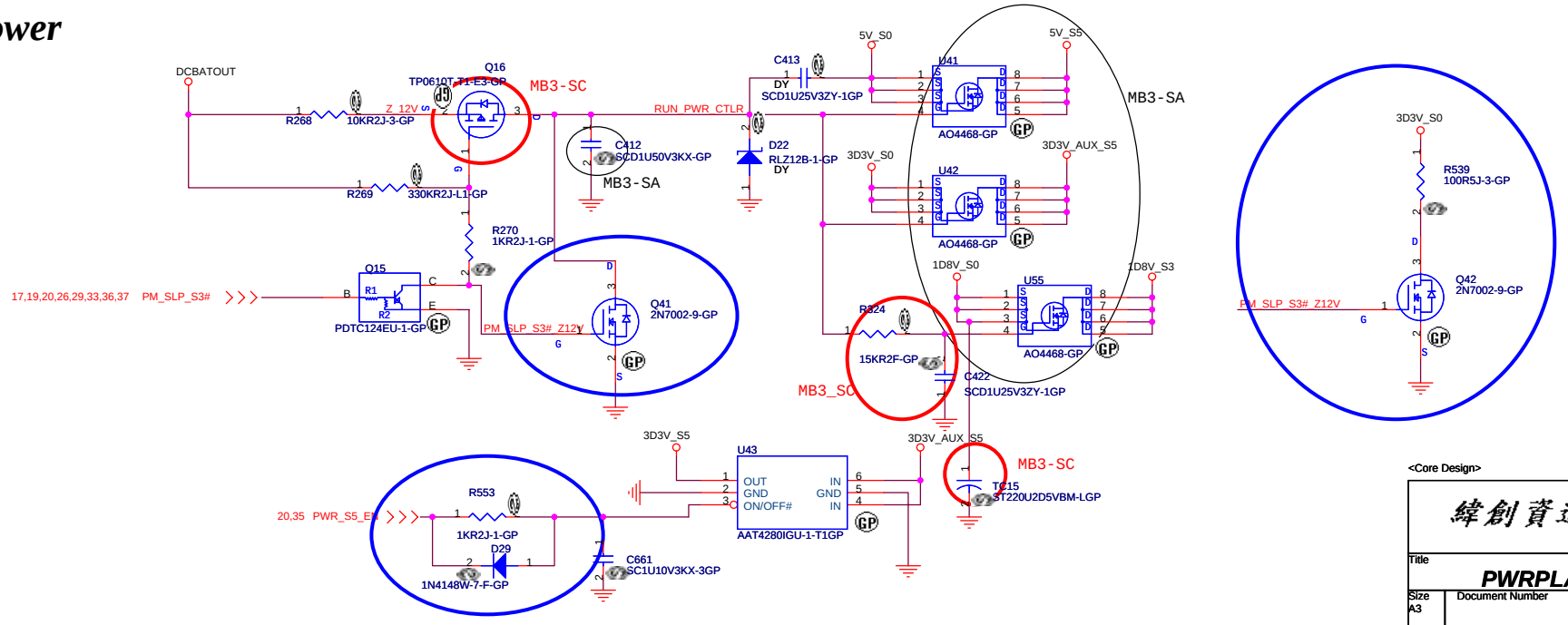
Title: FWH and Debug

Size	Document Number	Rev
A3	MB3	SA

Date: Thursday, August 24, 2006 Sheet 31 of 44



Run Power



<Core Design>

Wistron Corporation
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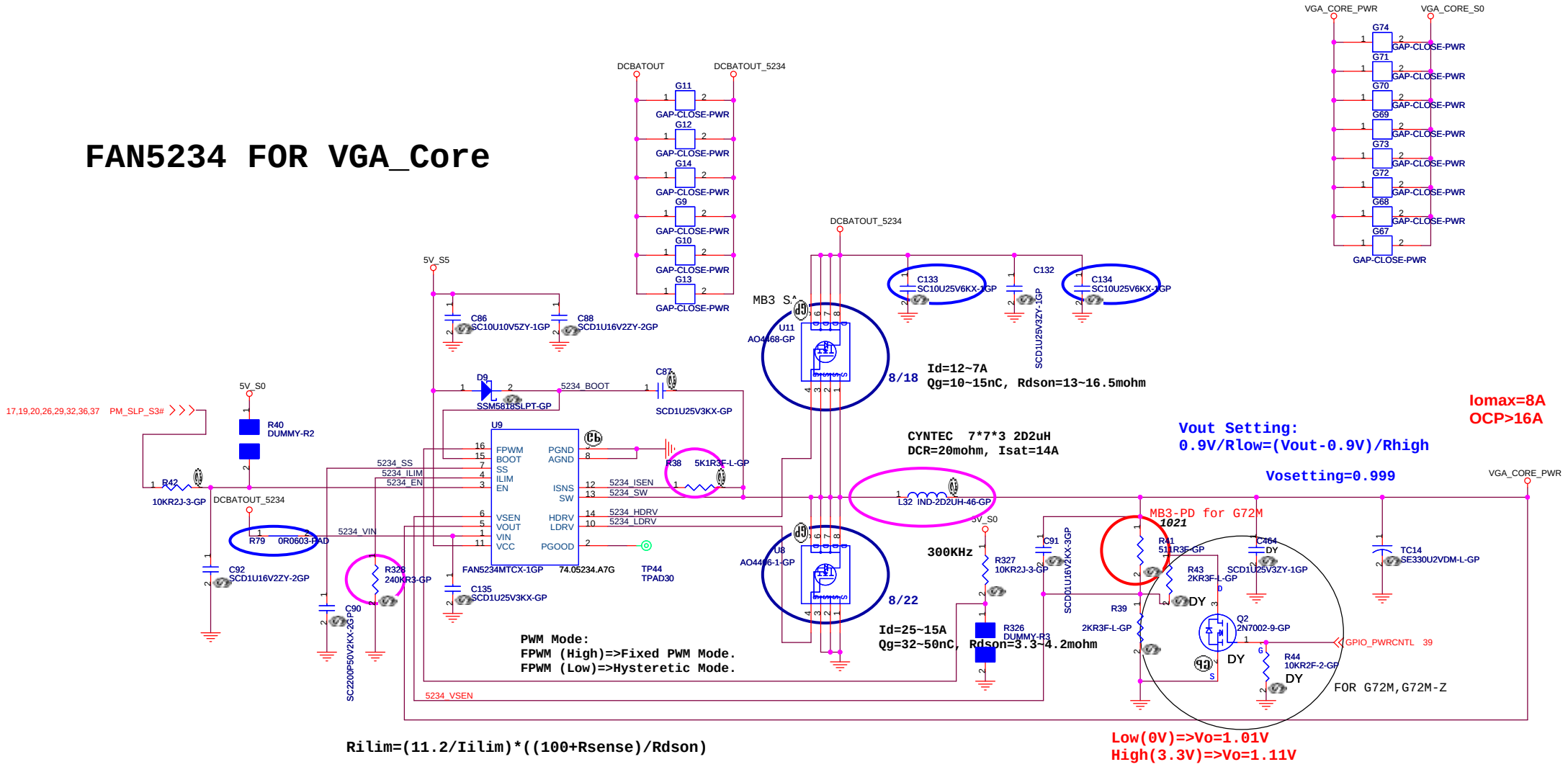
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PWRPLANE&RESETLOGIC***

Size	Document Number	Rev
A3	MB3	SA

Date: Wednesday, October 18, 2006 Sheet 32 of 44

FAN5234 FOR VGA_Core



<Core Design>

緯創資通 Wistron Corporation
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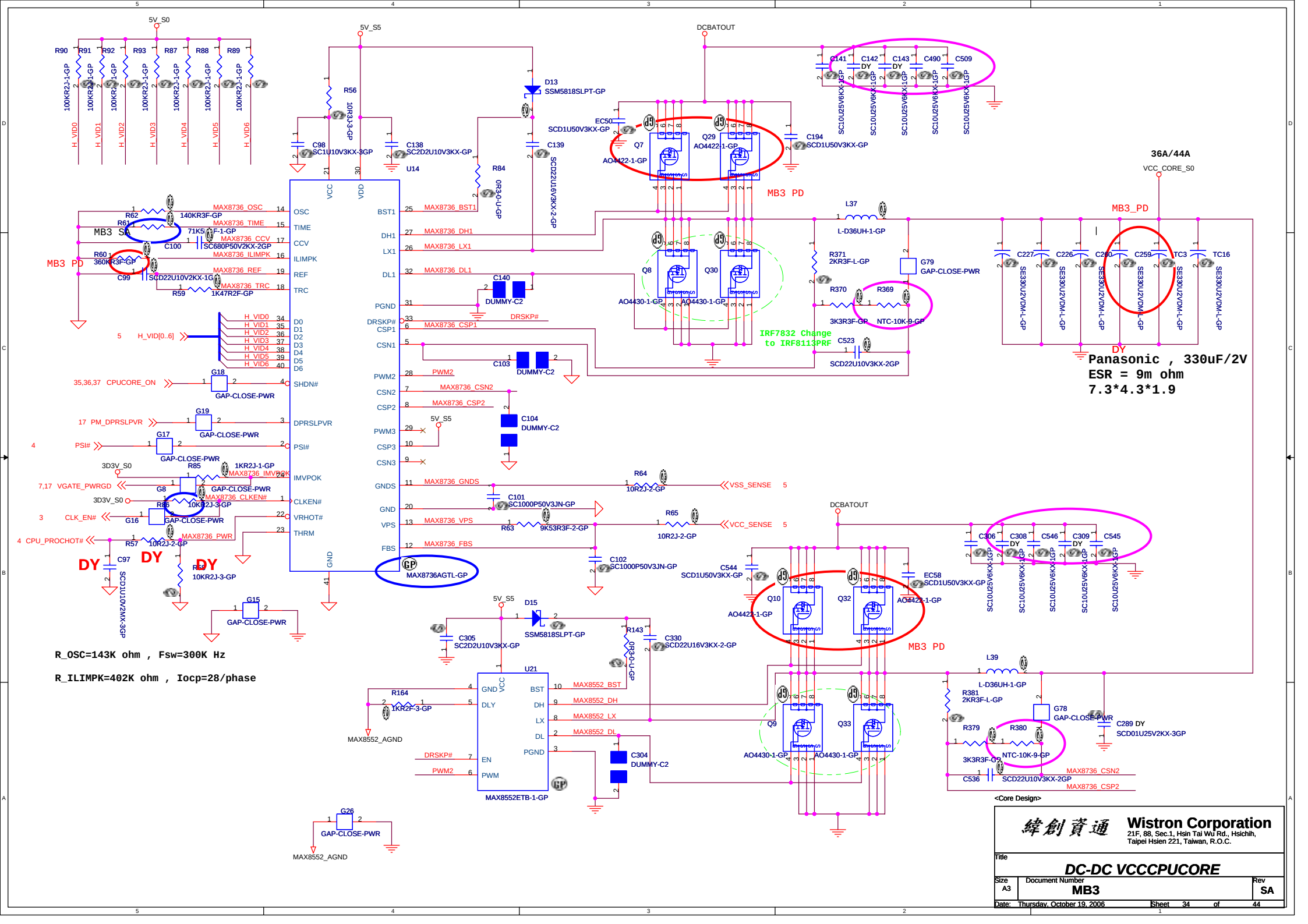
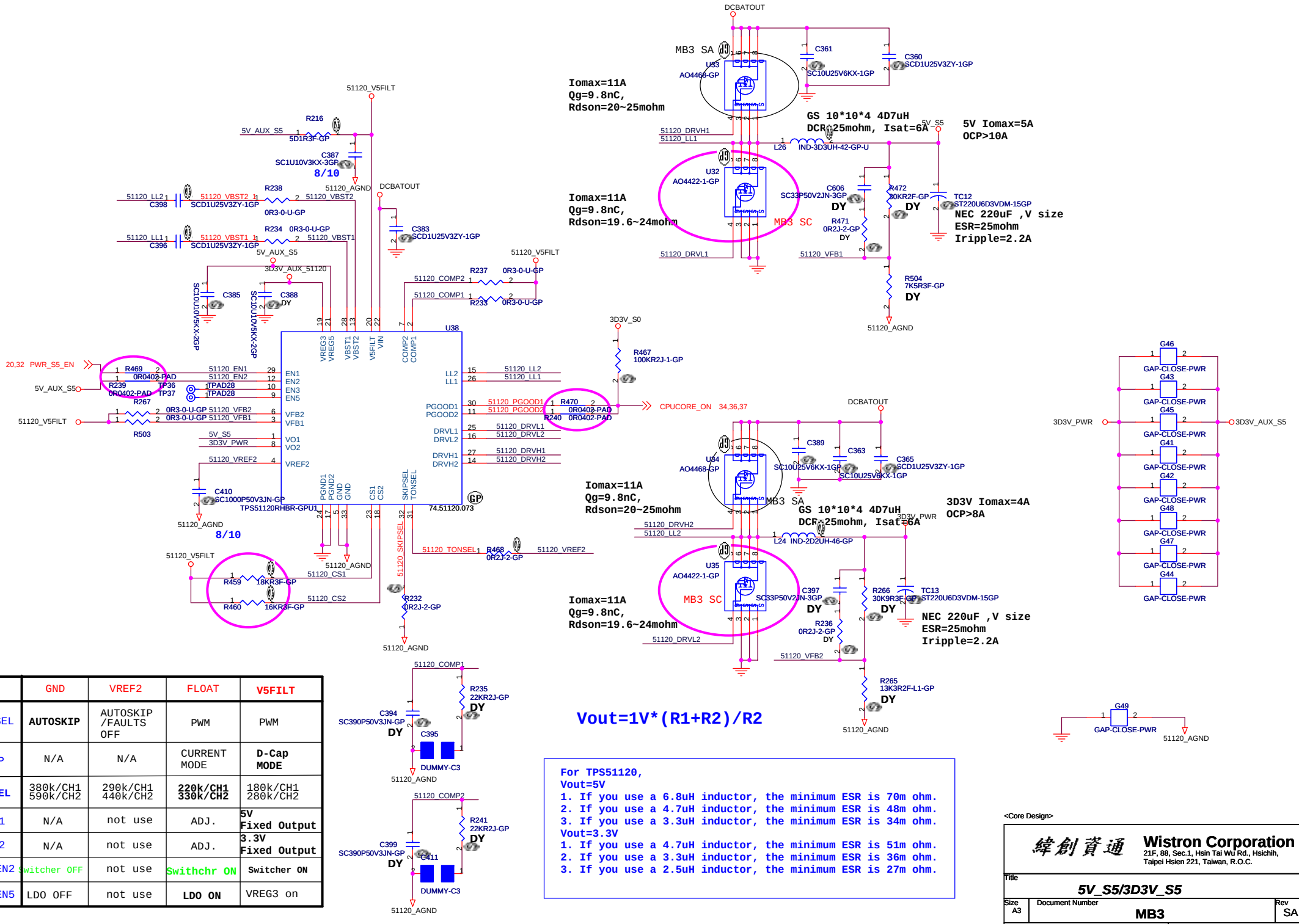
Title	VGA CORE 1V	
Size A3	Document Number MB3	Rev SA
Date: Wednesday, October 25, 2006	Sheet 33 of 44	


5V_S0
5V_S5
DCBATOUT
MB3 PD
MB3_PD
36A/44A
VCC_CORE_S0
MB3 SA
DY
Panasonic , 330uF/2V
ESR = 9m ohm
7.3*4.3*1.9
IRF7832 Change
to IRF8113PRF
R_OSC=143K ohm , Fsw=300K Hz
R_ILIMPK=402K ohm , Iocp=28/phase
MAX8736AGTL-GP
MAX8552ETB-1-GP
MAX8552_AGND
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC-DC VCCCPUCORE
Size A3
Document Number MB3
Rev SA
Date: Thursday, October 19, 2006
Sheet 34 of 44



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

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Title: 5V_S5/3D3V_S5

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Date: Wednesday, October 18, 2006 Sheet 35 of 44

Iocp=7.0 2 = 14A*
Rds,on=17m ohm
*Vcs1=Iocp*Rds,on=238mV*
VILIM=Vcs1/0.1=2.38V

*Iocp=7.0*2 = 14A*
Rds,on=17m ohm
*Vcs2=Iocp*Rds,on=28mV*
VILIM2=Vcs2/0.1=2.38V

1D8V / 7.0A
OCP>=14A

1D05V_S0/7A
OCP>=14A

1D8V_S3 1D8V_PWR
G82 GAP-CLOSE-PWR
G81 GAP-CLOSE-PWR
G85 GAP-CLOSE-PWR
G84 GAP-CLOSE-PWR
G83 GAP-CLOSE-PWR
G86 GAP-CLOSE-PWR
G80 GAP-CLOSE-PWR
G87 GAP-CLOSE-PWR

5V_S5
C342 SCD1U10V2MX-3GP
C341 SC1U10V3KX-3GP
DCBATOUT
C356 SCD1U10V2MX-3GP
C344 SC1U25V5ZY-4GP
8/18

D17 BAW56-7-F-GP
R183 10R3J-3-GP
MAX8743_BST2

DCBATOUT
C364 SC10U25V6KX-1GP
EC80 SCD1U25V3ZY-1GP
MB3 SA
U30 AO4468-GP
8/18
MAX8743_BST1L
R193 0R3-0-U-GP
C354 SCD1U25V3ZY-1GP

MAX8743_VCC
R410 100KR2F-L1-GP
C339 SC1U10V3KX-3GP
R409 90K9R3F-GP
R415 100KR2F-L1-GP
MAX8743_ILIM2
R416 90K9R3F-GP
R182 0R3-0-U-GP
C340 SCD1U25V3ZY-1GP

U25 MAX8743EEI-1-GP
UVP VCC VDD V+ ILIM2 BST2
ILIM1 BST1 DH1 LX1 DL1 CS1
OUT1 FB1 ON1 TON REF SKIP#
DH2 LX2 DL2 CS2 OUT2 FB2 ON2 PGOOD OVP GND

NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

MAX8743_ILIM1
MAX8743_BST1R
MAX8743_DH1
MAX8743_LX1
MAX8743_DL1
MAX8743_BST2R
MAX8743_DH2
MAX8743_LX2
MAX8743_DL2

L23 IND-2D2UH-46-GP
TC10 SE220U2D5VDM-3GP
DY
C338 SCD1U25V3ZY-1GP
U31 FDS6690DS-GP
Panasonic 220uF/2D5V
ESR=15m ohm
Iripple=2.7 A

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

MAX8743_ON1
MAX8743_TON
MAX8743_VREF
MAX8743_ON2
MAX8743_PGOOD
C548 SC1U10V3KX-3GP 74.08743.A79

R195 8K2R3F-GP
MAX8743_FB1
Voutsetting=1.860V
R196 9K76R3F-GP
MB3_SC

5V_S5
DY
R412 0R2J-2-GP
8/18
MAX8743_VREF
R413 DUMMY-R2
R411 DUMMY-R2

17,26,29,37 PM_SLP_S4#
R418 0R2J-2-GP MAX8743_ON1
17,19,20,26,29,32,33,37 PM_SLP_S3#
R417 0R2J-2-GP MAX8743_ON2

Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

17,26,29,37 PM_SLP_S4#
R185 220KR2J-L2-GP
17,19,20,26,29,32,33,37 PM_SLP_S3#
R262 220KR2J-L2-GP
DY
MAX8743_SKIP#
C343 SC1000P50V3JN-GP
R184 0R2J-2-GP
DY

DCBATOUT
U29 AO4468-GP
MB3 SA
EC83 SCD1U25V3ZY-1GP
C362 SC10U25V6KX-1GP
C353 SC10U25V6KX-1GP
NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5
8/18

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

1D05V_PWR 1D05V_S0
G34 GAP-CLOSE-PWR
G31 GAP-CLOSE-PWR
G30 GAP-CLOSE-PWR
G29 GAP-CLOSE-PWR
G33 GAP-CLOSE-PWR
G32 GAP-CLOSE-PWR
G27 GAP-CLOSE-PWR
G28 GAP-CLOSE-PWR

L22 IND-2D2UH-46-GP
U28 FDS6690DS-GP
TC9 SE220U2VDM-8GP
C337 DY SCD1U25V3ZY-1GP
Panasonic 220uF/2V
ESR=15m ohm
Iripple=2.7 A

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

MAX8743_FB2
Vout=Vfb*(1+(R1/R2))
Where Vfb=1.0V,R2=10Kohm

R160 5K11R3F-1-GP
R159 100KR3F-GP
Voutsetting=1.0511V

R414 0R0402-PAD CPUCORE_ON 34,35,37

<Core Design>

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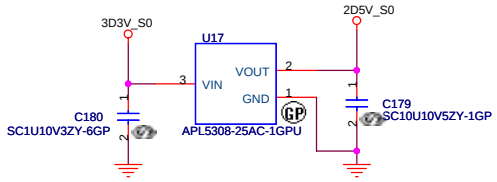
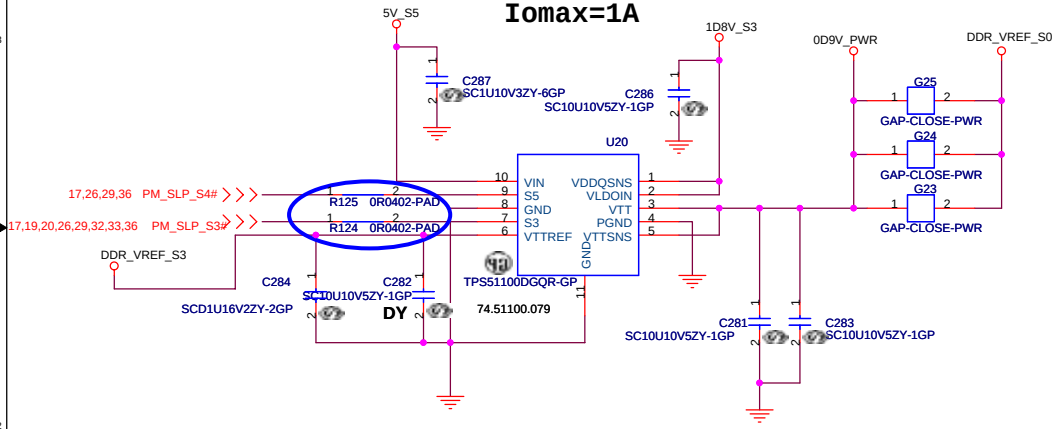
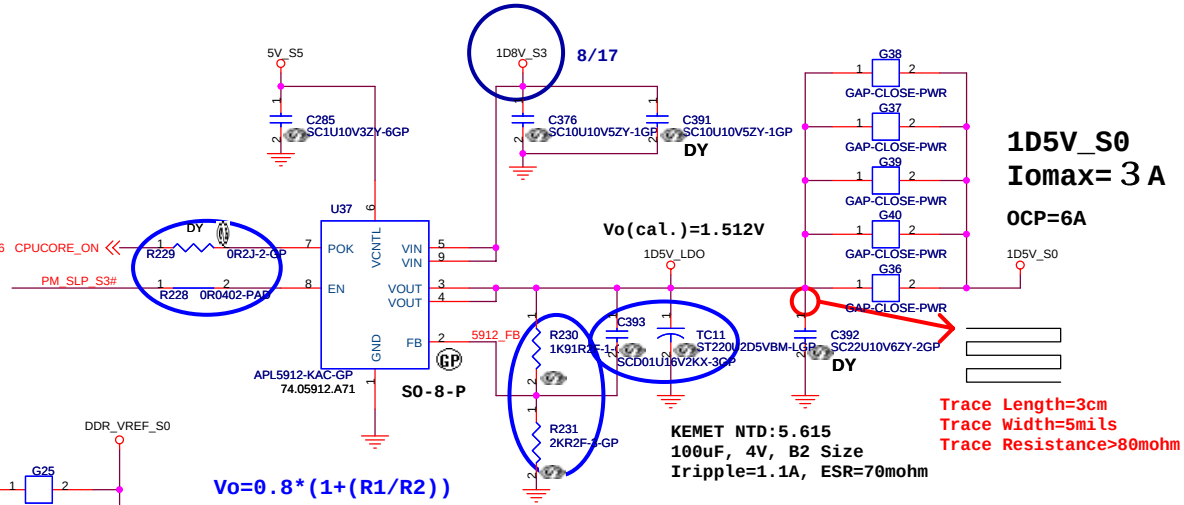
Title: *1D8V_S3/1D5V_S0*
Size: A3 | Document Number: MB3 | Rev: SA
Date: Wednesday, October 18, 2006 | Sheet 36 of 44

2D5V_S0
Iomax=300mA



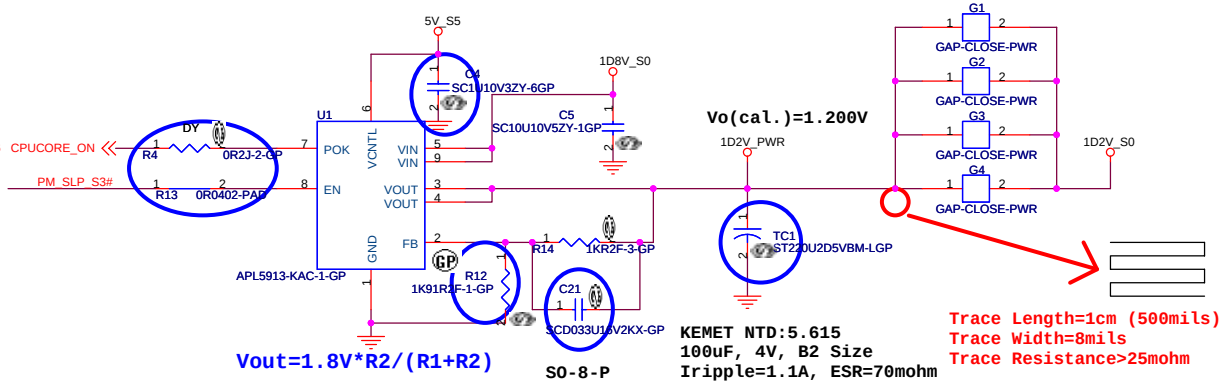
0D9V
Iomax=1A





1D5V_S0
Iomax= 3 A
OCP=6A

1D2V_S0
Iomax=3A



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V_LDO/1D2V_LDO/1D5V_LDO/2D5V_LDO

Size	Document Number	Rev
A3	MB3	SA

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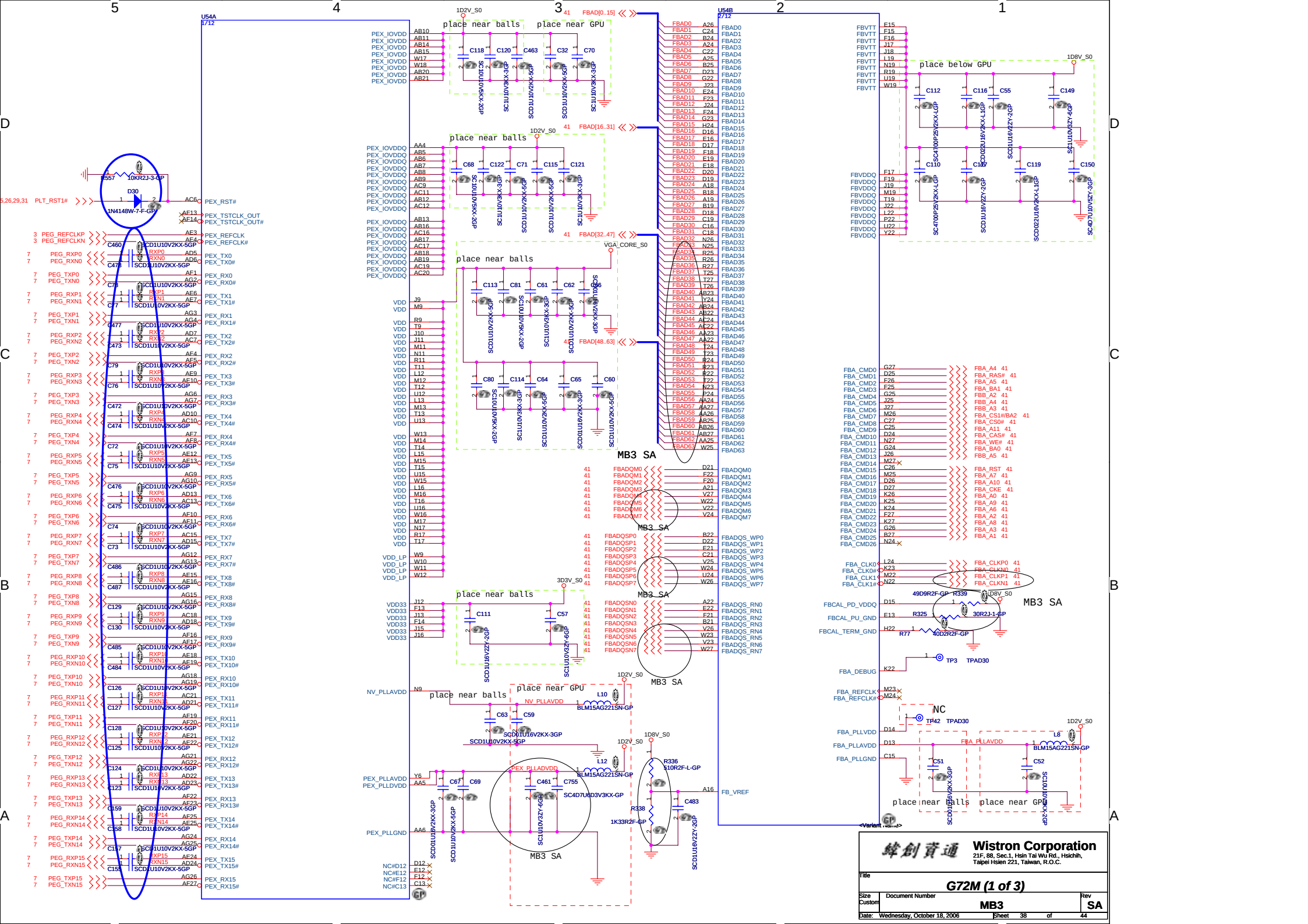
U54A
1/12
U54B
2/12
place near balls
place near GPU
place below GPU
MB3 SA
NC
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
G72M (1 of 3)
Document Number
MB3
Rev
SA
Wednesday, October 18, 2006
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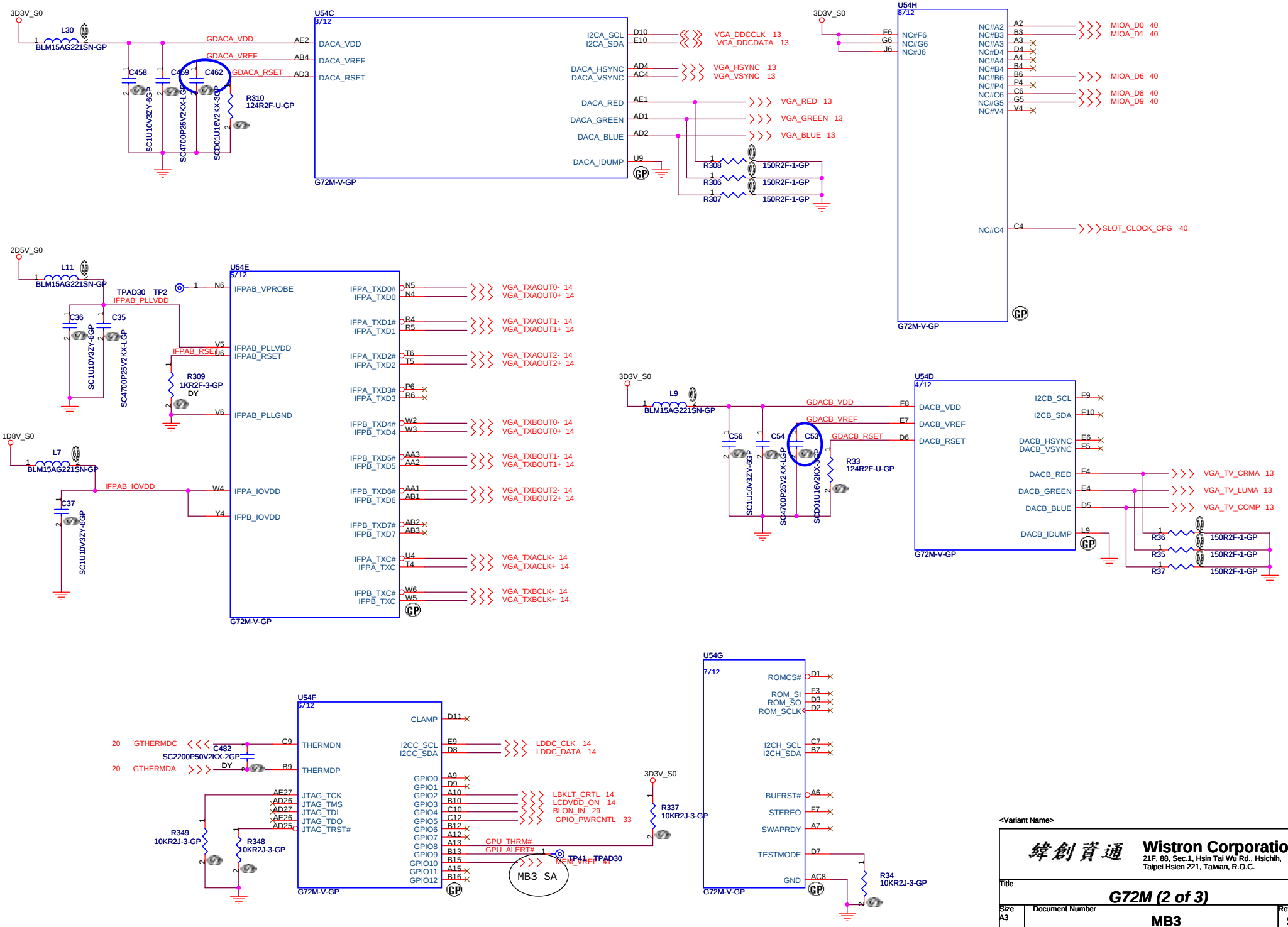

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M (2 of 3)

Size	Document Number	Rev
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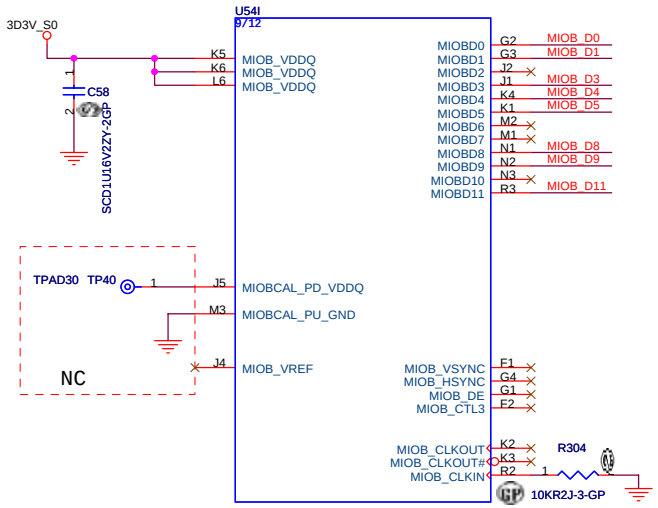
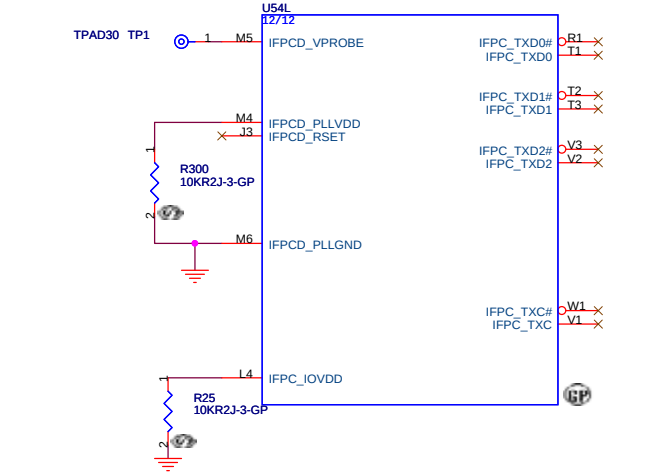
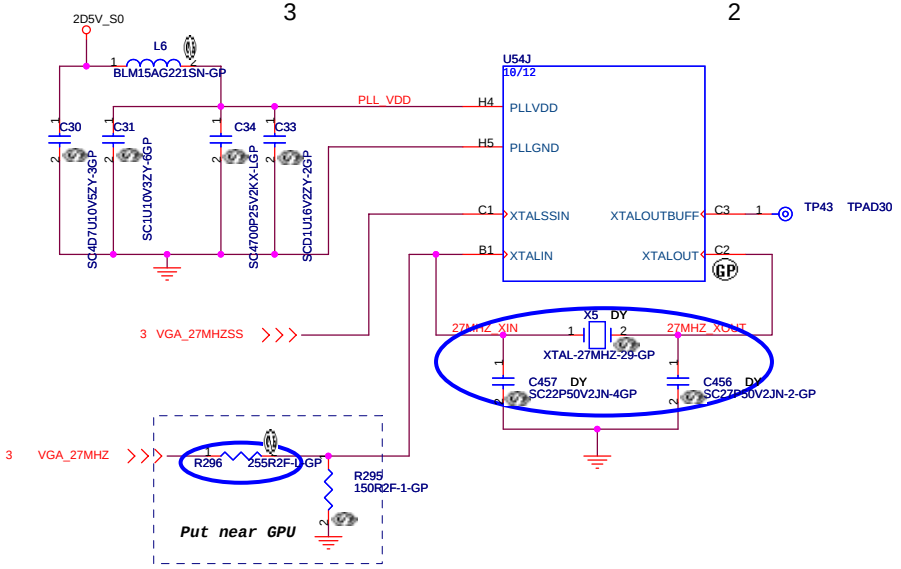
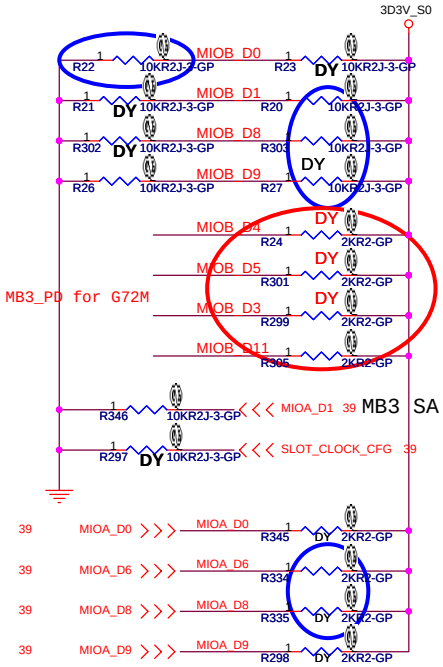


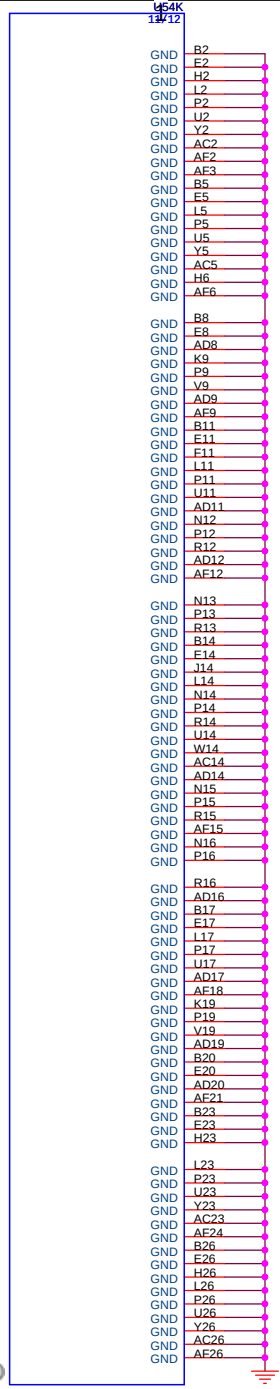






1 means 1 pic,0 means 2 pic

Bit	Signal	Values	
MIOB_D0:	RAM_CFG_0	GDDR3 8Mx32 64bit	
MIOB_D1:	RAM_CFG_1	1101	Infineon
MIOB_D8:	RAM_CFG_2	1110	Hynix
MIOB_D9:	RAM_CFG_3	1111	Samsung
MIOB_D4:	PCI_DEVID_0		
MIOB_D5:	PCI_DEVID_1	G72M	1000
MIOB_D3:	PCI_DEVID_2	G72M-V	0111
MIOB_D11:	PCI_DEVID_3	G72M-Z	0110
MIOA_D1:	SUB_VENDOR	0 SYSTEM BIOS 1 ADAPTER BIOS	(DEFAULT)
MIOA_D0:	PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED	(DEFAULT)
MIOA_D6:	3GIO_PADCFG_LUT_ADDR[0]	0 DESKTOP 1 MOBILE	(DEFAULT)
MIOA_D8:	3GIO_PADCFG_LUT_ADDR[1]		
MIOA_D9:	3GIO_PADCFG_LUT_ADDR[2]		



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: G72M (3 of 3)

Size	Document Number	Rev
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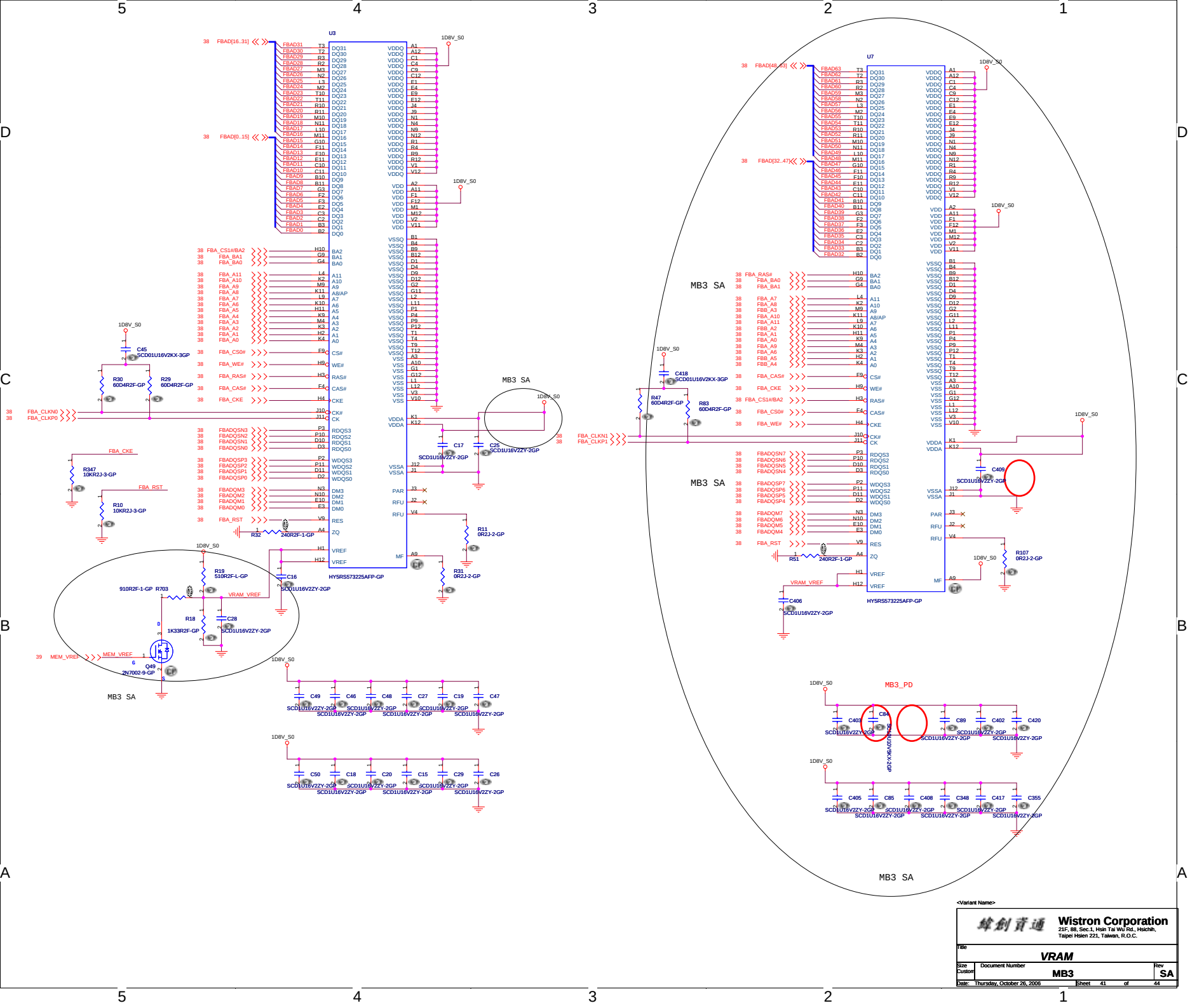
Date: Wednesday, October 25, 2006 Sheet 40 of 44



Wistron Corporation
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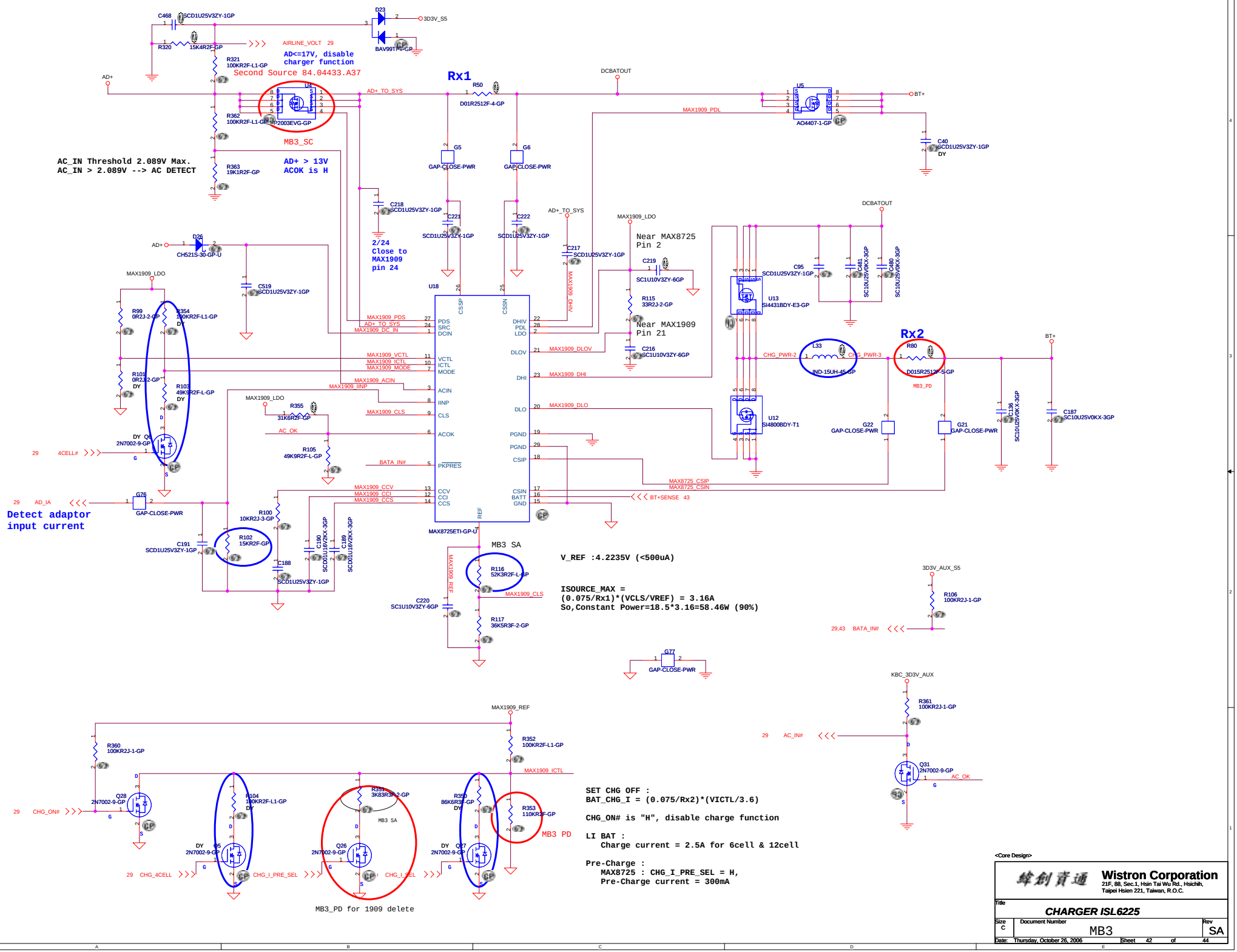
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: VRAM

Size	Document Number	Rev
Custom	MB3	SA

Date: Thursday, October 26, 2006 Sheet 41 of 44


AIRLINE_VOLT 29
AD<=17V, disable charger function
Second Source 84.04433.A37
Rx1
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
MB3_SC
AD+ > 13V
ACOK is H
2/24 Close to MAX1909 pin 24
Near MAX8725 Pin 2
Near MAX1909 Pin 21
Rx2
MB3_PD
Detect adaptor input current
MB3 SA
V_REF :4.2235V (<500uA)
ISOURCE_MAX =
(0.075/Rx1)*(VCLS/VREF) = 3.16A
So,Constant Power=18.5*3.16=58.46W (90%)
SET CHG OFF :
BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6)
CHG_ON# is "H", disable charge function
LI BAT :
Charge current = 2.5A for 6cell & 12cell
Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA
MB3_PD for 1909 delete
MAX8725ETI-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER ISL6225
Document Number MB3
Rev SA
Date: Thursday, October 26, 2006
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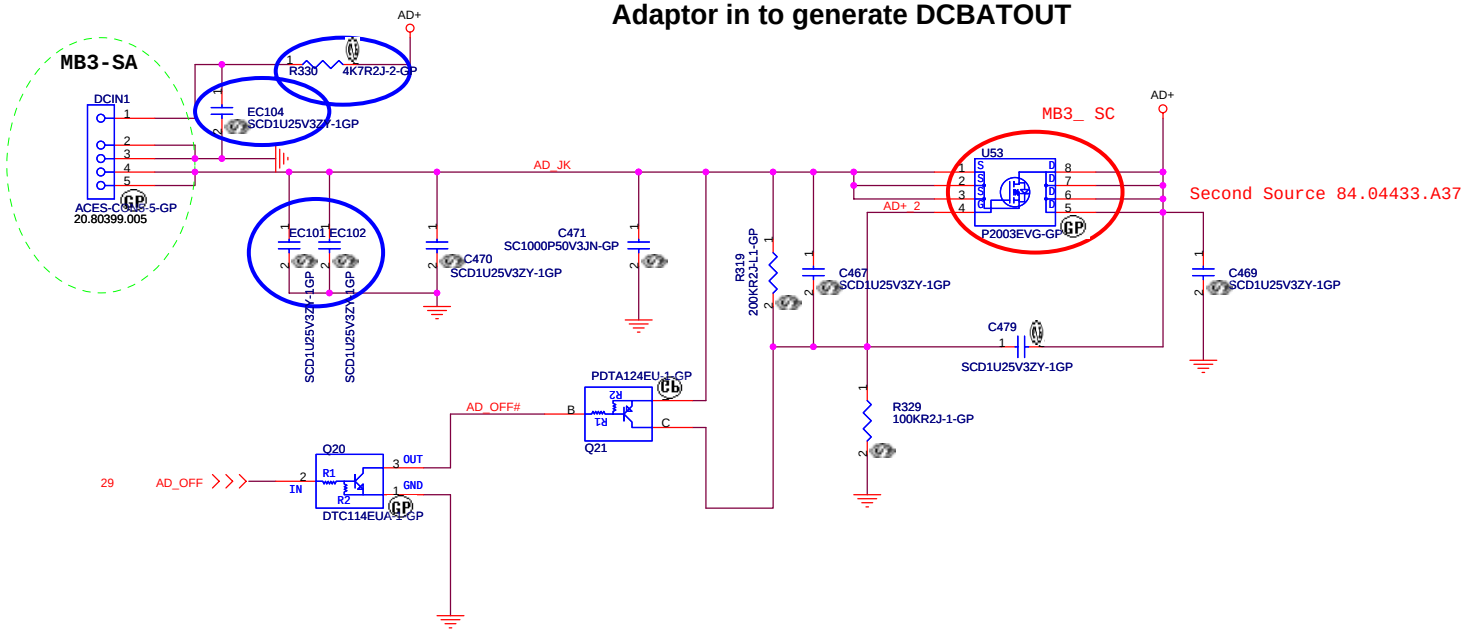
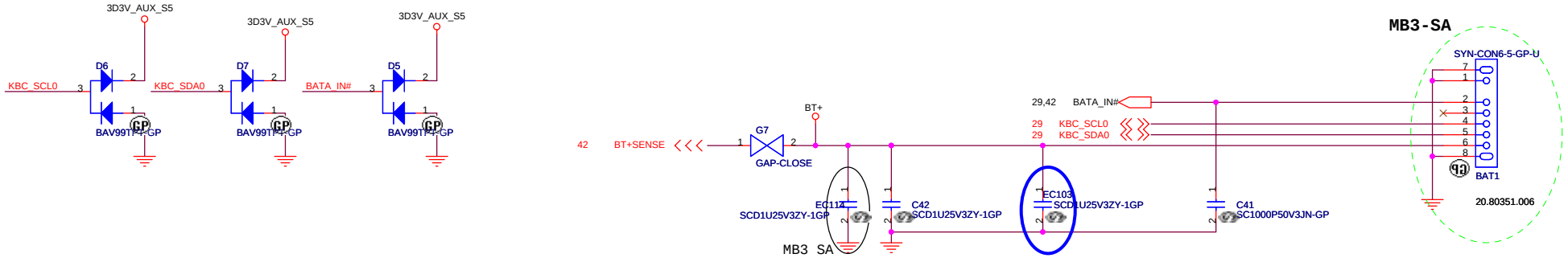
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

Size	Document Number	Rev
A3	MB3	SE

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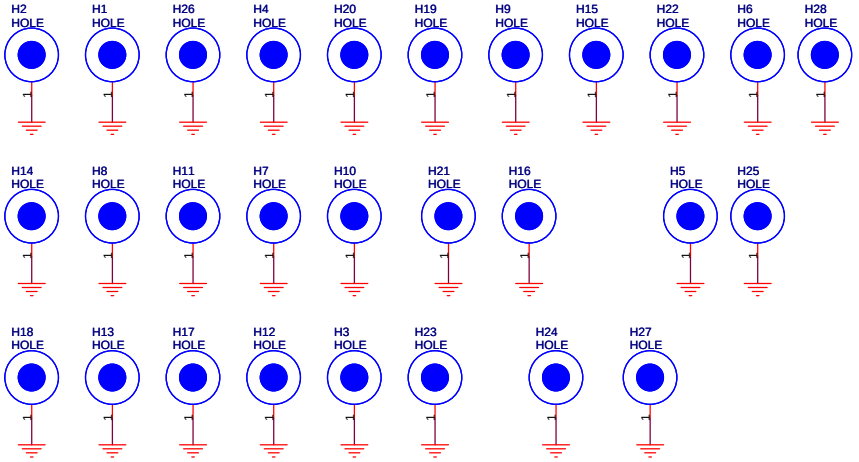
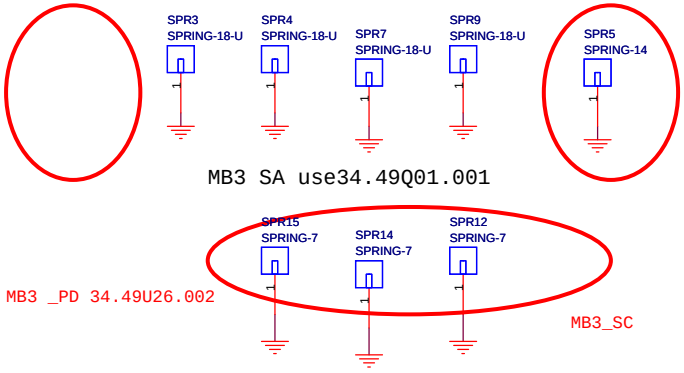
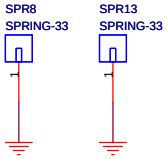


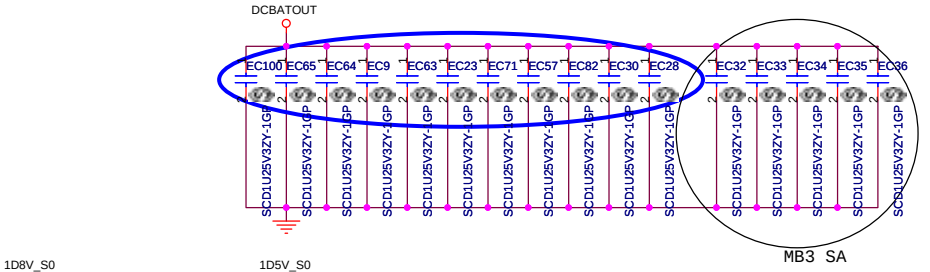


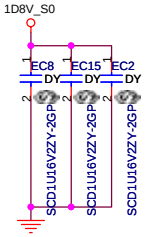


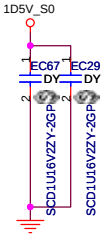
MB3 SA use34.4B312.001

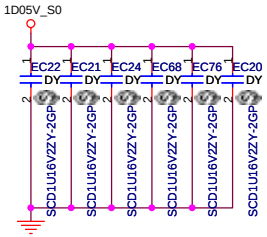
all of the parts followed MB2.

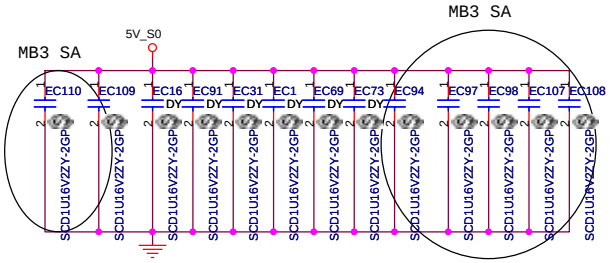
check them later

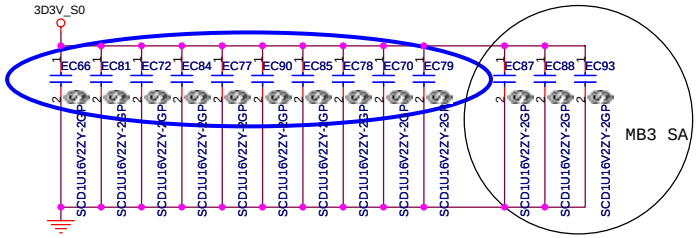












<Core Design>

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