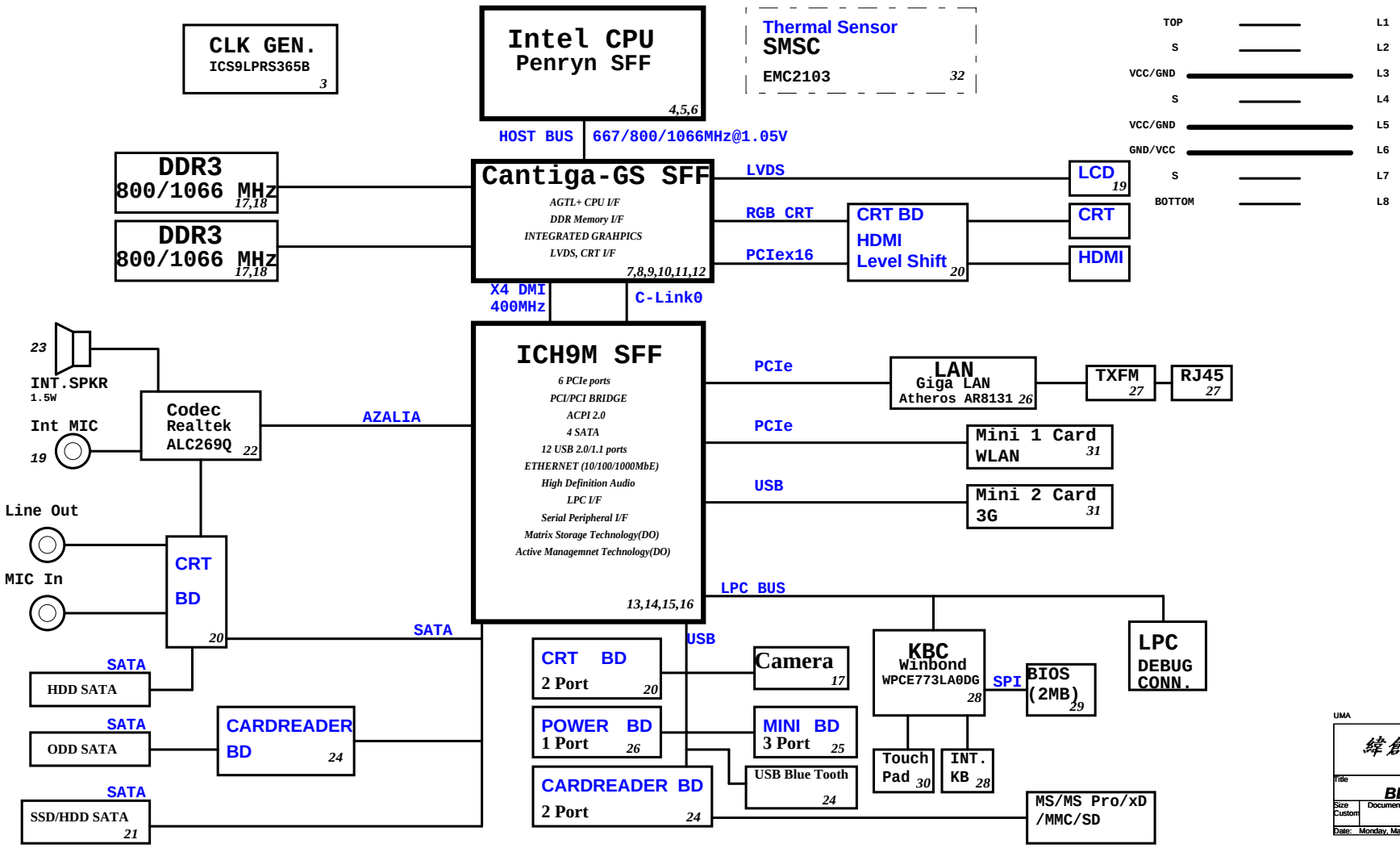
JM41/JM51 UMA Block Diagram

Project code: 91.4CQ01.001
PCB P/N : 48.4CQ01.021
REVISION : 08266-2



PCB STACKUP

TOP	L1
S	L2
VCC/GND	L3
S	L4
VCC/GND	L5
GND/VCC	L6
S	L7
BOTTOM	L8

SYSTEM DC/DC TPS51125 36	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5
RT8202 37	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A)
RT8202 38	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(11A)
RT9026 39	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 (1.2A)
CHARGER MAX8731A 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC ADP3207A 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 64A
VGA ISL6263A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: JM41/JM51 UMA | Rev: -2

Date: Monday, March 30, 2009 | Sheet 1 of 40

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5

page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

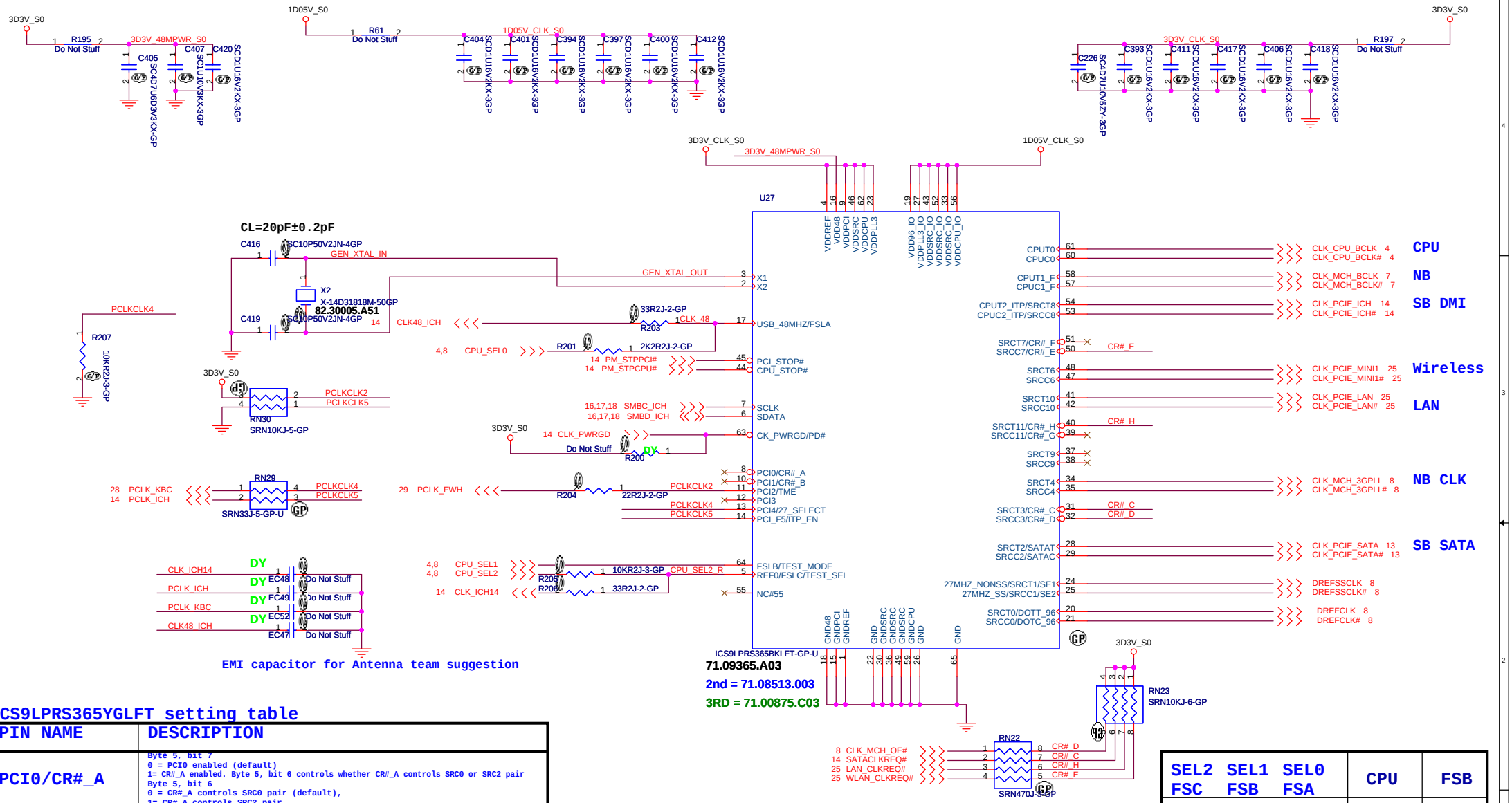
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size: A3 | Document Number: JM41/JM51_UMA | Rev: -2

Date: Thursday, March 19, 2009 | Sheet 2 of 40



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

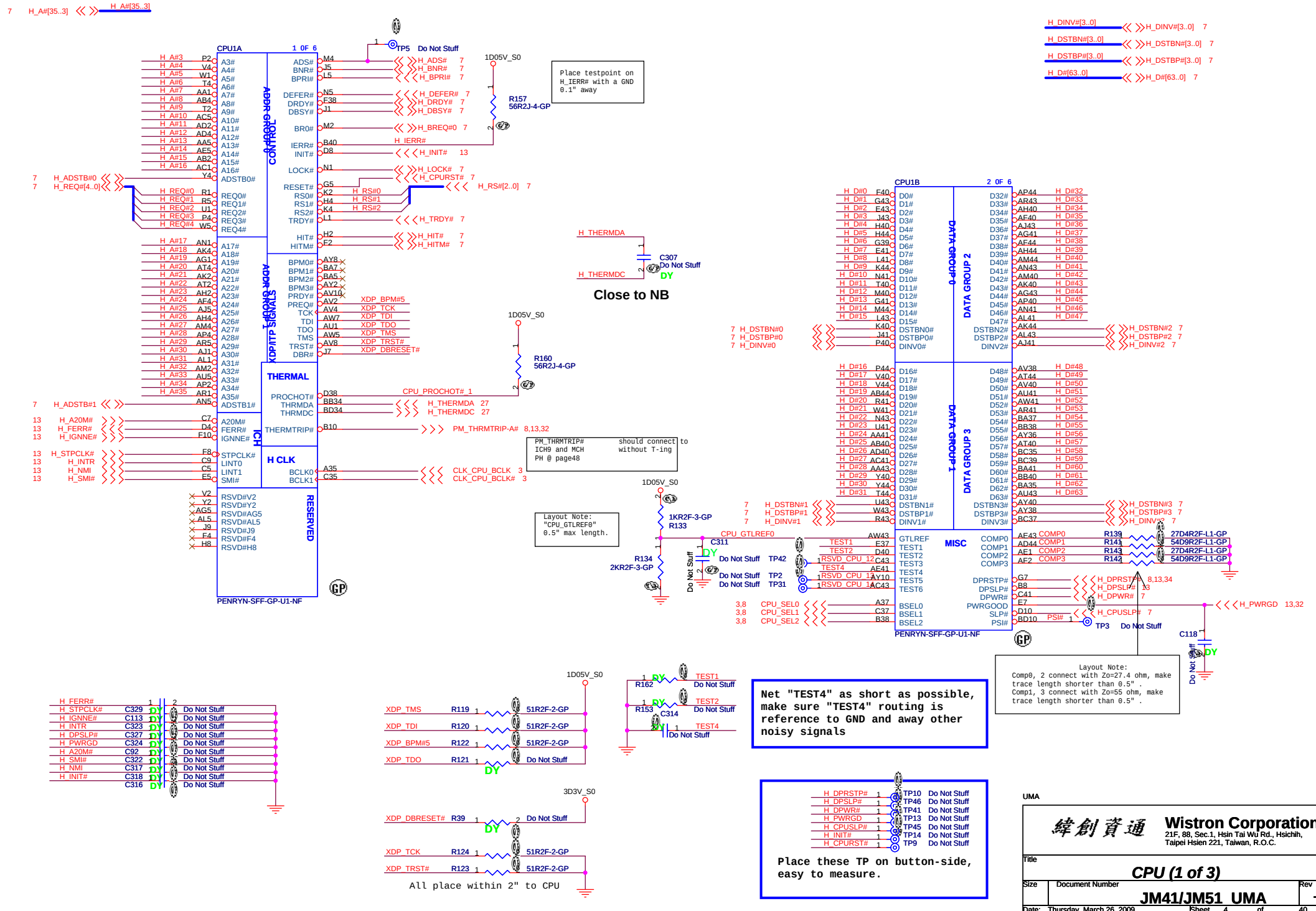
UMA

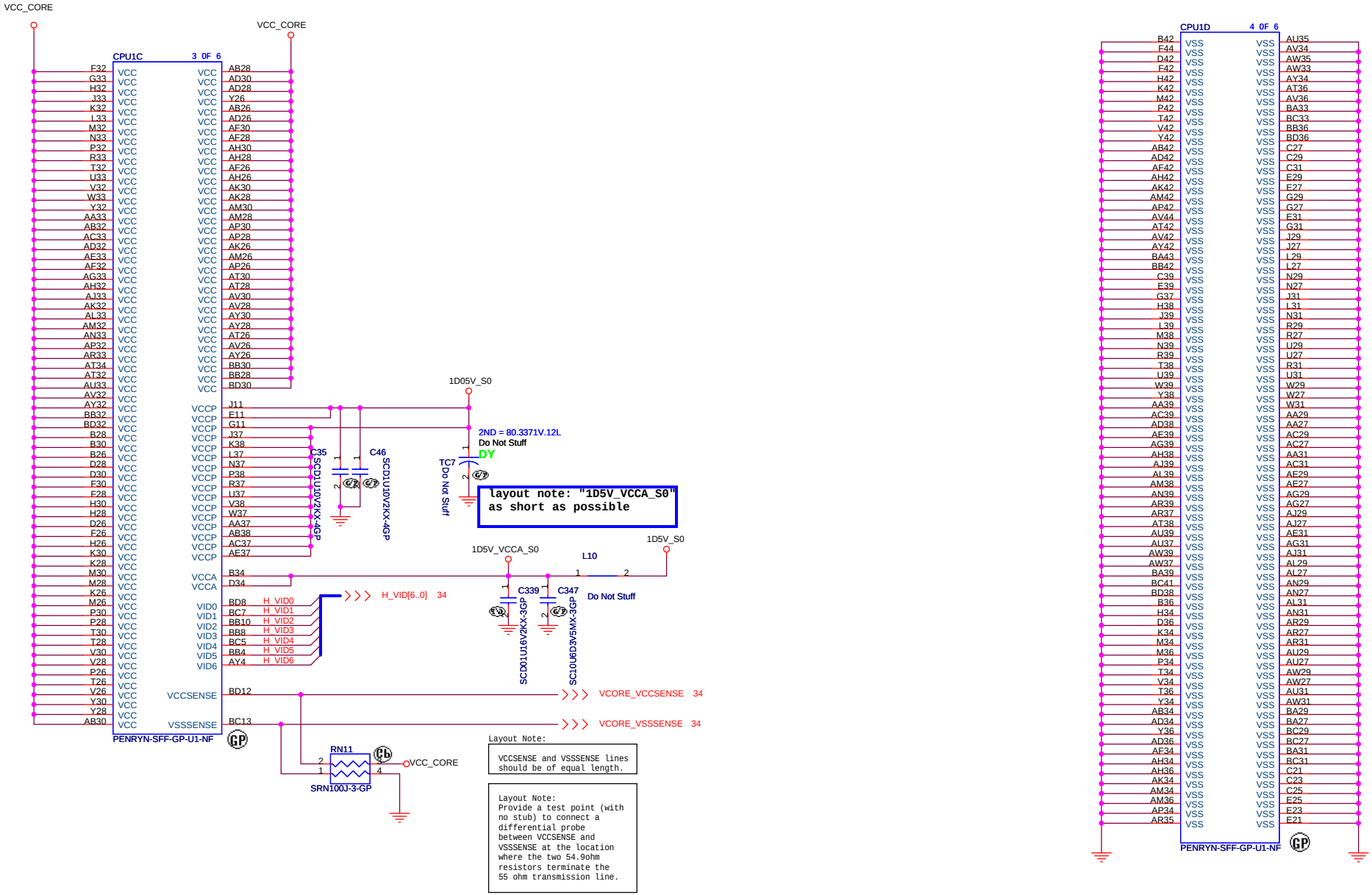
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

Size | Document Number: JM41/JM51_UMA | Rev: -2

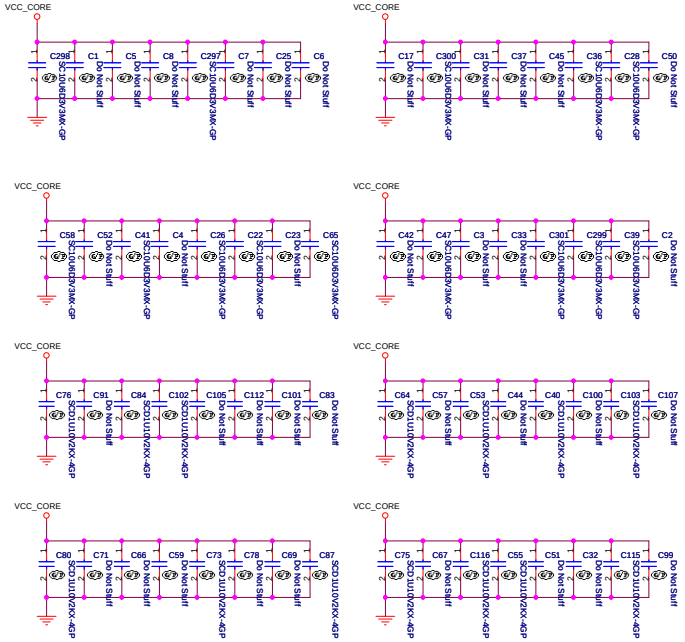
Date: Thursday, March 26, 2009 | Sheet 3 of 40


CPU1A
1 0F 6
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
PENRYN-SFF-GP-U1-NF
TP5 Do Not Stuff
1D05V_S0
R157 56R2J-4-GP
R160 56R2J-4-GP
Place testpoint on H_IERR# with a GND 0.1" away
C307 Do Not Stuff
DY
Close to NB
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
1KR2F-3-GP R133
2KR2F-3-GP R134
C311
TP42
TP2
TP31
CPU1B
2 0F 6
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
MISC
PENRYN-SFF-GP-U1-NF
TP3 Do Not Stuff
C118
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
XDP_TMS R119 51R2F-2-GP
XDP_TDI R120 51R2F-2-GP
XDP_BPM#5 R122 51R2F-2-GP
XDP_TDO R121 Do Not Stuff
XDP_DBRESET# R39 Do Not Stuff
XDP_TCK R124 51R2F-2-GP
XDP_TRST# R123 51R2F-2-GP
All place within 2" to CPU
3D3V_S0
R162 TEST1 Do Not Stuff
R153 TEST2 Do Not Stuff
C314 TEST4 Do Not Stuff
H_FERR# C329 Do Not Stuff
H_STPCLK# C113 Do Not Stuff
H_IGNNE# C323 Do Not Stuff
H_INTR C327 Do Not Stuff
H_DPSLP# C324 Do Not Stuff
H_PWRGD C92 Do Not Stuff
H_A20M# C322 Do Not Stuff
H_SMI# C317 Do Not Stuff
H_NMI C318 Do Not Stuff
H_INIT# C316 Do Not Stuff
TP10 Do Not Stuff
TP46 Do Not Stuff
TP41 Do Not Stuff
TP13 Do Not Stuff
TP45 Do Not Stuff
TP14 Do Not Stuff
TP9 Do Not Stuff
Place these TP on button-side, easy to measure.
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (1 of 3)
Size
Document Number
JM41/JM51 UMA
Rev
-2
Date: Thursday, March 26, 2009
Sheet 4 of 40

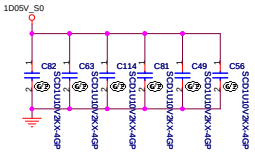


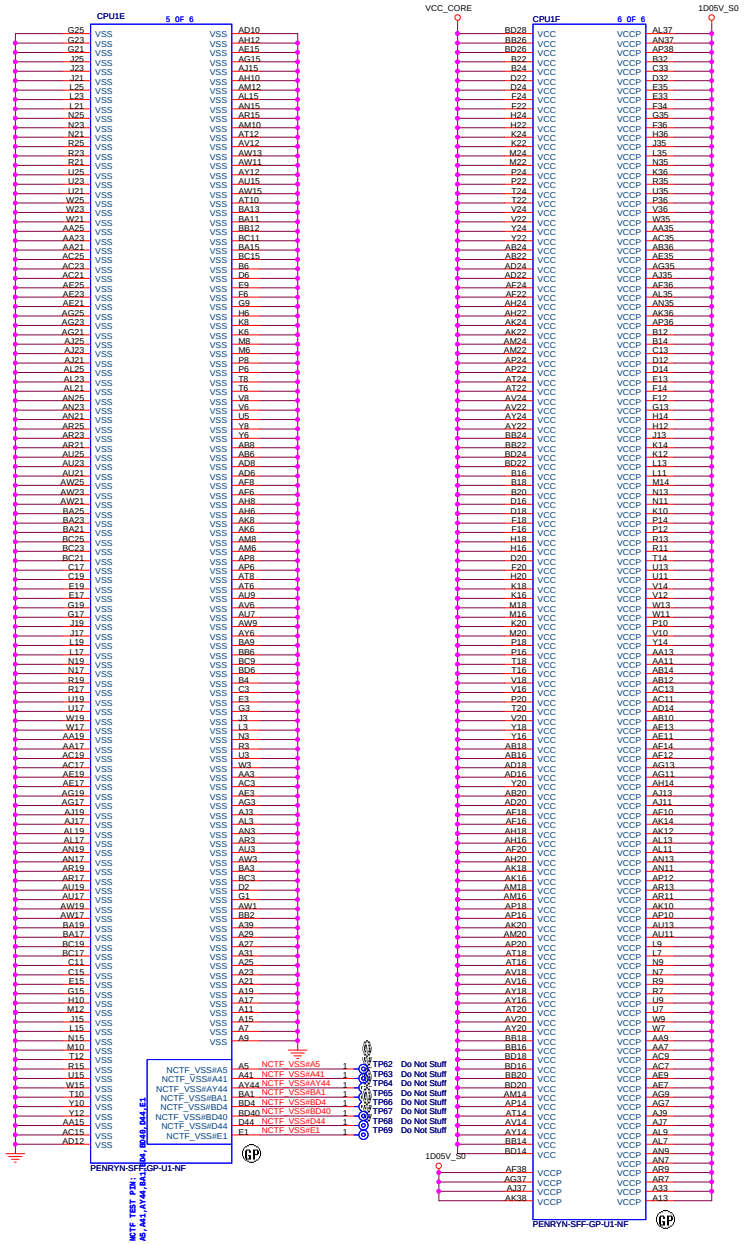
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU (2 of 3)***
Size / Document Number	**JM41/JM51 UMA**
Rev	-2
Date: Thursday, March 26, 2009	Sheet 5 of 40

Place these inside socket
cavity on L8(North side Secondary)



Place these inside socket
cavity on L8(North side Secondary)

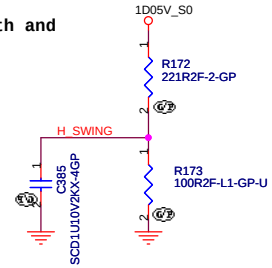




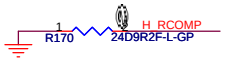
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU (3 of 3)***
Size / Document Number	**JM41/JM51_UMA**
Rev	-2
Date: Thursday, March 19, 2009	Sheet 8 of 40

H_SWING routing Trace width and Spacing use 10 / 20 mil

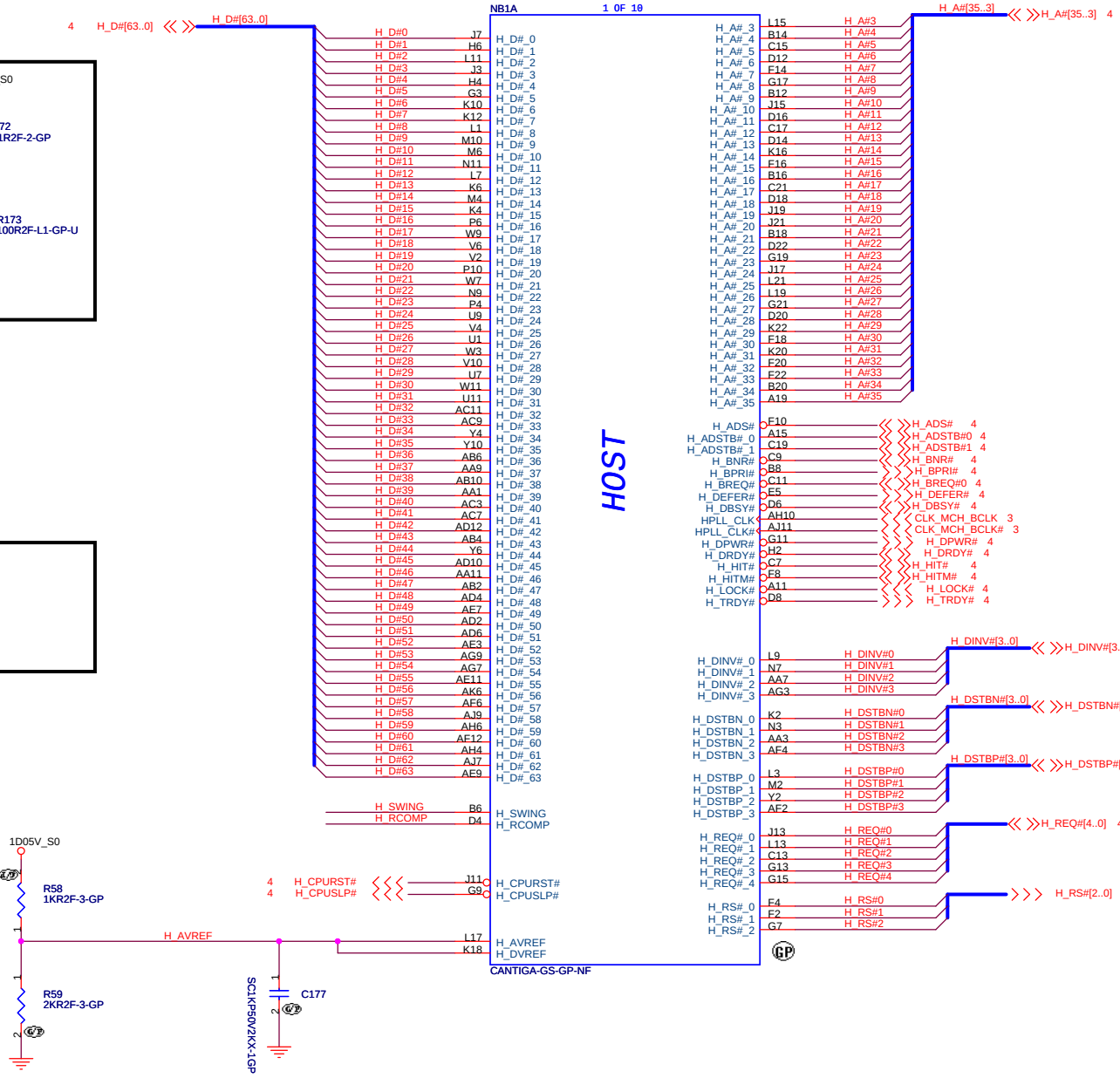
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

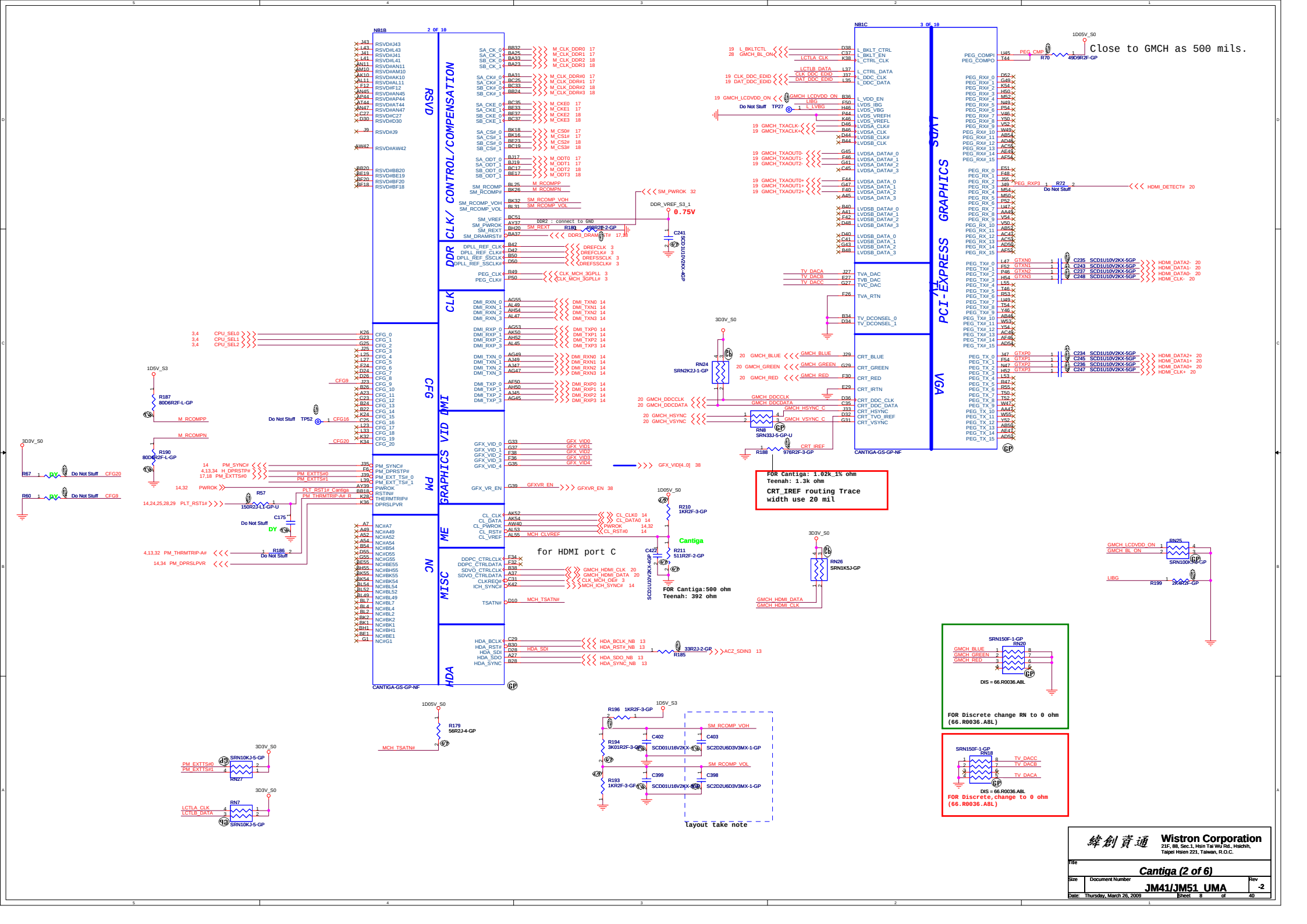


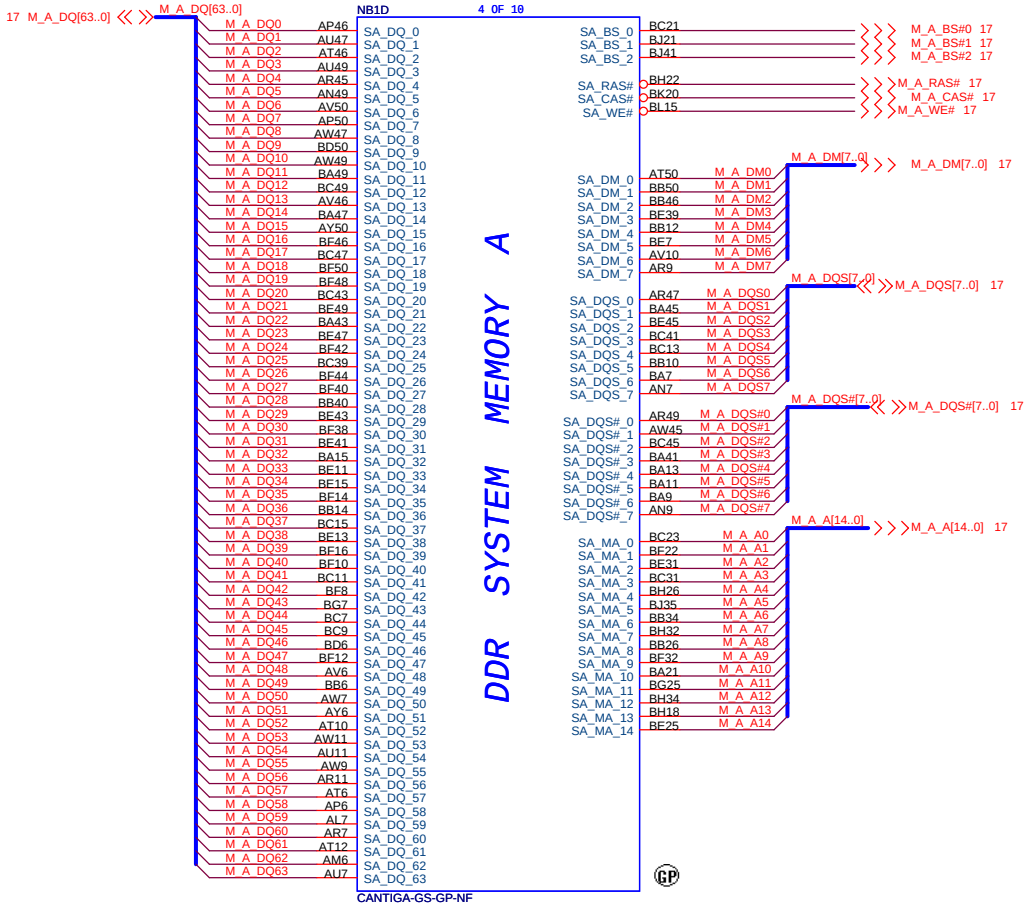
Place them near to the chip (< 0.5")

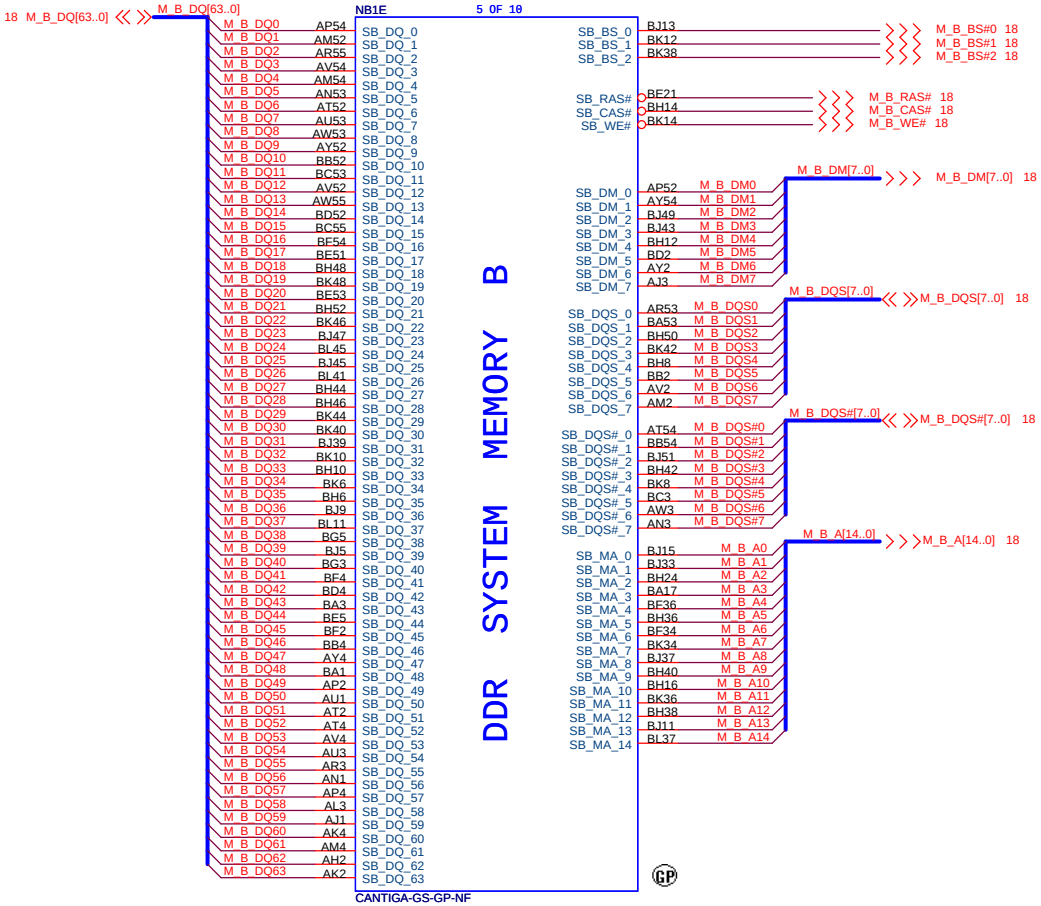


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Cantiga (1 of 6)***
Size / Document Number	**JM41/JM51_UMA**
Rev	-2
Date: Thursday, March 26, 2009	Sheet 7 of 40

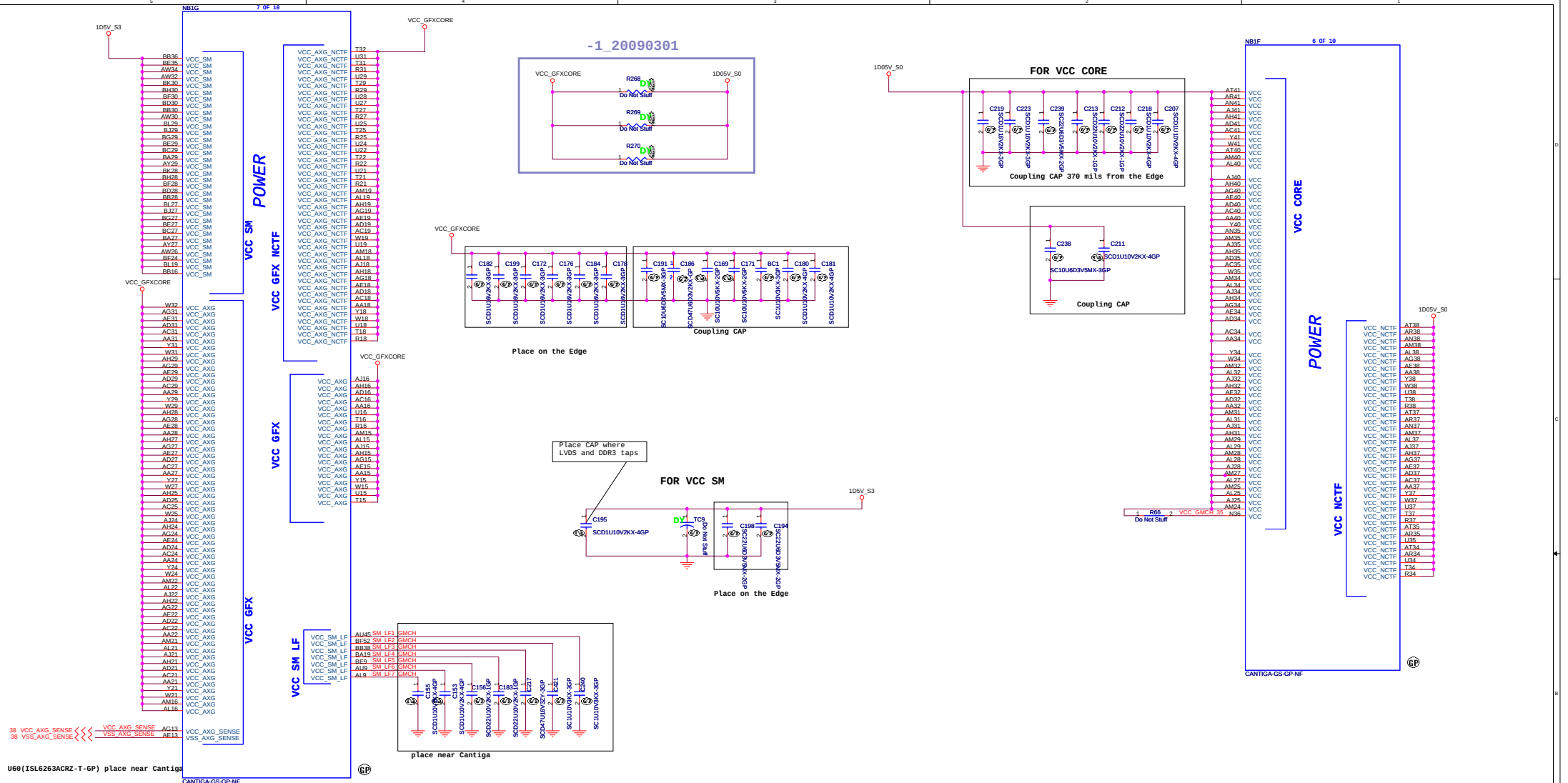

NB1B
2 OF 10
RSVD
CLK/ CONTROL/COMPENSATION
DDR
CLK
CFG
DMI
GRAPHICS VID
PM
ME
MISC
HDA
NC
CANTIGA-GS-GP-NF
NB1C
3 OF 10
PCI-EXPRESS GRAPHICS
VGA
CANTIGA-GS-GP-NF
Close to GMCH as 500 mils.
for HDMI port C
Cantiga
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Discrete change RN to 0 ohm (66.R0036.A8L)
FOR Discrete,change to 0 ohm (66.R0036.A8L)
layout take note
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Cantiga (2 of 6)
Size
Document Number
JM41/JM51 UMA
Rev
-2
Date: Thursday, March 26, 2009
Sheet 8 of 40



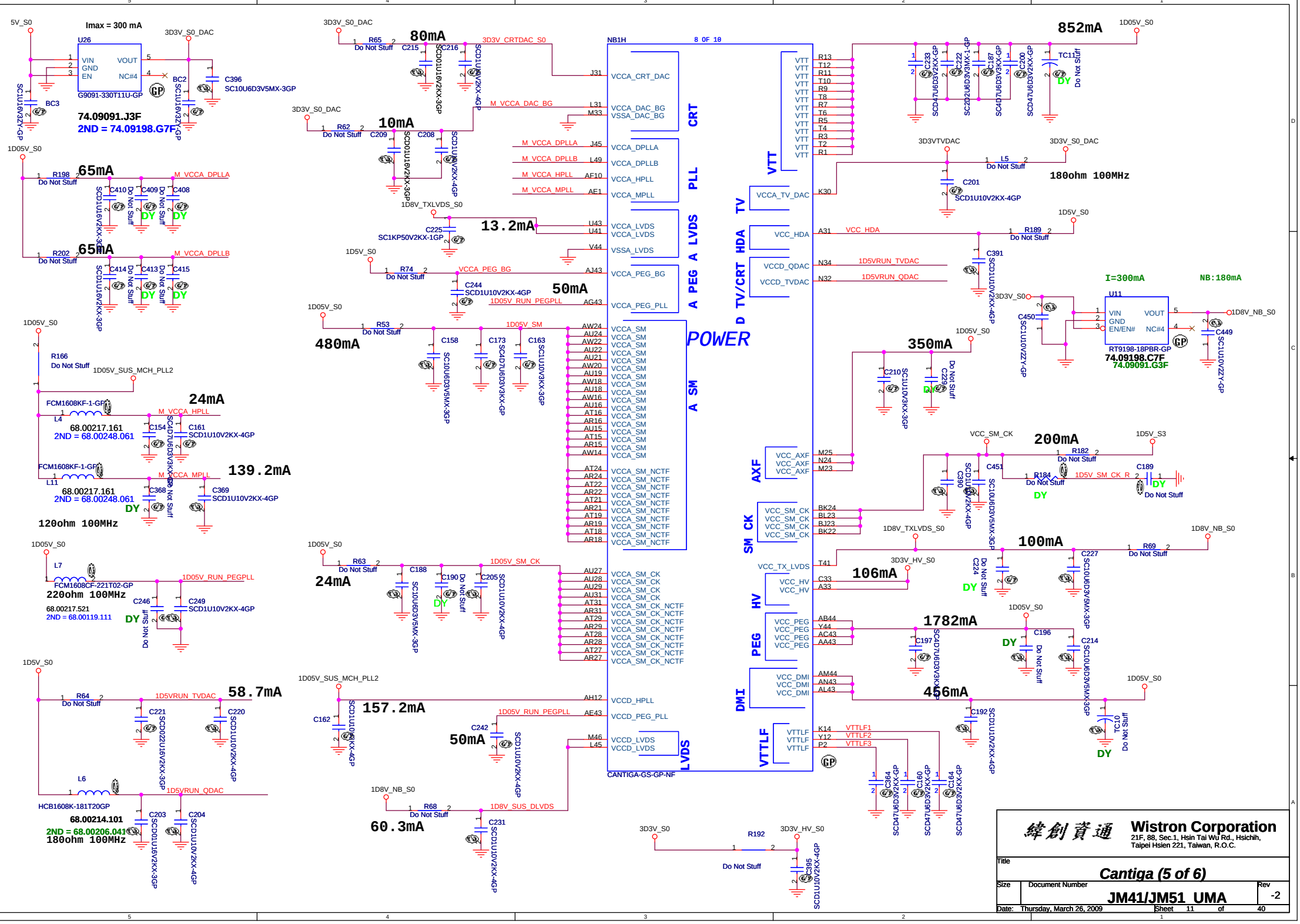


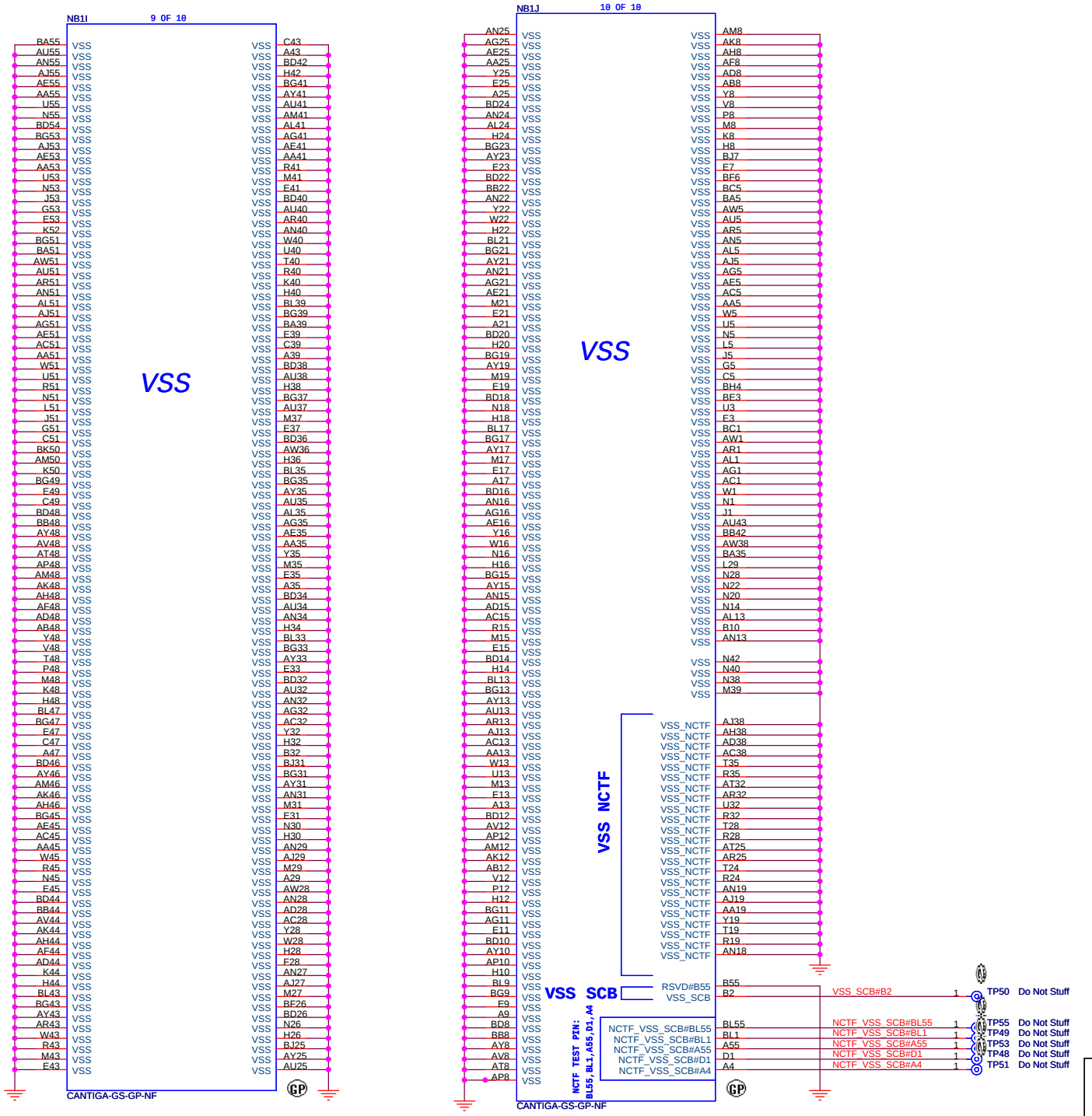
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cantiga (3 of 6)
Size	
Document Number	JM41/JM51 UMA
Rev	-2
Date: Thursday, March 26, 2009	Sheet 9 of 40



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Cantiga (4 of 6)*
Size / Document Number	JM41/JM51_UMA
Rev	-2
Date: Thursday, March 26, 2009	Sheet 10 of 40


Imax = 300 mA
U26
G9091-330T11U-GP
74.09091.J3F
2ND = 74.09198.G7F
80mA
10mA
65mA
65mA
13.2mA
50mA
480mA
24mA
139.2mA
120ohm 100MHz
220ohm 100MHz
58.7mA
157.2mA
50mA
60.3mA
180ohm 100MHz
852mA
180ohm 100MHz
350mA
200mA
100mA
106mA
1782mA
456mA
I=300mA
NB:180mA
U11
RT9198-18PBR-GP
74.09198.C7F
74.09091.G3F
NB1H
8 OF 10
CRT
PLL
LVDS
A PEG
A SM
POWER
TV
HDA
TV/CRT
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
CANTIGA-GS-GP-NF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Cantiga (5 of 6)
Size
Document Number
JM41/JM51 UMA
Rev
-2
Date: Thursday, March 26, 2009
Sheet 11 of 40

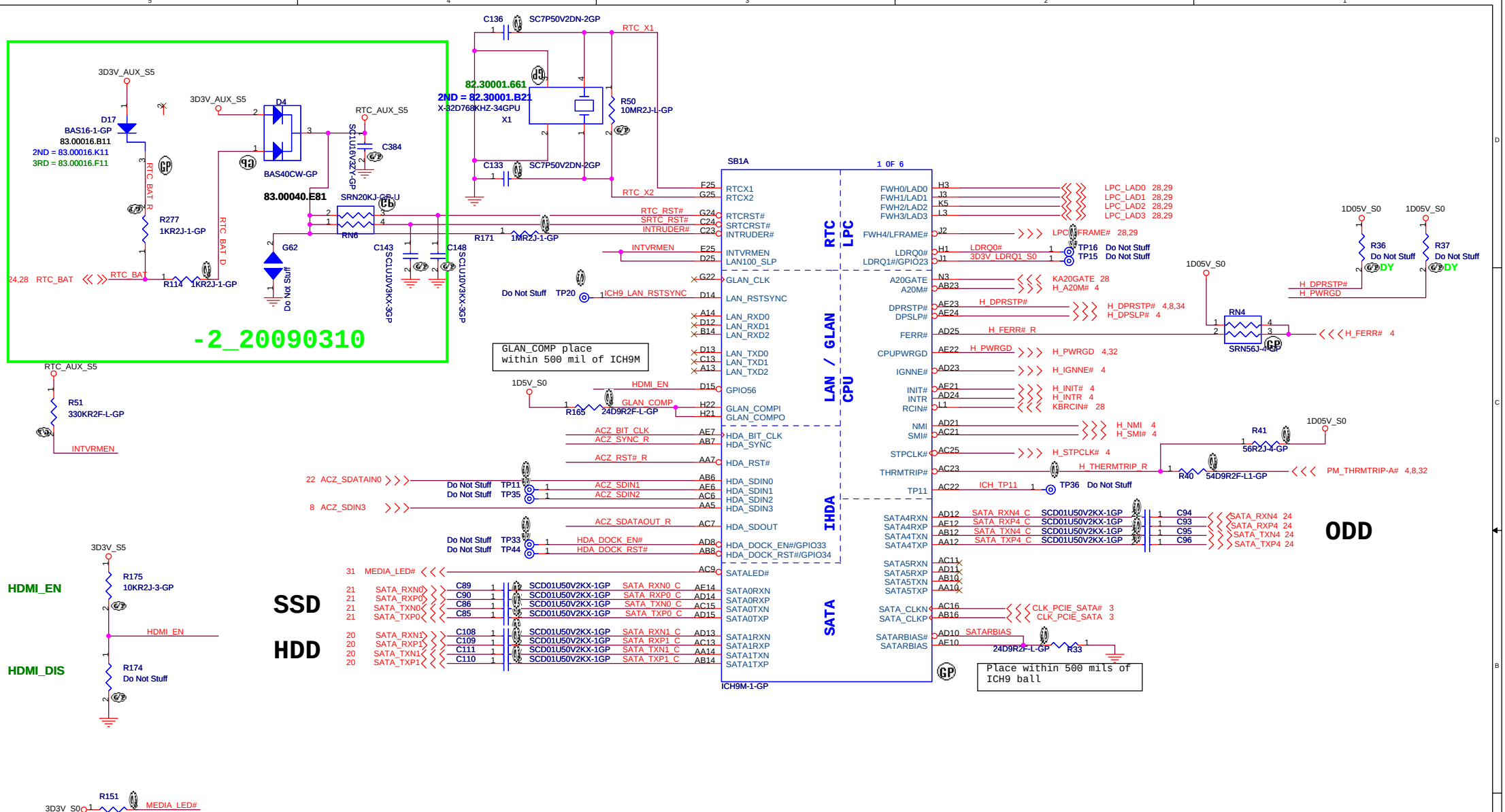


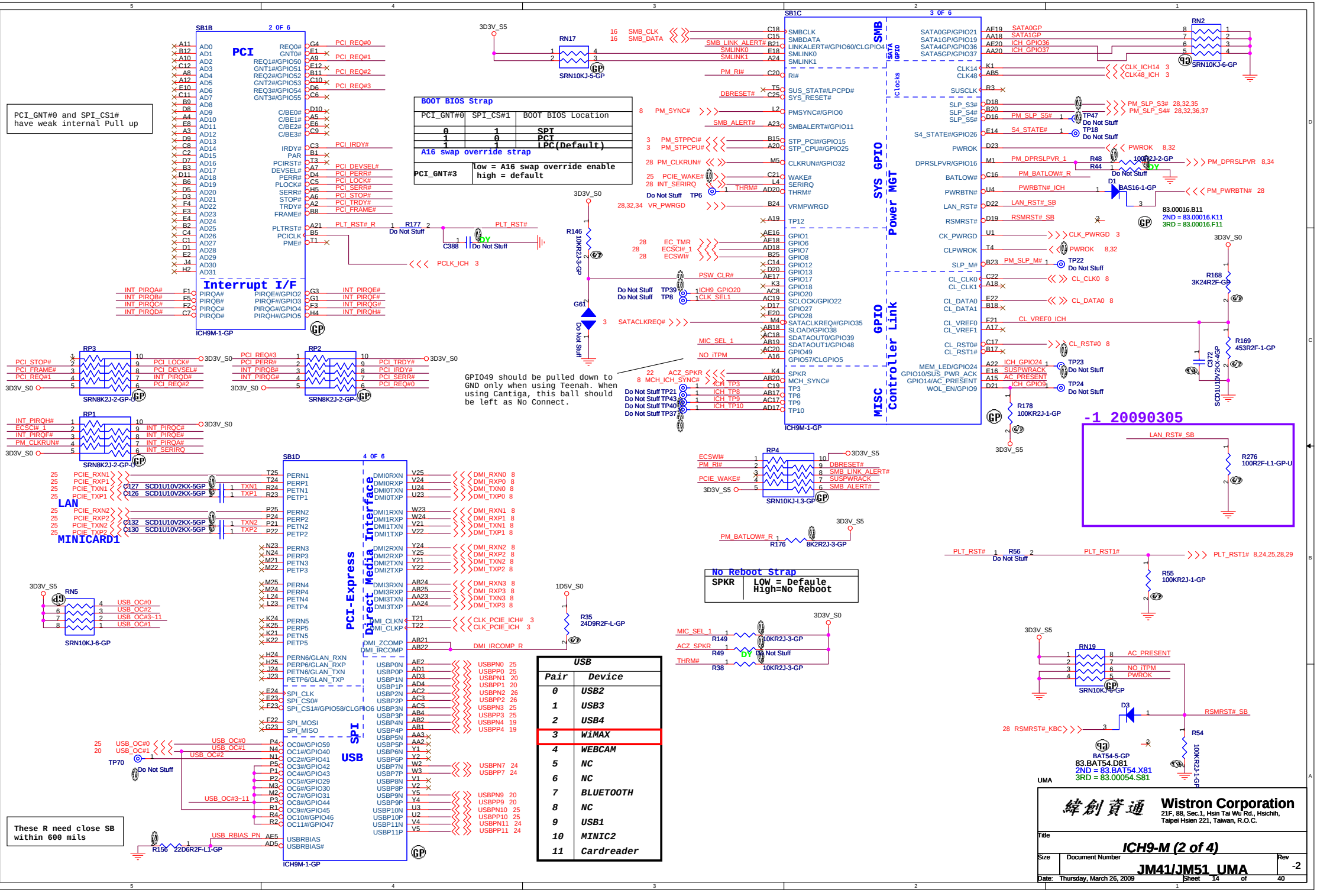
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

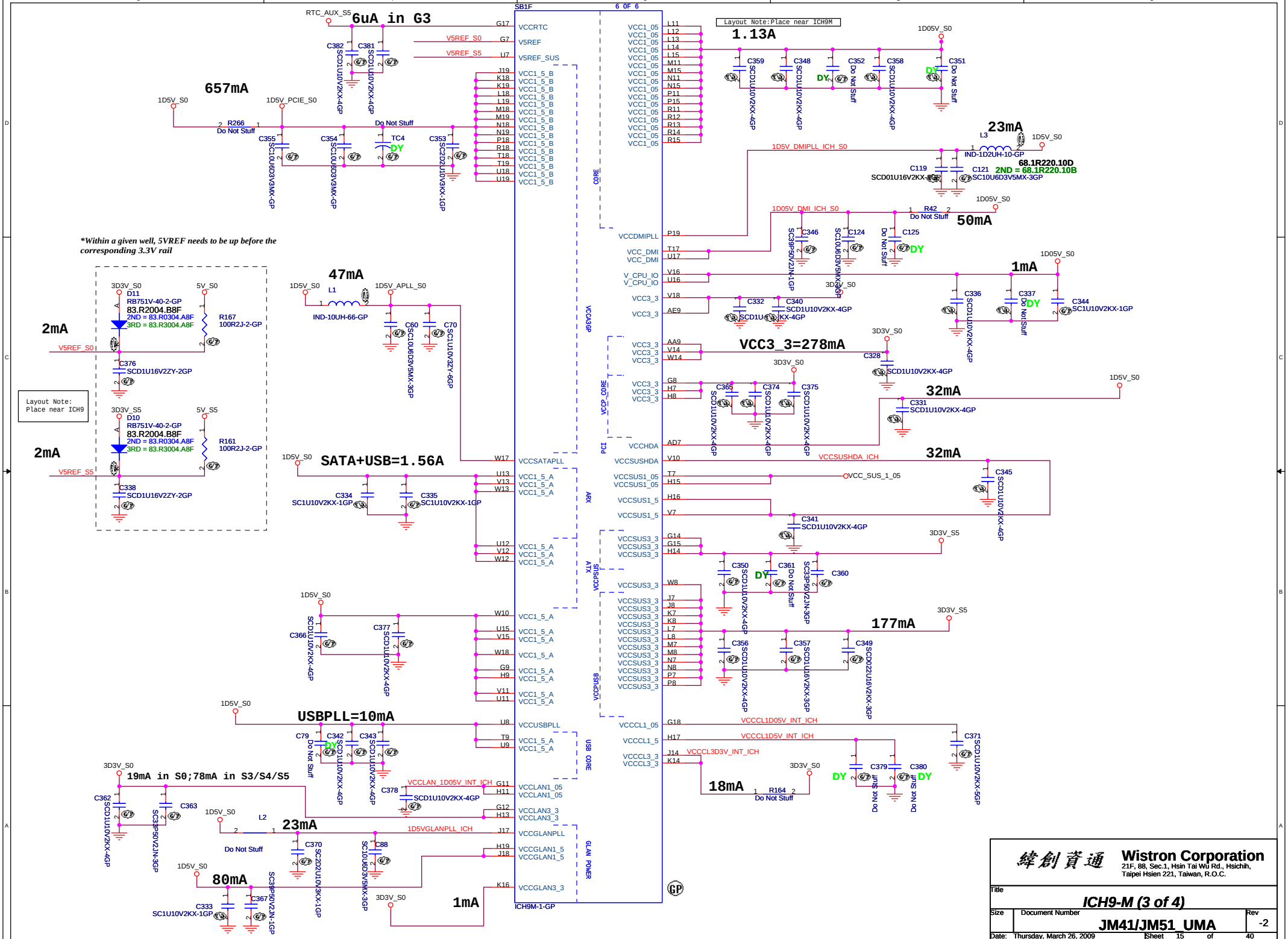
Title: ***Cantiga (6 of 6)***

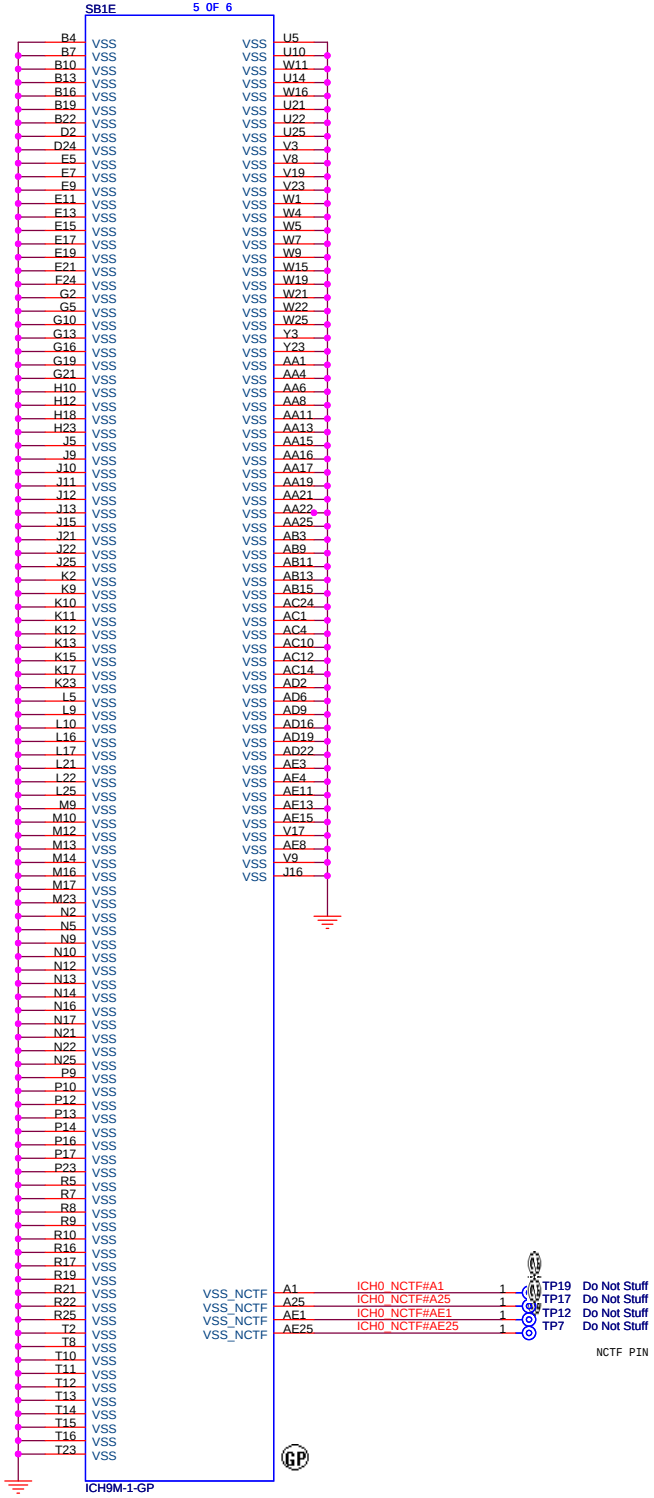
Size | Document Number: **JM41/JM51 UMA** | Rev: -2

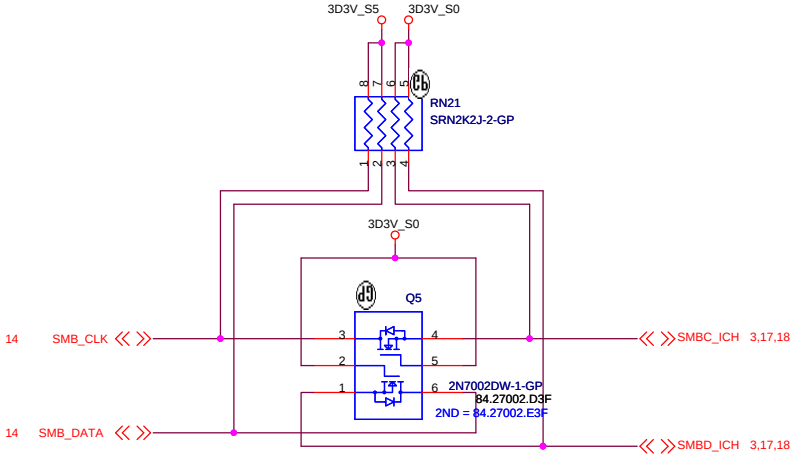
Date: Thursday, March 19, 2009 | Sheet 12 of 40


-2_20090310
SB1A
1 0F 6
ICH9M-1-GP
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
SSD
HDD
ODD
HDMI_EN
HDMI_DIS
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
82.30001.661
2ND = 82.30001.B21
X-32D768KHZ-34GPU
X1
R50
10MR2J-L-GP
C136
C133
SC7P50V2DN-2GP
RTC_X1
RTC_X2
D17
BAS16-1-GP
83.00016.B11
2ND = 83.00016.K11
3RD = 83.00016.F11
D4
BAS40CW-GP
83.00040.E81
SRN20KJ-GP-U
RN6
R277
1KR2J-1-GP
R114
1KR2J-1-GP
G62
Do Not Stuff
C384
C143
C148
R171
1MR2J-1-GP
RTC_BAT
RTC_BAT_R
RTC_BAT_D
3D3V_AUX_S5
RTC_AUX_S5
R51
330KR2F-L-GP
INTVRMEN
R165
24D9R2F-L-GP
GLAN_COMP
HDMI_EN
R175
10KR2J-3-GP
R174
Do Not Stuff
R151
10KR2J-3-GP
MEDIA_LED#
3D3V_S5
3D3V_S0
RN13
SRN33J-7-GP
RN3
SRN0J-7-GP
C97
DY
RN4
SRN56J-4-GP
R36
R37
Do Not Stuff
R41
56R2J-4-GP
R40
54D9R2F-L1-GP
PM_THRMTRIP-A# 4,8,32
TP36
Do Not Stuff
R33
24D9R2F-L-GP
1D05V_S0
H_DPRSTP#
H_PWRGD
H_FERR# 4
H_PWRGD 4,32
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRCIN# 28
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP_R
ICH_TP11
TP11
LPC_LAD0 28,29
LPC_LAD1 28,29
LPC_LAD2 28,29
LPC_LAD3 28,29
LPC_FRAME# 28,29
LDRQ0#
3D3V_LDRQ1_S0
TP16
TP15
KA20GATE 28
H_A20M# 4
H_DPRSTP# 4,8,34
H_DPSLP# 4
H_FERR# R
SATA_RXN4 24
SATA_RXP4 24
SATA_TXN4 24
SATA_TXP4 24
SCD01U50V2KX-1GP
CLK_PCIE_SATA# 3
CLK_PCIE_SATA 3
SATARBIAS
ACZ_RST# R
ACZ_SDATAOUT_R
ACZ_SYNC_R
ACZ_BIT_CLK
HDA_RST#_NB
HDA_SDO_NB
HDA_SYNC_NB
HDA_BCLK_NB
ACZ_RST#
ACZ_SDATAOUT
ACZ_SYNC
ACZ_BITCLK
ACZ_SDATAIN0
ACZ_SDIN3
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDATAOUT_R
HDA_DOCK_EN#
HDA_DOCK_RST#
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN1_C
SATA_RXP1_C
SATA_TXN1_C
SATA_TXP1_C
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
JM41/JM51 UMA
Rev
-2
Date: Monday, March 30, 2009
Sheet 13 of 40


PCI_GNT#0 and SPI_CS1# have weak internal Pull up
BOOT BIOS Strap
PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location
0 | 1 | SPI
1 | 0 | PCI
1 | 1 | LPC(Default)
A16 swap override strap
PCI_GNT#3 | low = A16 swap override enable high = default
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
No Reboot Strap
SPKR | LOW = Defaule High=No Reboot
USB
Pair | Device
0 | USB2
1 | USB3
2 | USB4
3 | WiMAX
4 | WEBCAM
5 | NC
6 | NC
7 | BLUETOOTH
8 | NC
9 | USB1
10 | MINIC2
11 | Cardreader
These R need close SB within 600 mils
-1 20090305
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (2 of 4)
JM41/JM51 UMA
Thursday, March 26, 2009
Sheet 14 of 40


SB1F
6 OF 6
ICH9M-1-GP
6uA in G3
RTC_AUX_S5
V5REF_S0
V5REF_S5
657mA
1D5V_S0
1D5V_PCIE_S0
R266
Do Not Stuff
C355
C354
TC4
C353
1.13A
Layout Note:Place near ICH9M
C359
C348
C352
C358
C351
23mA
L3
IND-1D2UH-10-GP
1D5V_DMIPLL_ICH_S0
68.1R220.10D
2ND = 68.1R220.10B
C119
C121
SC10U6D3V5MX-3GP
1D05V_DMI_ICH_S0
R42
50mA
C346
C124
C125
1mA
C336
C337
C344
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
3D3V_S0
5V_S0
D11
RB751V-40-2-GP
83.R2004.B8F
2ND = 83.R0304.A8F
3RD = 83.R3004.A8F
R167
100R2J-2-GP
2mA
C376
SCD1U16V2ZY-2GP
Layout Note:
Place near ICH9
3D3V_S5
5V_S5
D10
R161
100R2J-2-GP
C338
47mA
L1
IND-10UH-66-GP
C60
C70
C332
C340
VCC3_3=278mA
C328
32mA
C365
C374
C375
C331
VCCSUSHDA_ICH
C345
SATA+USB=1.56A
C334
C335
C341
C350
C361
C360
177mA
C356
C357
C349
USBPLL=10mA
C79
C342
C343
C366
C377
VCCLAN_1D05V_INT_ICH
C378
19mA in S0;78mA in S3/S4/S5
C362
C363
L2
23mA
1D5VGLANPLL_ICH
C370
C88
80mA
C367
C333
1mA
VCCCL1D05V_INT_ICH
VCCCL3D3V_INT_ICH
18mA
R164
C379
C380
C371
CORE
VCCA3GP
VCC3_3_CORE
PCI
ARX
ATX
VCCA3GSUS
USB CORE
GLAN POWER
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (3 of 4)
Size
Document Number
JM41/JM51_UMA
Rev
-2
Date: Thursday, March 26, 2009
Sheet 15 of 40



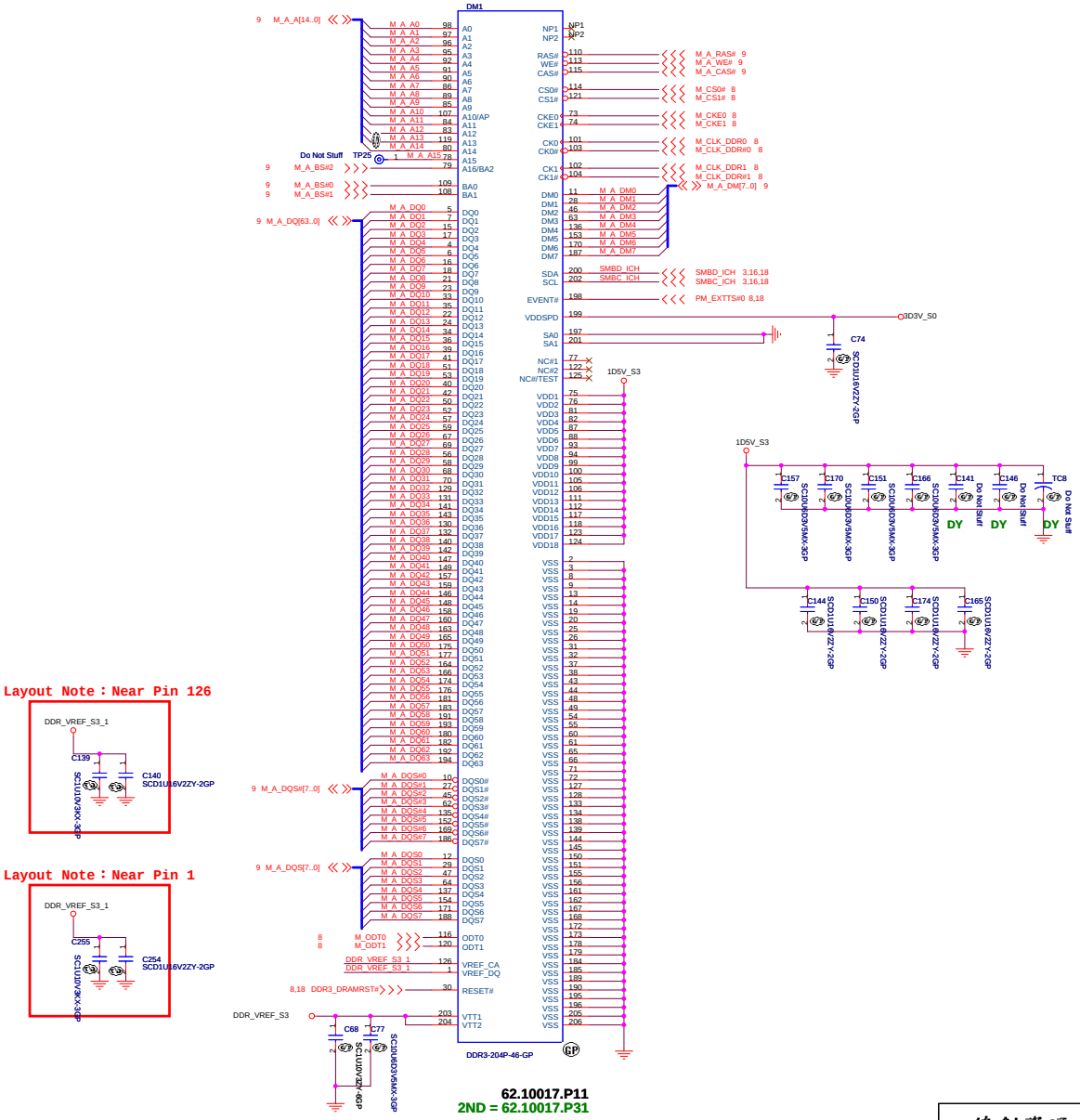


SMBUS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

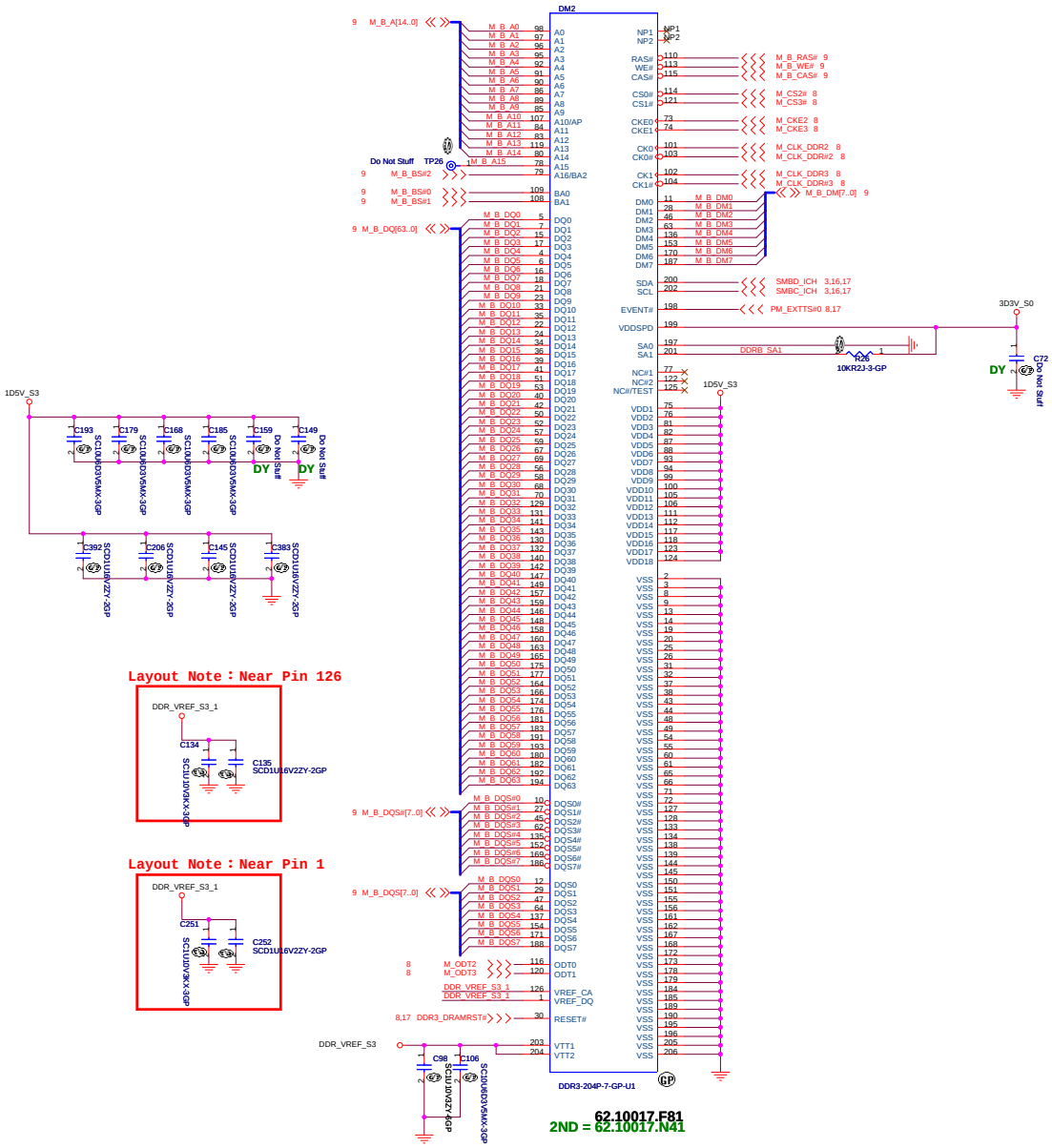
Title	ICH9-M (4 of 4)	
Size	Document Number: JM41/JM51 UMA	Rev -2
Date: Thursday, March 26, 2009	Sheet 16 of 40	

DDR3 SOCKET_1



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDR3 Socket1
Size / Document Number	JM41/JM51_UMA
Rev	-2
Date: Thursday, March 26, 2009	Sheet 17 of 40

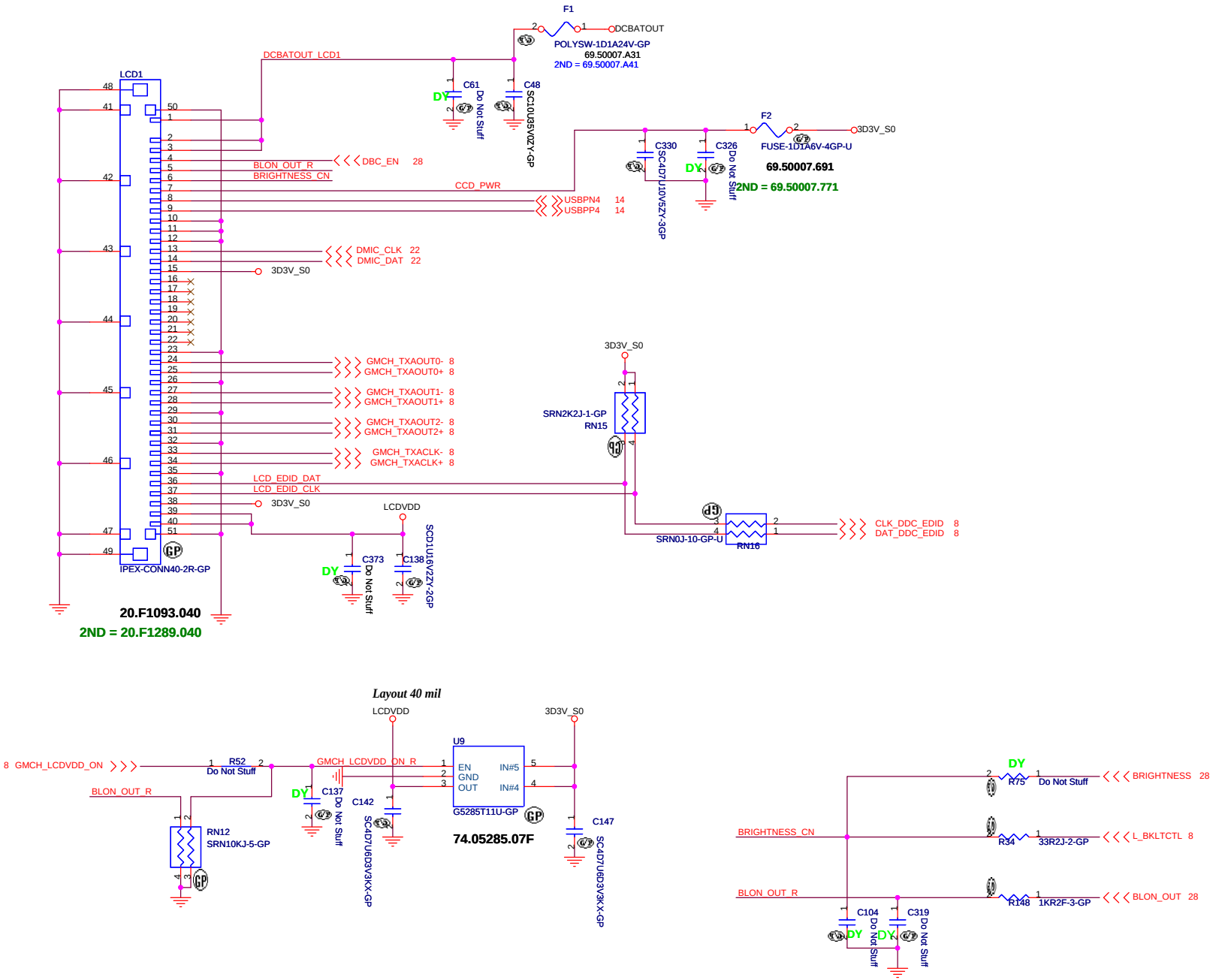
DDR3 SOCKET_2



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDR3 Socket2
Size / Document Number	JM41/JM51 UMA
Rev	-2
Date: Thursday, March 26, 2009	Sheet 18 of 40

LCD/CCD CONN

Internal MIC



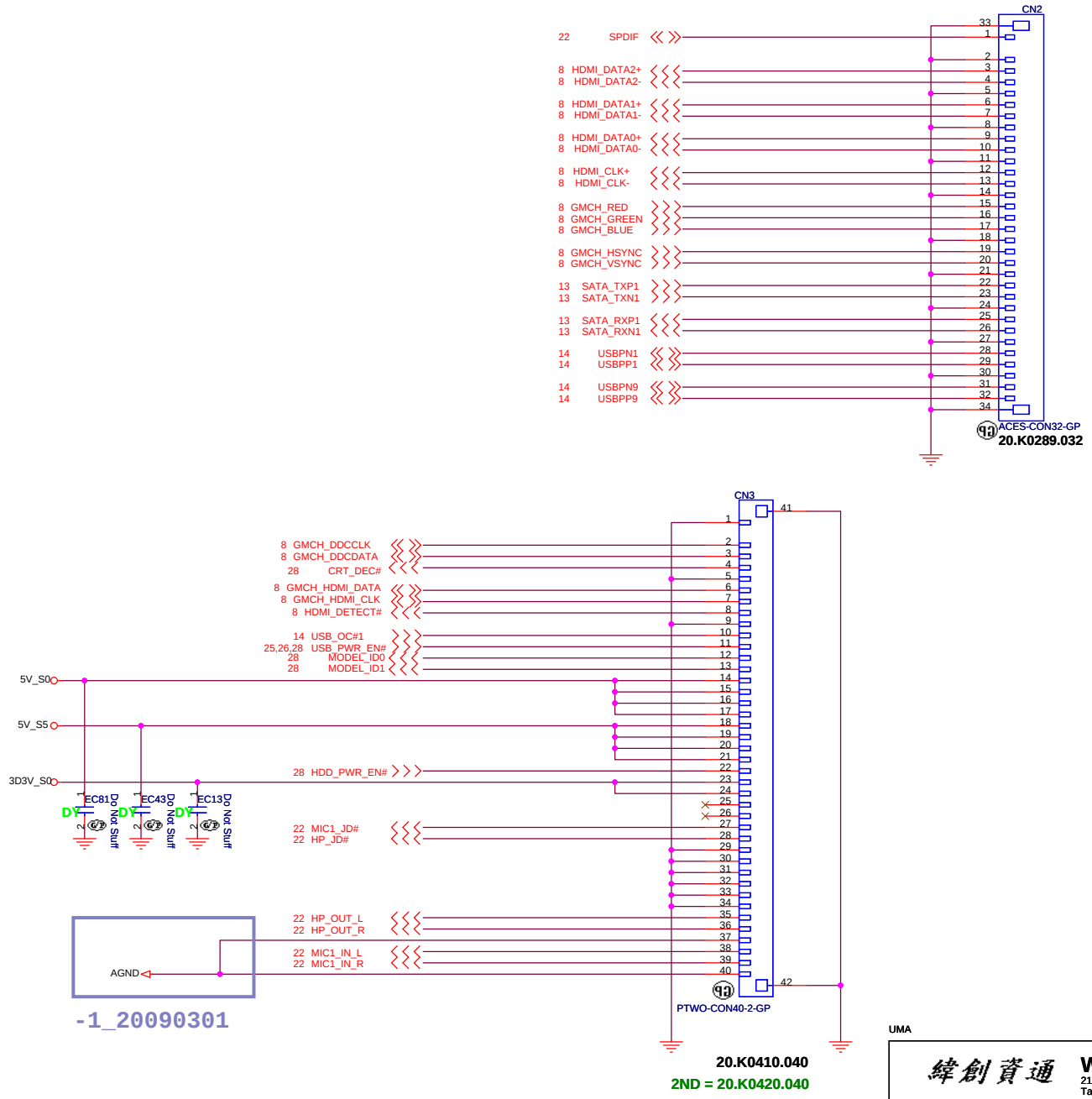
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN**

Size | Document Number: **JM41/JM51 UMA** | Rev: -2

Date: Monday, March 30, 2009 | Sheet 19 of 40

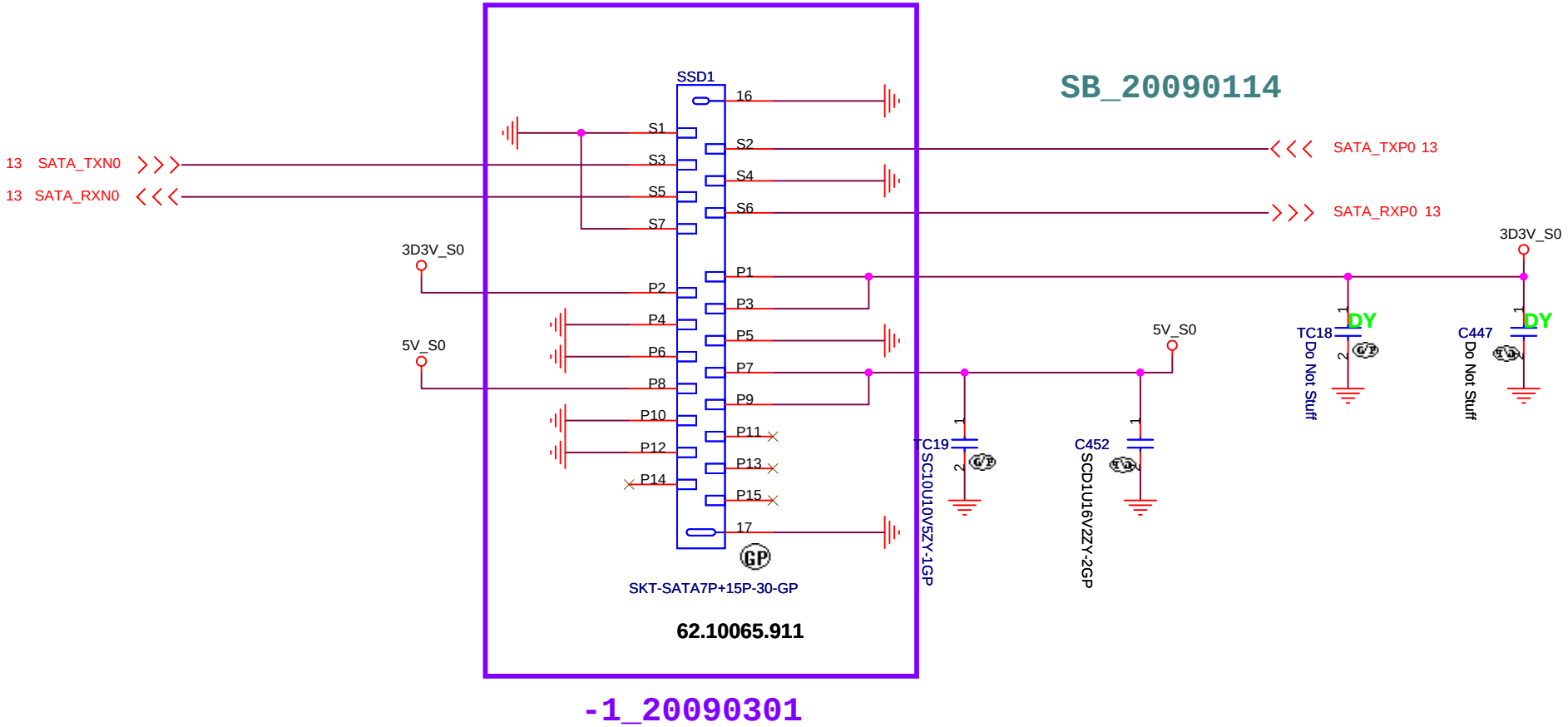


UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

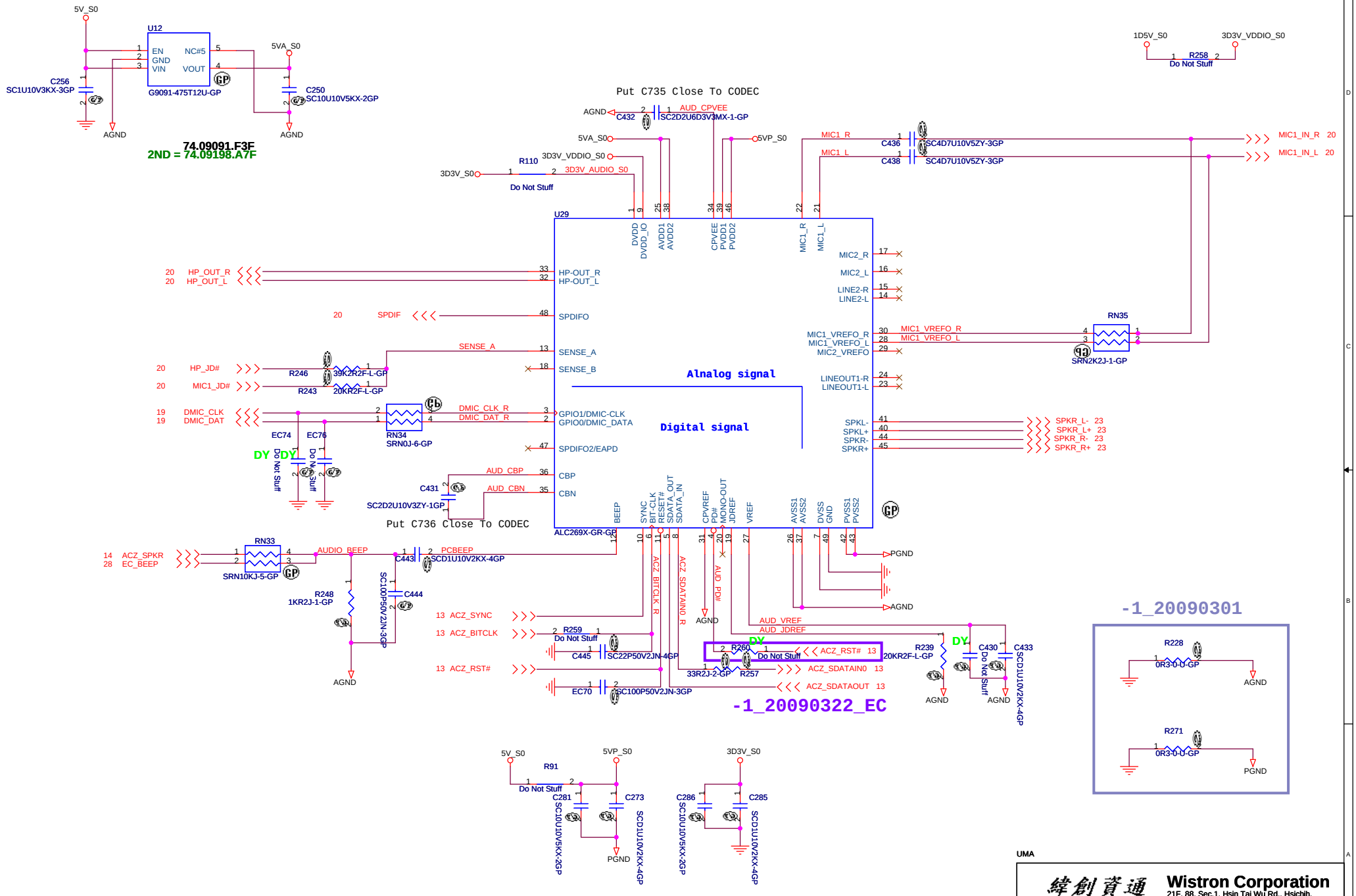
Title		
CRT BD CONN		
Size	Document Number	Rev
	JM41/JM51 UMA	-2
Date: Thursday, March 26, 2009	Sheet 20 of 40	

SSD SATA Connector

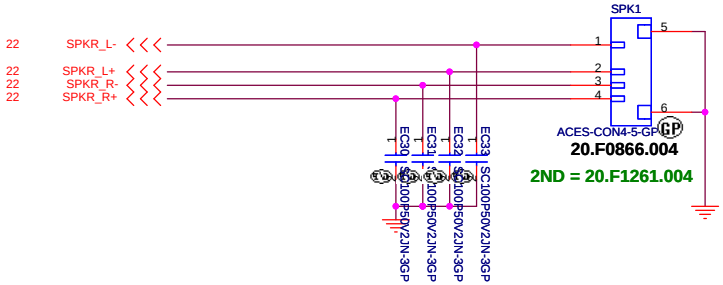


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD CONN***	
Size	Document Number **JM41/JM51 UMA**	Rev -2
Date: Thursday, March 26, 2009	Sheet 21 of 40	


U12
G9091-475T12U-GP
EN
GND
VIN
NC#5
VOUT
5V_S0
5VA_S0
C256
SC1U10V3KX-3GP
C250
SC10U10V5KX-2GP
AGND
74.09091.F3F
2ND = 74.09198.A7F
Put C735 Close To CODEC
AUD_CPVEE
SC2D2U6D3V3MX-1-GP
C432
5VP_S0
3D3V_VDDIO_S0
3D3V_S0
3D3V_AUDIO_S0
R110
Do Not Stuff
1D5V_S0
R258
MIC1_R
MIC1_L
C436
C438
SC4D7U10V5ZY-3GP
MIC1_IN_R 20
MIC1_IN_L 20
U29
DVDD
DVDD_IO
AVDD1
AVDD2
CPVEE
PVDD1
PVDD2
HP-OUT_R
HP-OUT_L
20 HP_OUT_R
20 HP_OUT_L
20 SPDIFO
SPDIFO
SENSE_A
SENSE_B
20 HP_JD#
20 MIC1_JD#
R246
39K2R2F-L-GP
R243
20KR2F-L-GP
19 DMIC_CLK
19 DMIC_DAT
DMIC_CLK_R
DMIC_DAT_R
GPIO1/DMIC-CLK
GPIO0/DMIC_DATA
RN34
SRN0J-6-GP
EC74
EC76
DY
Do Not Stuff
SPDIFO2/EAPD
AUD_CBP
AUD_CBN
C431
SC2D2U10V3ZY-1GP
Put C736 Close To CODEC
CBP
CBN
Alnalog signal
Digital signal
MIC2_R
MIC2_L
LINE2-R
LINE2-L
MIC1_VREFO_R
MIC1_VREFO_L
MIC2_VREFO
RN35
SRN2K2J-1-GP
LINEOUT1-R
LINEOUT1-L
SPKL-
SPKL+
SPKR-
SPKR+
SPKR_L- 23
SPKR_L+ 23
SPKR_R- 23
SPKR_R+ 23
BEEP
SYNC
BIT-CLK
RESET#
SDATA_OUT
SDATA_IN
CPVREF
PD#
MONO-OUT
JDREF
VREF
AVSS1
AVSS2
DVSS
GND
PVSS1
PVSS2
ALC269X-GR-GP
PGND
AGND
14 ACZ_SPKR
28 EC_BEEP
RN33
SRN10KJ-5-GP
AUDIO_BEEP
C443
PCBEEP
SCD1U10V2KX-4GP
R248
1KR2J-1-GP
SC100P50V2JN-3GP
C444
13 ACZ_SYNC
13 ACZ_BITCLK
13 ACZ_RST#
R259
C445
SC22P50V2JN-4GP
EC70
SC100P50V2JN-3GP
ACZ_BITCLK_R
ACZ_SDATAIN0_R
AUD_PD#
AUD_VREF
AUD_JDREF
R260
ACZ_RST# 13
33R2J-2-GP
R257
ACZ_SDATAIN0 13
ACZ_SDATAOUT 13
R239
20KR2F-L-GP
C430
C433
-1_20090322_EC
-1_20090301
R228
0R3-0-U-GP
R271
R91
C281
C273
C286
C285
Close Pim.39
and Pin.46
Close Pim.1
and Pin.9
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC REALTEK ALC269
Size
Document Number
JM41/JM51 UMA
Rev
-2
Date: Monday, March 30, 2009
Sheet 22 of 40

Internal Speaker



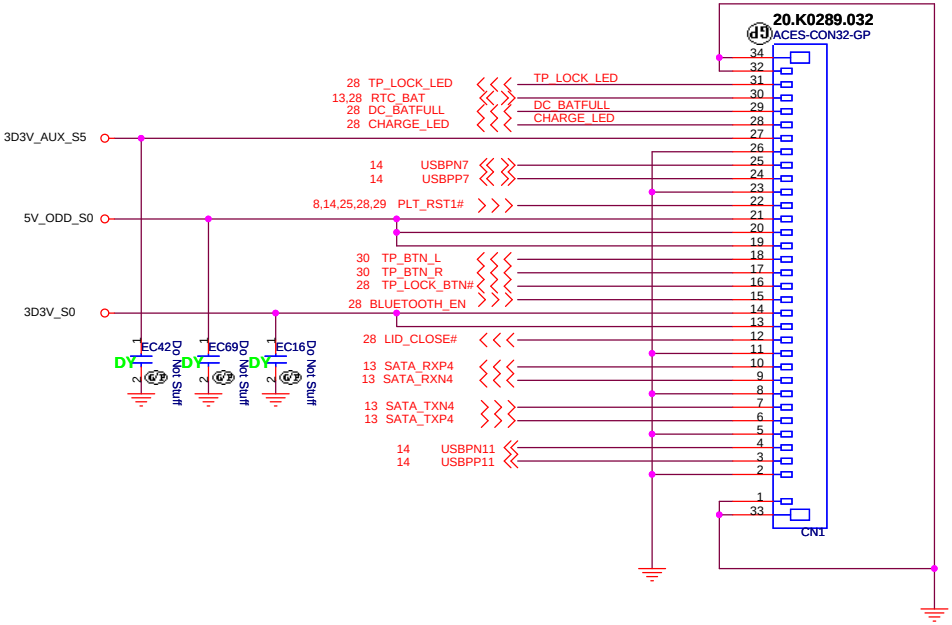
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO JACK*

Size	Document Number	Rev
	JM41/JM51 UMA	-2

Date: Thursday, March 26, 2009 Sheet 23 of 40



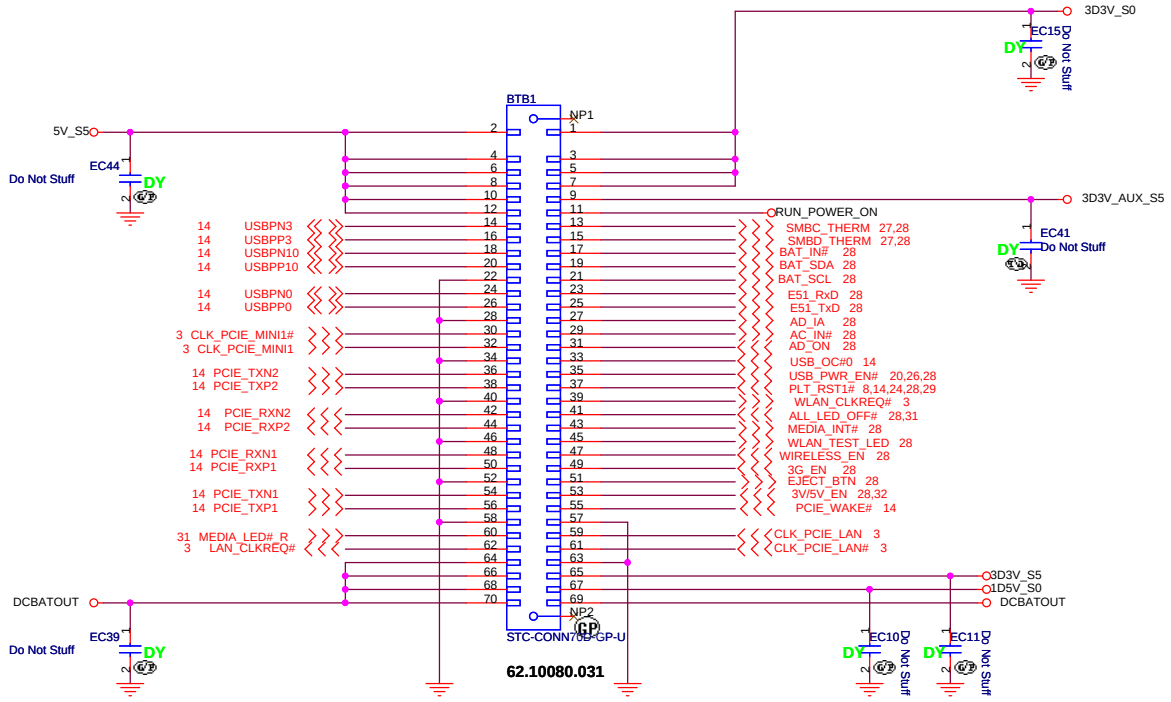
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CARDREADER BD CONN*

Size	Document Number	Rev
	JM41/JM51 UMA	-2

Date: Thursday, March 26, 2009 Sheet 24 of 40



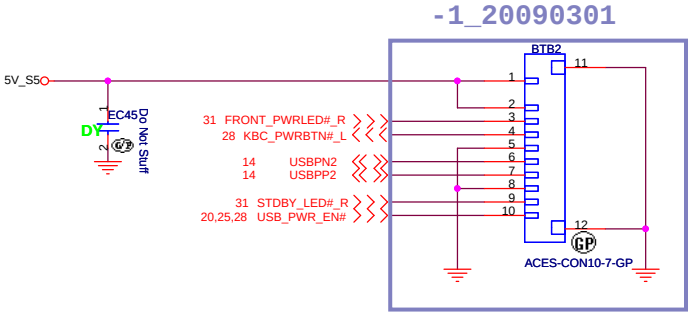
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINI BD CONN***

Size	Document Number	Rev
A3	JM41/JM51_UMA	-2

Date: Monday, March 30, 2009 Sheet 25 of 40



20.F0866.010
2ND = 20.F1261.010

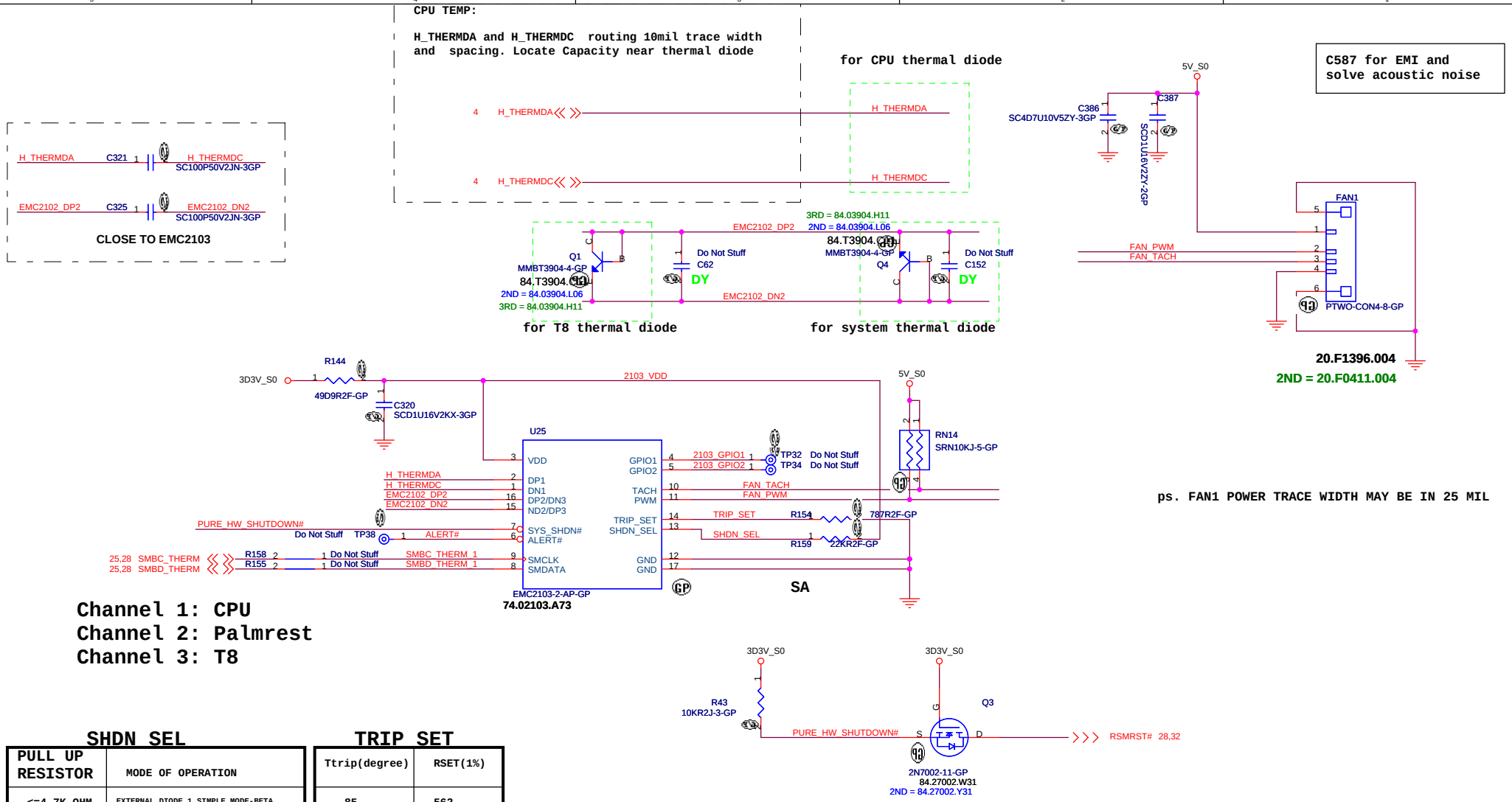
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER BUTTON CONN***

Size	Document Number	Rev
A3	JM41/JM51_UMA	-2

Date: Thursday, March 26, 2009 Sheet 26 of 40



SHDN_SEL

PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED,REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED,REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED

TRIP_SET

Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

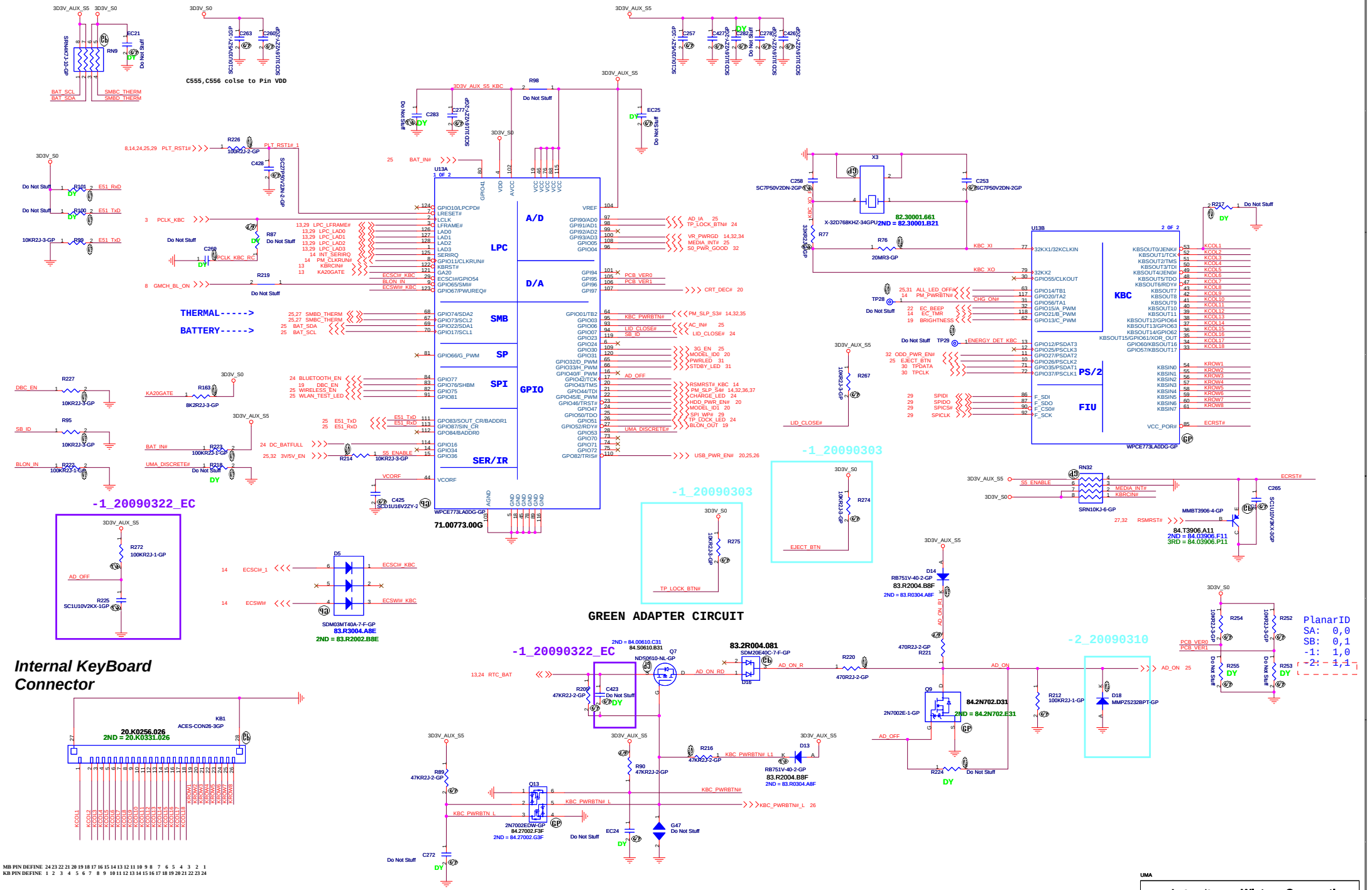
UMA

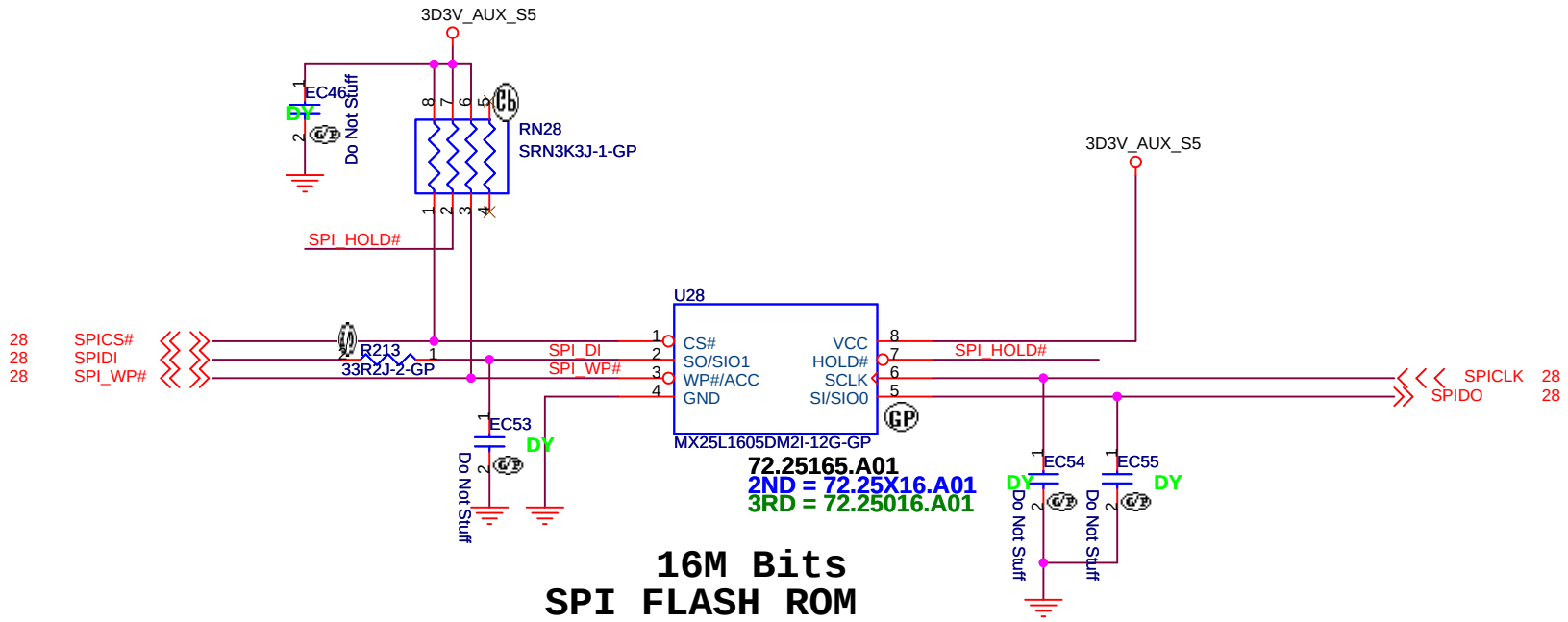
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size | Document Number: JM41/JM51_UMA | Rev: -2

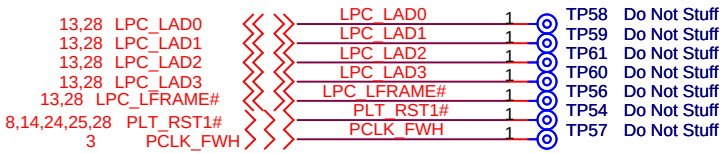
Date: Monday, March 30, 2009 | Sheet 27 of 40

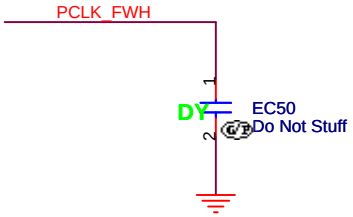

C555,C556 colse to Pin VDD
U13A
WPCE773LA0DG-GP
71.00773.00G
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
THERMAL----->
BATTERY----->
U13B
KBC
PS/2
FIU
WPCE773LA0DG-GP
X3
X-32D768KHZ-34GPU
82.30001.661
2ND = 82.30001.B21
20MR3-GP
-1_20090322_EC
-1_20090303
-2_20090310
GREEN ADAPTER CIRCUIT
Internal KeyBoard Connector
KB1
ACES-CON26-3GP
20.K0256.026
2ND = 20.K0331.026
MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
K/B
24 1
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-2: 1,1
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC WPC773
Size A2
Document Number
JM41/JM51 UMA
Rev -2
Date: Monday, March 30, 2009
Sheet 28 of 40



16M Bits
SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD

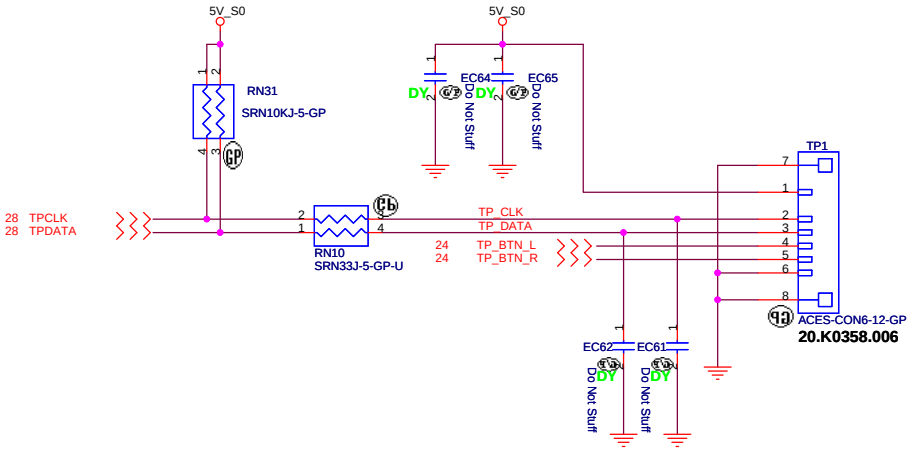




UMA

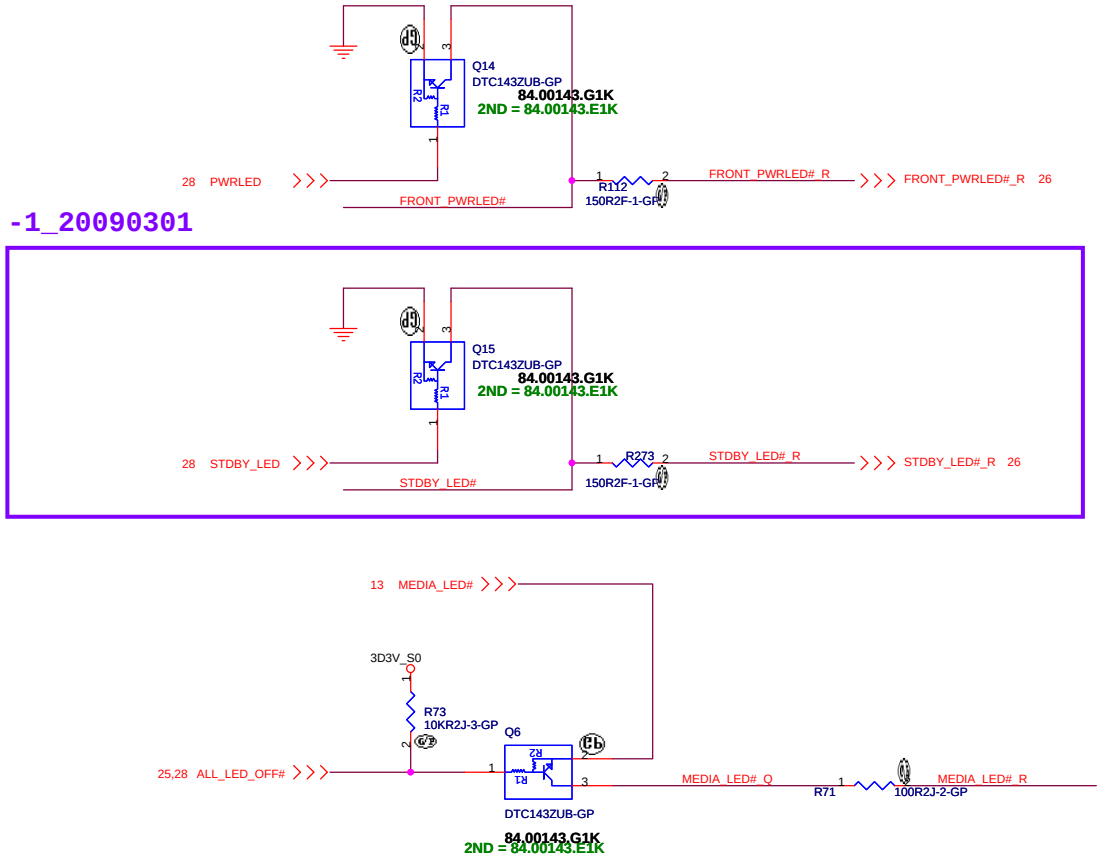
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BIOS***	
Size	Document Number **JM41/JM51 UMA**	Rev -2
Date: Monday, March 30, 2009	Sheet 29 of 40	

TOUCH PAD



UMA

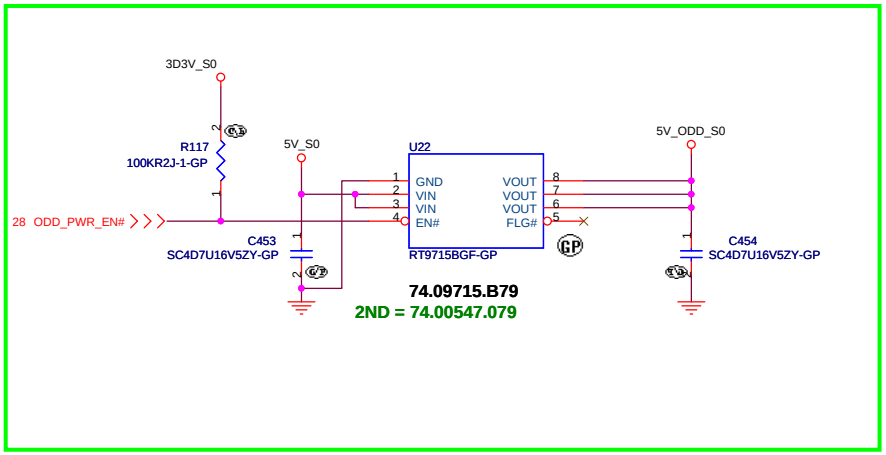
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*Touch PAD*	
Size	Document Number JM41/JM51 UMA	Rev -2
Date: Thursday, March 26, 2009	Sheet 30 of 40	



UMA

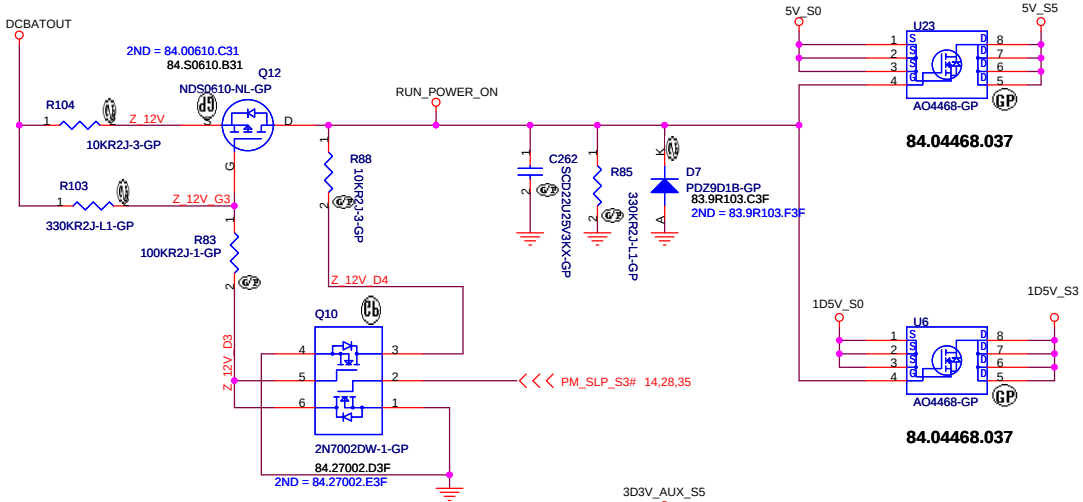
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LED**	
Size	Document Number **JM41/JM51_UMA**	Rev -2
Date: Thursday, March 26, 2009	Sheet 31 of 40	

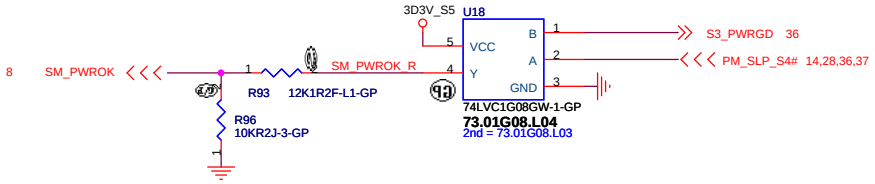
ODD Power

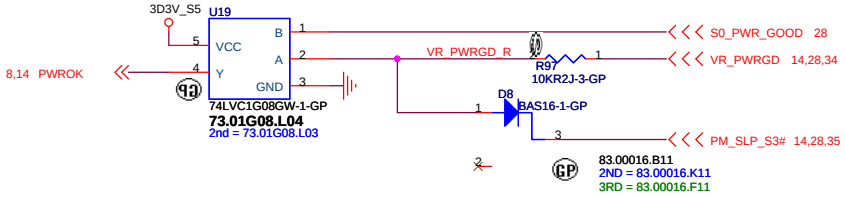


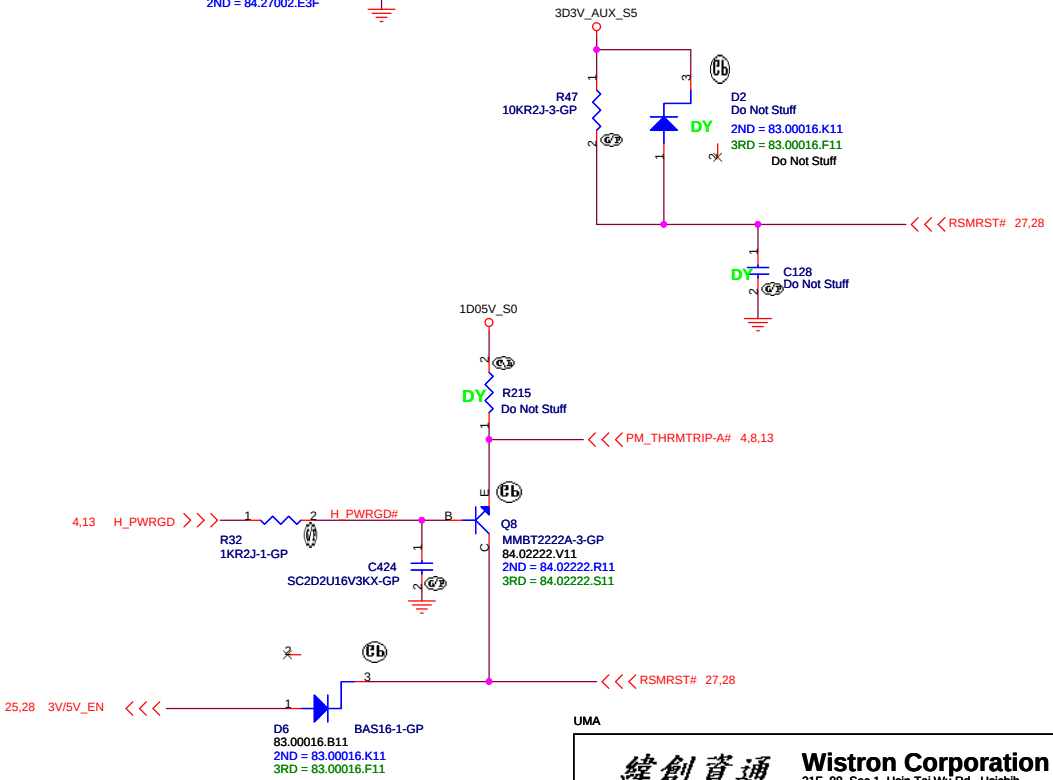
-2_20090310

Run Power



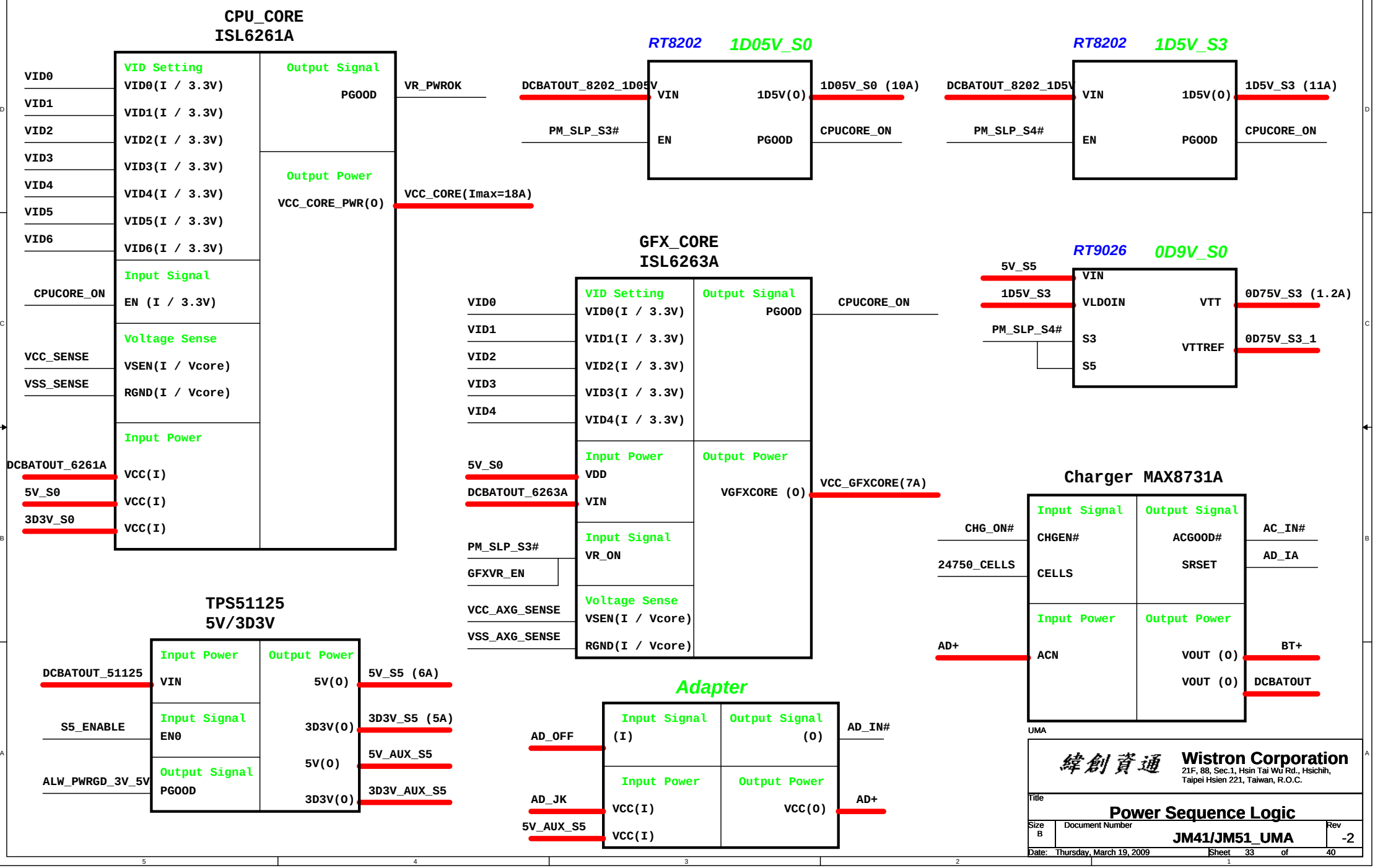


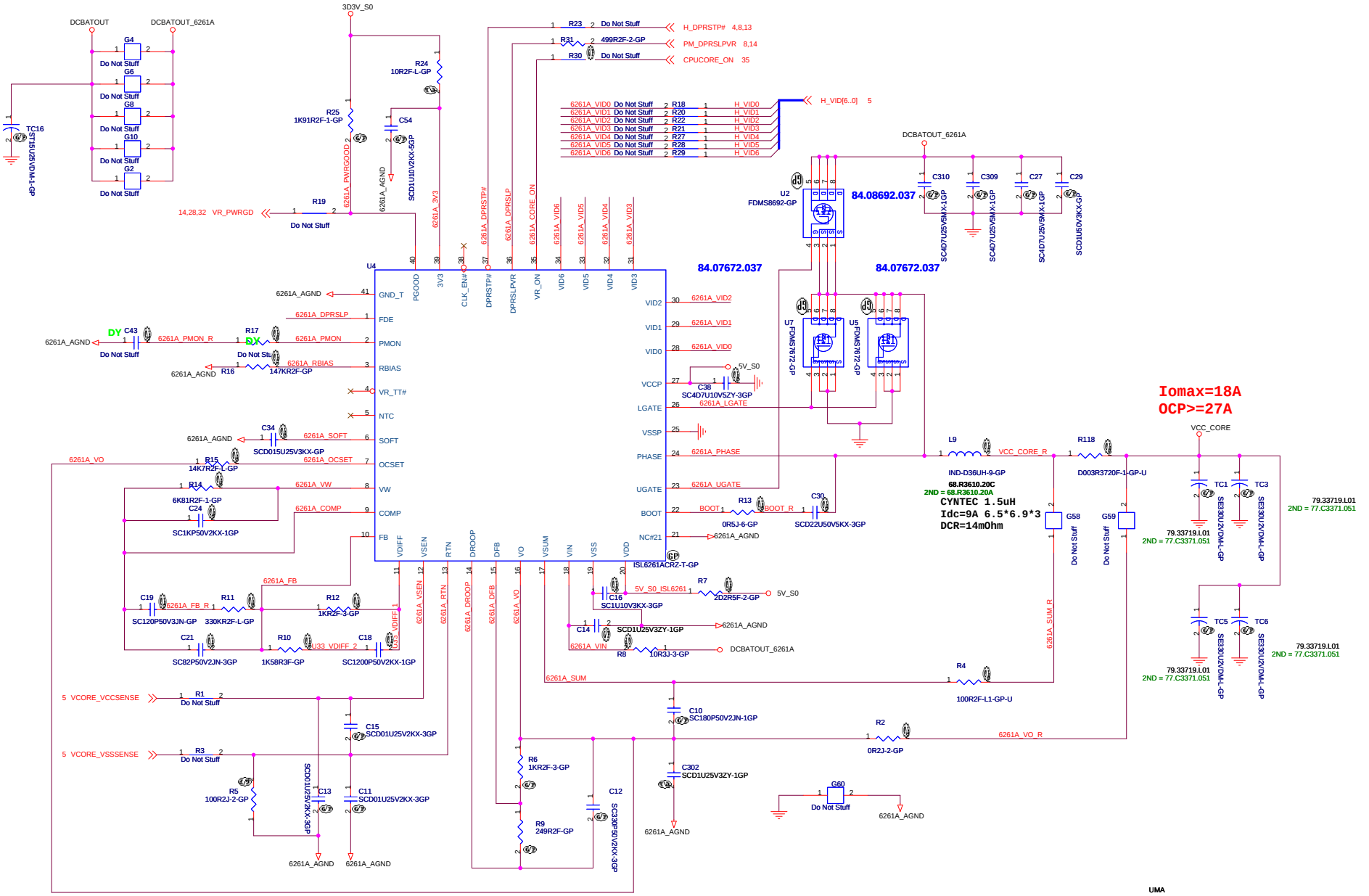


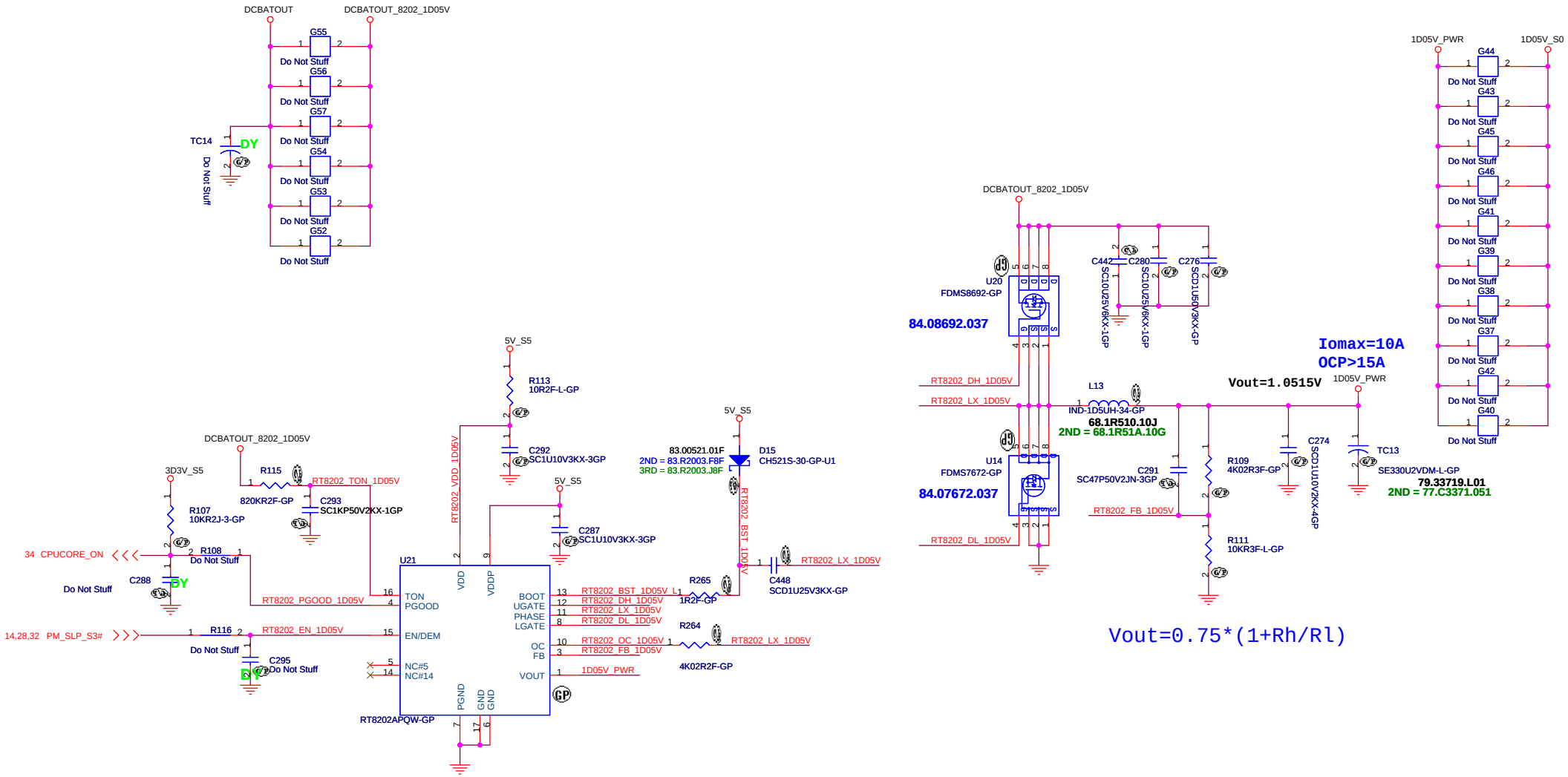


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**RUN & ODD POWER**	
Size	Document Number **JM41/JM51_UMA**	Rev -2
Date: Thursday, March 26, 2009	Sheet 32 of 40	


CPU_CORE
ISL6261A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6261A
5V_S0
3D3V_S0
VR_PWROK
VCC_CORE(Imax=18A)
RT8202
1D05V_S0
VIN
EN
1D5V(O)
PGOOD
DCBATOUT_8202_1D05V
PM_SLP_S3#
1D05V_S0 (10A)
CPUCORE_ON
RT8202
1D5V_S3
VIN
EN
1D5V(O)
PGOOD
DCBATOUT_8202_1D5V
PM_SLP_S4#
1D5V_S3 (11A)
CPUCORE_ON
GFX_CORE
ISL6263A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Input Power
VDD
VIN
Input Signal
VR_ON
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Output Signal
PGOOD
Output Power
VGFXCORE (O)
VID0
VID1
VID2
VID3
VID4
5V_S0
DCBATOUT_6263A
PM_SLP_S3#
GFXVR_EN
VCC_AXG_SENSE
VSS_AXG_SENSE
CPUCORE_ON
VCC_GFXCORE(7A)
RT9026
0D9V_S0
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D5V_S3
PM_SLP_S4#
0D75V_S3 (1.2A)
0D75V_S3_1
Charger MAX8731A
Input Signal
CHGEN#
CELLS
Output Signal
ACGOOD#
SRSET
Input Power
ACN
Output Power
VOUT (O)
VOUT (O)
CHG_ON#
24750_CELLS
AD+
AC_IN#
AD_IA
BT+
DCBATOUT
UMA
TPS51125
5V/3D3V
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)
DCBATOUT_51125
S5_ENABLE
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (5A)
5V_AUX_S5
3D3V_AUX_S5
Adapter
Input Signal
(I)
Output Signal
(O)
Input Power
VCC(I)
VCC(I)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Sequence Logic
Size
B
Document Number
JM41/JM51_UMA
Rev
-2
Date: Thursday, March 19, 2009
Sheet 33 of 40


DCBATOUT
DCBATOUT_6261A
3D3V_S0
U4
ISL6261ACRZ-T-GP
U2
FDMS8692-GP
84.08692.037
84.07672.037
84.07672.037
U7
FDMS7672-GP
U5
FDMS7672-GP
Iomax=18A
OCP>=27A
VCC_CORE
L9
IND-D36UH-9-GP
68.R3610.20C
2ND = 68.R3610.20A
CYNTEC 1.5uH
Idc=9A 6.5*6.9*3
DCR=14mOhm
R118
D003R3720F-1-GP-U
79.33719.L01
2ND = 77.C3371.051
SB_20090203
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6261A CPU CORE
Size
Custom
Document Number
JM41/JM51 UMA
Rev
-2
Date: Monday, March 30, 2009
Sheet 34 of 40



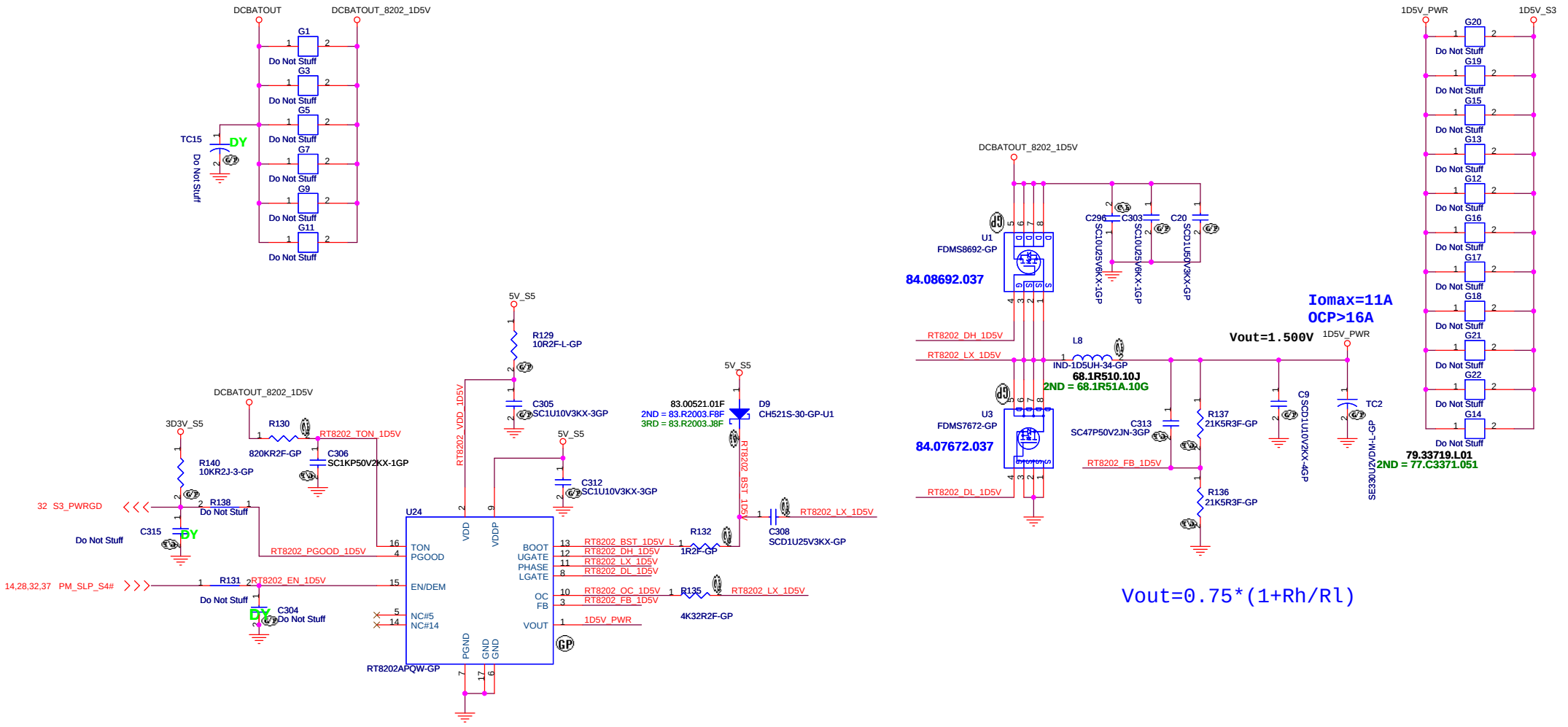
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RT8202_1D05V***

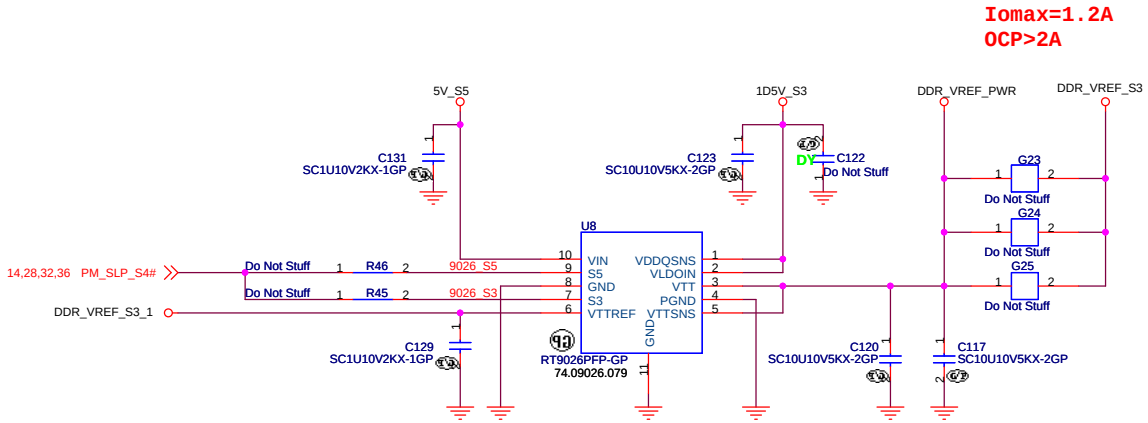
Size	Document Number	Rev
A3	JM41/JM51_UMA	-2

Date: Thursday, March 26, 2009 Sheet 35 of 40



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RT8202 1D5V***	
Size A3	Document Number **JM41/JM51 UMA**	Rev **-2**
Date: Thursday, March 26, 2009	Sheet 36 of 40	



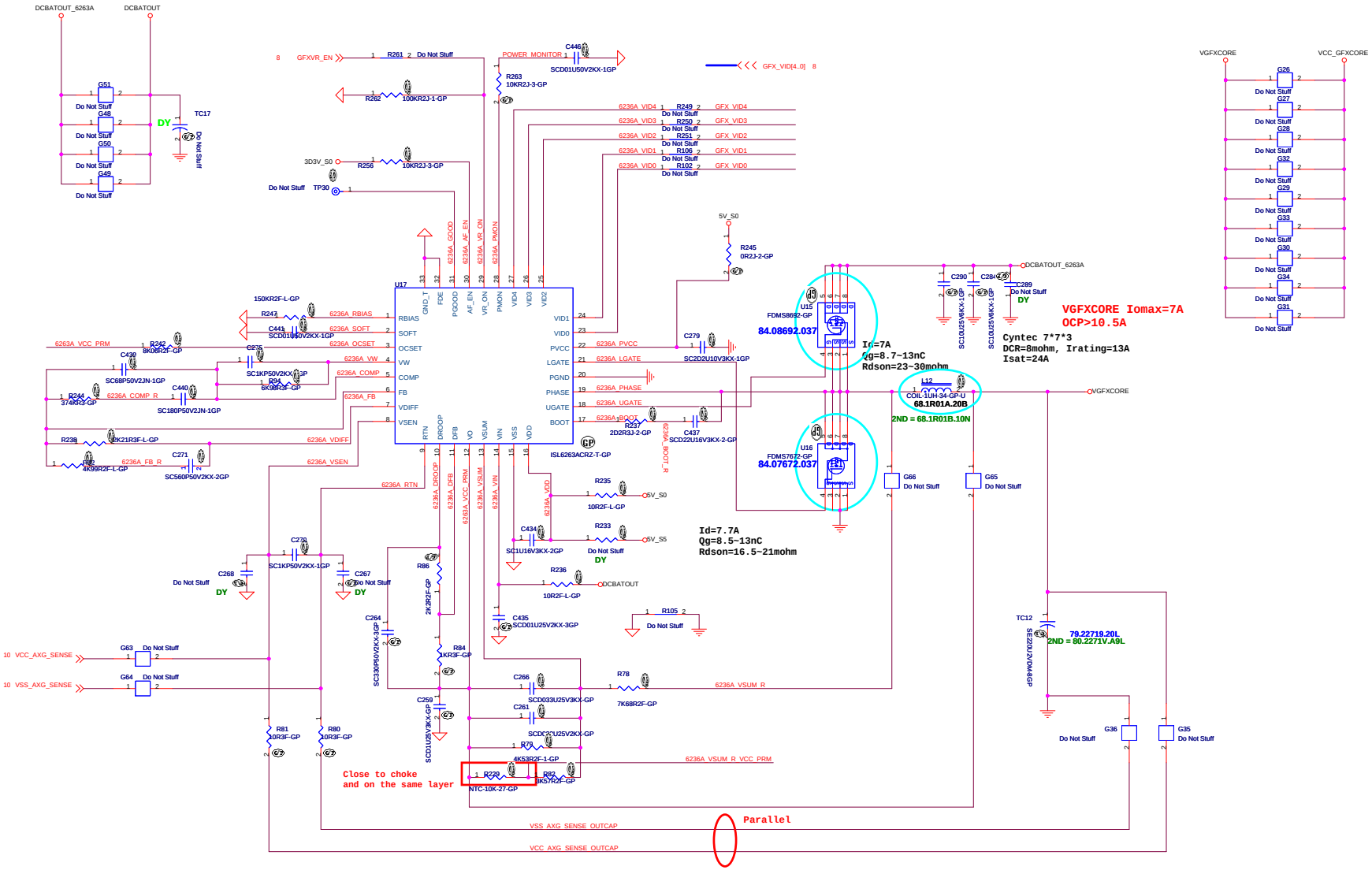
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RT9026_0D75V***

Size	Document Number	Rev
A3	JM41/JM51_UMA	-2

Date: Thursday, March 26, 2009 Sheet 37 of 40



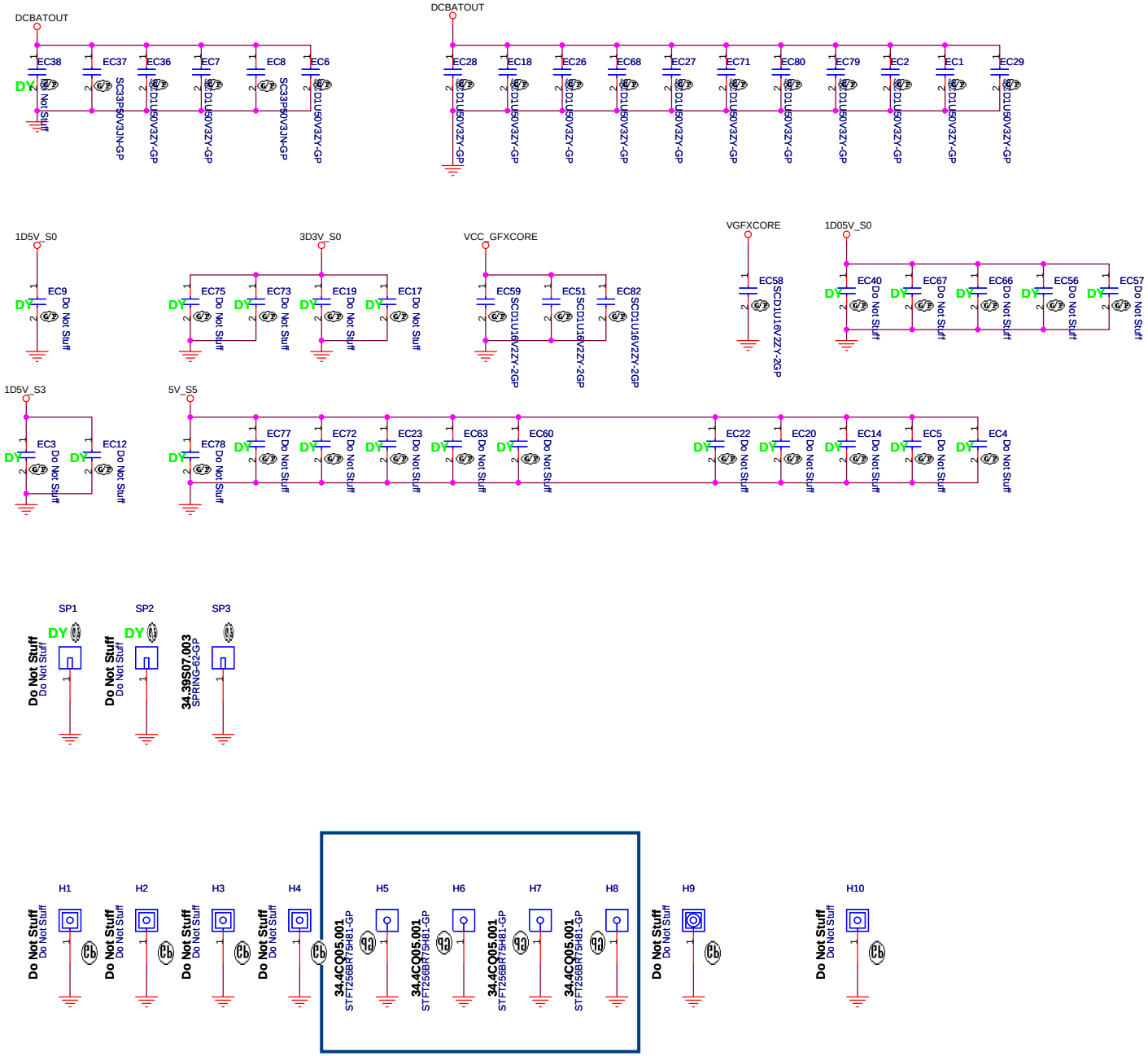
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6263A GFX CORE

Size: A2 | Document Number: JM41/JM51 UMA | Rev: -2

Date: Thursday, March 26, 2009 | Sheet 38 of 40



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size | Document Number: **JM41/JM51 UMA** | Rev: -2

Date: Thursday, March 26, 2009 | Sheet 39 of 40

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HISTORY***

Size	Document Number	Rev
A2	JM41/JM51_UMA	-2

Date: Thursday, March 19, 2009 Sheet 40 of 40