

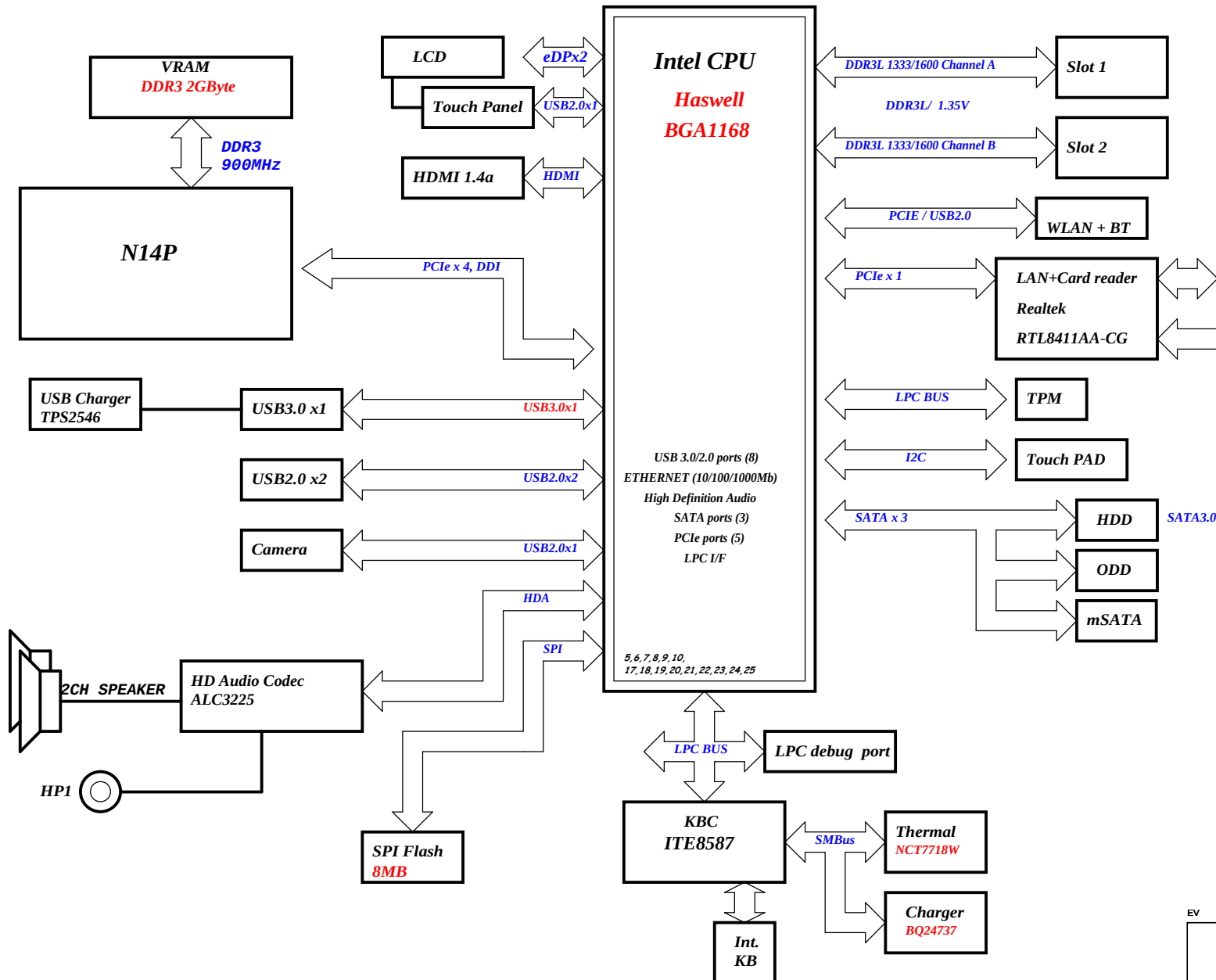
EA40_HU_ULT
Schematics Document

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EV			A		
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Title					
Cover Page					
Size	Document Number				Rev
A3	EA40 HW ULT				1
Date:	Monday, May 13, 2013		Sheet	1	of 102
			1		

EA40-HW ULV Board Block Diagram

Project code : 91.4YN01.001
PCB P/N : 12243
Revision : 1



CHARGER	
BQ24737	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
TPS51225	45
INPUTS	OUTPUTS
DCBATOUT	5V_Charger 3D3V_S5
CPU DC/DC	
TPS51622	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
SYS8208A	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
RT8207	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
SYSTEM DC/DC	
SYW232	50
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0
SYSTEM DC/DC	
SYW232	51
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0
TPS51728RHAR	
82	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
Switches	
83	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D8V_S0	1D8V_VGA_S0
1V_S0	1V_VGA_S0
TPS51728RHAR	
83	
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0
PCB LAYER	
L1:Top L2:VCC L3:Signal L4:Signal L5:GND L6:Bottom	

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Block Diagram	
Size	Document Number
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Date: Monday, May 13, 2013	Sheet 2 of 102
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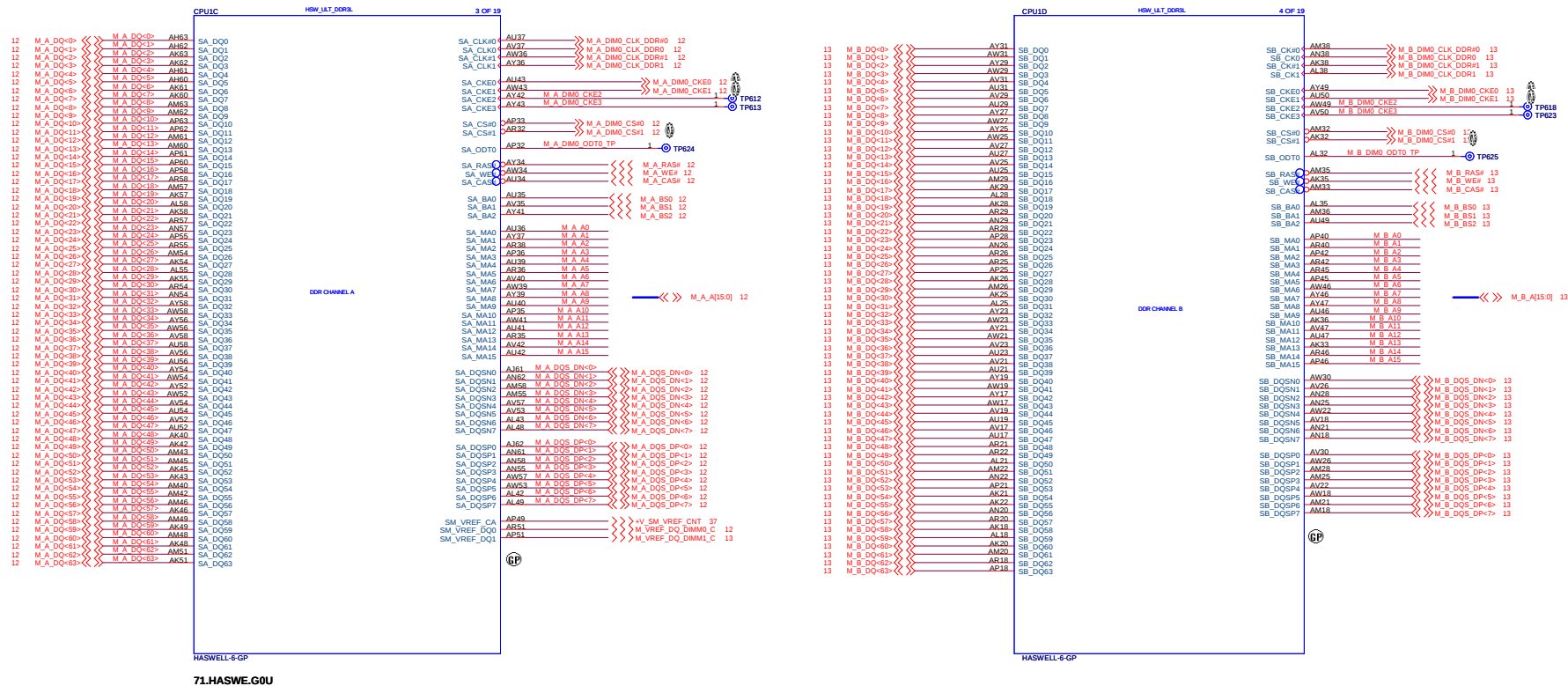
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SSID = CPU

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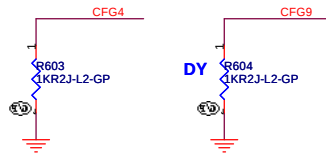
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Title			
CPU (Reserved)			
Size	Document Number		Rev
A3	EA40 HW ULT		1
Date:	Monday, May 13, 2013	Sheet	3 of 102

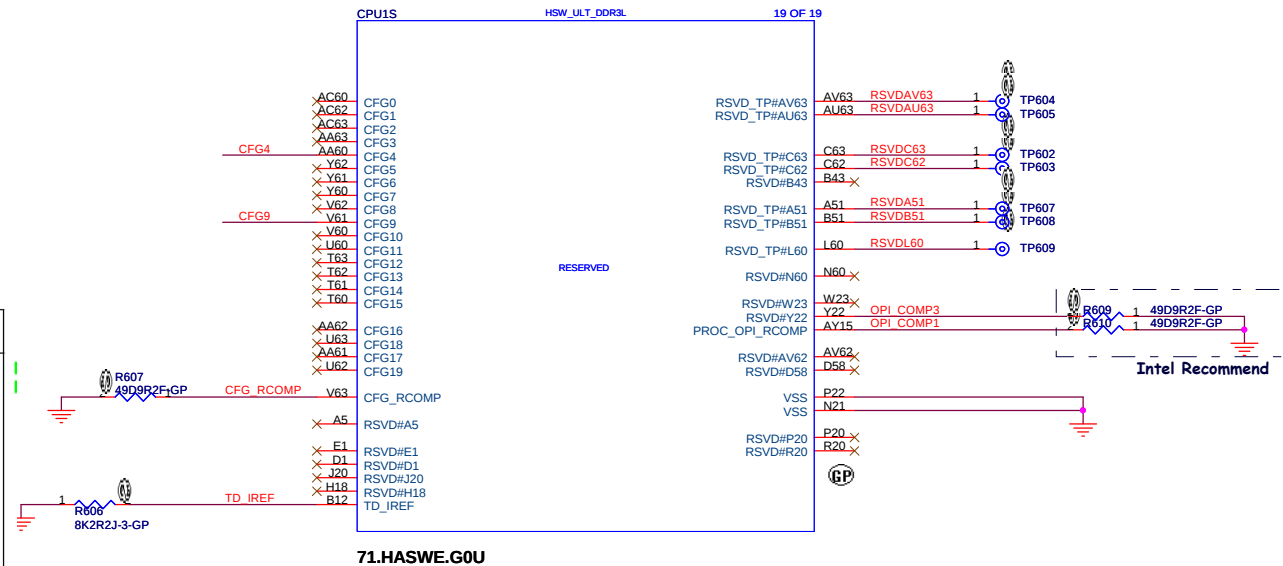


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eDP Enable	
CFG4	1:Disable 9:Enable



Signal Name	Description	Direction/Buffer Type
CFG[19:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. - CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes. - PCI Express* Static x16 Lane Numbering Reversal. — — • - CFG[4]: eDP enable 1 = Disabled 0 = Enabled [19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	—
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	
continued...		



7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left unconnected

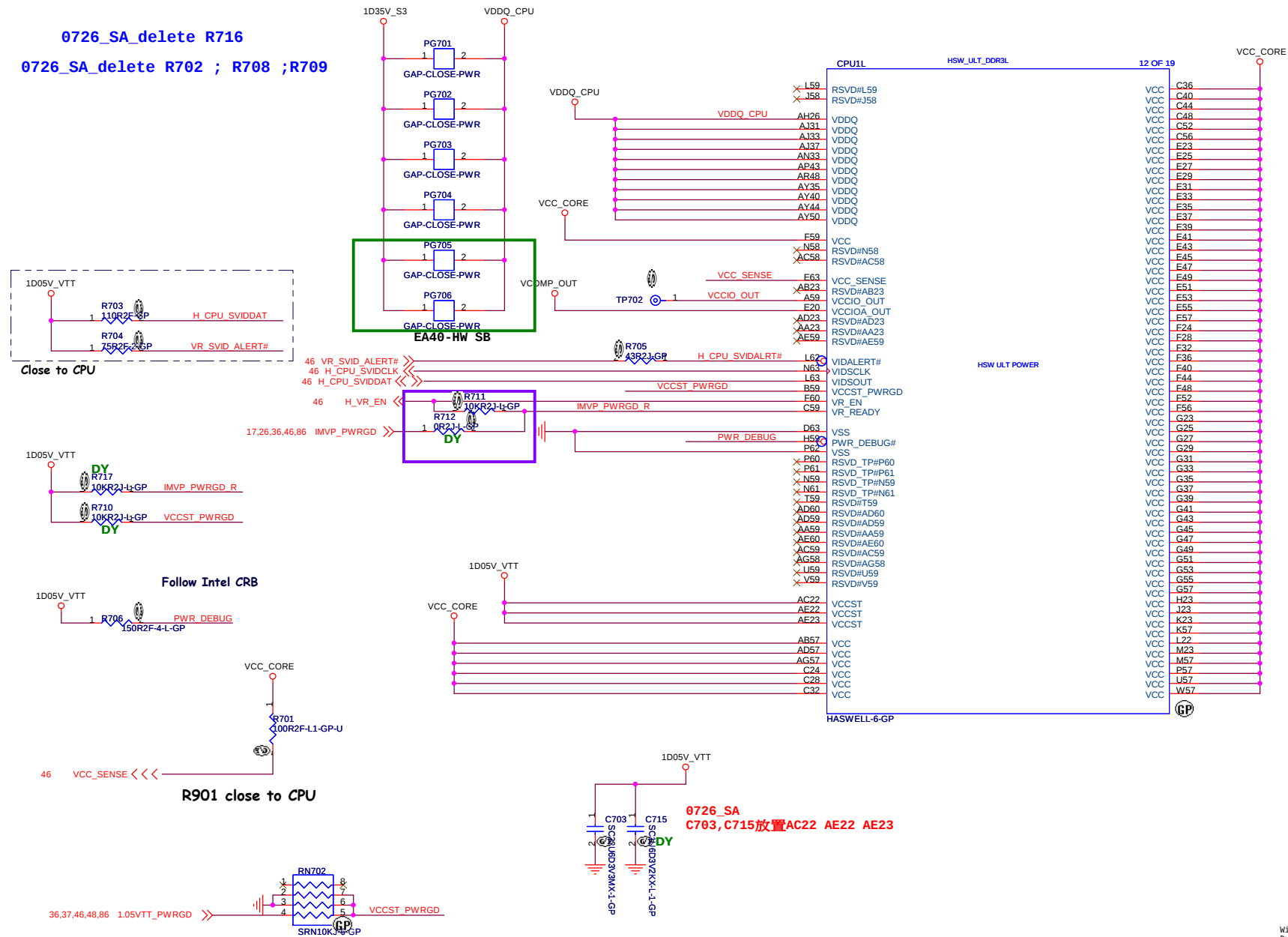
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Title			
CPU (CFG)			
Size Custom	Document Number	Rev	1
EA40 HW ULT			
Date: Monday, May 13, 2013	Sheet 6	of	102

SSID = CPU

0726_SA_delete R716

```
0726_SA_delete R702 ; R708 ;R709
```



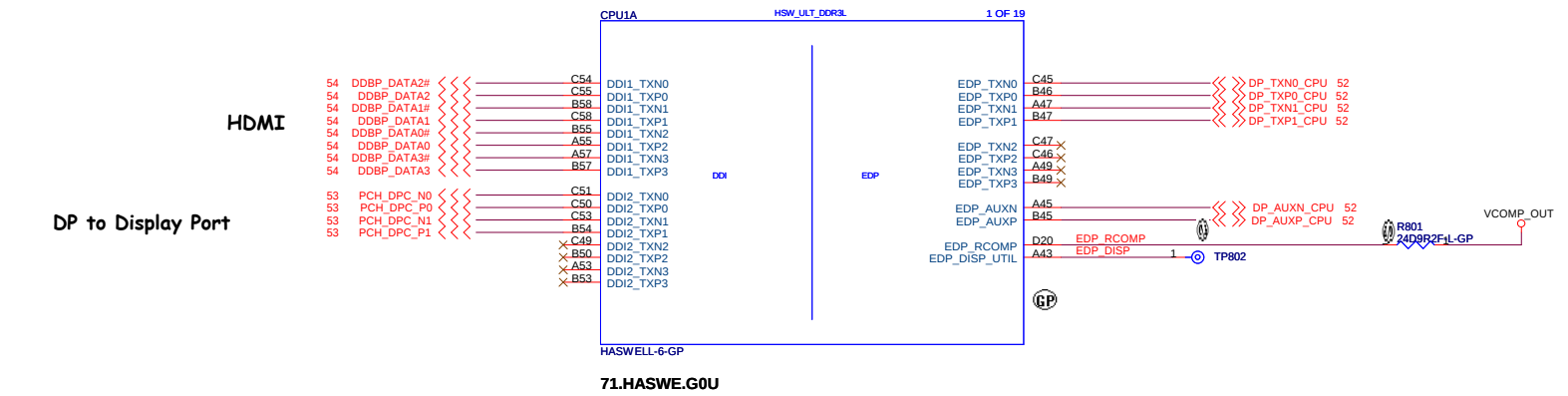
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Title			
CPU (VCC CORE)			
Size A3	Document Number		Rev
	EA40 HW ULT		1
Date:	Monday, May 13, 2013	Sheet 7 of	102

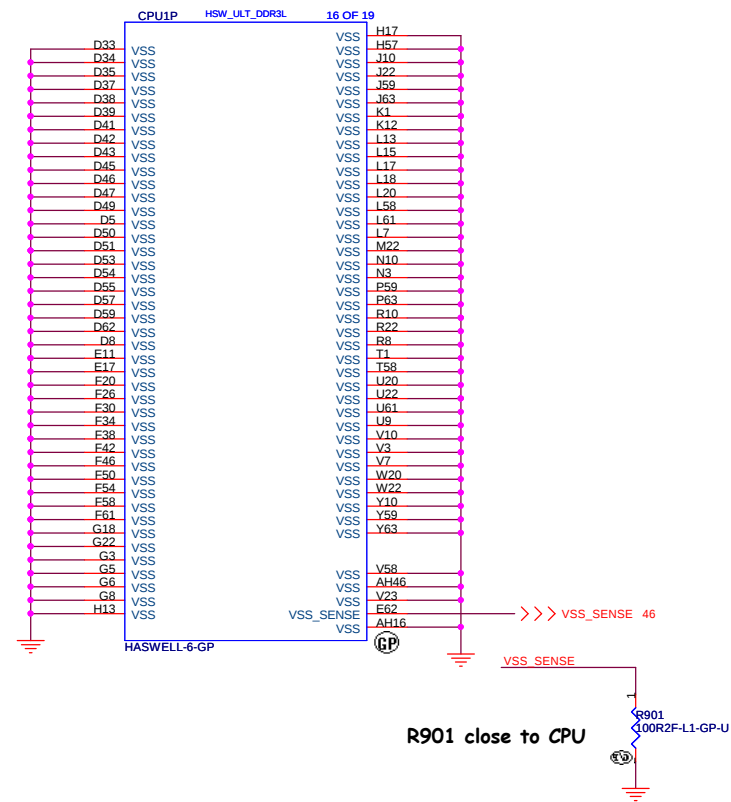
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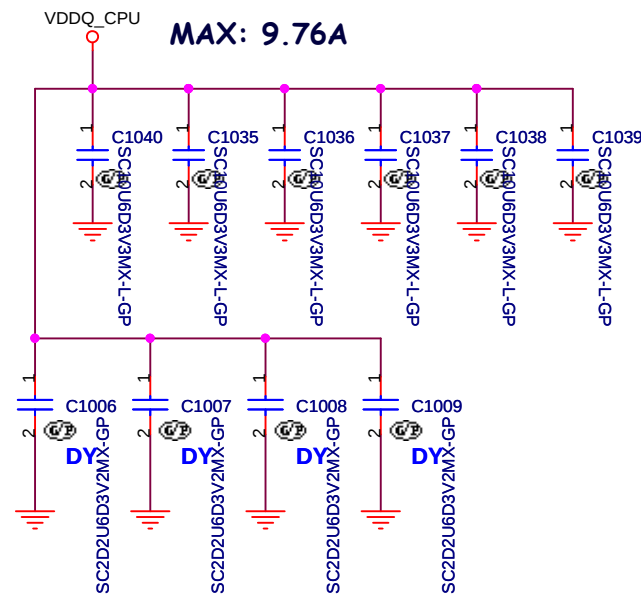


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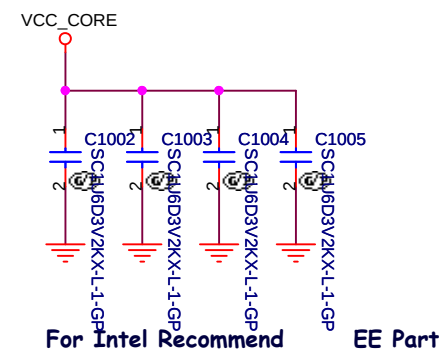
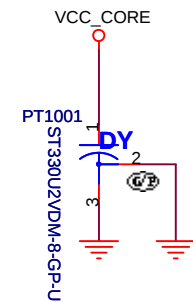
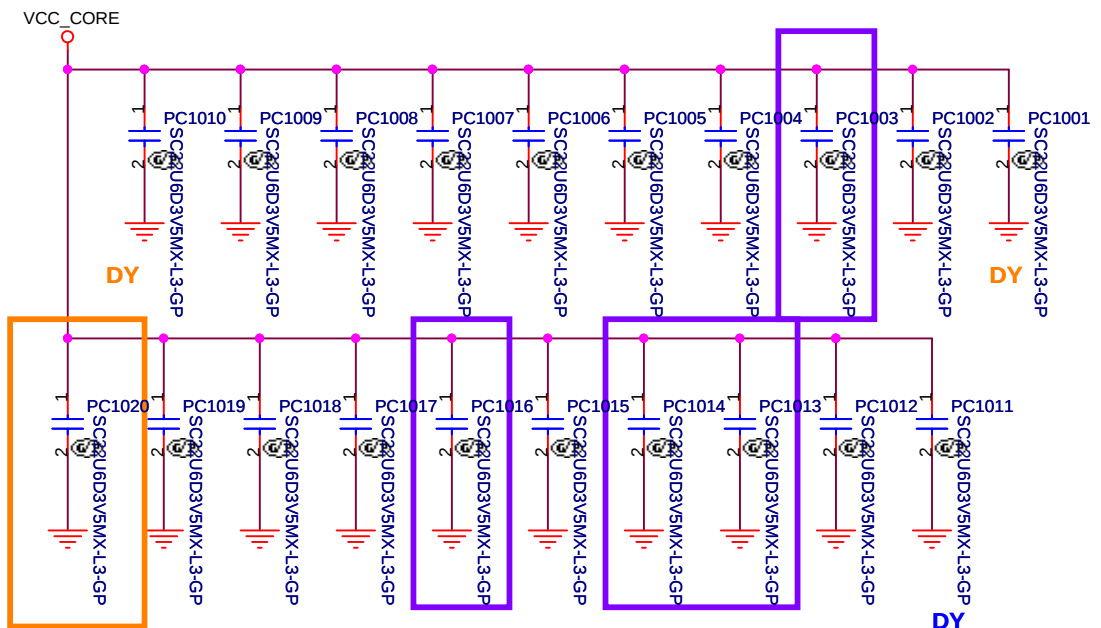
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title					
CPU (DDI/EDP)					
Size	Custom	Document Number	EA40 HW ULT		Rev
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SSID = CPU





For Intel Recommend EE Part

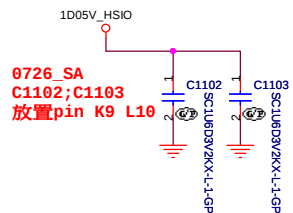


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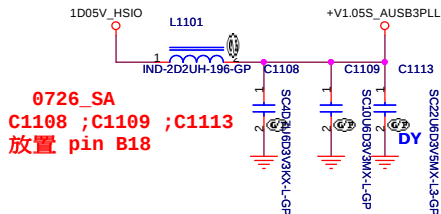
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Title	
CPU (Power CAP1)	
Size	Document Number
A4	EA40 HW ULT
Date:	Thursday, June 06, 2013
Sheet	10 of 102
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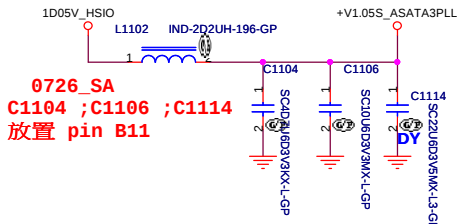
0726_SA 擺放電容的位置請參考Page 21
每個位置如下



0726_SA
C1102;C1103
放置pin K9 L10

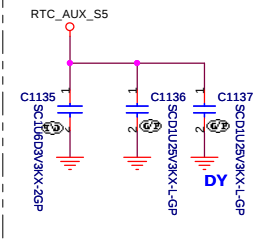


0726_SA
C1108 ;C1109 ;C1113
放置 pin B18

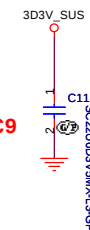


0726_SA
C1104 ;C1106 ;C1114
放置 pin B11

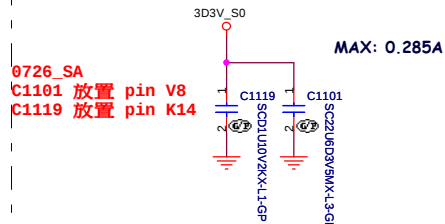
0726_SA DY C1137



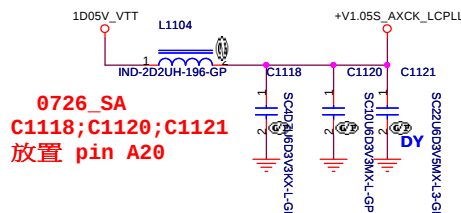
0726_SA
C1135;C1136;C1137
放置 pin AG10



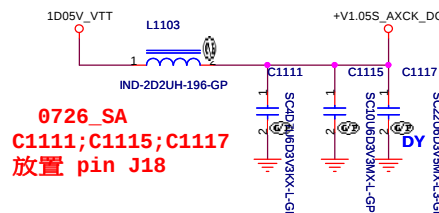
0726_SA
C1116放置 pin AC9



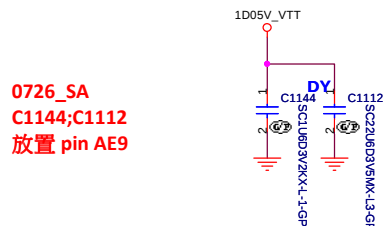
0726_SA
C1101 放置 pin V8
C1119 放置 pin K14



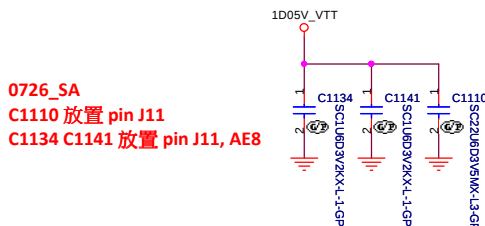
0726_SA
C1118;C1120;C1121
放置 pin A20



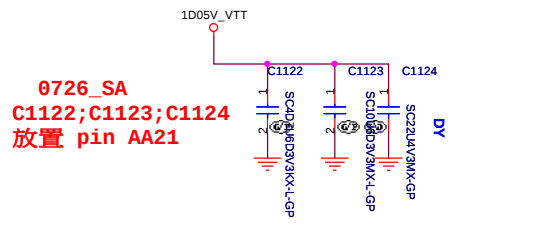
0726_SA
C1111;C1115;C1117
放置 pin J18



0726_SA
C1144;C1112
放置 pin AE9



0726_SA
C1110 放置 pin J11
C1134 C1141 放置 pin J11, AE8



0726_SA
C1122;C1123;C1124
放置 pin AA21

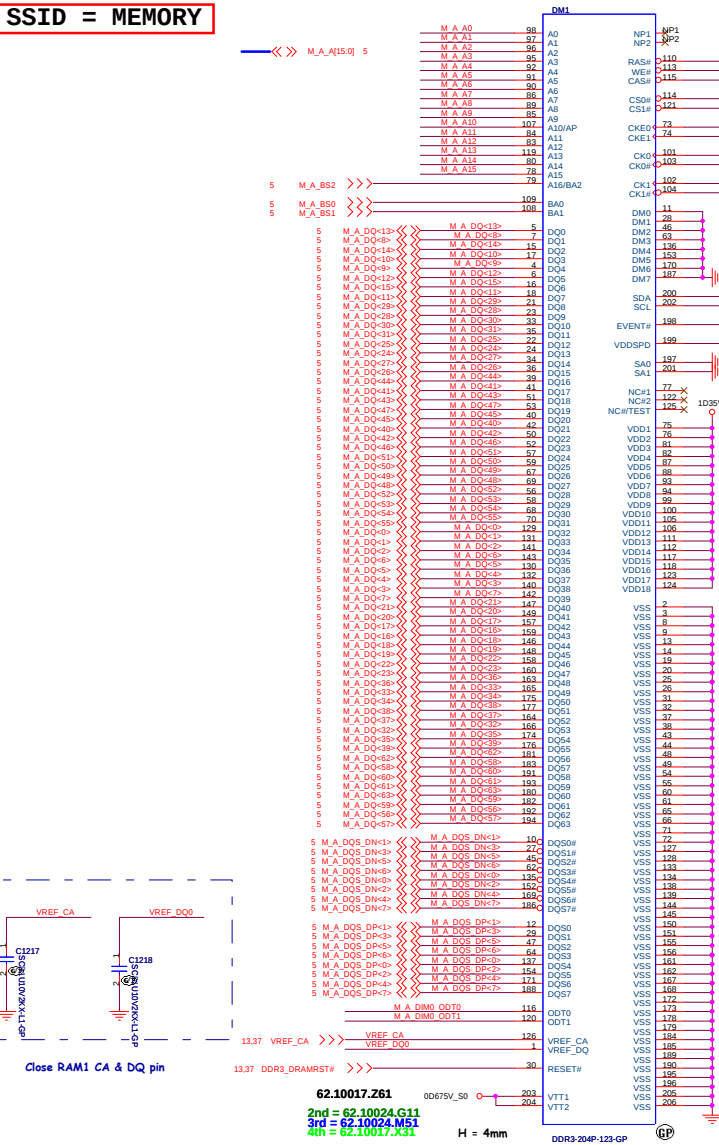
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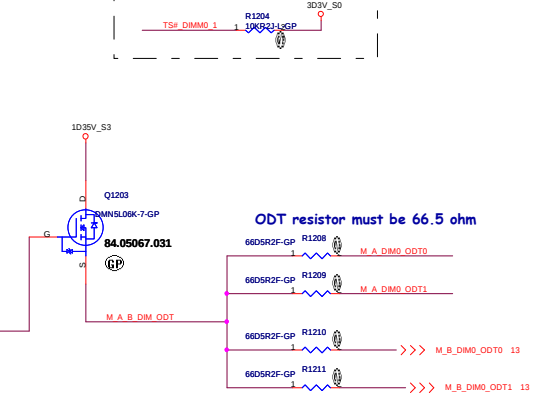
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CPU (Power CAP2)		
Size	Document Number	Rev
Custom	EA40 HW ULT	1
Date:	Monday, May 13, 2013	Sheet 11 of 102

SSID = MEMORY



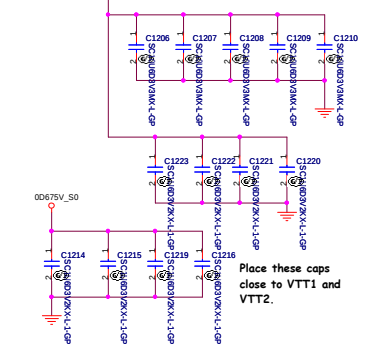
Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30
 If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32

0726_SA	Thermal EVENT
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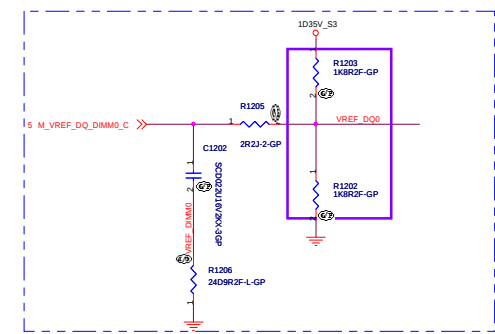


Q1202 Q1203限用於84.05067.031
因為此刻 V_{th} 為1V

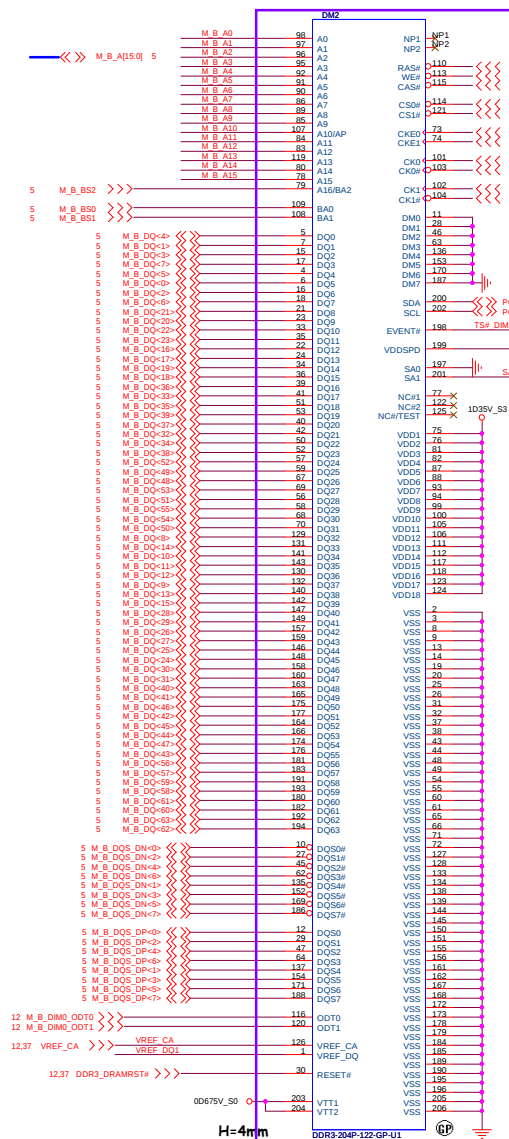
Layout Note:
Place these Caps near
SO-DIMM.



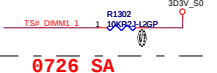
For Intel Recommend Close to DIMM



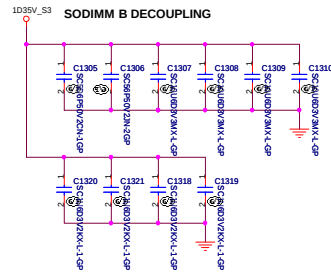
The image shows two circuit diagrams for connecting RAM3 pins. The left diagram, labeled 'VREF CA', shows a capacitor C1302 connected between the CA pin and ground. The right diagram, labeled 'VREF DQ1', shows a capacitor C1304 connected between the DQ1 pin and ground. Both capacitors are 100nF. Below the diagrams, the text 'Close RAM3 CA & DQ pin' is written in blue.



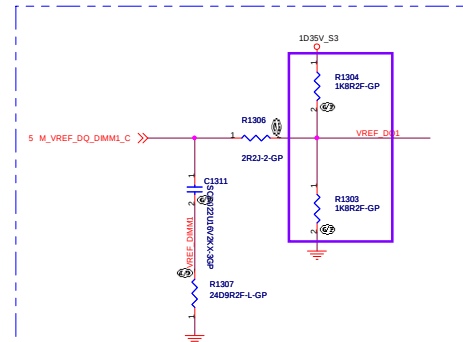
Thermal EVENT



Layout Note:
Place these Caps near
SO-DIMMB.



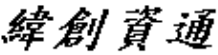
For Intel Recommend Close to DIMM



5	4	3	2	1
D				
C				
B				
A				

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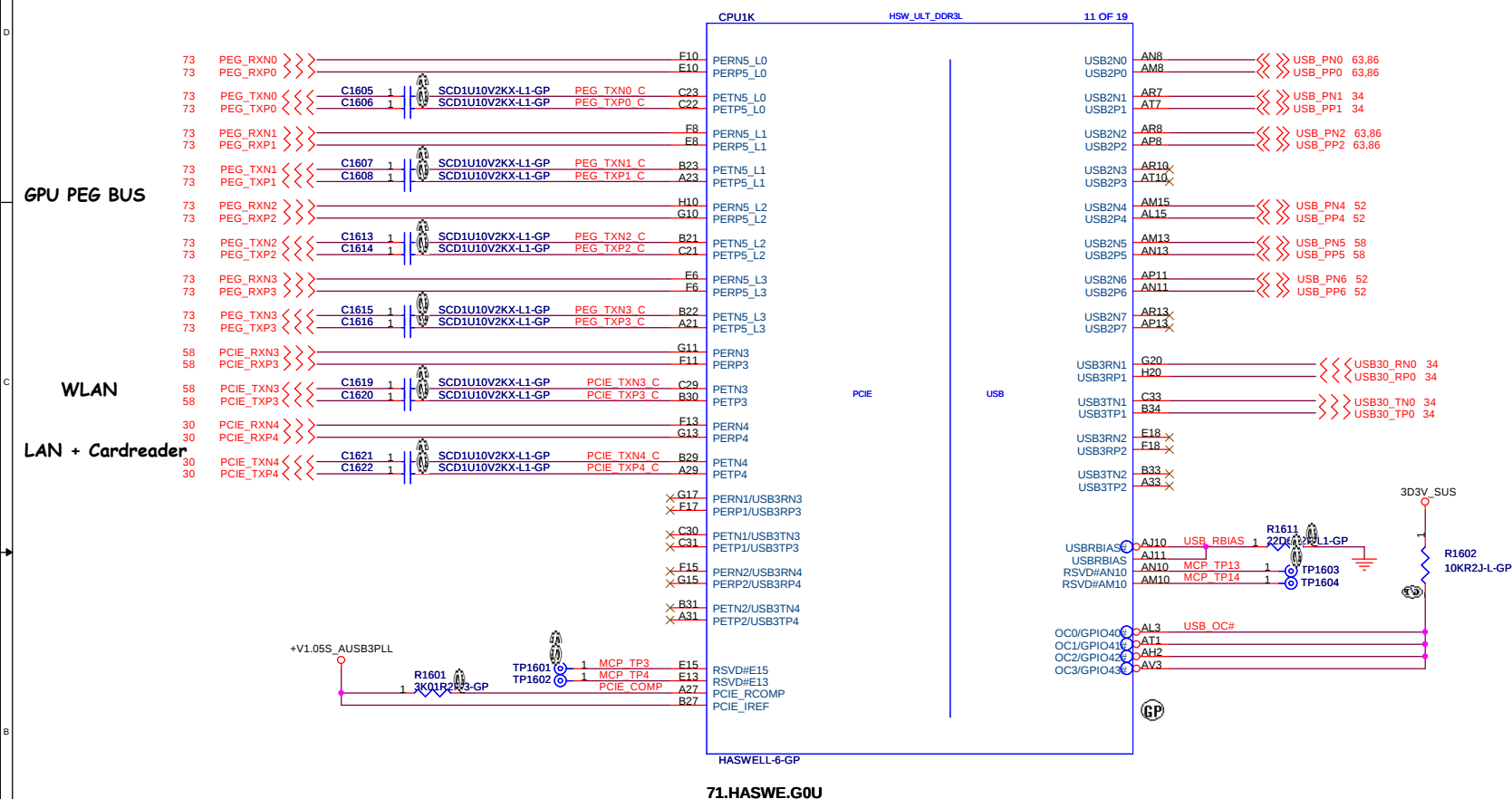
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Title (Reserved) SODIMM SODIMM4		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 14	of 102

SSID = PCH

USB Table

Pair	Device
0	USB2.0 Port 1
1	USB3.0 Port 2(USB2.0)
2	USB2.0 Port 3
3	
4	CCD
5	WLAN(Bluetooth)
6	Touch Penal
7	



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Title

CPU (PCI/USB)

Size
A3

Document Number

EA40 HW ULT

REV
1

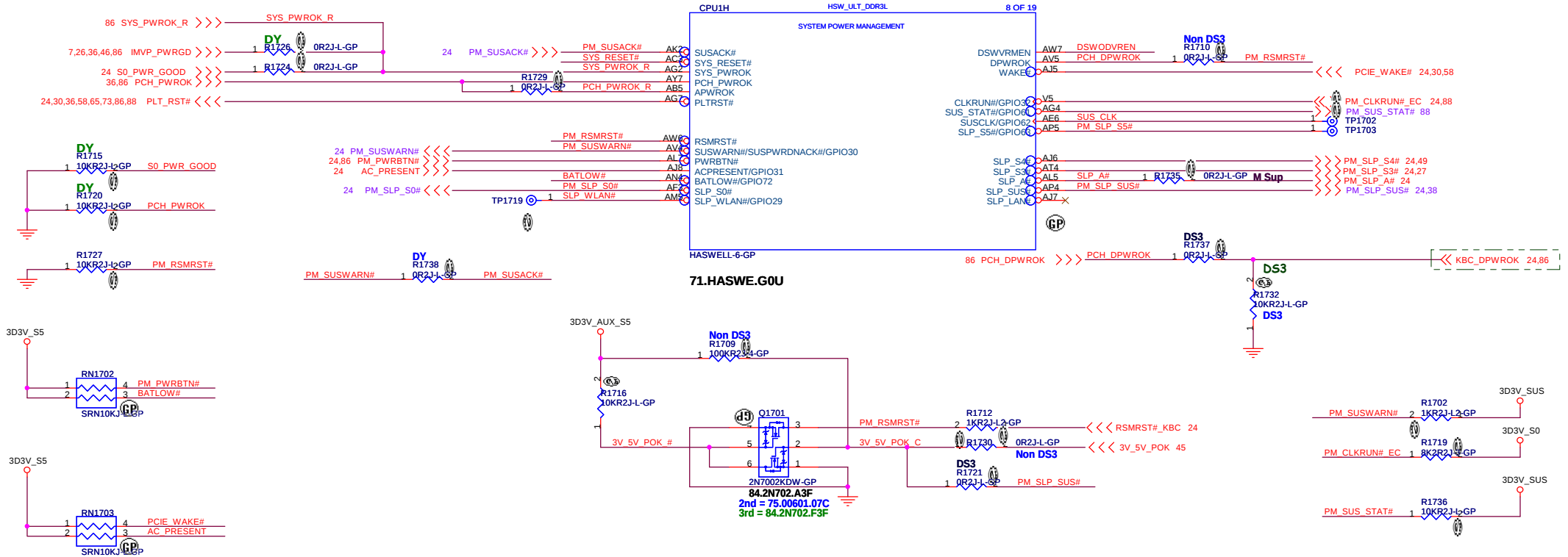
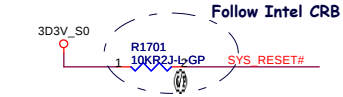
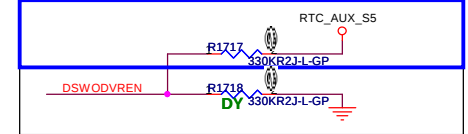
Date: Monday, May 13, 2013

Sheet 16 of 102

SSID = PCH

Bit	Description
31:3	Reserved
2	WAKE# Pin Deep Sx Enable (WAKE_PIN_DSX_EN) - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': - Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. - Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. NOTE: Deep Sx disabled configuration must leave this bit at '0'.

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

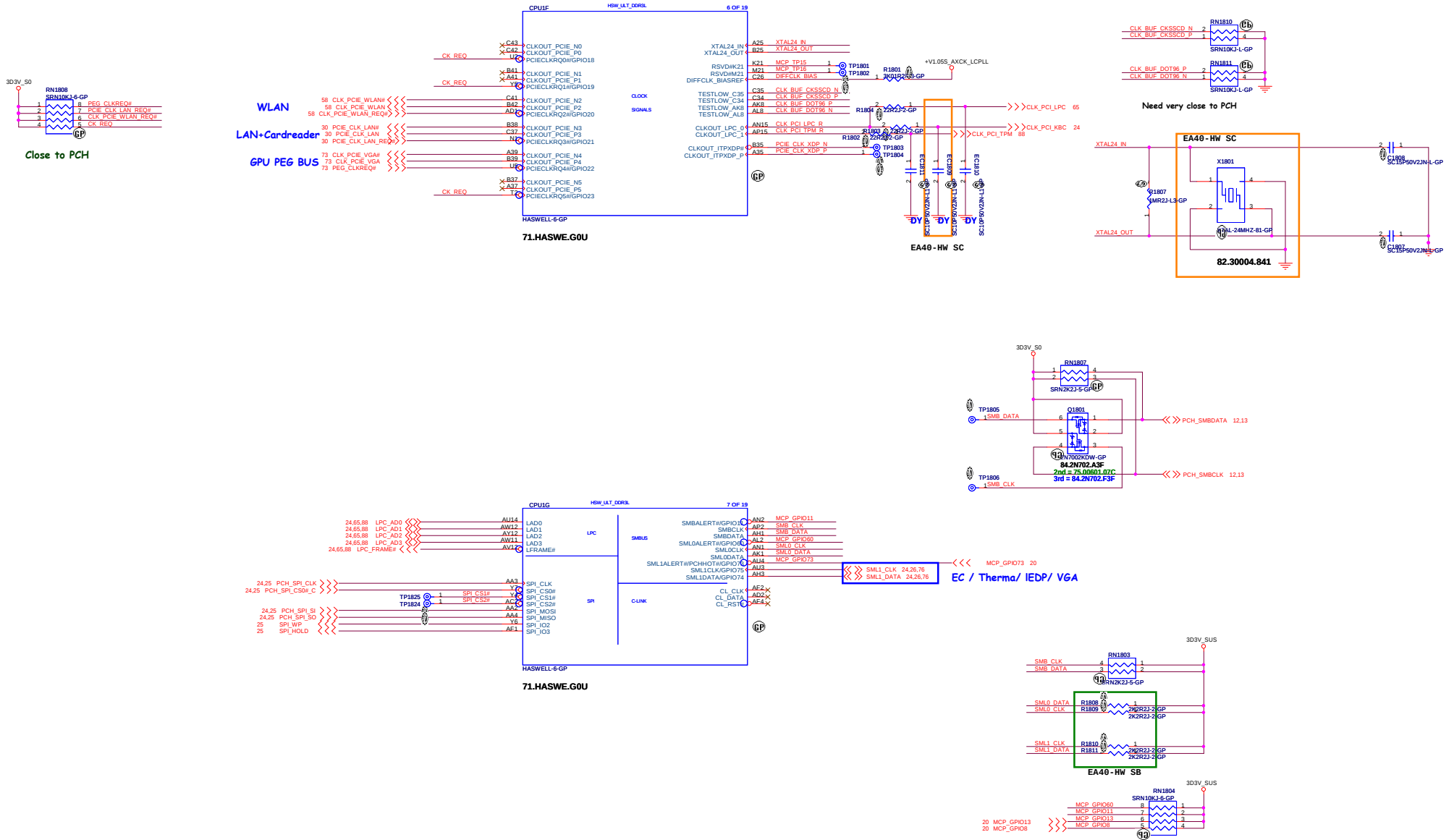


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Title			
CPU (DMI/FDI/PM)			
Size	Document Number	Rev	
A3	EA40 HW ULT	1	
Date:	Monday, May 13, 2013	Sheet	17 of 102

SSID = PCH



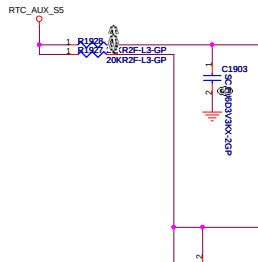
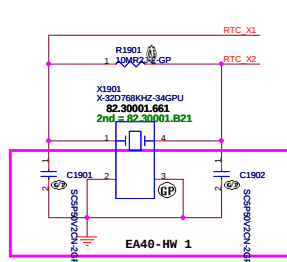
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EV application without get Wistron permission

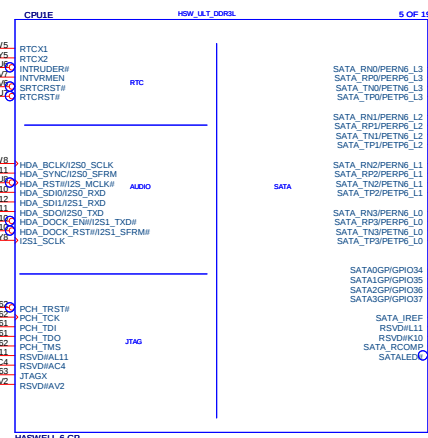
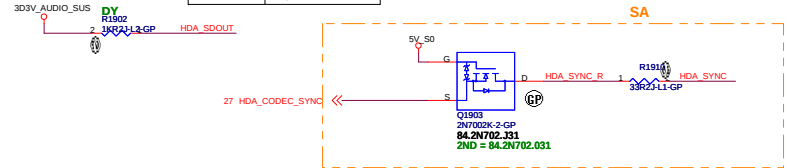
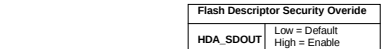
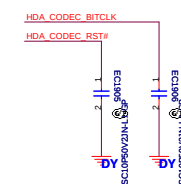
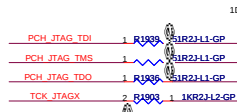
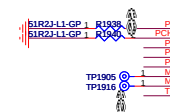
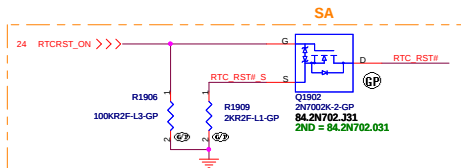
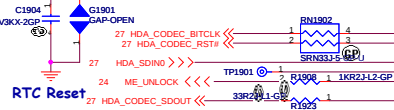
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Title			
CPU (PCI-E/SMBUS/CLOCK/CL)			
Size A2	Document Number	Rev	
	EA40 HW ULT	1	
Date:	Monday, May 13, 2013	Sheet	18 of 102

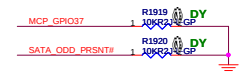
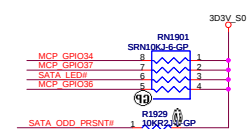
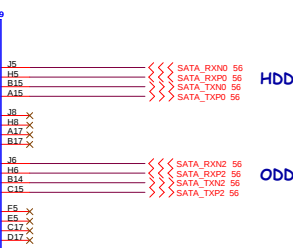
SSID = PCH



INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs



71.HASWE.GOU

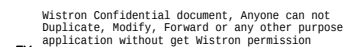


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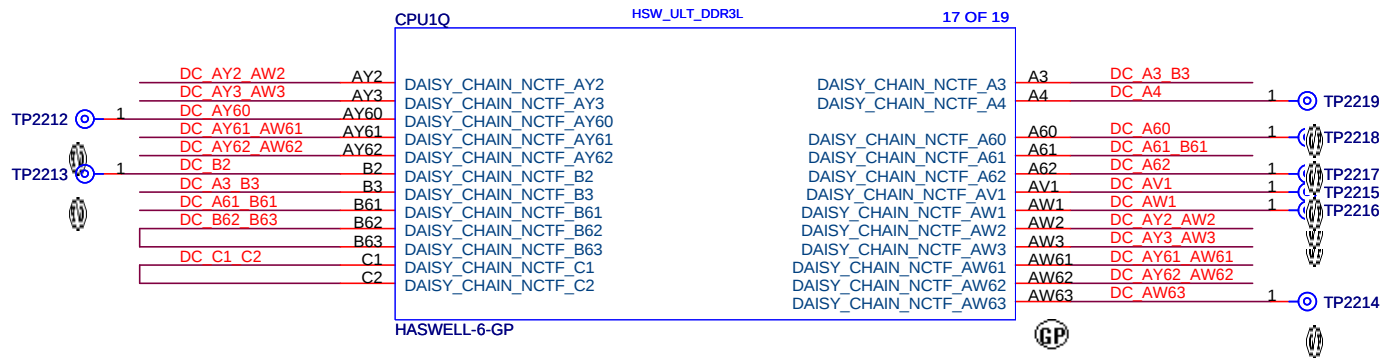
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CPU (RTC/LPC/SATA/HDA)		
Size	Document Number	Rev
Custom	EA40 HW ULT	1
Date	Monday, May 13, 2013	Sheet 19 of 102

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to [Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.](#)



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Title			
CPU (POWER1)			
Size A3	Document Number		Rev
	EA40 HW ULT		1
Date:	Monday, May 13, 2013	Sheet	21 of 102

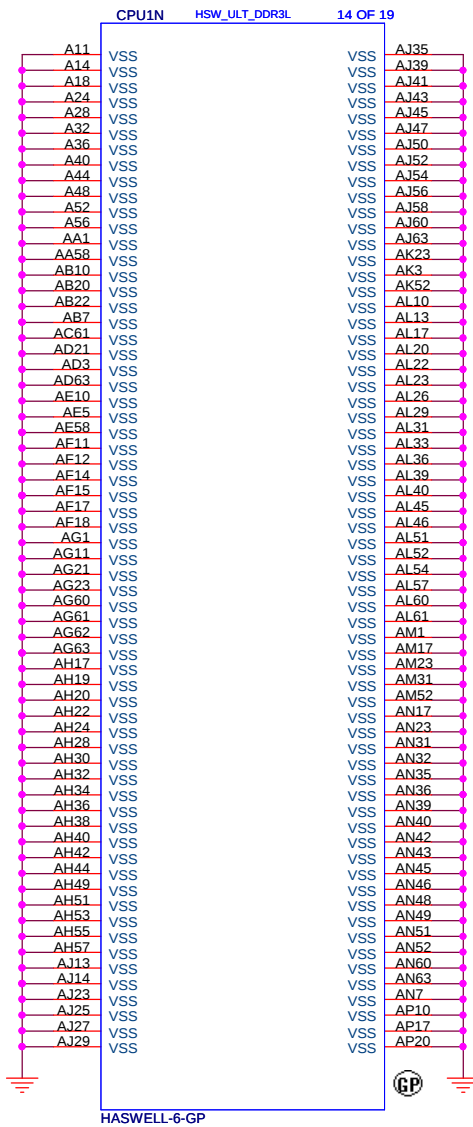


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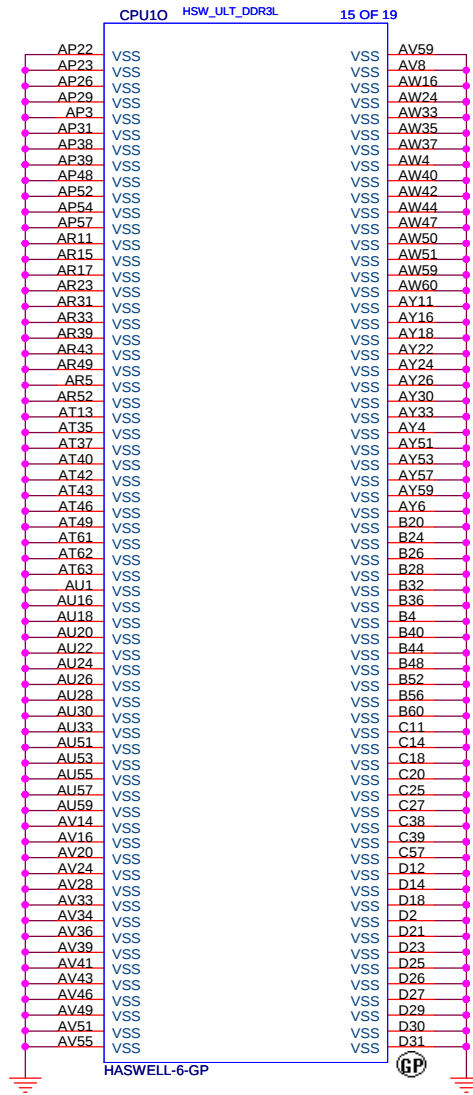
EV

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Title			
CPU (RSVD)			
Size	Document Number	Rev	
Custom	EA40 HW ULT	1	
Date:	Monday, May 13, 2013	Sheet	22 of 102

SSID = PCH



71.HASWE.G0U

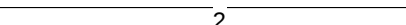
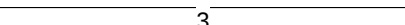
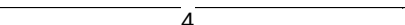
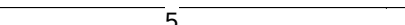


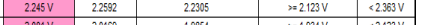
71.HASWE.G0U

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EV

Title		
CPU (VSS)		
Size	Document Number	Rev
Custom	EA40_HW ULT	1
Date:	Monday, May 13, 2013	Sheet 23 of 102



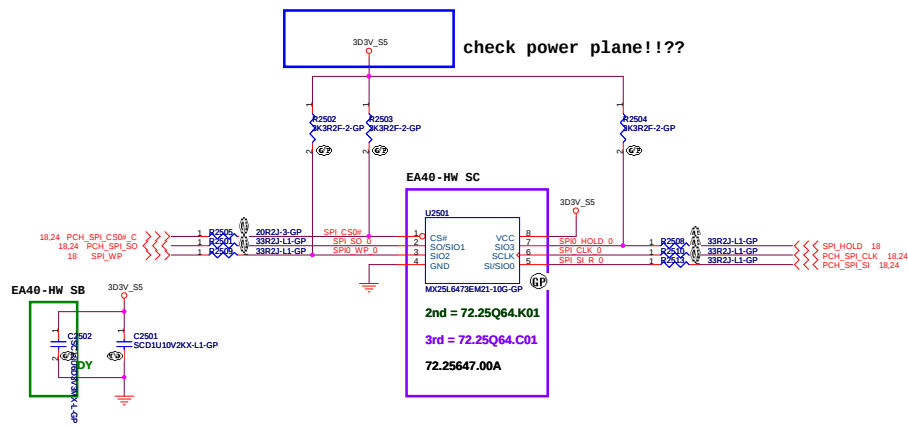


WB	WB AD	Pull-Down Resistor	Pull-Up Resistor	Typical Voltage	Max Voltage	Min Voltage	XBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945		
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408		>= 2.816 V < 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688		>= 2.363 V < 2.616 V
-I	100.0 K	47.0 K	2.245 V	2.2592	2.2305		>= 2.123 V < 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854		>= 1.934 V < 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503		>= 1.758 V < 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6685	1.6335		>= 1.504 V < 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421		>= 1.281 V < 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891		>= 1.126 V < 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334		>= 0.924 V < 1.126 V

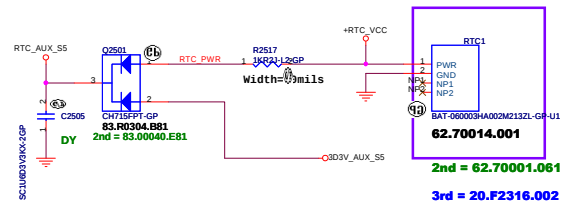
1

SSID = Flash.ROM **SPI FLASH ROM (8M byte) for PCH**

SPI ROM Equal length need to less than 500mil



SSID = RBAT



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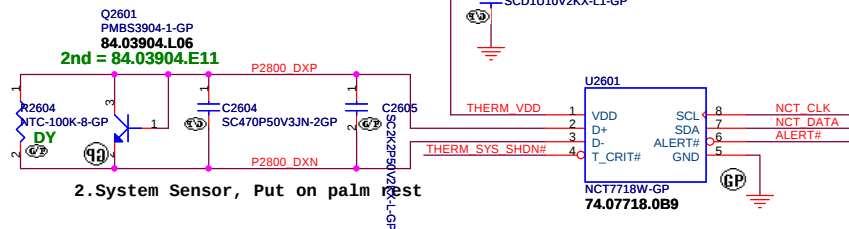
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Title			
Flash(KBC+PCH)/RTC			
Size A2	Document Number		Rev
	EA40 HW ULT		1
Date:	Monday, May 12, 2013	Sheet 25 of	102

SSID = Thermal

Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.



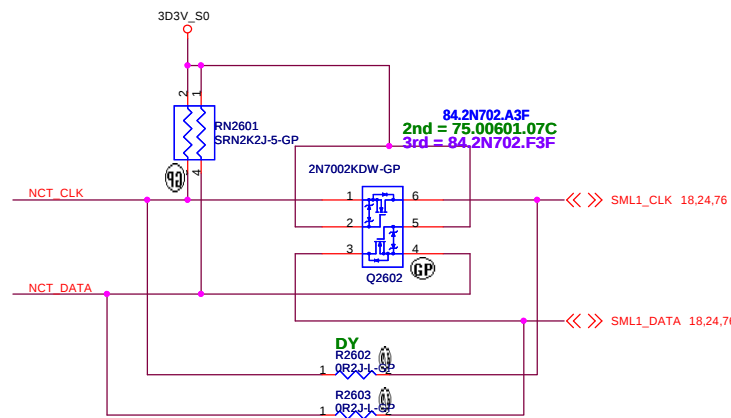
1.H/W T8 Shutdown

ALERT# /T CRIT#
Pull-up Resistor

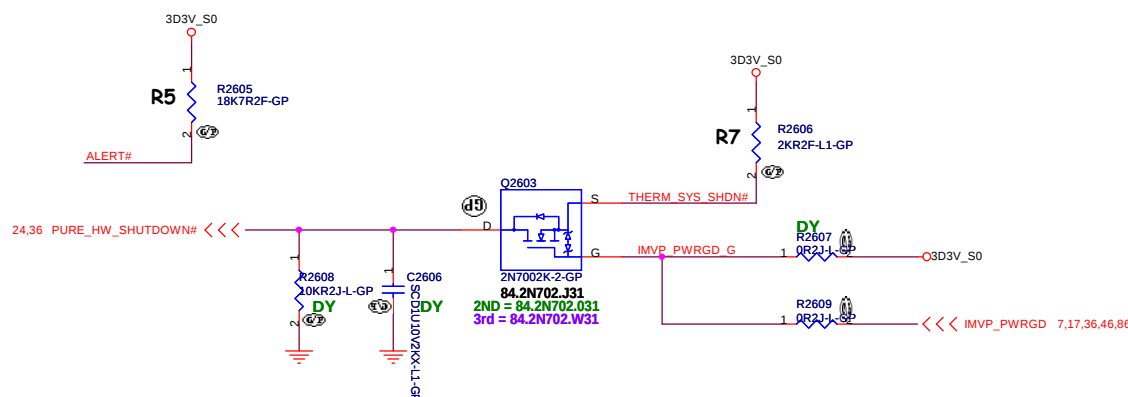
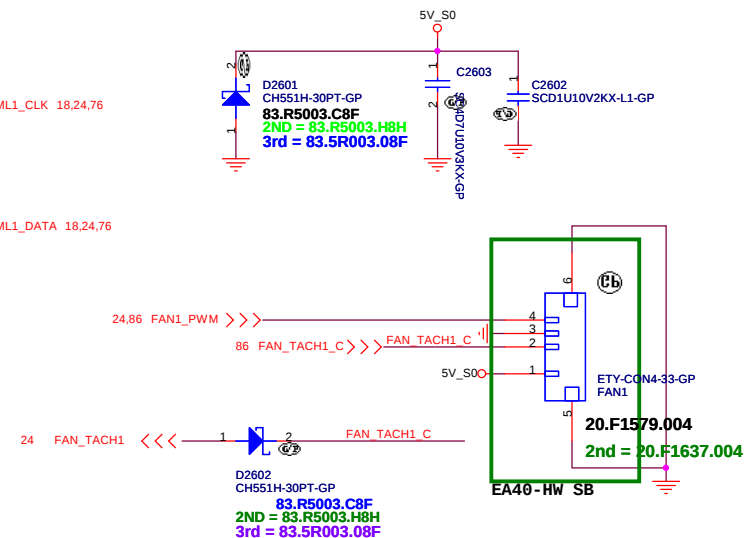
R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

T8=85 degree



Layout 15 mil



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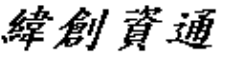
EV

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Title	
Thermal 7718/Fan Controller P2793	
Size	Document Number
A3	EA40 HW ULT
Date:	Rev
Monday, May 13, 2013	1
Sheet	of
26	102

5	4	3	2	1
D				
C				
B				
A				

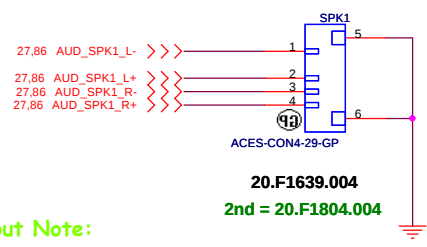
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Title		
Audio AMP_1001		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 28	of 102

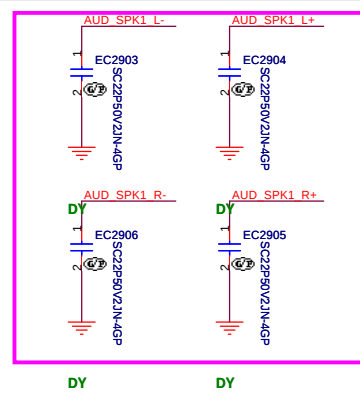
SSID = AUDIO

Speaker

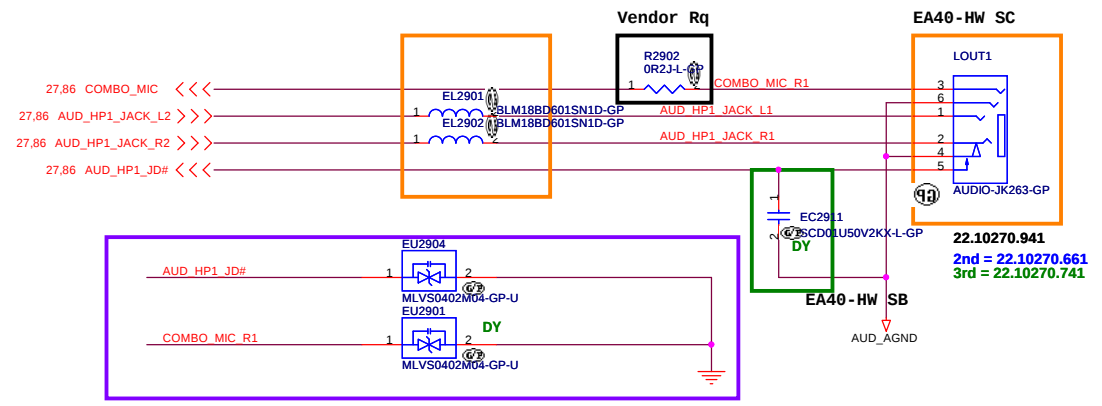


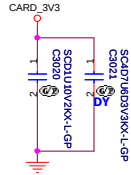
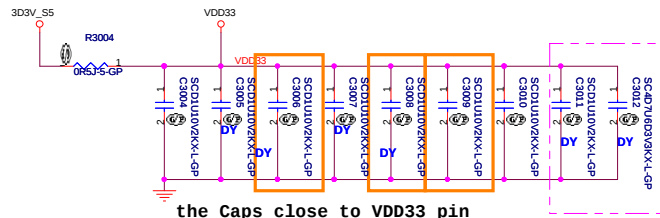
Layout Note:

Trace width=40mil



Combo Jack

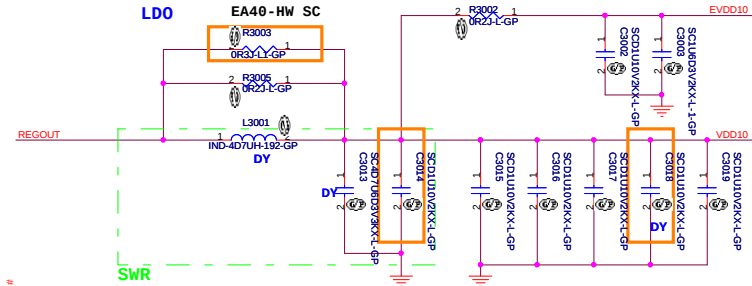
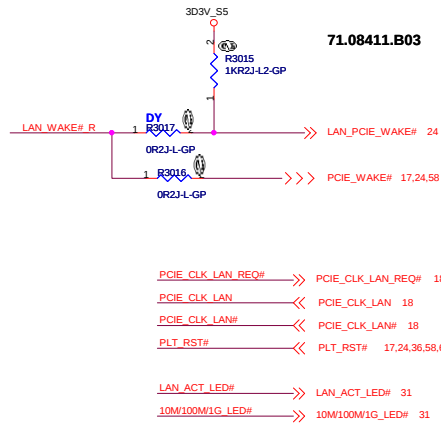




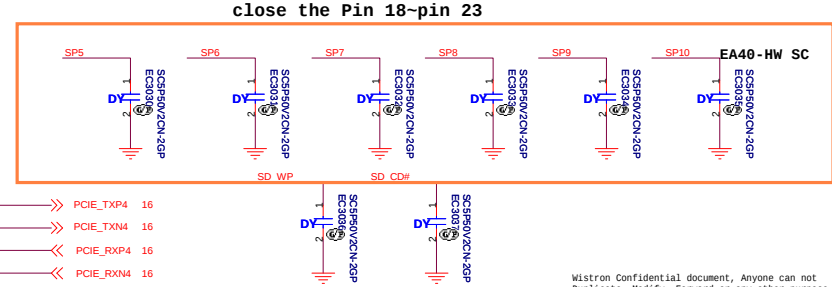
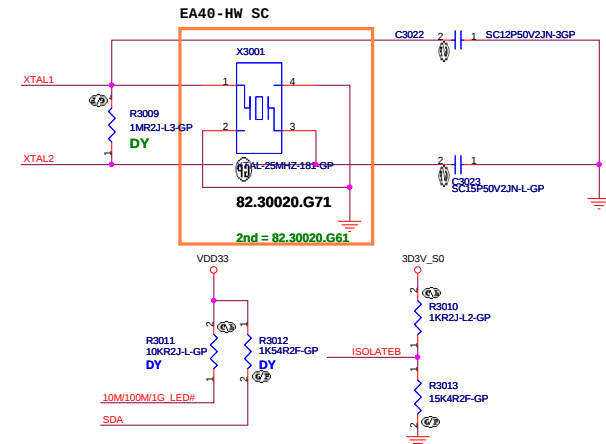
SP1	SD_7	MS_INS#	xD_RDY
SP2	SD_6	MS_RE#	xD_RE#
SP3	SD_5	MS_CD#	xD_CD#
SP4	SD_4	MS_WE#	xD_WE#
SP5	SD_3	MS_D0	xD_D0
SP6	SD_2	MS_D1	xD_D1
SP7	SD_1	MS_D2	xD_D2
SP8	SD_0	MS_D3	xD_D3
SP9	SD_CMD	MS_D4	xD_D4
SP10	SD_CLK	MS_D5	xD_D5
SP11	SD_WP	MS_D6	xD_D6
SP12	SD_CD#	MS_D7	xD_D7
SP13	SD_WP	MS_D8	xD_D8
SP14	SD_CD#	MS_D9	xD_D9
SP15	SD_WP	MS_D10	xD_D10
SP16	SD_CD#	MS_D11	xD_D11

EA40-HW SC

SP5	2	ER3014	22KJ2-GP	SD_DATA1	33,86
SP6	2	ER3022	22KJ2-GP	SD_DATA0	33,86
SP7	2	ER3021	33KJ2-L1-GP	SD_CLK	33,86
SP8	2	ER3024	22KJ2-GP	SD_CMD	33,86
SP9	2	ER3023	22KJ2-GP	SD_DATA3	33,86
SP10	2	ER3025	22KJ2-GP	SD_DATA2	33,86
SD_WP				SD_WP	33
SD_CD#				SD_CD#	33



24 MCP_GPIO9 >>>



PCIE_TXP4	>>>	PCIE_TXP4	16
PCIE_TXN4	>>>	PCIE_TXN4	16
PCIE_RXP4	>>>	PCIE_RXP4	16
PCIE_RXN4	>>>	PCIE_RXN4	16

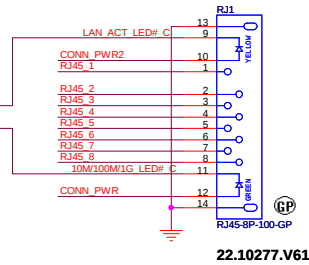
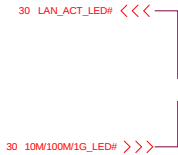
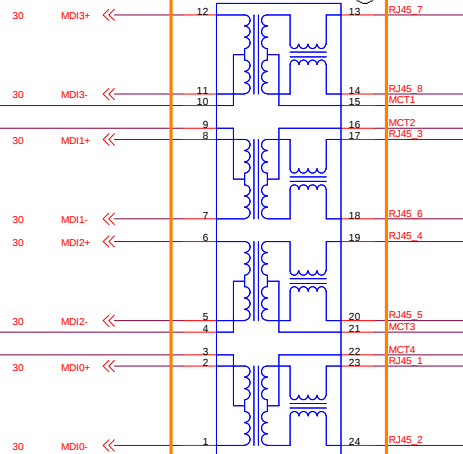
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Title		LAN(RTL8411)	
Size	Document Number	Rev	1
Custom	EA40 HW ULT	Date	Monday, May 13, 2013
Sheet		30	of 102

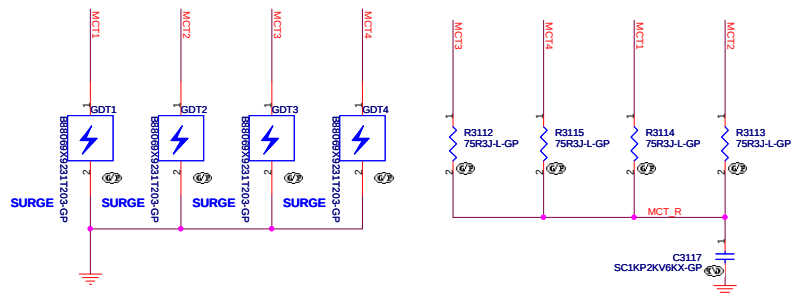
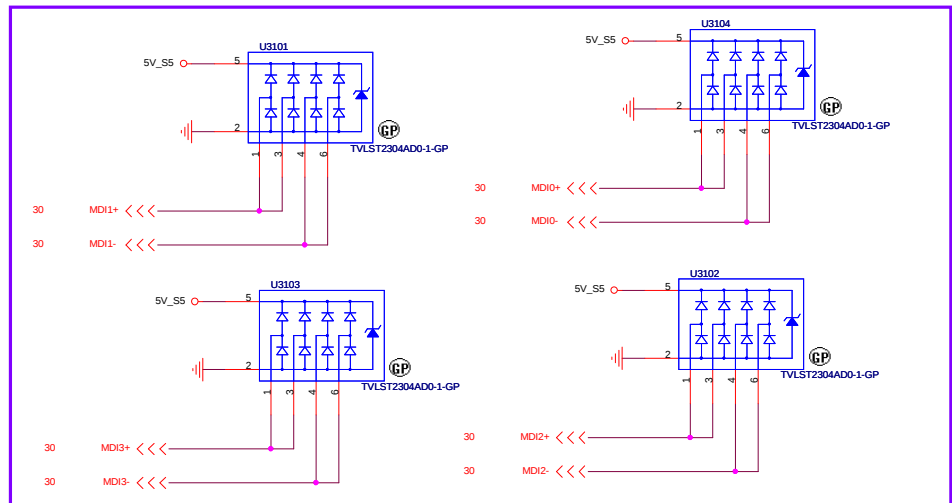
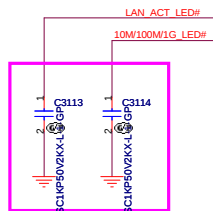
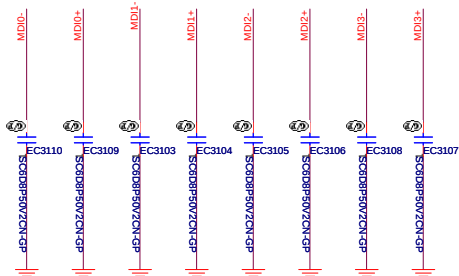
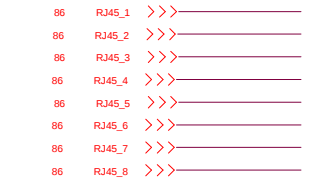
SSID = LAN

EA40-HW SC

3rd = 68.00069.30A
2nd = 68.1H115.30A
68.69241.301
XFORM-270-GP-U



303V_S5



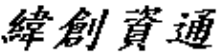
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EV		
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Title (LAN+VGA) CONNECTOR		
Size Custom	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 31	of 102

5	4	3	2	1
D				
C				
B				
A				

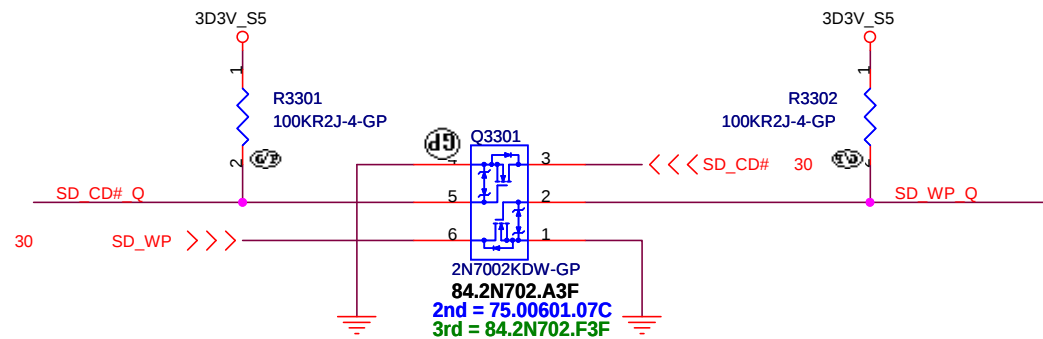
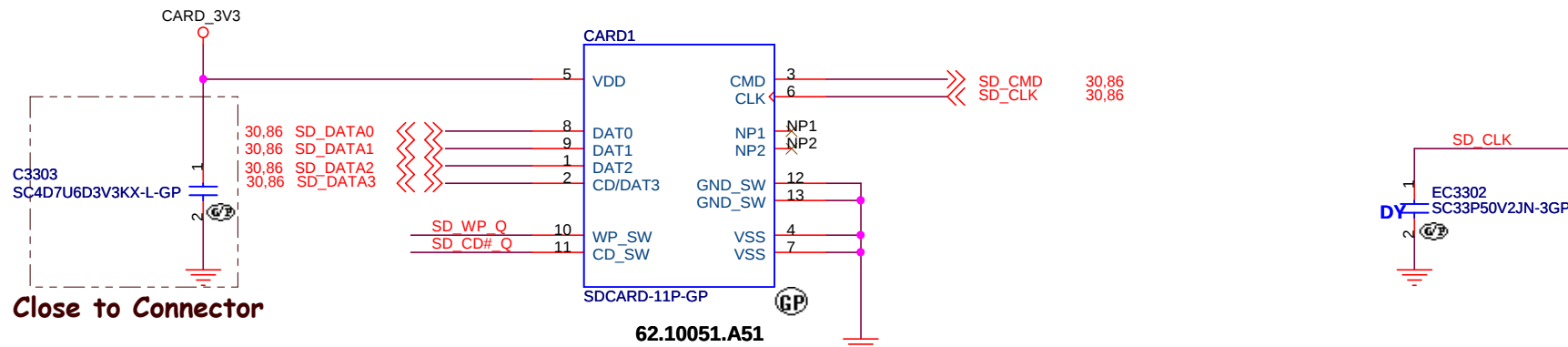
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Title RTS5229(CARD READER)		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013		Sheet 32 of 102

SSID = SDIO

SD//MS Card Reader

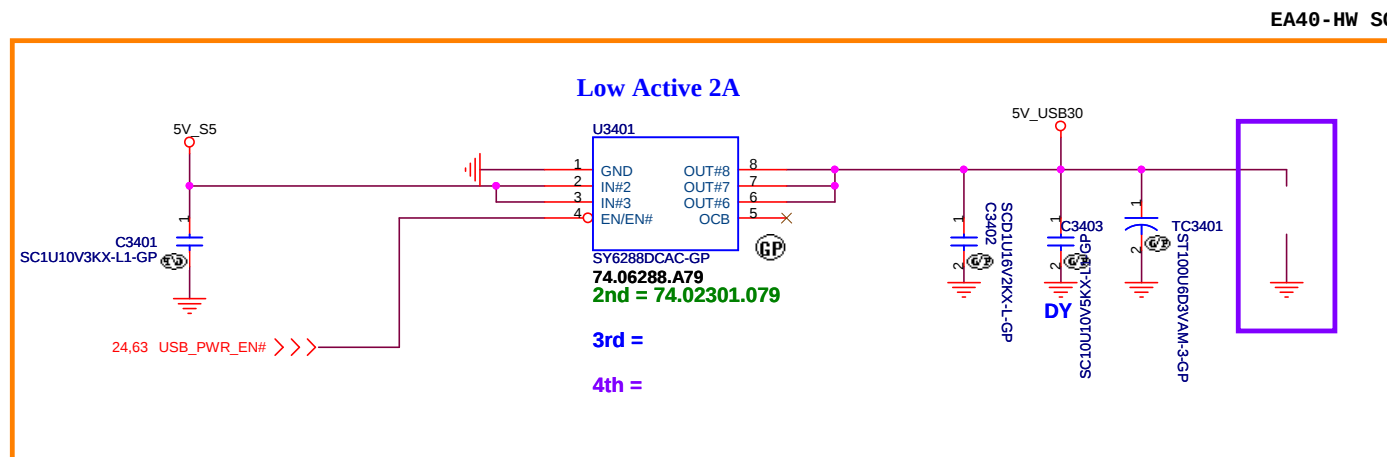


86 SD_WP_Q >>> _____
86 SD_CD#_Q >>> _____

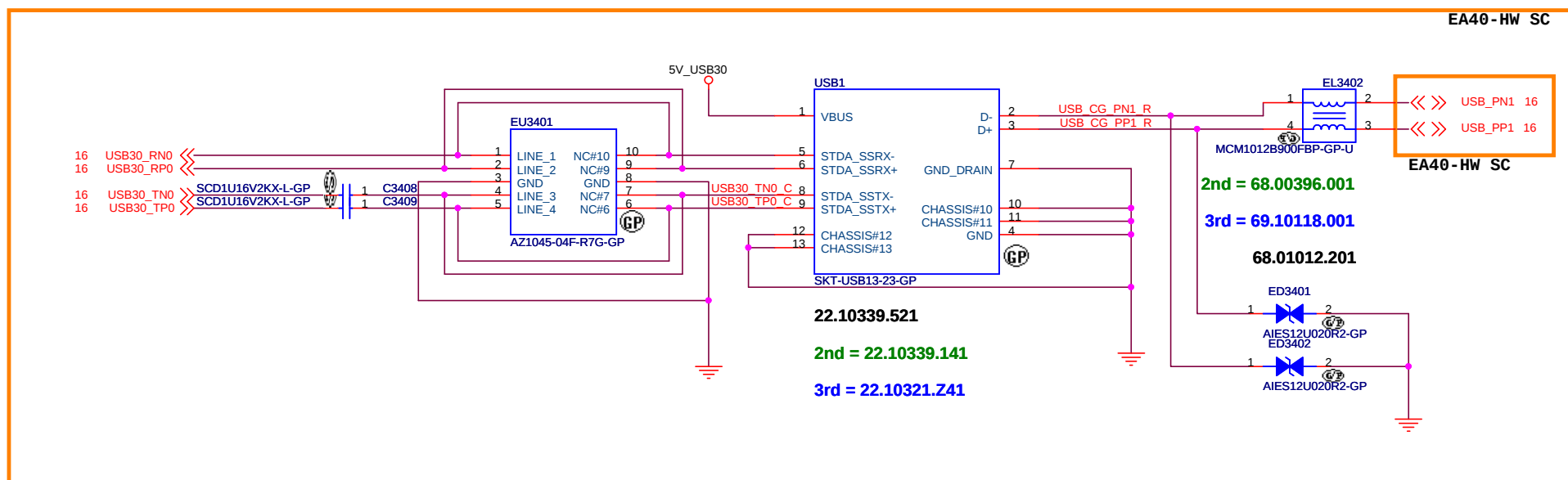
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Title			
CARD Reader CONN			
Size Custom	Document Number EA40 HW ULT		Rev 1
Date:	Monday, May 13, 2013	Sheet 33 of	102



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



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A

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Title

USB 2.0 / 3.0 Port

Size Custom

Document Number

EA40 HW ULT

Date: Monday, May 13, 2013

Sheet 34 of 102

Rev 1

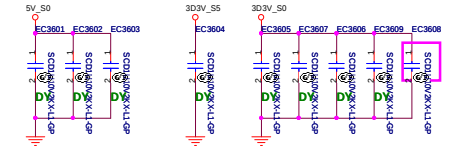
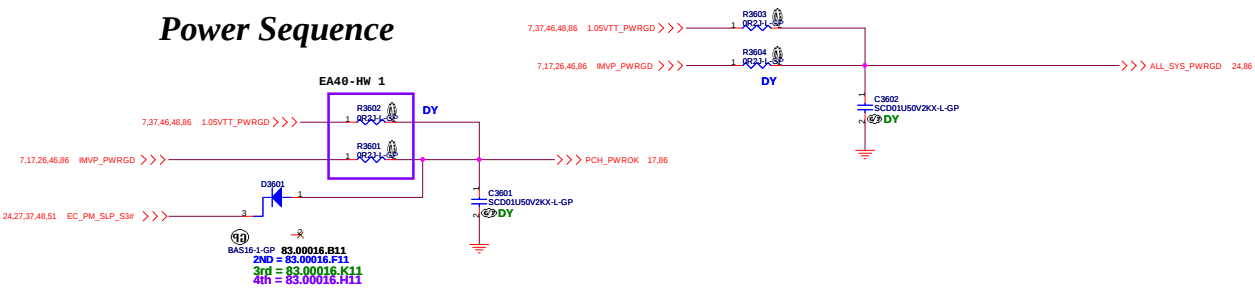
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D				
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A				

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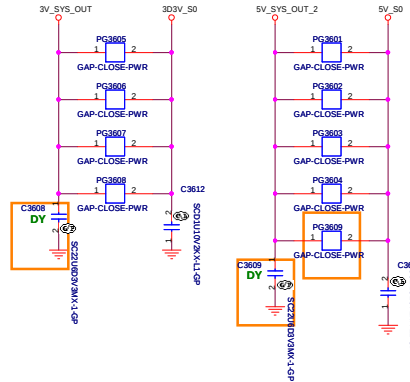
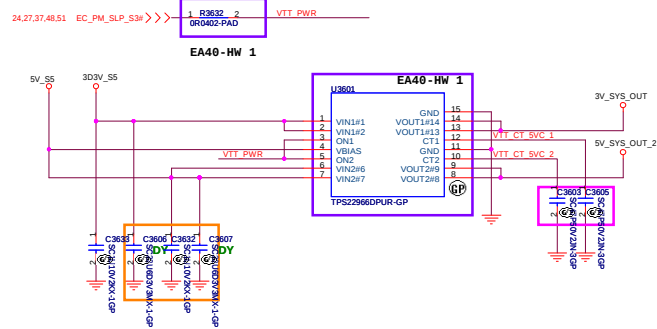
EV

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Title		
USB CHARGER		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 35	of 102

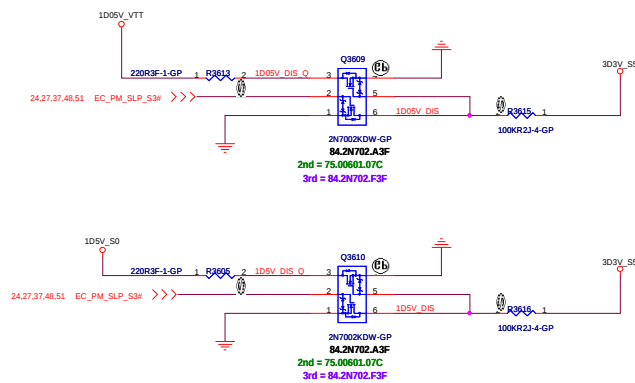
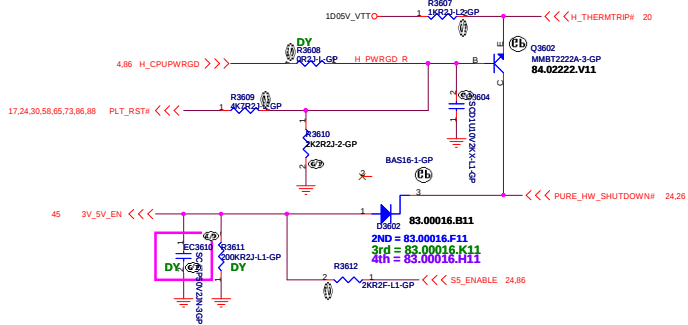
Power Sequence



ANNIE Run Power



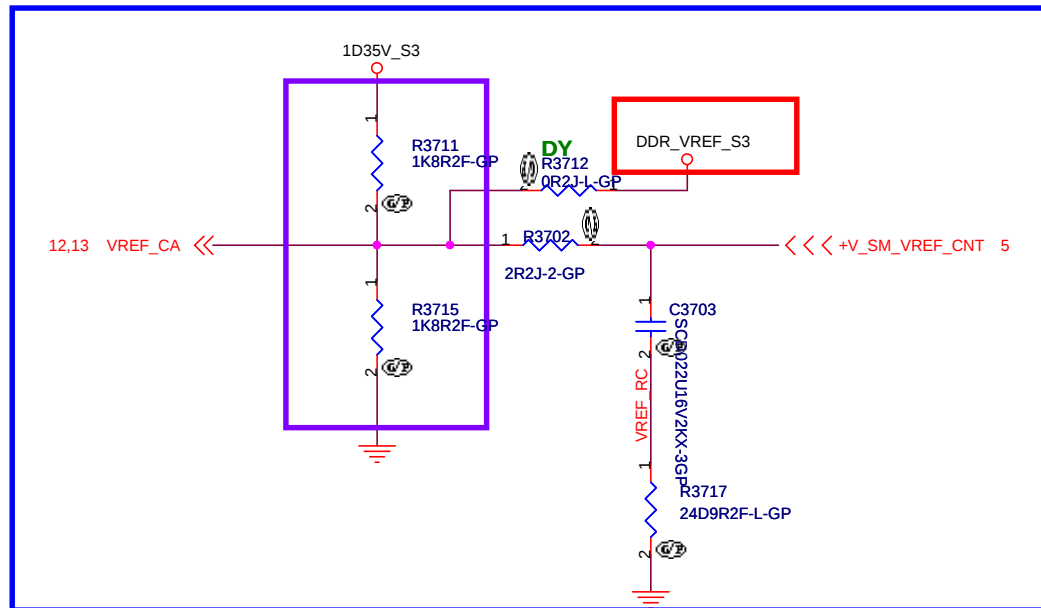
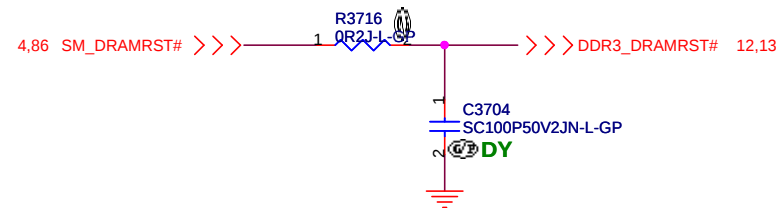
Discharge circuit



DY 3D3V_S0 discharge circuit

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File	Power Plane Enable & SEQUENCE
Size	Document Number
K2	EA40 HW ULT
Rev	1
Doc. No.	10859, May 21, 2010
Page	36 of 102

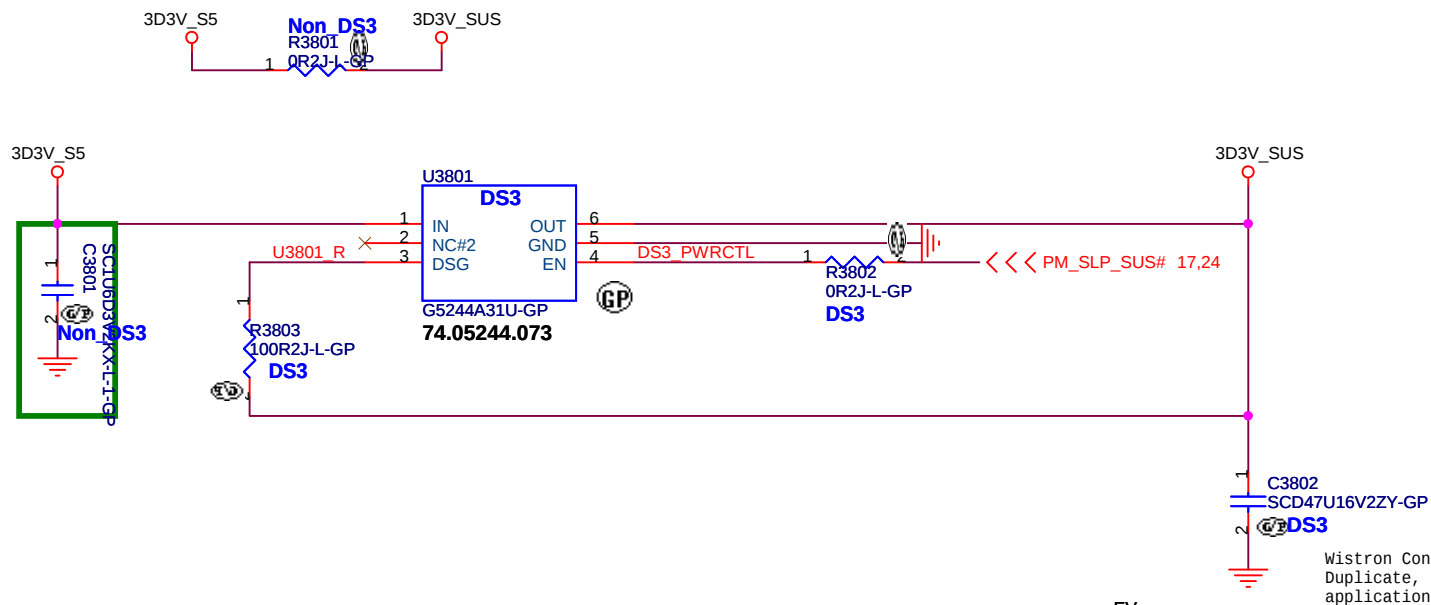


For Intel Recommend Close to DIMM

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EV

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Title					
ADAPTER OCP / S3 reduction					
Size	Document Number				Rev
Custom	EA40 HW ULT				1
Date:	Monday, May 13, 2013		Sheet	37	of 102



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Title

DS3

Size
A4

Document Number

EA40 HW ULT

Rev

1

Date: Monday, May 13, 2013

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Power Sequence

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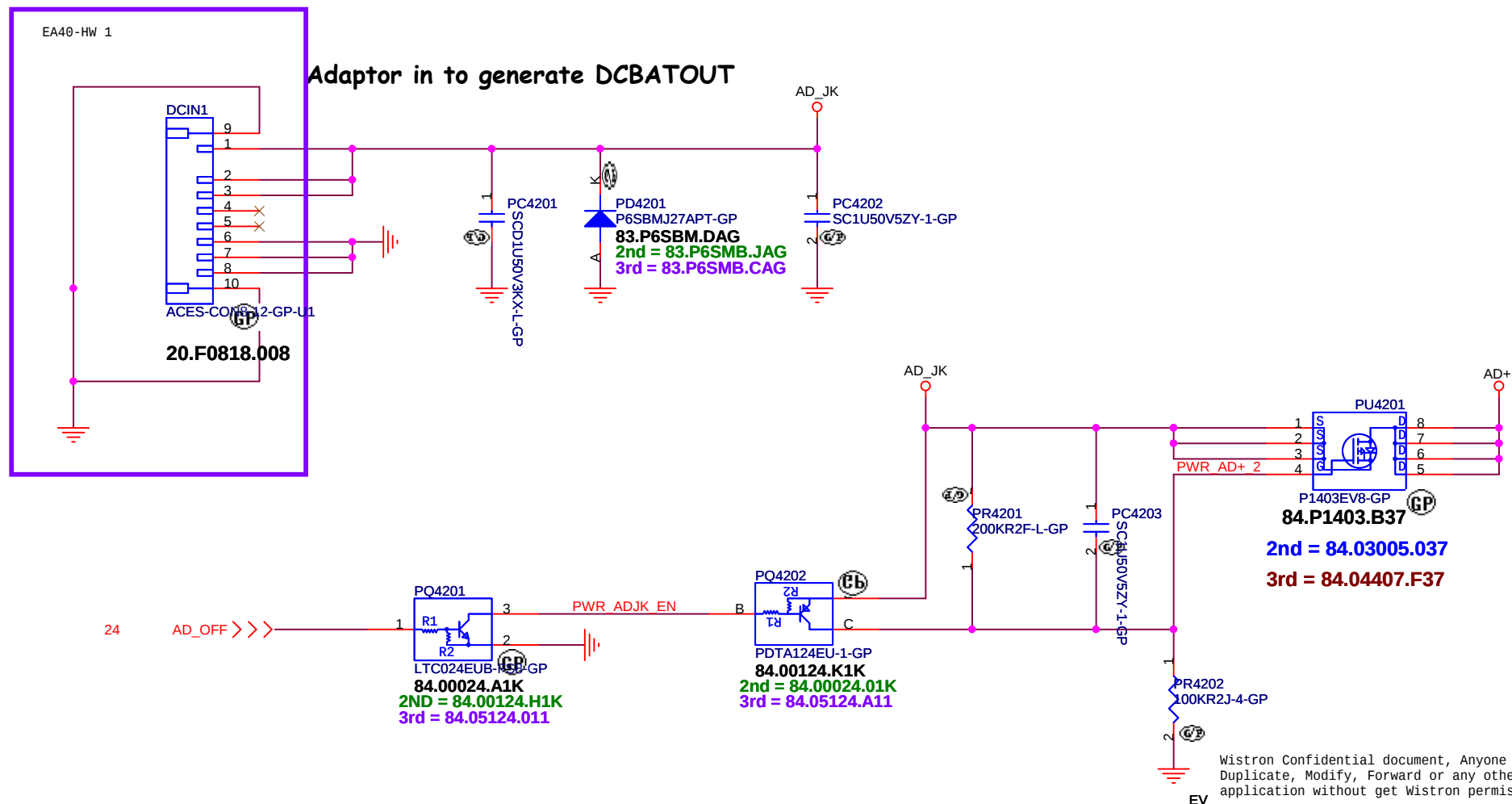
EV

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1D05 M			
Size	Document Number		Rev
Custom	EA40 HW ULT		1
Date:	Monday, May 13, 2013		Sheet 39 of 102

	5	4	3	2	1
D					D
C					C
B					B
A				Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission EV 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. Title Connected Standby1 Size Document Number Rev A EA40 HW ULT 1 Date: Monday, May 13, 2013 Sheet 40 of 102	A
	5	4	3	2	1

	5	4	3	2	1
D					D
C					C
B					B
A				Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission EV 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. Title Connected Standby2 Size Document Number Rev EA40 HW ULT 1 Date: Monday, May 13, 2013 Sheet 41 of 102	A
	5	4	3	2	1

ANNIE solution



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Title

DCIN JACK

Size
A4

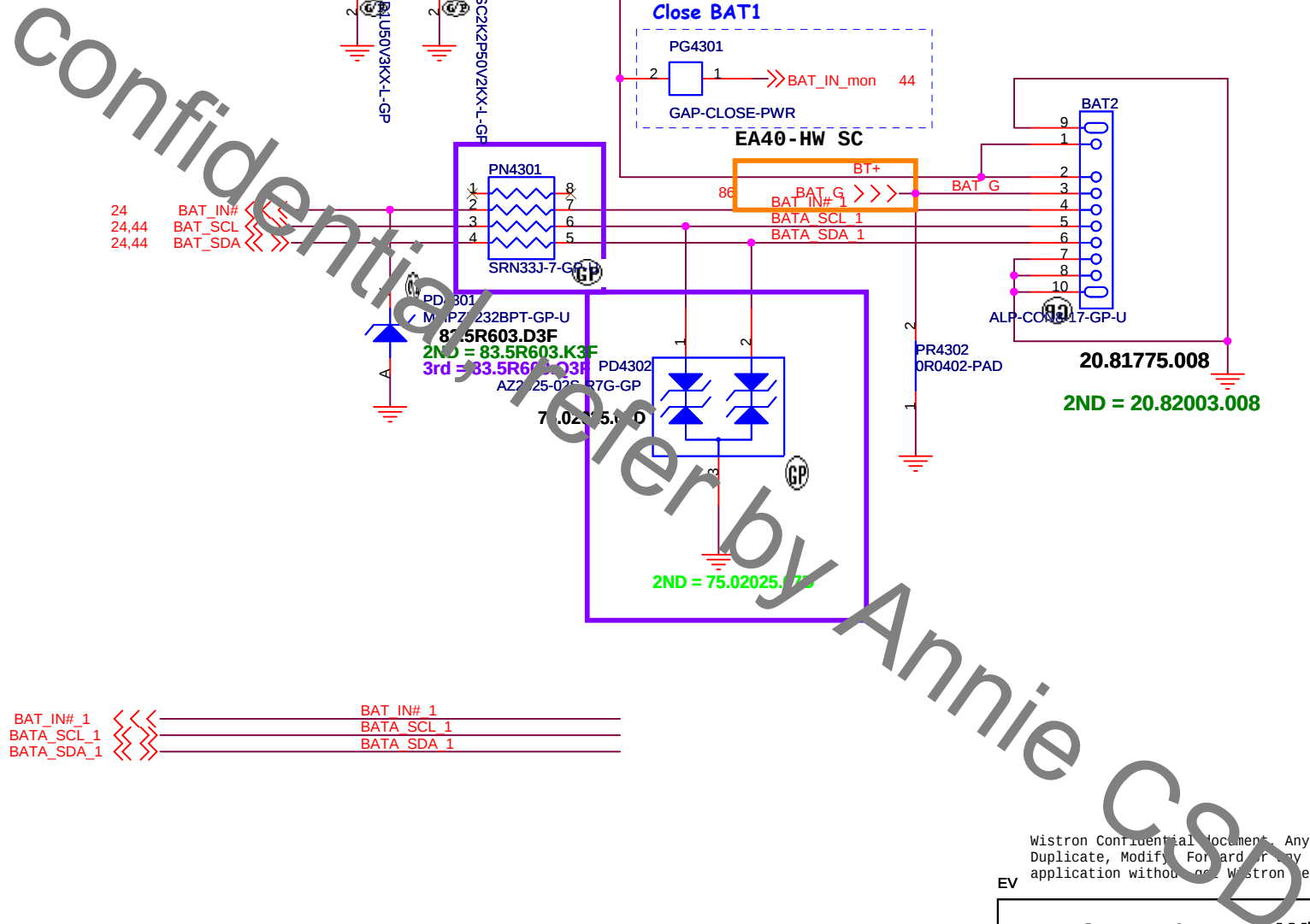
Document Number

EA40 HW ULT

Rev
1

Date: Monday, May 13, 2013

Sheet 42 of 102



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Title

BATT CONN

Size
A4

Document Number

EA40 HW ULT

Rev
1

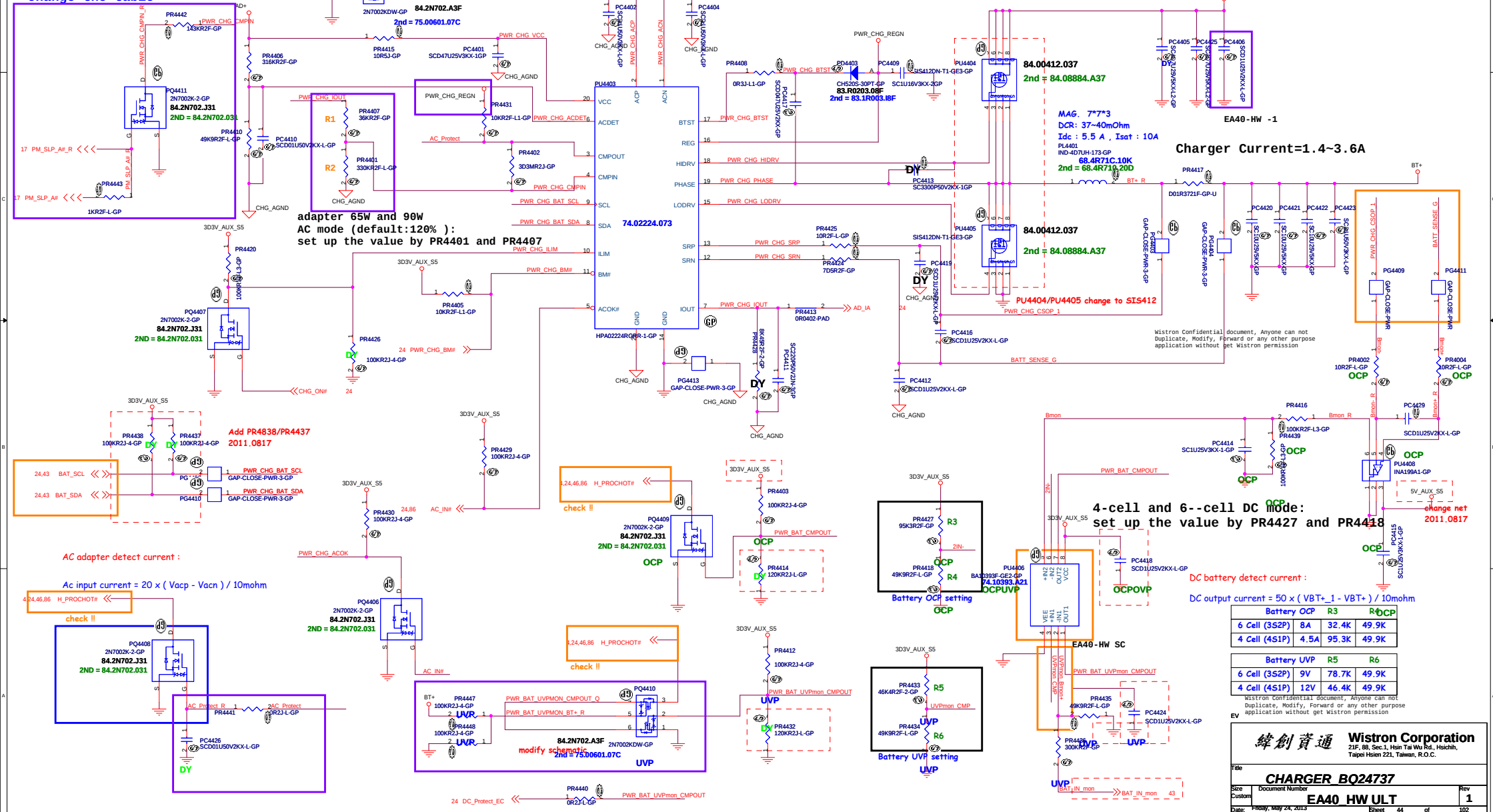
Date: Monday, May 13, 2013

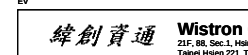
Sheet 43 of 102

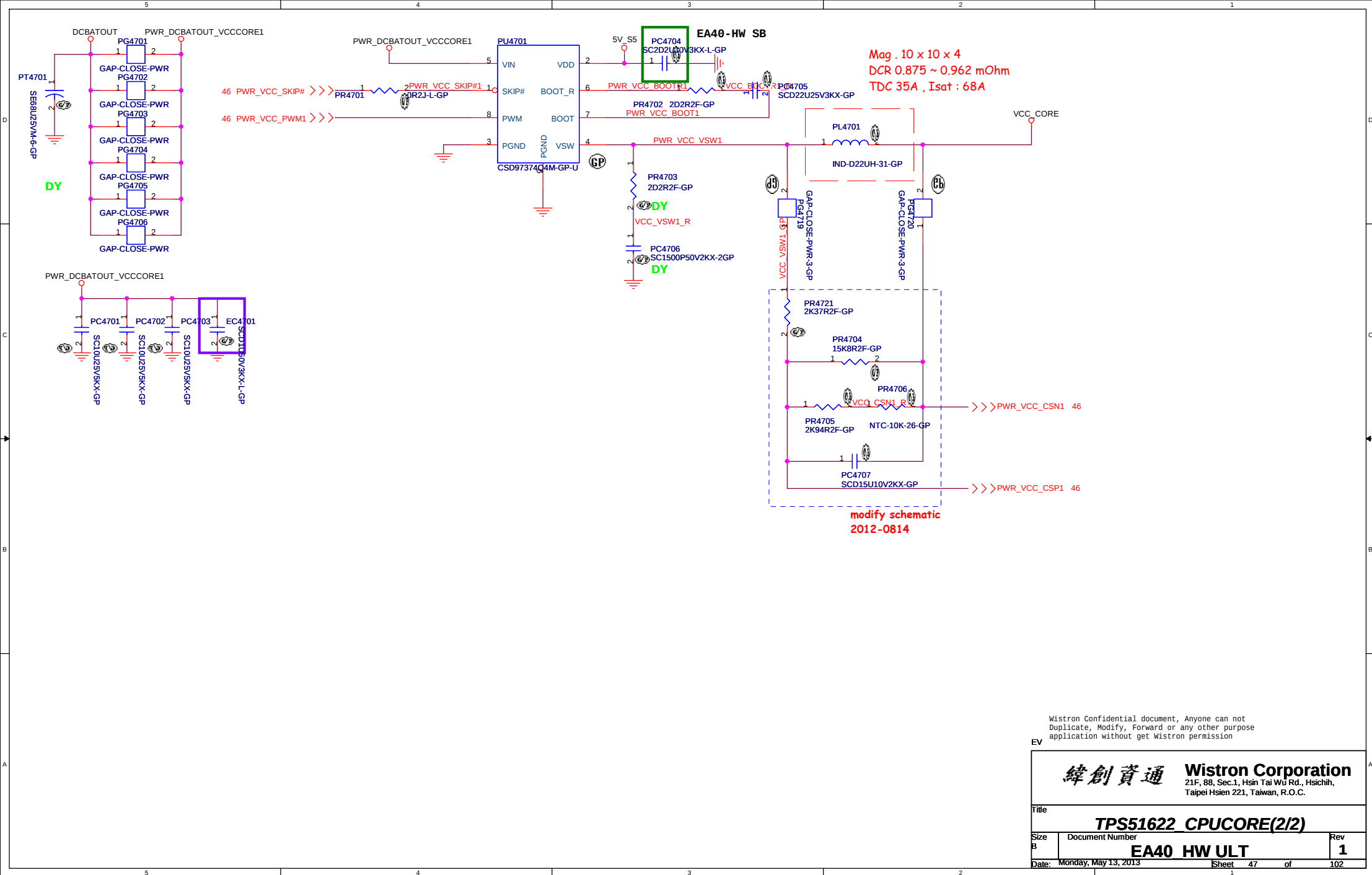
SSID = Charger

D	AD+ total power	R1	R2
	65w	36K	100K
	90w	90K9	100K

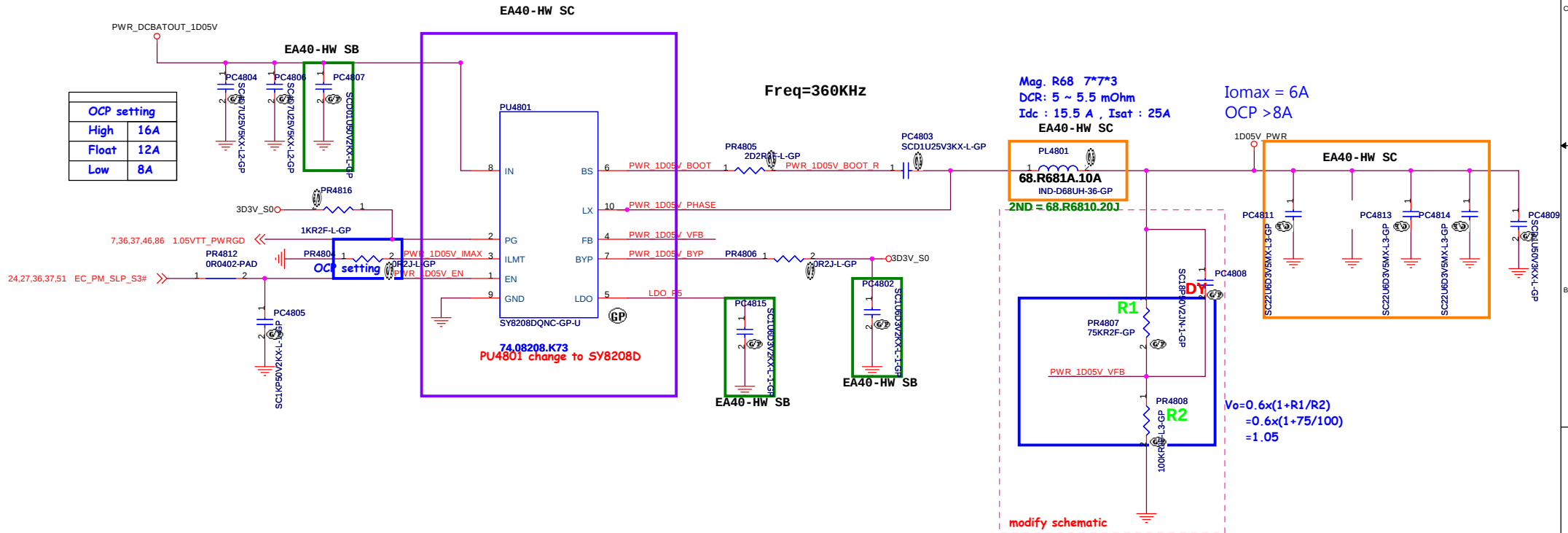
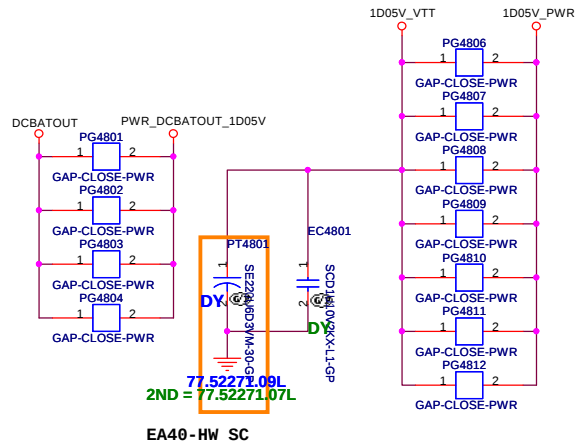
change the table







SY8208D for 1D05V



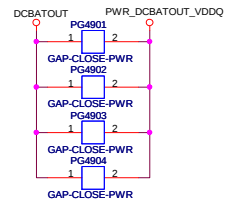
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EV

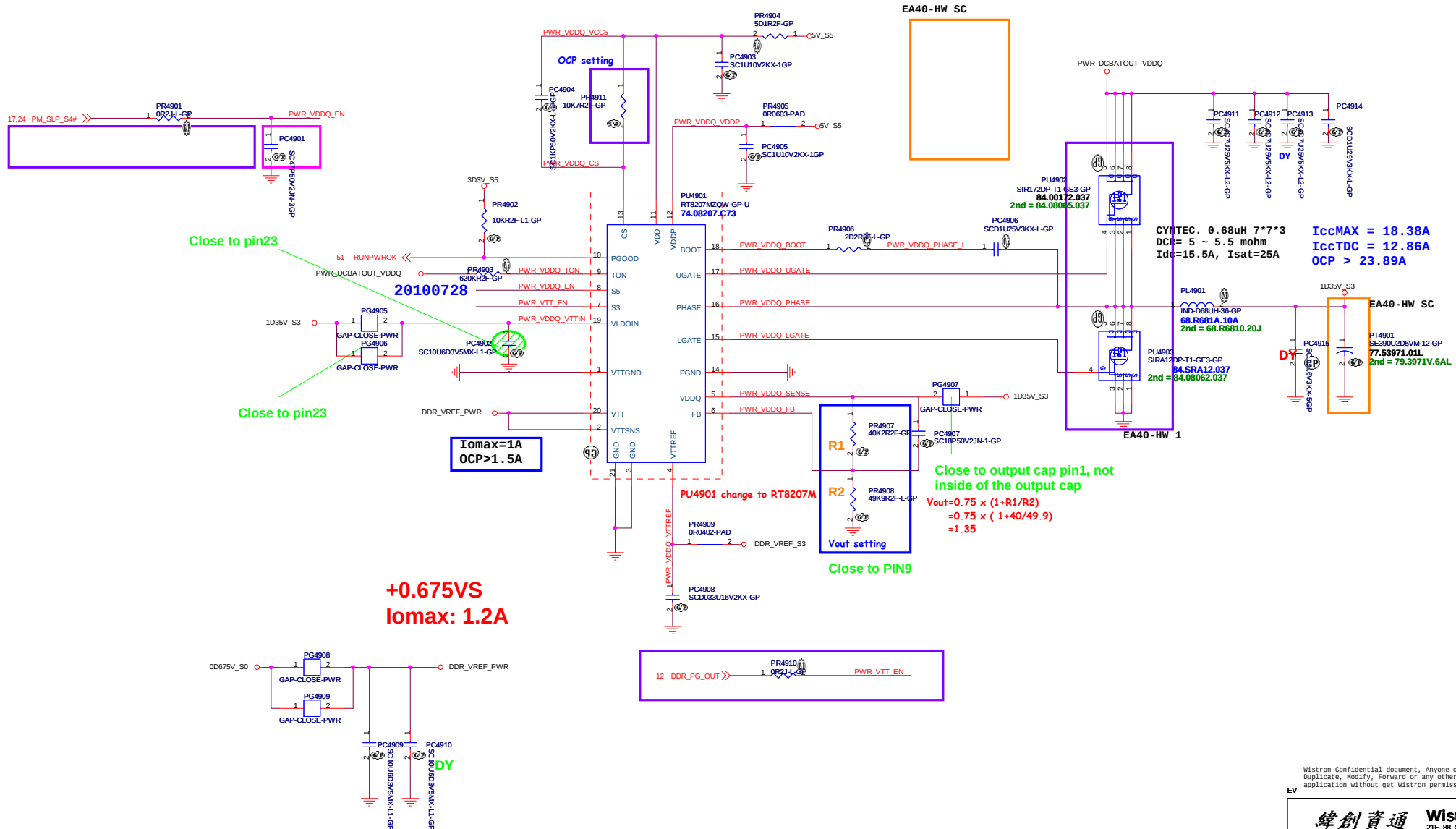
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
DC to DC 1D05V(SY8208D)			
Size A3	Document Number		Rev
	EA40 HW ULT		1
Date:	Friday, May 24, 2013	Sheet 48 of	102

SSID = PWR.Plane.Regulator_1p2v0p6v



RT8207L for VDDQ



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Title			
RT8207(VDDQ VTT)			
Size	Document Number		Rev
Custom	EA40 HW ULT		1
Date:	Monday, May 13, 2013	Sheet 49 of	102

SYW232 for 1D8V_S0

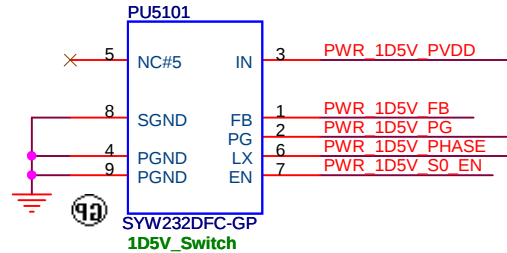
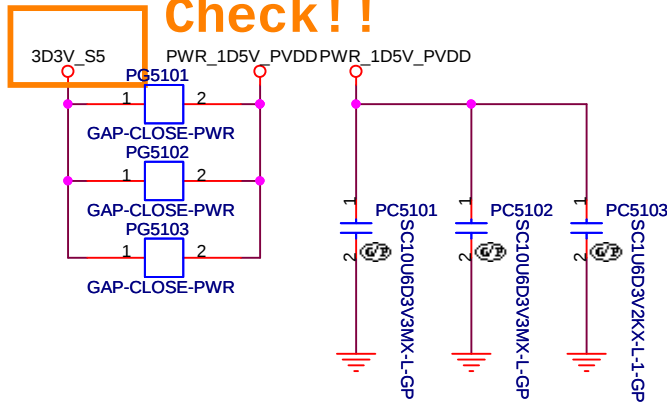
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Title		
1D8V_S0 SYW232		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 50	of 102

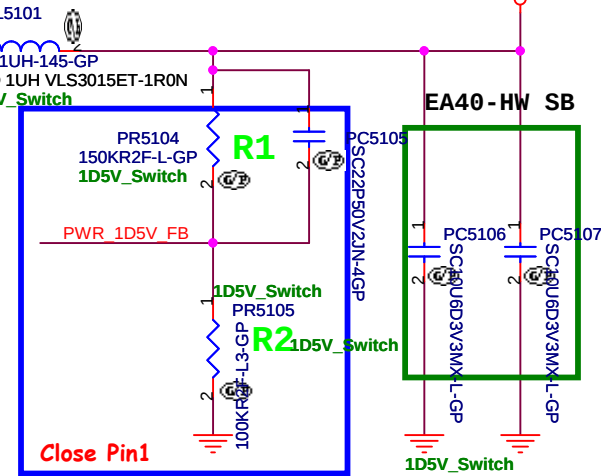
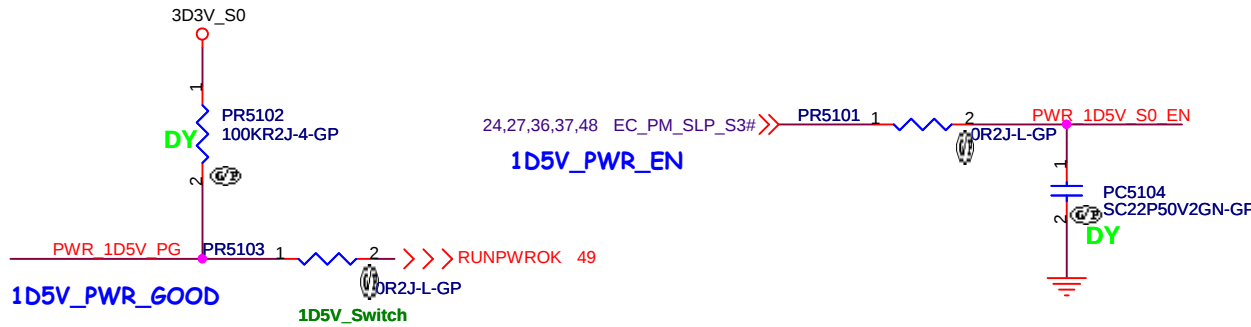
SYW232 for 1D5V_S0

Check!!



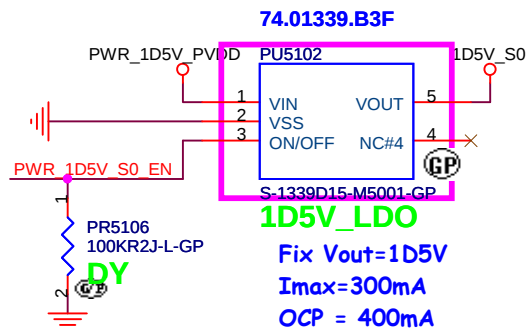
Mag. 2D2uH 5.3 x 4.7 x 3
DCR=29 ~ 35mohm
Isat : 5.5 ~ 9 A

Iomax=3.2A
OCP>5A



$$V_o = 0.6 \times (1 + R1/R2) \\ = 0.6 \times (1 + 150/100) \\ = 1.5$$

EA40-HW SC



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Title

1D5V_S0 SYW232

Size A4

Document Number

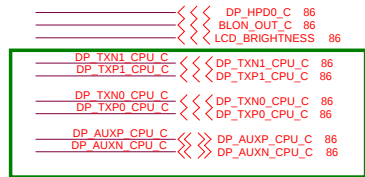
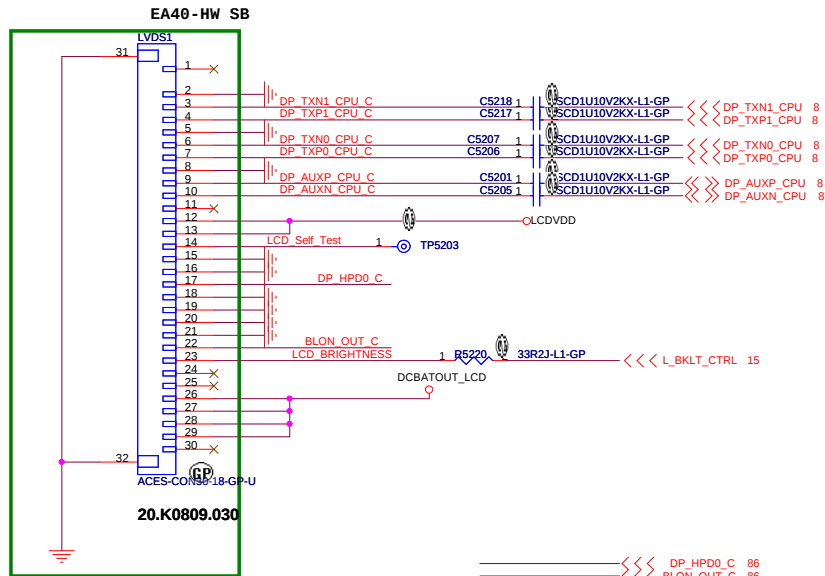
EA40 HW ULT

Rev 1

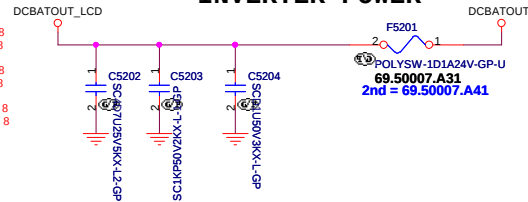
Date: Monday, May 13, 2013

Sheet 51 of 102

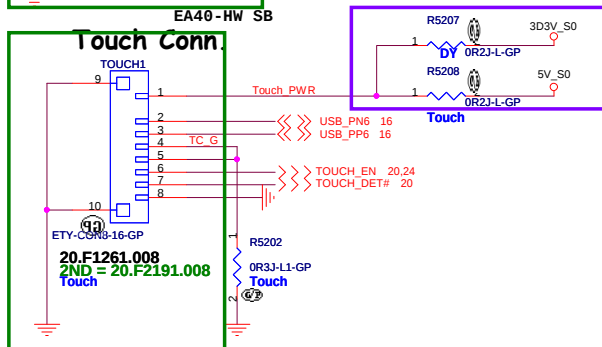
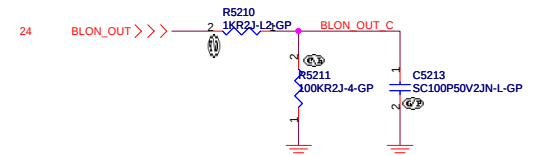
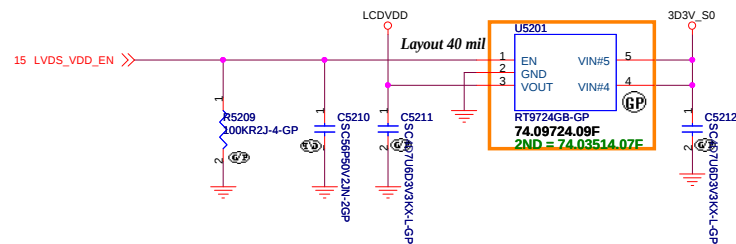
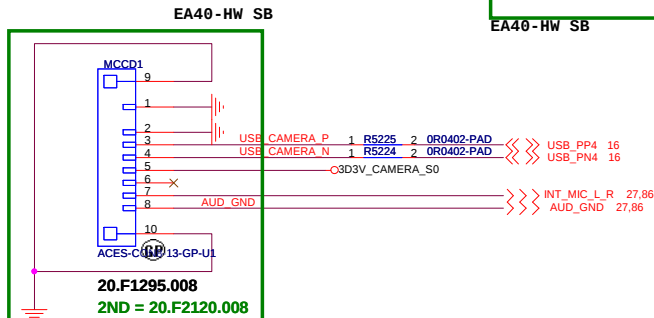
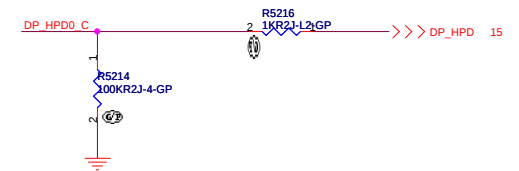
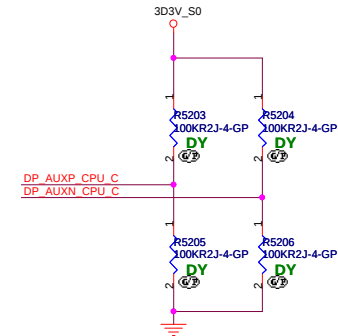
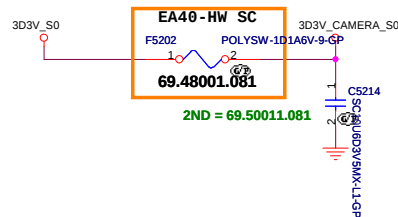
SSID = VIDEO



INVERTER POWER



Camera Power



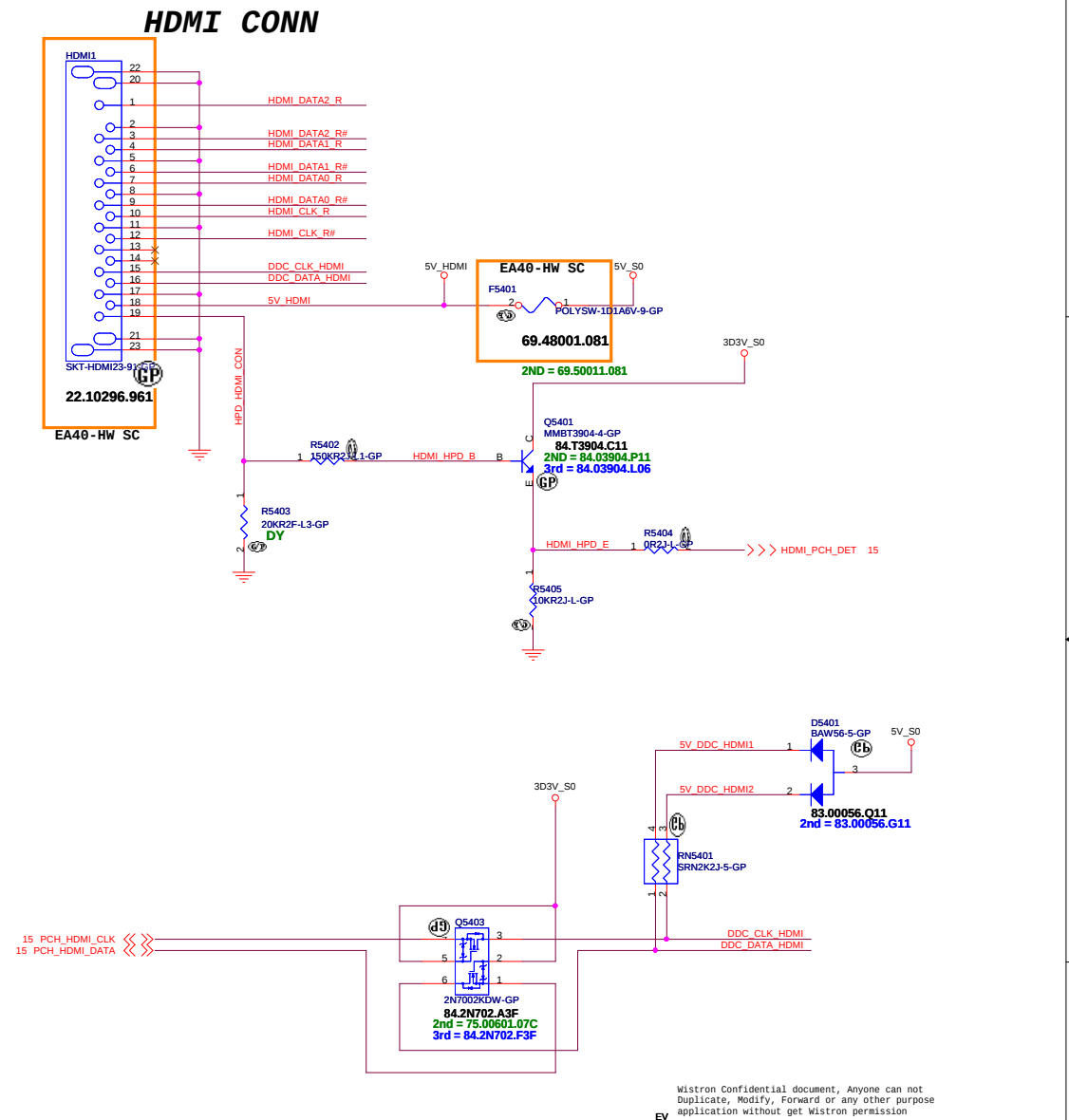
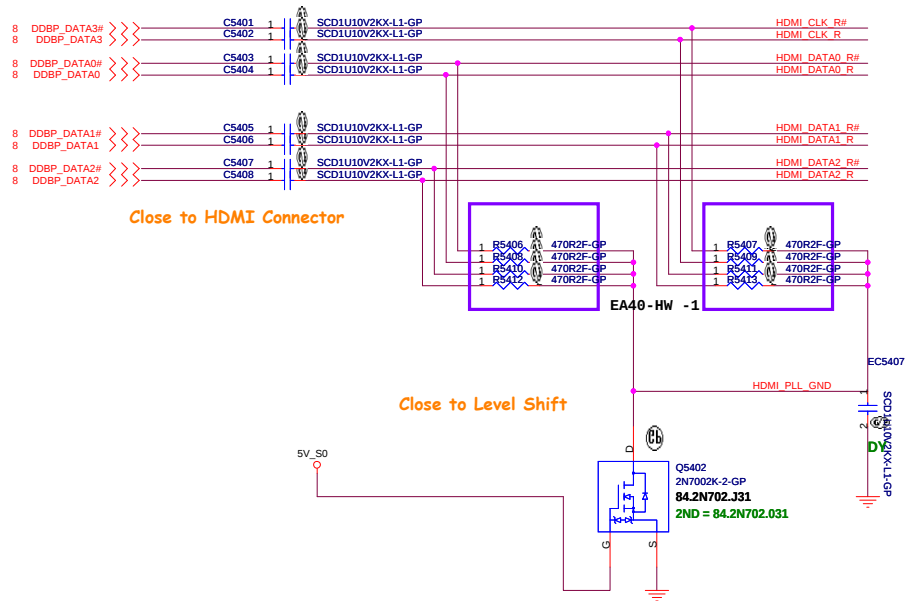
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Title	LCD Connector	
Size	Document Number	Rev
Custom	EA40 HW ULT	1
Date:	Thursday, May 30, 2013	Sheet 52 of 102

SSID = VIDEO

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister



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Title	
HDMI Level Shifter/Connector	
Size Custom	Document Number
EA40 HW ULT	
Date: Monday, May 13, 2013	Sheet 54 of 102
Rev 1	

D

D

C

C

B

B

A

A

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Title

Display Port

Size	Custom
------	--------

Document Number

Rev

EA40 HW ULT

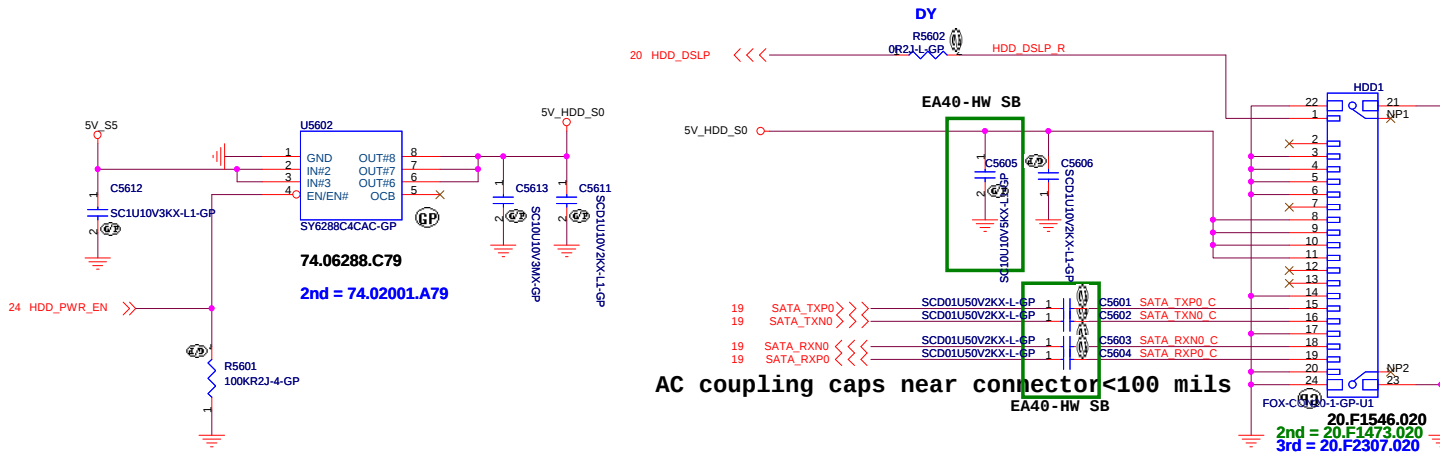
Rev
1

Date: Monday, May 13, 2013

Sheet	55	of	102
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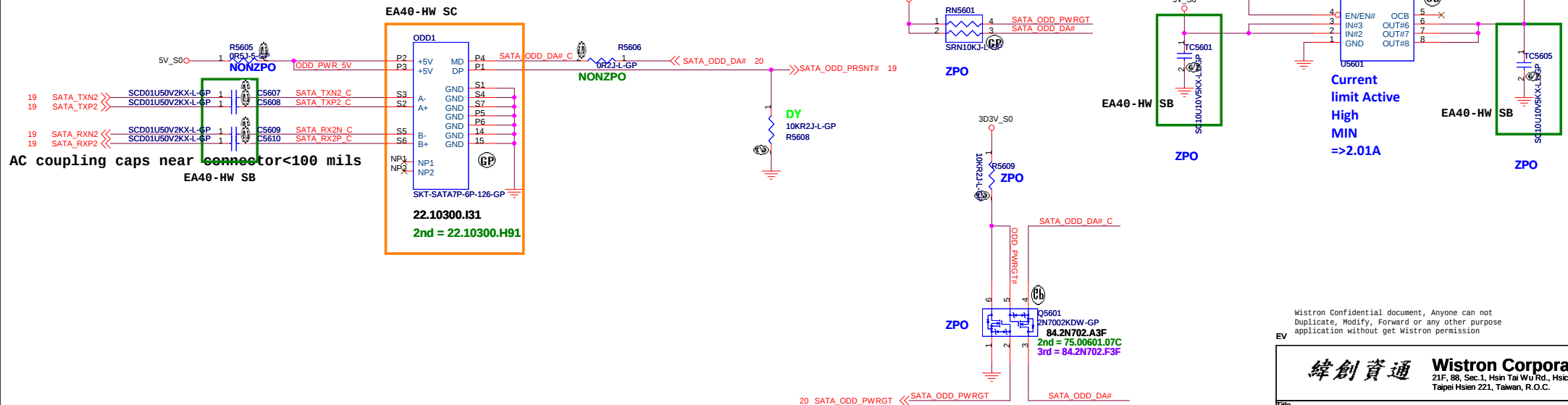
SSID = SATA

SATA HDD Connector



ODD Connector

SATA Zero Power ODD



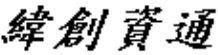
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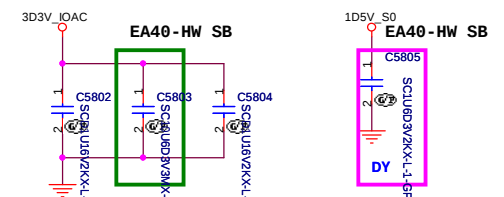
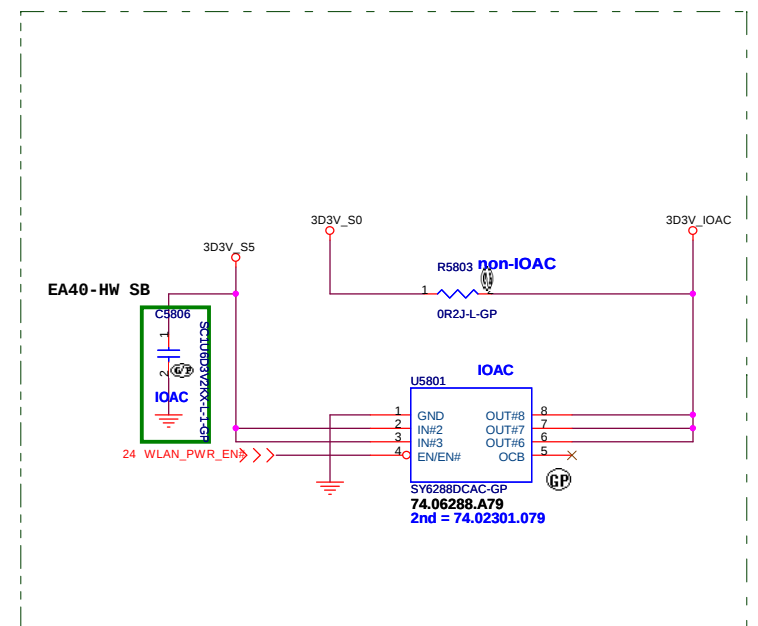
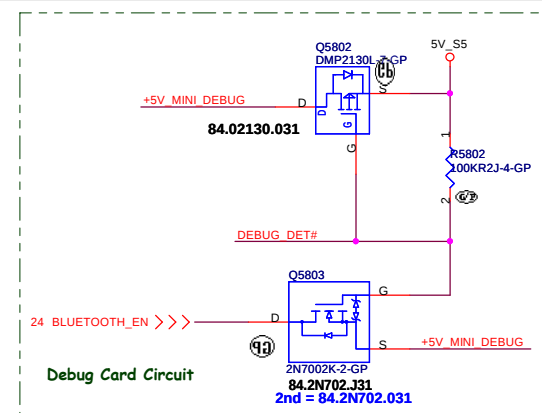
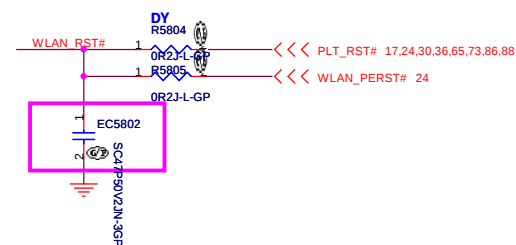
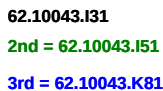
EV		
Title		
HDD / ODD / NGFF SSD		
Size	Document Number	Rev
Custom	EA40 HW ULT	1
Date:	Monday, May 13, 2013	Sheet 56 of 102

5	4	3	2	1
D				
C				
B				
A				

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
E-SATA		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 57	of 102



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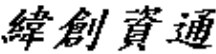
Title			
MINICARD(WLAN)			
Size	Document Number	Rev	
Custom	EA40 HW ULT	1	
Date:	Monday, May 13, 2013	Sheet 58 of	102

SSID = Wireless

Mini Card Connector(mSATA)

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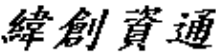
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title WWAN CONN		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013		Sheet 59 of 102

SSID = mSATA

Mini Card Connector(mSATA)

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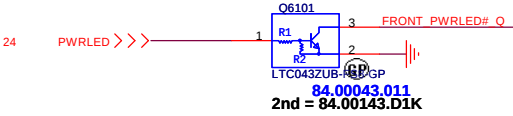
EV

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title mSATA Connector		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 60	of 102

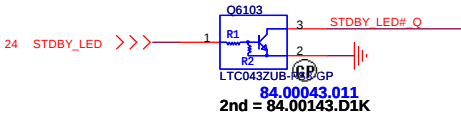
SSID = User.Interface

WLAN_LED

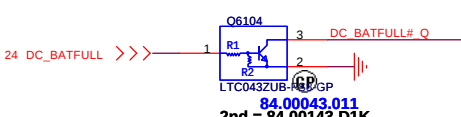
Power button LED



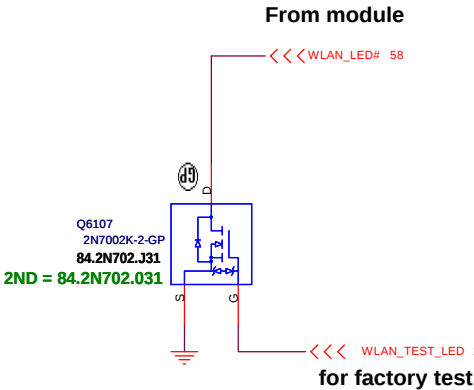
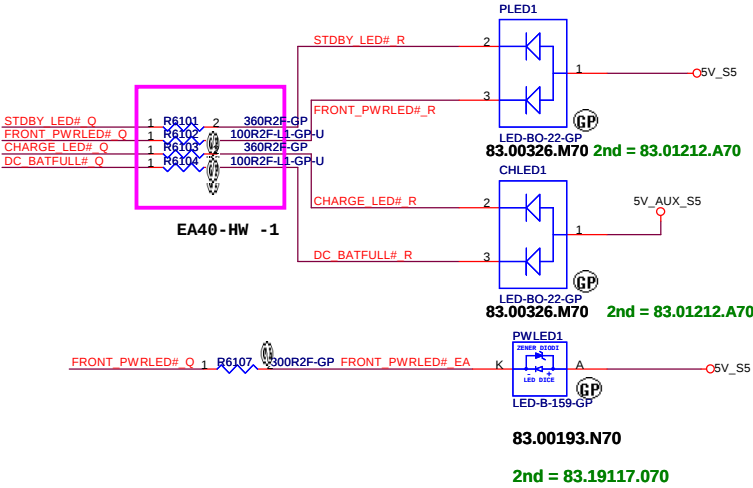
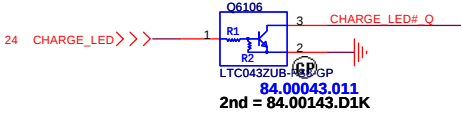
Power STDBY_LED



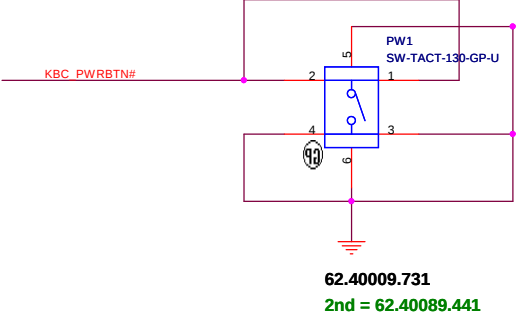
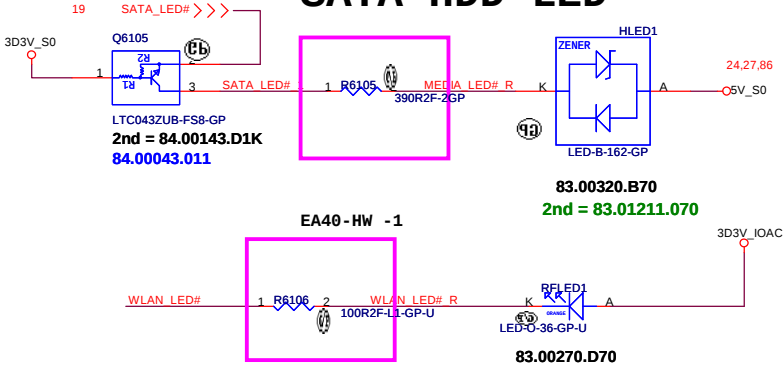
Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)

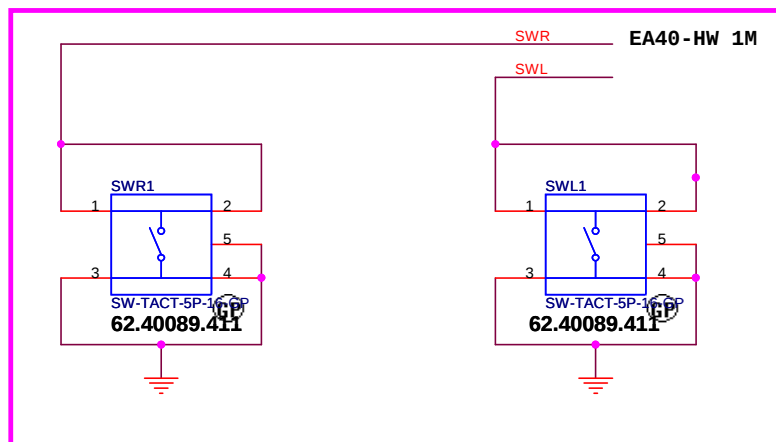


SATA HDD LED

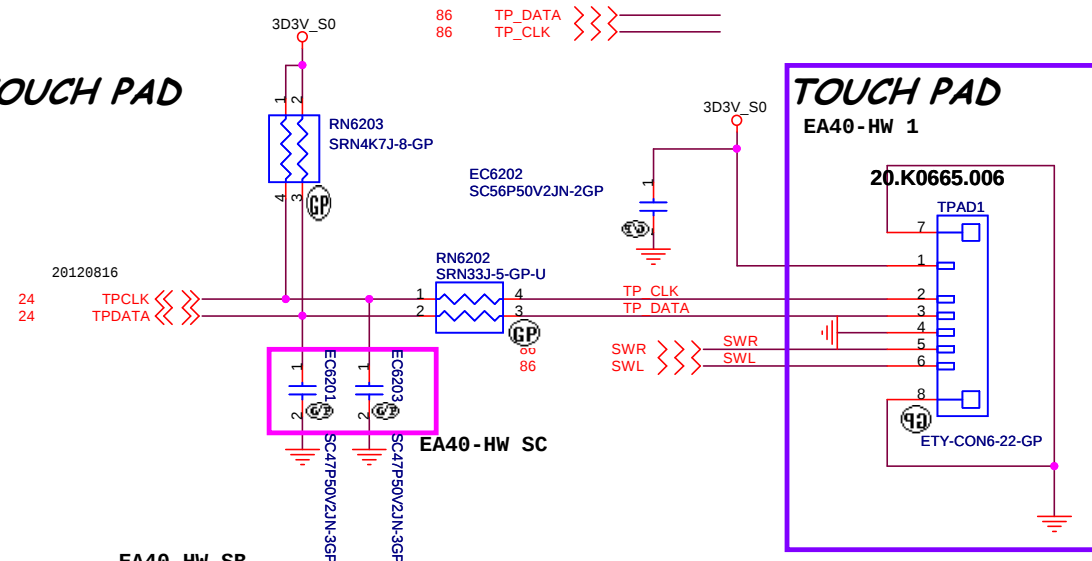


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SSID = KBC

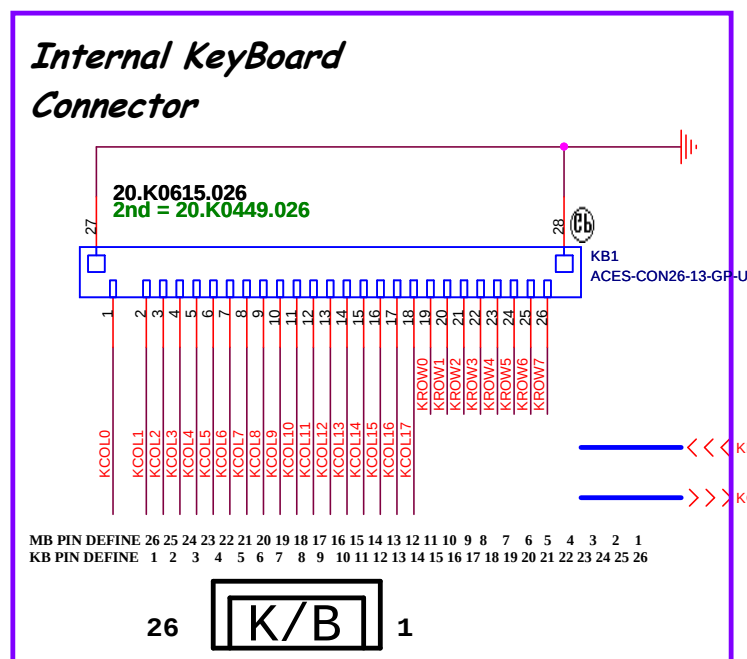


TOUCH PAD

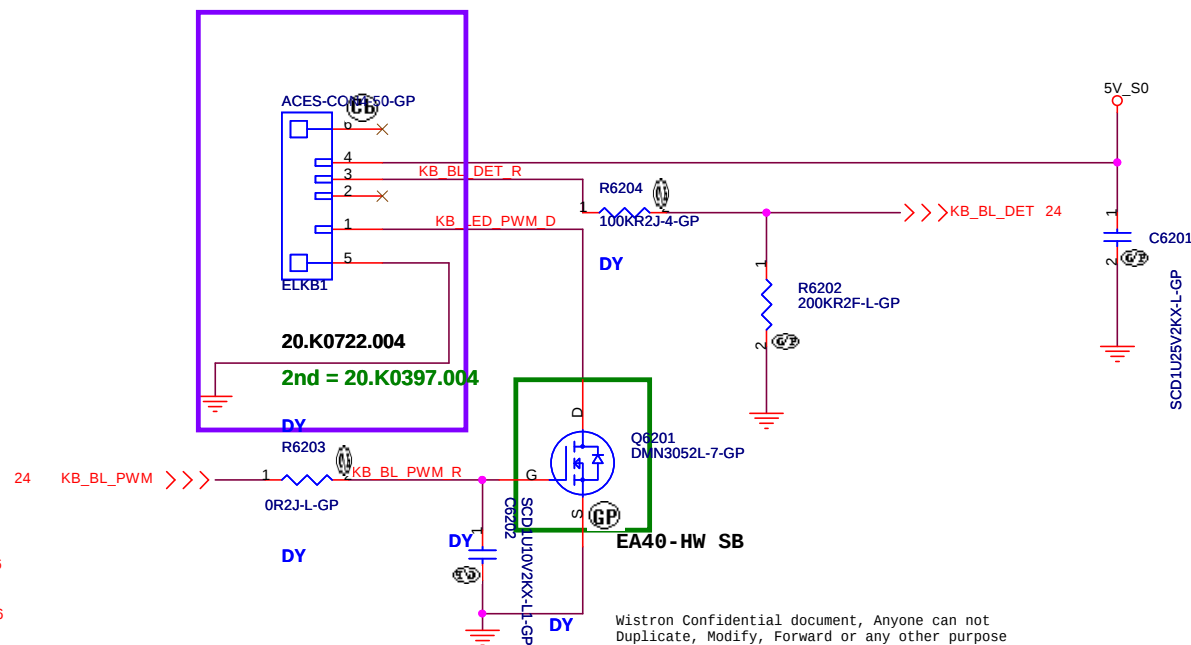


EA40-HW SB

Internal KeyBoard Connector



EA40-HW SB

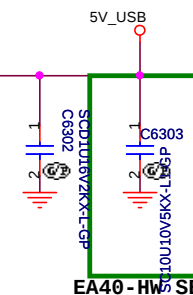
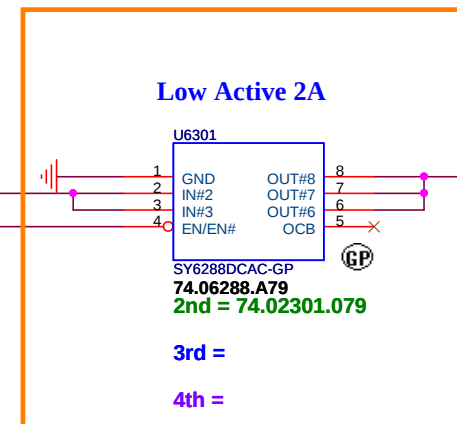
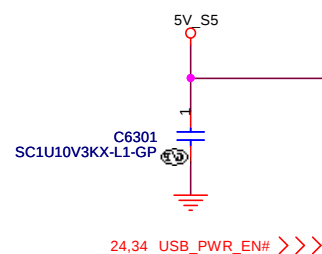
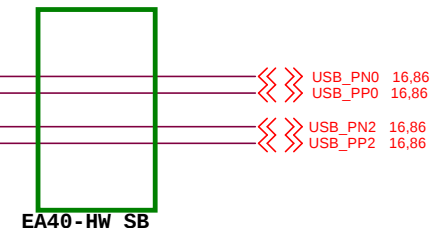
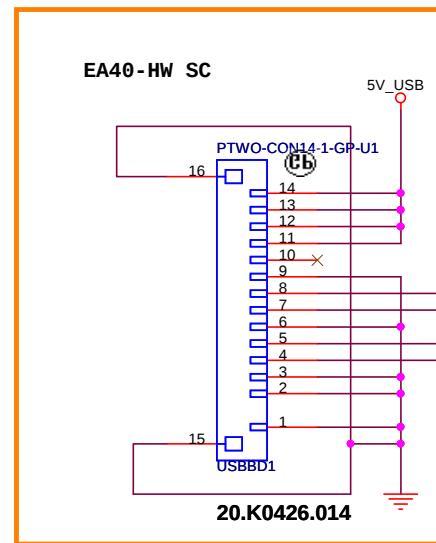
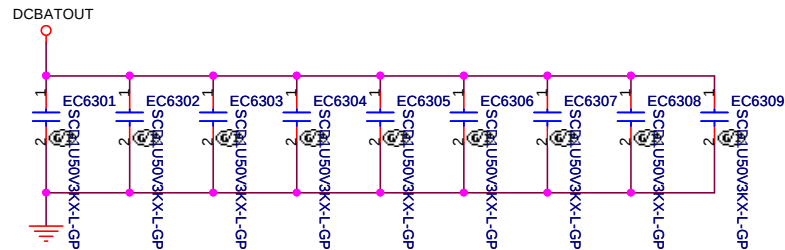


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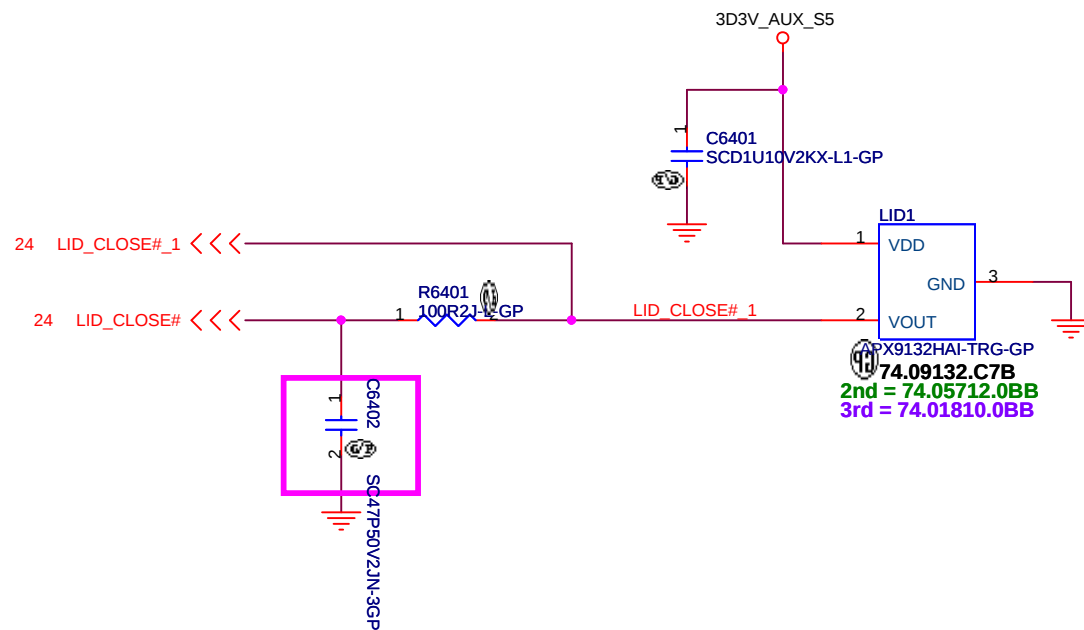
Title		
Key Board/Touch Pad		
Size	Document Number	Rev
Custom	EA40 HW ULT	1
Date:	Monday, May 13, 2013	Sheet 62 of 102



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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
IO Board Connector			
Size	Document Number		Rev
Custom	EA40 HW ULT		1
Date:	Monday, May 13, 2013	Sheet 63 of	102



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Title

Hall Sensor

Size
A4

Document Number

EA40 HW ULT

Rev
1

Date: Monday, May 13, 2013

Sheet 64 of 102

(Blanking)

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Title

SENSOR HUB

Size
A3

Document Number
EA40 HW ULT

Rev
1

Date: Monday, May 13, 2013

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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SDO="H"; address="3Ah"
***SDO="L"; address="38h"**

***CS="H"; mode="I2C"**
CS="L"; mode="SPI"

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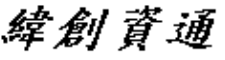
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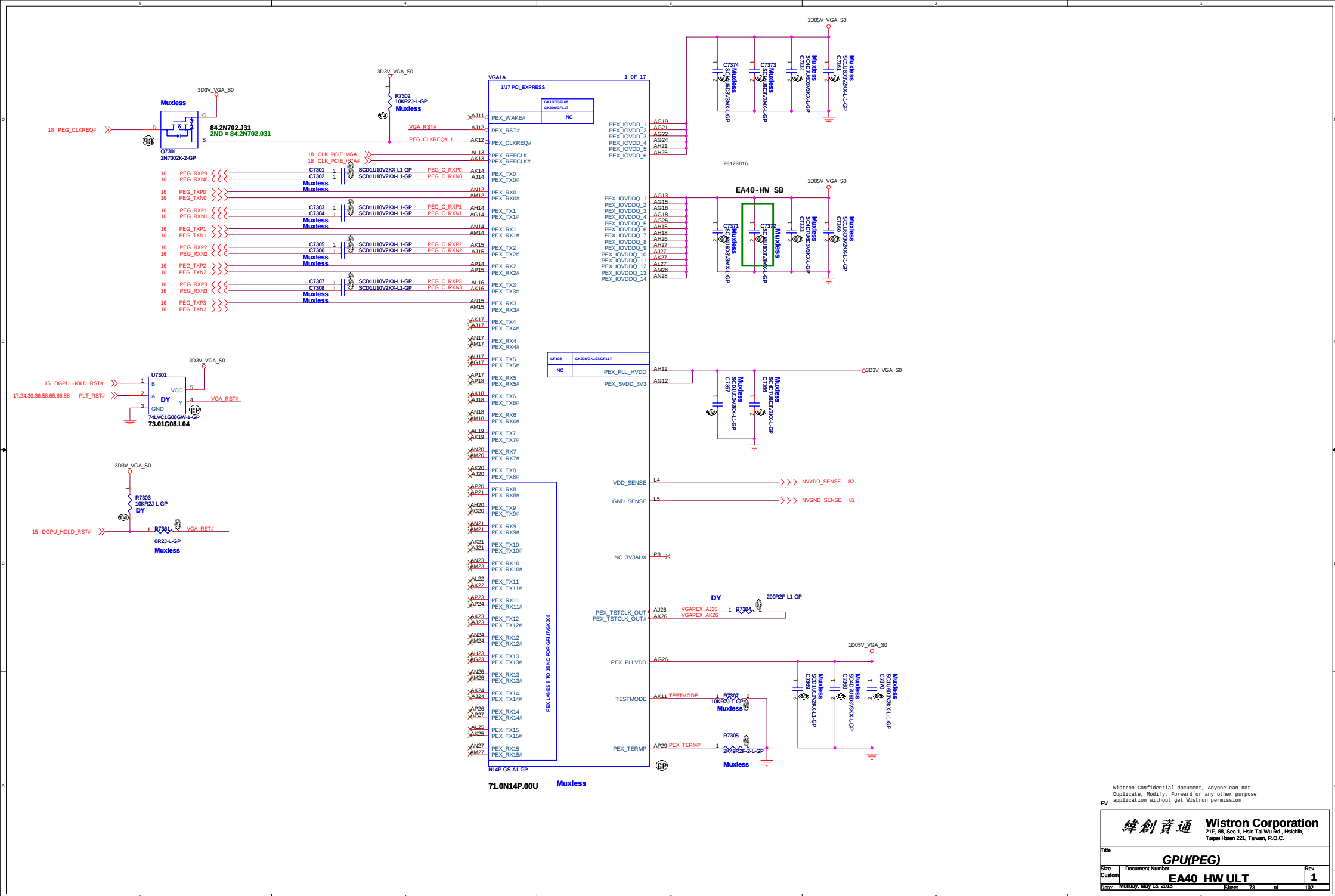
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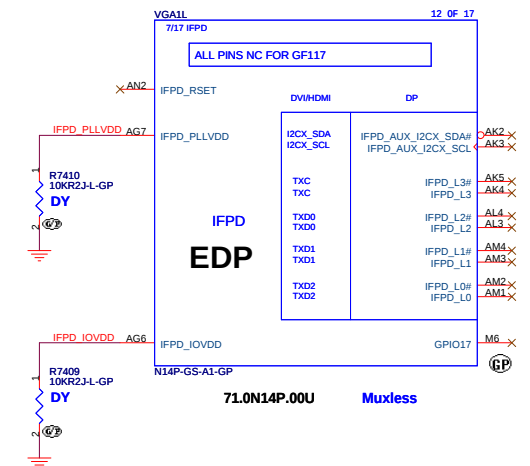
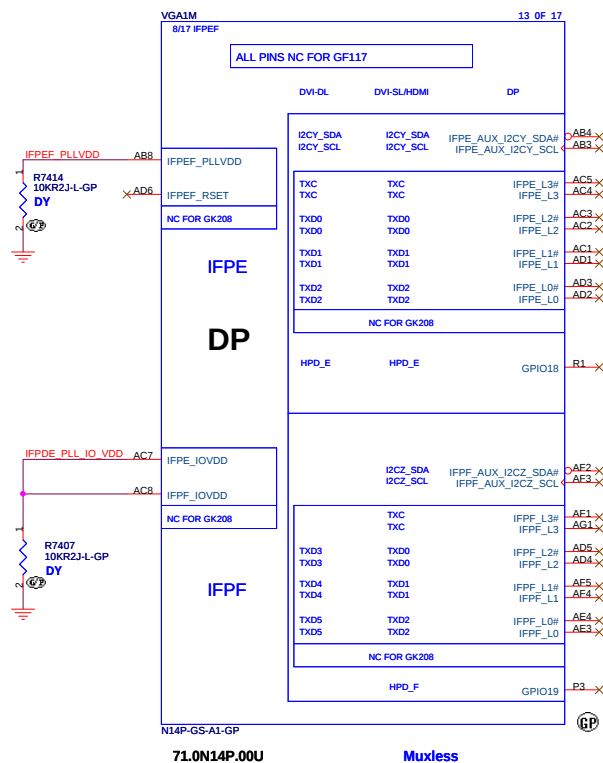
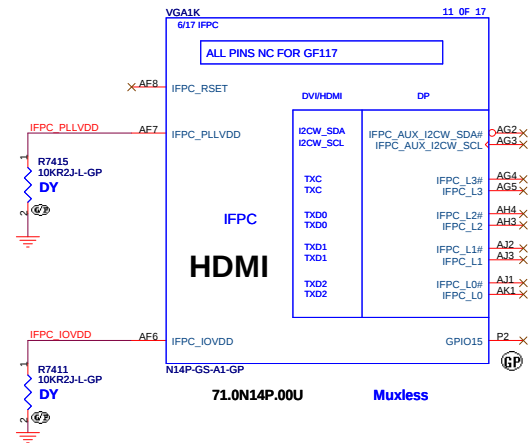
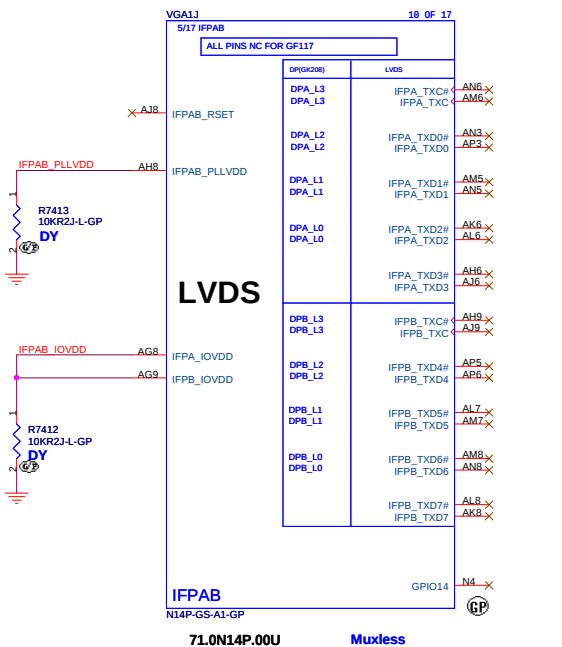


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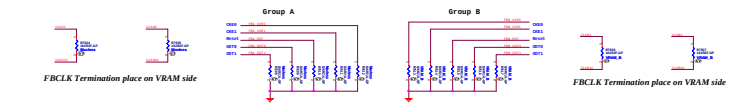
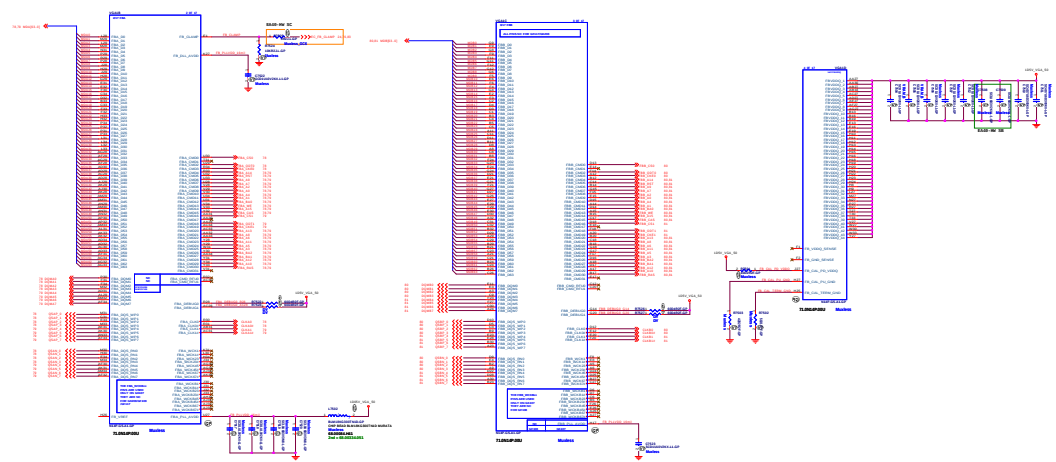
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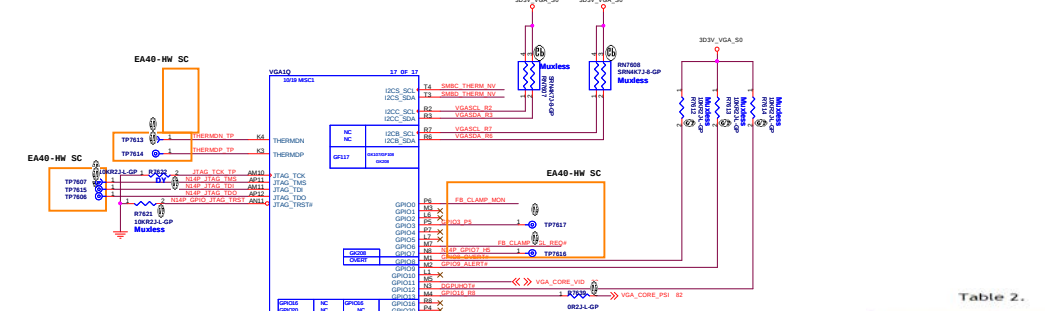
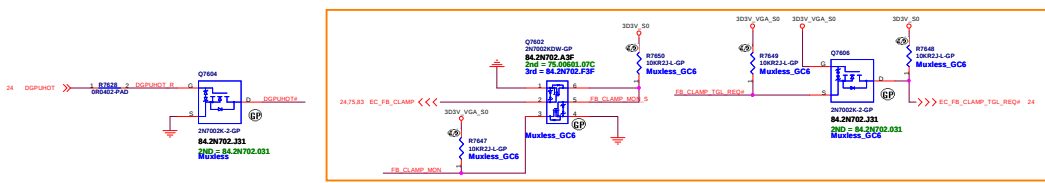
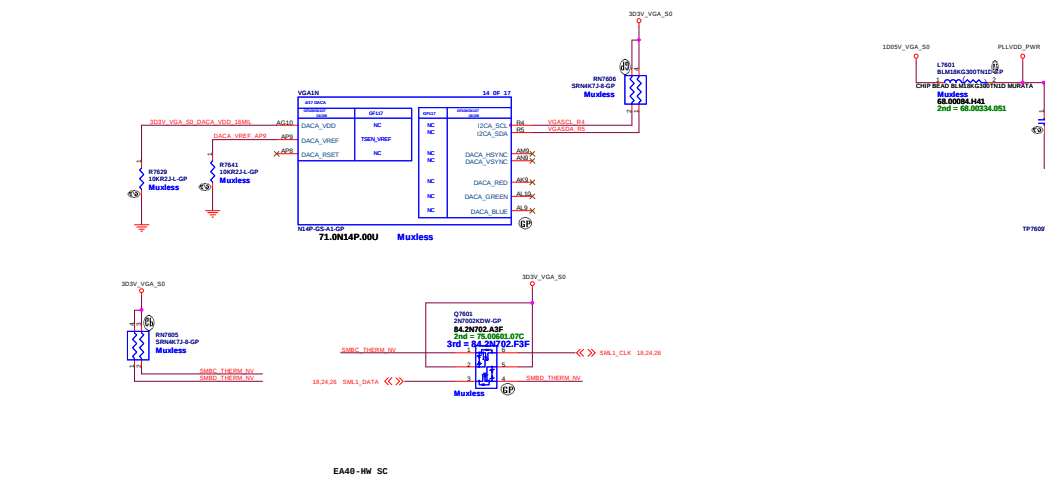
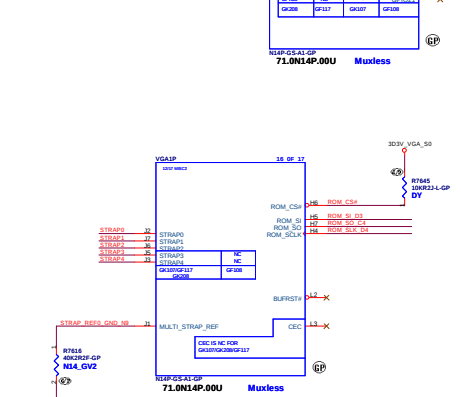


Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

4.99Kohm	64.49915.6DL
10Kohm	64.10025.1.0L
15Kohm	64.15025.6DL
20Kohm	64.20025.6DL
24.9Kohm	64.24925.6DL
30.1Kohm	64.30125.6DL
34.8Kohm	64.34825.6DL
45Kohm	64.45325.6DL



N14M-GE use Binary Strap. Please see the below information.

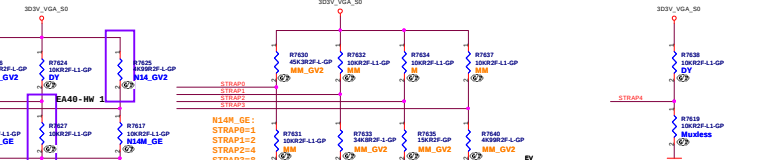
Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VEHDR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

Strap Pin Name	Logical Strapping Bit0	Logical Strapping Bit1	Logical Strapping Bit2	Logical Strapping Bit3
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	SOB0_EXPOSED	SOB0_PADCFG[2]	SOB0_PADCFG[1]	SOB0_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOB1_EXPOSED	SOB1_EXPOSED	SOB1_EXPOSED	SOB1_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_ORN3	PCIE_MAX_SPEED	DF_PLL_VDD33V

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
Configuration 256Mx16 DDR3	Samsung	0x8	1.5 V / 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0x0	1.5 V / 1.5 V	MT41K256M16HA-1070JE	900	N/A	Production ready
Configuration 128Mx16 DDR3	Hynix	0x3	1.5V / 1.5V	H5TQ4G63MFR-11C	900	N/A	Production ready
	Samsung	0x5	1.5 V / 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
Configuration 128Mx16 DDR3	Hynix	0x6	1.5V / 1.5V	H5TQ2G63DFR-11C	900	N/A	Production ready



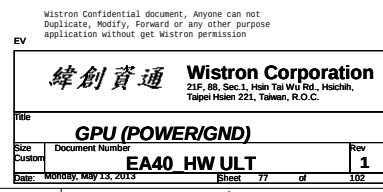
ROM_SCLK	Strap2
N14P-GT1-A2	0x0FE4 0010 15K ohm pull down 0100 25K ohm pull down
N14P-GV2-B-A1	0x1252 1000 5K ohm pull up 0010 15K ohm pull down

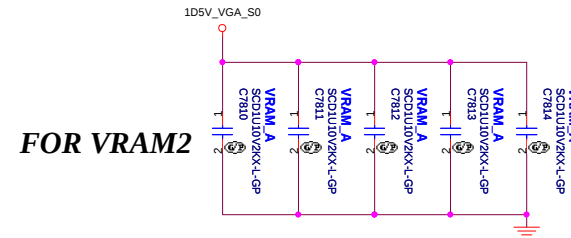
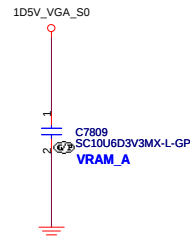
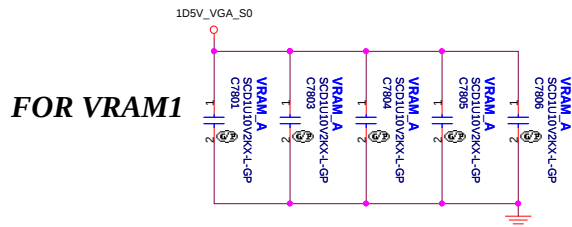
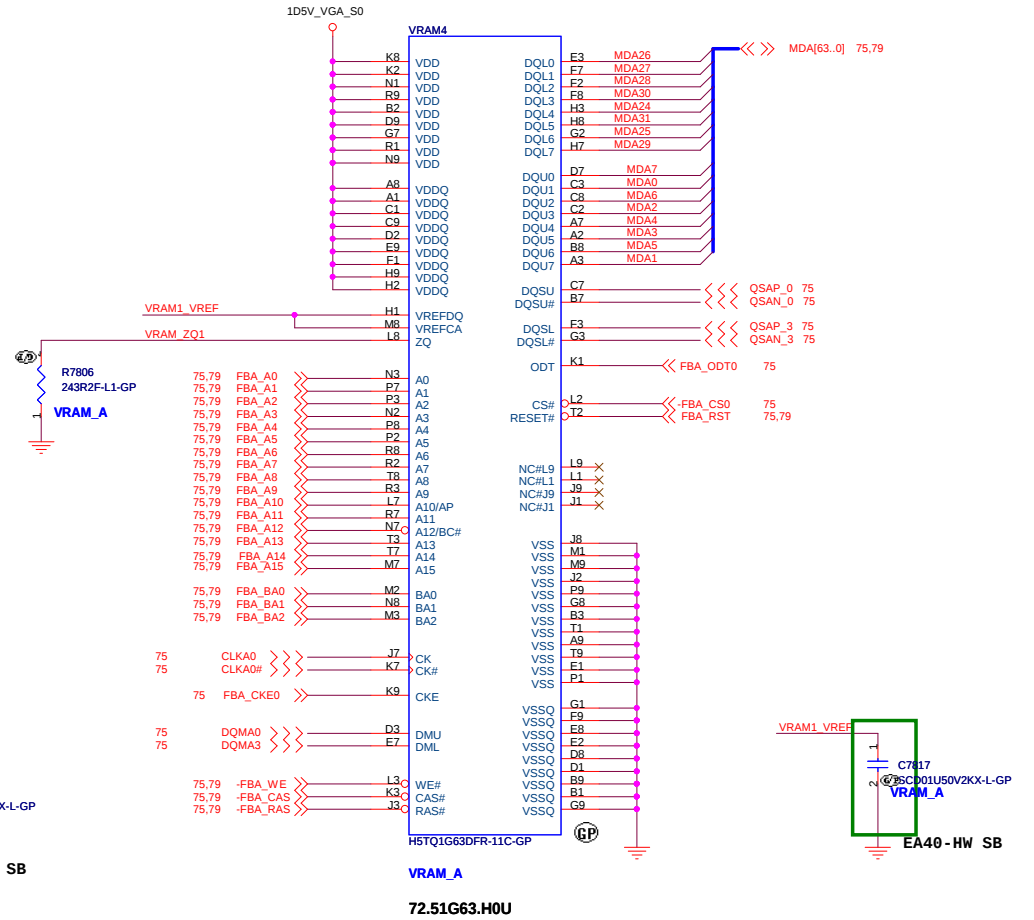
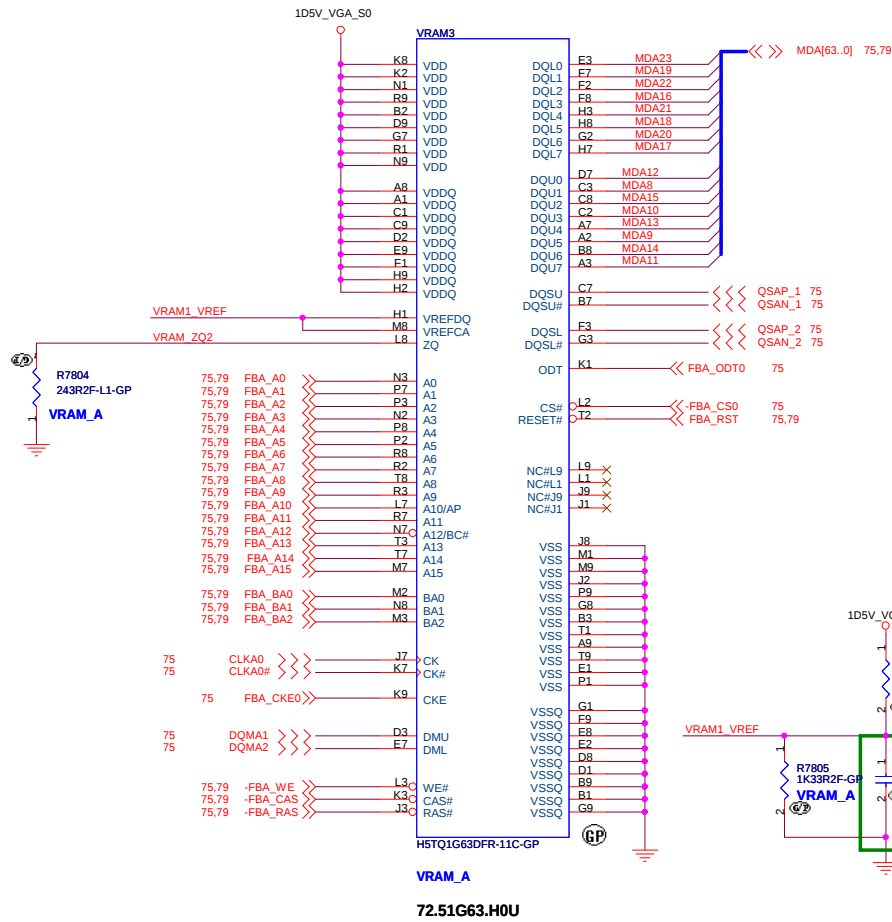
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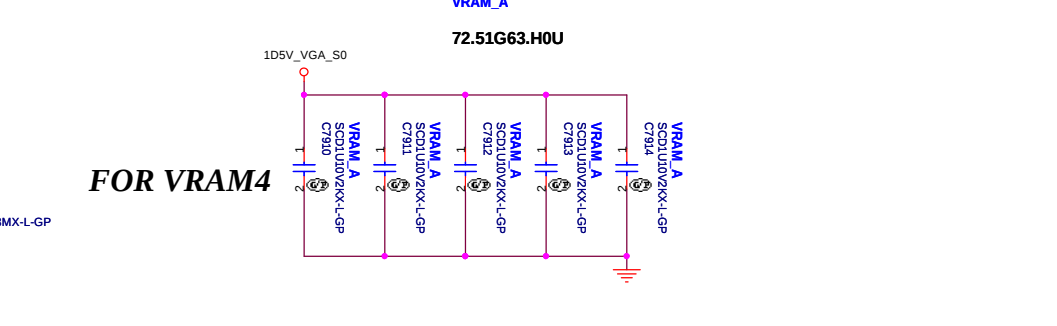
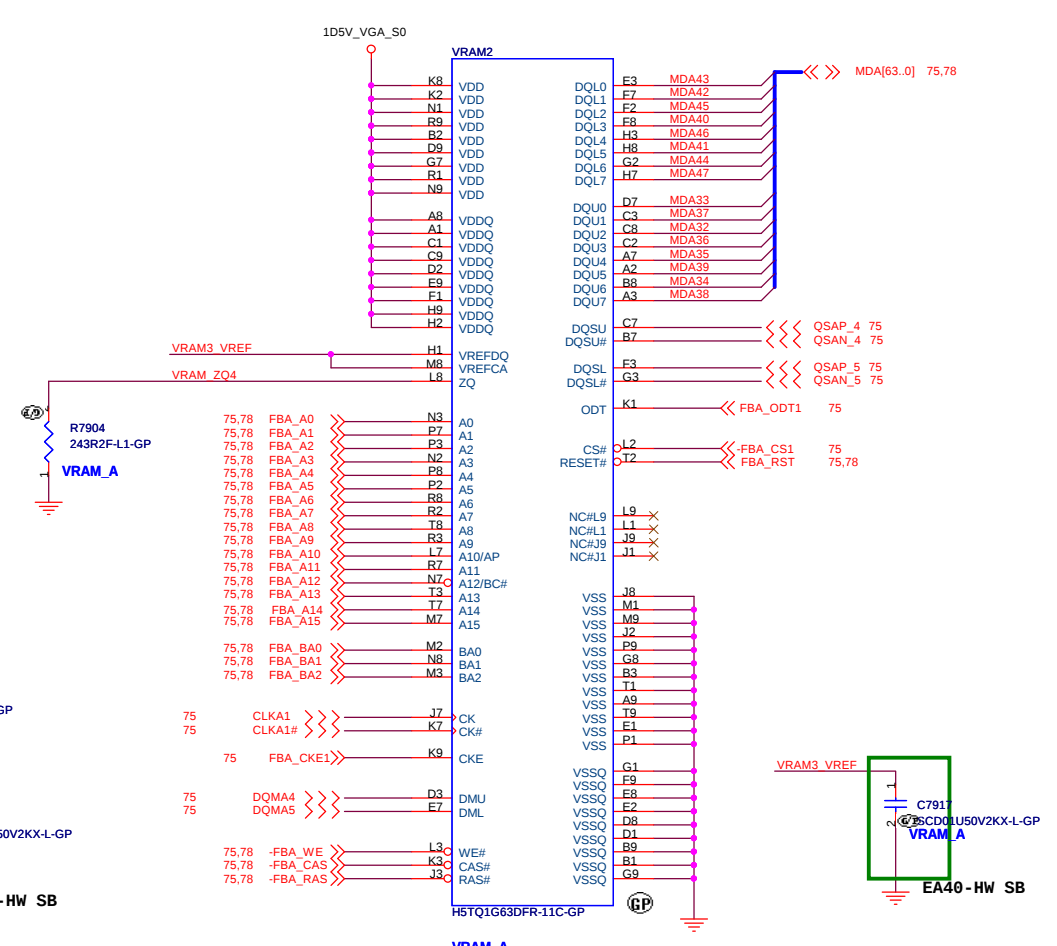
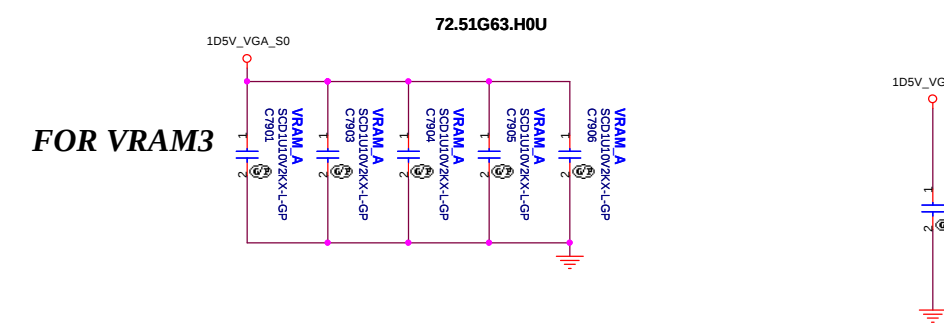
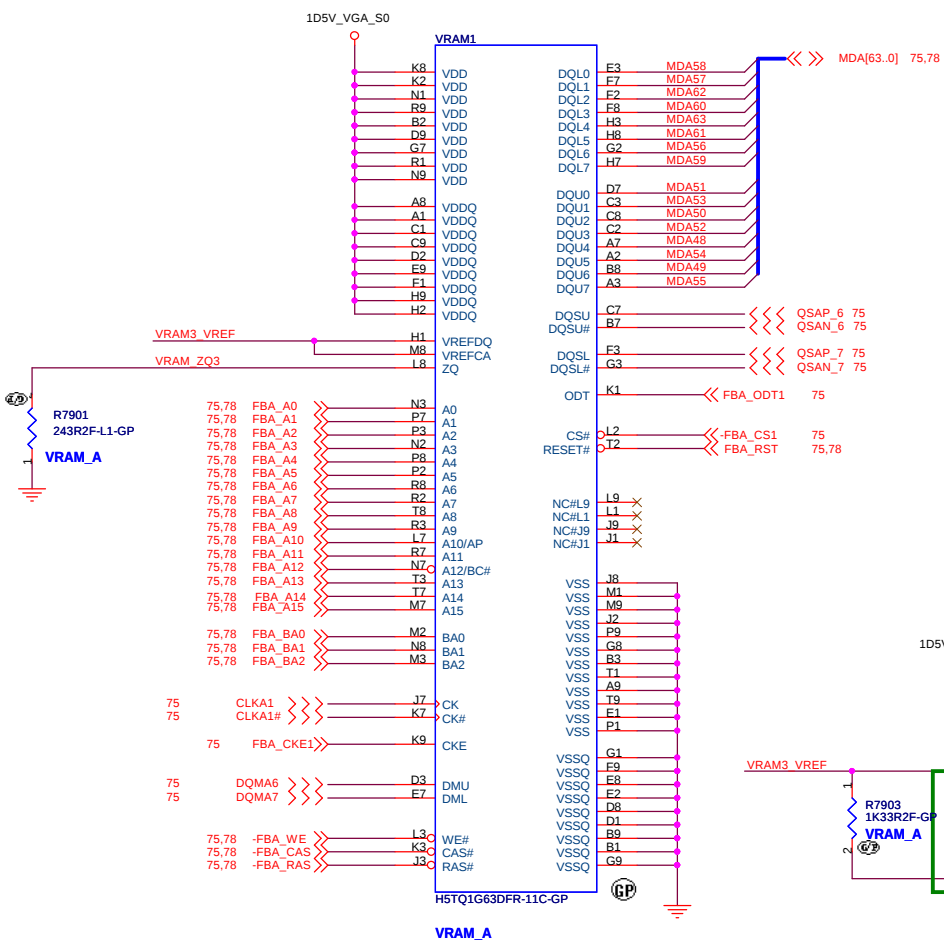
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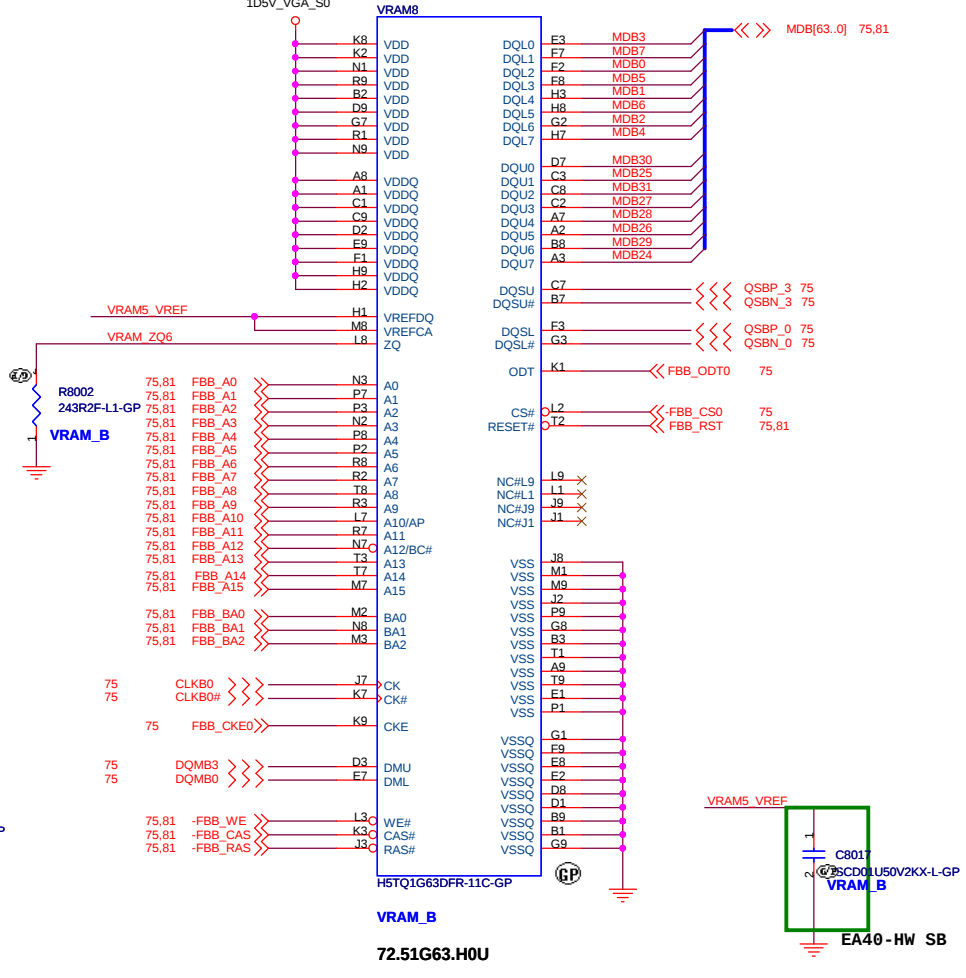
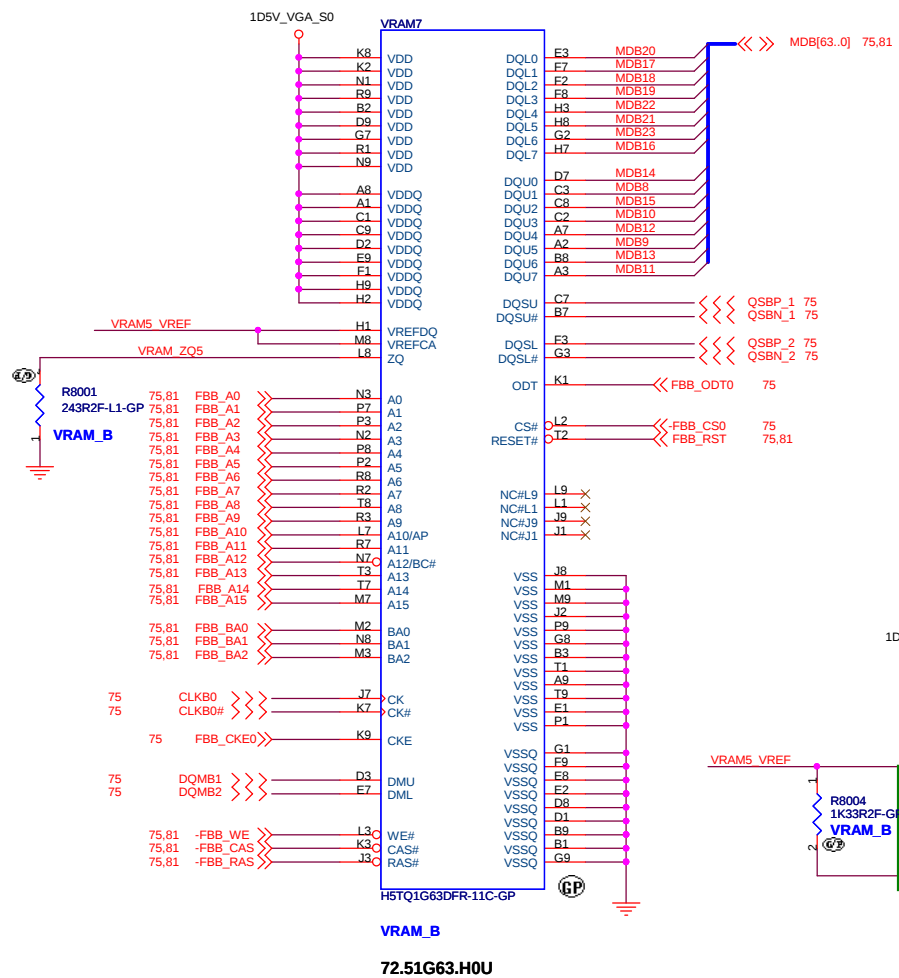




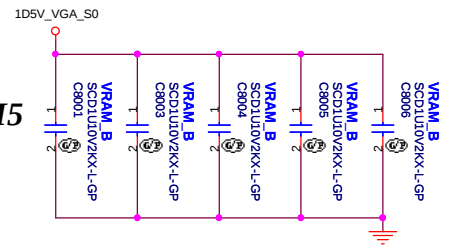
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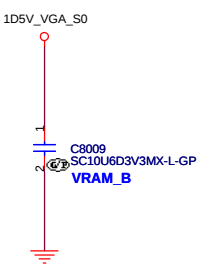


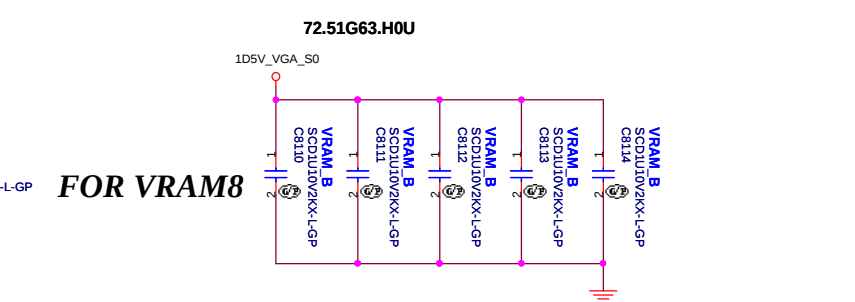
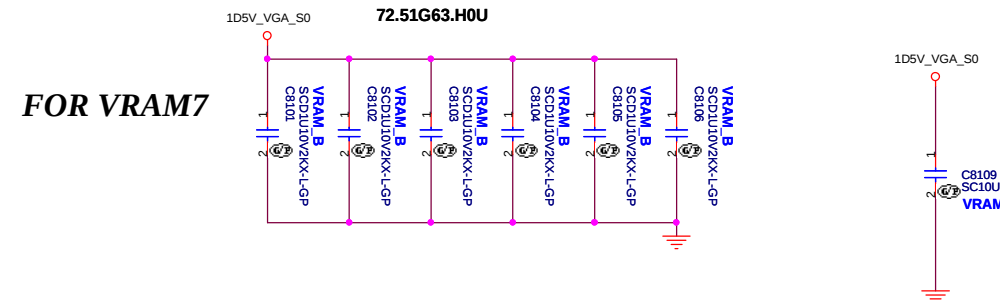
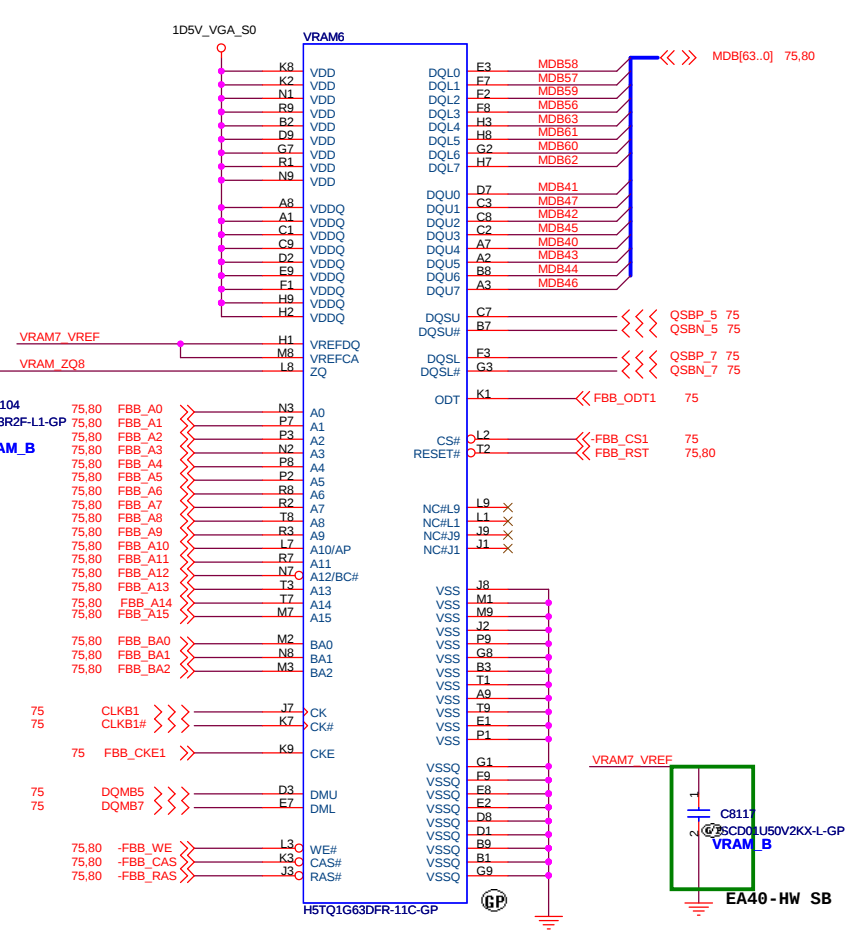
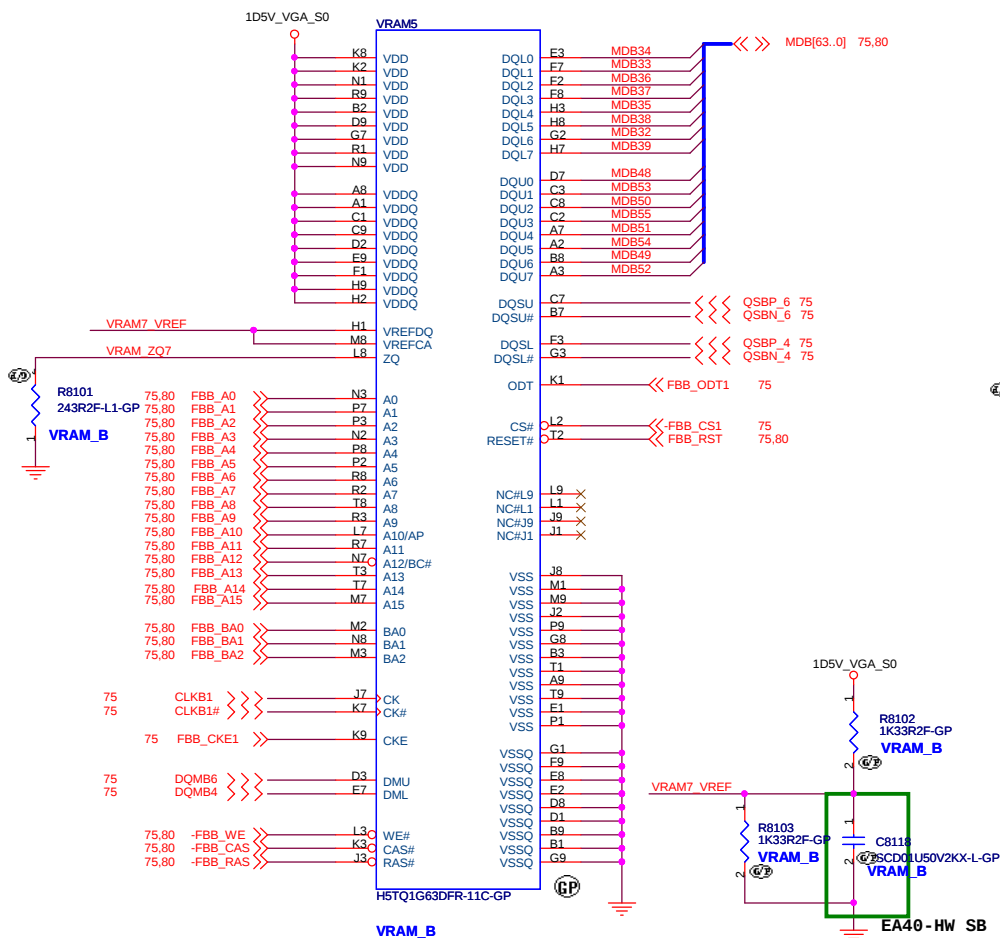


FOR VRAM5



FOR VRAM6

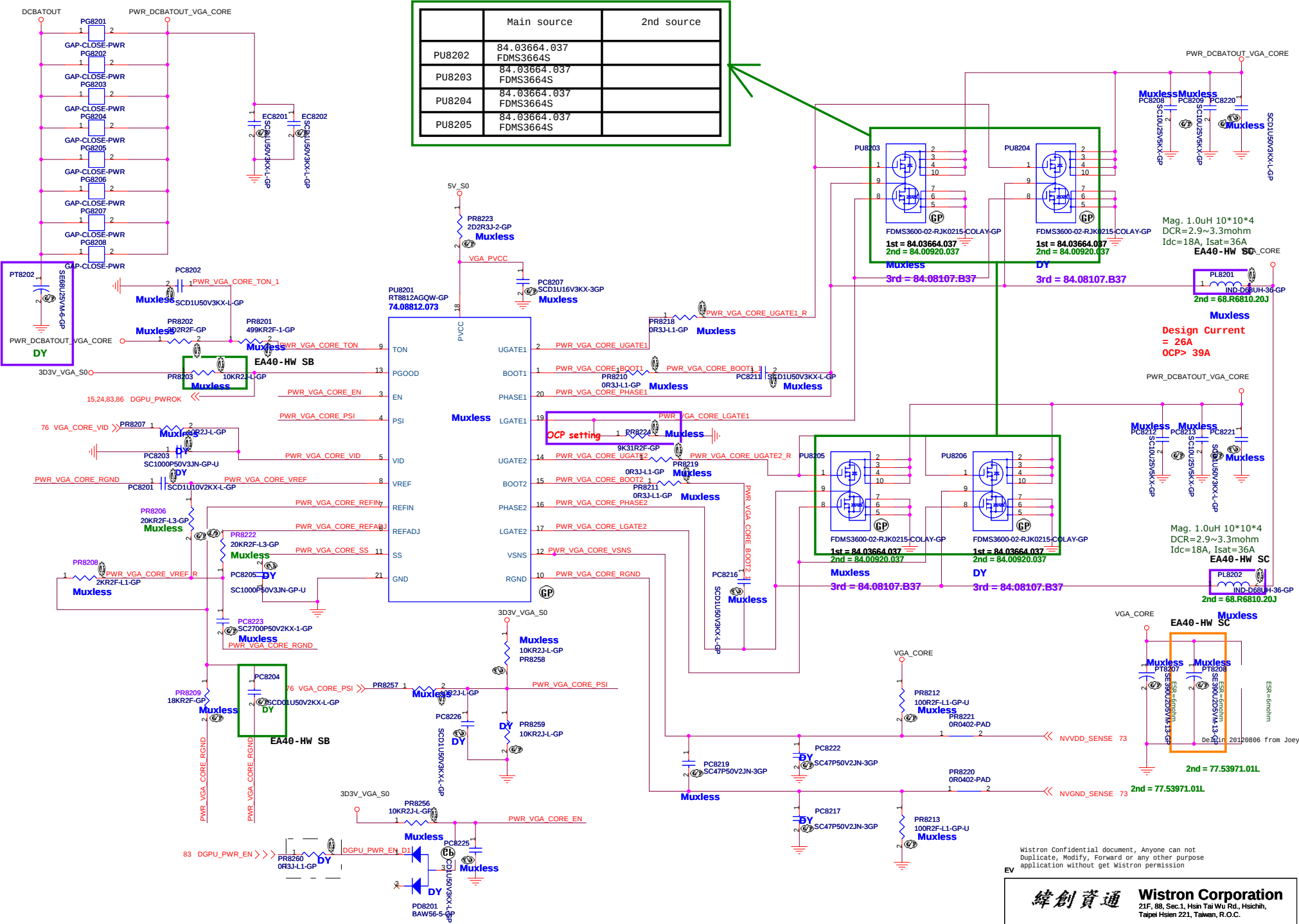




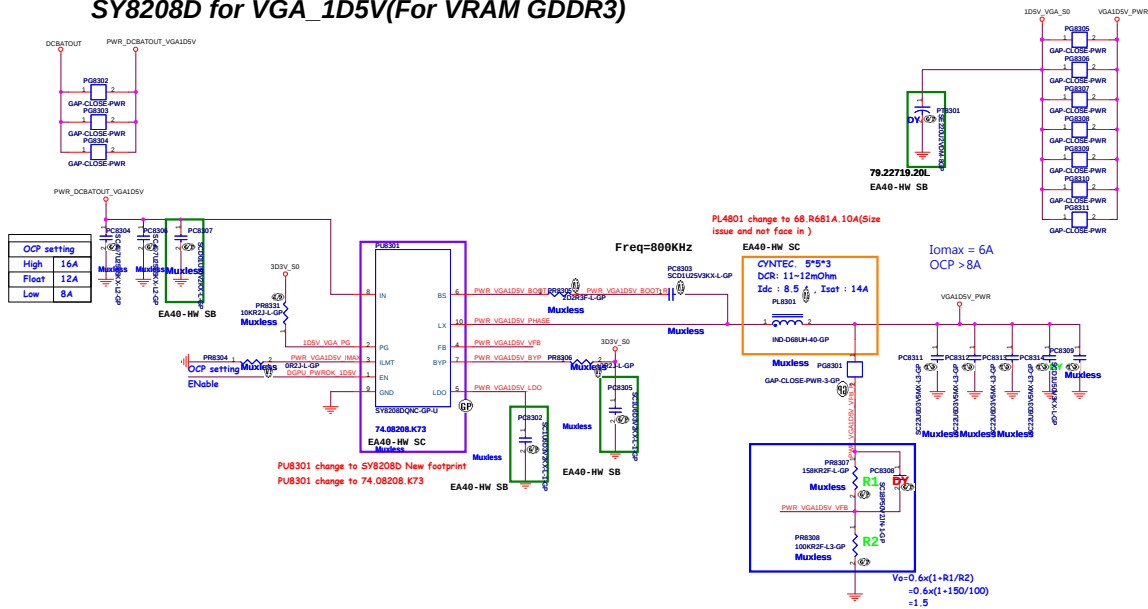
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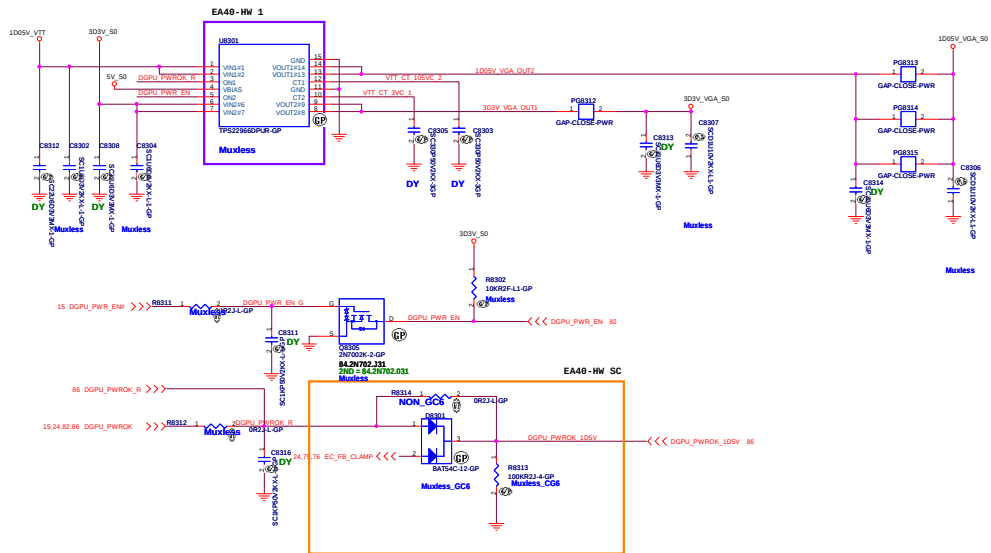
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PU8205	84.03664.037 FDMS3664S	



SY8208D for VGA 1D5V(For VRAM GDDR3)



3D3V_S0 to 3D3V_VGA_S0
1D05V VTT to 1D05V VGA S0



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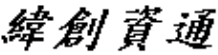
DISCRETE VGA POWER

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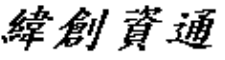
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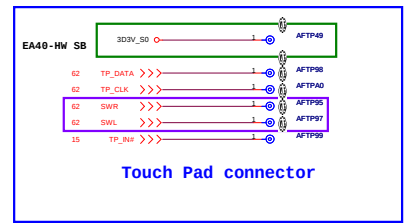
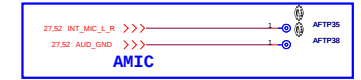
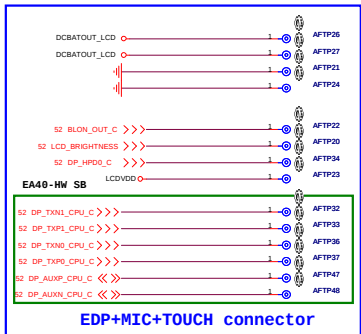
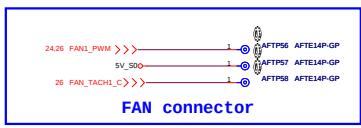
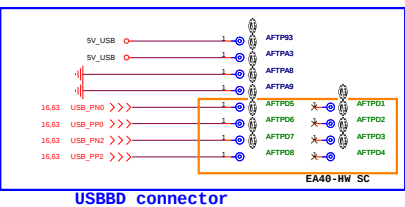
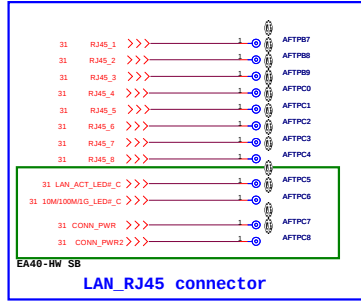
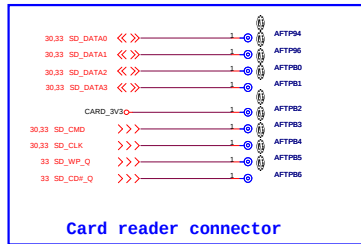
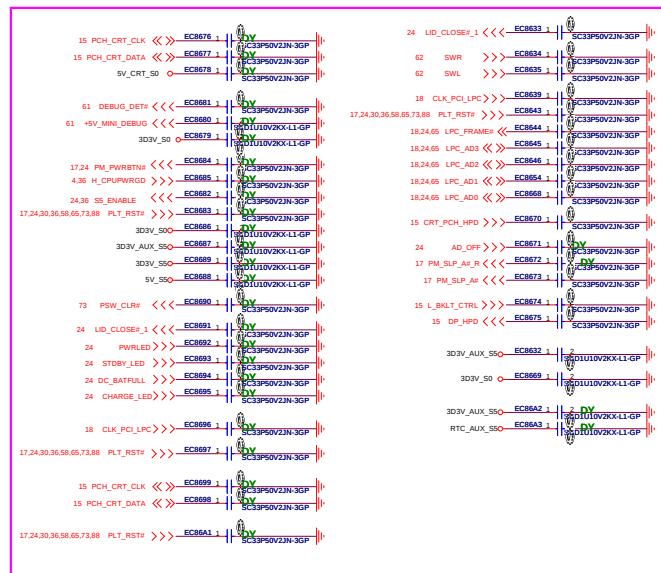
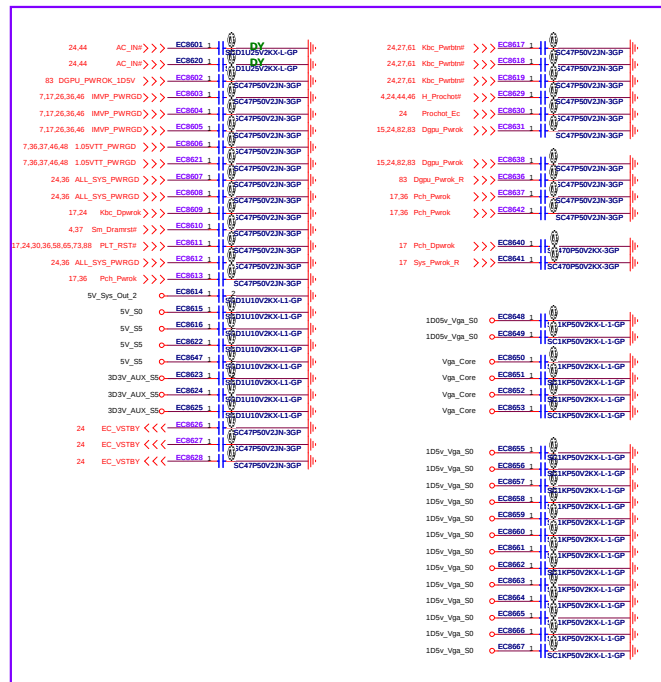
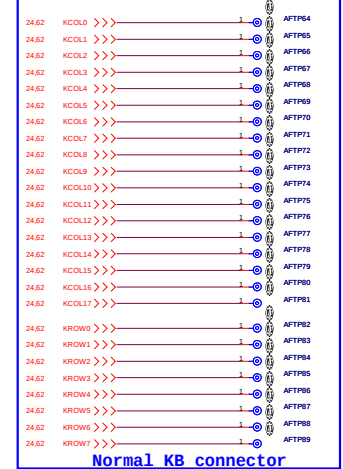
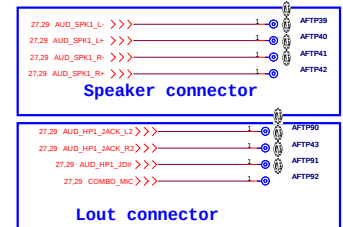
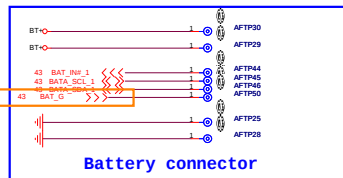
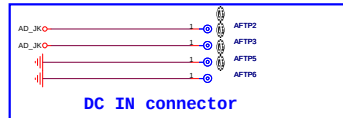
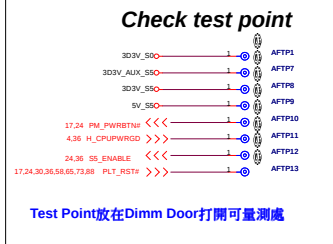
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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	123-129
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	78-84
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	890-896

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Title				
Express Card				
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Title				
Bottom Docking				
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title		
PCH_XDP		
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Title		
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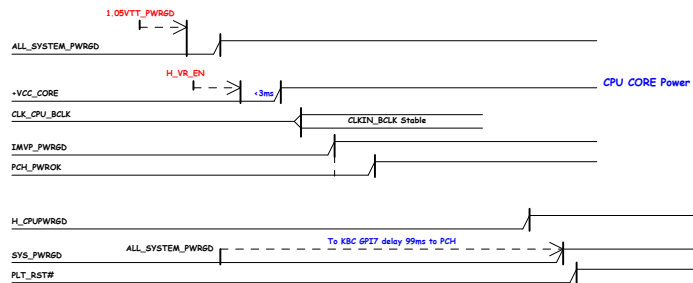
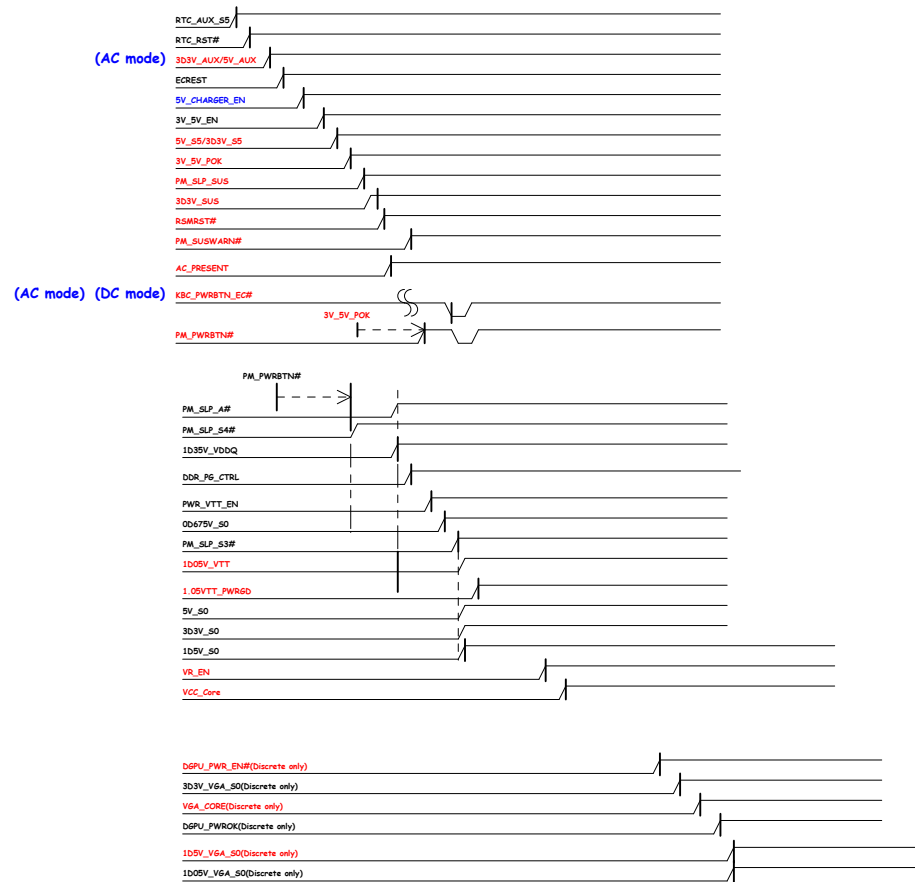
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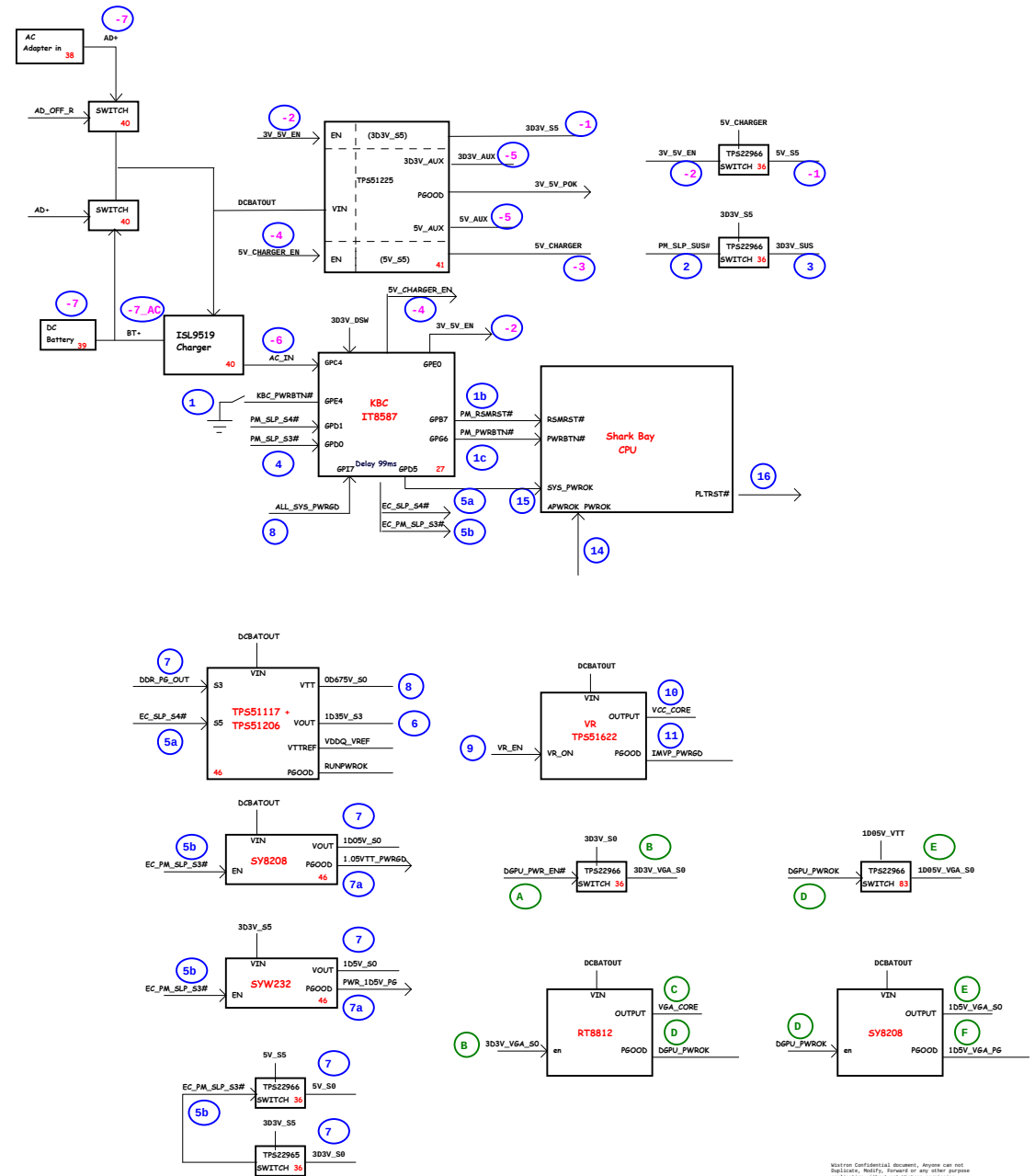
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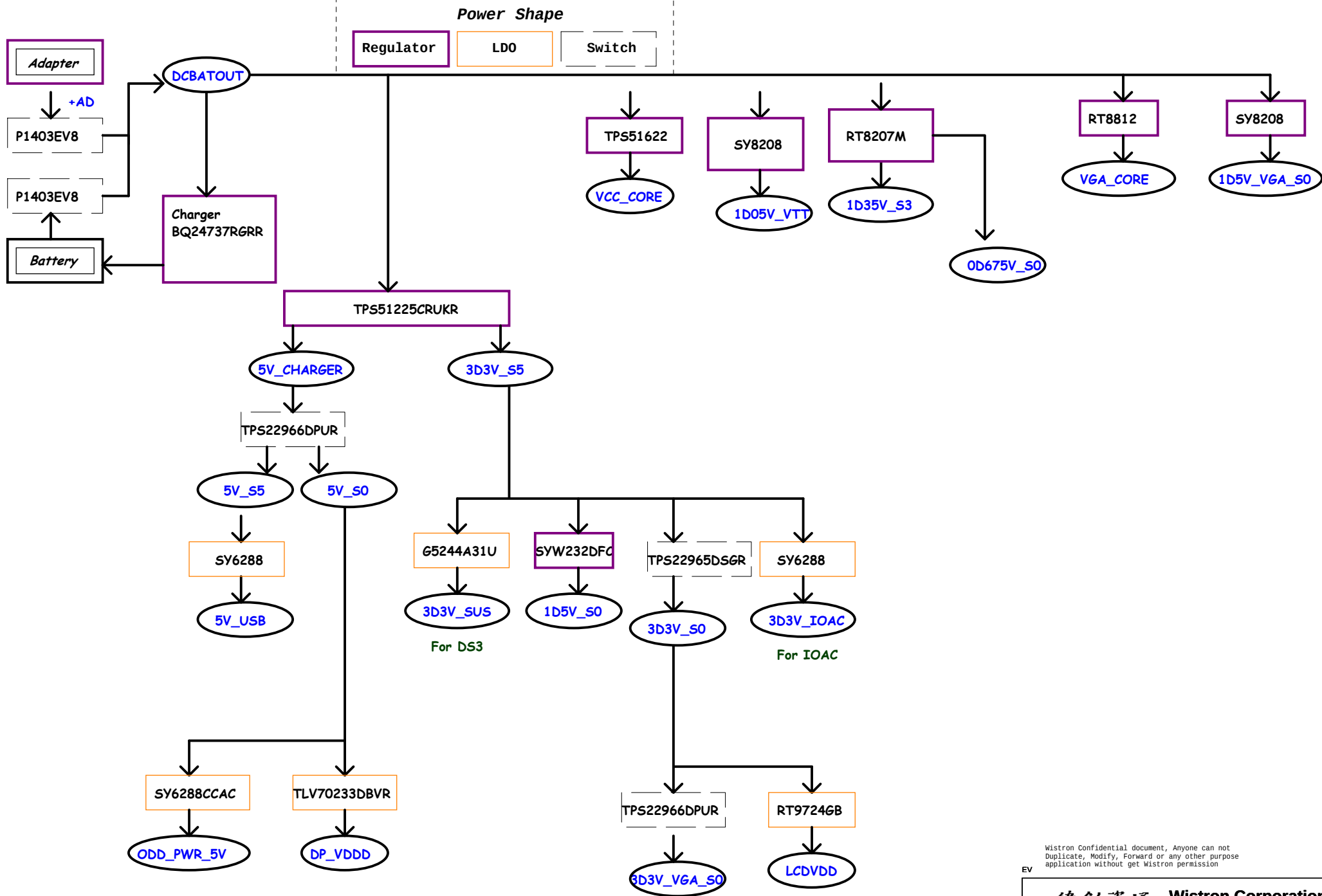
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Intel-Power Up Sequence



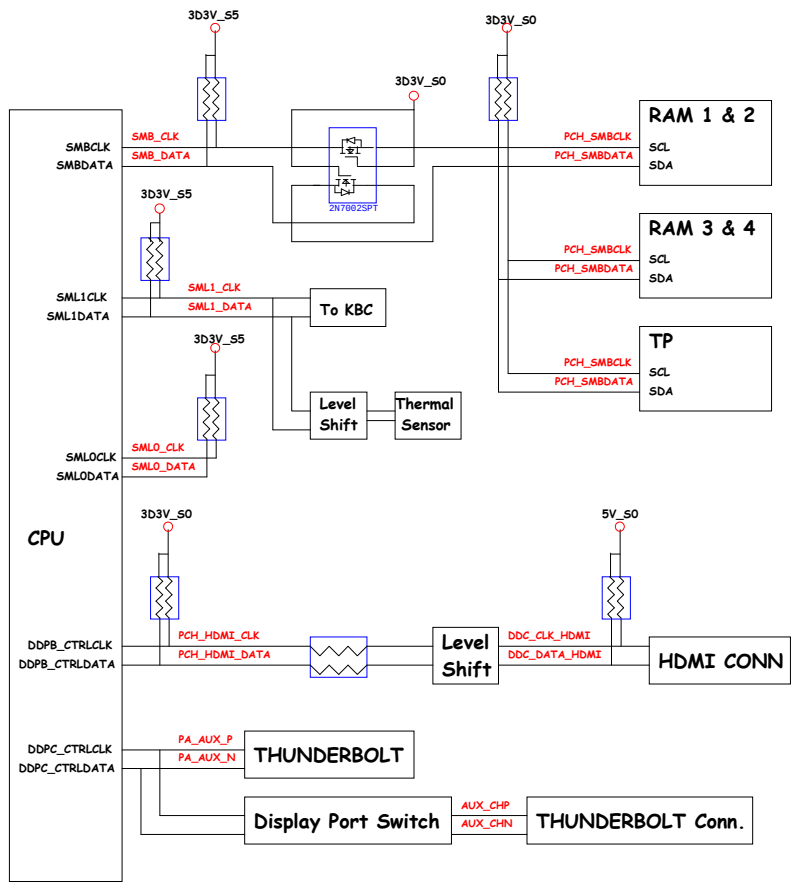
SHARK BAY POWER UP SEQUENCE DIAGRAM



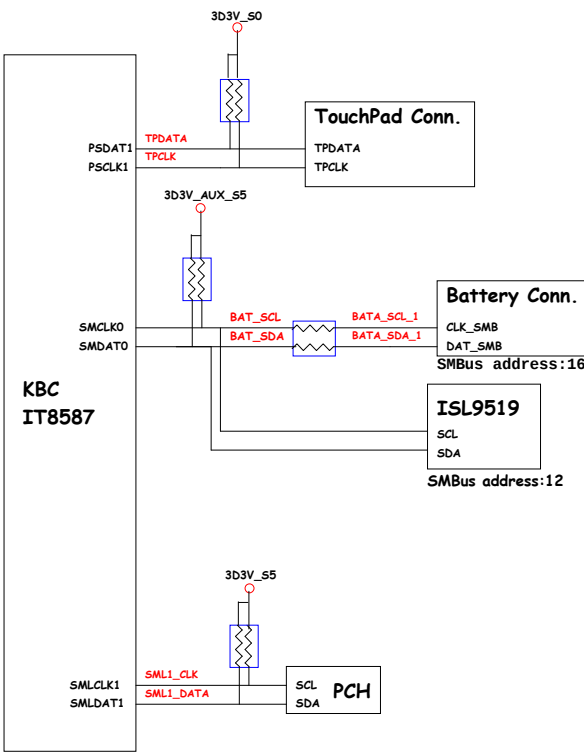


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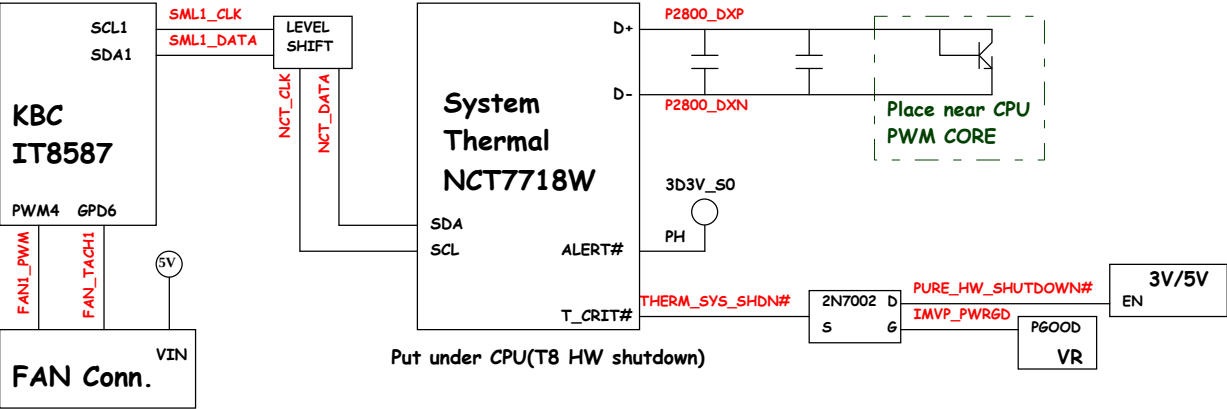
PCH SMBus Block Diagram



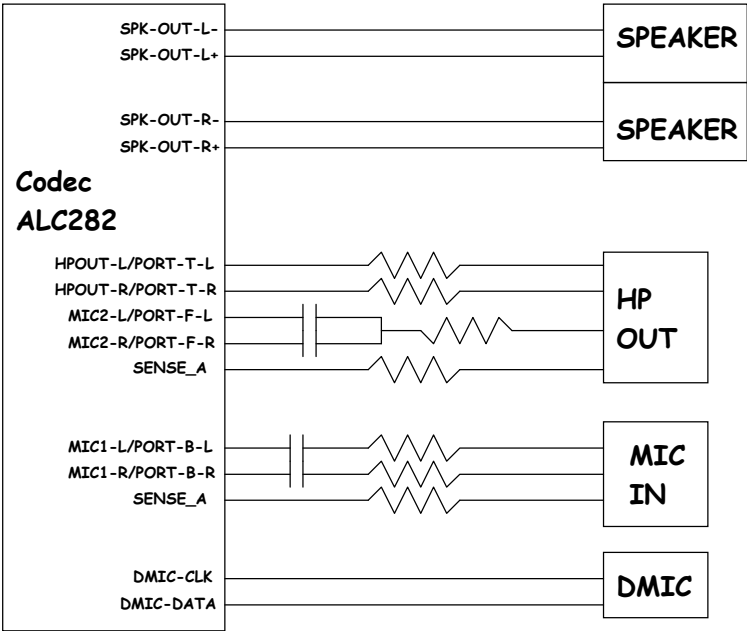
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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