JV71-TR Block Diagram

Project code: 91.4FP01.001
PCB P/N : 48.4FP02.0SB
REVISION : 09243-SB

DDR2 667/800 MHz 16,17
DDR2 667/800 MHz 16,17
667/800MHz
667/800MHz
AMD Caspian CPU S1G3 (35W)
638-Pin uFCPGA638 4,5,6,7
OUT
IN
16X16
G792 34
CRT 20
LCD 19
HDMI 21
VDDR3 57,58
16X
M92XT 53,54,55,56,57,58,59
CLK GEN. 3
ICS9LPRS480BKLFT 71.09480.A03
RTM880N-796-VB-GRT 71.00880.A03
North Bridge
AMD RS880M
CPU I/F LVDS, CRT I/F
INTEGRATED GRAHPICS
8,9,10
LAN Giga LAN BCM5784 26
TXFM 27
RJ45 27
PCIex1
Mini Card Kedron a/b/g/n 33
A-Link 4X4
INT MIC 30
Line In 30
MIC In 30
INT.SPKR 30
Line Out (SPDIF) 30
Codec ALC888S 28
AZALIA
OP AMP MAX9789 29
South Bridge
AMD SB710
USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
ATA 66/100
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
11,12,13,14,15
LPC BUS
KBC Winbond WPC773 35
BIOS MXIC MX25L1605 36
LPC DEBUG CONN. 36
Touch Pad 37
INT. KB 35
RJ11
MODEM MDC Card 31
SATA
USB
HDD SATA 22
ODD SATA 23
Mini USB Blue Tooth 24
Finger Printer 31
CardReader Realtek RTS5159 32
MS/MS Pro/xD /MMC/SD 5 in 1 32
USB 4 Port 25
Camera
Daughter Board USB Board 08649
Daughter Board LED Board 08651
Daughter Board Finger Printer Board 08650
Daughter Board Mini sensor Board 08696

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC RT8205A 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC RT8209B 48	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)

RT9025 49	
5V_S5	1D1V_M92

RT9161 49	
3D3V_S0	2D5V_S0 (200mA)

G957 49	
3D3V_S0	1D5V_S0 (1A)

G9161 49	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

UMA

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: JV71-TR | Rev: SB
Date: Monday, July 06, 2009 | Sheet 1 of 61

UMA

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Title: **USB/PCIE Routing**

Size	Document Number	Rev
A3	JV71-TR	SA

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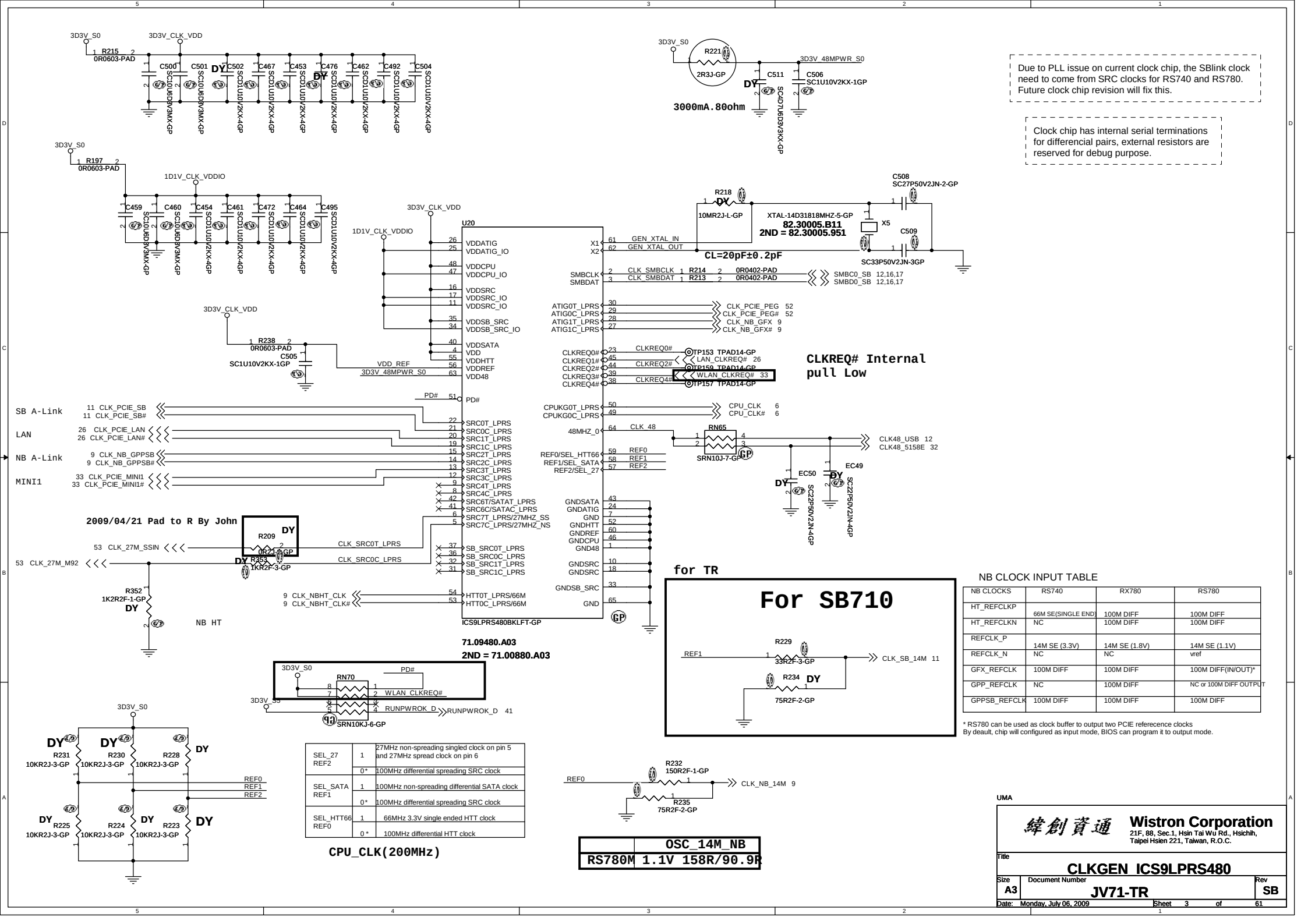
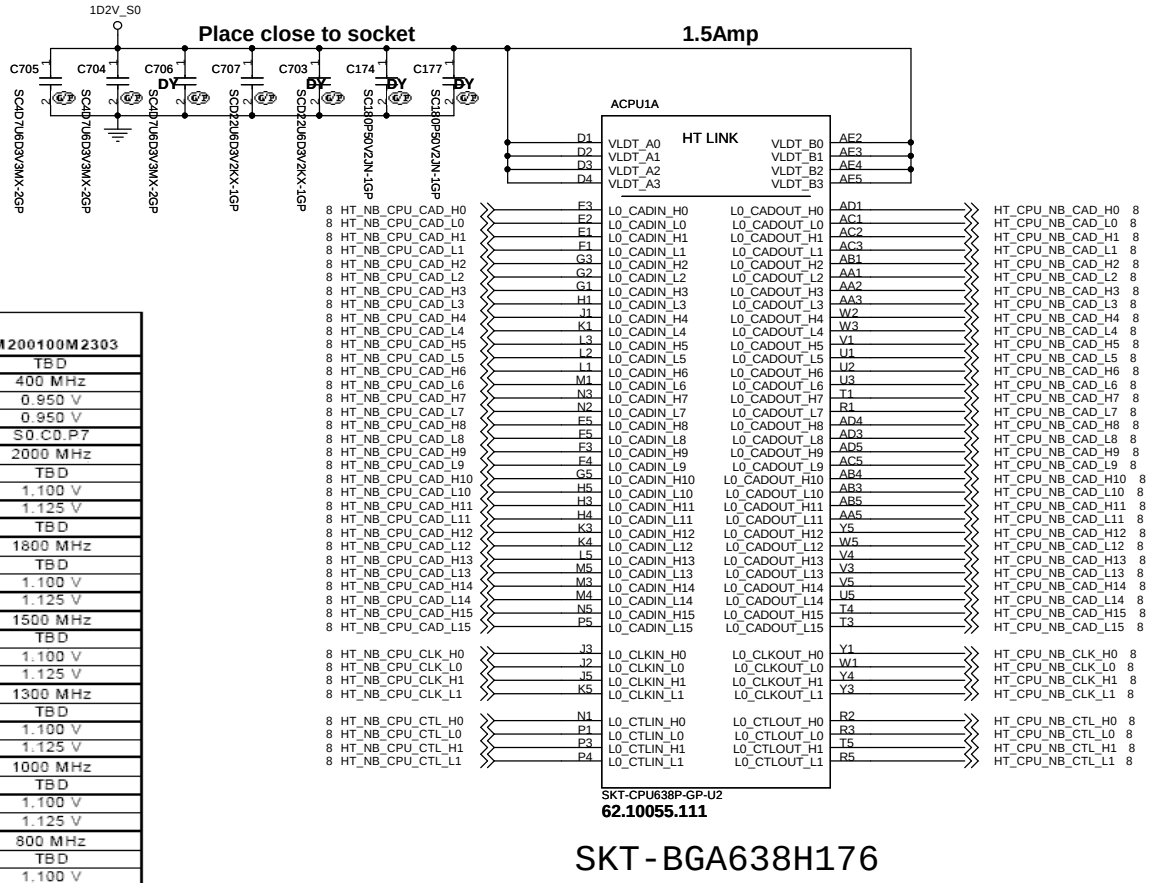

3D3V_S0
3D3V_CLK_VDD
R215 0R0603-PAD
C500 C501 C502 C467 C453 C476 C462 C492 C504
DY
SC1U10V2KX-4GP
SC10U6D3V3MX-GP
3D3V_S0
R221 2R3J-GP
3D3V_48MPWR_S0
C511 SC4D7U6D3V3KX-GP
C506 SC1U10V2KX-1GP
3000mA.80ohm
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
3D3V_S0
R197 0R0603-PAD
1D1V_CLK_VDDIO
C459 C460 C454 C461 C472 C464 C495
SC10U6D3V3MX-GP
SC1U10V2KX-4GP
3D3V_CLK_VDD
U20
1D1V_CLK_VDDIO
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDD
VDDHTT
VDDREF
VDD48
R218 DY 10MR2J-L-GP
XTAL-14D31818MHZ-5-GP
82.30005.B11
2ND = 82.30005.951
X5
C508 SC27P50V2JN-2-GP
C509 SC33P50V2JN-3GP
CL=20pF±0.2pF
X1 X2
GEN_XTAL_IN
GEN_XTAL_OUT
SMBCLK SMBDAT
CLK_SMBCLK R214 0R0402-PAD
CLK_SMBDAT R213 0R0402-PAD
SMBC0_SB 12,16,17
SMBD0_SB 12,16,17
ATIG0T_LPRS ATIG0C_LPRS ATIG1T_LPRS ATIG1C_LPRS
CLK_PCIE_PEG 52
CLK_PCIE_PEG# 52
CLK_NB_GFX 9
CLK_NB_GFX# 9
3D3V_CLK_VDD
R238 0R0603-PAD
C505 SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
CLKREQ0# CLKREQ1# CLKREQ2# CLKREQ3# CLKREQ4#
TP153 TPAD14-GP
LAN_CLKREQ# 26
TP159 TPAD14-GP
WLAN_CLKREQ# 33
TP157 TPAD14-GP
CLKREQ# Internal pull Low
PD#
SB A-Link
LAN
NB A-Link
MINI1
11 CLK_PCIE_SB
11 CLK_PCIE_SB#
26 CLK_PCIE_LAN
26 CLK_PCIE_LAN#
9 CLK_NB_GPPSB
9 CLK_NB_GPPSB#
33 CLK_PCIE_MINI1
33 CLK_PCIE_MINI1#
SRC0T_LPRS SRC0C_LPRS SRC1T_LPRS SRC1C_LPRS SRC2T_LPRS SRC2C_LPRS SRC3T_LPRS SRC3C_LPRS SRC4T_LPRS SRC4C_LPRS SRC6T/SATAT_LPRS SRC6C/SATAC_LPRS SRC7T_LPRS/27MHZ_SS SRC7C_LPRS/27MHZ_NS
CPUKG0T_LPRS CPUKG0C_LPRS
CPU_CLK 6
CPU_CLK# 6
48MHZ_0
CLK_48
RN65 SRN10J-7-GP
CLK48_USB 12
CLK48_5158E 32
REF0/SEL_HTT66
REF1/SEL_SATA
REF2/SEL_27
REF0 REF1 REF2
EC50 SC22P50V2JN-4GP
EC49 SC22P50V2JN-4GP
GNDSATA GNDATIG GND GNDHTT GNDREF GNDCPU GND48 GNDSRC GNDSRC GNDSB_SRC GND
2009/04/21 Pad to R By John
53 CLK_27M_SSIN
53 CLK_27M_M92
R209 0R2J-2-GP
R353 1KR2F-3-GP
CLK_SRC0T_LPRS
CLK_SRC0C_LPRS
SB_SRC0T_LPRS SB_SRC0C_LPRS SB_SRC1T_LPRS SB_SRC1C_LPRS
R352 1K2R2F-1-GP
NB HT
9 CLK_NBHT_CLK
9 CLK_NBHT_CLK#
HTT0T_LPRS/66M
HTT0C_LPRS/66M
ICS9LPRS480BKLFT-GP
71.09480.A03
2ND = 71.00880.A03
for TR
For SB710
R229 33R2F-3-GP
CLK_SB_14M 11
R234 DY 75R2F-2-GP
REF1
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
3D3V_S0
RN70 SRN10KJ-6-GP
PD#
WLAN_CLKREQ#
RUNPWROK_D
RUNPWROK_D 41
R231 R230 R228 R225 R224 R223
10KR2J-3-GP
REF0 REF1 REF2
SEL_27 REF2
1 27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
0* 100MHz differential spreading SRC clock
SEL_SATA REF1
1 100MHz non-spreading differential SATA clock
0* 100MHz differential spreading SRC clock
SEL_HTT66 REF0
1 66MHz 3.3V single ended HTT clock
0* 100MHz differential HTT clock
CPU_CLK(200MHz)
R232 150R2F-1-GP
R235 75R2F-2-GP
CLK_NB_14M 9
OSC_14M_NB
RS780M 1.1V 158R/90.9R
UMA
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CLKGEN ICS9LPRS480
Size A3
Document Number JV71-TR
Rev SB
Date: Monday, July 06, 2009
Sheet 3 of 61



SKT-BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

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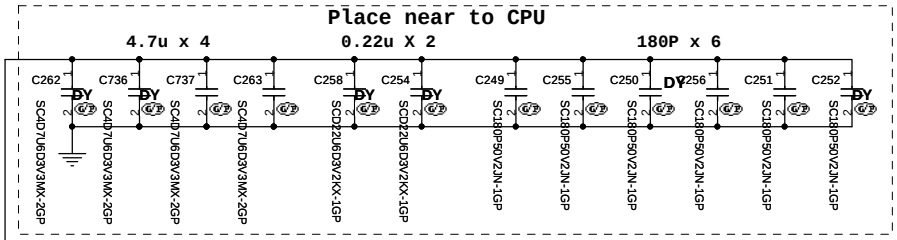
Title: **CPU_HT_LINK I/F (1/4)**

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 4 of 61



750 mA

CLOSE TO CPU

0D9V_S3

1D8V_S3

ACPU1B

MEM:CMD/CTRL/CLK

R381 39D2R2F-L-GP

R383 39D2R2F-L-GPTP111

C397 SCD1U10V2KX-4GP

VREF_DDR_CLAW

RN48 SRN1KJ-7-GP

C391 SC1KP50V2KX-1GP

C388 SCD1U10V2KX-4GP

TP106TPAD14-GP

TP112

SKT-CPU638P-GP-U2

62.10055.111

ACPU1C

MEM:DATA

SKT-CPU638P-GP-U2

62.10055.111

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Title: CPU_DDR_(2/4)

Size: A3 | Document Number: JV71-TR | Rev: SA

Date: Monday, July 06, 2009 | Sheet 5 of 61

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

1D8V_S0 RN40 SRN300J-1-GP DY C196 SC100P50V2JN-3GP

11,51 CPU_LDT_RST# R78 0R0402-PAD LDT_RST#_CPU 9
11,51 CPU_PWRGD R86 0R0402-PAD LDT_PWROK
11 CPU_LDT_STOP# R79 0R0402-PAD LDT_STP#_CPU 9
9 ALLOW_LDTSTOP R72 0R2J-2-GP CPU_LDT_REQ#_CPU

DY

for TR

1D8V_S3 R364 390R2J-1-GP CPU_SIC

1D8V_S3 DY R616 510R2J-1-GP CPU_TEST25_H
R617 510R2J-1-GP CPU_TEST25_L DY

for TR

1D8V_S3 R614 510R2J-1-GP CPU_TEST25_L
R615 510R2J-1-GP CPU_TEST25_H

2D5V_S0 R401 0R0603-PAD 2D5V_VDDA_S0

C739 SC10U6D3V3MX-GP DY C745 SC4D7U6D3V3MX-2GP DY C227 SC3900P50V2KX-2GP DY C752 SC10U10V5ZY-1GP DY C264 SCD22U16V3ZY-GP

Cloce To CPU

3 CPU_CLK R386 169R2F-GP CLKCPU_IN
3 CPU_CLK# C734 SC3900P50V2KX-2GP CLKCPU# _IN
C732 SC3900P50V2KX-2GP

LDT_RST# CPU
LDT_PWROK
LDT_STP# CPU
CPU_LDT_REQ# CPU

For HDT DBG
HDT_RST# R74 0R0402-PAD
TPAD14-GP TP186 CPU_SIC
TPAD14-GP TP185 CPU_SID
TPAD14-GP TP87 CPU_ALERT#

1D2V_S0 R84 44D2R2F-GP CPU_HTREF0
R83 44D2R2F-GP CPU_HTREF1

R110 0R0402-PAD CPU_VDD0_RUN_FB_H_R
R108 0R0402-PAD CPU_VDD0_RUN_FB_L_R
44 CPU_VDD0_RUN_FB_H
44 CPU_VDD0_RUN_FB_L

R104 0R0402-PAD CPU_VDD1_RUN_FB_H_R
R105 0R0402-PAD CPU_VDD1_RUN_FB_L_R
44 CPU_VDD1_RUN_FB_H
44 CPU_VDD1_RUN_FB_L

CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI

TP93 CPU_TEST23
CPU_TEST18
CPU_TEST19
TP105 CPU_TEST25_H
TP103 CPU_TEST25_L
TP104 CPU_TEST21
TP97 CPU_TEST20
TP94
CPU_TEST24
CPU_TEST22
TP95 CPU_TEST12
TP187 CPU_TEST27
R77 0R0402-PAD CPU_TEST9

RN42 SRN300J-1-GP

ACPU1D

F8 VDDA1		KEY1	M11
F9 VDDA2		KEY2	W18
A9 CLKIN_H		SVC	A6
A8 CLKIN_L		SVD	A4
B7 RESET_L			
A7 PWROK			
F10 LDTSTOP_L		THERMTRIP_L	AF6
C6 LDTREQ_L		PROCHOT_L	AC7
		MEMHOT_L	AA8
AF4 SIC			
AF5 SID			
AF6 ALERT_L		THERMDC	W7
		THERMDA	W8
R6 HT_REF0			
P6 HT_REF1			
R6 VDD0_FB_H		VDDIO_FB_H	W9
E6 VDD0_FB_L		VDDIO_FB_L	Y9
Y6 VDD1_FB_H		VDDNB_FB_H	H6
AB6 VDD1_FB_L		VDDNB_FB_L	G6
G10 DBRDY			
AA9 TMS		DBREQ_L	F10
AC9 TCK			
AD9 TRST_L		TDO	AE9
AF9 TDI			
AD7 TEST23		TEST28_H	J7
		TEST28_L	H8
H10 TEST18			
G9 TEST19		TEST17	D7
		TEST16	F7
E9 TEST25_H		TEST15	F7
E8 TEST25_L		TEST14	C7
AB8 TEST21		TEST7	C3
AE7 TEST20		TEST10	K8
AE7 TEST24			
AE8 TEST22		TEST8	C4
AC8 TEST12			
AF8 TEST27			
C2 TEST9		TEST29_H	C9
AA6 TEST6		TEST29_L	C8
A3 RSVD1		RSVD10	H18
A5 RSVD2		RSVD9	H19
B3 RSVD3		RSVD8	AA7
B5 RSVD4		RSVD7	D5
C1 RSVD5		RSVD6	C5

SKT-CPU638P-GP-U2

62.10055.111

1D8V_S3 RN87 SRN1KJ-7-GP
RN84 SRN300J-1-GP DY R366 300R2J-4-GP

CPU_SVC 44
CPU_SVD 44

CPU_DBREQ#
PROCHOT# R67 0R0402-PAD PROCHOT#_SB 11

internal pull high 300 ohm

H_THERMDC 34
H_THERMDA 34
DY C213 SC3300P50V2KX-1GP

TP99 CPU_VDDIO_SUS_FB_H
TP100 CPU_VDDIO_SUS_FB_L

CPU_VDDNB_RUN_FB_H 44
CPU_VDDNB_RUN_FB_L 44

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

TP92 CPU_TEST28_H
TP98 CPU_TEST28_L
TP89 CPU_TEST17
TP90 CPU_TEST16
TP91 CPU_TEST15
TP88 CPU_TEST14
CPU_TEST10
TP101 CPU_TEST29H
TP102 CPU_TEST29L

1D2V_S0 DY R610 300R2J-4-GP

1D8V_S3 3D3V_S0 R81 2K2R2J-2-GP DY
R101 10KR2J-3-GP DY
LDT_PWROK_G DY
Q8 MMBT3904-4-GP
44 CPU_PWRGD_SVID_REG LDT_PWROK
84.T3904.C11
2ND = 84.03904.L06
C205 SCD1U16V2ZY-2GP DY
Near CPU PIN

CPU_PWRGD_SVID_REG R375 LDT_PWROK
0R0402-PAD

LDT_PWROK
R376 2K2R2J-2-GP
C723 SCD1U16V2ZY-2GP
1D8V_SUS_Q2
Q24 MMBT3904-4-GP
THERMTRIP# RSMRST# 34,35
84.T3904.C11
2ND = 84.03904.L06

CPU exceeds to 125℃

CPU_TEST18 R612 300R2J-4-GP DY
CPU_TEST19 R611 300R2J-4-GP DY
CPU_TEST22 R613 300R2J-4-GP DY

HDT Connectors

HDT1 DY
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
1D8V_S3
HDT_RST#
SMC-CONN26A-FP

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **CPU_Control&Debug_(3/4)**

Size	Document Number	Rev
A3	JV71-TR	SA

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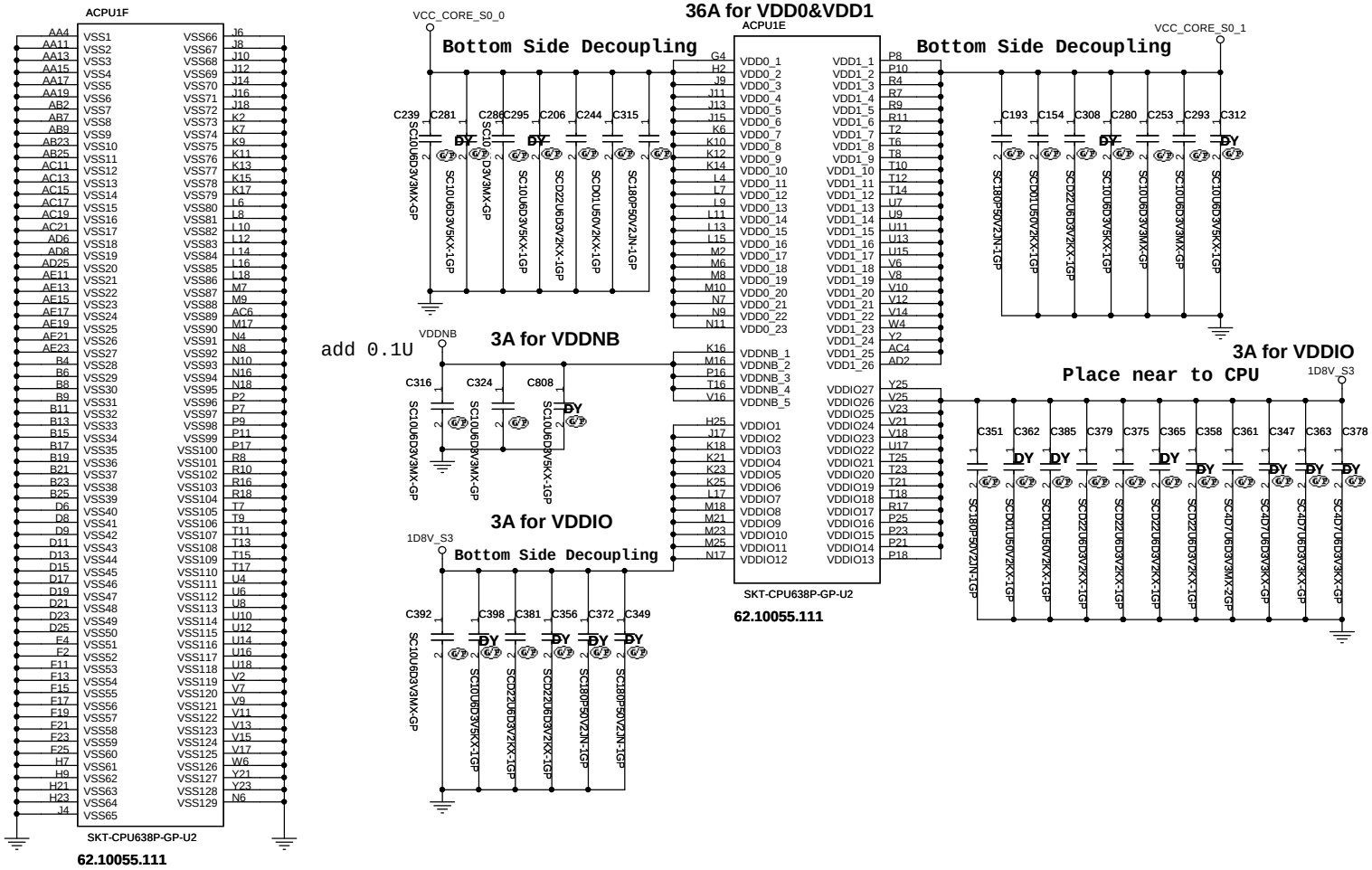

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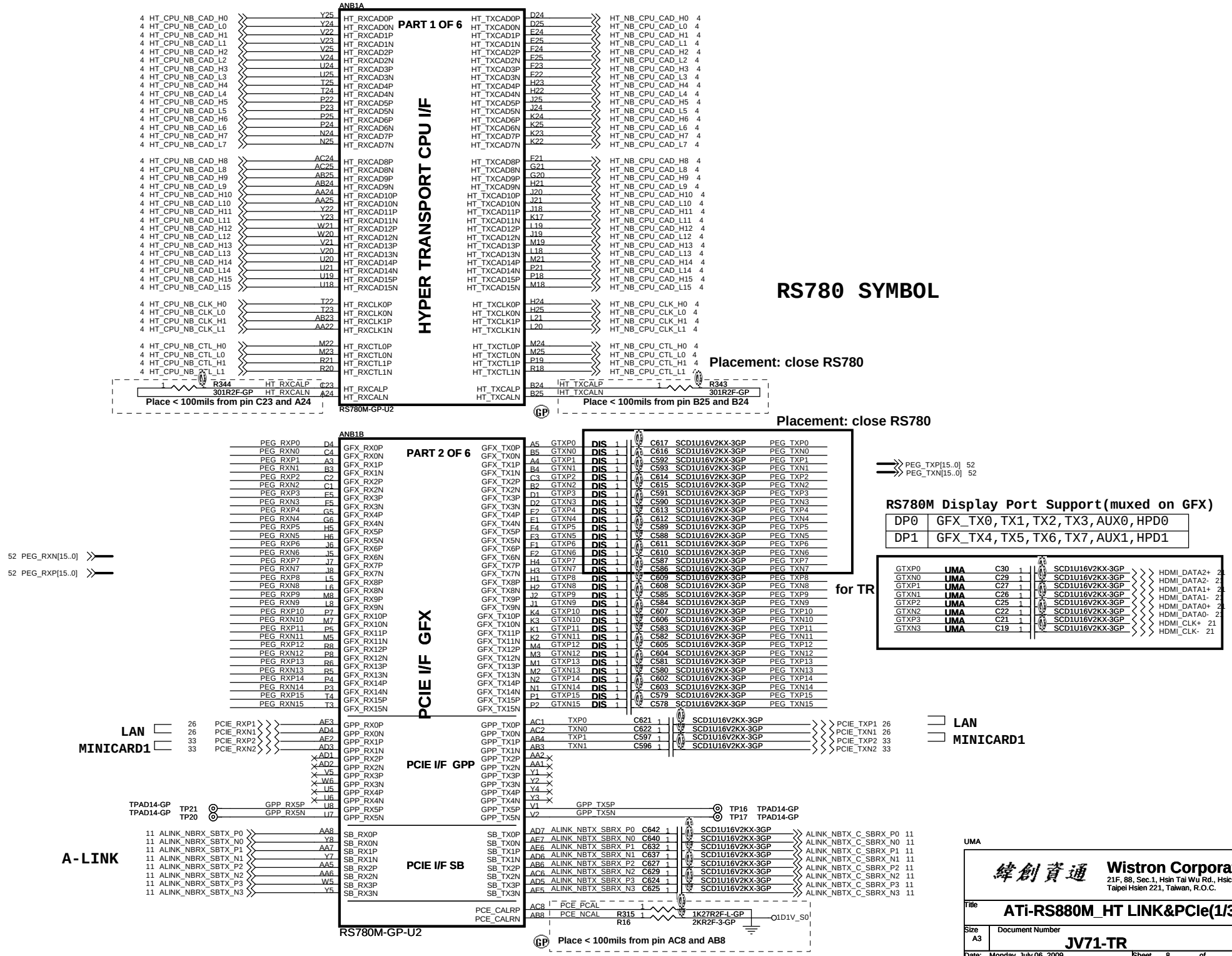
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_Power_(4/4)	
Size: A3	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 7 of 61	



UMA

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Title: **ATi-RS880M_HT LINK&PCIe(1/3)**

Size	Document Number	Rev
A3	JV71-TR	SA

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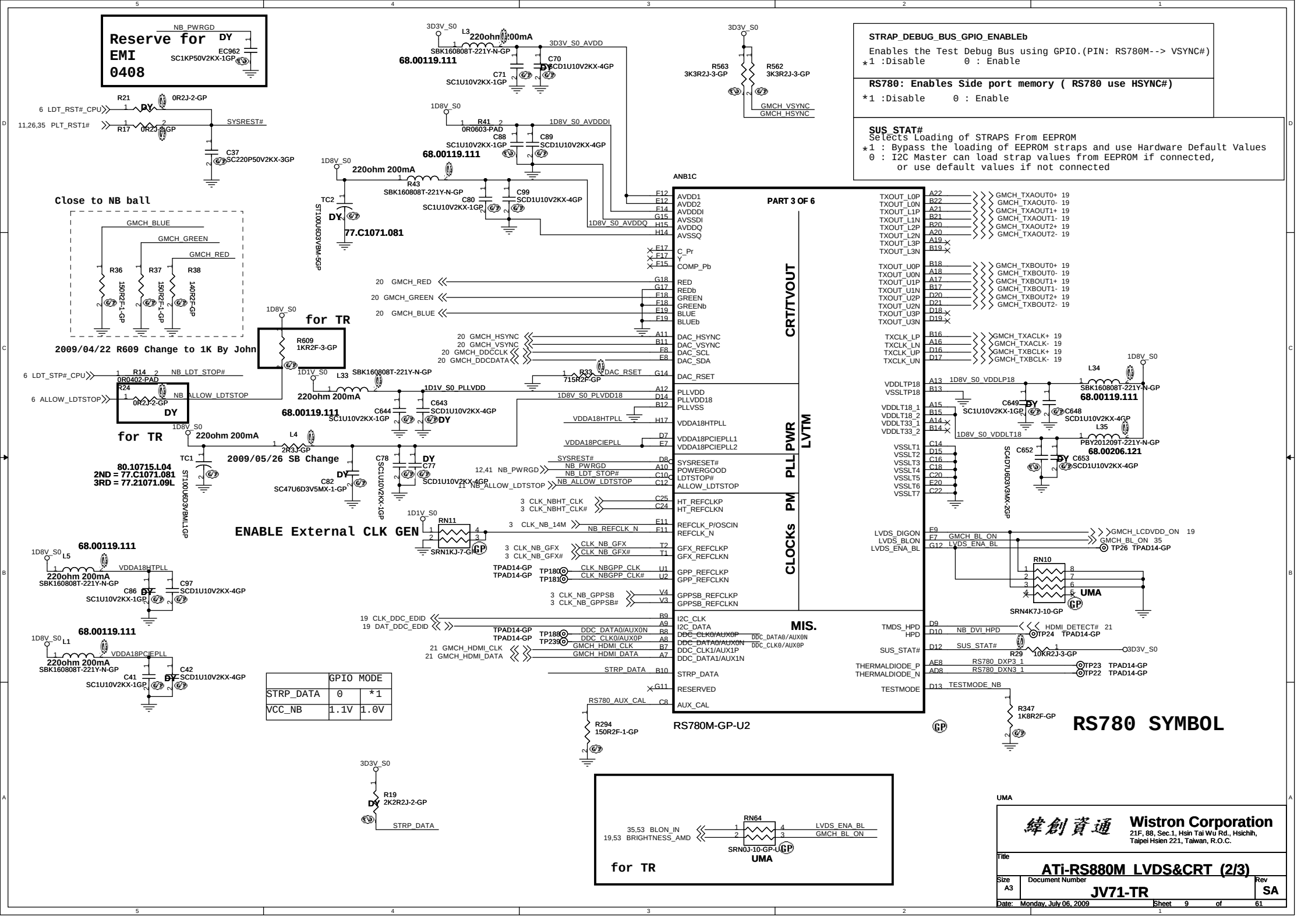
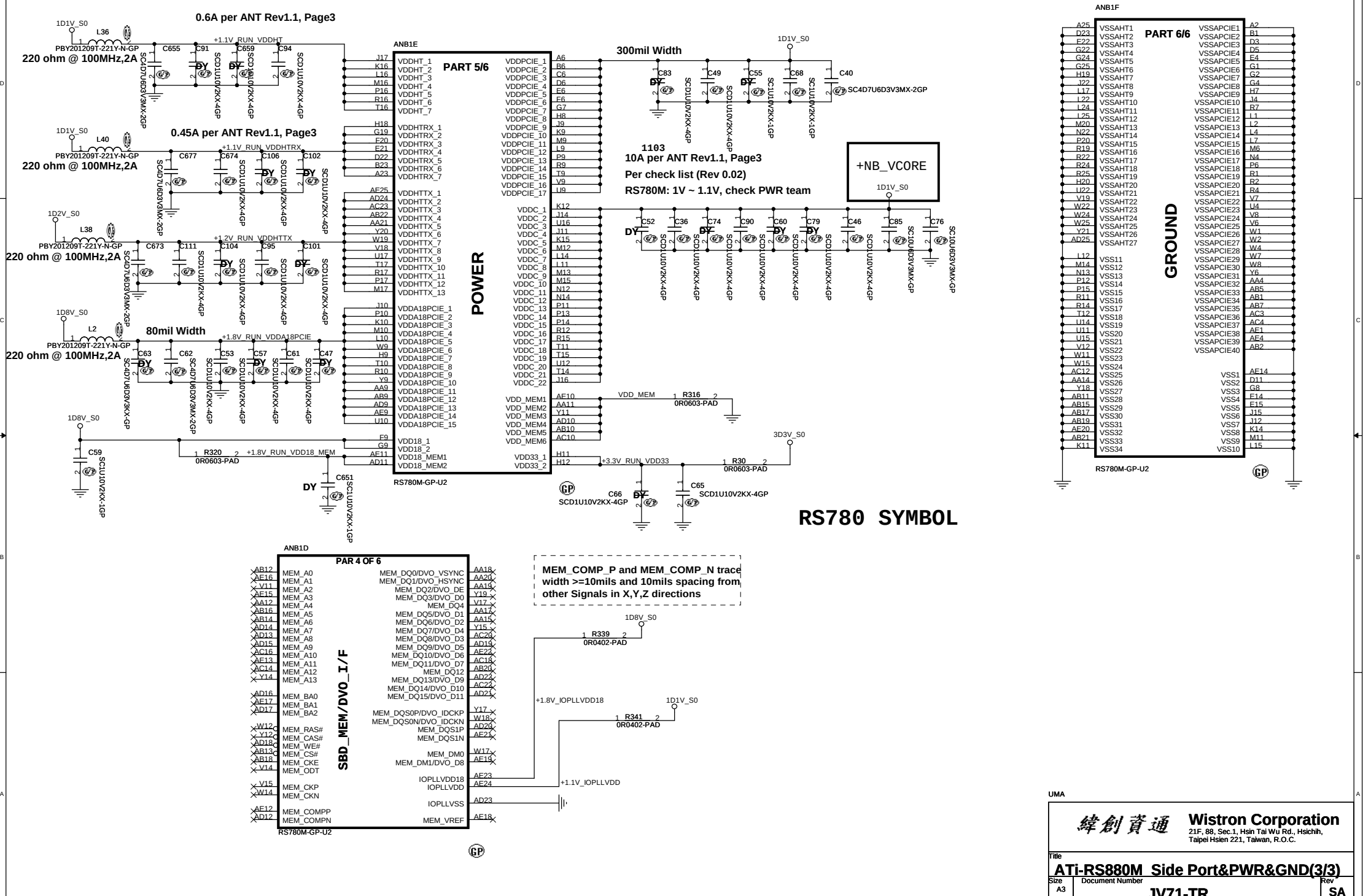


	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.1V	1.0V



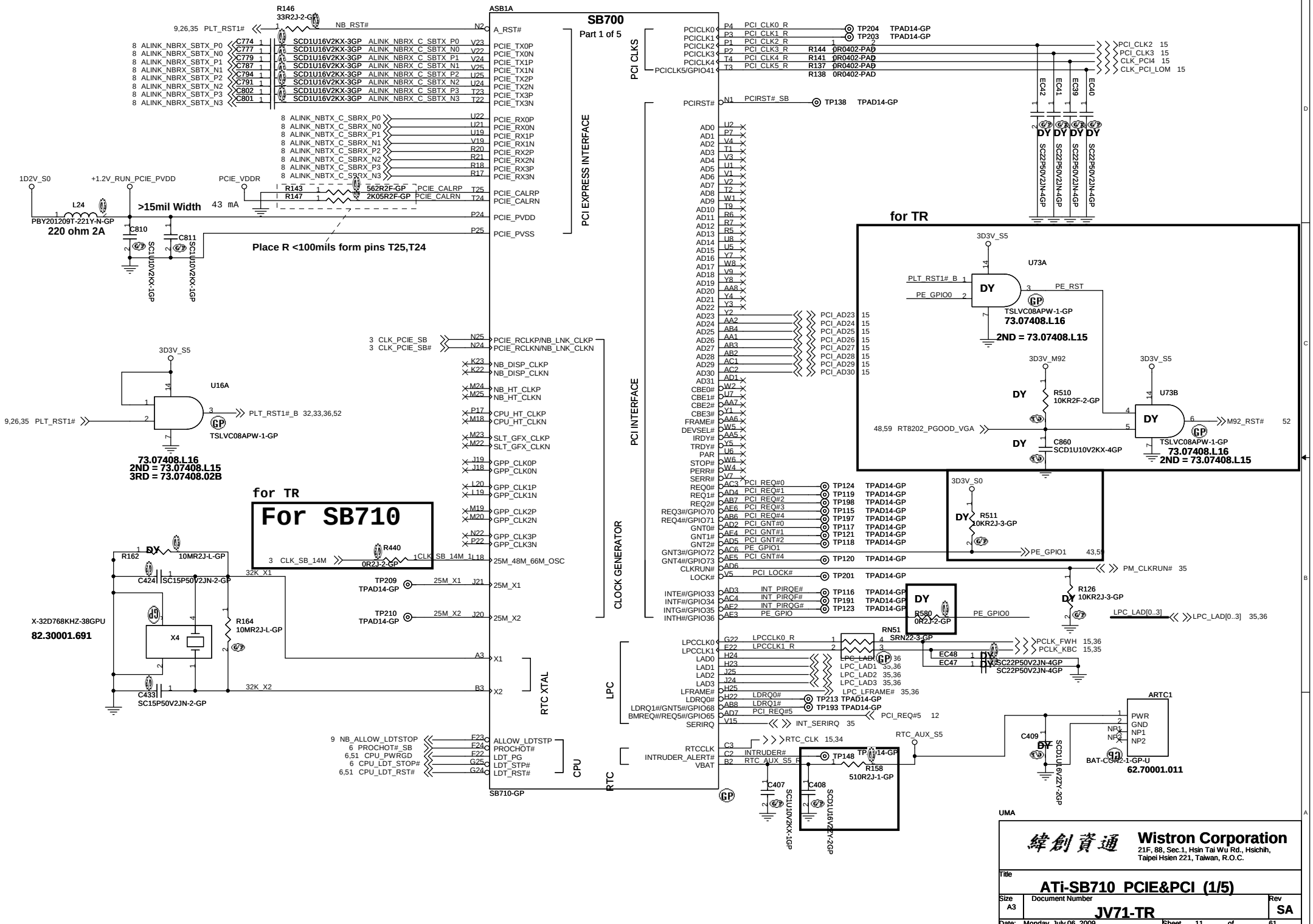
UMA

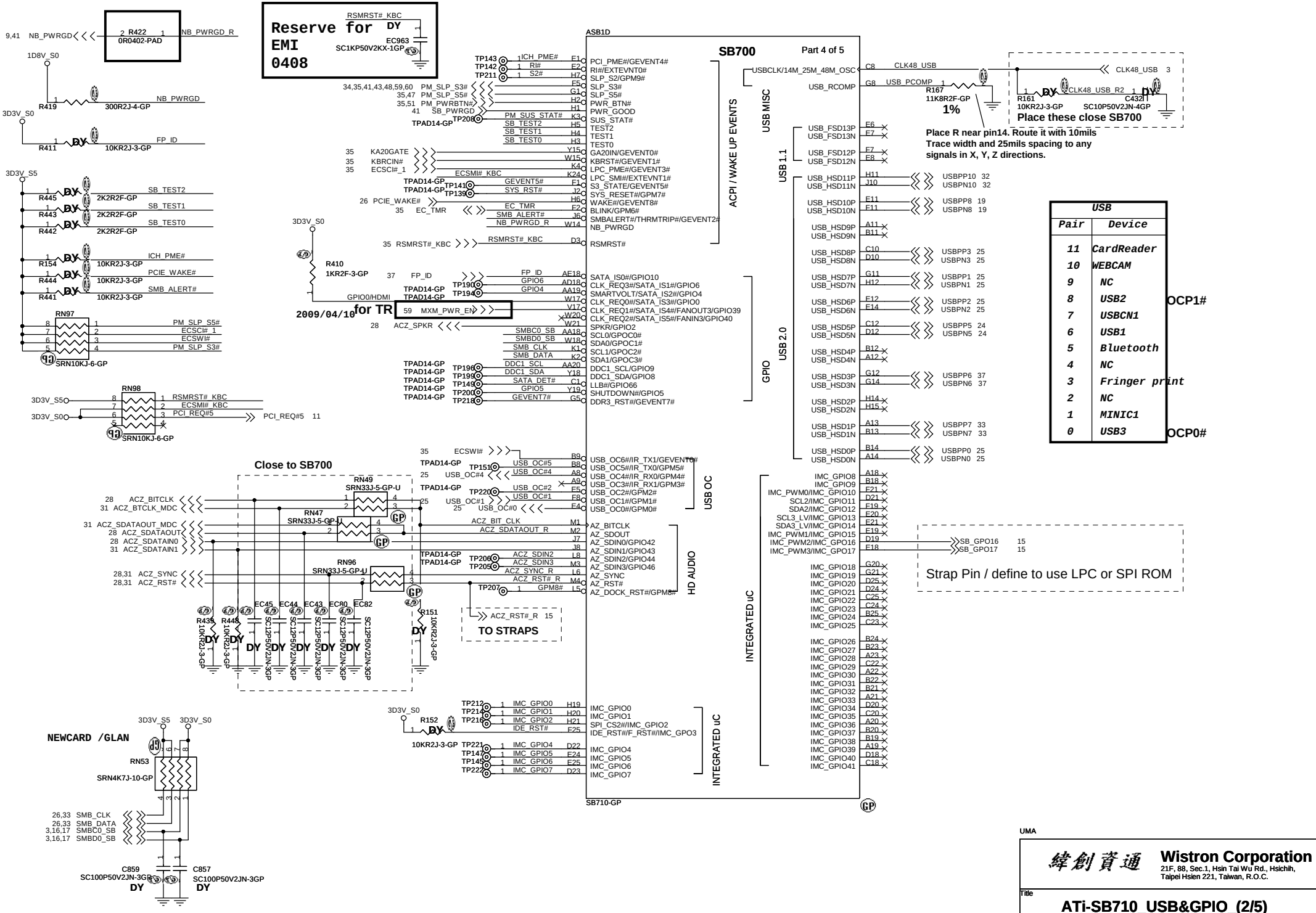
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATi-RS880M_Side Port&PWR&GND(3/3)**

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 10 of 61


SB700
Part 1 of 5
ASB1A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB710-GP
R146 33R2J-2-GP
NB_RST#
9,26,35 PLT_RST1#
A_RST#
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_CALRP
PCIE_CALRN
PCIE_PVDD
PCIE_PVSS
R143 562R2F-GP PCIE_CALRP
R147 2K05R2F-GP PCIE_CALRN
1D2V_S0
+1.2V_RUN_PCIE_PVDD
PCIE_VDDR
L24
PBY201209T-221Y-N-GP
220 ohm 2A
>15mil Width
43 mA
C810
C811
SCD1U10V2KX-1GP
Place R <100mils form pins T25,T24
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCI_CLK0_R
PCI_CLK1_R
PCI_CLK2_R
PCI_CLK3_R
PCI_CLK4_R
PCI_CLK5_R
TP204 TPAD14-GP
TP203 TPAD14-GP
R144 0R0402-PAD
R141 0R0402-PAD
R137 0R0402-PAD
R138 0R0402-PAD
PCI_CLK2 15
PCI_CLK3 15
CLK_PCI4 15
CLK_PCI_LOM 15
EC42
EC41
EC39
EC40
SC22P50V2JN-4GP
PCIRST#
PCIRST# SB
TP138 TPAD14-GP
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
PCI_AD23 15
PCI_AD24 15
PCI_AD25 15
PCI_AD26 15
PCI_AD27 15
PCI_AD28 15
PCI_AD29 15
PCI_AD30 15
CBE0#
CBE1#
CBE2#
CBE3#
FRAME#
DEVSEL#
IRDY#
TRDY#
PAR
STOP#
PERR#
SERR#
REQ0#
REQ1#
REQ2#
REQ3#/GPIO70
REQ4#/GPIO71
GNT0#
GNT1#
GNT2#
GNT3#/GPIO72
GNT4#/GPIO73
CLKRUN#
LOCK#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_REQ#4
PCI_GNT#0
PCI_GNT#1
PCI_GNT#2
PE_GPIO1
PCI_GNT#4
PCI_LOCK#
TP124 TPAD14-GP
TP119 TPAD14-GP
TP198 TPAD14-GP
TP115 TPAD14-GP
TP197 TPAD14-GP
TP117 TPAD14-GP
TP121 TPAD14-GP
TP118 TPAD14-GP
TP120 TPAD14-GP
TP201 TPAD14-GP
INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
PE_GPIO
TP116 TPAD14-GP
TP191 TPAD14-GP
TP123 TPAD14-GP
R580 0R2J-2-GP
PE_GPIO0
PM_CLKRUN# 35
R126 10KR2J-3-GP
LPC_LAD[0..3]
LPC_LAD[0..3] 35,36
RN51 SRN22-3-GP
PCLK_FWH 15,36
PCLK_KBC 15,35
LPCCLK0
LPCCLK1
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#/GNT5#/GPIO68
BMREQ#/REQ5#/GPIO65
SERIRQ
LPCCLK0_R
LPCCLK1_R
LPC_LAD0 35,36
LPC_LAD1 35,36
LPC_LAD2 35,36
LPC_LAD3 35,36
LPC_LFRAME# 35,36
LDRQ0#
LDRQ1#
PCI_REQ#5
INT_SERIRQ 35
TP213 TPAD14-GP
TP193 TPAD14-GP
PCI_REQ#5 12
SRN22-3-GP
SC22P50V2JN-4GP
RTCCLK
INTRUDER_ALERT#
VBAT
RTC_CLK 15,34
RTC_AUX_S5
INTRUDER#
RTC_AUX_S5_R
TP148 TPAD14-GP
R158 510R2J-1-GP
C407 SC1U10V2KX-1GP
C408 SCD1U16V2ZY-2GP
ARTC1
PWR
GND
NP1
NP2
C409 SCD1U16V2ZY-2GP
BAT-CON2-1-GP-U
62.70001.011
ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
9 NB_ALLOW_LDTSTOP
6 PROCHOT#_SB
6,51 CPU_PWRGD
6 CPU_LDT_STOP#
6,51 CPU_LDT_RST#
CLK_PCIE_SB
CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
25M_48M_66M_OSC
25M_X1
25M_X2
X1
X2
TP209 TPAD14-GP
TP210 TPAD14-GP
CLK_SB_14M
CLK_SB_14M_1
R440 0R2J-2-GP
32K_X1
32K_X2
R162 DY 10MR2J-L-GP
C424 SC15P50V2JN-2-GP
C433 SC15P50V2JN-2-GP
R164 10MR2J-L-GP
X-32D768KHZ-38GPU
82.30001.691
X4
for SB710
for TR
U16A
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
3D3V_S5
PLT_RST1#_B 32,33,36,52
U73A
PLT_RST1#_B
PE_GPIO0
PE_RST
73.07408.L16
2ND = 73.07408.L15
3D3V_M92
U73B
R510 10KR2F-2-GP
RT8202_PGOOD_VGA 48,59
M92_RST# 52
C860 SCD1U10V2KX-4GP
3D3V_S0
R511 10KR2J-3-GP
PE_GPIO1 43,5
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 PCIE&PCI (1/5)
Size A3
Document Number JV71-TR
Rev SA
Date: Monday, July 06, 2009
Sheet 11 of 61


Reserve for EMI 0408
SB700
Part 4 of 5
ASB1D
SB710-GP
for TR
2009/04/10
Close to SB700
NEWCARD /GLAN
TO STRAPS
Place these close SB700
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
Strap Pin / define to use LPC or SPI ROM
USB
Pair Device
11 CardReader
10 WEBCAM
9 NC
8 USB2
7 USBCN1
6 USB1
5 Bluetooth
4 NC
3 Fringer print
2 NC
1 MINIC1
0 USB3
OCP1#
OCP0#
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 USB&GPIO (2/5)
Size A3
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Rev SA
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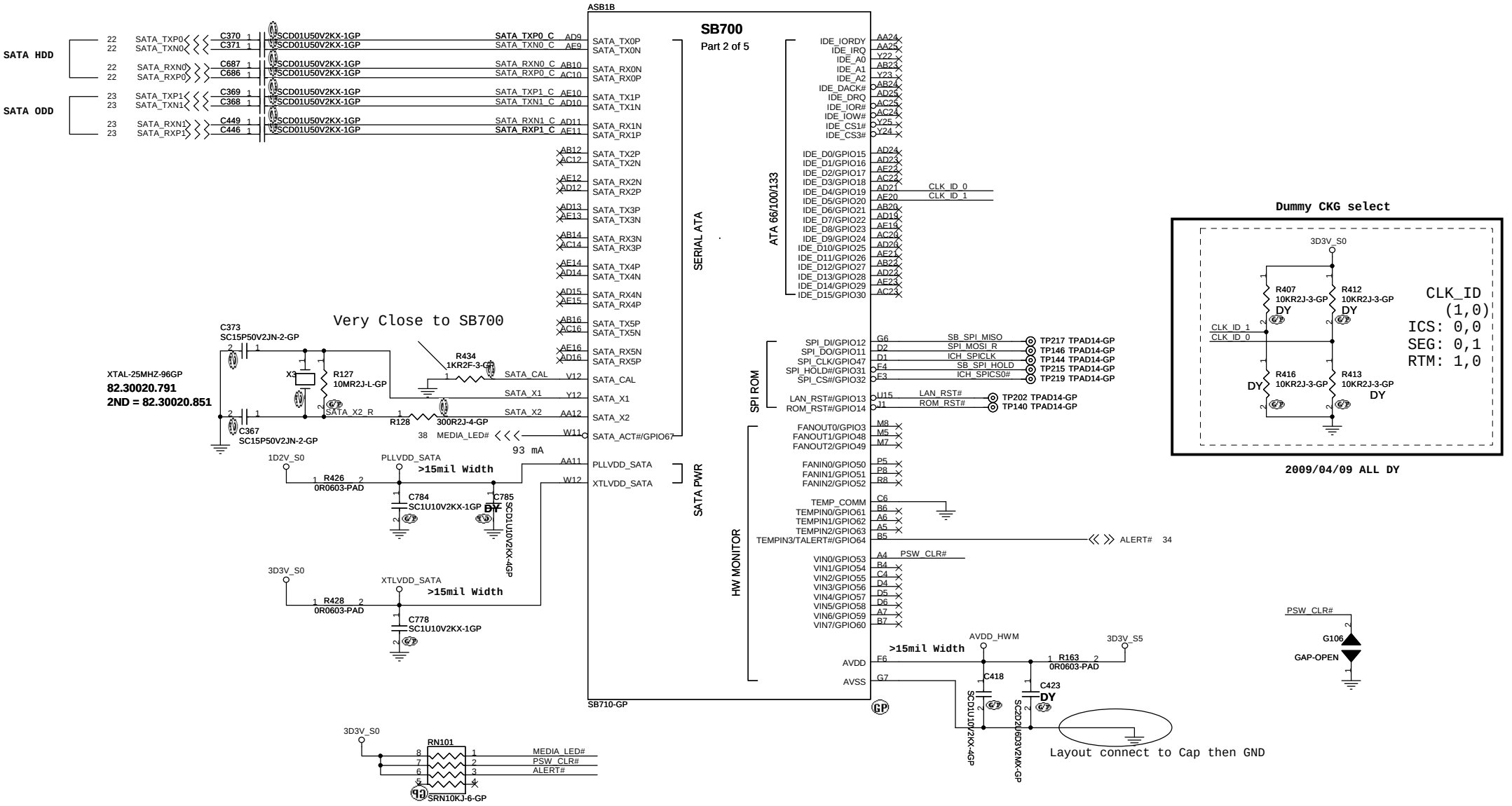
PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATi-SB710 SATA-IDE (3/5)**

Size	Document Number	Rev
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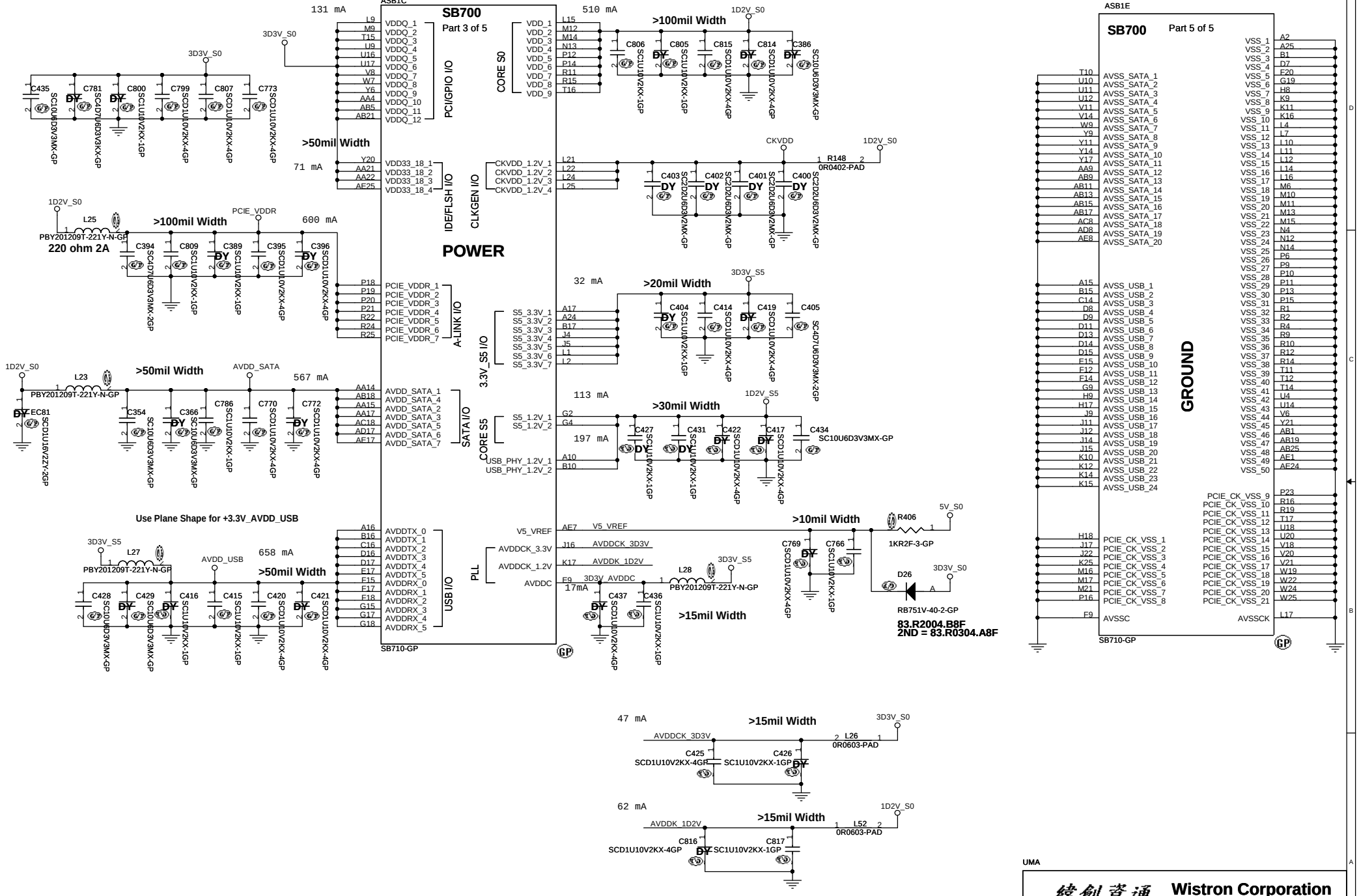
Date: Monday, July 06, 2009 Sheet 13 of 61



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ATi-SB710 POWER&GND (4/5)**
Size: A3	Document Number: JV71-TR
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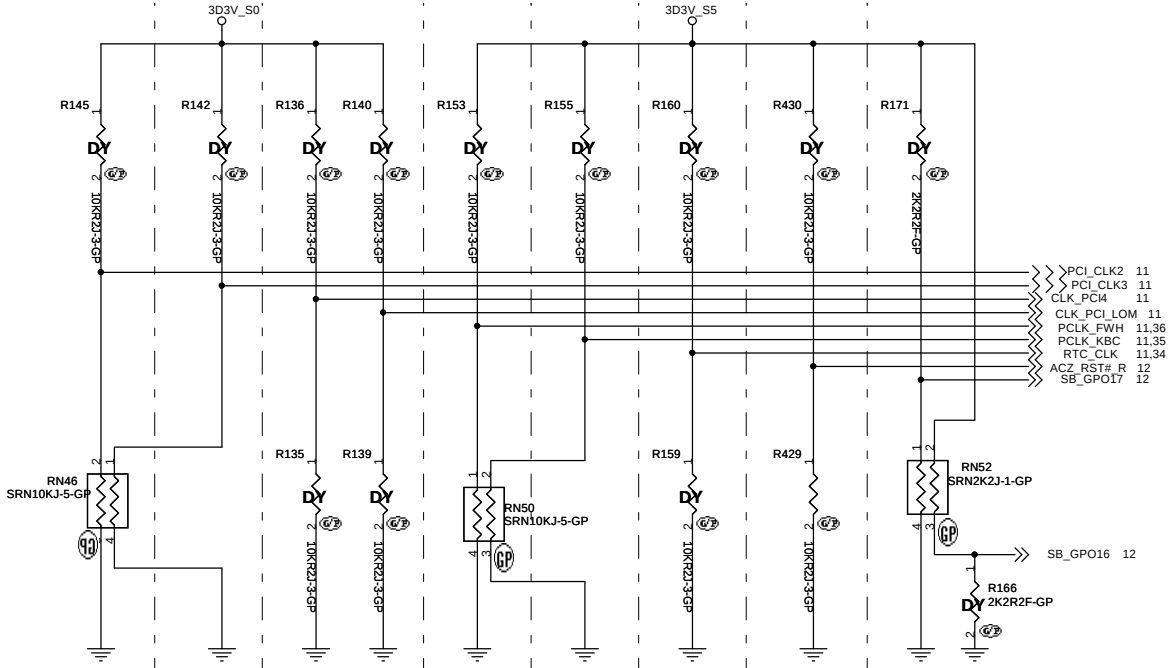
Date: Monday, July 06, 2009	Sheet 14 of 61

REQUIRED STRAPS

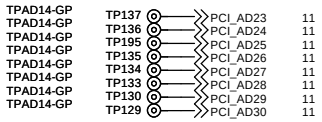
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
								ROM TYPE:
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	H, H = Reserved H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM DEFAULT L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

UMA

緯創資通 **Wistron Corporation**
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Title: **ATi-SB710 STRAPPING (5/5)**

Size	Document Number	Rev
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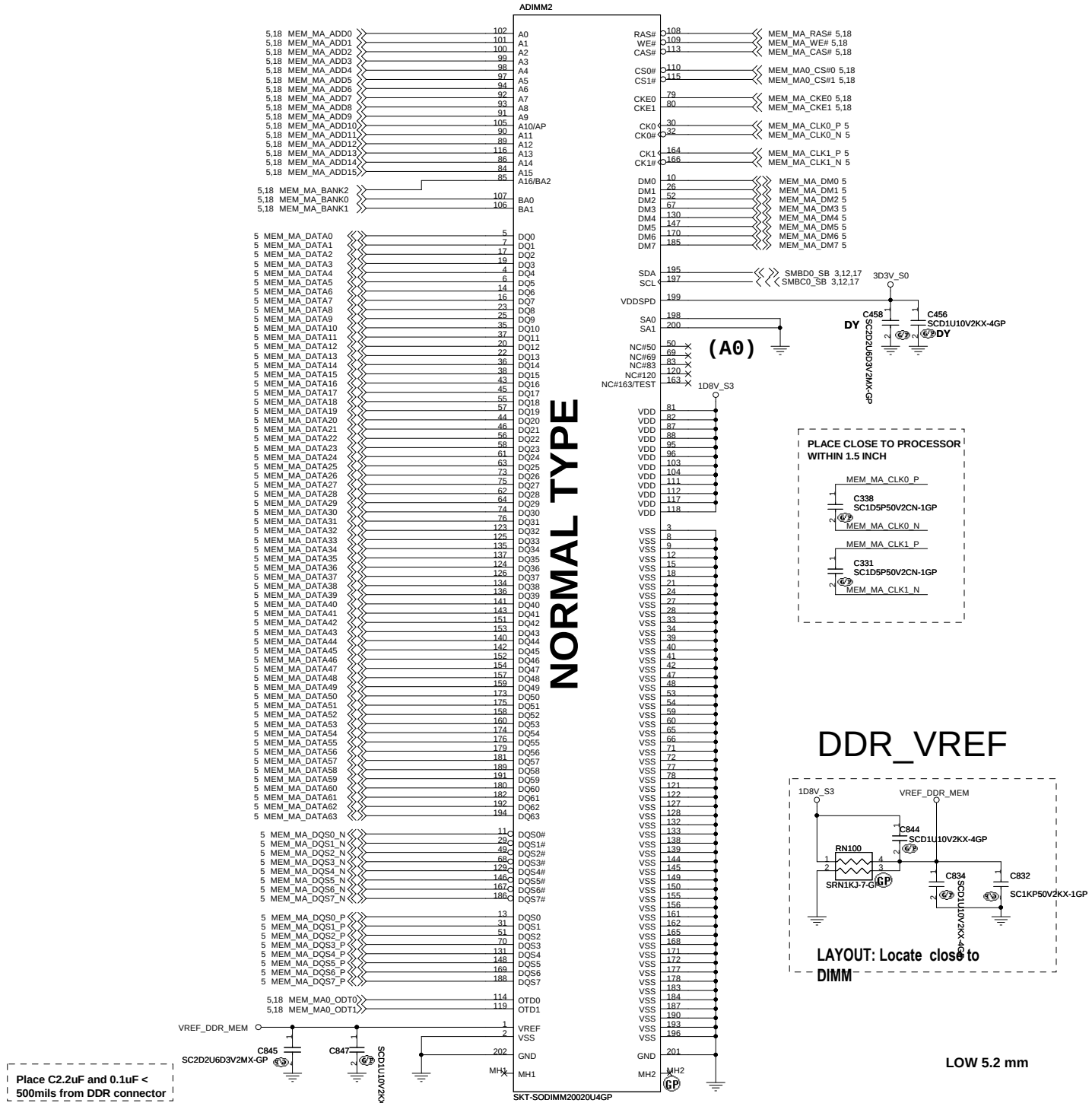
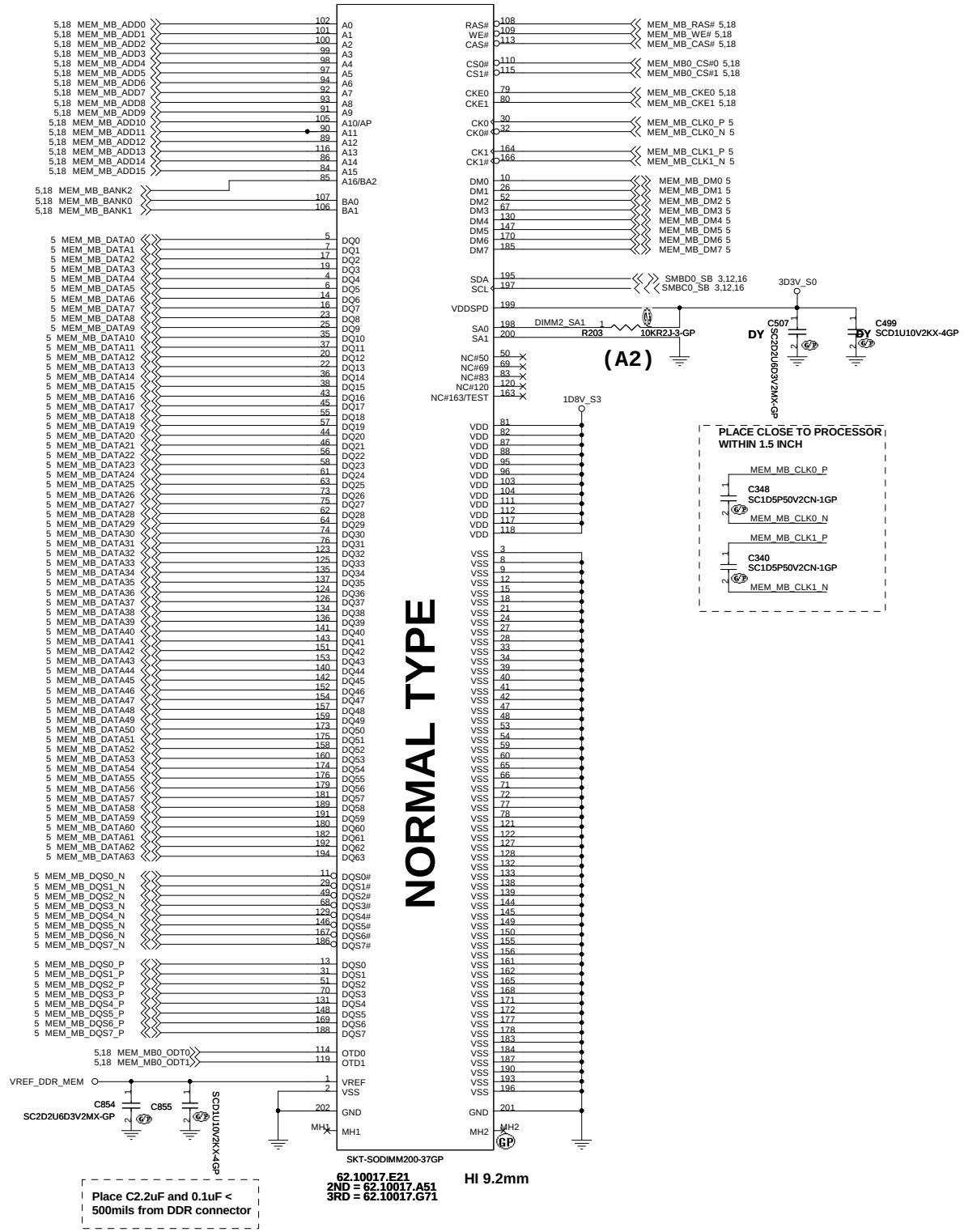


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**DDR_SO-DIMM SKT_1**
Size: Custom	Document Number: **JV71-TR**
Rev	**SB**
Date: Monday, July 06, 2009	Sheet 16 of 61

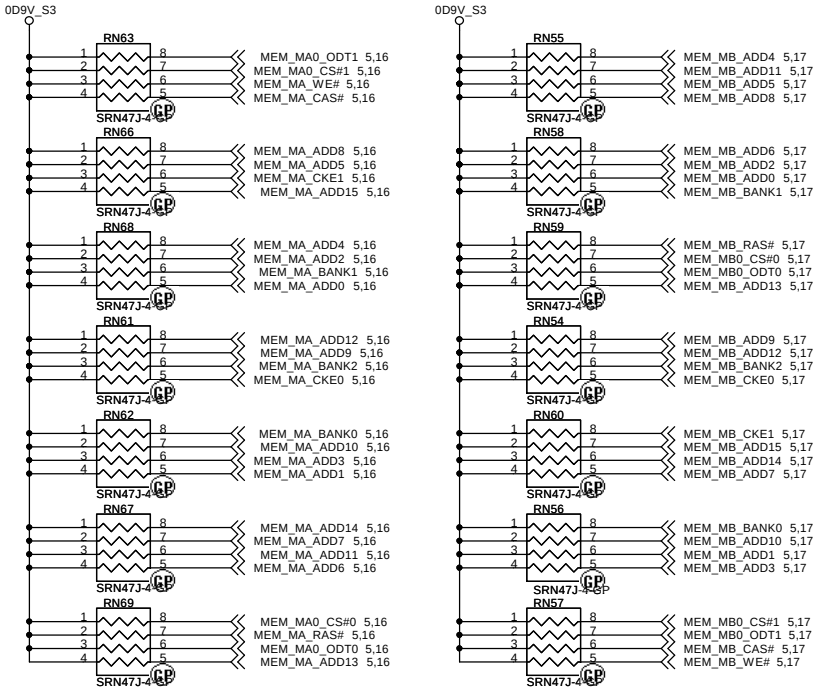


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**DDR_SO-DIMM SKT_2**	
Size: Custom	Document Number: **JV71-TR**	Rev: **SB**
Date: Monday, July 06, 2009	Sheet 17 of 61	

PARALLEL TERMINATION

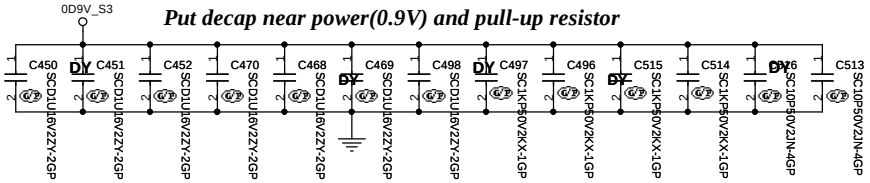
Put decap near power(0.9V) and pull-up resistor



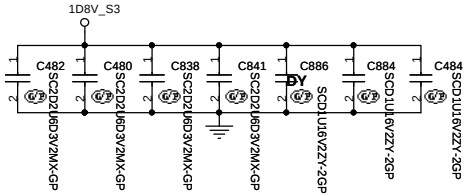
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

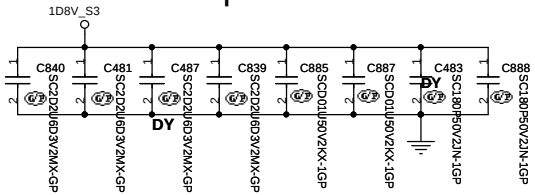


Place these Caps near DM1



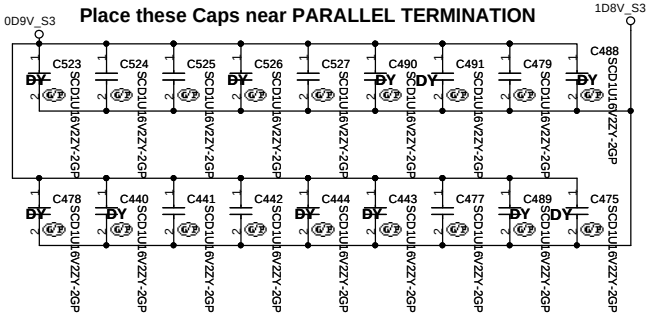
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR_DAMPING & TERMINATION**

Size	Document Number	Rev
A3	JV71-TR	SB

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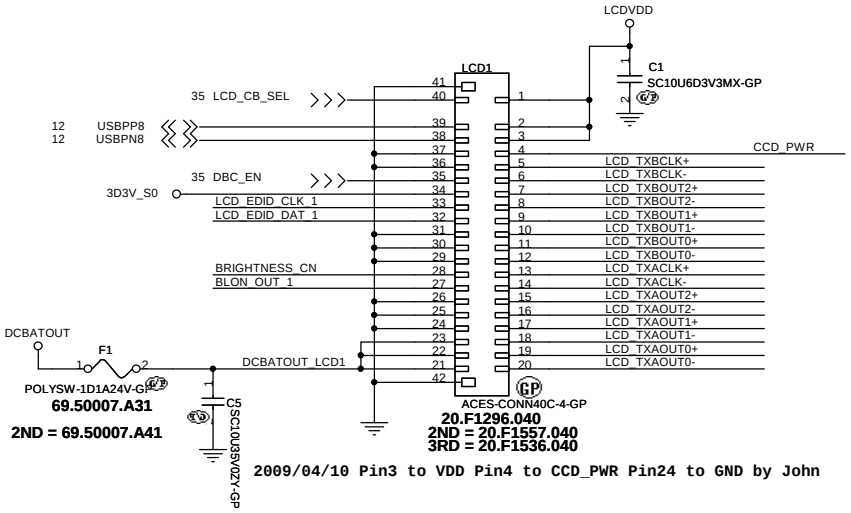
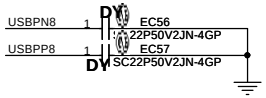
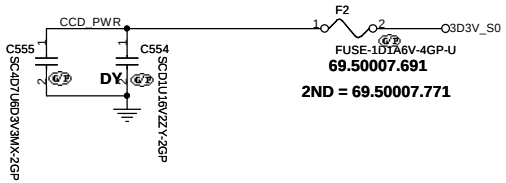
LCD/INVERTER/CCD CONN

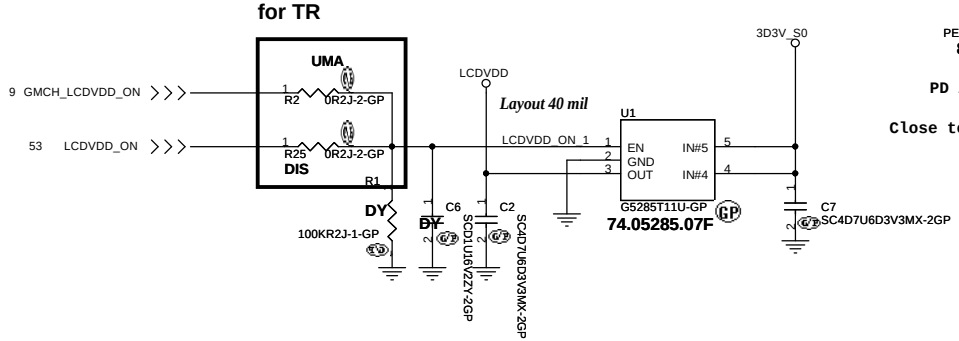


2009/04/10 Pin3 to VDD Pin4 to CCD_PWR Pin24 to GND by John

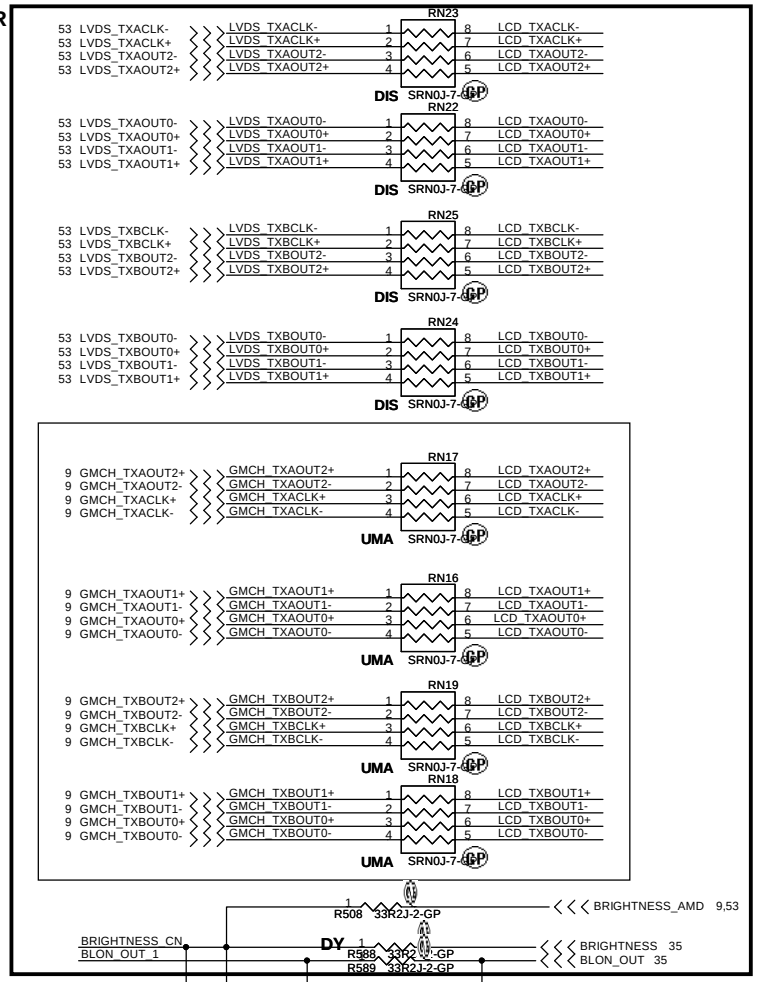




for TR

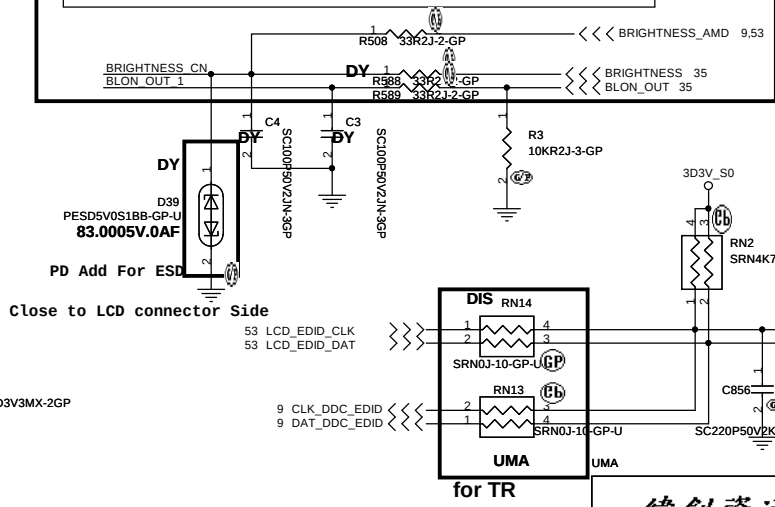


for TR



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



緯創資通 Wistron Corporation
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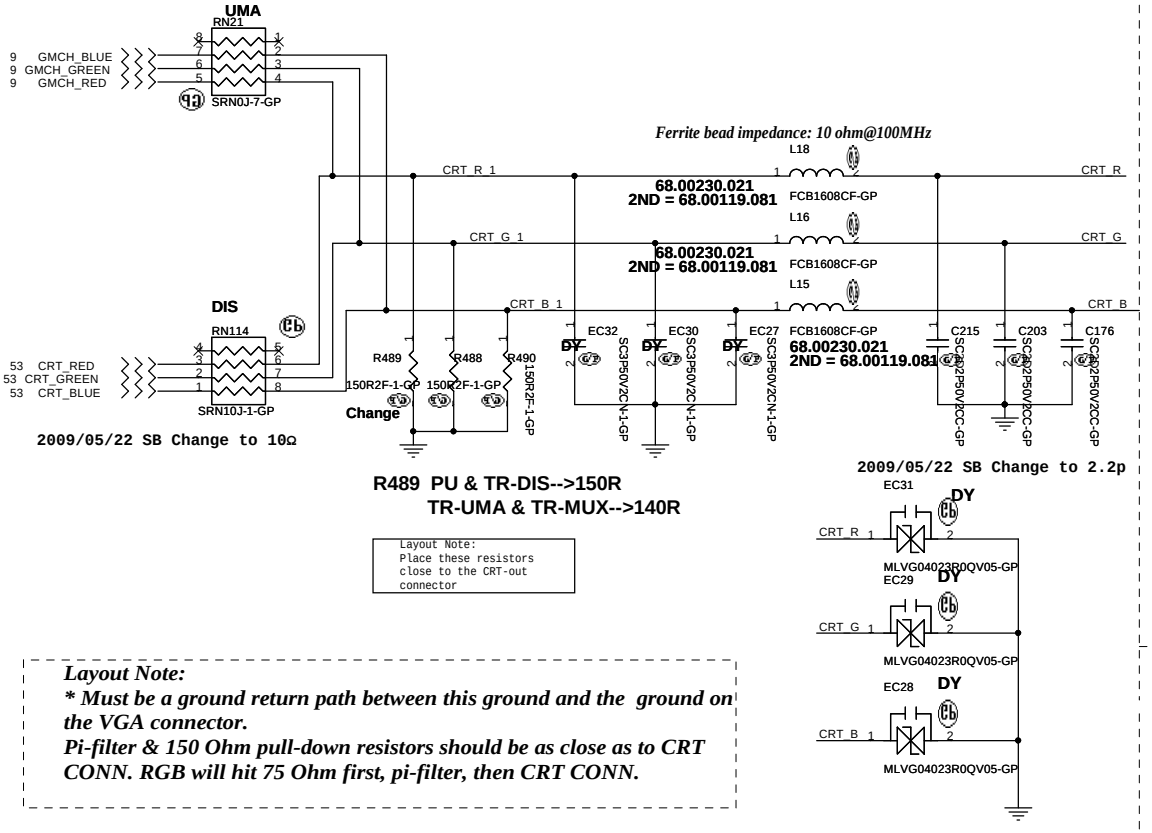
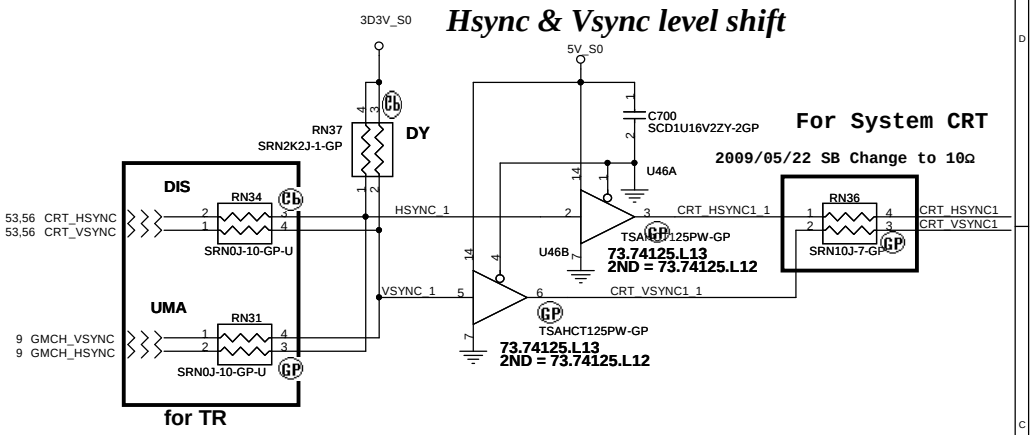
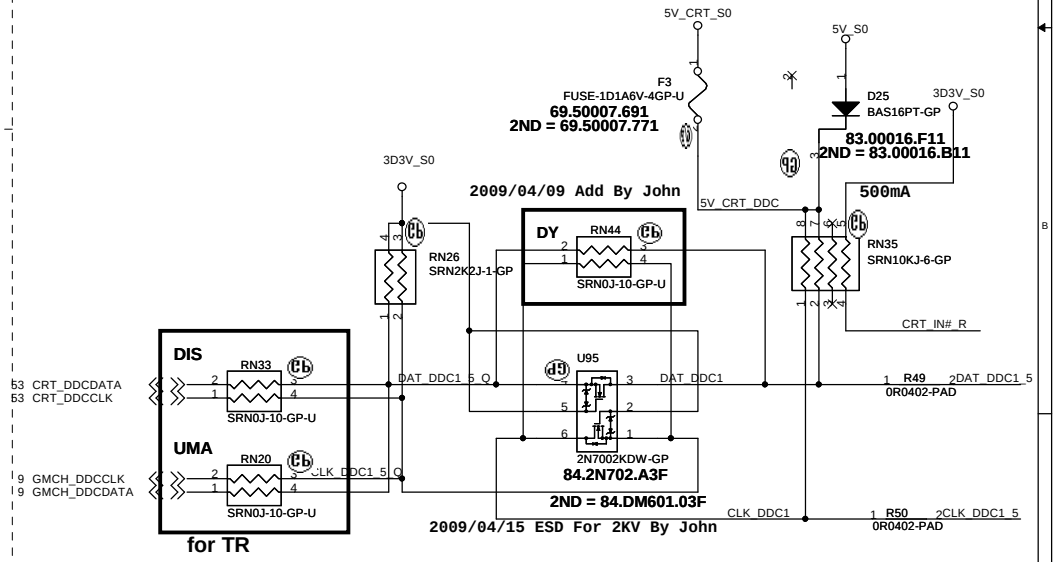
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LCD CONN		
Size: A3	Document Number: JV71-TR	Rev: -1
Date: Monday, July 06, 2009	Sheet 19 of 61	

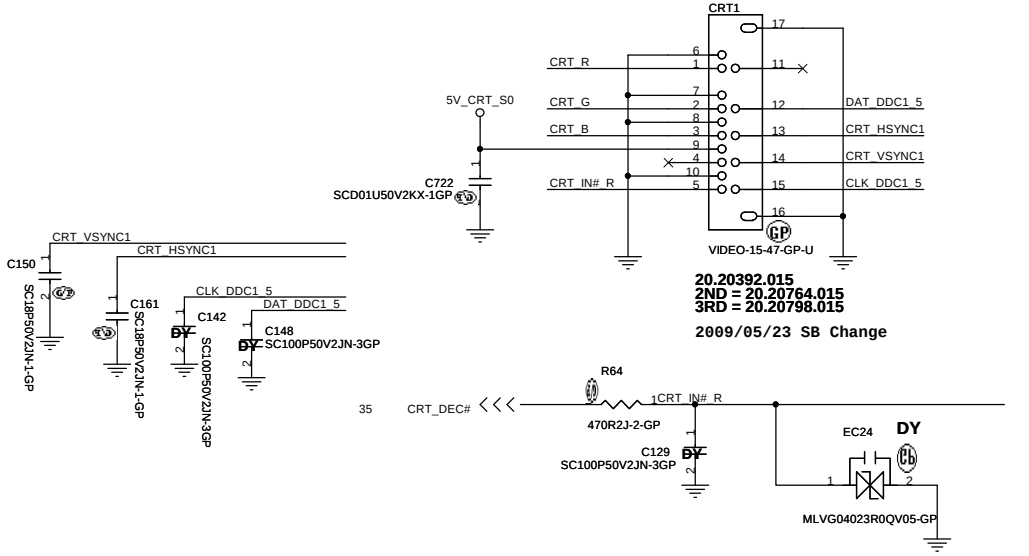


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





CRT I/F & CONNECTOR



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size | Document Number: **JV71-TR** | Rev: **SB**

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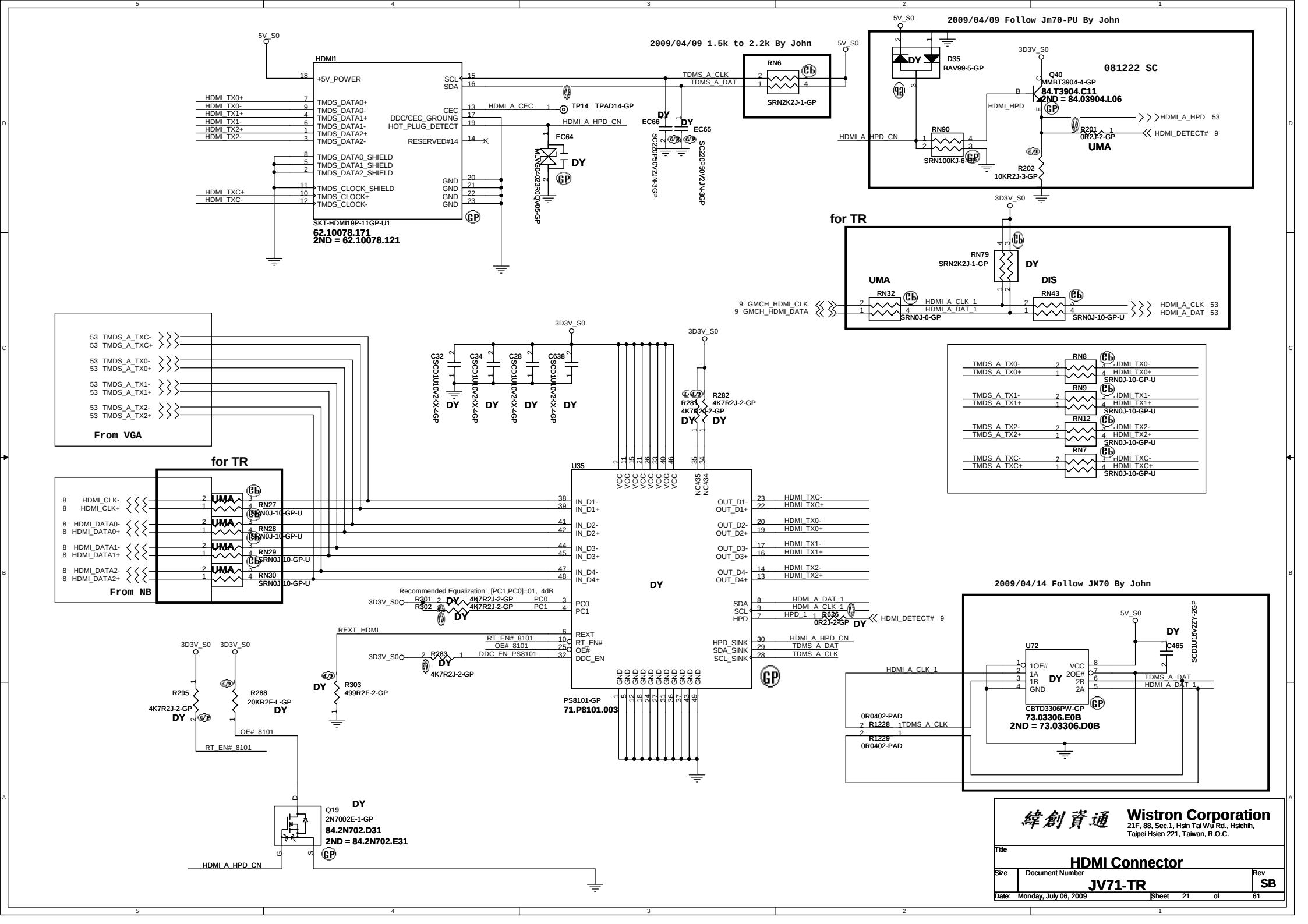
2009/04/09 1.5k to 2.2k By John
2009/04/09 Follow Jm70-PU By John
081222 SC
HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
2ND = 62.10078.121
RN6
SRN2K2J-1-GP
D35
BAV99-5-GP
Q40
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.L06
RN90
SRN100KJ-6-GP
R201
0R2J-2-GP
R202
10KR2J-3-GP
UMA
for TR
RN79
SRN2K2J-1-GP
DIS
RN32
RN43
SRN0J-6-GP
SRN0J-10-GP-U
From VGA
From NB
RN8
RN9
RN12
RN7
U35
PS8101-GP
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
2009/04/14 Follow JM70 By John
U72
CBTD3306PW-GP
73.03306.E0B
2ND = 73.03306.D0B
Q19
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
HDMI Connector
JV71-TR
Rev SB
Date: Monday, July 06, 2009
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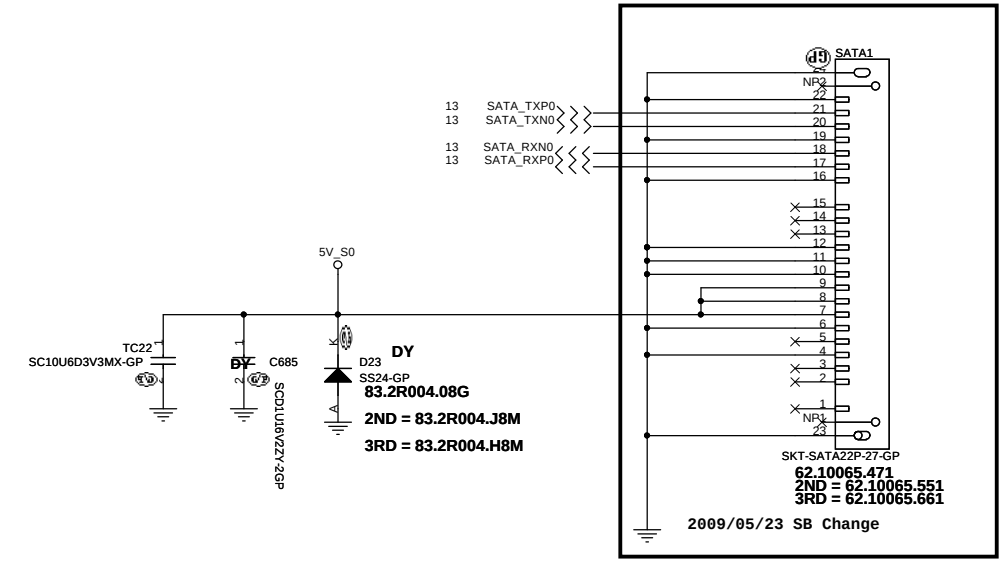
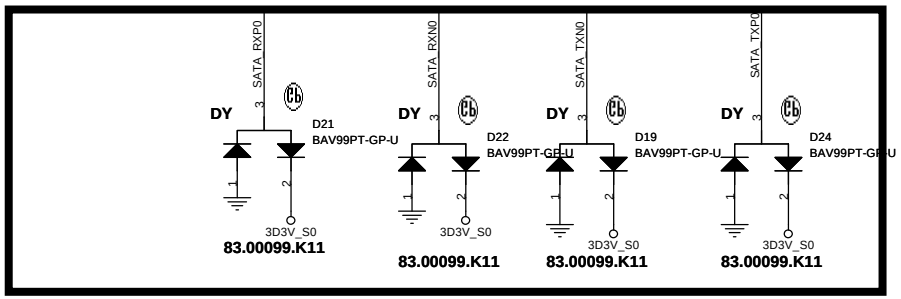
SATA Connector





UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD		
Size	Document Number: JV71-TR	Rev: SB
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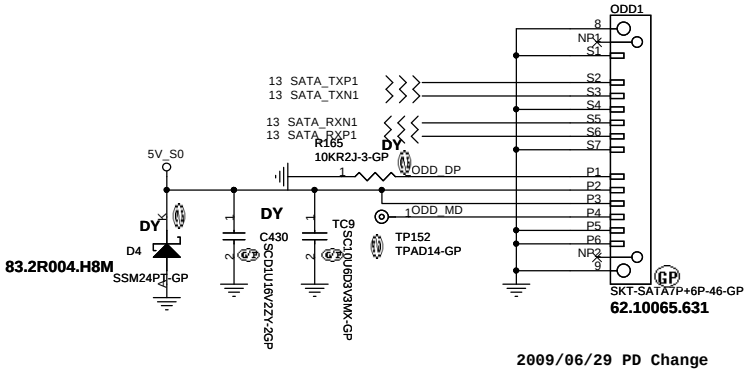
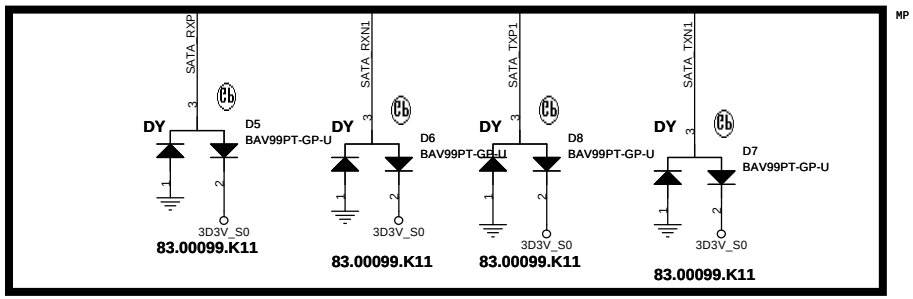
SATA ODD Connector



2009/06/29 PD Change



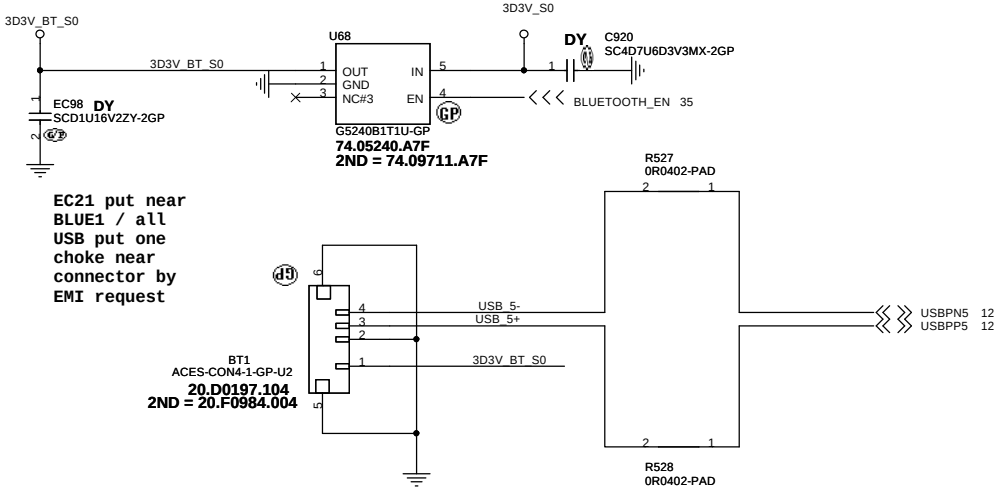
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ODD**		
Size	Document Number: **JV71-TR**	Rev: **SB**
Date: Monday, July 06, 2009	Sheet 23 of 61	

BLUETOOTH MODULE

1.5A / High Active Voltage 2V



UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
BLUETOOTH		
Size	Document Number **JV71-TR**	Rev **SA**
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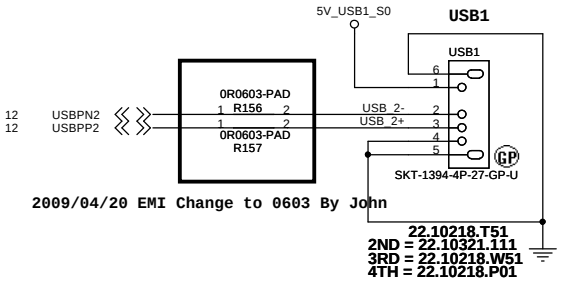

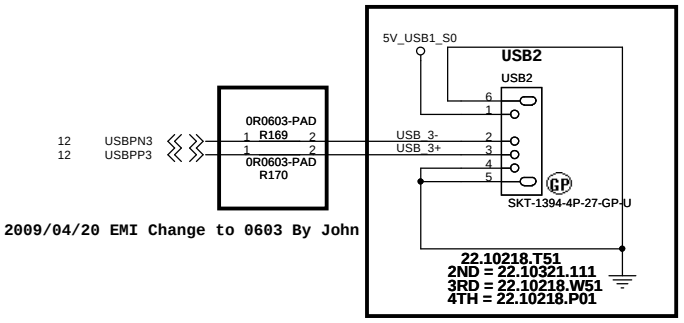

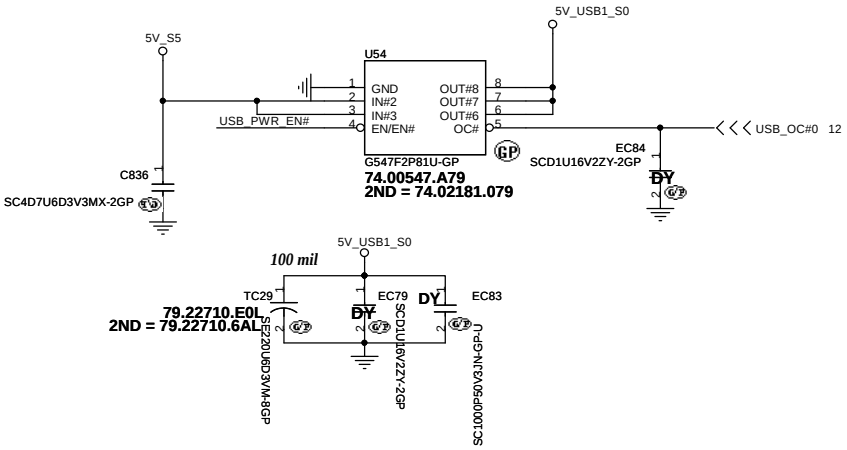

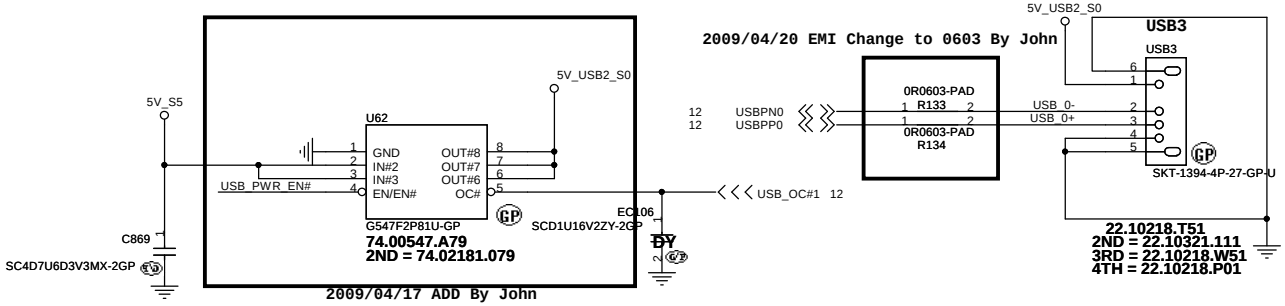

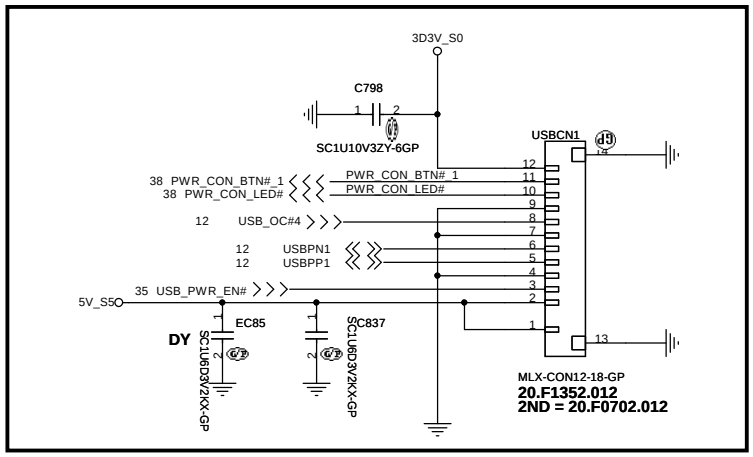

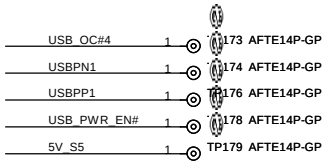

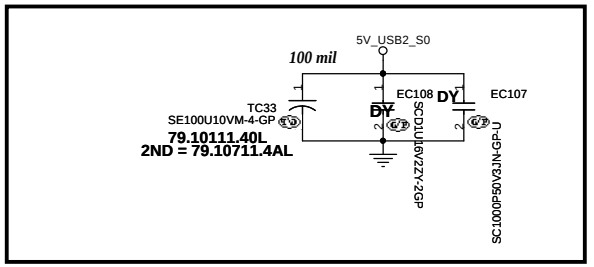

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB**	
Size	Document Number **JV71-TR**	Rev **SA**
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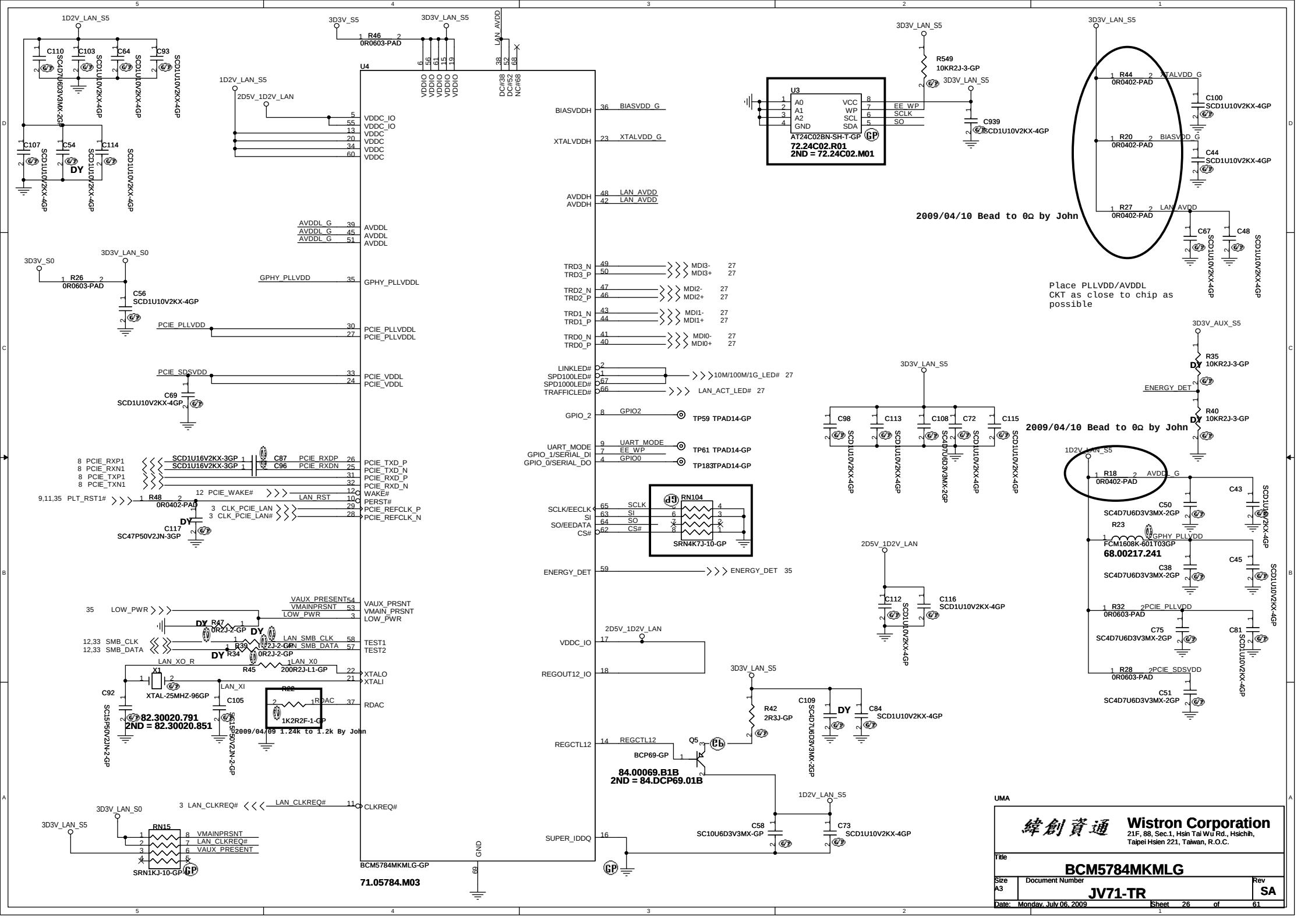
U4
BCM5784MKMLG-GP
71.05784.M03
U3
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01
2009/04/10 Bead to 0Ω by John
Place PLLVDD/AVDDL
CKT as close to chip as
possible
2009/04/10 Bead to 0Ω by John
82.30020.791
2ND = 82.30020.851
2009/04/09 1.24k to 1.2k By John
84.00069.B1B
2ND = 84.DCP69.01B
SRN4K7J-10-GP
SRN1KJ-10-GP
FCM1608K-601T03GP
68.00217.241
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5784MKMLG
Size A3
Document Number JV71-TR
Rev SA
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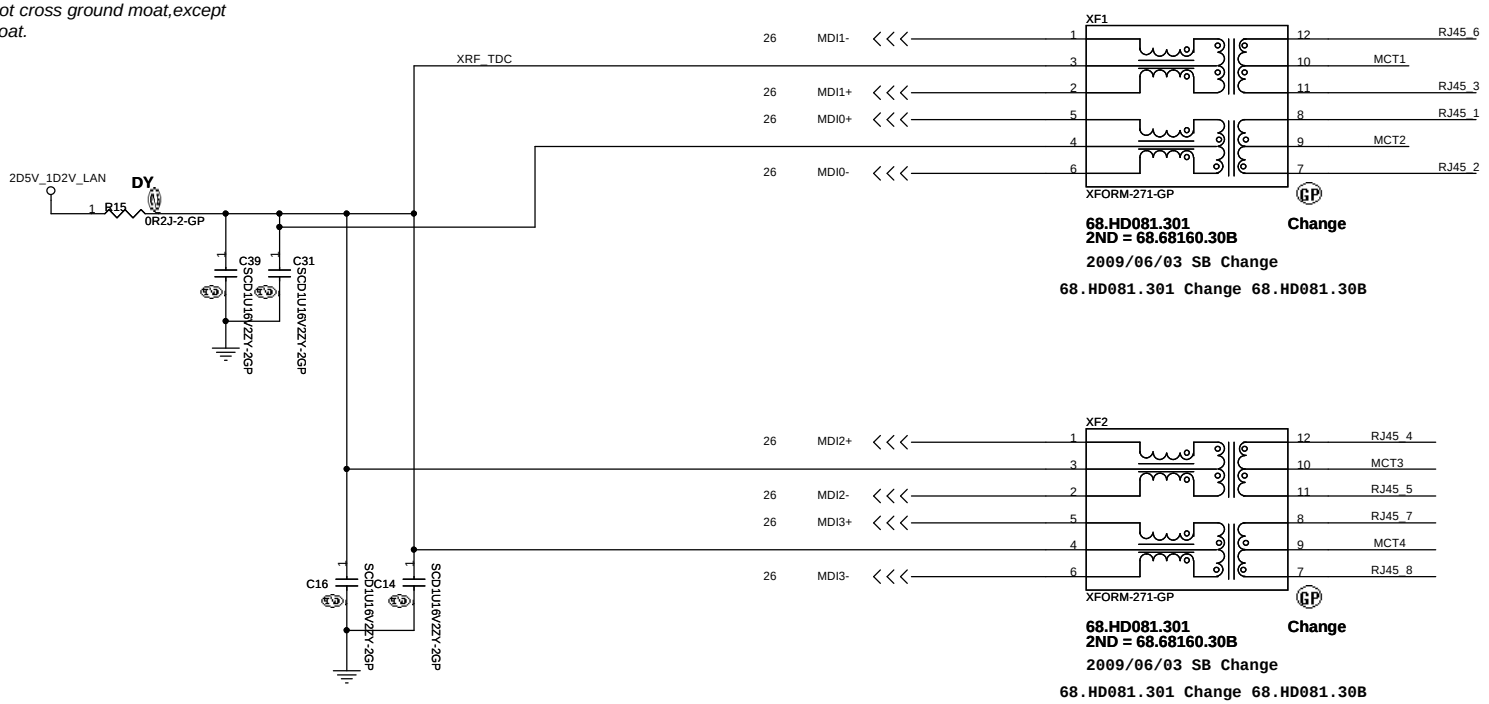
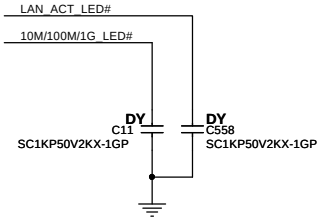
LAN Connector

GIGA Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



68.HD081.301 Change
2ND = 68.68160.30B
2009/06/03 SB Change
68.HD081.301 Change 68.HD081.30B

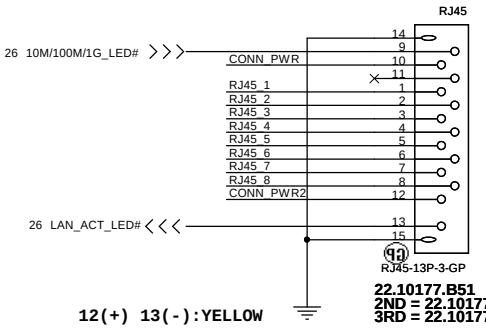


DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10(+) 9(-)::GREEN
10(+) 11(-):ORANGE

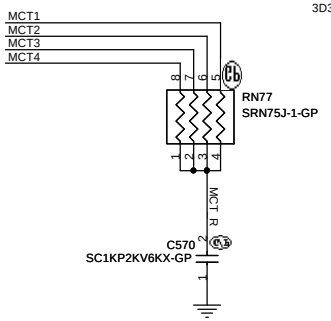
2009/04/09 Change 4P2R By John

LAN Connector

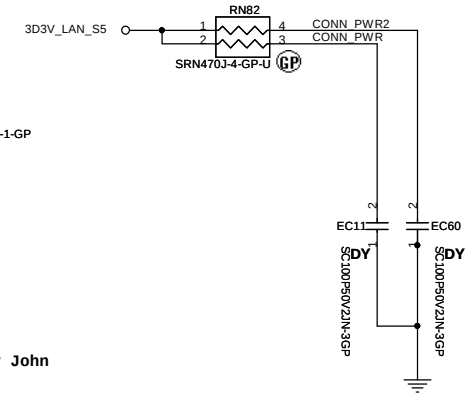


22.10177.B51
2ND = 22.10177.B81
3RD = 22.10177.C21
2009/05/23 SB Change

12(+) 13(-):YELLOW



2009/04/09 Follow JV70-PU By John



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN CONN		
Size: A3	Document Number: JV71-TR	Rev: SB
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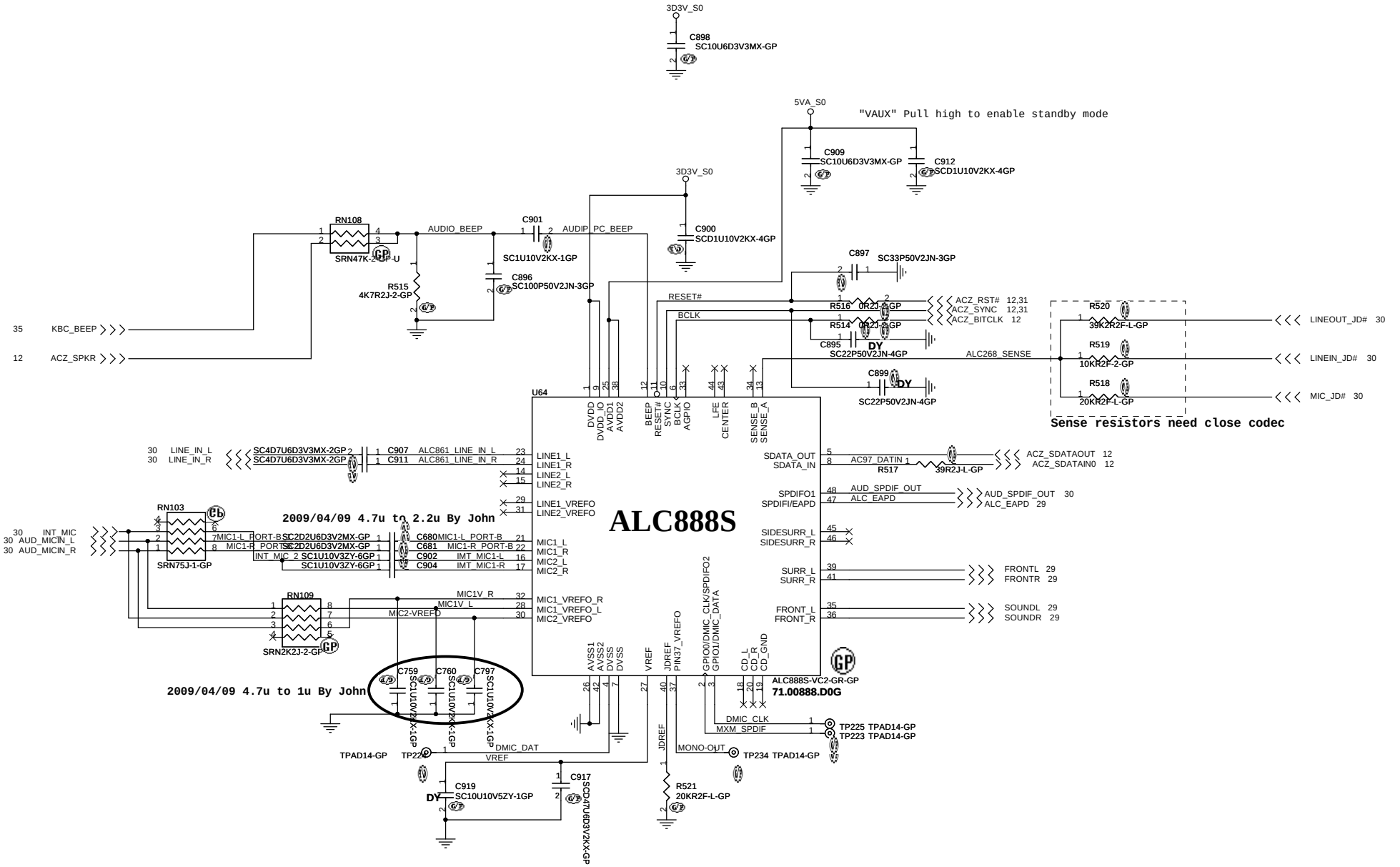
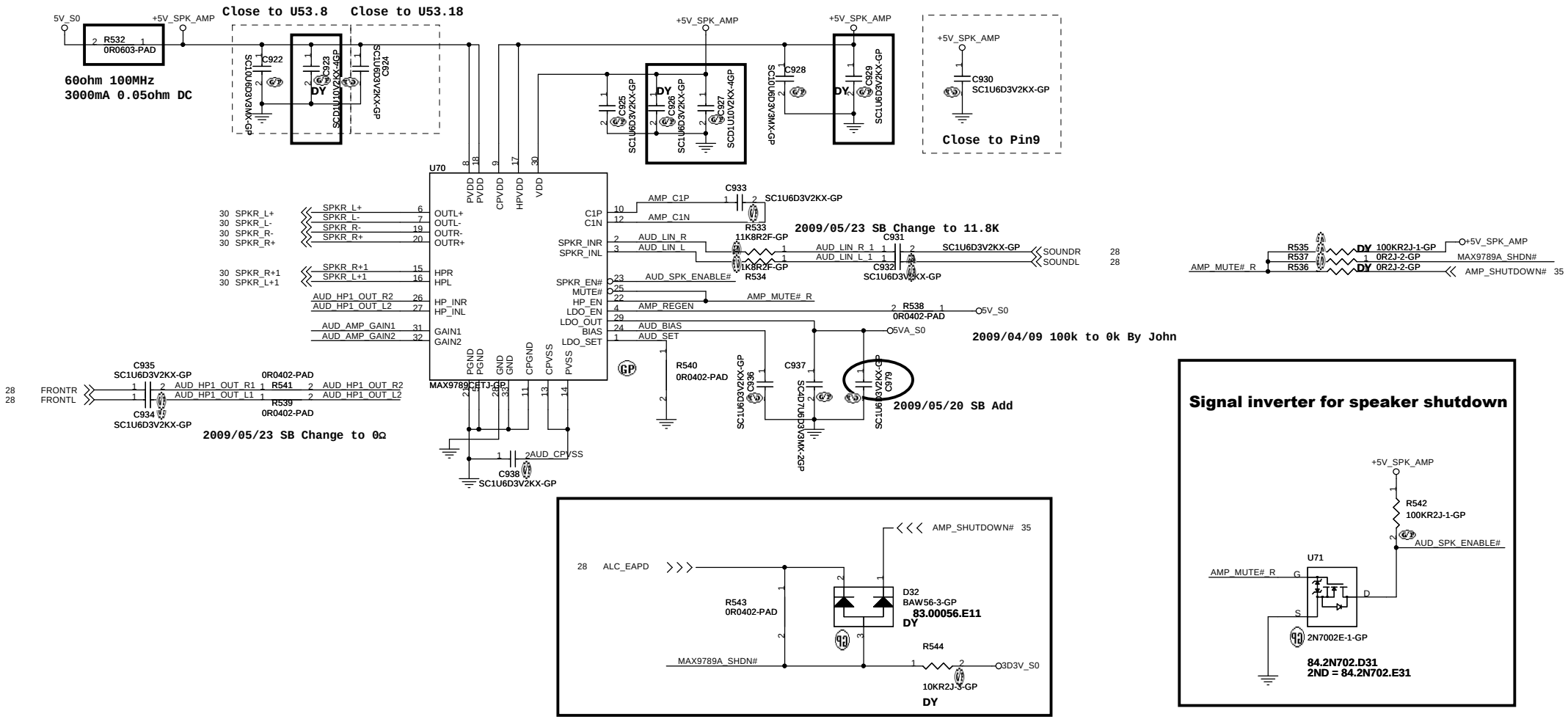


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Azalia codec ALC888**	
Size A3	Document Number **JV71-TR**	Rev **SB**
Date: Monday, July 06, 2009	Sheet 28 of 61	



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP**

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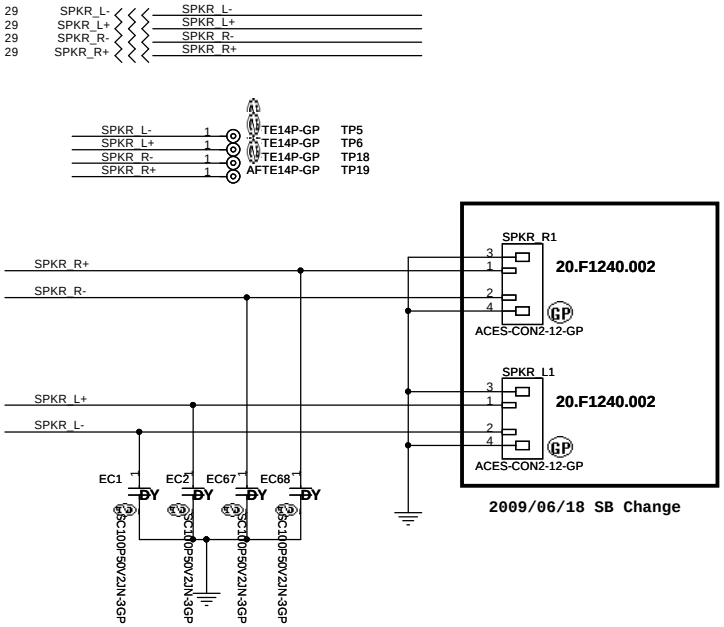
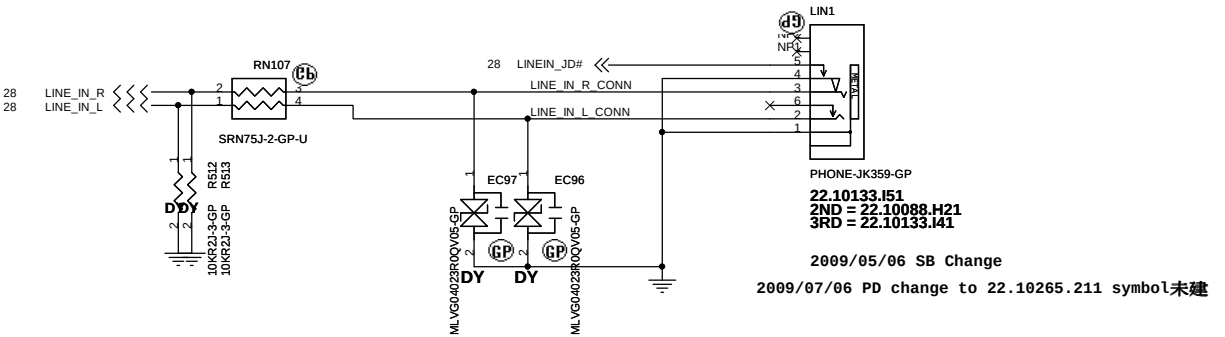
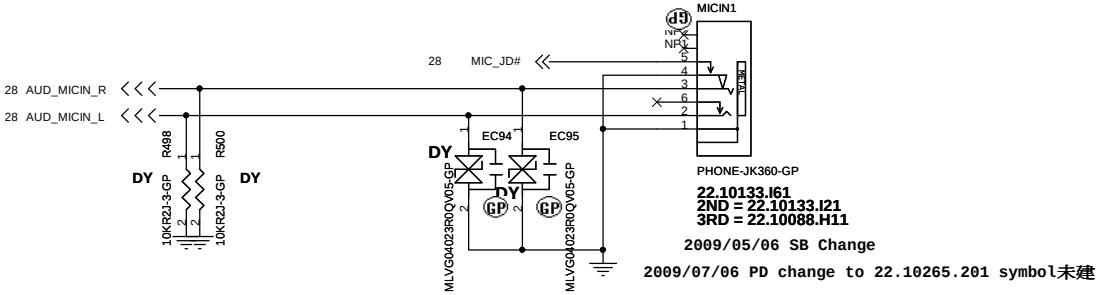
Internal Speaker



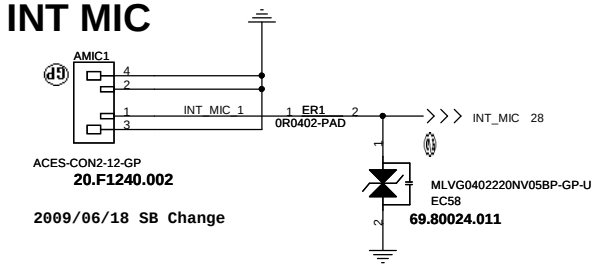
LINE IN



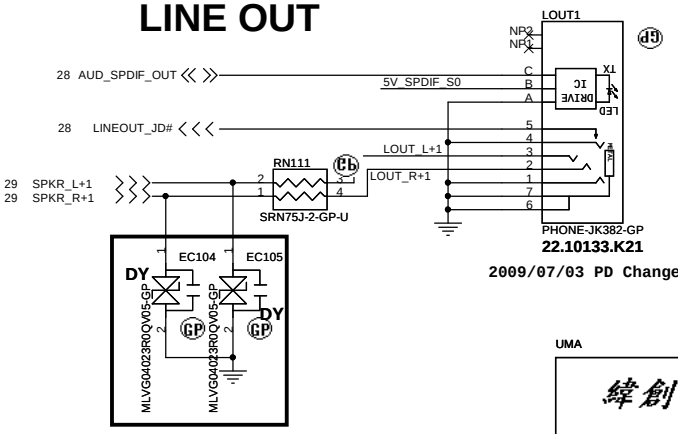
MIC IN

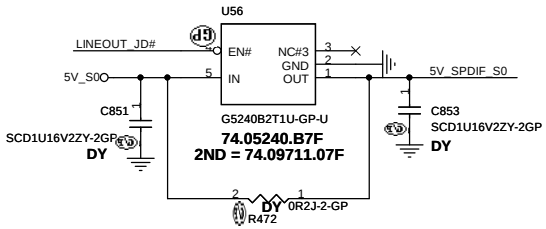


INT MIC



LINE OUT





UMA

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Title	**AUDIO JACK**	
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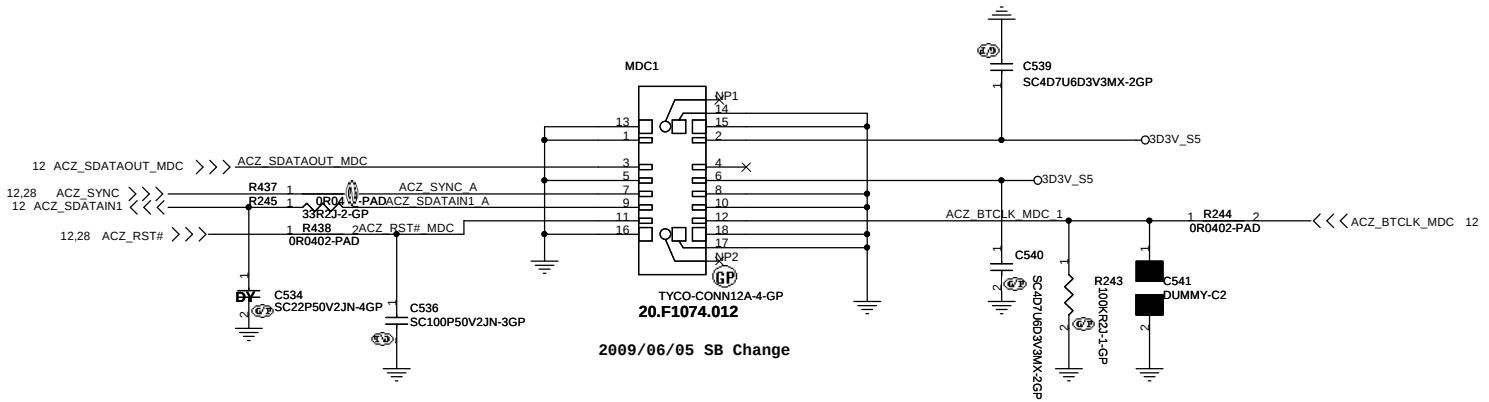
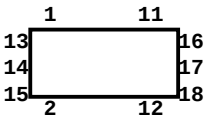
MDC 1.5 CONN





UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC		
Size	Document Number: JV71-TR	Rev: SB
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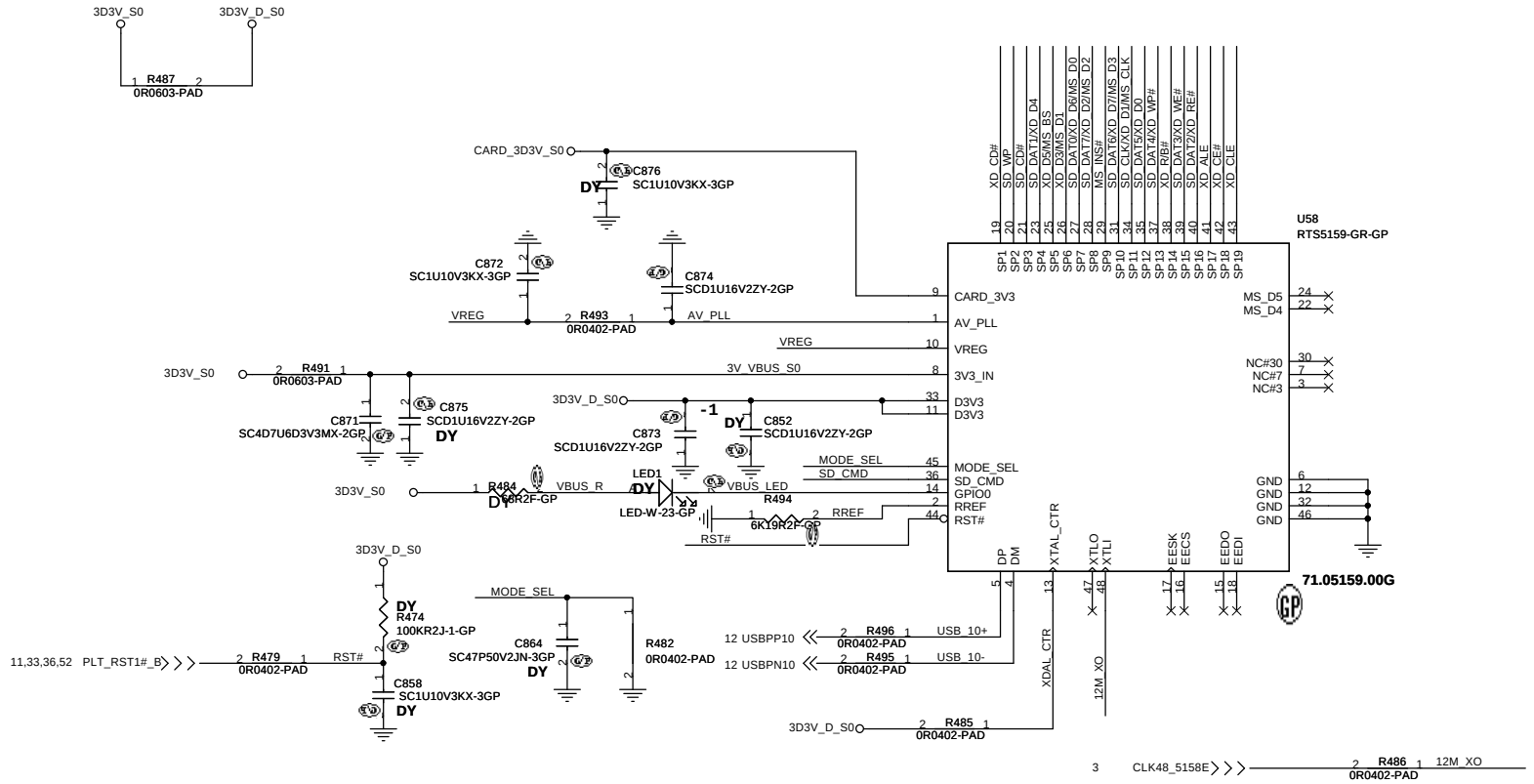
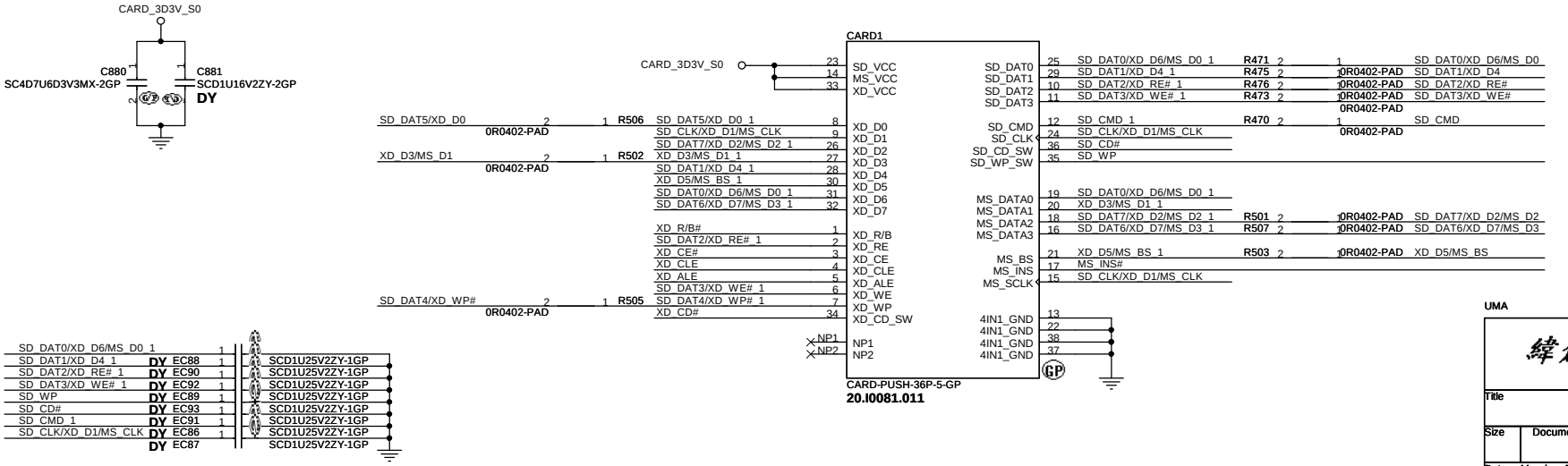


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	**CARDREADER- RTS5159**		
Size	Document Number **JV71-TR**		Rev **SB**
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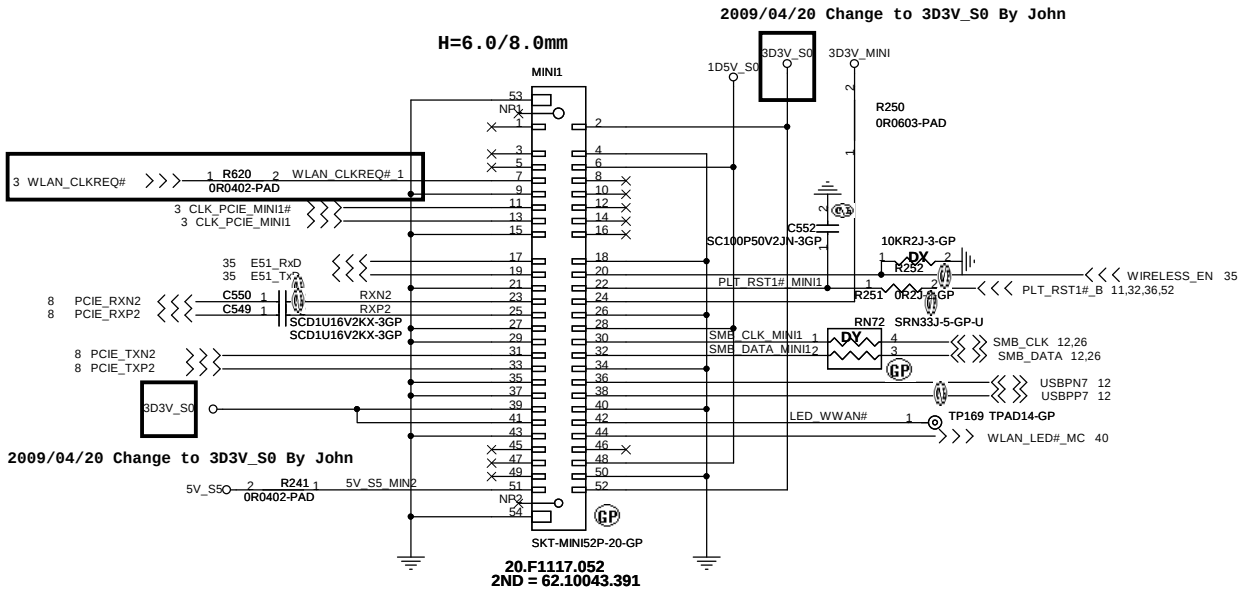
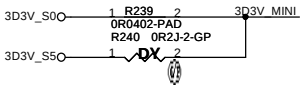
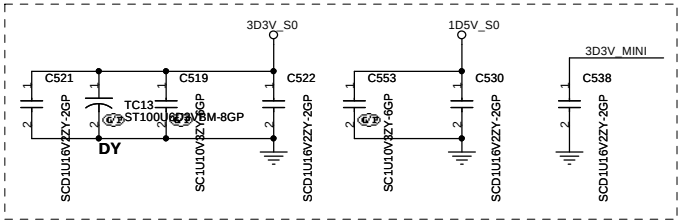
Mini Card Connector(WLAN)



2009/04/16 Change By John



Place near MINI1



UMA

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Title: MINI CARD		
Size	Document Number: JV71-TR	Rev: SA
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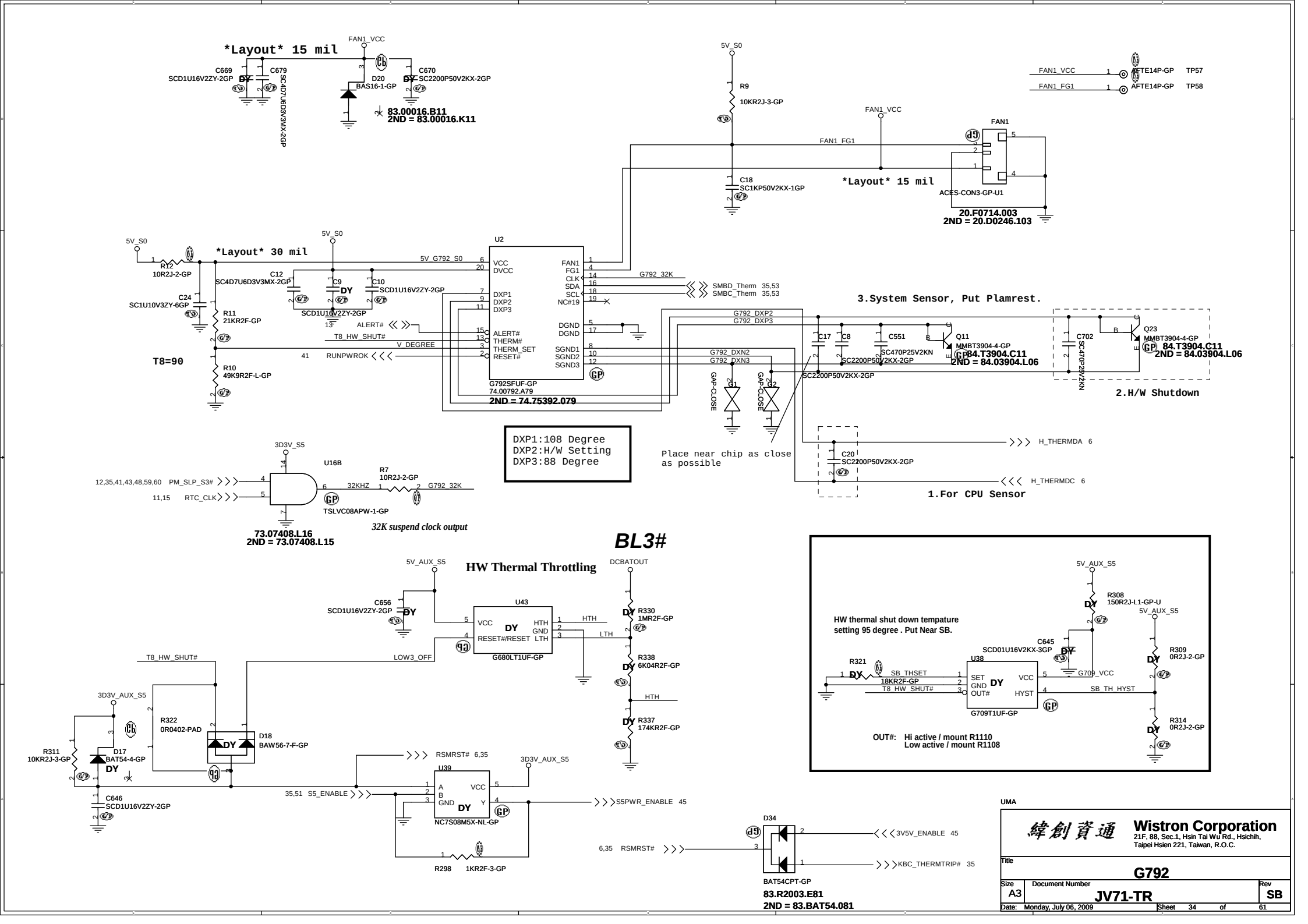

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	G792	
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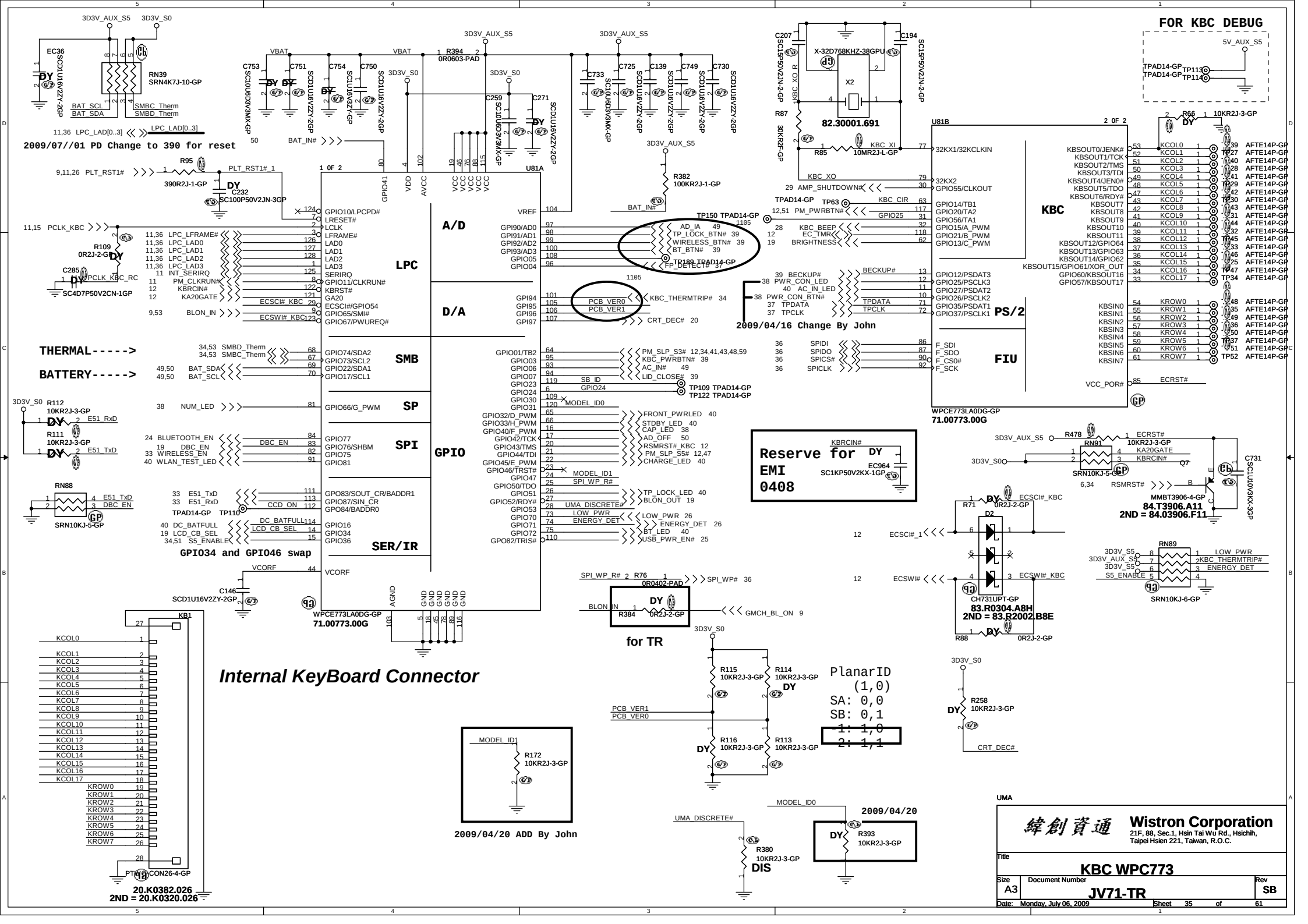
FOR KBC DEBUG
2009/07//01 PD Change to 390 for reset
2009/04/16 Change By John
THERMAL----->
BATTERY----->
GPIO034 and GPIO046 swap
Reserve for EMI 0408
for TR
2009/04/20 ADD By John
Internal KeyBoard Connector
PlanarID (1,0)
SA: 0,0
SB: 0,1
1: 1,0
2: 1,1
2009/04/20
DIS
KBC
PS/2
FIU
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
WPCE773LA0DG-GP
71.00773.00G
Wistron Corporation
KBC WPC773
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SB
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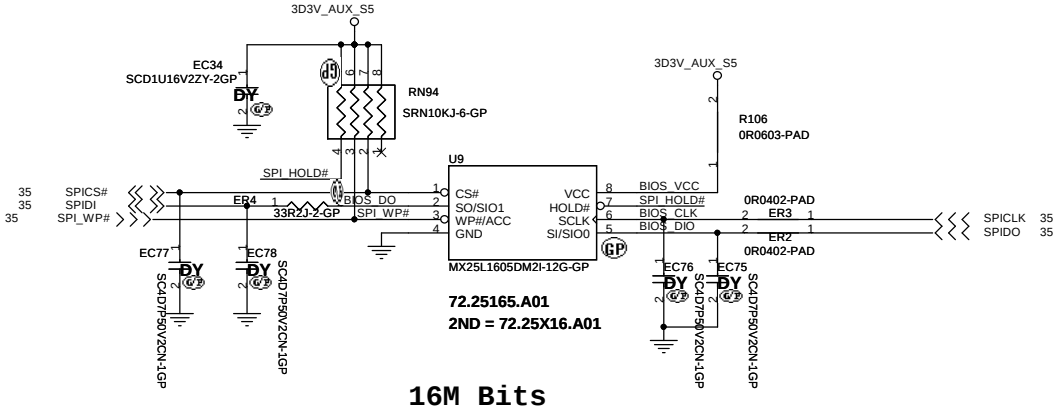
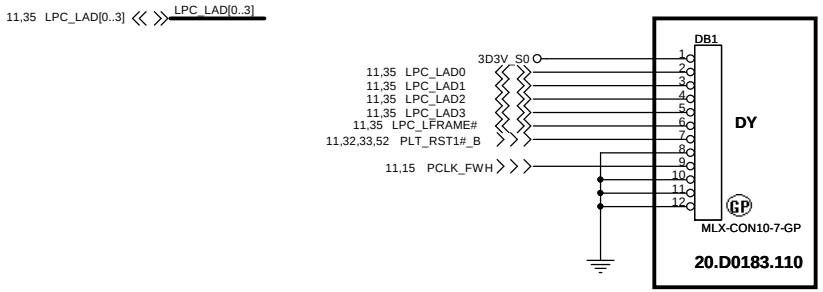


16M Bits

SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

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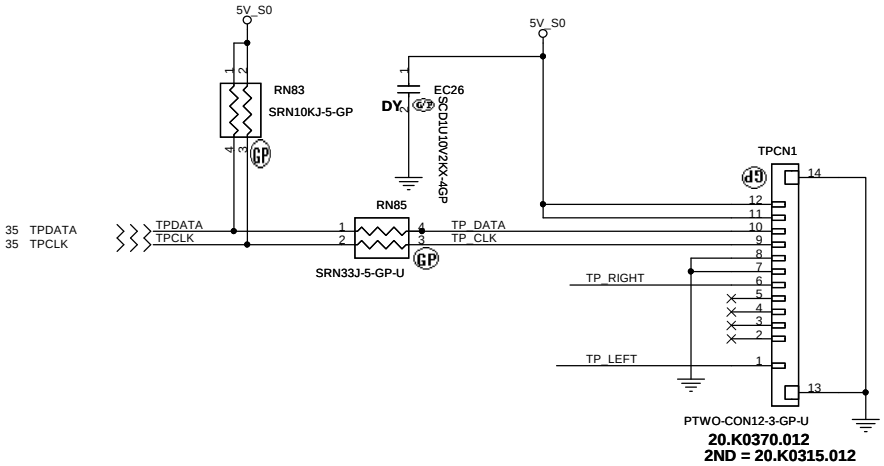
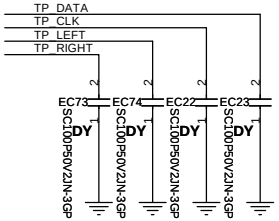
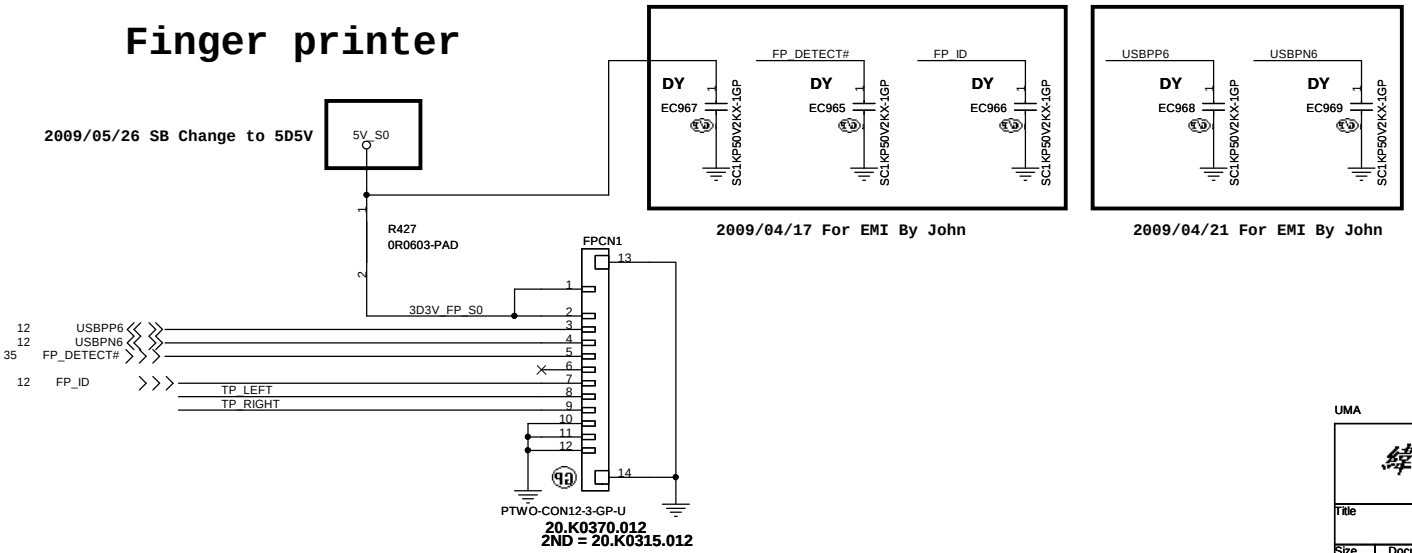
TOUCH PAD





Finger printer

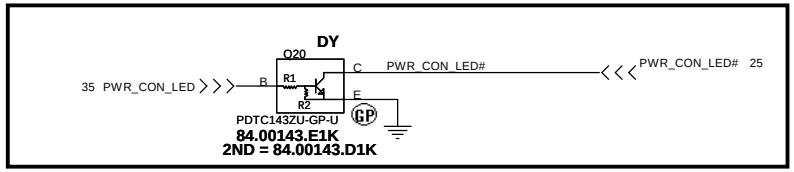


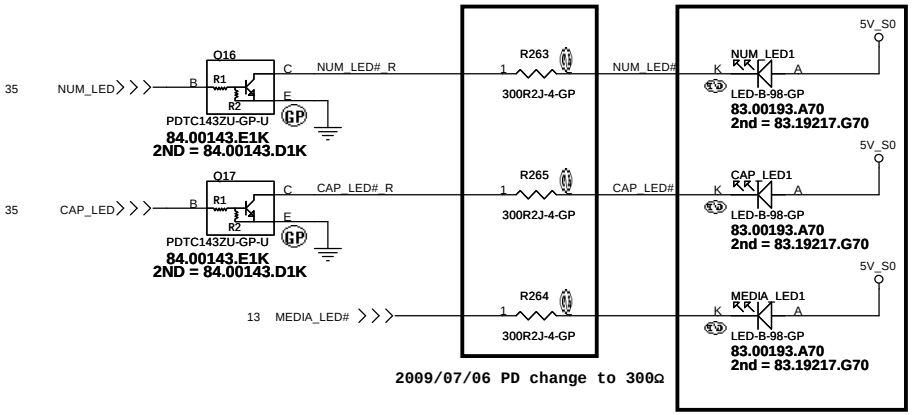
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

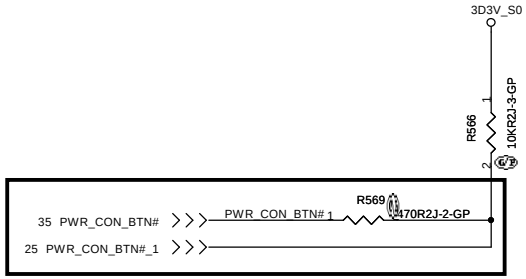
Title		
Touch PAD/Finger printer		
Size: A3	Document Number: **JV71-TR**	Rev: **SB**
Date: Monday, July 06, 2009	Sheet 37 of 61	

2009/04/16 Change By John

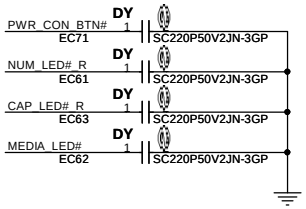




2009/07/06 PD change to 300Ω



2009/04/16 Change By John



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAUNCH BOARD		
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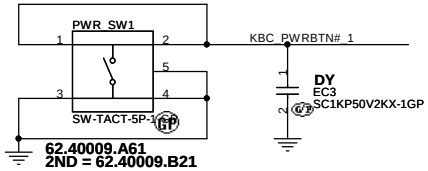
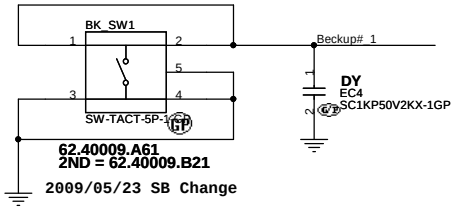
Power Button



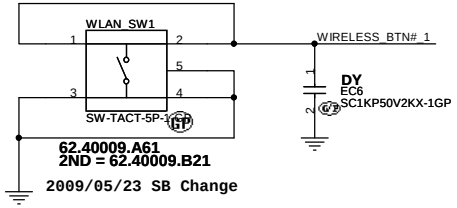
2009/05/23 SB Change

Beckup Button



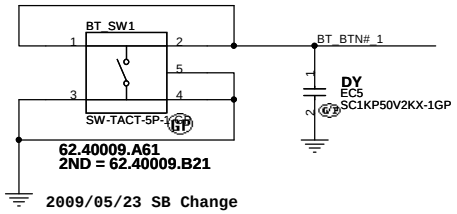
2009/05/23 SB Change

WIRELESS Button



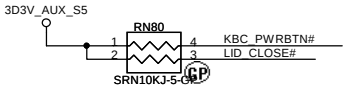
2009/05/23 SB Change

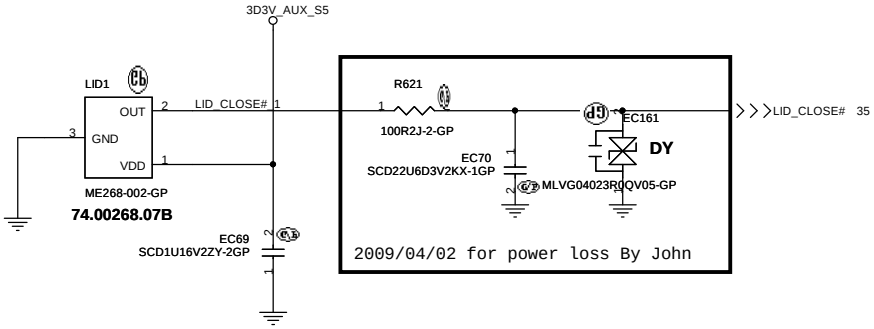
BT/3G Button

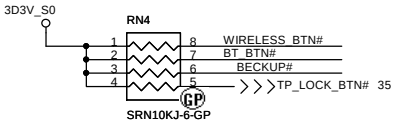


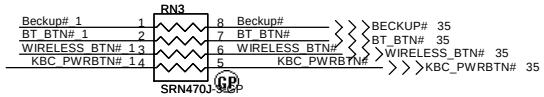
2009/05/23 SB Change

Cover Up Switch

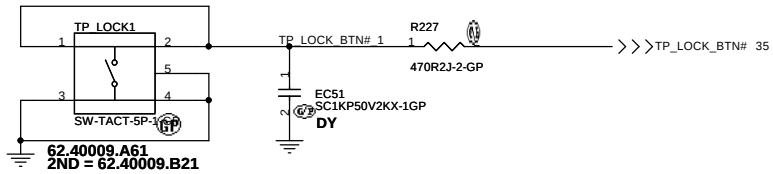








T/P lock Button



2009/05/23 SB Change

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SWITCH		
Size: A3	Document Number: JV71-TR	Rev: SA
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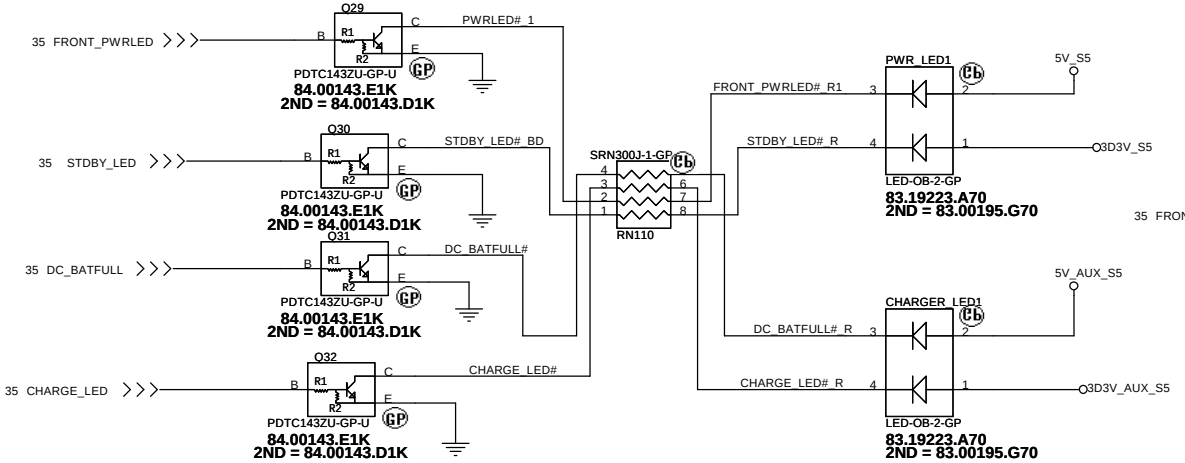
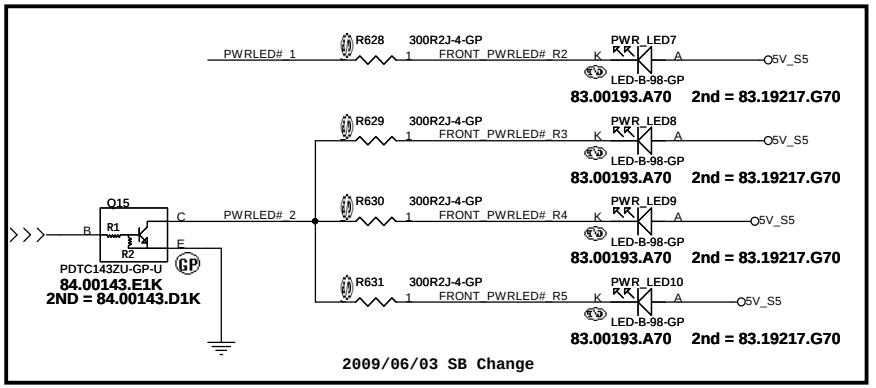
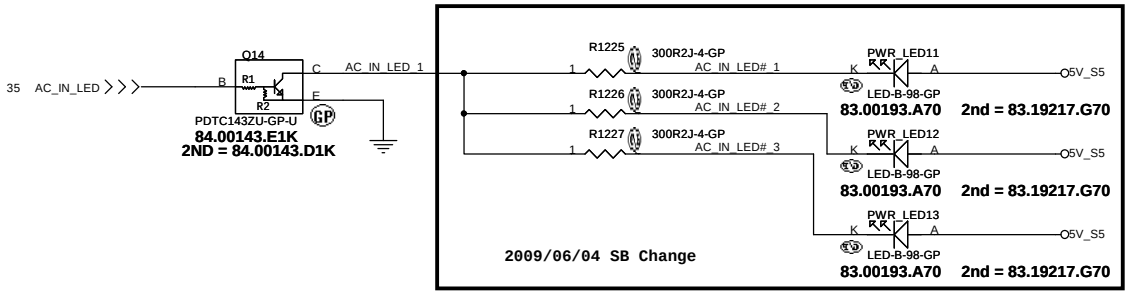
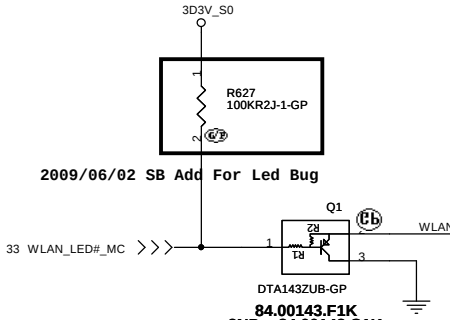
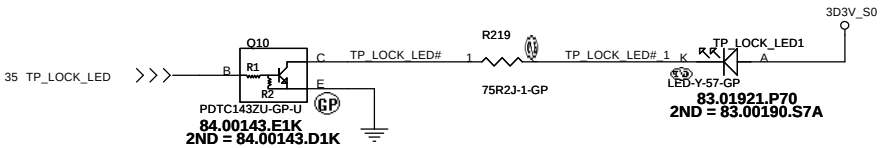
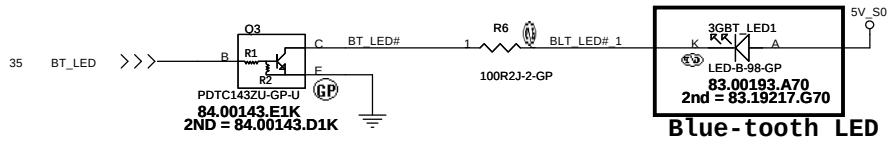




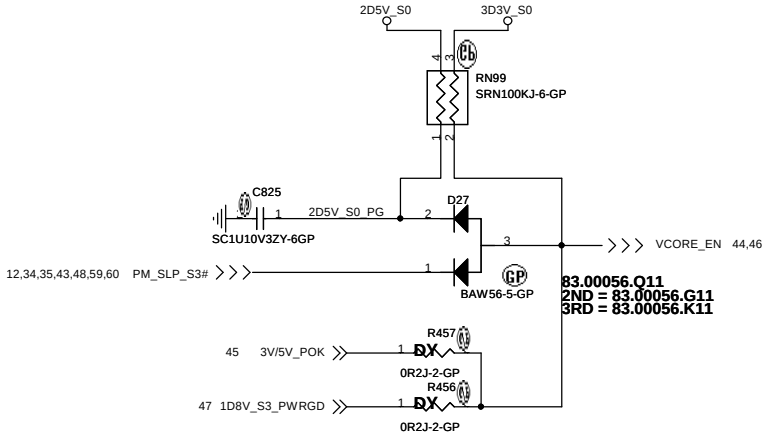




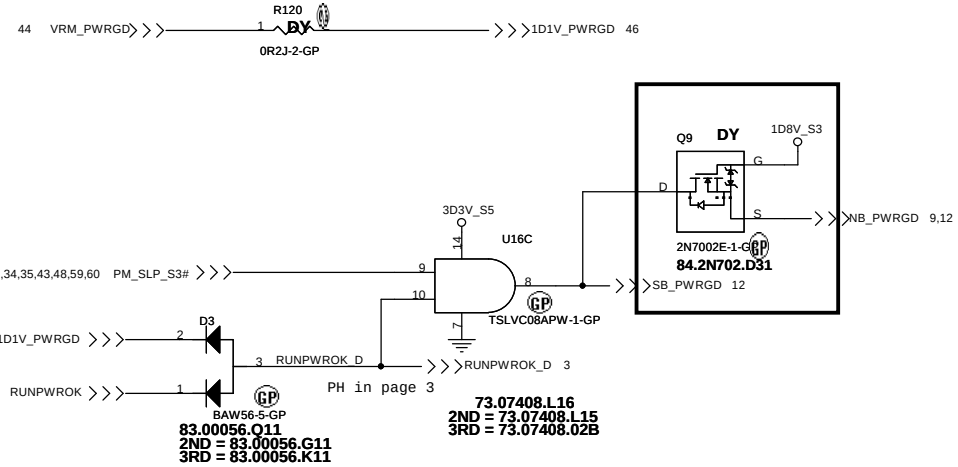




緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LED**	
Size: A3	Document Number: **JV71-TR**	Rev: **SB**
Date: Wednesday, July 08, 2009	Sheet 40 of 61	



P/H @ 1D8V_S3 PAGE



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER ON LOGIC**

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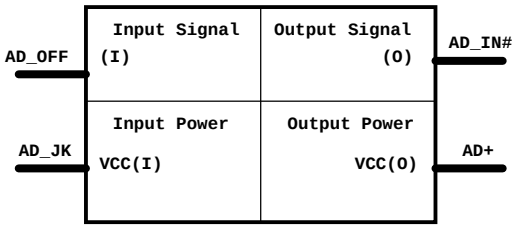
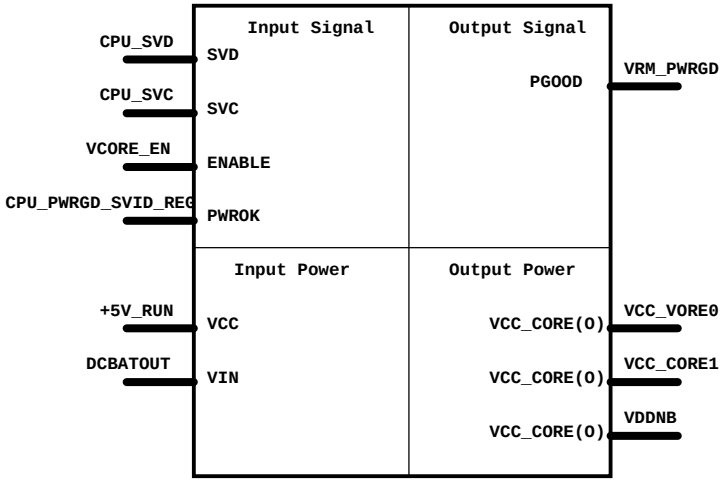
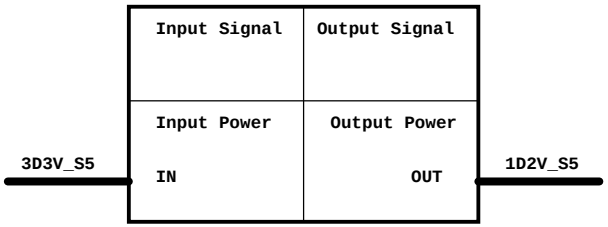
Adapter



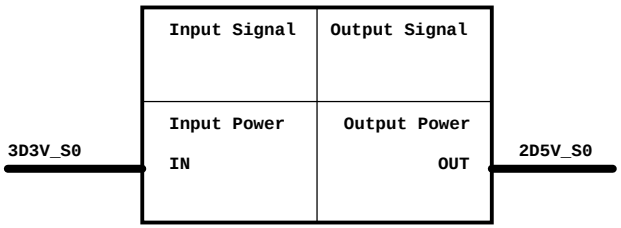
CPU_CORE
ISL6265HRTZ



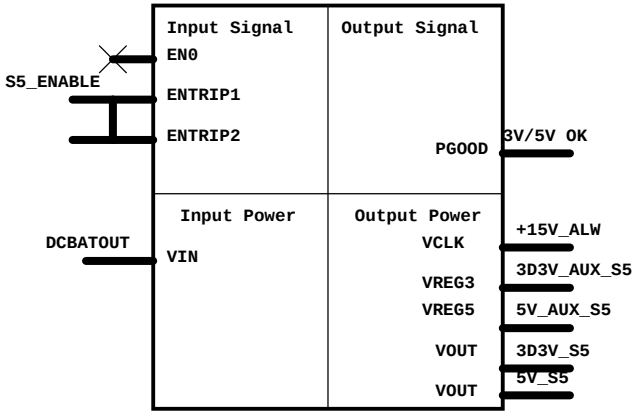
1D2V LDO G9161



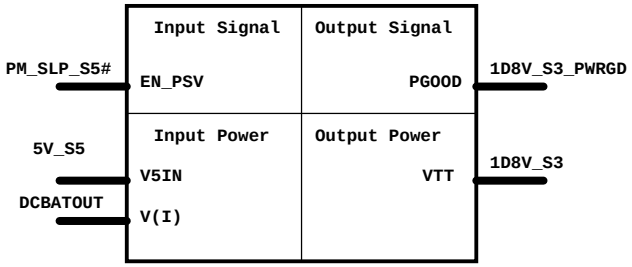
2D5V LDO R9161



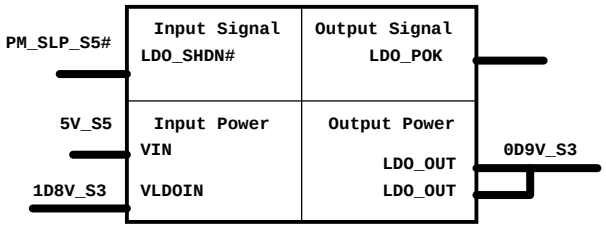
DCDC 5V/3D3V(RT8205A)



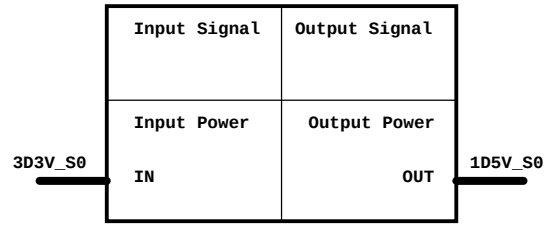
DCDC 1D8V(RT8209B)



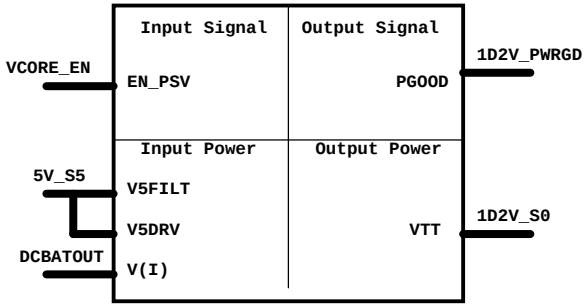
0D9V LDO RT9026



1D5V LDO G9571



DCDC 1D2V(TPS51124)



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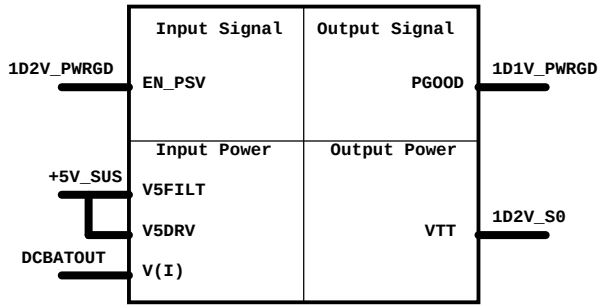
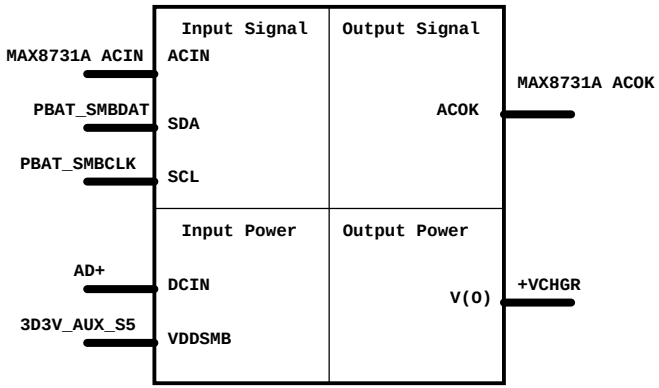


CHARGER MAX8731



UMA

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Title: **Power Block Diagram**

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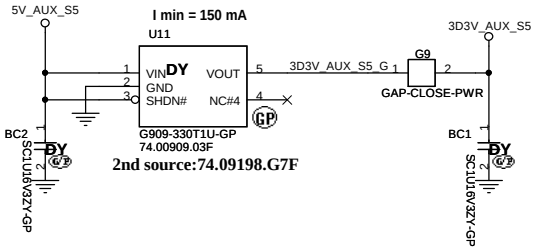
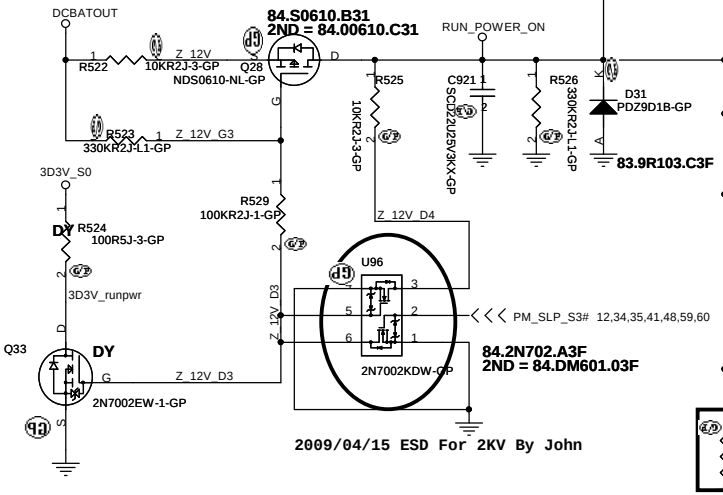
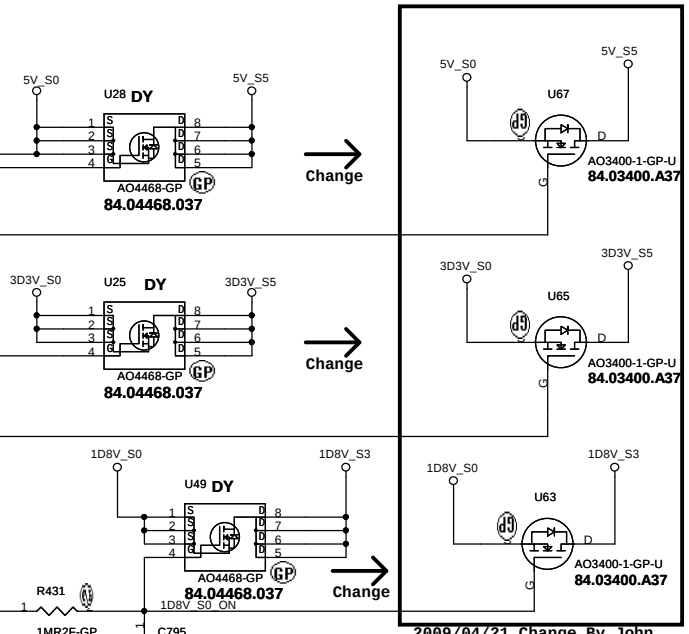
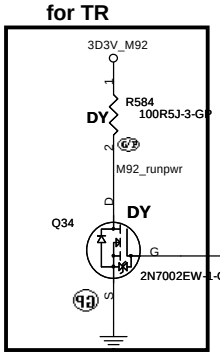
Aux Power 3D3V_AUX_S5

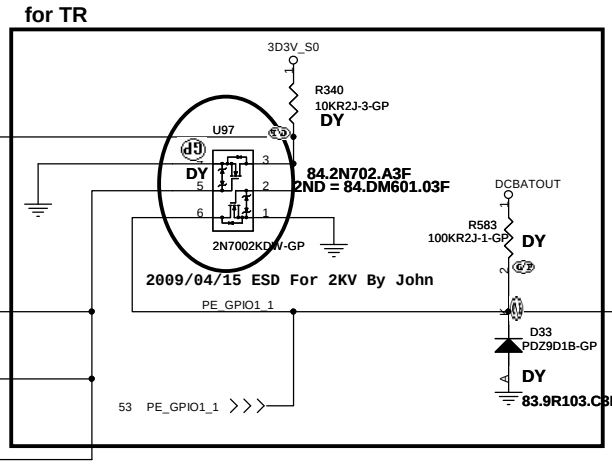


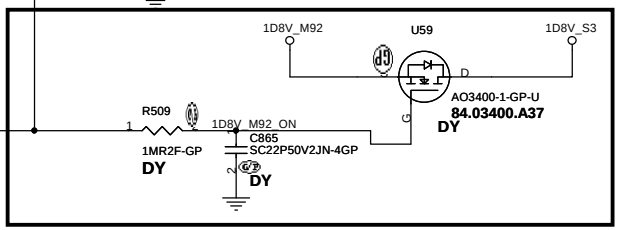
Run Power

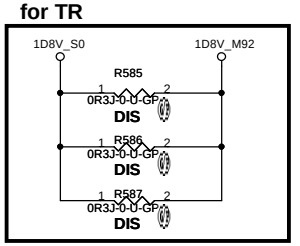


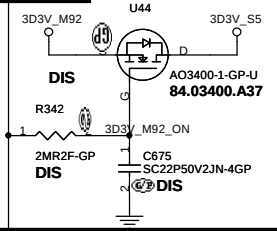












R509,R342→10MΩ
C865→22pF
C675→1000pF
For VGA sequence issue

UMA

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Title: RUN AND AUX POWER

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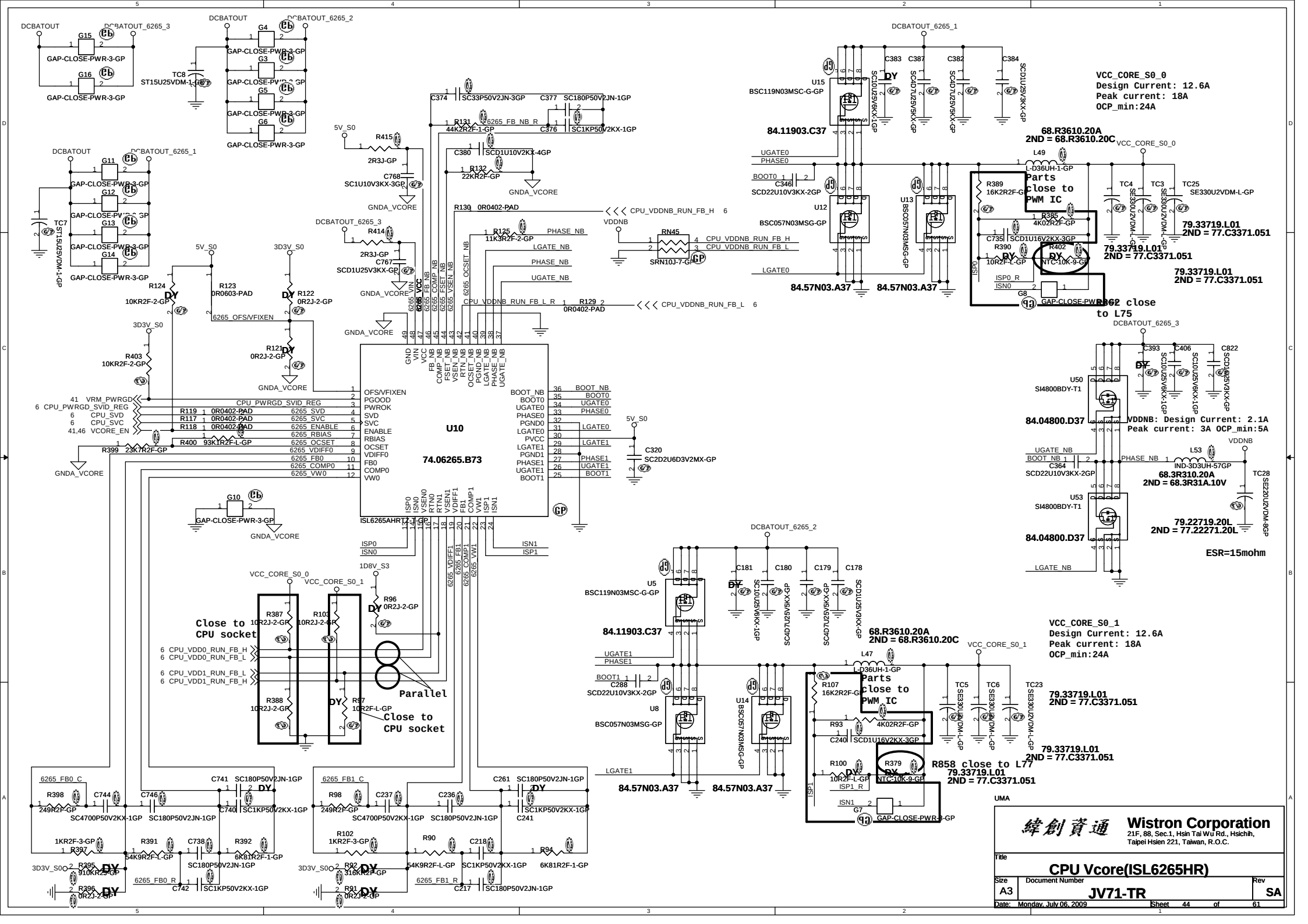
U10
ISL6265AHRTZ-T-GP
74.06265.B73
U15
BSC119N03MSC-G-GP
U12
BSC057N03MSG-GP
U13
BSC057N03MSG-GP
U5
BSC119N03MSC-G-GP
U8
BSC057N03MSG-GP
U14
BSC057N03MSG-GP
U50
SI4800BDY-T1
U53
SI4800BDY-T1
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
ESR=15mohm
84.11903.C37
84.57N03.A37
84.04800.D37
68.R3610.20A
2ND = 68.R3610.20C
68.R310.20A
2ND = 68.3R31A.10V
79.33719.L01
2ND = 77.C3371.051
79.22719.20L
2ND = 77.22271.20L
Parts close to PWM IC
R858 close to L77
Close to CPU socket
Parallel
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
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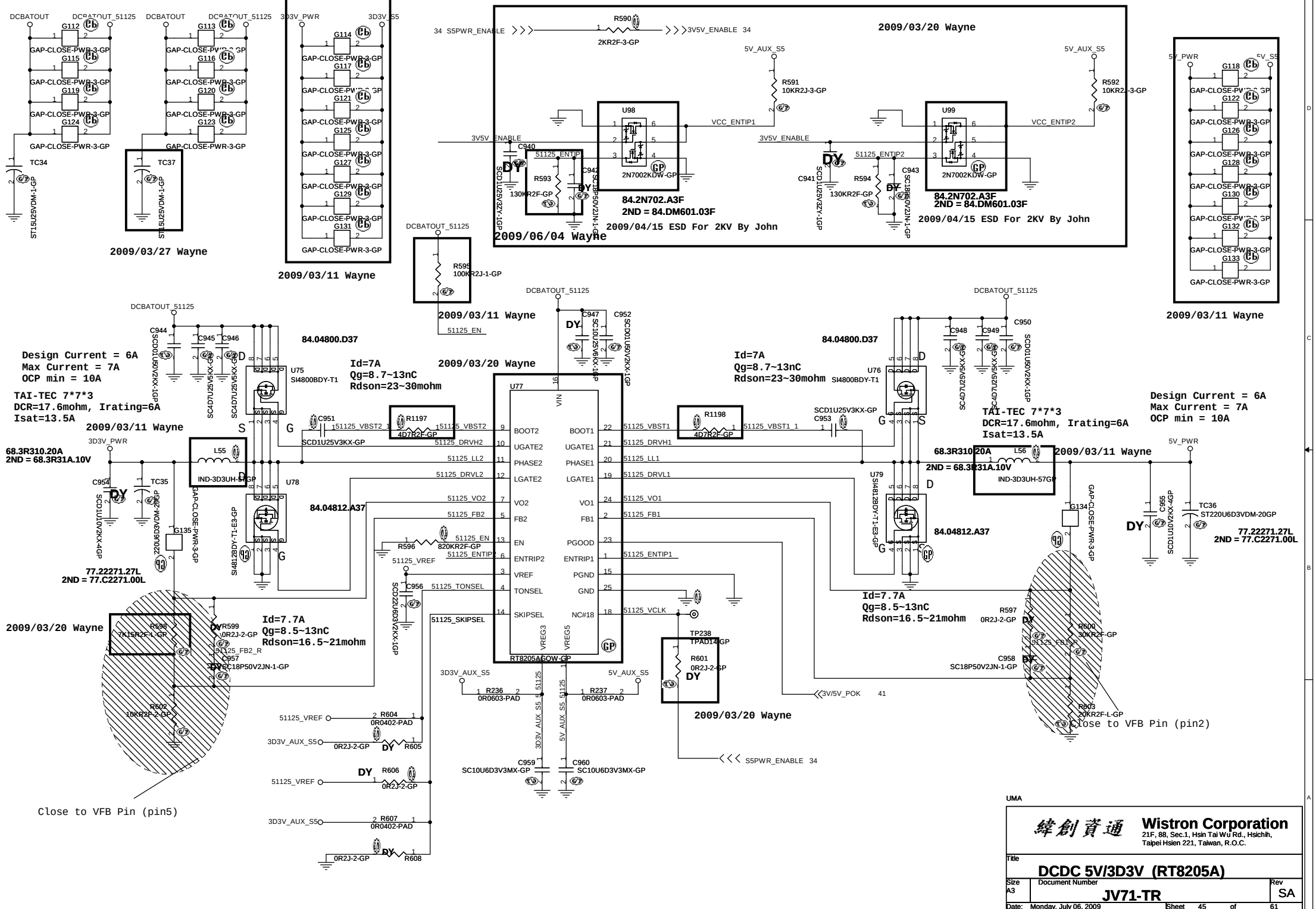
DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_PWR
5V_S5
5V_AUX_S5
3V5V_ENABLE
34 S5PWR_ENABLE
3V5V_ENABLE 34
2009/03/20 Wayne
2009/03/27 Wayne
2009/03/11 Wayne
2009/06/04 Wayne
2009/04/15 ESD For 2KV By John
84.2N702.A3F
2ND = 84.DM601.03F
84.04800.D37
84.04812.A37
Design Current = 6A
Max Current = 7A
OCP min = 10A
TAI-TEC 7*7*3
DCR=17.6mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
68.3R310.20A
2ND = 68.3R31A.10V
77.22271.27L
2ND = 77.C2271.00L
RT8205AGQW-GP
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
UMA
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (RT8205A)
JV71-TR
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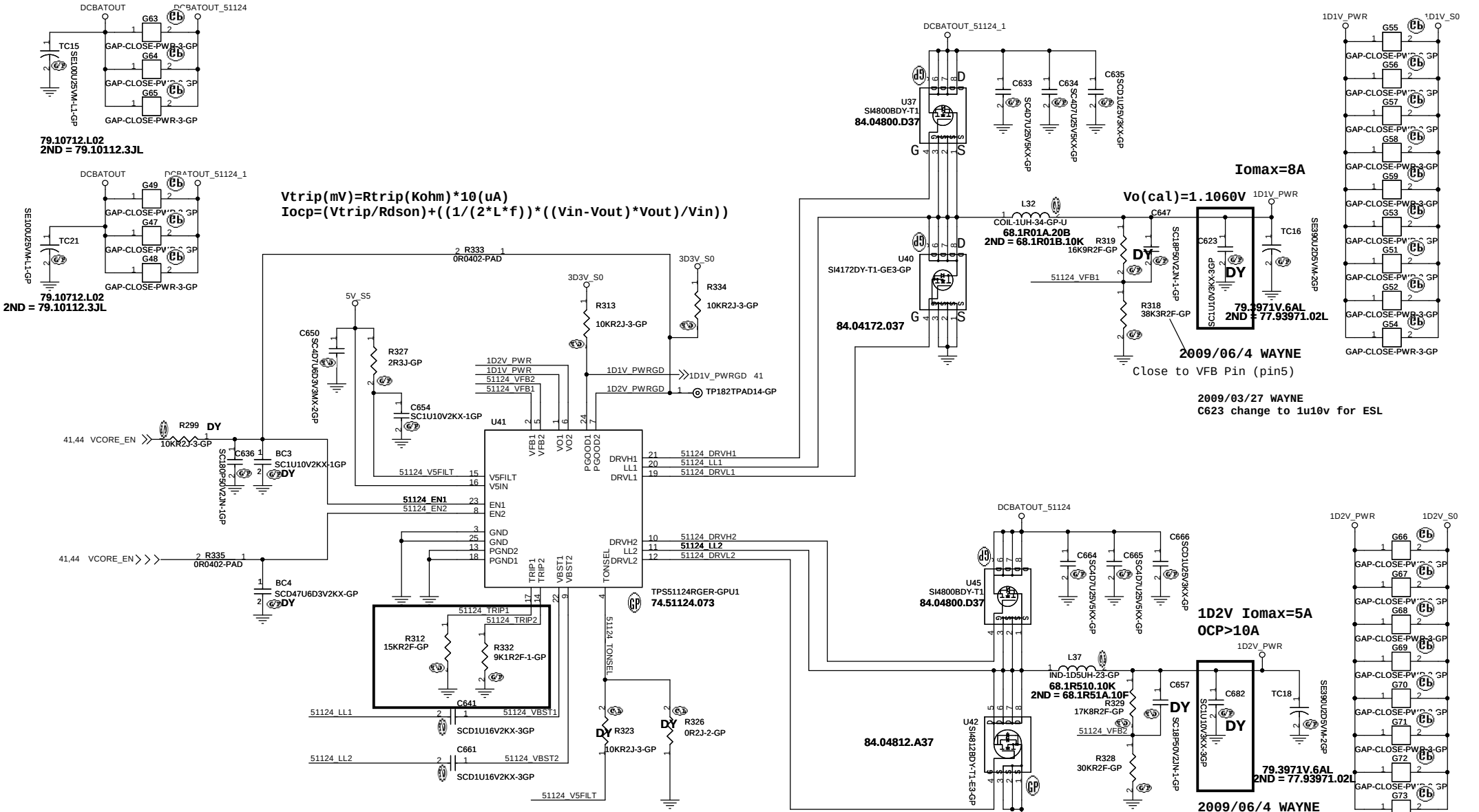

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	**300k/CH1** **360k/CH2**	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

UMA

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Title: ***TPS51124_1D1V_1D2V***

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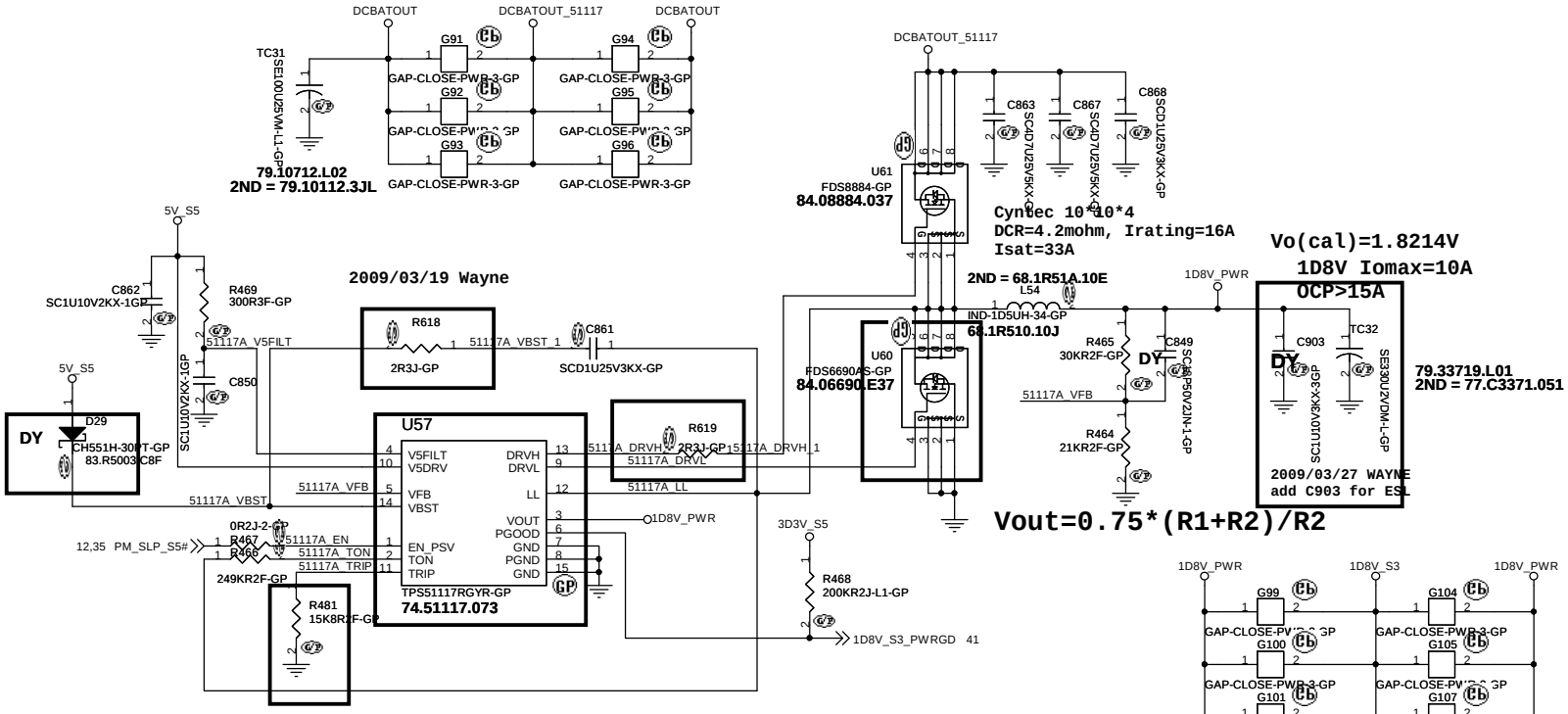
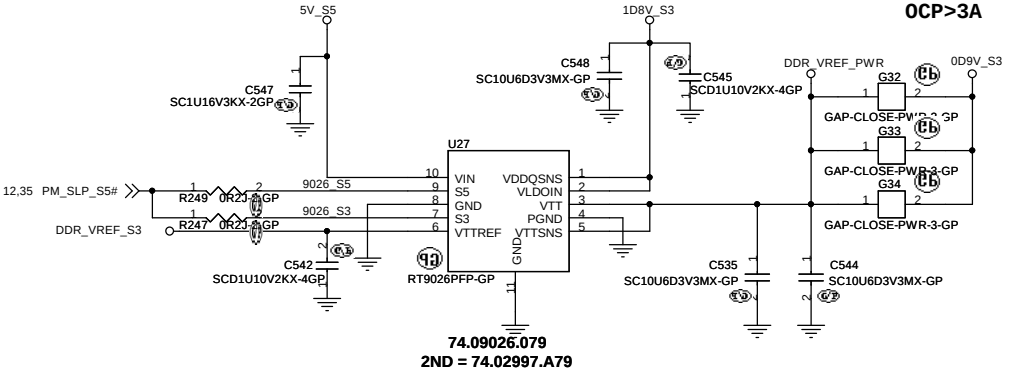


DDR_0.9V

Iomax=1.5A
OCP>3A



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCDC_1D8V_APW7141/LDO 0D9V**

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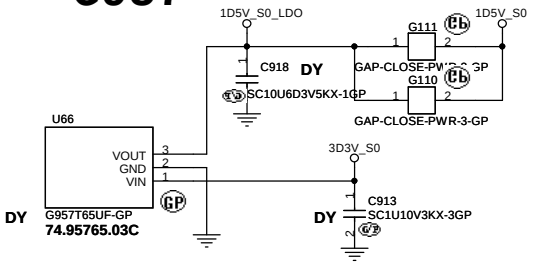
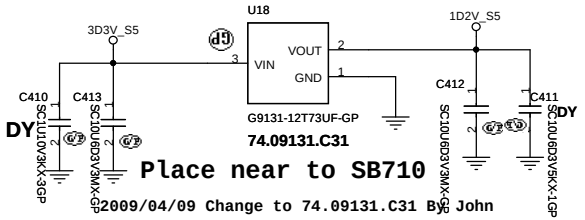
G957

1D5V_S0
Iomax=1A



For MINI Card.NEW Card power SW

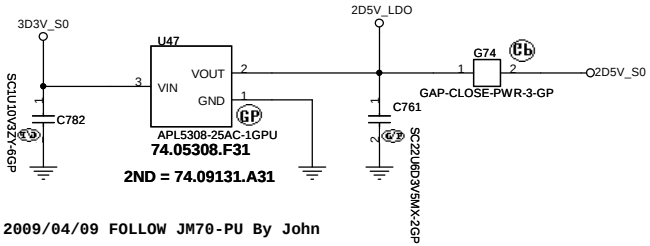
1D2V_S5
Iomax=400mA



Place near to SB710

2009/04/09 Change to 74.09131.C31 By John

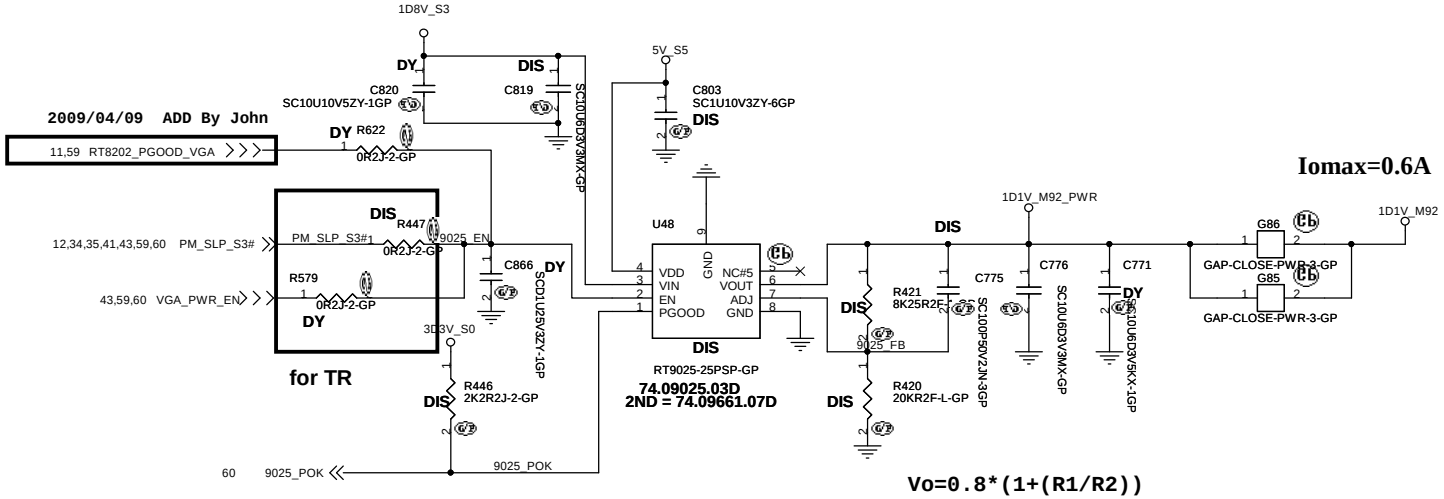
2D5V
Iomax=0.2A



2009/04/09 FOLLOW JM70-PU By John

Place near to CPU

Iomax=0.6A



Vo=0.8*(1+(R1/R2))

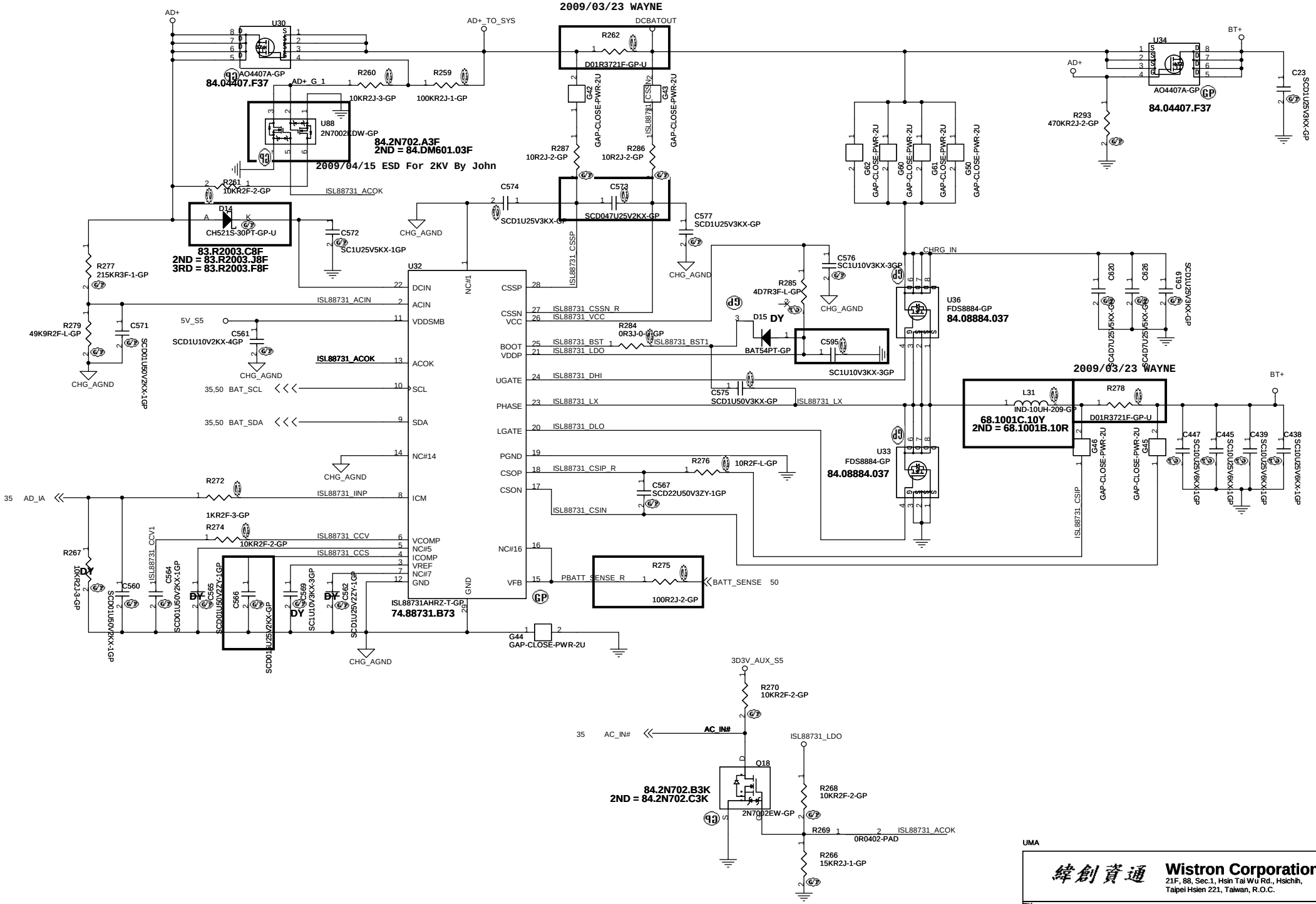
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LDO 2D5V/1D5V/1D2V_S5/1D1V_M92**

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 48 of 61



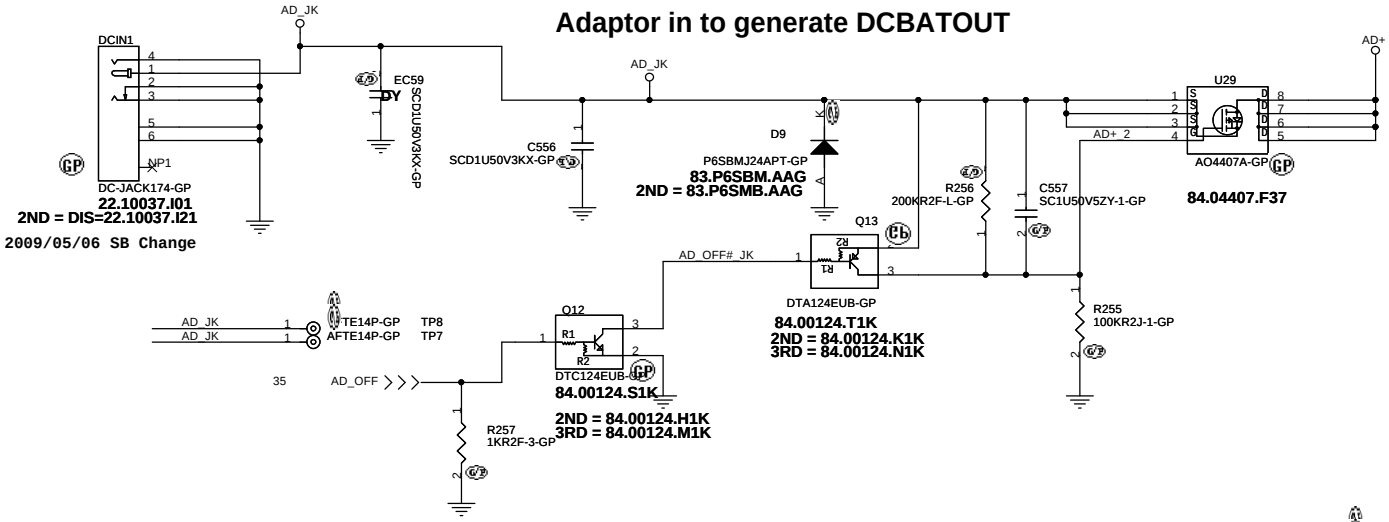
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

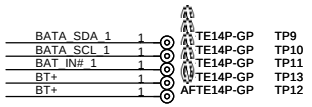
Title: ISL88731A Charger

Size: A3 | Document Number: JV71-TR | Rev: SA

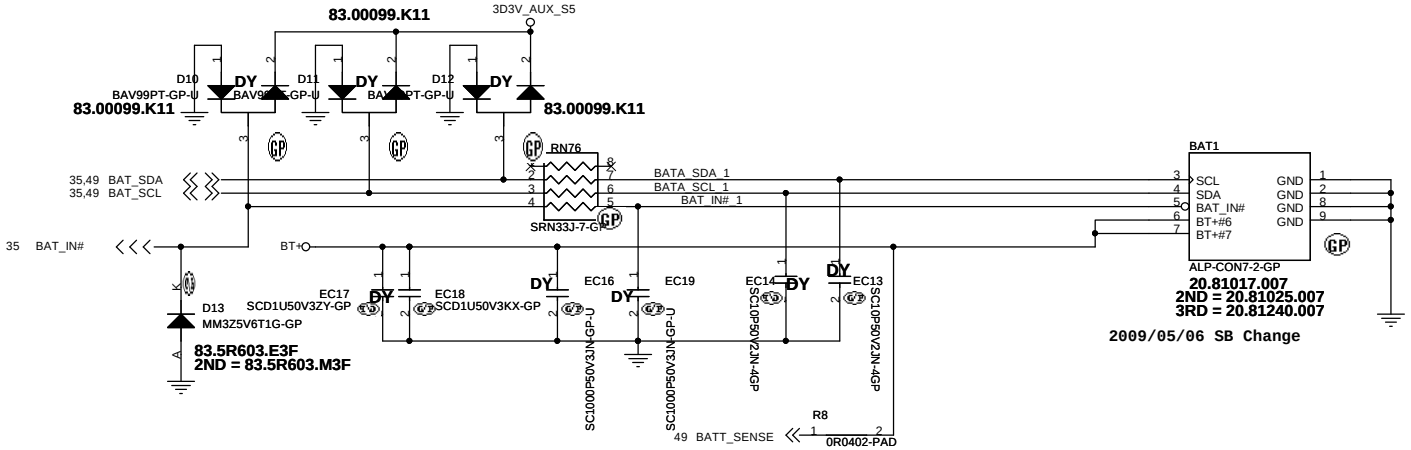
Date: Monday, July 06, 2009 | Sheet 49 of 61

Adaptor in to generate DCBATOUT



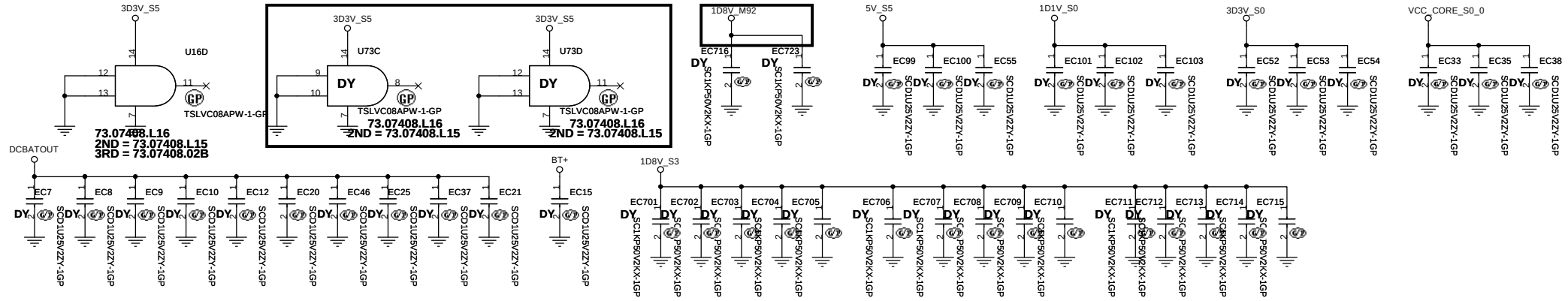


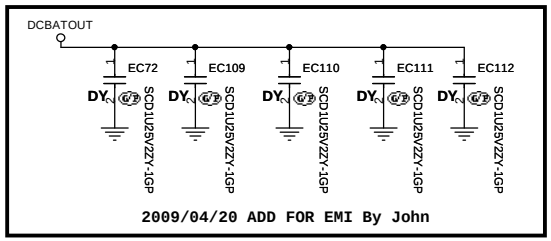
BATTERY CONNECTOR

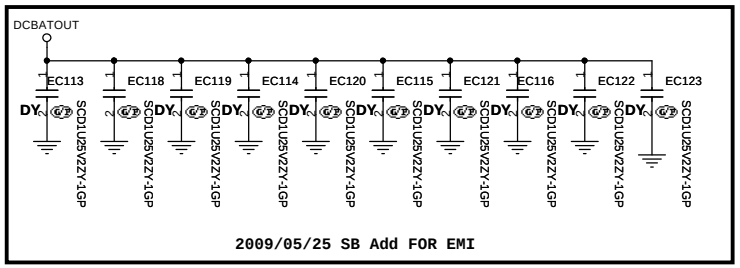


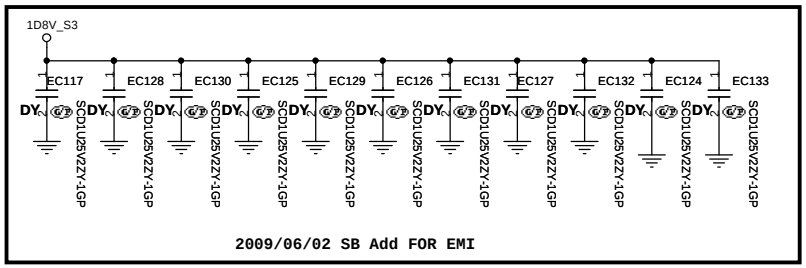
UMA

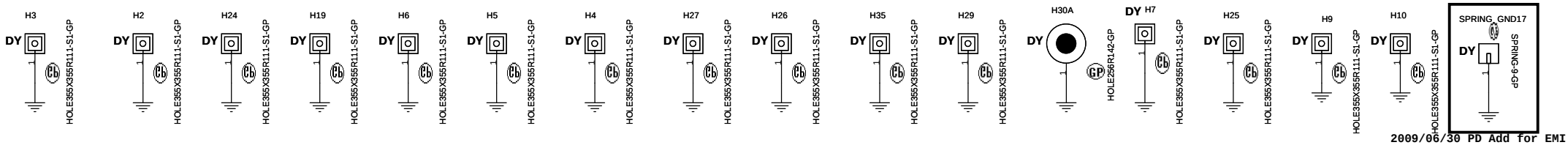
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AD/BATT CONN**	
Size	Document Number **JV71-TR**	Rev **SB**
Date: Monday, July 06, 2009	Sheet 50 of 61	

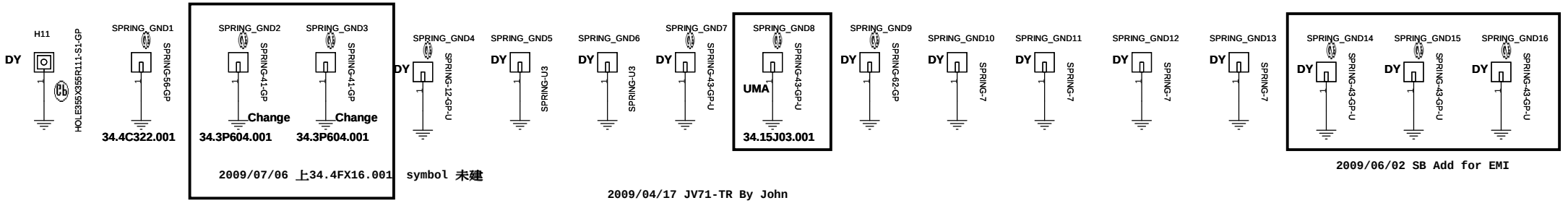


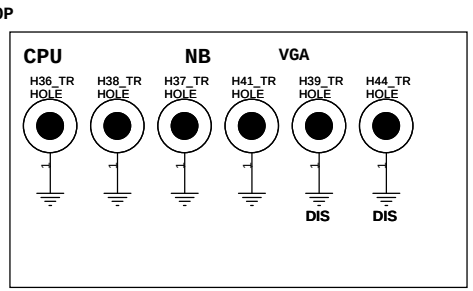


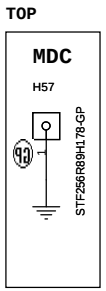


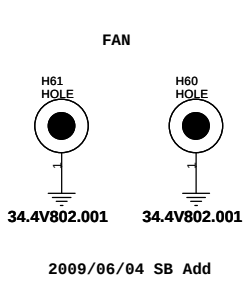












Check test point

3D3V_S0	TP233	TPAD14-GP	
3D3V_AUX_S5	TP232	TPAD14-GP	
3D3V_S5	TP231	TPAD14-GP	
5V_S5	TP230	TPAD14-GP	
12,35 PM_PWRBTN#	TP229	TPAD14-GP	
6,11 CPU_PWRGD	TP228	TPAD14-GP	
34,35 S5_ENABLE	TP227	TPAD14-GP	
6,11 CPU_LDT_RST#	TP226	TPAD14-GP	

Test Point放在Dimm Door打開可量測處

SA SB -1

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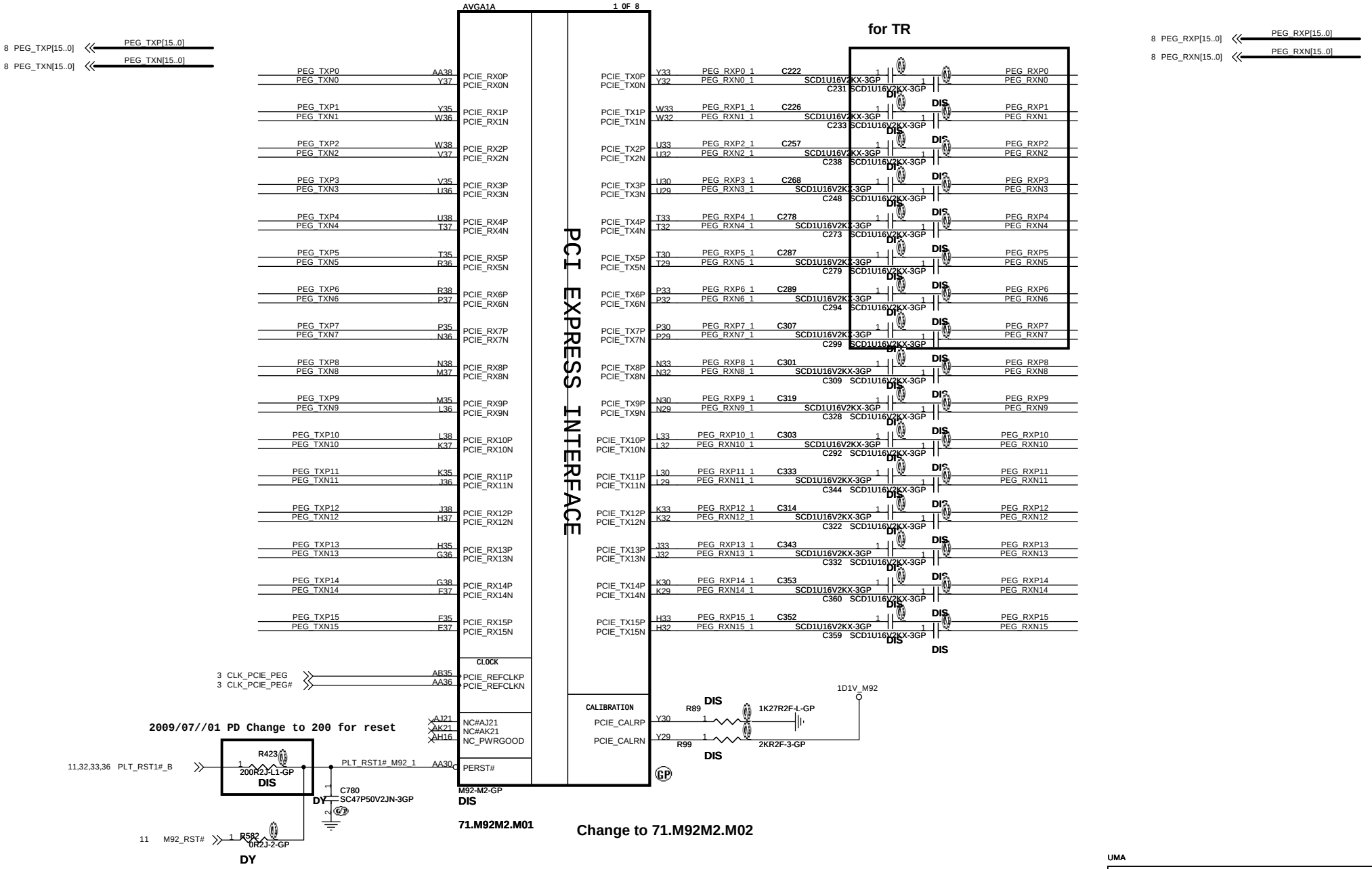
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI/Spring/Boss**

Size | Document Number: **JV71-TR** | Rev: **SB**

Date: Friday, July 10, 2009 | Sheet 51 of 61



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **M92 PCIE**		
Size: A3	Document Number: **JV71-TR**	Rev: **SB**
Date: Monday, July 06, 2009	Sheet 52 of 61	

Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)

It's strap for GDDR3-136ball
Need to Clarify

Back Bias (body bias) which minimizes power consumption in battery modes.
PD = Disable
PU = Enable

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

Depending on OSC used select voltage divider resist values R25 R70 to ensure XTALIN voltage level of 1.8V

For Thermal sensor

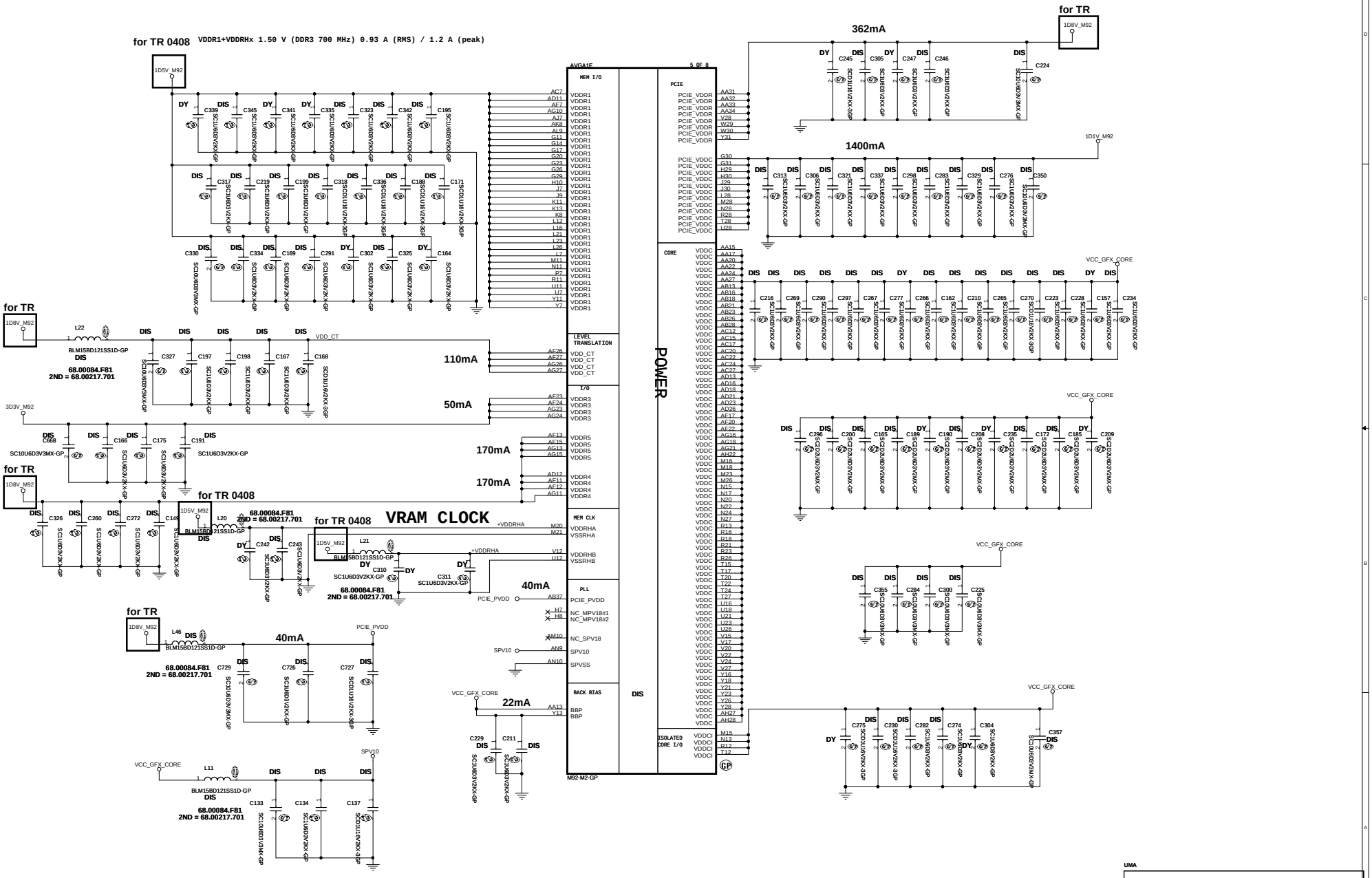
84.2N702.B3K
2ND = 84.2N702.C3K

84.2N702.A3F
2ND = 84.DM601.03F

2009/04/15 ESD For 2KV By John

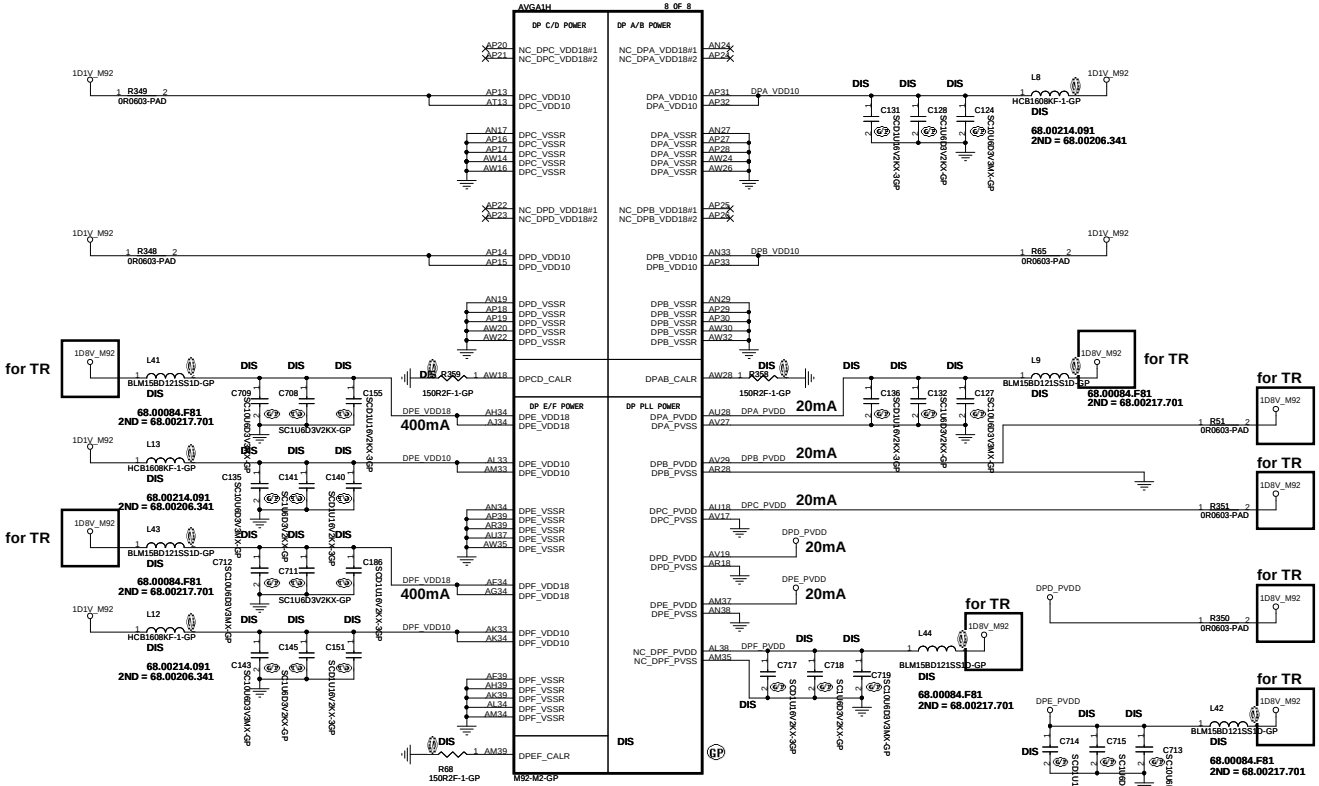
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

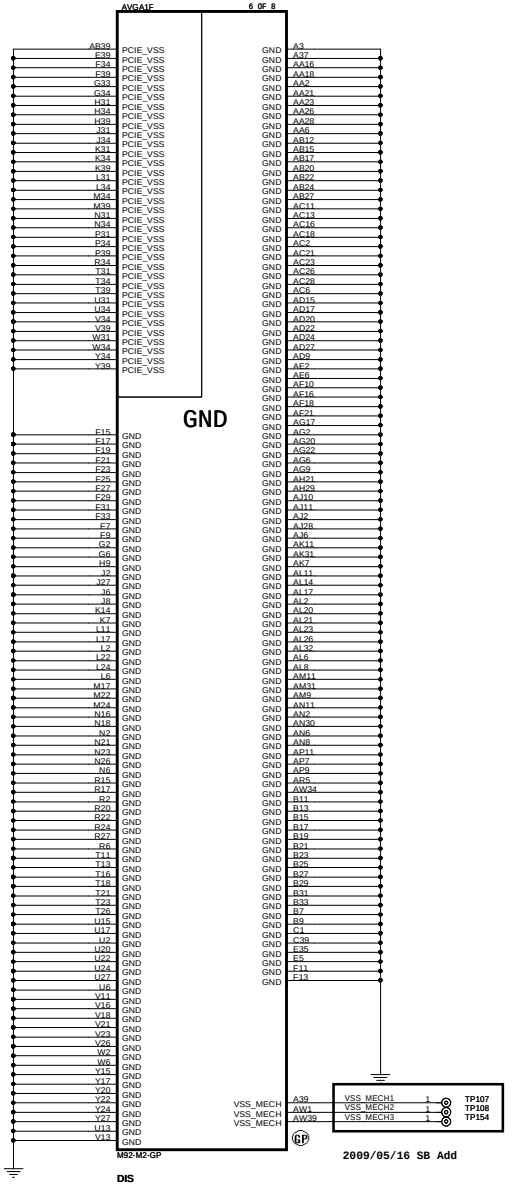
Title: M92 IO
Size: A2 | Document Number: JV71-TR | Rev: SA
Date: Monday, July 06, 2009 | Sheet 53 of 61



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**M92 POWER**	
Size: A2	Document Number: **JV71-TR**	Rev: **SA**
Date: Monday, July 06, 2009	Sheet 54 of 61	

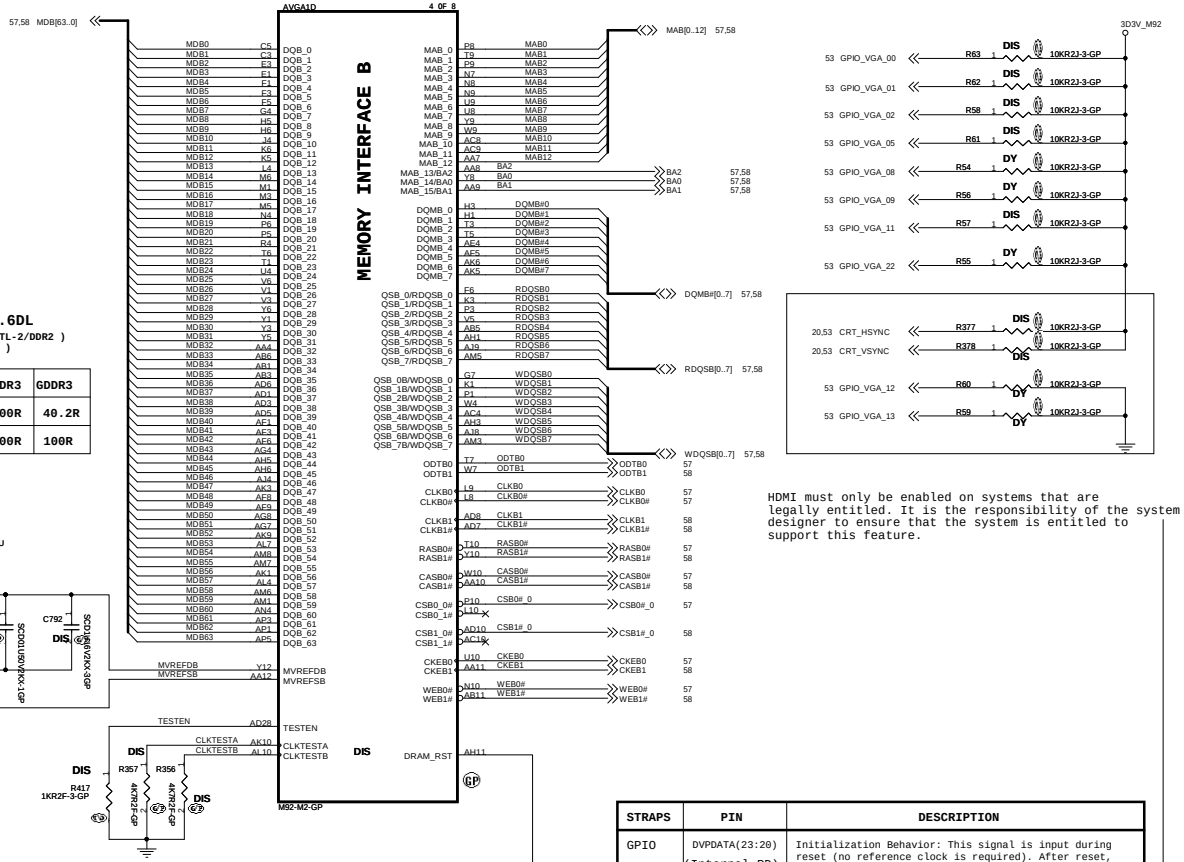




UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**DP POWER_GND**	
Size A2	Document Number **JV71-TR**	Rev **SA**
Date: Monday, July 06, 2009	Sheet 55 of 61	

M92-M2 uses memory group B only



40.2R PN:64.40R25.6DL
(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

DIVIDER RESISTORS	DDR2	DDR3	GDDR3
MVREF TO 1.8V	100R	100R	40.2R
MVREF TO GND	100R	100R	100R

HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Memory / Straps

Size: A2 | Document Number: JV71-TR | Rev: SA

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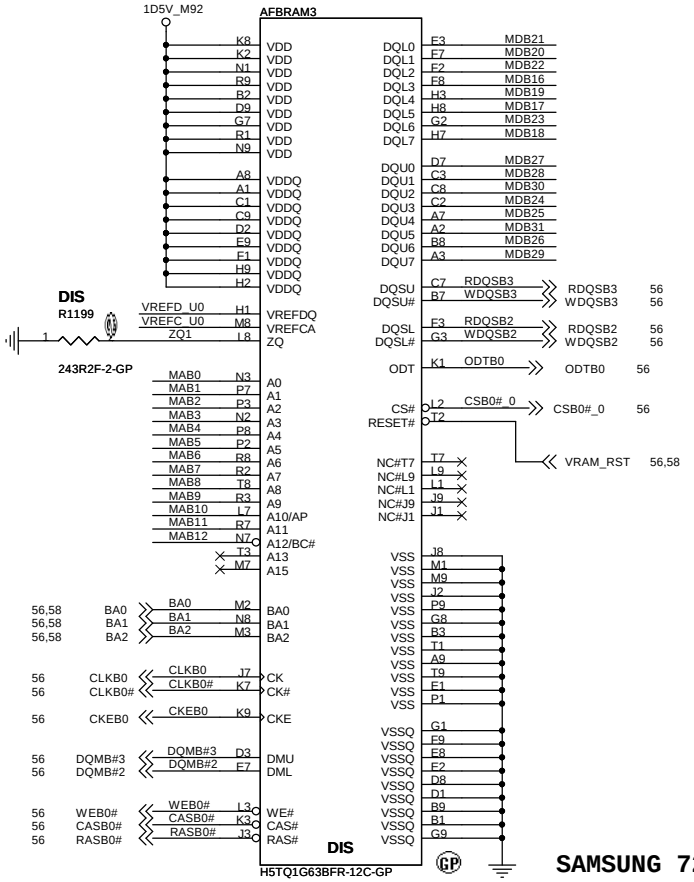
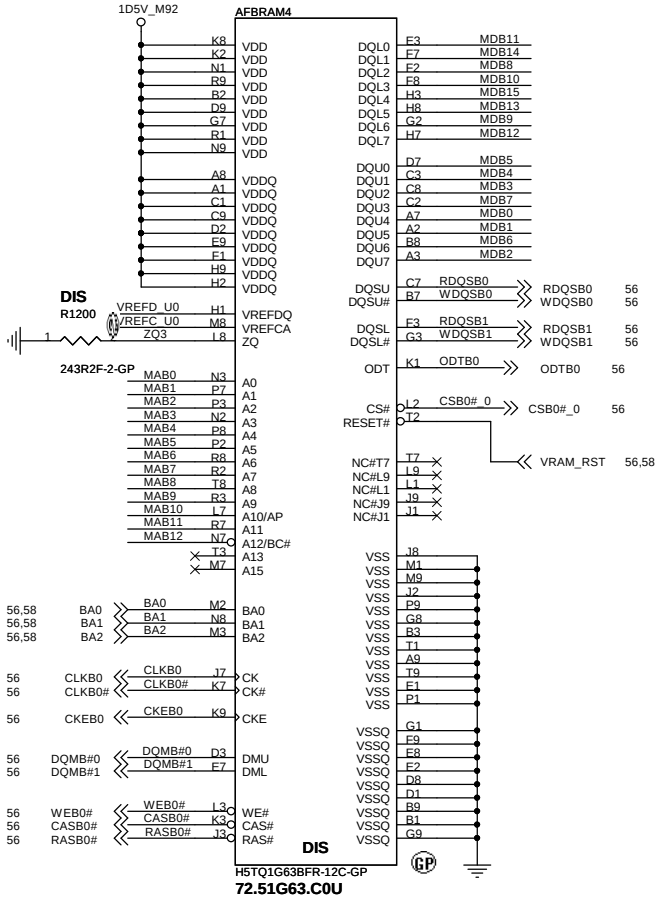
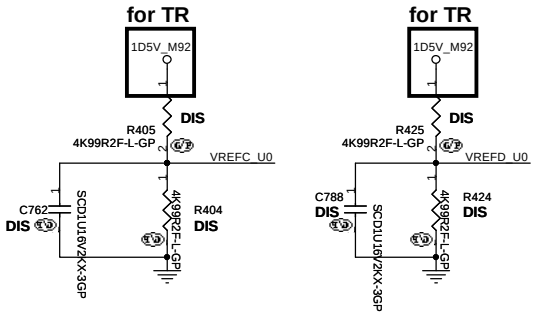
DDR3

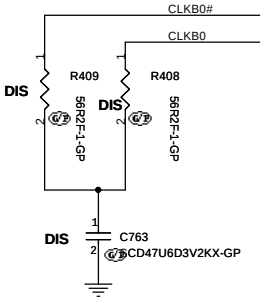


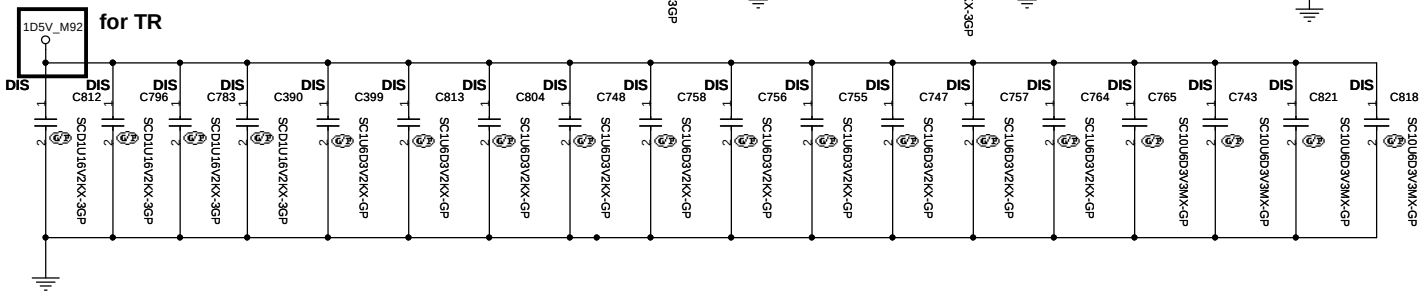


SAMSUNG 72.41164.H0U
HYUNIX 72.51G63.C0U

56,58 DQMB#[0..7]
56,58 RDQSB[0..7]
56,58 WDQSB[0..7]
56,58 MAB[0..12]
56,58 MDB[63..0]

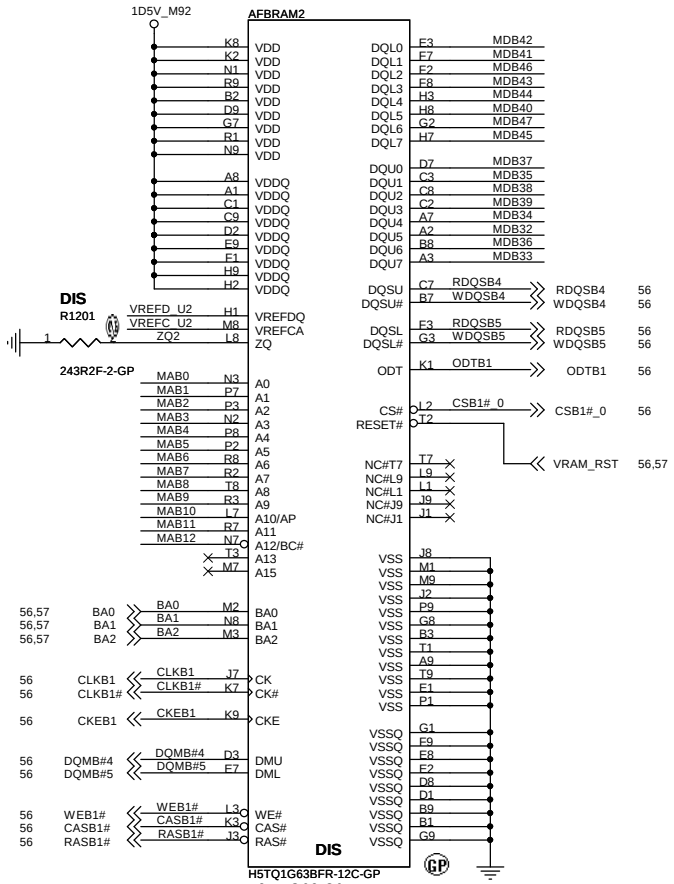


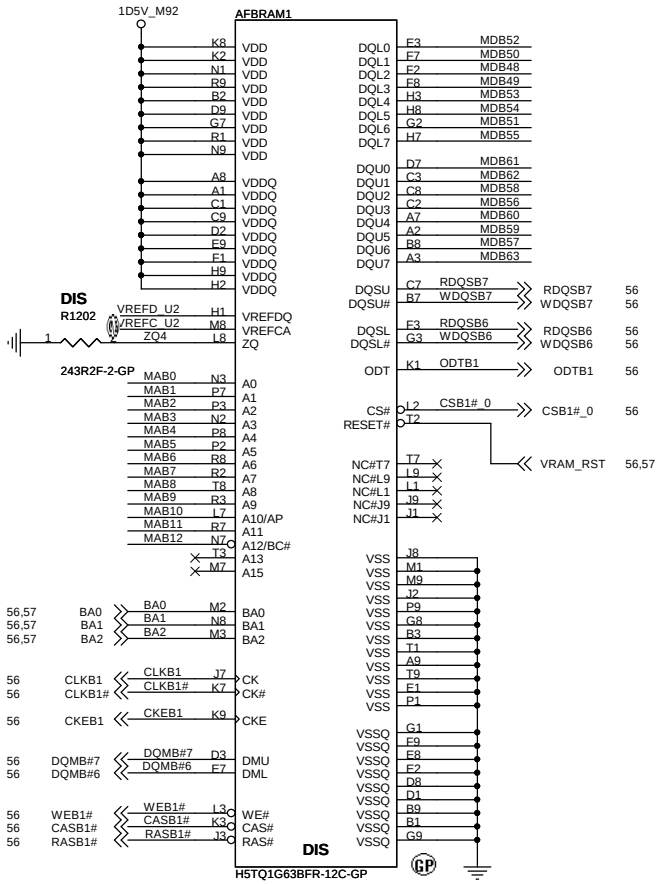




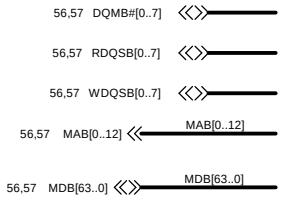
UMA

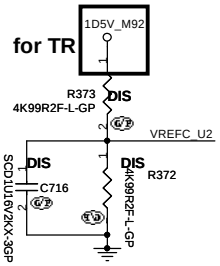
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR3 B0		
Size: A3	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 57 of 61	

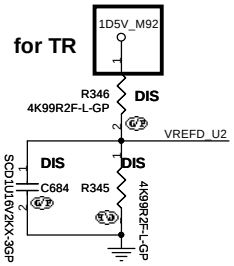


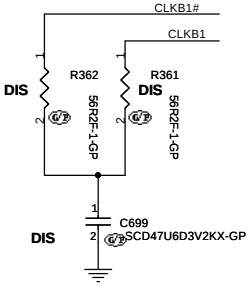


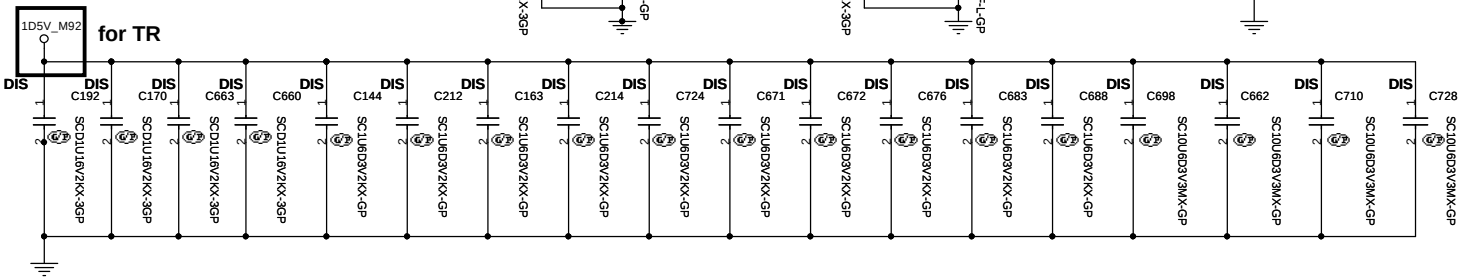
SAMSUNG 72.41164.H0U
HYUNIX 72.51G63.C0U





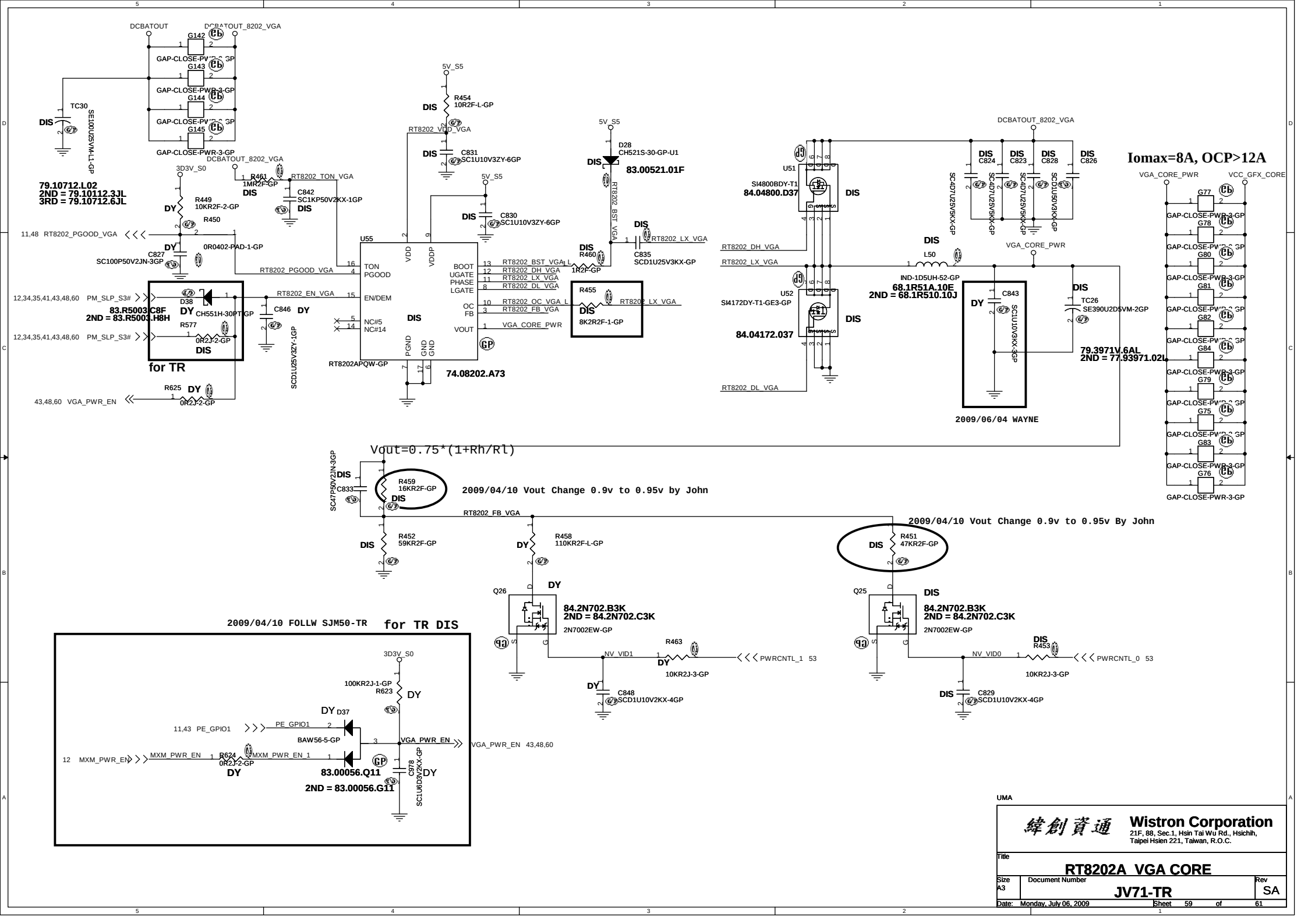






UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 DDR3 B1		
Size: A3	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 58 of 61	


DCBATOUT
DCBATOUT_8202_VGA
G142
G143
G144
G145
GAP-CLOSE-PWR-3-GP
TC30
SE100U25VM-L1-GP
DIS
79.10712.L02
2ND = 79.10112.3JL
3RD = 79.10712.6JL
3D3V_S0
R461
1MR2F-GP
RT8202_TON_VGA
C842
SC1KP50V2KX-1GP
R449
10KR2F-2-GP
DY
R450
0R0402-PAD-1-GP
11,48 RT8202_PGOOD_VGA
C827
SC100P50V2JN-3GP
5V_S5
R454
10R2F-L-GP
RT8202_VDD_VGA
C831
SC1U10V3ZY-6GP
C830
SC1U10V3ZY-6GP
U55
TON
PGOOD
VDD
VDDP
BOOT
UGATE
PHASE
LGATE
OC
FB
VOUT
NC#5
NC#14
EN/DEM
PGND
GND
RT8202_BST_VGA
RT8202_DH_VGA
RT8202_LX_VGA
RT8202_DL_VGA
RT8202_OC_VGA_L
RT8202_FB_VGA
VGA_CORE_PWR
RT8202_EN_VGA
RT8202APQW-GP
74.08202.A73
D28
CH521S-30-GP-U1
83.00521.01F
RT8202_BST_VGA
C835
SCD1U25V3KX-GP
R460
1R2F-GP
R455
8K2R2F-1-GP
12,34,35,41,43,48,60 PM_SLP_S3#
D38
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
R577
0R2J-2-GP
for TR
C846
SCD1U25V3ZY-1GP
R625
43,48,60 VGA_PWR_EN
U51
SI4800BDY-T1
84.04800.D37
U52
SI4172DY-T1-GE3-GP
84.04172.037
SC407U25V5KX-GP
SCD1U50V3KX-GP
L50
IND-1D5UH-52-GP
68.1R51A.10E
2ND = 68.1R510.10J
C843
SC1U10V3KX-3GP
TC26
SE390U2D5VM-2GP
79.3971V.6AL
2ND = 77.93971.02L
2009/06/04 WAYNE
Iomax=8A, OCP>12A
VGA_CORE_PWR
VCC_GFX_CORE
G77
G78
G80
G81
G82
G84
G79
G75
G83
G76
Vout=0.75*(1+Rh/Rl)
SC47P50V2JN-3GP
C833
R459
16KR2F-GP
2009/04/10 Vout Change 0.9v to 0.95v by John
R452
59KR2F-GP
R458
110KR2F-L-GP
Q26
84.2N702.B3K
2ND = 84.2N702.C3K
2N7002EW-GP
R463
10KR2J-3-GP
C848
SCD1U10V2KX-4GP
NV_VID1
PWRCNTL_1 53
2009/04/10 Vout Change 0.9v to 0.95v By John
R451
47KR2F-GP
Q25
84.2N702.B3K
2ND = 84.2N702.C3K
2N7002EW-GP
R453
10KR2J-3-GP
C829
SCD1U10V2KX-4GP
NV_VID0
PWRCNTL_0 53
2009/04/10 FOLLW SJM50-TR
for TR DIS
100KR2J-1-GP
R623
D37
BAW56-5-GP
11,43 PE_GPIO1
VGA_PWR_EN
VGA_PWR_EN 43,48,60
12 MXM_PWR_EN
R624
0R2J-2-GP
83.00056.Q11
2ND = 83.00056.G11
C978
SC1U6D3V2KX-GP
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8202A VGA CORE
Size
A3
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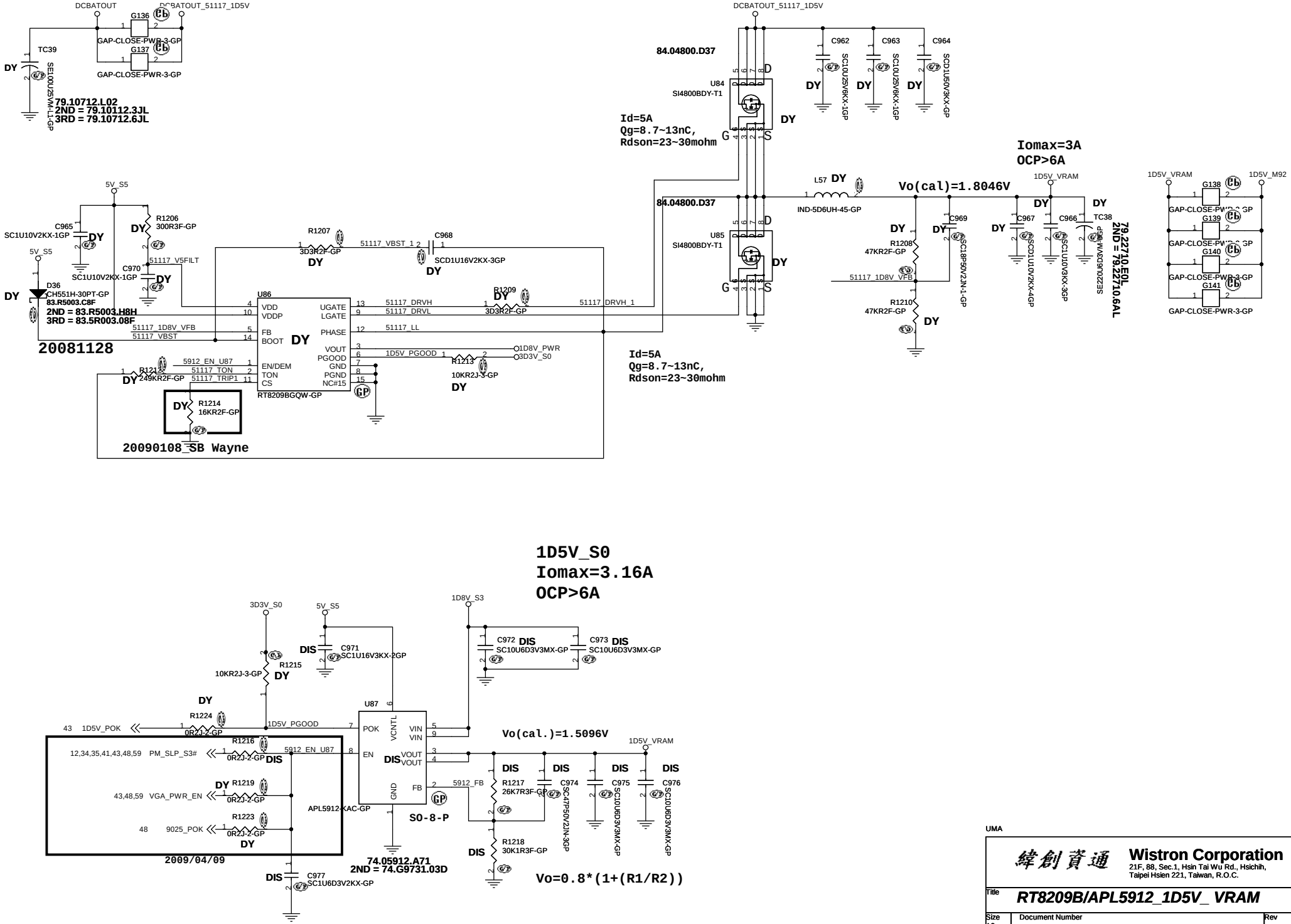
DCBATOUT
DCBATOUT_51117_1D5V
G136
GAP-CLOSE-PWR-3-GP
G137
GAP-CLOSE-PWR-3-GP
TC39
DY
SE100U25VM-LL-GP
79.10712.L02
2ND = 79.10112.3JL
3RD = 79.10712.6JL
DCBATOUT_51117_1D5V
84.04800.D37
U84
SI4800BDY-T1
C962
C963
C964
SC10U25V6KX-1GP
SC10U25V6KX-1GP
SCD1U50V3KX-GP
Id=5A
Qg=8.7~13nC,
Rdson=23~30mohm
Iomax=3A
OCP>6A
L57
IND-5D6UH-45-GP
Vo(cal)=1.8046V
1D5V_VRAM
84.04800.D37
U85
SI4800BDY-T1
C969
SC18P50V2JN-1-GP
C967
C966
TC38
SCD1U10V2KX-4GP
SC1U10V8KX-3GP
A3D6U022SE
79.22710.E0L
2ND = 79.22710.6AL
R1208
47KR2F-GP
51117_1D8V_VFB
R1210
47KR2F-GP
1D5V_VRAM
1D5V_M92
G138
G139
G140
G141
GAP-CLOSE-PWR-3-GP
GAP-CLOSE-PWR-3-GP
GAP-CLOSE-PWR-3-GP
GAP-CLOSE-PWR-3-GP
5V_S5
C965
SC1U10V2KX-1GP
R1206
300R3F-GP
C970
SC1U10V2KX-1GP
51117_V5FILT
D36
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3RD = 83.5R003.08F
20081128
R1207
3D3R2F-GP
51117_VBST_1
C968
SCD1U16V2KX-3GP
R1209
3D3R2F-GP
51117_DRVH_1
U86
VDD
VDDP
FB
BOOT
EN/DEM
TON
CS
UGATE
LGATE
PHASE
VOUT
PGOOD
GND
PGND
NC#15
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51117_DRVL
51117_LL
51117_1D8V_VFB
51117_VBST
5912_EN_U87
51117_TON
51117_TRIP1
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1D8V_PWR
3D3V_S0
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249KR2F-GP
R1213
10KR2J-3-GP
R1214
16KR2F-GP
RT8209BGQW-GP
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Rdson=23~30mohm
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Iomax=3.16A
OCP>6A
3D3V_S0
5V_S5
1D8V_S3
C971
SC1U16V3KX-2GP
C972
SC10U6D3V3MX-GP
C973
SC10U6D3V3MX-GP
R1215
10KR2J-3-GP
R1224
0R2J-2-GP
R1216
0R2J-2-GP
R1219
0R2J-2-GP
R1223
0R2J-2-GP
43 1D5V_POK
12,34,35,41,43,48,59 PM_SLP_S3#
43,48,59 VGA_PWR_EN
48 9025_POK
5912_EN_U87
1D5V_PGOOD
U87
POK
EN
GND
VCNTL
VIN
VOUT
FB
APL5912-KAC-GP
SO-8-P
Vo(cal.)=1.5096V
1D5V_VRAM
R1217
26K7R3F-GP
R1218
30K1R3F-GP
C974
SC47P50V2JN-3GP
C975
SC10U6D3V3MX-GP
C976
SC10U6D3V3MX-GP
5912_FB
C977
SC1U6D3V2KX-GP
74.05912.A71
2ND = 74.G9731.03D
Vo=0.8*(1+(R1/R2))
2009/04/09
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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