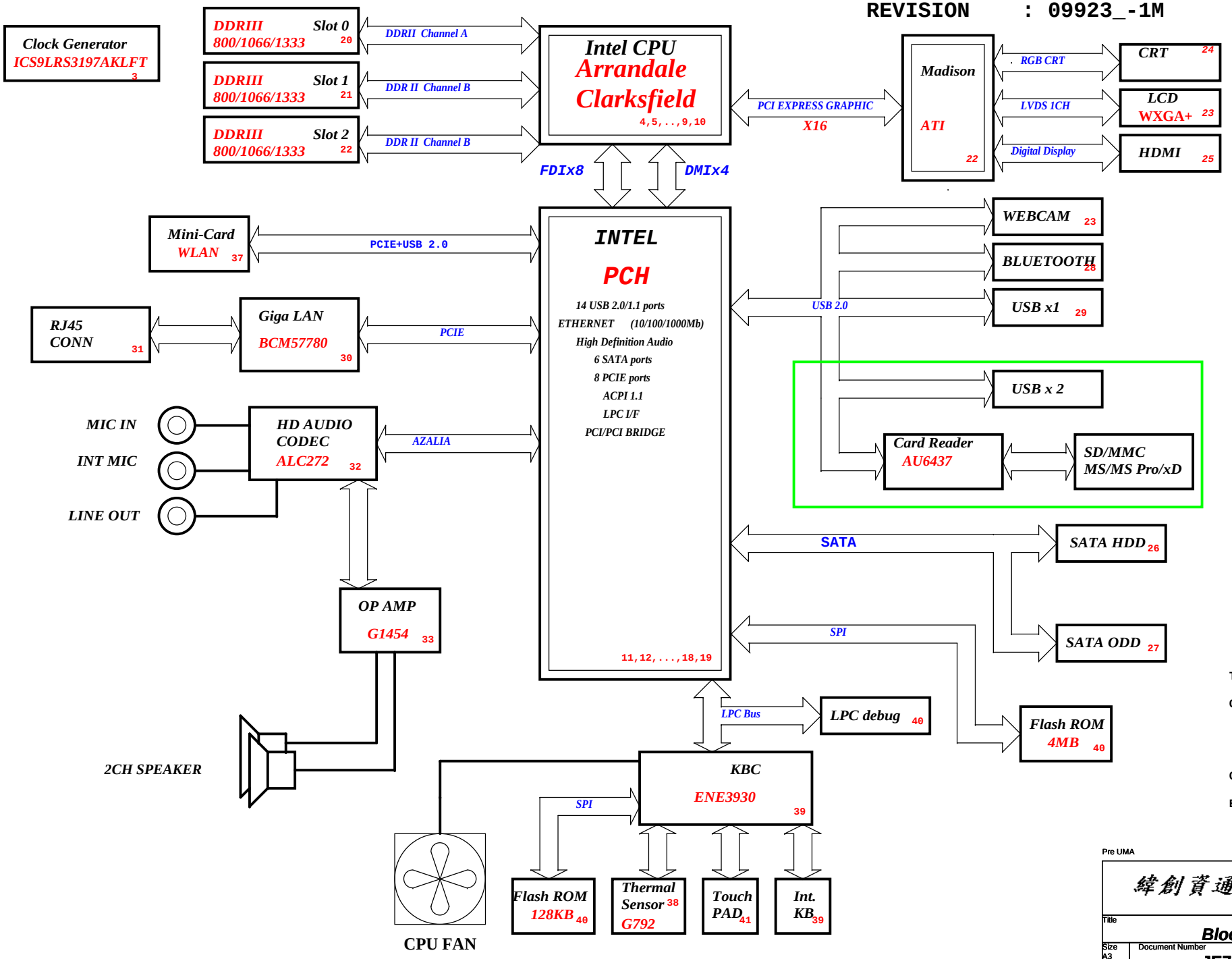
JE70-CP Block Diagram

Project code: 91.4HN01.001
PCB P/N : 48.4HN01.0SD
REVISION : 09923_-1M



SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 47

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 48

SYSTEM DC/DC RT8209B	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 49

SYSTEM DC/DC TPS51611	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE 52

CPU DC/DC TPS51621	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 45,46

MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
DCBATOUT	BT+ 51

PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

Pre UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

Pre UMA

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Title: Table of Content

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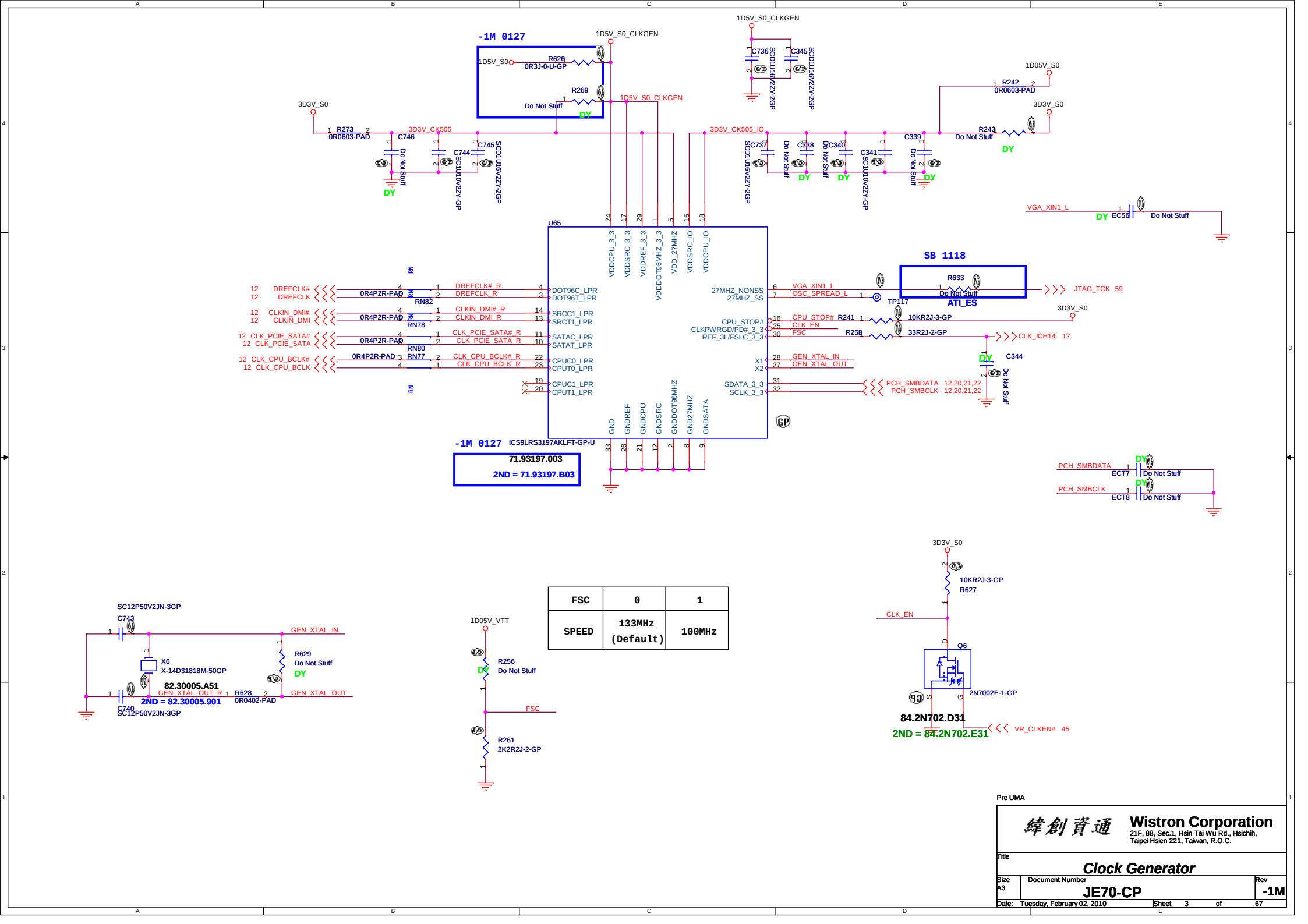

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: **Clock Generator**

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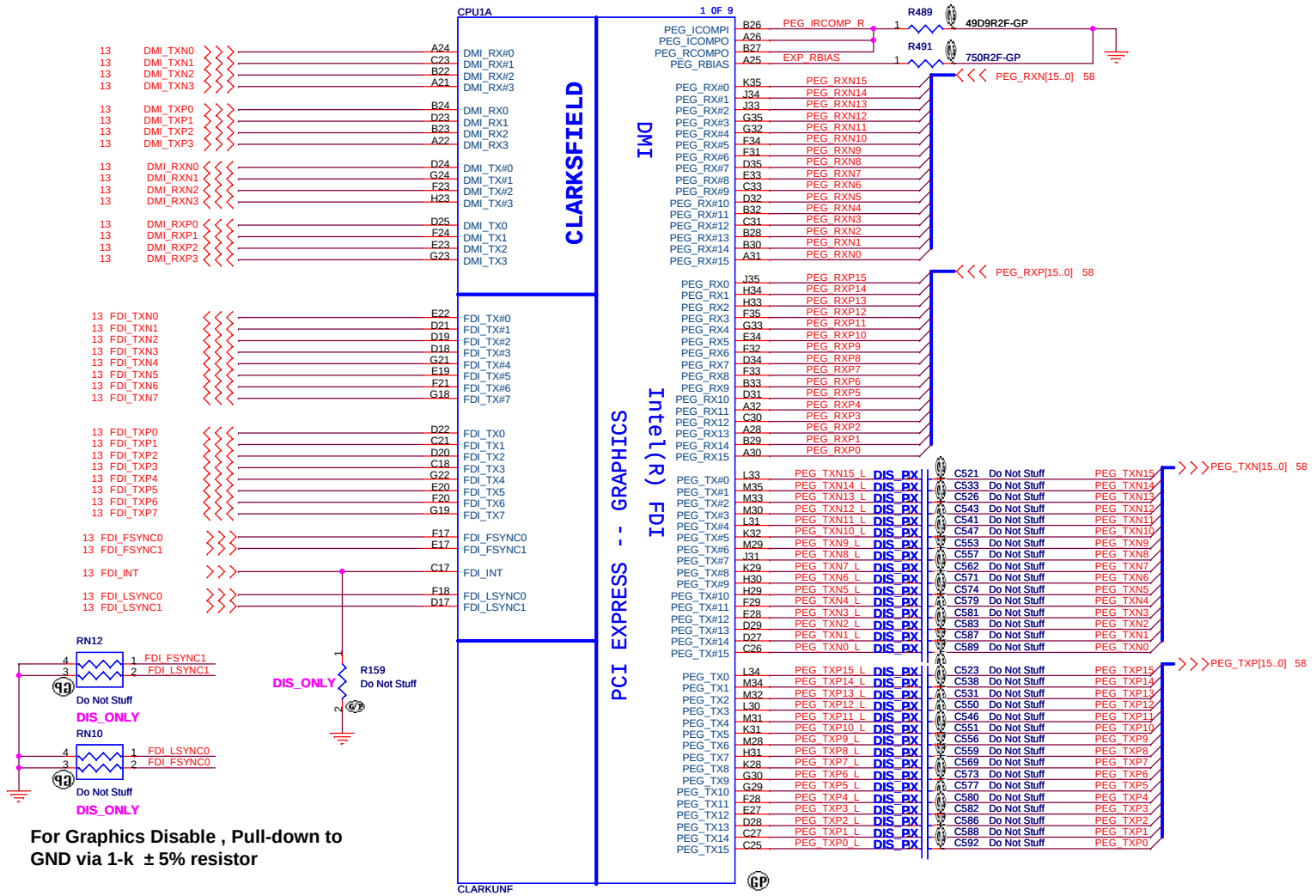

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Title: CPU (1/7)

Size	Document Number	Rev
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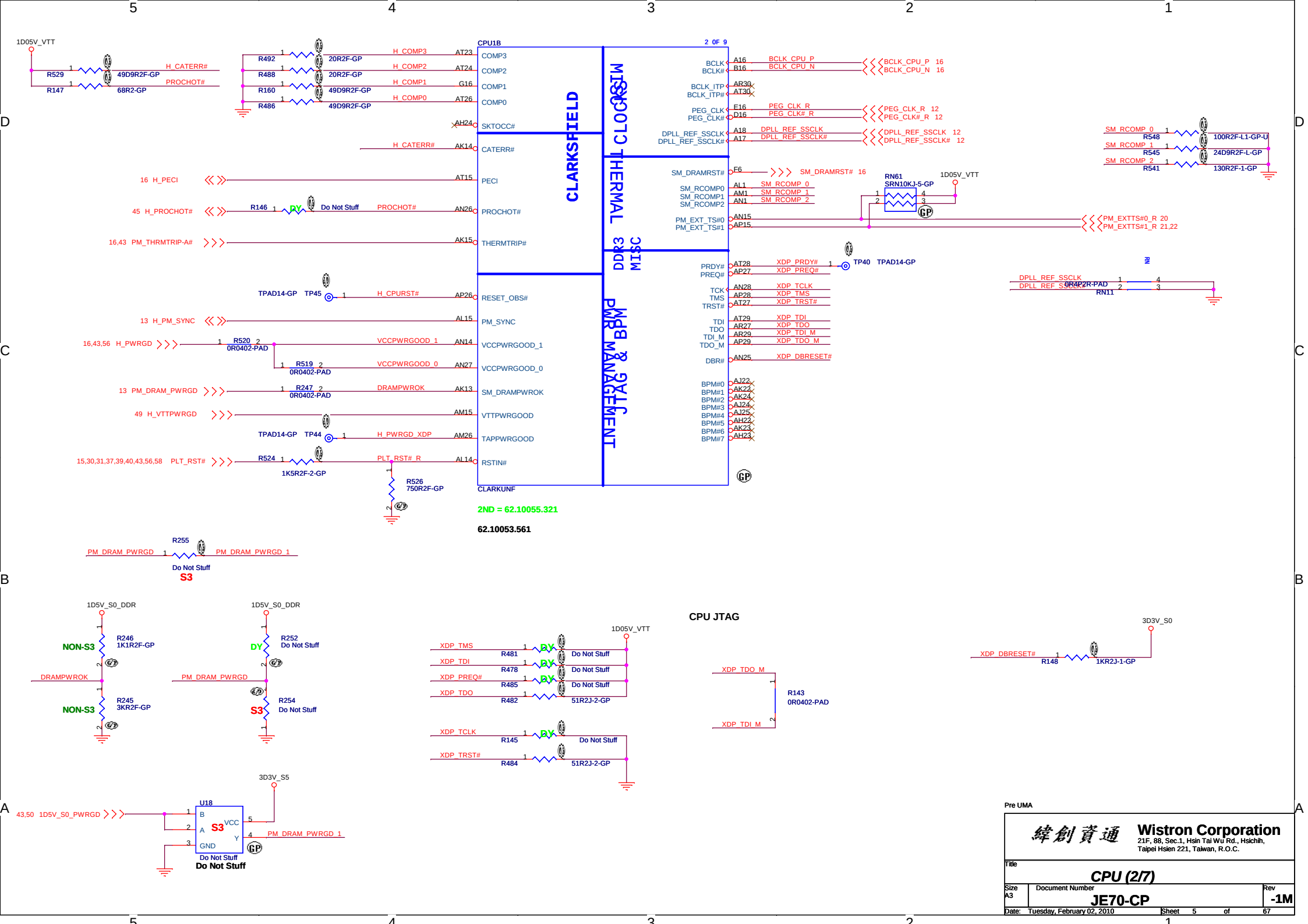

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Title: CPU (2/7)

Size	Document Number	Rev
A3	JE70-CP	-1M

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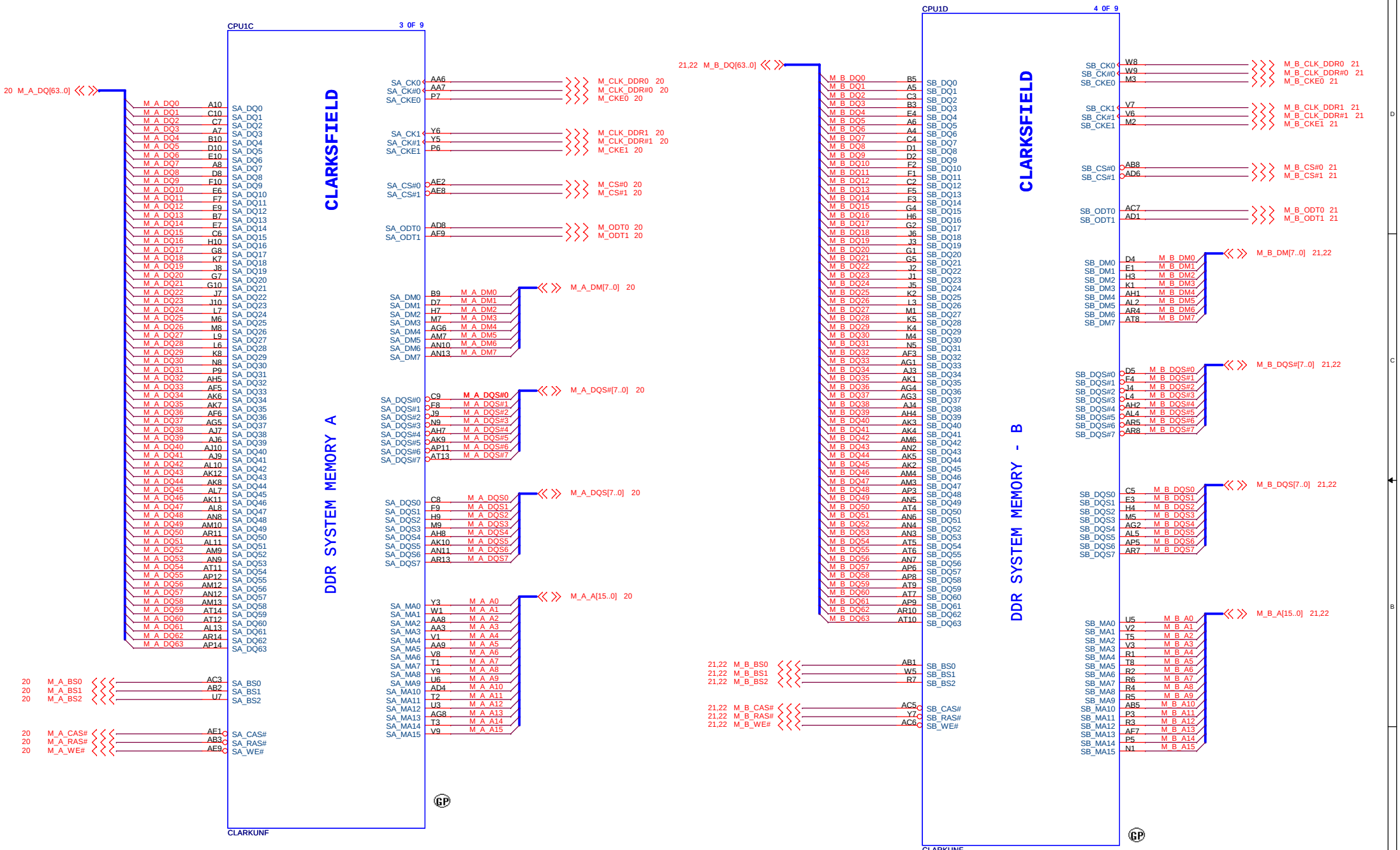

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Title: CPU (3/7)	
Size: A3	Document Number: JE70-CP
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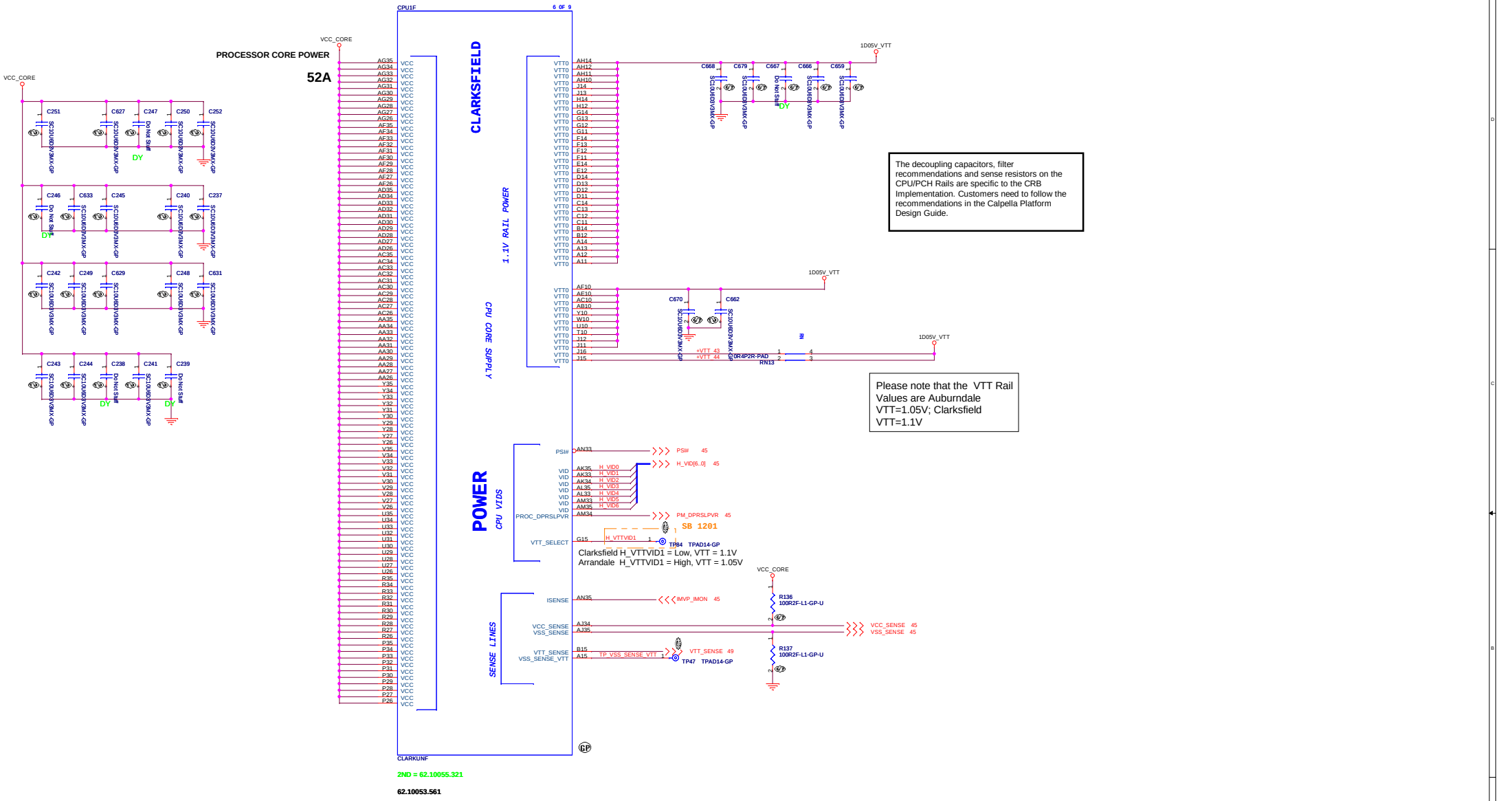

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Title	CPU (4/7)
Size A2	Document Number JE70-CP
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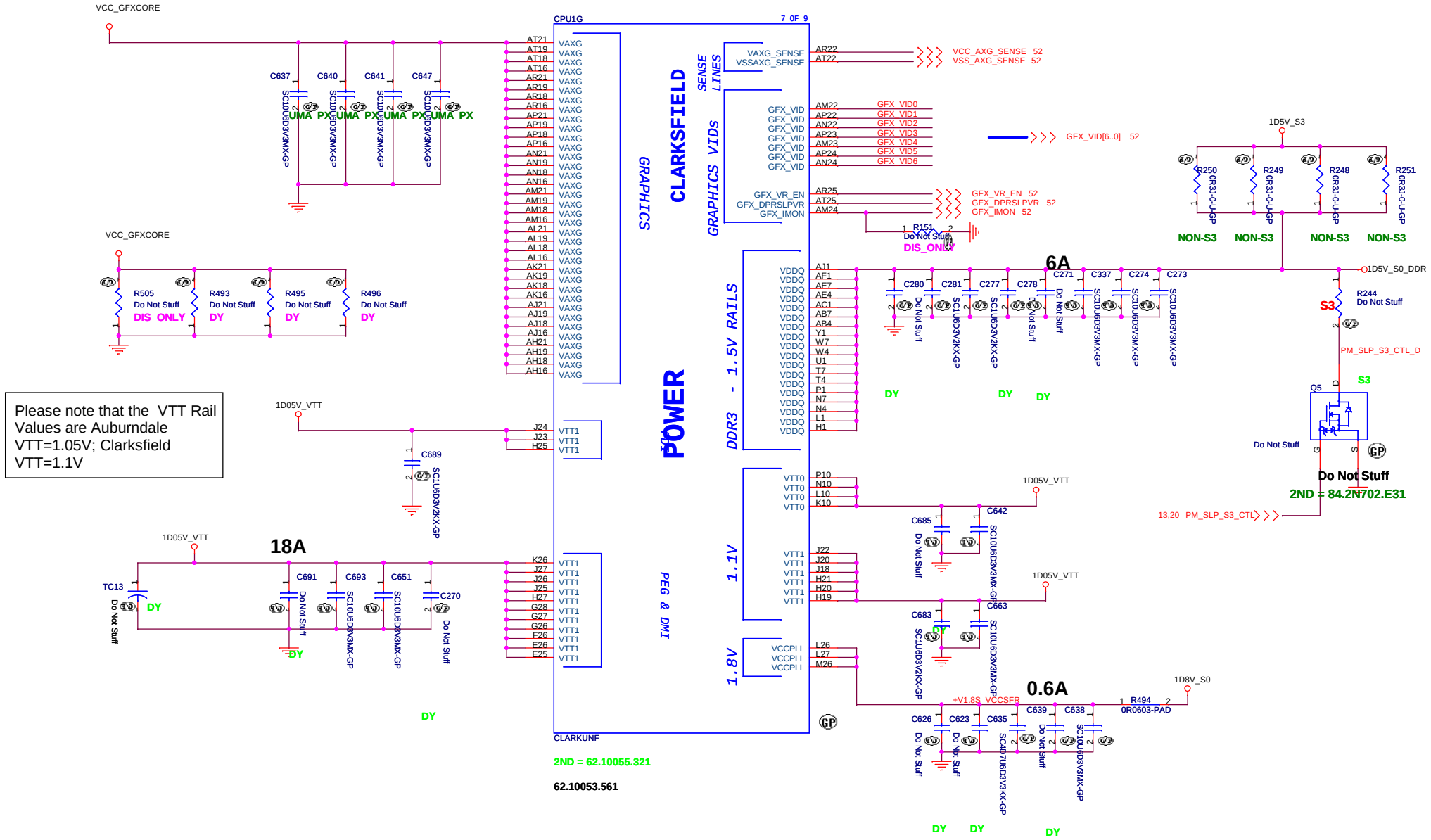
CPU1G
7 0F 9
CLARKSFIELD
GRAPHICS
POWER
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
1.1V
1.8V
PEG & DMI
CLARKUNF
VCC_GFXCORE
UMA_PX
DIS_ONLY
DY
Do Not Stuff
1D05V_VTT
18A
6A
0.6A
1D8V_S0
1D5V_S3
1D5V_S0_DDR
NON-S3
S3
PM_SLP_S3_CTL_D
PM_SLP_S3_CTL
Do Not Stuff
2ND = 84.2N702.E31
2ND = 62.10055.321
62.10053.561
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
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Title
CPU (5/7)
Size A3
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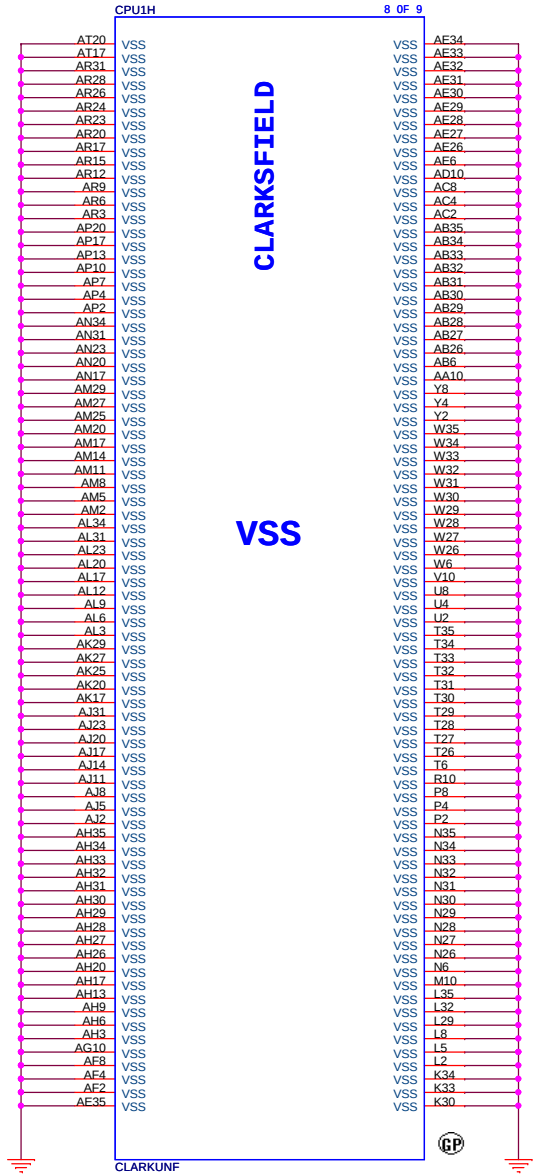

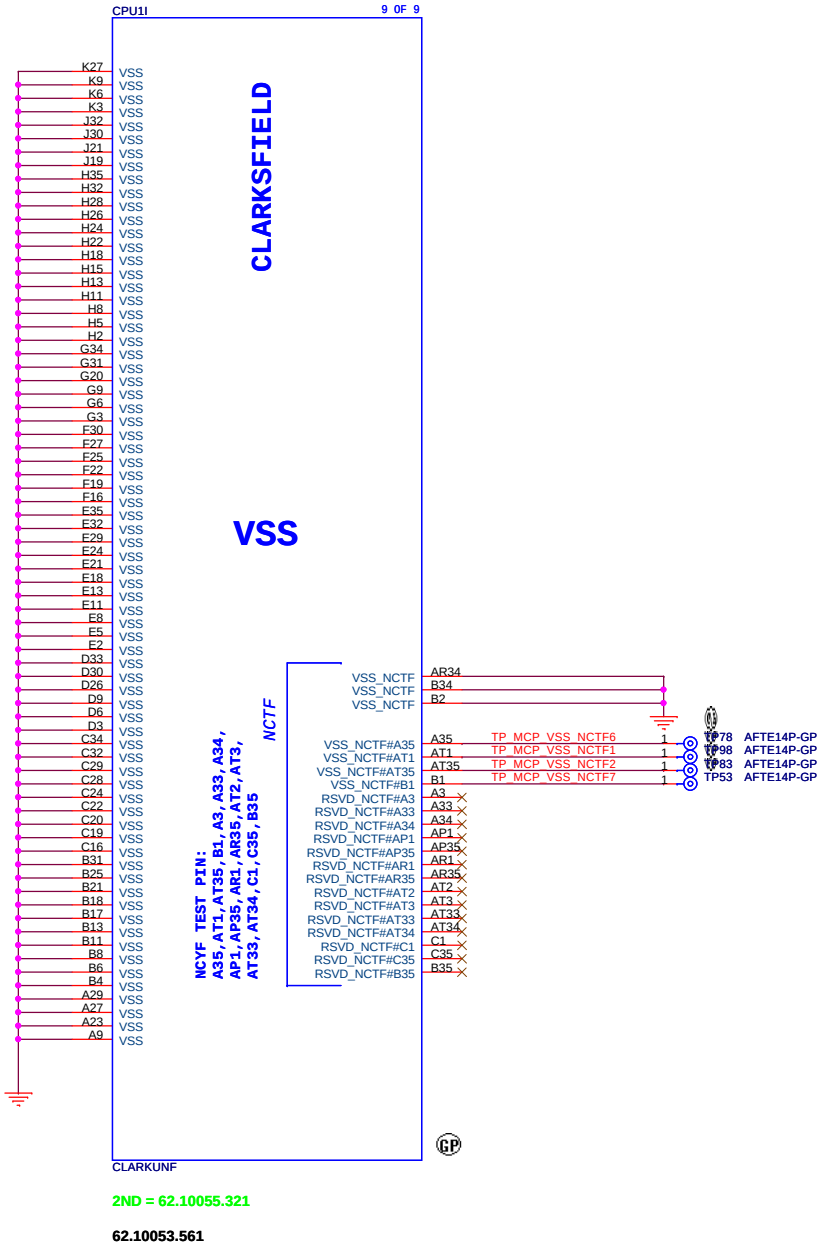

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Title: ***CPU (6/7)***

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SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor

DY
RN33
20 M_VREF_DQ_DIMM0
21 M_VREF_DQ_DIMM1
H_RSVD9_R
H_RSVD10_R
Do Not Stuff
GP

CPU1E
5 0F 9
CLARKSFIELD
RESERVED
CLARKUNF

AP25 RSVD#AP25
AL25 RSVD#AL25
AL24 RSVD#AL24
AL22 RSVD#AL22
AJ33 RSVD#AJ33
AG9 RSVD#AG9
M27 RSVD#M27
L28 RSVD#L28
J17 SA_DIMM_VREF
H17 SB_DIMM_VREF
G25 RSVD#G25
G17 RSVD#G17
E31 RSVD#E31
E30 RSVD#E30

RSVD#AJ13 AJ13
RSVD#AJ12 AJ12
RSVD#AH25 AH25
RSVD#AK26 AK26
RSVD#AL26 AL26
RSVD_NCTF_37 AR2
RSVD#AJ26 AJ26
RSVD#AJ27 AJ27

RSVD#AL28 AL28
RSVD#AL29 AL29
RSVD#AP30 AP30
RSVD#AP32 AP32
RSVD#AL27 AL27
RSVD#AT31 AT31
RSVD#AT32 AT32
RSVD#AP33 AP33
RSVD#AR33 AR33

RSVD#AR32 AR32

RSVD_TP#E15 E15
RSVD_TP#F15 F15
KEY A2
RSVD#D15 D15
RSVD#C15 C15
RSVD#AJ15 AJ15
RSVD#AH15 AH15

CFG0 AM30 CFG0
CFG1 AM28 CFG1
CFG2 AP31 CFG2
CFG3 AL32 CFG3
CFG4 AL30 CFG4
CFG5 AM31 CFG5
CFG6 AN29 CFG6
CFG7 AM32 CFG7
CFG8 AK32 CFG8
CFG9 AK31 CFG9
CFG10 AK28 CFG10
CFG11 AJ28 CFG11
CFG12 AN30 CFG12
CFG13 AN32 CFG13
CFG14 AJ32 CFG14
CFG15 AJ29 CFG15
CFG16 AJ30 CFG16
CFG17 AK30 CFG17
H16 RSVD_TP_86

TPAD14-GP TP43
TPAD14-GP TP33
TPAD14-GP TP35
TPAD14-GP TP41
TPAD14-GP TP29
TPAD14-GP TP34
TPAD14-GP TP42
TPAD14-GP TP39
TPAD14-GP TP38
TPAD14-GP TP31
TPAD14-GP TP30
TPAD14-GP TP36
TPAD14-GP TP32
TPAD14-GP TP37

RN
0R4P2R-PAD
RN55
H_RSVD17_R
H_RSVD18_R

B19 RSVD#B19
A19 RSVD#A19
A20 RSVD#A20
B20 RSVD#B20
U9 RSVD#U9
T9 RSVD#T9
AC9 RSVD#AC9
AB9 RSVD#AB9
J29 RSVD#J29
J28 RSVD#J28

RSVD64_R
RSVD64_P
0R4P2R-PAD
RN58

SA_CK2 AA5
SA_CK#2 AA4
SA_CKE2 R8
SA_CS#2 AD3
SA_ODT2 AD2
SA_CK3 AA2
SA_CK#3 AA1
SA_CKE3 R9
SA_CS#3 AG7
SA_ODT3 AE3

SB_CK2 V4
SB_CK#2 V5
SB_CKE2 N2
SB_CS#2 AD5
SB_ODT2 AD7
SB_CK3 W3
SB_CK#3 W2
SB_CKE3 N3
SB_CS#3 AE5
SB_ODT3 AD9

SA 1013
M_B_CLK_DDR2 22
M_B_CLK_DDR#2 22
M_B_CKE2 22
M_B_CS#2 22
M_B_ODT2 22
M_B_CLK_DDR3 22
M_b_CLK_DDR#3 22
M_B_CKE3 22
M_B_CS#3 22
M_B_ODT3 22

VSS AP34
RSVD_VSS
R139
0R0402-PAD

2ND = 62.10055.321

62.10053.561

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

CFG0
R142
Do Not Stuff

CFG3
R141
3KR2F-GP

CFG4
R144
Do Not Stuff

CFG7
R140
Do Not Stuff

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

Pre UMA

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integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

ICH_RTCX1 — R553 10MR2J-L-GP — ICH_RTCX2
X5 — X-32D768KHZ-34GPU — 82.30001.661
C712 SC7P50V2DN-2GP — C709 SC7P50V2DN-2GP
2nd = 82.30001.B21

RTC_AUX_S5 — RN22 SRN20KJ-GP-U — C315 SC1U6D3V2KX-GP
RTC_AUX_S5 — R550 1MR2J-1-GP — SM_INTRUDER#
R551 330KR2F-L-GP — ICH_INTVRMEN

ACZ_RST# — DY ECT3 — Do Not Stuff
ACZ_SYNC — DY ECT5 — Do Not Stuff
ACZ_BIT_CLK — DY ECT4 — Do Not Stuff
ACZ_SDATAOUT — DY ECT6 — Do Not Stuff

C322 SC1U6D3V2KX-GP — G121 GAP-OPEN
SRTCRST# new signal Pin
Close to DM1 connector

33 ACZ_RST#_AUDIO
33 ACZ_SYNC_AUDIO
33 ACZ_BITCLK_AUDIO
33 ACZ_SDATAOUT_AUDIO
SRN33J-4-GP RN20 — ACZ_RST# ACZ_SYNC ACZ_BIT_CLK ACZ_SDATAOUT

1D5V_S0 — R549 DY Do Not Stuff — ACZ_SYNC

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.

NO REBOOT STRAP

3D3V_S0 — R583 DY Do Not Stuff — ACZ_SPKR

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

3D3V_S5
PCH_JTAG_TMS — R592 Do Not Stuff
PCH_JTAG_TDO — R589 DY Do Not Stuff
PCH_JTAG_TDI — R591 DY Do Not Stuff
PCH_JTAG_RST# — R590 DY Do Not Stuff
PCH_JTAG_TMS — R224 Do Not Stuff
PCH_JTAG_TDO — R221 DY Do Not Stuff
PCH_JTAG_TDI — R223 DY Do Not Stuff
PCH_JTAG_RST# — R220 DY Do Not Stuff
PCH_JTAG_TCK — R593 51R2F-2-GP

When unused all JTAG pins may be NC

PCH1A — 1 OF 10

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14
LPC: FWH0/LAD0 D33, FWH1/LAD1 B33, FWH2/LAD2 C32, FWH3/LAD3 A32 — LPC_LAD0 39,40 … LPC_LAD3 39,40
FWH4/LFRAME# C34 — LPC_LFRAME# 39,40
LDRQ0# A34
LDRQ1#/GPIO23 F34 — PCH_GPIO23 — TP52 TPAD14-GP
SERIRQ AB9 — INT_SERIRQ — INT_SERIRQ 39

IHDA: HDA_BCLK A30 — ACZ_BIT_CLK; HDA_SYNC D29 — ACZ_SYNC; SPKR P1 — 33 ACZ_SPKR; HDA_RST# C30 — ACZ_RST#
HDA_SDIN0 G30 — 33 ACZ_SDATAIN0; HDA_SDIN1 F30 — ACZ_SDATAIN1 — TPAD14-GP TP55; HDA_SDIN2 E32 — HDA_SDIN2 — TPAD14-GP TP54; HDA_SDIN3 F32
HDA_SDO B29 — ACZ_SDATAOUT

SATA: HDA_DOCK_EN#/GPIO33 H32 — HDA_DOCK_EN# — R182 0R0402-PAD — 39 ME_UNLOCK#; HDA_DOCK_RST#/GPIO13 J30 — R186 DY Do Not Stuff
SATA0RXN AK7, SATA0RXP AK6, SATA0TXN AK11, SATA0TXP AK9 — SATA_RXN0 27 … SATA_TXP0 27 — **HDD**
SATA1RXN AH6, SATA1RXP AH5, SATA1TXN AH9, SATA1TXP AH8
SATA2RXN AF11, SATA2RXP AF9, SATA2TXN AF7, SATA2TXP AF6
SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AF3, SATA3TXP AF1
SATA4RXN AD9, SATA4RXP AD8, SATA4TXN AD6, SATA4TXP AD5 — SATA_RXN4 28 … SATA_TXP4 28 — **ODD**
SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1
SATAICOMPO AF16, SATAICOMPI AF15 — SATAICOMP — R192 37D4R2F-GP — 1D05V_S0
SATALED# T3 — SATA_LED# — SATA_LED# 42
SATA0GP/GPIO21 Y9 — SATA_DET#0_R
SATA1GP/GPIO19 V1 — SATA_DET#1_R

JTAG: PCH_JTAG_TCK M3 — JTAG_TCK; PCH_JTAG_TMS K3 — JTAG_TMS; PCH_JTAG_TDI K1 — JTAG_TDI; PCH_JTAG_TDO J2 — JTAG_TDO; PCH_JTAG_RST# J4 — TRST#

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

SPI: 40 PCH_SPI_CLK — R239 15R2J-GP — SPI_CLK_R BA2 — SPI_CLK
40 PCH_SPI_CS#0 — R236 15R2J-GP — SPI_CS0_R AV3 — SPI_CS0#
SPI_CS1# AY3
40 PCH_SPI_MOSI — R238 15R2J-GP — SPI_MOSI_R AY1 — SPI_MOSI
40 SPI_MOSO_R — SPI_MOSO_R AV1 — SPI_MISO

IBEXPEAK-M-GP-NF

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
3D3V_S0 — R219 DY Do Not Stuff — SPI_MOSI_R

RTC_AUX_S5 — R339 0R0603-PAD — RTC_PWR_L — D8 BAS40CW-GP — 3D3V_AUX_S5
C459 SC1U10V2ZY-GP
RTC_PWR — R331 1KR2J-1-GP — RTC_BAT — RTC1 BAT-CON2-1-GP-U
83.00040.E81
2nd = 83.00040.M81
62.70001.011
2nd = 62.70001.041

RN26 SRN10KJ-7GP — 3D3V_S0
SATA_DET#0_R
SATA_LED#
SATA_DET#1_R
INT_SERIRQ

Pre UMA

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Title: **PCH (1/9)**

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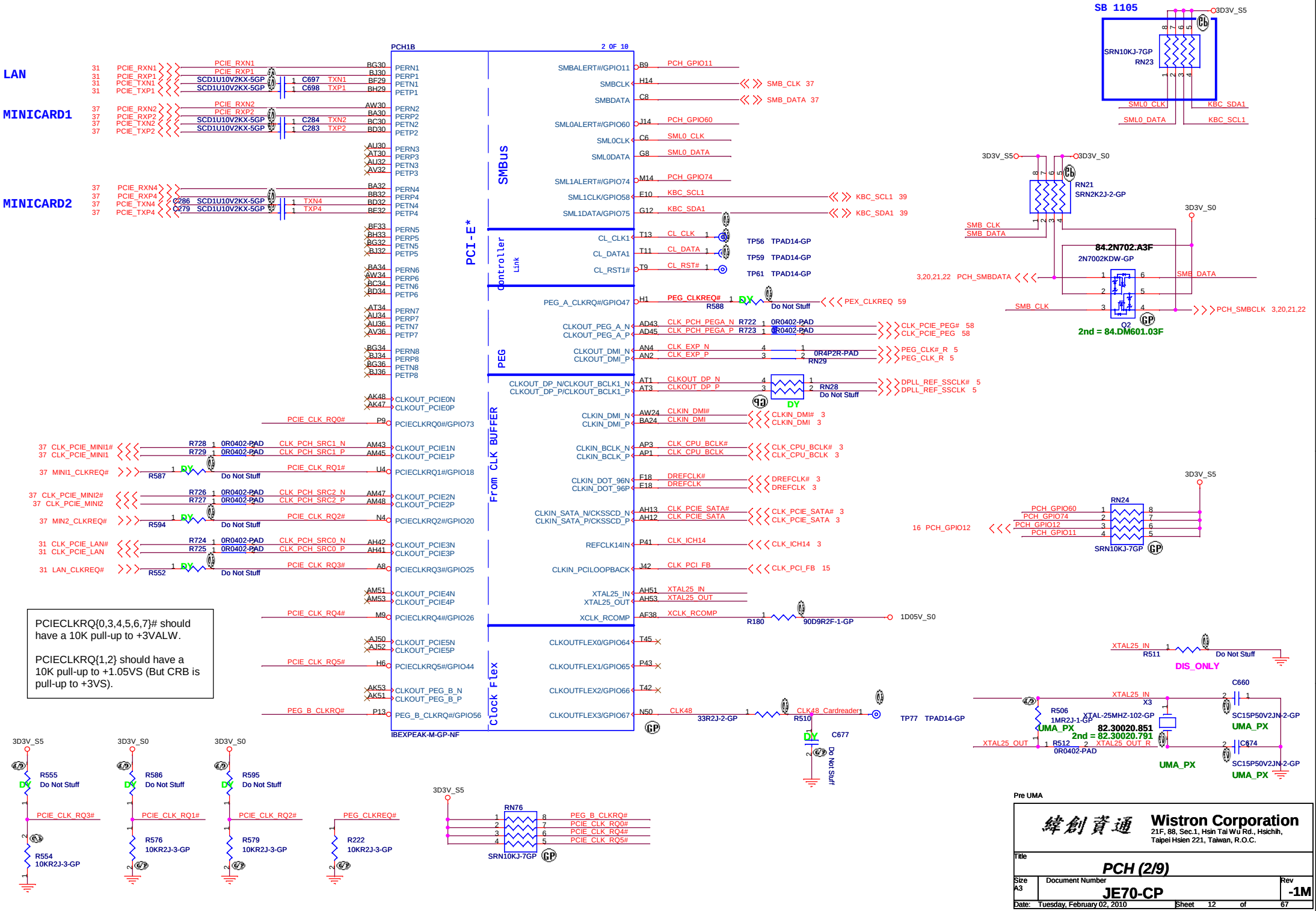
LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
SB 1105
SRN10KJ-7GP
RN23
SML0_CLK
SML0_DATA
KBC_SDA1
KBC_SCL1
RN21
SRN2K2J-2-GP
84.2N702.A3F
2N7002KDW-GP
2nd = 84.DM601.03F
Q2
RN24
SRN10KJ-7GP
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
RN76
SRN10KJ-7GP
XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30020.791
UMA_PX
DIS_ONLY
Do Not Stuff
0R0402-PAD
0R4P2R-PAD
90D9R2F-1-GP
33R2J-2-GP
10KR2J-3-GP
SC15P50V2JN-2-GP
TPAD14-GP
Pre UMA
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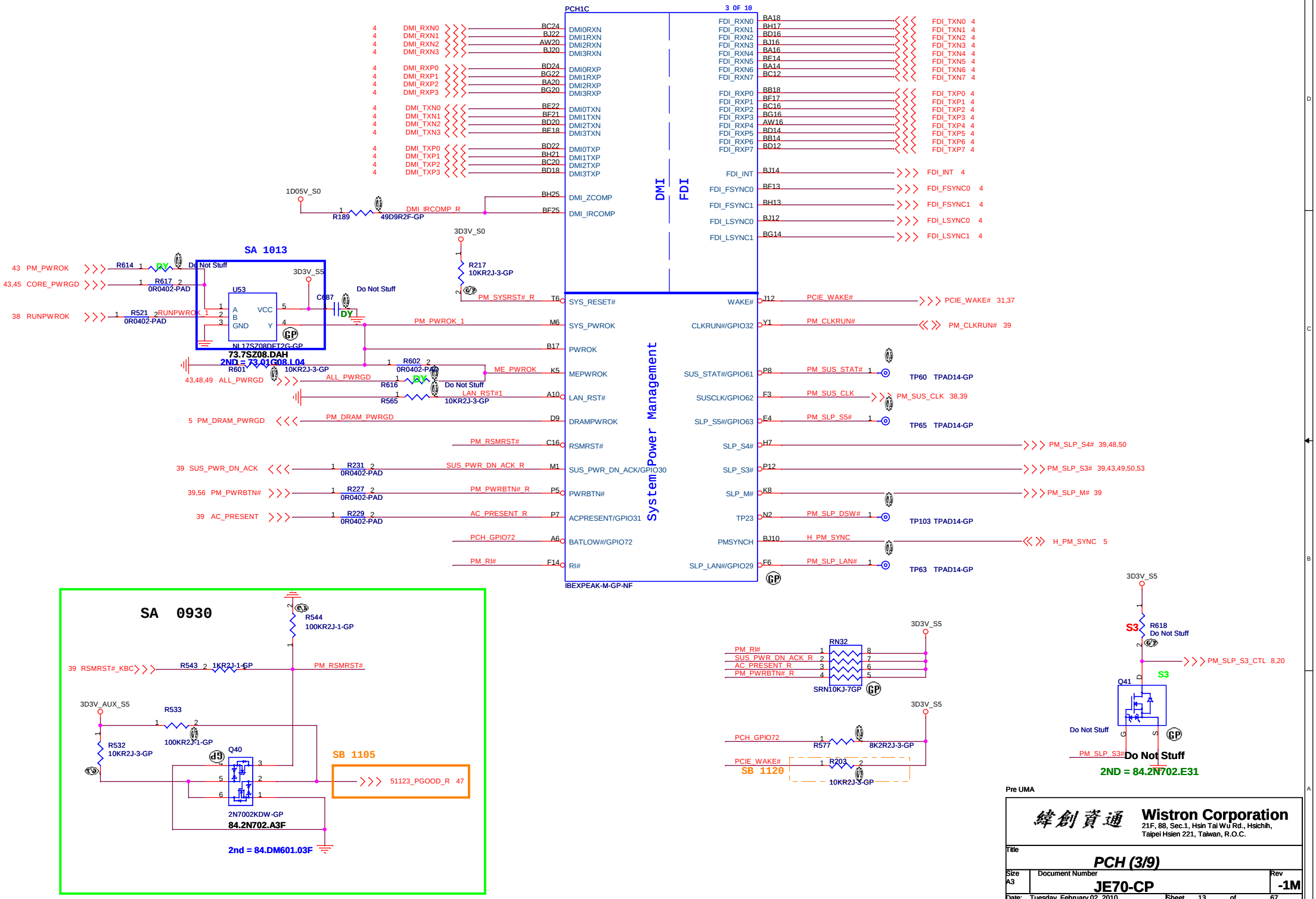
PCH1C
3 OF 10
DMI
FDI
System Power Management
IBEXPEAK-M-GP-NF
SA 1013
SA 0930
SB 1105
SB 1120
Do Not Stuff
73.7SZ08.DAH
2ND = 73.01G08.L04
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
SRN10KJ-7GP
2ND = 84.2N702.E31
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (3/9)
JE70-CP
-1M
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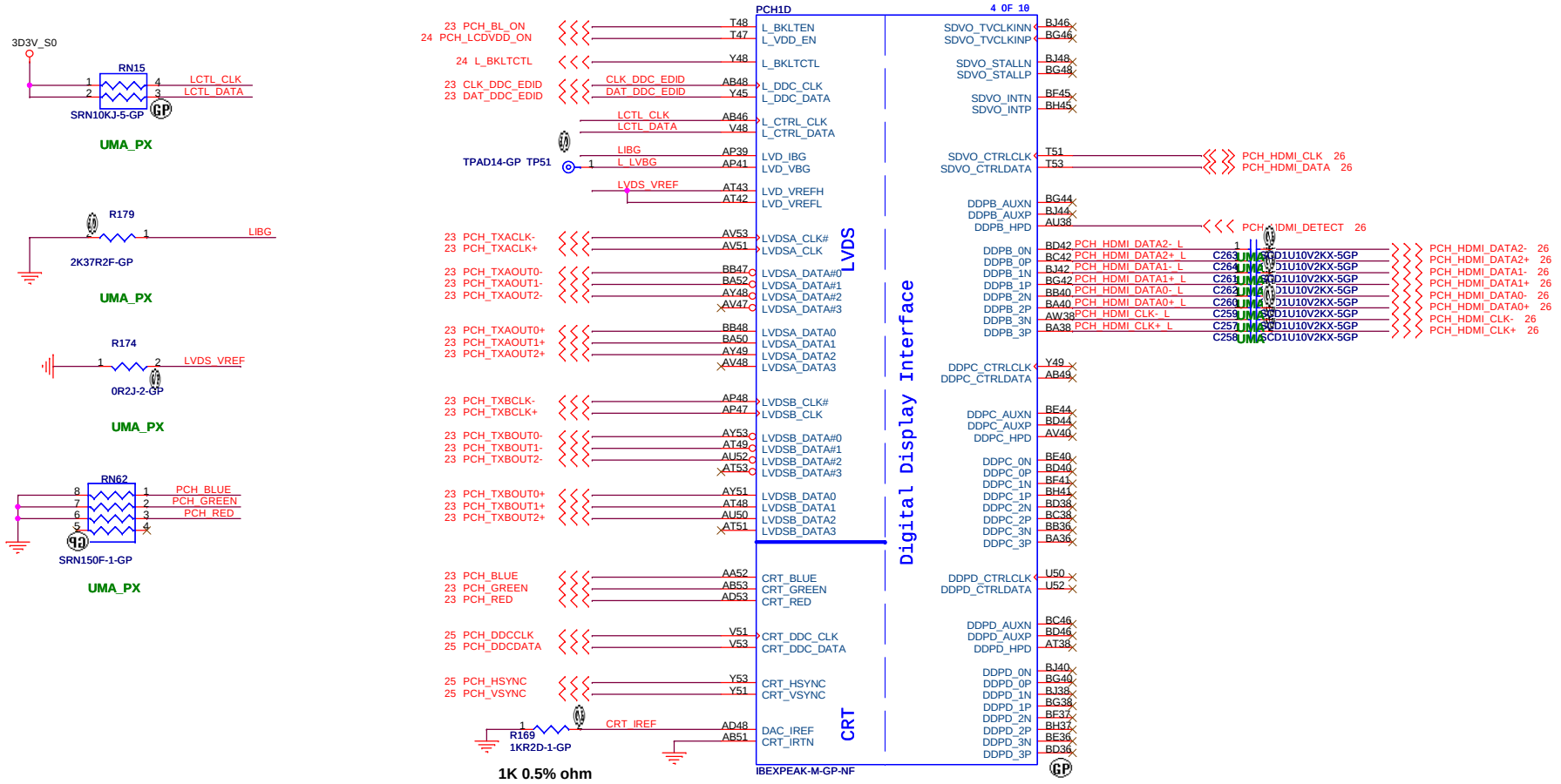

Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (4/9)**

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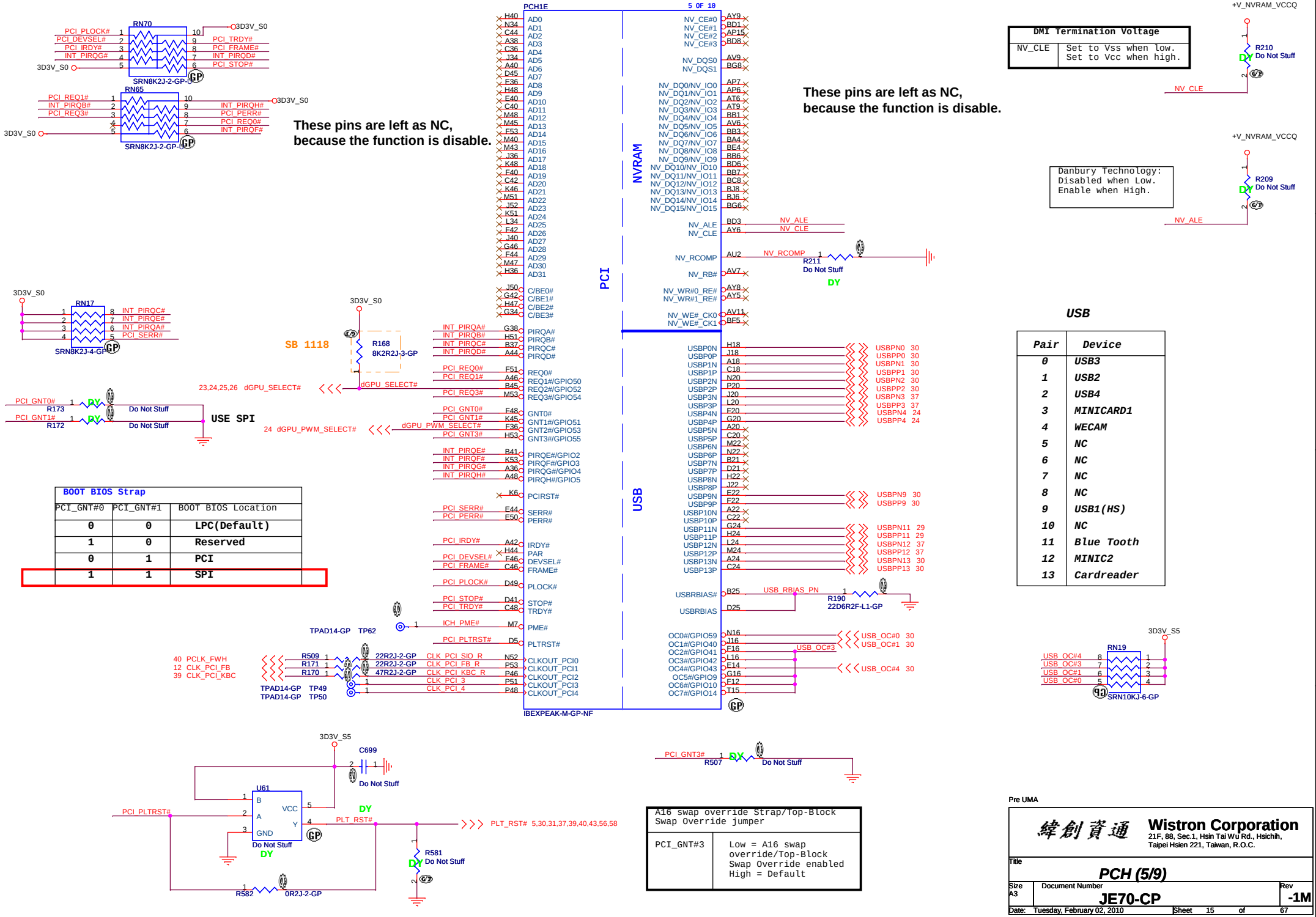
PCH1E
5 OF 10
PCI
NVRAM
USB
IBEXPEAK-M-GP-NF
RN70
SRN8K2J-2-GP-U
RN65
SRN8K2J-2-GP-U
These pins are left as NC, because the function is disable.
These pins are left as NC, because the function is disable.
DMI Termination Voltage
NV_CLE | Set to Vss when low. Set to Vcc when high.
Danbury Technology: Disabled when Low. Enable when High.
R210 Do Not Stuff
R209 Do Not Stuff
R211 Do Not Stuff
RN17
SRN8K2J-4-GP
SB 1118
R168 8K2R2J-3-GP
USE SPI
R173 Do Not Stuff
R172 Do Not Stuff
BOOT BIOS Strap
PCI_GNT#0 | PCI_GNT#1 | BOOT BIOS Location
0 | 0 | LPC(Default)
1 | 0 | Reserved
0 | 1 | PCI
1 | 1 | SPI
USB
Pair | Device
0 | USB3
1 | USB2
2 | USB4
3 | MINICARD1
4 | WECAM
5 | NC
6 | NC
7 | NC
8 | NC
9 | USB1(HS)
10 | NC
11 | Blue Tooth
12 | MINIC2
13 | Cardreader
R190 22D6R2F-L1-GP
RN19
SRN10KJ-6-GP
TPAD14-GP TP62
TPAD14-GP TP49
TPAD14-GP TP50
22R2J-2-GP
47R2J-2-GP
U61
Do Not Stuff
R581 Do Not Stuff
R582 0R2J-2-GP
R507 Do Not Stuff
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled High = Default
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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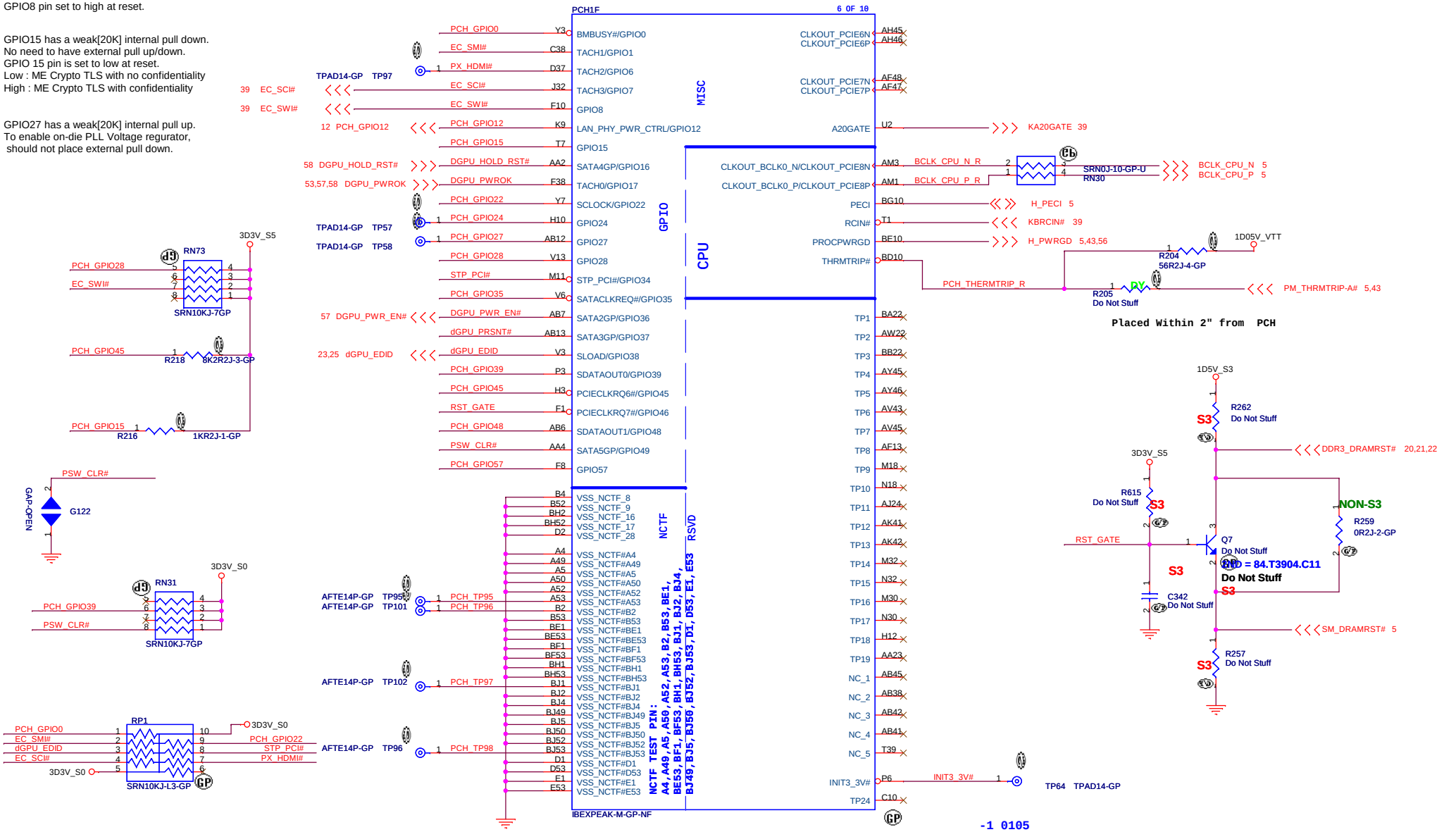
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PCH (6/9)***	
Size A3	Document Number **JE70-CP**	Rev **-1M**
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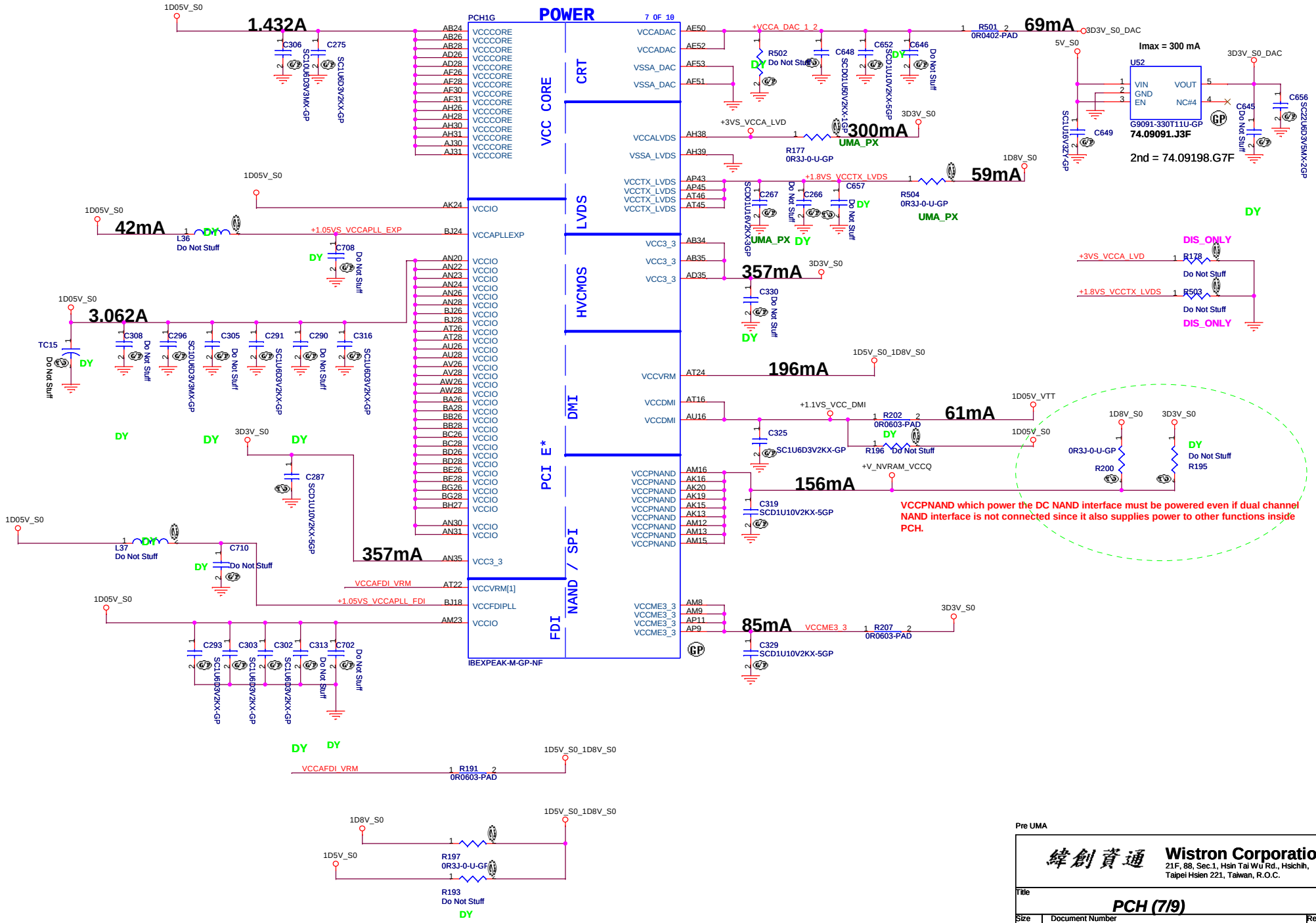
POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
PCI E*
DMI
NAND / SPI
FDI
1.432A
3.062A
42mA
357mA
196mA
61mA
156mA
85mA
69mA
300mA
59mA
357mA
Imax = 300 mA
G9091-330T11U-GP
74.09091.J3F
2nd = 74.09198.G7F
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
IBEXPEAK-M-GP-NF
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (7/9)
Size A3
Document Number
JE70-CP
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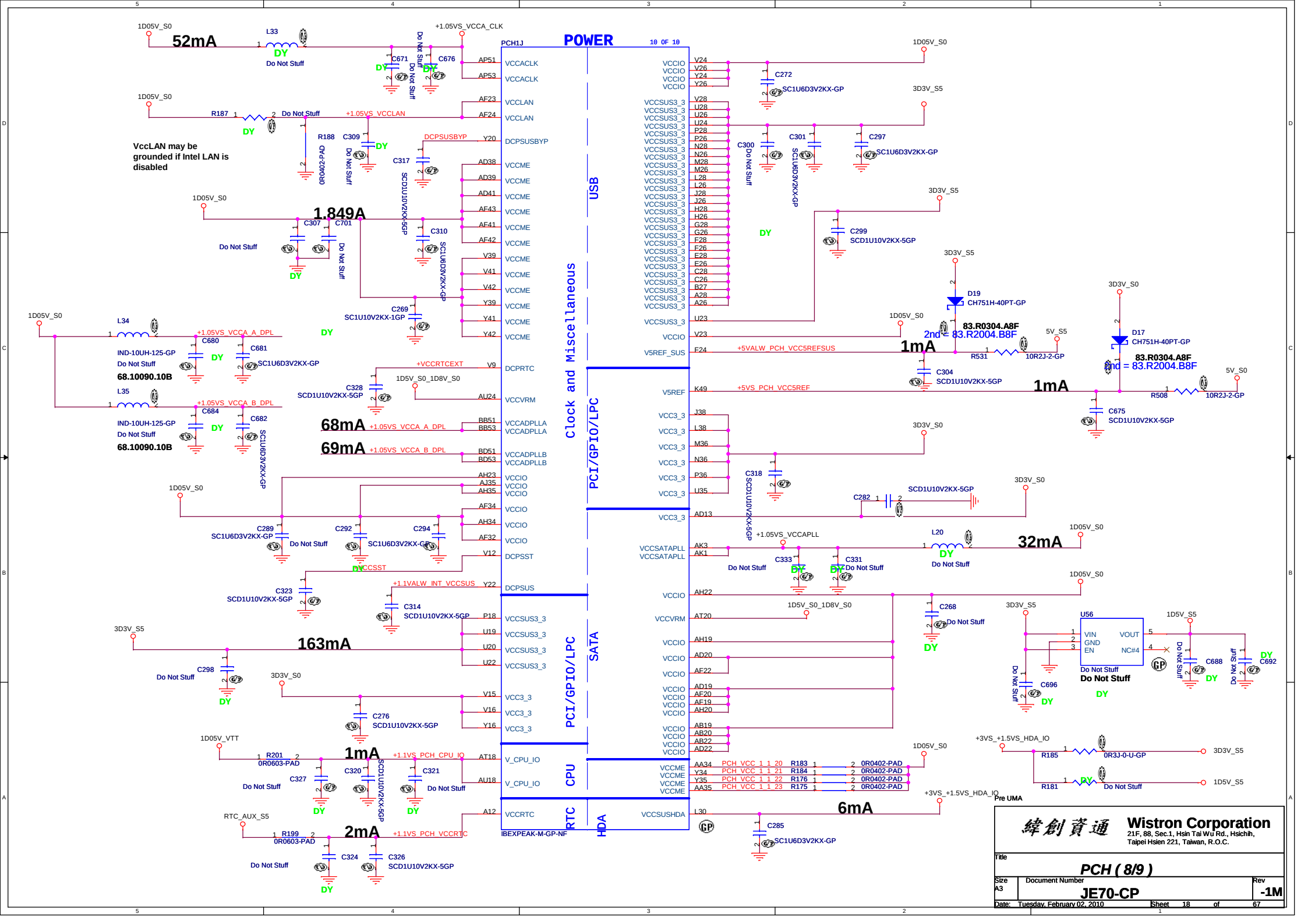
POWER
10 OF 10
PCH1J
IBEXPEAK-M-GP-NF
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
163mA
68mA
69mA
1mA
32mA
6mA
2mA
VccLAN may be grounded if Intel LAN is disabled
Do Not Stuff
DY
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
Size A3
Document Number
JE70-CP
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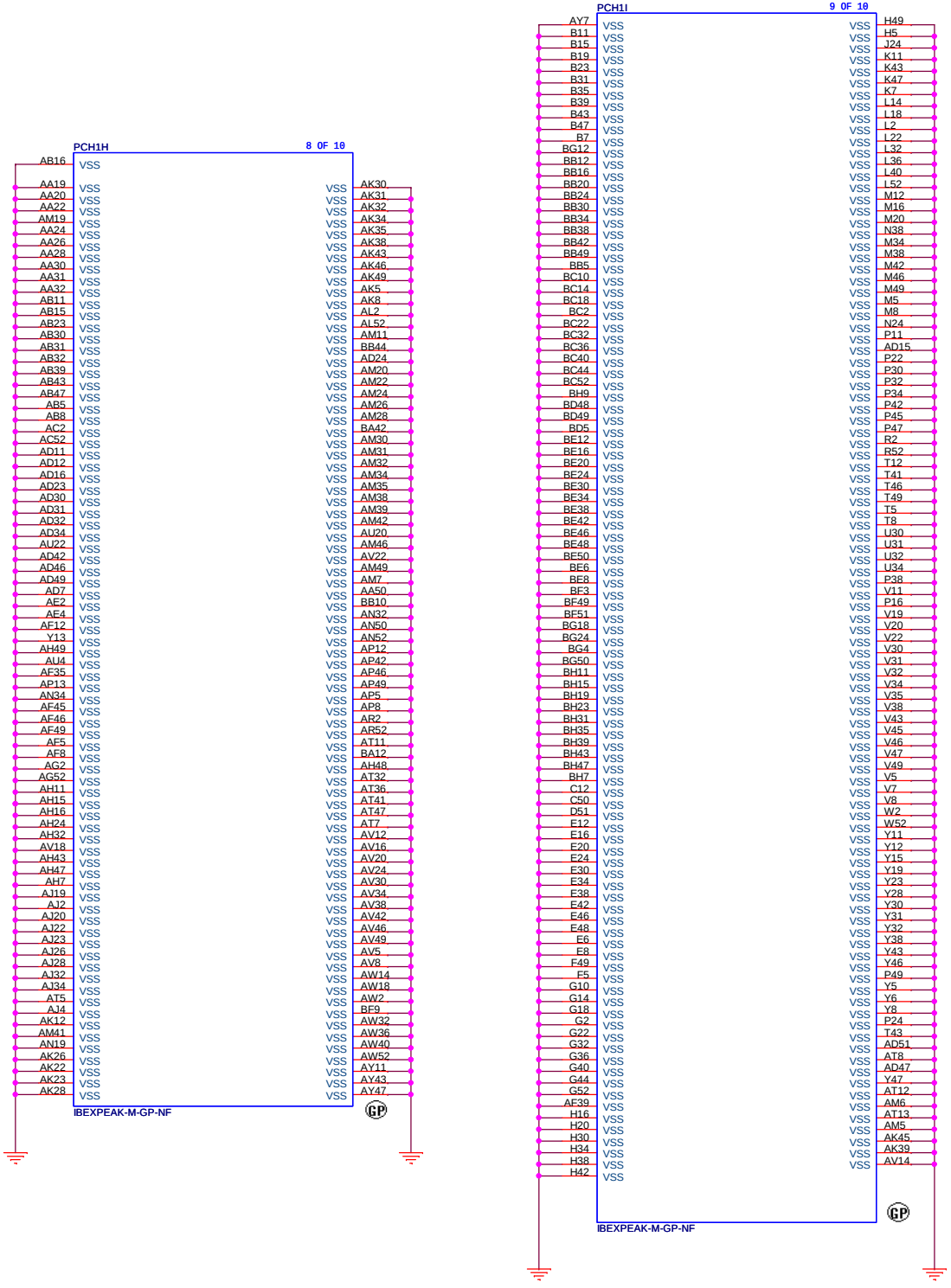

Pre UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (9/9)***

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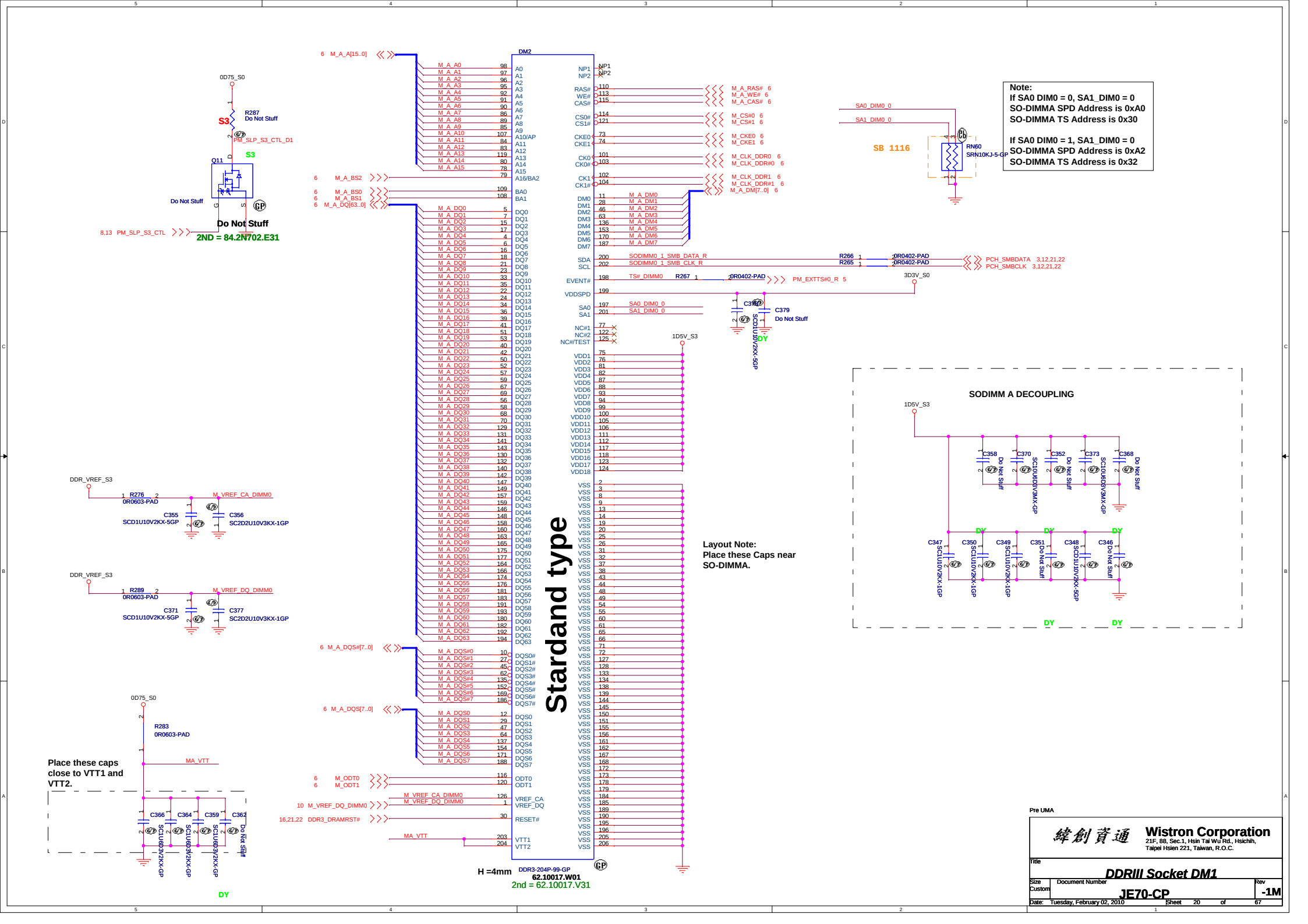
DM2
Stardand type
H =4mm
DDR3-204P-99-GP
62.10017.W01
2nd = 62.10017.V31
2ND = 84.2N702.E31
Do Not Stuff
Place these caps close to VTT1 and VTT2.
Layout Note: Place these Caps near SO-DIMMA.
SODIMM A DECOUPLING
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
SB 1116
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM1
Size Custom
Document Number
JE70-CP
Rev
-1M
Date: Tuesday, February 02, 2010
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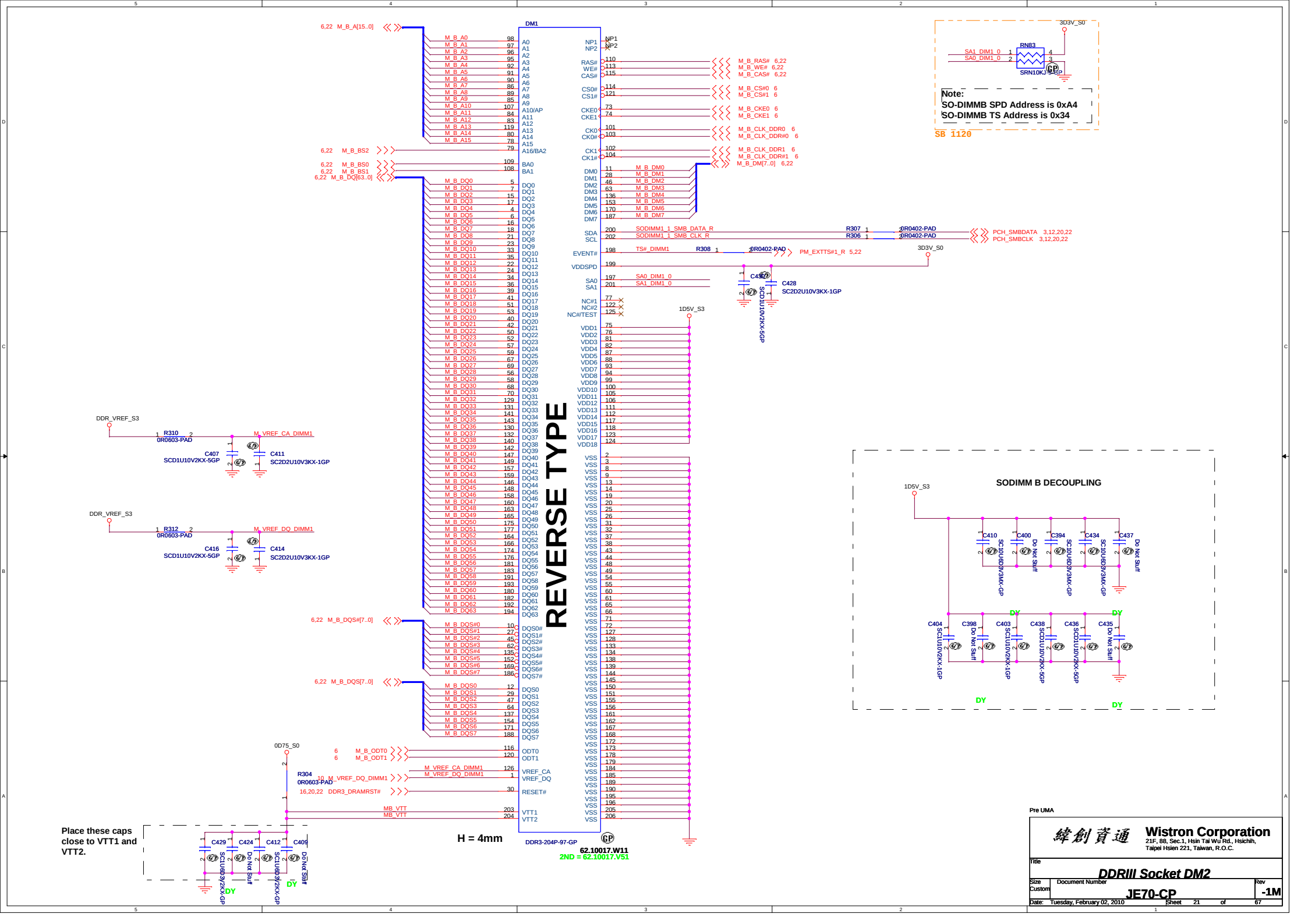
DM1
REVERSE TYPE
DDR3-204P-97-GP
H = 4mm
62.10017.W11
2ND = 62.10017.V51
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SB 1120
SODIMM B DECOUPLING
Place these caps close to VTT1 and VTT2.
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
DDRIII Socket DM2
JE70-CP
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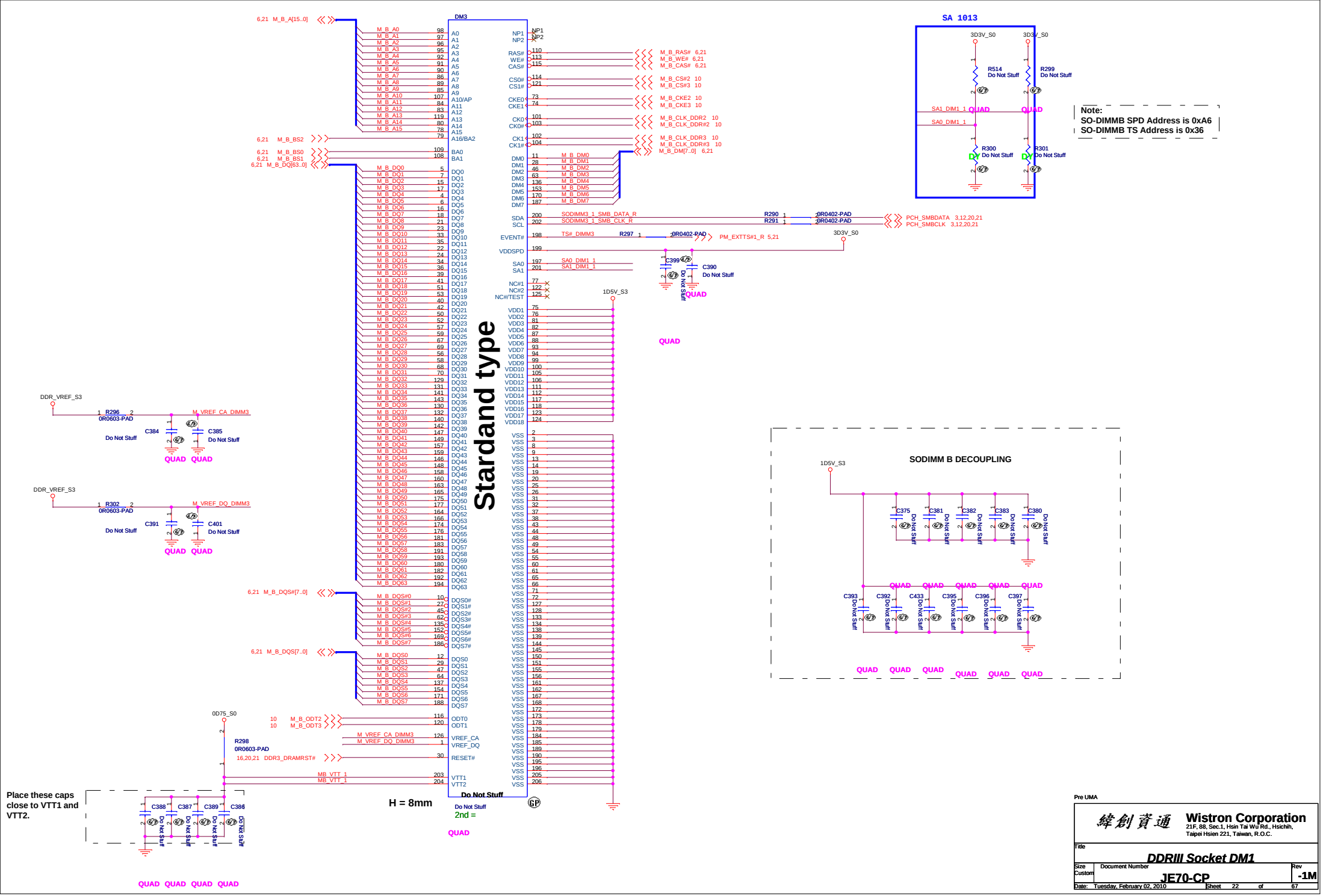
67


DM3
Stardand type
SA 1013
Note:
SO-DIMMB SPD Address is 0xA6
SO-DIMMB TS Address is 0x36
SODIMM B DECOUPLING
Place these caps close to VTT1 and VTT2.
H = 8mm
Do Not Stuff
2nd =
Pre UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM1
Size
Custom
Document Number
JE70-CP
Rev
-1M
Date: Tuesday, February 02, 2010
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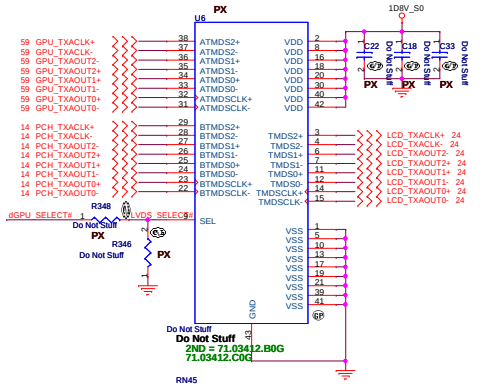
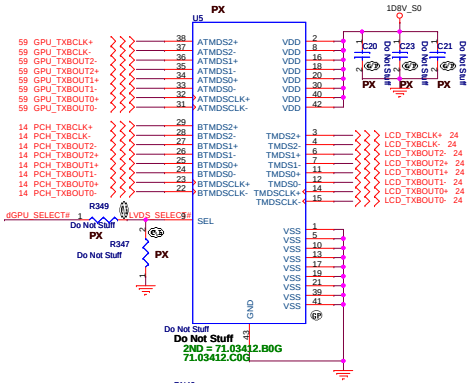
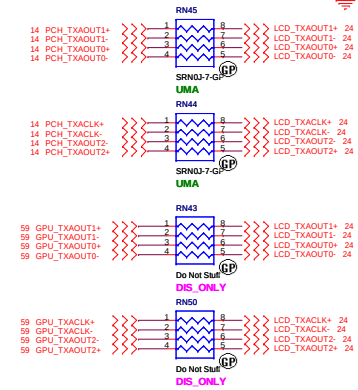
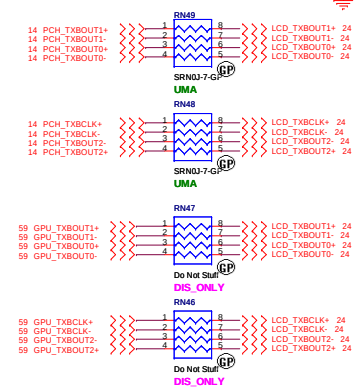
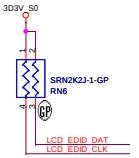
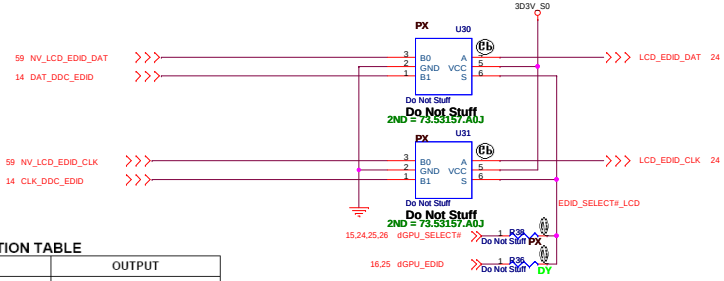






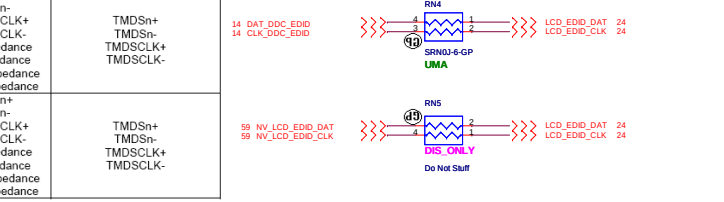


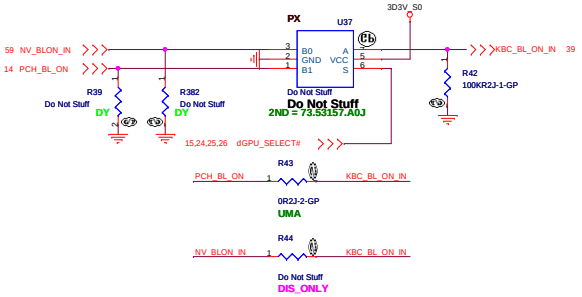


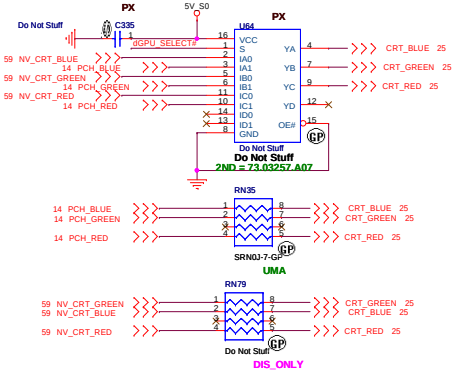


FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-







$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PX SWITCH

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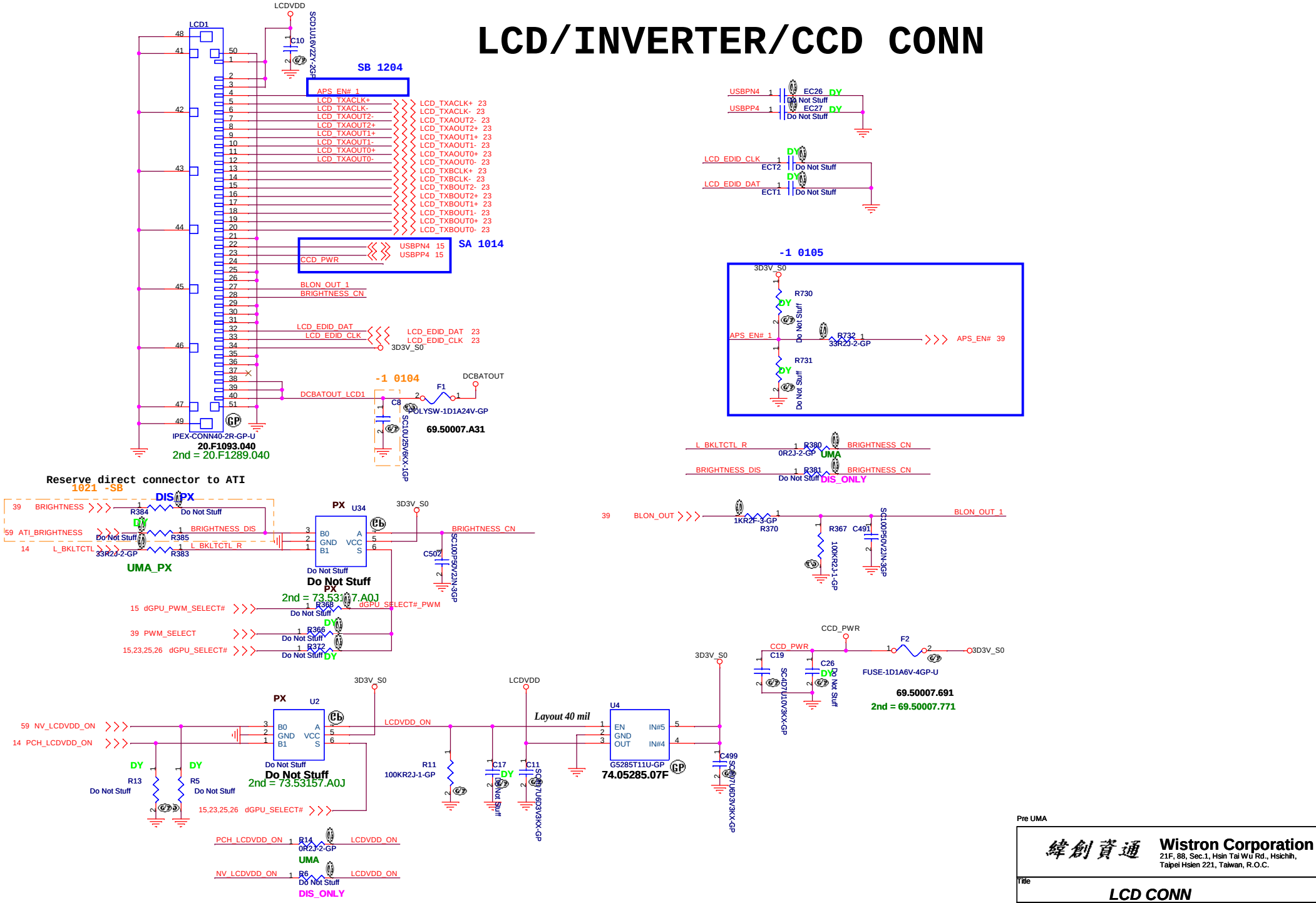
LCD/INVERTER/CCD CONN



Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
LCD CONN			
Size	Document Number		Rev
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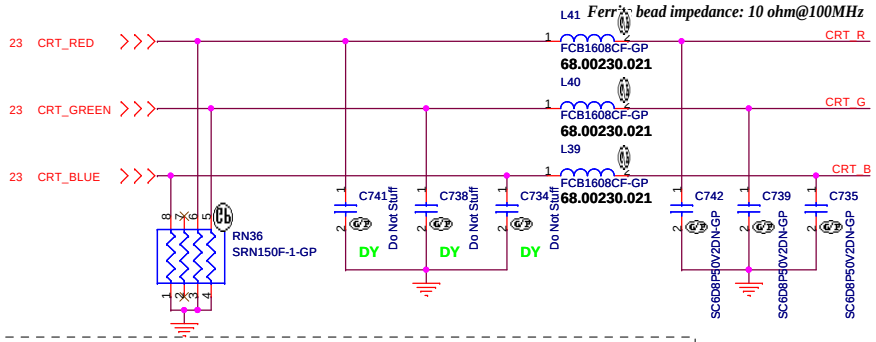
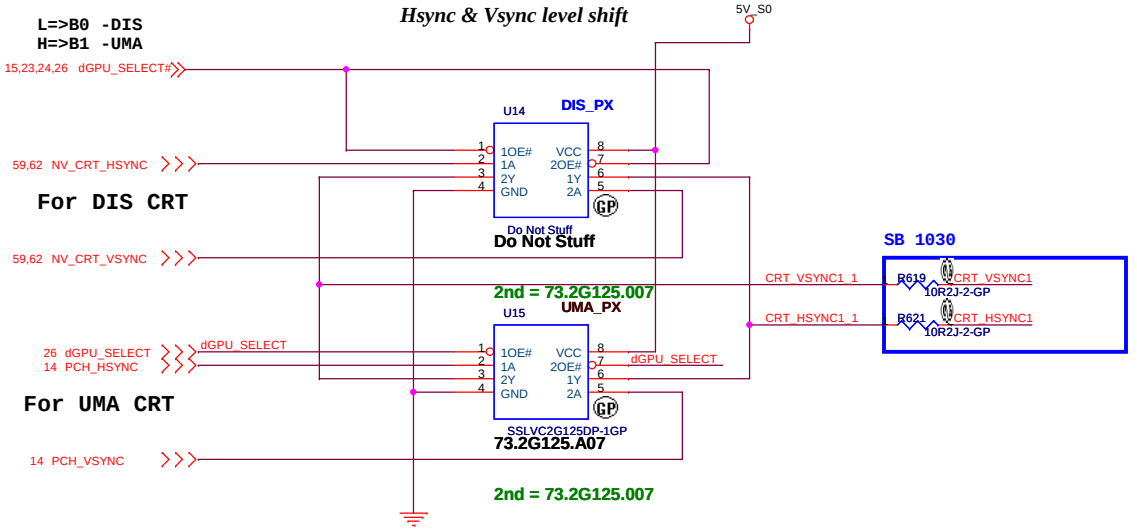
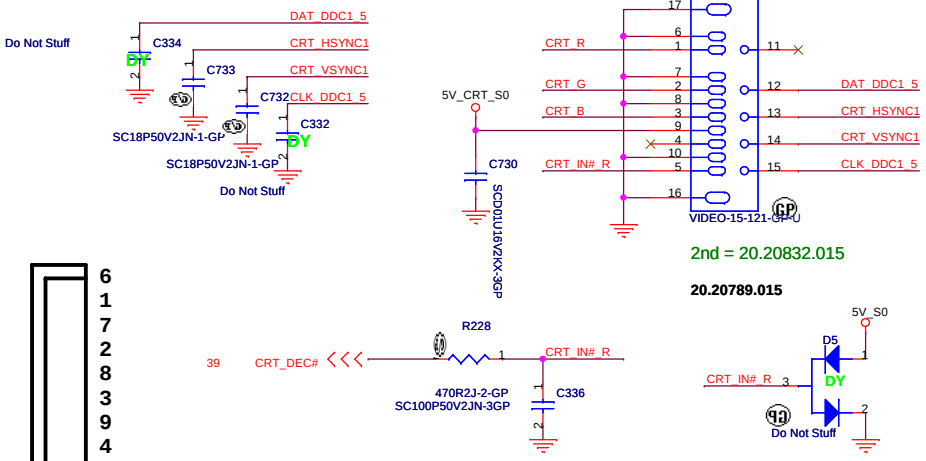
Layout Note:
Place these resistors close to the CRT-out connector

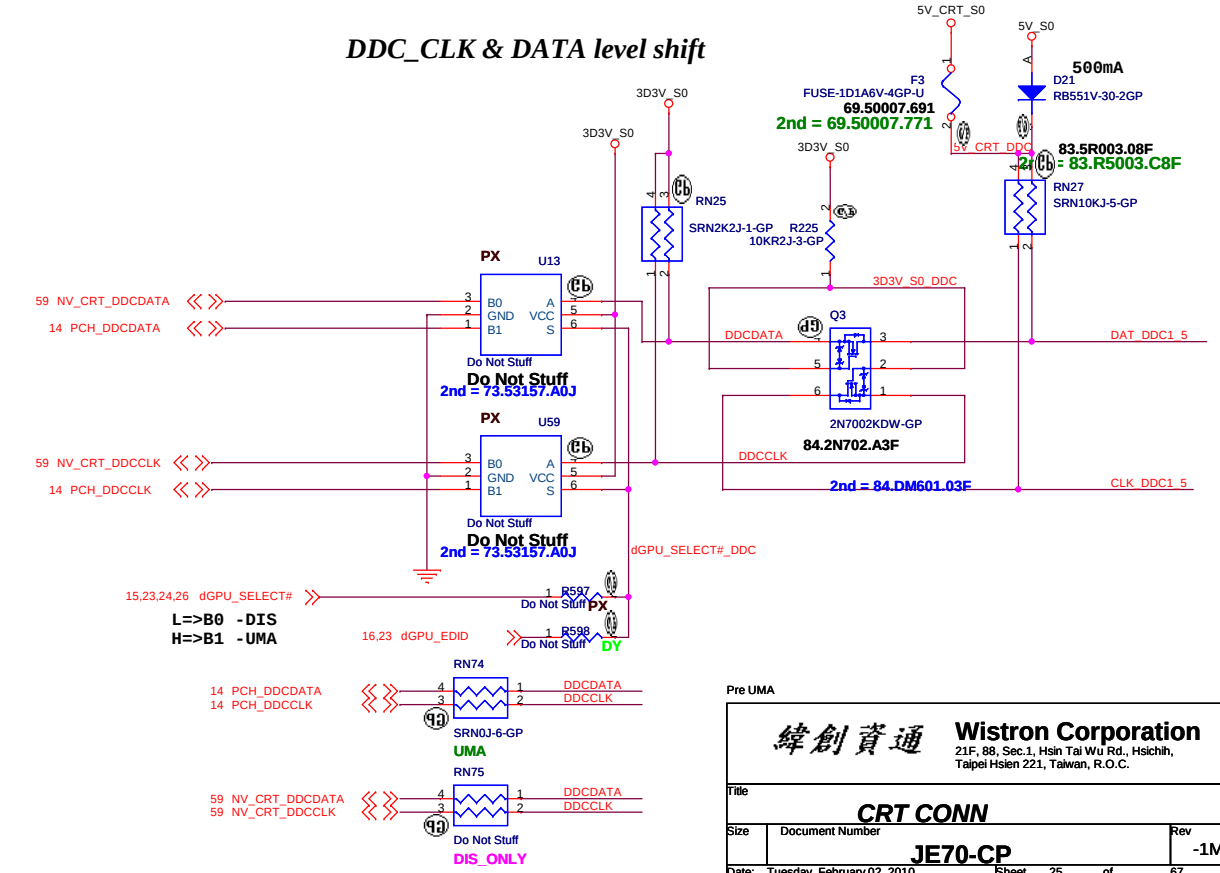


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



CRT I/F & CONNECTOR





Pre UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT CONN	
Size	Document Number JE70-CP	Rev -1M
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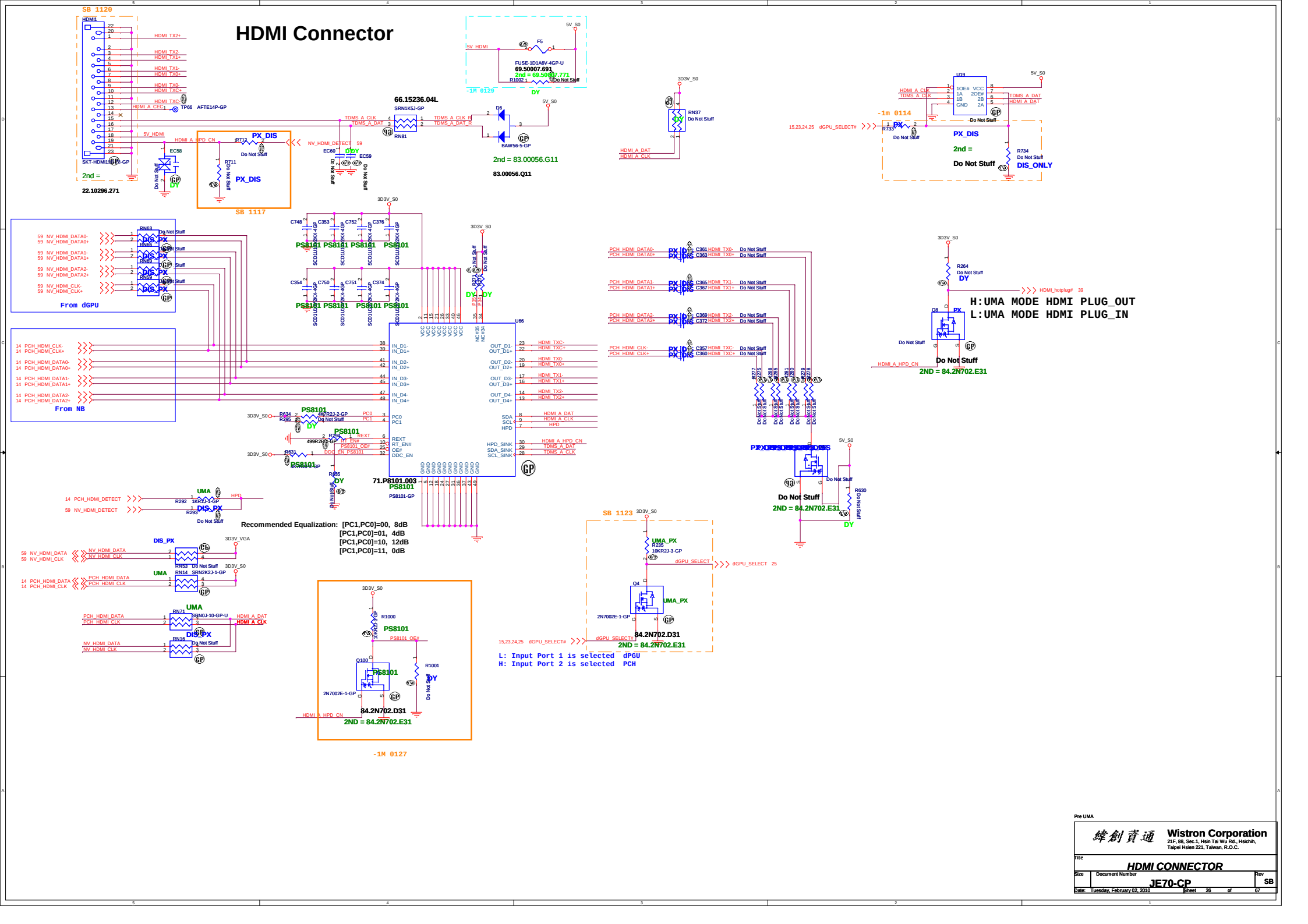
6 1 7 2 8 3 9 4 10 5

HDMI Connector



Pre UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI CONNECTOR	
Size	Document Number: JE70-CP	Rev: SB
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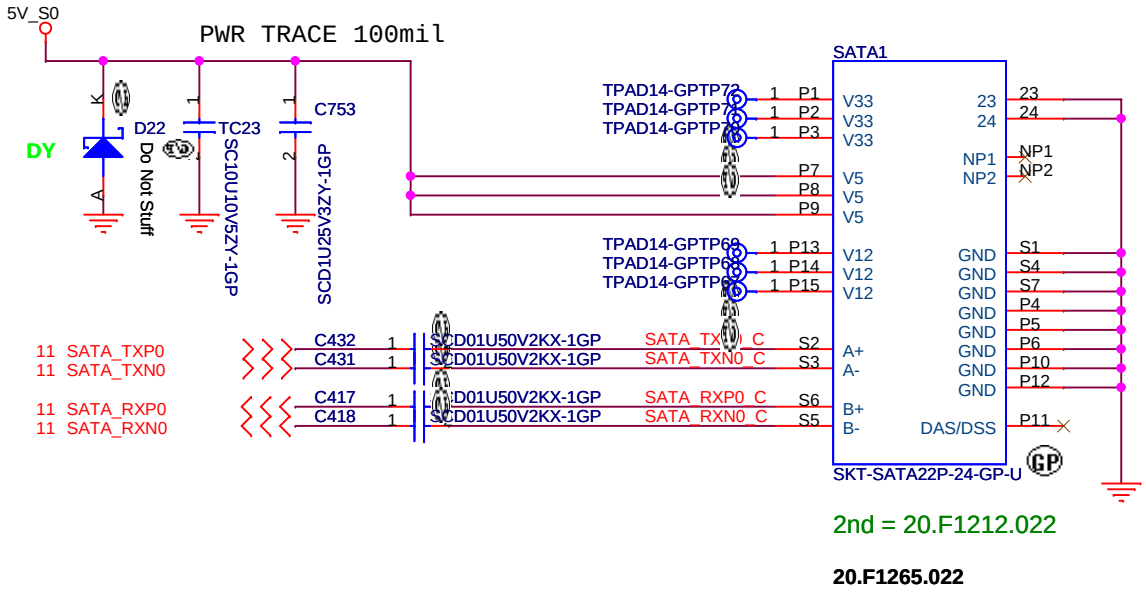
SATA Connector



2nd = 20.F1212.022

20.F1265.022

Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD CONN***	
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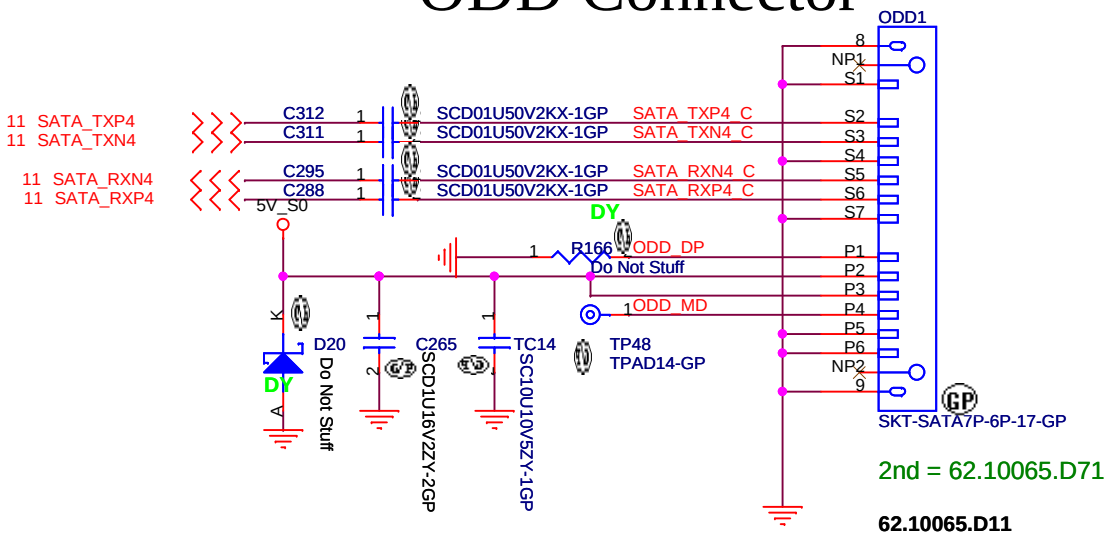
ODD Connector



Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***ODD***	
Size	Document Number **JE70-CP**	Rev -1M
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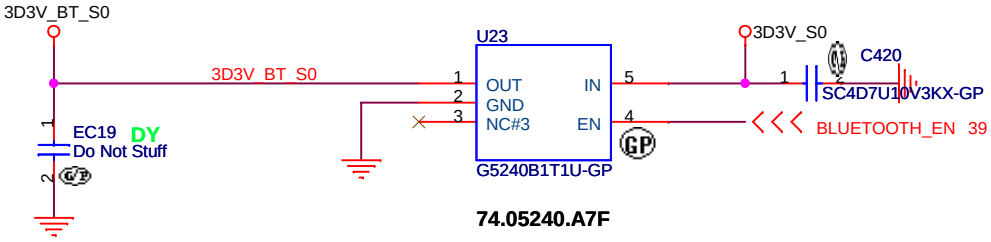
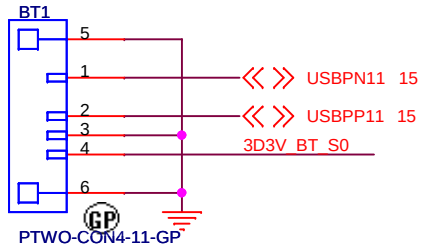
BLUETOOTH MODULE



74.05240.A7F

2nd = 74.09711.A7F

EC20 put near BLUE1 / all USB put one choke near connector by EMI request



20.F1561.004

2nd = 20.F1621.004

Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLUETOOTH		
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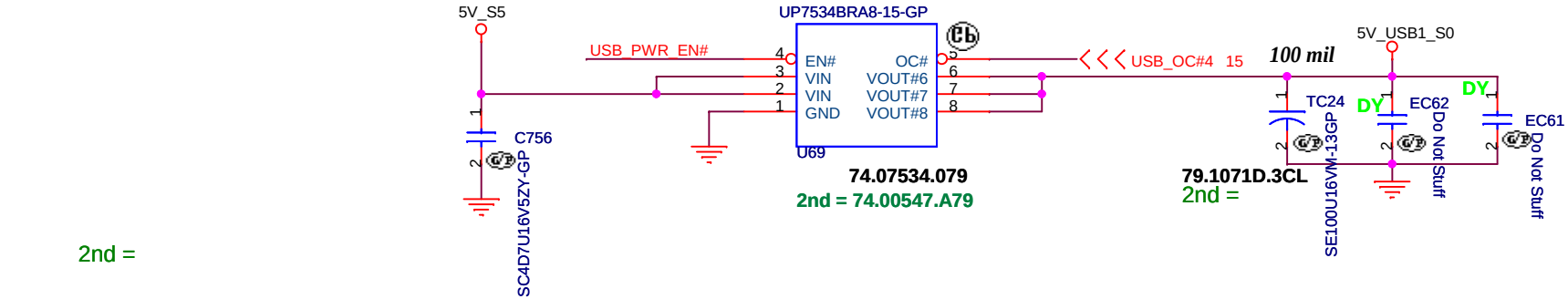
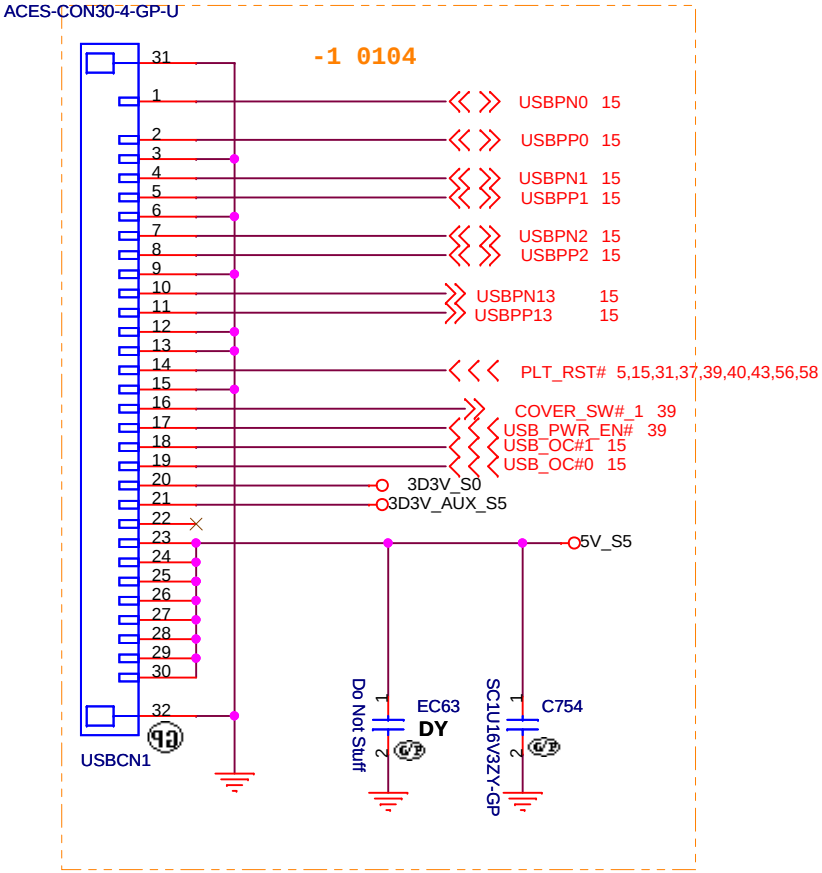
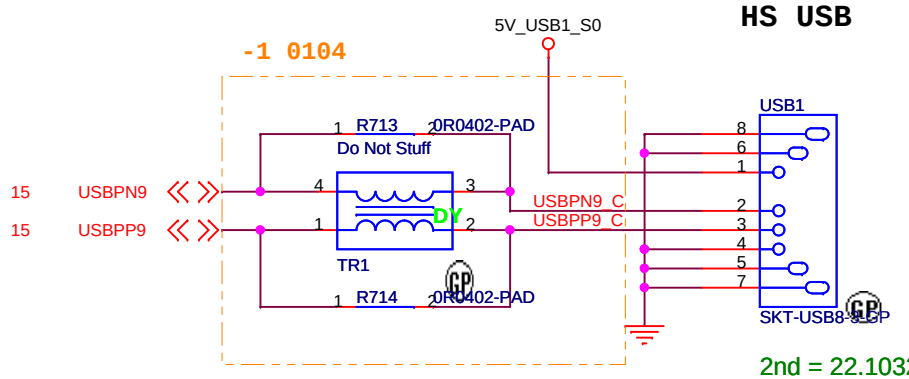


2nd =

20.K0276.030





Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *USB CONN*		
Size	Document Number: JE70-CP	Rev: -1M
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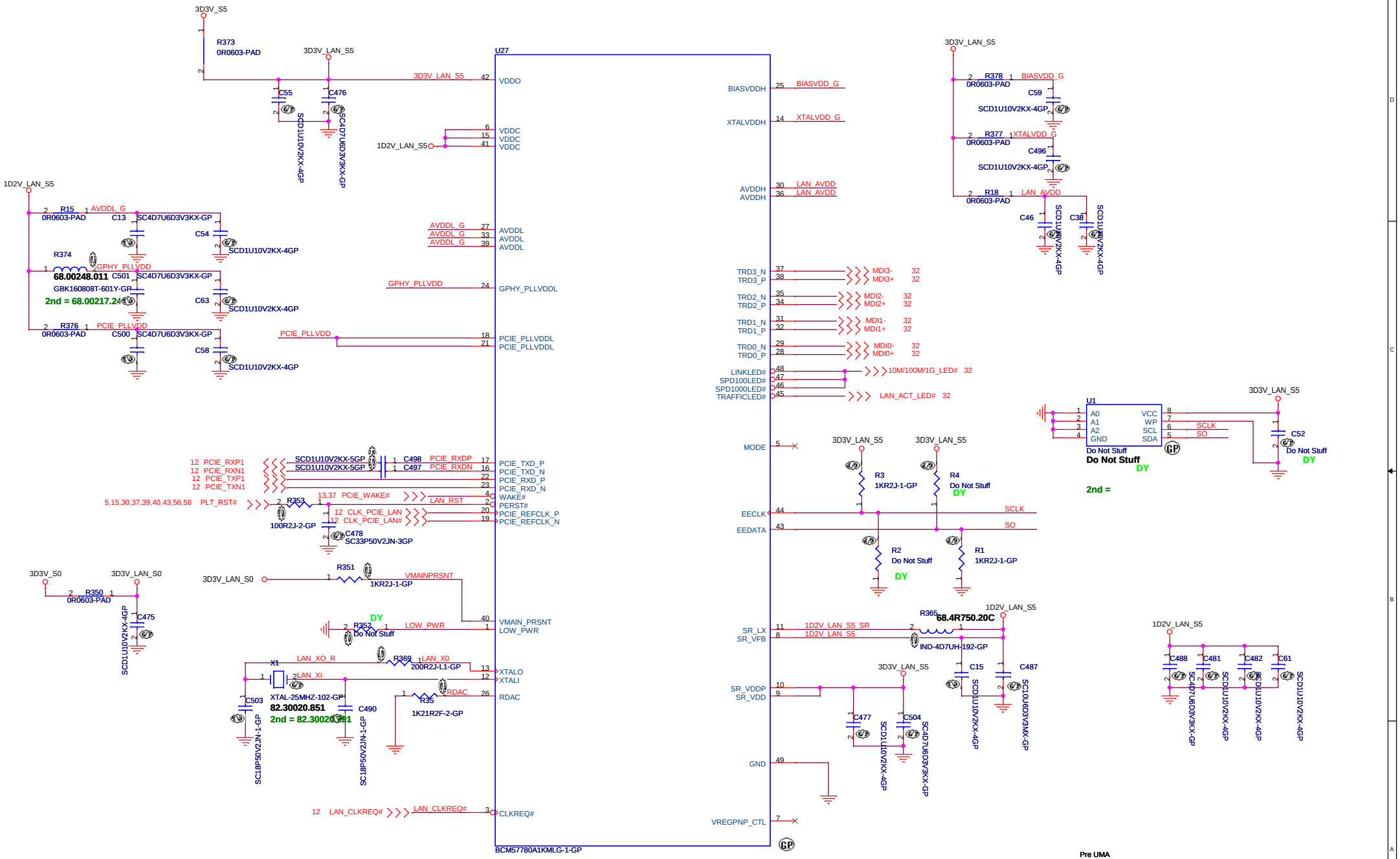
U27
BCM57780A1KMLG-1-GP
71.57780.M04
3D3V_S5
3D3V_LAN_S5
1D2V_LAN_S5
3D3V_S0
3D3V_LAN_S0
R373 0R0603-PAD
C55 SCD1U10V2KX-4GP
C476 SC4D7U6D3V3KX-GP
R15 0R0603-PAD
C13 SC4D7U6D3V3KX-GP
C54 SCD1U10V2KX-4GP
R374 68.00248.011 GBK160808T-601Y-GP
2nd = 68.00217.241
C501 SC4D7U6D3V3KX-GP
C63 SCD1U10V2KX-4GP
R376 0R0603-PAD
C500 SC4D7U6D3V3KX-GP
C58 SCD1U10V2KX-4GP
R350 0R0603-PAD
C475 SCD1U10V2KX-4GP
R351 1KR2J-1-GP
R352 Do Not Stuff
DY
R353 100R2J-2-GP
C478 SC33P50V2JN-3GP
X1 XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30026.281
C503 SC18P50V2JN-1-GP
C490 SC18P50V2JN-1-GP
R369 200R2J-L1-GP
R35 1K21R2F-2-GP
C498 SCD1U10V2KX-5GP
C497 SCD1U10V2KX-5GP
R378 0R0603-PAD
C59 SCD1U10V2KX-4GP
R377 0R0603-PAD
C496 SCD1U10V2KX-4GP
R18 0R0603-PAD
C46 SCD1U10V2KX-4GP
C38 SCD1U10V2KX-4GP
U1
A0 A1 A2 GND VCC WP SCL SDA
Do Not Stuff
C52 Do Not Stuff
R3 1KR2J-1-GP
R4 Do Not Stuff
R2 Do Not Stuff
R1 1KR2J-1-GP
R365 68.4R750.20C
IND-4D7UH-192-GP
C15 SCD1U10V2KX-4GP
C487 SC10U6D3V3MX-GP
C477 SCD1U10V2KX-4GP
C504 SC4D7U6D3V3KX-GP
C488 SC4D7U6D3V3KX-GP
C481 SCD1U10V2KX-4GP
C482 SCD1U10V2KX-4GP
C61 SCD1U10V2KX-4GP
VDDO VDDC VDDC VDDC
BIASVDDH XTALVDDH AVDDH AVDDH
AVDDL AVDDL AVDDL
GPHY_PLLVDDL
PCIE_PLLVDDL PCIE_PLLVDDL
TRD3_N TRD3_P TRD2_N TRD2_P TRD1_N TRD1_P TRD0_N TRD0_P
MDI3- MDI3+ MDI2- MDI2+ MDI1- MDI1+ MDI0- MDI0+
LINKLED# SPD100LED# SPD1000LED# TRAFFICLED#
10M/100M/1G_LED# LAN_ACT_LED#
MODE EECLK EEDATA
SR_LX SR_VFB SR_VDDP SR_VDD GND VREGPNP_CTL
PCIE_TXD_P PCIE_TXD_N PCIE_RXD_P PCIE_RXD_N WAKE# PERST# PCIE_REFCLK_P PCIE_REFCLK_N
VMAIN_PRSNT LOW_PWR XTALO XTALI RDAC CLKREQ#
PCIE_RXP1 PCIE_RXN1 PCIE_TXP1 PCIE_TXN1 PLT_RST# LAN_RST LAN_CLKREQ#
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM57780
Size Custom
Document Number JE70-CP
Rev -1M
Date: Tuesday, February 02, 2010
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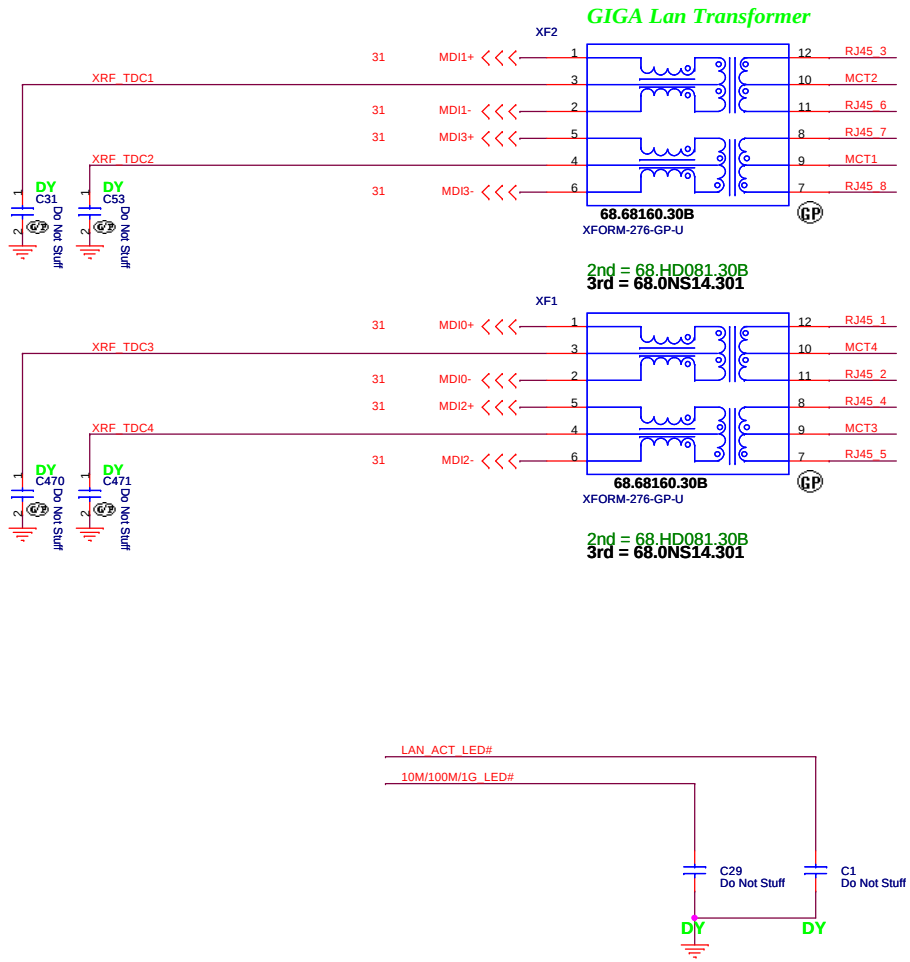
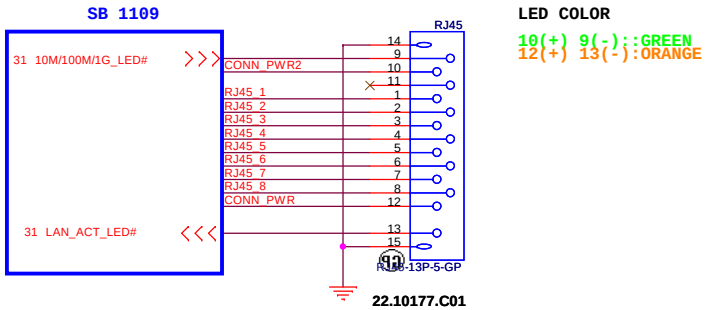
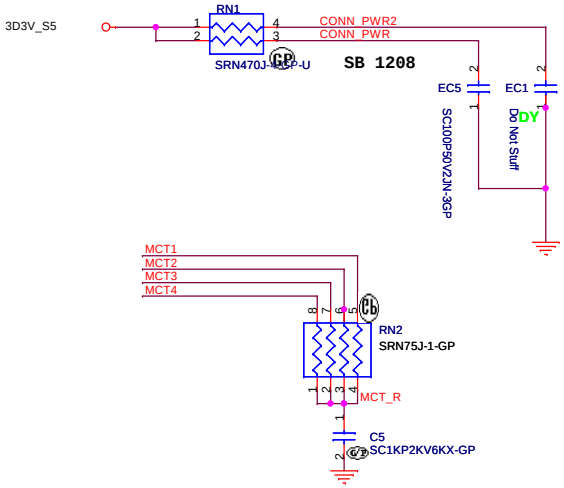
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

LAN Connector



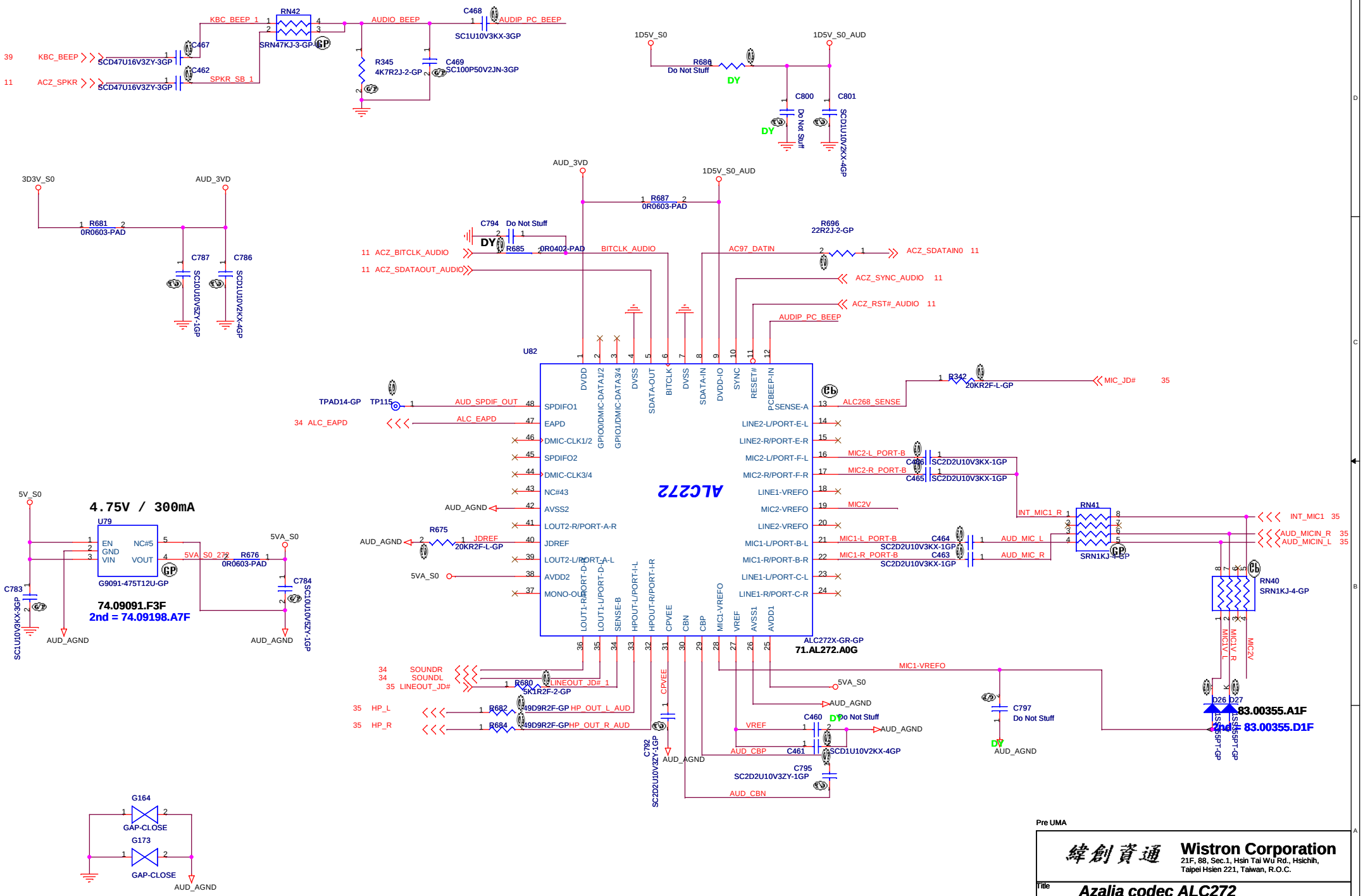




Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**		
Size: A3	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 32 of 67	



Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Azalia codec ALC272***

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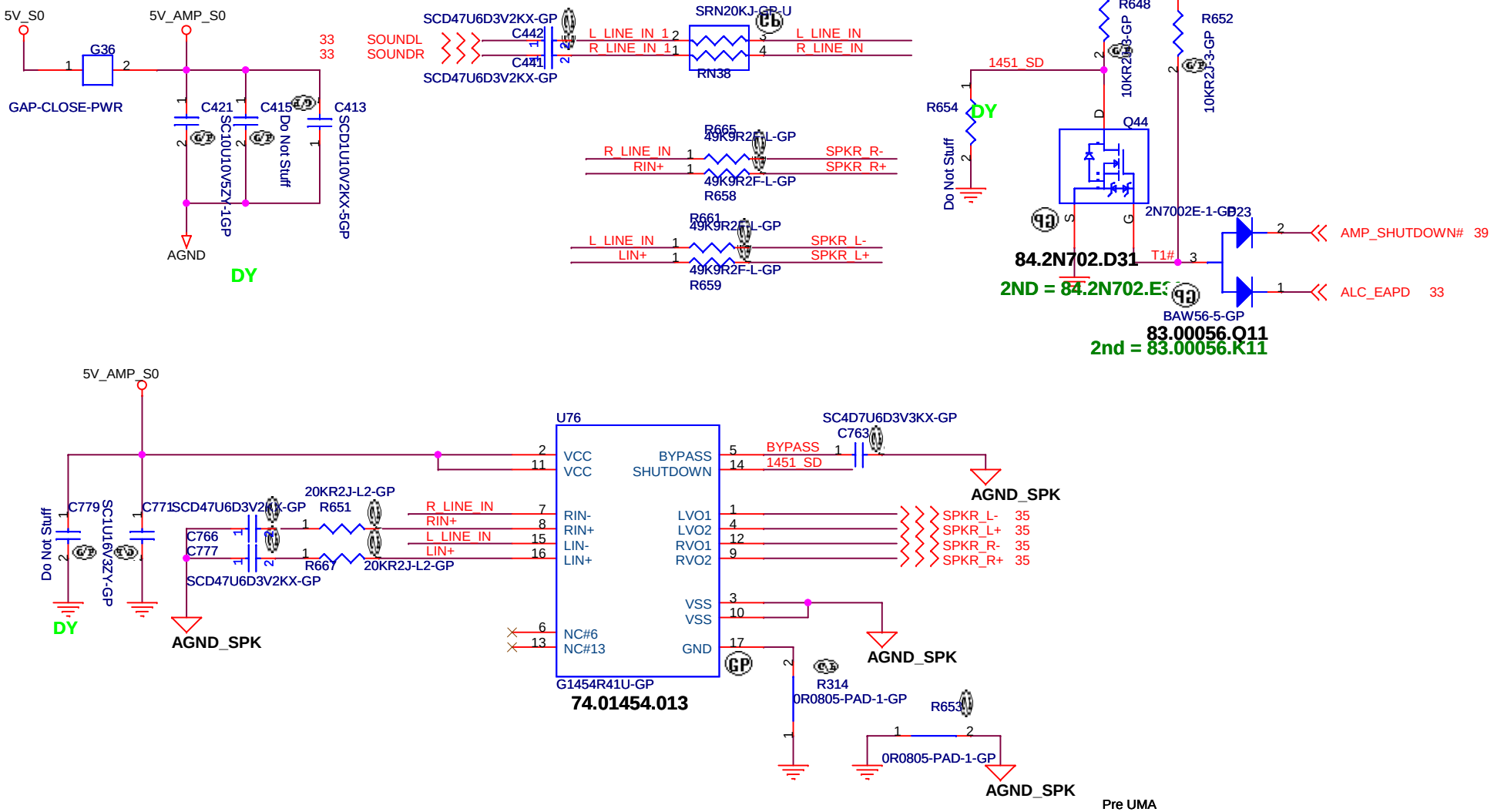
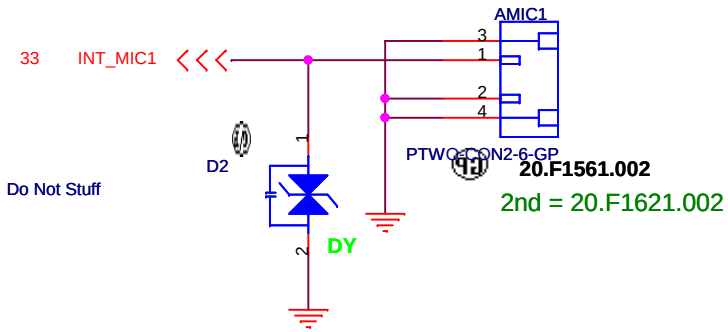
AUDIO OP AMPLIFIER



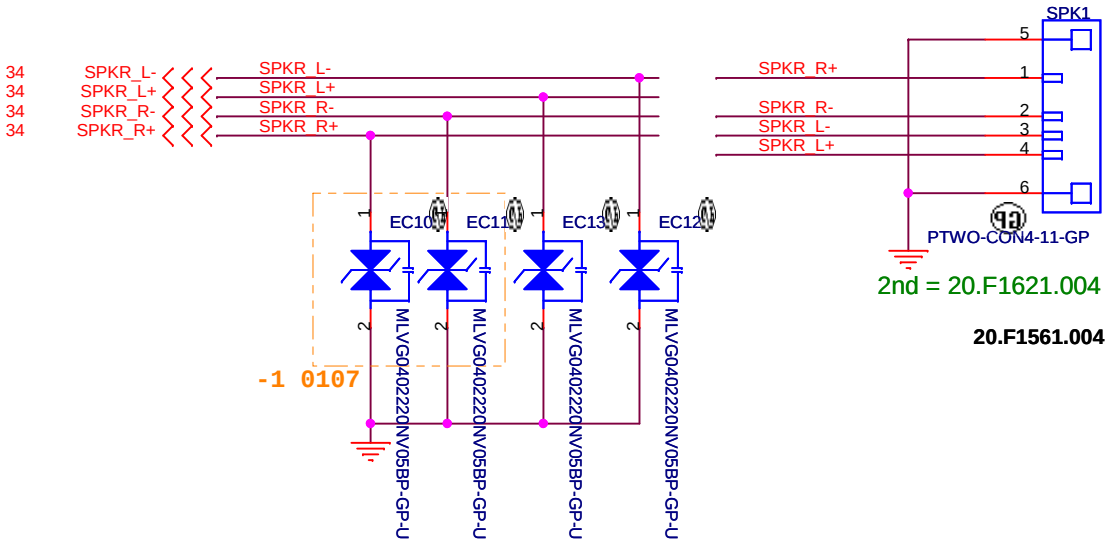
Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO AMP*	
Size	Document Number JE70-CP	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 34 of 67	

Internal Mic



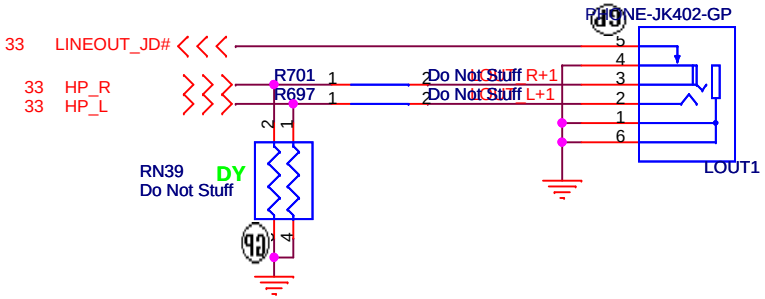
Internal Speaker

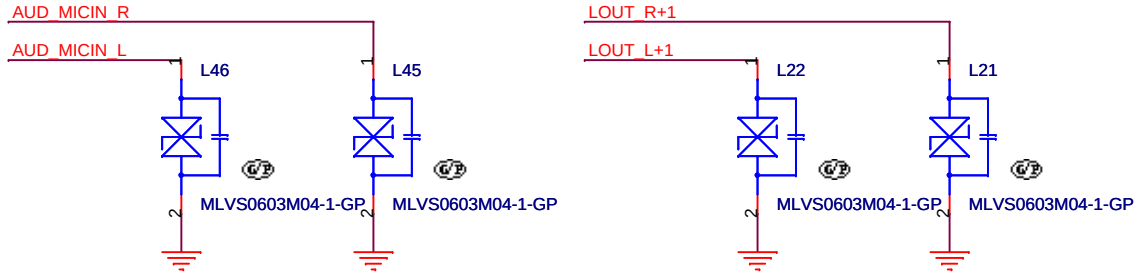


LINE OUT

22.10265.261

2nd =





MIC IN

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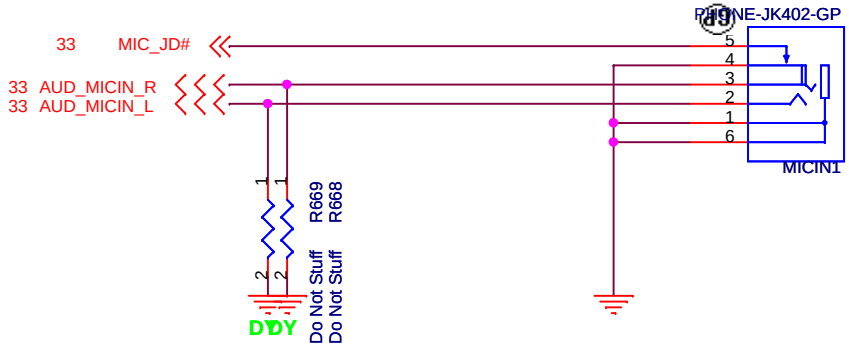


Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO jack*	
Size	Document Number JE70-CP	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 35 of 67	

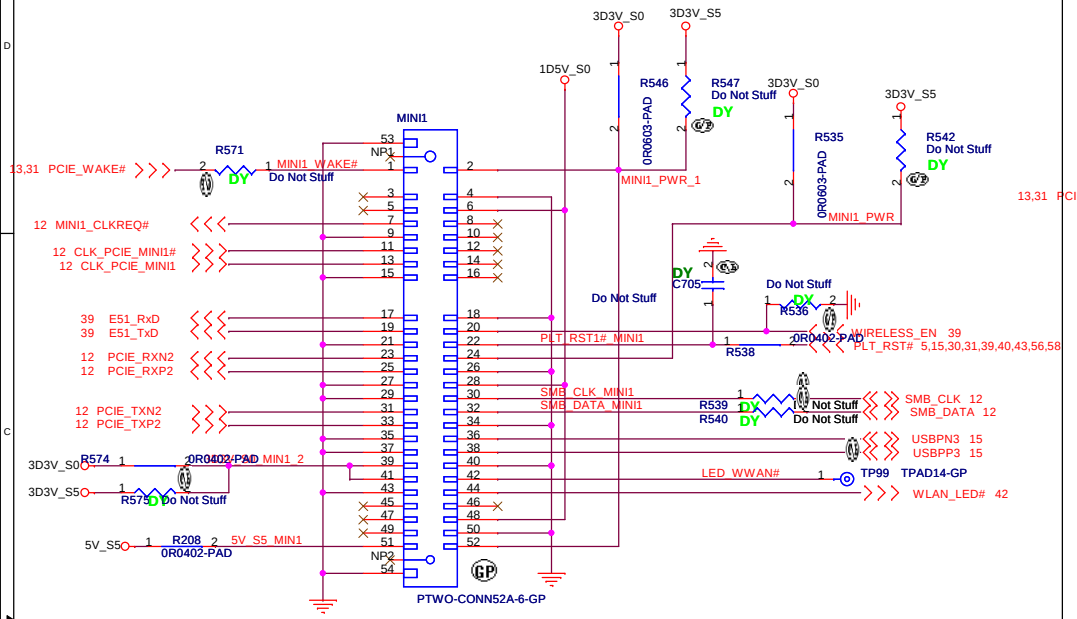
Pre UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cardreader*		
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 36 of 67	

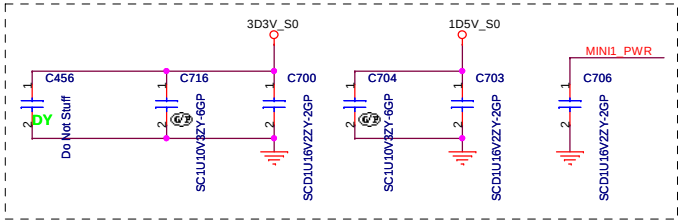
Mini Card Connector(WLAN)
Support debug-card



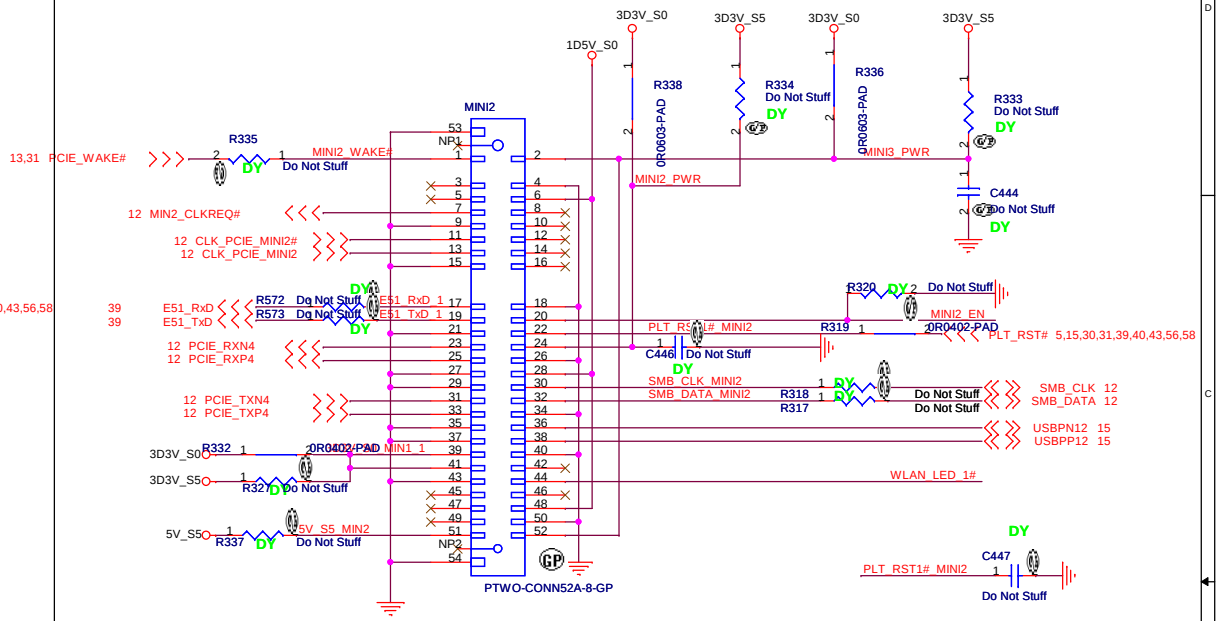
2nd = 62.10043.461

20.F1517.052

Place near MINI1



Mini Card Connector(Robson2 and 3G)



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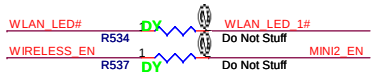
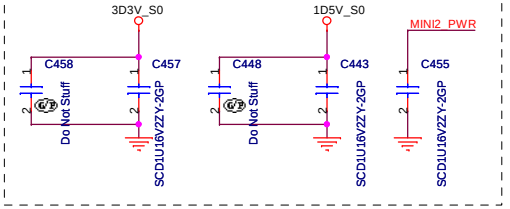
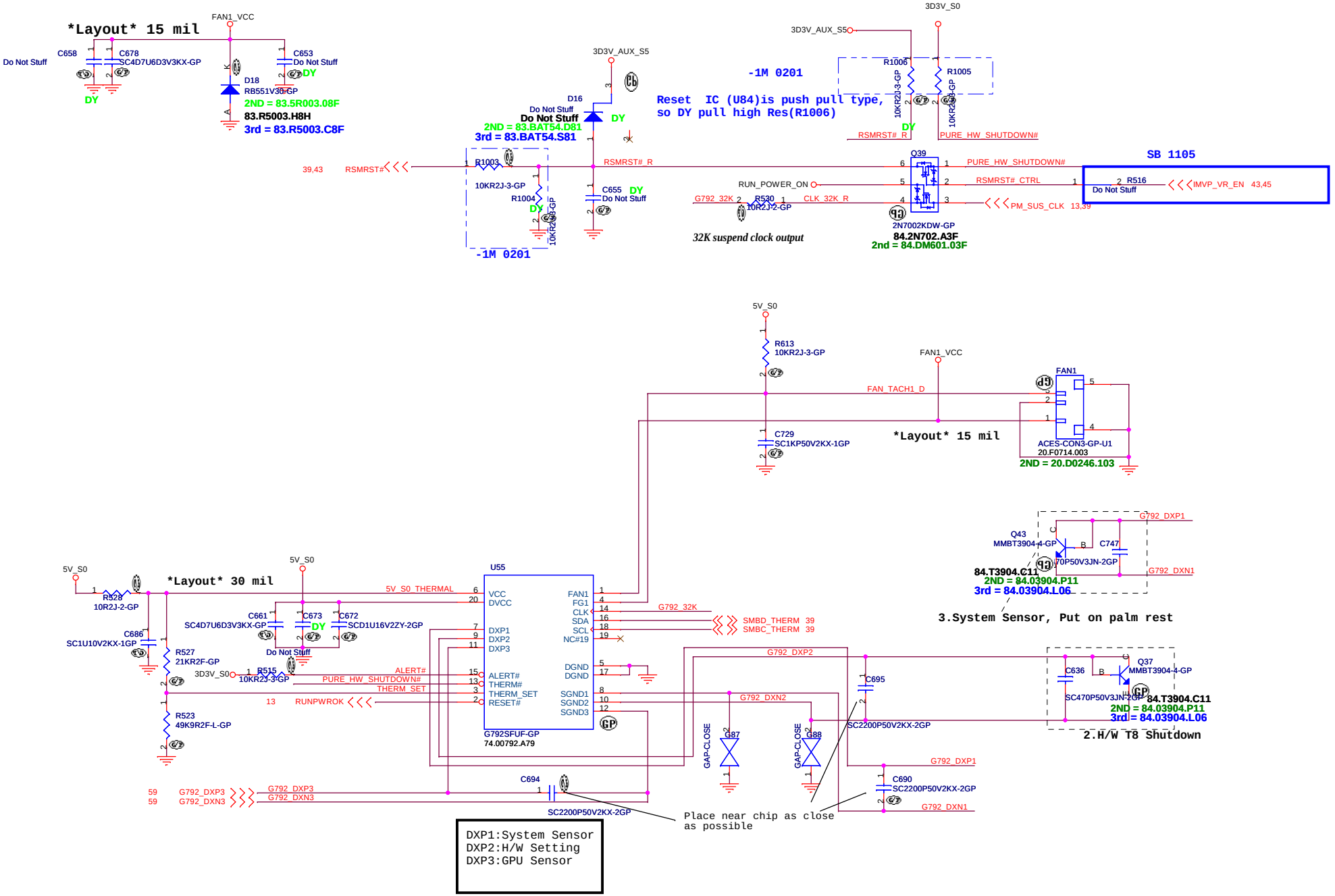


Place near MINIC2



Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size: A3	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 37 of 67	



Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Connector

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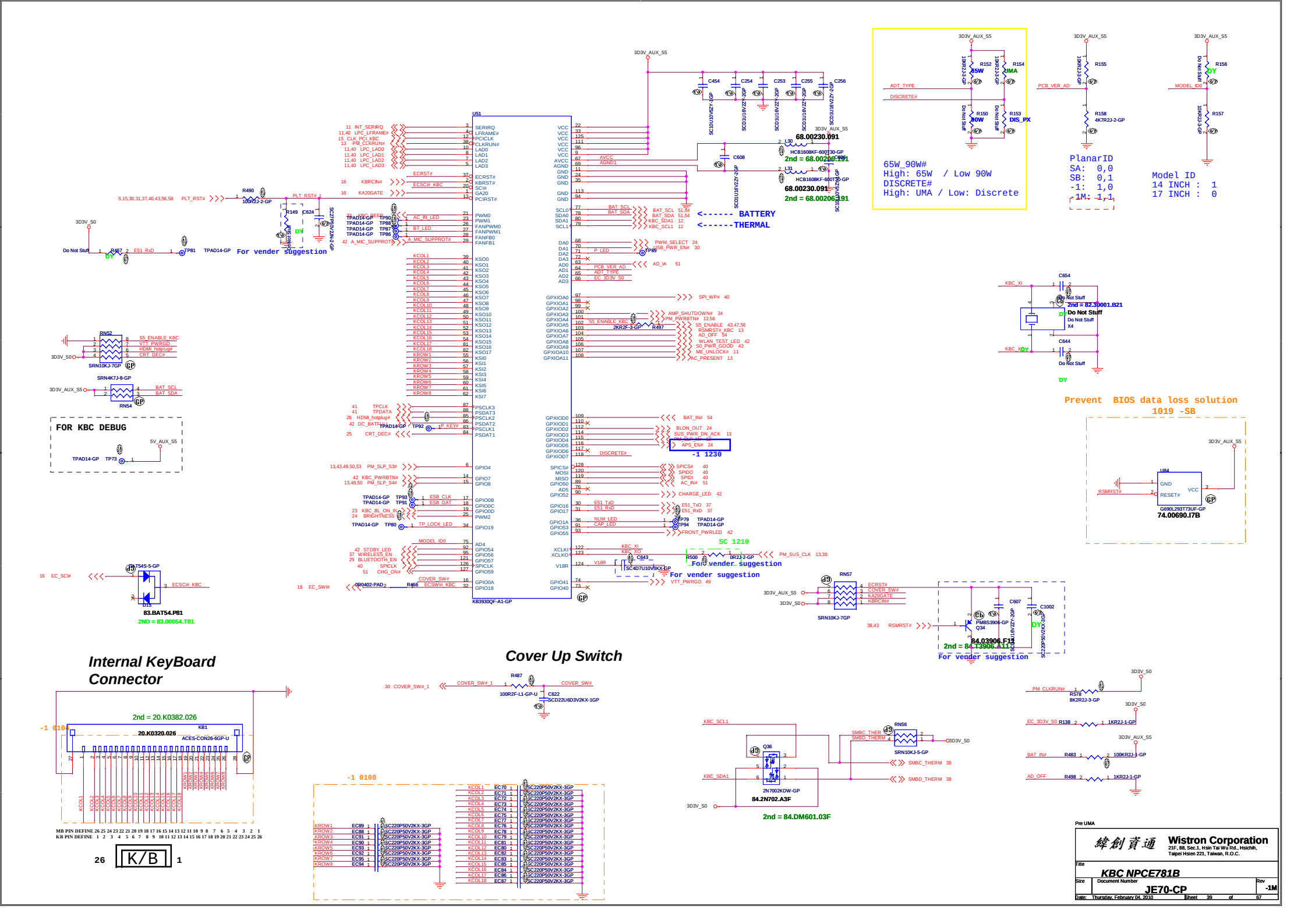
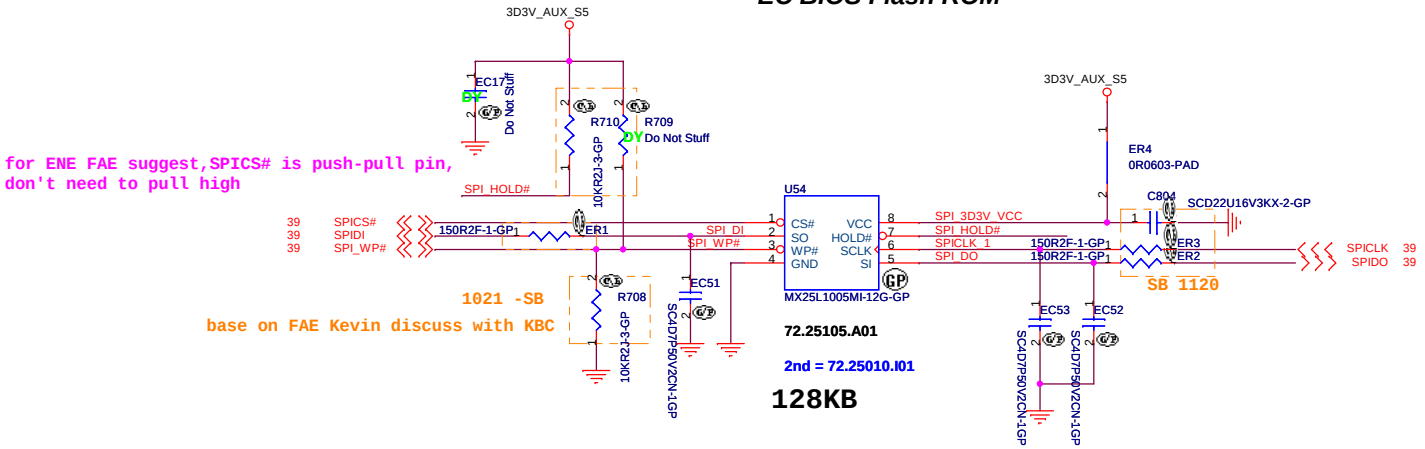
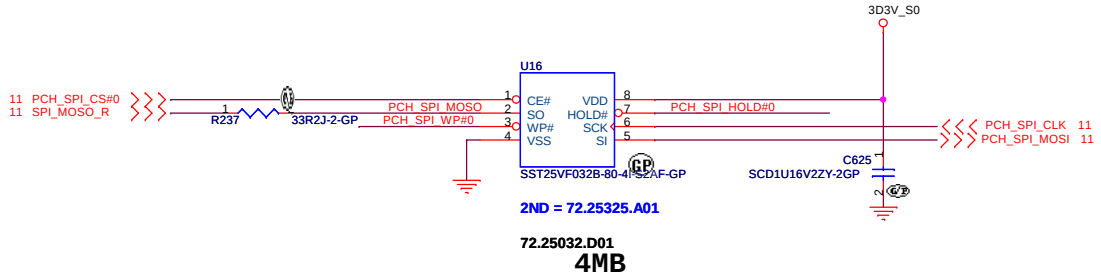
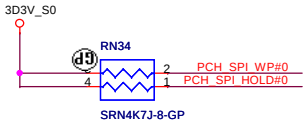

65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
Model ID
14 INCH : 1
17 INCH : 0
U51
KB3930QF-A1-GP
BATTERY
THERMAL
FOR KBC DEBUG
Prevent BIOS data loss solution
1019 -SB
Internal KeyBoard Connector
Cover Up Switch
For vender suggestion
Wistron Corporation
KBC NPCE781B
JE70-CP

EC BIOS Flash ROM

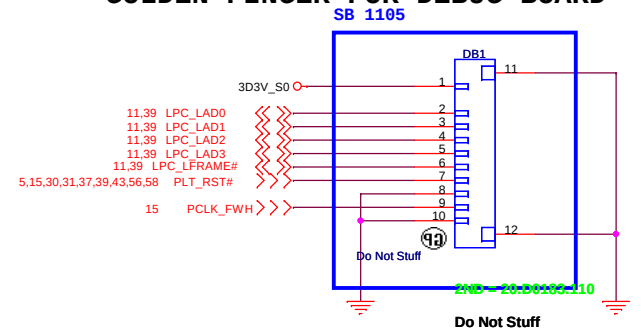


System BIOS Flash ROM





GOLDEN FINGER FOR DEBUG BOARD



Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

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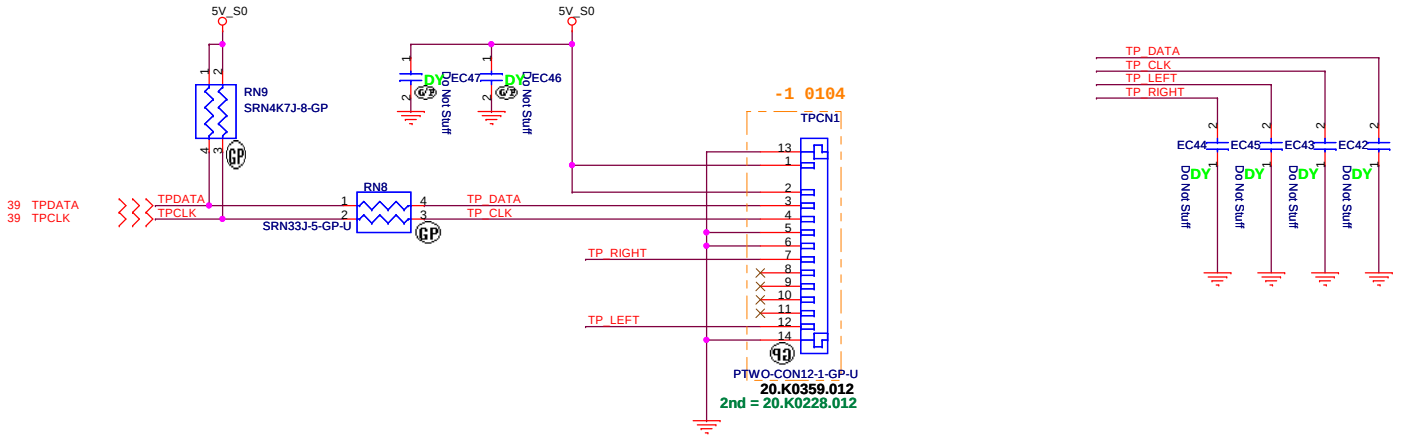
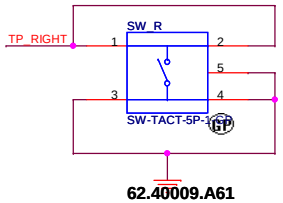
TOUCH PAD

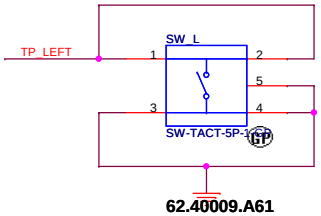


1 12

T/P



62.40009.A61
2nd = 62.40009.B21



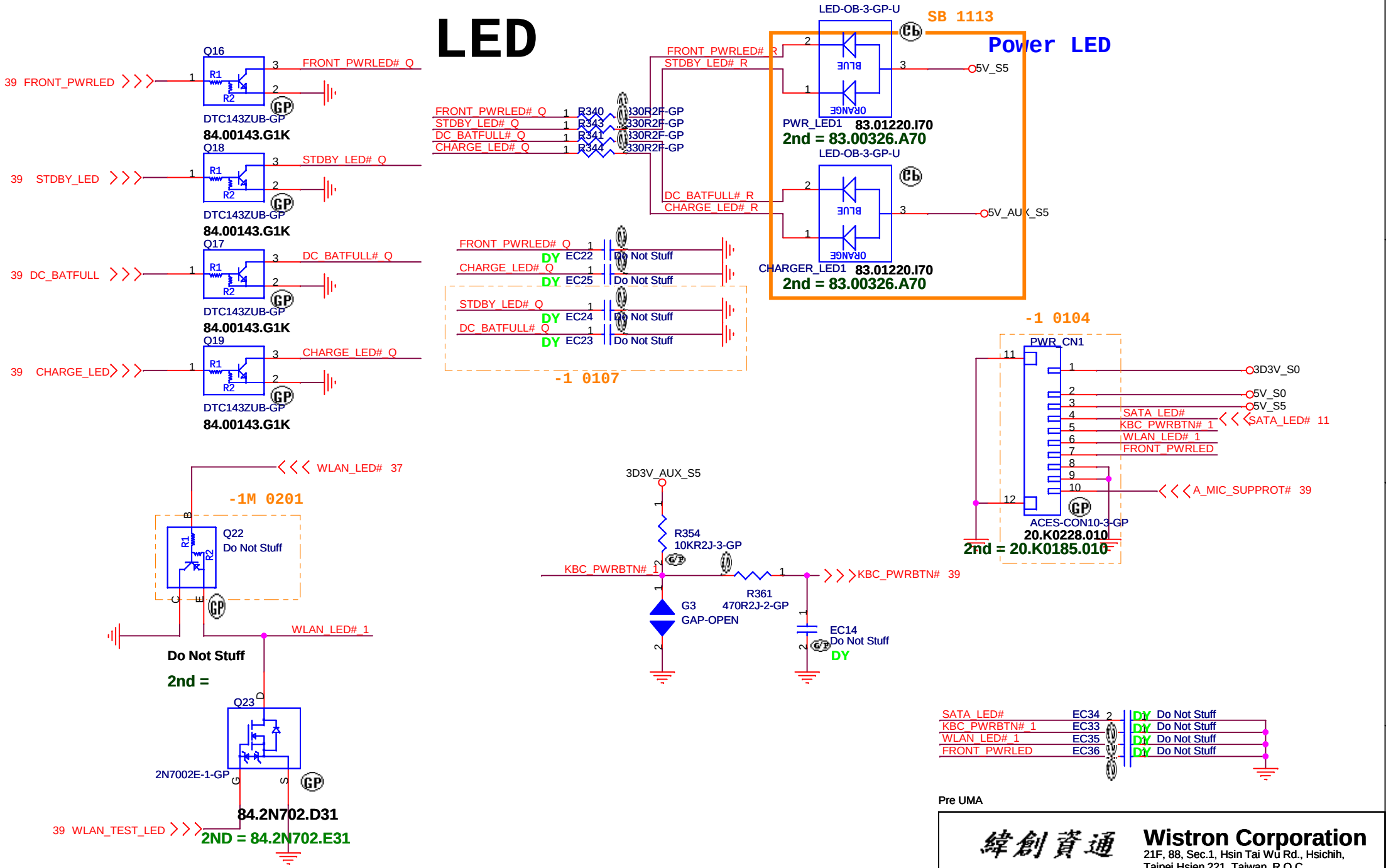
62.40009.A61
2nd = 62.40009.B21

Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Touch PAD and FP*		
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 41 of 67	

LED



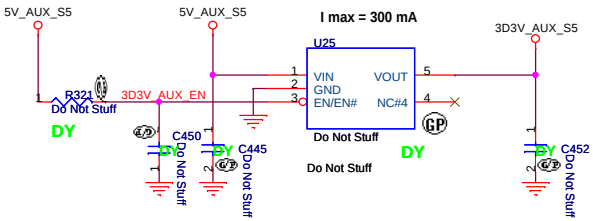
Pre UMA

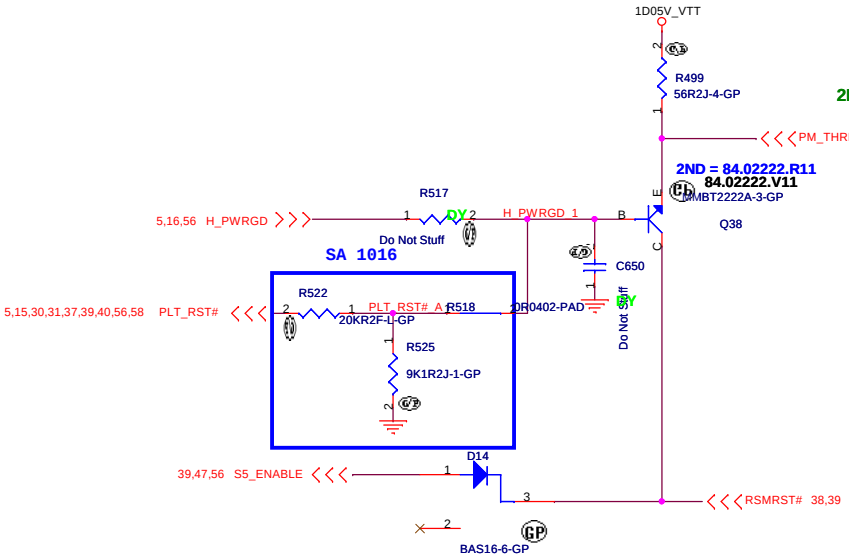
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LED&POWERBD CONN***	
Size	Document Number **JE70-CP**	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 42 of 67	

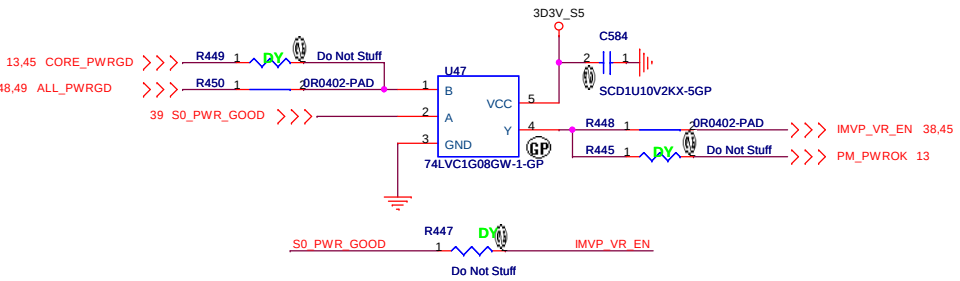
Run Power

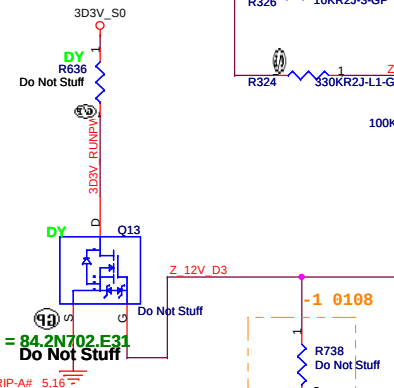
Aux Power

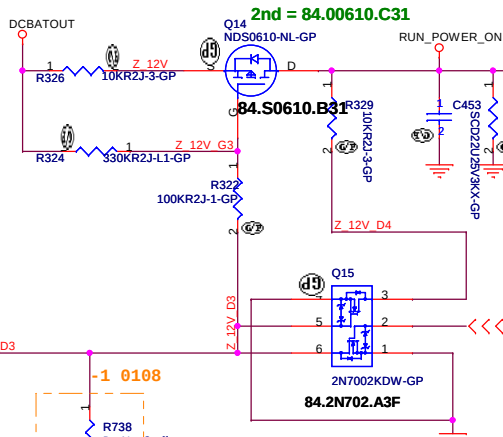
3D3V_AUX_S5

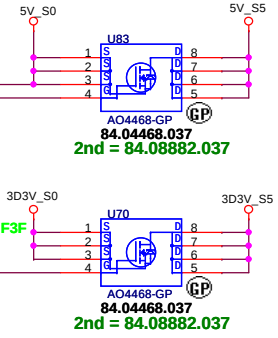


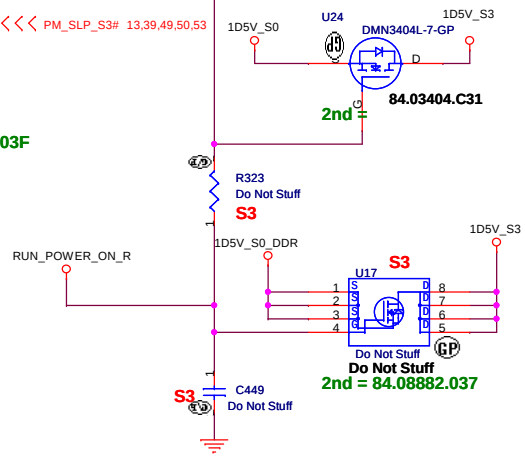


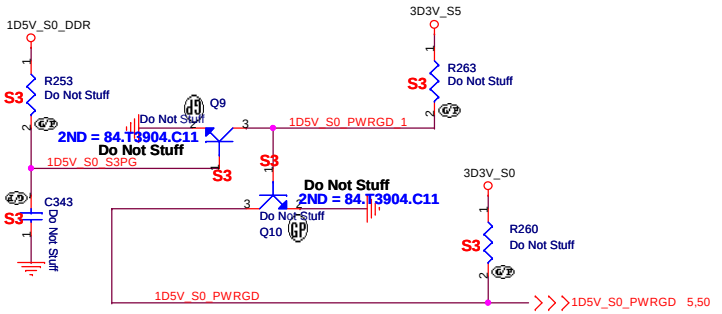






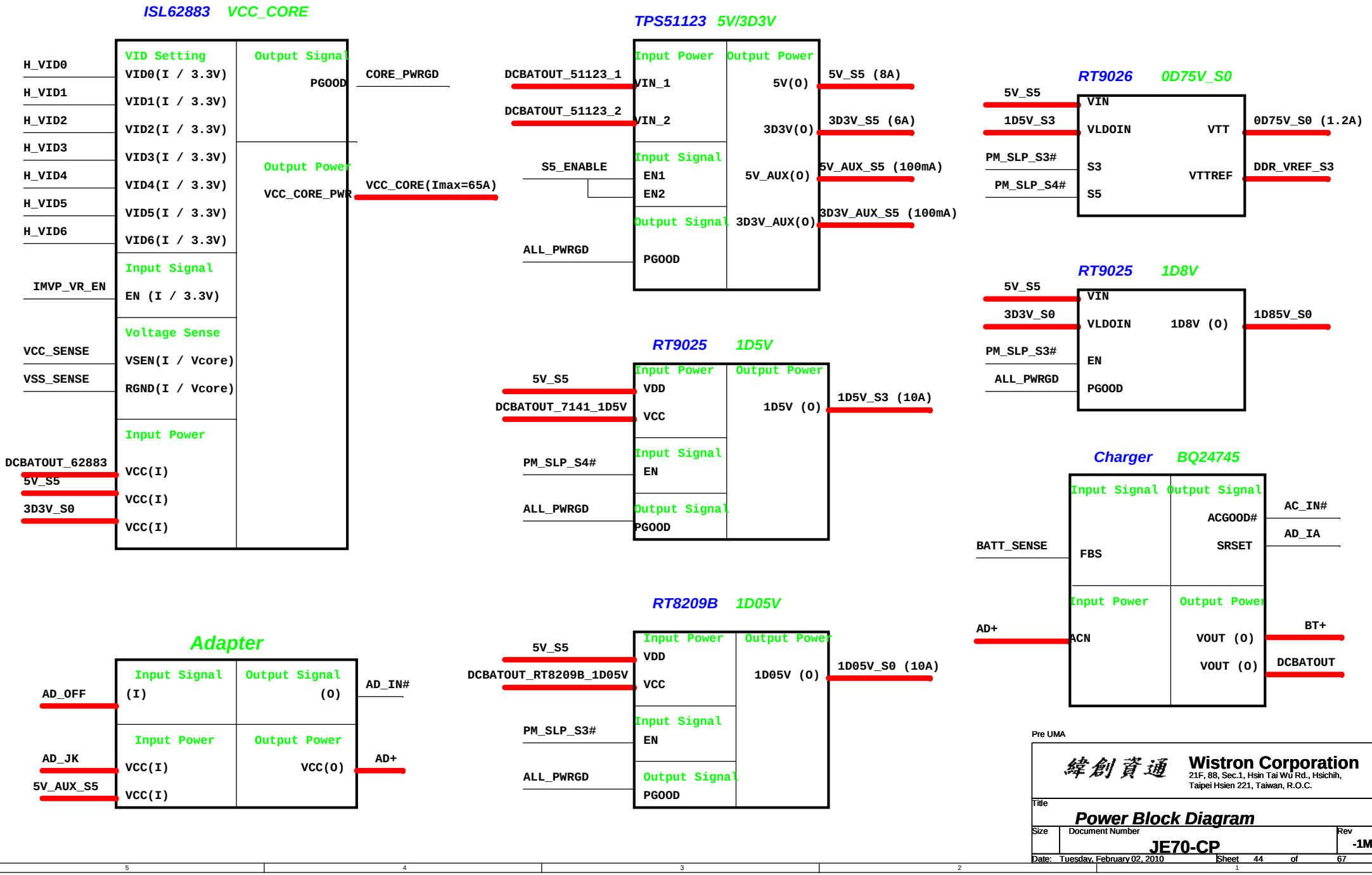






Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RUN POWER and 3D3V_AUX_S5***	
Size	Document Number **JE70-CP**	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 43 of 67	



Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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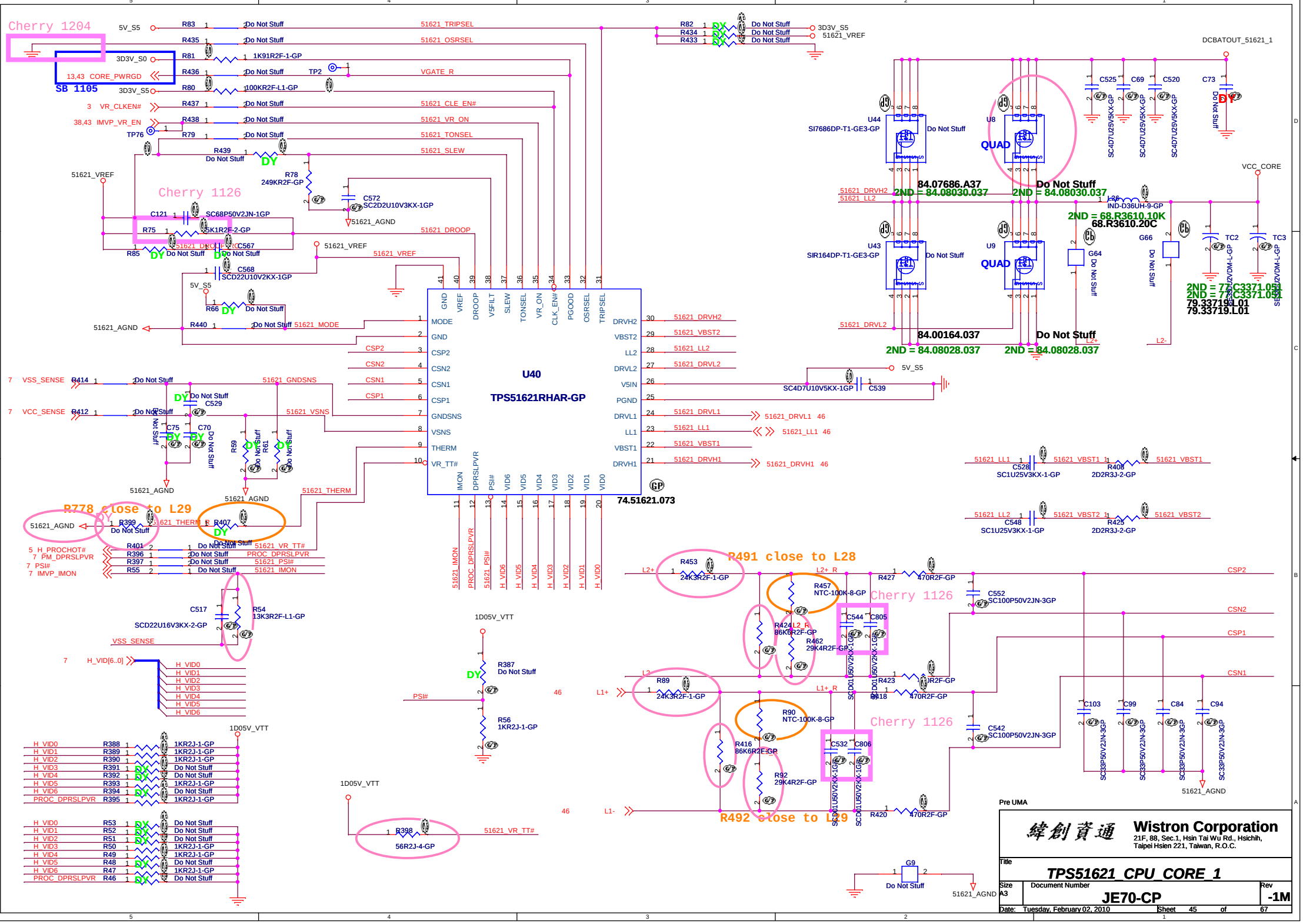
Cherry 1204
SB 1105
Cherry 1126
U40
TPS51621RHAR-GP
74.51621.073
R778 close to L29
R491 close to L28
R492 close to L29
84.07686.A37
2ND = 84.08030.037
84.00164.037
2ND = 84.08028.037
68.R3610.20C
2ND = 68.R3610.10K
79.33719.L01
2ND = 77C3371.051
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51621_CPU_CORE_1
JE70-CP
-1M
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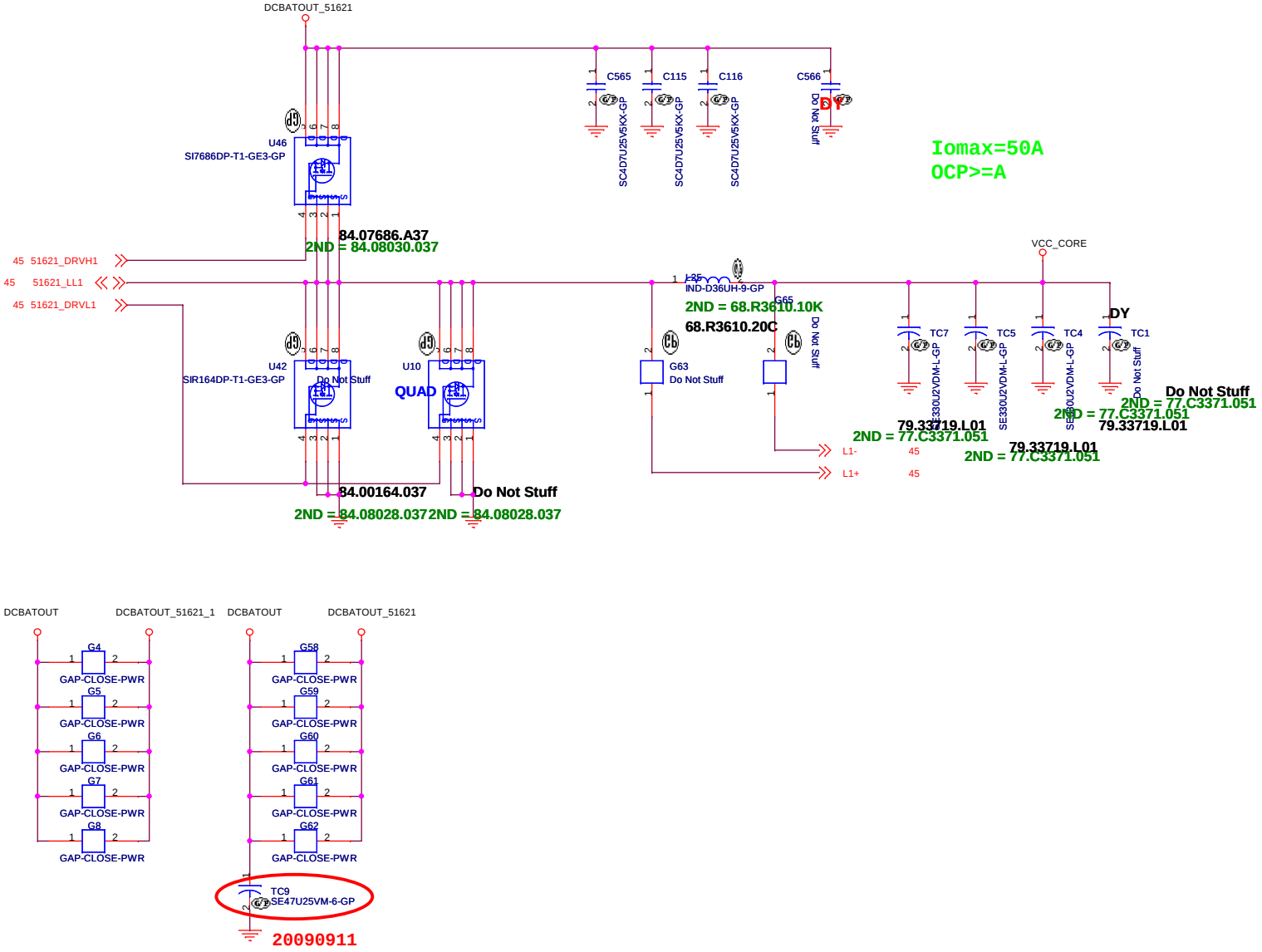
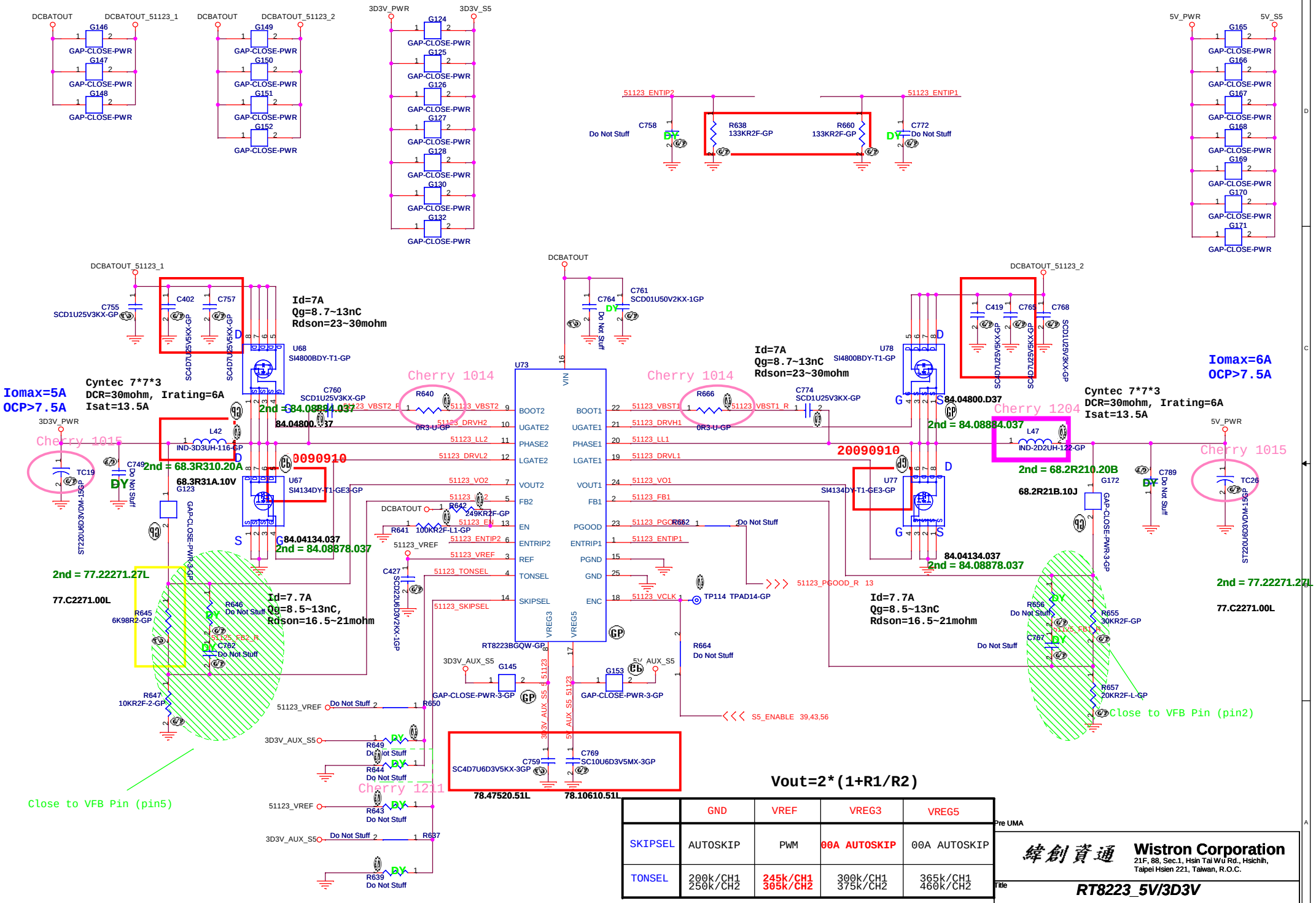
67



Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *ISL62882 CPU CORE (1/2)*		
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 46 of 67	



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

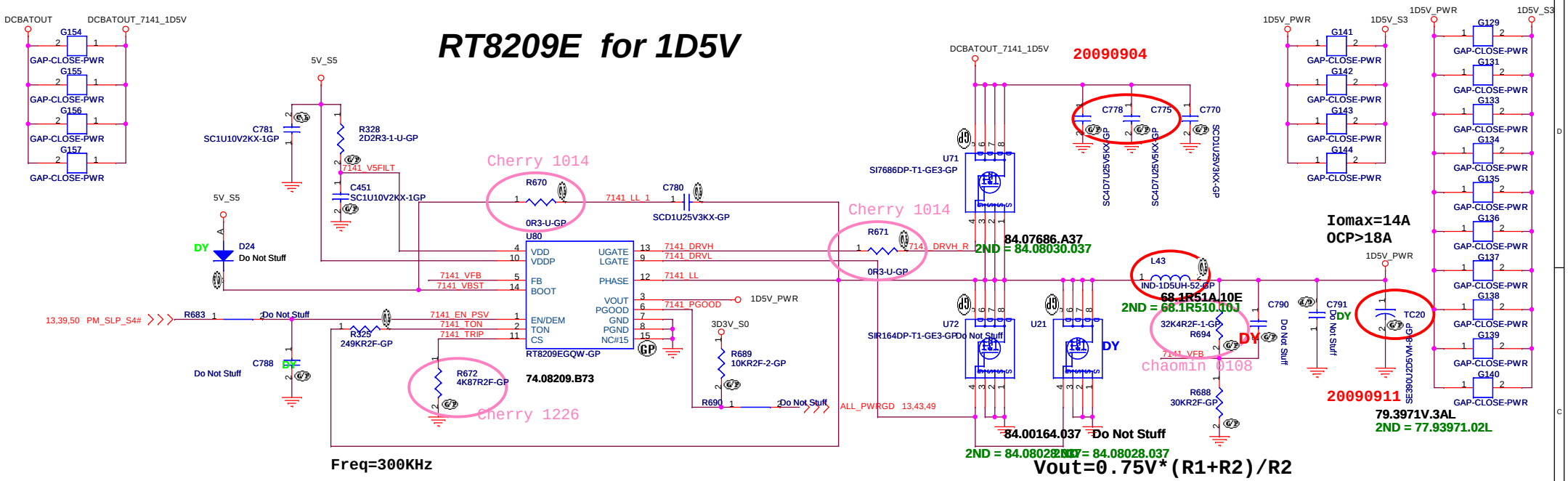
Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223_5V/3D3V

Size: | Document Number: JE70-CP | Rev: -1M

Date: Tuesday, February 02, 2010 | Sheet 47 of 67



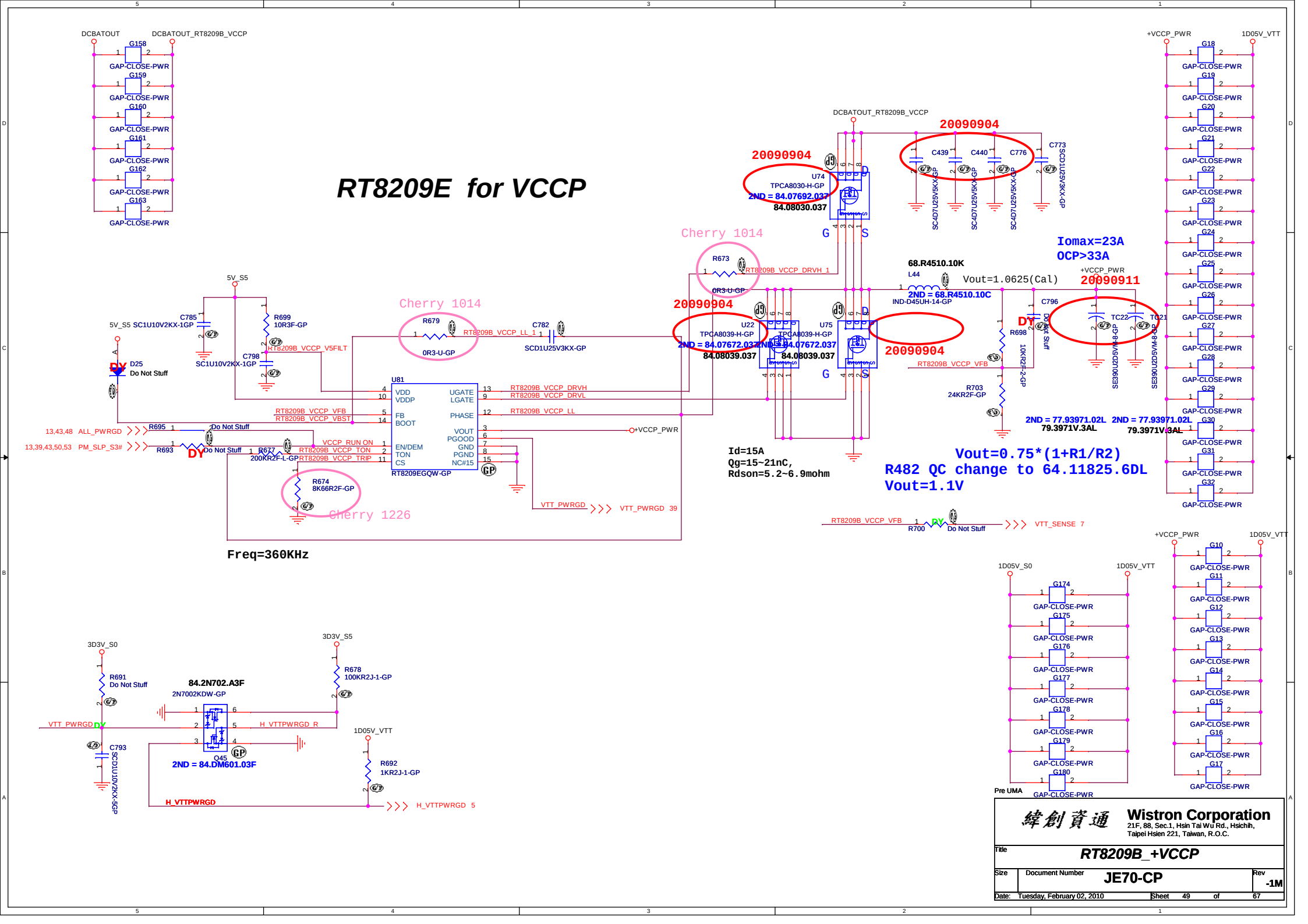
Pre UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

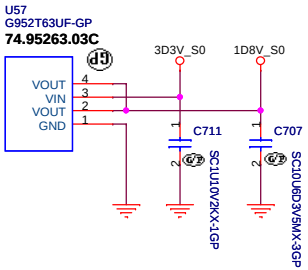
Title: RT8209E 1D5V

Size | Document Number: JE70-CP | Rev: -1M

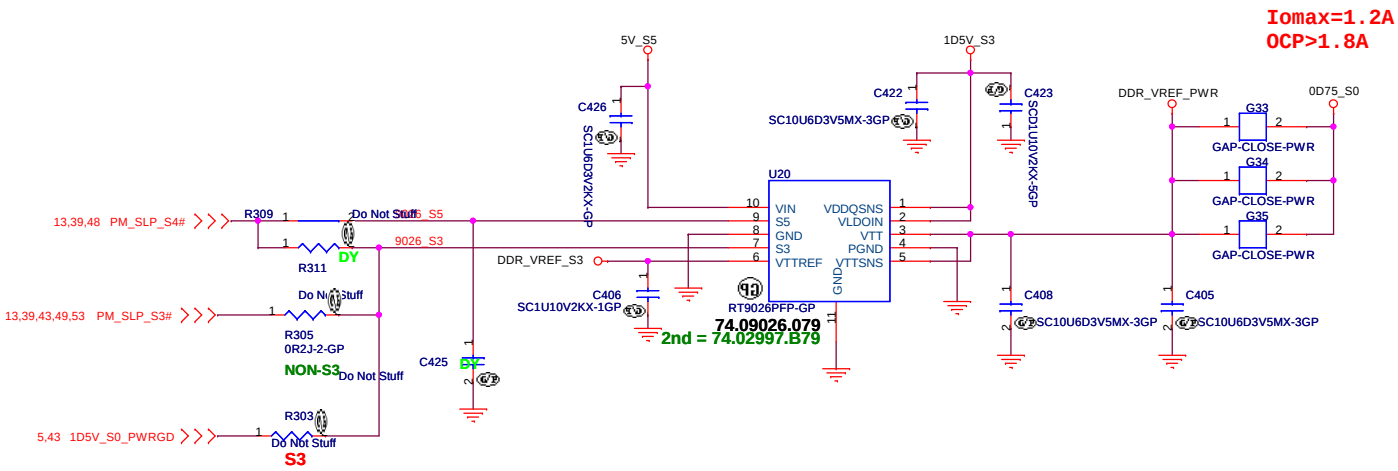
Date: Tuesday, February 02, 2010 | Sheet 48 of 67


RT8209E for VCCP
DCBATOUT
DCBATOUT_RT8209B_VCCP
GAP-CLOSE-PWR
5V_S5
SC1U10V2KX-1GP
R699 10R3F-GP
C798
RT8209B_VCCP_V5FILT
D25 Do Not Stuff
Cherry 1014
R679
0R3-U-GP
RT8209B_VCCP_LL_1
C782
SCD1U25V3KX-GP
U81
VDD
VDDP
FB
BOOT
EN/DEM
TON
CS
UGATE
LGATE
PHASE
VOUT
PGOOD
GND
PGND
NC#15
RT8209EGQW-GP
RT8209B_VCCP_DRVH
RT8209B_VCCP_DRVL
RT8209B_VCCP_LL
RT8209B_VCCP_VFB
RT8209B_VCCP_VBST
RT8209B_VCCP_TON
RT8209B_VCCP_TRIP
VCCP_RUN ON
+VCCP_PWR
R695 Do Not Stuff
R693 Do Not Stuff
R677 200KR2F-L-GP
R674 8K66R2F-GP
Cherry 1226
VTT_PWRGD
VTT_PWRGD 39
13,43,48 ALL_PWRGD
13,39,43,50,53 PM_SLP_S3#
Freq=360KHz
20090904
U74 TPCA8030-H-GP
2ND = 84.07692.037
84.08030.037
C439
C440
C776
C773
SC4D7U25V5KX-GP
SCD1U25V3KX-GP
U22 TPCA8039-H-GP
2ND = 84.07672.037
84.08039.037
U75 TPCA8039-H-GP
2ND = 84.07672.037
84.08039.037
Iomax=23A
OCP>33A
68.R4510.10K
L44
2ND = 68.R4510.10C
IND-D45UH-14-GP
Vout=1.0625(Cal)
20090911
C796 Do Not Stuff
TC22
TC21
SE390U2D5VM-8-GP
R698 10KR2F-2-GP
R703 24KR2F-GP
2ND = 77.93971.02L
79.3971V.3AL
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
Vout=0.75*(1+R1/R2)
R482 QC change to 64.11825.6DL
Vout=1.1V
R700 Do Not Stuff
VTT_SENSE 7
3D3V_S0
3D3V_S5
R691 Do Not Stuff
R678 100KR2J-1-GP
84.2N702.A3F
2N7002KDW-GP
Q45
2ND = 84.DM601.03F
H_VTTPWRGD_R
H_VTTPWRGD
H_VTTPWRGD 5
C793
SCD1U10V2KX-5GP
1D05V_S0
1D05V_VTT
R692 1KR2J-1-GP
+VCCP_PWR
Pre UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8209B_+VCCP
Size
Document Number
JE70-CP
Rev
-1M
Date: Tuesday, February 02, 2010
Sheet 49 of 67

1.8V_S0 1.8V 1A Regulator

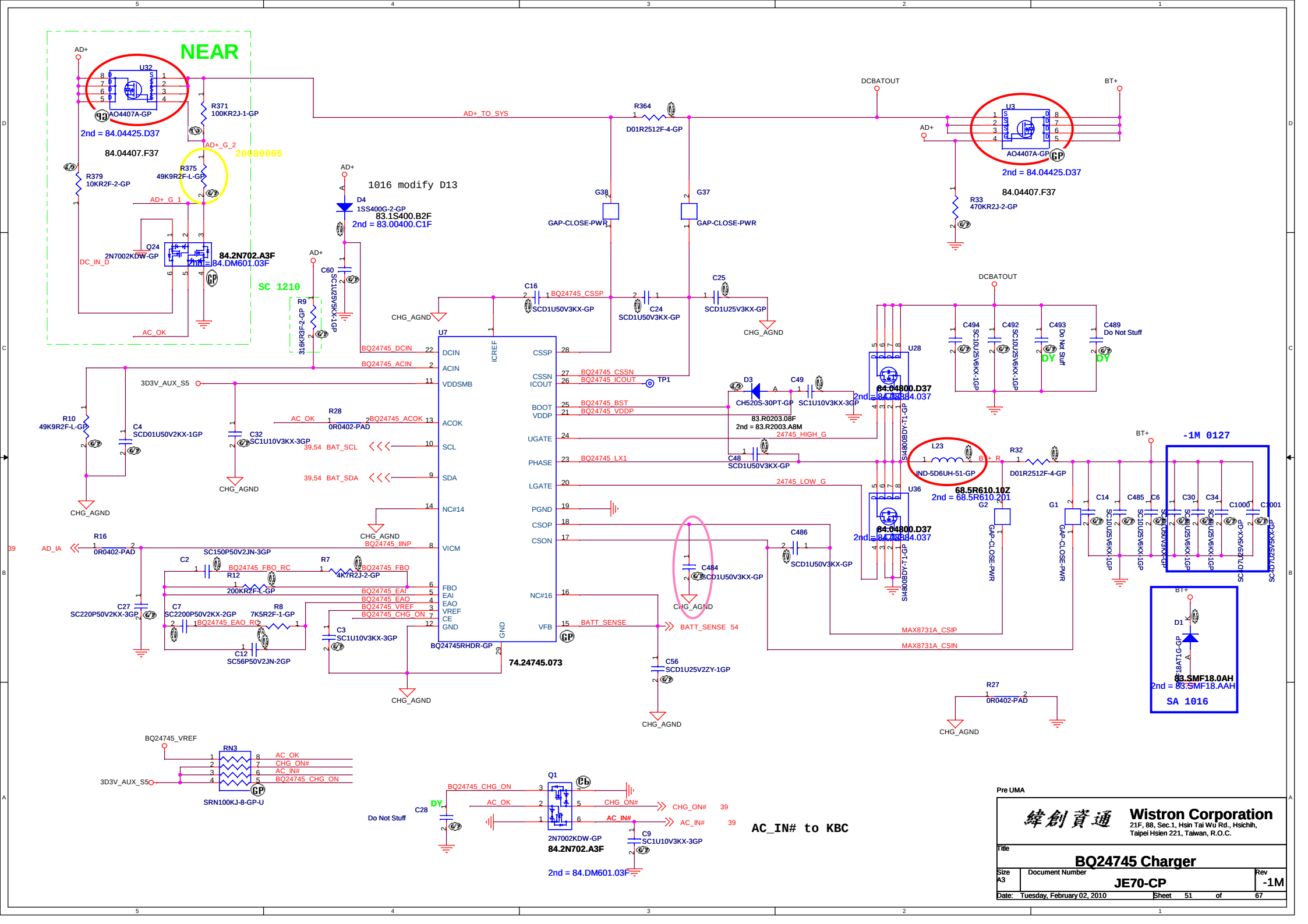


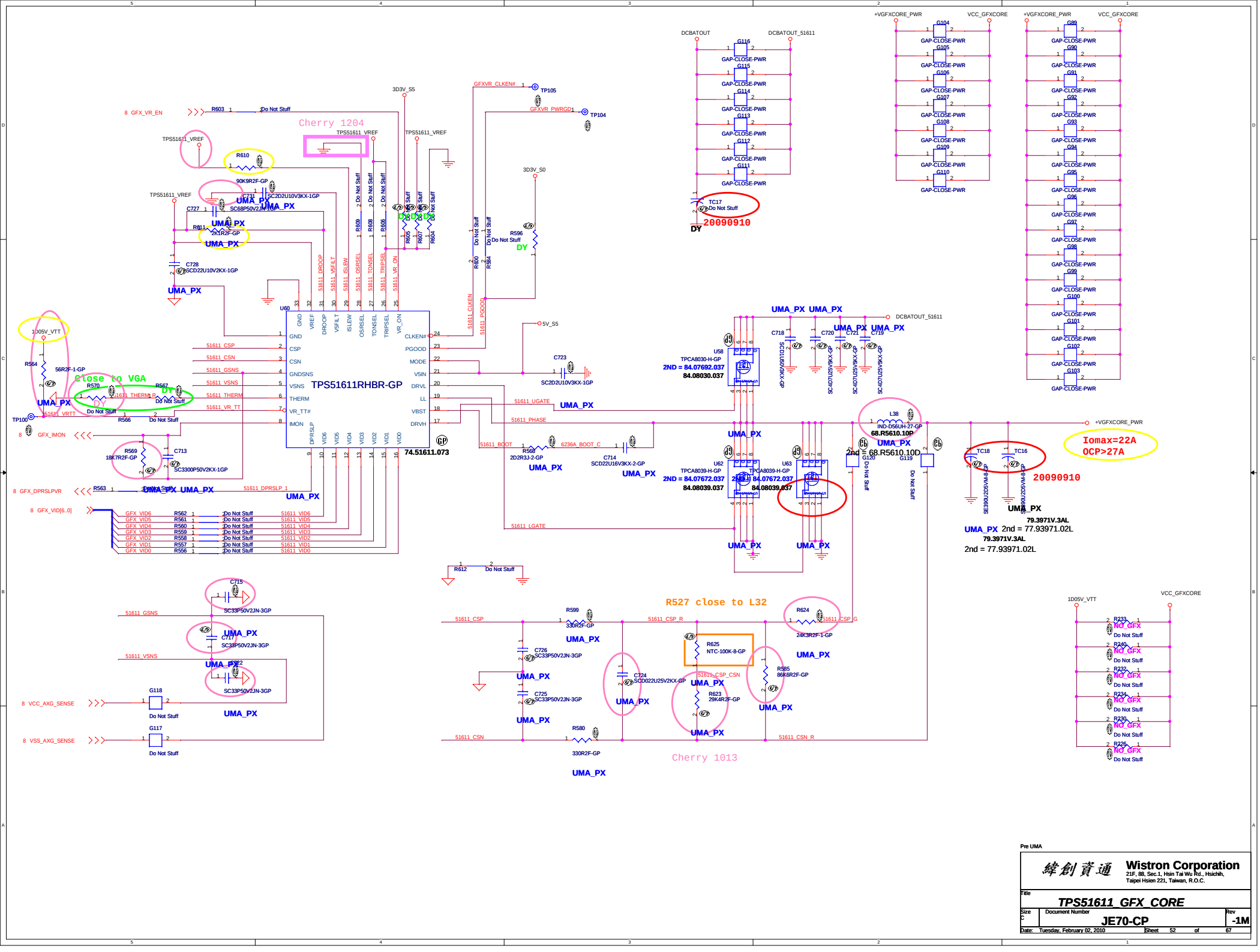
RT9026 for 0D75V_S3



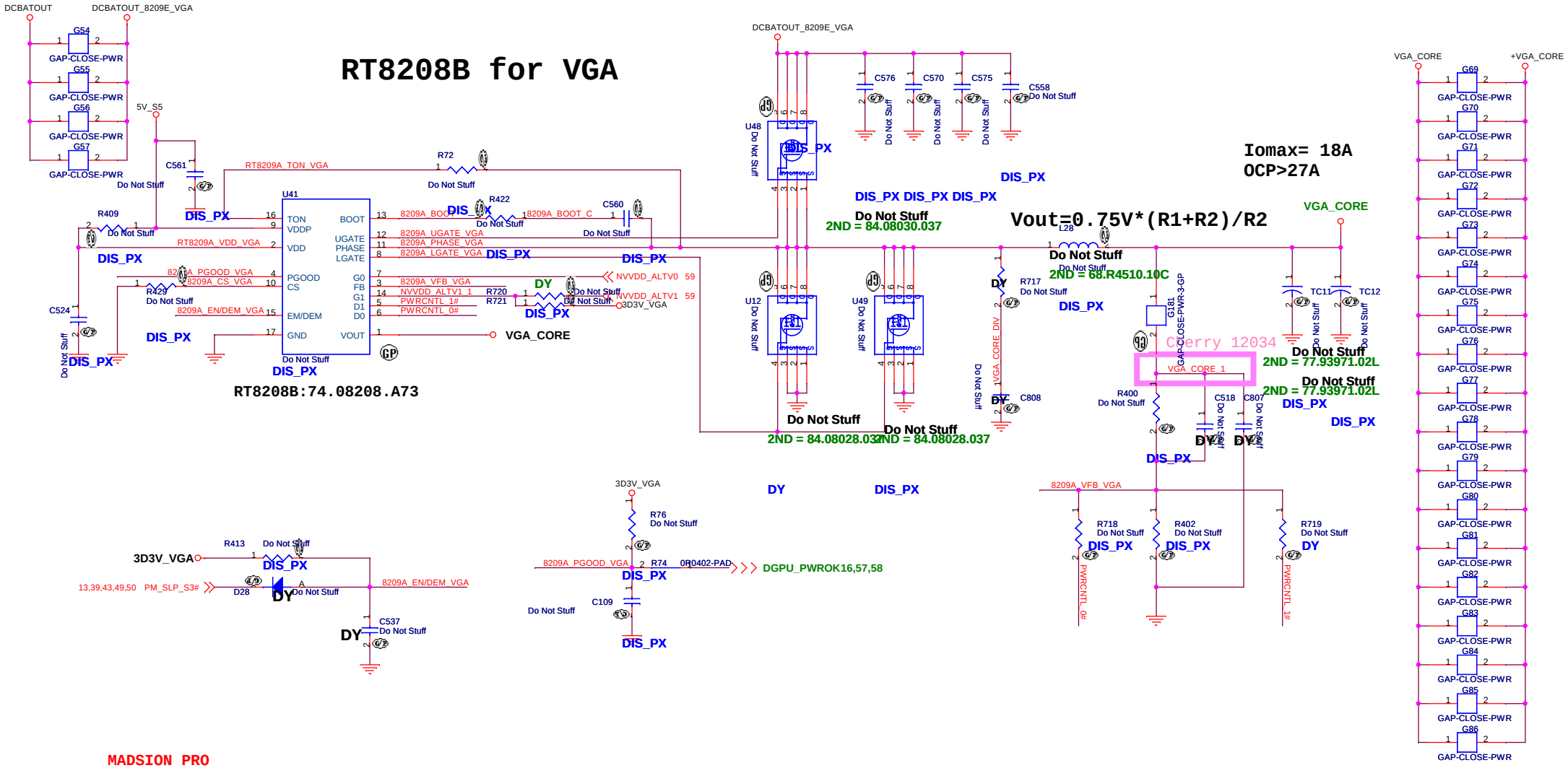
Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8015A for 1D8V/RT9026_0D75		
Size	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 50 of 67	


NEAR
AD+
U32
AO4407A-GP
2nd = 84.04425.D37
84.04407.F37
R371
100KR2J-1-GP
AD+_TO_SYS
R364
D01R2512F-4-GP
DCBATOUT
BT+
U3
AO4407A-GP
2nd = 84.04425.D37
84.04407.F37
R33
470KR2J-2-GP
AD+_G_2
20080605
R379
10KR2F-2-GP
R375
49K9R2F-L-GP
AD+_G_1
Q24
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
DC_IN_D
AC_OK
SC 1210
1016 modify D13
D4
1SS400G-2-GP
83.1S400.B2F
2nd = 83.00400.C1F
C60
SC1U25V5KX-1GP
R9
316KR3F-2-GP
G38
GAP-CLOSE-PWR
G37
GAP-CLOSE-PWR
C16
SCD1U50V3KX-GP
BQ24745_CSSP
C24
SCD1U50V3KX-GP
C25
SCD1U25V3KX-GP
CHG_AGND
U7
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
R10
49K9R2F-L-GP
C4
SCD01U50V2KX-1GP
C32
SC1U10V3KX-3GP
R28
0R0402-PAD
AC_OK
BQ24745_ACOK
39,54 BAT_SCL
39,54 BAT_SDA
BQ24745_CSSN
BQ24745_ICOUT
TP1
BQ24745_BST
BQ24745_VDDP
D3
CH520S-30PT-GP
C49
SC1U10V3KX-3GP
83.R0203.08F
2nd = 83.R2003.A8M
24745_HIGH_G
C48
SCD1U50V3KX-GP
BQ24745_LX1
24745_LOW_G
U28
U36
SI4800BDY-T1-GP
84.04800.D37
2nd = 84.04884.037
L23
IND-5D6UH-51-GP
68.5R610.10Z
2nd = 68.5R610.201
R32
D01R2512F-4-GP
-1M 0127
C494
C492
C493
Do Not Stuff
C489
Do Not Stuff
DY
C14
C485
C6
C30
C34
C1000
C1001
SC10U25V6KX-1GP
SC1U25V3KX-GP
SCD1U25V5KX-GP
R16
0R0402-PAD
AD_IA
SC150P50V2JN-3GP
BQ24745_IINP
C2
R12
200KR2F-L-GP
BQ24745_FBO_RC
R7
4K7R2J-2-GP
BQ24745_FBO
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
C27
SC220P50V2KX-3GP
C7
SC2200P50V2KX-2GP
R8
7K5R2F-1-GP
BQ24745_EAO_RC
C12
SC56P50V2JN-2GP
C3
SC1U10V3KX-3GP
BQ24745RHDR-GP
74.24745.073
C484
SCD1U50V3KX-GP
C486
SCD1U50V3KX-GP
C56
SCD1U25V2ZY-1GP
BATT_SENSE
BATT_SENSE 54
MAX8731A_CSIP
MAX8731A_CSIN
R27
0R0402-PAD
D1
18AT1G-GP
83.SMF18.0AH
2nd = 83.SMF18.AAH
SA 1016
BQ24745_VREF
RN3
SRN100KJ-8-GP-U
3D3V_AUX_S5
AC_OK
CHG_ON#
AC_IN#
BQ24745_CHG_ON
Q1
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
C28
Do Not Stuff
C9
SC1U10V3KX-3GP
CHG_ON#
AC_IN#
AC_IN# to KBC
Pre UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size
A3
Document Number
JE70-CP
Rev
-1M
Date: Tuesday, February 02, 2010
Sheet 51 of 67


Cherry 1204
TPS51611_VREF
TPS51611RHBR-GP
74.51611.073
close to VGA
DY
20090910
Iomax=22A
OCP>27A
R527 close to L32
Cherry 1013
Wistron Corporation
TPS51611_GFX_CORE
JE70-CP
-1M
Tuesday, February 02, 2010

RT8208B for VGA



MADSION PRO

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

PARK XT

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V

Park==>R718=33K (64.33025.6DL)
Madison==>R718=71.5K (64.71525.6DL)

NVVDD_ALTV1	NVVDD_ALTV0	+VGA_CORE
H	L	1.12V or 1V OUT=[R400+(R402//R718)}/(R402//R718)
H	H	0.9V OUT=(R400+R402)/R402

Pre UMA

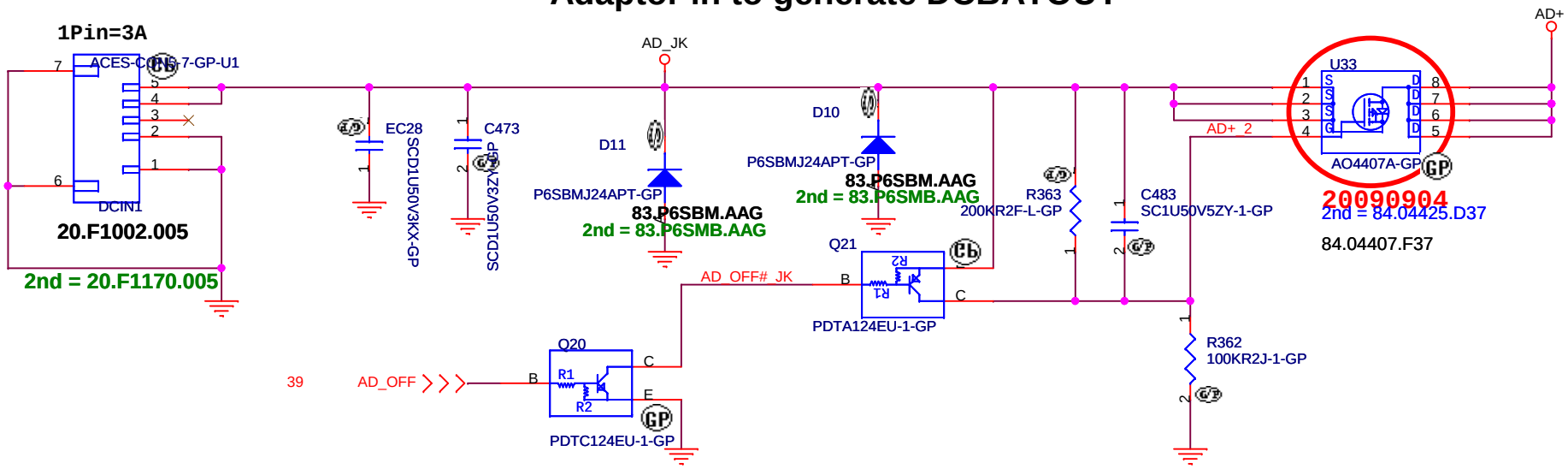
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E VGA CORE

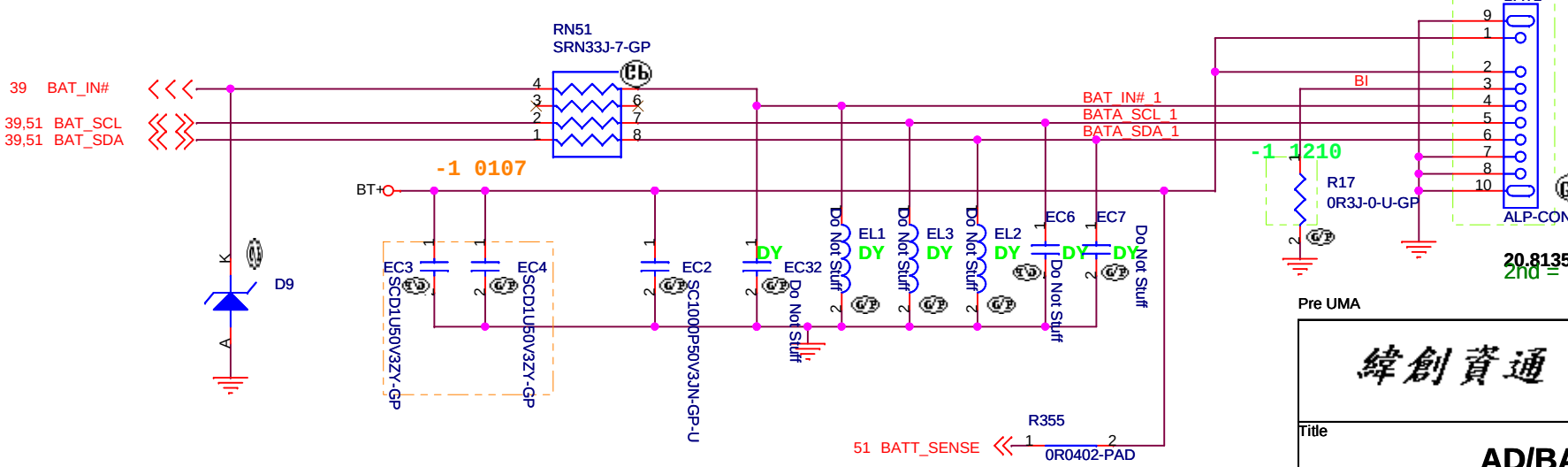
Size: A3 | Document Number: JE70-CP | Rev:

Date: Tuesday, February 02, 2010 | Sheet 53 of 67

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Pin NO	Symbol
1	GND
2	GND
3	SMD
4	SMC
5	TS
6	B/I
7	BT+
8	BT+

Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
	JE70-CP	-1M

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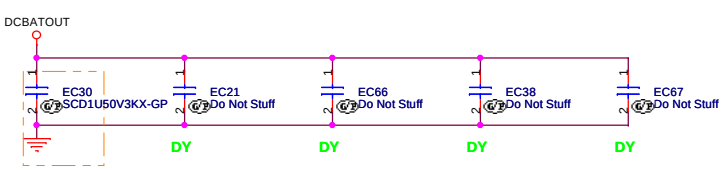
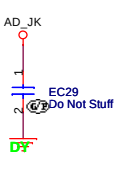
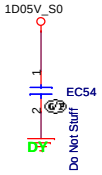
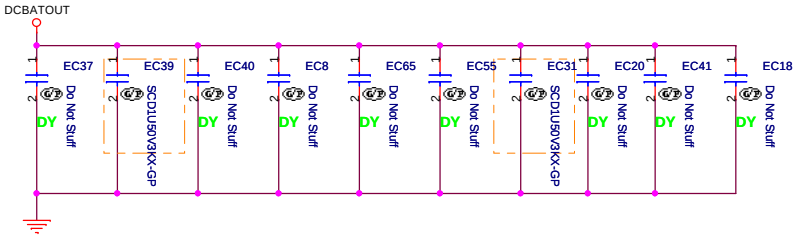
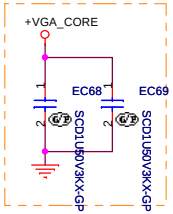


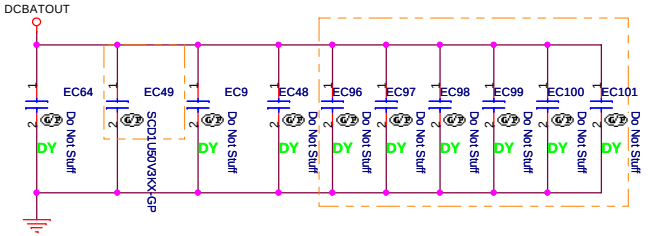




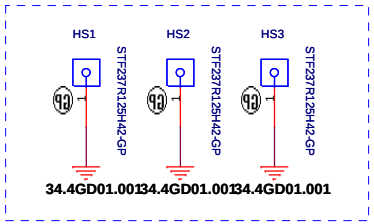


SB 1120

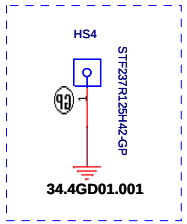




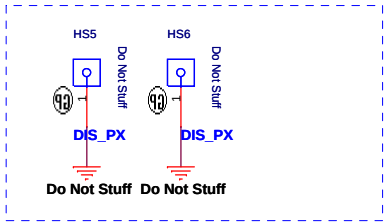
CPU



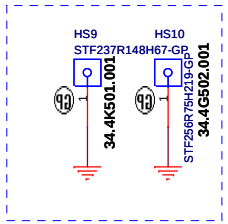
PCH

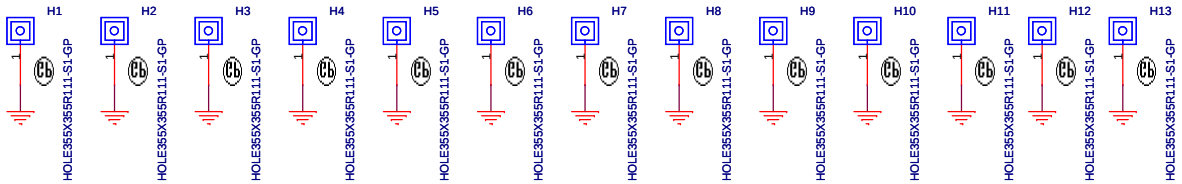


VGA



MINICARD



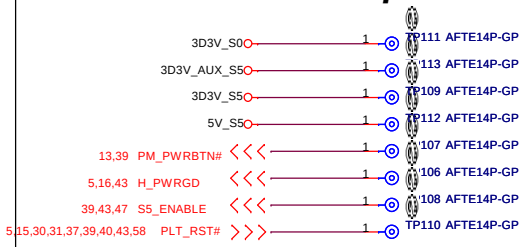


Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***EMI/Spring/Boss***	
Size	Document Number **JE70-CP**	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 55 of 67	

Check test point



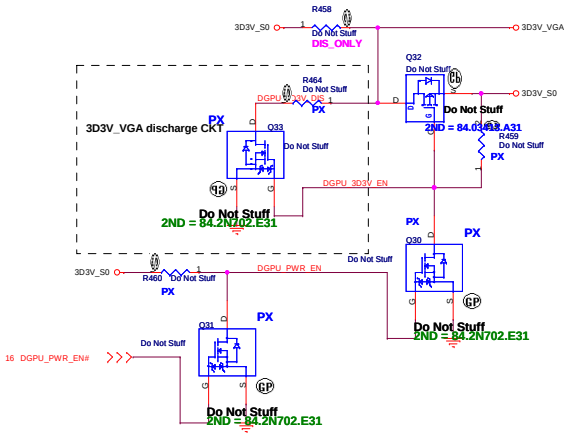
Test Point放在Dimm Door打開可量測處

Pre UMA

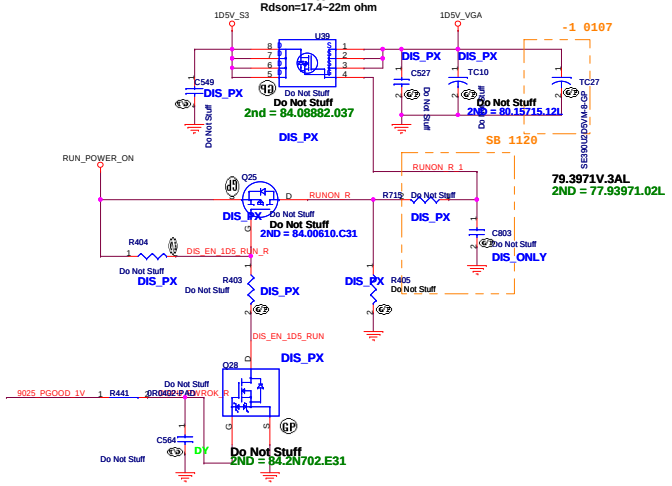
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AFTE_TP***	
Size	Document Number **JE70-CP**	Rev **-1M**
Date: Tuesday, February 02, 2010	Sheet 56 of 67	

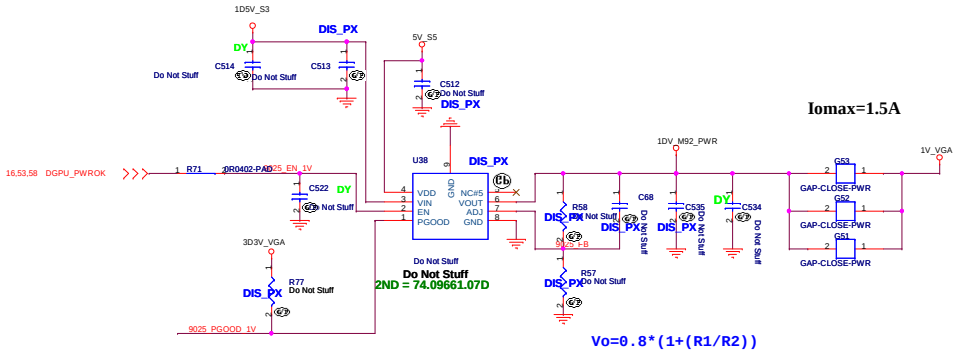
+3VS to 3.3V_DELAY Transfer



AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm



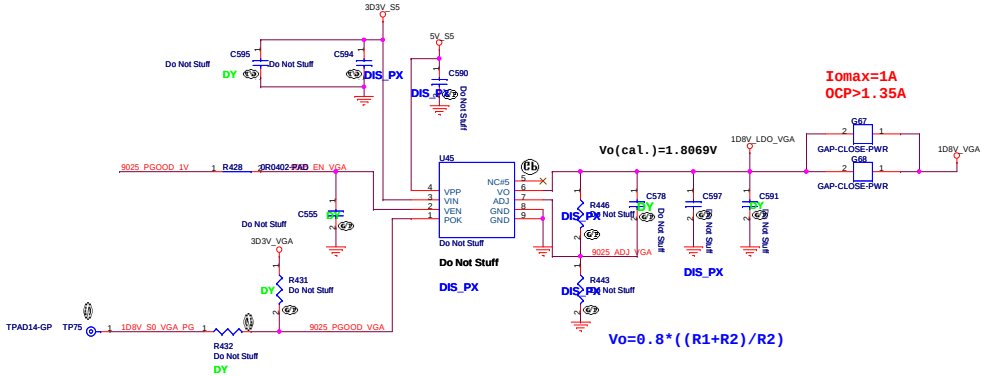
RT9025 for 1V_VGA



Iomax=1.5A

Vo=0.8*(1+(R1/R2))

G9661 for 1D8V_VGA



Iomax=1A
OCP>1.35A

Vo(cal.)=1.8069V

Vo=0.8*((R1+R2)/R2)

Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI_POWER

Size	Document Number	Rev
A2	JE70-CP	-1M

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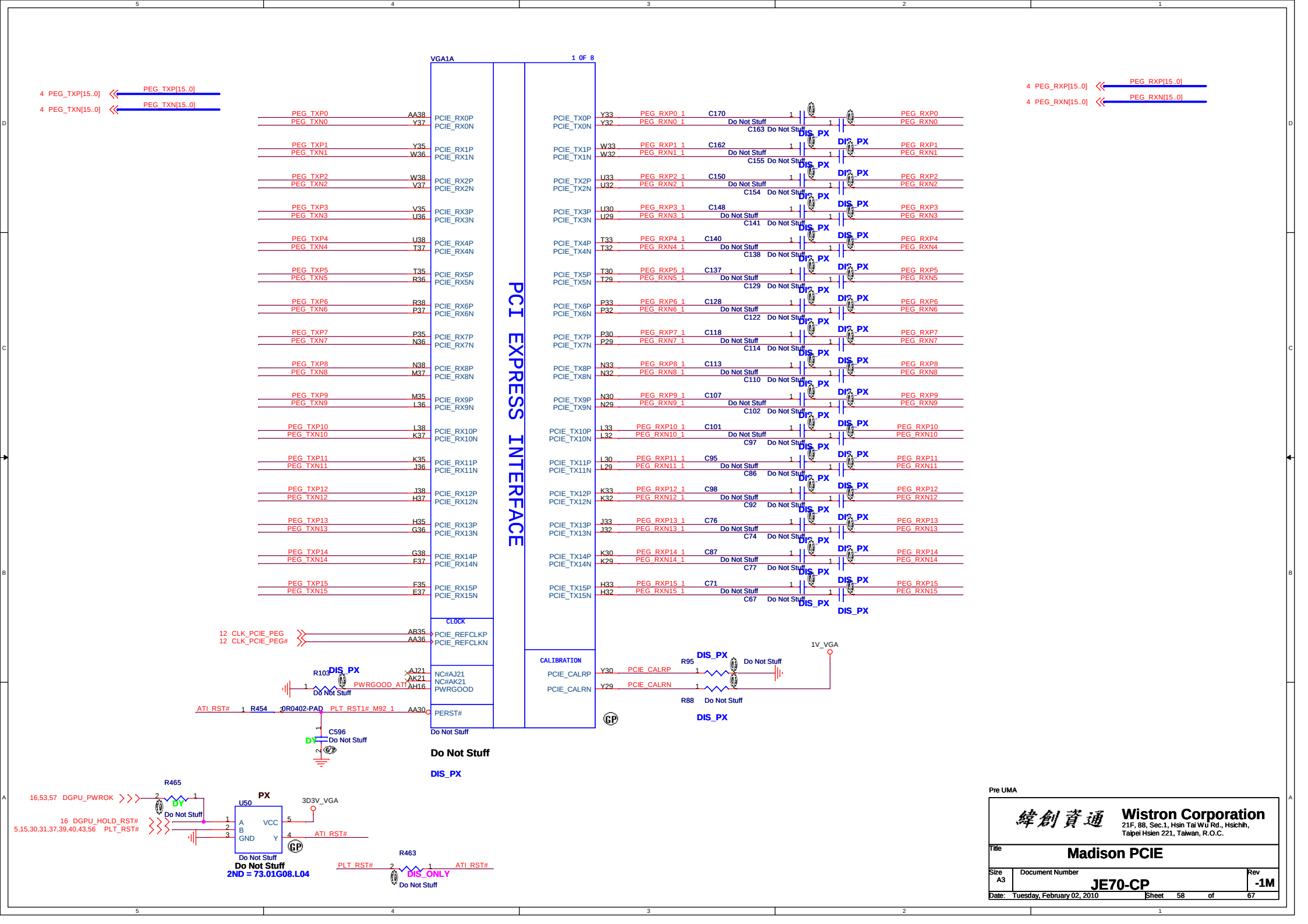

Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Madison PCIE		
Size: A3	Document Number: JE70-CP	Rev: -1M
Date: Tuesday, February 02, 2010	Sheet 58 of 67	

Layout notice:
It should be pleace near HDMI connector

JV50-CP_JV70-CP_SJV50-CP / Madsion-Pro

0 1 0 0 Hynix Orion-die (H5TQ1G63BFR-12C, 800MHz)64*16 x 8 pcs2GB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 8 pcs1GB
1 1 0 0 Reserve64*16 x 8 pcs1GB

JV50-CP_JV70-CP_SJV50-CP / Park-XT

0 1 0 0 Hynix Orion-die (H5TQ1G63BFR-12C, 800MHz)64*16 x 4 pcs512MB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 4 pcs512MB
1 1 0 0 Reserve64*16 x 4 pcs512MB

It's strap for GDDR3-136ball
Need to Clarify

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

SB 1118

For Thermal sensor

SB 1120

SB 1117

Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: Madison IO			
Size: A2	Document Number: JE70-CP	Rev: SB	
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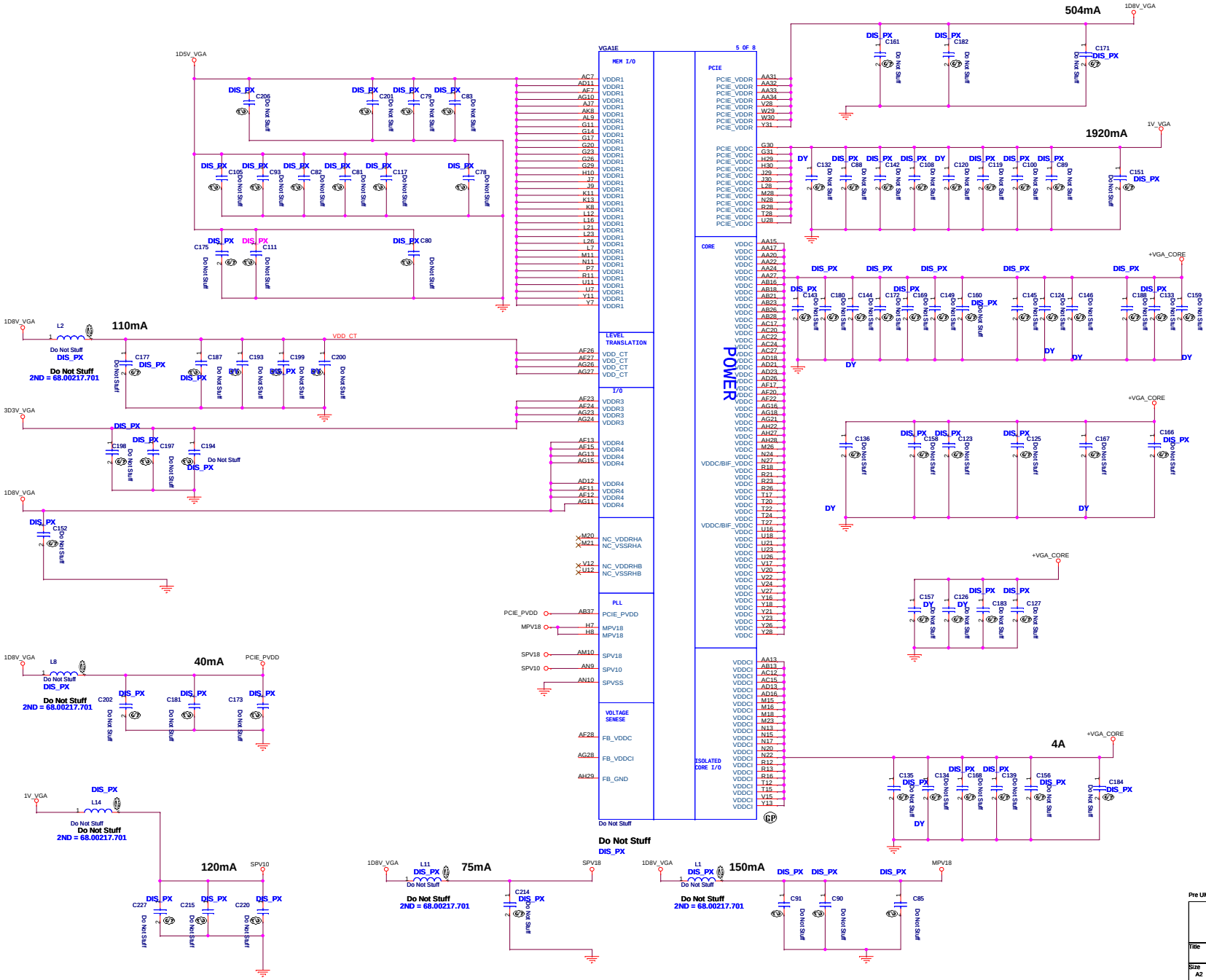
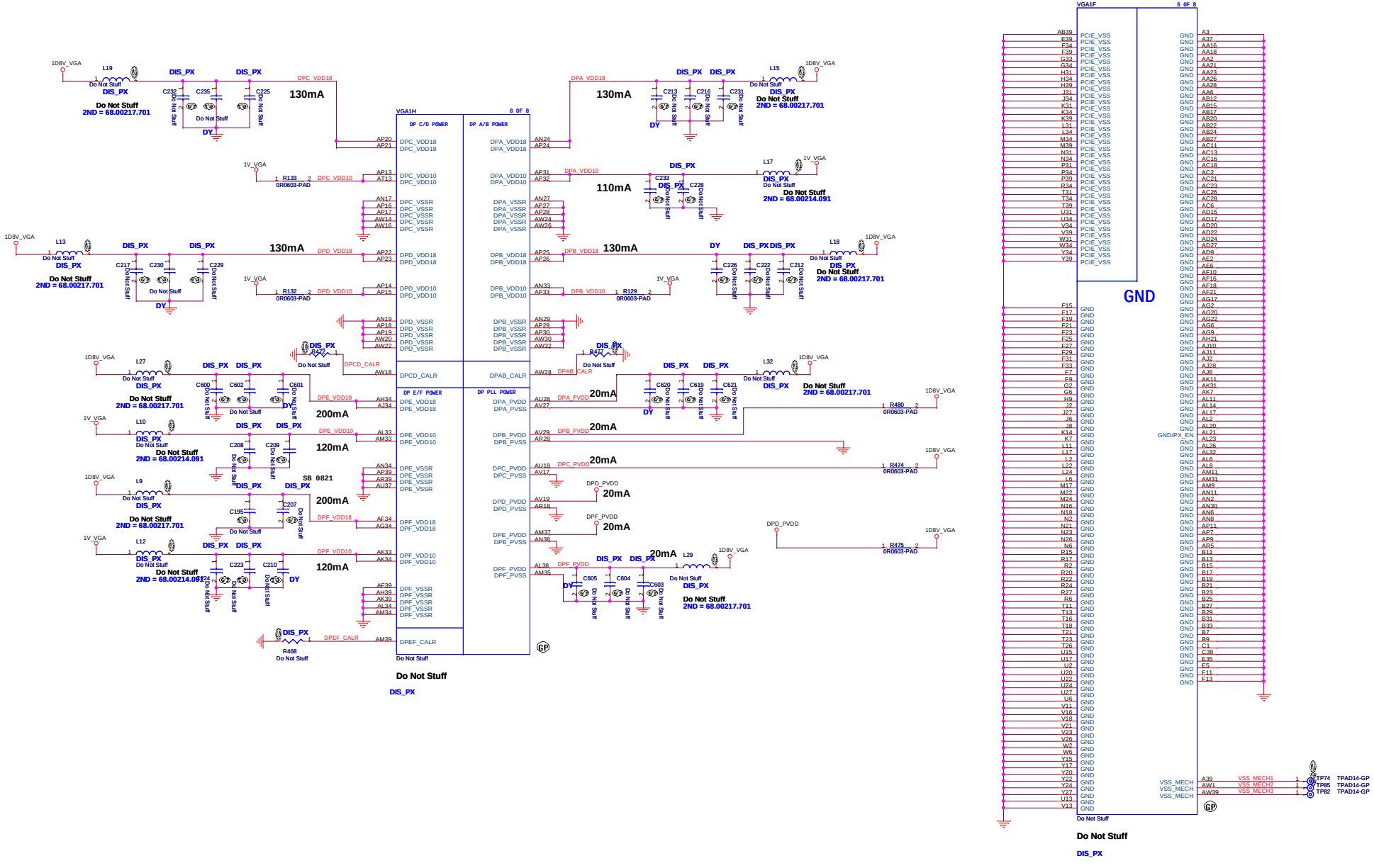


Pre UMA

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Madison POWER
Size A2 / Document Number	JE70-CP
Rev	-1M
Date: Tuesday, February 02, 2010	Sheet 60 of 67



Pre UMA

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	DP POWER_GND	
Size: A2	Document Number: JE70-CP	Rev: -1M
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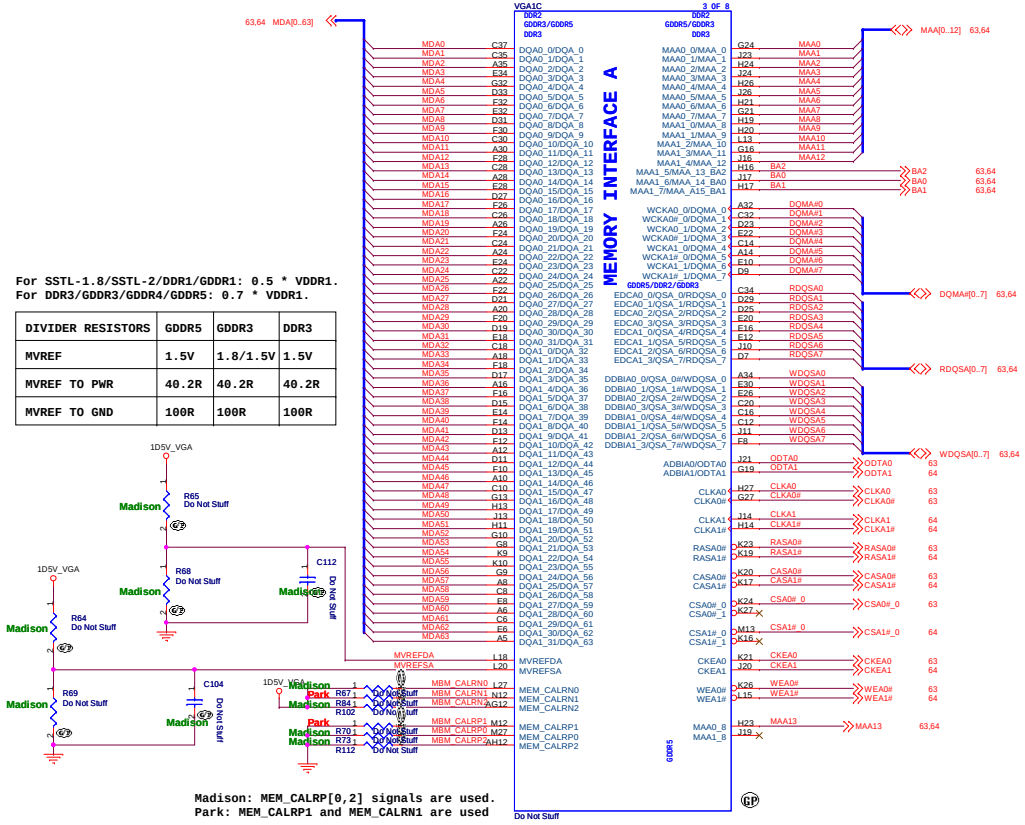
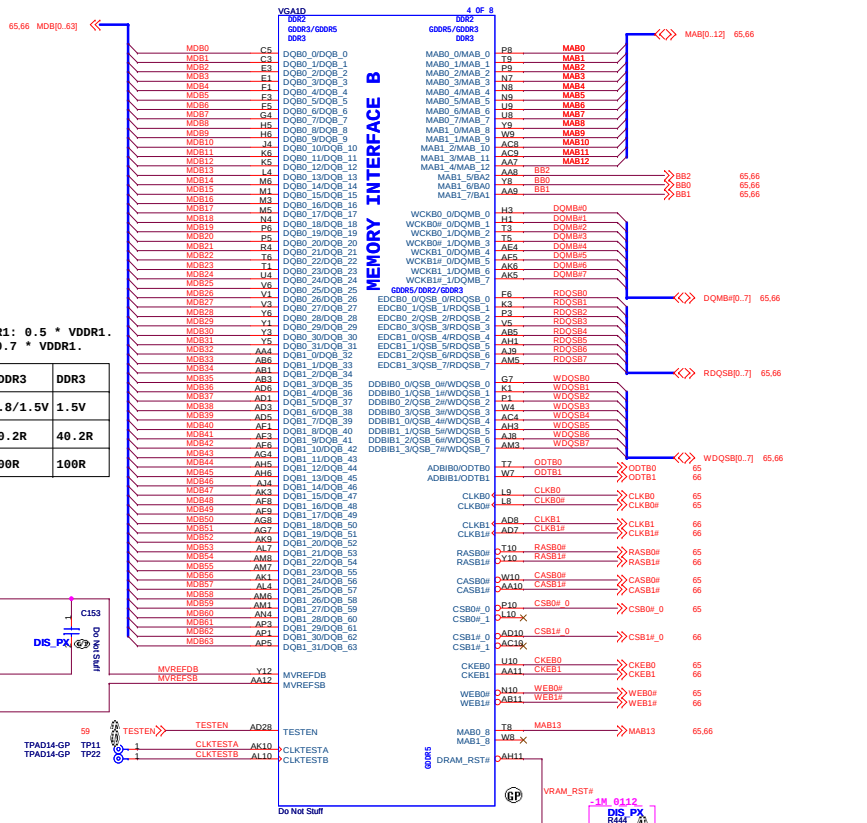


DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

Pre UMA

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Title: Madison Memory / Straps

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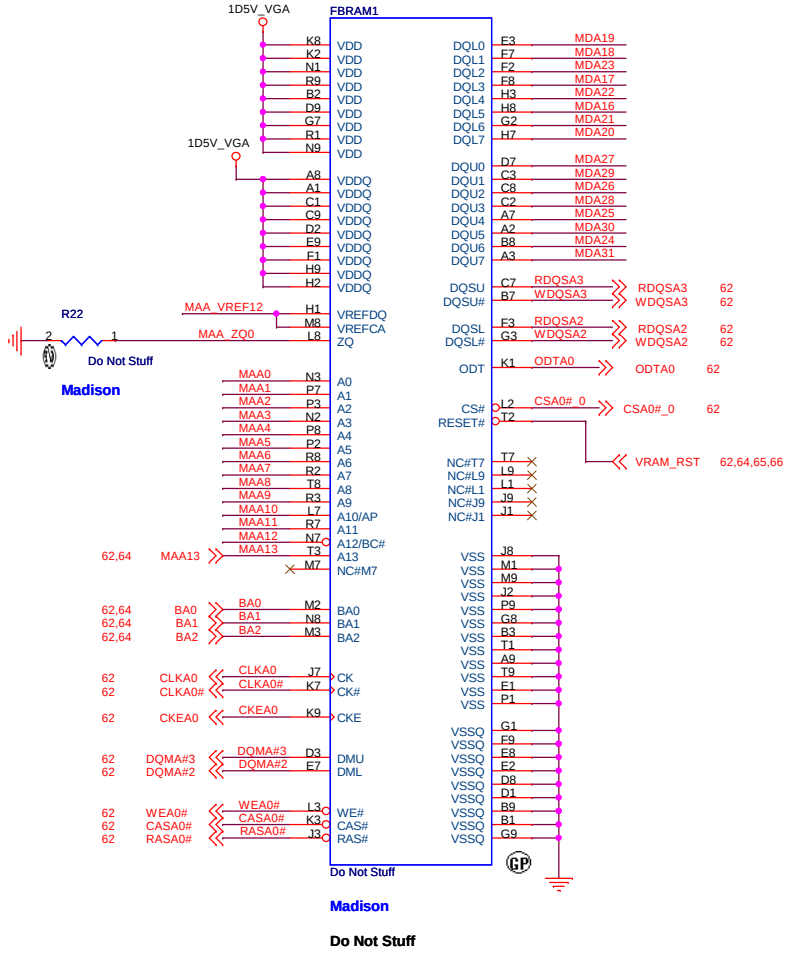
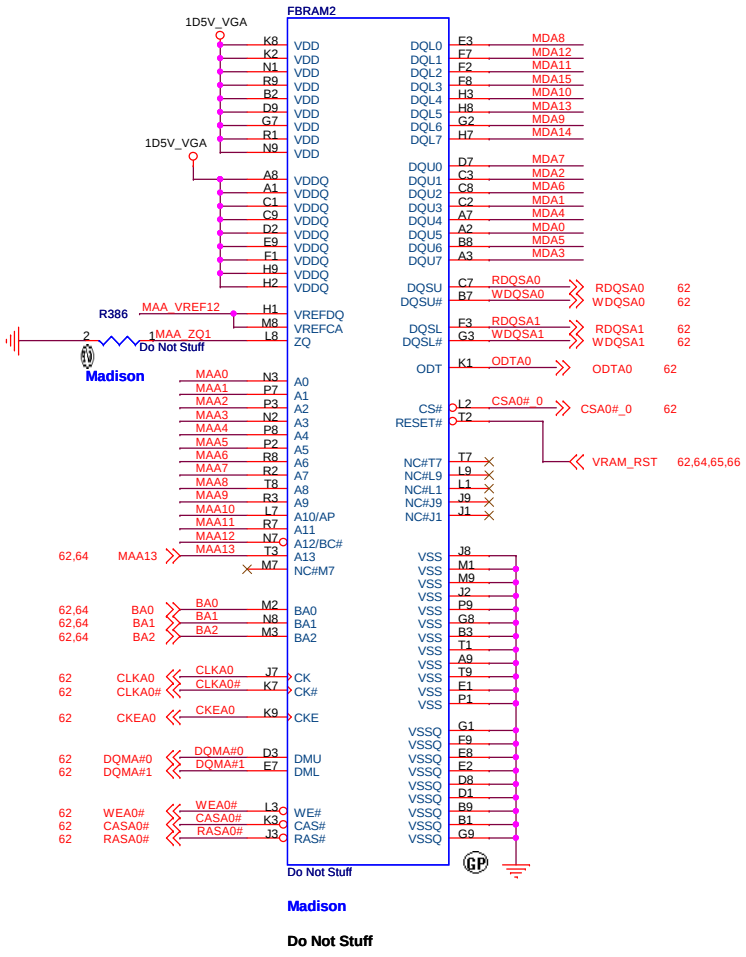
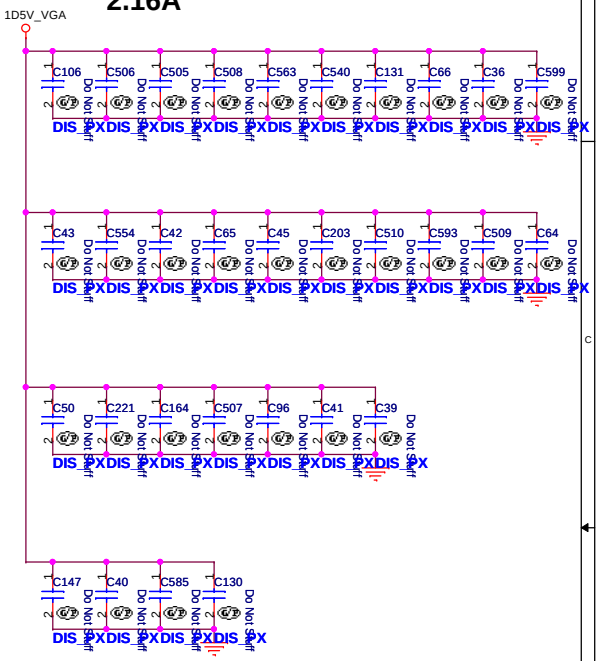
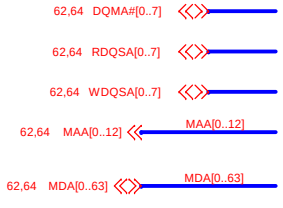
DDR3

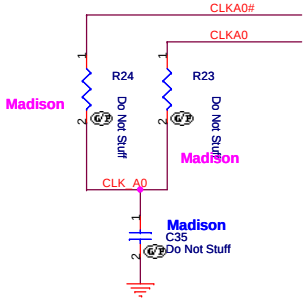


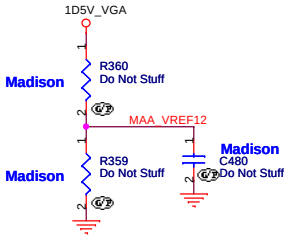




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U







Pre UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***VRAM(1/4)***	
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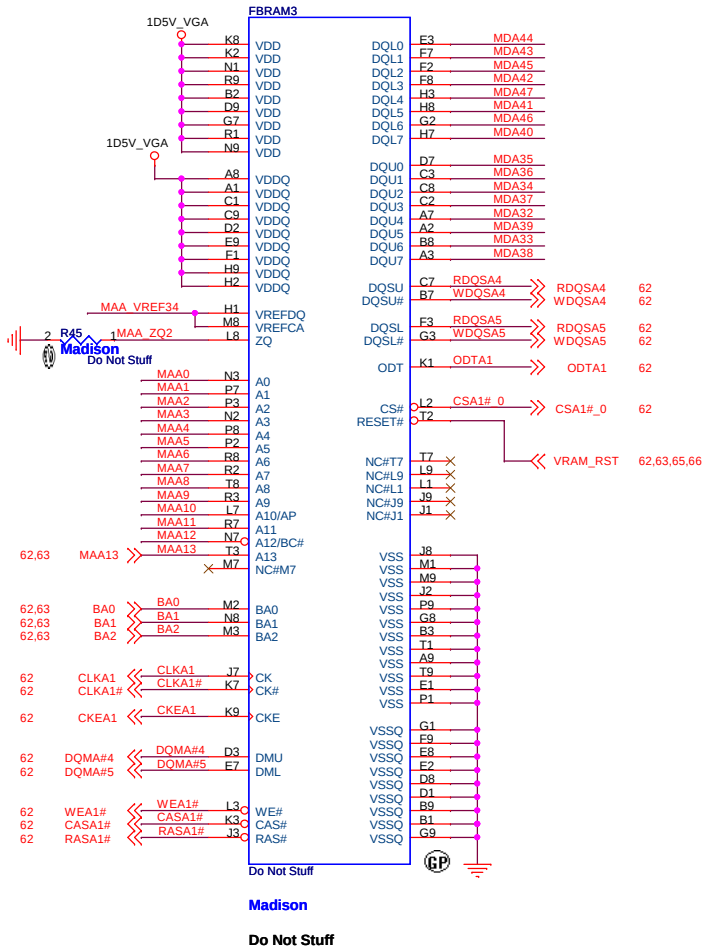
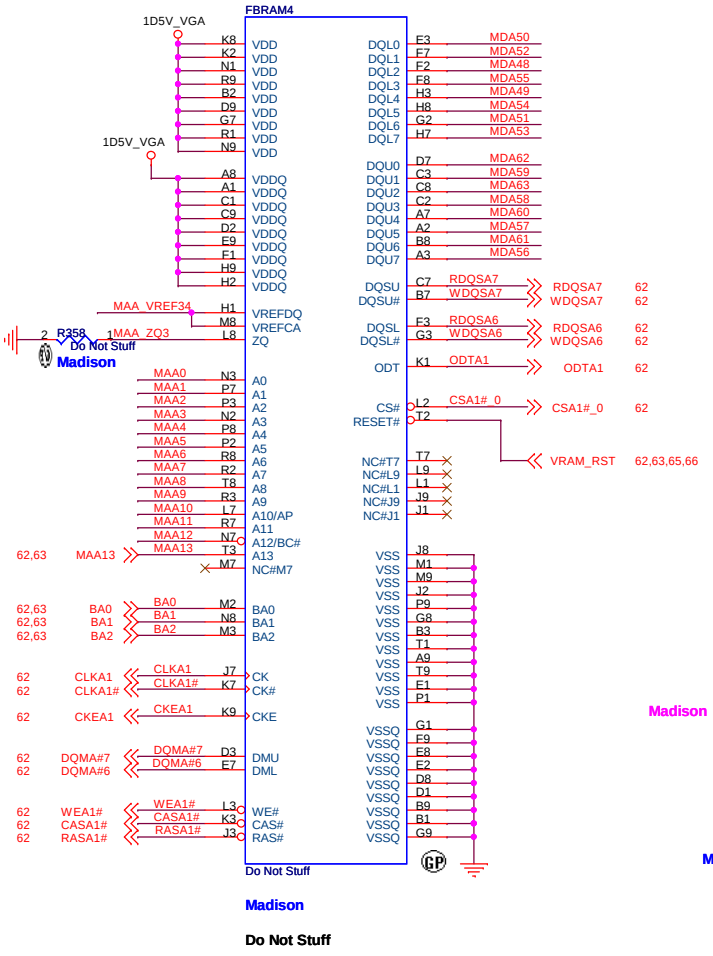
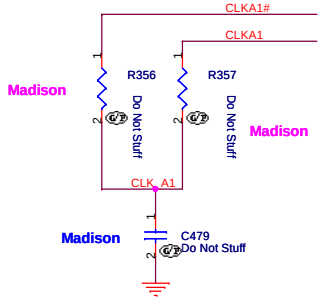
DDR3

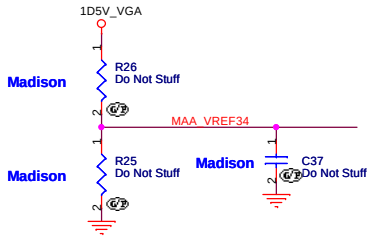






SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

62,63 DQMA#[0..7]
62,63 RDQSA[0..7]
62,63 WDQSA[0..7]
62,63 MAA[0..12] MAA[0..12]
62,63 MDA[0..63] MDA[0..63]



Pre UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(2/4)***	
Size A3	Document Number **JE70-CP**	Rev **-1M**
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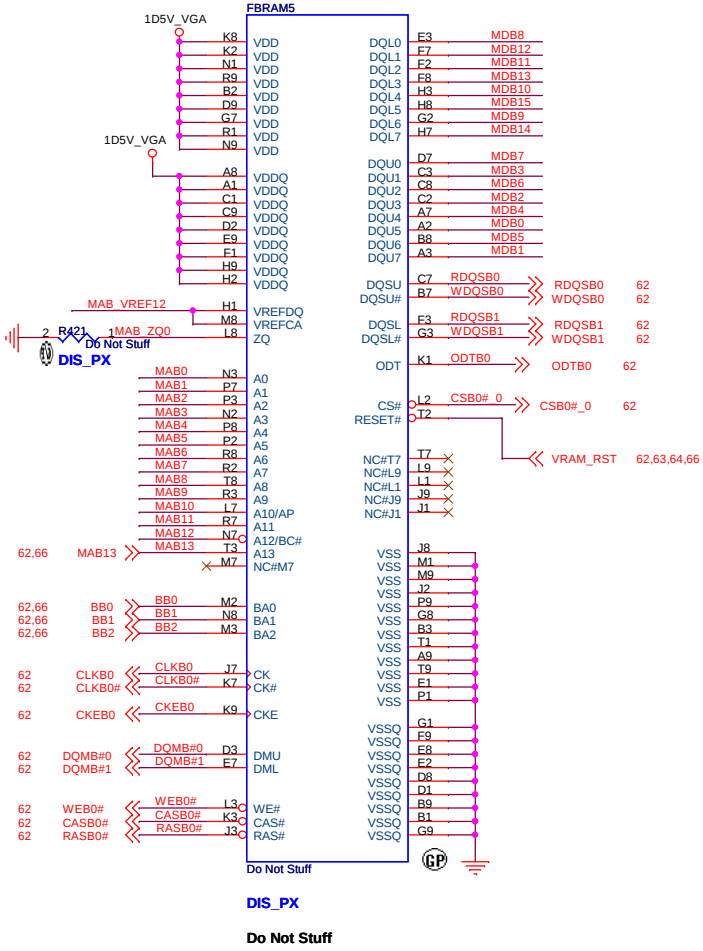
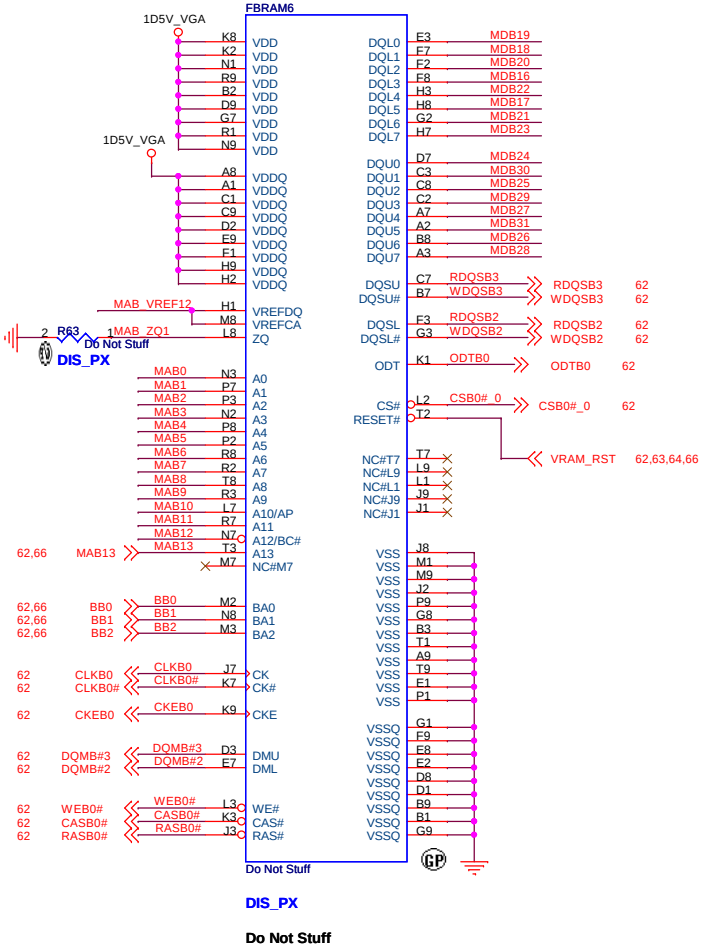
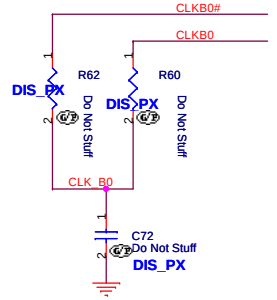
DDR3







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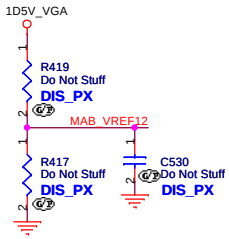
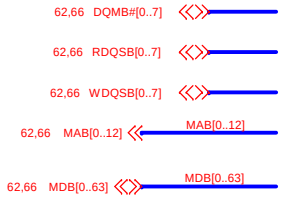
HYNIX: 72.51G63.C0U





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Title	*VRAM(3/4)*	
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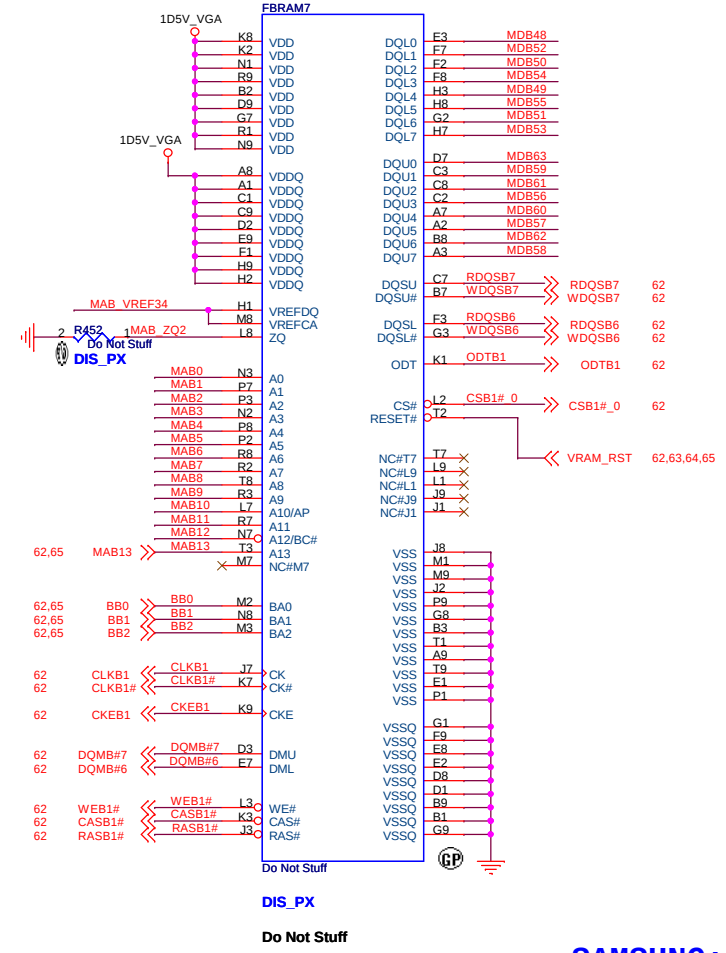
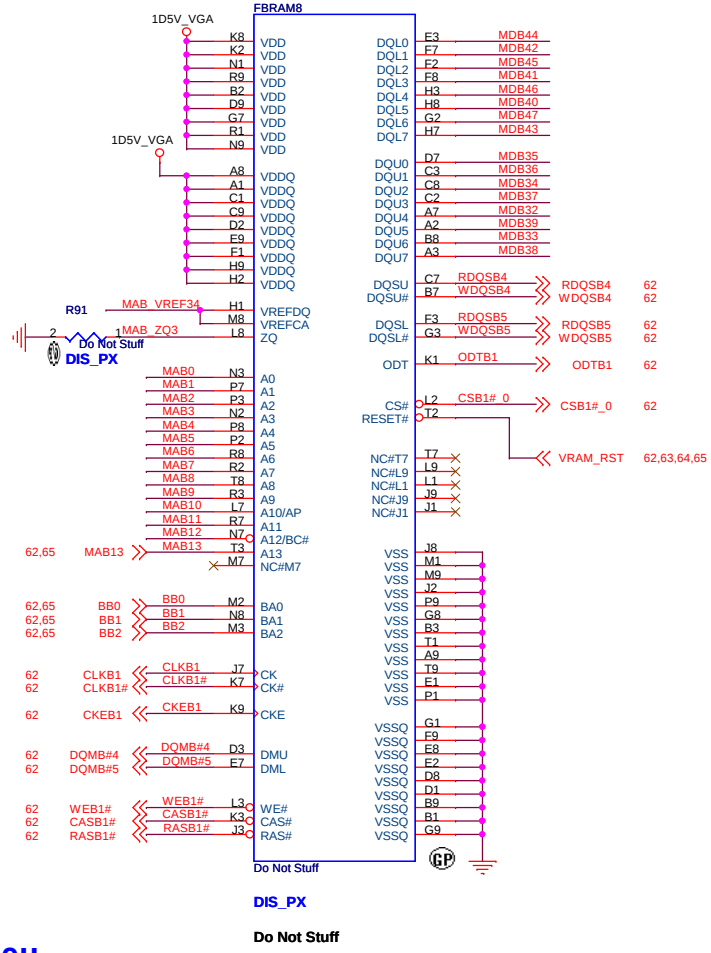
DDR3





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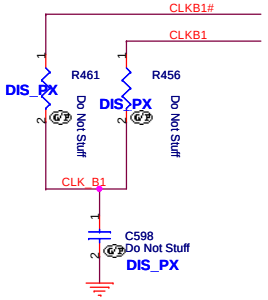

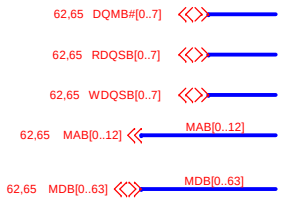

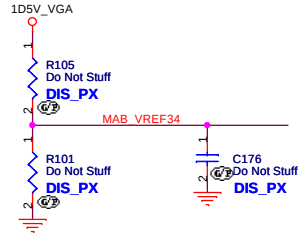

Pre UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM(4/4)		
Size: A3	Document Number: JE70-CP	Rev: -1M
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Pre UMA

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Modify History

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