Roberts Discrete VGA ATI M92LP-S2 Schematics Document

uFCPGA Mobile Penryn

Intel PM45 + ICH9M

2009-05-19

REV :-1

DY : Nopop Component

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*

Size: Custom | Document Number: *Roberts Discrete* | Rev: *-1*

Date: Tuesday, May 19, 2009 | Sheet 1 of 60

Roberts Discrete Block Diagram

Project code : 91.4AQ01.001
PCB P/N : 48.4AQ12.011
Revision : 08224-1

Clock Generator
SLG8SP513VTR
19

Intel Mobile CPU
Penryn
Socket P
4,5,6

FSB
800/1066MHz

VRAM
32Mx32bx2 (256MB)
55

GDDR3
700MHz

CRT
(on I/Oboard) 48

LCD
20

RGB CRT

LVDS(Dual Channel)

ATI M92LP-S2
51,52,53,54

PCIe x 16

Intel
PM45
AGTL+ CPU I/F
DDR Memory I/F
External Graphics
7,8,9,10,11,12

DDRII 667/800 Channel A

DDR II 667/800 Channel B

DDRII 667/800 Slot 0
17

DDRII 667/800 Slot 1
18

DMIx4

C-LINK

Power SW
G577BR91U 25

New Card 25

PCIE x 1 & USB 2.0 x 1

PCIE x 1

10/100 NIC
Marvell 88E8040 38

I/O Board Connector
48

RJ45 CONN

USB 2.0 x 2

Left Side:
USB x 2

PCIE

SD/SDIO/MMC
MS/MS Pro/xD 26

CardReader
Realtek
RTS5159
32

USB2.0

Intel
ICH9-M
USB 2.0/1.1 ports (12)
PCI Express ports (6)
High Definition Audio
SATA ports (4)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
13,14,15,16

PCIE x 1& USB 2.0 x 1

Mini-Card
802.11a/b/g 26

USB 2.0

USB 2.0 x 1

CAMERA
(Option) 25

Digital Mic Array

MIC IN

Internal Analog MIC

Azalia
CODEC
IDT
92HD71B7
36

AZALIA

USB 2.0 x 1

Bluetooth 25

LPC Bus

USB 2.0 x 1

Right Side:
USB x 1 31

HP1

OP AMP
MAX9789C
37

2CH SPEAKER

SATA

SATA

KBC
WINBOND
WPCE773L
29

SPI

HDD 23

ODD 23

Flash ROM
2MB 30

Touch PAD 33

Int. KB 33

Thermal
EMC2102 35

Fan 23

CPU DC/DC ISL6266A 39,40	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51117 43	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

SYSTEM DC/DC MAX17020 41	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC TPS51116 44	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS +0.9V_DDR_VTT +V_DDR_MCH_REF

SYSTEM DC/DC APL5912 42	
INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN +1.1V_RUN

VGA TPS51117 50	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE_RUN

MAXIM CHARGER MAX8731A 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC LDO 34	
INPUTS	OUTPUTS
+5V_ALW	+5V_RUN
+3.3V_ALW	+3.3V_RUN
+1.8V_SUS	+1.8V_RUN

PCB LAYER

L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Signal
L7: GND
L8: Bottom

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Title: Block Diagram

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

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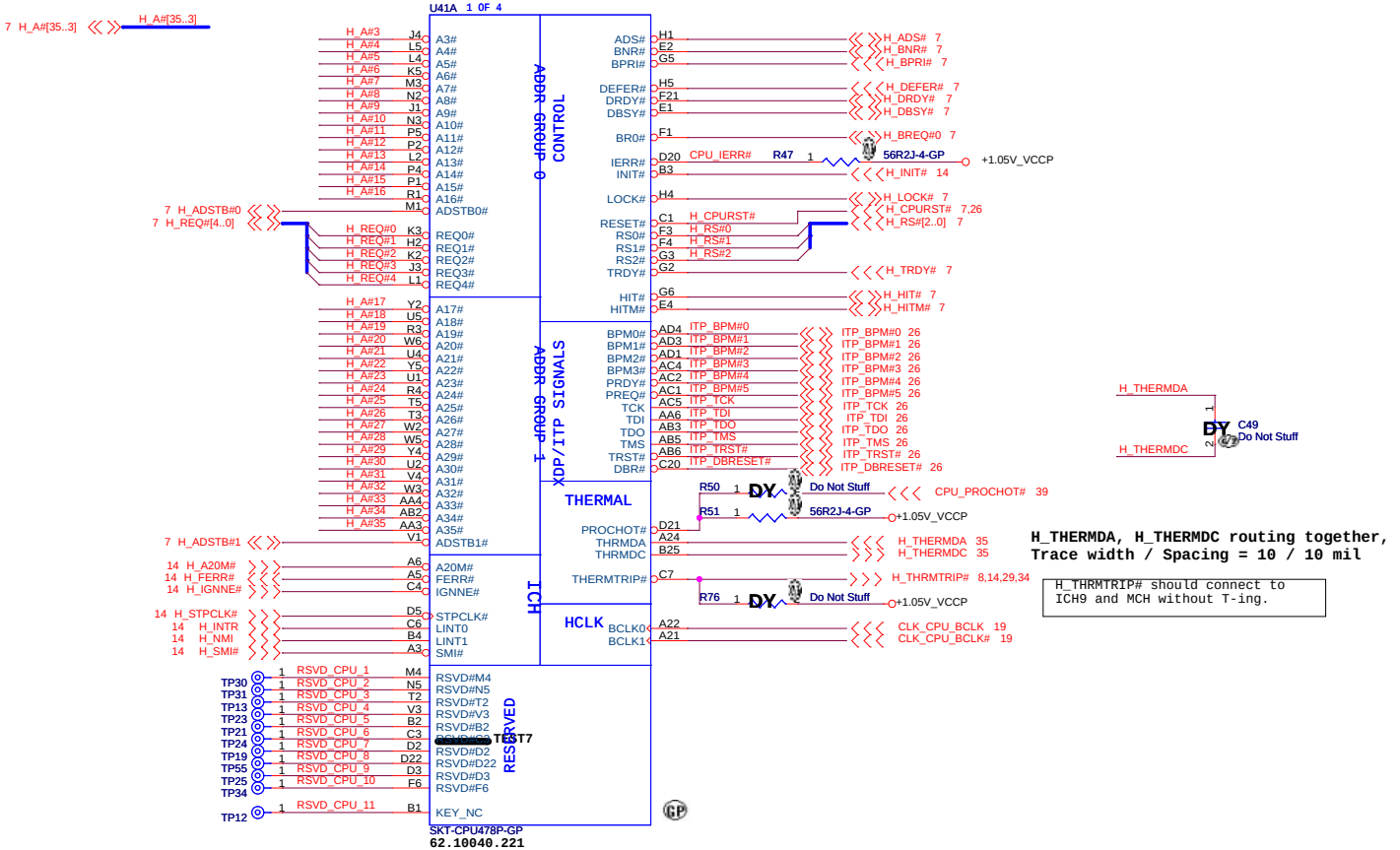
Title: Table of Content
Size: Custom | Document Number: Roberts Discrete | Rev: -1
Date: Tuesday, May 19, 2009 | Sheet 3 of 60

SSID = CPU



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Title: **CPU-FSB(1/3)**

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Date: Tuesday, May 19, 2009 Sheet 4 of 60

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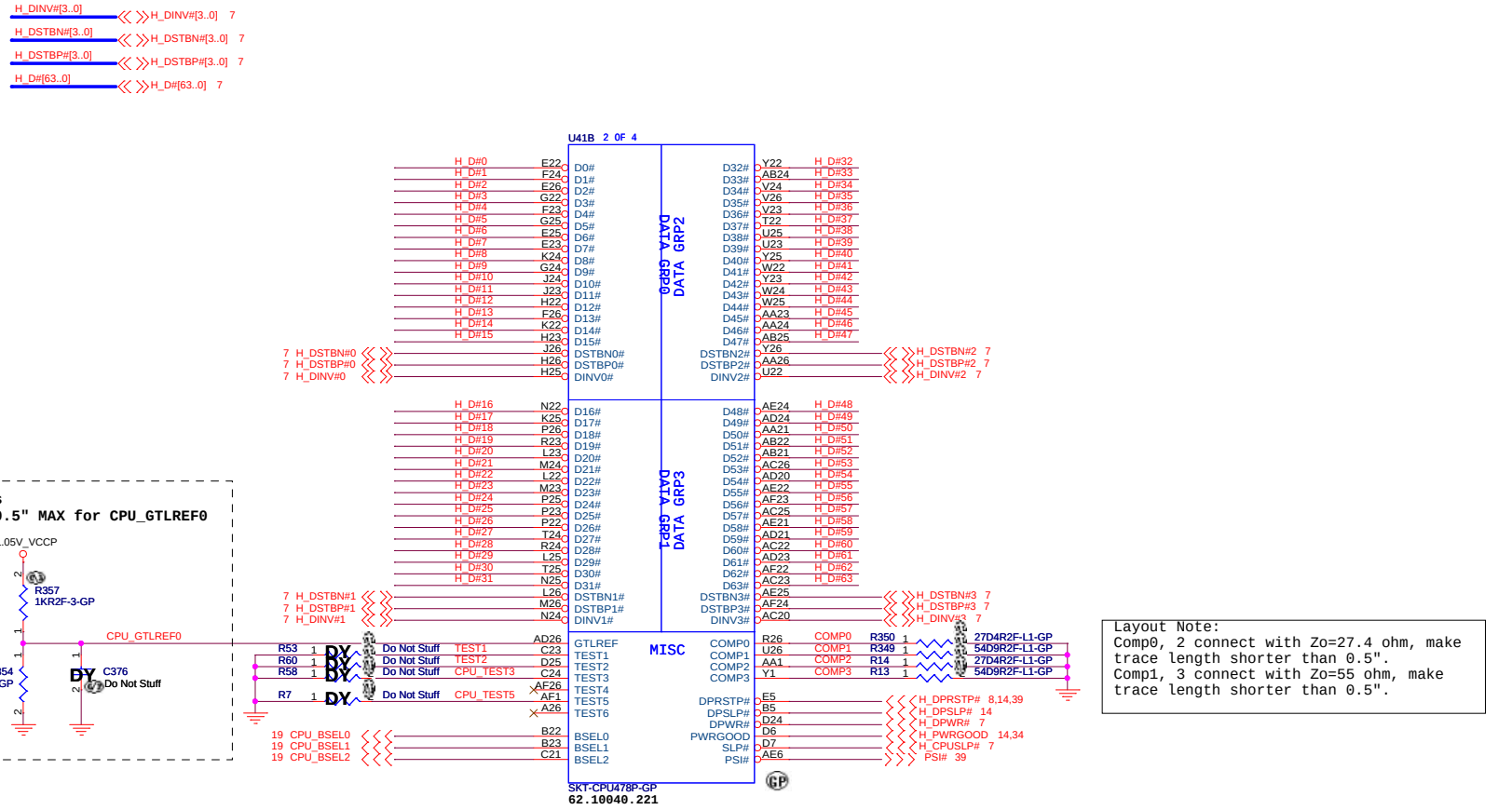

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Title: CPU-FSB(2/3)

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Date: Tuesday, May 19, 2009 | Sheet 5 of 60

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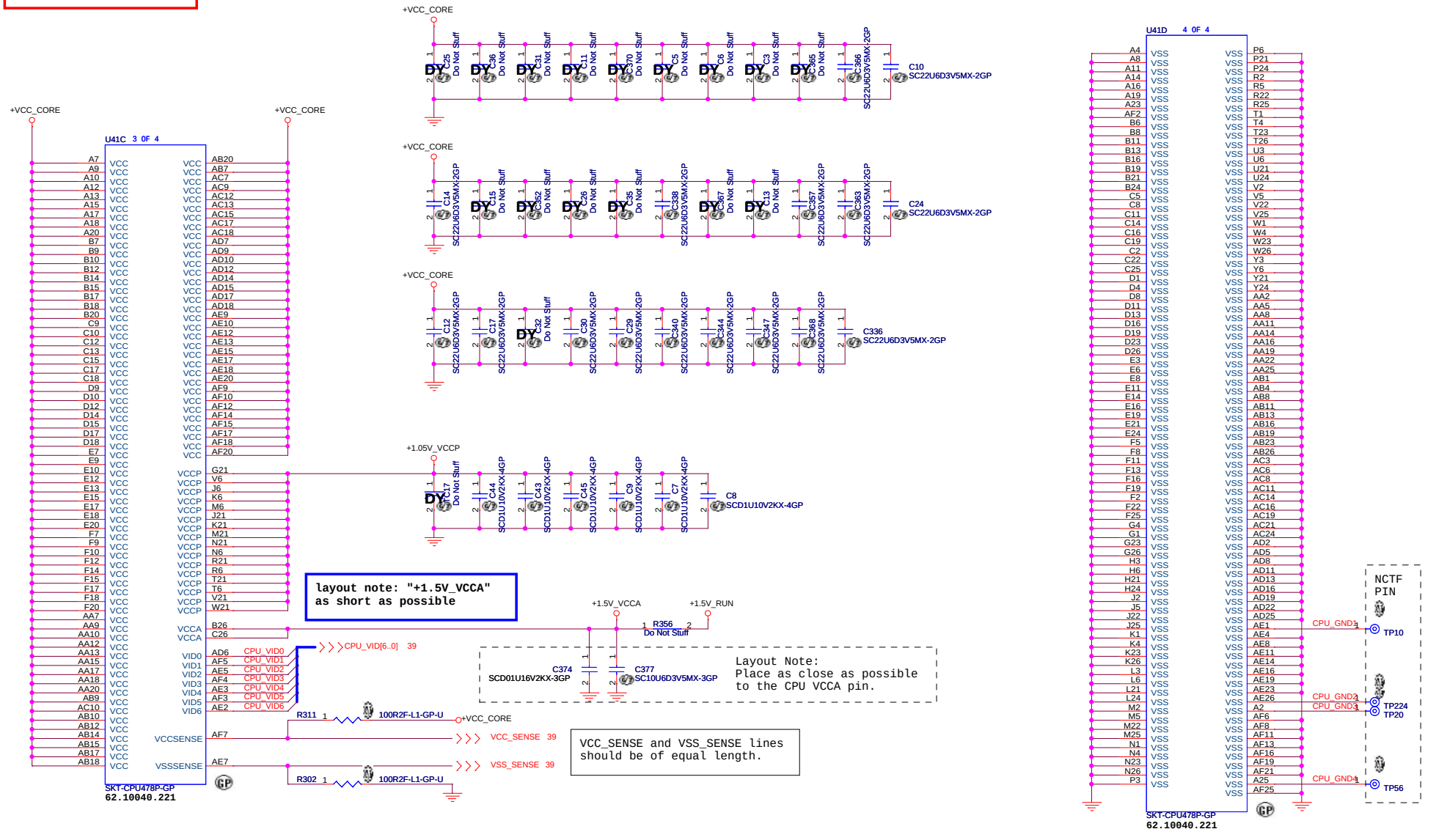

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Title: CPU-Power(3/3)

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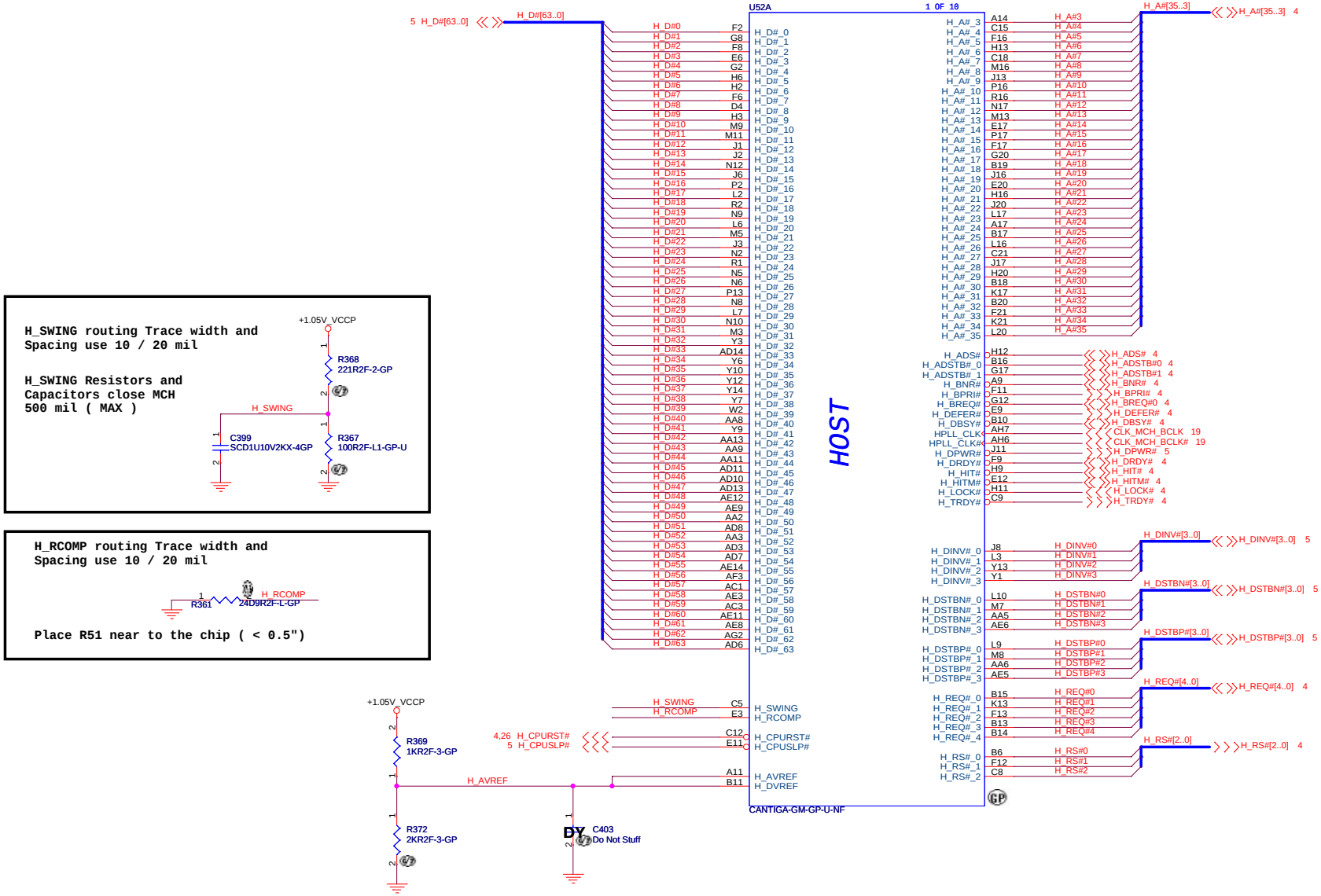
Date: Tuesday, May 19, 2009 | Sheet 6 of 60

SSID = MCH



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Title: Cantiga-HOST(1/6)

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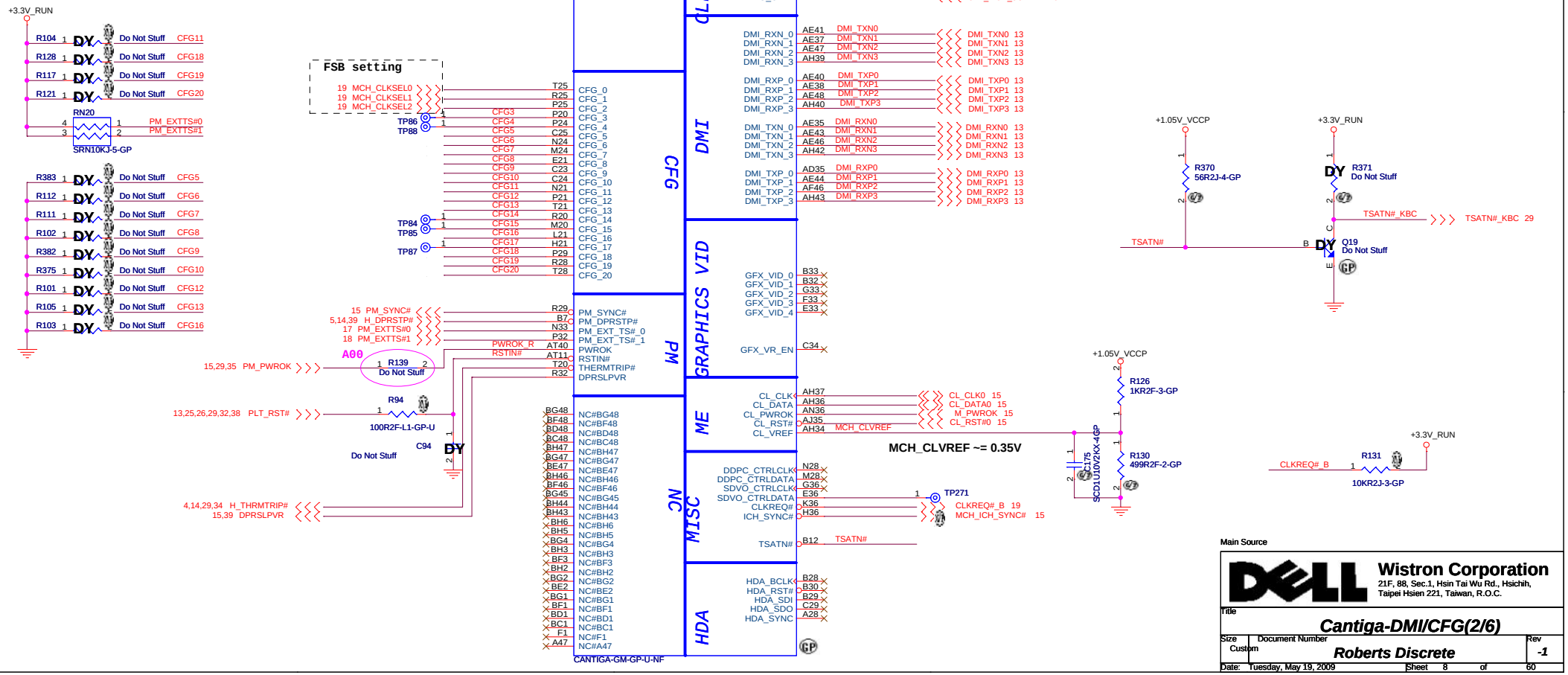
Date: Tuesday, May 19, 2009 | Sheet 7 of 60

SSID = MCH

* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in oder *
CFG 10	PCIE loopback enable	PCIE loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19 DMI Lane Reserved	Normal operation *	Reverse DMI lanes
CFG 20 SDVO concurrent with PCIE	Only PCIE or SDVO is operational *	PCIE and SDVO are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable *	SDVO interface enable
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled



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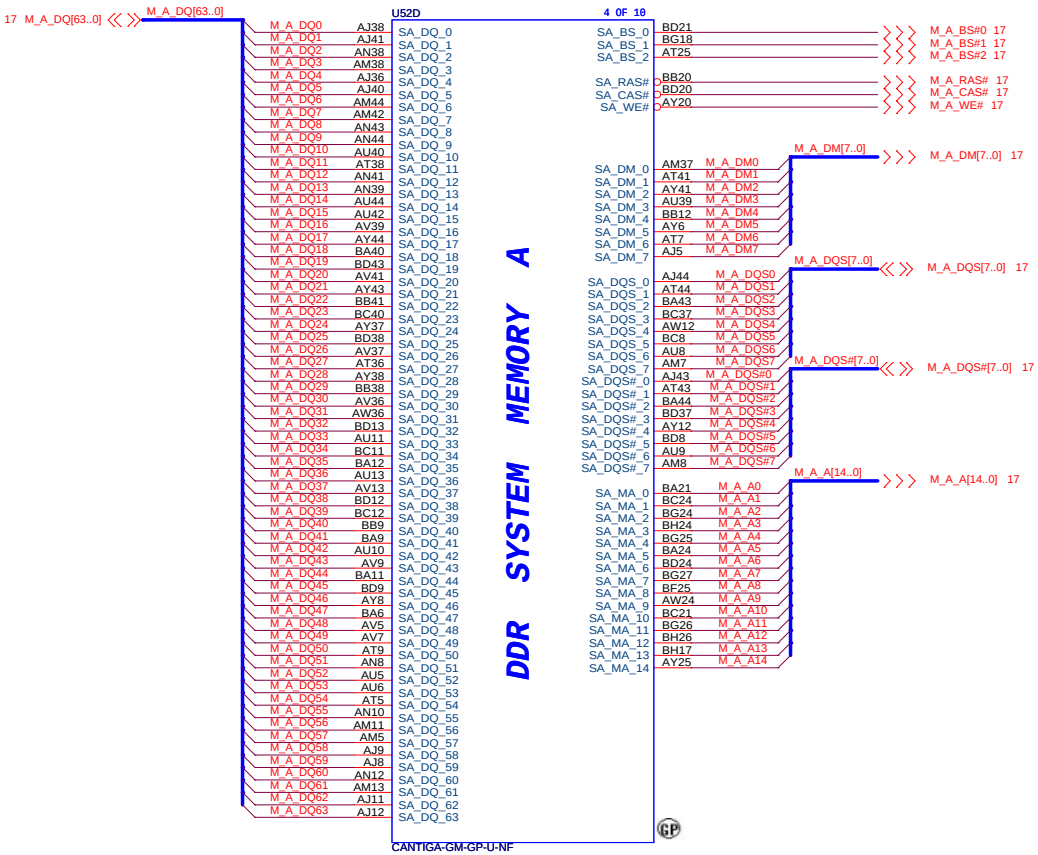

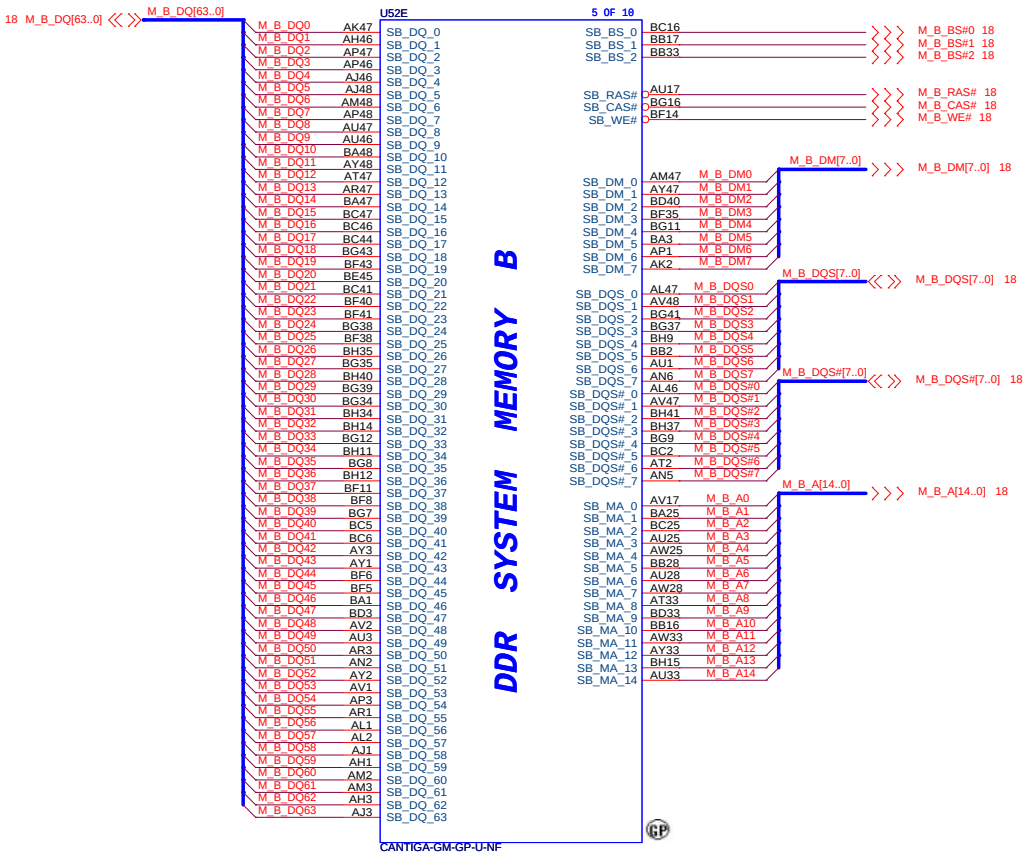

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Title: *Cantiga-DDR(3/6)*

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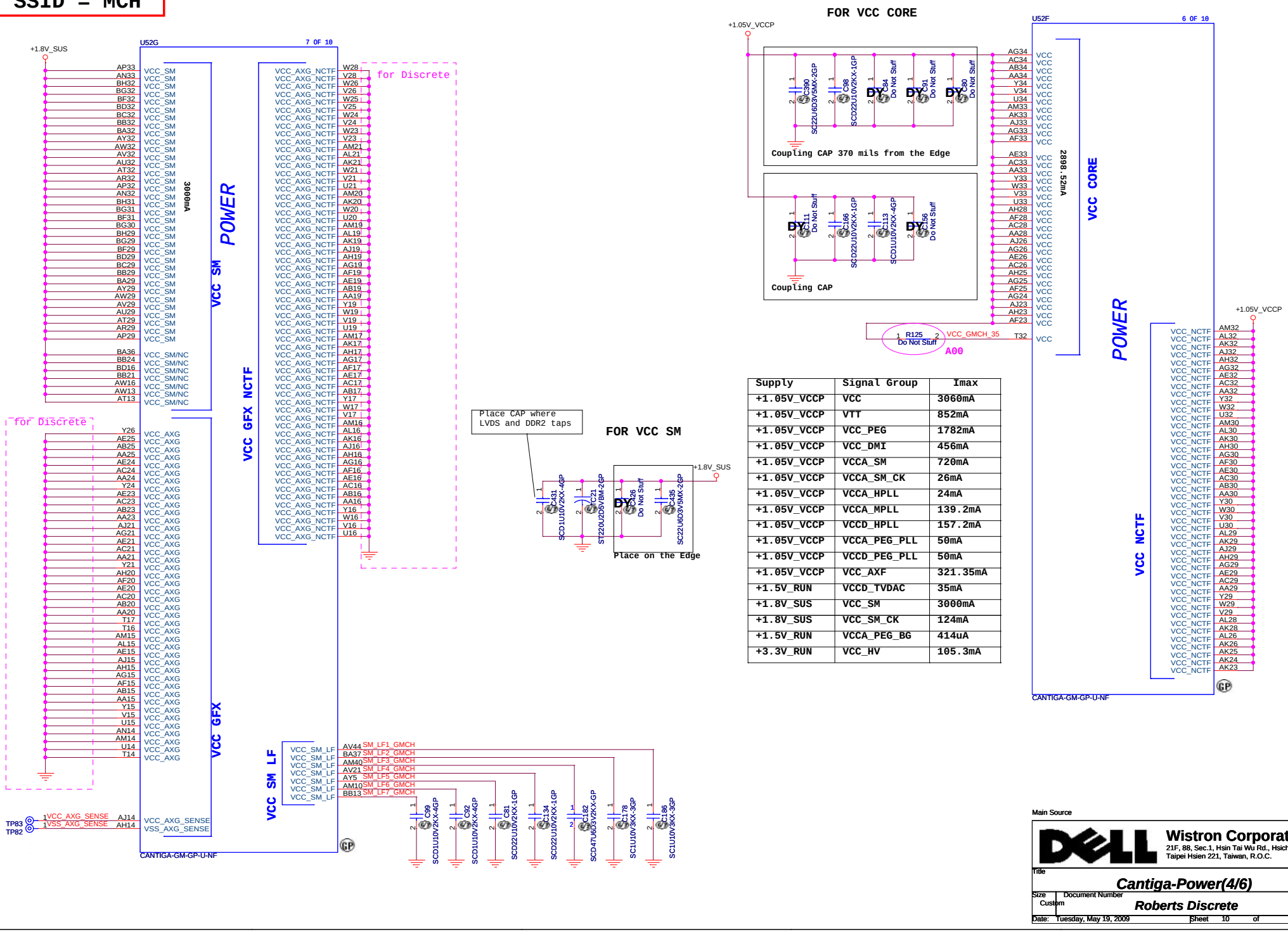

Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

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Title: **Cantiga-Power(4/6)**

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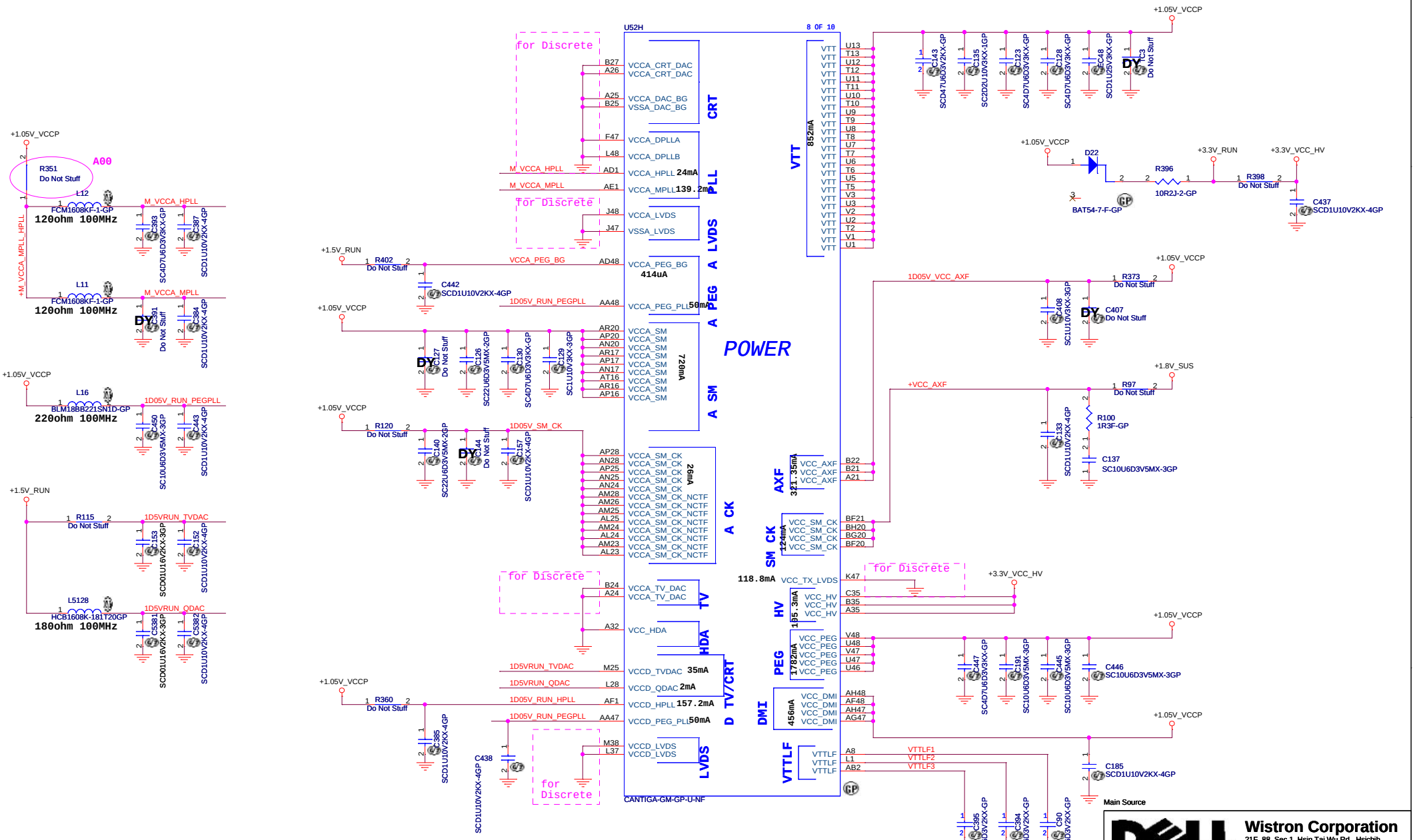

hexainf@hotmail.com
GRATIS - FOR FREE

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Title: Cantiga-Power/Filter(5/6)

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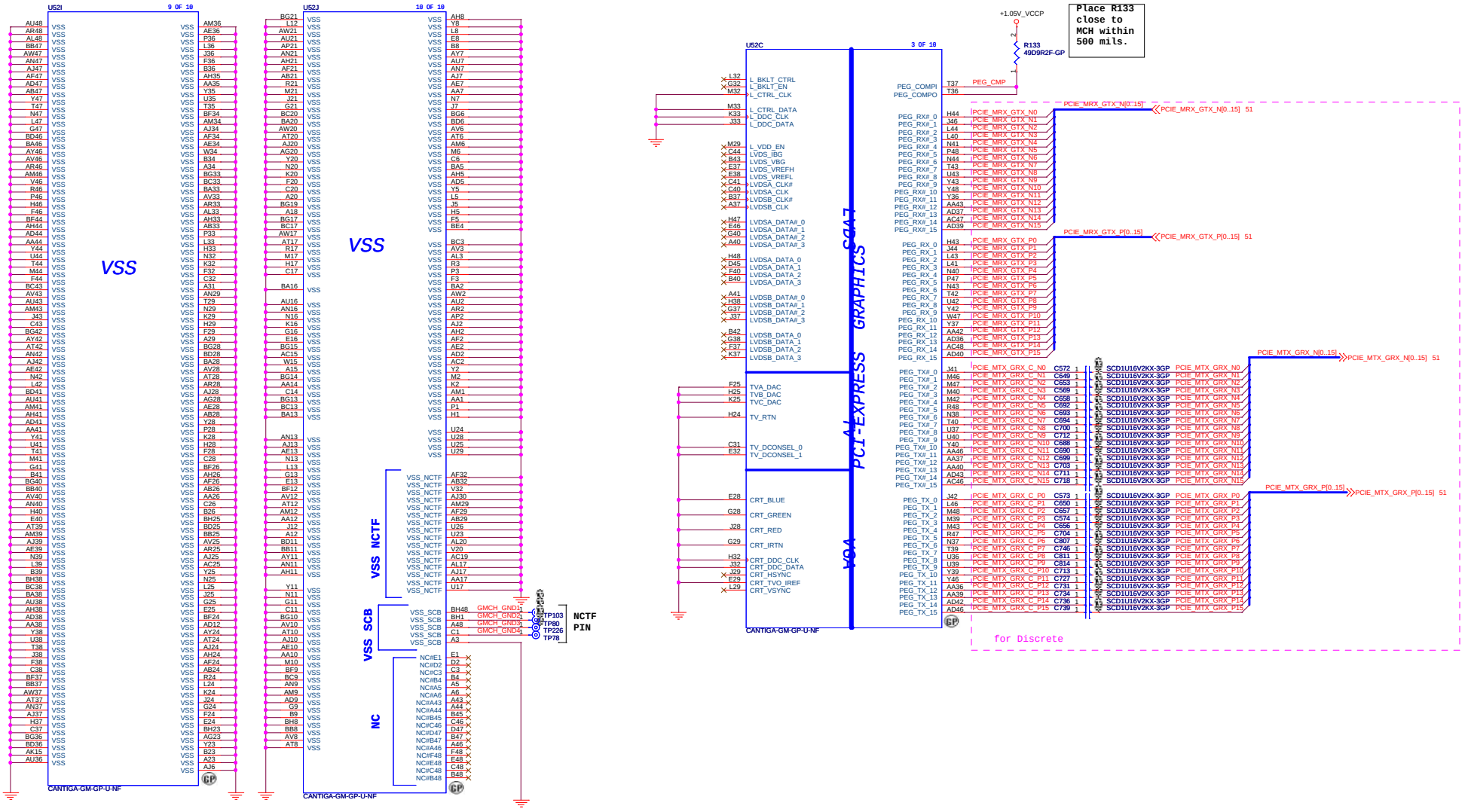

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Size	Document Number	Rev
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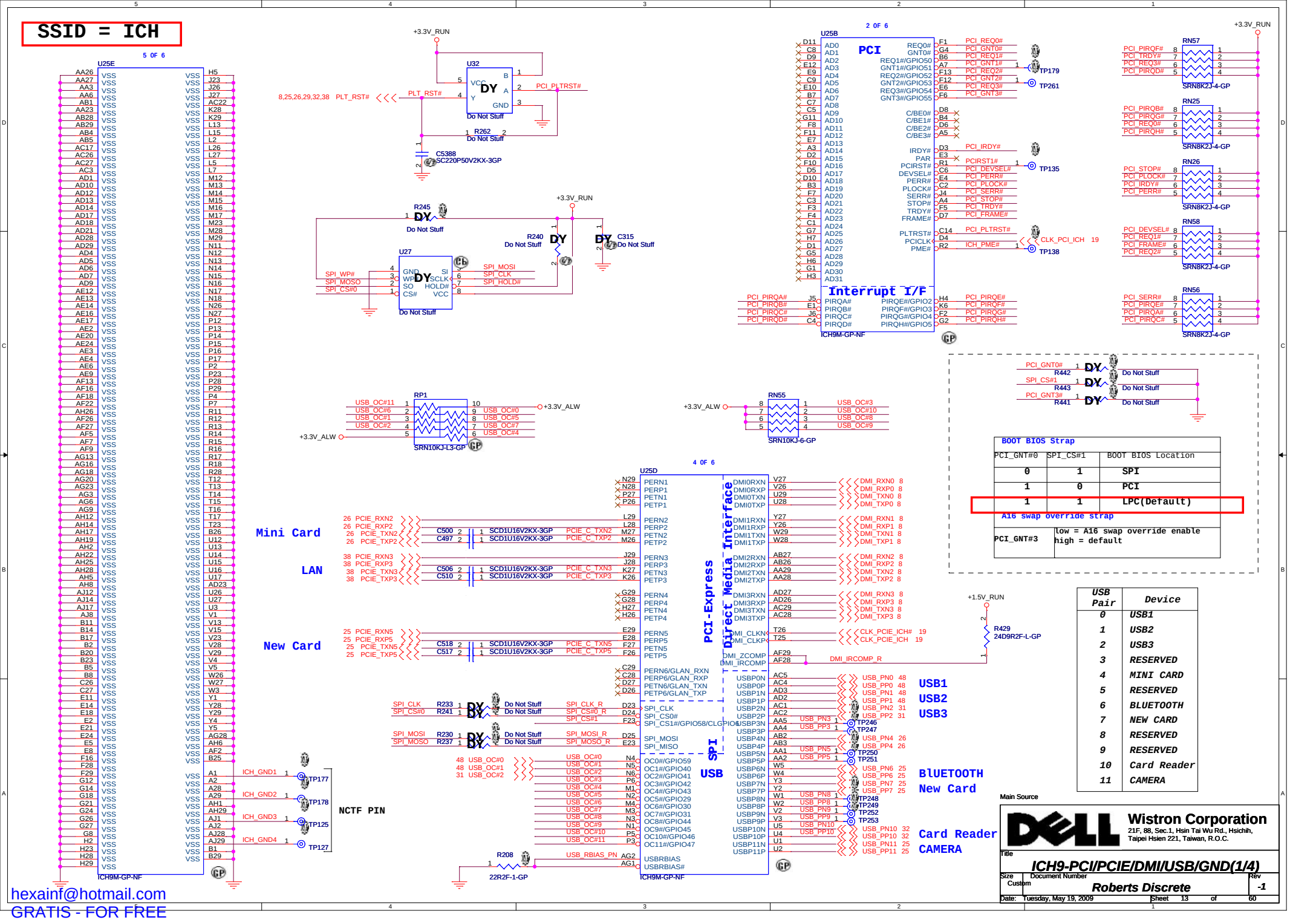

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

USB Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

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Title: **ICH9-PCI/PCIE/DMI/USB/GND(1/4)**

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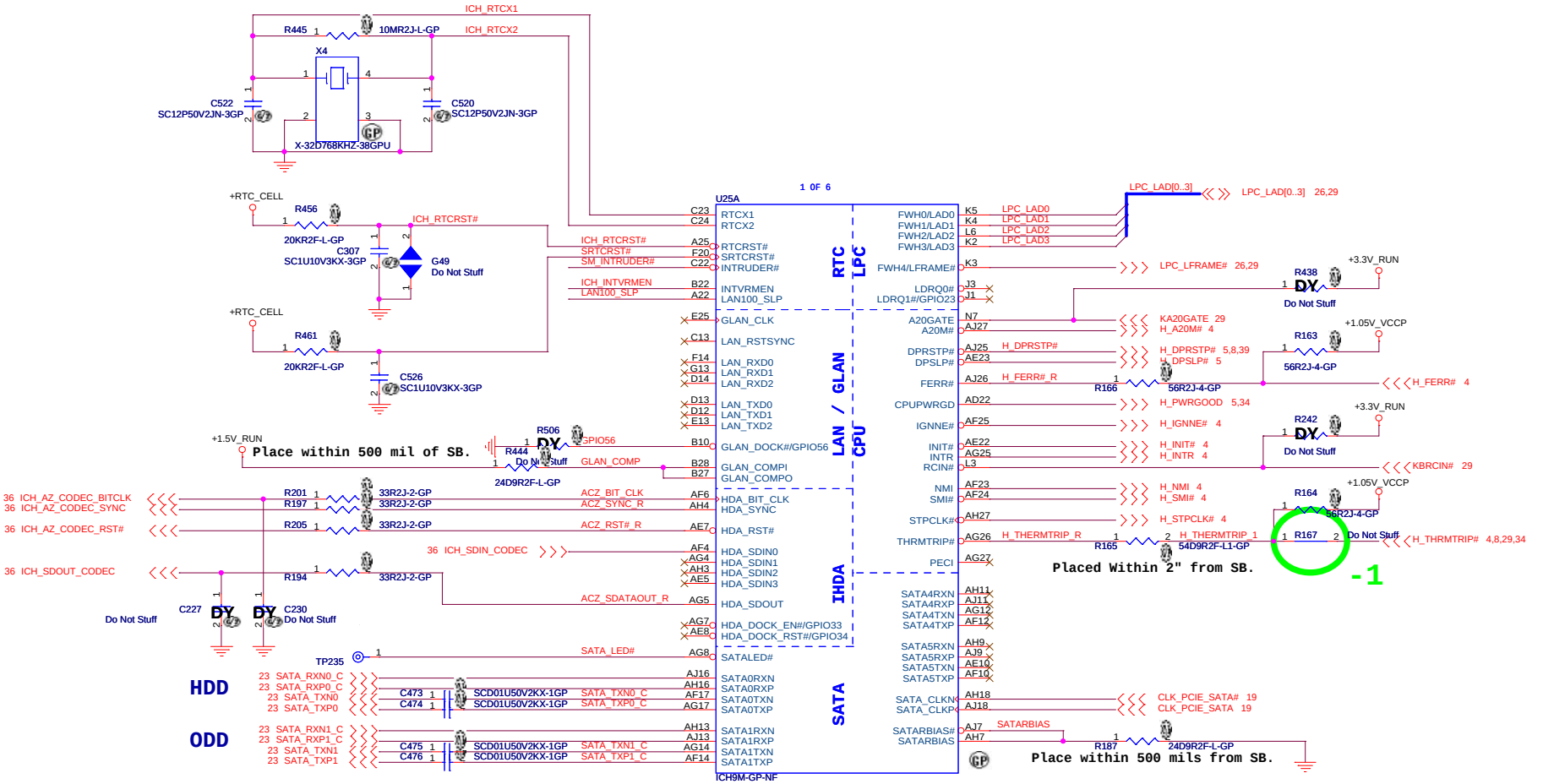

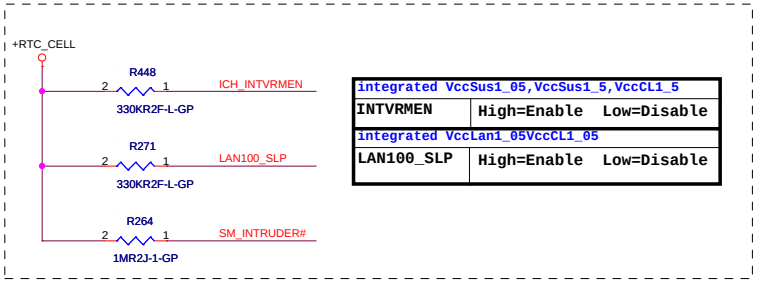

integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

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Title: ICH9-LAN/HDA/SATA/LPC(2/4)

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Date: Tuesday, May 19, 2009	Sheet 14 of 60	

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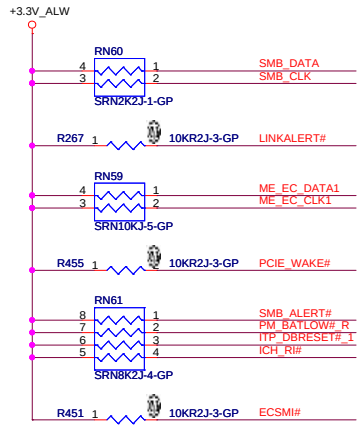

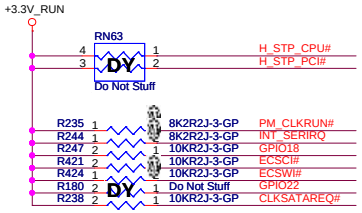

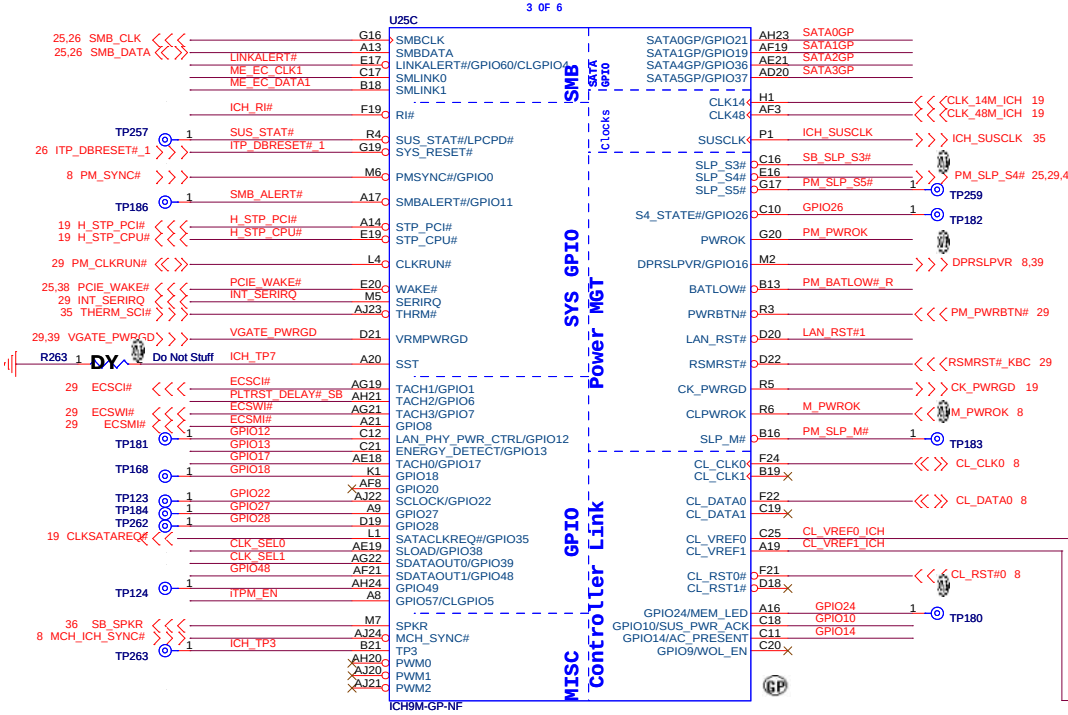

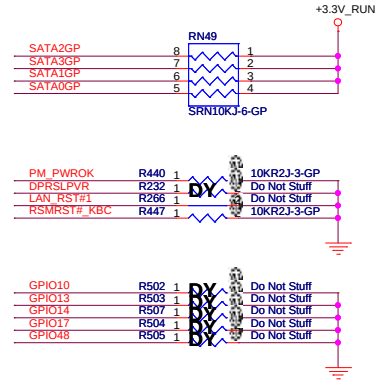

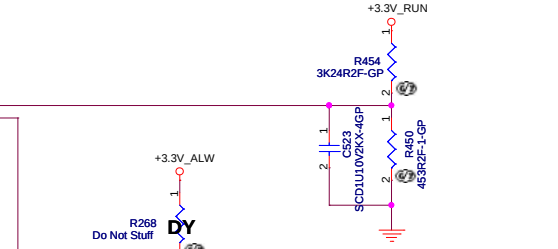

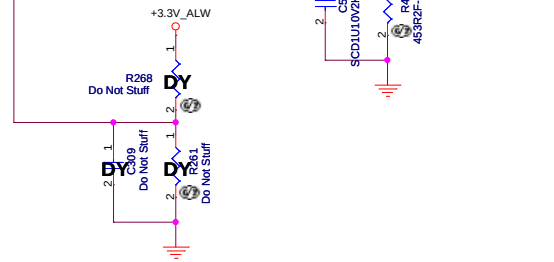

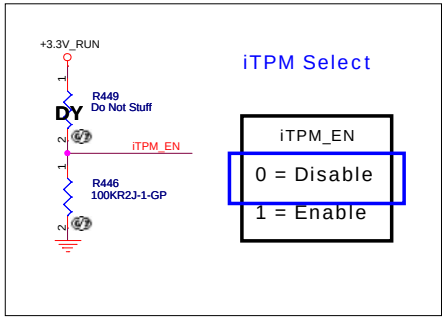

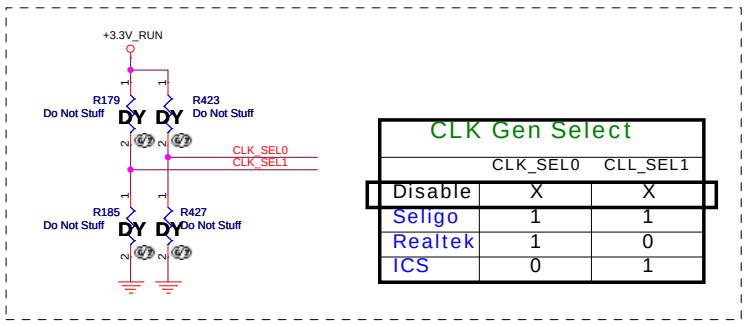

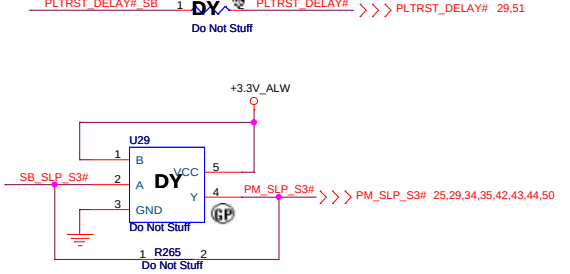

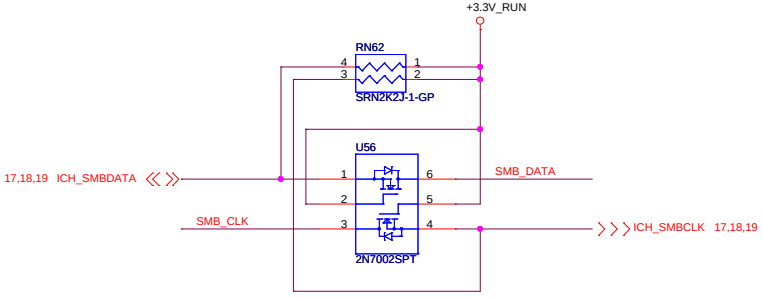

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-GPIO/PM/CL(3/4)**

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Custom	Roberts Discrete	-1

Date: Tuesday, May 19, 2009 Sheet 15 of 60

SSID = ICH

6 OF 6

U25F

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

+RTC_CELL
+1.05V_VCCP
+1.5V_RUN
+3.3V_RUN
+3.3V_ALW
+VCCSATAPLL
1D5V_DMIPLL_ICH_S0
1D5V_USB_S0
VCCLAN1D05
VCC_GLAN_PLL
SB_VCCLAN3_3
SB_V_CPU_IO
SB_VCC_3_3_C
SB_VCCHDA
SB_VCCSUS3_3
SB_VCCCL3_3
VCCDMI
PCI_VCCP_CORE_S0
3D3V_VCCPCORE_ICH_S0
+VCCSUSHDA
VCCSUS1_05[1]
VCCSUS1_05[2]
VCCSUS1_05[3]
VCCSUS1_5[1]
VCCSUS1_5[2]
VCCSUS1_5[3]
V5REF_S0
V5REF_S5

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-POWER(4/4)

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 16 of 60

SSID = MEMORY

DM2

SKT-SODIMM200-37GP

62.10017.E21

Layout Note:
Place near DM1

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.

Layout Note:
Place these resistors close to DM1,
all trace length Max=1.5".

put near connector

-1

Main Source

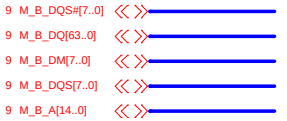
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

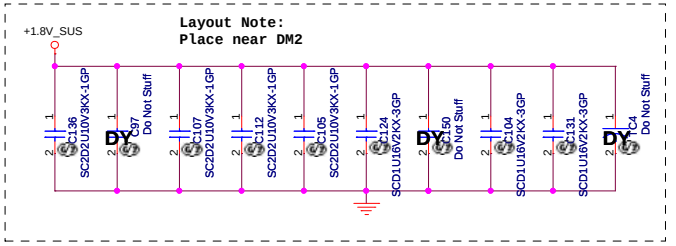
Title: DDRII-SODIMM SLOT1

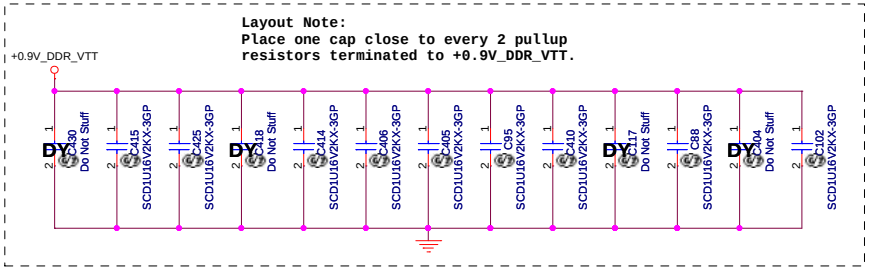
Size: Custom | Document Number: Roberts Discrete | Rev: -1

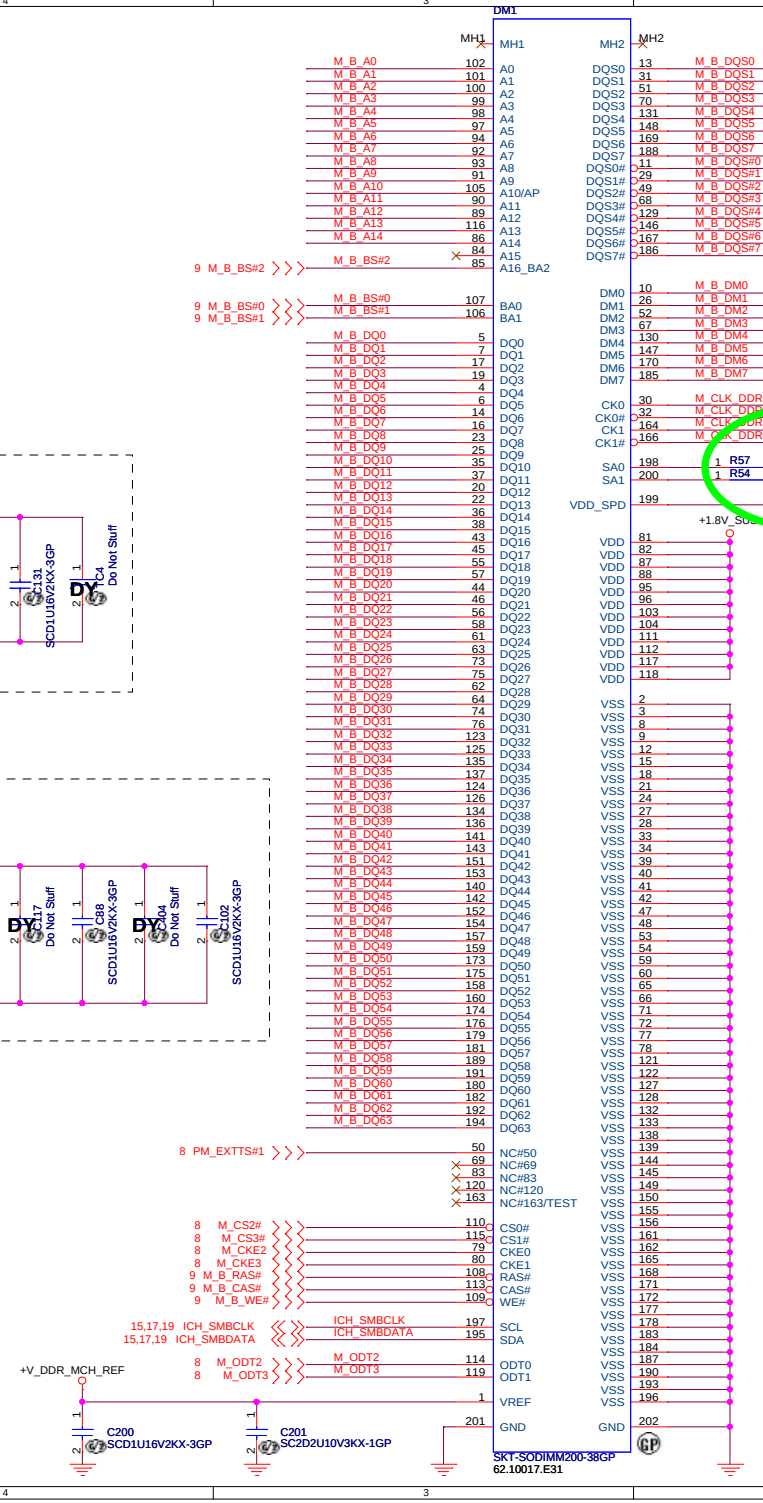
Date: Tuesday, May 19, 2009 | Sheet 17 of 60

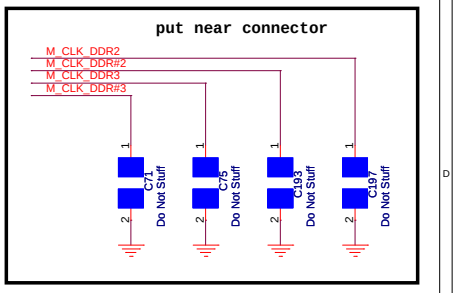
SSID = MEMORY



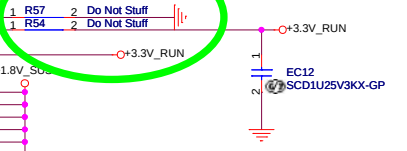


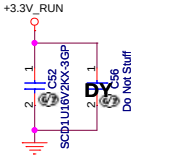


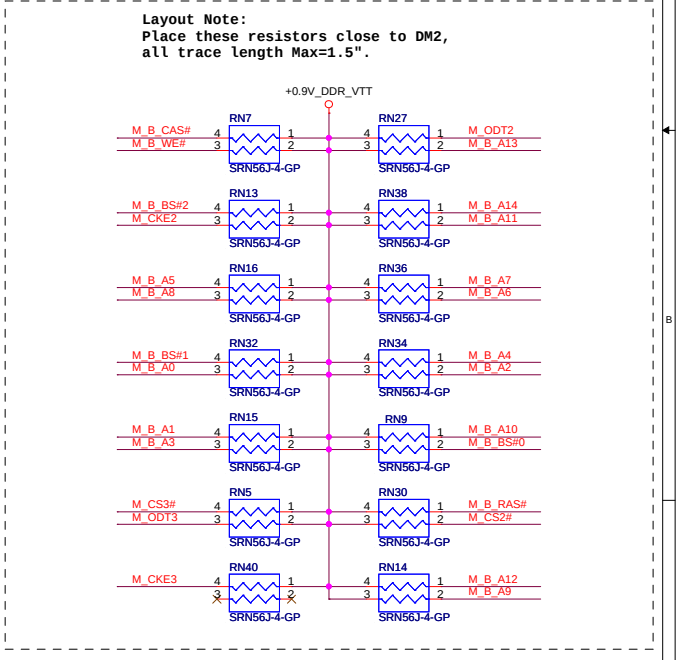




-1







Main Source

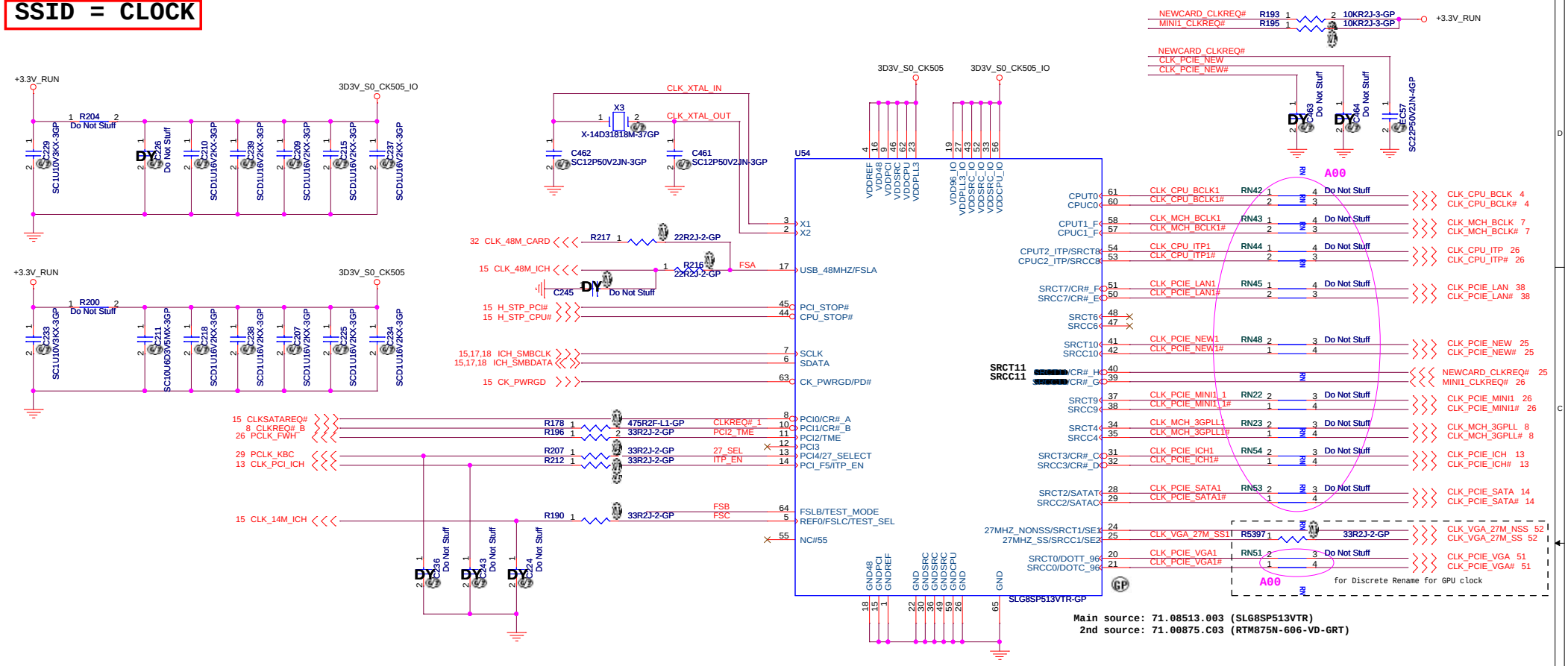
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT2

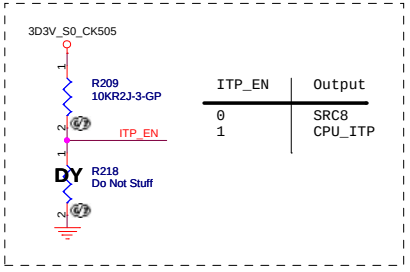
Size	Document Number	Rev
Custom	Roberts Discrete	-1

Date: Tuesday, May 19, 2009 Sheet 18 of 60

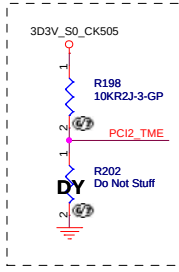
SSID = CLOCK



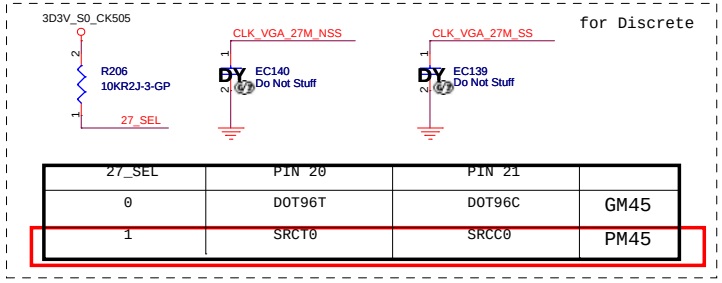
Main source: 71.08513.003 (SLG8SP513VTR)
2nd source: 71.00875.C03 (RTM875N-606-VD-GRT)



ITP_EN	Output
0	SRC8
1	CPU_ITP

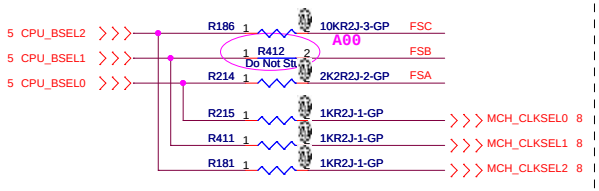


PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed



27_SEL	PIN 20	PIN 21	
0	DOT96T	DOT96C	GM45
1	SRCT0	SRCC0	PM45

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M



Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

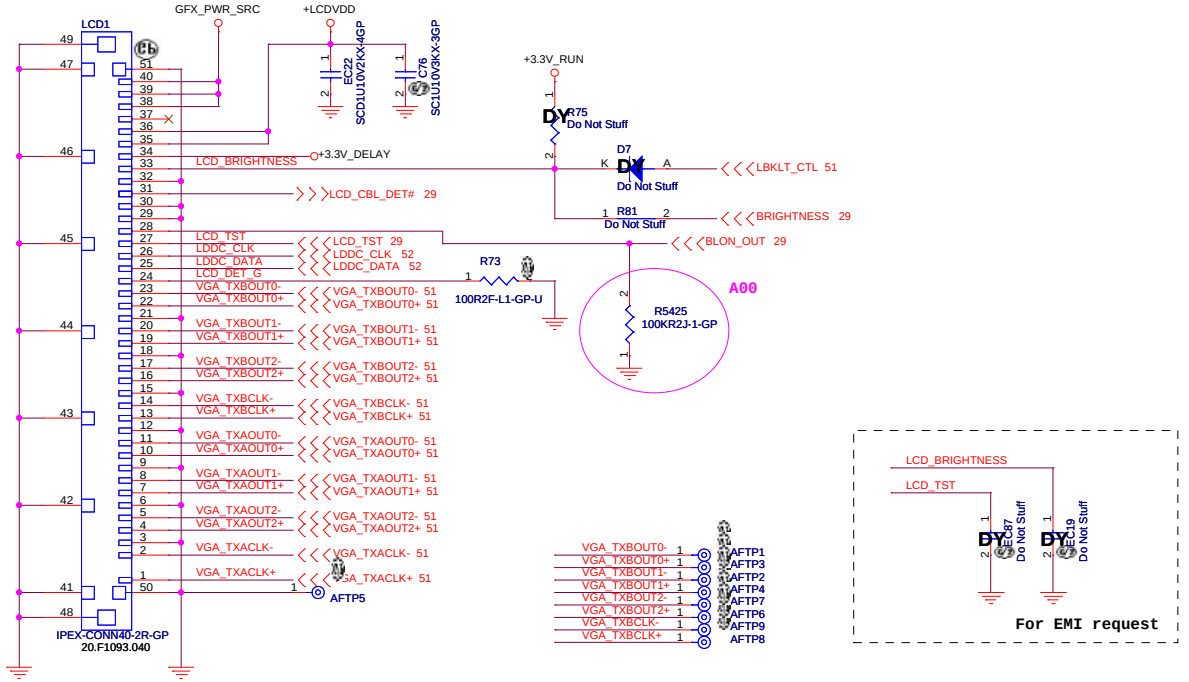
Title: Clock Generator SLG8SP513VTR

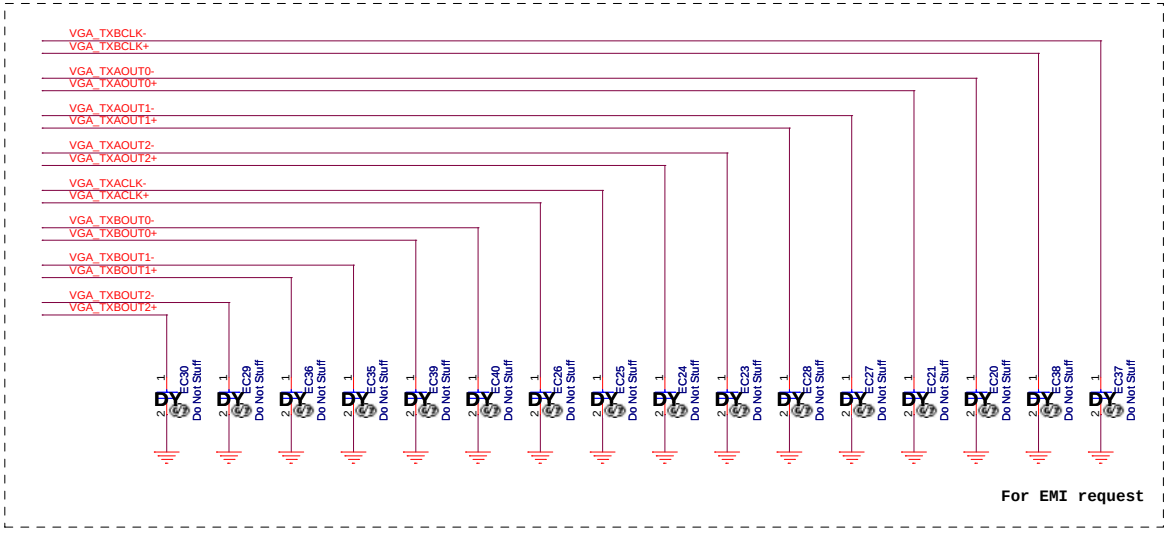
Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 19 of 60

SSID = VIDEO

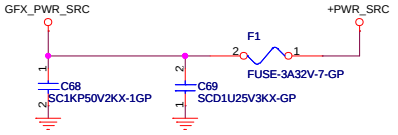
LVDS CONNECTOR





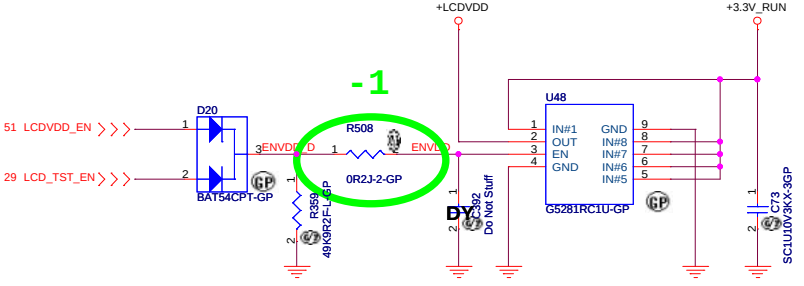
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 20 of 60

(Blanking)

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 21 of 60

(Blanking)

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

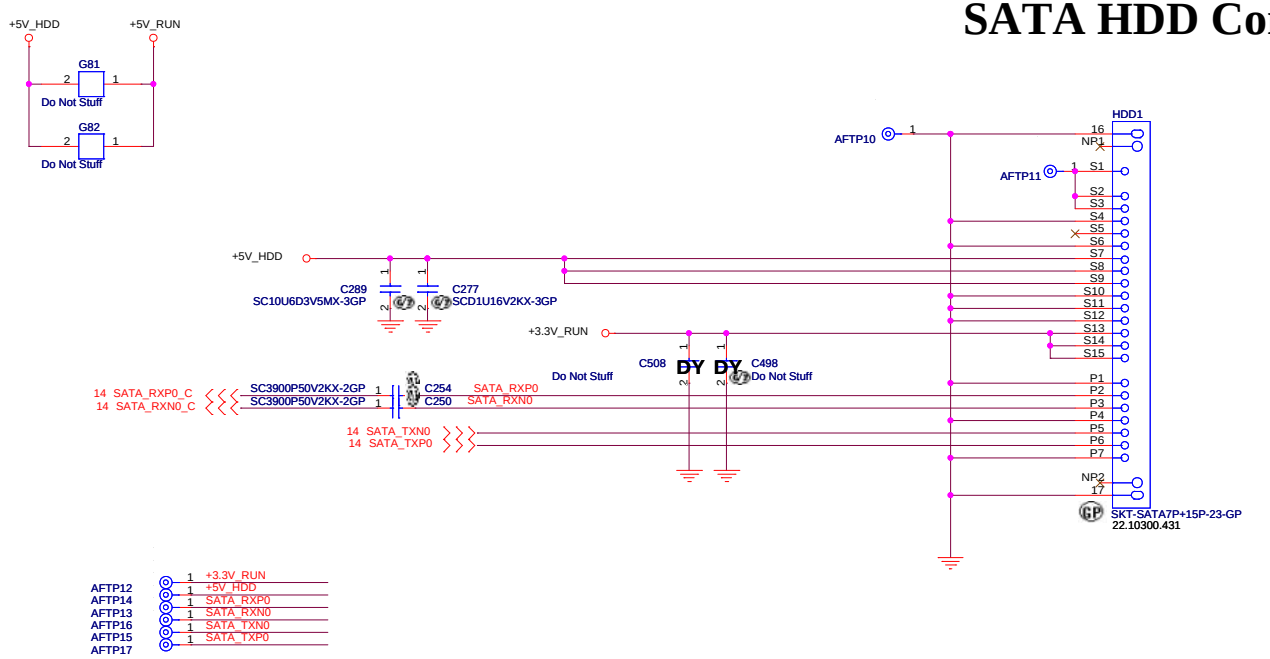
Title: HDMI

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 22 of 60

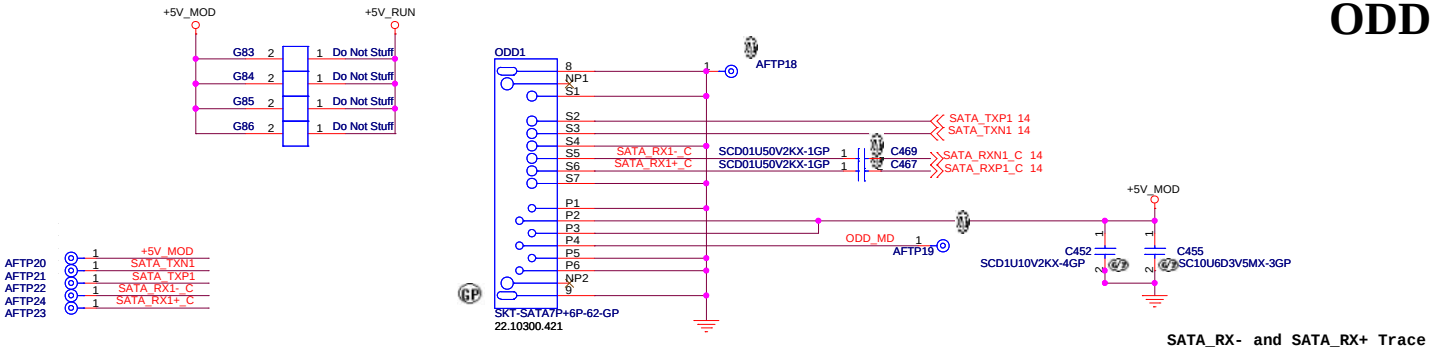
SSID = SATA

SATA HDD Connector



SSID = SATA

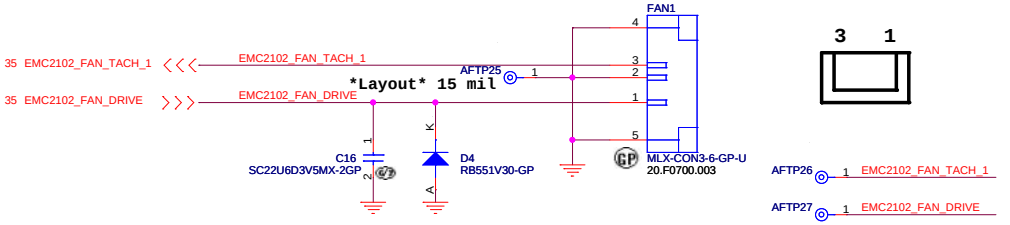
ODD Connector



SATA_RX- and SATA_RX+ Trace Length match within 20 mil

SSID = Thermal

Fan Connector



hexainf@hotmail.com
GRATIS - FOR FREE

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD/FAN

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 23 of 60

(Blanking)

Main Source

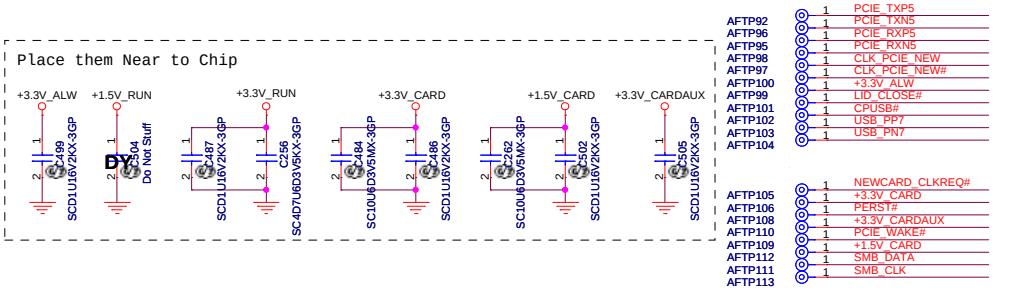
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

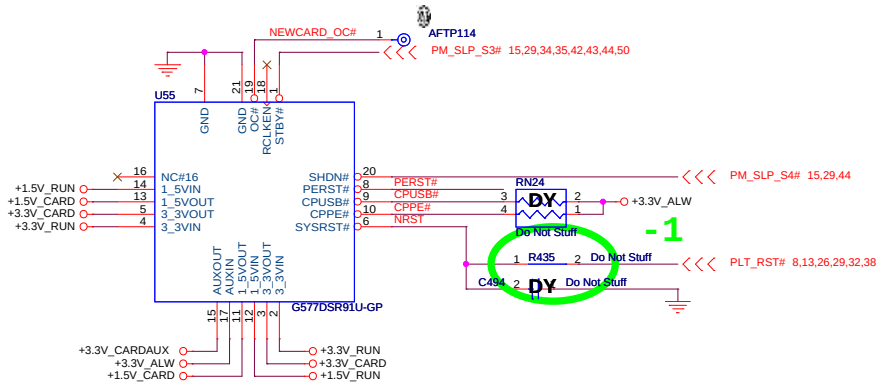
Title: PCI

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 24 of 60

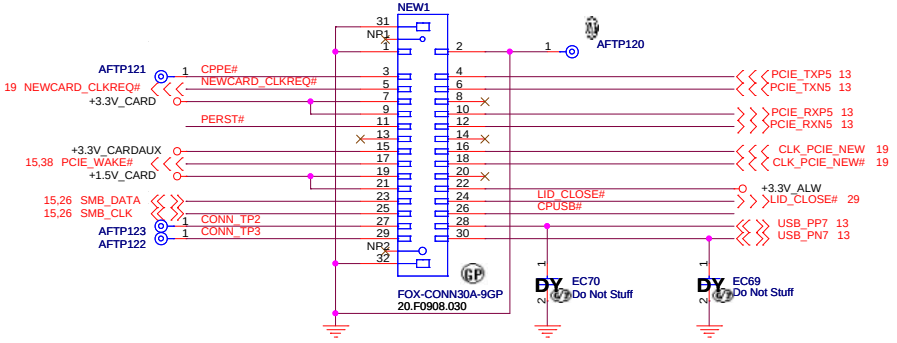
SSID = ExpressCard





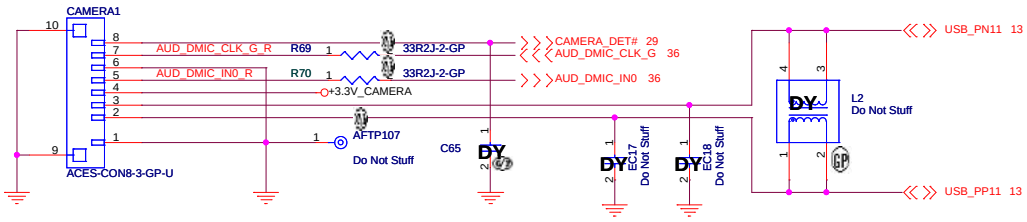
+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

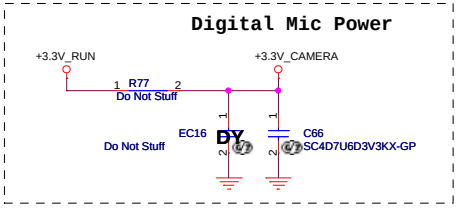
New Card Connector

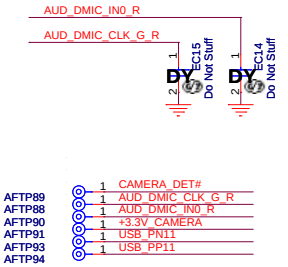


SSID = User.Interface

Camera Connector

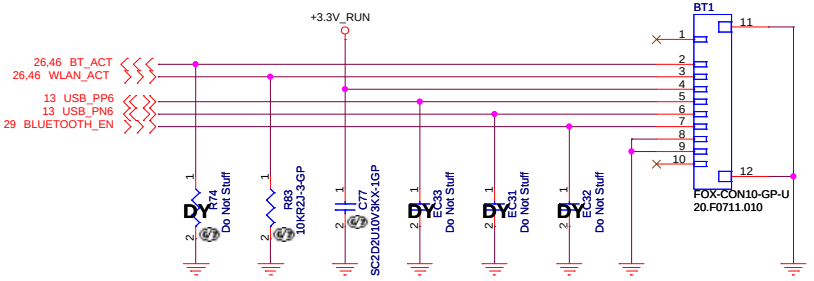


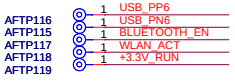




SSID = User.Interface

Bluetooth Module conn.





Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth/CAM/New Card***

Size	Document Number	Rev
Custom	***Roberts Discrete***	-1

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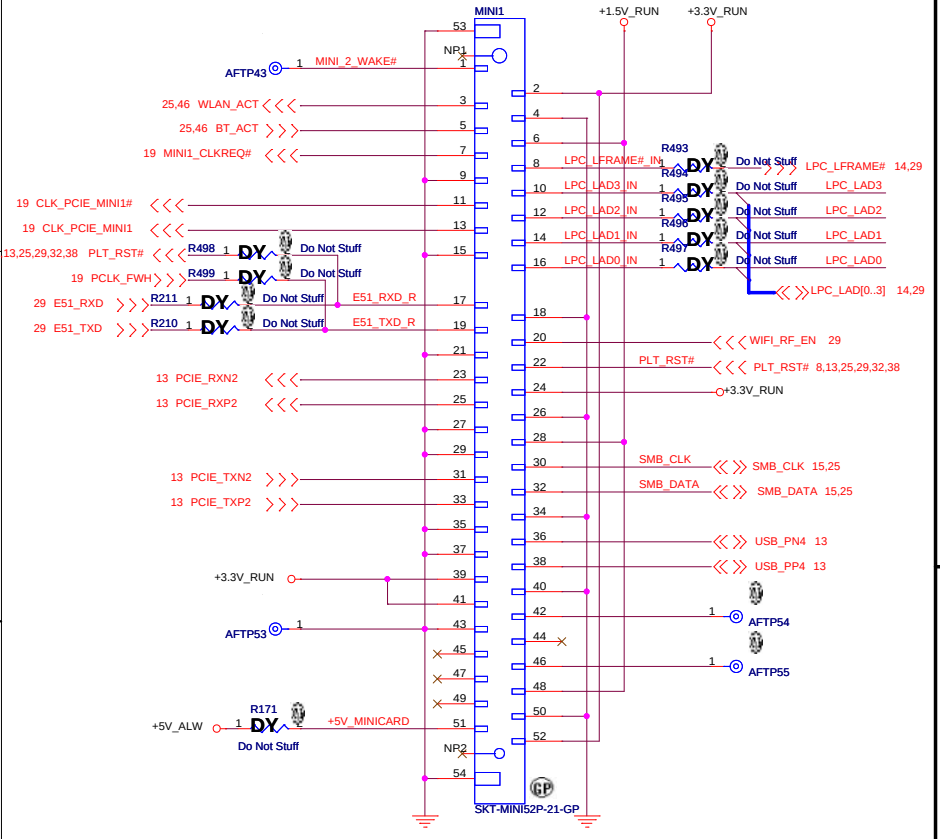
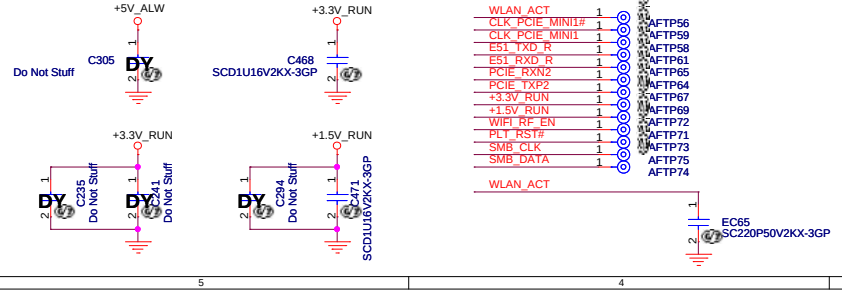
SSID = Wireless

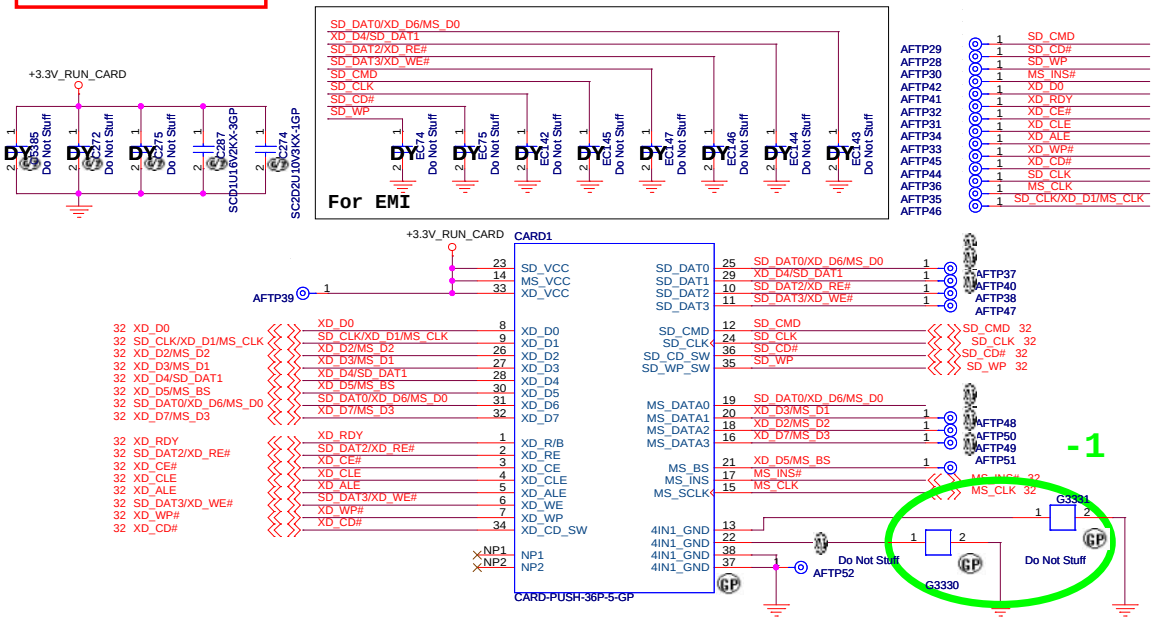
Mini Card Connector(802.11a/b/g)





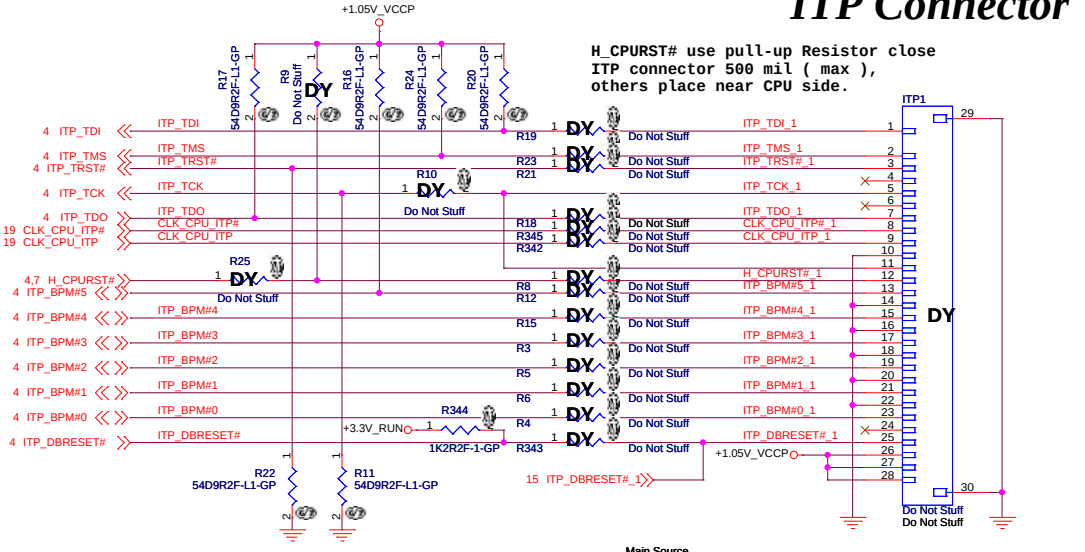
SSID = SDIO

SD/XD/MS Card Reader



SSID = User.Interface

ITP Connector



Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD/SD/ITP CONN

Size	Document Number	Rev
Custom	Roberts Discrete	-1

Date: Tuesday, May 19, 2009 Sheet 26 of 60

(Blanking)

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 27 of 60

(Blanking)

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WPAN

Size: Custom | Document Number: Roberts Discrete | Rev: -1

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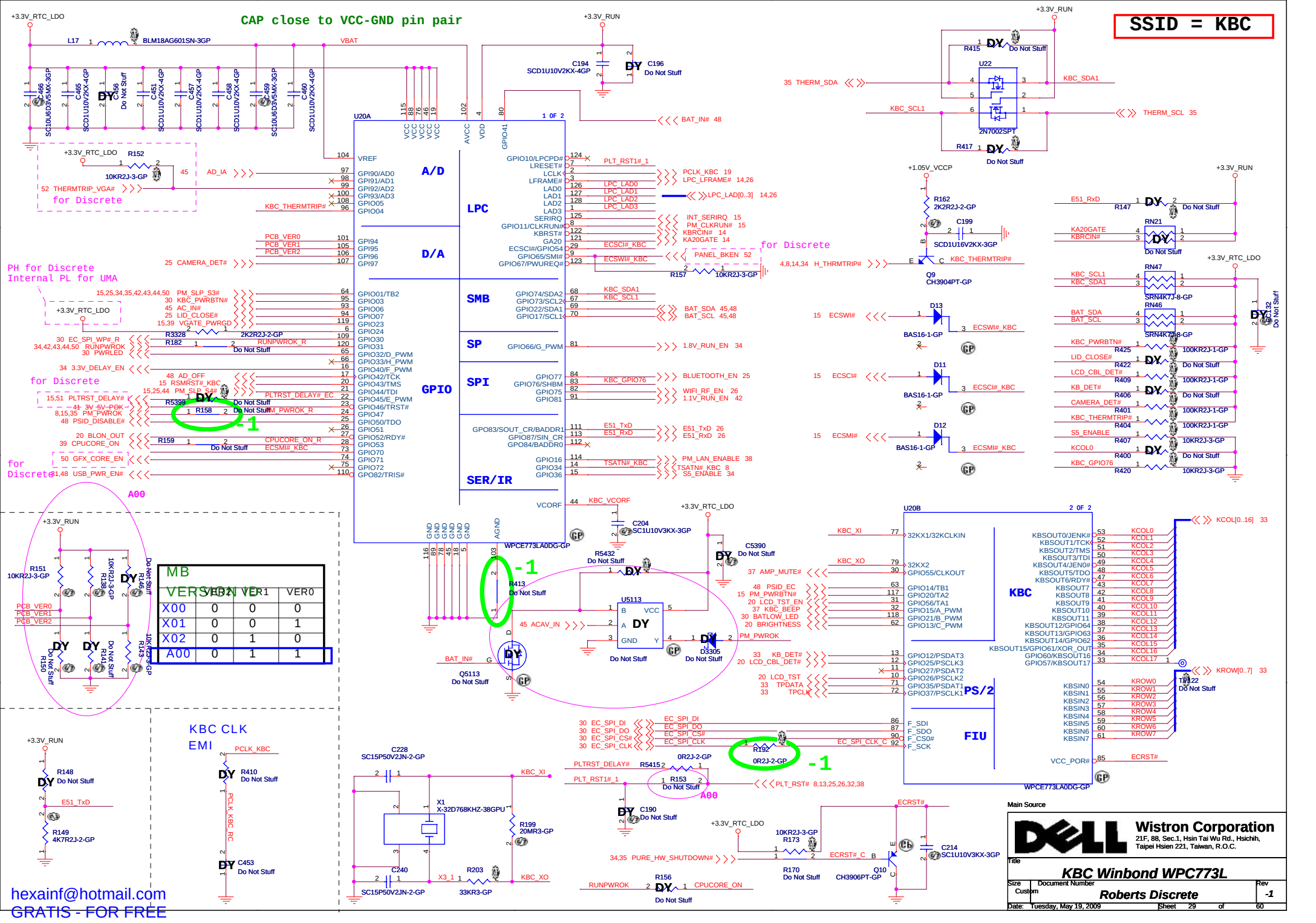
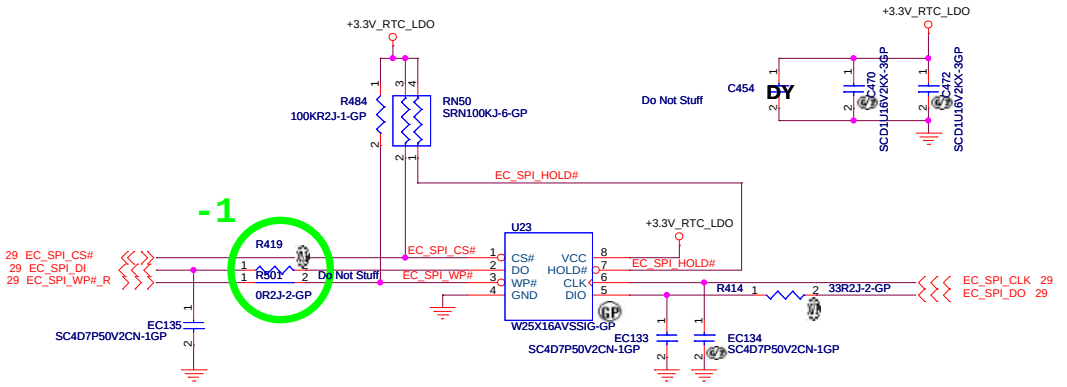

CAP close to VCC-GND pin pair
SSID = KBC
U20A
1 0F 2
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
for Discrete
PH for Discrete
Internal PL for UMA
MB VERSION
VER3 VER2 VER1 VER0
X00 0 0 0
X01 0 0 1
X02 0 1 0
A00 0 1 1
KBC CLK
EMI
U20B
2 0F 2
KBC
PS/2
FIU
WPCE773LA0DG-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC Winbond WPC773L
Roberts Discrete
Tuesday, May 19, 2009
hexainf@hotmail.com
GRATIS - FOR FREE

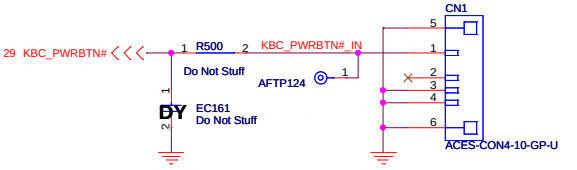
SPI FLASH ROM (16M bits)

SSID = Flash.ROM



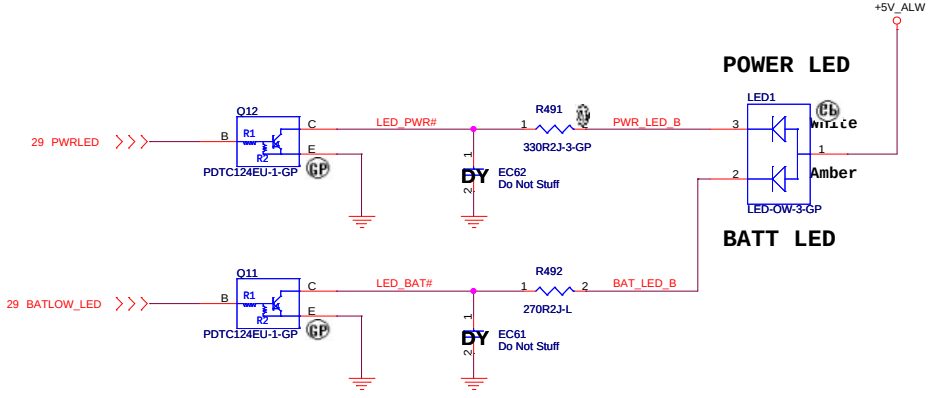
SSID = User.Interface

Power Board to Board CONN



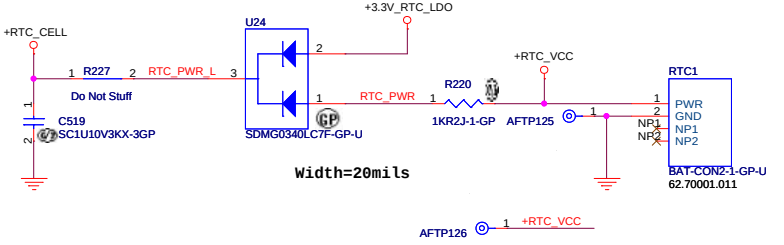
SSID = User.Interface

Power/Battery LED



SSID = RBATT

RTC Connector



Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

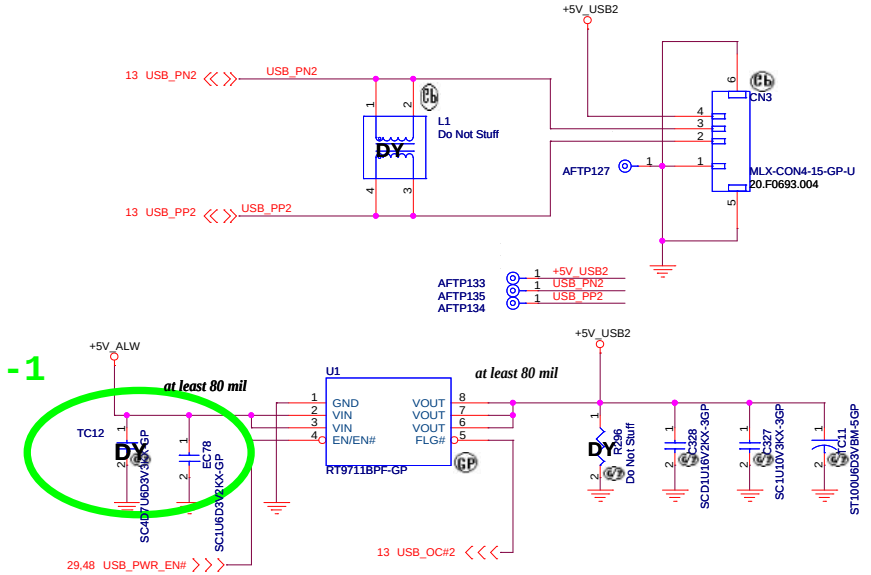
Title: ***FWH/LED/Power Dash/RTC***

Size	Document Number	Rev
Custom	***Roberts Discrete***	*-1*

Date: Tuesday, May 19, 2009 Sheet 30 of 60

SSID = USB

Right USB Port CONN

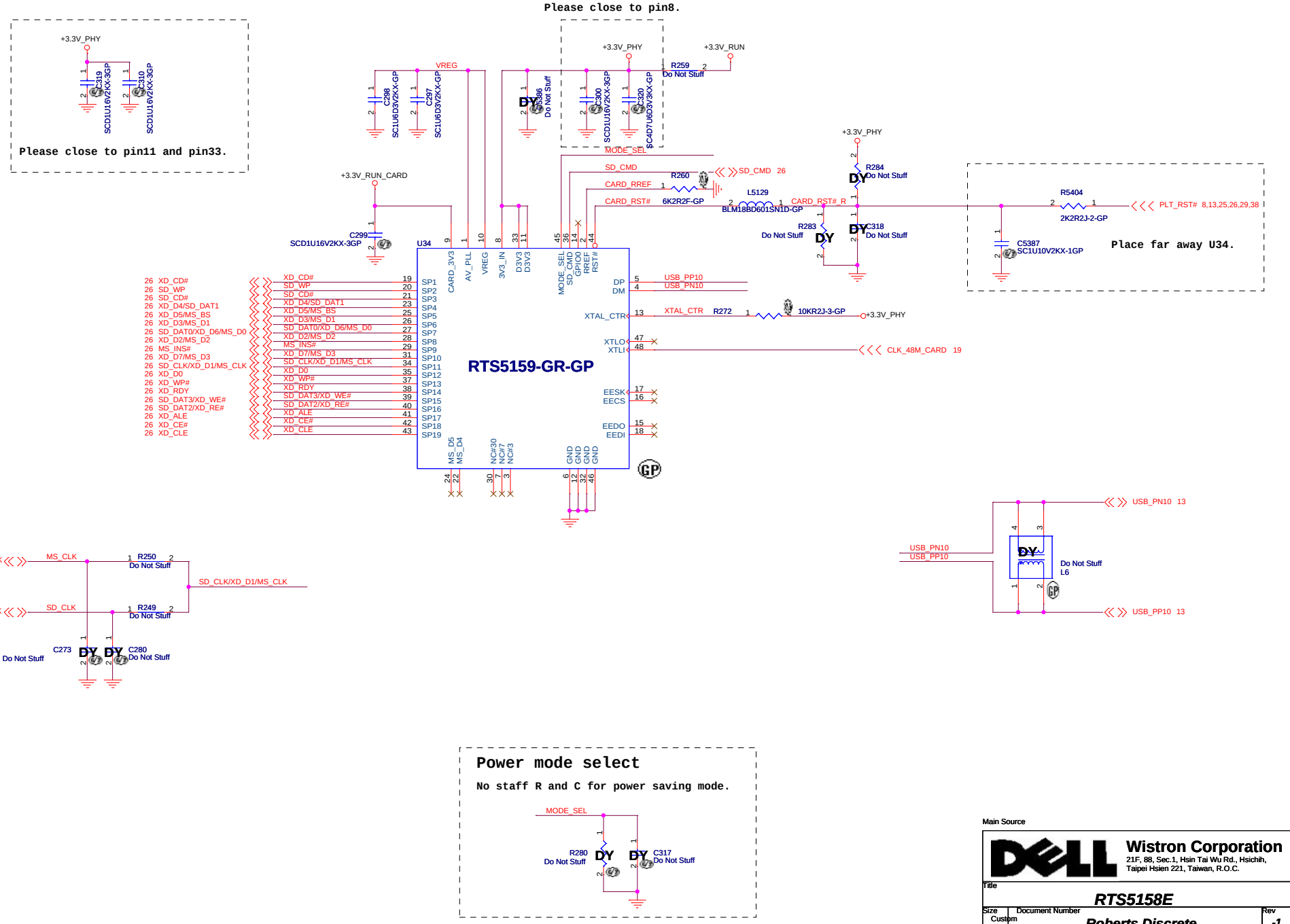


Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***USB***	
Size: Custom	Document Number: ***Roberts Discrete***	Rev: ***-1***
Date: Tuesday, May 19, 2009	Sheet 31 of 60	

SSID = SDIO



Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

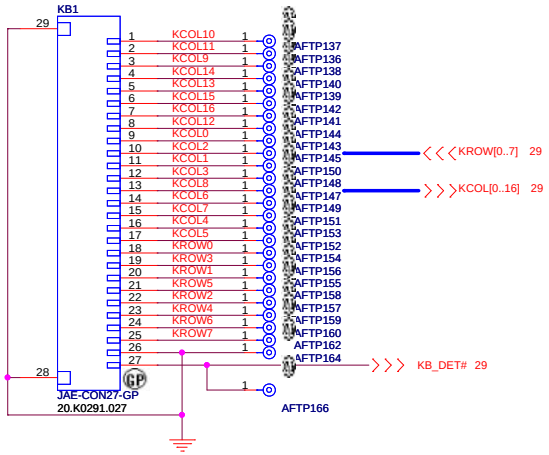
Title: ***RTS5158E***

Size	Document Number	Rev
Custom	***Roberts Discrete***	-1

Date: Tuesday, May 19, 2009 Sheet 32 of 60

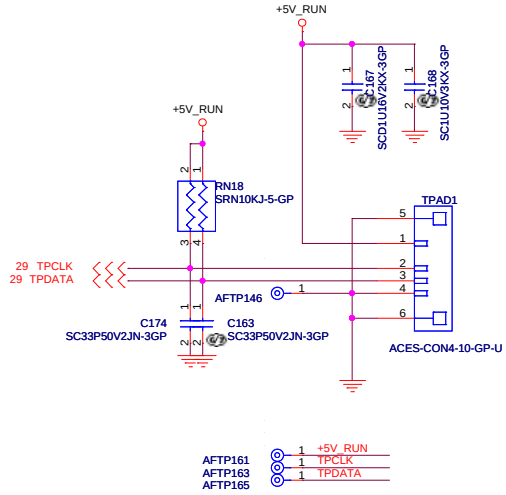
SSID = KBC

Internal KeyBoard Connector

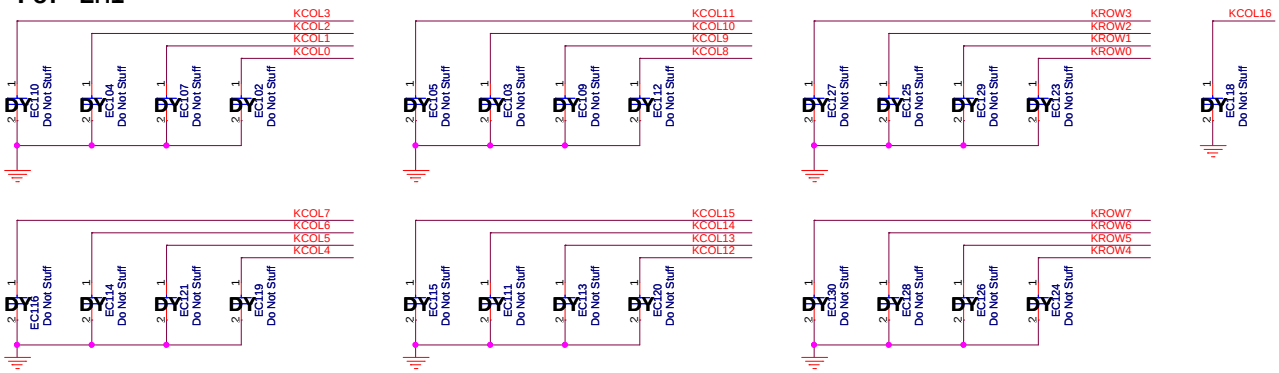


SSID = Touch.Pad

TouchPad Connector



For EMI

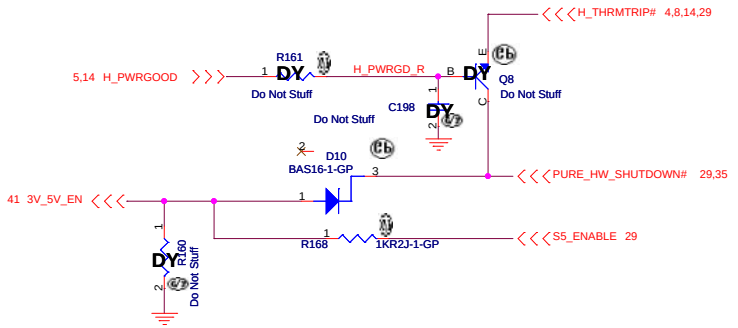


Main Source

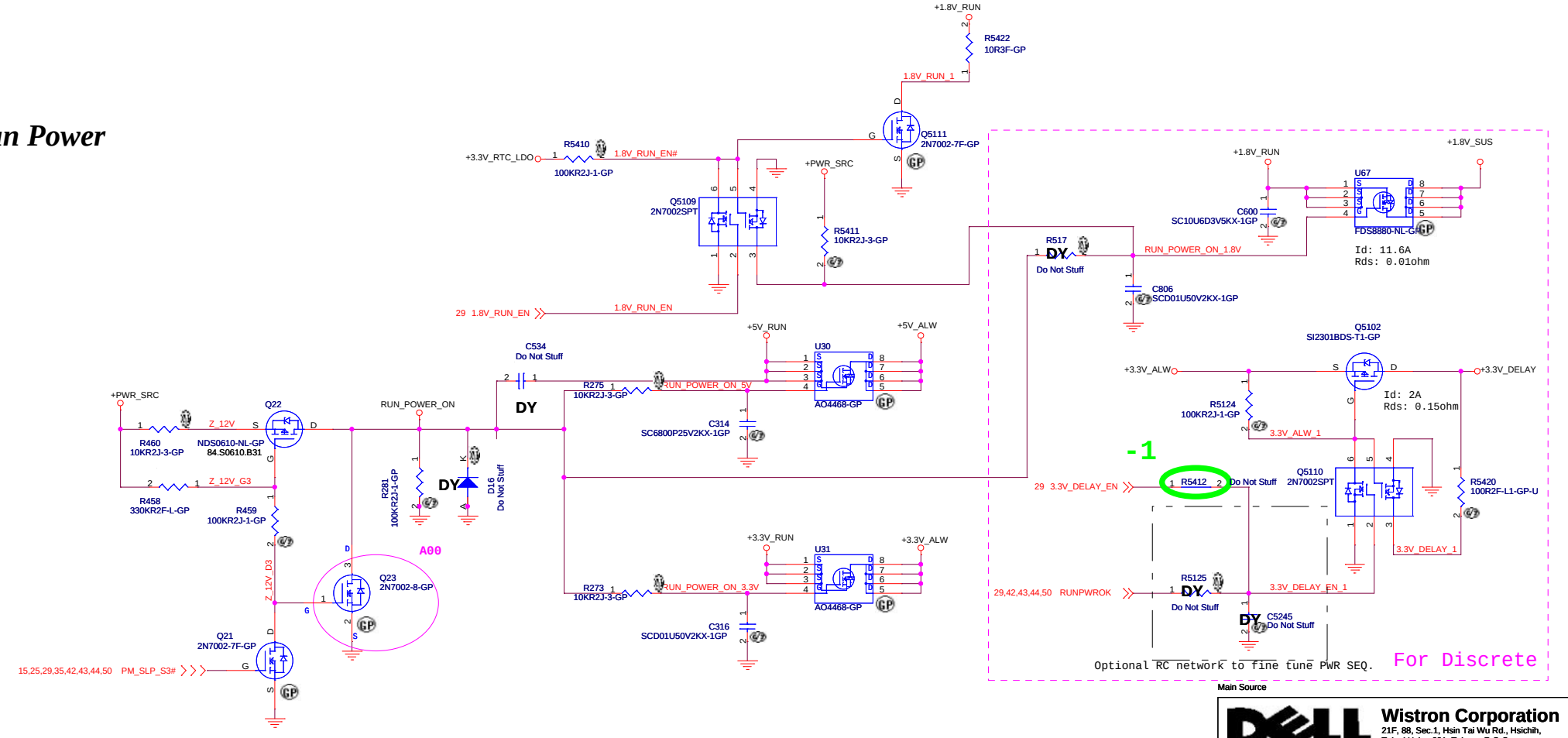
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	KeyBoard/Touch Pad	
Size: Custom	Document Number: Roberts Discrete	Rev: -1
Date: Tuesday, May 19, 2009	Sheet 33 of 60	

SSID = Reset.Suspend



Run Power



Main Source

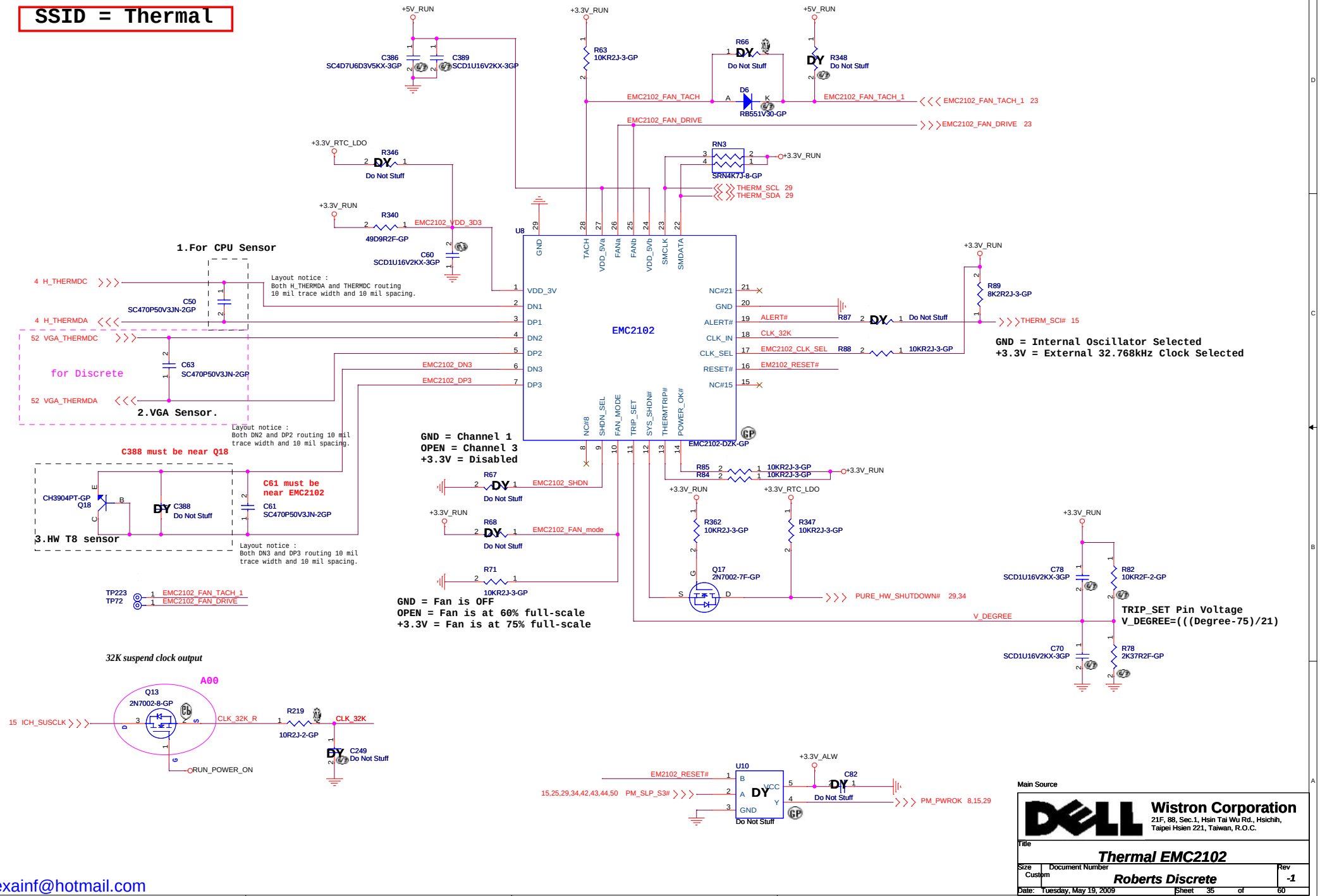
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Plane Enable***

Size	Document Number	Rev
Custom	***Roberts Discrete***	*-1*

Date: Tuesday, May 19, 2009 Sheet 34 of 60

SSID = Thermal

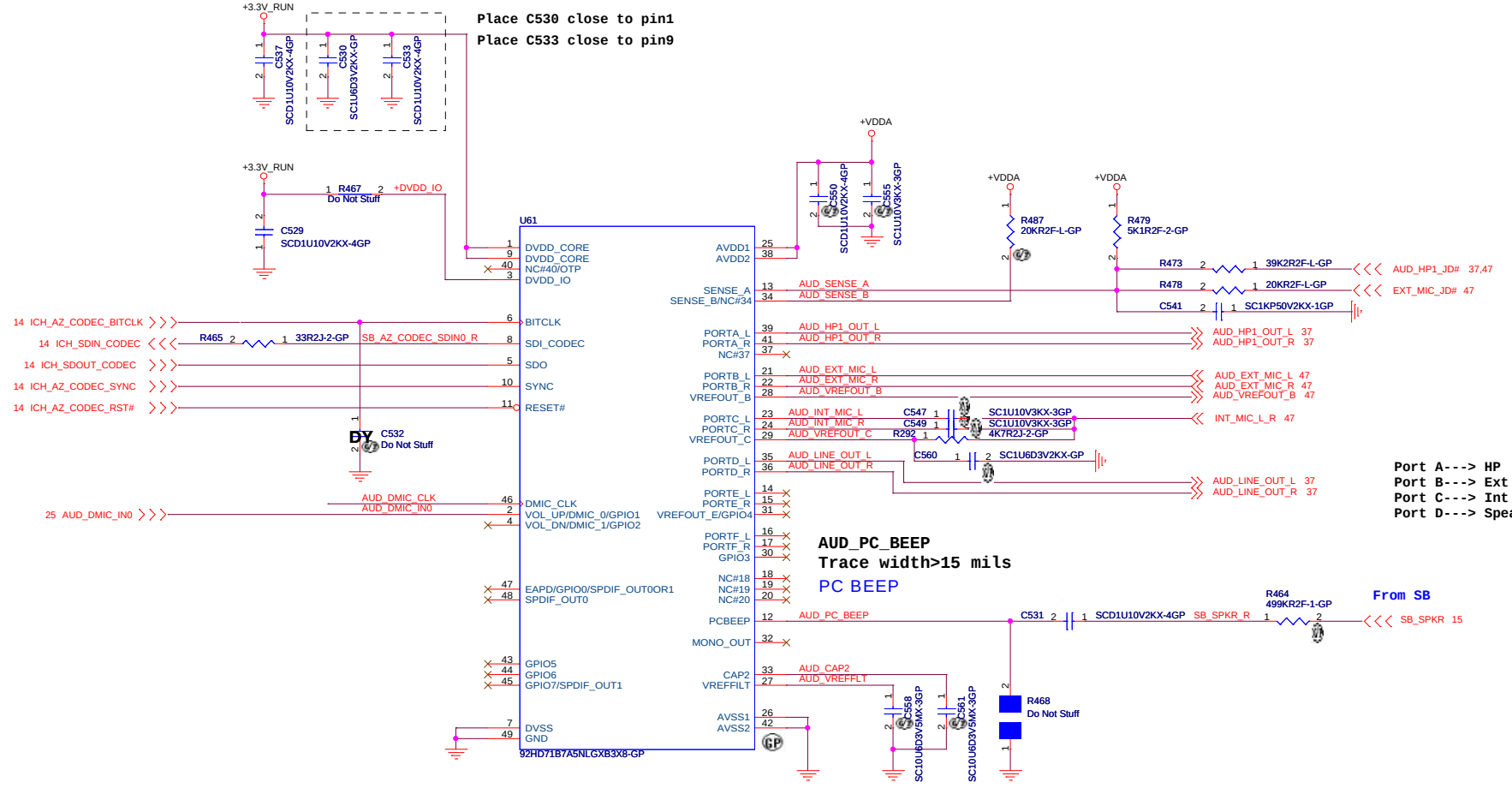


Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Thermal EMC2102	
Size: Custom	Document Number: Roberts Discrete	Rev: -1
Date: Tuesday, May 19, 2009	Sheet 35 of 60	

SSID = AUDIO



Main Source

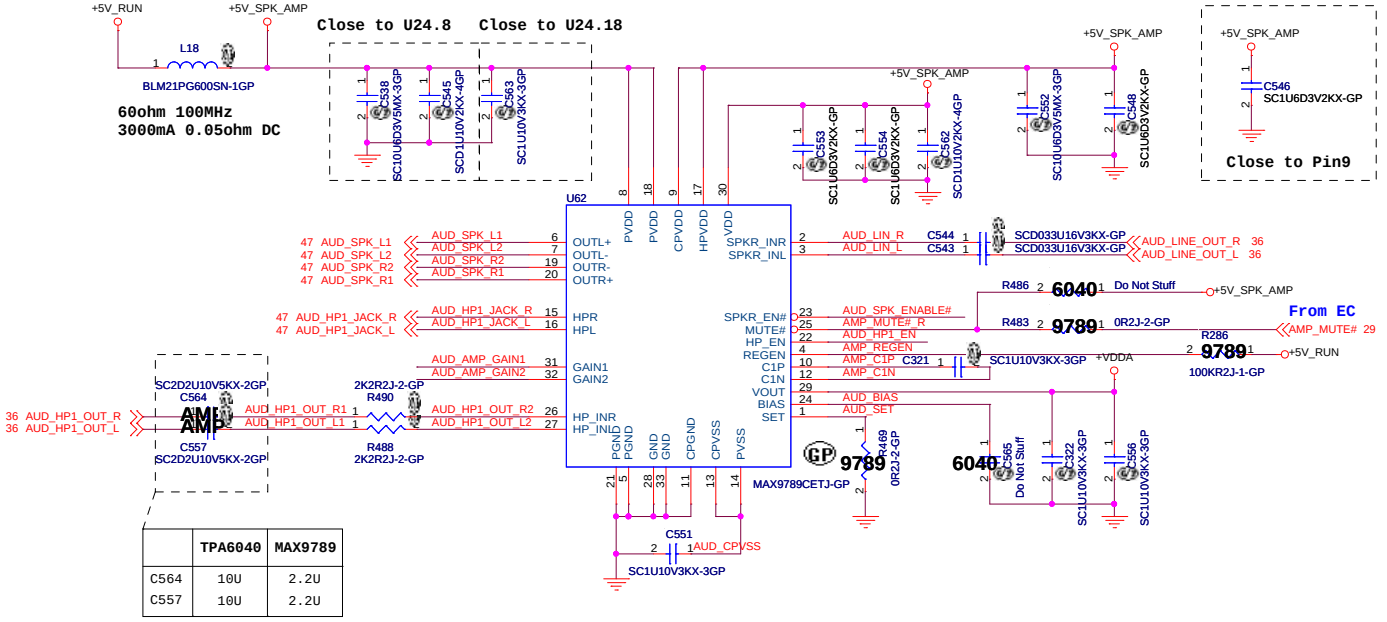
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC 92HD71B7**

Size	Document Number	Rev
Custom	Roberts Discrete	-1

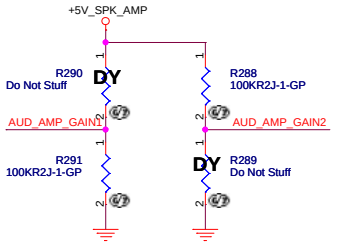
Date: Tuesday, May 19, 2009 Sheet 36 of 60

SSID = AUDIO



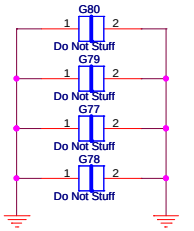
	TPA6040	MAX9789
C564	10U	2.2U
C557	10U	2.2U

GAIN SETTING

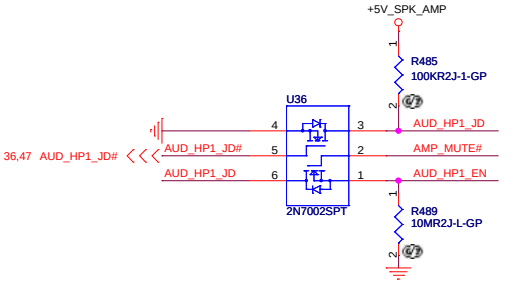


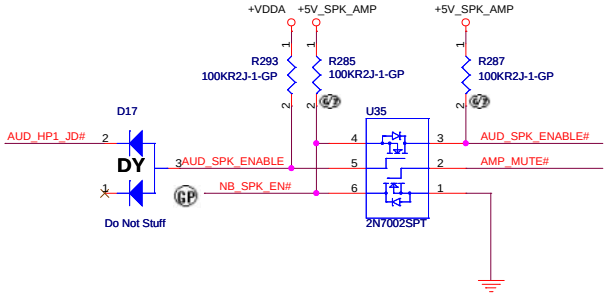
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

	Main source	Second source
	TPA6040A (74.06040.013)	MAX9789A (74.09789.013)
R486	100K	No ASM
R483	No ASM	0 Ohm
R469	No ASM	0 Ohm
R286	No ASM	100K
C535	0.033uF	No ASM
C566	0.033uF	No ASM
C565	1uF	No ASM
C567	No ASM	0.1uF
C564	10uF	2.2uF
C557	10uF	2.2uF



Signal inverter for speaker shutdown





Main Source

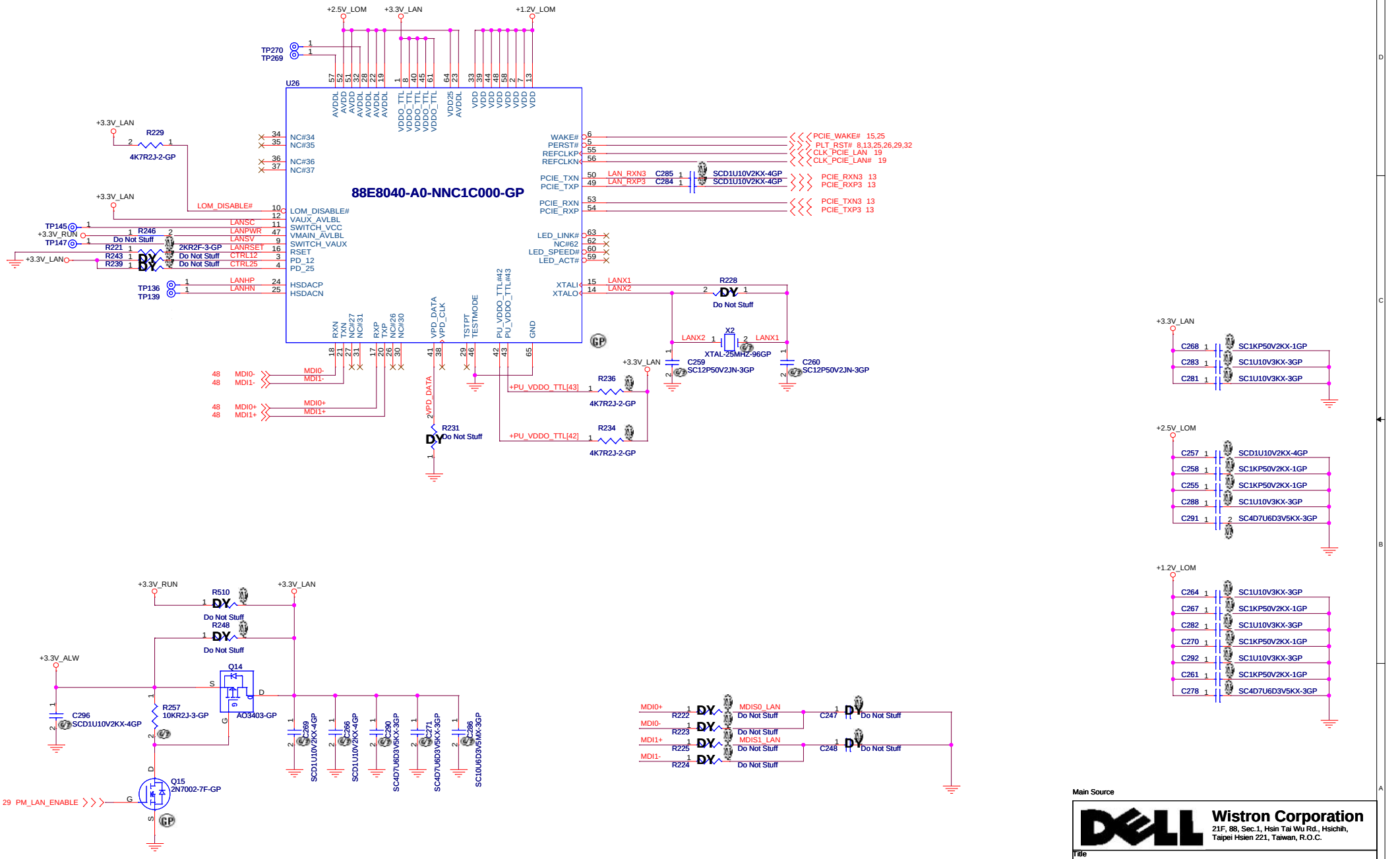
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 37 of 60

SSID = LOM



Main Source

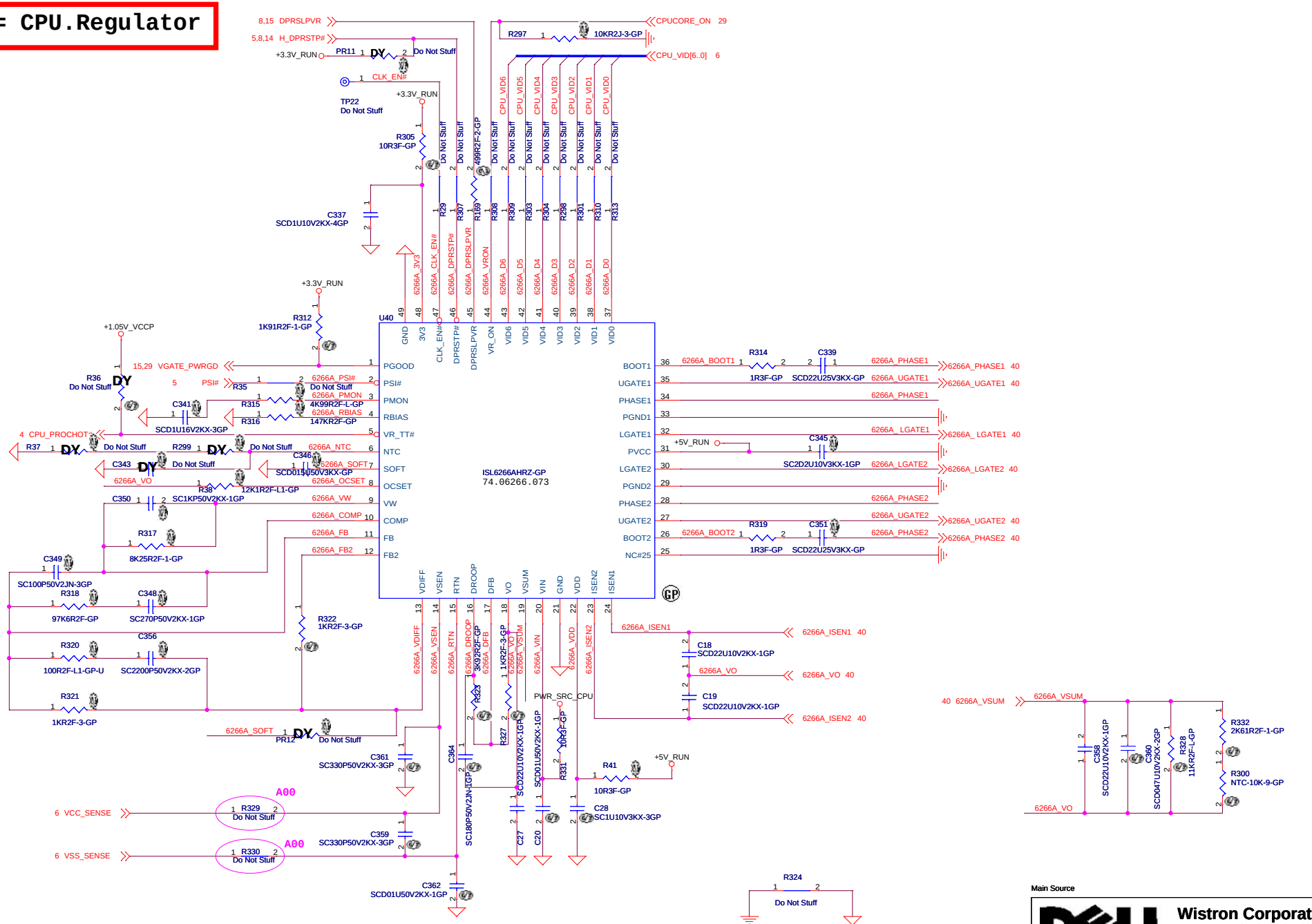
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Marvell-88E8040**

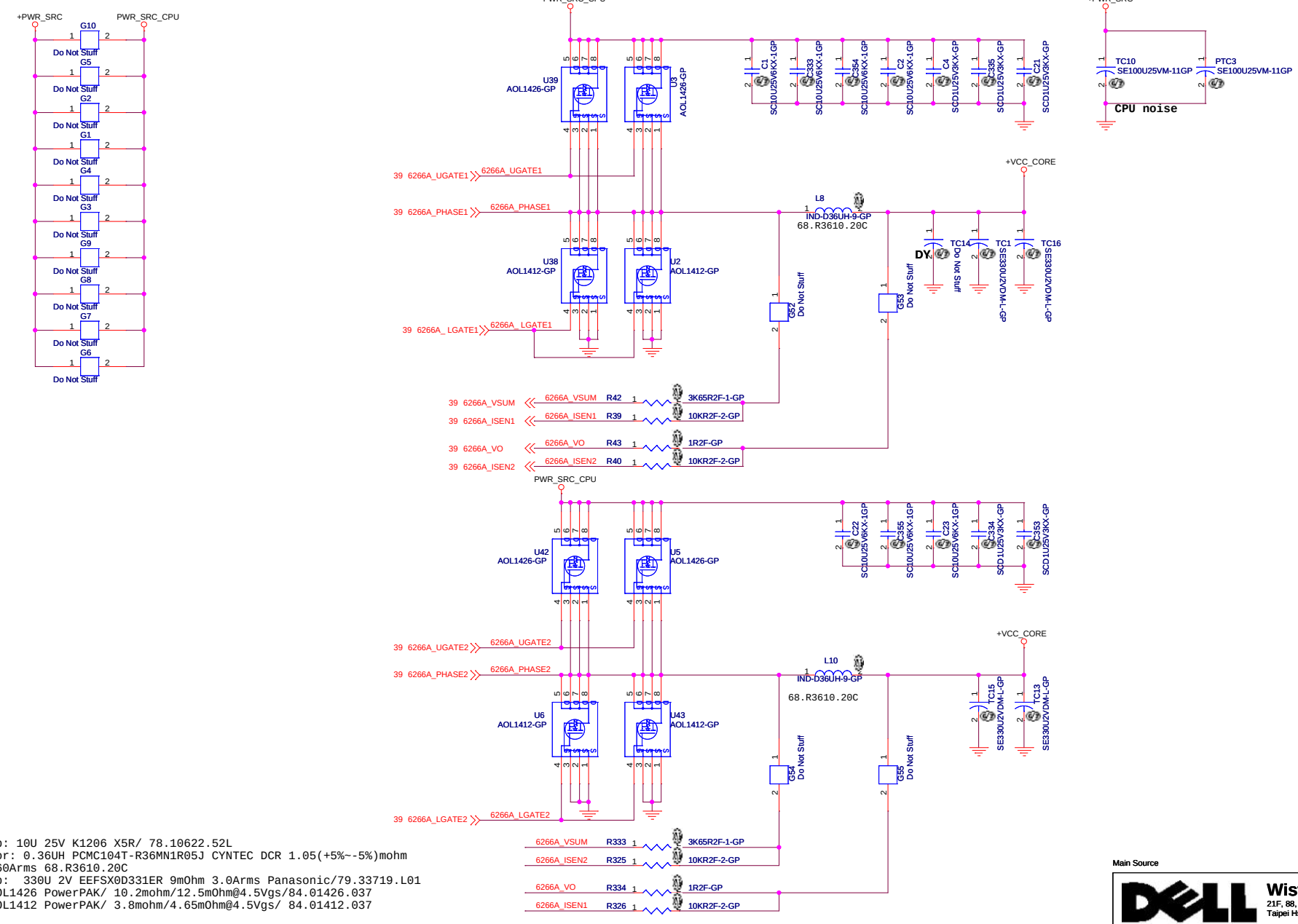
Size	Document Number	Rev
Custom	Roberts Discrete	-1

Date: Tuesday, May 19, 2009 Sheet 38 of 60

SSID = CPU.Regulator



SSID = CPU.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: AOL1426 PowerPAK/ 10.2mohm/12.5mOhm@4.5Vgs/84.01426.037
L/S: AOL1412 PowerPAK/ 3.8mohm/4.65mOhm@4.5Vgs/ 84.01412.037

Main Source

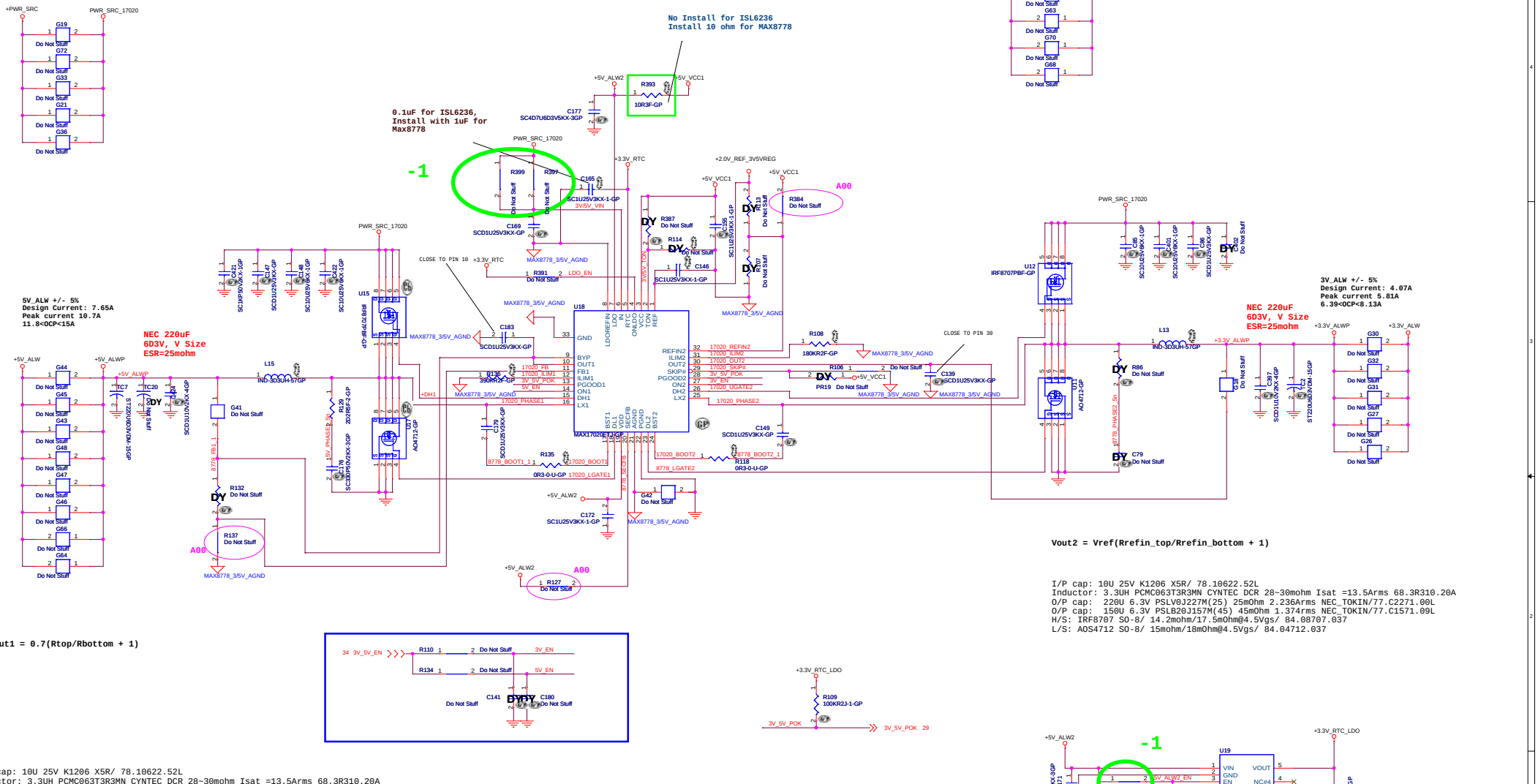
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU VCORE POWER(2/2)

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 40 of 60

SSID = PWR.Plane.Regulator_3p3v5v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC063T3R3MN CYNTEC DCR 28~30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 150U 6.3V PSLB20J157M(45) 45mOhm 1.374rms NEC_TOKIN/77.C1571.09L
H/S: IRF8707 SO-8/ 14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: AOS4712 SO-8/ 15mohm/18mOhm@4.5Vgs/ 84.04712.037

SKIPSEL	GND	Open/REF (2V)	High (VCC or 3.3V)
Operating Mode	pulse-skipping mode	ultrasonic mode	forced-PWM operation

TONSEL	GND	Open (REF)	High (VCC)
CH1 Freq	400kHz	400kHz	200kHz
CH2 Freq	500kHz	300kHz	300kHz

LDOREFIN	GND	VCC	VLDOREFIN = 0.5V
Operating Mode	4.90/5.0/5.10	3.23/3.3/3.37	0.96/1.0/1.04

FB1	GND	VCC	
Operating Mode	4.925/5.00/5.075	1.482/1.50/1.518	

REFIN2	5V	RTC (3.3V)	
Operating Mode	3.255/3.30/3.345	1.038/1.050 /1.062	

Main Source

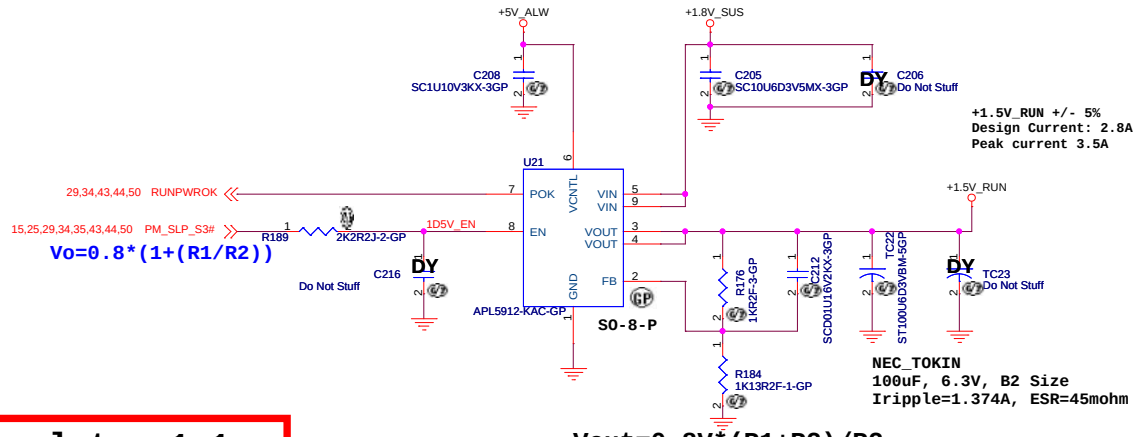
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 3.3V/5V

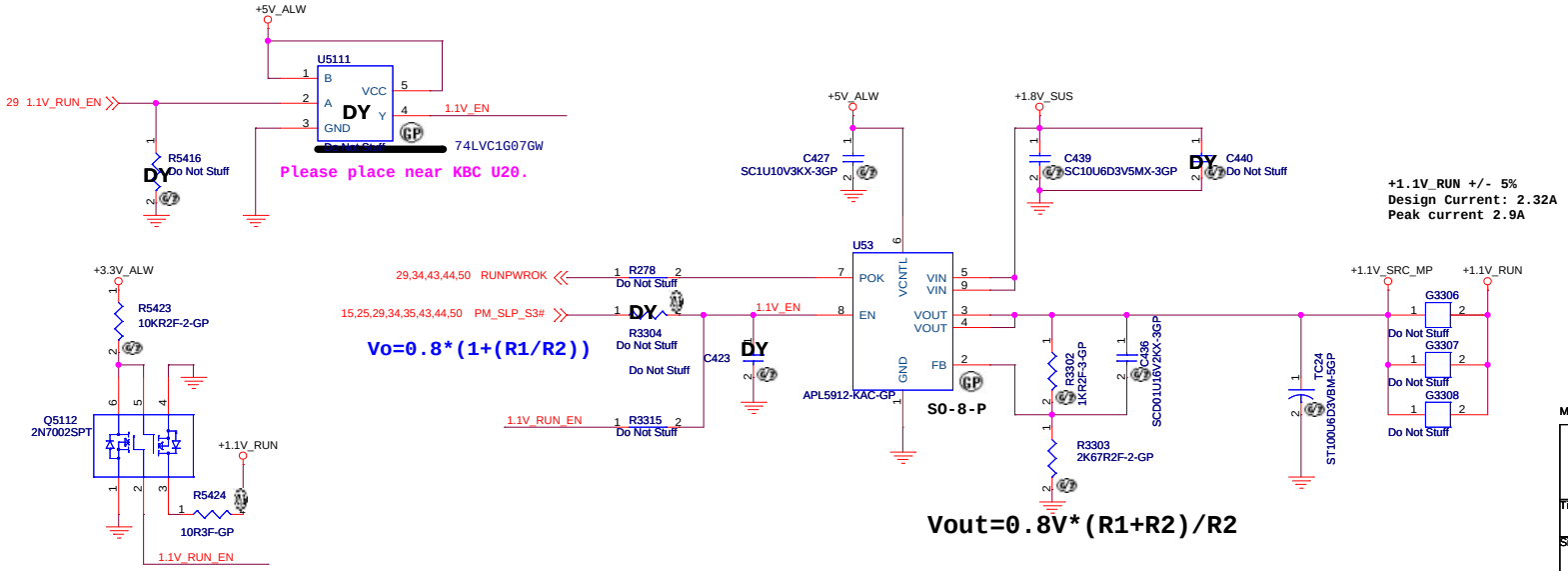
Size	Document Number	Rev
A2	Roberts Discrete	-1

Date: Tuesday, May 19, 2009 Sheet 41 of 60

SSID = PWR.Plane.Regulator_1p5v



SSID = PWR.Plane.Regulator_1p1v

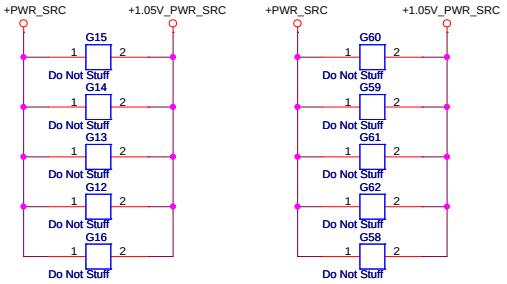


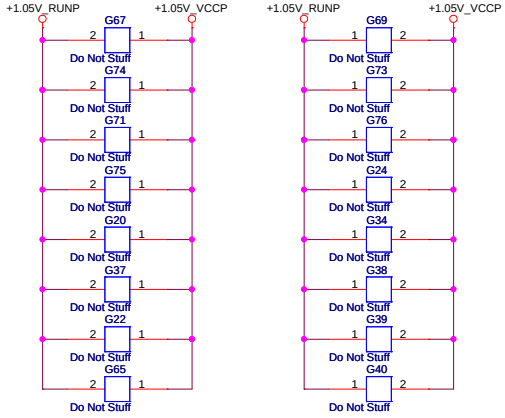
Main Source

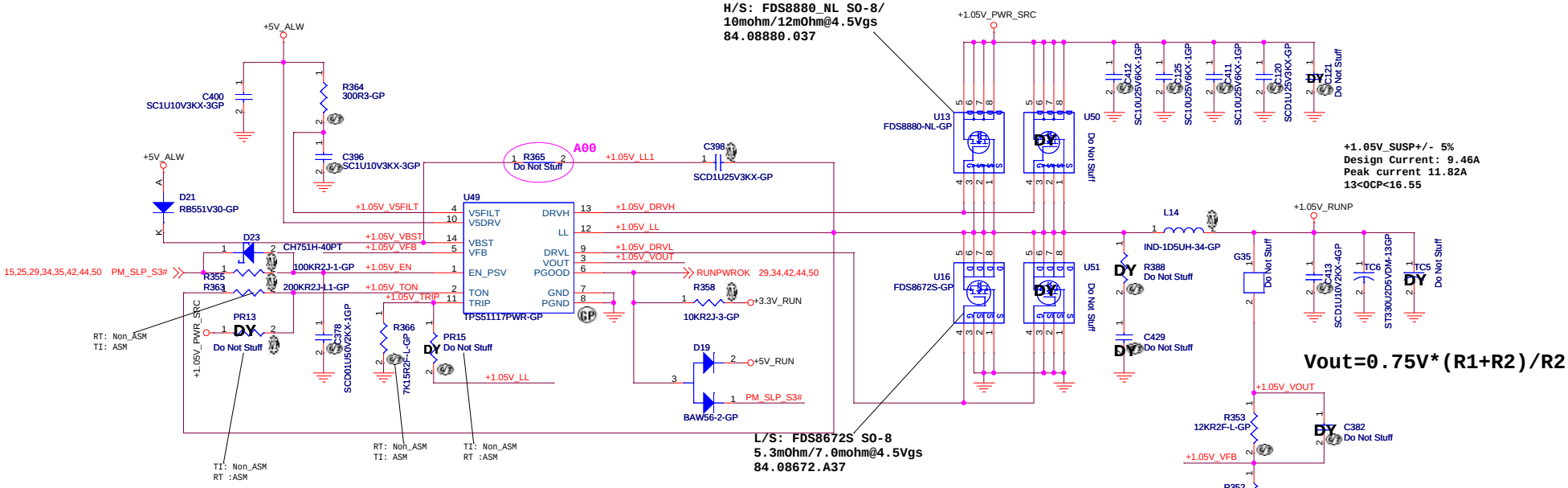
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC to DC 1.5V/1.1V	
Size: Custom	Document Number: Roberts Discrete	Rev: -1
Date: Tuesday, May 19, 2009	Sheet 42 of 60	

SSID = PWR.Plane.Regulator_1p05v







I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:3.8 ~4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: IRF8707 SO-8/14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->350KHz

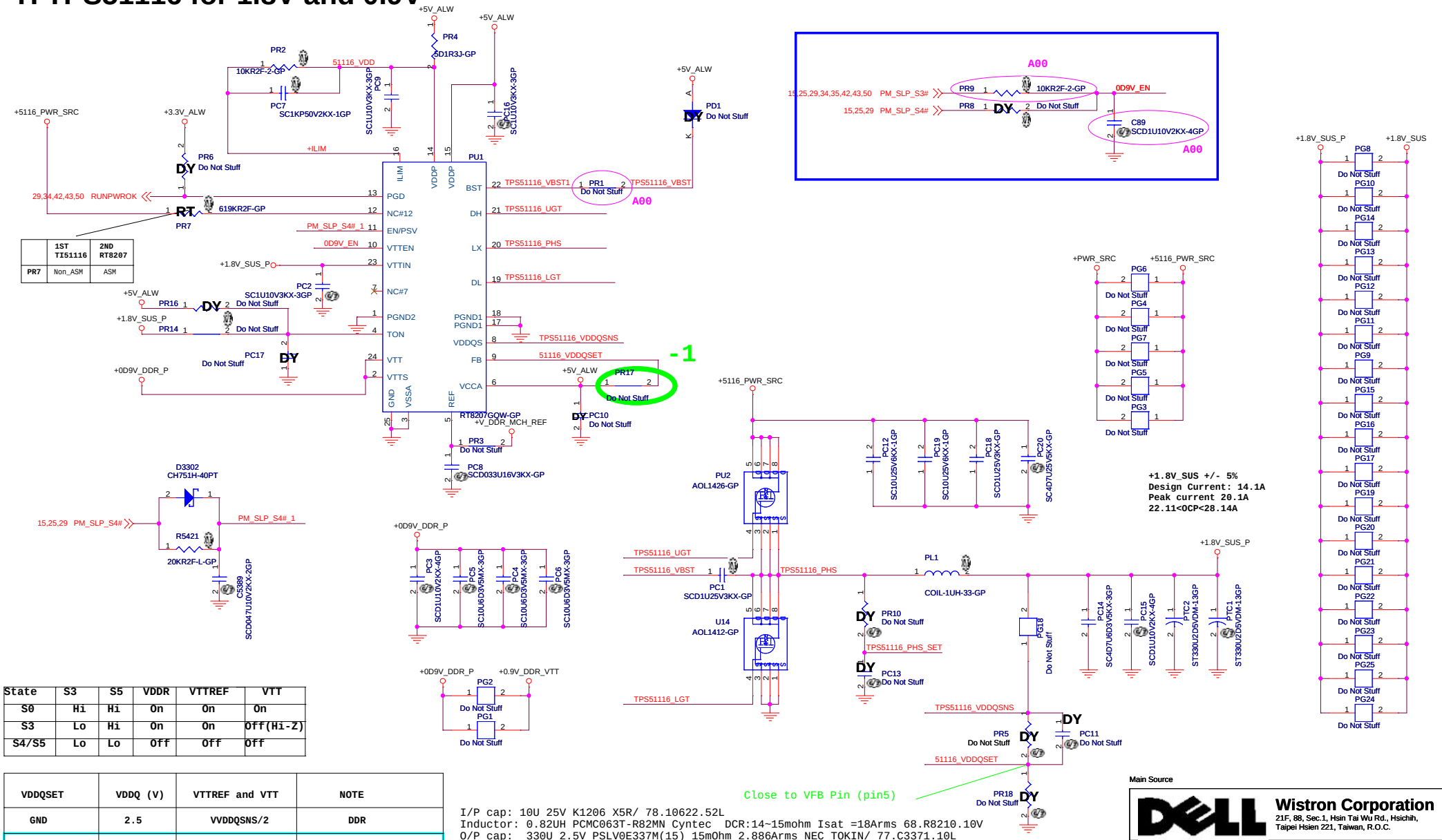
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC to DC 1.05V	
Size: Custom	Document Number: Roberts Discrete	Rev: -1
Date: Tuesday, May 19, 2009	Sheet 43 of 60	

SSID = PWR.Plane.Regulator_1p8v0p9v

TI TPS51116 for 1.8V and 0.9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

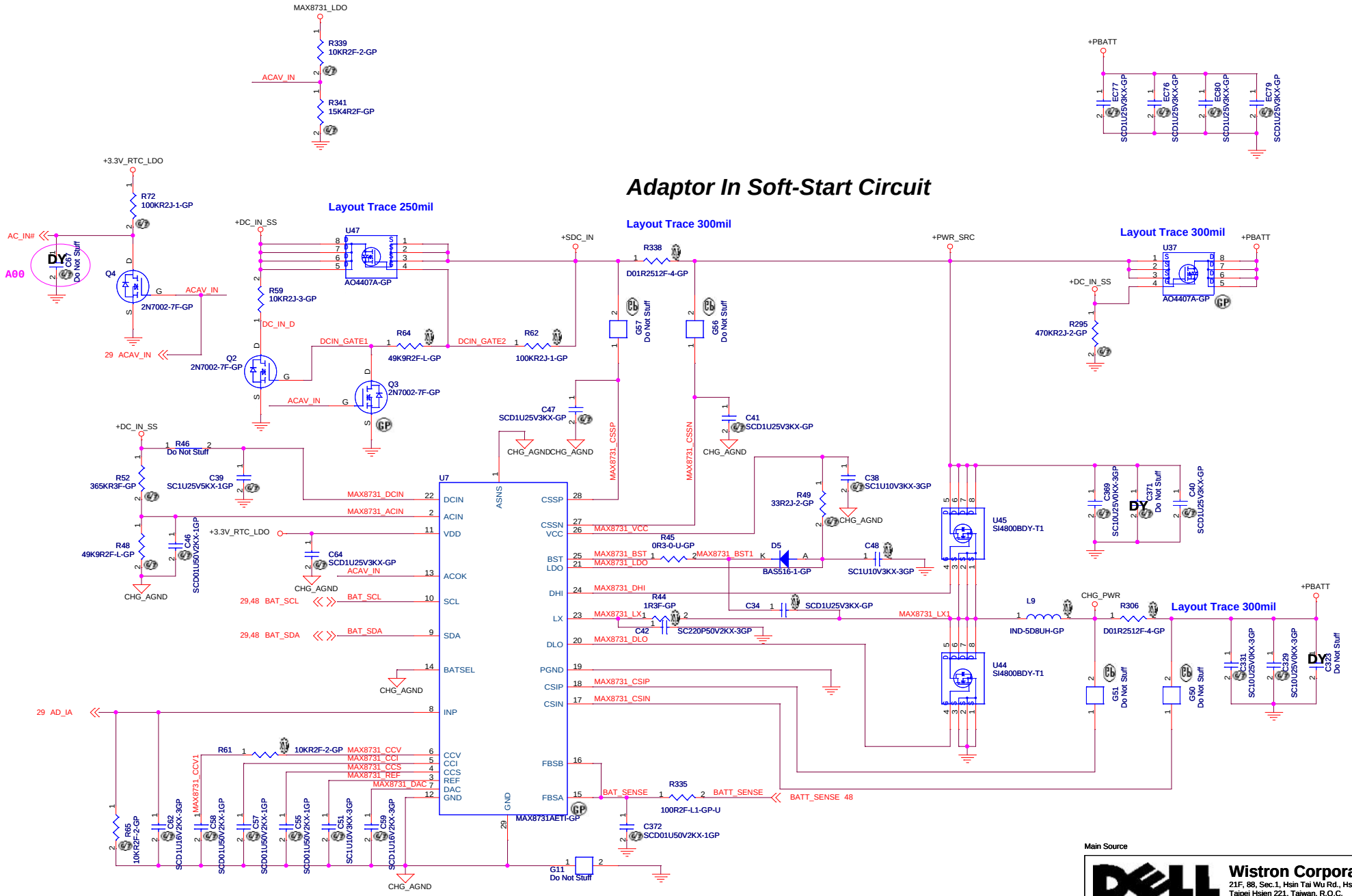
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.82UH PCMC063T-R82MN Cyntec DCR:14~15mohm Isat =18Arms 68.R8210.10V
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: AOL1426 PowerPAK/ 10.2mohm/12.5mOhm@4.5Vgs/84.01426.037
L/S: AOL1412 PowerPAK/ 3.8mohm/4.65mOhm@4.5Vgs/ 84.01412.037
Switching freq-->400KHz

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.8V/0.9V
Size: Custom | Document Number: Roberts Discrete | Rev: -1
Date: Tuesday, May 19, 2009 | Sheet 44 of 60

SSID = Charger



Main Source

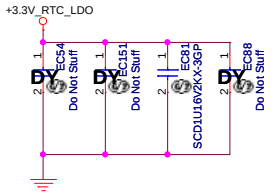
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

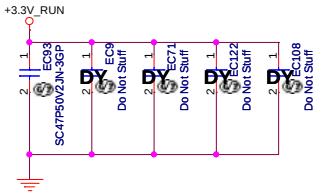
Title: CHARGER MAX8731

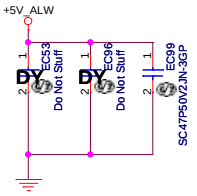
Size	Document Number	Rev
Custom	Roberts Discrete	-1

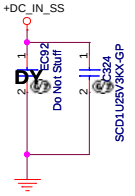
Date: Tuesday, May 19, 2009 Sheet 45 of 60

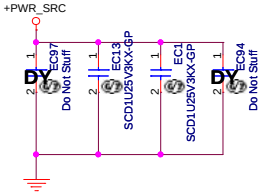
SSID = Mechanical

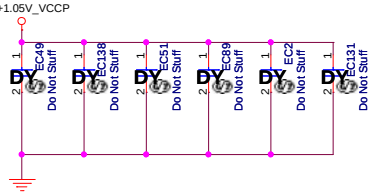


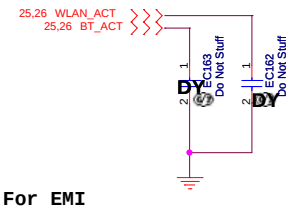


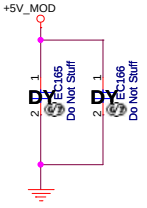


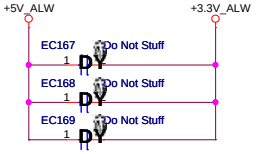


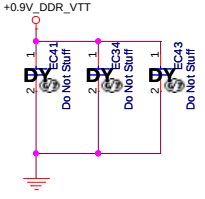


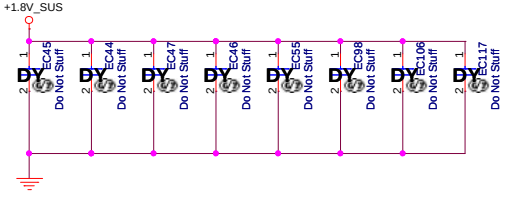




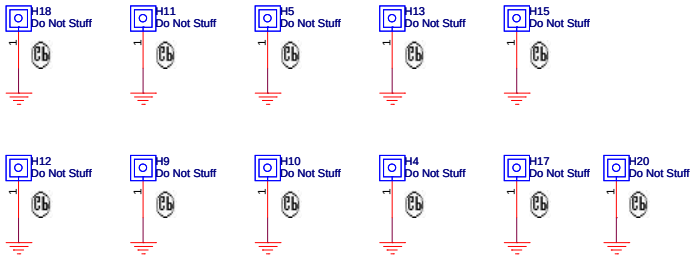








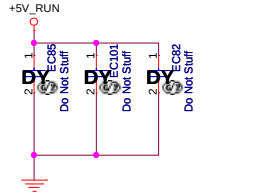
For EMI

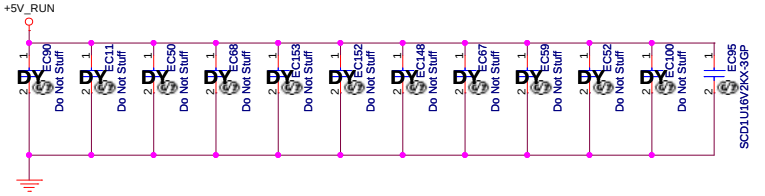


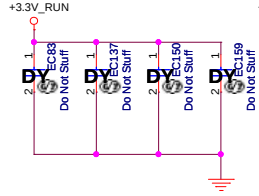
34.4W005.301
Mini Card BOSS

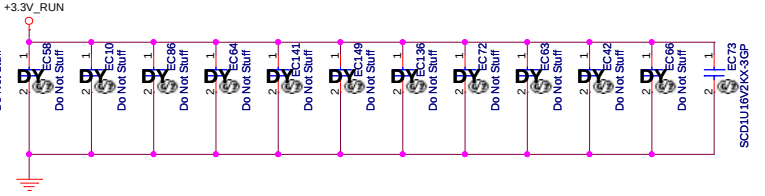
34.4W004.501
New Card BOSS

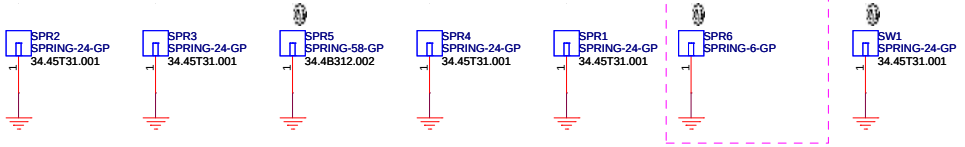
34.4W001.201
NB Thermal BOSS

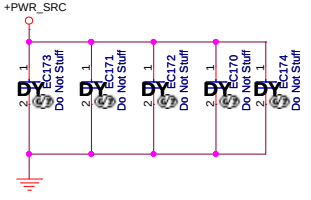












Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

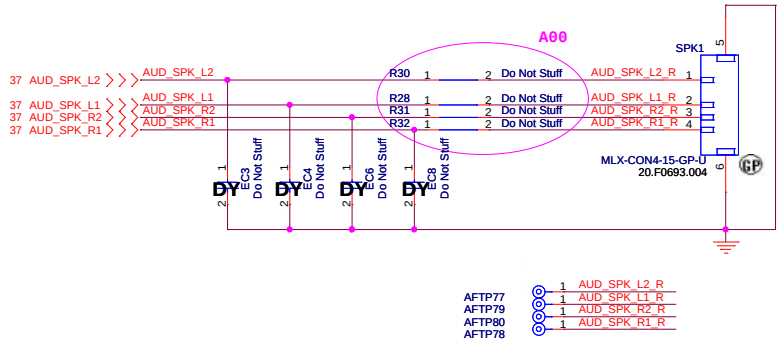
Title: MISC

Size: Custom | Document Number: Roberts Discrete | Rev: -1

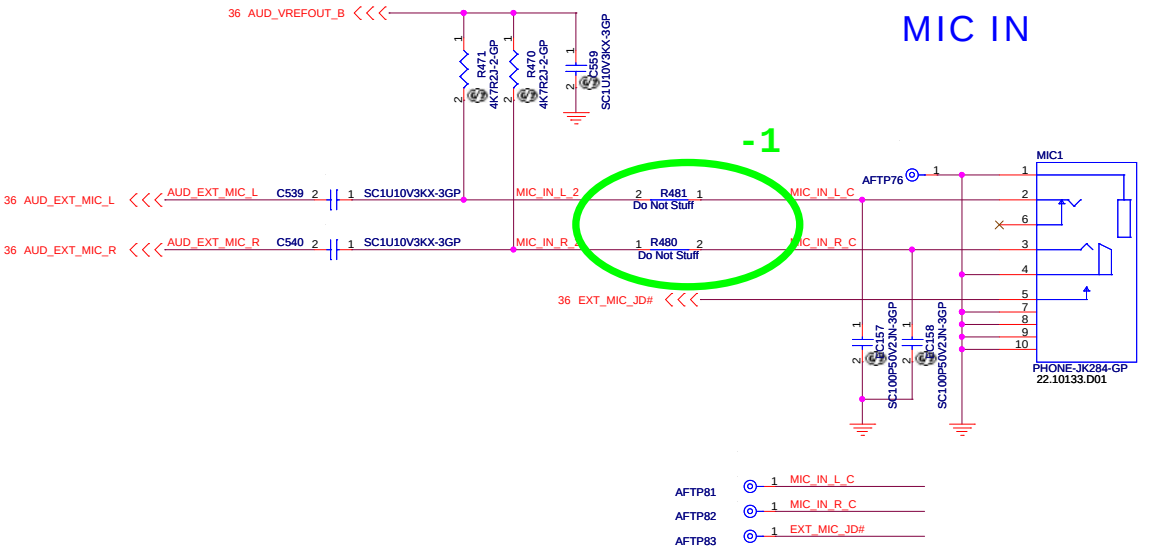
Date: Tuesday, May 19, 2009 | Sheet 46 of 60

SSID = AUDIO

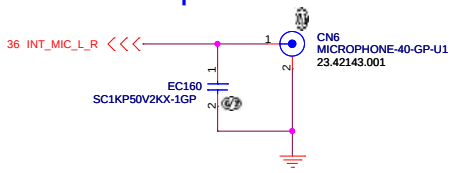
Speaker Connector



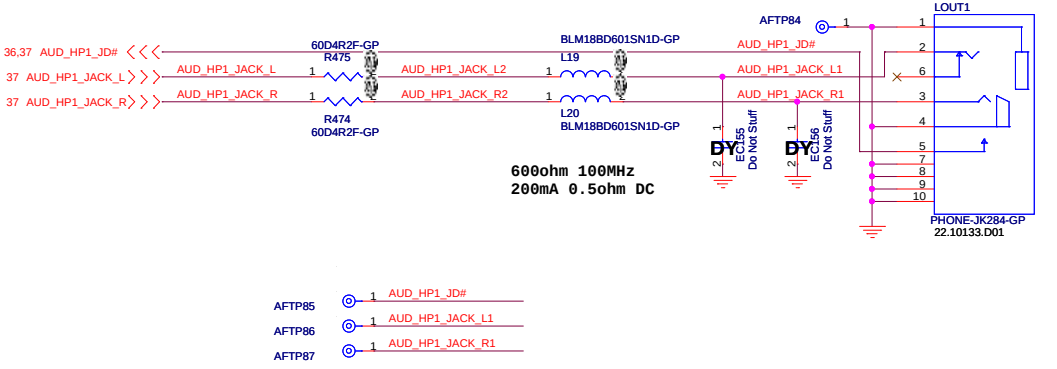
MIC IN



Internal Microphone



LINE1 OUT



Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

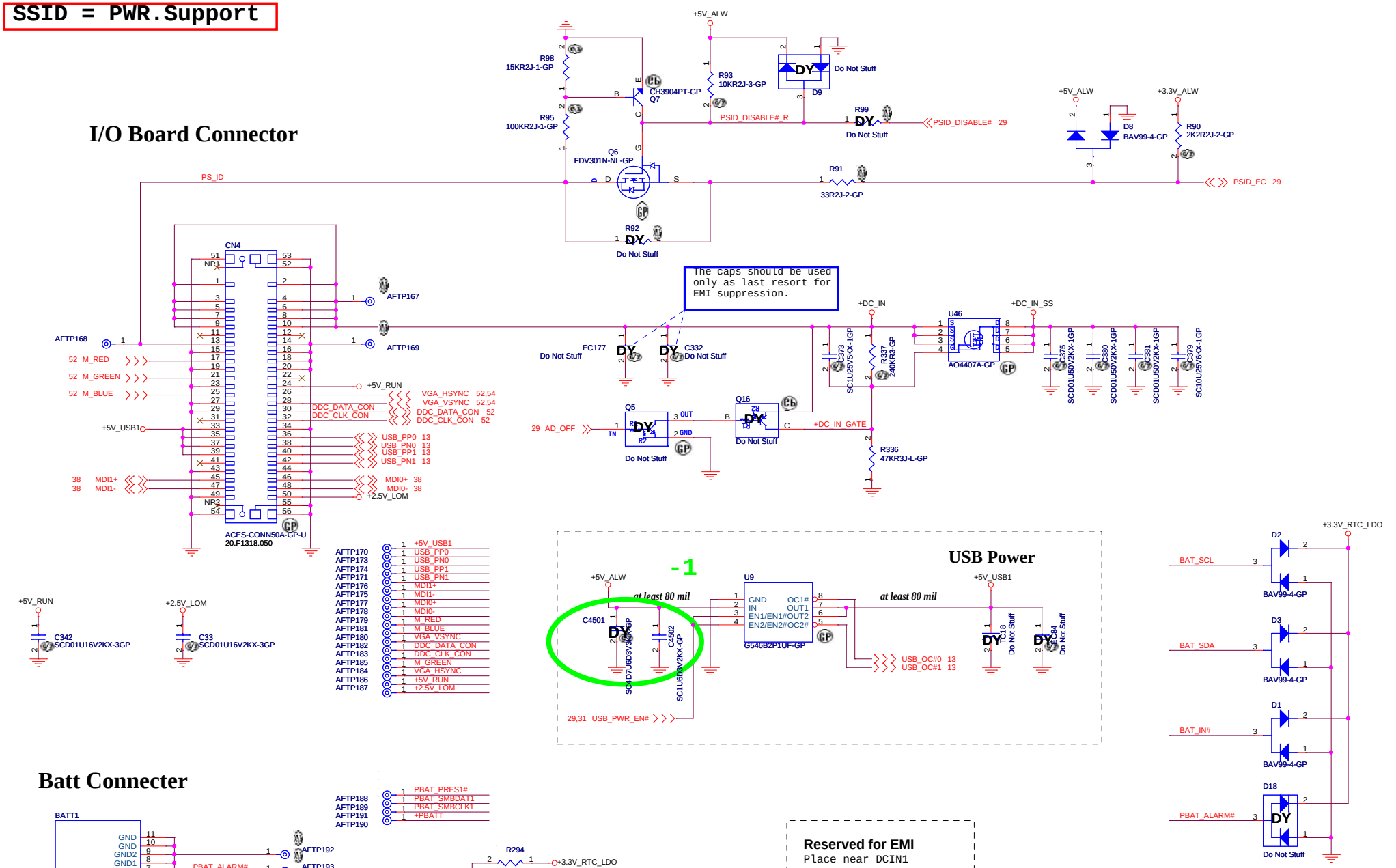
Title: ***Audio Jack***

Size: Custom | Document Number: ***Roberts Discrete*** | Rev: -1

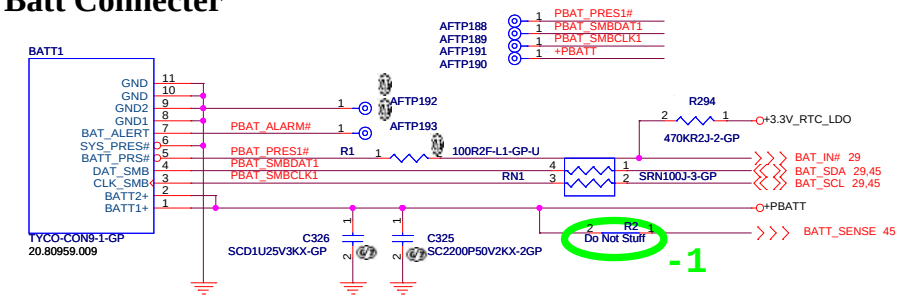
Date: Tuesday, May 19, 2009 | Sheet 47 of 60

SSID = PWR.Support

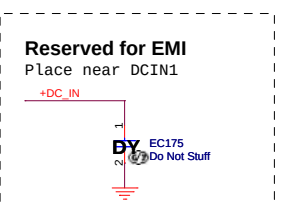
I/O Board Connector



Batt Connecter



Reserved for EMI
Place near DCIN1



Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LEFT IO/BATT CONN	
Size: Custom	Document Number: Roberts Discrete	Rev: -1
Date: Tuesday, May 19, 2009	Sheet 48 of 60	

(Blanking)

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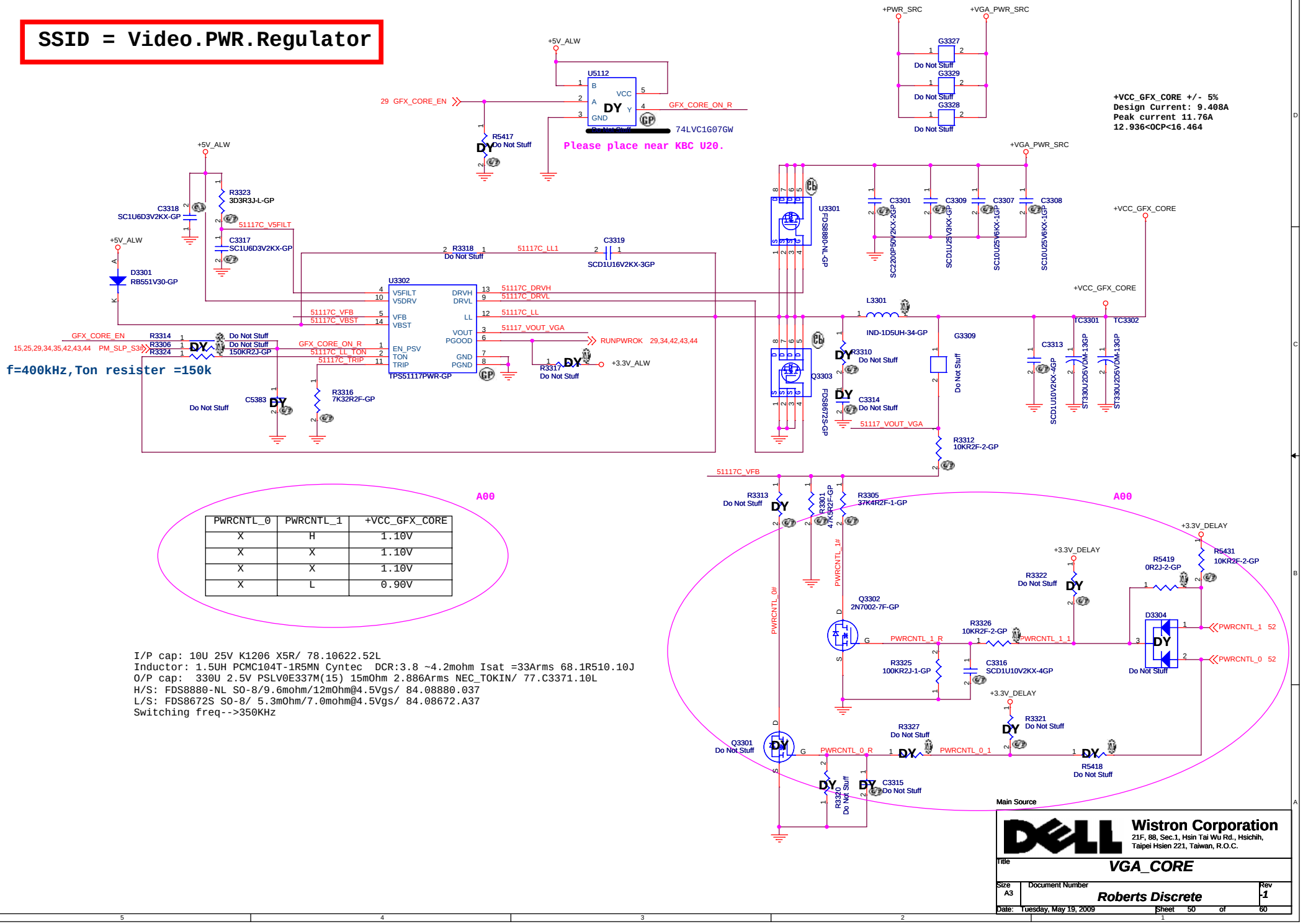
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Port

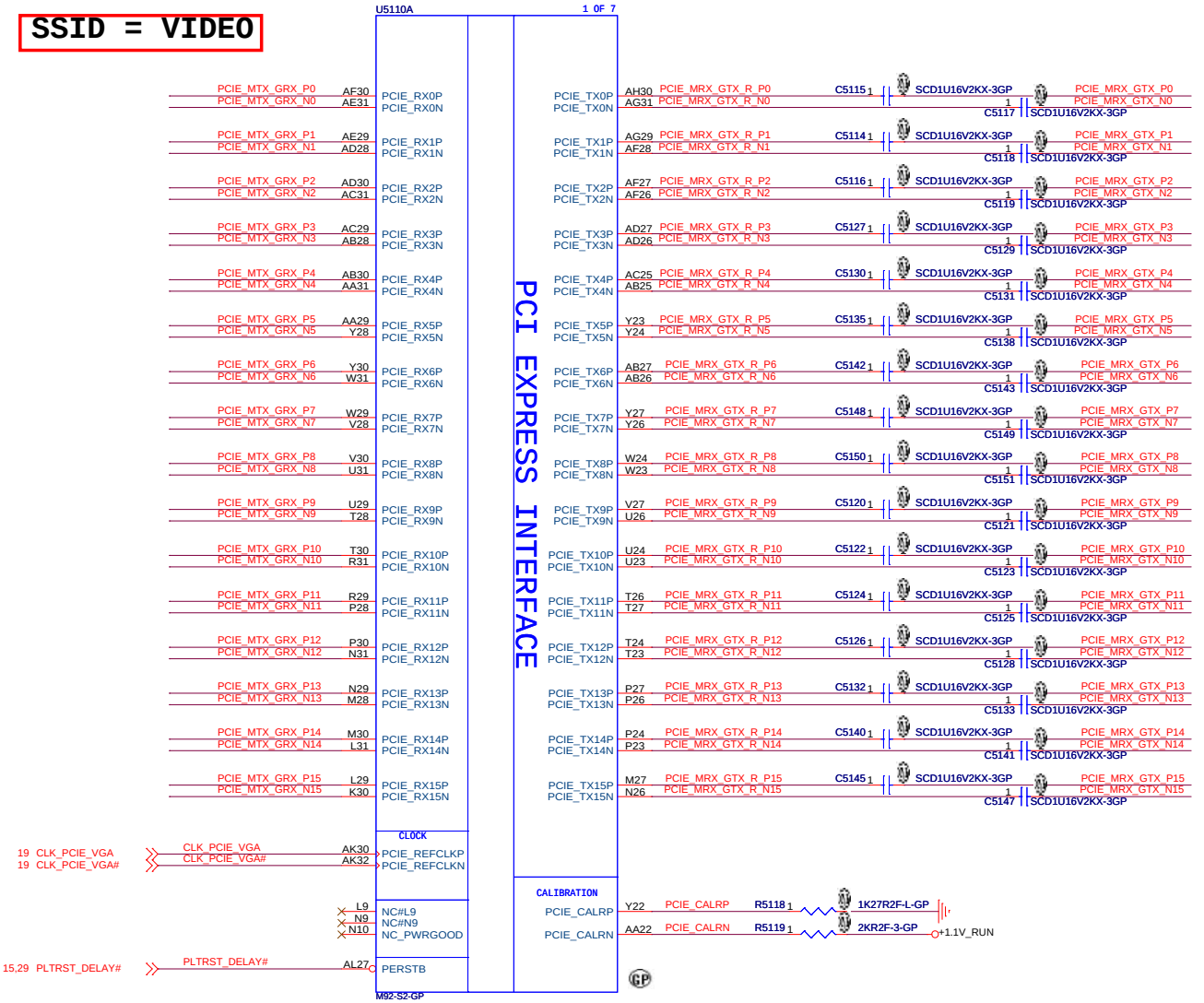
Size: Custom | Document Number: Roberts Discrete | Rev: -1

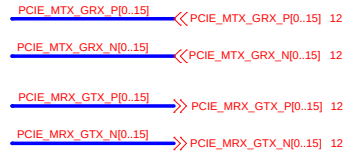
Date: Tuesday, May 19, 2009 | Sheet 49 of 60

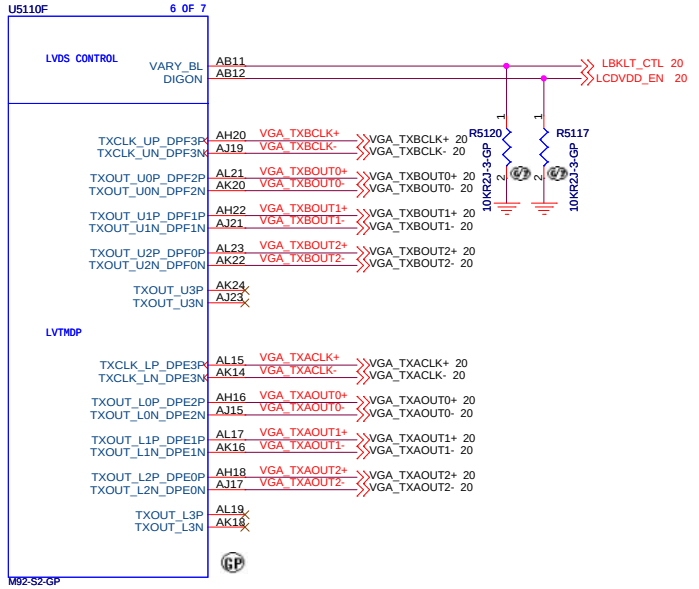
SSID = Video.PWR.Regulator



SSID = VIDEO







Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-PCIE/LVDS(1/4)

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 51 of 60

SSID = VIDEO

U5110B

2 OF 7

MUTI GFX

DPA

DPB

I2C

GENERAL PURPOSE I/O

DAC1

DAC2

DDC/AUX

PLL/CLOCK

THERMAL

M92-S2-GP

+DPLL_PVDD

+1.8V_RUN

L5126

BLM15BD121SN1D-GP

+DPLL_VDDC

+1.1V_RUN

L5122

+3.3V_DELAY

R144 Do Not Stuff

R140 Do Not Stuff

20 LDDC_CLK

20 LDDC_DATA

R5215 Do Not Stuff

R5216 Do Not Stuff

SCL

SDA

R5203 10KR2J-3-GP

VGA_CLK_REQ#

54 DVPDATA20

54 DVPDATA21

54 DVPDATA22

54 DVPDATA23

54 GPIO_VGA_00

54 GPIO_VGA_01

54 GPIO_VGA_02

54 GPIO_VGA_05

TP5141

29 PANEL_BKEN

R5213 Do Not Stuff

54 GPIO_VGA_08

54 GPIO_VGA_09

54 GPIO_VGA_11

54 GPIO_VGA_12

54 GPIO_VGA_13

50 PWRCNTL_0

19 CLK_VGA_27M_SS

VGA_THERM#

TP5134

TP5133

THERMTRIP_VGA

50 PWRCNTL_1

R5121 10KR2J-3-GP

54 GPIO_VGA_22

VGA_CLK_REQ#

29 THERMTRIP_VGA#

Do Not Stuff R5218

Do Not Stuff R5219

GPIO_VGA_29

GPIO_VGA_30

Q5105 2N7002-7F-GP

R5302 1KR2J-1-GP

-1

JTAG_TRSTB

JTAG_TESTEN

TP5143

TP5142

TP5144

TP5145

TP5146

TP5151

GENERICB

TP5150

TP5138

R5196 1KR2J-1-GP

R5167 499R2F-2-GP

VREFG VOLTAGE DIVIDER IS

VREFG = VDDR4,5(1.8V) / 3 = .6V)

VGA_VREFG

R5186 249R2F-GP

C5291 SCD1U16V2KX-3GP

R5396 124R2F-U-GP

19 CLK_VGA_27M_NSS

XTALIN_R

TP5139

R5395 150R2F-1-GP

35 VGA_THERMDA

35 VGA_THERMDC

L5121 BLM15BD121SN1D-GP

TP5140

FAN_PWM

+TSVDD

C5304 SCU1U0X5X-3GP

C5290

SCD1U16V2KX-3GP

20mA

+DAC1_AVDD

+1.8V_RUN

L5120 BLM15BD121SN1D-GP

+DAC1_VDD1DI

L5125 BLM15BD121SN1D-GP

M_RED

M_GREEN

M_BLUE

R5381 150R2F-1-GP

R5382 150R2F-1-GP

R5383 150R2F-1-GP

M_RED 48

M_GREEN 48

M_BLUE 48

VGA_HSYNC 48,54

VGA_VSYNC 48,54

(Placed between this pin and AVSSQ)

VGA_RSET

R5220 499R2F-2-GP

70mA

+DAC1_AVDD

45mA

+DAC1_VDD1DI

+DAC2_VDD2DI

40mA

R5210 Do Not Stuff

Need confirm rating.

+3.3V_DELAY

+DAC2_A2VDD

65mA

R5211 Do Not Stuff

DAC2_HSYNC 54

DAC2_VSYNC 54

+DAC2_VDD2DI

+DAC2_A2VDD

+DAC2_A2VDDQ

1mA

L5127 BLM15BD121SN1D-GP

VGA_R2SET

R5162 715R2F-GP

R123 2K2R2J-2-GP

R124 2K2R2J-2-GP

R5212 Do Not Stuff

R5214 Do Not Stuff

LDDC_CLK 20

LDDC_DATA 20

R5204 Do Not Stuff

R5166 Do Not Stuff

DDC_CLK_CON

DDC_DATA_CON

M92CRT_DDCCLK

M92CRT_DDCDATA

Ask ATI do we still need 2N7002?

RN2 SRN2K2J-1-GP

U4 2N7002SPT

48 DDC_CLK_CON

DDC_DATA_CON 48

5V @ CRT side

Main Source

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

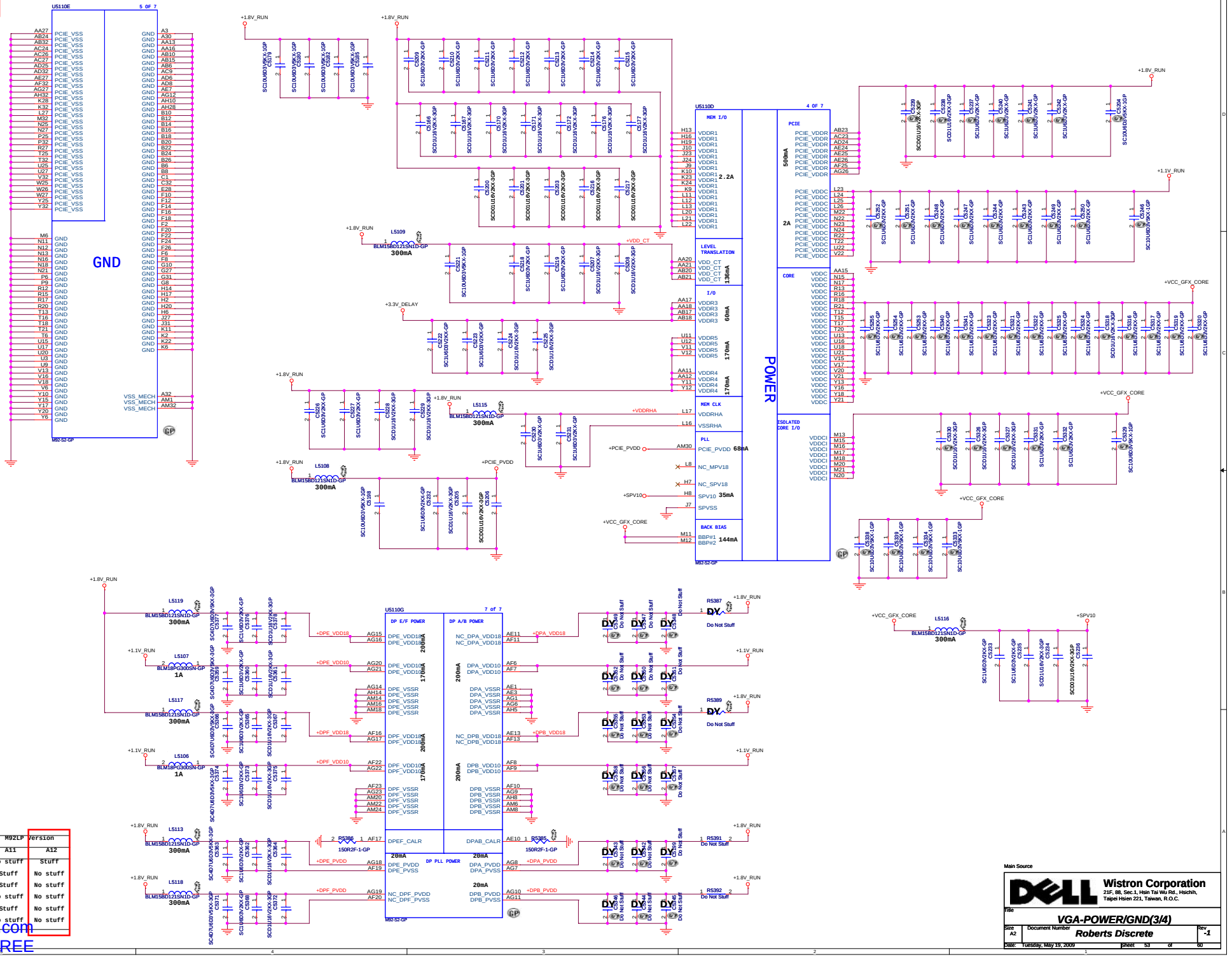
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-TV/CRT/DP PORT

Size: C | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 52 of 60

SSID = VIDEO

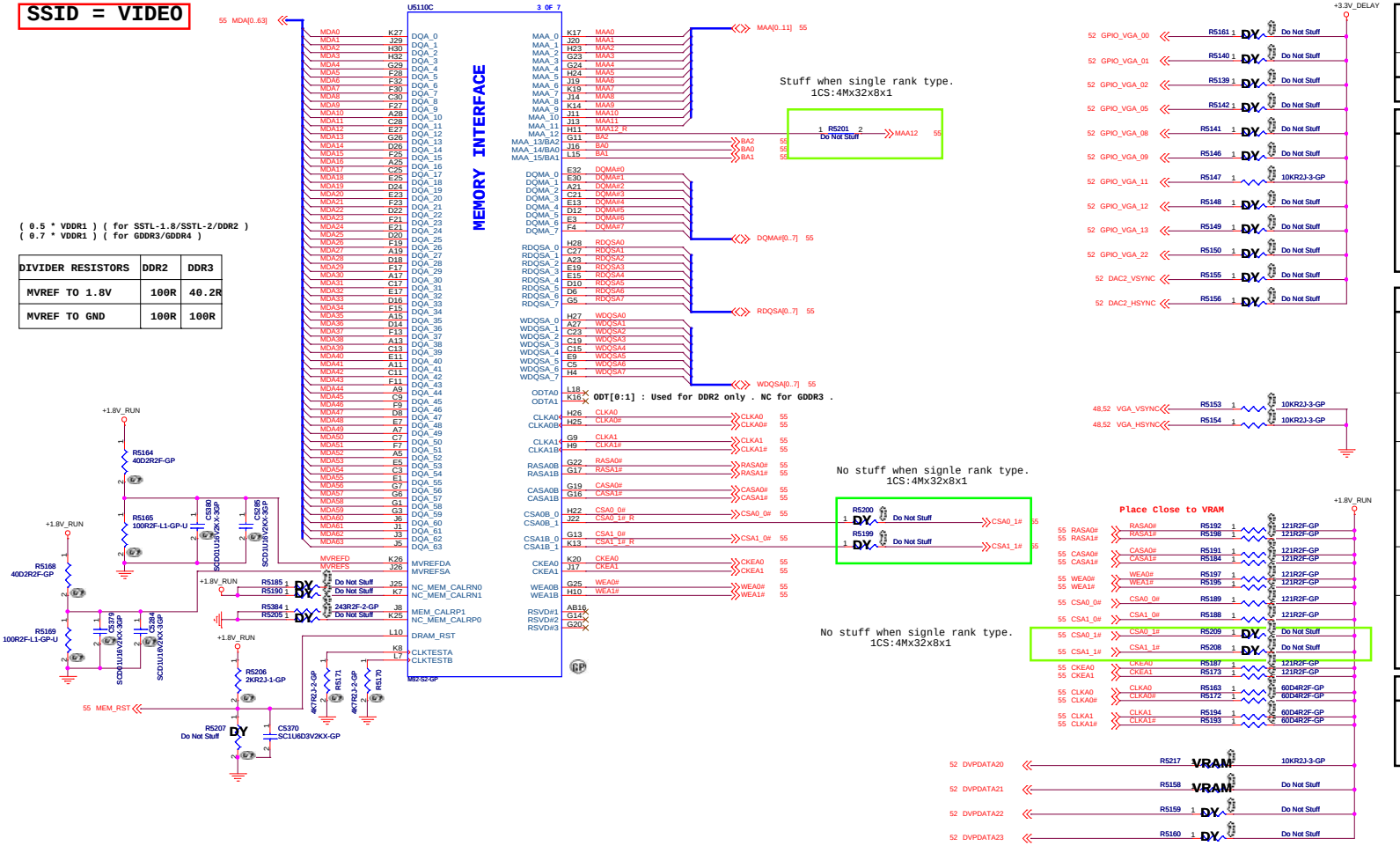


	M92LP Version	
Part	A11	A12
R5401	No stuff	Stuff
Q5106	Stuff	No stuff
R5402	Stuff	No stuff
R5403	No stuff	No stuff
Q5107	Stuff	No stuff
C5384	No stuff	No stuff

SSID = VIDEO

(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO3 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
V 256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Transmitter Power Savings Enable V 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable V 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	V0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	V0= Disable CLKREQ#power management capability 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] V00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(23:20) (Internal PD)	MEMORY TYPE,MAKE AND SIZE INFO 0000 - GDDR3 16Mx32 Qimonda 0001 - GDDR3 32Mx32 Hynix 0010 - GDDR3 32Mx32 Qimonda 0011 - GDDR3 32Mx32 Samsung V

Main Source

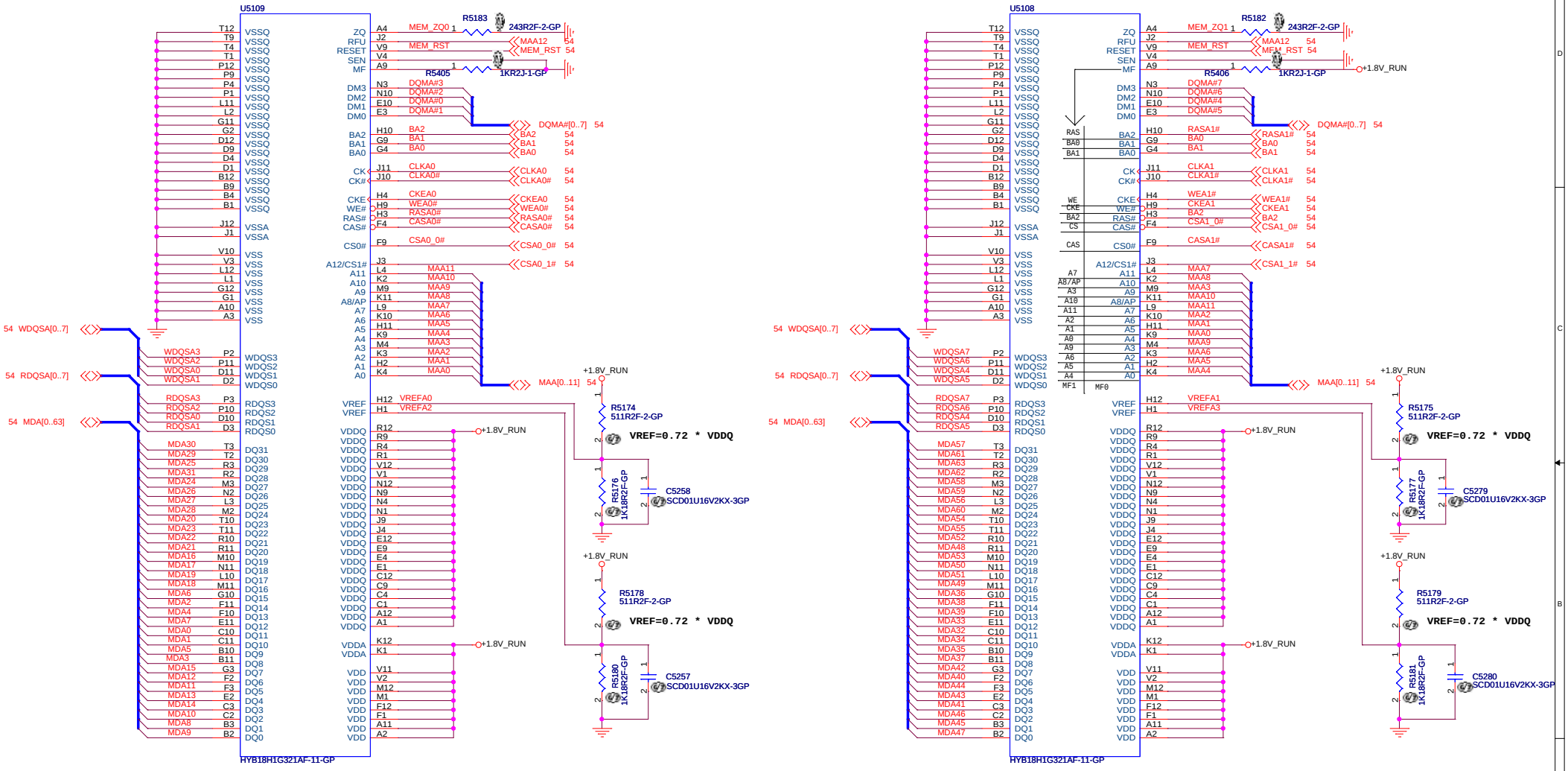
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

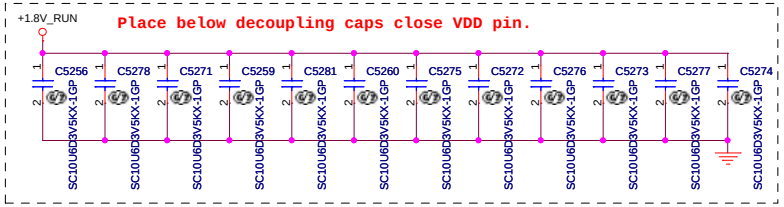
Title: VGA-MEMORY/STRAPS(4/4)

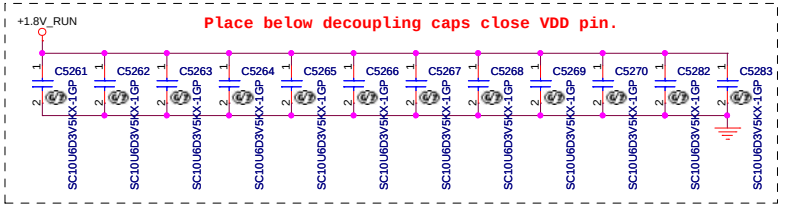
Size: A2 | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 54 of 60

SSID = VIDEO







Main Source

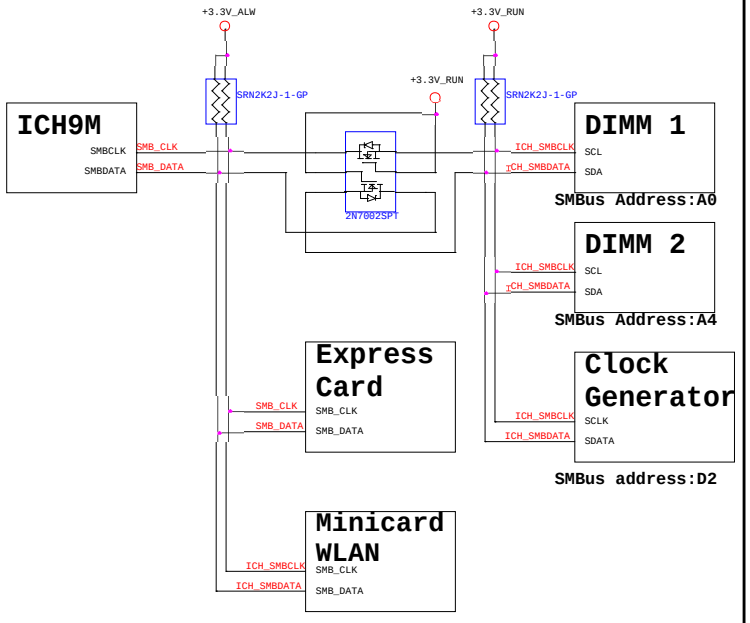
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM**

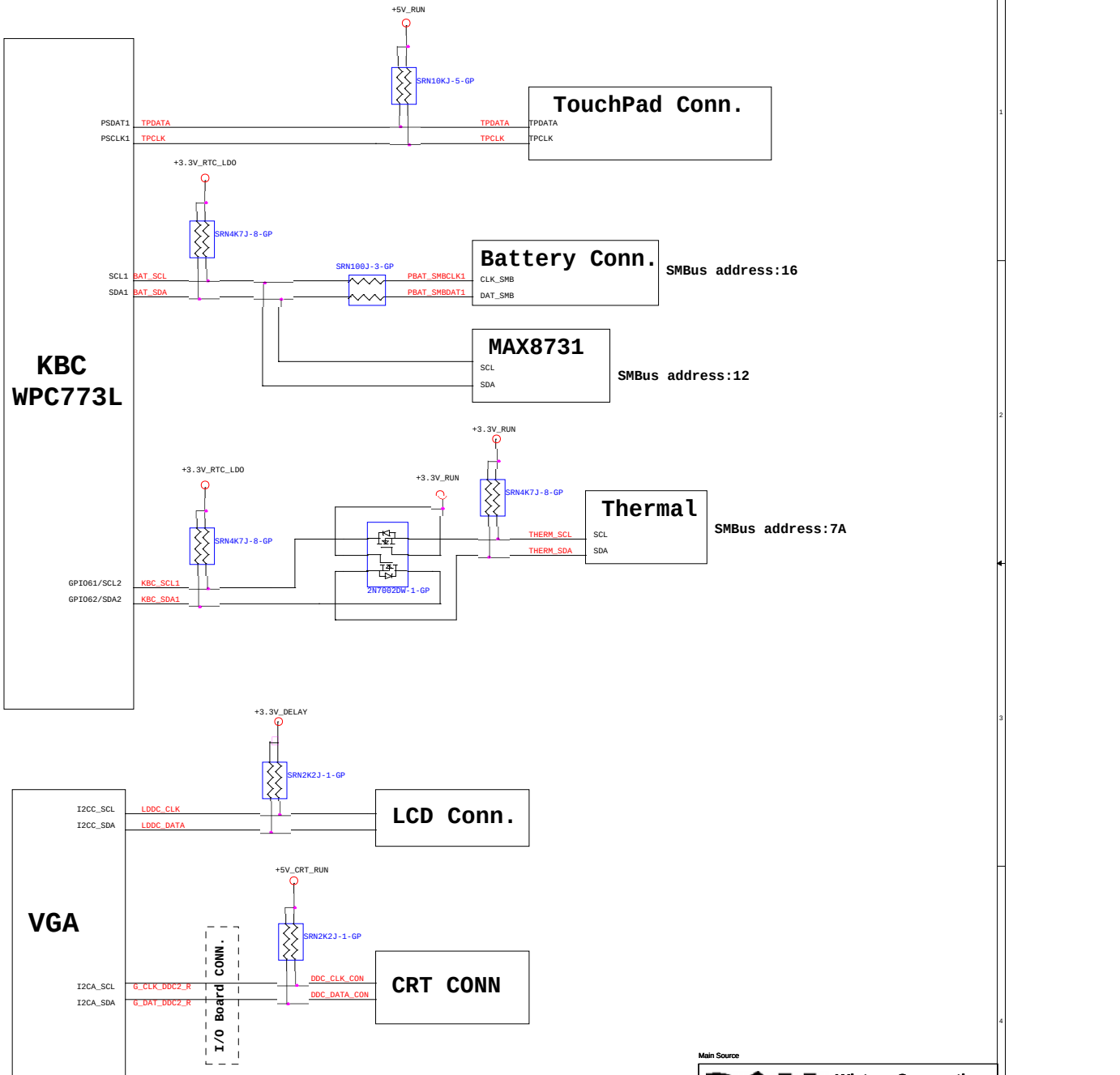
Size: Custom | Document Number: **Roberts Discrete** | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 55 of 60

ICH9M SMBus Block Diagram



KBC SMBus Block Diagram



Main Source

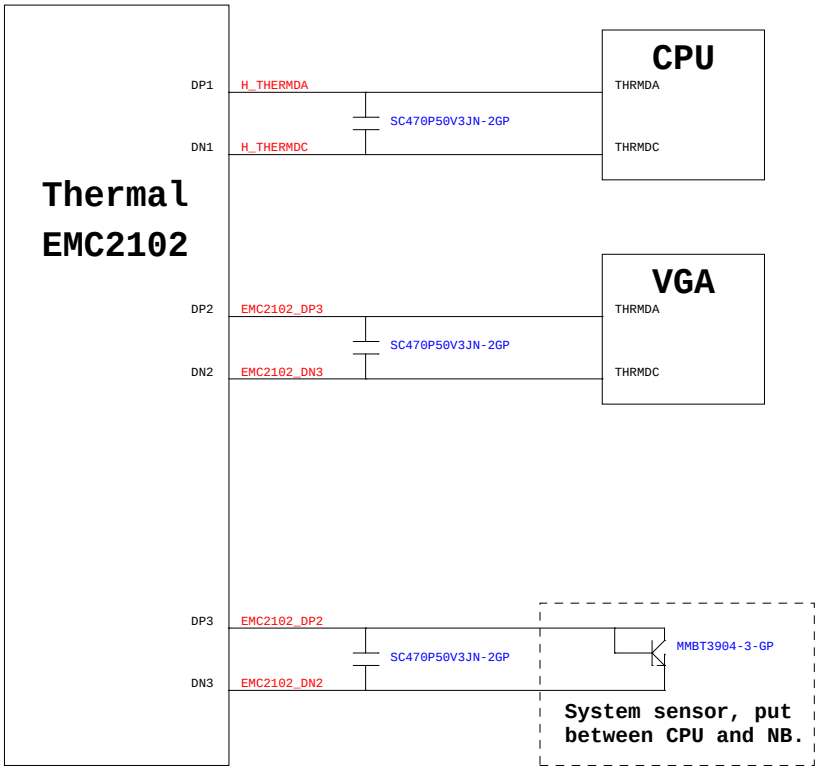
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

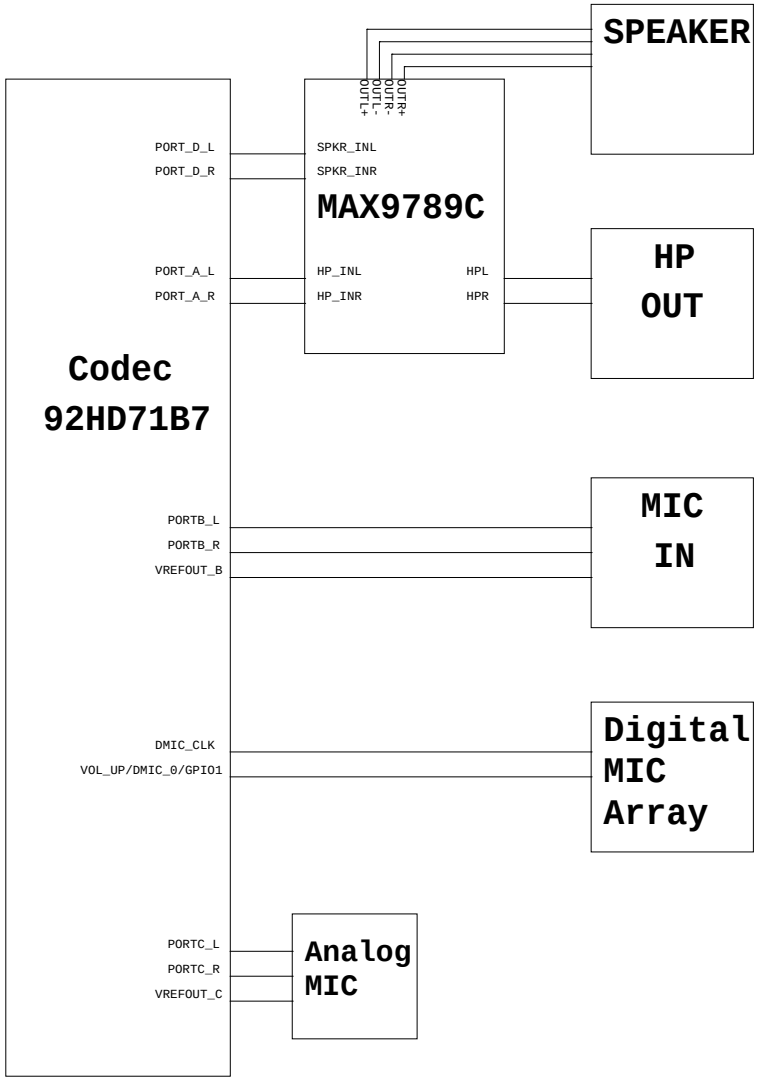
Size	Document Number	Rev
C	Roberts Discrete	-1

Date: Tuesday, May 19, 2009 Sheet 56 of 60

Thermal Block Diagram



Audio Block Diagram



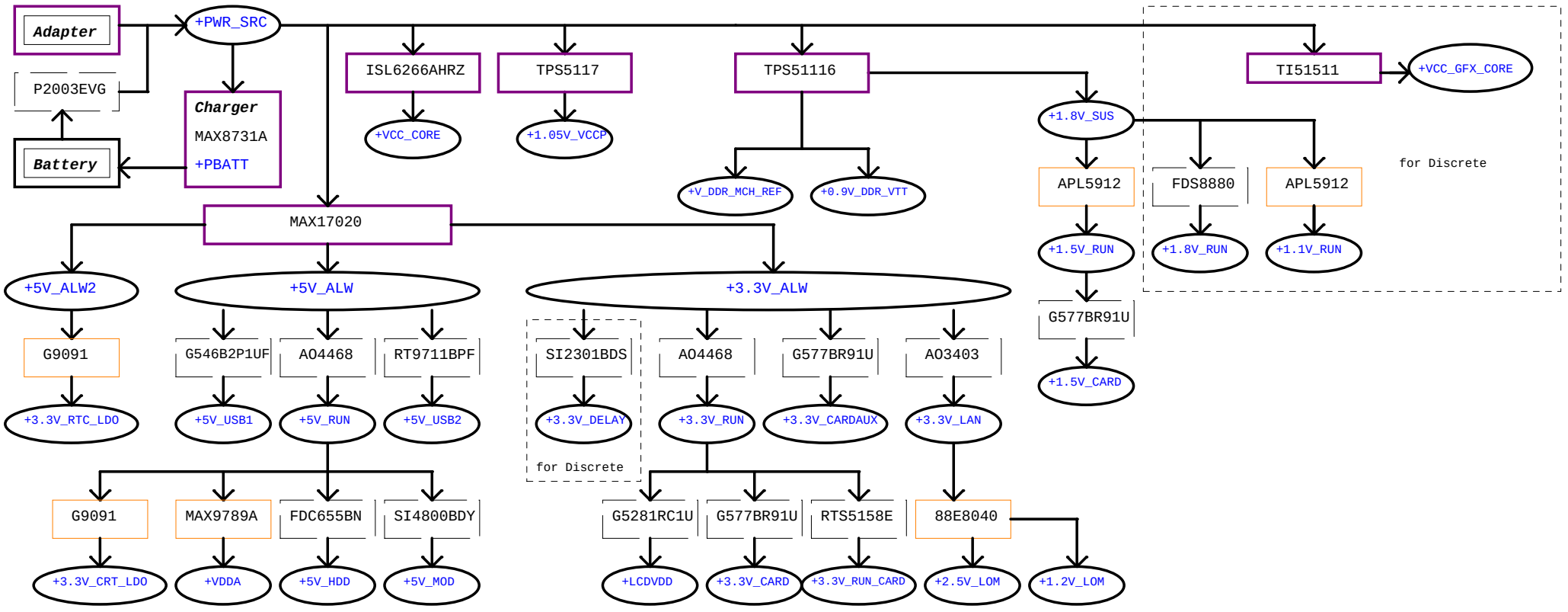
Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 57 of 60



Power Shape

Regulator	LDO	Switch

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
Custom	Roberts Discrete	-1

Date: Tuesday, May 19, 2009 Sheet 58 of 60

DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER
01/09	A00	1	29	Stuff R151, no stuff R150.	Change board ID from X02 to A00.	EE
		2	20	Add R5425.	Add resistor 100k ohm pull low to ground. To solve panel blinking issue.	EE
01/12		3	16	Delete R432, R433.	Delete zero ohm resistors for cost concern.	EE
		4	8,10, 11,16 19,29, 39,41, 43,44, 47	Replace R139, R125, R412, R384, R153, R329, R330, R127, R137, PR1, R351, R453, R5400, R365, R28, R30, R31, R32, RN42, RN43, RN44, RN45, RN48, RN22, RN23, RN54, RN53, RN51 with pads.	Replace zero ohm resistors with pad for cost concern.	EE
01/13		5	44	Change PR9 from pad into 10k ohm resistor. Change C89 from dummy into 0.1u capacitor.	Adding RC circuit.	EE
01/21		6	50	Dummy R3313, Q3301, R3320, C3315, R3327, R3321, R5418, R5419. Add R5431 and D3304. R3305 change to 37.4K ohm.	Changing Power Play voltage control.	EE
		7	34,35	Use 84.27002.L04 for Q13 and Q23.	To prevent components being damaged by high voltages.	EE
01/22		8	41	Change R5413 into zero ohm resistor.		EE
02/02		9	50	Dummy D3304. Undummy R5419.		EE
02/04		11	45	Dummy C67.		EE
		12	29	Add circuit D3305, U5113, R5432, C5390, Q5113, but dummy all. Change R158 to zero ohm resistor.		EE
05/19		1	14 25 17 18 29 30 34 41 44 47 48 52	Change R167 R435 R158 R413 R501 R5412 R5413 PR17 R5212 R5214 R397 R399 R2 R481 R480 R54 R55 R56 R57 to short pad.		EE
		2	52	change circuit R5218 R5219 to short pad		EE
		3	26	change G3330 G3331 gap type		EE
		4	48	add circuit C4501 C4502		EE
		5	31	Change EC78 0.1u to 1u,Change TC12 to 4.7u but DUMMY		EE

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List-EE

Size: Custom | Document Number: Roberts Discrete | Rev: -1

Date: Tuesday, May 19, 2009 | Sheet 59 of 60

DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Change List Power

Size	Document Number	Rev
Custom	***Roberts Discrete***	*-1*

Date: Tuesday, May 19, 2009 Sheet 60 of 60