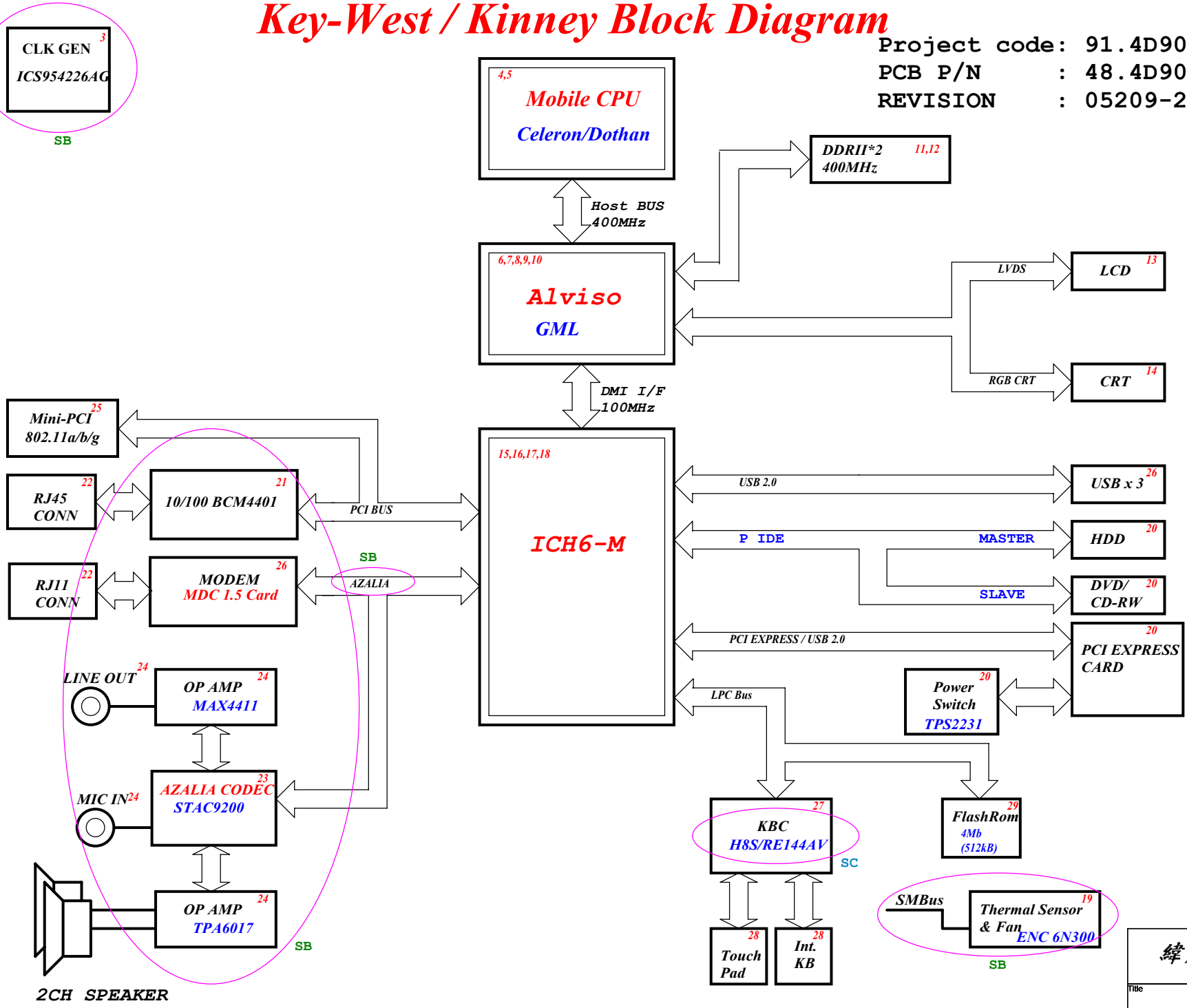
Key-West / Kinney Block Diagram

Project code: 91.4D901.001
PCB P/N : 48.4D901.021
REVISION : 05209-2



SYSTEM DC/DC 33 MAX8734A SB	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S3

SYSTEM DC/DC 34,35 TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 1D8V_S3

MAXIM CHARGER 31 MAX1909	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC 32 MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER

L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: Key-West / Kinney | Rev: -2
Date: Thursday, December 22, 2005 | Sheet 1 of 37

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

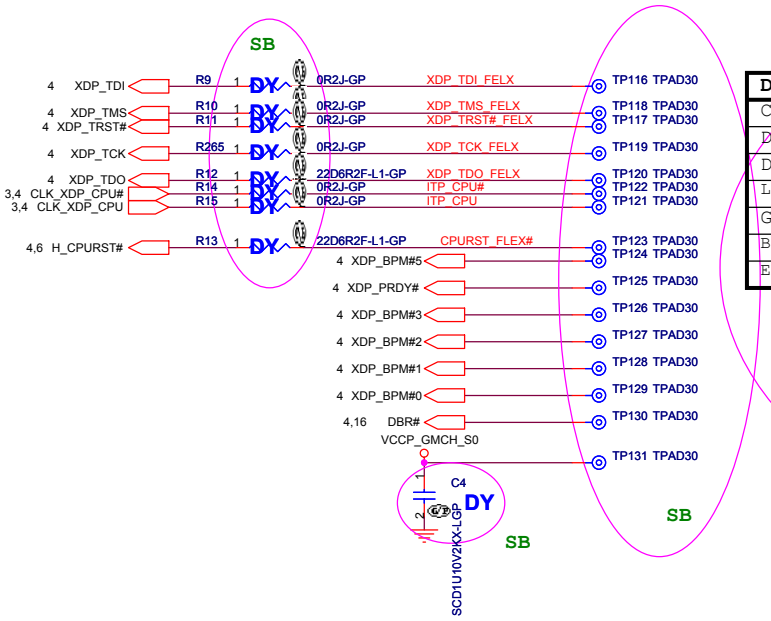
DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

Key-West / Kinney difference

	Key-West	Kenny
	non-Wake on LAN from S5	Wake on LAN from S5
R595	Stuff 1K ohm 0402	Dummy
R132, R573	Stuff 0 ohm 0805	Dummy
R360	Dummy	Stuff 1K ohm 0402
R131	Dummy	Stuff 10K ohm 0402
R368	Dummy	Stuff 100K ohm 0402
R367	Dummy	Stuff 200K ohm 0402
U56	Dummy	Stuff NC7SZ32M5X_NL
C172	Dummy	Stuff 0.01U 16V 0402
C174	Dummy	Stuff 10U 6.3V 0805
C308	Dummy	Stuff 0.047U 25V 0603
Q14	Dummy	Stuff DDTC144EUA-7-F
Q15	Dummy	Stuff FDN338P_NL
U58	Dummy	Stuff SI3456BDV-T1-E3
Q39	Dummy	Stuff 2N7002

-1

10,34,35,36,37 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,15,17,19,32,37 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,37 CORE_GMCH_S0 — CORE_GMCH_S0
12,35,36 0D9V_S0 — 0D9V_S0
7,11,35 DDR_VREF_S3 — DDR_VREF_S3
5,7,9,16,17,20,36,37 1D5V_S0 — 1D5V_S0
17,34,35,36 1D5V_S3 — 1D5V_S3
5 1D5V_VCCA_S0 — 1D5V_VCCA_S0
5,32,36 VCC_CORE_S0 — VCC_CORE_S0
7,9,10,11,12,16,34,35,36,37 1D8V_S3 — 1D8V_S3
7,9,14,17,34,36 2D5V_S0 — 2D5V_S0
9 2D5V_CRTDAC_S0 — 2D5V_CRTDAC_S0
13 3D3V_LCD_S0 — 3D3V_LCD_S0
3,4,5,7,9,11,13,15,16,17,18,19,20,23,24,25,27,29,32,34,36,37 3D3V_S0 — 3D3V_S0
16,17,18,19,20,25,26,33,37 3D3V_S3 — 3D3V_S3
4,13,16,19,27,28,29,30,31,32,33,34,35,36 3D3V_S5 — 3D3V_S5
21,22,36,37 3D3V_LAN_S5 — 3D3V_LAN_S5
33,36 +3V_SRC — +3V_SRC
15,19,28,33,36 +3D3VRTC — +3D3VRTC
15,17 RTC_AUX_S5 — RTC_AUX_S5
23 VDDA — VDDA
13,14,17,18,19,20,24,25,27,28,32,35,36,37 5V_S0 — 5V_S0
13,17,19,23,24,26,33,34,35,36,37 5V_S3 — 5V_S3
13,32,33,34,36 5V_S5 — 5V_S5
14,37 5V_CRT_S0 — 5V_CRT_S0
13,19,33,36,37 +15V — +15V
13,31,33,34,35,36,37 DCBATOUT — DCBATOUT
30,31,37 BT+ — BT+
30,31,37 AD+ — AD+



Device	SMBus addr.
Clock Gen.	D2
DDR Module 1	A0
DDR Module 2	A4
LCD	58
Guardian	5E
Battery	16
EEPROM	A2

USB Port	Key West Define
USBP[0]	USB1 Up connector
USBP[1]	New card used
USBP[2]	USB1 Down connector
USBP[3]	NC
USBP[4]	USB2 connector
USBP[5]	NC
USBP[6]	NC
USBP[7]	NC

PCIE Port	Key West Define
PE[1]	NC
PE[2]	NC
PE[3]	NC
PE[4]	New card used

SB

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD19	P_INTB# / P_INTD#	REQ3#/GNT3#
LAN	AD16	P_INTC#	REQ4#/GNT4#

SB

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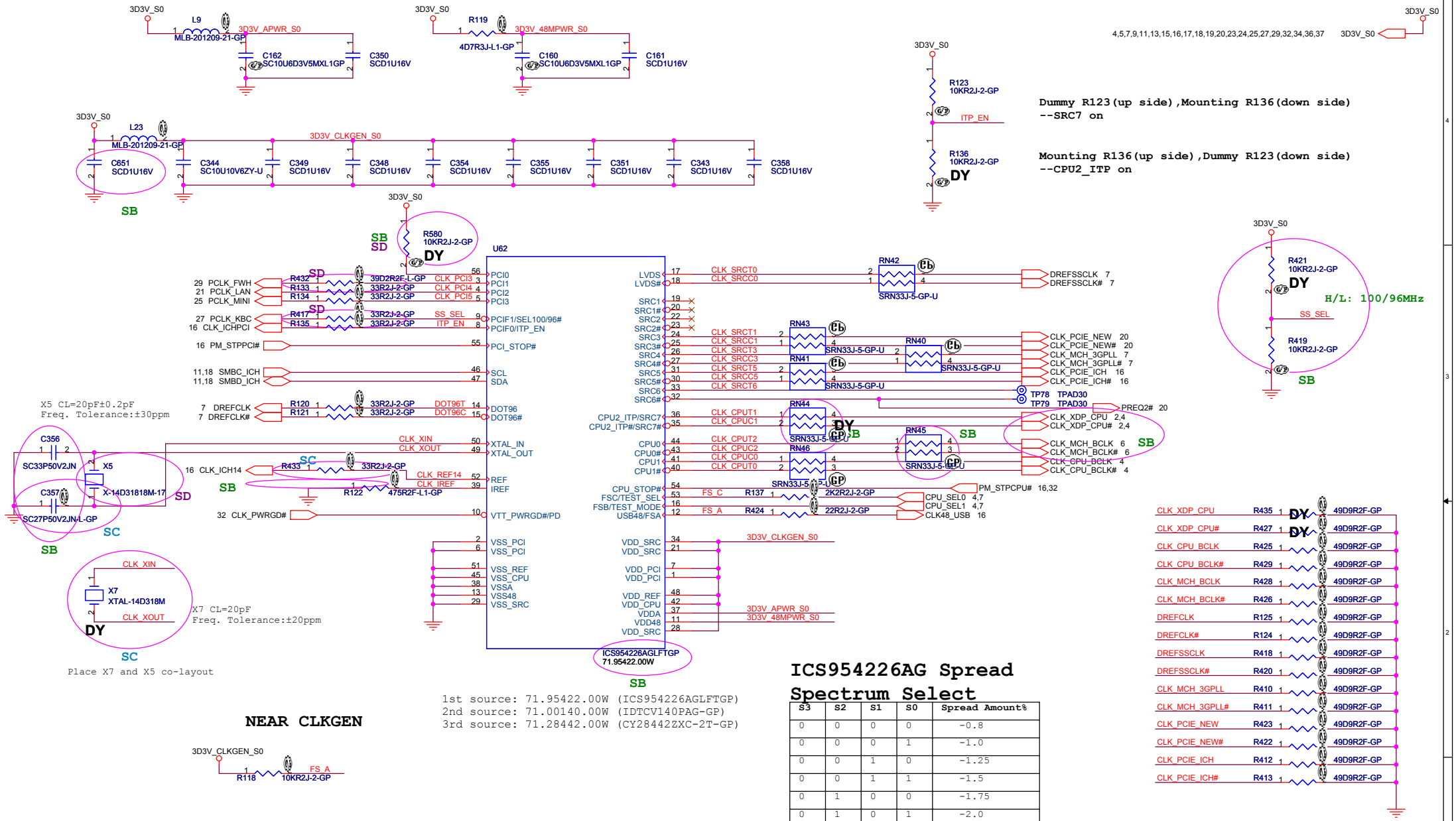
Title: *ITP*

Size: A3 | Document Number: *Key-West / Kinney* | Rev: -2

Date: Friday, December 23, 2005 | Sheet 2 of 37



1st source: 71.95422.00W (ICS954226AGLFTGP)
2nd source: 71.00140.00W (IDTCV140PAG-GP)
3rd source: 71.28442.00W (CY28442ZXC-2T-GP)

NEAR CLKGEN

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

ICS954226AG Spread Spectrum Select

S3	S2	S1	S0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+/-0.3
1	0	0	1	+/-0.4
1	0	1	0	+/-0.5
1	0	1	1	+/-0.6
1	1	0	0	+/-0.8
1	1	0	1	+/-1.0
1	1	1	0	+/-1.25
1	1	1	1	+/-1.5

<Variant Name>

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Title: Clock Generator (ICS954226AG)

Size: A3 | Document Number: Key-West / Kinney | Rev: -2

Date: Friday, December 23, 2005 | Sheet 3 of 37

1st source:62.10079.001
2nd source:62.10053.341

U46A 62.10055.011

U46B 62.10055.011

PZ47903

CPU

ITP Conn.

TCK(PIN A13)

TCK(PIN 5)

FBO(PIN 11)

Only support 400MHz (GML)

SD

SB

DY

All place within 2" to CPU

Place testpoint on H_IERR# with a GND 0.1" away

PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

Layout Note: 0.5" max length.

BSEL[1:0] Freq.(MHz)
L H 100
L L 133

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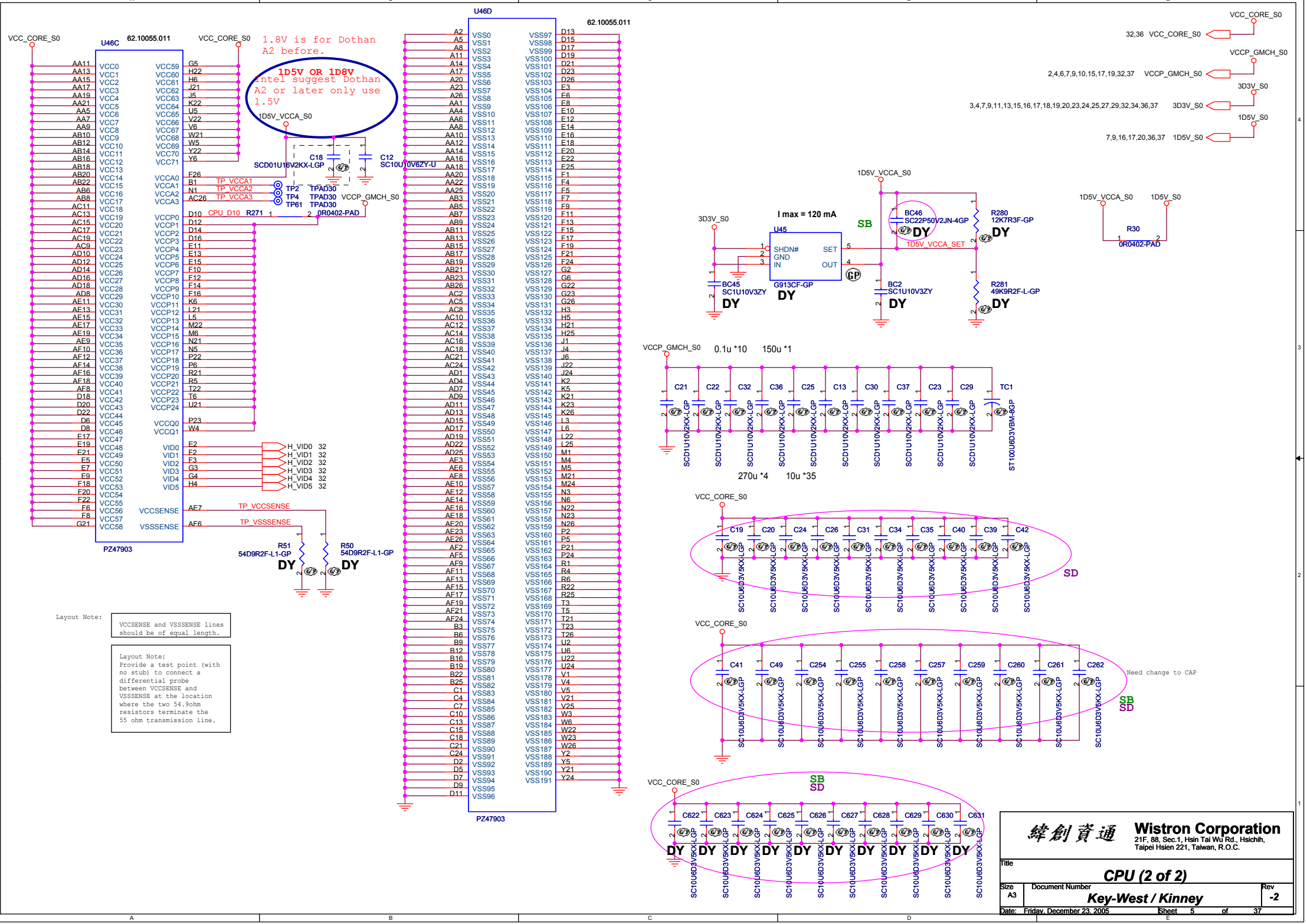
Title: CPU (1 of 2)

Size: A3 | Document Number: Key-West / Kinney | Rev: -2

Date: Friday, December 23, 2005 | Sheet 4 of 37


U46C
62.10055.011
PZ47903
VCC_CORE_S0
1.8V is for Dothan A2 before.
1D5V OR 1D8V
Intel suggest Dothan A2 or later only use 1.5V
1D5V_VCCA_S0
SCD01U16V2KX-LGP
C18
C12
SC10U10V6ZY-U
TP_VCCA1
TP_VCCA2
TP_VCCA3
TP2
TP4
TP61
TPAD30
0R0402-PAD
VCCP_GMCH_S0
CPU_D10
R271
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
TP_VCCSENSE
TP_VSSSENSE
R51
R50
54D9R2F-L1-GP
DY
U46D
62.10055.011
PZ47903
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
32,36 VCC_CORE_S0
2,4,6,7,9,10,15,17,19,32,37 VCCP_GMCH_S0
3,4,7,9,11,13,15,16,17,18,19,20,23,24,25,27,29,32,34,36,37 3D3V_S0
7,9,16,17,20,36,37 1D5V_S0
3D3V_S0
I max = 120 mA
U45
SHDN#
GND
IN
SET
OUT
G913CF-GP
BC45
SC1U10V3ZY
BC46
SC22P50V2JN-4GP
SB
1D5V_VCCA_SET
BC2
R280
12K7R3F-GP
R281
49K9R2F-L-GP
R30
0R0402-PAD
VCCP_GMCH_S0
0.1u *10
150u *1
270u *4
10u *35
SCD1U10V2KX-LGP
ST100U6D3VBM-8GP
SC10U6D3V5KX-LGP
SD
SC10U6D3V5KX-LGP
Need change to CAP
SB
SD
SC10U6D3V5KX-LGP
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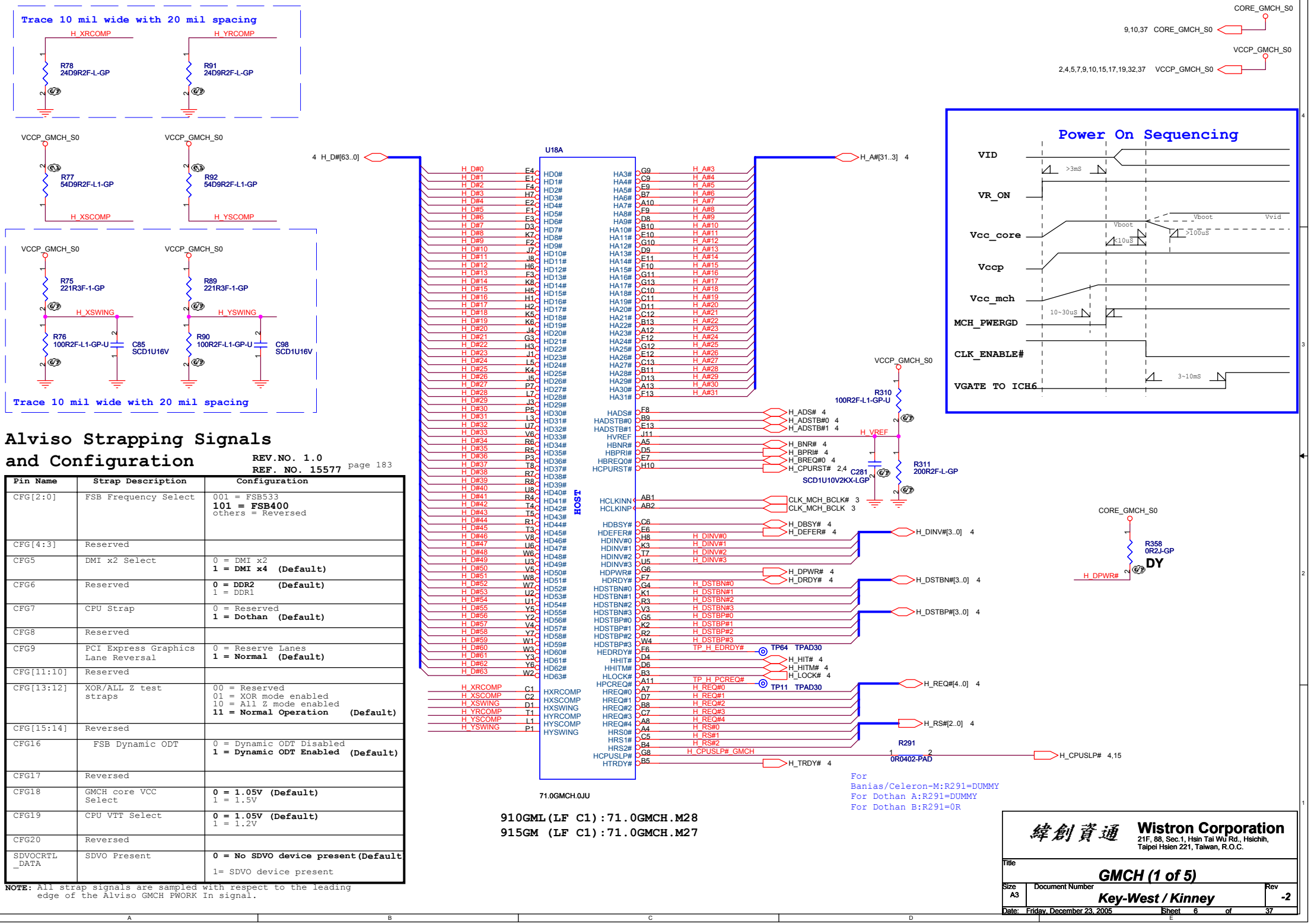
Title
CPU (2 of 2)
Size
A3
Document Number
Key-West / Kinney
Rev
-2
Date: Friday, December 23, 2005
Sheet 5 of 37



Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 **101 = FSB400** others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	Reserved	**0 = DDR2 (Default)** 1 = DDR1
CFG7	CPU Strap	0 = Reserved **1 = Dothan (Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes **1 = Normal (Default)**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation (Default)**
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V (Default)** 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V (Default)** 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present (Default** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

910GML(LF C1):71.0GMCH.M28
915GM (LF C1):71.0GMCH.M27

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Title: **GMCH (1 of 5)**
Size: A3 | Document Number: **Key-West / Kinney** | Rev: -2
Date: Friday, December 23, 2005 | Sheet 6 of 37

3,4,5,9,11,13,15,16,17,18,19,20,23,24,25,27,29,32,34,36,37 3D3V_S0 → 3D3V_S0
9,14,17,34,36 2D5V_S0 → 2D5V_S0
9,10,11,12,16,34,35,36,37 1D8V_S3 → 1D8V_S0
5,9,16,17,20,36,37 1D5V_S0 → 1D5V_S0
2,4,5,6,9,10,15,17,19,32,37 VCCP_GMCH_S0 → VCCP_GMCH_S0
11,35 DDR_VREF_S3 → DDR_VREF_S3

Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die

Intel suggest NC Due to votusly DVO

U18B

DMI: DMIRXN0 DMIRXN1 DMIRXN2 DMIRXN3 DMIRXP0 DMIRXP1 DMIRXP2 DMIRXP3 DMITXN0 DMITXN1 DMITXN2 DMITXN3 DMITXP0 DMITXP1 DMITXP2 DMITXP3
CRG/RSVD: CFG0–CFG20, RSVD21–RSVD27
DDR MUXING: SM_CK0 SM_CK1 SM_CK2 SM_CK3 SM_CK4 SM_CK5 SM_CK0# SM_CK1# SM_CK2# SM_CK3# SM_CK4# SM_CK5# SM_CKE0 SM_CKE1 SM_CKE2 SM_CKE3 SM_CS0# SM_CS1# SM_CS2# SM_CS3# SM_OCDCOMP0 SM_OCDCOMP1 SM_ODT0 SM_ODT1 SM_ODT2 SM_ODT3 SMRCOMPN SMRCOMPP SMVREF0 SMVREF1 SMXSLEWIN SMXSLEWOUT SMYSLEWIN SMYSLEWOUT
PM: BM_BUSY# EXT_TS0# EXT_TS1# THRMTRIP# PWROK RSTIN#
CLK: DREF_CLKN DREF_CLKP DREF_SSCLKN DREF_SSCLKP
NC: NC#AP37 NC#AN37 NC#AP36 NC#AP2 NC#AP1 NC#AN1 NC#B1 NC#A2 NC#B37 NC#A36 NC#A37

U18G

MISC: SDVOCTRL_DATA SDVOCTRL_CLK GCLKN GCLKP
TV: TVDAC_A TVDAC_B TVDAC_C TV_REFSET TV_IRTNA TV_IRTNB TV_IRTNC
VGA: DDCCLK DDCDATA BLUE BLUE# GREEN GREEN# RED RED# VSYNC HSYNC REFSET
LVDS: LBKLT_CRTL LBKLT_EN LCTLA_CLK LCTLB_DATA LDDC_CLK LDDC_DATA LVDD_EN LIBG LVBG LVREFH LVREFL LACLKN LACLKP LBCLKN LBCLKP LADATAN0 LADATAN1 LADATAN2 LADATAP0 LADATAP1 LADATAP2 LBDATAN0 LBDATAN1 LBDATAN2 LBDATAP0 LBDATAP1 LBDATAP2
PCI-EXPRESS GRAPHICS: EXP_RXN0–EXP_RXN15 EXP_RXP0–EXP_RXP15 EXP_TXN0–EXP_TXN15 EXP_TXP0–EXP_TXP15

SB
SC
DY
NO STUFF

Layout Note: Route as short as possible

Trace impendance 50ohm Less than 0.5", trace impendance 37.5ohm

When Low 2.2K Ohm
When High 1K Ohm

FOR DDR2
For Dothan-B

CFG(2..1) FREQ.(MHz)
10 400
00 533
11 Reserved

CPU_SEL0=0 (R67) :133MHZ
CPU_SEL0=1 (R66) :100MHZ

Ref ALVISO EDS-1 Page 115

71.0GMCH.0JU

Strapping

CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors

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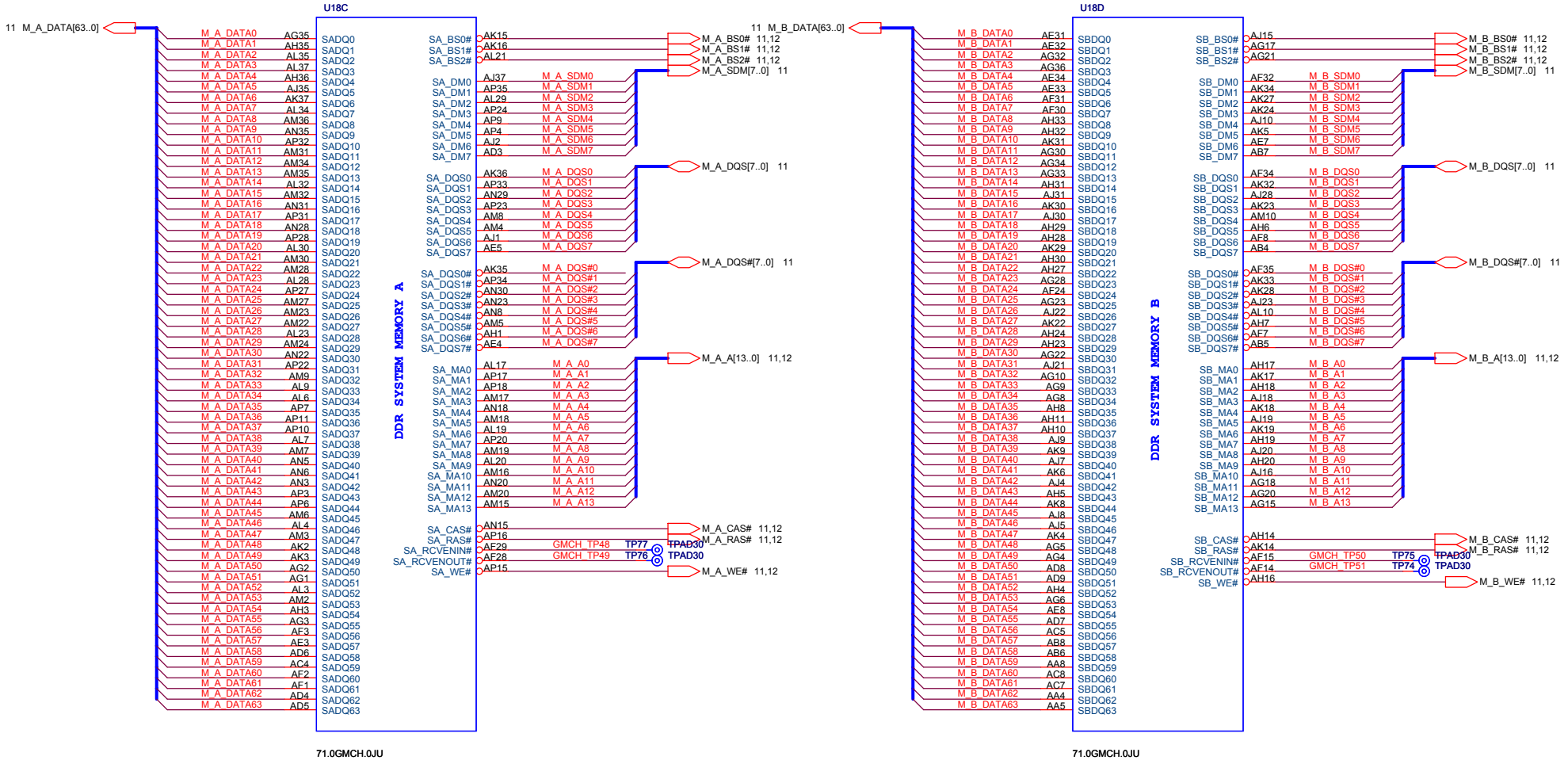
Title: GMCH (2 of 5)
Size: A3 | Document Number: Key-West / Kinney | Rev: -2
Date: Friday, December 23, 2005 | Sheet 7 of 37

SUPPORT DDRII 400



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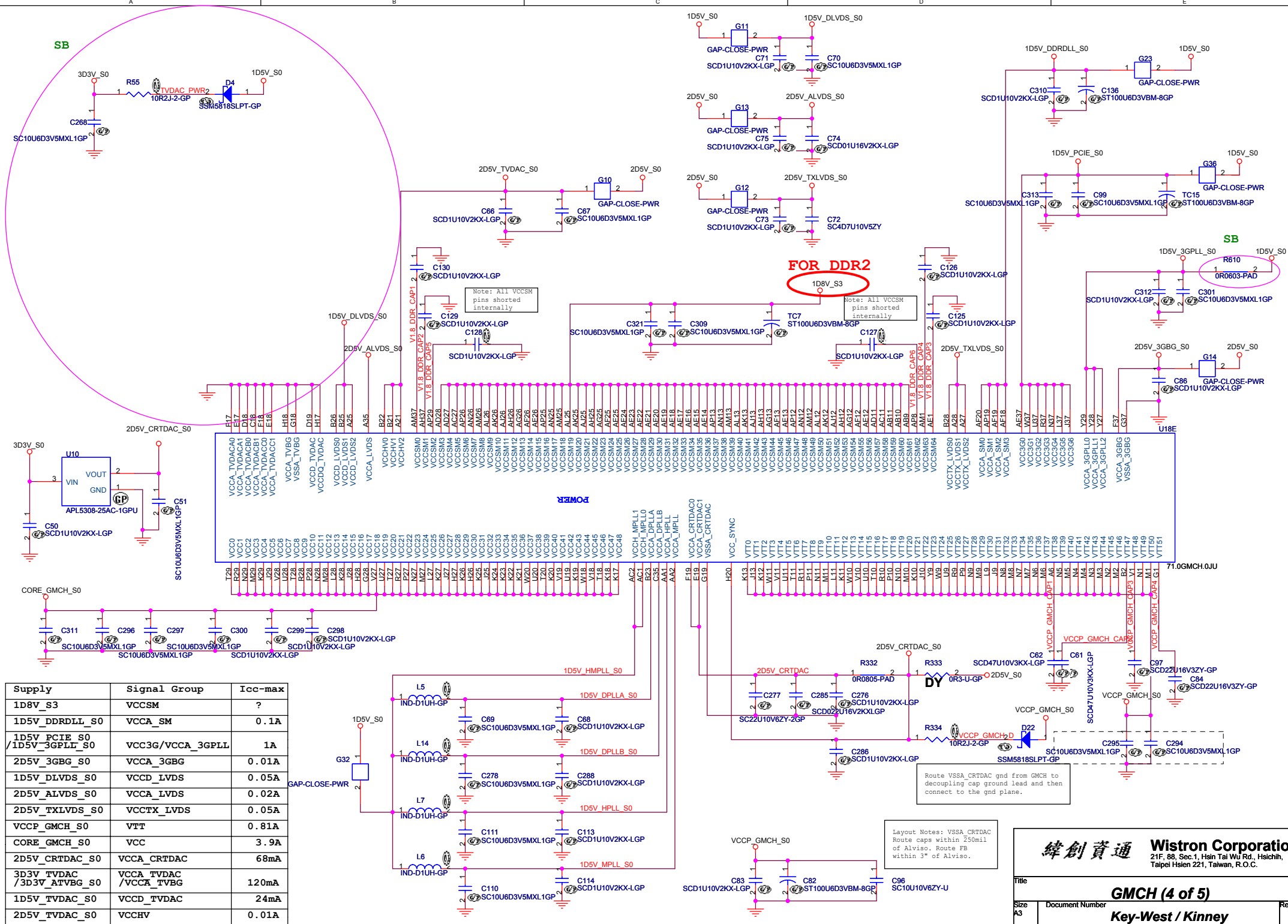
Title: GMCH (3 of 5)

Size: A3 | Document Number: Key-West / Kinney | Rev: -2

Date: Friday, December 23, 2005 | Sheet 8 of 37



Supply	Signal Group	Icc-max
1D8V_S3	VCCSM	?
1D5V_DDRDLL_S0	VCCA_SM	0.1A
1D5V_PCIE_S0 /1D5V_3GPLL_S0	VCC3G/VCCA_3GPLL	1A
2D5V_3GBG_S0	VCCA_3GBG	0.01A
1D5V_DLVDS_S0	VCCD_LVDS	0.05A
2D5V_ALVDS_S0	VCCA_LVDS	0.02A
2D5V_TXLVDS_S0	VCCTX_LVDS	0.05A
VCCP_GMCH_S0	VTT	0.81A
CORE_GMCH_S0	VCC	3.9A
2D5V_CRTDAC_S0	VCCA_CRTDAC	68mA
3D3V_TVDAC /3D3V_ATVBG_S0	VCCA_TVDAC /VCCA_TVBG	120mA
1D5V_TVDAC_S0	VCCD_TVDAC	24mA
2D5V_TVDAC_S0	VCCHV	0.01A

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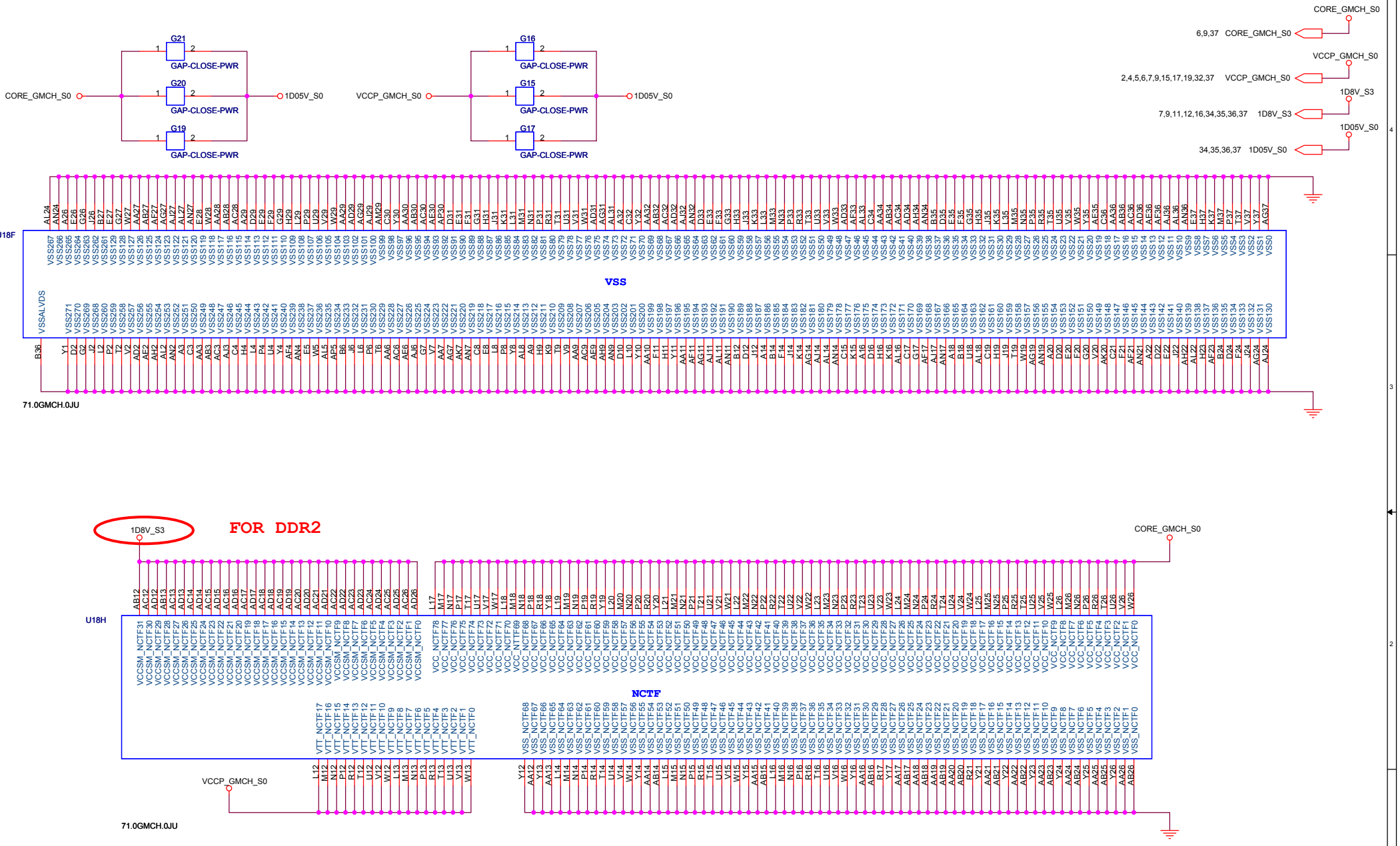
Title: GMCH (4 of 5)

Size: A3 | Document Number: Key-West / Kinney | Rev: -2

Date: Thursday, December 22, 2005 | Sheet 9 of 37



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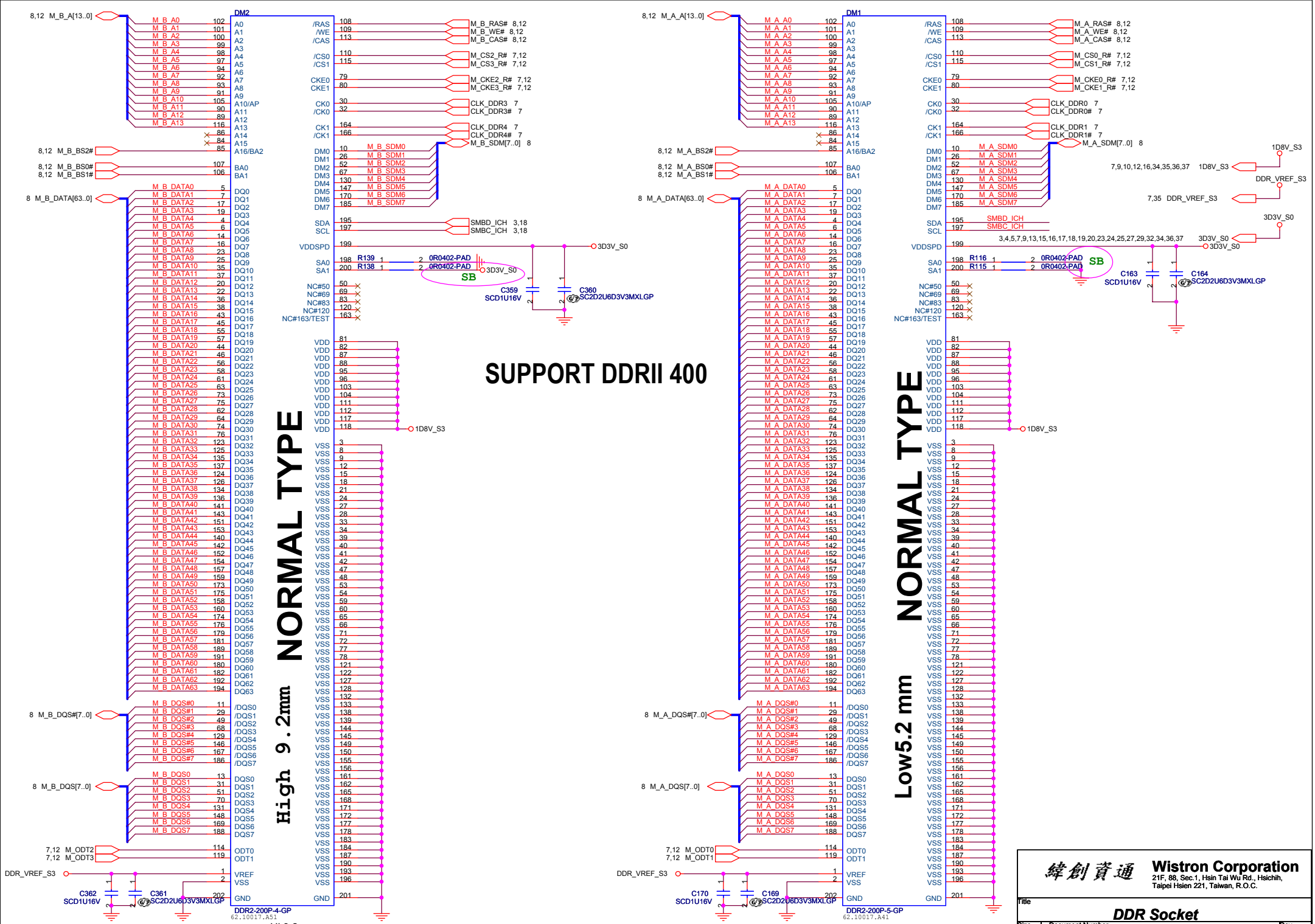
Title: **GMCH (5 of 5)**

Size	Document Number	Rev
A3	**Key-West / Kinney**	-2

Date: Friday, December 23, 2005 Sheet 10 of 37



Hi 9.2 mm

1st source:62.10017.A51
2nd source:62.10017.A61

1st source:62.10017.A41
2nd source:62.10017.B01

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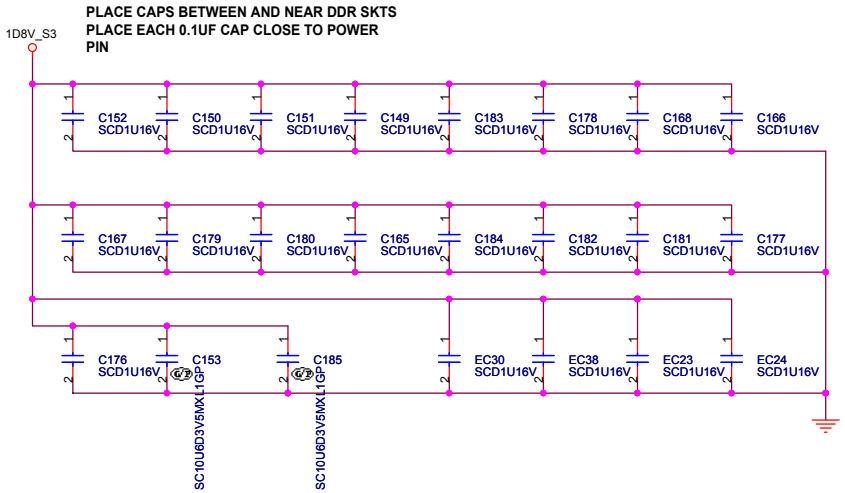
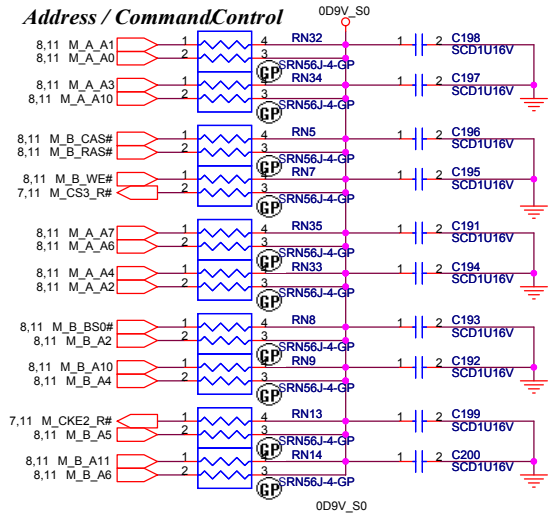
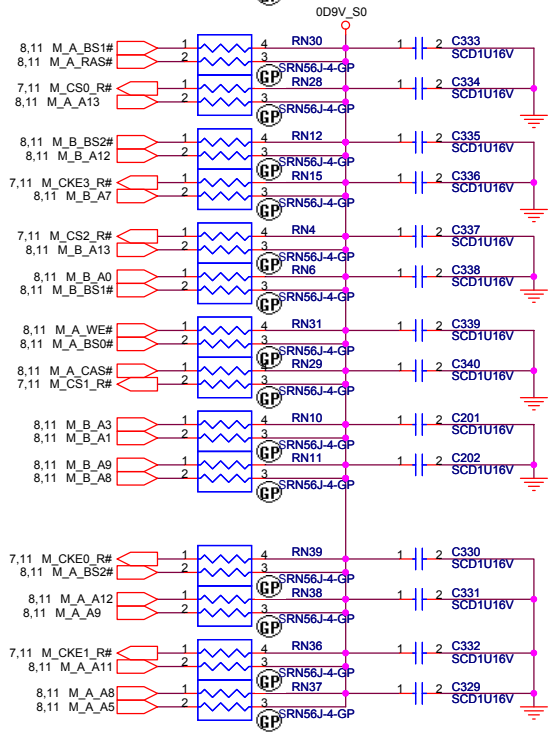
Title: **DDR Socket**

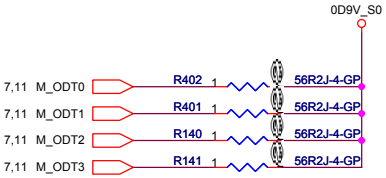
Size	Document Number	Rev
Custom	Key-West / Kinney	-2

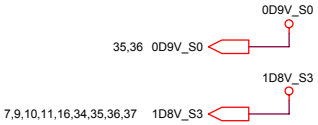
Date: Friday, December 23, 2005 Sheet 11 of 37











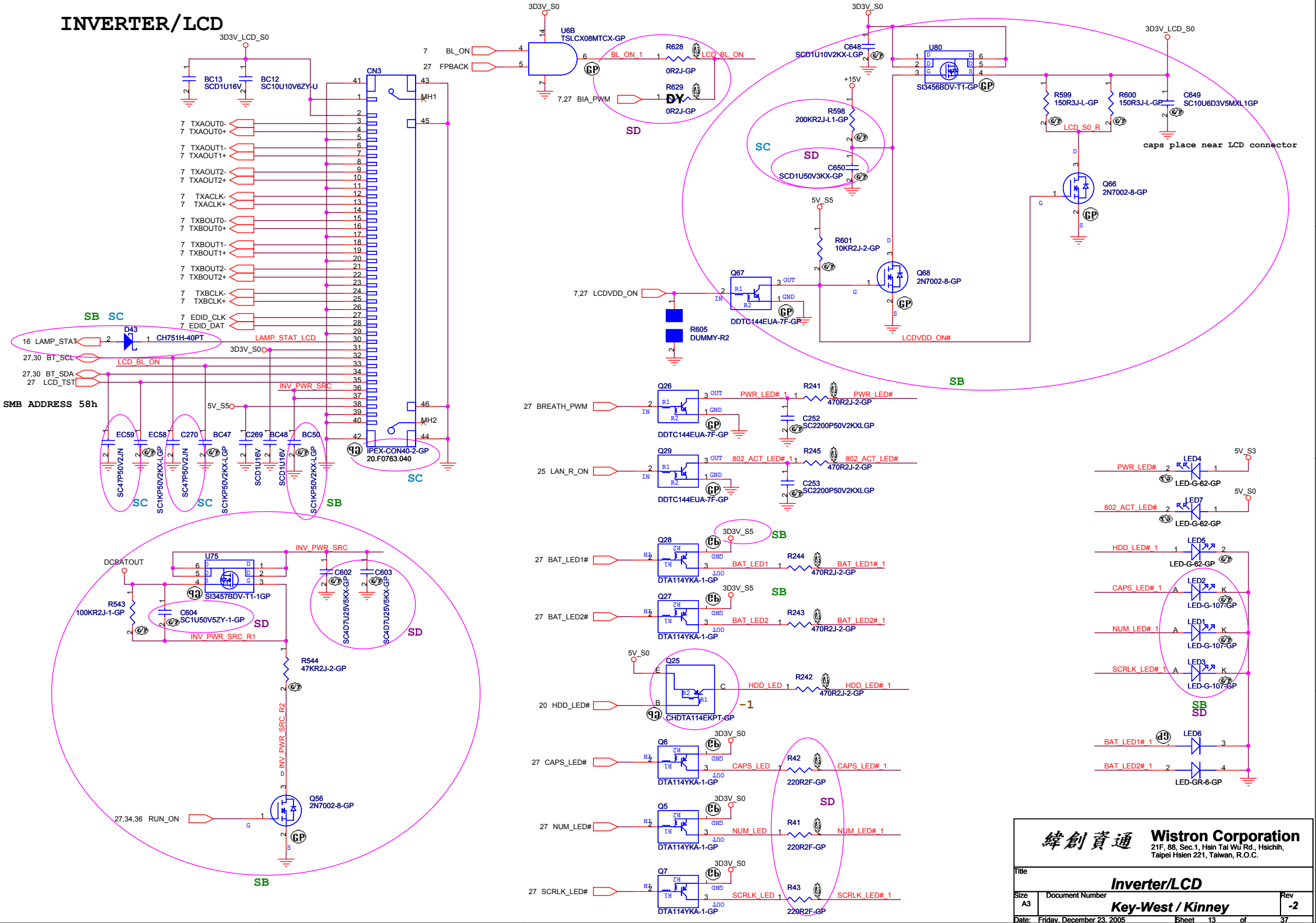
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR Serial/Terminator Resistor***

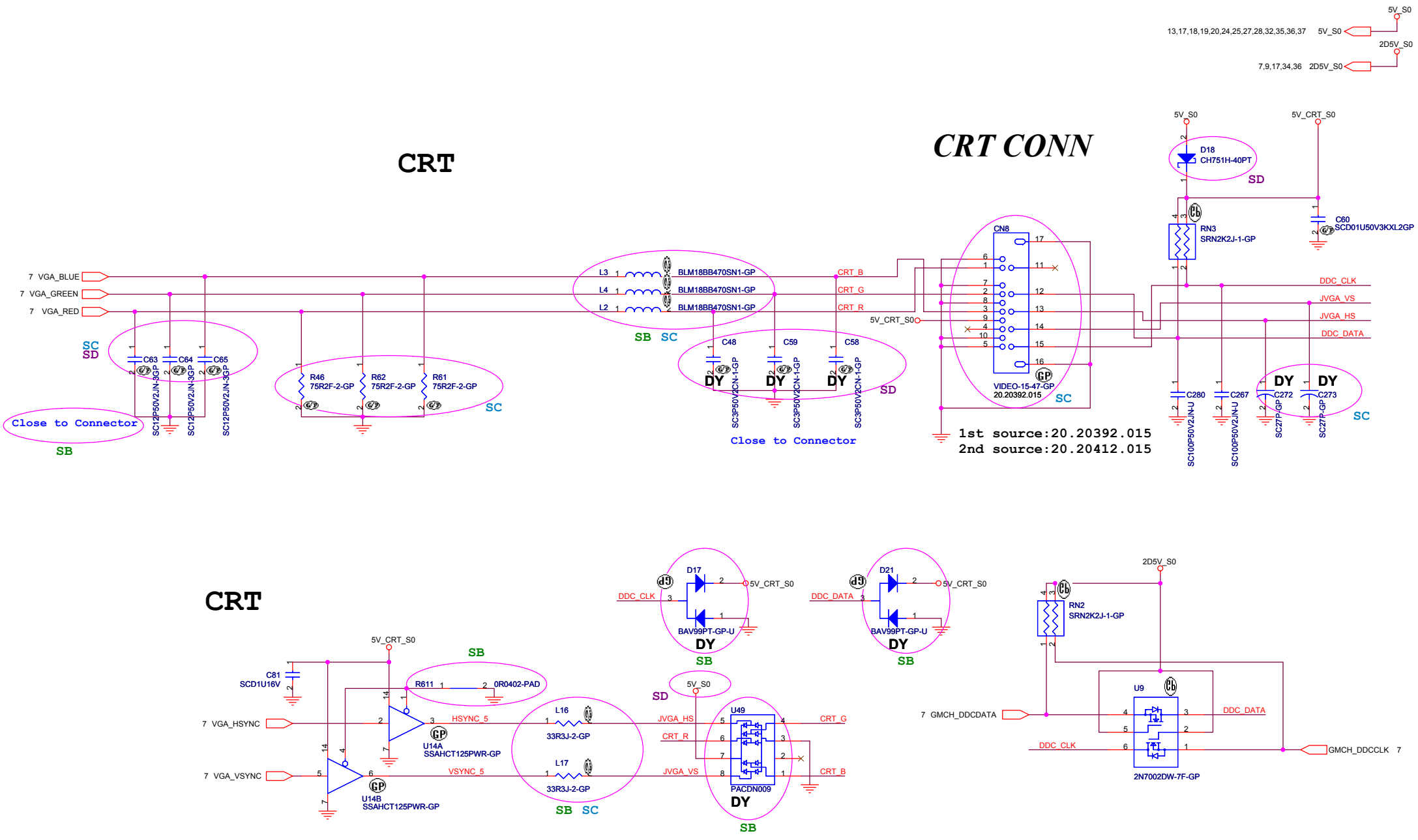
Size	Document Number	Rev
A3	***Key-West / Kinney***	-2

Date: Friday, December 23, 2005 Sheet 12 of 37

INVERTER/LCD



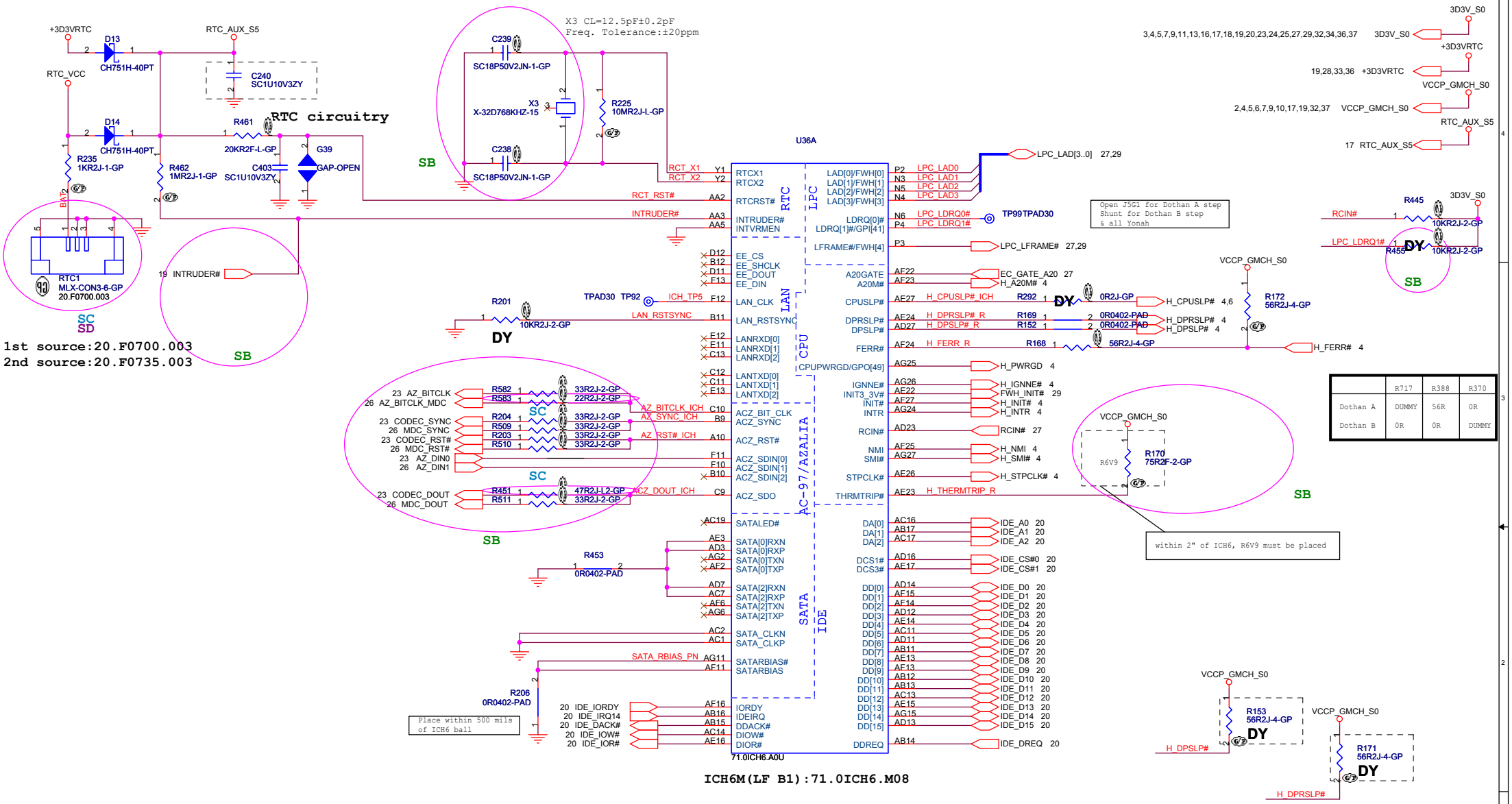
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***Inverter/LCD***		
Size A3	Document Number ***Key-West / Kinney***	Rev -2	
Date: Friday, December 23, 2005	Sheet 13 of 37		



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT	
Size A3	Document Number Key-West / Kinney	Rev -2
Date: Friday, December 23, 2005	Sheet 14 of 37	



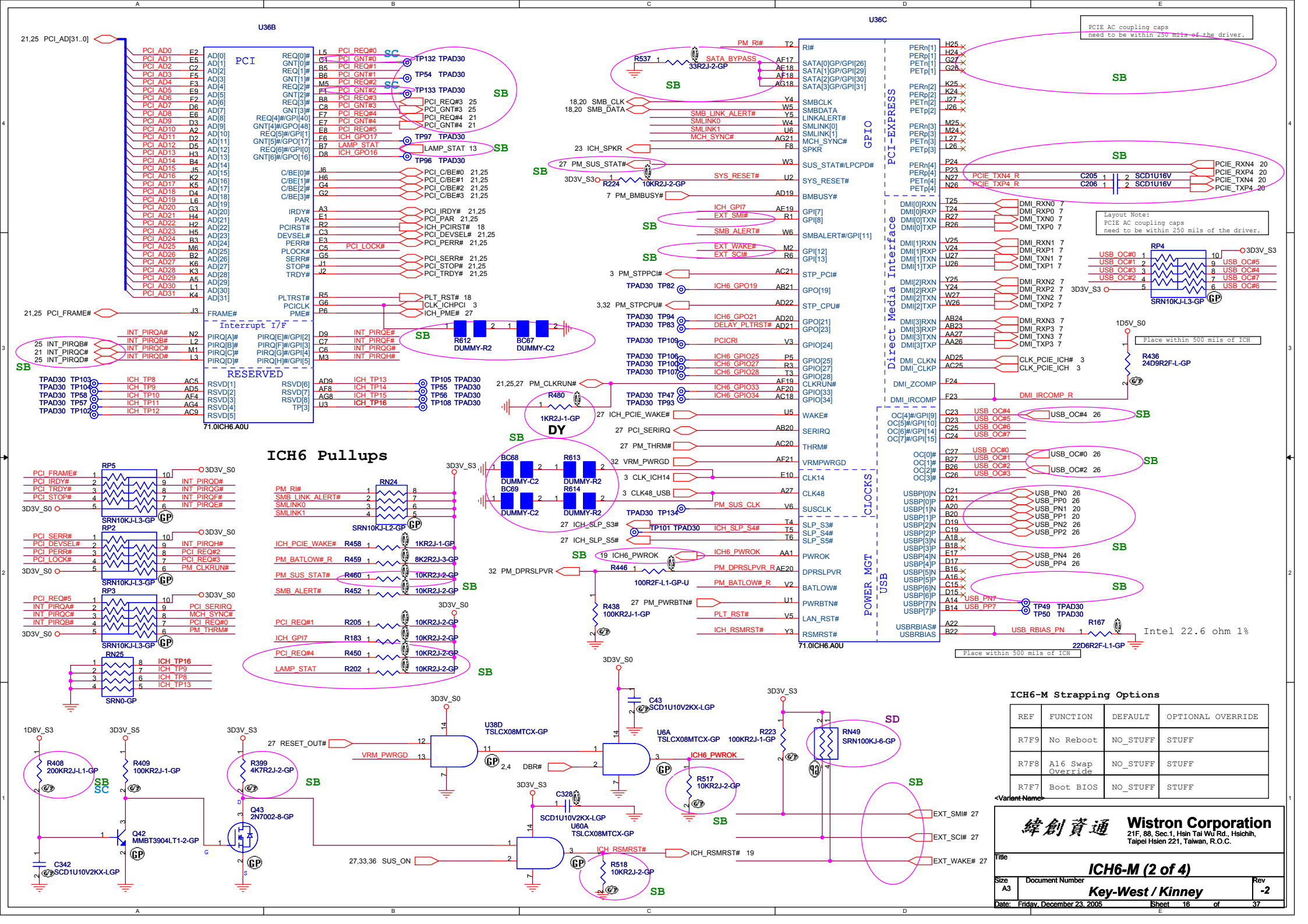
	R717	R388	R370
Dothan A	DUMMY	56R	0R
Dothan B	0R	0R	DUMMY

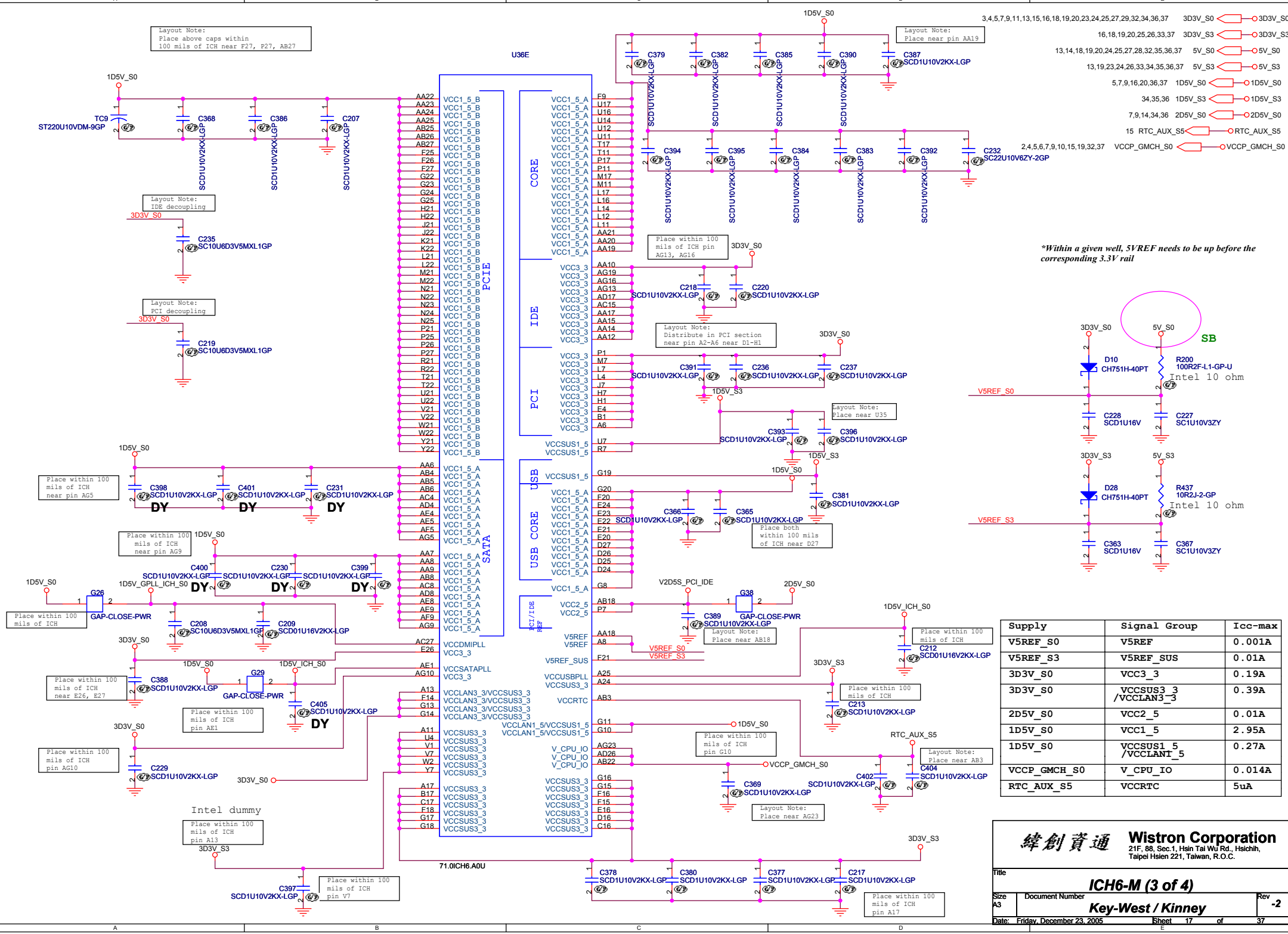
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH6-M (1 of 4)**

Size	Document Number	Rev
A3	Key-West / Kinney	-2

Date: Friday, December 23, 2005 Sheet 15 of 37


U36B
U36C
PCI
Interrupt I/F
RESERVED
Direct Media Interface
PCI-EXPRESS
GPIO
CLOCKS
USB
POWER_MGT
71.0ICH6.A0U
ICH6 Pullups
SB
SC
SD
DY
PCIE AC coupling caps need to be within 250 mils of the driver.
Layout Note: PCIE AC coupling caps need to be within 250 mils of the driver.
Place within 500 mils of ICH
Intel 22.6 ohm 1%
ICH6-M Strapping Options
REF | FUNCTION | DEFAULT | OPTIONAL OVERRIDE
R7F9 | No Reboot | NO_STUFF | STUFF
R7F8 | A16 Swap Override | NO_STUFF | STUFF
R7F7 | Boot BIOS | NO_STUFF | STUFF
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (2 of 4)
Size A3
Document Number
Key-West / Kinney
Rev -2
Date: Friday, December 23, 2005
Sheet 16 of 37



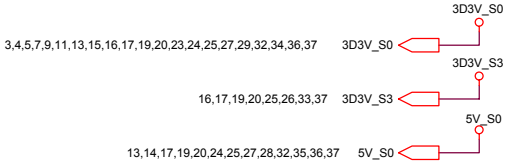
Supply	Signal Group	Icc-max
V5REF_S0	V5REF	0.001A
V5REF_S3	V5REF_SUS	0.01A
3D3V_S0	VCC3_3	0.19A
3D3V_S0	VCCSUS3_3 /VCCLAN3_3	0.39A
2D5V_S0	VCC2_5	0.01A
1D5V_S0	VCC1_5	2.95A
1D5V_S0	VCCSUS1_5 /VCCLANI_5	0.27A
VCCP_GMCH_S0	V_CPU_IO	0.014A
RTC_AUX_S5	VCCRTC	5uA

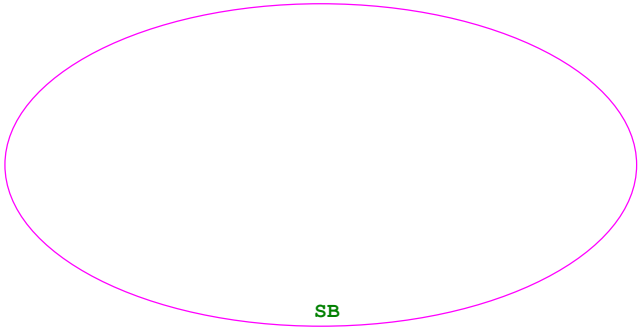
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

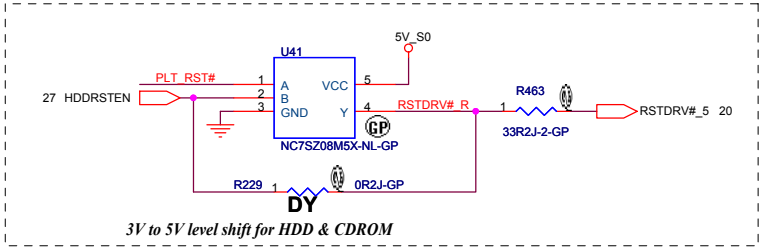
Title: **ICH6-M (3 of 4)**

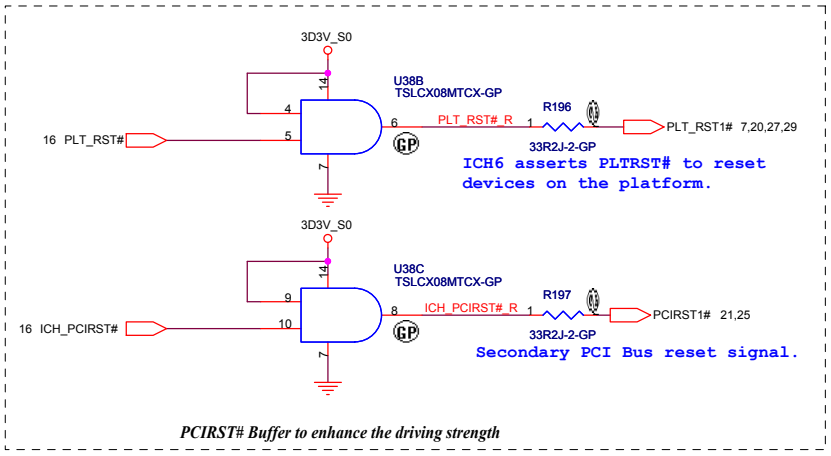
Size	Document Number	Rev
A3	Key-West / Kinney	-2

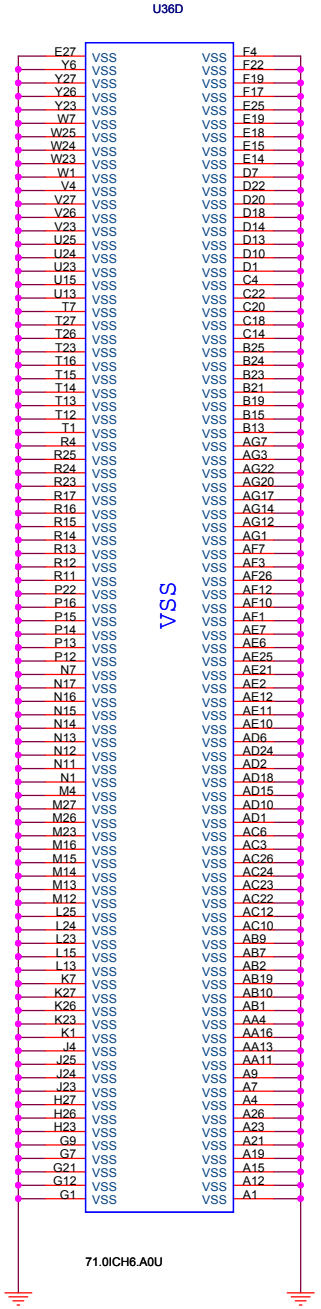
Date: Friday, December 23, 2005 Sheet 17 of 37



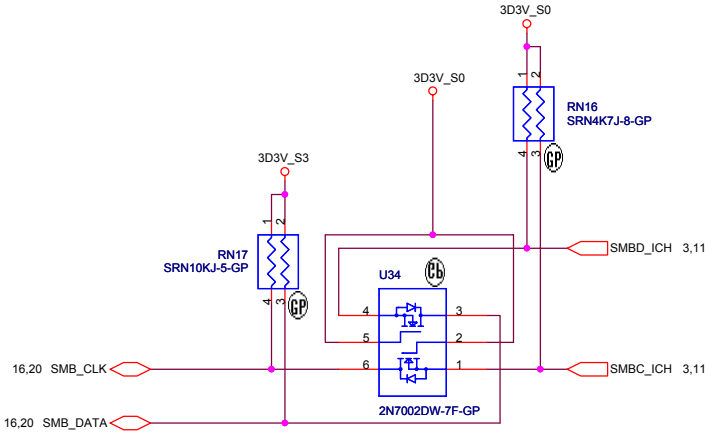




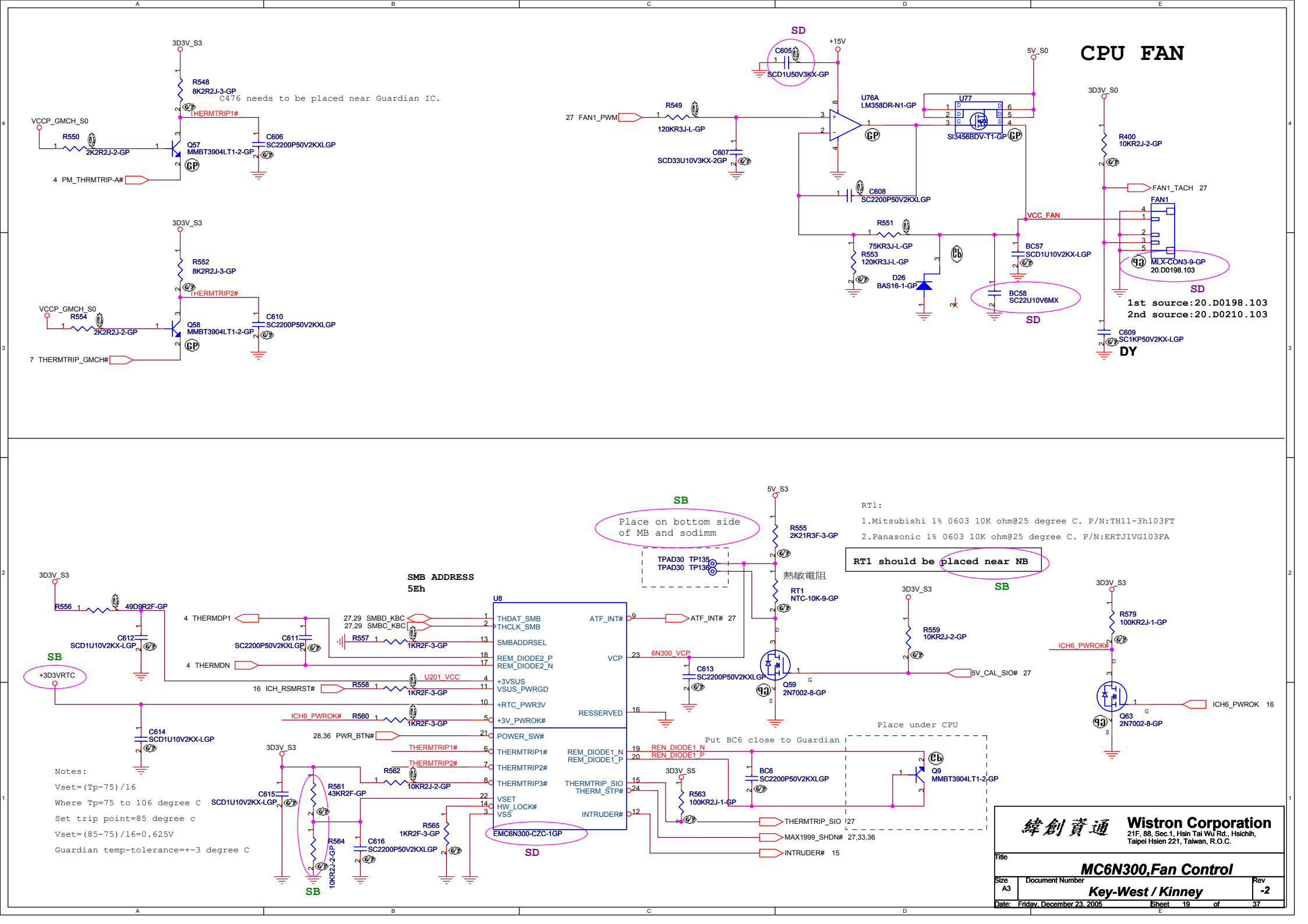




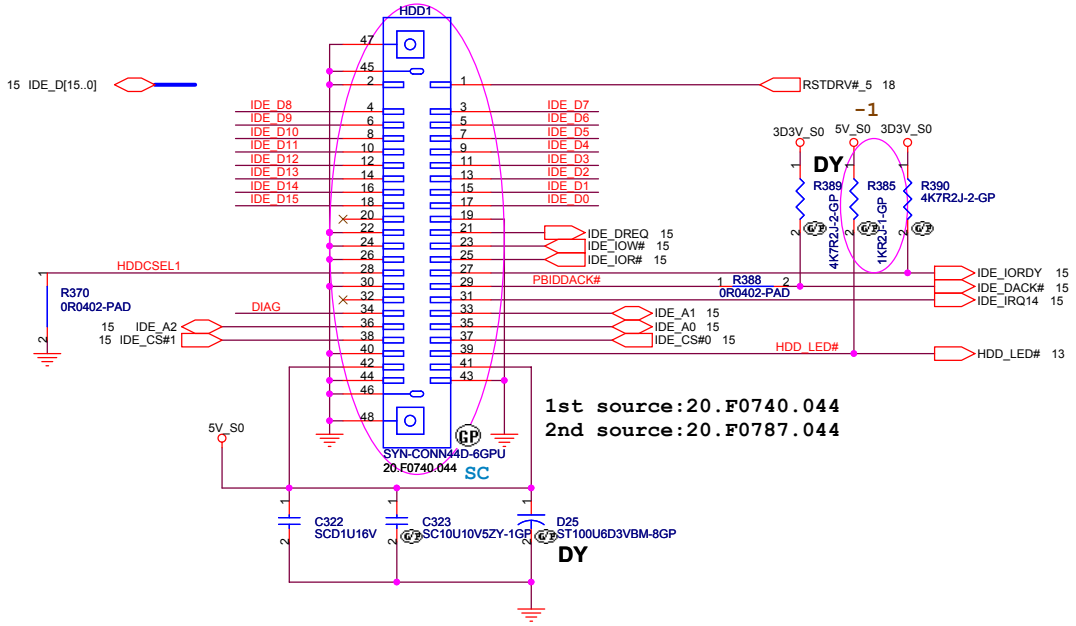
SMBUS(ICH6 ---> SODIMM,CLKGEN)



Wistron Corporation 緯創資通	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ICH6-M (4 of 4)		
Size: A3	Document Number: Key-West / Kinney	Rev: -2
Date: Friday, December 23, 2005	Sheet 18 of 37	

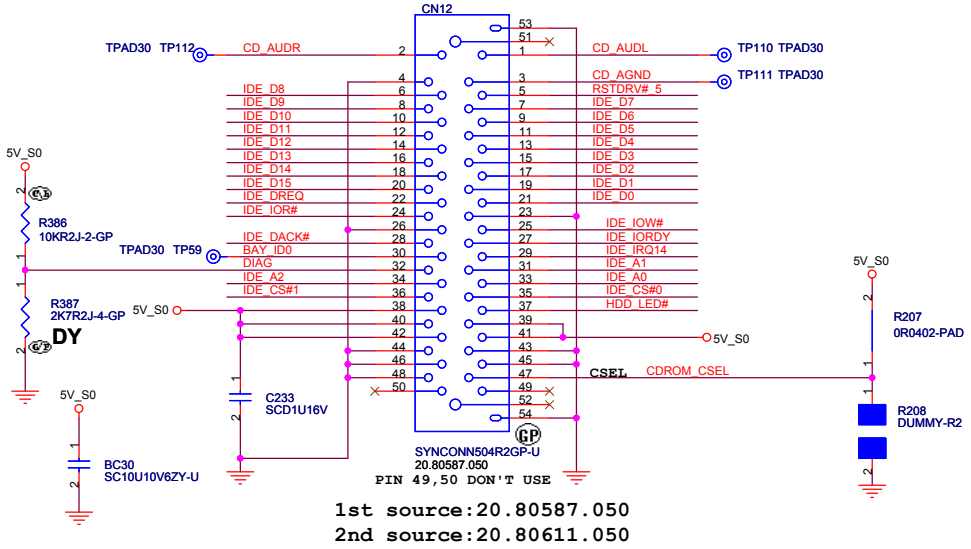

CPU FAN
C476 needs to be placed near Guardian IC.
3D3V_S3
R548 8K2R2J-3-GP
THERMTRIP1#
VCCP_GMCH_S0
R550 2K2R2J-2-GP
Q57 MMBT3904LT1-2-GP
C606 SC2200P50V2KXLGP
4 PM_THRMTRIP-A#
R552 8K2R2J-3-GP
THERMTRIP2#
R554 2K2R2J-2-GP
Q58 MMBT3904LT1-2-GP
C610 SC2200P50V2KXLGP
7 THERMTRIP_GMCH#
SD
C605 SCD1U50V3KX-GP
+15V
5V_S0
27 FAN1_PWM
R549 120KR3J-L-GP
C607 SCD33U10V3KX-2GP
U76A LM358DR-N1-GP
U77 SI3456BDV-T1-GP
C608 SC2200P50V2KXLGP
R551 75KR3J-L-GP
R553 120KR3J-L-GP
D26 BAS16-1-GP
VCC_FAN
BC57 SCD1U10V2KX-LGP
BC58 SC22U10V6MX
SD
3D3V_S0
R400 10KR2J-2-GP
FAN1_TACH 27
FAN1
MLX-CON3-9-GP 20.D0198.103
SD
1st source:20.D0198.103
2nd source:20.D0210.103
C609 SC1KP50V2KX-LGP
DY
SB
Place on bottom side of MB and sodimm
TPAD30 TP135
TPAD30 TP136
5V_S3
R555 2K21R3F-3-GP
熱敏電阻
RT1 NTC-10K-9-GP
RT1:
1.Mitsubishi 1% 0603 10K ohm@25 degree C. P/N:TH11-3h103FT
2.Panasonic 1% 0603 10K ohm@25 degree C. P/N:ERTJ1VG103FA
RT1 should be placed near NB
SB
3D3V_S3
R559 10KR2J-2-GP
5V_CAL_SIO# 27
Q59 2N7002-8-GP
3D3V_S3
R579 100KR2J-1-GP
ICH6_PWROK#
ICH6_PWROK 16
Q63 2N7002-8-GP
SMB ADDRESS
5Eh
U8
3D3V_S3
R556 49D9R2F-GP
C612 SCD1U10V2KX-LGP
SB
+3D3VRTC
C614 SCD1U10V2KX-LGP
4 THERMDP1
4 THERMDN
C611 SC2200P50V2KXLGP
27,29 SMBD_KBC
27,29 SMBC_KBC
R557 1KR2F-3-GP
16 ICH_RSMRST#
R558 1KR2F-3-GP
U201_VCC
ICH6_PWROK#
R560 1KR2F-3-GP
28,36 PWR_BTN#
THDAT_SMB
THCLK_SMB
SMBADDRSEL
REM_DIODE2_P
REM_DIODE2_N
+3VSUS
VSUS_PWRGD
+RTC_PWR3V
+3V_PWROK#
POWER_SW#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
VSET
HW_LOCK#
VSS
EMC6N300-CZC-1GP
SD
ATF_INT#
VCP
RESSERVED
REM_DIODE1_N
REM_DIODE1_P
THERMTRIP_SIO
THERM_STP#
INTRUDER#
ATF_INT# 27
6N300_VCP
C613 SC2200P50V2KXLGP
Put BC6 close to Guardian
Place under CPU
REN_DIODE1_N
REN_DIODE1_P
3D3V_S5
R563 100KR2J-1-GP
BC6 SC2200P50V2KXLGP
Q9 MMBT3904LT1-2-GP
THERMTRIP_SIO 27
MAX1999_SHDN# 27,33,36
INTRUDER# 15
3D3V_S3
C615 SCD1U10V2KX-LGP
R561 43KR2F-GP
R562 10KR2J-2-GP
R564 10KR2J-2-GP
C616 SC2200P50V2KXLGP
R565 1KR2F-3-GP
SB
Notes:
Vset=(Tp-75)/16
Where Tp=75 to 106 degree C
Set trip point=85 degree c
Vset=(85-75)/16=0.625V
Guardian temp-tolerance=+-3 degree C
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MC6N300,Fan Control
Size A3
Document Number
Key-West / Kinney
Rev -2
Date: Friday, December 23, 2005
Sheet 19 of 37

HDD Connector

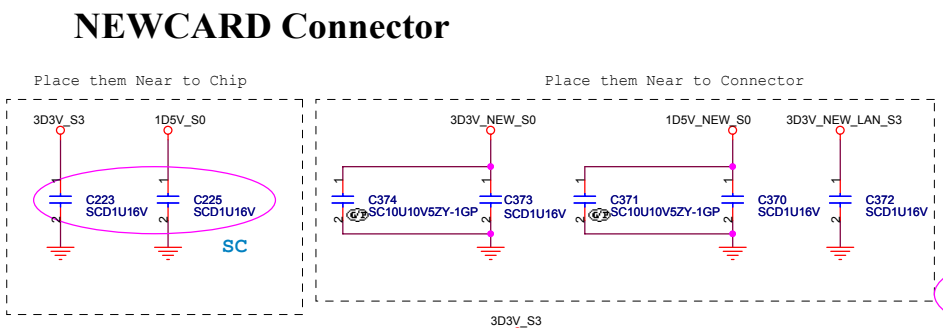


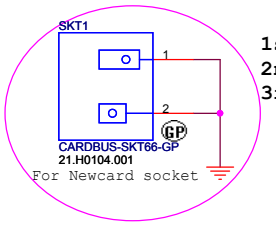
3,4,5,7,9,11,13,15,16,17,18,19,23,24,25,27,29,32,34,36,37 3D3V_S0 3D3V_S0
16,17,18,19,25,26,33,37 3D3V_S3 3D3V_S3
13,14,17,18,19,24,25,27,28,32,35,36,37 5V_S0 5V_S0
5,7,9,16,17,36,37 1D5V_S0 1D5V_S0

CDROM

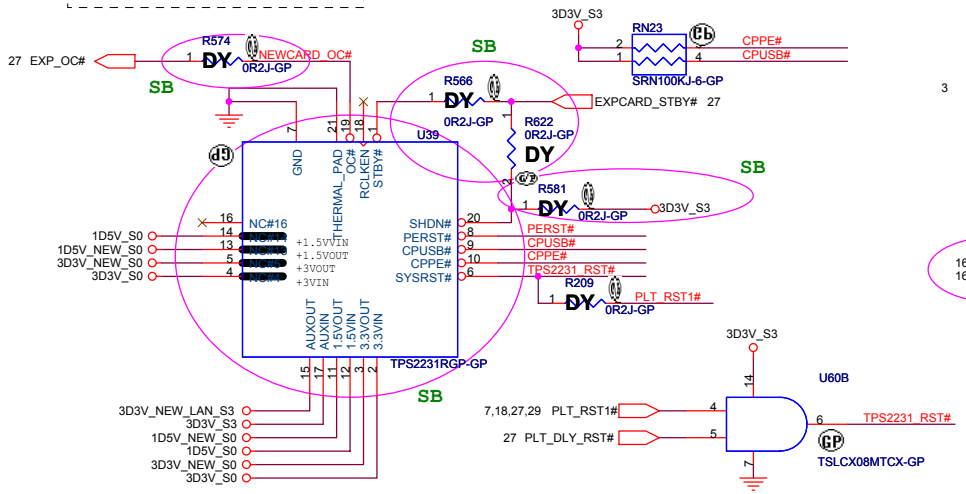


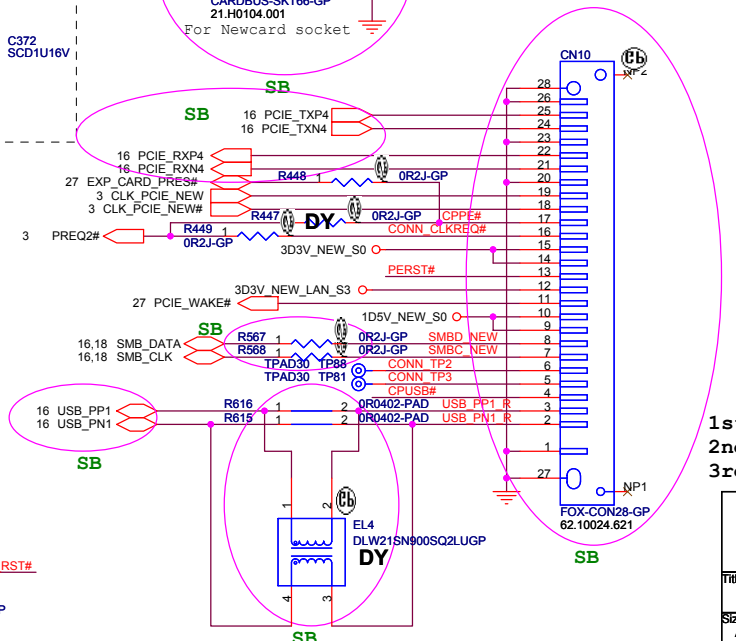
NEWCARD Connector





1st source:21.H0104.001
2nd source:21.H0103.011
3rd source:21.H0111.001





SMBUS (ICH6--NEWCARD,LAN)

1st source:62.10024.621
2nd source:62.10081.021
3rd source:20.F0782.026

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD / CDROM / NEW CARD**

Size	Document Number	Rev
A3	Key-West / Kinney	-2

Date: Friday, December 23, 2005 Sheet 20 of 37

Broadcom LAN

BCM4401

LAN EEPROM

Note: The BCM4401L has weak internal pulldown resistors on the follow signals:

SPROM_CS,SPROM_CLK,SPROM_DOUT,SPROM_DIN

BCM4401 requires 16-Bit R/W data width

1st source: Atmal: AT93C46-10SI "72.93C46.R01",
2nd source: ST : M93C46-W "72.93C46.N01",

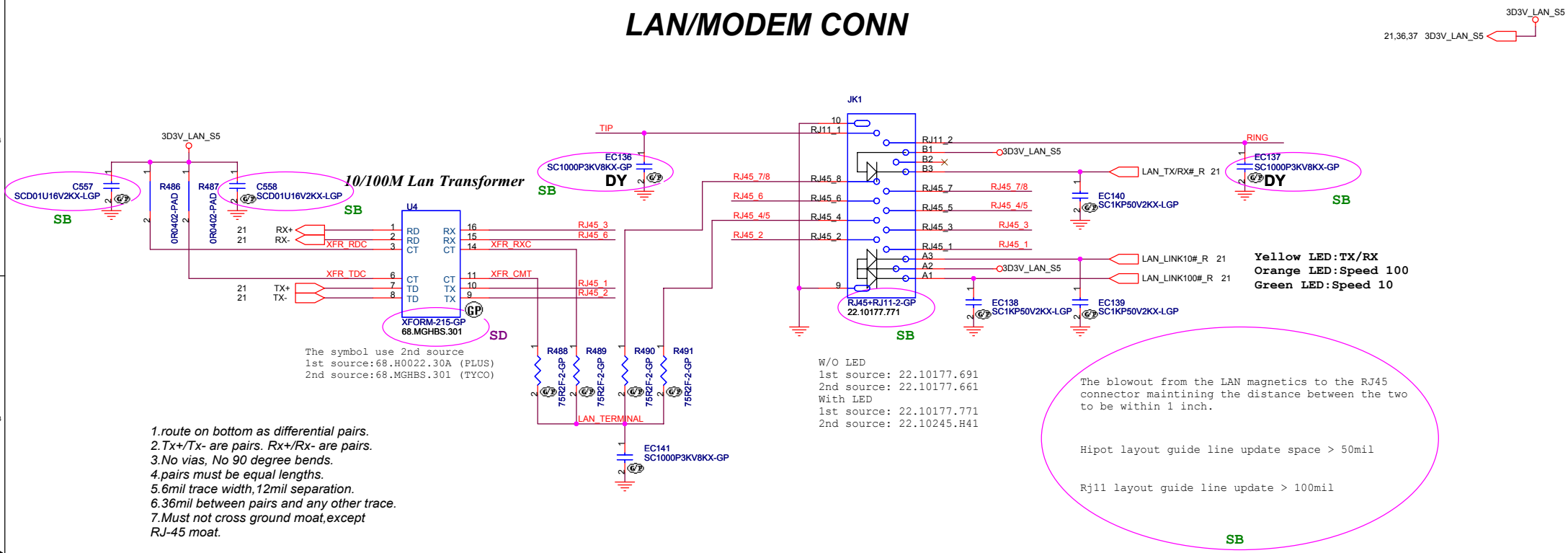
EXT_POR_L is an active low signal used to place the BCM4401 into IDDQ mode, <5 mA current consumption

X6 CL=20pF±0.2pF
Freq. Tolerance:±30ppm

Change LAN solution

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LAN BCM4401
Size: Custom	Document Number: Key-West / Kinney
Rev	-2
Date: Friday, December 23, 2005	Sheet 21 of 37

LAN/MODEM CONN



The symbol use 2nd source
1st source:68.H0022.30A (PLUS)
2nd source:68.MGHBS.301 (TYCO)

W/O LED
1st source: 22.10177.691
2nd source: 22.10177.661
With LED
1st source: 22.10177.771
2nd source: 22.10245.H41

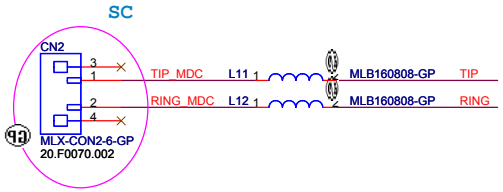
The blowout from the LAN magnetics to the RJ45 connector maintining the distance between the two to be within 1 inch.

Hipot layout guide line update space > 50mil

Rj11 layout guide line update > 100mil

SB

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

Change LAN solution

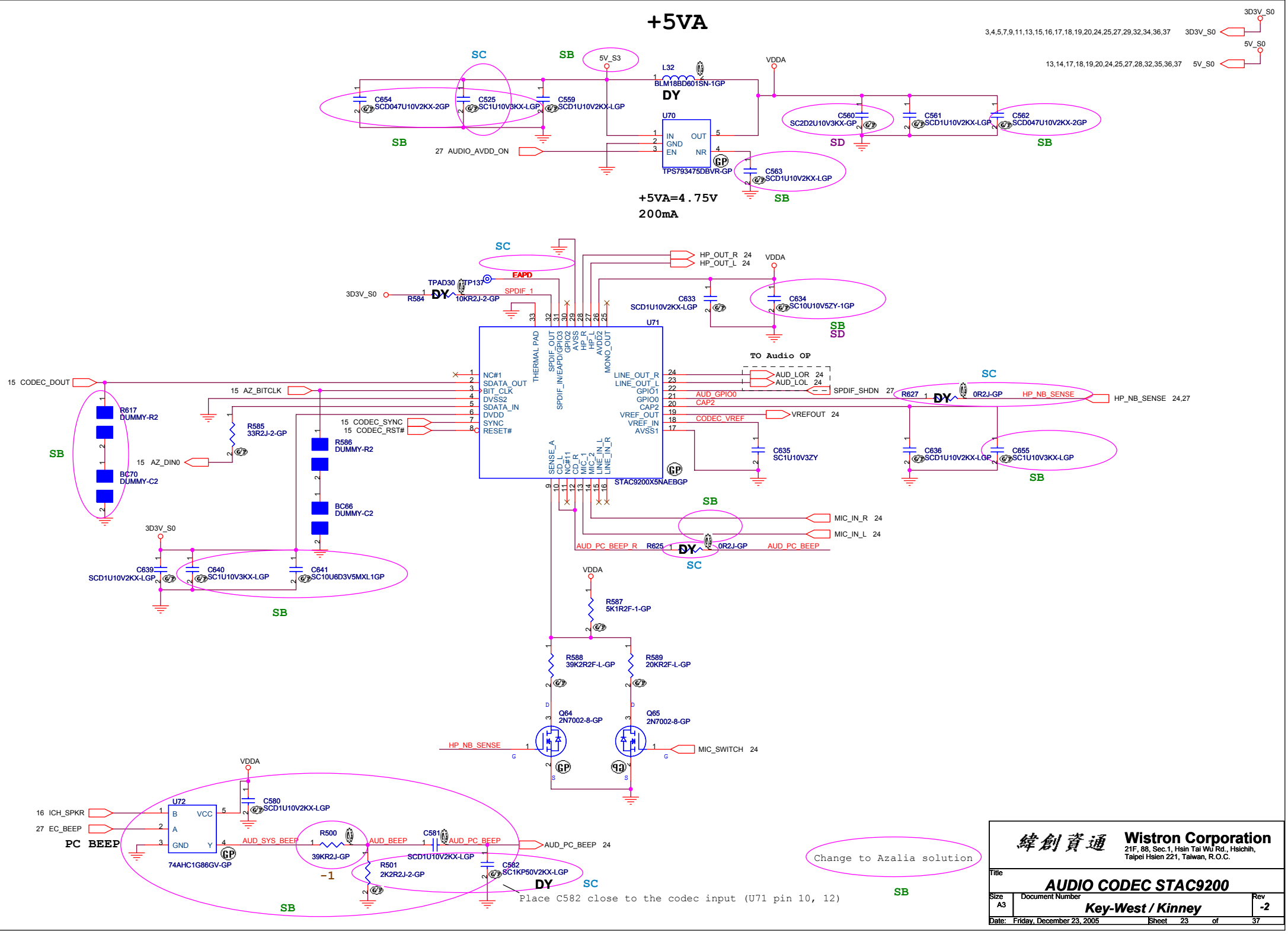
SB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

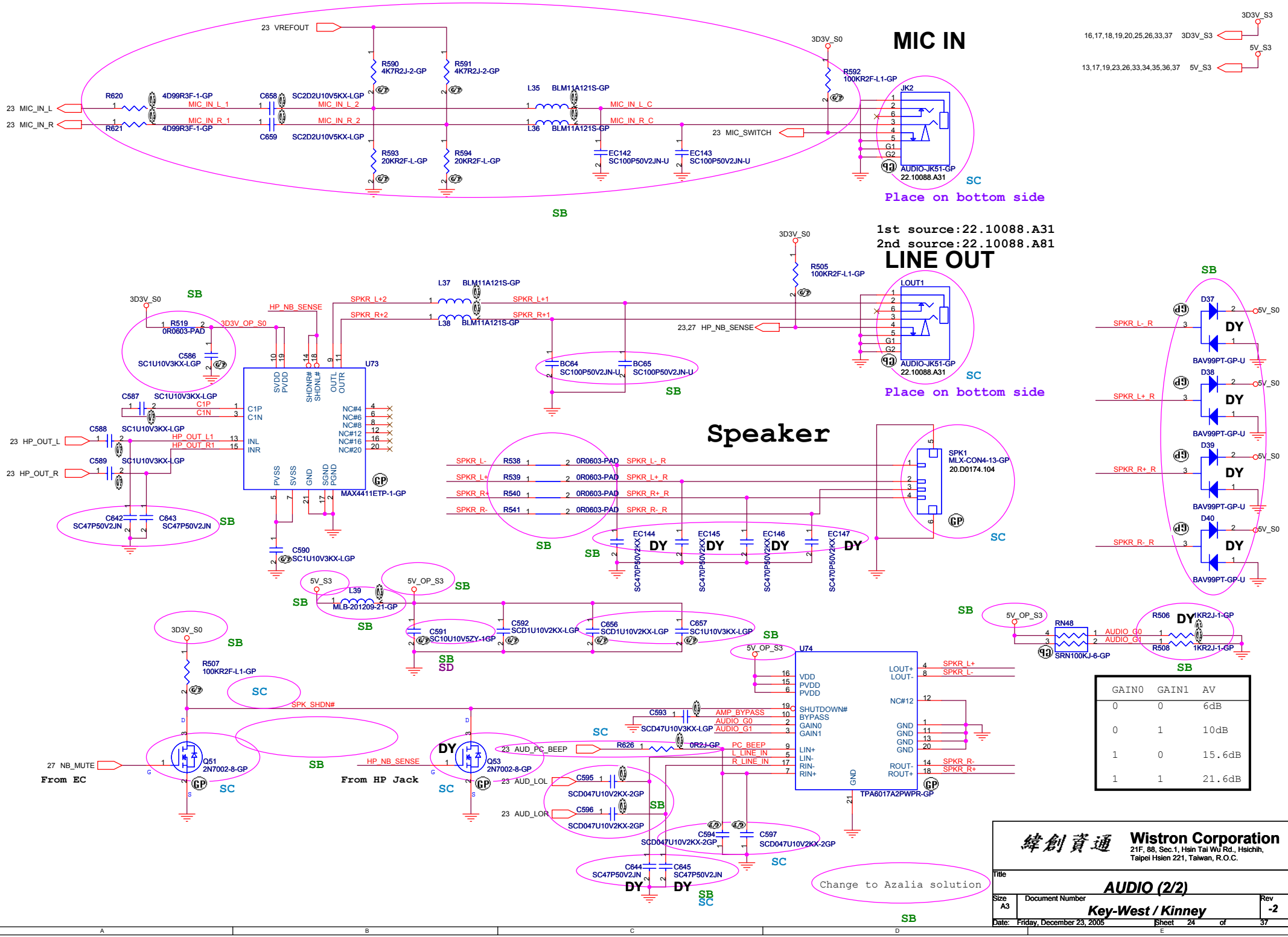
Title: LAN Connector

Size	Document Number	Rev
A3	Key-West / Kinney	-2

Date: Friday, December 23, 2005 Sheet 22 of 37



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AUDIO CODEC STAC9200**	
Size A3	Document Number **Key-West / Kinney**	Rev -2
Date: Friday, December 23, 2005	Sheet 23 of 37	



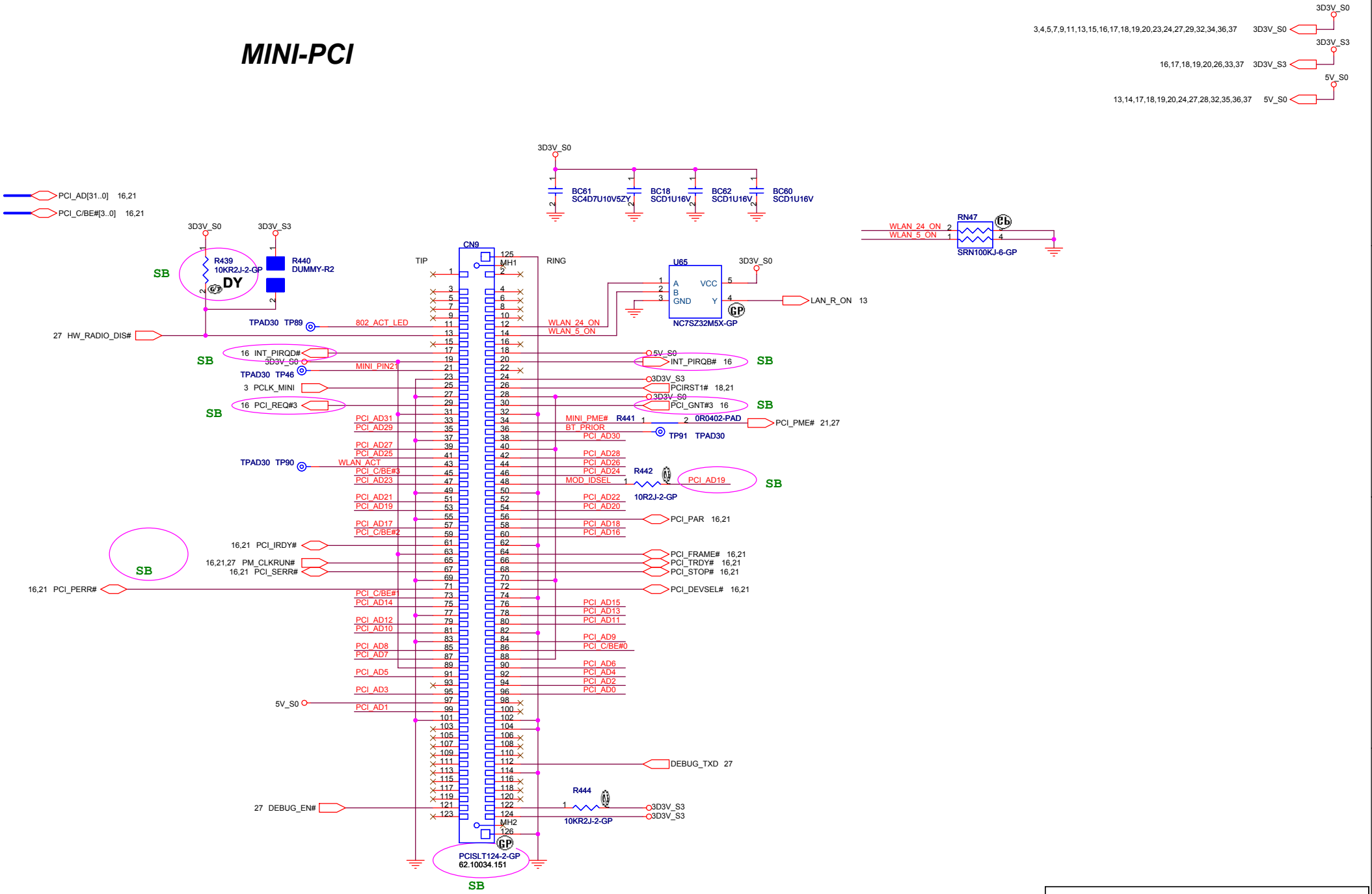
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO (2/2)

Size: A3 | Document Number: Key-West / Kinney | Rev: -2

Date: Friday, December 23, 2005 | Sheet 24 of 37

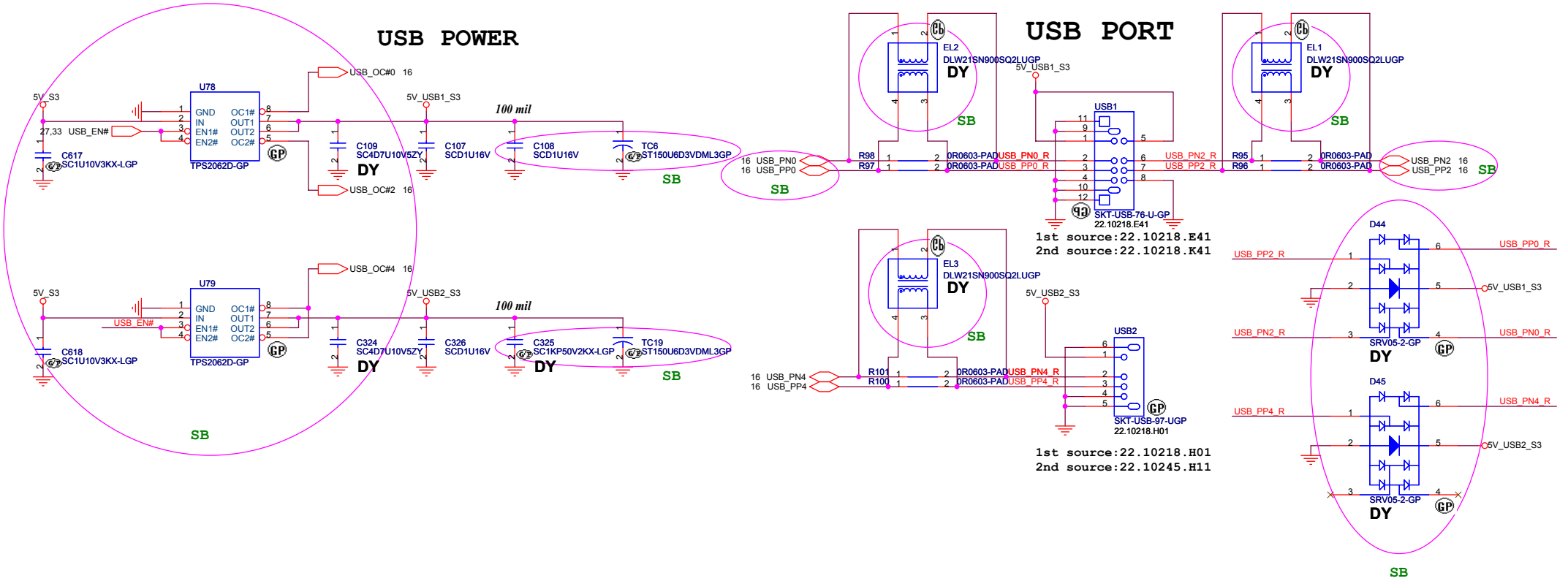
MINI-PCI

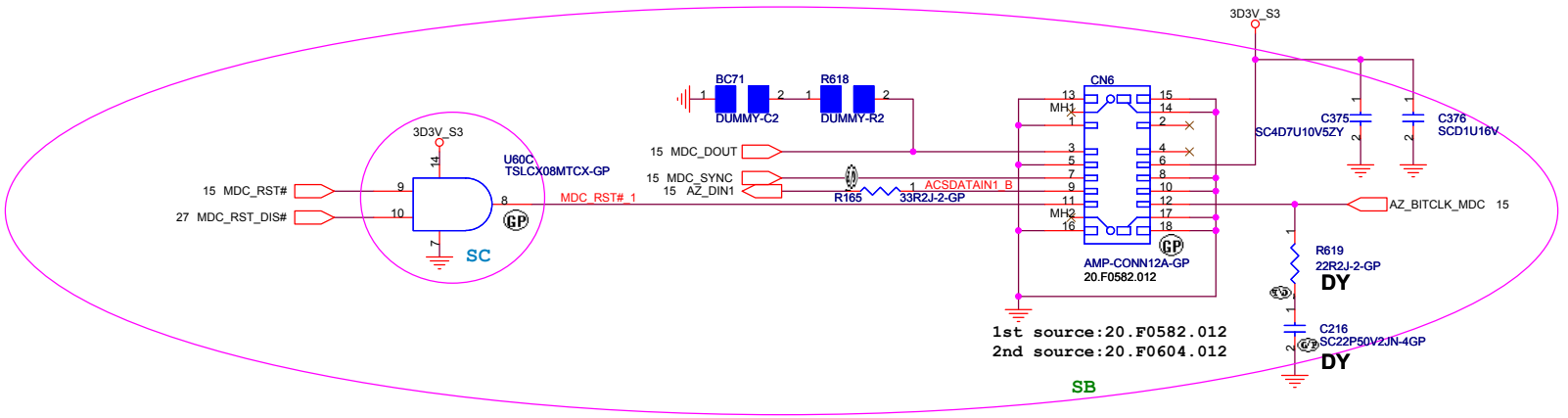


1st source:62.10034.151
2nd source:62.10043.151

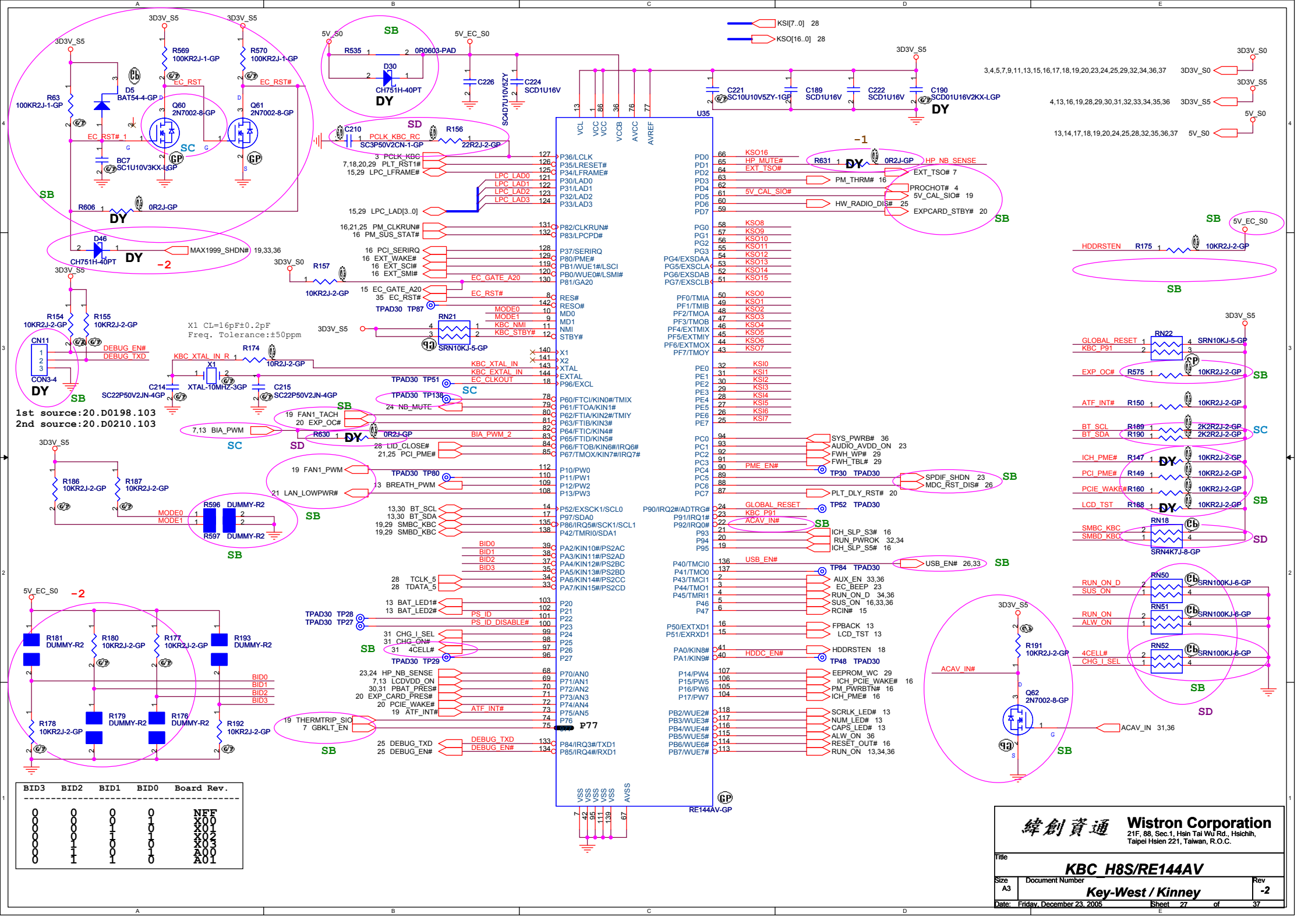
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINI-PCI	
Size A3	Document Number Key-West / Kinney	Rev -2
Date: Friday, December 23, 2005	Sheet 25 of 37	





緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB / MDC CONN.***	
Size A3	Document Number ***Key-West / Kinney***	Rev -2
Date: Friday, December 23, 2005	Sheet 26 of 37	


1st source:20.D0198.103
2nd source:20.D0210.103
X1 CL=16pF±0.2pF
Freq. Tolerance:±50ppm
U35
RE144AV-GP
P77
KSI[7..0] 28
KSO[16..0] 28
3,4,5,7,9,11,13,15,16,17,18,19,20,23,24,25,29,32,34,36,37
4,13,16,19,28,29,30,31,32,33,34,35,36
13,14,17,18,19,20,24,25,28,32,35,36,37
BID3 BID2 BID1 BID0 Board Rev.
0 0 0 0 NFF
0 0 0 1 X00
0 0 1 0 X01
0 0 1 1 X02
0 1 0 0 X03
0 1 0 1 A00
0 1 1 0 A01
Wistron Corporation
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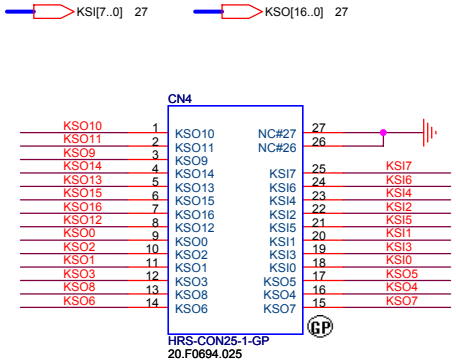
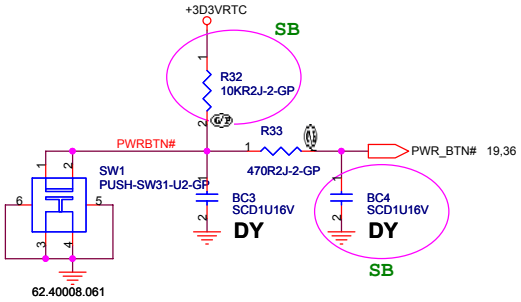
Title
KBC_H8S/RE144AV
Size A3
Document Number
Key-West / Kinney
Rev -2
Date: Friday, December 23, 2005
Sheet 27 of 37

INTERNAL KEYBOARD CONNECTOR



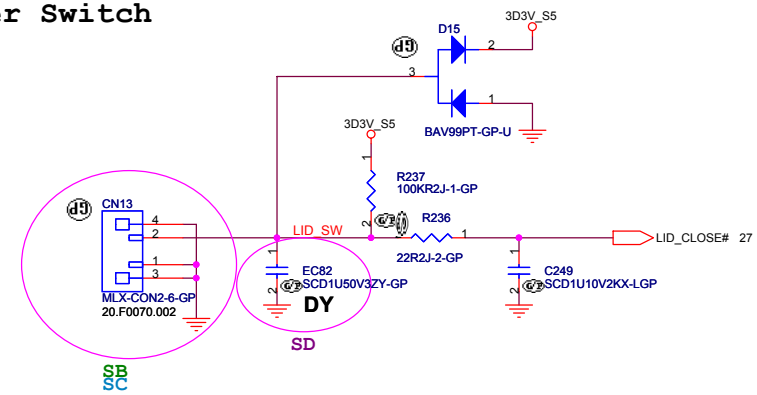
1st source : 20.F0694.025
2nd source : 20.F0642.025

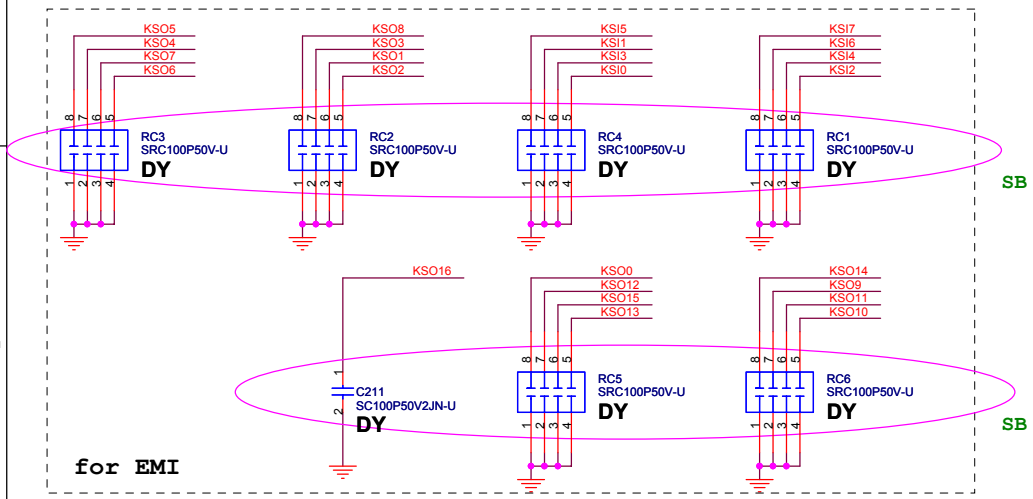
POWER BUTTON



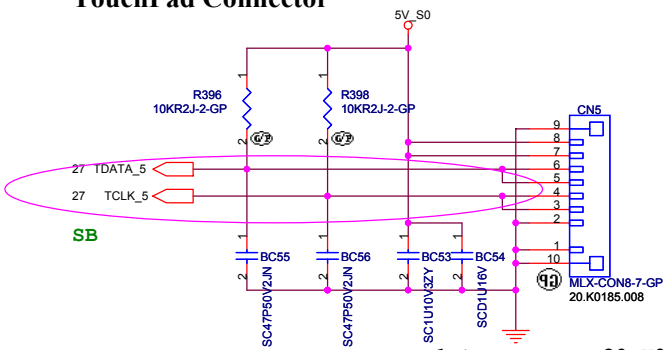
1st source : 62.40008.061
2nd source : 62.40009.191

Cover Switch





TouchPad Connector



1st source : 20.K0185.008
2nd source : 20.K0212.008

<Variant Name>

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Title: ***KB / TPAD / LID SW / PWR BTN***

Size	Document Number	Rev
A3	***Key-West / Kinney***	-2

Date: Friday, December 23, 2005 Sheet 28 of 37

3D3V_S5

4,13,16,19,27,28,30,31,32,33,34,35,36 3D3V_S5

512KB Flash

Unused FGPI pins must not be float

LPC_LAD[3..0] 15,27

RP1
SELECT_FWH 1
FWH_FGPI4 2
FWH_FGPI3 3
FWH_FGPI2 4
5
10
9
8
7 FWH_FGPI1
6 FWH_FGPI0
SRN10KJ-L3-GP

SB
3D3V_S0
C242 SCD1U16V
C241 SC1U10V3ZY

LPC_LFRAME# 15,27
FWH_INIT# 15
PLT_RST1# 7,18,20,27
SELECT_FWH
PCLK_FWH 3

R227 DUMMY-R3
PCLK_FWH_RC
C243 DUMMY-C3

U40
VDD 25
VDD 32
WE#/FWH4 23
OE#/INIT# 24
R/C#/CLK 31
RST# 2
IC 29

A0/ID0 12
A1/ID1 11
A2/ID2 10
A3/ID3 9
A4/TBL# 8
A5/WP# 7
A6/FGPI0 6
A7/FGPI1 5
A8/FGPI2 4
A9/FGPI3 3
A10/FGPI4 30

DQ0/FWH0 13 LPC_LAD0
DQ1/FWH1 14 LPC_LAD1
DQ2/FWH2 15 LPC_LAD2
DQ3/FWH3 17 LPC_LAD3
DQ4/RES 18
DQ5/RES 19
DQ6/RES 20
DQ7/RES 21

VSS 28
VSS 16
NC#27 27
NC#26 26
NC#22 22
NC#1 1

49LF004B334C-GP
72.49004.F03

SB
3D3V_S0
RN20
SRN10KJ-5-GP
27 FWH_TBL#
27 FWH_WP#
FWH_FGPI0
FWH_FGPI1
FWH_FGPI2
FWH_FGPI3
FWH_FGPI4

SCOKET:
62.10002.032
62.10005.032

1st source:72.49004.F03 (SST)
2nd source:72.49004.G03 (PMC)
3rd source:72.39040.J03 (Winbond)

SMBus address A2

User Password

3D3V_S5
U32
A0 1
A1 2
A2 3
GND 4
VCC 8
WP 7
SCL 6
SDA 5
AT24C04N-10SU-GP
72.24C04.E01

3D3V_S5
C188
SCD1U10V2KX-LGP
EEPROM_WC 27
SMBC_KBC 19,27
SMBD_KBC 19,27

The symbol use 2nd source
1st source:72.24C04.G01 (ST)
2nd source:72.24C04.E01 (ATMEL)

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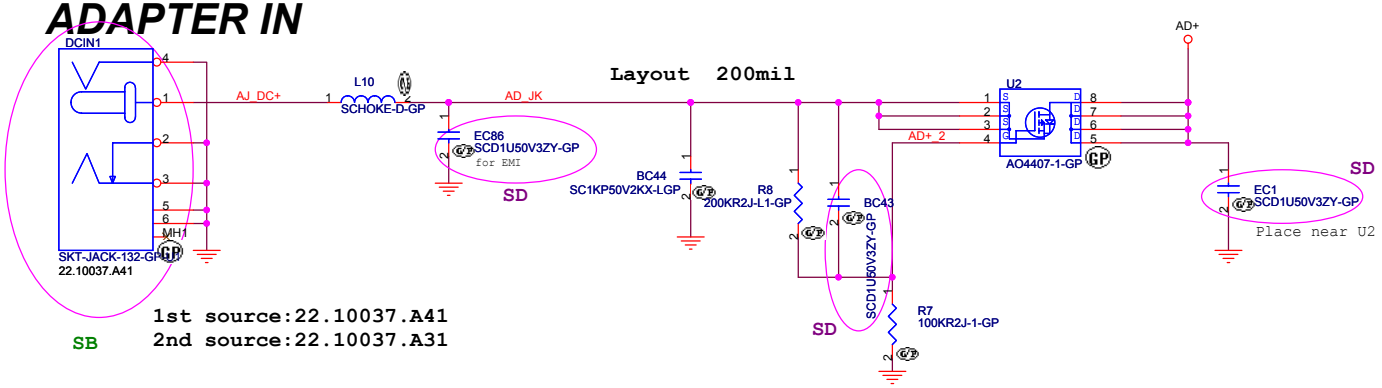
Title	**BIOS**	
Size A3	Document Number **Key-West / Kinney**	Rev -2
Date: Friday, December 23, 2005	Sheet 29 of 37	

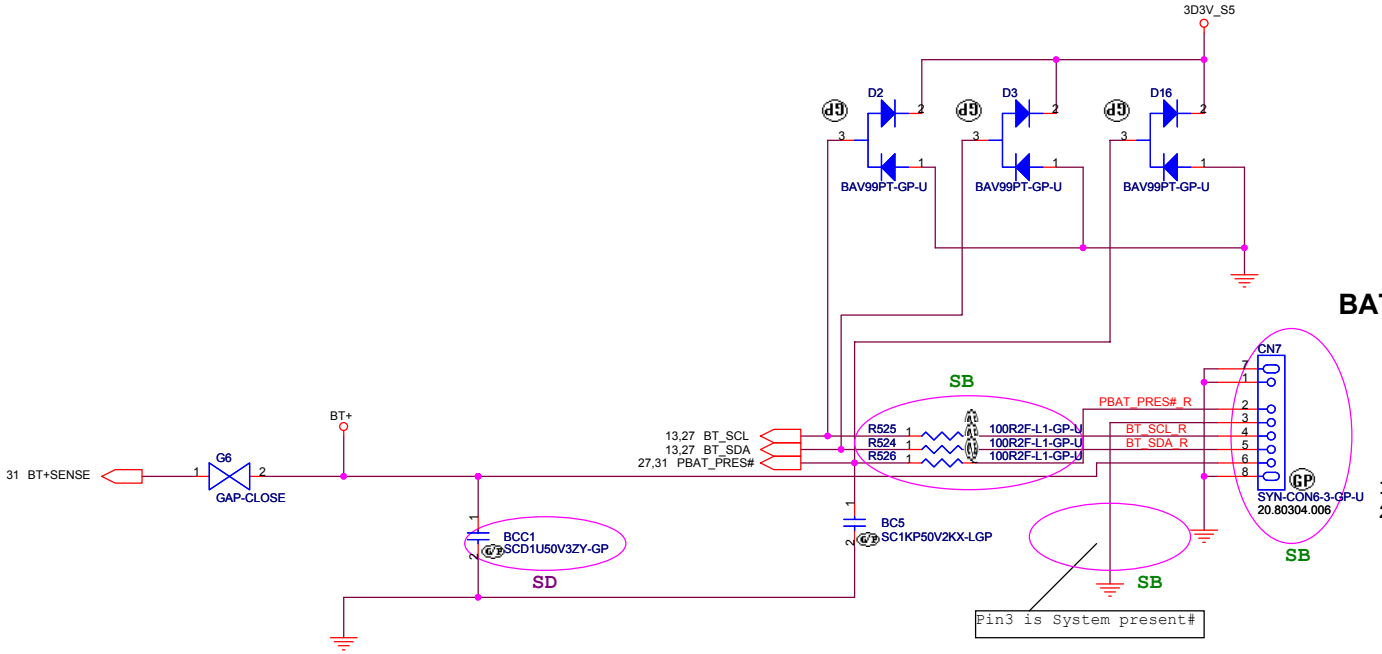
Adaptor in to generate DCBATOUT

ADAPTER IN



SB

1st source:22.10037.A41
2nd source:22.10037.A31



BATTERY CONNECTOR

1st source:20.80304.006
2nd source:20.80385.006

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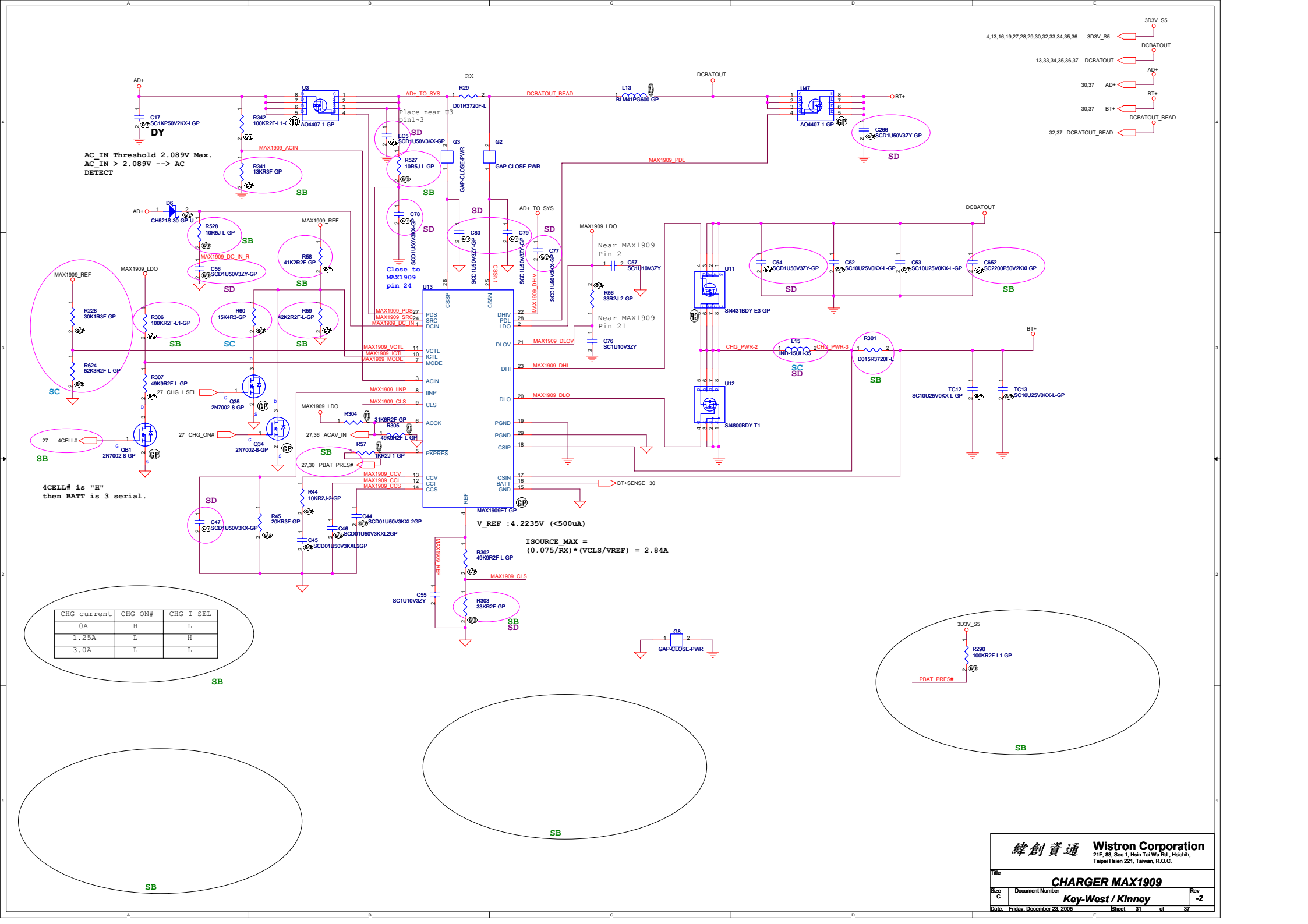
Title	***Adaptor/ Bettery conn.***	
Size A3	Document Number ***Key-West / Kinney***	Rev -2
Date: Friday, December 23, 2005	Sheet 30 of 37	


AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
4CELL# is "H"
then BATT is 3 serial.
Close to MAX1909 pin 24
Near MAX1909 Pin 2
Near MAX1909 Pin 21
Place near U3 pin1~3
V_REF :4.2235V (<500uA)
ISOURCE_MAX = (0.075/RX)*(VCLS/VREF) = 2.84A
MAX1909ET-GP
CHG current | CHG_ON# | CHG_I_SEL
0A | H | L
1.25A | L | H
3.0A | L | L
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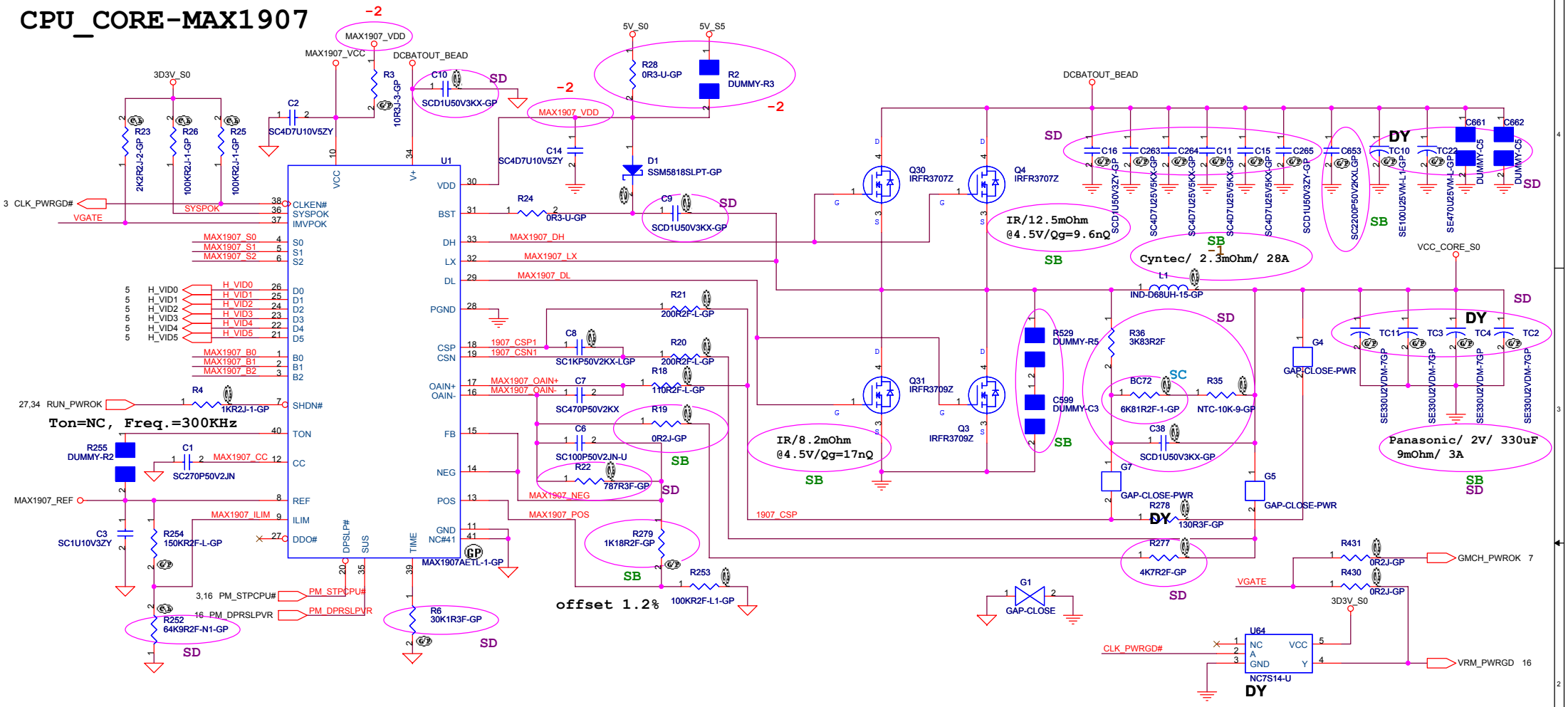
CHARGER MAX1909
Key-West / Kinney
Size C
Rev -2
Date: Friday, December 23, 2005
Sheet 31 of 37

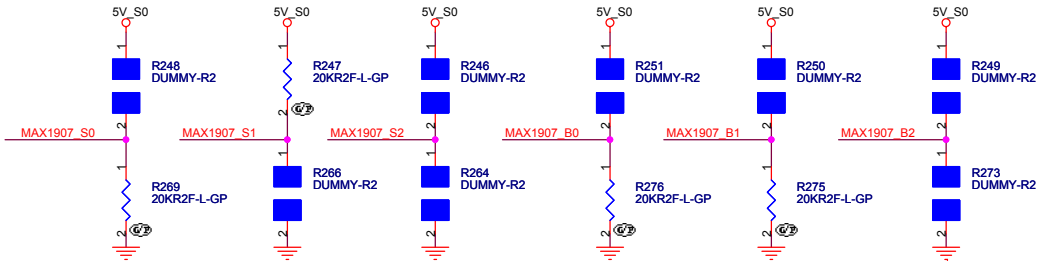
CPU_CORE-MAX1907



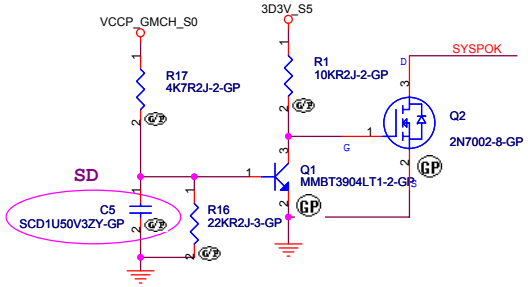
OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940



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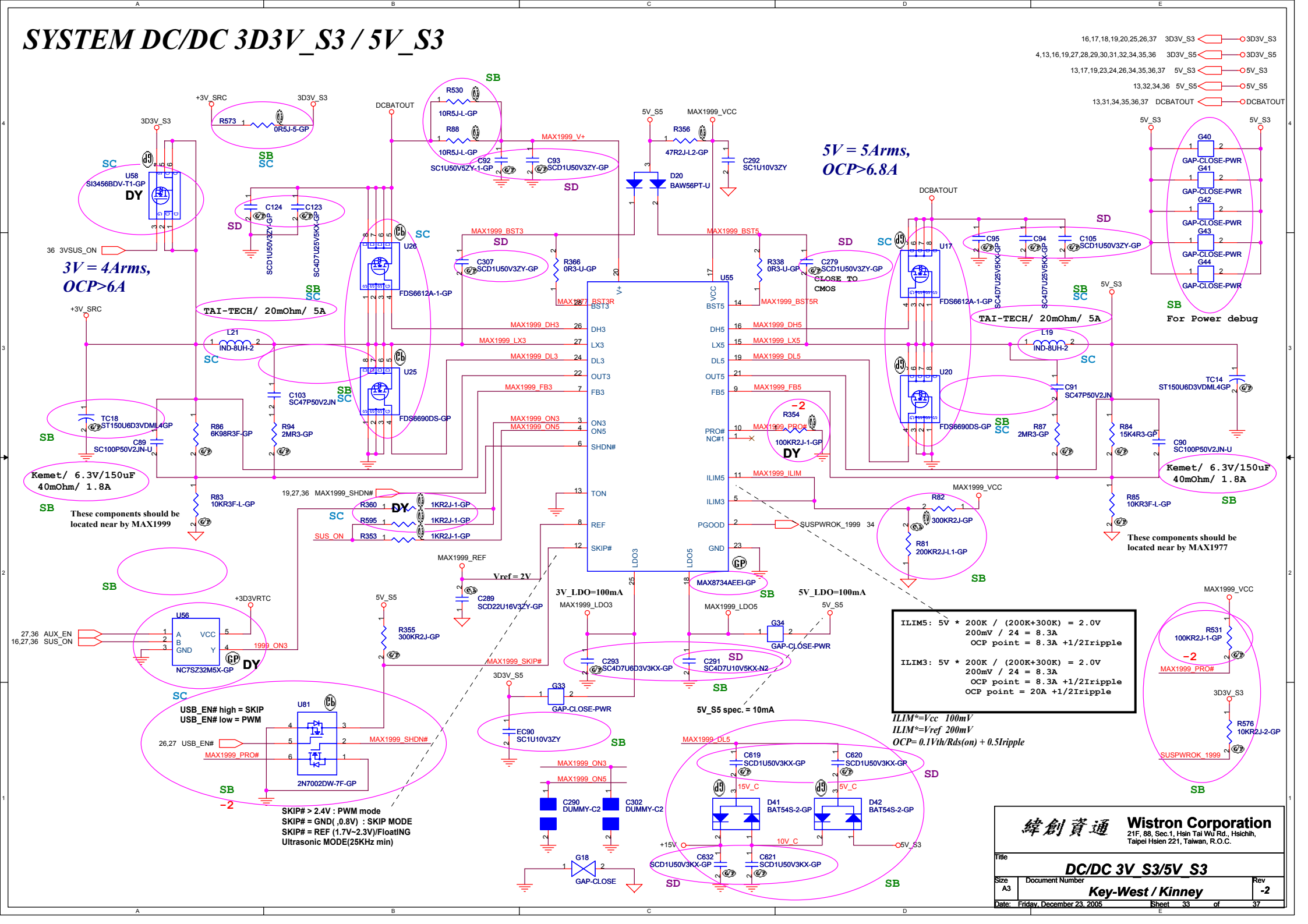
Title: **IMVP IV-CPU POWER-MAX1907**

Size	Document Number	Rev
A3	Key-West / Kinney	-2

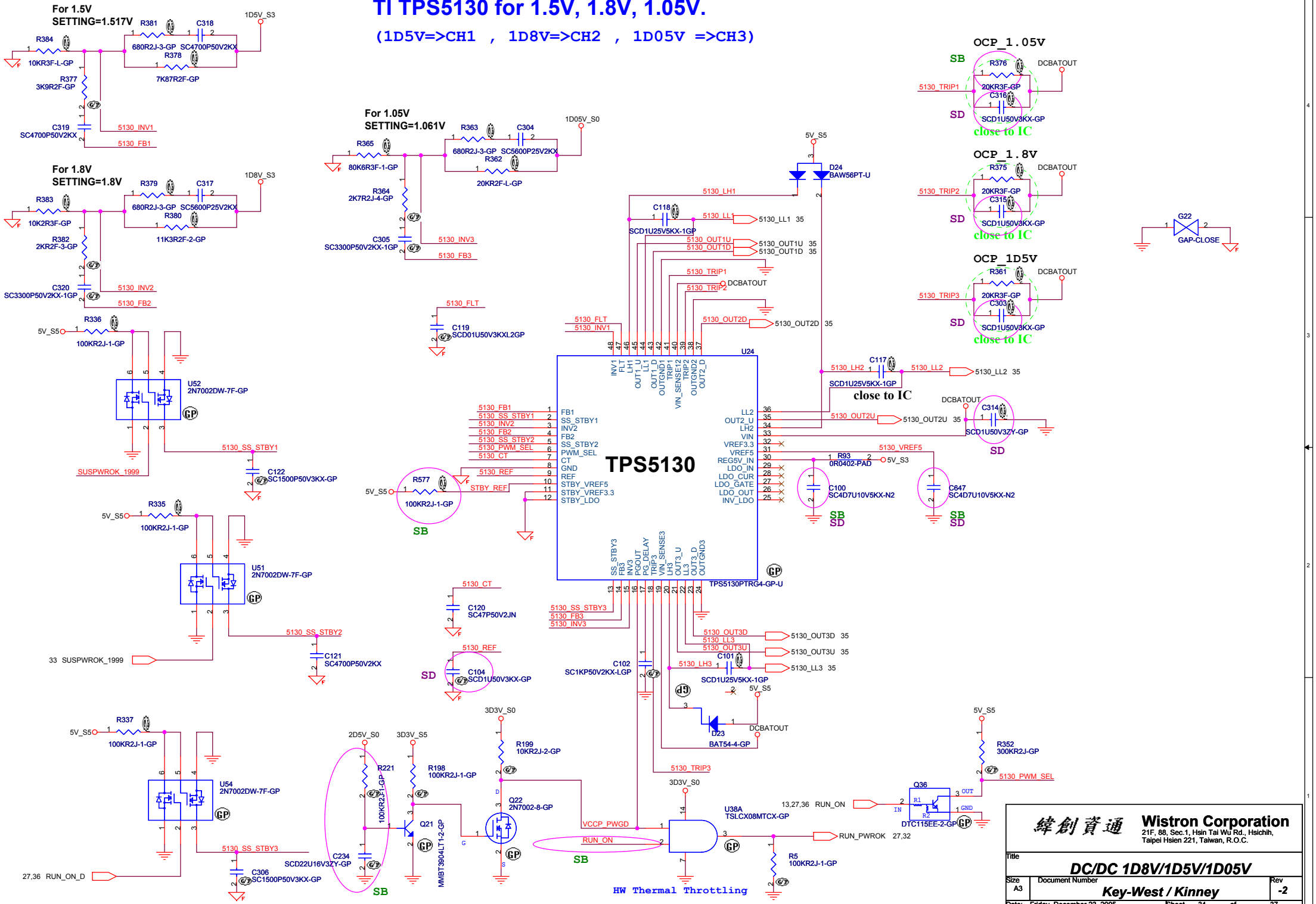
Date: Friday, December 23, 2005 Sheet 32 of 37

SYSTEM DC/DC 3D3V_S3 / 5V_S3



TI TPS5130 for 1.5V, 1.8V, 1.05V.

(1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)



Wistron Corporation	緯創資通
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Title	DC/DC 1D8V/1D5V/1D05V
Size A3	Document Number Key-West / Kinney
Rev -2	
Date: Friday, December 23, 2005	Sheet 34 of 37

TI TPS5130 for 1.5V, 1.8V, 1.05V

(1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)

13,31,33,34,36,37 DCBATOUT
13,32,33,34,36 5V_S5
10,34,36,37 1D05V_S0
7,9,10,11,12,16,34,36,37 1D8V_S3
13,14,17,18,19,20,24,25,27,28,32,36,37 5V_S0
12,36 0D9V_S0
17,34,36 1D5V_S3

For DDR REF S3 Power

DDR_VREF_S3 need 10 mil and must neat NB and DIMM

VREFOUT = 0.9V

Power budget:0.9V/2.2Apeak (For DDR2_VTT)

0D9V / 1A

L3# circuit

1D5V/5A
OCP=10A

1D8V/5A
OCP=10A

1D05V/5A
OCP=10A

Rds(on)=20mOhm

VISHAY/30mOhm
@4.5V/Qg=8.7nQ

IR/18.2mOhm
@4.5V/Qg=7.2nQ

GANG SONG/16mOhm/6.8A

Panasonic/2V/220uF
9mOhm/3A

KEMENT/4V/220uF
40mOhm/ 1.8A

KEMENT/4V/220uF
25mOhm/ 2.2A

For Power debug

SB SC SD DY

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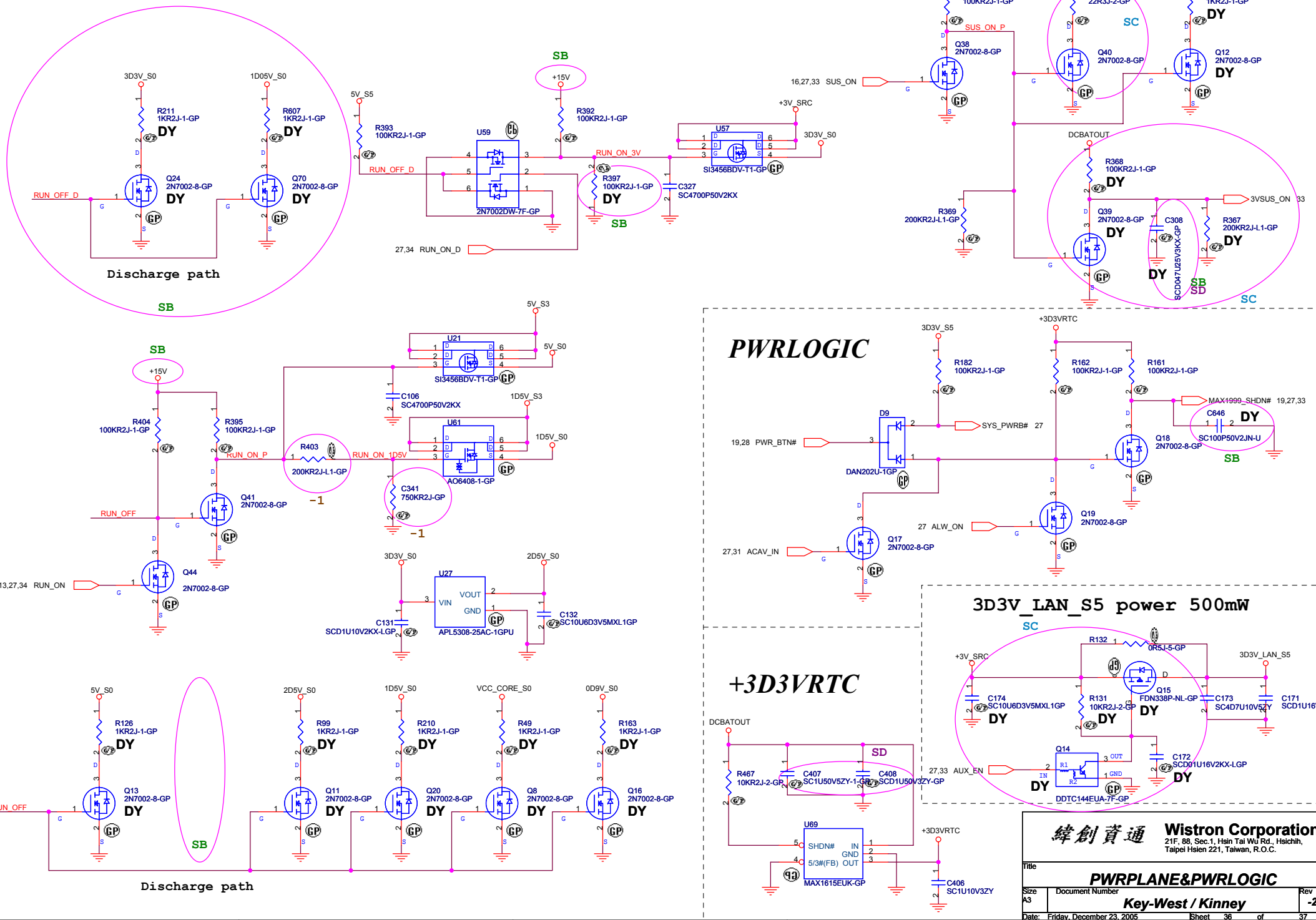
Title: DC/DC 1D8V/1D5V/1D05V-2
Size: A3
Document Number: Key-West / Kinney
Rev: -2
Date: Friday, December 23, 2005
Sheet 35 of 37

Run Power



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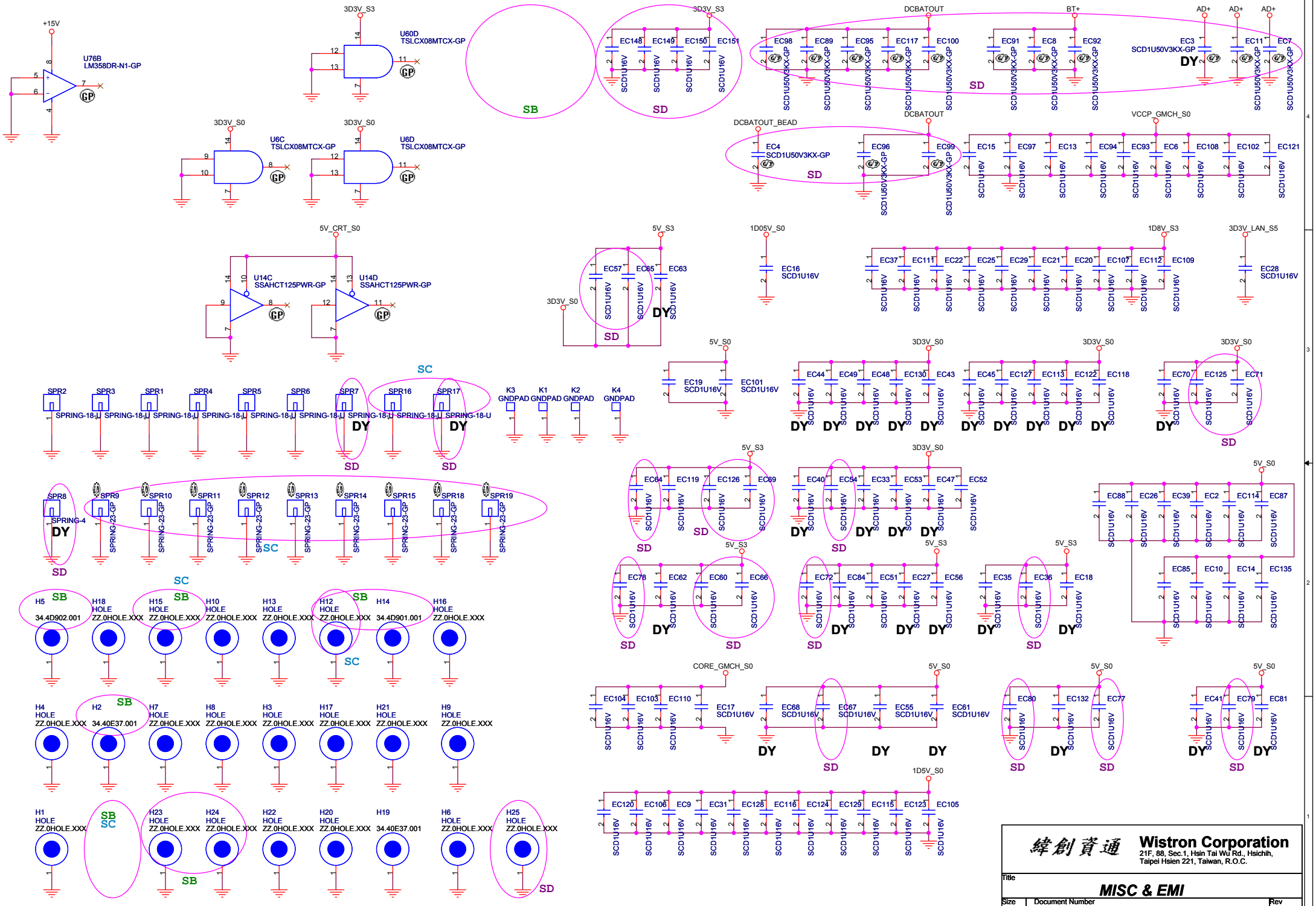
Title	**PWRPLANE&PWRLOGIC**
Size: A3	Document Number: **Key-West / Kinney**
Rev: -2	
Date: Friday, December 23, 2005	Sheet 36 of 37



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Title: **MISC & EMI**

Size	Document Number	Rev
A3	Key-West / Kinney	-2

Date: Thursday, December 22, 2005 Sheet 37 of 37