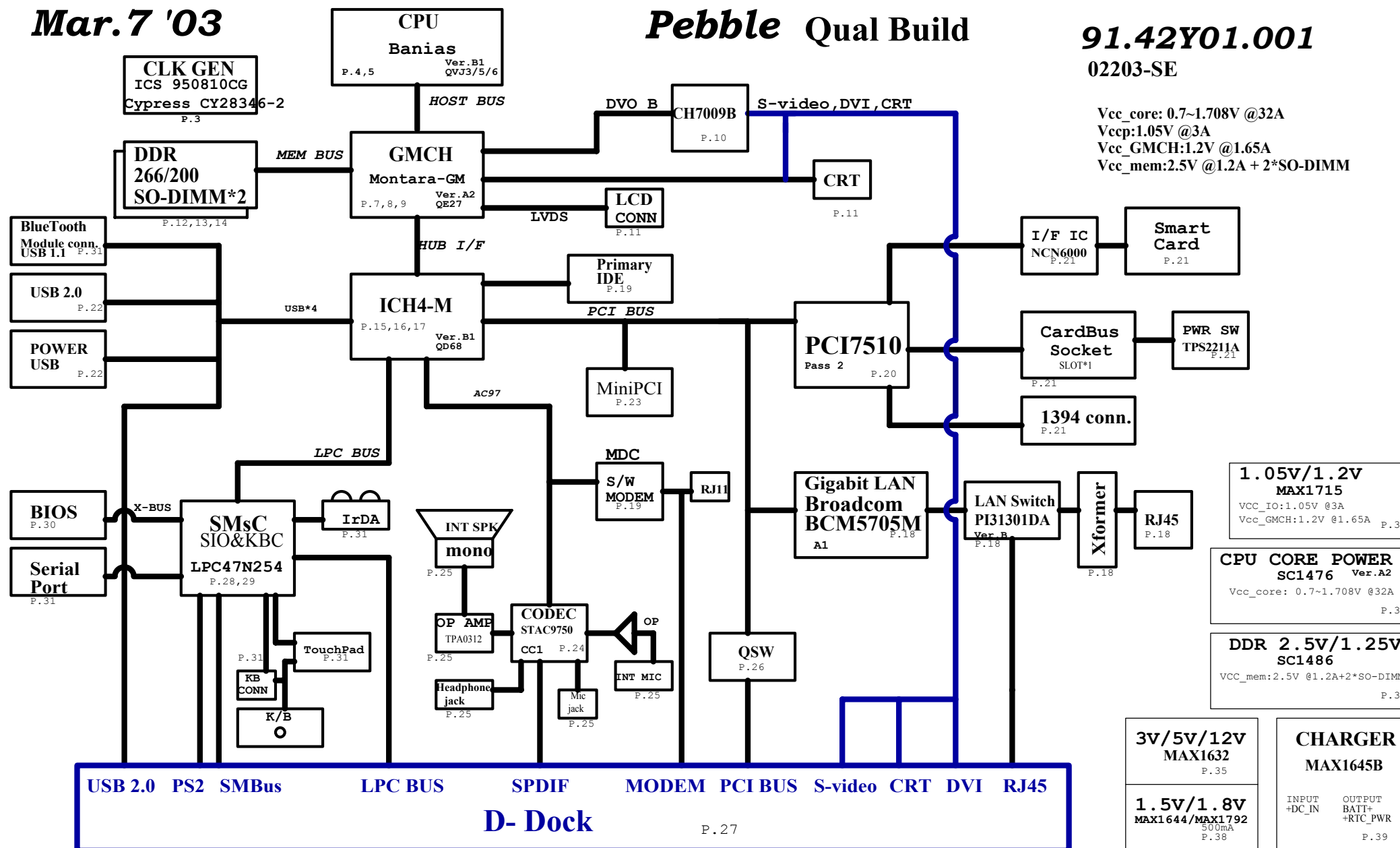


Mar. 7 '03

Pebble Qual Build

91.42Y01.001

02203-SE



DELL-Wistron confidential

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CG_*	: CPU GTL+
CC_*	: CPU CMOS
M_*	: MEMORY BUS
G_*	: AGP BUS
P_*	: PCI BUS
HL_*	: HUB LINK I/F
LPC_*	: LPC I/F
ICH_AC_*	: AC'97 LINK I/F
IDE_*	: IDE BUS

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#	DREQ/DGNT
PCMCIA PCI7510	AD17	PIRQD# PIRQC#	REQB# / GNTB#	REQ#1 / GNT#1
LAN Broadcom BCM5705M	AD16	PIRQC#		REQ4# / GNT4#
MINIPCI SLOT	AD19	PIRQB# PIRQD#		REQ3# / GNT3#
D-DOCK	AD24	PIRQB#		REQ0# / GNT0#

Montania to Montania+ changes

1.Changed VR resistor to generate 1.35V for MGM+ core(R529,R530)
2.Changed R112 from 27.4 to 37.4 Ohm (changes HLZCOMP for MGM+)
3.Put R612,R613,R614 1K ohm
4.Need Changed PSWING,HLVREF for MGM+ if use MGM core (For Pebble don't need change because we use +1.5VRUN)
5.Layour meet DDR333 require (For Pebble already done)

+DC_IN		+DC_IN	27,37,39
DOCK_DC_IN		DOCK_DC_IN	27
PWR_SRC		PWR_SRC	11,22,27,33,35,36,37,38,39
DOCK_PWR_SRC		DOCK_PWR_SRC	27
VCC_IO		VCC_IO	4,5,6,7,9,16,17,33,38
VCC_CORE		VCC_CORE	5,33,36
+1.5VRUN		+1.5VRUN	4,7,8,9,10,11,15,17,33
+1.8VRUN		+1.8VRUN	4,33,38
+1.2VRUN		+1.2VRUN	7,9,38

+3VRUN		+3VRUN	3,4,6,8,9,10,11,12,15,16,17,18,19,23,24,26,28,29,31,32,33,34,36,38,40
+3VSUS		+3VSUS	6,11,15,16,17,18,19,20,21,23,25,27,31,33,34,37,38,40
+3VALW		+3VALW	16,25,27,28,29,30,34,40
+3.VRTC		+3.VRTC	16,28,34,37
+5VRUN		+5VRUN	6,8,10,11,17,19,23,26,29,31,32,33,34,36,37,40

+5VSUS		+5VSUS	6,11,17,21,22,24,25,31,32,33,34,35,37,38,40
+5VALW		+5VALW	11,27,28,32,33,34,39
+5V_QDOCK		+5V_QDOCK	26
+3VAUX_LAN		+3VAUX_LAN	18,23,33
+1.2VAUX_LAN		+1.2VAUX_LAN	18
+2.5VAUX_LAN		+2.5VAUX_LAN	18,27
BATT+		BATT+	39
+5VHDD		+5VHDD	19,33

LCDVDD		LCDVDD	11
AC97_5V		AC97_5V	19
AC97_3V		AC97_3V	19
CRT_VCC		CRT_VCC	11
CBS_VCC		CBS_VCC	20,21
CBS_VPP		CBS_VPP	21
CBS_VCCF		CBS_VCCF	21
+1.25VRUN		+1.25VRUN	13,14,33,37
+2.5VSUS		+2.5VSUS	6,7,9,12,14,33,37
ICH_VBIAS		ICH_VBIAS	16
VCC_RTC		VCC_RTC	16
+RTCSRC		+RTCSRC	37
+RTC_PWR		+RTC_PWR	34,35,37,39,40

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
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Size	Document Number	Rev
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Date:	Monday, February 24, 2003	Sheet 2 of 40

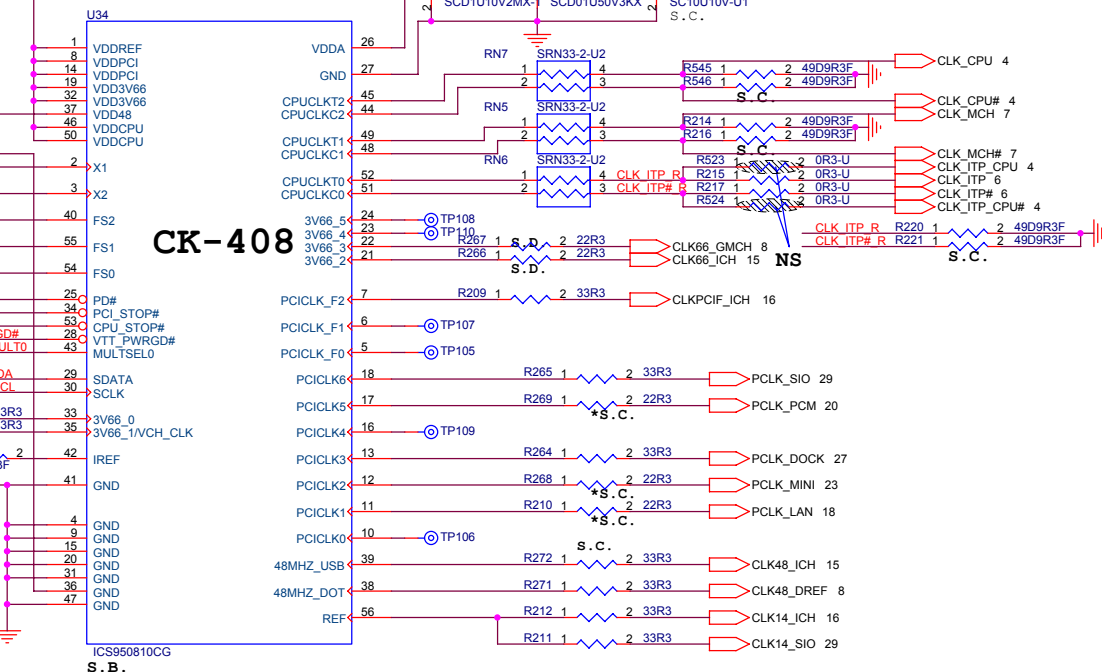
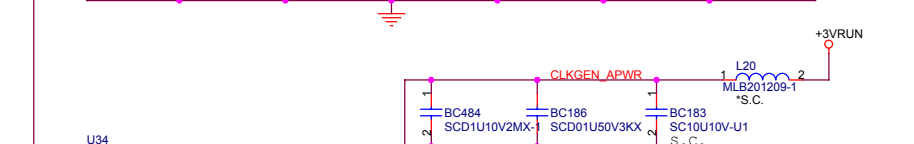
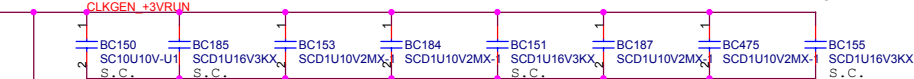
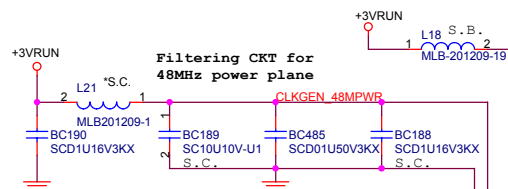
FS1/0 = 00	66MHz
FS1/0 = 01	100MHz
FS1/0 = 10	200MHz
FS1/0 = 11	133MHz

FS2 = 0 unbuffer mode (disable 66MHz-IN)
FS2 = 1 buffer mode

Mult0 = 0 Rr=221,Iref=5mA =>Vswing=1.0V@50ohm
Mult0 = 1 Rr=475,Iref=2.32mA =>Vswing=0.7V@50ohm

The schematic diagram illustrates the CK408 IMVP_PWRGRD power plane. It features a +3VRUN input connected to a network of resistors and dummy components. The network includes resistors R544 (10KR3), R520 (1KR3), R519 (DUMMY-R3), R543 (DUMMY-R3), R521 (DUMMY-R3), R522 (1KR3), and R291 (10KR3). A shaded oval highlights a section with two 8C10P capacitors and a 8C10P capacitor. The output is connected to pin 7,34 of the CK408_IMVP_PWRGRD component, which is also connected to pin 1 of a component labeled D 8 DREFS, Q3 20 CLK_4, S 2N7002.

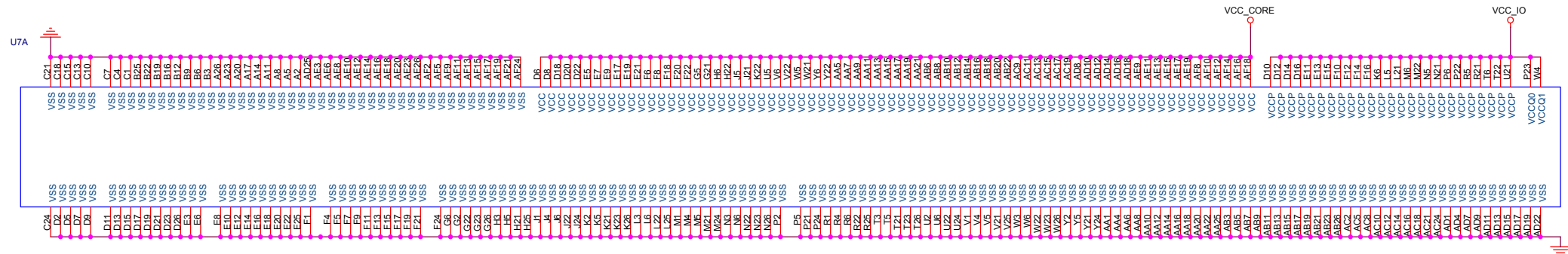
No stuff:
caps are internal to CK-TITAN.



CK-408

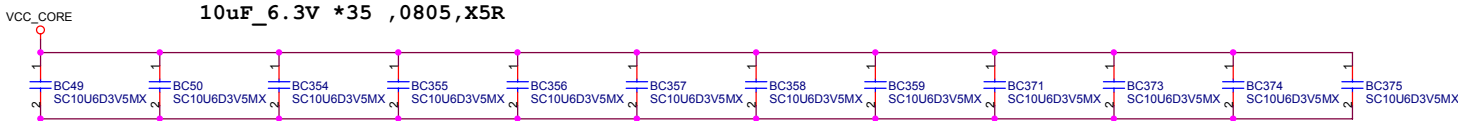
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<i>Clock GEN.</i>			
Size	Document Number	Rev	
A3	PEBBLE--02203	SD	
Date:	Thursday, March 13, 2003	Sheet	3 of 40

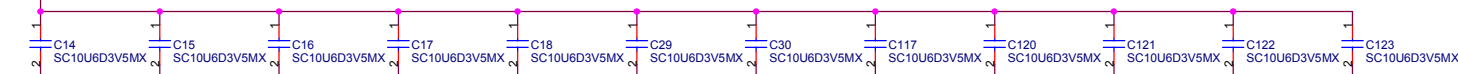


BANIAS-1D6G-1U

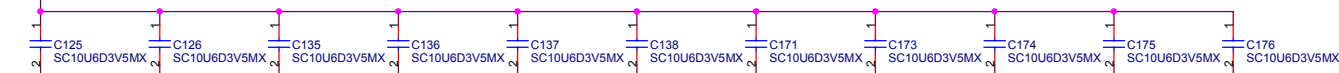
10uF_6.3V *35 ,0805,X5R



VCC_CORE



VCC_CORE



Banias CPU part number

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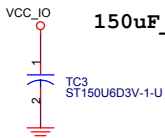
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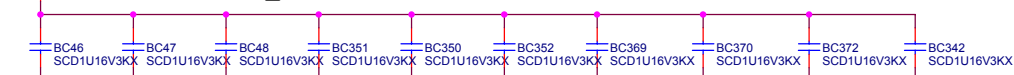
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B9.00020.001 IC CPU BANIAS1.3G UFCBGA

VCC_IO 150uF 6.3V *1

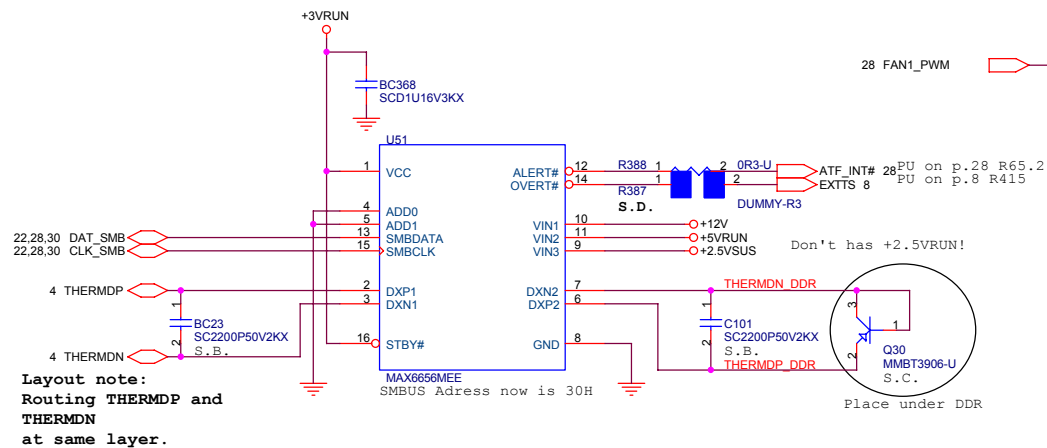


0.1uF_16V *10 ,0603,X7R

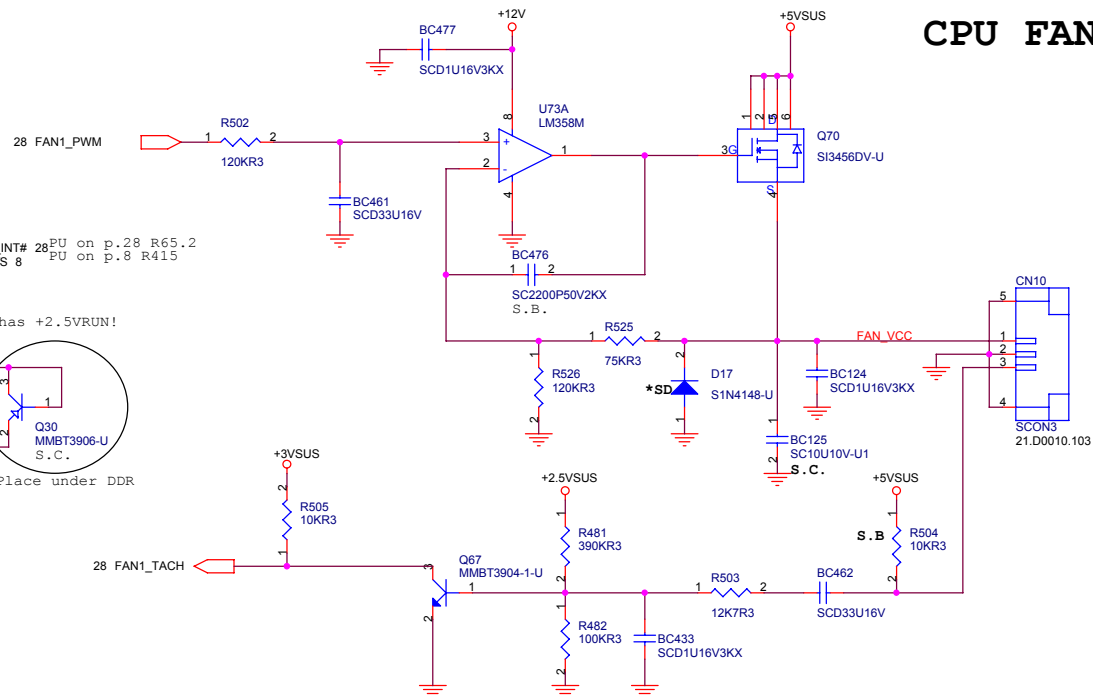


Place near CPU

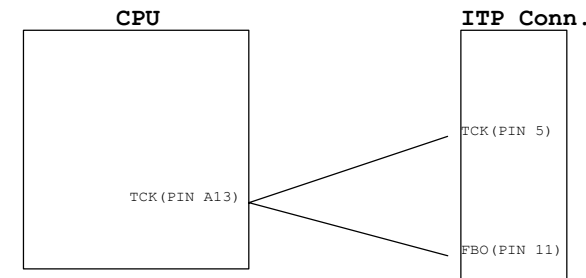
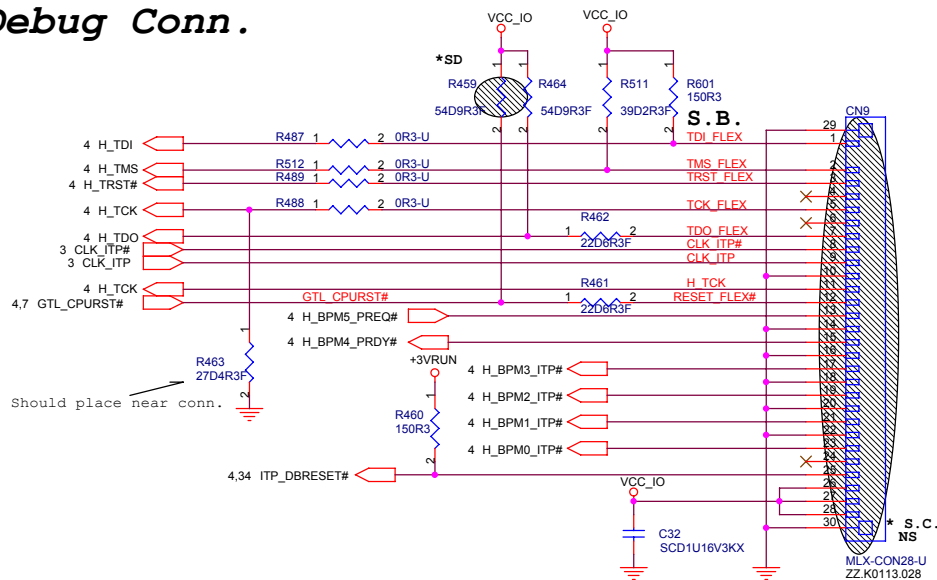
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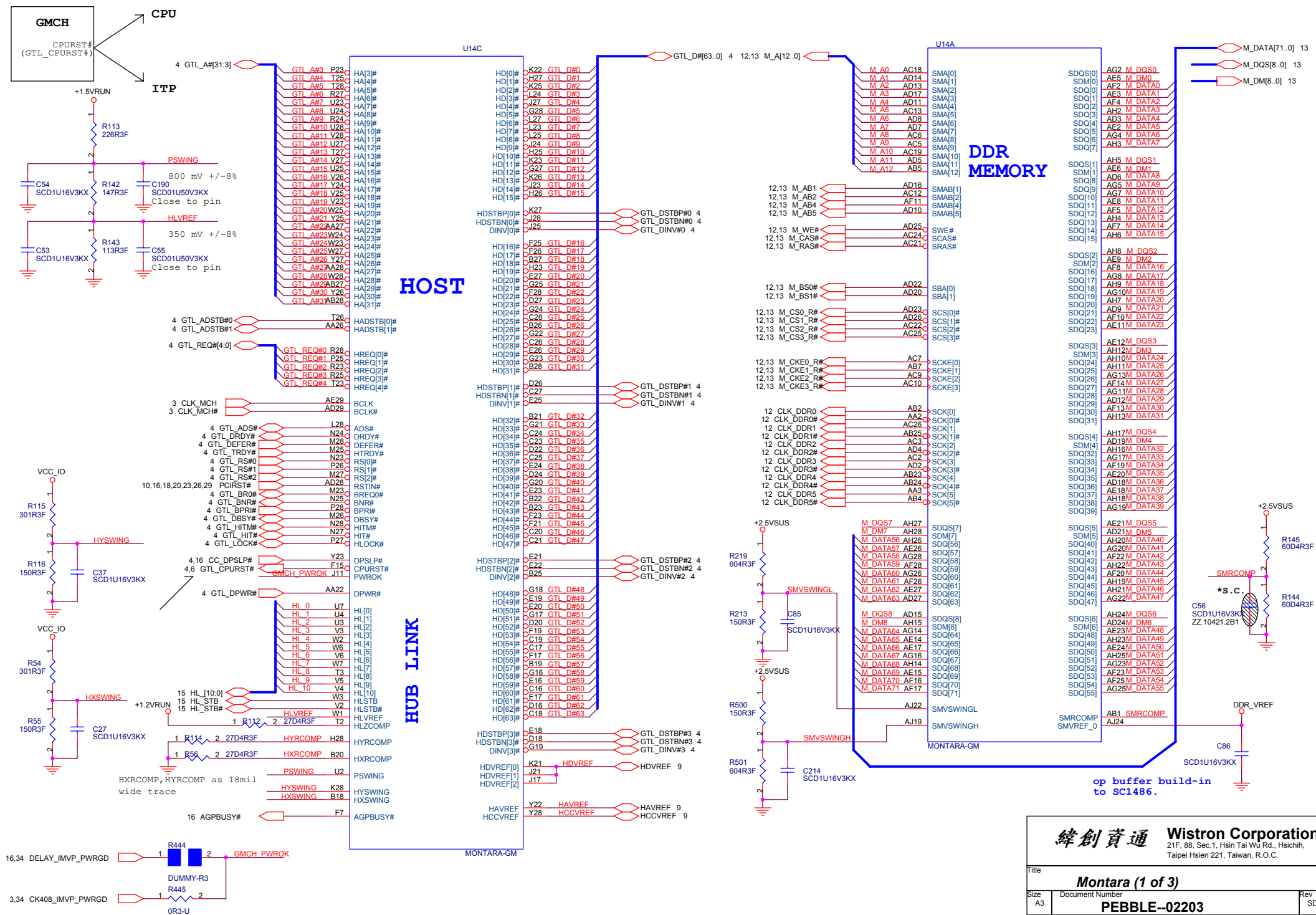


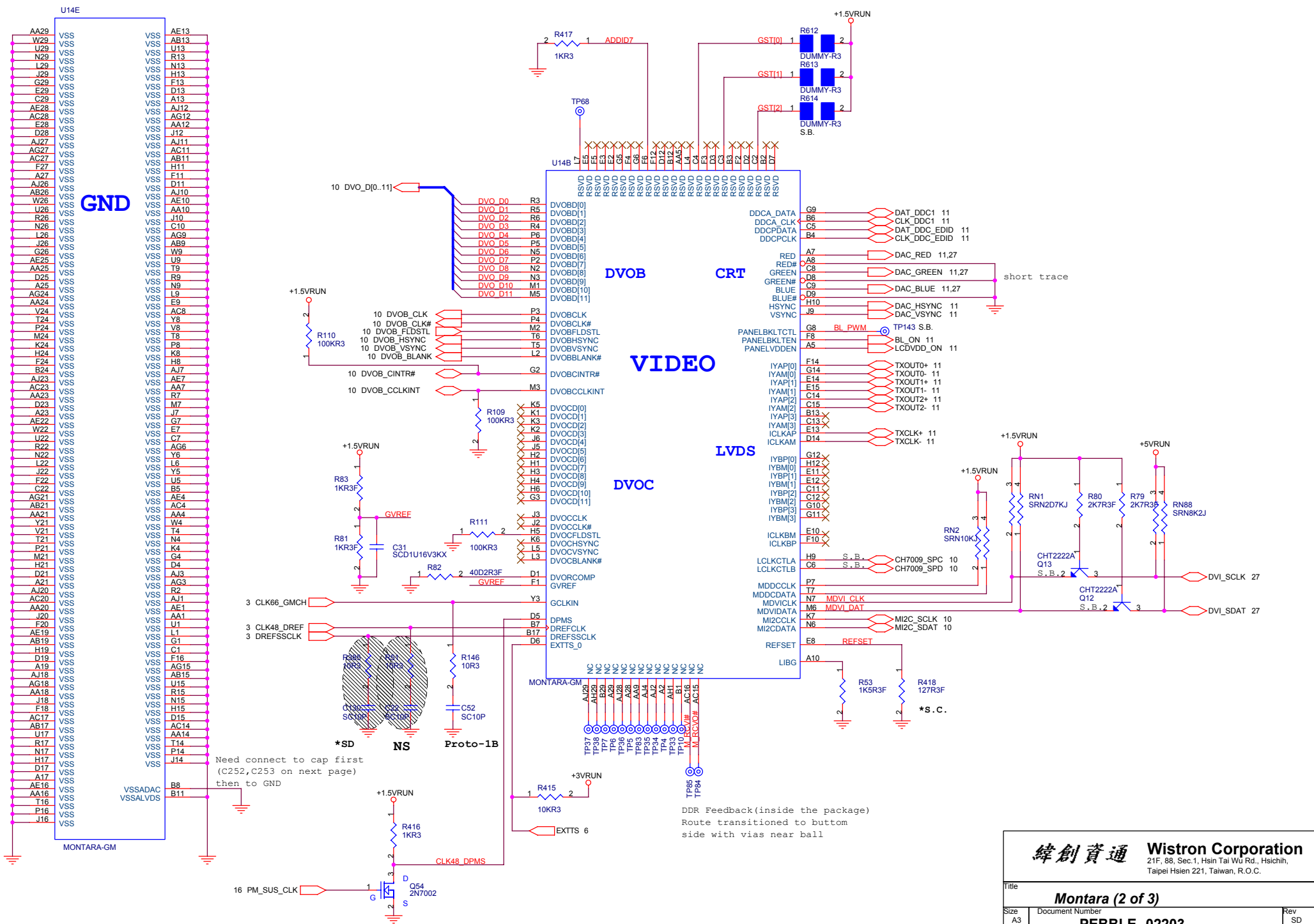
CPU FAN

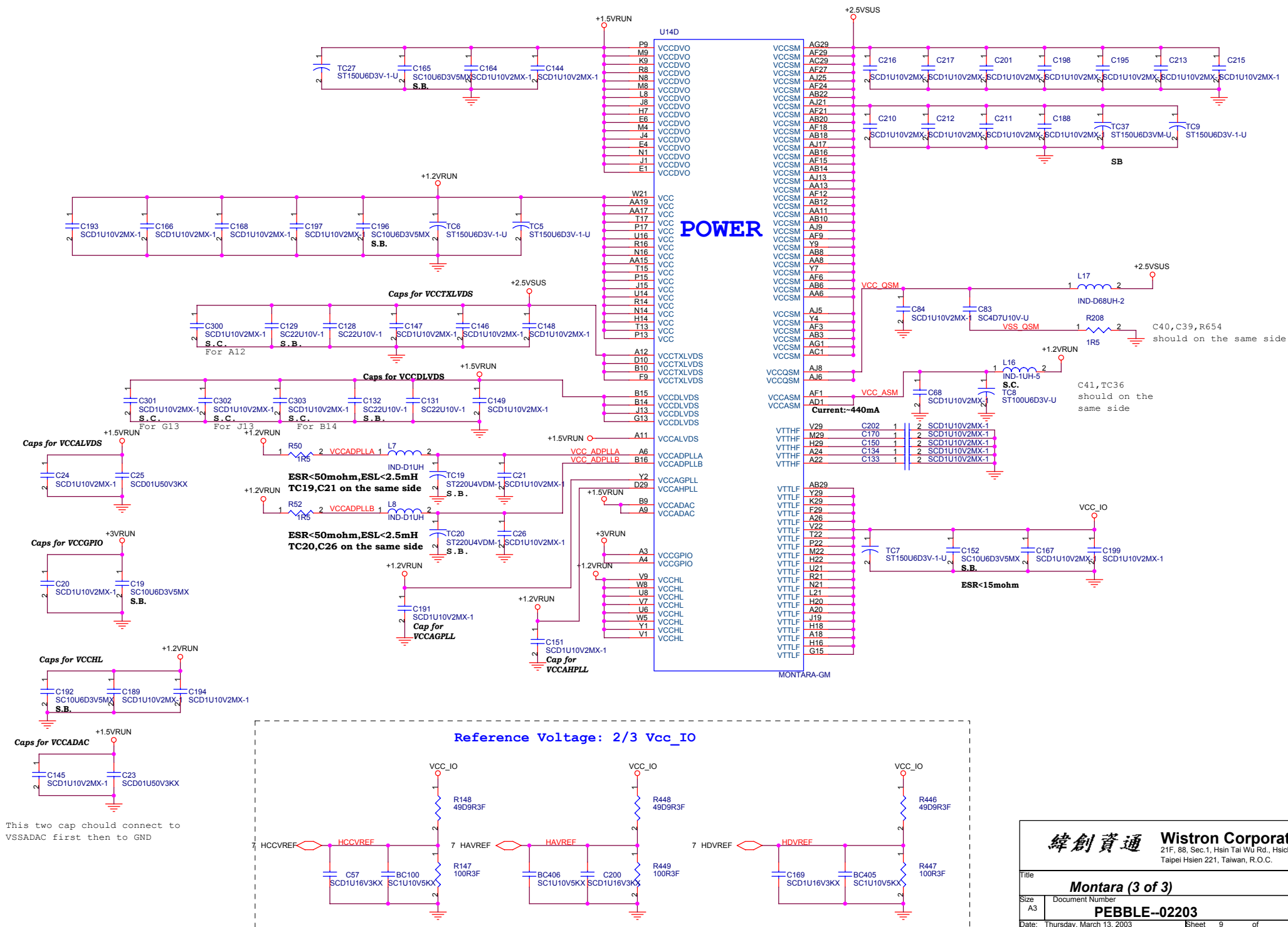


ITP Debug Conn.



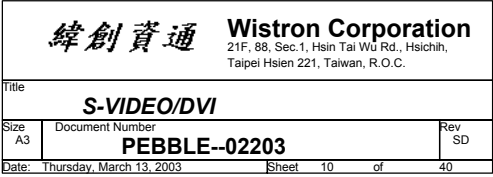




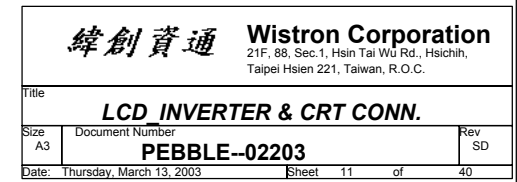
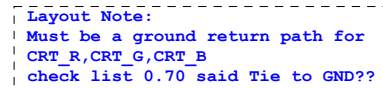


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Title		
Montara (3 of 3)		
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CRT

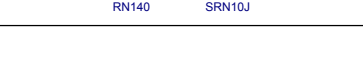
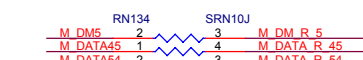
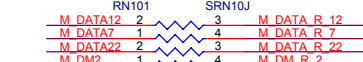
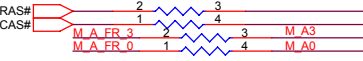
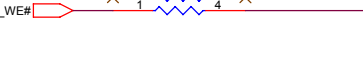
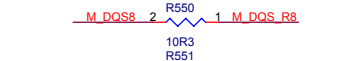
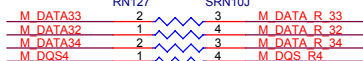
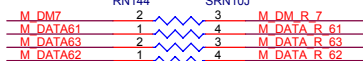
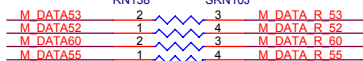
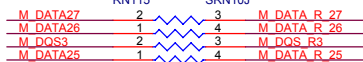
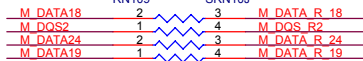
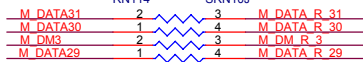
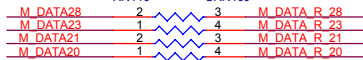
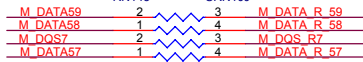
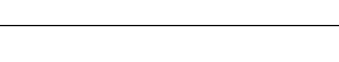
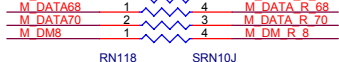
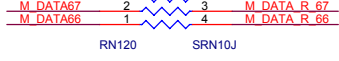
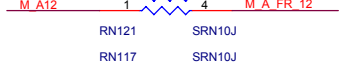
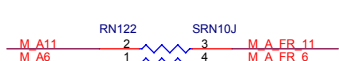
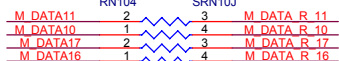
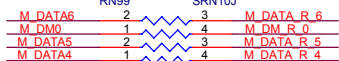
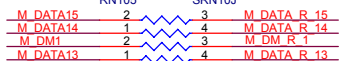
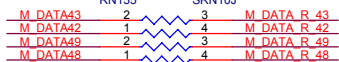
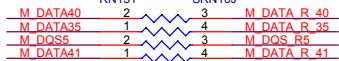
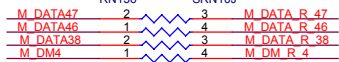
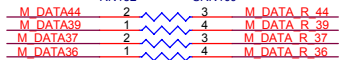
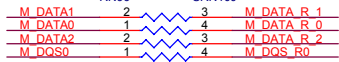
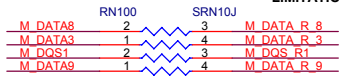


SERIES DAMPING

PLACE RNs CLOSE TO DM0, < 0.75"

STRICT EQUAL LENGTH

LIMITATION WITH DQS, CB PINS

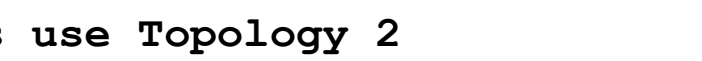
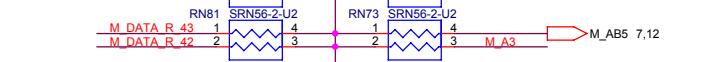
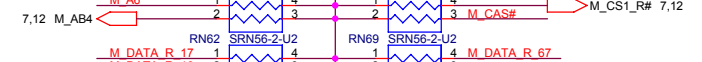
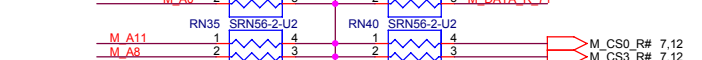
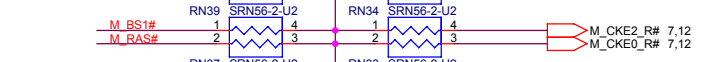
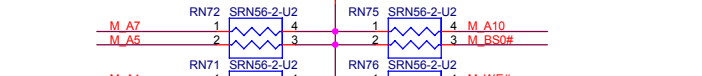
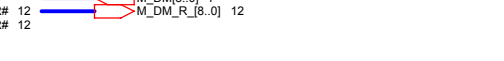
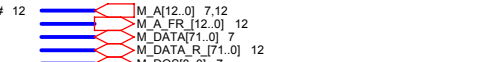
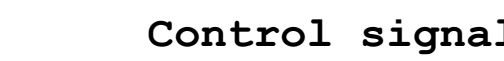


PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", Command < 0.25", PLACE

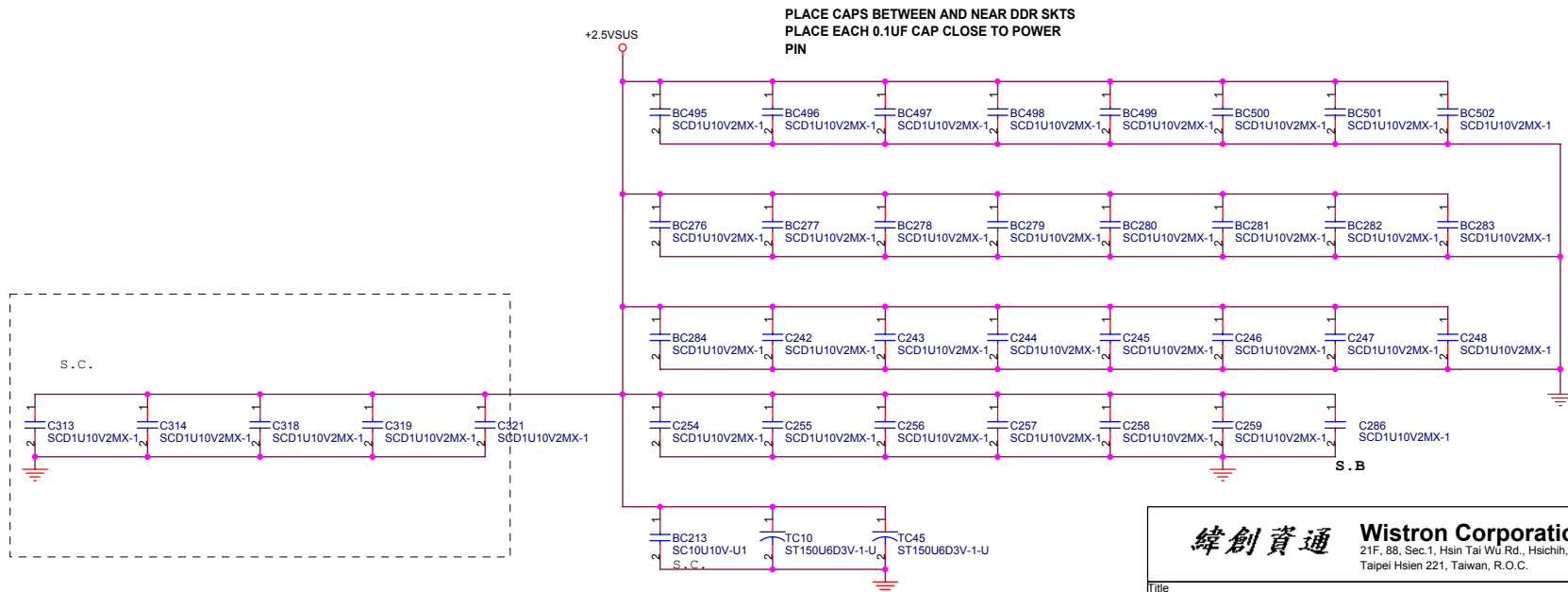
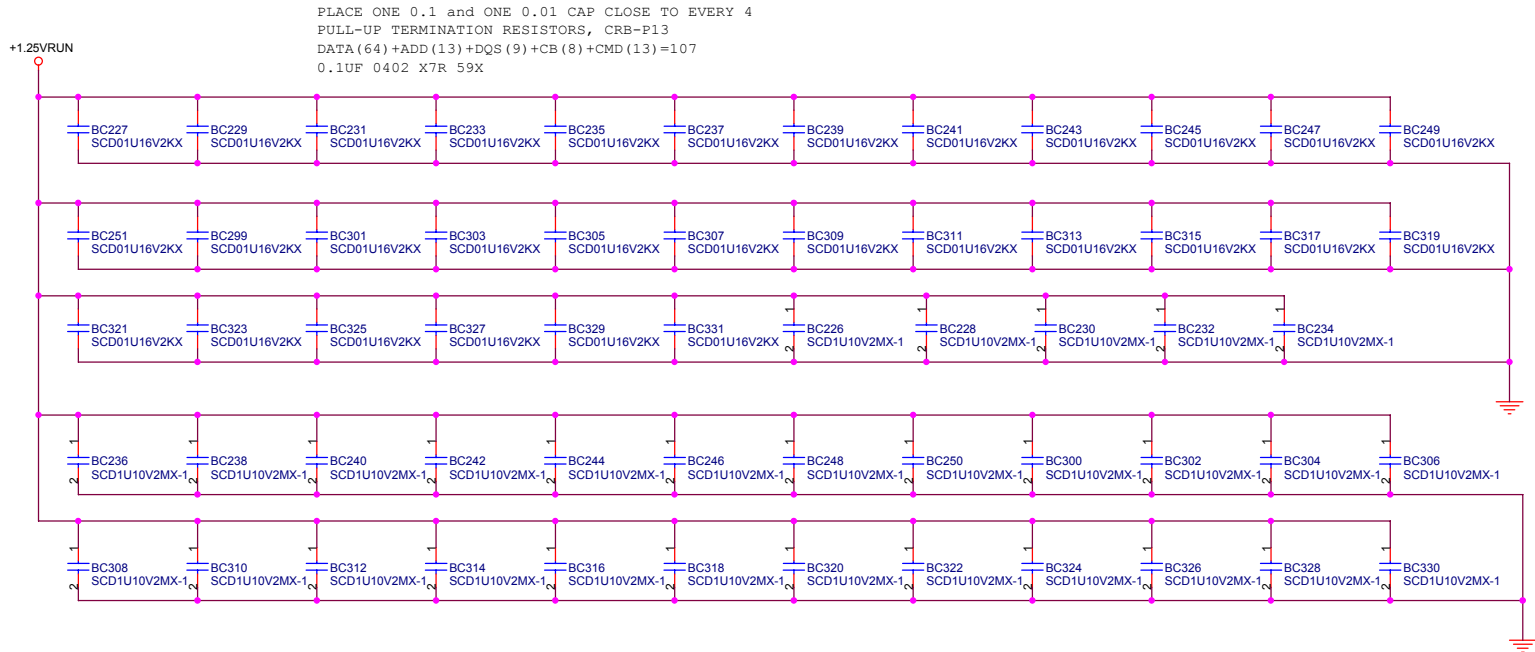
RPs CLOSE TO DM1 NO EQUAL LENGTH

LIMITATION

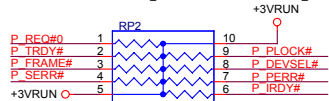


Control signals use Topology 2

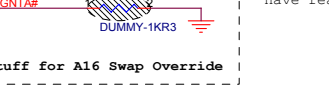
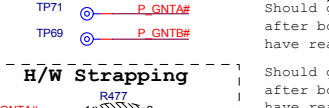
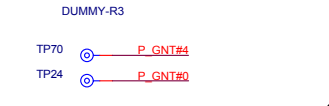
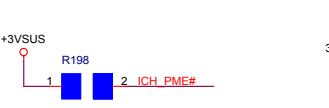
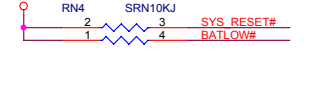
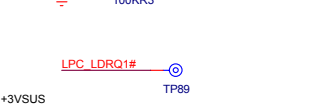
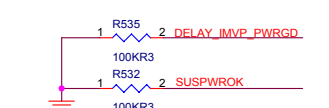
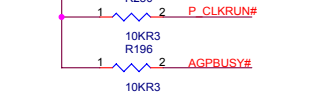
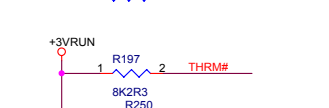
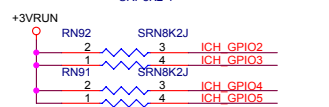
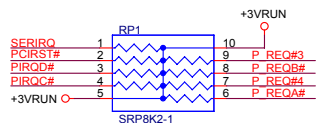
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
DDR Serial/Terminator Resistor	
Size	Document Number
A3	PEBBLE--02203
Date:	Thursday, March 13, 2003
Sheet	13 of 40



PCI/Interrupt I/F Pullups



REQ4:Broadcom LAN
REQ3:Mini PCI
REQ2:USB 2.0(No on Pebble)
REQ1:Card Bus
REQ0:Docking
REQB:PCI4515 ???



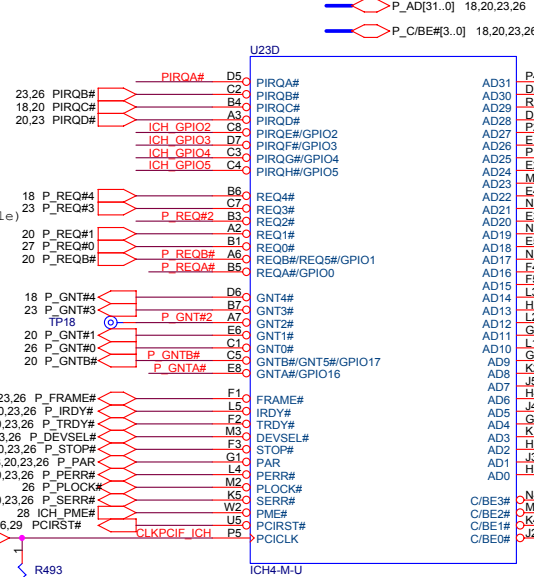
Should go high no sooner than 10ms after both +3VRUN and +1.8VRUN have reach their nominal voltage

Should go high no sooner than 10ms after both +3VSUS and +1.8VSUS have reach their nominal voltage

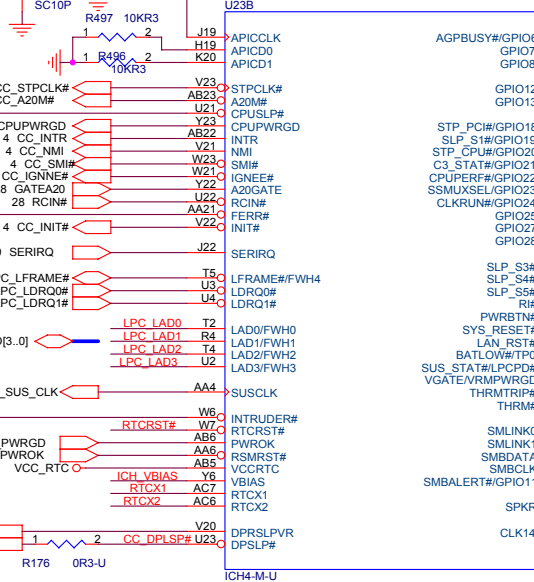
H/W Strapping



Stuff for A16 Swap Override



BIOS NOTE:
BIOS should disable PM_STPCPU# on CK_Titan.
(Use H_DPSLP# instead)



CLK termination close to ICH4

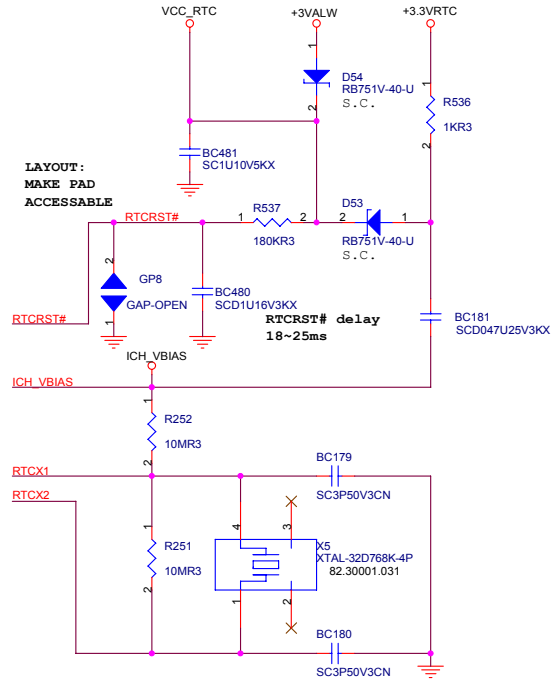


H/W Strapping



Stuff for No Reboot

RTC Circuitry



LAYOUT:
MAKE PAD
ACCESSABLE

RTCRST#

RTCRST#

RTCRST#

RTCRST#

RTCRST#

RTCRST#

RTCRST#

RTCRST#

RTCRST#

RTCRST#

RTCRST#

RTCRST#

RTCRST#

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RTCRST#

RTCRST#

RTCRST#

RTCRST#

RTCRST#

RTCRST#

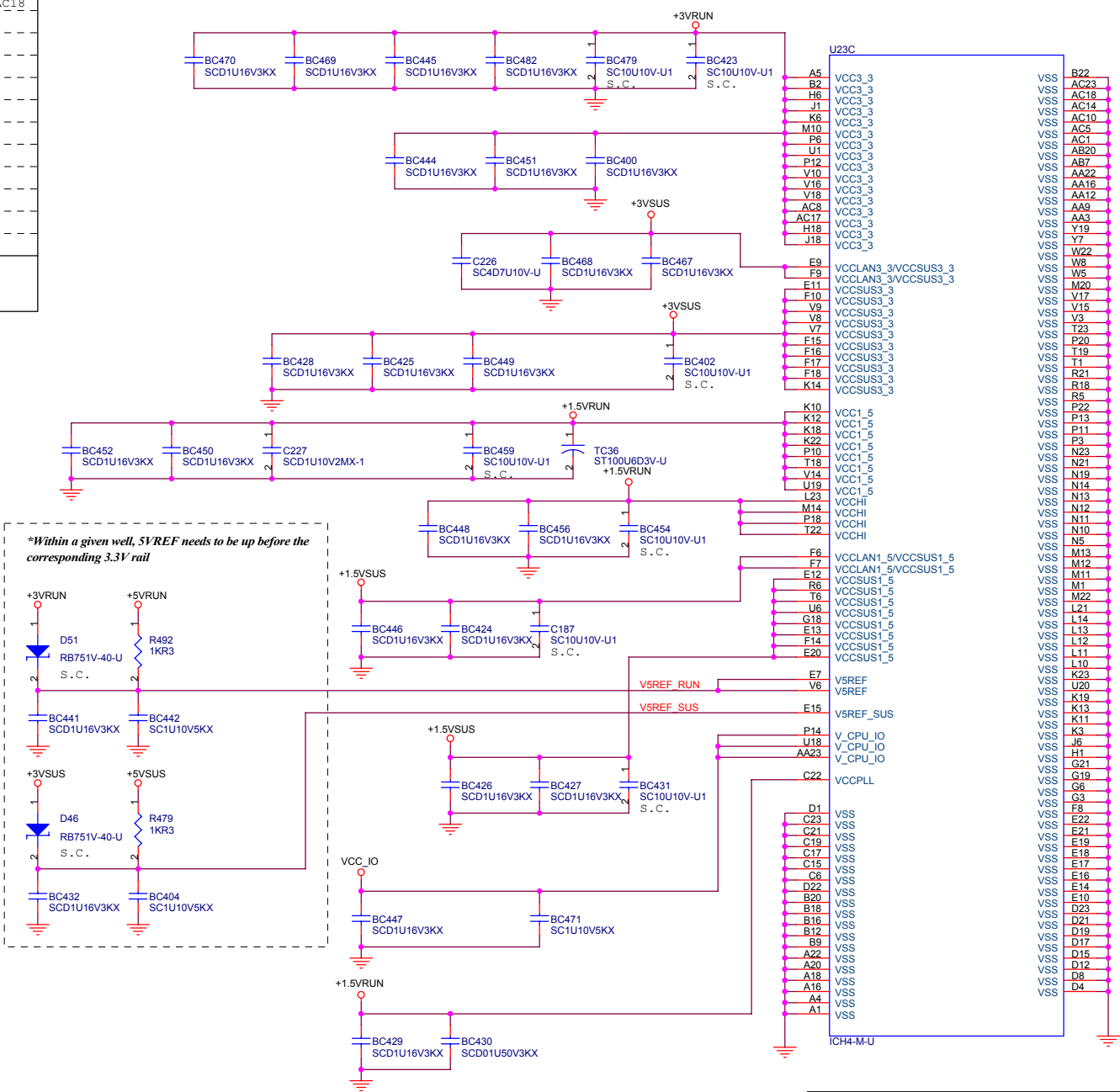
RTCRST#

RTCRST#

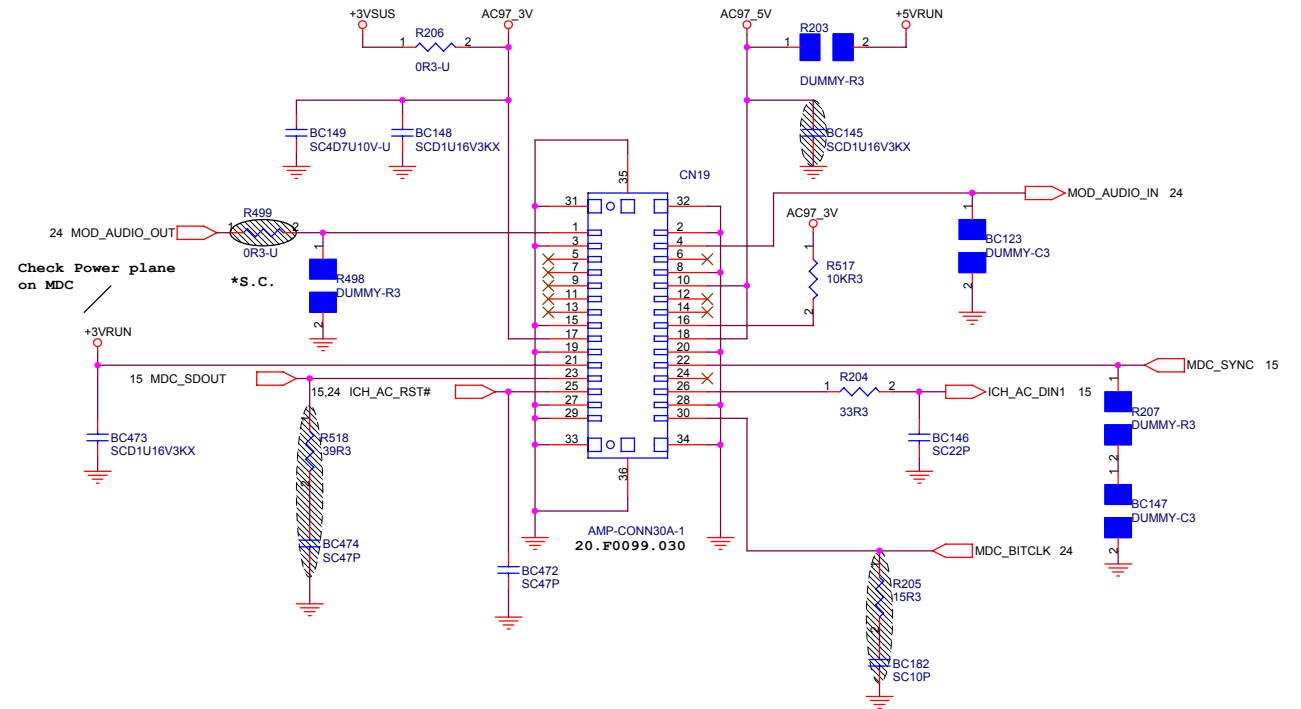
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		ICH4-M (2 of 3)	
Size	Document Number	PEBBLE--02203	
Custpm	Rev	SD	
Date: Thursday, March 13, 2003	Sheet	16	of 40

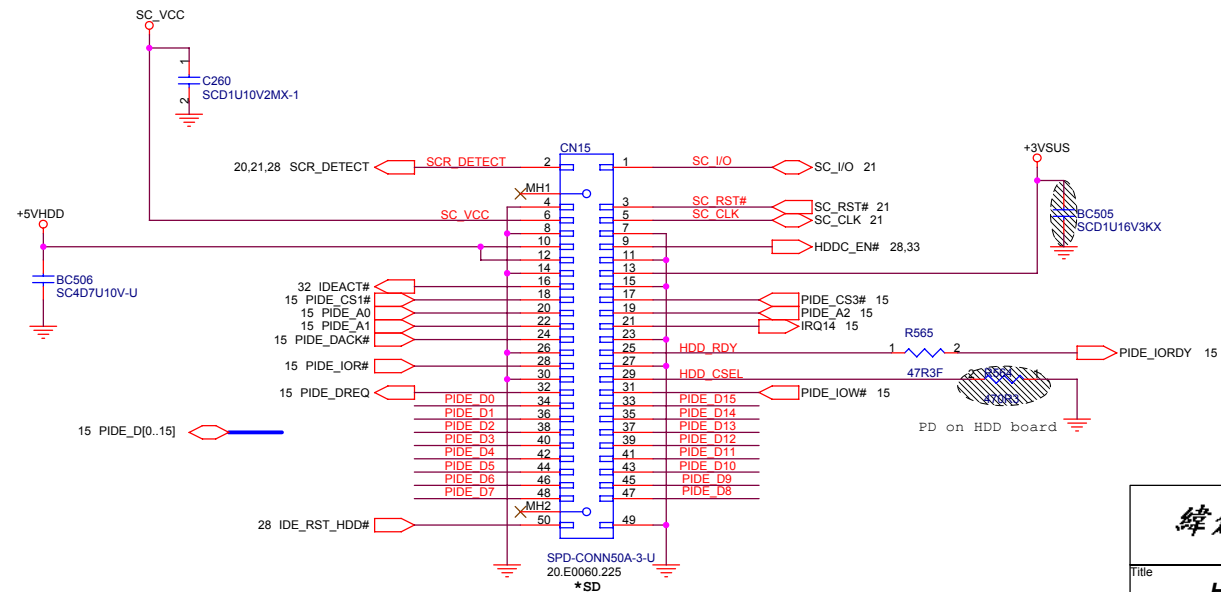
3.3VRUN	22uF*2, 0.1uF*9	0.1uF*6	A1, A4, H1, T1, AC10, AC18
1.5VRUN	100uF*1, 22uF*1, 0.1uF*4	0.1uF*2	K23, C23
3.3VSUS	22uF*1, 0.1uF*4	0.1uF*2	A22, AC5
1.5VSUS	10uF*1, 0.1uF*3	0.1uF*2	A16, AC1
1.8VRUN	22uF*1, 0.1uF*2	0.1uF*2	T23, N23
VCC_IO	1uF*1, 0.1uF*2	0.1uF*1	AA23
3.3VLAN	22uF*1, 4.7uF*1, 0.1uF*2	0.1uF*2	E9, F9
1.5VLAN	22uF*1, 0.1uF*2	0.1uF*2	E6, F7
VCCPLL	0.1uF*1, 0.01uF*1	0.1uF*1	C22
VCC5REF		0.1uF*1	E7
VCC5REFSUS		0.1uF*1	A16
VCCRTC		0.1uF*1	AB5
Intel ERB Ver.0.5 p17		Intel MGM Checklist Ver.0.7 p41	



Modem Connector



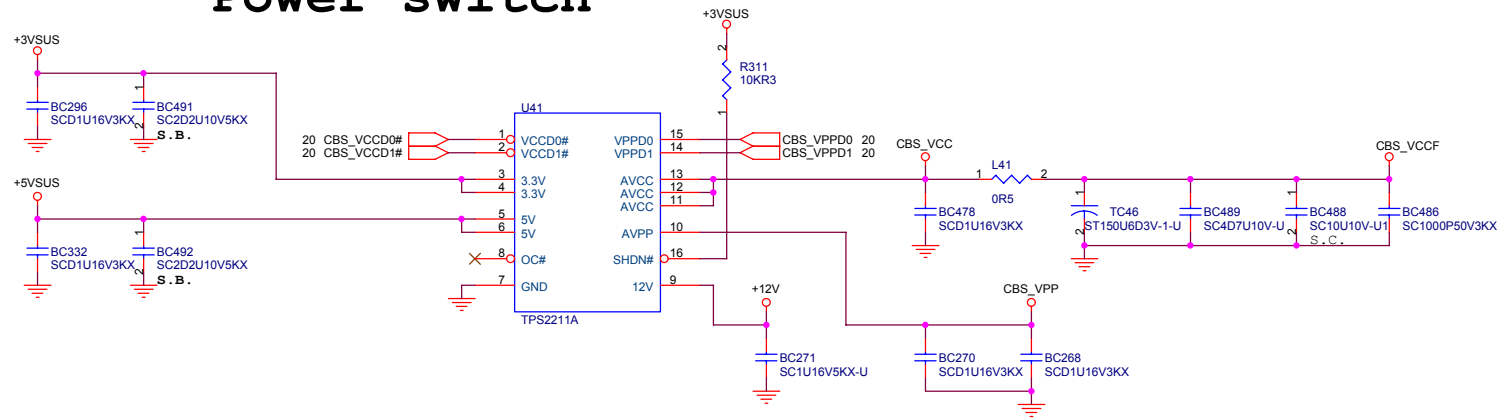
HDD & SMART CARD CONNECTOR



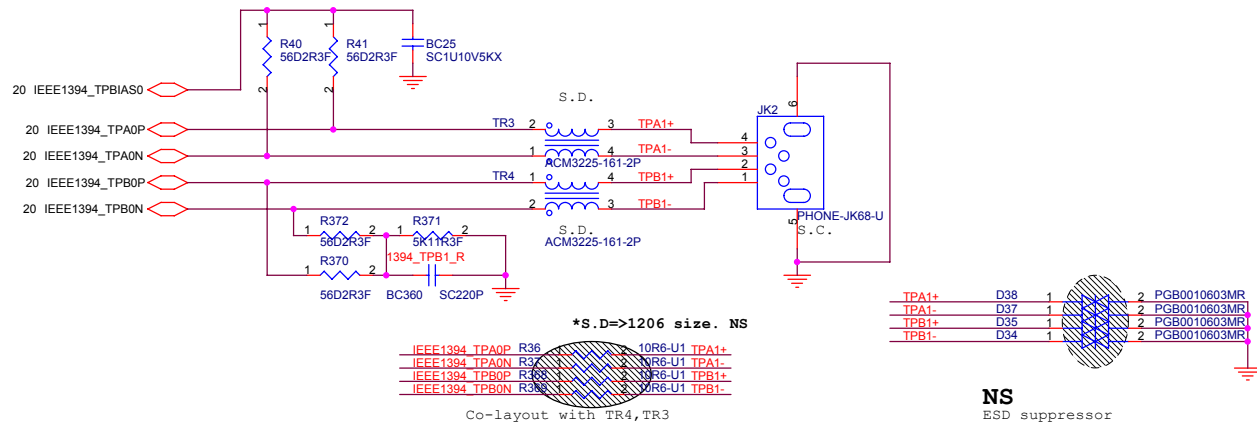
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD & MDC CONN.		
Size	Document Number	Rev
A3	PEBBLE--02203	SD
Date:	Thursday, March 13, 2003	Sheet 19 of 40

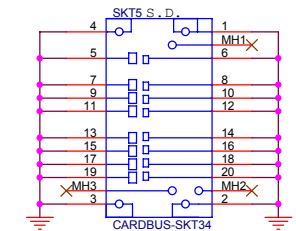
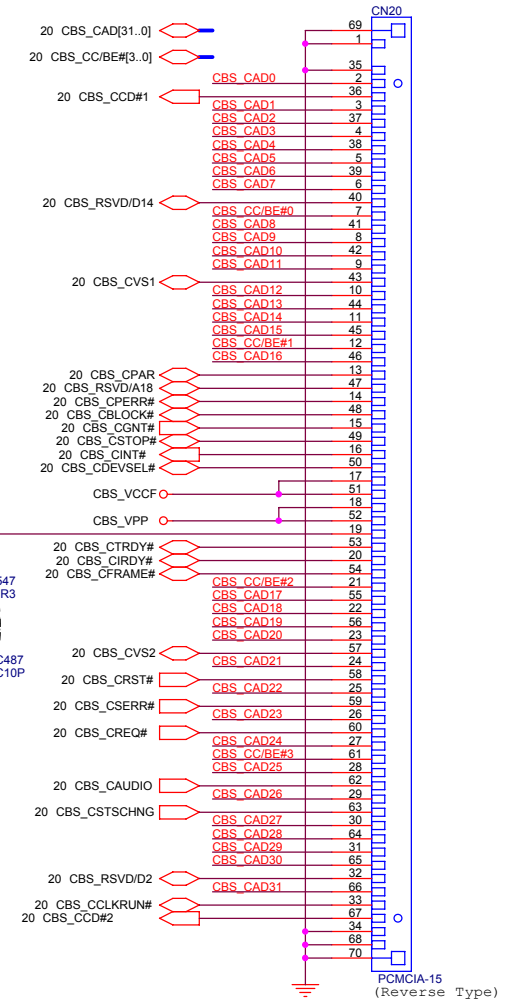
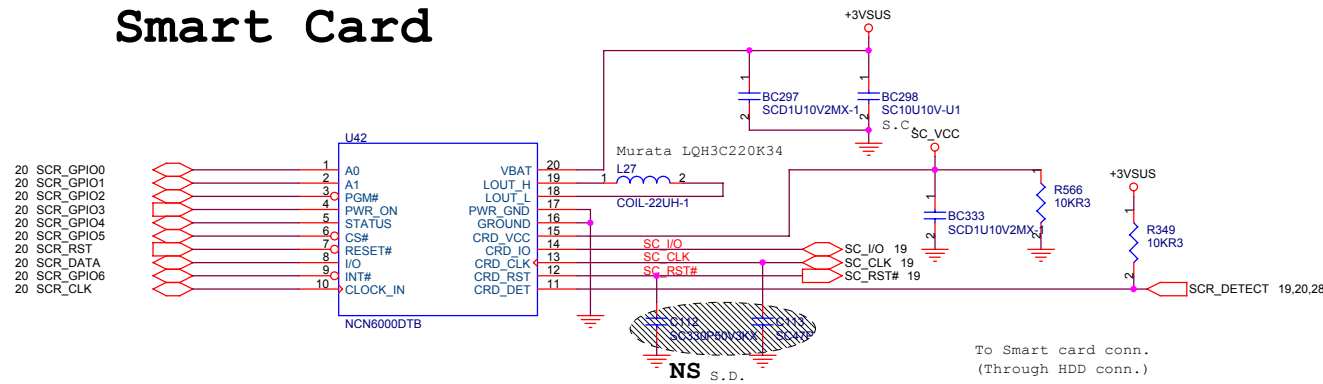
Power switch



1394 conn.



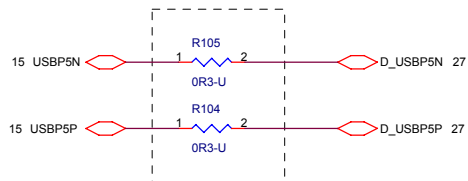
Smart Card



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Title			
CARDBUS CONNECTOR & POWER SWITCH			
Size	Document Number	Rev	
A3	PEBBLE--02203	SD	
Date:	Thursday, March 13, 2003	Sheet	21 of 40

TO D DOCK

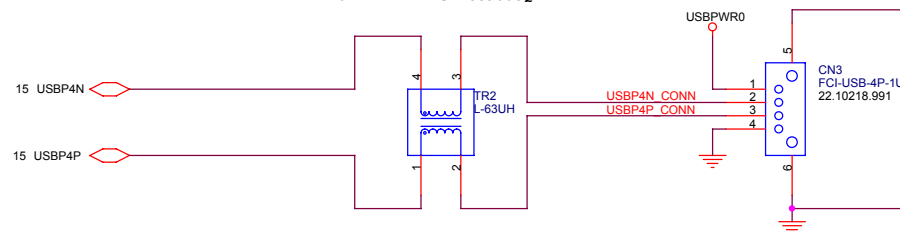


ICH4 provides an output driver impedance of 45 Ohm and integrates 15K Ohm Pull-down R

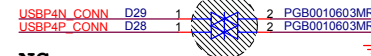
*SE

USB Port#	Destination
0	
1	BlueTooth
2	
3	Power USB
4	Rear
5	D-Dock

USB Common mode choke
MURATA PLW3216S900SQ2

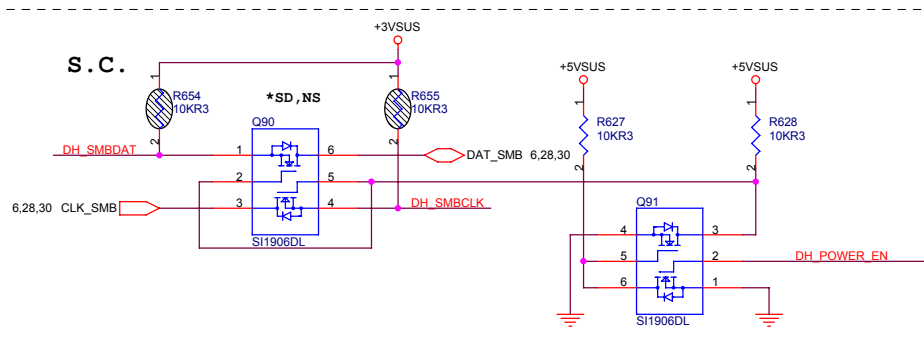
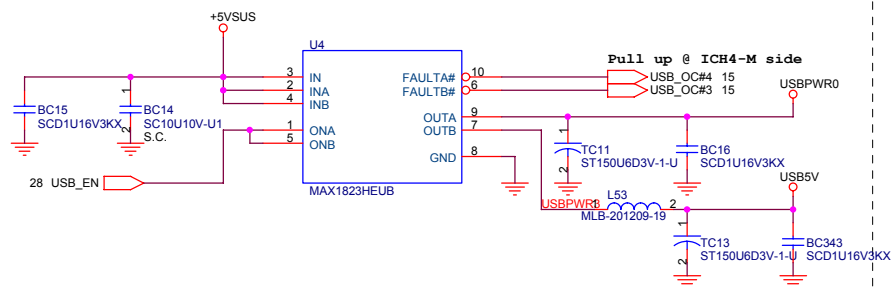


USB Common mode choke
MURATA PLW3216S900SQ2



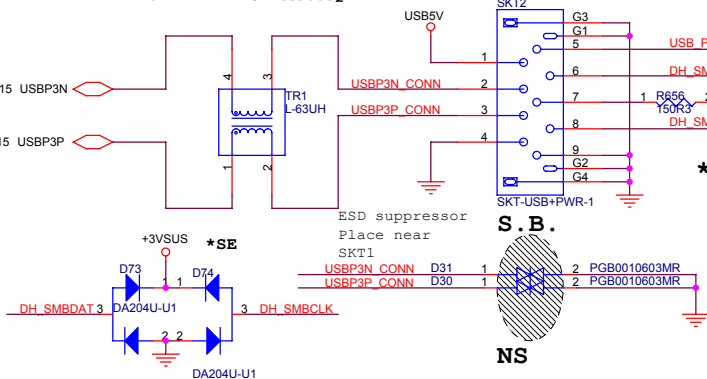
NS
ESD suppressor
Place near
CN9&10

Dual USB switch for USB0/Power USB

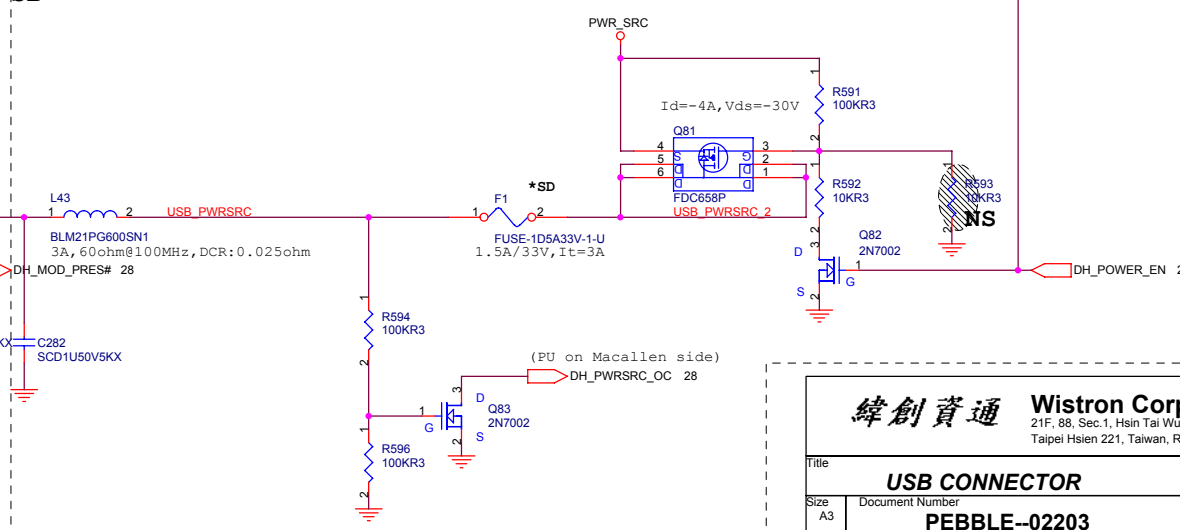


POWER USB

USB Common mode choke
MURATA PLW3216S900SQ2



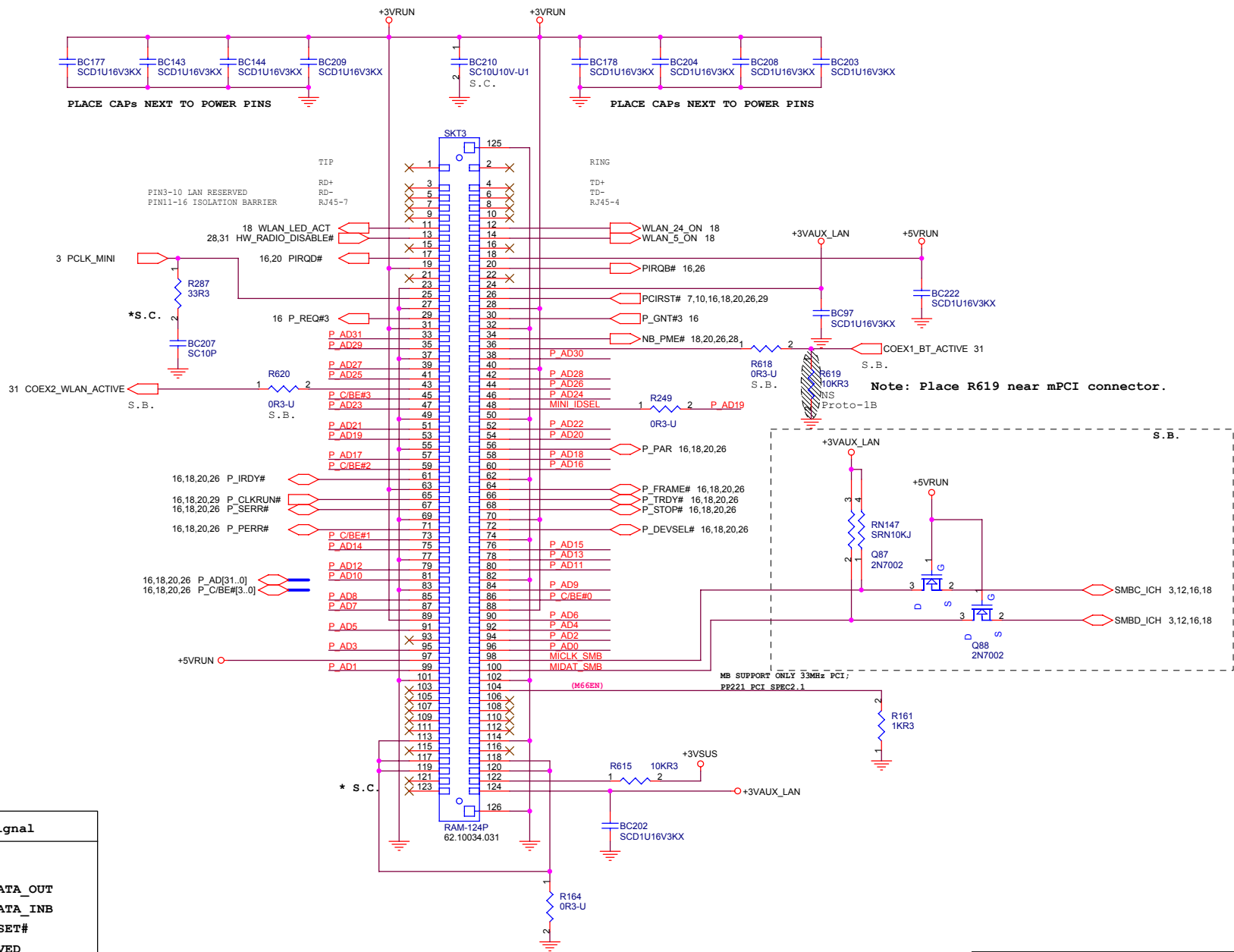
SB



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Title USB CONNECTOR		
Size A3	Document Number PEBBLE--02203	Rev SE
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MINIPCI SLOT



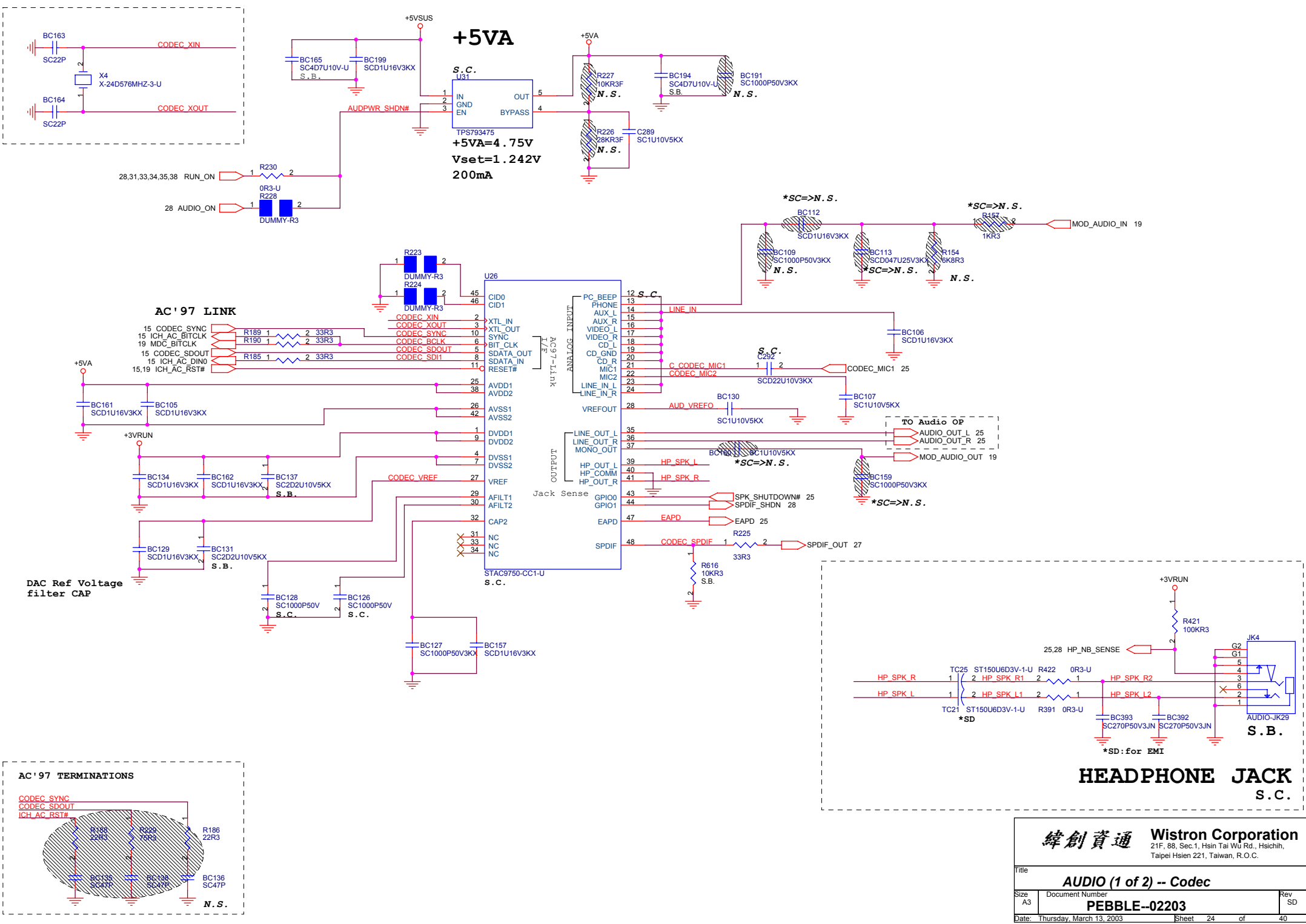
MINIPCI SPEC.

Pin#	Signal	Pin#	Signal
101	GND	102	GND
103	AC_SYNC	104	M66EN
105	AC_SDATA_INA	106	AC_SDATA_OUT
107	AC_BIT_CLK	108	AC_SDATA_INB
109	AC_PRIMARY#	110	AC_RESET#
111	MOD_AUDIO_MON	112	RESERVED
113	AUDIO_GND	114	GND
115	SYS_AUDIO_OUT	116	SYS_AUDIO_IN
117	SYS_AUDIO_OUT_GND	118	SYS_AUDIO_IN_GND
119	AUDIO_GND	120	AUDIO_GND
121		122	MPCIACT#
123	VCC5A	124	3.3VAUX

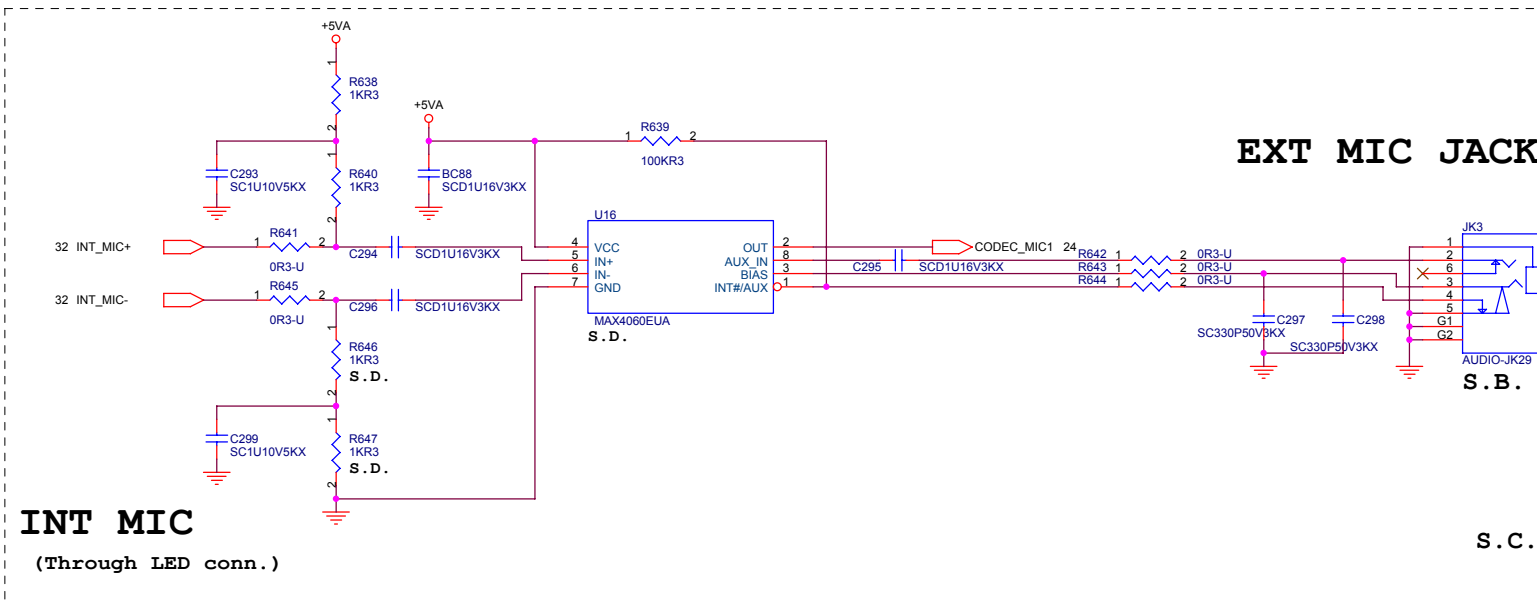
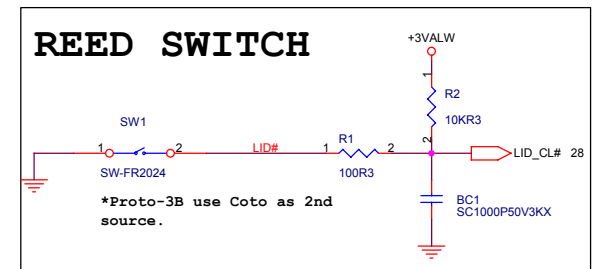
POWER REQUIREMENT TOTAL = 2W
+5VRUN = 100 mA
+3VAUX = 375 mAMPMAX

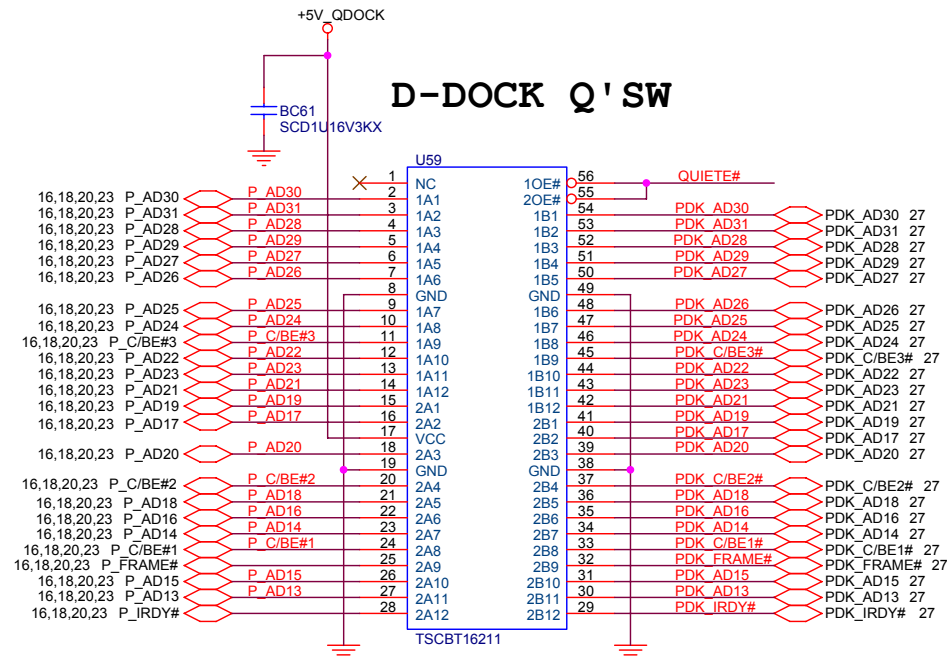
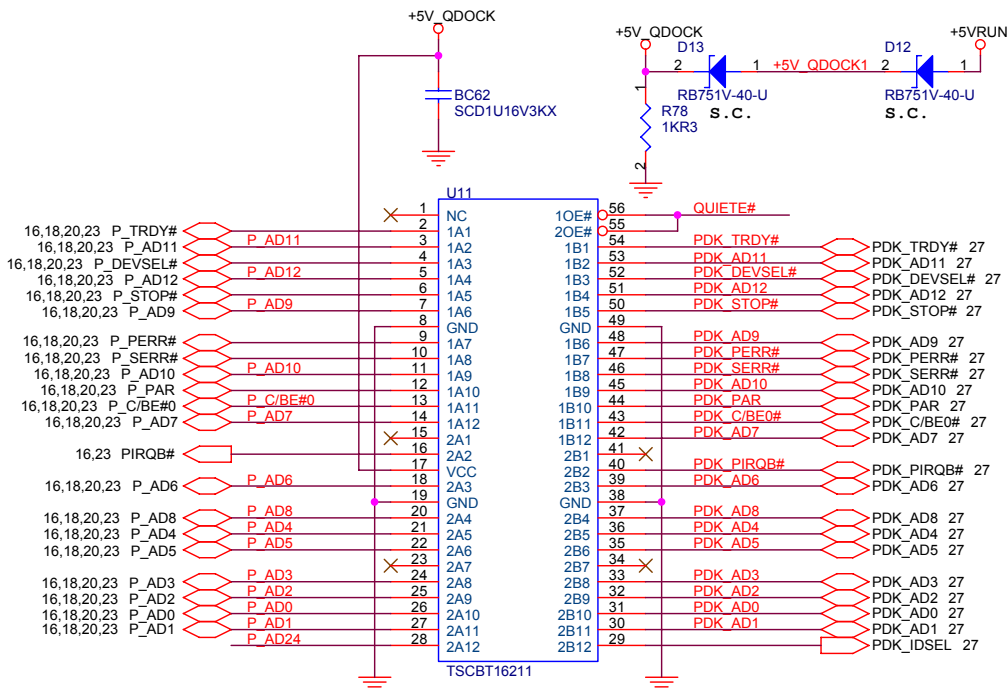
緯創資通Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

TitleMini-PCI CONNECTOR
Size A3Document NumberPEBBLE--02203
Date: Thursday, March 13, 2003Sheet 23 of 40

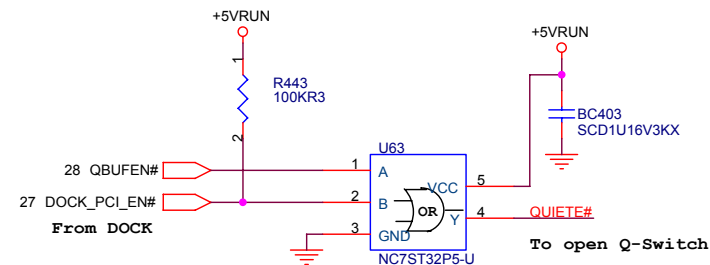
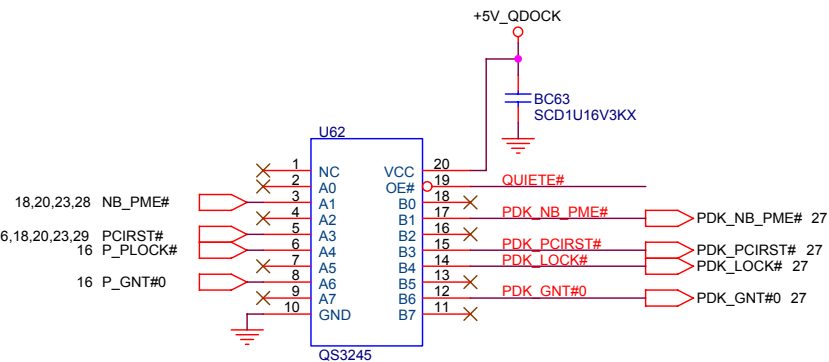


Title			
AUDIO (2 of 2) --Phone Jack			
Size A3	Document Number PEBBLE--02203		Rev SD
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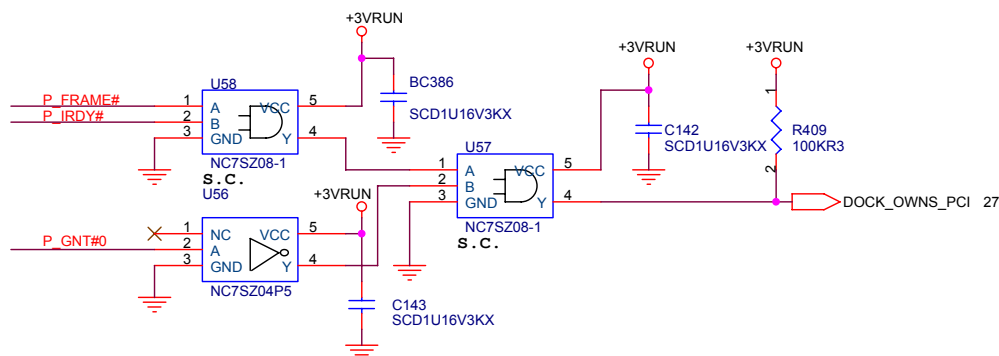


D-DOCK Q' SW



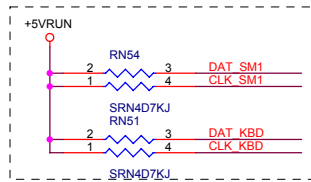
Dock on sequence

- * BIOS requests through SMB to connect to PCI bus in the dock
- * D-dock state machine generates REQ 0
- * ICH4 generates GNT0
- * Notebook waits for next Idle bus cycle (IORDY# and FRAME#)
- * DOCK_QWNS_PCI is generated
- * on rising edge of PCI clock REQ0 is deasserted and DOCK_PCI_EN# is asserted
- * now Q-switch is enabled and PCI goes through to the dock
- * D-dock reports connection through SMB
- * re-enumeration is done by BIOS



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Title		
D Dock Buffer		
Size	Document Number	Rev
Custom	PEBBLE--02203	SD
Date: Thursday, March 13, 2003	Sheet 26	of 40



PS/2 I/F Pull-ups

To D-DOCK PS/2 (KB)

To Touchpad CONN

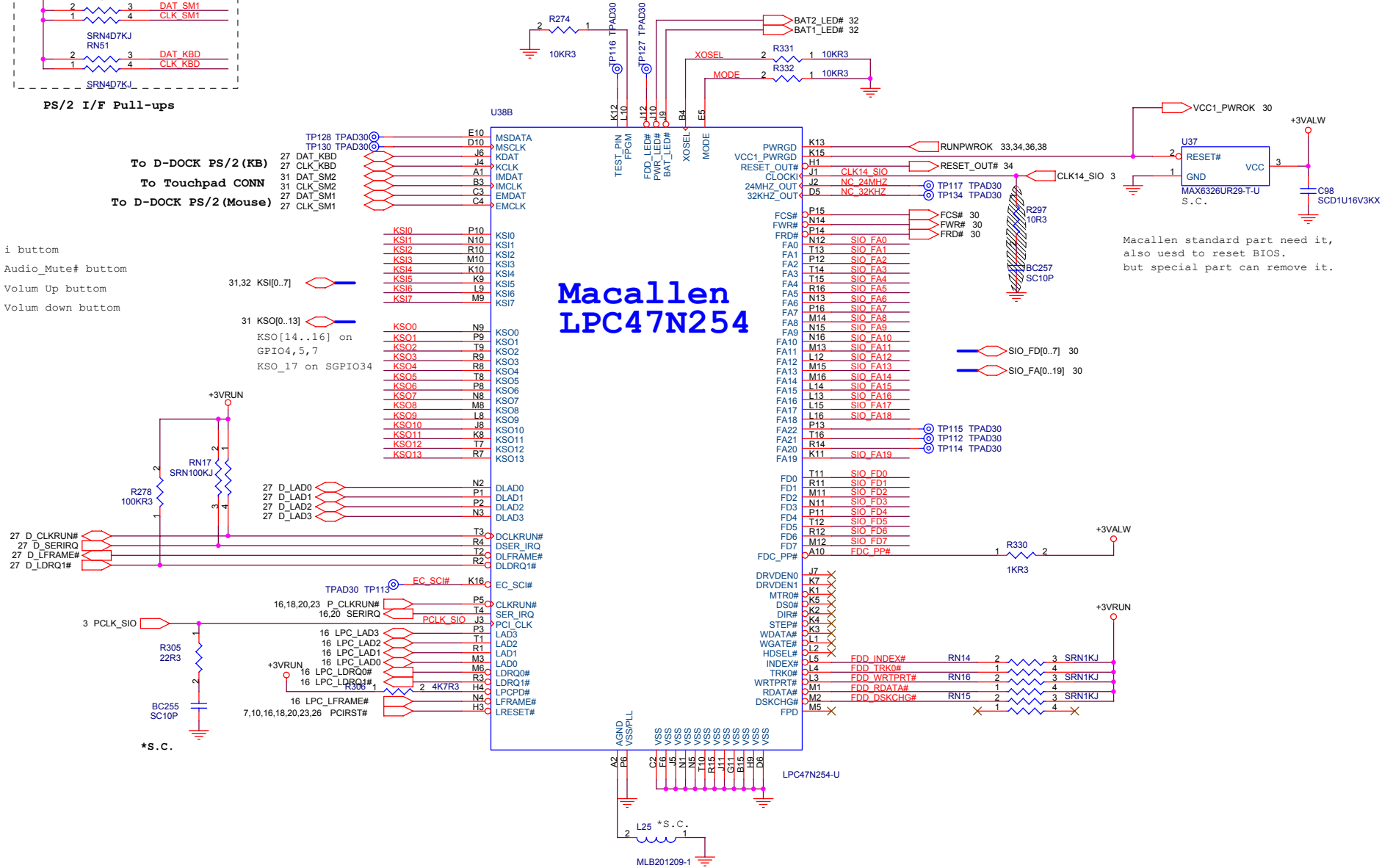
To D-DOCK PS/2 (Mouse)

KSO_17 and KSI0 for i button

KSO_17 and KSI6 for Audio_Mute# button

KSO_17 and KSI4 for Volum Up button

KSO_17 and KSI5 for Volum down button

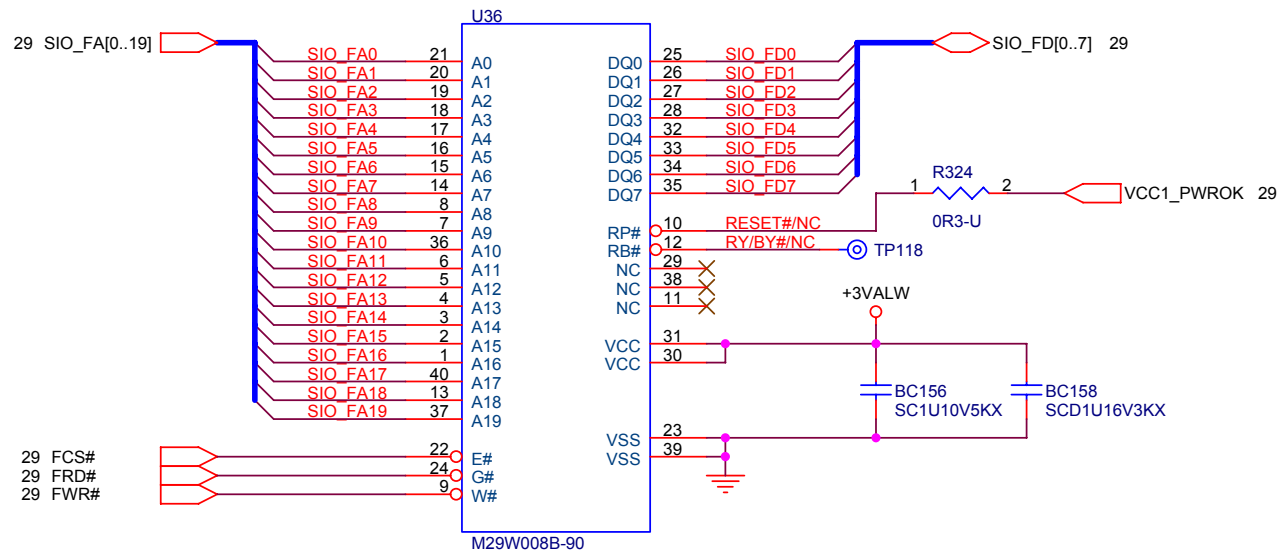


Macallen standard part need it,
also used to reset BIOS.
but special part can remove it.

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Taipei Hsien 221, Taiwan, R.O.C.

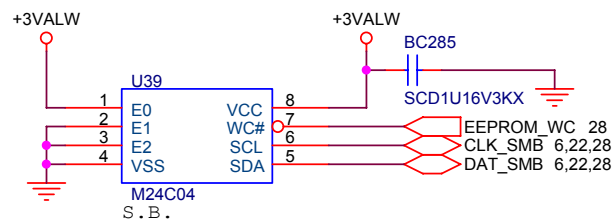
Title		
Macallen (2 of 2)		
Size	Document Number	Rev
A3	PEBBLE--02203	SD
Date:	Thursday, March 13, 2003	Sheet 29 of 40

8Mbit(1M Byte),No PLCC type



SMBus address A2

User Password



緯創資通

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Title

BIOS

Size
A4

Document Number

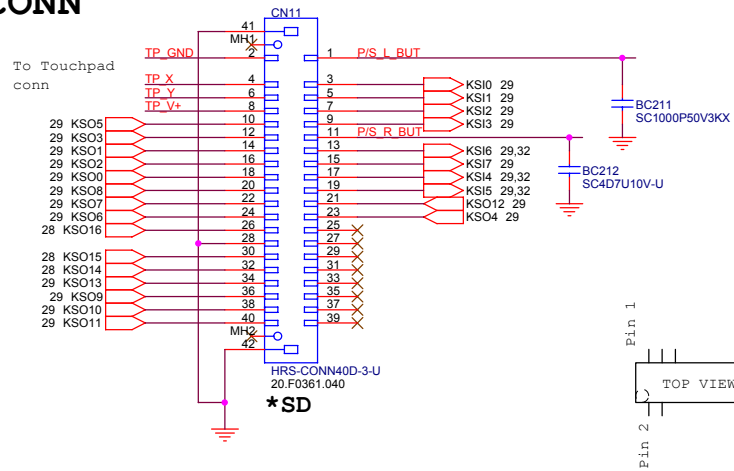
PEBBLE--02203

Rev
SD

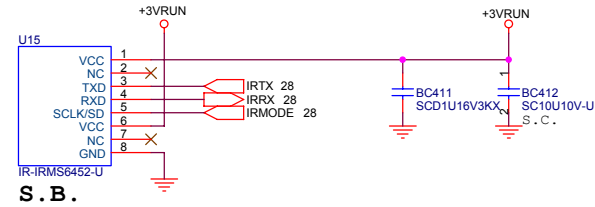
Date: Thursday, March 13, 2003

Sheet 30 of 40

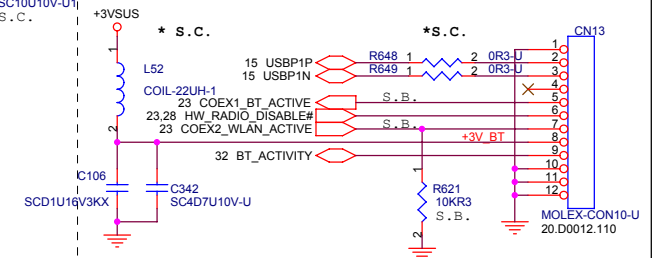
KB CONN



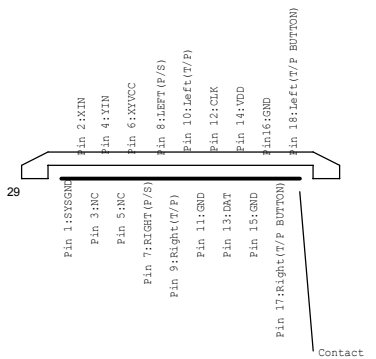
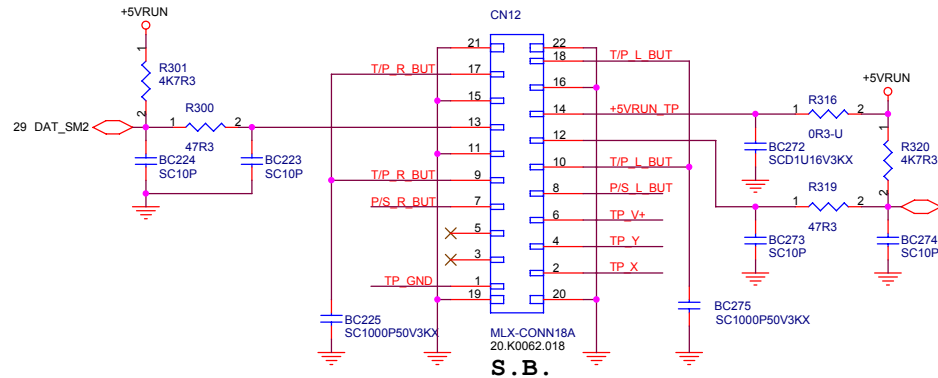
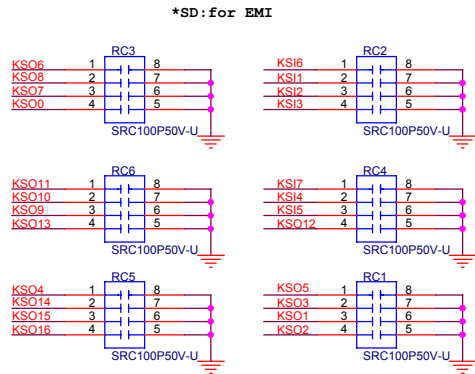
FIR



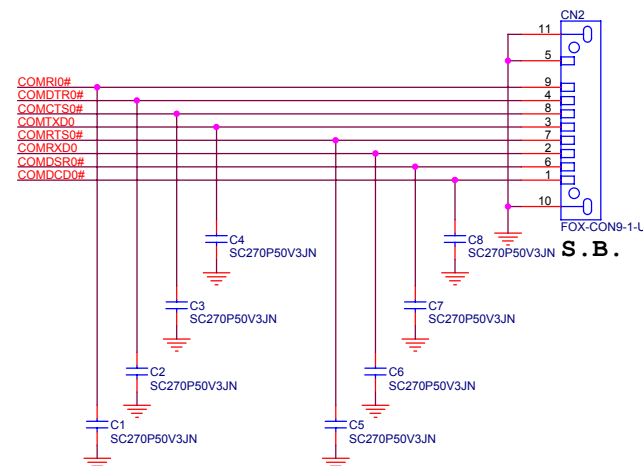
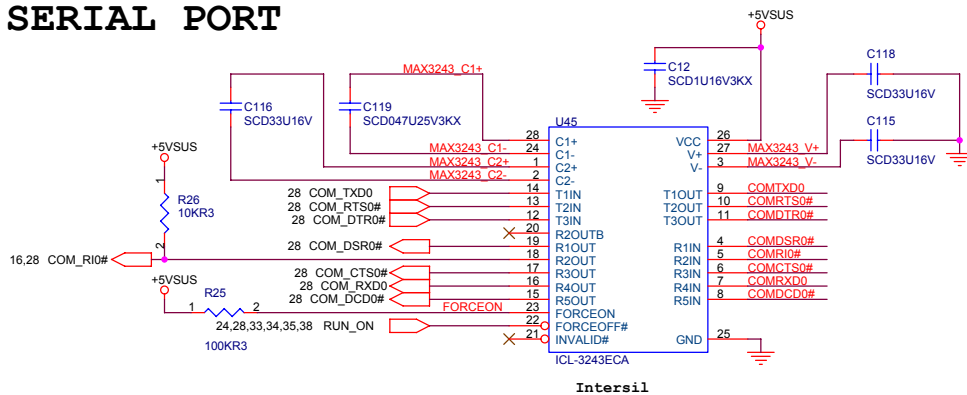
Bluetooth Module conn.



Note: Place R621 near CN13.



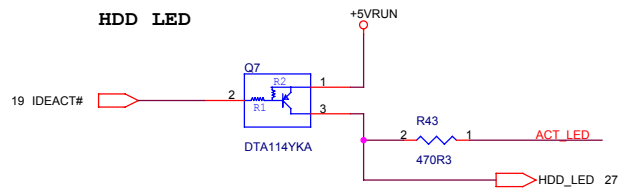
SERIAL PORT



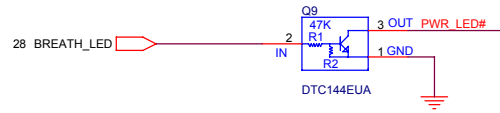
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<i>T/P,KB Connector & IrDA</i>			
Size	Document Number	Rev	
A3	PEBBLE--02203	SD	
Date:	Thursday, March 13, 2003	Sheet	31 of 40

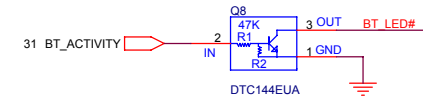
HDD LED



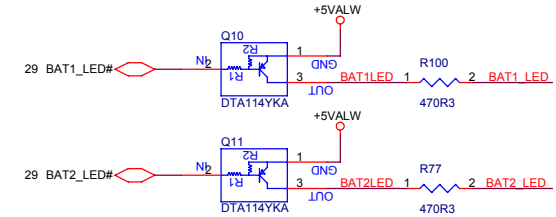
POWER LED



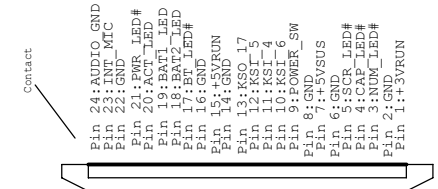
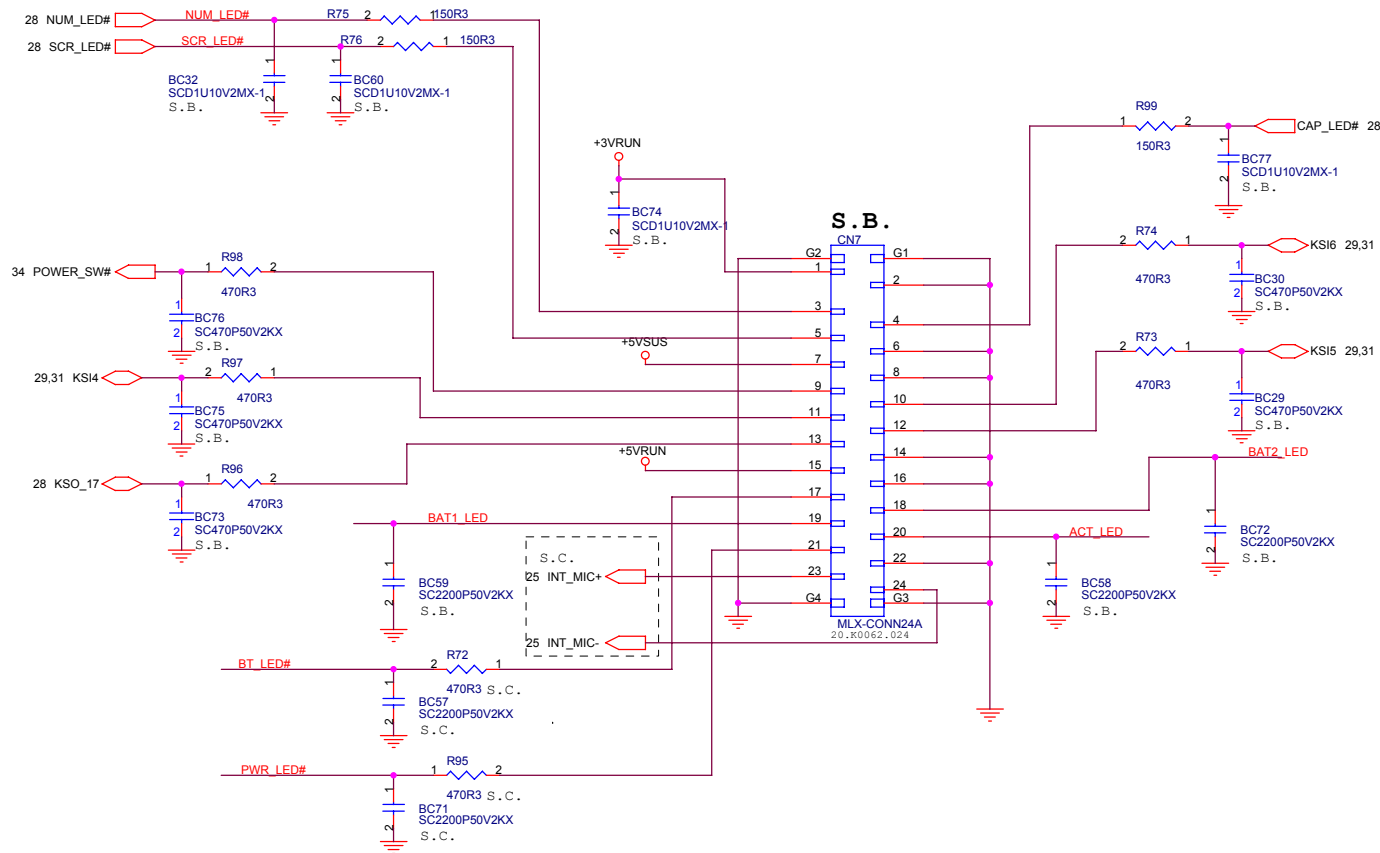
BLUETOOTH LED



BATTERY LED

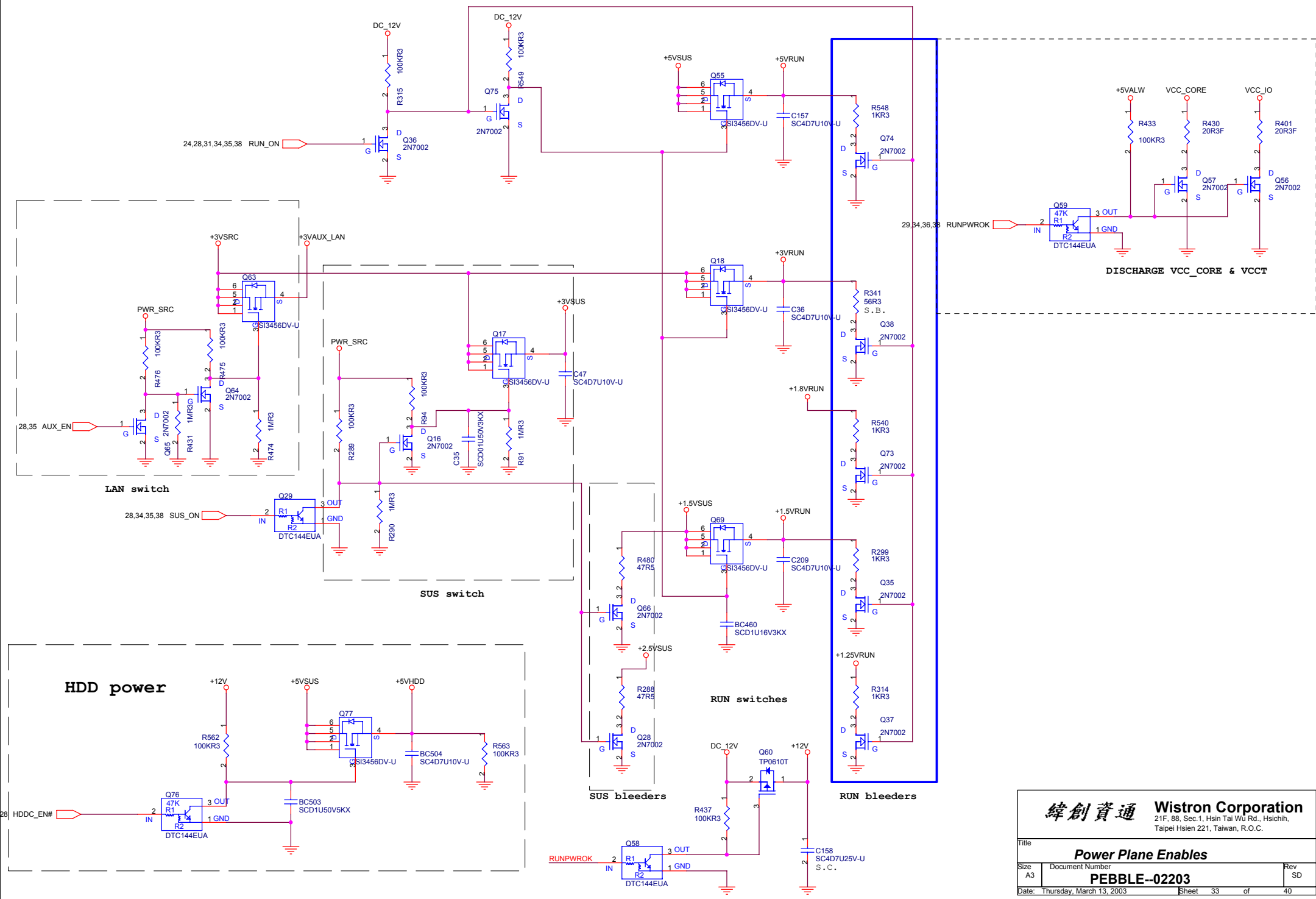


LED & BUTTON BD CONN



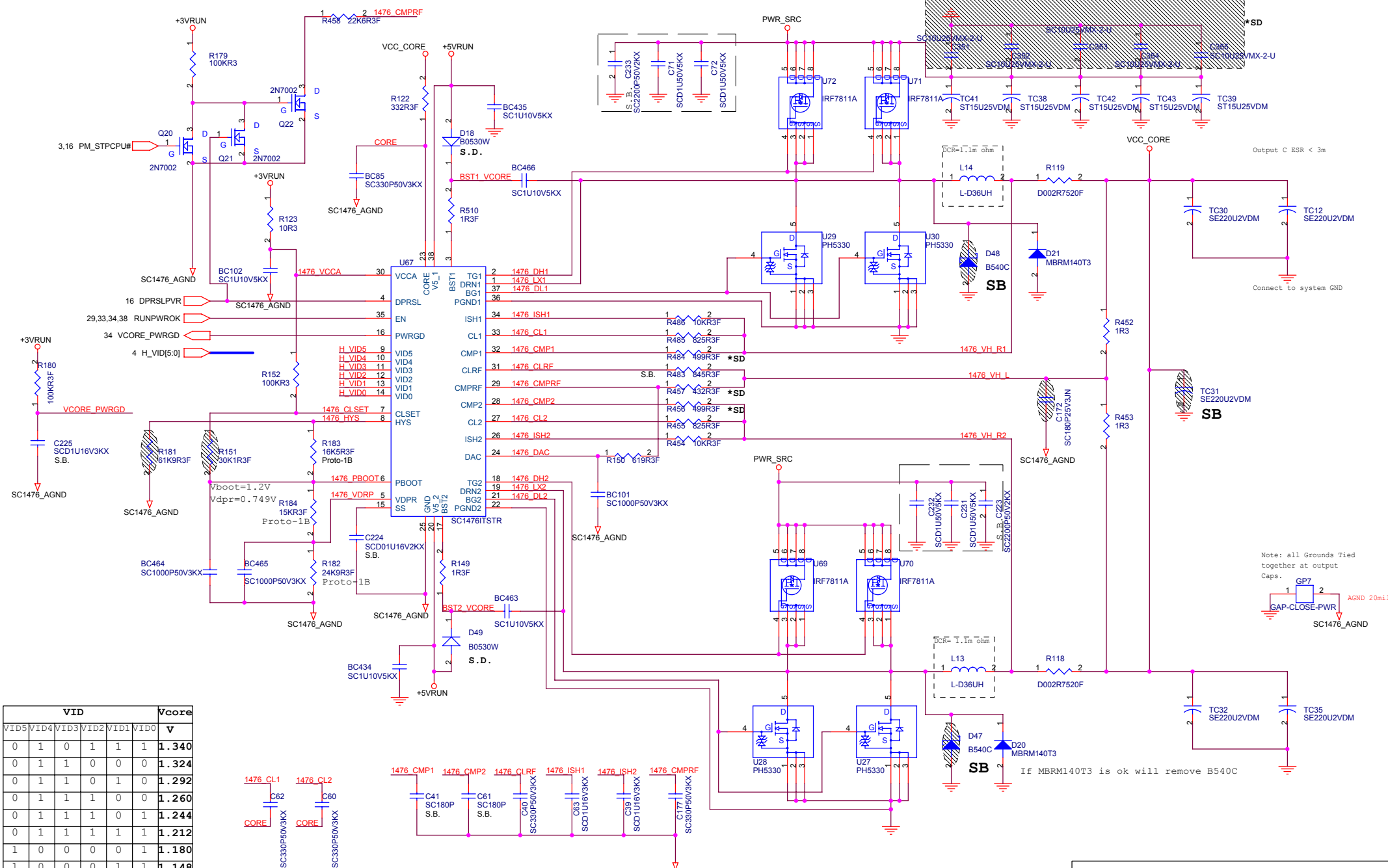
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			LED Button FPC Connector	
Size	A3	Document Number	PEBBLE--02203	
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Title		
Power Plane Enables		
Size	Document Number	Rev
A3	PEBBLE--02203	SD
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VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

10 mil Trace list for layout

PIN4
PIN5
PIN7
PIN25
PIN30

20 mil Trace list for layout

The +5VRUN (PIN38 and PIN20)
BST1_VCORE
BST2_VCORE

100 mil Trace list for layout

1476_DH1
1476_LX1
1476_DL1
1476_DH2
1476_LX2
1476_DL2

緯創資通

Wistron Corporation

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Title

CPU CORE--IMVP4

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A3

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Thursday, March 13, 2003

Sheet

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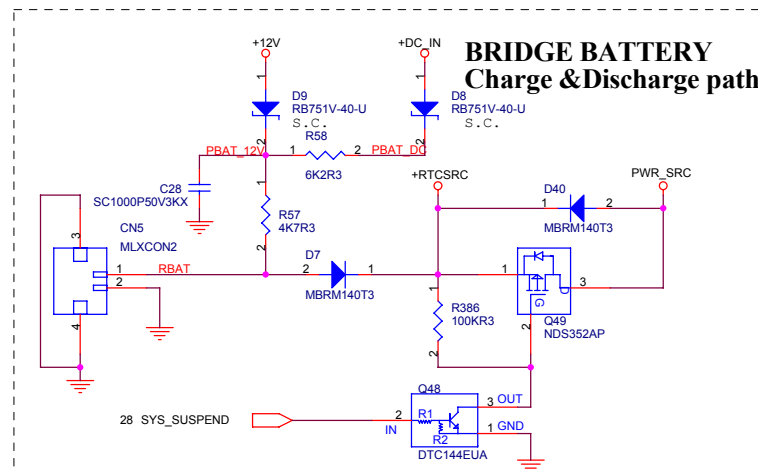
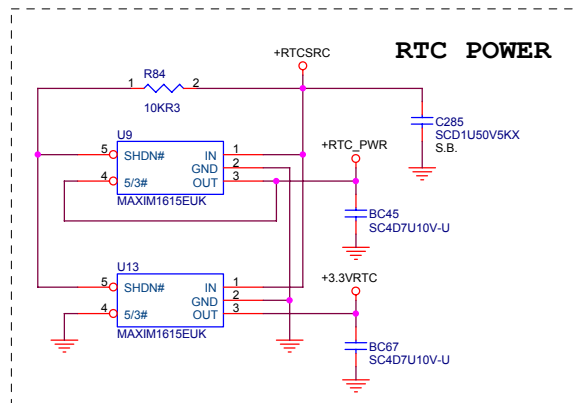
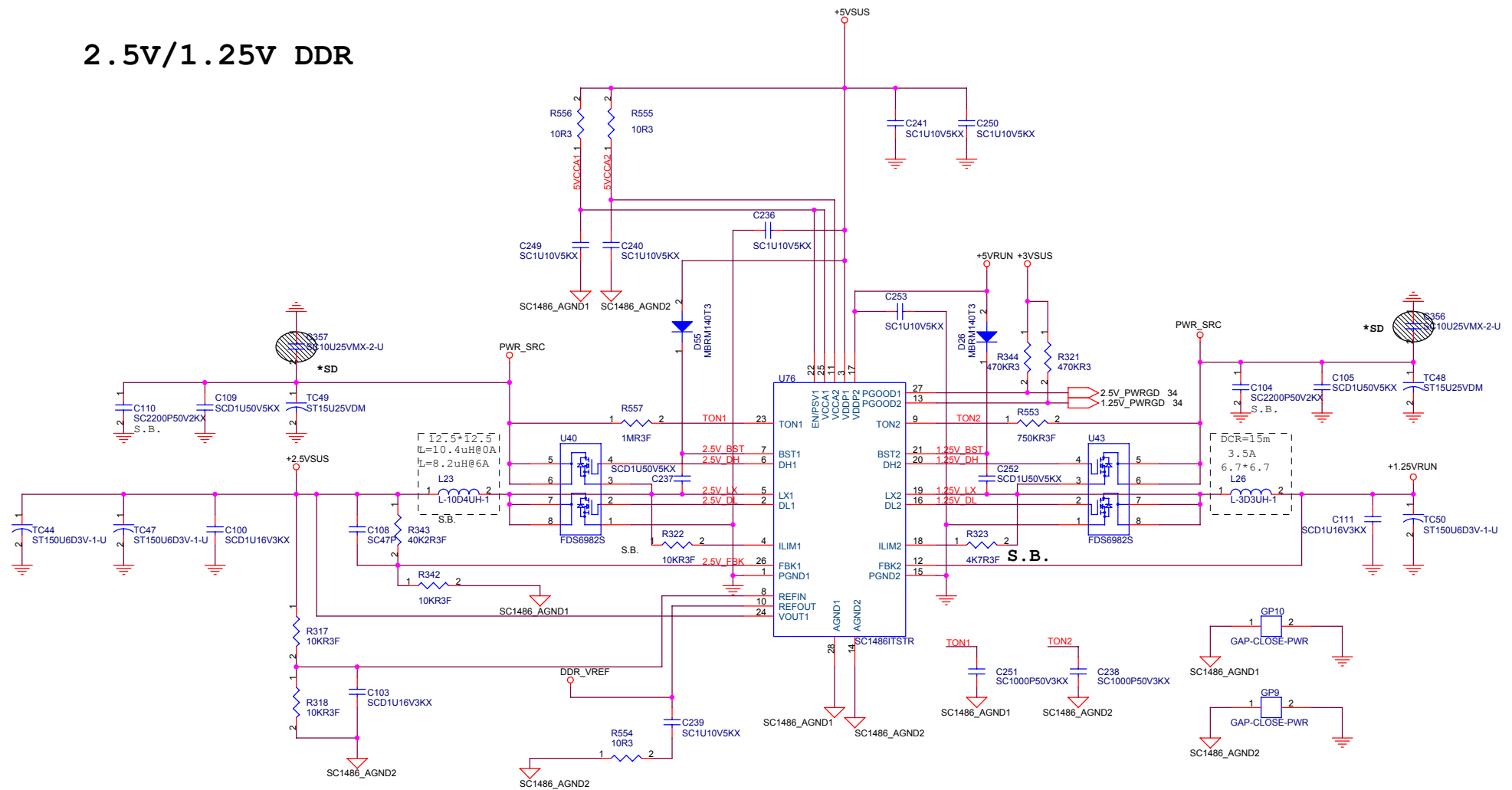
of

40

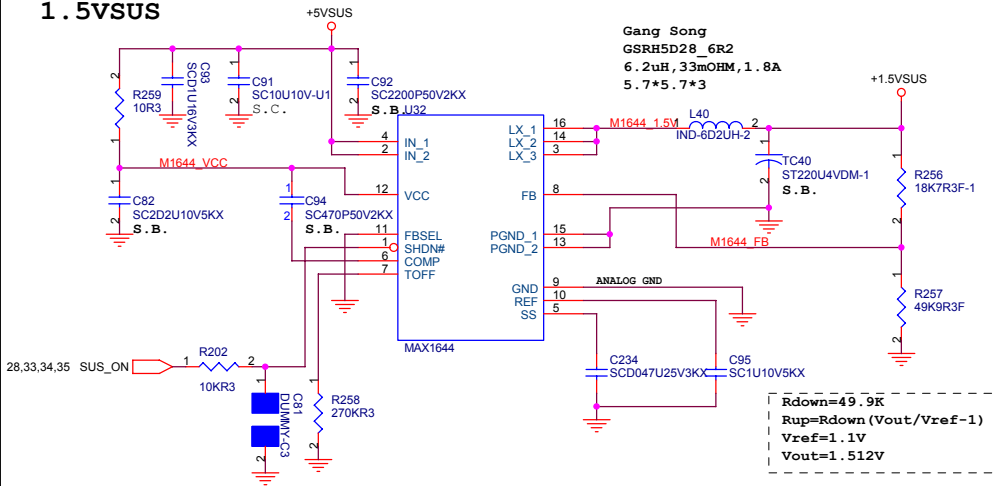
Note: all Grounds Tied together at output Caps.

If MBRM140T3 is ok will remove B540C

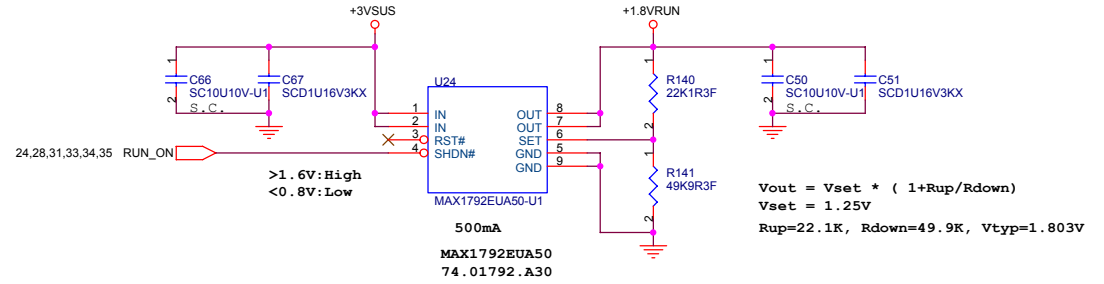
2.5V/1.25V DDR



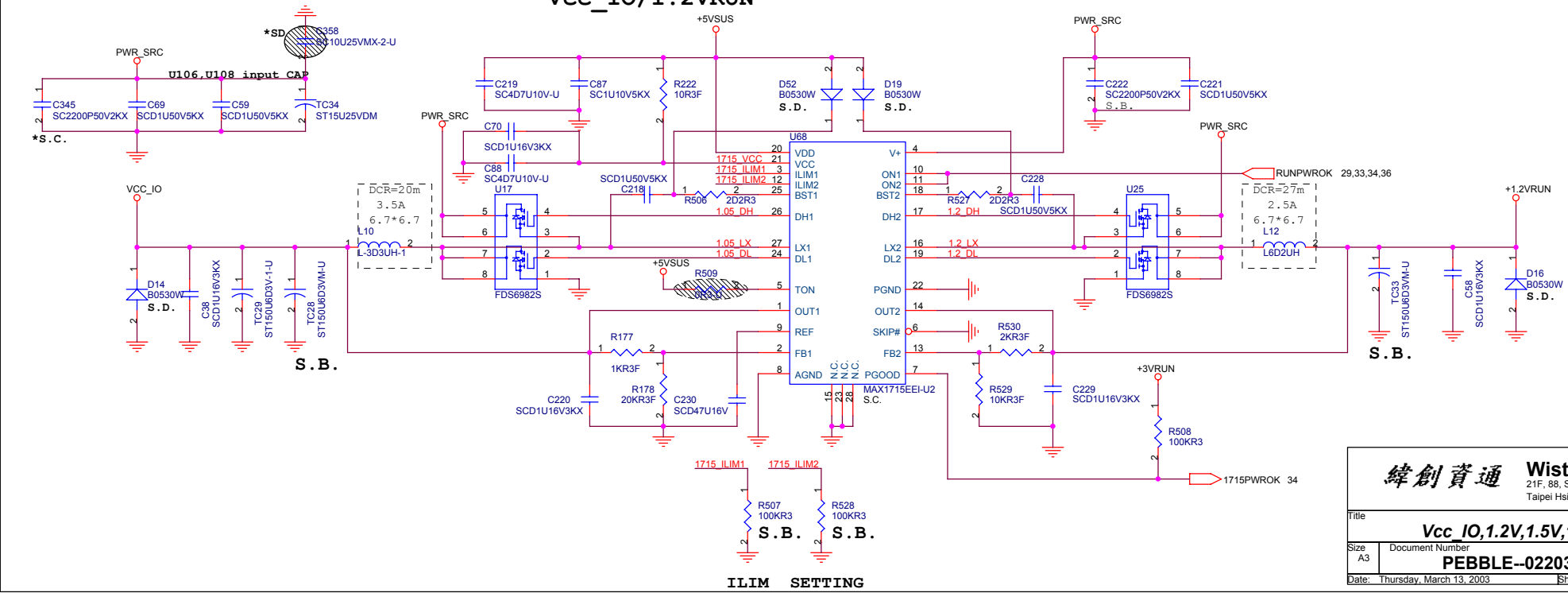
1.5VSUS



1.8VRUN



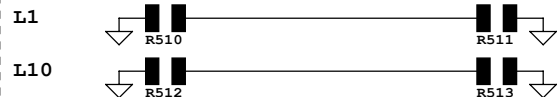
VCC_IO/1.2VRUN



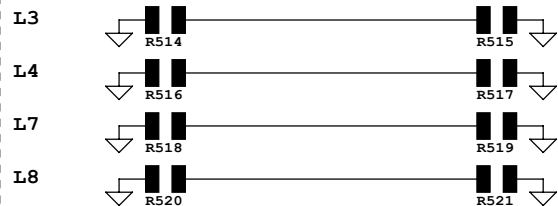
Impedance measurement coupon

Trace length >= 4 inches

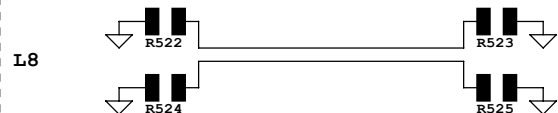
Trace width / Spacing = 5 / 5 mil----45 ohm



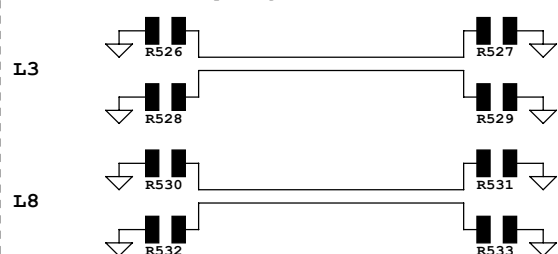
Trace width / Spacing = 4 / 5 mil----55 ohm



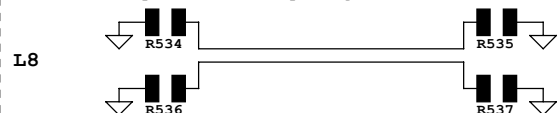
USB Diff. pair Twidh/Tspacing = 4/5 mil----90 ohm



Diff. pair for LVDS, LAN
Twidh/Tspacing = 4/8 mil----100 ohm



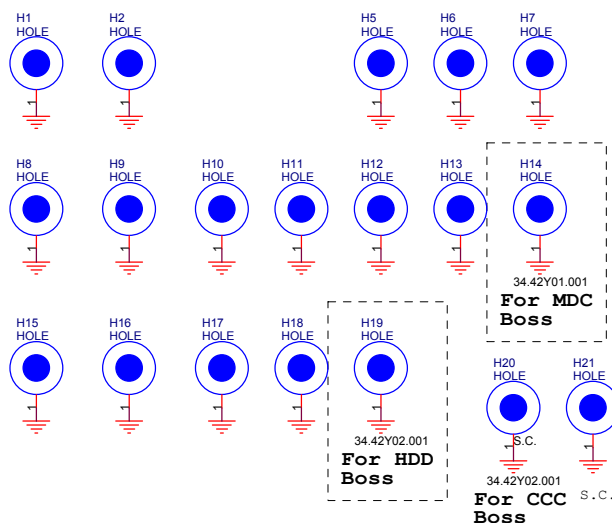
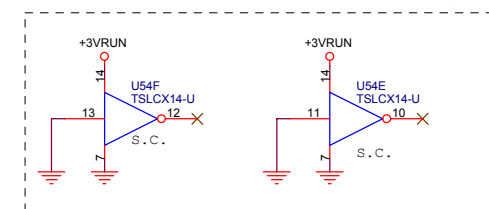
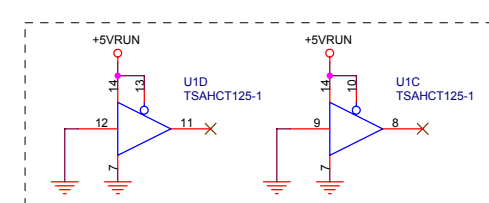
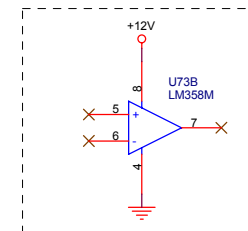
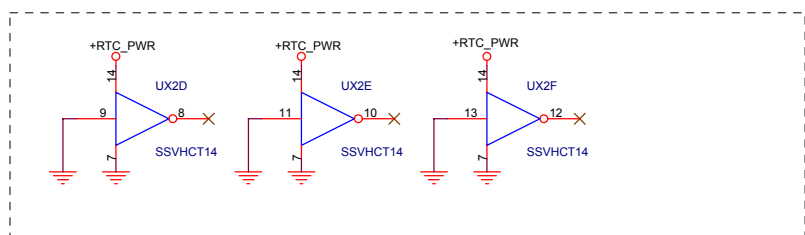
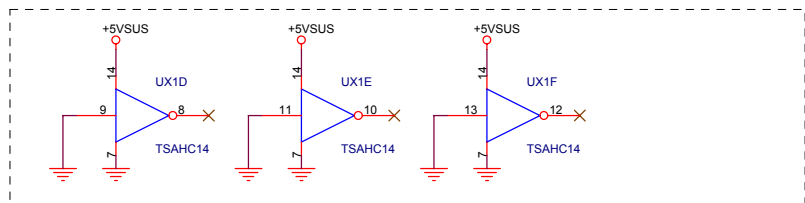
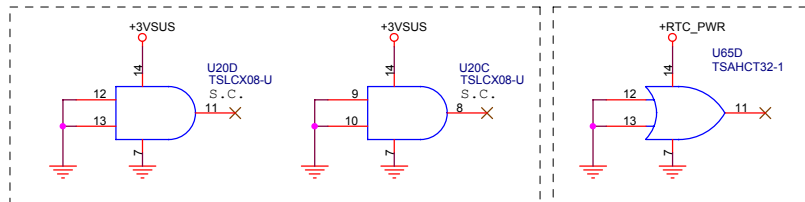
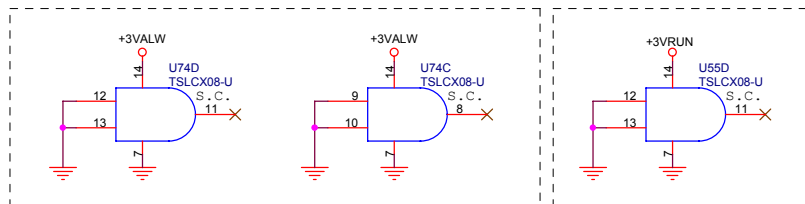
1394 Diff. pair Twidh/Tspacing = 4/10 mil----110 ohm



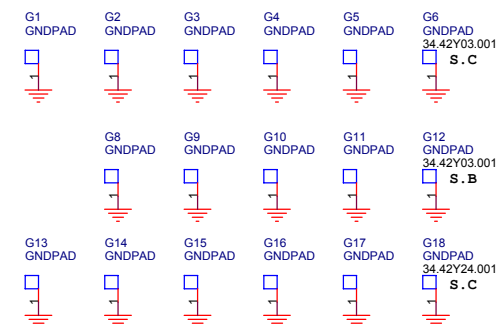
Host CLK signal Trace Twidh/Tspacing = 4/8 mil----100ohm



DDR CLK signal Trace Twidh/Tspacing = 7/4 mil----70ohm



EMI SPRING 34.42P26.001



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