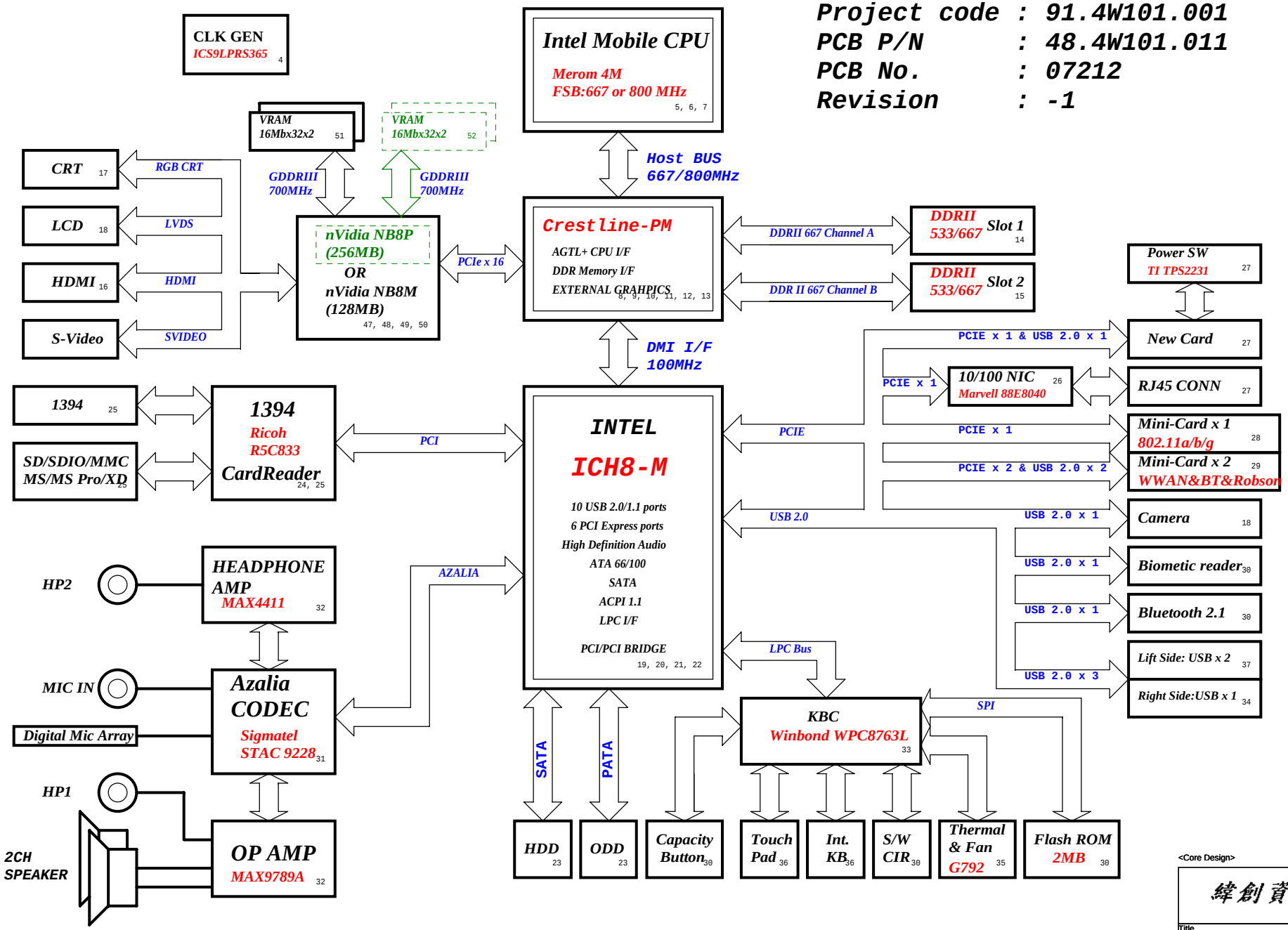
Hawke Intel Discrete Block Diagram

Project code : 91.4W101.001
PCB P/N : 48.4W101.011
PCB No. : 07212
Revision : -1



BATTERY CHARGER MAX8731A 38	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC TPS51120 39	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS5117 42, 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC TPS51100 44	
INPUTS	OUTPUTS
1D8V_S3	0D9V_S3

SYSTEM DC/DC RT9018 44	
INPUTS	OUTPUTS
1D8V_S3 1D8V_S3	1D5V_S0 1D25V_S0

VGA DC/DC TPS5117 53	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFX_CORE_S0

CPU DC/DC ISL6262A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

PCB LAYER

L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Singal
L7:GND
L8:BOT

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: System Block Diagram
Size: A3 | Document Number: Hawke-Intel | Rev: -1
Date: Sunday, September 09, 2007 | Sheet 1 of 57

Adapter

Input Signal	Output Signal
(I)	(O)
Input Power	**Output Power**
VCC(I)	VCC(O)
VCC(I)	

AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+

Charger MAX8731A

Input Signal	Output Signal
CLS (I / 3.3V)	LDO (O / 5.4V)
	(O)
FBSA/B (I/3.3V)	(O)
SCL (IO / 3.3V)	
SDA (IO / 3.3V)	
Output Power	
VCC (O)	
VCC (O)	
ACIN	
Input Power	
DCIN (I)	

CHARGE_OFF
BAT+SENSE
BAT_SCL
BAT_SDA
MAX8731_ACIN
AD+
MAX8731_LDO
ACAV_IN
AD_IA
DCBATOUT
BT+

TI TPS51120 3D3V/5V

Input Signal	Output Signal
51120_EN2 FOR 3.3V	PGOUT(OD / 5V)
51120_EN1 FOR 5.0V	
Input Power	**Output Power**
VIN	(O)
REG5V_IN(I / 5V)	(O)
	5V (O)
	3.3V (O)

3V/5V_EN
3V/5V_EN
DCBATOUT
5V_AUX_S5
CPUCORE_ON
5V_AUX_S5
3D3V_AUX_S5
5V_S5 (6A)
3D3V_S5 (5A)

TPS51117 1D8V

Input Signal	Output Signal
EN_PSV(I / 5V)	(O)
Input Power	**Output Power**
VCC	
VIN	(O)

PM_SLP_S4#
5V_S5
DCBATOUT
CPUCORE_ON
1D8V_S3(19A)

TPS51117 1D05V

Input Signal	Output Signal
EN_PSV(I / 5V)	(O)
Input Power	**Output Power**
VCC	
VIN	(O)

PM_SLP_S3#
5V_S5
DCBATOUT
CPUCORE_ON
1D05V_S0(5A)

TI TPS51100 0.9V/DDR_VREF_S3

Input Signal	
S5	
S3	
Input Power	**Output Power**
VCC(I)	VCC(O)
VIN(I)	VCC(O)

PM_SLP_S4#
PM_SLP_S4#
5V_S5
1D8V_S3
DDR_VREF_S3
DDR_VERF_S0

RT9018A 1D5V

Input Signal	Output Signal
EN(I / 5V)	(O)
Input Power	**Output Power**
VCC	
VIN	(O)

PM_SLP_S3#
5V_S5
1D8V_S3
CPUCORE_ON
1D5V_S0(2.2A)

RT9018A 1D25V

Input Signal	Output Signal
EN(I / 5V)	(O)
Input Power	**Output Power**
VCC	
VIN	(O)

PM_SLP_S3#
5V_S5
1D8V_S3
CPUCORE_ON
1D25V_S0(2.7A)

TPS51117 VGA_CORE

Input Signal	Output Signal
EN_PSV(I / 5V)	(O)
Input Power	**Output Power**
VCC	
VIN	(O)

PM_SLP_S3#
5V_S5
DCBATOUT
CPUCORE_ON
VCC_GFX_CORE_S0 (18.4A)

ISL6262A CPU_CORE

VID Setting	Output Signal
VID0(I / 3.3V)	VROK(O)
VID1(I / 3.3V)	
VID2(I / 3.3V)	
VID3(I / 3.3V)	**Output Power**
VID4(I / 3.3V)	
VID5(I / 3.3V)	
VID6(I / 3.3V)	VCC_CORE_PWR(O)
Input Signal	
EN (I / 3.3V)	
Voltage Sense	
VSEN(I / Vcore)	
RGND(I / Vcore)	
Input Power	
VIN(I)	
VCC(I)	
VCC(I)	

CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
CPU_VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT
5V_S0
3D3V_S0
VGATE_PWRGD
VCC_CORE_S0 (Imax=47A)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
A3	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 2 of 57

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD	tp3	AZ_DOUT_ICH	Description
0	0		RSVD
0	1		Enter XOR Chain
1	0		Normal Operation(default)
1	1		Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	
	low = A16 swap override enable
	high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

20,22 +RTCVCC → +RTCVCC
5,6,7,8,10,11,12,20,22,33,42,46 1D05V_S0 → 1D05V_S0
8,11,22,44,47,48,49 1D25V_S0 → 1D25V_S0
26 1D2V_LAN_S5 → 1D2V_LAN_S5
27 1D5V_NEW_S0 → 1D5V_NEW_S0
6,11,20,21,22,27,28,29,44 1D5V_S0 → 1D5V_S0
8,11,12,14,15,43,44,45,46 1D8V_S3 → 1D8V_S3
26,27 2D5V_LAN_S5 → 2D5V_LAN_S5
20,30,33,35,38,39,46 3D3V_AUX_S5 → 3D3V_AUX_S5
26,27 3D3V_LAN_S5 → 3D3V_LAN_S5
4,8,11,14,15,16,18,19,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,40,42,45,46,47,49,50,53 3D3V_S0 → 3D3V_S0
19,21,22,26,27,30,37,39,45,46 3D3V_S5 → 3D3V_S5
18,38,39,46 5V_AUX_S5 → 5V_AUX_S5
16,17,18,22,23,30,32,34,35,36,40,44,45,46 5V_S0 → 5V_S0
22,23,29,30,34,36,37,39,42,43,44,45,53 5V_S5 → 5V_S5
37,38,46 AD+ → AD+
18,38,39,40,41,42,43,45,46,53 DCBATOUT → DCBATOUT
14,15,44,46 DDR_VREF_S0 → DDR_VREF_S0
8,14,15,44 DDR_VREF_S3 → DDR_VREF_S3
18 +LCDVDD → +LCDVDD
6,7,41 VCC_CORE_S0 → VCC_CORE_S0

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0

USB TABLE

USB0	Ext Lift Side (Bottom)
USB1	Ext Lift Side (Top)
USB2	Ext Right Side
USB3	N/A
USB4	WWAN
USB5	Bluetooth
USB6	Camera
USB7	Biometric
USB8	Express Card
USB9	3rd mini card

PCIE Routing

LANE1	10/100M Bit LOM
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN
LANE4	BT/UWB/Robson
LANE5	Express Card
LANE6	N/A

<Core Design>

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Title: Table of Content

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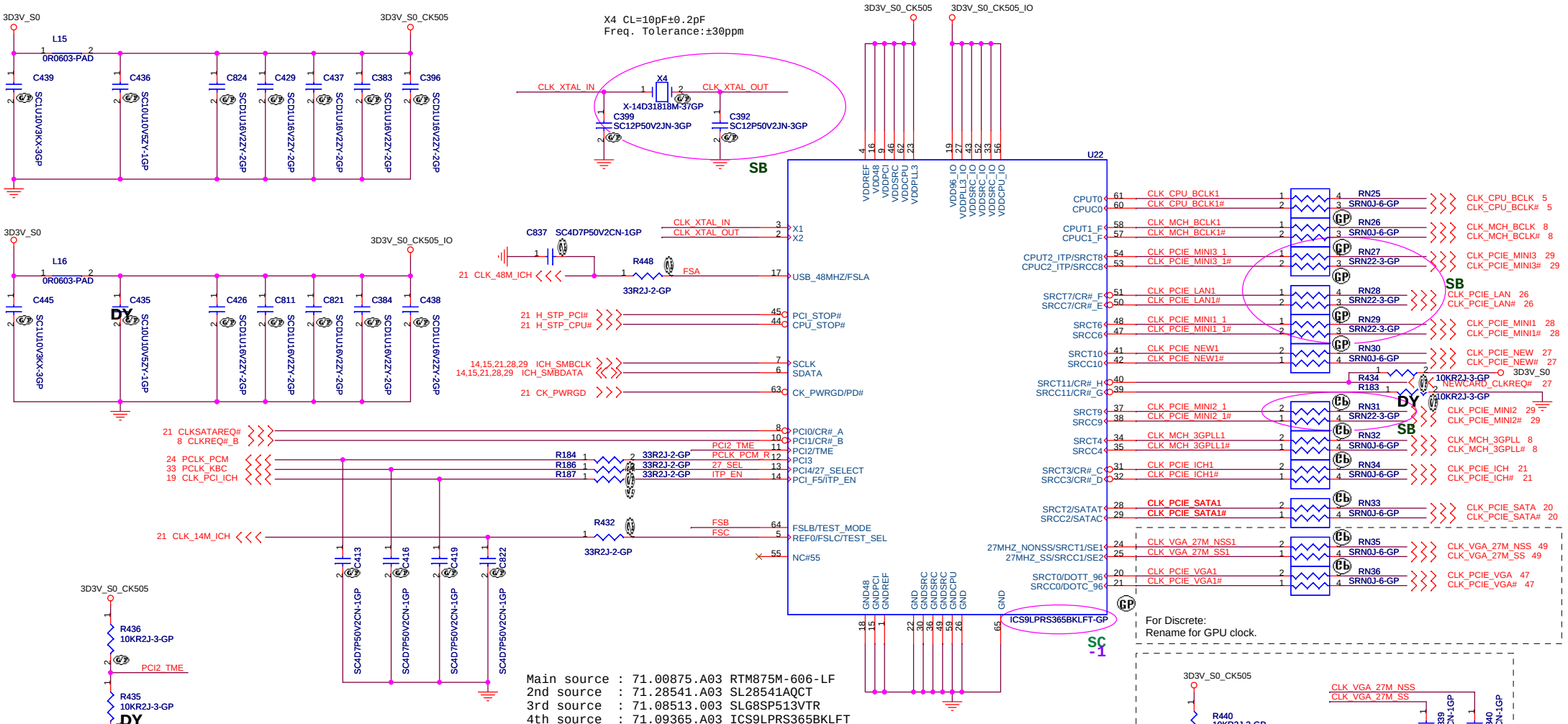

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

ITP_EN	Output
0	SRC8
1	CPU_ITP

27_SEL strap 0:For 965GM, 1:For 965PM

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25	
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100	965GM
1	SRCT0	SRCC0	27M_NSS	27M_SS	965PM

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. ICS9LPRS365 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Core Design>

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Title: **Clock generator ICS9LPRS365**

Size: A3 | Document Number: Hawke-Intel | Rev: -1

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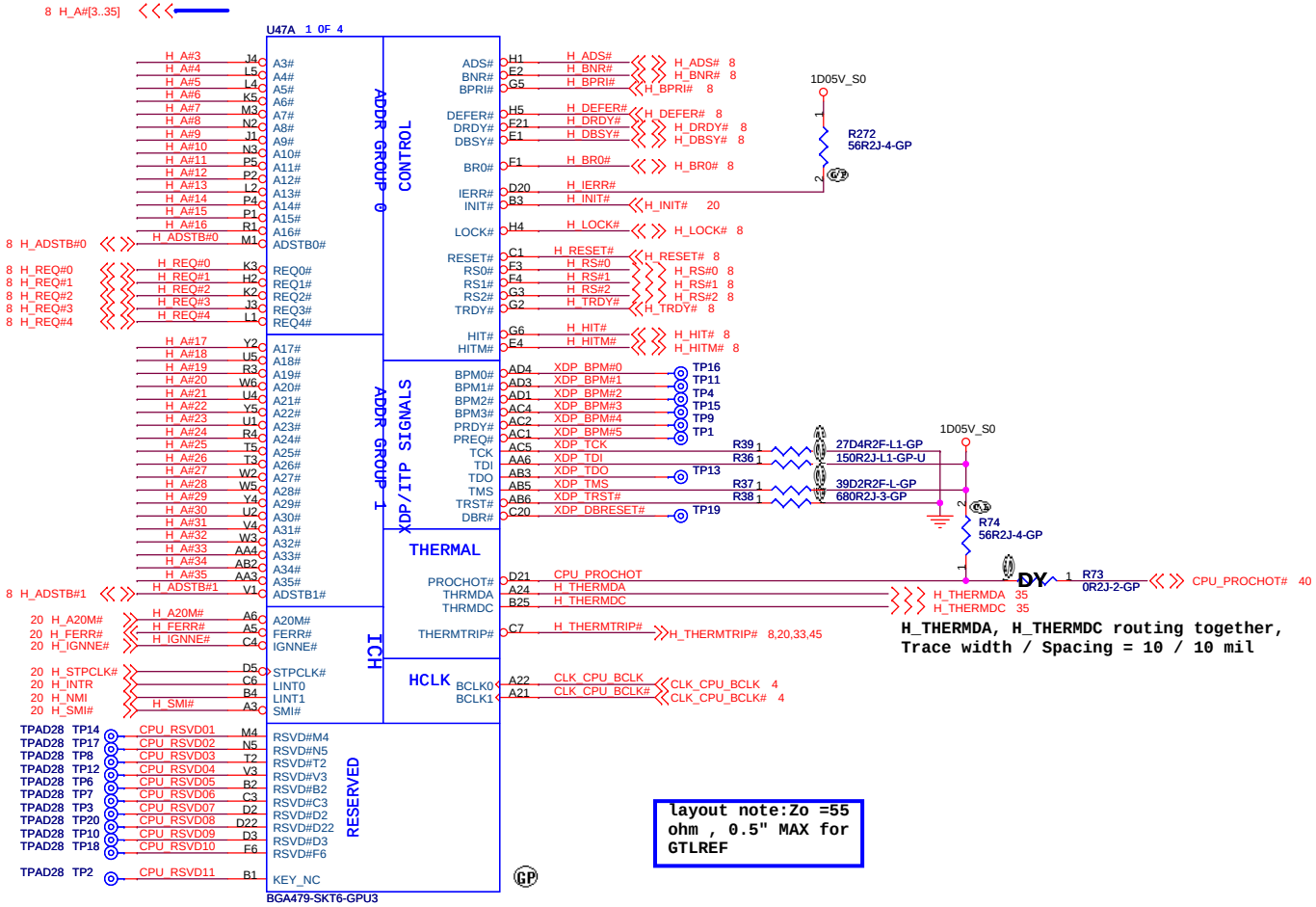

Main source : 62.10079.021 Tyco 2-1871873-4
2nd source : 62.10040.221 Foxconn PZ47827-274M-41

<Core Design>

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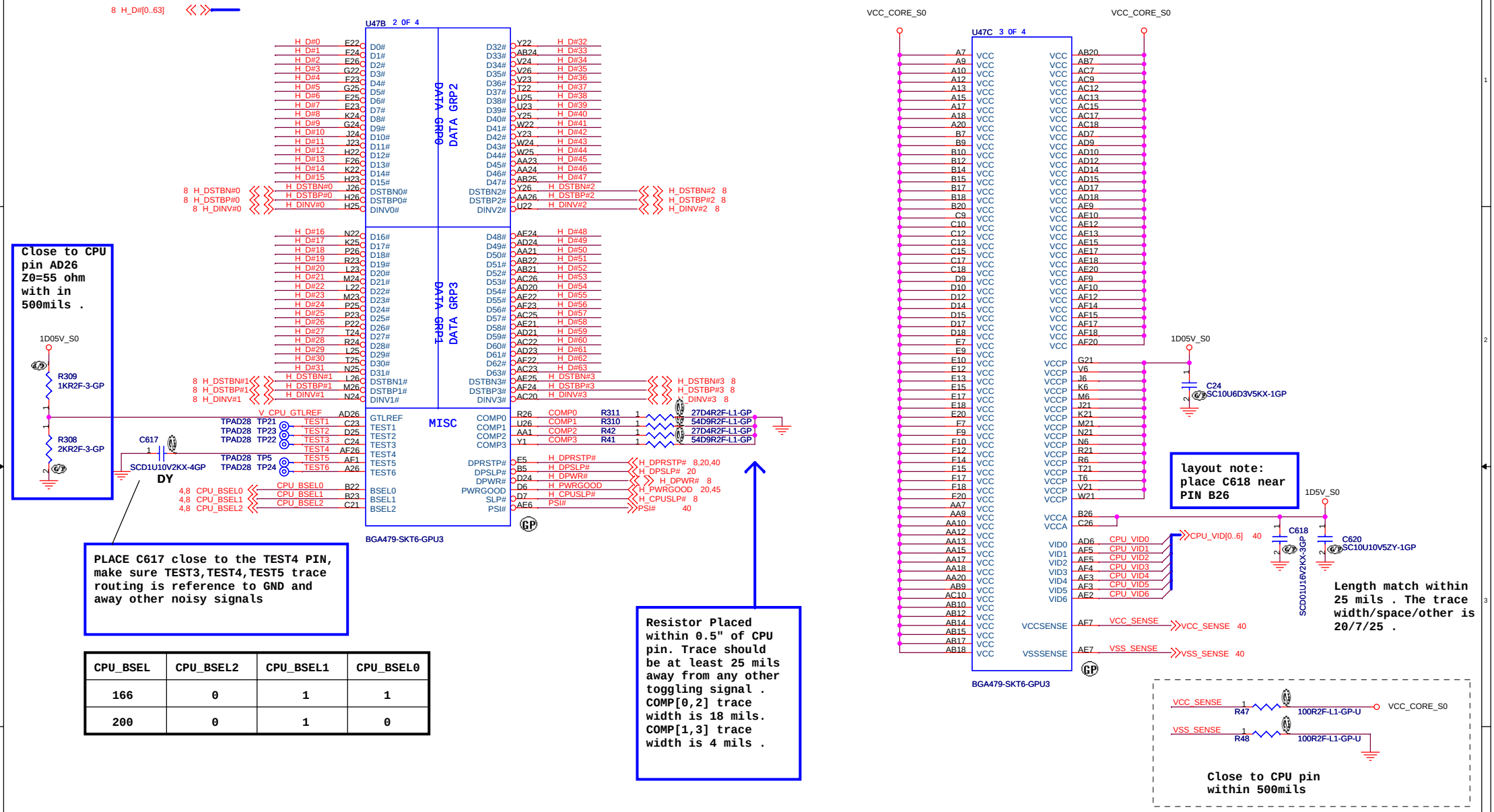
Title: Meron(1/3)-AGTL+/XDP

Size: A3 | Document Number: Hawke-Intel | Rev: -1

Date: Sunday, September 09, 2007 | Sheet 5 of 57



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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Title: ***Meron(2/3)-AGTL+/PWR***

Size	Document Number	Rev
A3	Hawke-Intel	-1

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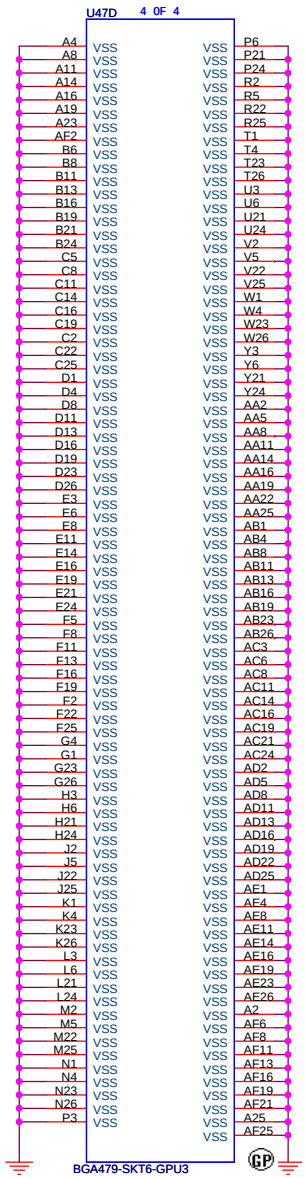

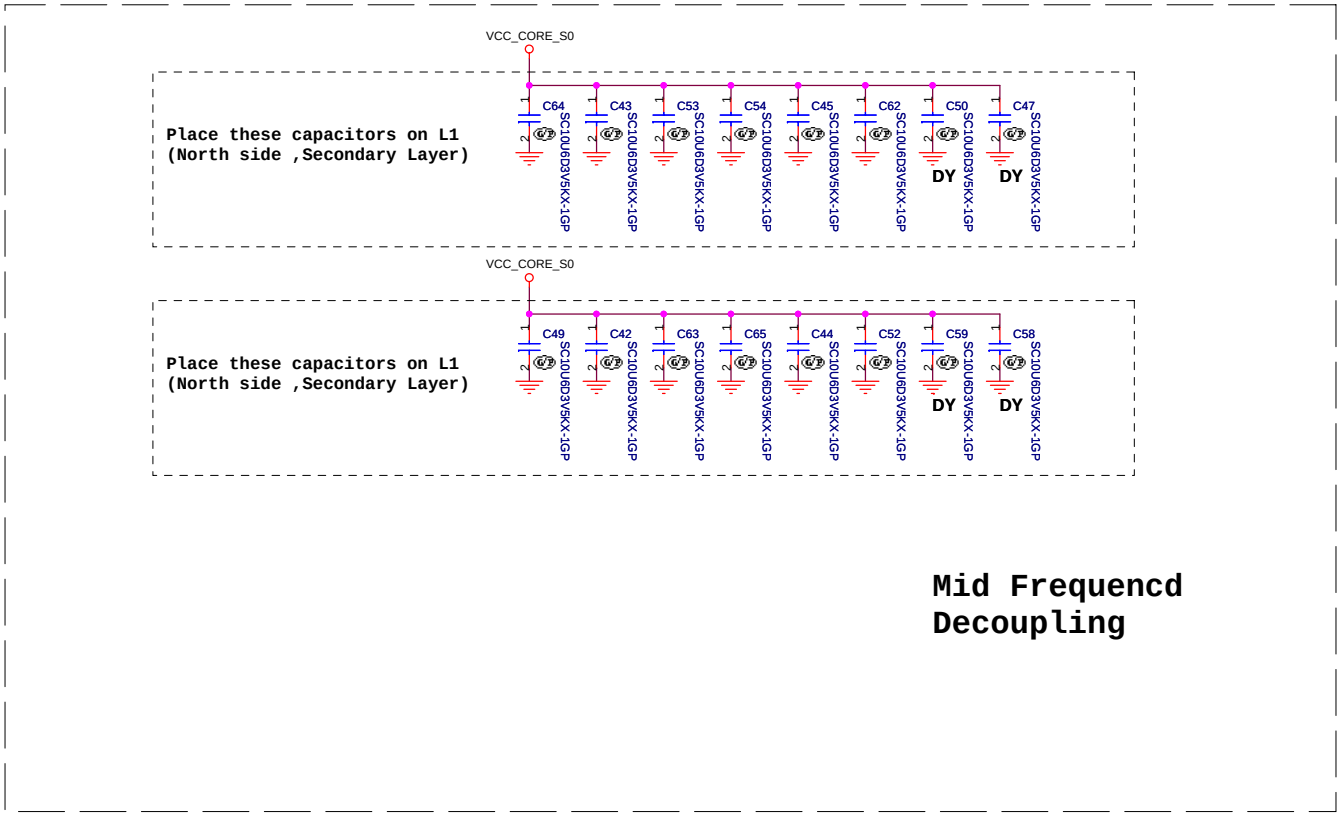

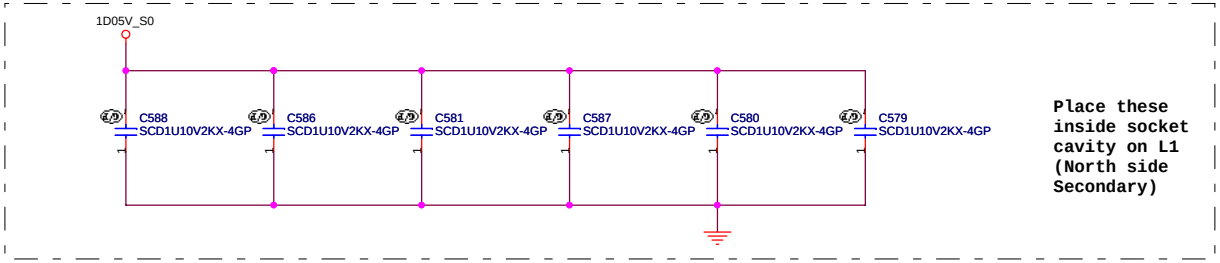

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Title: Meron(3/3)-GND&Bypass

Size	Document Number	Rev
A3	Hawke-Intel	-1

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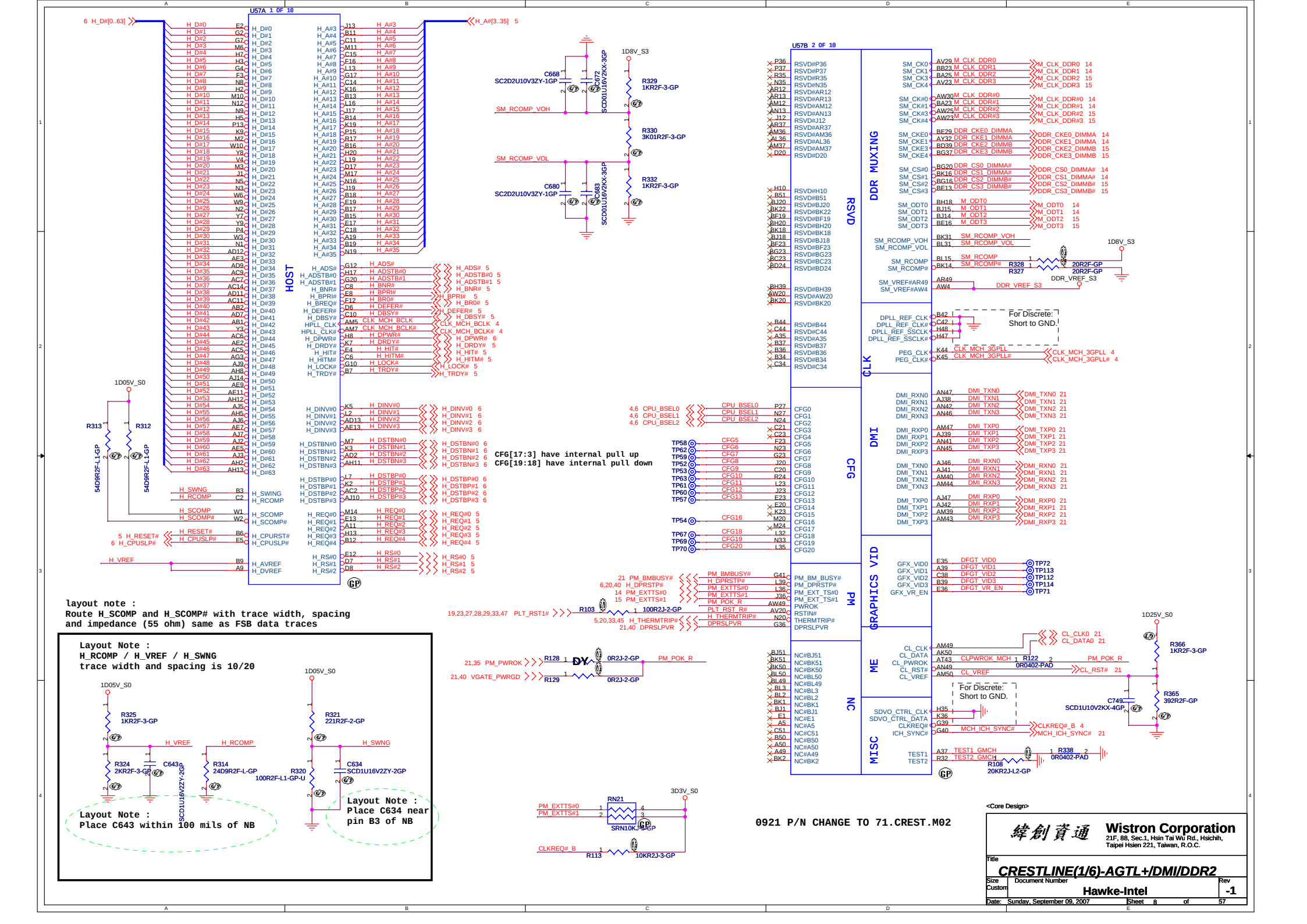
U57A 1 OF 10
HOST
U57B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing
and impedance (55 ohm) same as FSB data traces
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down
Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
Layout Note :
Place C643 within 100 mils of NB
Layout Note :
Place C634 near
pin B3 of NB
For Discrete:
Short to GND.
For Discrete:
Short to GND.
0921 P/N CHANGE TO 71.CREST.M02
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRESTLINE(1/6)-AGTL+/DMI/DDR2
Size
Custom
Document Number
Hawke-Intel
Rev
-1
Date: Sunday, September 09, 2007
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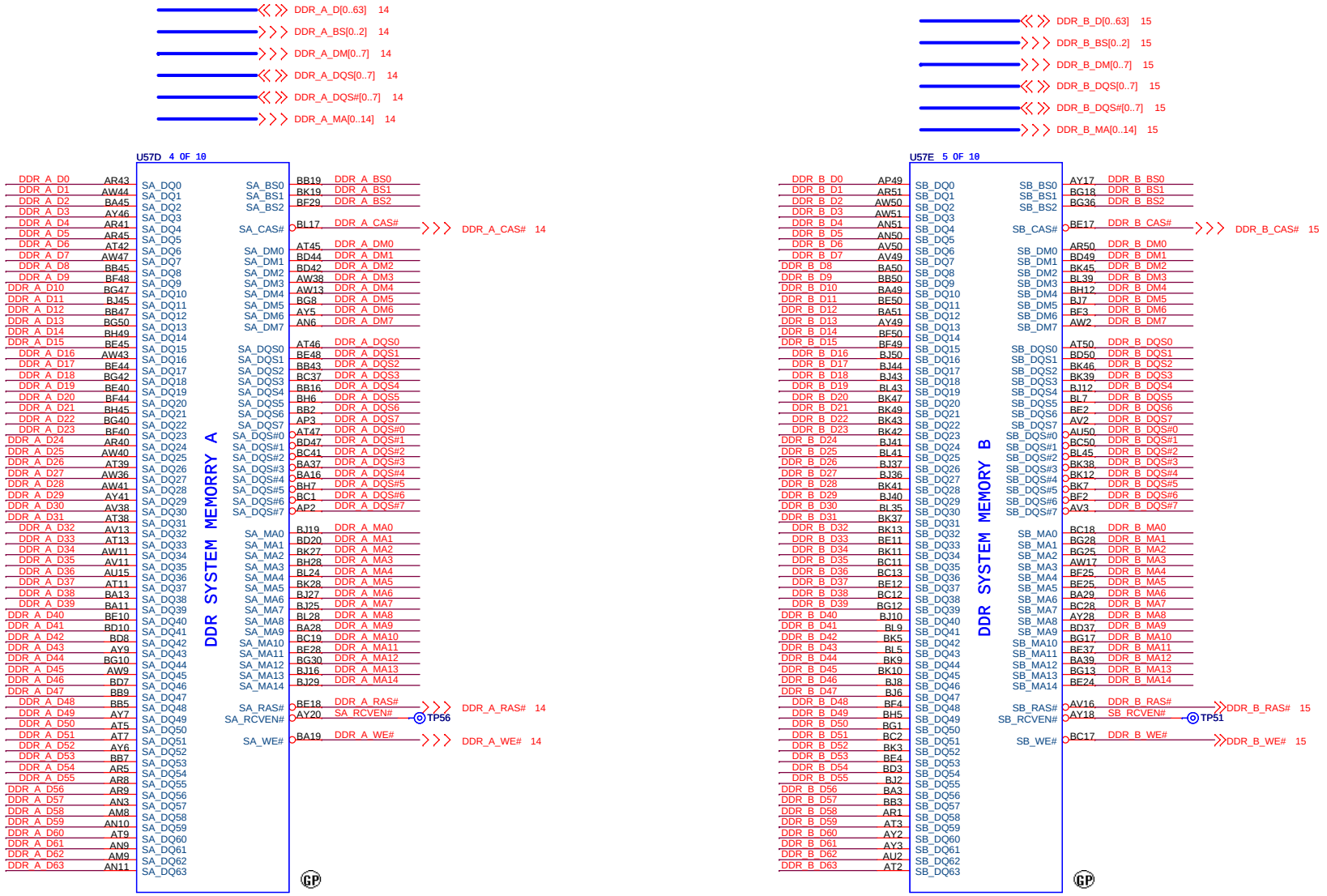

<Core Design>

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Title
CRESTLINE(2/6)-DDR2 A/B CH

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A3	Hawke-Intel	-1

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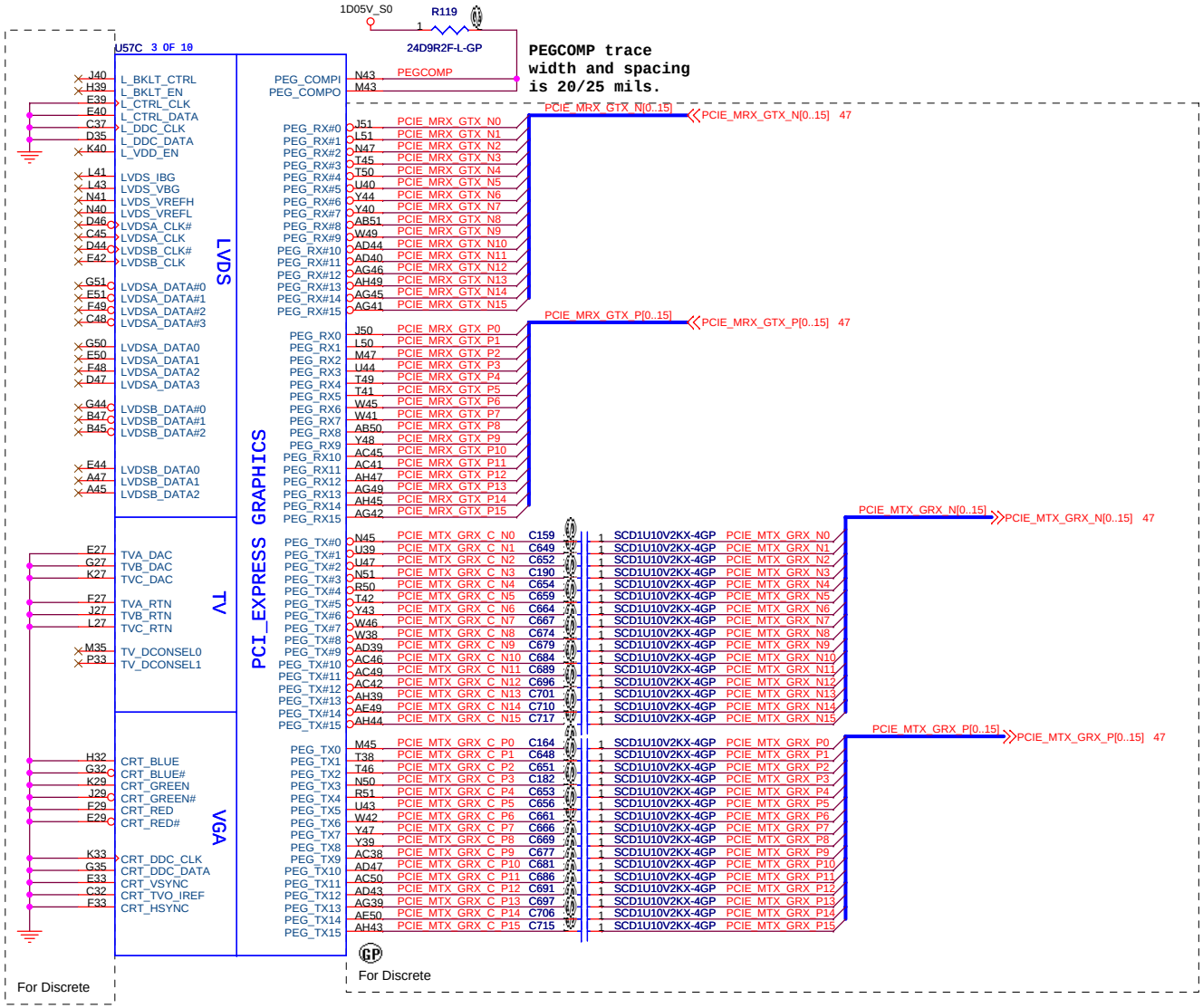

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

<Core Design>

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Title: CRESTLINE(3/6)-VGA/LVDS/TV

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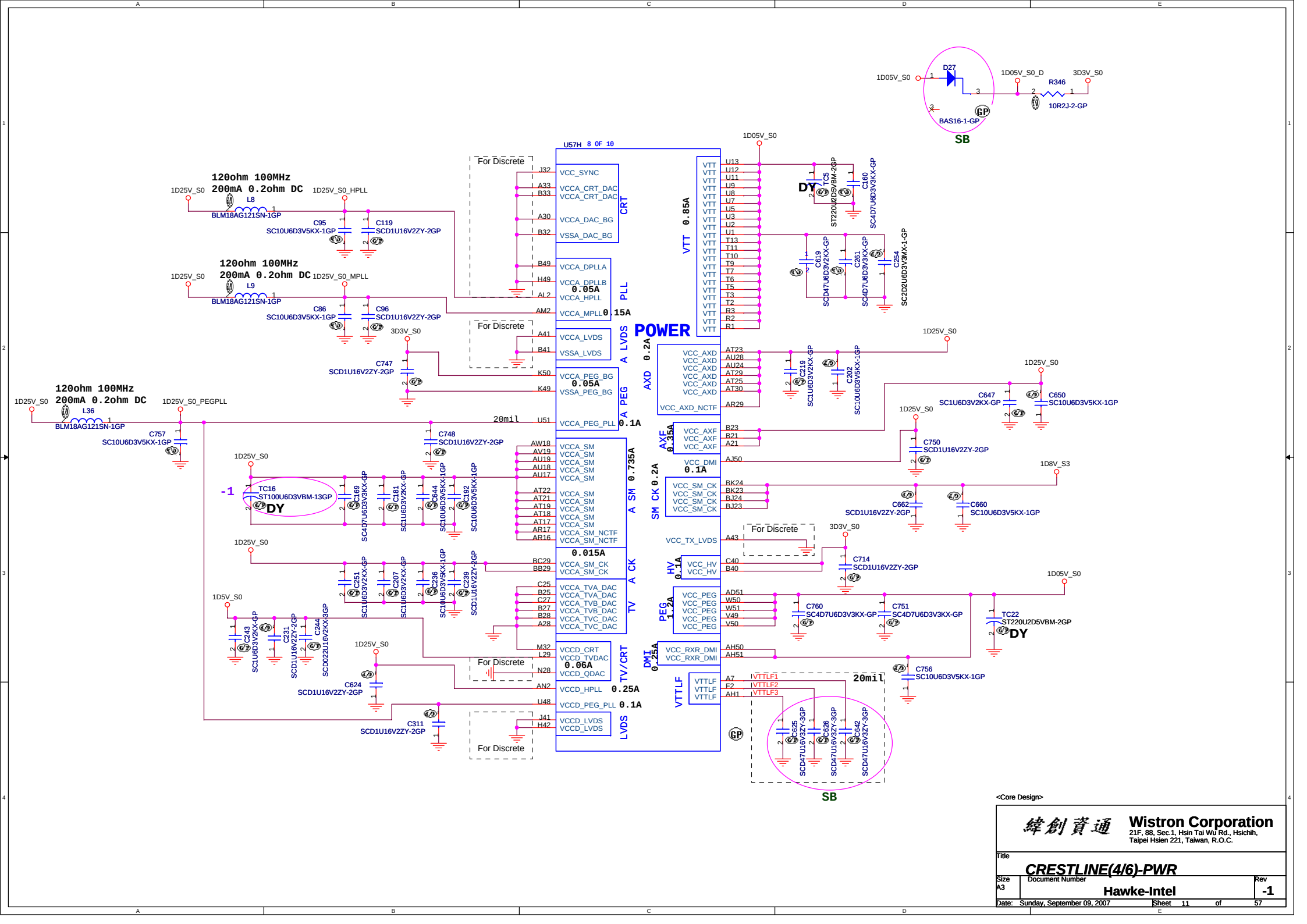
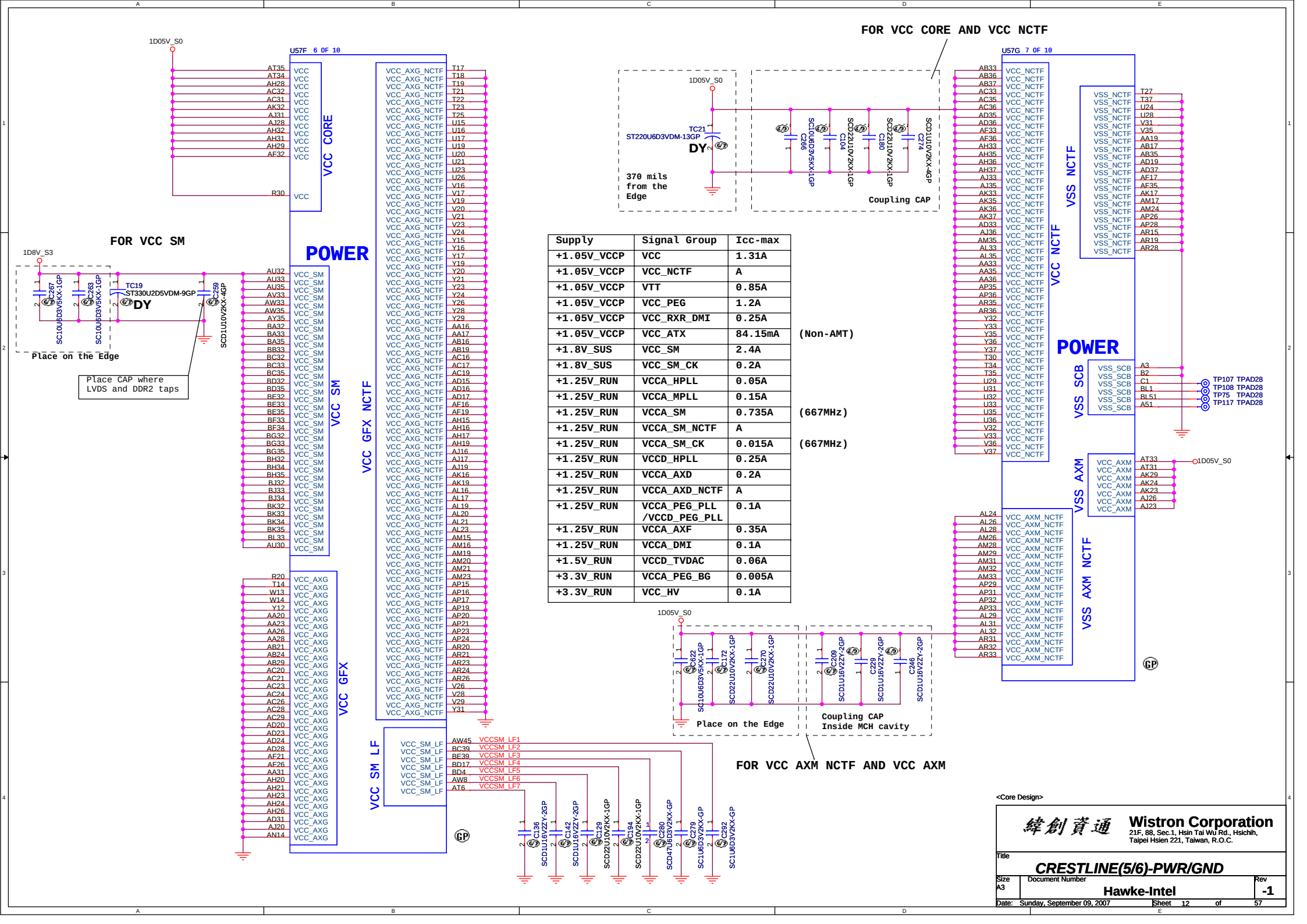

U57H 8 OF 10
POWER
VTT 0.85A
AXD 0.2A
AXF 0.35A
SM CK 0.2A
A SM 0.735A
A CK 0.015A
TV 0.25A
HV 0.1A
PEG 1.2A
DMI 0.25A
VTTLF
CRT
PLL 0.15A
A LVDS 0.2A
A PEG 0.1A
TV/CRT 0.06A
LVDS 0.1A
VCC_SYNC
VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB 0.05A
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG 0.05A
VSSA_PEG_BG
VCCA_PEG_PLL
VCCA_SM
VCCA_SM_NCTF
VCCA_SM_CK
VCCA_TVA_DAC
VCCA_TVB_DAC
VCCA_TVC_DAC
VCCD_CRT
VCCD_TVDAC 0.06A
VCCD_QDAC
VCCD_HPLL 0.25A
VCCD_PEG_PLL 0.1A
VCCD_LVDS
VTT
VCC_AXD
VCC_AXD_NCTF
VCC_AXF
VCC_DMI 0.1A
VCC_SM_CK
VCC_TX_LVDS
VCC_HV
VCC_PEG
VCC_RXR_DMI
VTTLF1
VTTLF2
VTTLF3
120ohm 100MHz
200mA 0.2ohm DC
L8
BLM18AG121SN-1GP
L9
L36
1D25V_S0
1D25V_S0_HPLL
1D25V_S0_MPLL
1D25V_S0_PEGPLL
3D3V_S0
1D05V_S0
1D05V_S0_D
1D8V_S3
D27
BAS16-1-GP
R346
10R2J-2-GP
SB
DY
-1
TC16
ST100U6D3VBM-13GP
TC5
ST220U2D5VBM-2GP
TC22
ST220U2D5VBM-2GP
C95
SC10U6D3V5KX-1GP
C119
SCD1U16V2ZY-2GP
C86
C96
C747
C748
C757
C624
C311
C750
C760
C751
C714
C756
C647
C650
C662
C660
C619
SCD47U6D3V2KX-GP
C261
SC4D7U6D3V3KX-GP
C254
SC2D2U6D3V3MX-1-GP
C160
SC4D7U6D3V3KX-GP
C202
SC10U6D3V5KX-1GP
C219
SC1U6D3V2KX-GP
C169
C181
C644
C192
C251
C207
C236
C239
C243
C231
C244
C625
C626
C642
SCD47U16V3Y-3GP
For Discrete
20mil
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRESTLINE(4/6)-PWR
Size A3
Document Number
Hawke-Intel
Rev -1
Date: Sunday, September 09, 2007
Sheet 11 of 57



Supply	Signal Group	Icc-max	
+1.05V_VCCP	VCC	1.31A	
+1.05V_VCCP	VCC_NCTF	A	
+1.05V_VCCP	VTT	0.85A	
+1.05V_VCCP	VCC_PEG	1.2A	
+1.05V_VCCP	VCC_RXR_DMI	0.25A	
+1.05V_VCCP	VCC_ATX	84.15mA	(Non-AMT)
+1.8V_SUS	VCC_SM	2.4A	
+1.8V_SUS	VCC_SM_CK	0.2A	
+1.25V_RUN	VCCA_HPLL	0.05A	
+1.25V_RUN	VCCA_MPLL	0.15A	
+1.25V_RUN	VCCA_SM	0.735A	(667MHz)
+1.25V_RUN	VCCA_SM_NCTF	A	
+1.25V_RUN	VCCA_SM_CK	0.015A	(667MHz)
+1.25V_RUN	VCCD_HPLL	0.25A	
+1.25V_RUN	VCCA_AXD	0.2A	
+1.25V_RUN	VCCA_AXD_NCTF	A	
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A	
+1.25V_RUN	VCCA_AXF	0.35A	
+1.25V_RUN	VCCA_DMI	0.1A	
+1.5V_RUN	VCCD_TVDAC	0.06A	
+3.3V_RUN	VCCA_PEG_BG	0.005A	
+3.3V_RUN	VCC_HV	0.1A	

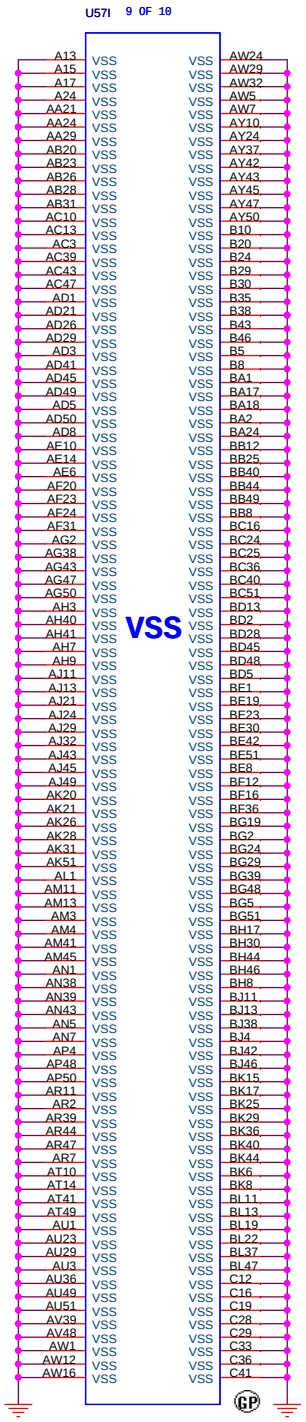
<Core Design>

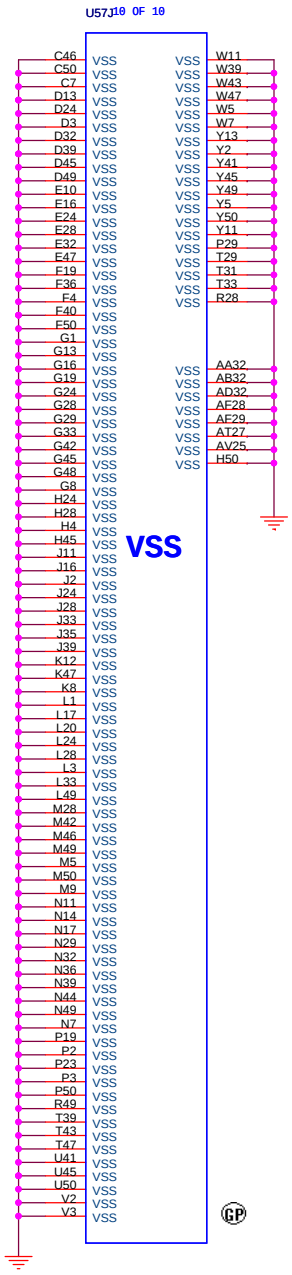
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(5/6)-PWR/GND

Size: A3 | Document Number: Hawke-Intel | Rev: -1

Date: Sunday, September 09, 2007 | Sheet 12 of 57





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CRESTLINE(6/6)-PWR/GND

Size	Document Number	Rev
A3	Hawke-Intel	-1

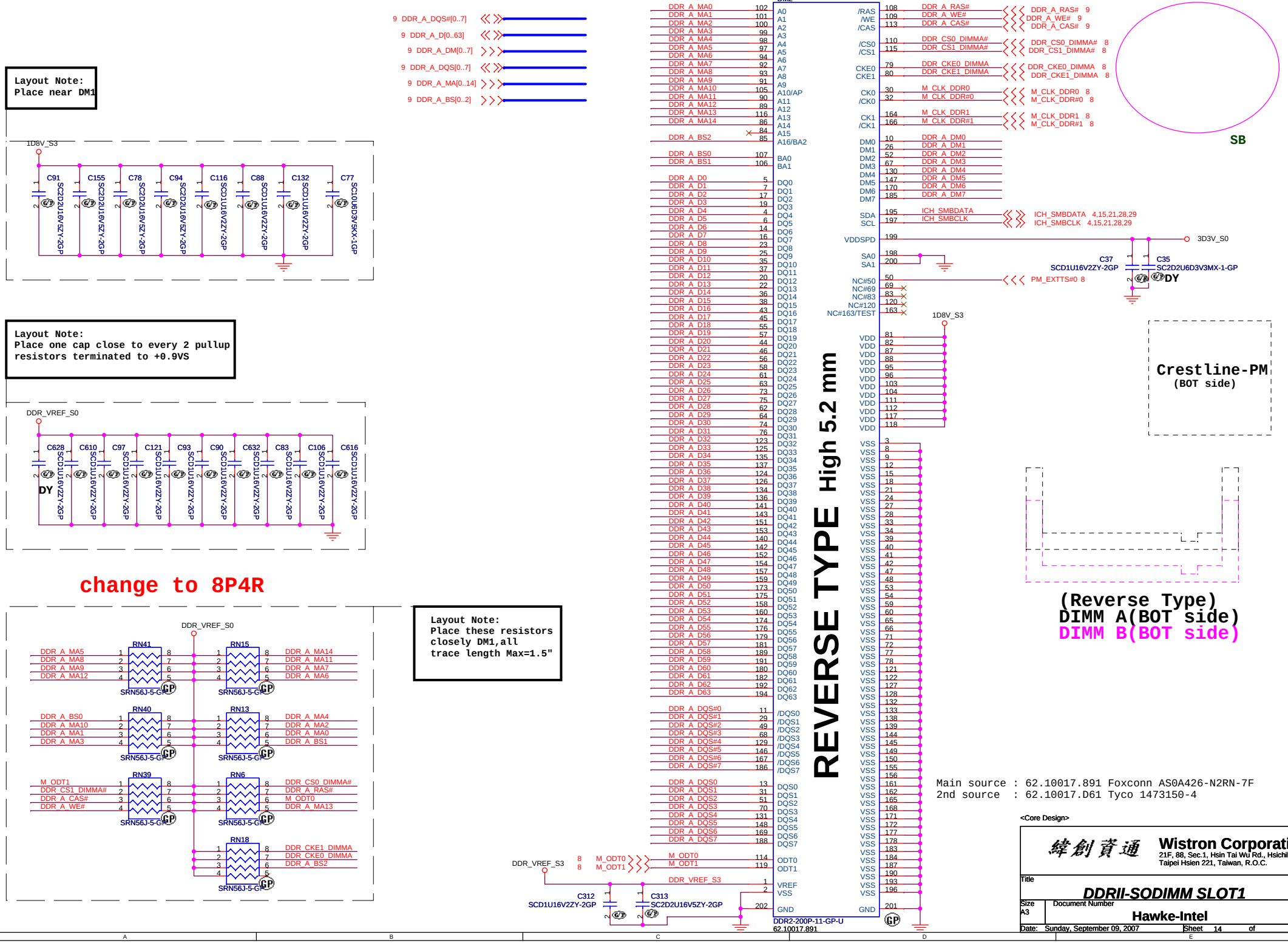
Date: Sunday, September 09, 2007 Sheet 13 of 57

Layout Note:
Place near DM1

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

change to 8P4R

Layout Note:
Place these resistors closely DM1,all trace length Max=1.5"



Main source : 62.10017.891 Foxconn AS0A426-N2RN-7F
2nd source : 62.10017.D61 Tyco 1473150-4

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT1

Size	Document Number	Rev
A3	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 14 of 57

Layout Note:
Place near DM2

1D8V_S3

C72 SC2D2U16V5ZY-2GP
C145 SC2D2U16V5ZY-2GP
C147 SC2D2U16V5ZY-2GP
C71 SC2D2U16V5ZY-2GP
C81 SCD1U16V2ZY-2GP
C108 SCD1U16V2ZY-2GP
C85 SCD1U16V2ZY-2GP
C92 SC10U6D3V5KX-1GP

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

DDR_VREF_S0

C122 SCD1U16V2ZY-2GP DY
C117 SCD1U16V2ZY-2GP
C80 SCD1U16V2ZY-2GP
C99 SCD1U16V2ZY-2GP
C79 SCD1U16V2ZY-2GP
C75 SCD1U16V2ZY-2GP
C105 SCD1U16V2ZY-2GP
C87 SCD1U16V2ZY-2GP
C98 SCD1U16V2ZY-2GP
C107 SCD1U16V2ZY-2GP

DDR_VREF_S0

RN11 SRN56J-5-GP: DDR_B_MA3, DDR_B_MA1, DDR_B_MA10, DDR_B_BS0
RN14 SRN56J-5-GP: DDR_B_MA5, DDR_B_MA8, DDR_B_MA9, DDR_B_MA12
RN12 SRN56J-5-GP: DDR_B_RAS#, DDR_B_MA0, DDR_B_MA2, DDR_B_MA4
RN16 SRN56J-5-GP: DDR_B_MA14, DDR_B_MA11, DDR_B_MA7, DDR_B_MA6
RN5 SRN56J-5-GP: DDR_B_WE#, DDR_B_CAS#, DDR_CS3_DIMMB#, M_ODT3
RN7 SRN56J-5-GP: DDR_CS2_DIMMB#, DDR_B_BS1, M_ODT2, DDR_B_MA13
RN17 SRN56J-5-GP: DDR_CKE3_DIMMB, DDR_B_BS2, DDR_CKE2_DIMMB

Layout Note:
Place these resistors closely DM2,all trace length Max=1.5"

9 DDR_B_DQS#[0..7]
9 DDR_B_D[0..63]
9 DDR_B_DM[0..7]
9 DDR_B_DQS[0..7]
9 DDR_B_MA[0..14]
9 DDR_B_BS[0..2]

DM1

DDR_B_MA0 102 A0
DDR_B_MA1 101 A1
DDR_B_MA2 100 A2
DDR_B_MA3 99 A3
DDR_B_MA4 98 A4
DDR_B_MA5 97 A5
DDR_B_MA6 94 A6
DDR_B_MA7 92 A7
DDR_B_MA8 93 A8
DDR_B_MA9 91 A9
DDR_B_MA10 105 A10/AP
DDR_B_MA11 90 A11
DDR_B_MA12 89 A12
DDR_B_MA13 116 A13
DDR_B_MA14 86 A14
84 A15
DDR_B_BS2 85 A16/BA2
DDR_B_BS0 107 BA0
DDR_B_BS1 106 BA1

DDR_B_D0 5 DQ0
DDR_B_D1 7 DQ1
DDR_B_D2 17 DQ2
DDR_B_D3 19 DQ3
DDR_B_D4 4 DQ4
DDR_B_D5 6 DQ5
DDR_B_D6 14 DQ6
DDR_B_D7 16 DQ7
DDR_B_D8 23 DQ8
DDR_B_D9 25 DQ9
DDR_B_D10 35 DQ10
DDR_B_D11 37 DQ11
DDR_B_D12 20 DQ12
DDR_B_D13 22 DQ13
DDR_B_D14 36 DQ14
DDR_B_D15 38 DQ15
DDR_B_D16 43 DQ16
DDR_B_D17 45 DQ17
DDR_B_D18 55 DQ18
DDR_B_D19 57 DQ19
DDR_B_D20 44 DQ20
DDR_B_D21 46 DQ21
DDR_B_D22 56 DQ22
DDR_B_D23 58 DQ23
DDR_B_D24 61 DQ24
DDR_B_D25 63 DQ25
DDR_B_D26 73 DQ26
DDR_B_D27 75 DQ27
DDR_B_D28 62 DQ28
DDR_B_D29 64 DQ29
DDR_B_D30 74 DQ30
DDR_B_D31 76 DQ31
DDR_B_D32 123 DQ32
DDR_B_D33 125 DQ33
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DDR_B_D36 124 DQ36
DDR_B_D37 126 DQ37
DDR_B_D38 134 DQ38
DDR_B_D39 136 DQ39
DDR_B_D40 141 DQ40
DDR_B_D41 143 DQ41
DDR_B_D42 151 DQ42
DDR_B_D43 153 DQ43
DDR_B_D44 140 DQ44
DDR_B_D45 142 DQ45
DDR_B_D46 152 DQ46
DDR_B_D47 154 DQ47
DDR_B_D48 157 DQ48
DDR_B_D49 159 DQ49
DDR_B_D50 173 DQ50
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DDR_B_D54 174 DQ54
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DDR_B_D56 179 DQ56
DDR_B_D57 181 DQ57
DDR_B_D58 189 DQ58
DDR_B_D59 191 DQ59
DDR_B_D60 180 DQ60
DDR_B_D61 182 DQ61
DDR_B_D62 192 DQ62
DDR_B_D63 194 DQ63

DDR_B_DQS#0 11 DQS0#
DDR_B_DQS#1 29 DQS1#
DDR_B_DQS#2 49 DQS2#
DDR_B_DQS#3 68 DQS3#
DDR_B_DQS#4 129 DQS4#
DDR_B_DQS#5 146 DQS5#
DDR_B_DQS#6 167 DQS6#
DDR_B_DQS#7 186 DQS7#

DDR_B_DQS0 13 DQS0
DDR_B_DQS1 31 DQS1
DDR_B_DQS2 51 DQS2
DDR_B_DQS3 70 DQS3
DDR_B_DQS4 131 DQS4
DDR_B_DQS5 148 DQS5
DDR_B_DQS6 169 DQS6
DDR_B_DQS7 188 DQS7

M_ODT2 114 OTD0
M_ODT3 119 OTD1

DDR_VREF_S3 1 VREF
2 VSS
202 GND
MH1 MH1

RAS# 108 DDR_B_RAS# → DDR_B_RAS# 9
WE# 109 DDR_B_WE# → DDR_B_WE# 9
CAS# 113 DDR_B_CAS# → DDR_B_CAS# 9
CS0# 110 DDR_CS2_DIMMB# → DDR_CS2_DIMMB# 8
CS1# 115 DDR_CS3_DIMMB# → DDR_CS3_DIMMB# 8
CKE0 79 DDR_CKE2_DIMMB → DDR_CKE2_DIMMB 8
CKE1 80 DDR_CKE3_DIMMB → DDR_CKE3_DIMMB 8
CK0 30 M_CLK_DDR2 → M_CLK_DDR2 8
CK0# 32 M_CLK_DDR#2 → M_CLK_DDR#2 8
CK1 164 M_CLK_DDR3 → M_CLK_DDR3 8
CK1# 166 M_CLK_DDR#3 → M_CLK_DDR#3 8
DM0 10 DDR_B_DM0
DM1 26 DDR_B_DM1
DM2 52 DDR_B_DM2
DM3 67 DDR_B_DM3
DM4 130 DDR_B_DM4
DM5 147 DDR_B_DM5
DM6 170 DDR_B_DM6
DM7 185 DDR_B_DM7

SDA 195 ICH_SMBDATA → ICH_SMBDATA 4,14,21,28,29
SCL 197 ICH_SMBCLK → ICH_SMBCLK 4,14,21,28,29
VDDSPD 199 → 3D3V_S0
SA0 198
SA1 200
R46 10KR2J-3-GP → 3D3V_S0
NC#50 50 → PM_EXTTS#1 8
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163

C46 SCD1U16V2ZY-2GP
C38 SC2D2U6D3V3MX-1-GP DY

1D8V_S3

VDD 81 82 87 88 95 96 103 104 111 112 117 118

VSS 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 162 165 168 171 172 177 178 183 184 187 190 193 196 201

MH2 MH2

DDR_VREF_S3 8 M_ODT2
8 M_ODT3
SCD1U16V2ZY-2GP 94
C293 SC2D2U16V5ZY-2GP

DDR2-200P-25-GP-U1
62.10017.B51

REVERSE TYPE High 9.2 mm

SB

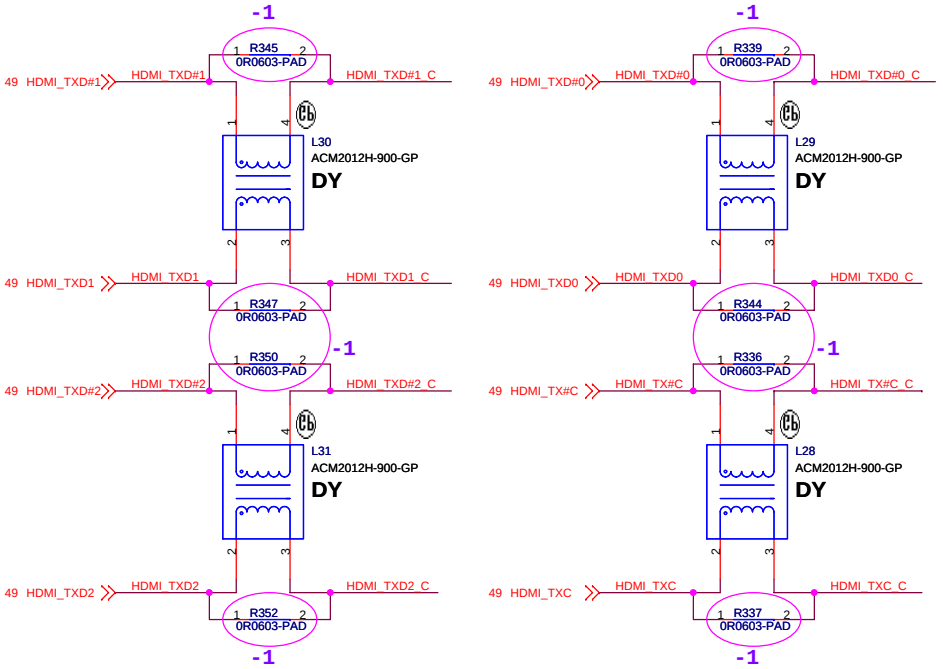
Main source : 62.10017.B51 Foxconn AS0A426-NARN-7F
2nd source : 62.10017.D61 Tyco C-1775860

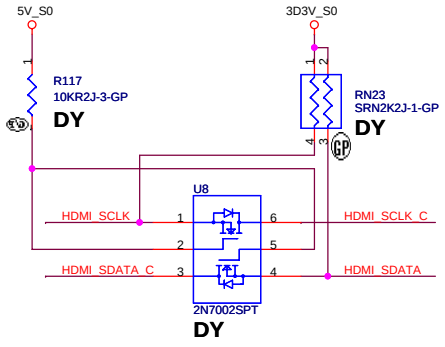
<Core Design>

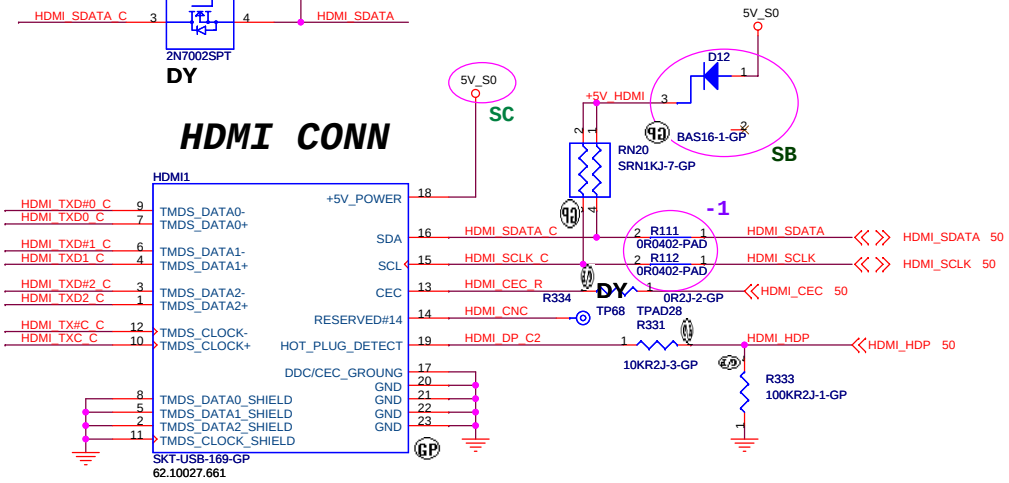
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT2
Size: Custom
Document Number: Hawke-Intel
Rev: -1
Date: Sunday, September 09, 2007
Sheet 15 of 57

HDMI I/F & CONNECTOR







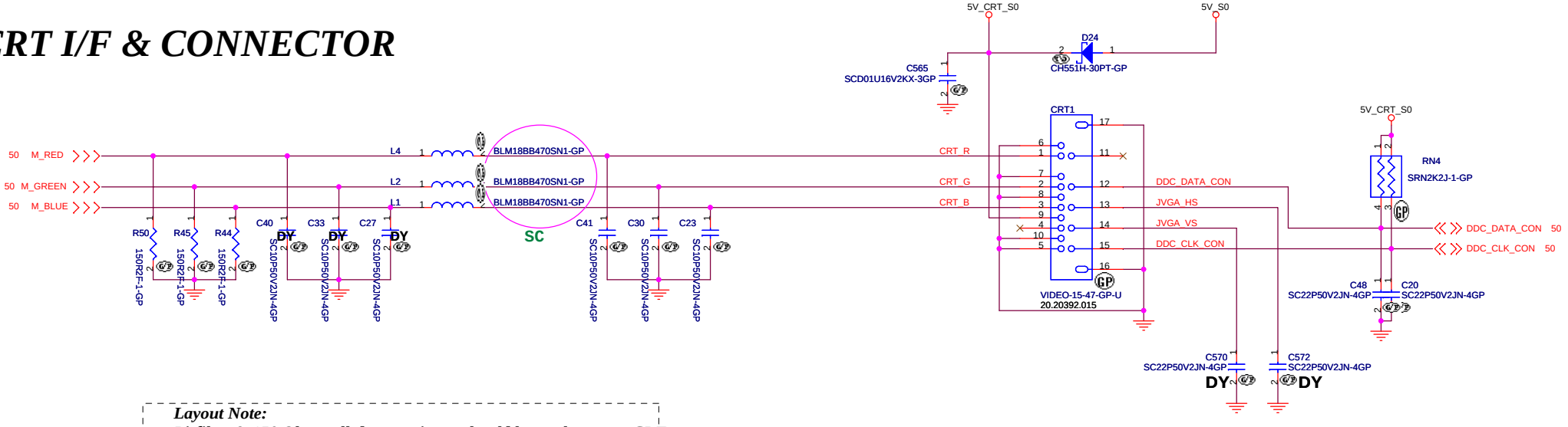
Main source : 62.10027.661 Molex 47408-0201
2nd source : 62.10078.121 Tyco C1759548-1

<Core Design>

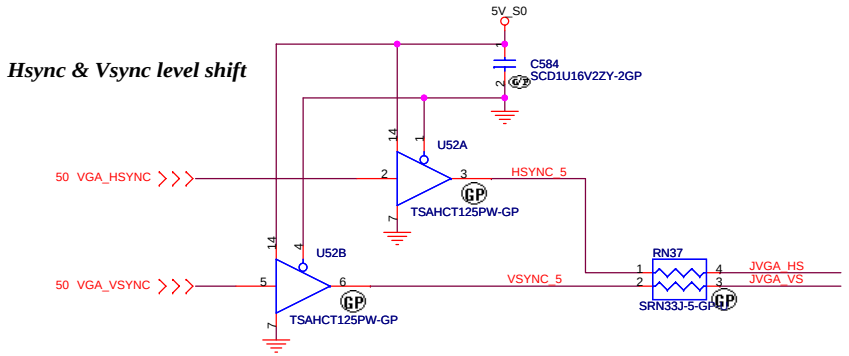
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

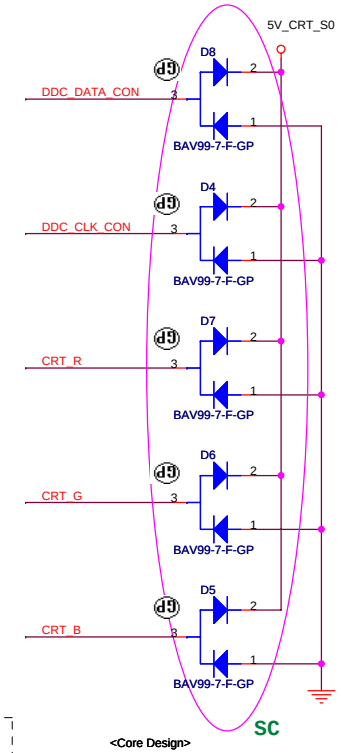
Title: **HDMI**		
Size: A3	Document Number: **Hawke-Intel**	Rev: **-1**
Date: Sunday, September 09, 2007	Sheet 16 of 57	

CRT I/F & CONNECTOR



Layout Note:
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





TP28-75-GP	TP177	1	5V_CRT_S0
TP28-75-GP	TP176	1	DDC_DATA_CON
TP28-75-GP	TP179	1	DDC_CLK_CON
TP28-75-GP	TP178	1	CRT_R
TP28-75-GP	TP180	1	CRT_G
TP28-75-GP	TP182	1	CRT_B
TP28-75-GP	TP181	1	JVGA_HS
TP28-75-GP	TP183	1	JVGA_VS

For AFTE, place them on the some side.

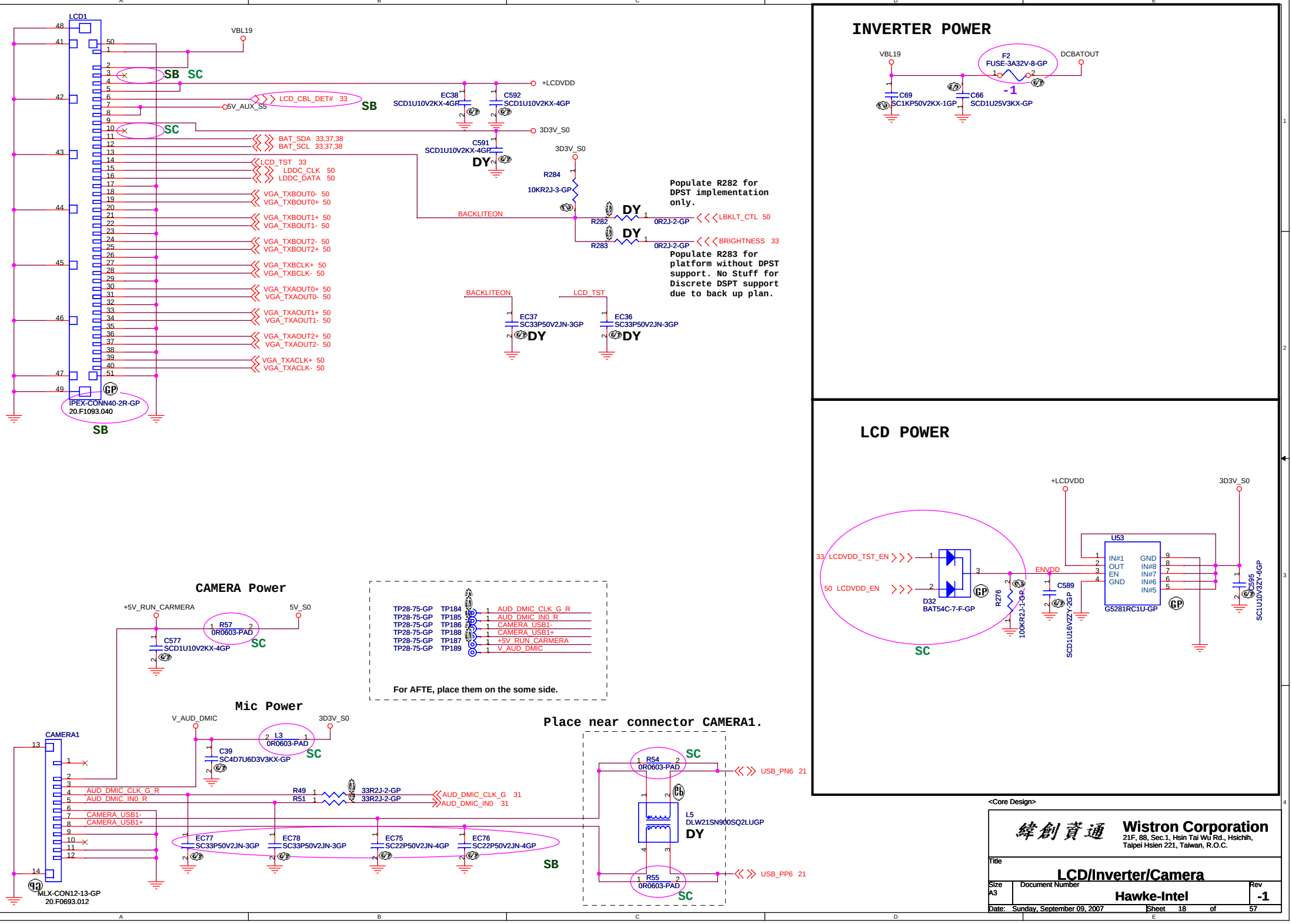
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

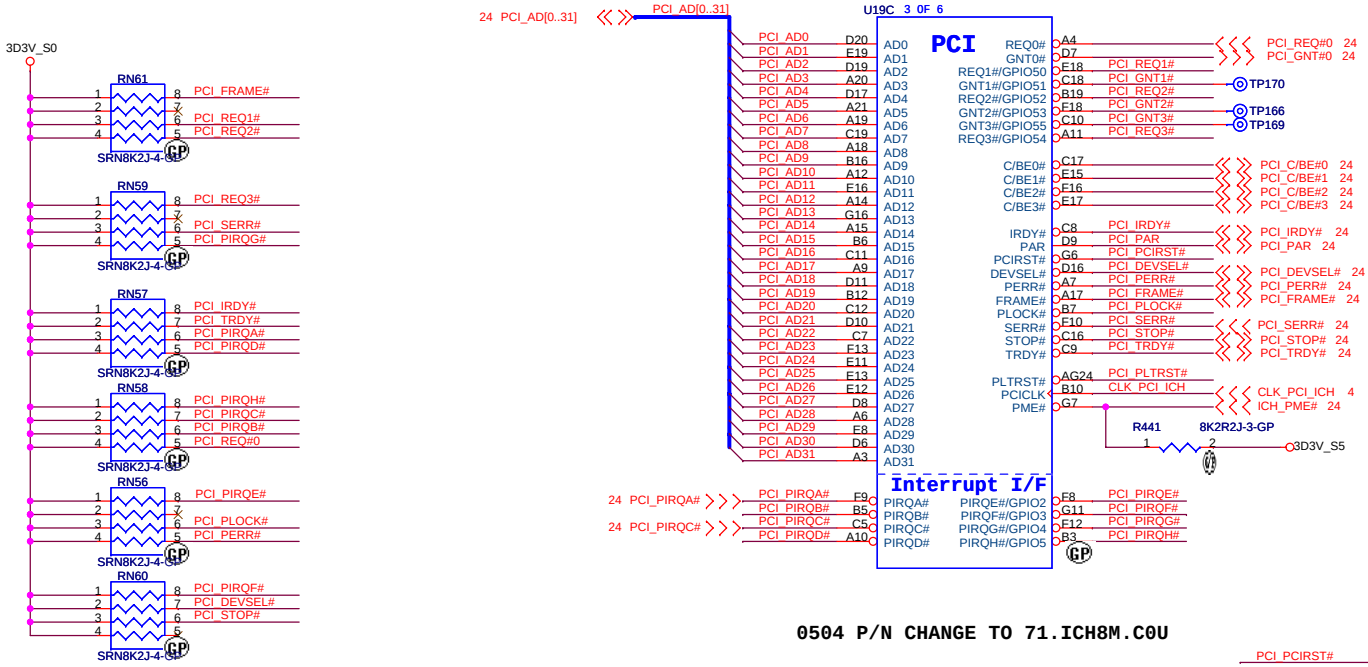
Size: A3 | Document Number: Hawke-Intel | Rev: -1

Date: Sunday, September 09, 2007 | Sheet 17 of 57

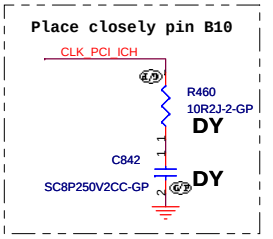

LCD1
IPEX-CONN40-2R-GP
20.F1093.040
VBL19
+LCDVDD
3D3V_S0
5V_AUX_S5
LCD_CBL_DET# 33
BAT_SDA 33,37,38
BAT_SCL 33,37,38
LCD_TST 33
LDDC_CLK 50
LDDC_DATA 50
VGA_TXBOUT0- 50
VGA_TXBOUT0+ 50
VGA_TXBOUT1+ 50
VGA_TXBOUT1- 50
VGA_TXBOUT2- 50
VGA_TXBOUT2+ 50
VGA_TXBCLK+ 50
VGA_TXBCLK- 50
VGA_TXAOUT0+ 50
VGA_TXAOUT0- 50
VGA_TXAOUT1+ 50
VGA_TXAOUT1- 50
VGA_TXAOUT2+ 50
VGA_TXAOUT2- 50
VGA_TXACLK+ 50
VGA_TXACLK- 50
EC38 SCD1U10V2KX-4GP
C592 SCD1U10V2KX-4GP
C591 SCD1U10V2KX-4GP
R284 10KR2J-3-GP
BACKLITEON
R282 0R2J-2-GP
R283 0R2J-2-GP
LBKLT_CTL 50
BRIGHTNESS 33
Populate R282 for DPST implementation only.
Populate R283 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.
EC37 SC33P50V2JN-3GP
EC36 SC33P50V2JN-3GP
INVERTER POWER
F2 FUSE-3A32V-8-GP
DCBATOUT
C69 SC1KP50V2KX-1GP
C66 SCD1U25V3KX-GP
LCD POWER
33 LCDVDD_TST_EN
50 LCDVDD_EN
D32 BAT54C-7-F-GP
R276 100KR2J-1-GP
ENVDD
C589 SCD1U16V2ZY-2GP
U53
G5281RC1U-GP
C595 SC1U10V3ZY-6GP
CAMERA Power
+5V_RUN_CARMERA
5V_S0
R57 0R0603-PAD
C577 SCD1U10V2KX-4GP
TP28-75-GP TP184 AUD_DMIC_CLK_G_R
TP28-75-GP TP185 AUD_DMIC_IN0_R
TP28-75-GP TP186 CAMERA_USB1-
TP28-75-GP TP188 CAMERA_USB1+
TP28-75-GP TP187 +5V_RUN_CARMERA
TP28-75-GP TP189 V_AUD_DMIC
For AFTE, place them on the some side.
Mic Power
V_AUD_DMIC
3D3V_S0
L3 0R0603-PAD
C39 SC4D7U6D3V3KX-GP
CAMERA1
MLX-CON12-13-GP
20.F0693.012
AUD_DMIC_CLK_G_R
AUD_DMIC_IN0_R
CAMERA_USB1-
CAMERA_USB1+
R49 33R2J-2-GP
R51 33R2J-2-GP
AUD_DMIC_CLK_G 31
AUD_DMIC_IN0 31
EC77 SC33P50V2JN-3GP
EC78 SC33P50V2JN-3GP
EC75 SC22P50V2JN-4GP
EC76 SC22P50V2JN-4GP
Place near connector CAMERA1.
R54 0R0603-PAD
R55 0R0603-PAD
L5 DLW21SN900SQ2LUGP
USB_PN6 21
USB_PP6 21
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LCD/Inverter/Camera
Size A3
Document Number
Hawke-Intel
Rev -1
Date: Sunday, September 09, 2007
Sheet 18 of 57

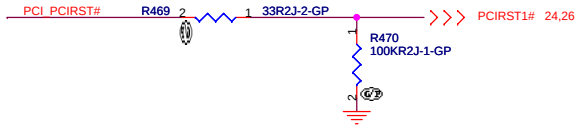
PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0



0504 P/N CHANGE TO 71.ICH8M.C0U

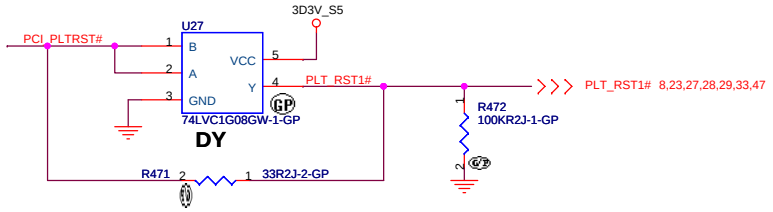


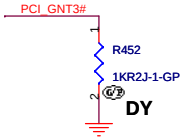


ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *





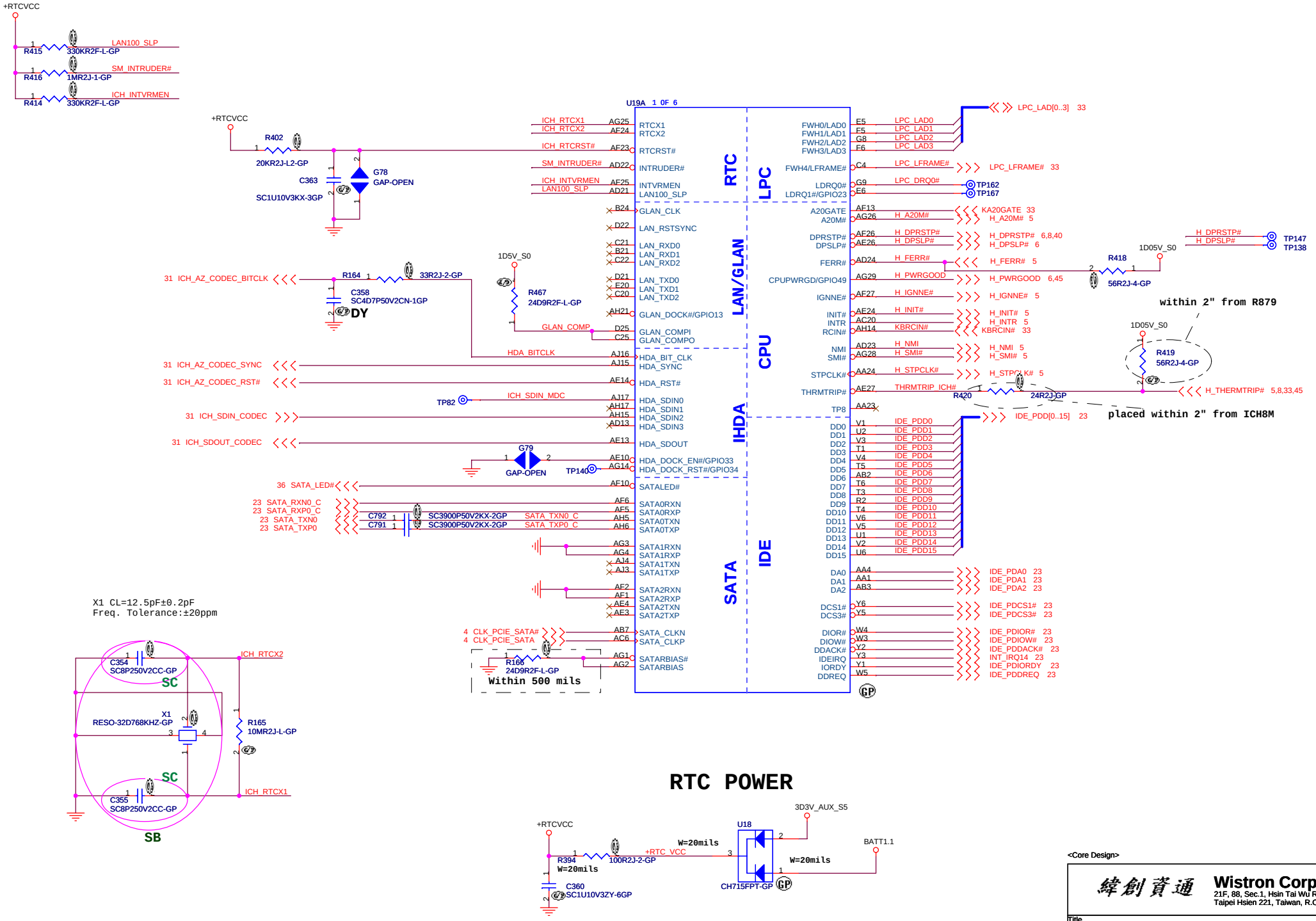
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(1/4)-PCI/INT

Size: A3 | Document Number: Hawke-Intel | Rev: -1

Date: Sunday, September 09, 2007 | Sheet 19 of 57



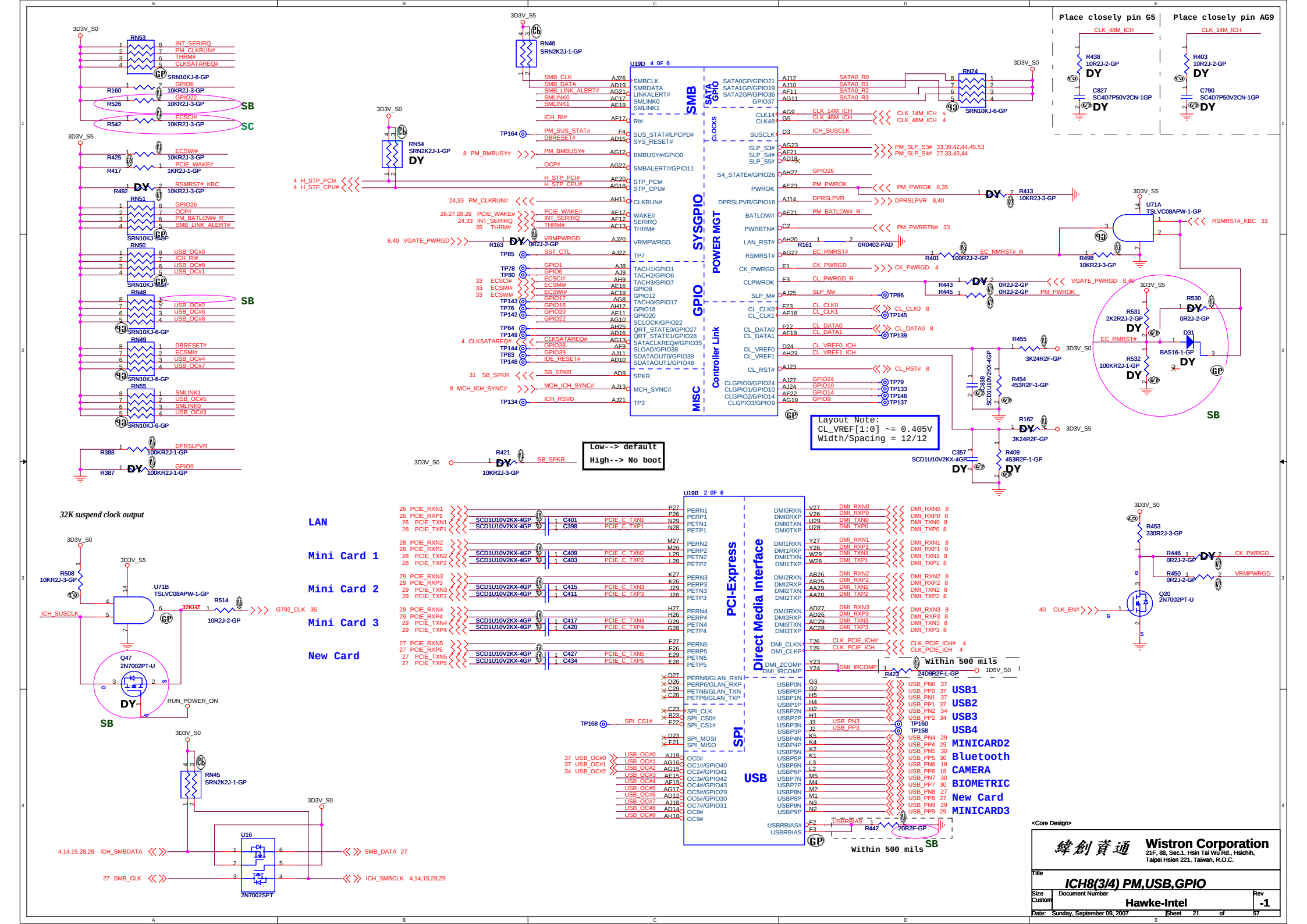
<Core Design>

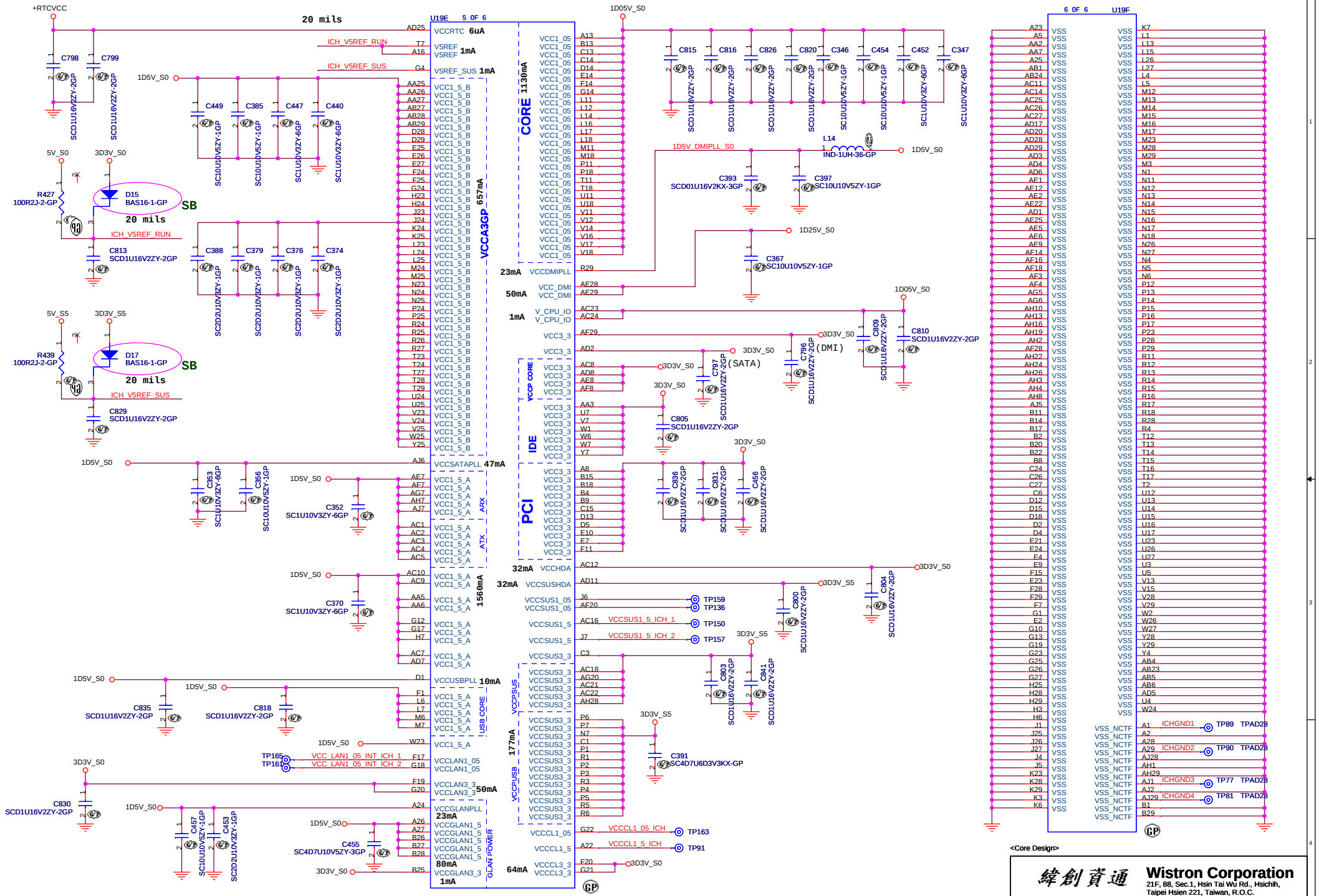
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(2/4) LAN,HD,IDE,LPC

Size	Document Number	Rev
A3	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 20 of 57


Place closely pin G5
Place closely pin AG9
U19D 4 OF 6
U19B 2 OF 6
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
PCI-Express
Direct Media Interface
SPI
USB
Layout Note:
CL_VREF[1:0] ~= 0.405V
Width/Spacing = 12/12
Low--> default
High--> No boot
32K suspend clock output
LAN
Mini Card 1
Mini Card 2
Mini Card 3
New Card
USB1
USB2
USB3
USB4
MINICARD2
Bluetooth
CAMERA
BIOMETRIC
New Card
MINICARD3
Within 500 mils
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH8(3/4) PM,USB,GPIO
Hawke-Intel
-1
Date: Sunday, September 09, 2007
Sheet 21 of 57



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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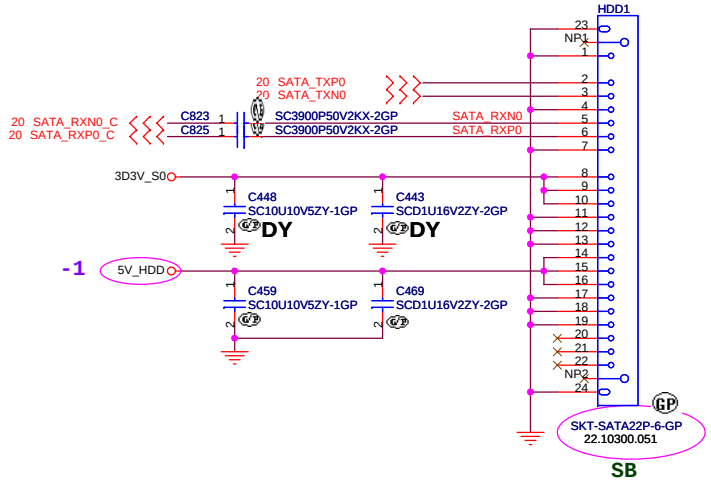
Title: ICH8(4/4) POWER&GND

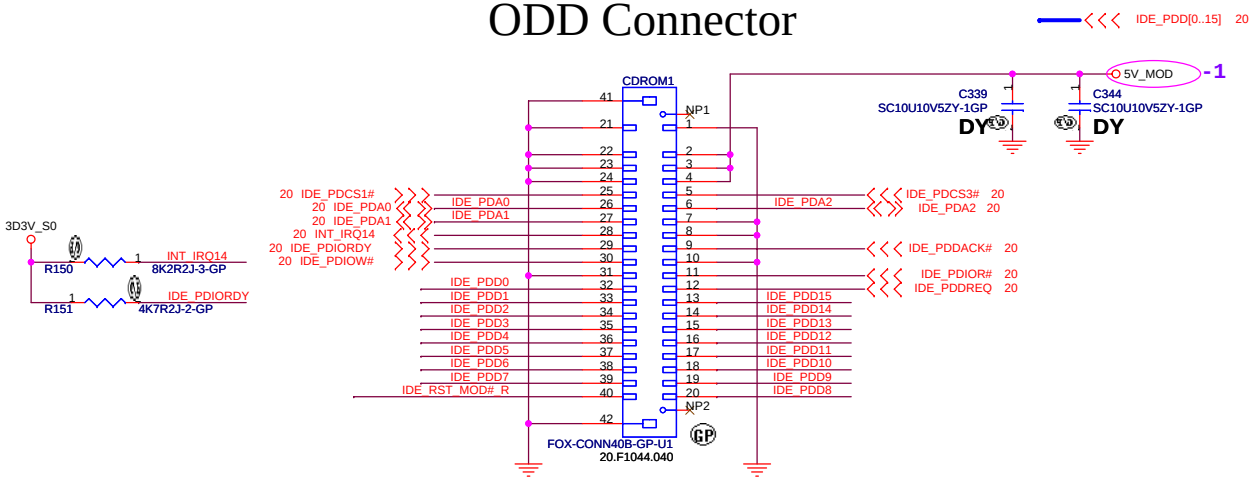
Size	Document Number	Rev
Custom	Hawke-Intel	-1

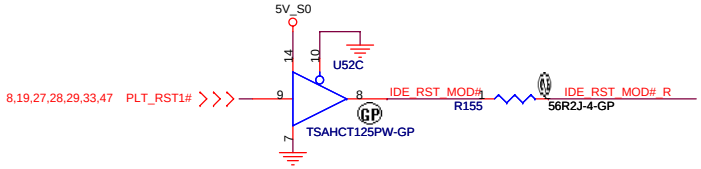
Date: Sunday, September 09, 2007 Sheet 22 of 57

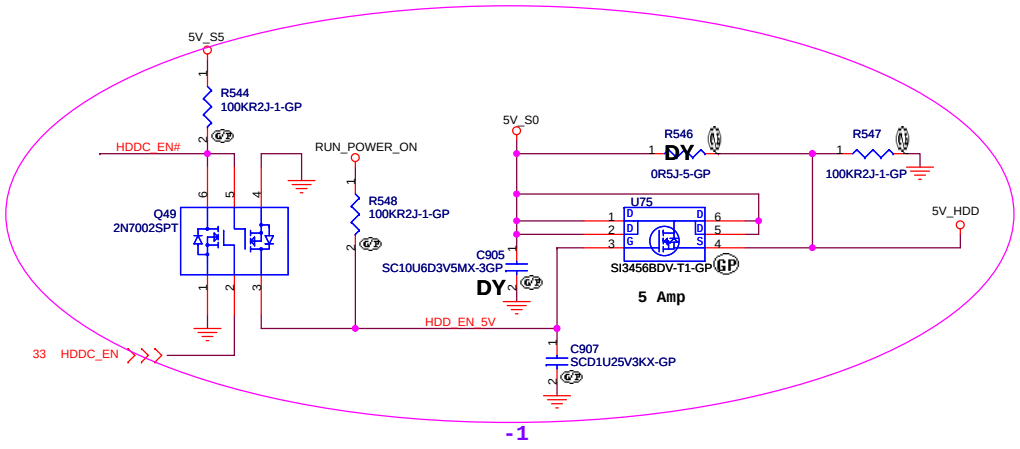
SATA HDD Connector

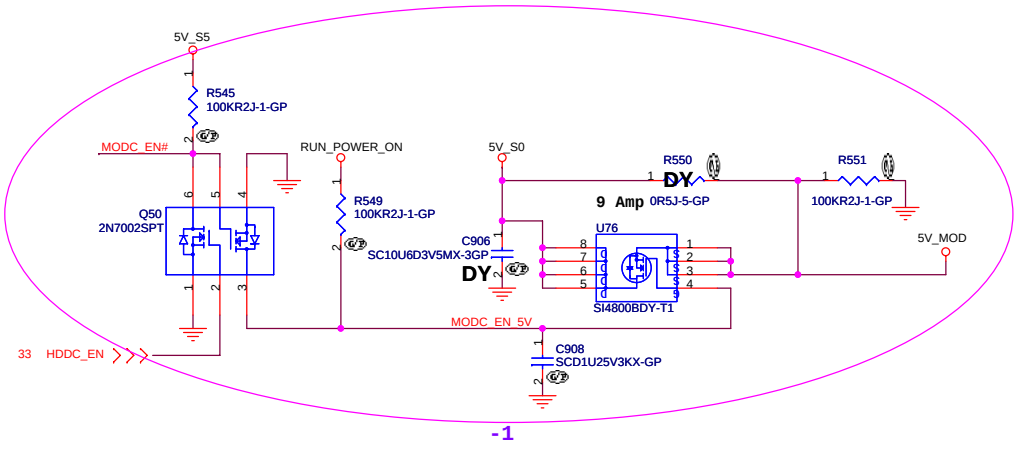


ODD Connector





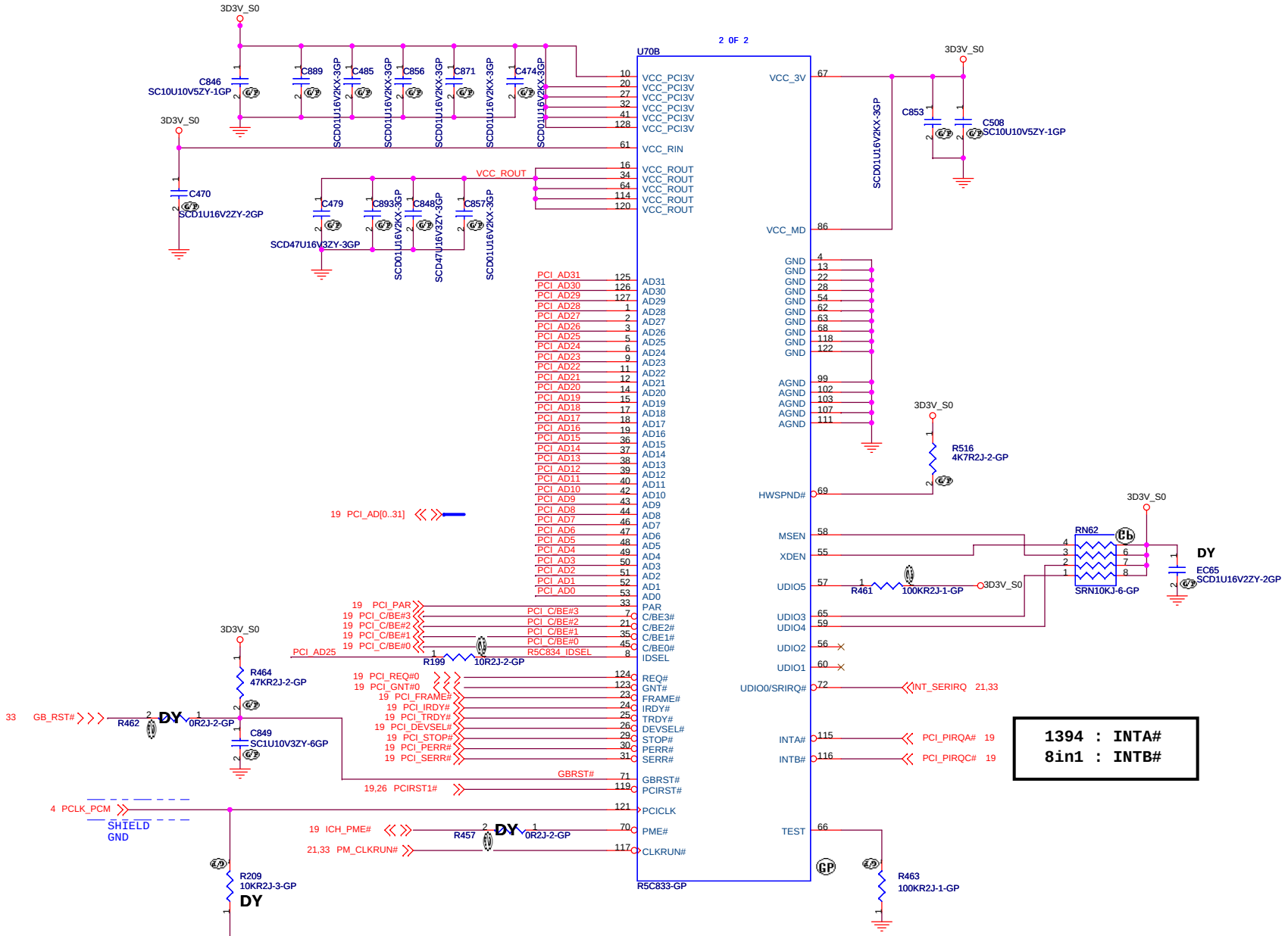




<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD/ODD	
Size A3	Document Number Hawke-Intel	Rev -1
Date: Sunday, September 09, 2007	Sheet 23 of 57	



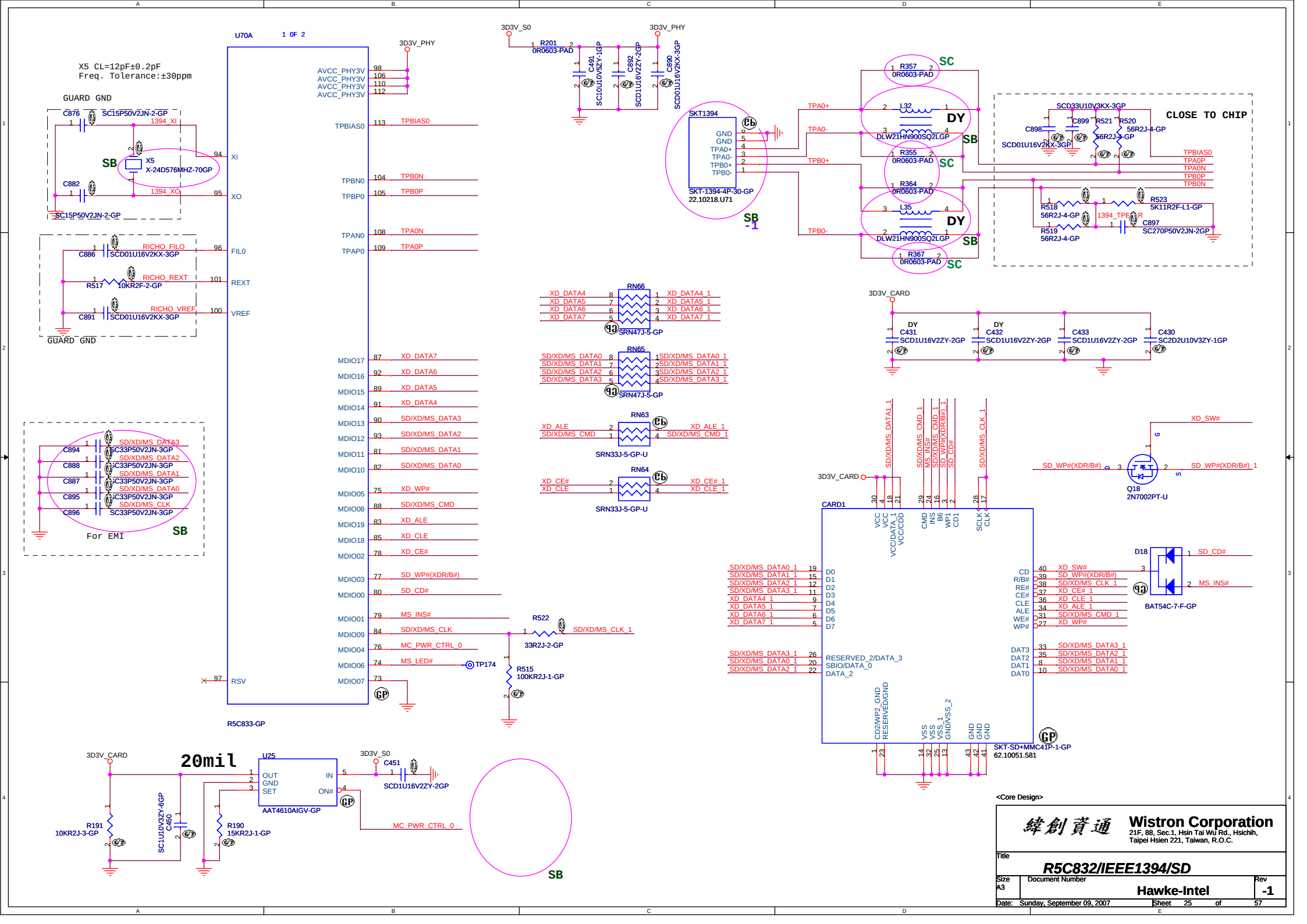
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***R5C833/PCI***

Size	Document Number	Rev
A3	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 24 of 57


U70A
1 OF 2
R5C833-GP
X5 CL=12pF±0.2pF
Freq. Tolerance:±30ppm
GUARD GND
SC15P50V2JN-2-GP
X5
X-24D576MHZ-70GP
SB
RICHO_FILO
RICHO_REXT
RICHO_VREF
SCD01U16V2KX-3GP
10KR2F-2-GP
For EMI
3D3V_PHY
3D3V_S0
3D3V_CARD
SKT1394
SKT-1394-4P-30-GP
22.10218.U71
DY
SC
CLOSE TO CHIP
SRN47J-5-GP
SRN33J-5-GP-U
CARD1
SKT-SD+MMC41P-1-GP
62.10051.581
BAT54C-7-F-GP
2N7002PT-U
AAT4610AIGV-GP
20mil
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C832/IEEE1394/SD
Hawke-Intel
-1
Sunday, September 09, 2007
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	R181	R176	R172	R173	R174	R175	C377	C378
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01u
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY

X3 CL=12pF±0.2pF
Freq. Tolerance:±30ppm

R178 DY 10MR2J-L-GP
X3 XTAL-25MHZ-96GP
LANX2 LANX1
C390 SC12P50V2JN-3GP
C387 SC12P50V2JN-3GP
SB

U21 88E8039-A0-GP

2D5V_LAN_S5 3D3V_LAN_S5 1D2V_LAN_S5

AVDDL VDDO_TTL VDD25 AVDD VDD

NC#34 NC#35 NC#36 NC#37

LOM_DISABLE# VAUX_AVLBL SWITCH_VCC VMAIN_AVLBL SWITCH_VAUX RSET CTRL12 CTRL25 HSDACP HSDACN

WAKE# PERST# REFCLKP REFCLKN PCIE_TXN PCIE_TXP PCIE_RXN PCIE_RXP

PCIE_WAKE# 21,27,28,29
PCIRST1# 19,24
CLK_PCIE_LAN 4
CLK_PCIE_LAN# 4
PCIE_RXN1 21
PCIE_RXP1 21
PCIE_TXN1 21
PCIE_TXP1 21

LAN_RXN1 C423 SCD1U10V2KX-4GP
LAN_RXP1 C422 SCD1U10V2KX-4GP

LED_LINK# NC#62 LED_SPEED# LED_ACT#
LINK_LED#
LAN100M_LED# 27
ACT_LED# 27

XTALI XTALO
LANX1 LANX2

RXN TXN NC#27 NC#31 RXP TXP NC#26 NC#30 VPD_DATA VPD_CLK TSTPT TESTMODE PU_VDDO_TTL#42 PU_VDDO_TTL#43 GND

MDI0- MDI1- MDI0+ MDI1+

TP153 TPAD28

VPD_CLK VPD_DATA

R181 DY 4K7R2J-2-GP
R180 4K7R2J-2-GP

3D3V_LAN_S5

R429 4K7R2J-2-GP

Marvell recommend:
2K Ohm

R437 0R0402-PAD
3D3V_S0

LOM_DISABLE#
LANSC TPAD28 TP154
LANSV TPAD28 TP156
LANPWR
LANRSET R176 1K91R2F-1-GP
CTRL12
CTRL25
LANHP TPAD28 TP152
LANHN TPAD28 TP151

U24 AT24C08AN-1-GP
A0 A1 A2 GND VCC WP SCL SDA
EEWP VPD_CLK VPD_DATA

R451 4K7R2J-2-GP
R447 4K7R2J-2-GP
R456 0R2J-2-GP
DY
EEWP
R459 0R2J-2-GP

Pull up for AT24C08 another pull low

MDI0+ R175 MDIS0_LAN 49D9R2F-GP C378 SCD01U16V2KX-3GP
MDI0- R174 49D9R2F-GP
MDI1+ R173 MDIS1_LAN 49D9R2F-GP C377 SCD01U16V2KX-3GP
MDI1- R172 49D9R2F-GP

LAN100M_LED# R185 10KR2J-3-GP
Q19 CH3904PT-GP
LINK_LED#
LAN10M_LED# 27
R189 DY 0R2J-2-GP

3D3V_LAN_S5 C408 SC1KP50V2KX-1GP C414 SC1U6D3V2KX-GP C400 SC1U6D3V2KX-GP
2D5V_LAN_S5 C424 SCD1U10V2KX-4GP C418 SC1KP50V2KX-1GP C380 SC1KP50V2KX-1GP C381 SC1U6D3V2KX-GP
1D2V_LAN_S5 C394 SC1U6D3V2KX-GP C425 SC1KP50V2KX-1GP C386 SC1U6D3V2KX-GP C410 SC1KP50V2KX-1GP C402 SC1U6D3V2KX-GP C395 SC1KP50V2KX-1GP

R159 DY 0R3-0-U-GP
3D3V_S5
C349 SCD1U10V2KX-4GP
R154 10KR2J-3-GP
Q11 AO3403-GP
C364 SC10U6D3V5KX-1GP
Q10 2N7002PT-U
33 PM_LAN_ENABLE

PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL

3D3V_LAN_S5
C361 SCD1U10V2KX-4GP
C365 SC4D7U6D3V5KX-3GP
R410 4K7R2J-2-GP
CTRL25
Q13 2SB772PT-1-GP
2D5V_LAN_S5
C373 SC4D7U6D3V5KX-3GP
C371 SCD1U10V2KX-4GP

8053:CTRL25.
8055:CTRL18.
8053:2.5V.
8055:1.8V.

PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL

3D3V_LAN_S5
R458 4K7R2J-2-GP
CTRL12
C441 SCD1U10V2KX-4
C442 SC4D7U6D3V5KX-3GP
Q21 2SB772PT-1-GP
1D2V_LAN_S5
C444 SCD1U10V2KX-4GP
C446 SC4D7U6D3V5KX-3GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN MARVELL
Size: A3
Document Number: Hawke-Intel
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Date: Sunday, September 09, 2007
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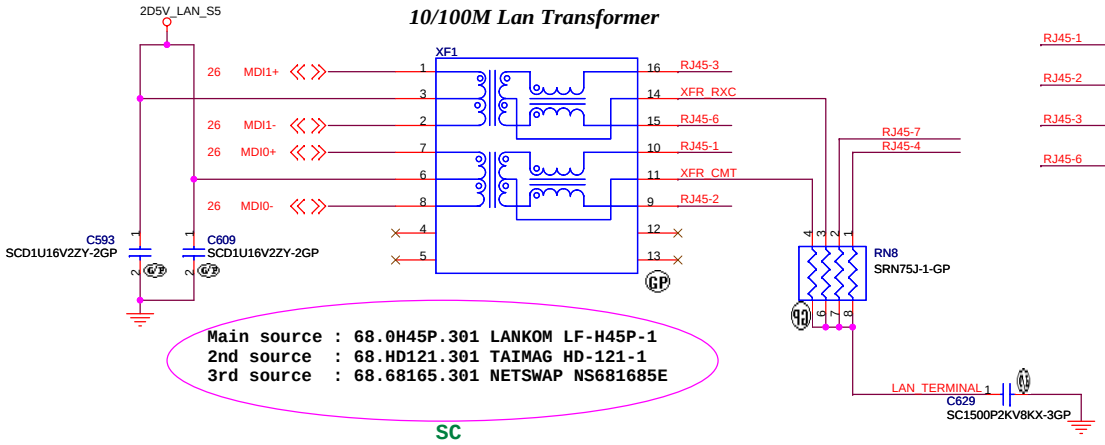
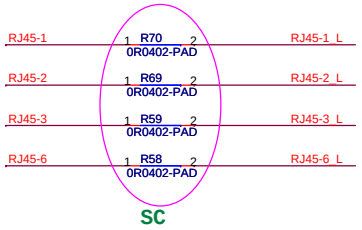
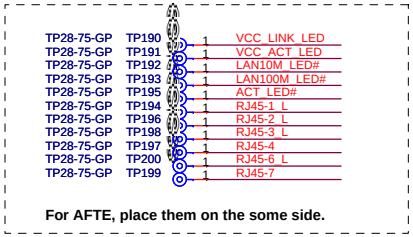
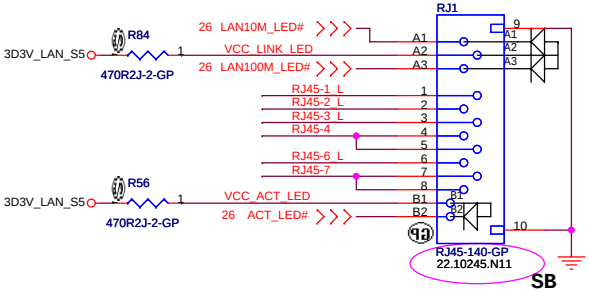
RJ45 Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.





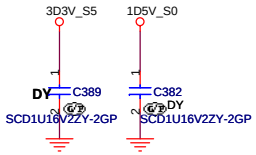




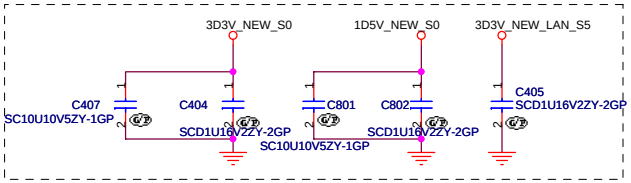
Yellow LED:TX/RX
Orange LED:Speed 100
Green LED:Speed 10

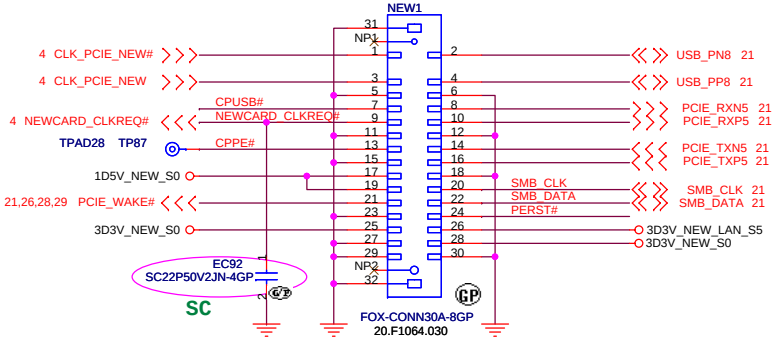
NEWCARD Connector

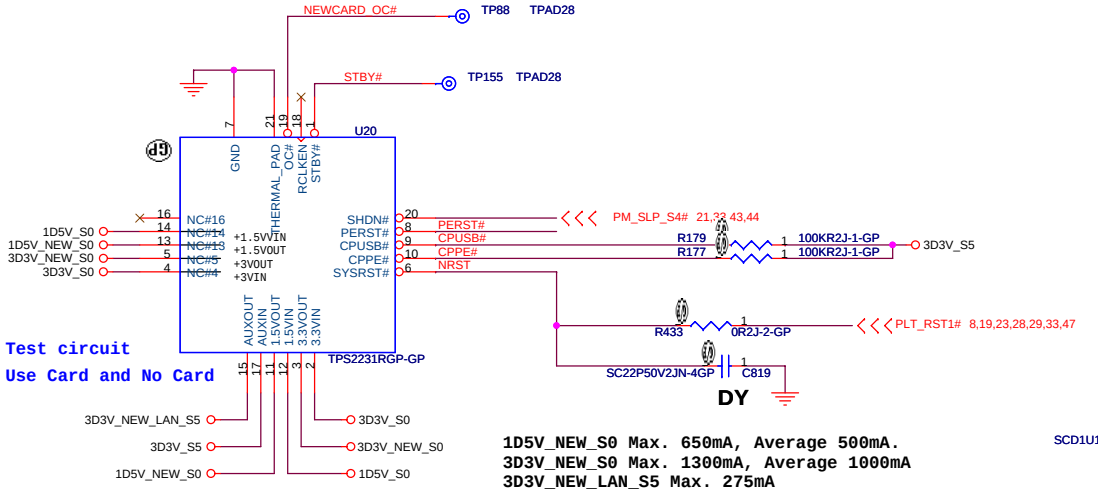
Place them Near to Chip



Place them Near to Connector

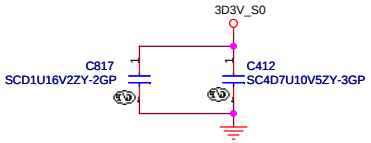






Test circuit
Use Card and No Card

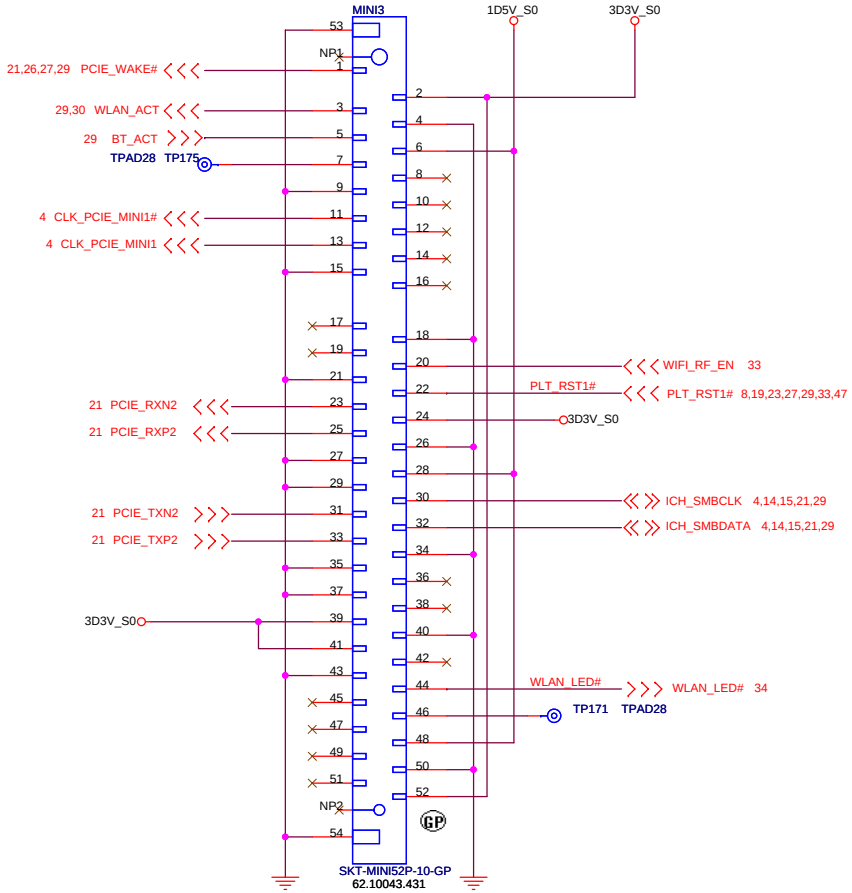
1D5V_NEW_S0 Max. 650mA, Average 500mA.
3D3V_NEW_S0 Max. 1300mA, Average 1000mA
3D3V_NEW_LAN_S5 Max. 275mA



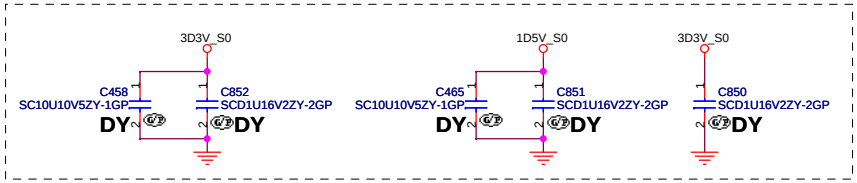
<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LAN connector/NEW CARD	
Size A3	Document Number Hawke-Intel	Rev -1
Date: Sunday, September 09, 2007	Sheet 27 of 57	

Mini Card Connector 1(802.11a/b/g)



Main source : 20.F0992.052 P-Two A54452-A0G16-N
2nd source : 62.10043.551 Tyco 1759553-1



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

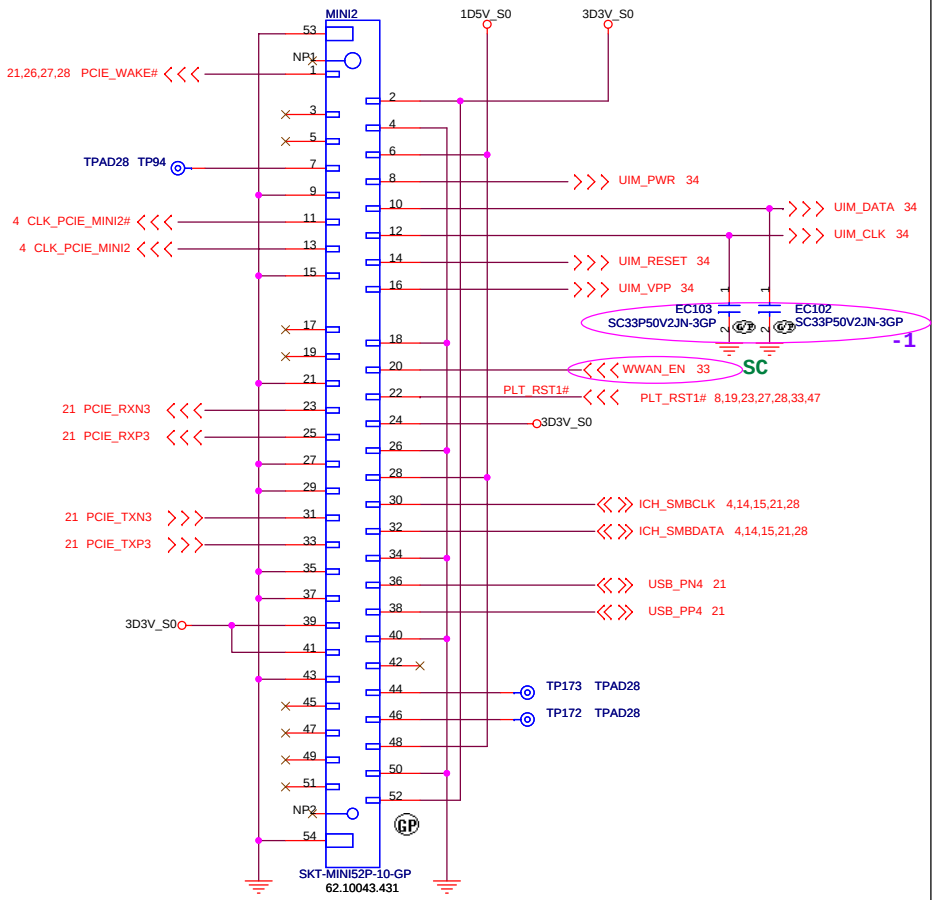
Title: **MINI CARD CONN 1**

Size	Document Number	Rev
A3	Hawke-Intel	-1

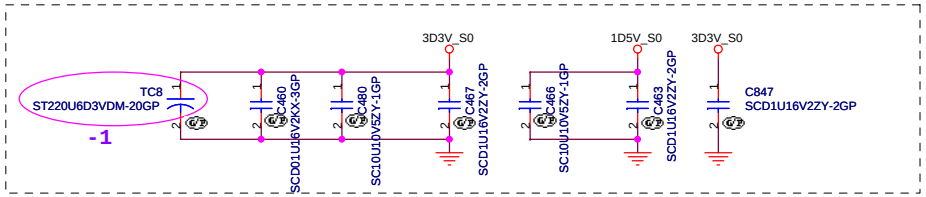
Date: Sunday, September 09, 2007 Sheet 28 of 57

Mini Card Connector

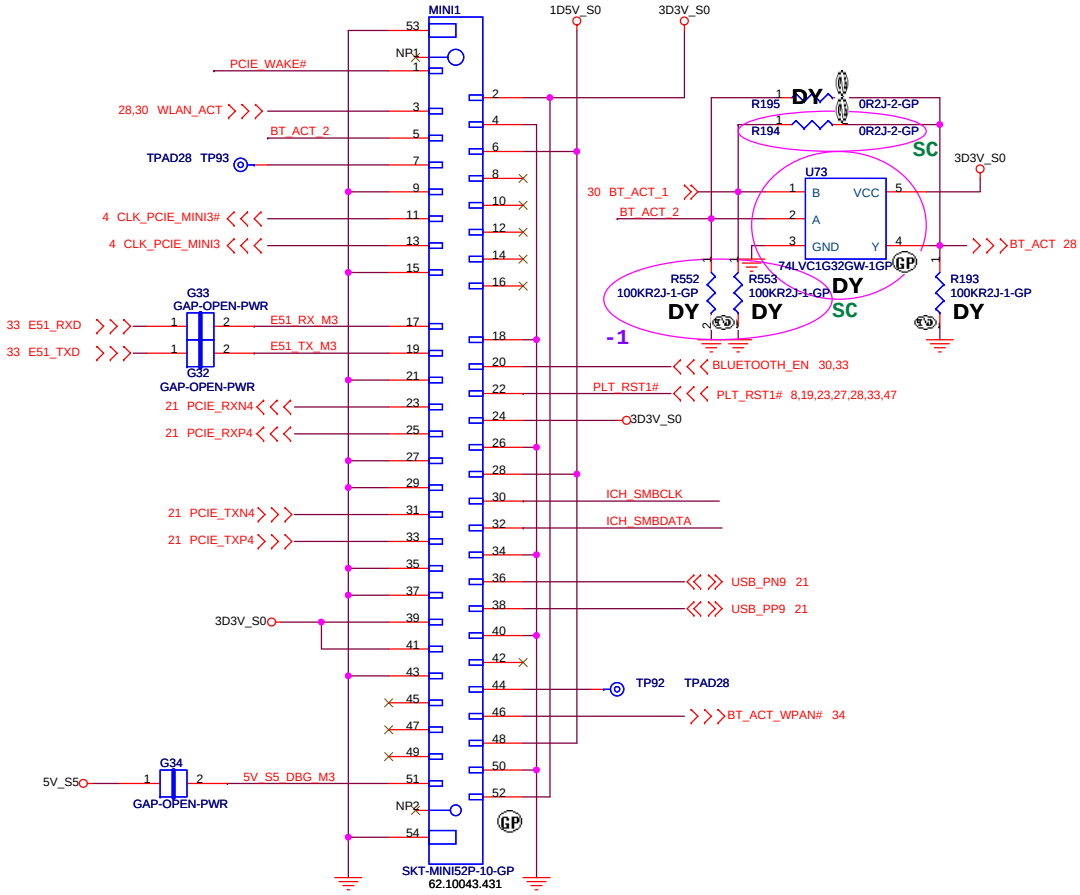
Mini Card Connector 2(WWAN)

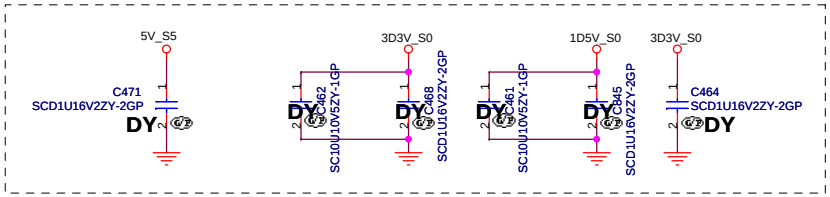


Main source : 20.F0992.052 P-Two A54452-A0G16-N
2nd source : 62.10043.551 Tyco 1759553-1



Mini Card Connector 3(Robson/BT)





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD CONN 2 & 3**

Size	Document Number	Rev
A3	Hawke-Intel	-1

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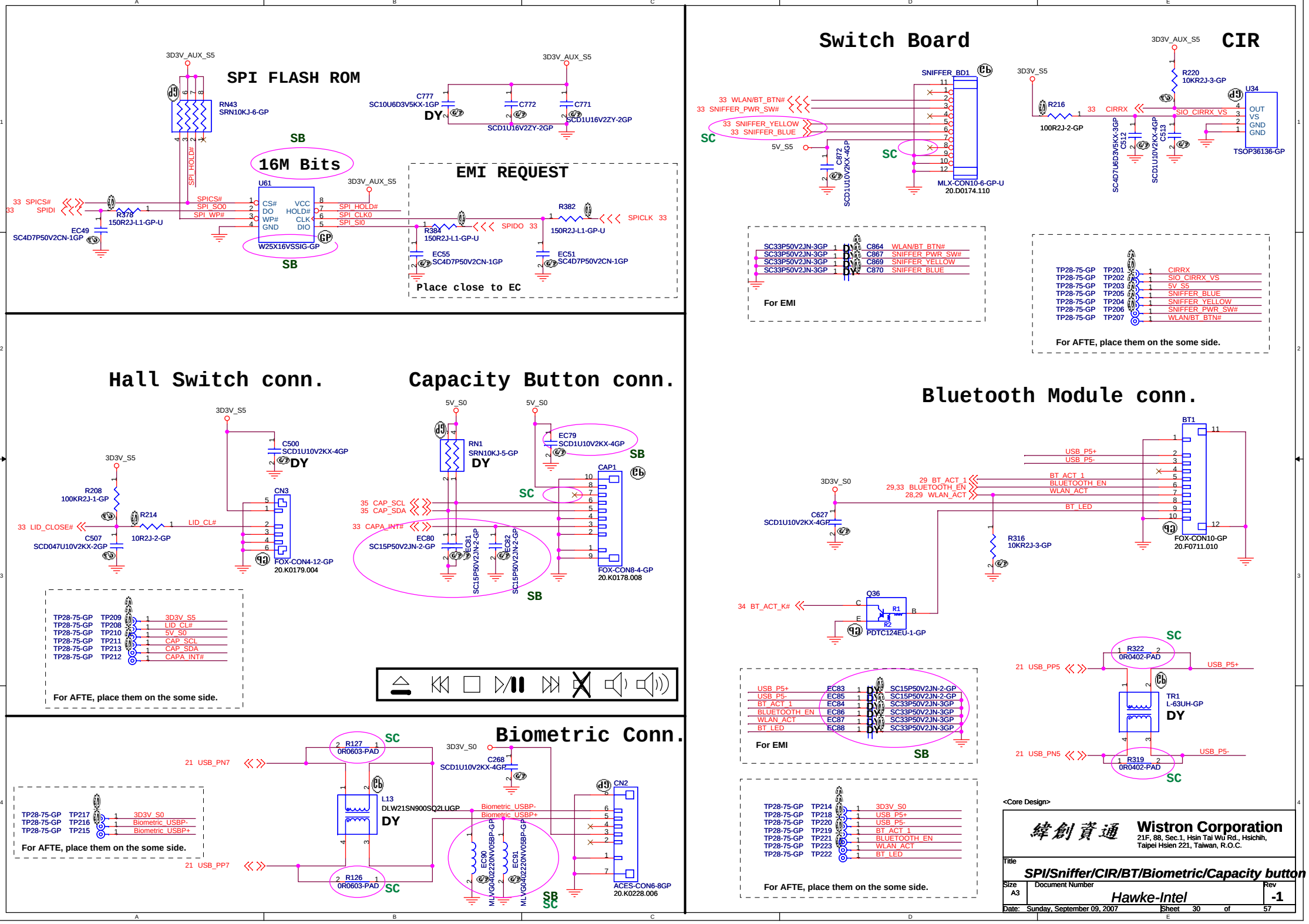
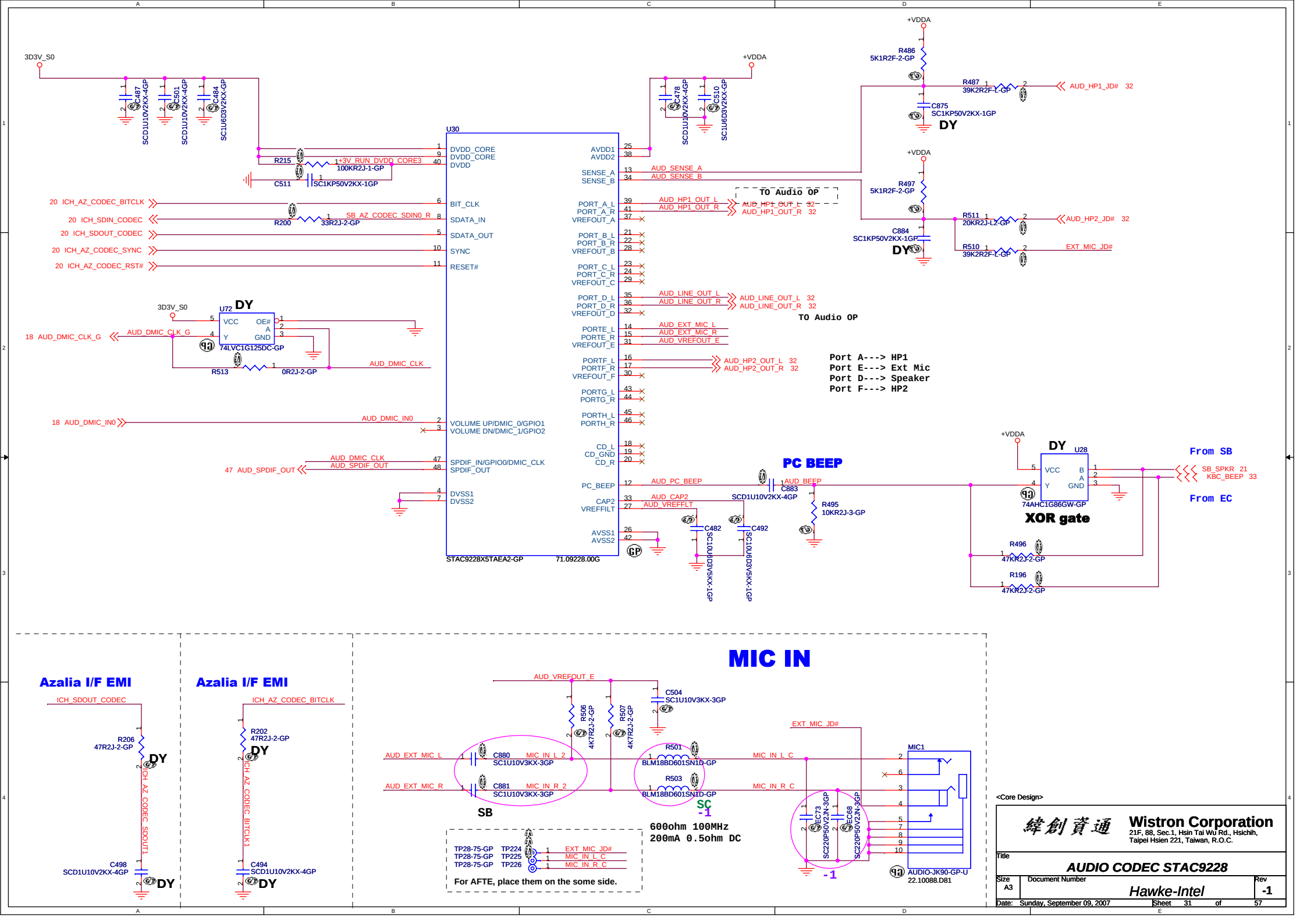
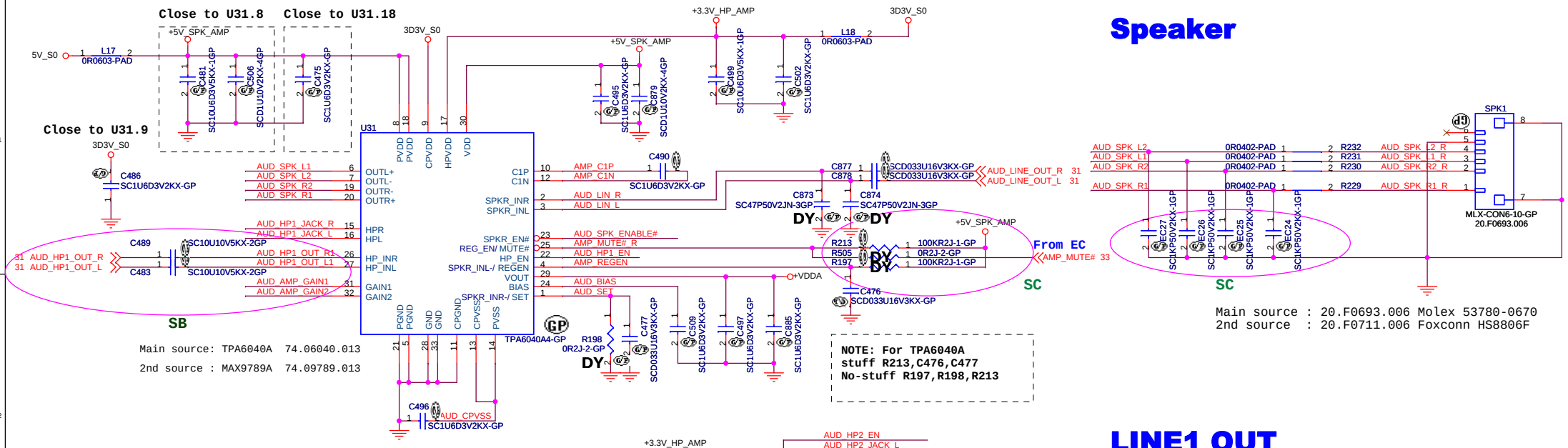
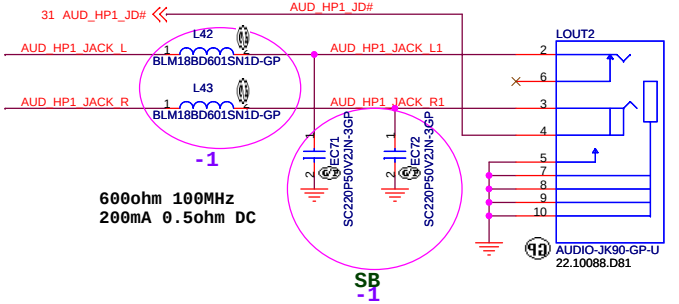

SPI FLASH ROM
3D3V_AUX_S5
RN43
SRN10KJ-6-GP
SPI_HOLD#
SB
16M Bits
U61
CS#
DO
WP#
GND
VCC
HOLD#
CLK
DIO
W25X16VSSIG-GP
SPICS#
SPI_SO0
SPI_WP#
SPI_HOLD#
SPI_CLK0
SPI_SI0
33 SPICS#
33 SPIDI
R378
150R2J-L1-GP-U
EC49
SC4D7P50V2CN-1GP
C777
SC10U6D3V5KX-1GP
DY
C772
C771
SCD1U16V2ZY-2GP
EMI REQUEST
R384
150R2J-L1-GP-U
SPIDO 33
R382
SPICLK 33
EC55
EC51
Place close to EC
Switch Board
SNIFFER_BD1
33 WLAN/BT_BTN#
33 SNIFFER_PWR_SW#
33 SNIFFER_YELLOW
33 SNIFFER_BLUE
SC
5V_S5
C872
SCD1U10V2KX-4GP
MLX-CON10-6-GP-U
20.D0174.110
SC33P50V2JN-3GP
C864 WLAN/BT_BTN#
C867 SNIFFER_PWR_SW#
C869 SNIFFER_YELLOW
C870 SNIFFER_BLUE
For EMI
CIR
3D3V_S5
R216
100R2J-2-GP
33 CIRRX
R220
10KR2J-3-GP
SIO_CIRRX_VS
U34
OUT
VS
GND
GND
TSOP36136-GP
SC47U6D3V5KX-3GP
C512
SCD1U10V2KX-4GP
C513
TP28-75-GP TP201 CIRRX
TP28-75-GP TP202 SIO_CIRRX_VS
TP28-75-GP TP203 5V_S5
TP28-75-GP TP205 SNIFFER_BLUE
TP28-75-GP TP204 SNIFFER_YELLOW
TP28-75-GP TP206 SNIFFER_PWR_SW#
TP28-75-GP TP207 WLAN/BT_BTN#
For AFTE, place them on the some side.
Hall Switch conn.
3D3V_S5
C500
SCD1U10V2KX-4GP
DY
R208
100KR2J-1-GP
R214
10R2J-2-GP
33 LID_CLOSE#
LID_CL#
C507
SCD047U10V2KX-2GP
CN3
FOX-CON4-12-GP
20.K0179.004
TP28-75-GP TP209 3D3V_S5
TP28-75-GP TP208 LID_CL#
TP28-75-GP TP210 5V_S0
TP28-75-GP TP211 CAP_SCL
TP28-75-GP TP213 CAP_SDA
TP28-75-GP TP212 CAPA_INT#
For AFTE, place them on the some side.
Capacity Button conn.
5V_S0
RN1
SRN10KJ-5-GP
DY
EC79
SCD1U10V2KX-4GP
SB
CAP1
SC
35 CAP_SCL
35 CAP_SDA
33 CAPA_INT#
EC80
SC15P50V2JN-2-GP
EC81
EC82
FOX-CON8-4-GP
20.K0178.008
SB
Bluetooth Module conn.
3D3V_S0
BT1
USB_P5+
USB_P5-
29 BT_ACT_1
29,33 BLUETOOTH_EN
28,29 WLAN_ACT
BT_ACT_1
BLUETOOTH_EN
WLAN_ACT
BT_LED
C627
SCD1U10V2KX-4GP
R316
10KR2J-3-GP
FOX-CON10-GP
20.F0711.010
34 BT_ACT_K#
Q36
R1
R2
PDTC124EU-1-GP
USB_P5+ EC83 SC15P50V2JN-2-GP
USB_P5- EC85 SC15P50V2JN-2-GP
BT_ACT_1 EC84 SC33P50V2JN-3GP
BLUETOOTH_EN EC86 SC33P50V2JN-3GP
WLAN_ACT EC87 SC33P50V2JN-3GP
BT_LED EC88 SC33P50V2JN-3GP
For EMI
SB
SC
21 USB_PP5
R322
0R0402-PAD
USB_P5+
TR1
L-63UH-GP
DY
21 USB_PN5
R319
0R0402-PAD
USB_P5-
TP28-75-GP TP214 3D3V_S0
TP28-75-GP TP218 USB_P5+
TP28-75-GP TP220 USB_P5-
TP28-75-GP TP219 BT_ACT_1
TP28-75-GP TP221 BLUETOOTH_EN
TP28-75-GP TP223 WLAN_ACT
TP28-75-GP TP222 BT_LED
For AFTE, place them on the some side.
Biometric Conn.
21 USB_PN7
R127
0R0603-PAD
SC
3D3V_S0
C268
SCD1U10V2KX-4GP
L13
DLW21SN900SQ2LUGP
DY
Biometric_USBP-
Biometric_USBP+
CN2
ACES-CON6-8GP
20.K0228.006
21 USB_PP7
R126
0R0603-PAD
EC90
EC91
MLVG0402220NV05BP-GP
SB
SC
TP28-75-GP TP217 3D3V_S0
TP28-75-GP TP216 Biometric_USBP-
TP28-75-GP TP215 Biometric_USBP+
For AFTE, place them on the some side.
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SPI/Sniffer/CIR/BT/Biometric/Capacity button
Size A3
Document Number
Hawke-Intel
Rev -1
Date: Sunday, September 09, 2007
Sheet 30 of 57


3D3V_S0
+VDDA
U30
STAC9228X5TAEA2-GP
71.09228.00G
DVDD_CORE
DVDD_CORE
DVDD
BIT_CLK
SDATA_IN
SDATA_OUT
SYNC
RESET#
AVDD1
AVDD2
SENSE_A
SENSE_B
PORT_A_L
PORT_A_R
VREFOUT_A
PORT_B_L
PORT_B_R
VREFOUT_B
PORT_C_L
PORT_C_R
VREFOUT_C
PORT_D_L
PORT_D_R
VREFOUT_D
PORTE_L
PORTE_R
VREFOUT_E
PORTF_L
PORTF_R
VREFOUT_F
PORTG_L
PORTG_R
PORTH_L
PORTH_R
CD_L
CD_GND
CD_R
PC_BEEP
CAP2
VREFFILT
AVSS1
AVSS2
DVSS1
DVSS2
SPDIF_IN/GPIO0/DMIC_CLK
SPDIF_OUT
VOLUME UP/DMIC_0/GPIO1
VOLUME DN/DMIC_1/GPIO2
AUD_SENSE_A
AUD_SENSE_B
AUD_HP1_OUT_L
AUD_HP1_OUT_R
AUD_LINE_OUT_L
AUD_LINE_OUT_R
AUD_EXT_MIC_L
AUD_EXT_MIC_R
AUD_VREFOUT_E
AUD_HP2_OUT_L
AUD_HP2_OUT_R
AUD_PC_BEEP
AUD_CAP2
AUD_VREFFLT
TO Audio OP
Port A---> HP1
Port E---> Ext Mic
Port D---> Speaker
Port F---> HP2
PC BEEP
ICH_AZ_CODEC_BITCLK
ICH_SDIN_CODEC
ICH_SDOUT_CODEC
ICH_AZ_CODEC_SYNC
ICH_AZ_CODEC_RST#
SB_AZ_CODEC_SDIN0_R
AUD_DMIC_CLK_G
AUD_DMIC_CLK
AUD_DMIC_IN0
AUD_SPDIF_OUT
74LVC1G125DC-GP
74AHC1G86GW-GP
XOR gate
From SB
From EC
SB_SPKR
KBC_BEEP
AUD_HP1_JD#
AUD_HP2_JD#
EXT_MIC_JD#
Azalia I/F EMI
ICH_SDOUT_CODEC
ICH_AZ_CODEC_BITCLK
MIC IN
AUD_VREFOUT_E
AUD_EXT_MIC_L
AUD_EXT_MIC_R
MIC_IN_L_2
MIC_IN_R_2
MIC_IN_L_C
MIC_IN_R_C
EXT_MIC_JD#
SB
600ohm 100MHz
200mA 0.5ohm DC
For AFTE, place them on the some side.
MIC1
AUDIO-JK90-GP-U
22.10088.D81
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC STAC9228
Hawke-Intel
Size A3
Rev -1
Date: Sunday, September 09, 2007
Sheet 31 of 57

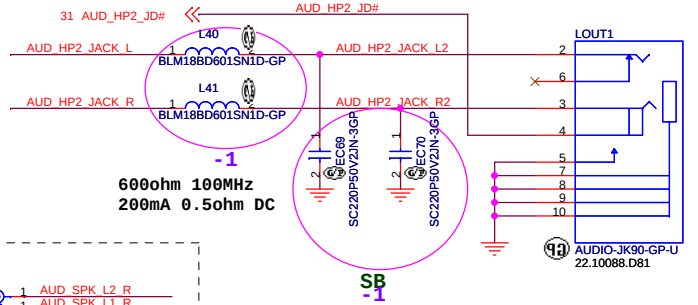
Speaker



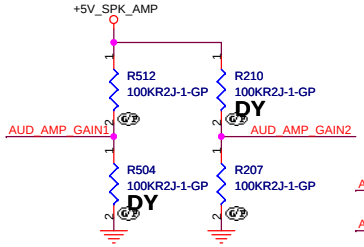
LINE1 OUT



LINE2 OUT

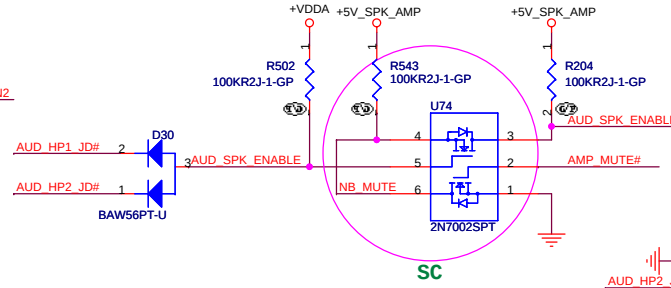


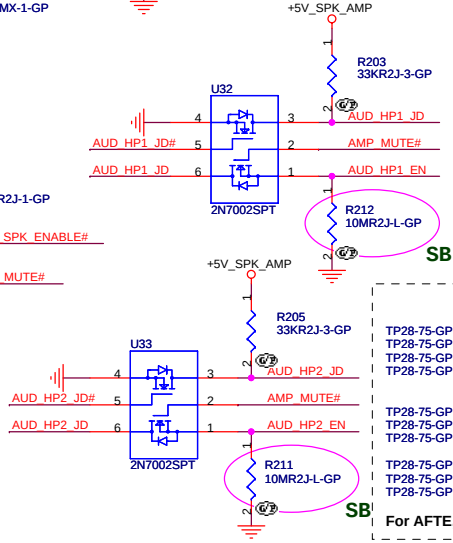
GAIN SETTING

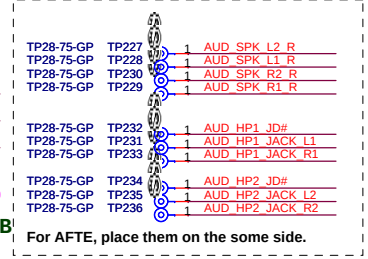


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown







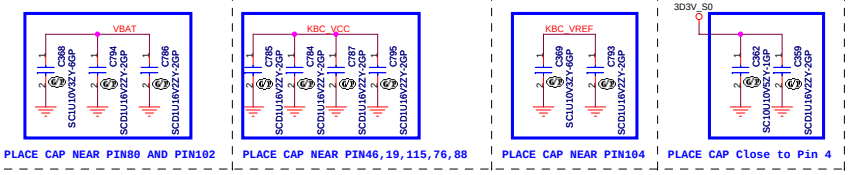
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size: A3 | Document Number: Hawke-Intel | Rev: -1

Date: Sunday, September 09, 2007 | Sheet 32 of 57



WPC8763L STRAP PIN

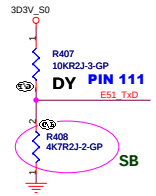
JEN0 (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES		GPIO Port	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

TRIS#(Pin 110) TRI-STATE

Forces the device to float all its output and I/O pins,if an external 10 KΩ pull-down resistor is conected.

BADDR1-0 (PIN 111, 112) I/O Base Address.

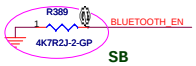
10KΩ external pull-down resistor on BADDR1: Core defined



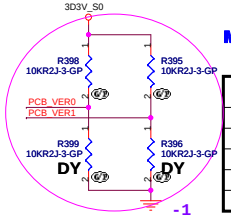
SHBM PIPN83 Shared Host BIOS Memory.

HIGH:NO SHARED(internal resistor)

LOW:SHARED BIOS memory.

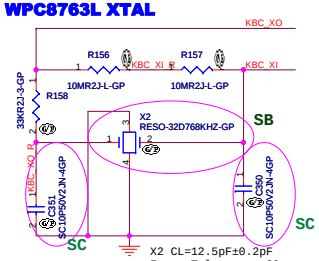


MB VERSION ID

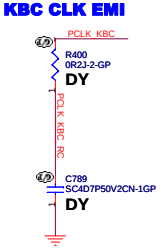


MB VERSION ID	VER0	VER1
SA	0	0
SB	0	1
SC	1	0
-1	1	1

WPC8763L XTAL



KBC CLK EMI



ADIA:to Charger

ACDC_ID:from Adapter Conn

KBC_PWRBTN#:from power button

BAT_IN#:from Battery Conn

DC_BATFULL#:for Battery charge LED 1

CHARGE_LED#:for Battery charge LED 2

WLAN_TEST:for WKS test WLAN LED

AD_OFF:enable AC adapter power source

WLAN/BT_BTN#:from Wlan on/off button

GMCH_BL_ON:Sense The Backlight On/Off Status from VGA Chip

WIRELESS_EN:Disable/Enable Wireless Module

BLUETOOTH_EN:Disable/Enable Bluetooth

USB_PWR_EN#:to on/off USB power switch

AC_IN#:From Charge

<Core Design>

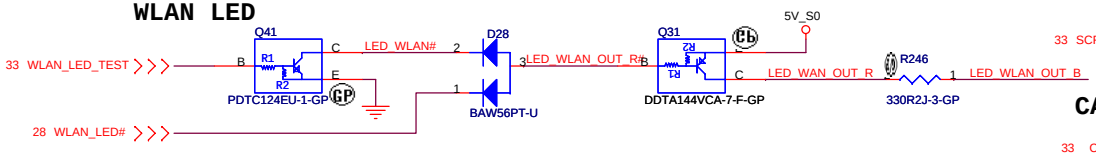
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC_Winbond WPC8763L**

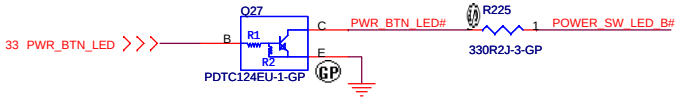
Size	Document Number	Rev
C	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 33 of 57

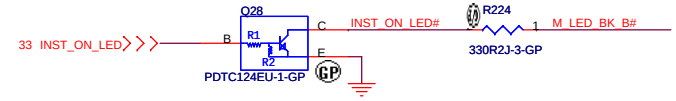
WLAN LED



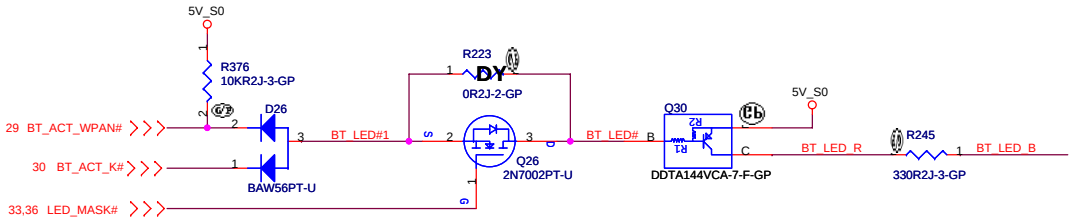
Power Button LED



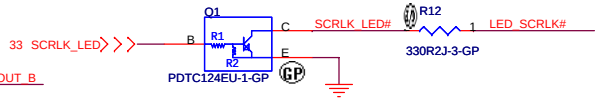
Instant Power Button LED



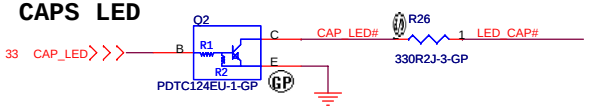
Bluetooth LED



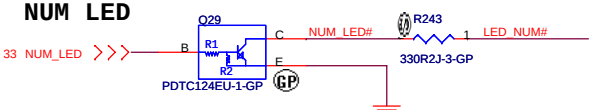
SCRLK LED



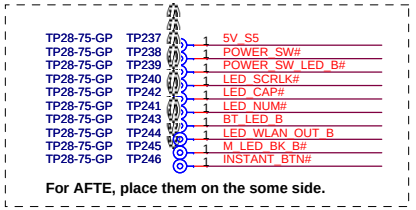
CAPS LED

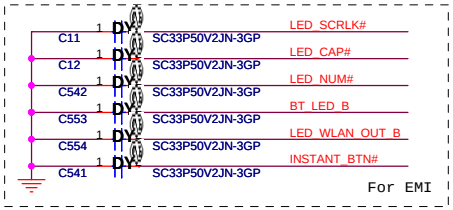


NUM LED

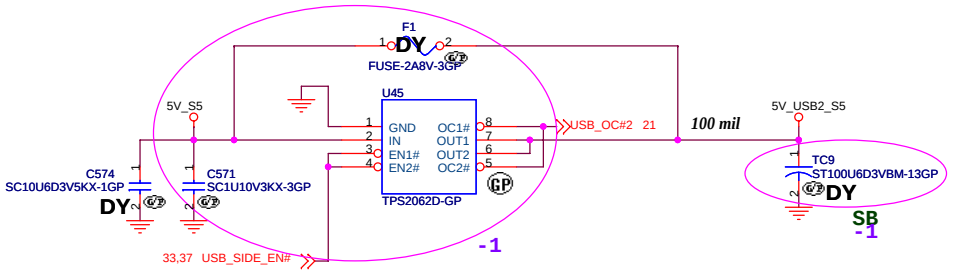


To LED Board

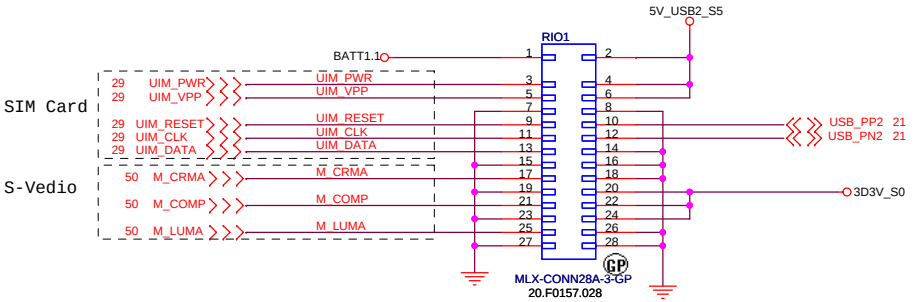


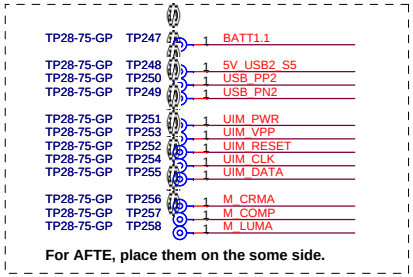


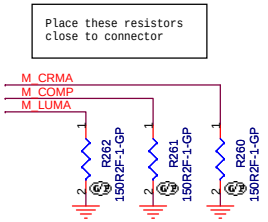
USB POWER



To Right I/O Board







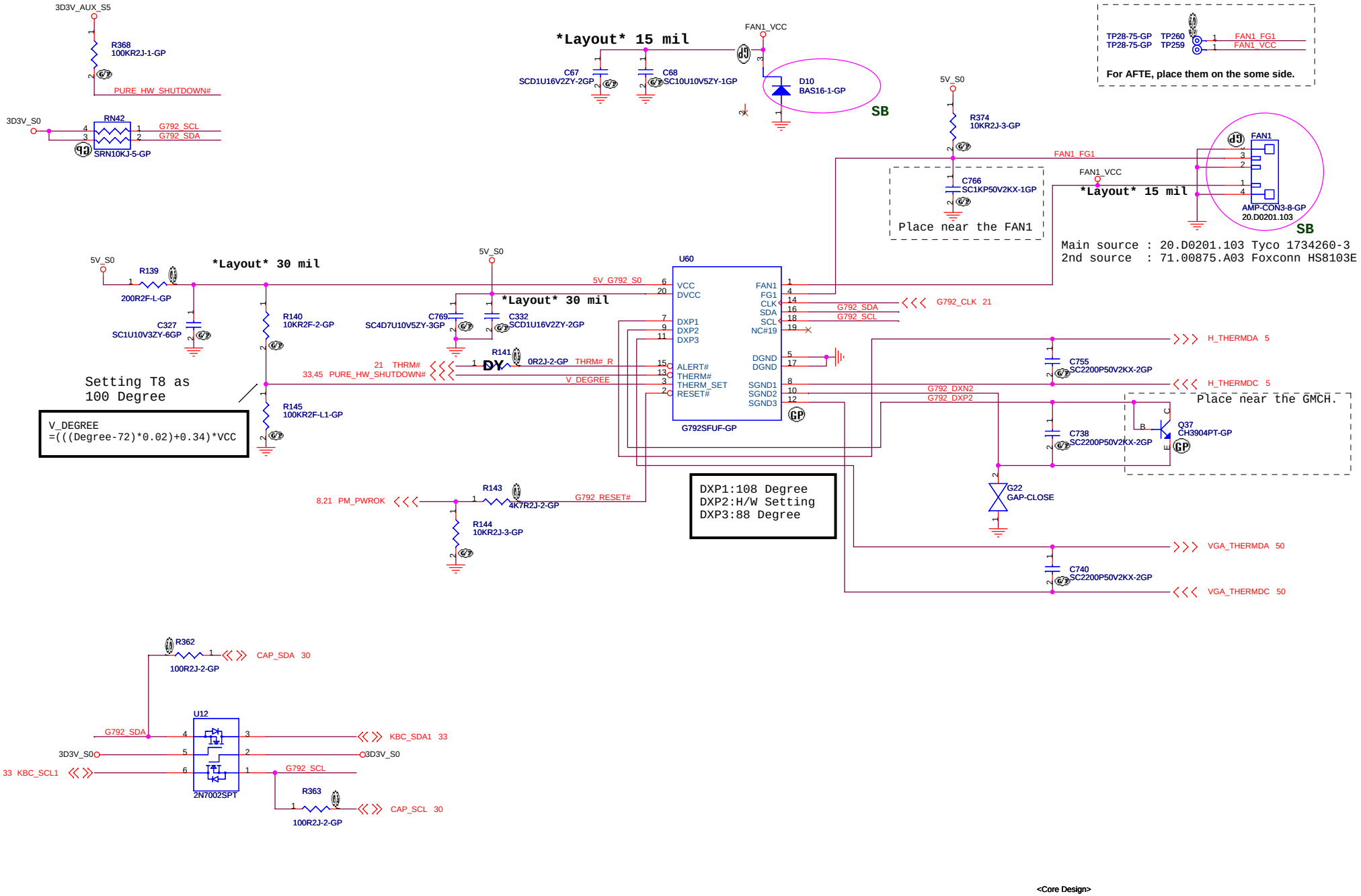
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Right I/O/ Power Dash***

Size	Document Number	Rev
A3	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 34 of 57



<Core Design>

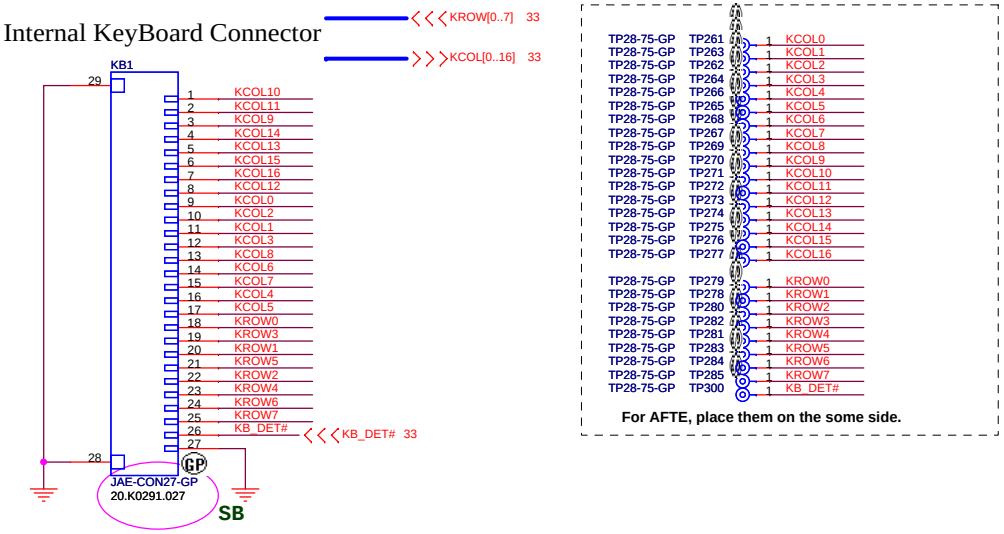
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor G792***

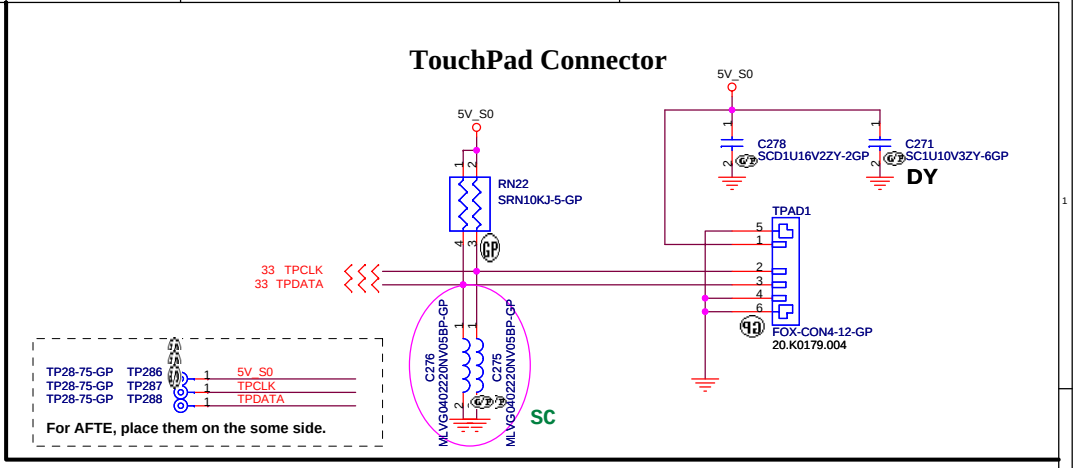
Size	Document Number	Rev
A3	Hawke-Intel	-1

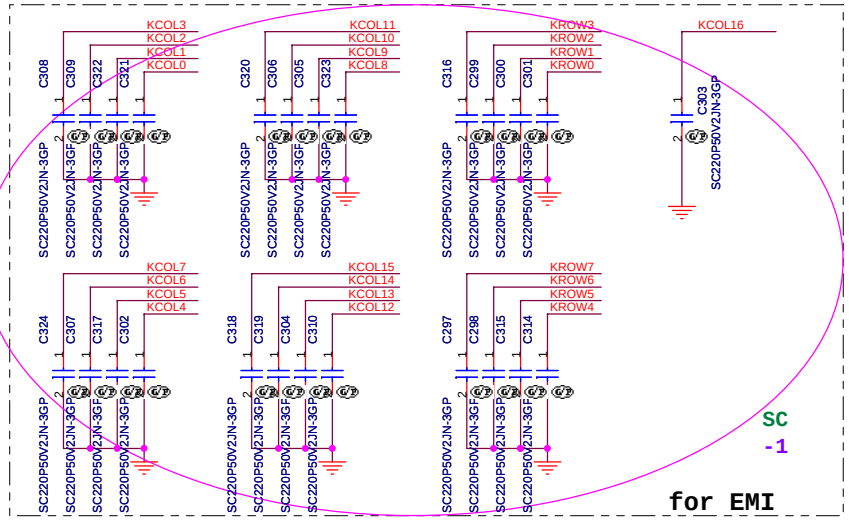
Date: Sunday, September 09, 2007 Sheet 35 of 57

Internal KeyBoard Connector

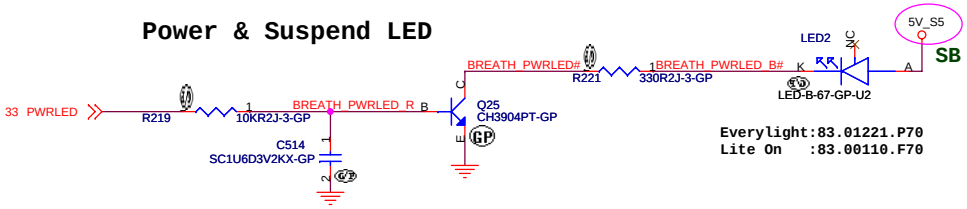


TouchPad Connector

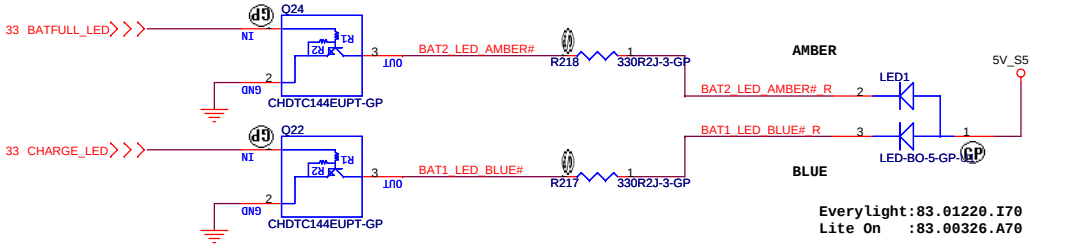




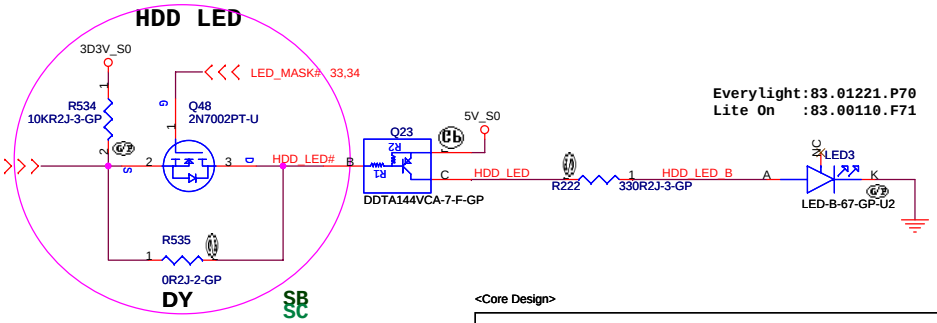
Power & Suspend LED



Battery LED



HDD LED



LED Board

LED NAME	ACTIVE SIGNAL	
Power Button LED	PWR_BTN_LED	*
Instant Power Button LED	INST_ON_LED	*
WLAN LED	WLAN_LED_TEST (from KBC) WLAN_LED# (from Mini)	
Bluetooth LED	BT_ACT_WPAN# (from Mini) BT_ACT_K# (from BT)	
NUM LED	NUM_LED (from KBC)	
SCRLK LED	SCRLK_LED (from KBC)	
CAPS LED	CAP_LED (from KBC)	

Main Board

Power & Suspend LED	PWRLED	(from KBC)
HDD LED	SATA_LED#	(from ICH)
Battery LED	BATFULL_LED CHARGE_LED	(from KBC)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard/Touchpad

Size: A3 | Document Number: Hawke-Intel | Rev: -1

Date: Sunday, September 09, 2007 | Sheet 36 of 57

USB POWER

F3 FUSE-2A8V-3GP DY

U51 TPS2062D-GP (GND, IN, EN1#, EN2#, OC1#, OUT1, OUT2, OC2#)

5V_S5

C603 SC10U6D3V5KX-1GP DY

C585 SC1U10V3KX-3GP

33,34 USB_SIDE_EN#

USB_OC#0 21

USB_OC#1 21

100 mil

-1

5V_USB0_S5

C610 ST100U6D3VBM-13GP

-1

R266 15KR2J-1-GP

Q33 CH3904PT-GP

R264 100KR2J-1-GP

Q32 2N7002PT-U

R265 DY 33R2J-2-GP

R267 33R2J-2-GP

5V_S5

R270 10KR2J-3-GP

D9 BAV99-7-F-GP DY

PSID_DISABLE# 33

5V_S5

D25 BAV99-7-F-GP

3D3V_S5

R268 2K2R2J-2-GP

ACDC_ID 33

Reserved for EMI

AD+ JK

C32 SCD01U25V2KX-3GP

Place near CN5

To Left I/O Board (Adapter In/ USB x 2)

5V_USB0_S5

CN5 MLX-CONN28A-1-GP 20.F1089.028

JACK_PSID_2

21 USB_PP0

21 USB_PN0

21 USB_PP1

21 USB_PN1

AD+_JK

C28 SCD1U25V3KX-GP DY

C578 SCD1U25V3KX-GP DY

For EMI

C569 SCD1U25V3KX-GP DY

This cap should be used only as last resort for EMI suppression.

AD+_JK

C575 SC1U25V5KX-1GP

R263 240KR3-GP

R269 47KR3J-L-GP

Q3 PDTA124EU-1-GP DY

33 AD_OFF

Q4 DDTC124EUA-7F-GP DY

U46 P2003EVG-GP

AD+

C583 SCD01U25V2KX-3GP

Id=17A
Qg=100~150nC
Rdson=5.4~6.5mohm

TP28-75-GP TP289 AD+_JK
TP28-75-GP TP290 JACK_PSID_2
TP28-75-GP TP292 5V_USB0_S5
TP28-75-GP TP291 USB_PP0
TP28-75-GP TP294 USB_PN0
TP28-75-GP TP293 USB_PP1
TP28-75-GP TP295 USB_PN1

For AFTE, place them on the some side.

3D3V_S5

PBAT_SMBCLK1 D2 BAV99-7-F-GP

PBAT_SMBDAT1 D1 BAV99-7-F-GP

BAT_IN# D21 BAV99-7-F-GP

PBAT_ALARM# D22 BAV99-7-F-GP

Batt Connecter

BT+

CN4 SYN-CON9-1-GP-U1 20.80590.009

BATT1+
BATT2+
CLK_SMB
DAT_SMB
BATT_PRS#
SYS_PRES#
BAT_ALERT
GND1
GND2
GND
GND

R2 0R0603-PAD

BATT_SENSE 38

PBAT_SMBCLK1 R6 100R2J-2-GP

PBAT_SMBDAT1 R5 100R2J-2-GP

PBAT_PRES1# R241 100R2J-2-GP

BAT_SCL 18,33,38

BAT_SDA 18,33,38

BAT_IN# 33

R244 100KR2J-1-GP 3D3V_S5

PBAT_ALARM# TP96

C6 SCD1U25V3KX-GP

C3 SC2200P50V2KX-2GP

Main source : 20.80590.009 Suyin 200275MR009G548ZL
2nd source : 20.80626.009 Foxconn BP02093-P5351-7F

TP28-75-GP TP296 BT+
TP28-75-GP TP297 PBAT_SMBCLK1
TP28-75-GP TP298 PBAT_SMBDAT1
TP28-75-GP TP299 PBAT_PRES1#

For AFTE, place them on the some side.

PBAT_SMBCLK1 C5 SC33P50V2JN-3GP DY

PBAT_SMBDAT1 C4 SC33P50V2JN-3GP DY

PBAT_PRES1# C526 SC33P50V2JN-3GP DY

For EMI

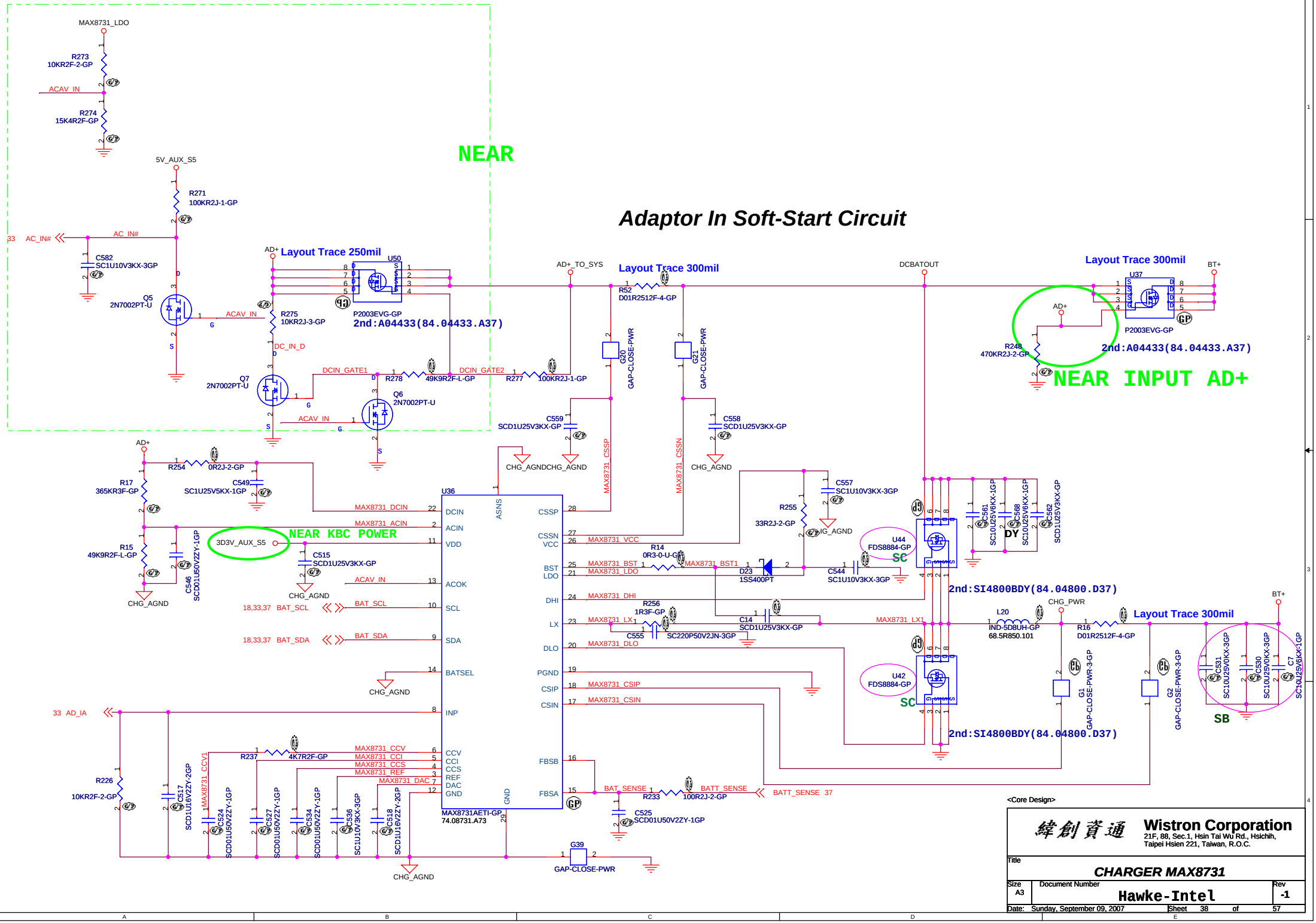
<Core Design>

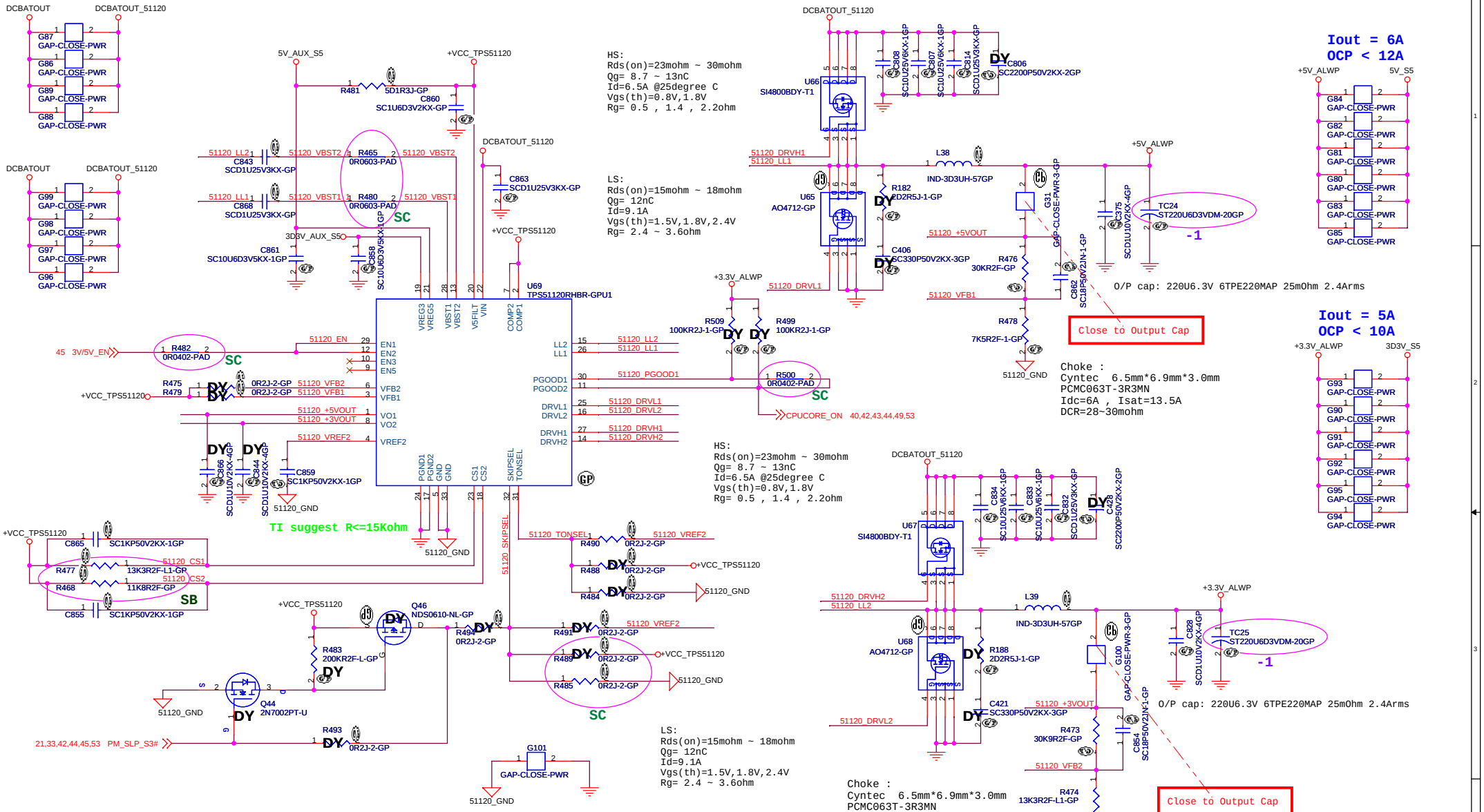
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

Size: A3 | Document Number: Hawke-Intel | Rev: -1

Date: Sunday, September 09, 2007 | Sheet 37 of 57


NEAR
Adaptor In Soft-Start Circuit
MAX8731_LDO
R273
10KR2F-2-GP
ACAV_IN
R274
15K4R2F-GP
5V_AUX_S5
R271
100KR2J-1-GP
33 AC_IN#
AC_IN#
C582
SC1U10V3KX-3GP
Q5
2N7002PT-U
ACAV_IN
AD+
Layout Trace 250mil
U50
P2003EVG-GP
R275
10KR2J-3-GP
2nd:A04433(84.04433.A37)
DC_IN_D
Q7
2N7002PT-U
DCIN_GATE1
R278
49K9R2F-L-GP
DCIN_GATE2
R277
100KR2J-1-GP
Q6
2N7002PT-U
ACAV_IN
AD+_TO_SYS
Layout Trace 300mil
R52
D01R2512F-4-GP
G20
GAP-CLOSE-PWR
G21
GAP-CLOSE-PWR
C559
SCD1U25V3KX-GP
C558
SCD1U25V3KX-GP
CHG_AGNDCHG_AGND
CHG_AGND
MAX8731_CSSP
MAX8731_CSSN
DCBATOUT
Layout Trace 300mil
BT+
U37
P2003EVG-GP
AD+
R248
470KR2J-2-GP
2nd:A04433(84.04433.A37)
NEAR INPUT AD+
AD+
R254
0R2J-2-GP
C549
SC1U25V5KX-1GP
R17
365KR3F-GP
R15
49K9R2F-L-GP
C546
SCD01U50V2ZY-1GP
CHG_AGND
NEAR KBC POWER
3D3V_AUX_S5
C515
SCD1U25V3KX-GP
CHG_AGND
U36
MAX8731_DCIN
MAX8731_ACIN
ACAV_IN
BAT_SCL
BAT_SDA
18,33,37 BAT_SCL
18,33,37 BAT_SDA
DCIN
ACIN
VDD
ACOK
SCL
SDA
BATSEL
INP
CCV
CCI
CCS
REF
DAC
GND
ASNS
CSSP
CSSN
VCC
BST
LDO
DHI
LX
DLO
PGND
CSIP
CSIN
FBSB
FBSA
MAX8731_VCC
MAX8731_BST
MAX8731_LDO
MAX8731_DHI
MAX8731_LX
MAX8731_DLO
MAX8731_CSIP
MAX8731_CSIN
MAX8731AETI-GP
74.08731.A73
R255
33R2J-2-GP
C557
SC1U10V3KX-3GP
IG_AGND
R14
0R3-0-U-GP
MAX8731_BST1
D23
1SS400PT
C544
SC1U10V3KX-3GP
U44
FDS8884-GP
SC
U42
FDS8884-GP
SC
C561
SC10U25V6KX-1GP
C568
SC10U25V6KX-1GP
DY
C562
SC1U25V3KX-GP
2nd:SI4800BDY(84.04800.D37)
2nd:SI4800BDY(84.04800.D37)
R256
1R3F-GP
C555
SC220P50V2JN-3GP
C14
SCD1U25V3KX-GP
L20
IND-5D8UH-GP
68.5R850.101
CHG_PWR
R16
D01R2512F-4-GP
Layout Trace 300mil
BT+
G1
GAP-CLOSE-PWR-3-GP
G2
GAP-CLOSE-PWR-3-GP
C531
SC10U25V6KX-3GP
C530
SC10U25V6KX-3GP
C7
SC10U25V6KX-1GP
SB
33 AD_IA
R226
10KR2F-2-GP
C517
SCD1U16V2ZY-2GP
MAX8731_CCV1
C524
SCD01U50V2ZY-1GP
R237
4K7R2F-GP
MAX8731_CCV
MAX8731_CCI
MAX8731_CCS
MAX8731_REF
MAX8731_DAC
C527
SCD01U50V2ZY-1GP
C534
SCD01U50V2ZY-1GP
C536
SC1U10V3KX-3GP
C518
SCD1U16V2ZY-2GP
CHG_AGND
BAT_SENSE
R233
100R2J-2-GP
BATT_SENSE
BATT_SENSE 37
C525
SCD01U50V2ZY-1GP
G39
GAP-CLOSE-PWR
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER MAX8731
Size
A3
Document Number
Hawke-Intel
Rev
-1
Date: Sunday, September 09, 2007
Sheet 38 of 57



Vout=1V*(R1+R2)/R2

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

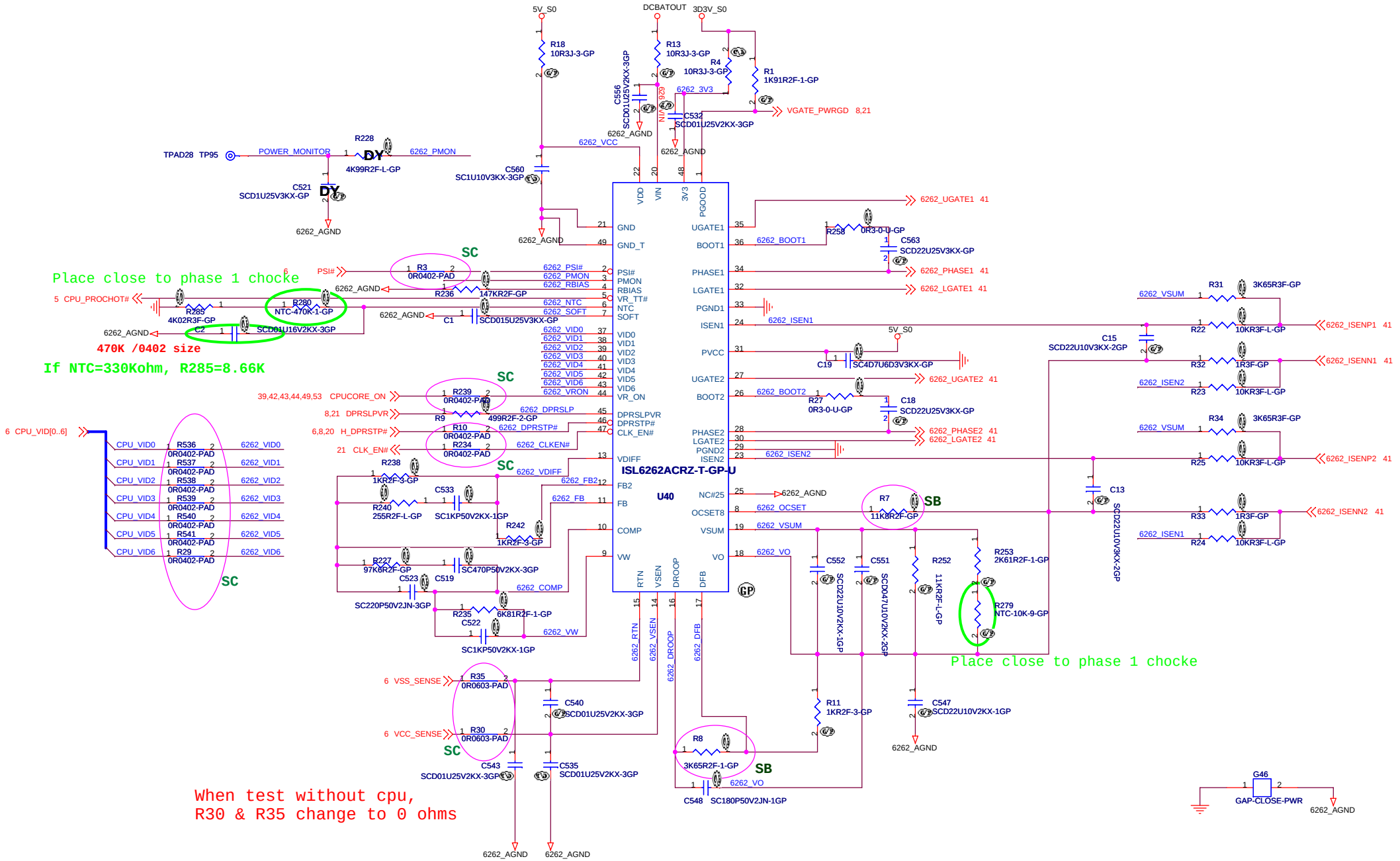
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 3.3V & 5V

Size: Custom | Document Number: Hawke-Intel | Rev: -1

Date: Sunday, September 09, 2007 | Sheet 39 of 57



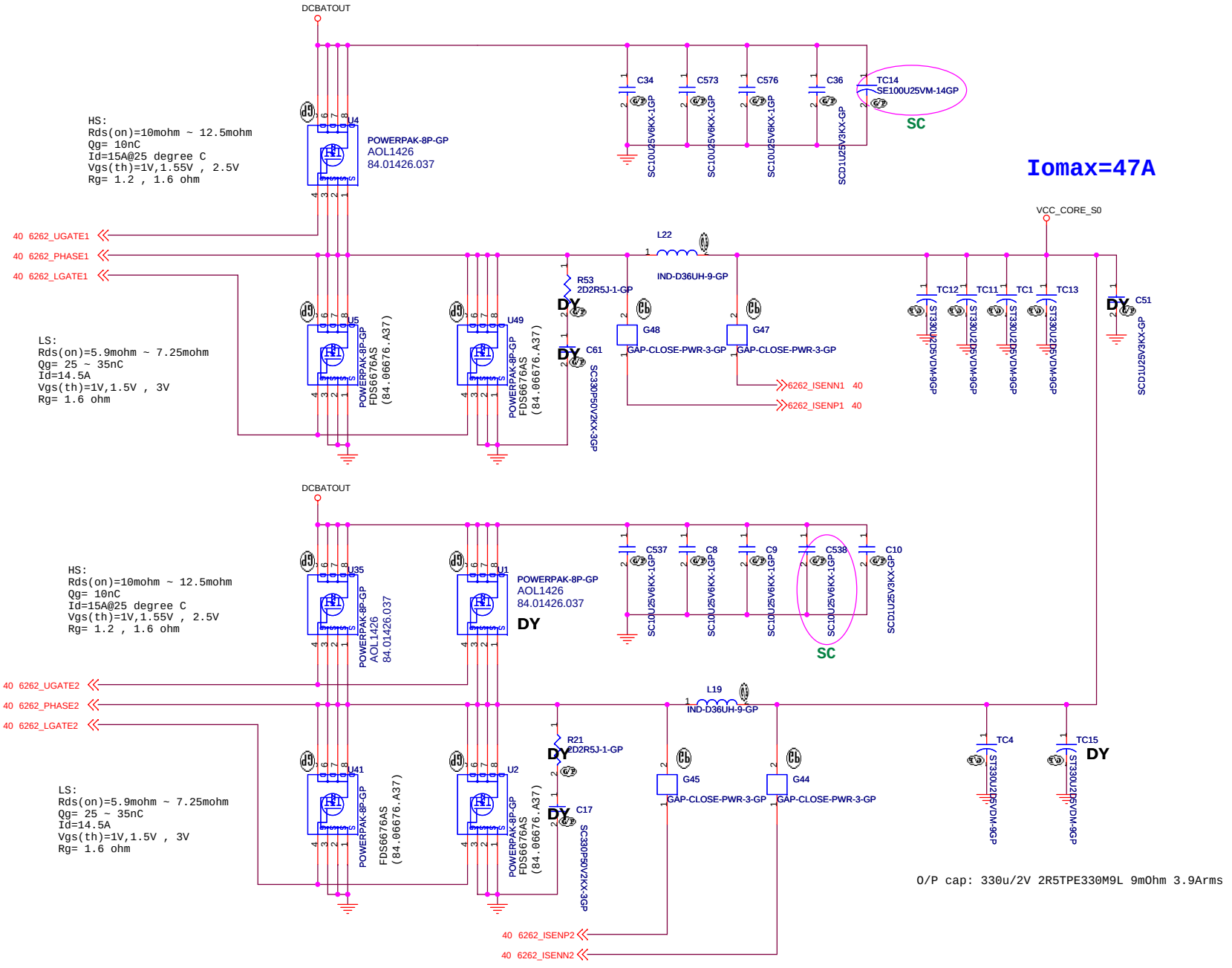
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC-DC VCCCPUCORE 1/2

Size	Document Number	Rev
A3	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 40 of 57



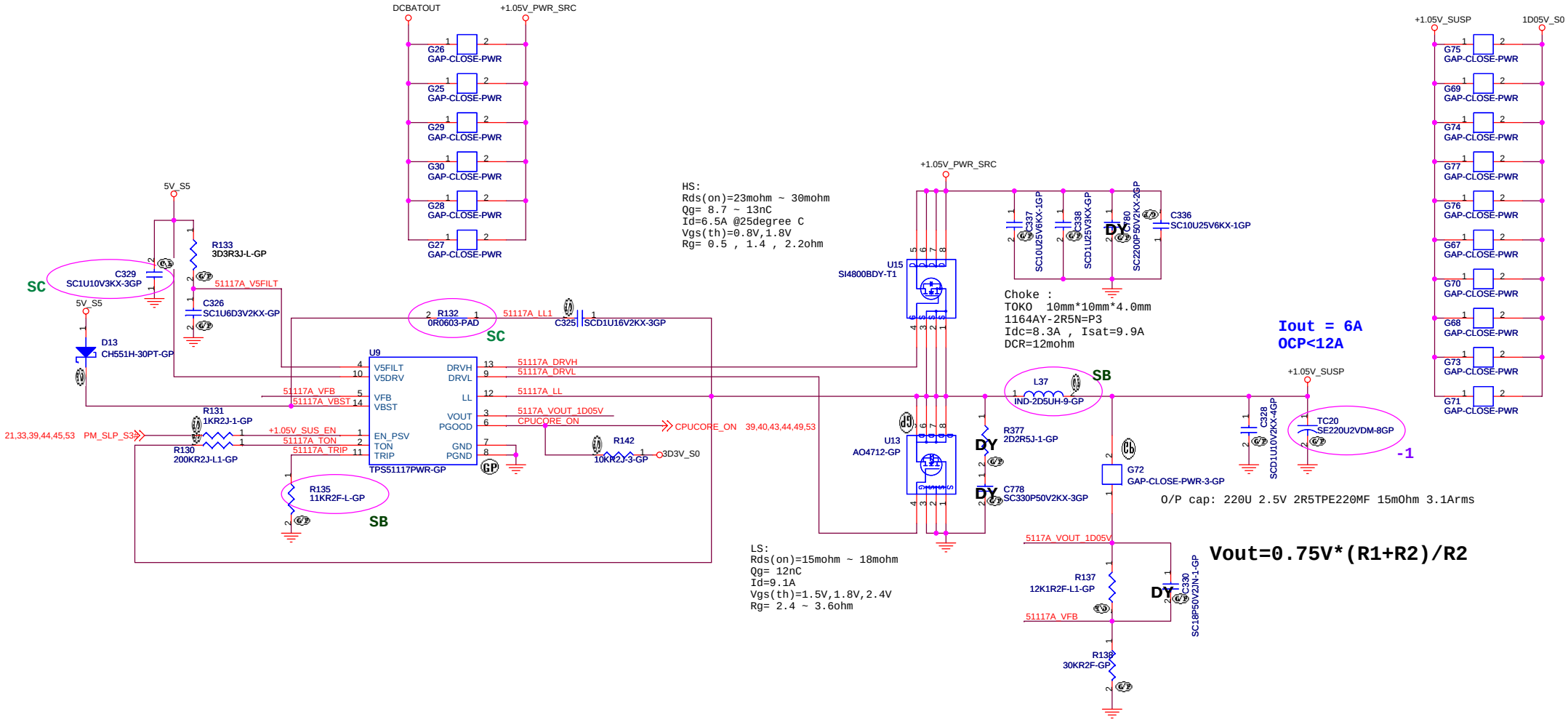
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC-DC VCCCPUCORE 2/2

Size	Document Number	Rev
A3	Hawke-Intel	-1

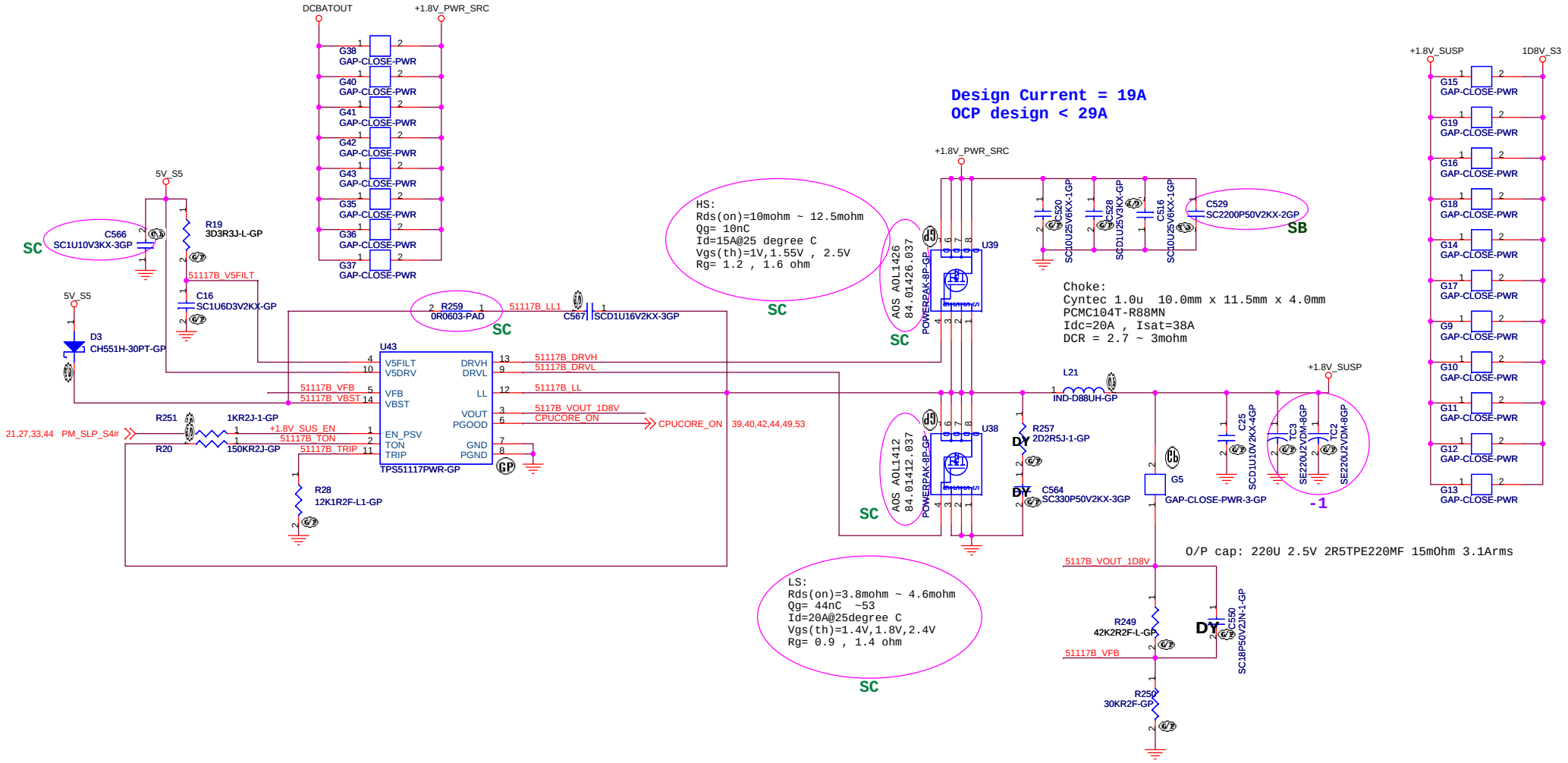
Date: Thursday, September 20, 2007 Sheet 41 of 57



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***DCDC 1.05V***	
Size A3	Document Number **Hawke-Intel**	Rev **-1**
Date: Sunday, September 09, 2007	Sheet 42 of 57	



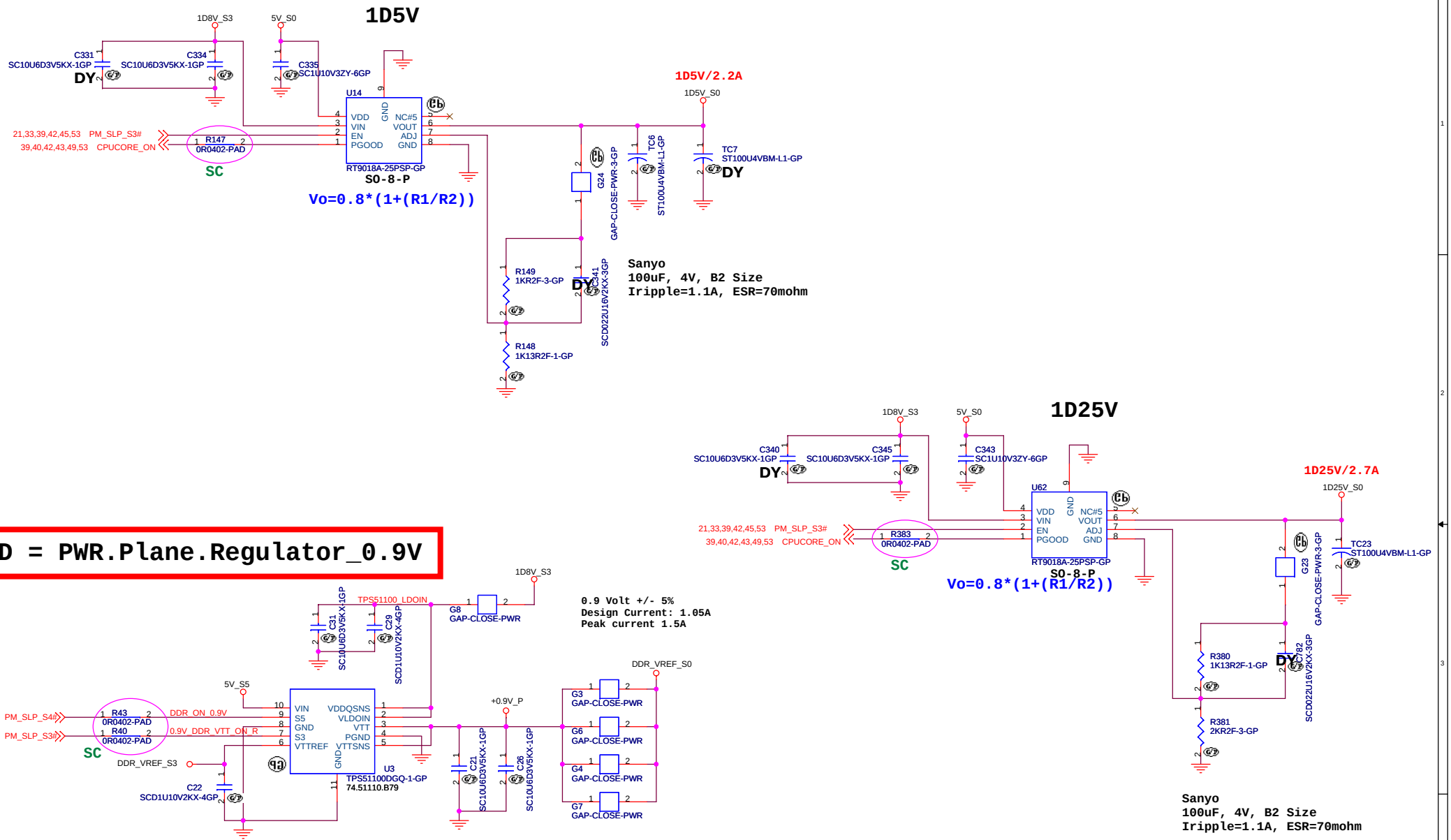
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC 1D8V(ISL6268)

Size	Document Number	Rev
A3	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 43 of 57



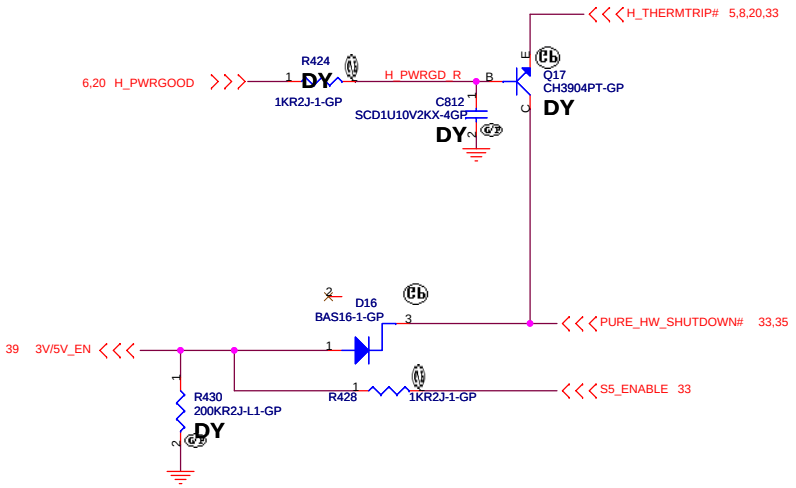
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

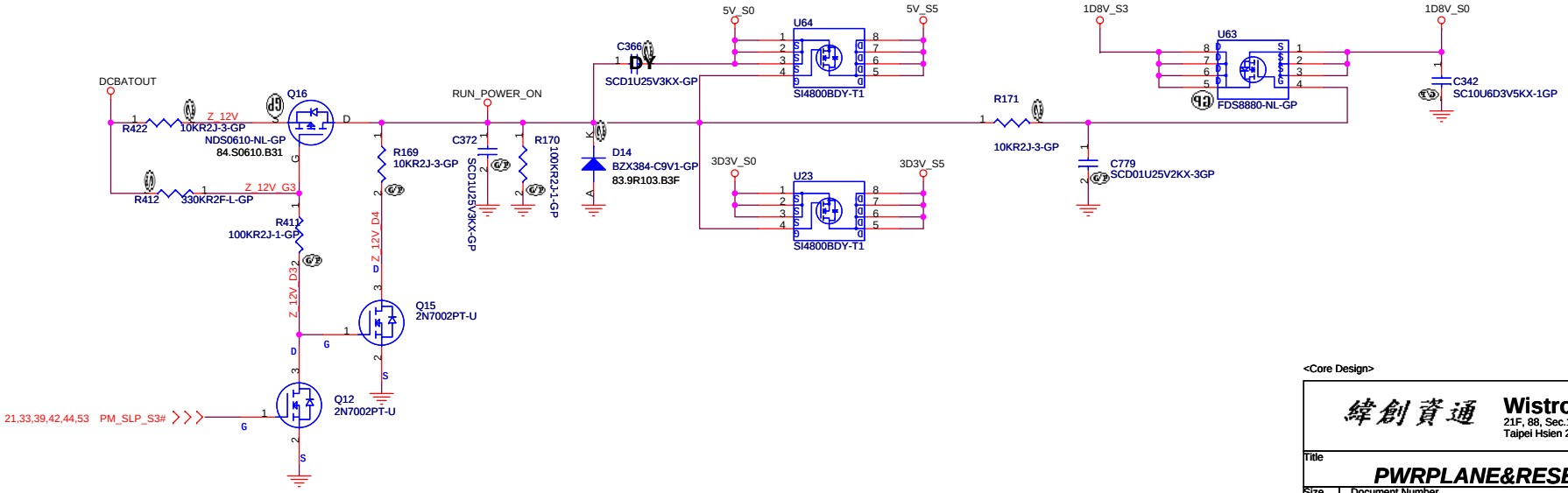
Title: DC to DC 1D5V / 0D9V / 1D25V

Size	Document Number	Rev
A3	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 44 of 57



Run Power



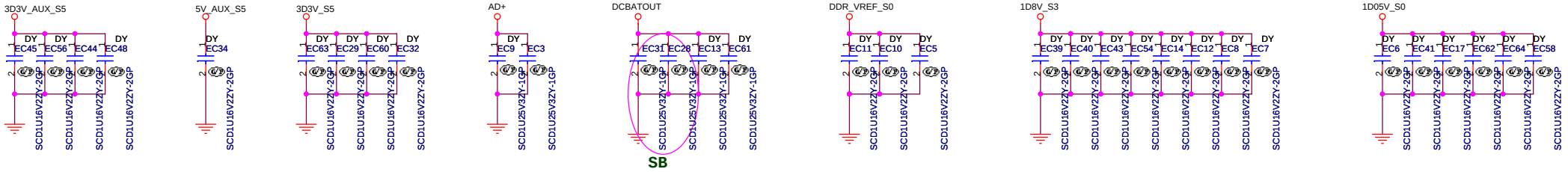
<Core Design>

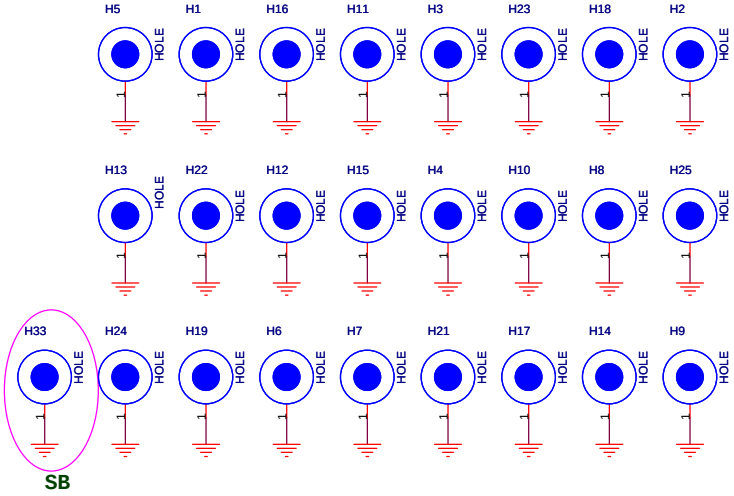
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

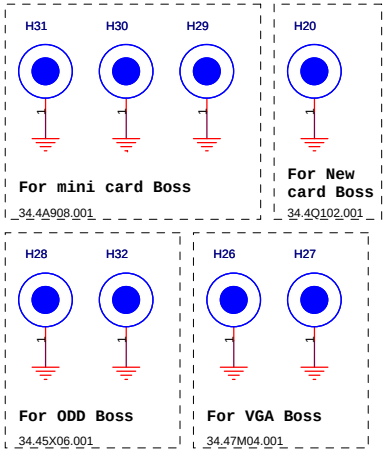
Title: ***PWRPLANE&RESETLOGIC***

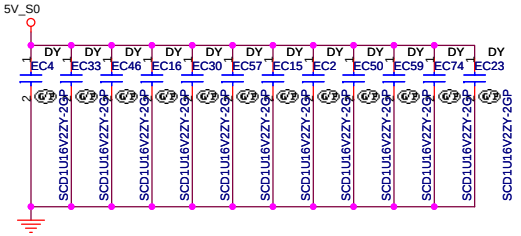
Size	Document Number	Rev
A3	Hawke-Intel	-1

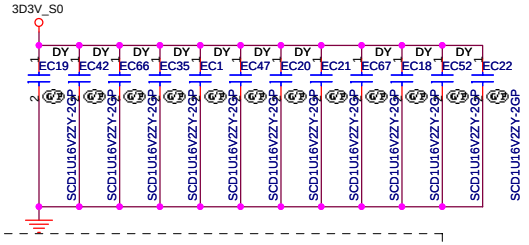
Date: Sunday, September 09, 2007 Sheet 45 of 57

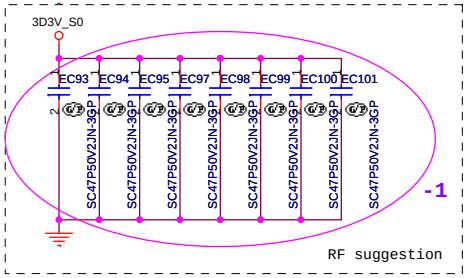


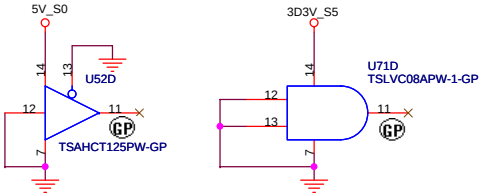


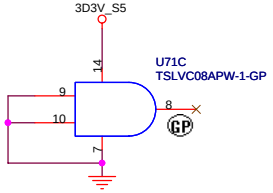


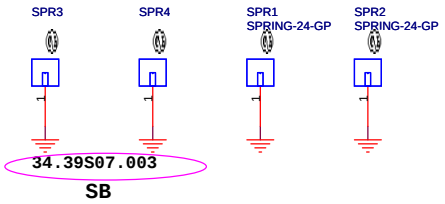












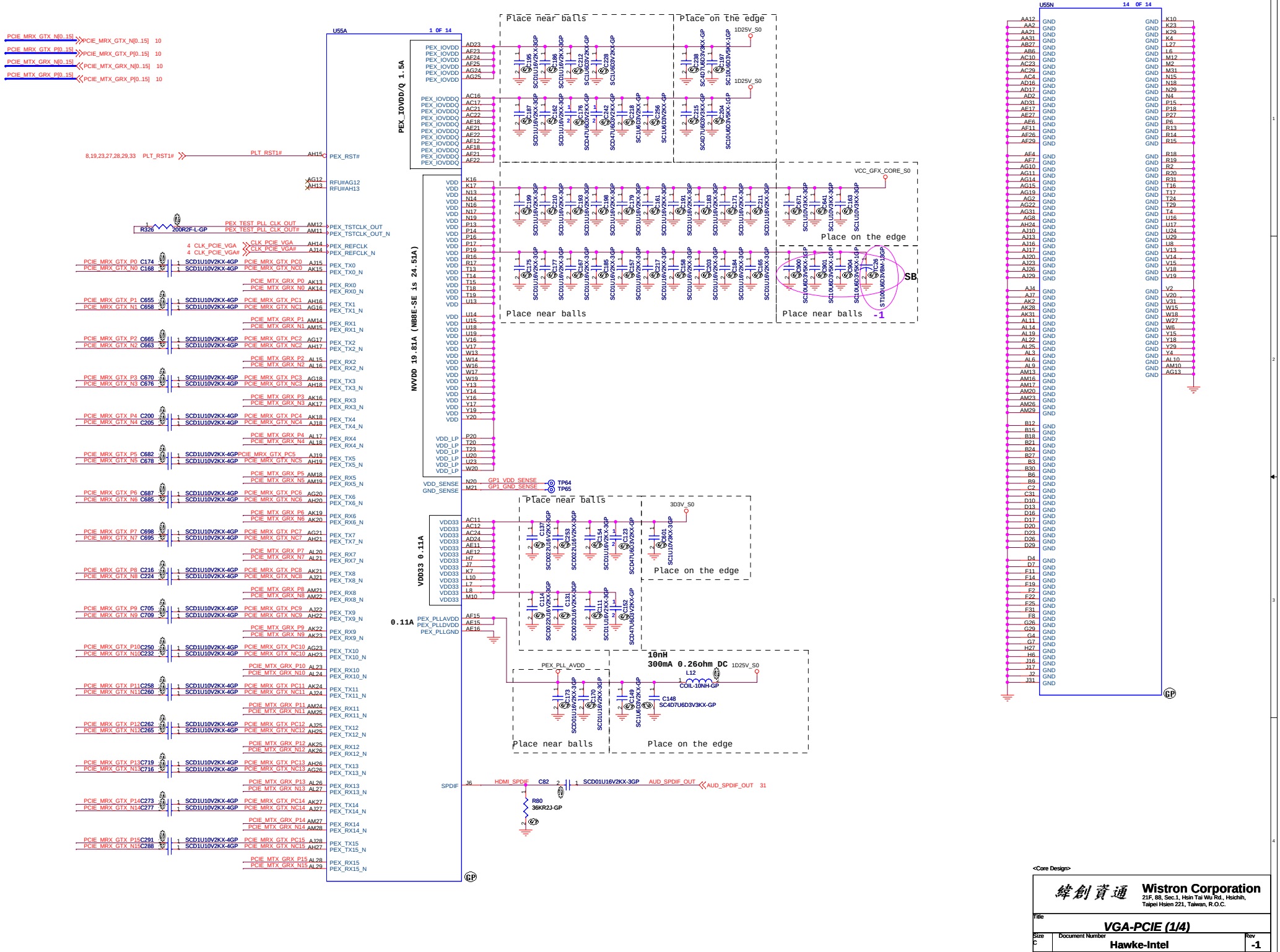
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MISC**

Size	Document Number	Rev
A3	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 46 of 57



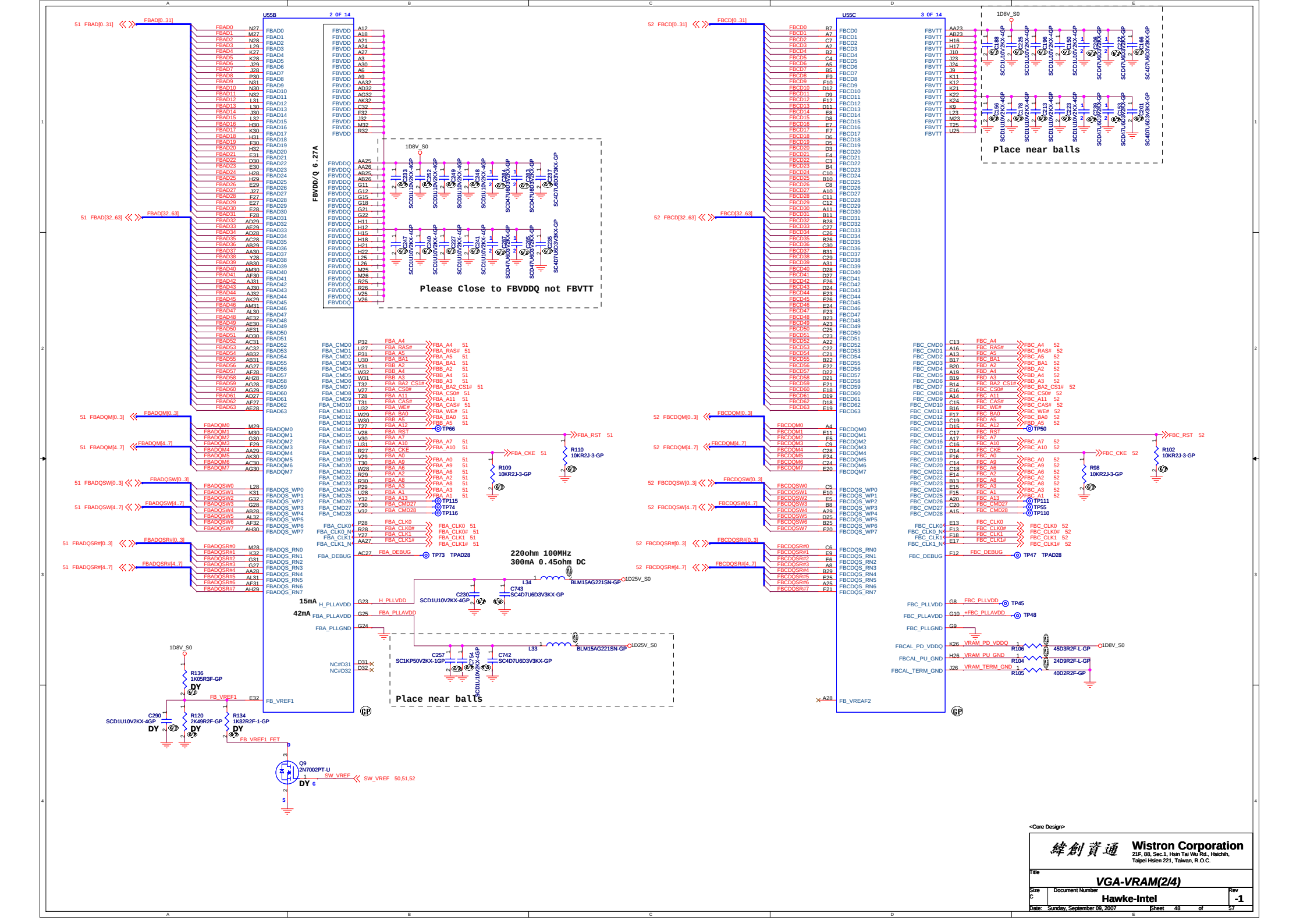
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

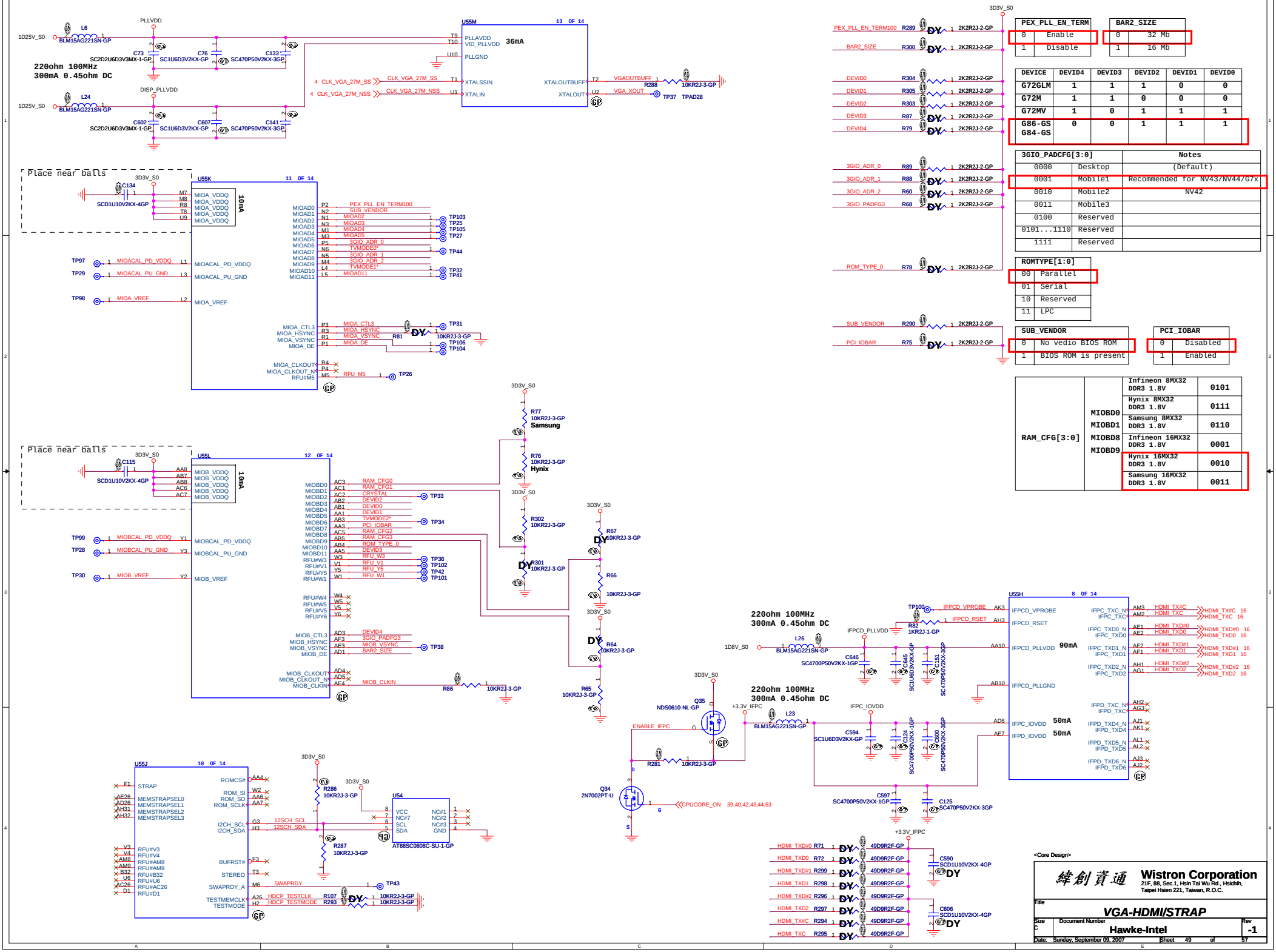
<Core Design>

Title: VGA-PCIE (1/4)

Size	Document Number	Rev
C	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 47 of 57


U55B
2 OF 14
FBVDD/Q 6.27A
Please Close to FBVDDQ not FBVTT
1D8V_S0
220ohm 100MHz
300mA 0.45ohm DC
15mA
42mA
Place near balls
U55C
3 OF 14
Place near balls
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA-VRAM(2/4)
Size C
Document Number
Hawke-Intel
Rev -1
Date: Sunday, September 09, 2007
Sheet 48 of 57


PLLVDD
1D25V_S0
L6
BLM15AG221SN-GP
220ohm 100MHz
300mA 0.45ohm DC
C73
SC2D2U6D3V3MX-1-GP
C76
SC1U6D3V2KX-GP
C133
SC470P50V2KX-3GP
DISP_PLLVDD
L24
C602
C607
C141
U55M
13 OF 14
PLLAVDD
VID_PLLVDD
36mA
PLLGND
CLK_VGA_27M_SS
CLK_VGA_27M_NSS
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
VGAOUTBUFF
VGA_XOUT
R288
10KR2J-3-GP
TP37
TPAD28
Place near balls
3D3V_S0
C134
SCD1U10V2KX-4GP
U55K
11 OF 14
10mA
MIOA_VDDQ
MIOACAL_PD_VDDQ
MIOACAL_PU_GND
MIOA_VREF
MIOAD0
MIOAD1
MIOAD2
MIOAD3
MIOAD4
MIOAD5
MIOAD6
MIOAD7
MIOAD8
MIOAD9
MIOAD10
MIOAD11
PEX_PLL_EN_TERM100
SUB_VENDOR
3GIO_ADR_0
3GIO_ADR_1
3GIO_ADR_2
TVMODE0*
TVMODE1*
TP97
TP29
TP98
TP103
TP25
TP105
TP27
TP44
TP32
TP41
MIOA_CTL3
MIOA_HSYNC
MIOA_VSYNC
MIOA_DE
R81
10KR2J-3-GP
TP31
TP106
TP104
MIOA_CLKOUT
MIOA_CLKOUT_N
RFU#M5
TP26
Place near balls
C115
SCD1U10V2KX-4GP
U55L
12 OF 14
10mA
MIOB_VDDQ
MIOBCAL_PD_VDDQ
MIOBCAL_PU_GND
MIOB_VREF
MIOBD0
MIOBD1
MIOBD2
MIOBD3
MIOBD4
MIOBD5
MIOBD6
MIOBD7
MIOBD8
MIOBD9
MIOBD10
MIOBD11
RAM_CFG0
RAM_CFG1
CRYSTAL
DEVID2
DEVID0
DEVID1
TVMODE2*
PCI_IOBAR
RAM_CFG2
RAM_CFG3
ROM_TYPE_0
DEVID3
RFU_W3
RFU_V1
RFU_Y5
RFU_W1
TP99
TP28
TP30
TP33
TP34
TP36
TP102
TP42
TP101
MIOB_CTL3
MIOB_HSYNC
MIOB_VSYNC
MIOB_DE
MIOB_CLKOUT
MIOB_CLKOUT_N
MIOB_CLKIN
DEVID4
3GIO_PADFG3
BAR2_SIZE
TP38
R86
10KR2J-3-GP
R77
10KR2J-3-GP
Samsung
R76
10KR2J-3-GP
Hynix
R302
10KR2J-3-GP
R301
10KR2J-3-GP
R67
10KR2J-3-GP
R66
10KR2J-3-GP
R64
10KR2J-3-GP
R65
10KR2J-3-GP
U55J
10 OF 14
STRAP
MEMSTRAPSEL0
MEMSTRAPSEL1
MEMSTRAPSEL2
MEMSTRAPSEL3
RFU#V3
RFU#V4
RFU#AM8
RFU#AM9
RFU#B32
RFU#U6
RFU#AC26
RFU#D1
ROMCS#
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST#
STEREO
SWAPRDY_A
TESTMEMCLK
TESTMODE
12SCH_SCL
12SCH_SDA
HDCP_TESTCLK
HDCP_TESTMODE
R286
10KR2J-3-GP
R287
10KR2J-3-GP
R107
10KR2J-3-GP
R293
10KR2J-3-GP
TP43
U54
VCC
NC#7
SCL
SDA
NC#1
NC#2
NC#3
GND
AT88SC0808C-SU-1-GP
3D3V_S0
Q35
NDS0610-NL-GP
ENABLE_IFPC
R281
10KR2J-3-GP
Q34
2N7002PT-U
CPUCORE_ON
39,40,42,43,44,53
220ohm 100MHz
300mA 0.45ohm DC
L26
BLM15AG221SN-GP
C646
SC4700P50V2KX-1GP
C645
SCU1U6D3V2KX-4GP
C151
SC470P50V2KX-3GP
L23
BLM15AG221SN-GP
C594
SC1U6D3V2KX-GP
C124
SC470P50V2KX-1GP
C300
SC470P50V2KX-3GP
C597
SC4700P50V2KX-1GP
C125
SC470P50V2KX-3GP
U55H
8 OF 14
IFPCD_VPROBE
IFPCD_RSET
IFPCD_PLLVDD
IFPCD_PLLGND
IFPC_IOVDD
IFPD_IOVDD
90mA
50mA
50mA
IFPC_TXC_N
IFPC_TXC
IFPC_TXD0_N
IFPC_TXD0
IFPC_TXD1_N
IFPC_TXD1
IFPC_TXD2_N
IFPC_TXD2
IFPD_TXC_N
IFPD_TXC
IFPD_TXD4_N
IFPD_TXD4
IFPD_TXD5_N
IFPD_TXD5
IFPD_TXD6_N
IFPD_TXD6
HDMI_TX#C
HDMI_TXC
HDMI_TX#0
HDMI_TXD0
HDMI_TX#1
HDMI_TXD1
HDMI_TX#2
HDMI_TXD2
16
TP100
R82
1KR2J-1-GP
HDMI_TXD#0
HDMI_TXD0
HDMI_TXD#1
HDMI_TXD1
HDMI_TXD#2
HDMI_TXD2
HDMI_TX#C
HDMI_TXC
HDMI_TXD#0 R71
HDMI_TXD0 R72
HDMI_TXD#1 R299
HDMI_TXD1 R298
HDMI_TXD#2 R296
HDMI_TXD2 R297
HDMI_TX#C R294
HDMI_TXC R295
49D9R2F-GP
C590
SCD1U10V2KX-4GP
C606
SCD1U10V2KX-4GP
+3.3V_IFPC
PEX_PLL_EN_TERM100 R289
BAR2_SIZE R300
DEVID0 R304
DEVID1 R305
DEVID2 R303
DEVID3 R87
DEVID4 R79
3GIO_ADR_0 R89
3GIO_ADR_1 R88
3GIO_ADR_2 R60
3GIO_PADFG3 R68
ROM_TYPE_0 R78
SUB_VENDOR R290
PCI_IOBAR R75
2K2R2J-2-GP
DY
PEX_PLL_EN_TERM
0 Enable
1 Disable
BAR2_SIZE
0 32 Mb
1 16 Mb
DEVICE | DEVID4 | DEVID3 | DEVID2 | DEVID1 | DEVID0
G72GLM | 1 | 1 | 1 | 0 | 0
G72M | 1 | 1 | 0 | 0 | 0
G72MV | 1 | 0 | 1 | 1 | 1
G86-GS G84-GS | 0 | 0 | 1 | 1 | 1
3GIO_PADCFG[3:0] | Notes
0000 Desktop (Default)
0001 Mobile1 Recommended for NV43/NV44/G7x
0010 Mobile2 NV42
0011 Mobile3
0100 Reserved
0101...1110 Reserved
1111 Reserved
ROMTYPE[1:0]
00 Parallel
01 Serial
10 Reserved
11 LPC
SUB_VENDOR
0 No vedio BIOS ROM
1 BIOS ROM is present
PCI_IOBAR
0 Disabled
1 Enabled
RAM_CFG[3:0]
MIOBD0
MIOBD1
MIOBD8
MIOBD9
Infineon 8MX32 DDR3 1.8V 0101
Hynix 8MX32 DDR3 1.8V 0111
Samsung 8MX32 DDR3 1.8V 0110
Infineon 16MX32 DDR3 1.8V 0001
Hynix 16MX32 DDR3 1.8V 0010
Samsung 16MX32 DDR3 1.8V 0011
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA-HDMI/STRAP
Size C
Document Number
Hawke-Intel
Rev -1
Date: Sunday, September 09, 2007
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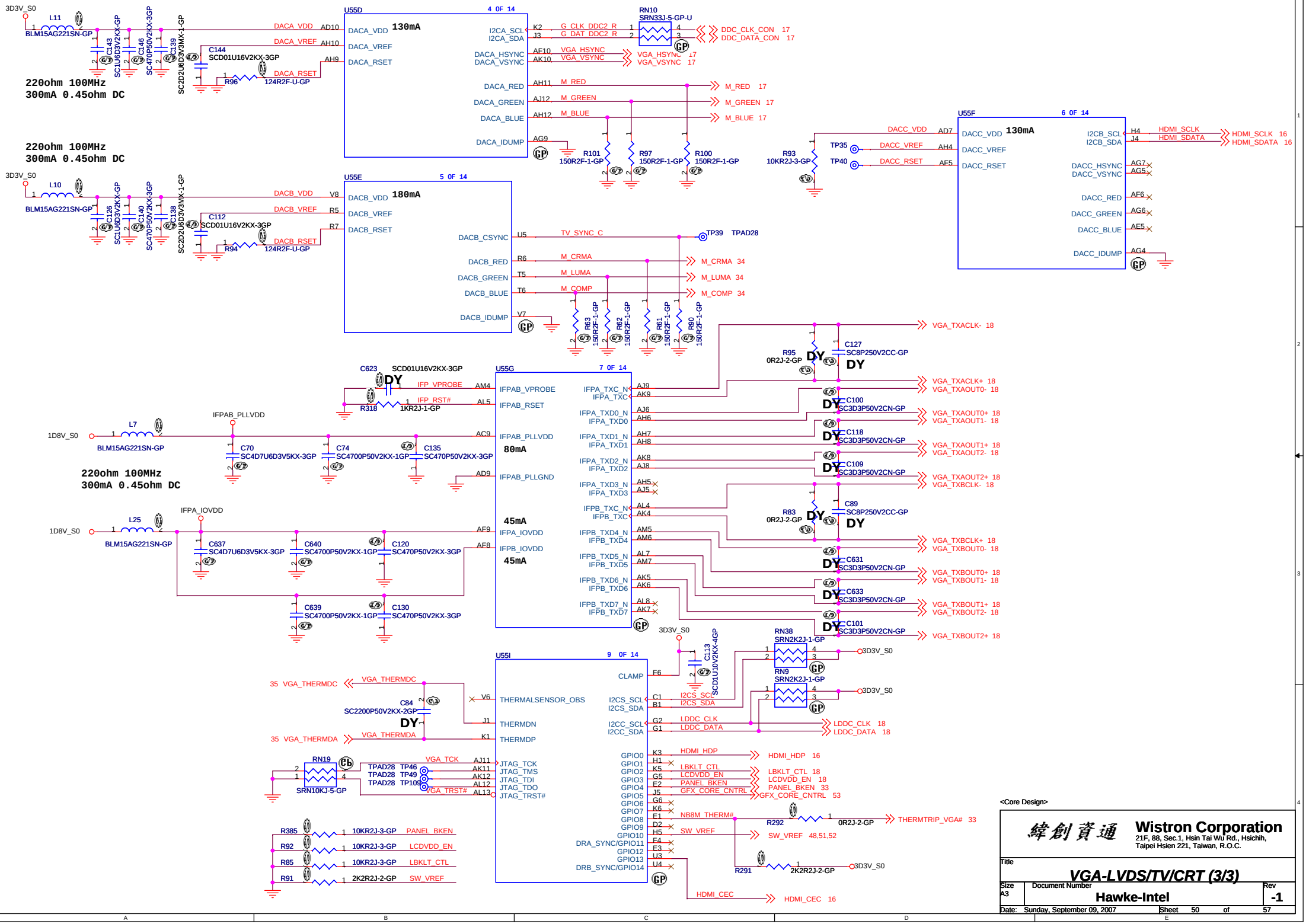
3D3V_S0
L11
BLM15AG221SN-GP
C143 SC1U6D3V2KX-GP
C146 SC470P50V2KX-3GP
C139 SC2D2U6D3V3MX-1-GP
220ohm 100MHz
300mA 0.45ohm DC
DACA_VDD AD10
DACA_VREF AH10
C144 SCD01U16V2KX-3GP
R96 124R2F-U-GP
DACA_RSET AH9
U55D
4 OF 14
DACA_VDD 130mA
DACA_VREF
DACA_RSET
I2CA_SCL K2 G_CLK_DDC2_R
I2CA_SDA J3 G_DAT_DDC2_R
RN10 SRN33J-5-GP-U
DDC_CLK_CON 17
DDC_DATA_CON 17
DACA_HSYNC AF10 VGA_HSYNC
DACA_VSYNC AK10 VGA_VSYNC
VGA_HSYNC 17
VGA_VSYNC 17
DACA_RED AH11 M_RED
DACA_GREEN AJ12 M_GREEN
DACA_BLUE AH12 M_BLUE
M_RED 17
M_GREEN 17
M_BLUE 17
DACA_IDUMP AG9
R101 150R2F-1-GP
R97 150R2F-1-GP
R100 150R2F-1-GP
R93 10KR2J-3-GP
TP35
TP40
DACC_VDD AD7
DACC_VREF AH4
DACC_RSET AF5
U55F
6 OF 14
DACC_VDD 130mA
DACC_VREF
DACC_RSET
I2CB_SCL H4 HDMI_SCLK
I2CB_SDA J4 HDMI_SDATA
HDMI_SCLK 16
HDMI_SDATA 16
DACC_HSYNC AG7
DACC_VSYNC AG5
DACC_RED AF6
DACC_GREEN AG6
DACC_BLUE AE5
DACC_IDUMP AG4
3D3V_S0
L10
BLM15AG221SN-GP
C126 SC1U6D3V2KX-GP
C140 SC470P50V2KX-3GP
C138 SC2D2U6D3V3MX-1-GP
220ohm 100MHz
300mA 0.45ohm DC
DACB_VDD V8
DACB_VREF R5
C112 SCD01U16V2KX-3GP
R94 124R2F-U-GP
DACB_RSET R7
U55E
5 OF 14
DACB_VDD 180mA
DACB_VREF
DACB_RSET
DACB_CSYNC U5 TV_SYNC_C
TP39 TPAD28
DACB_RED R6 M_CRMA
DACB_GREEN T5 M_LUMA
DACB_BLUE T6 M_COMP
M_CRMA 34
M_LUMA 34
M_COMP 34
DACB_IDUMP V7
R63 150R2F-1-GP
R62 150R2F-1-GP
R61 150R2F-1-GP
R90 150R2F-1-GP
C623 SCD01U16V2KX-3GP
DY
IFP_VPROBE AM4
IFP_RST# AL5
R318 1KR2J-1-GP
U55G
7 OF 14
IFPAB_VPROBE
IFPAB_RSET
IFPAB_PLLVDD
80mA
IFPAB_PLLGND
IFPA_TXC_N AJ9
IFPA_TXC AK9
IFPA_TXD0_N AJ6
IFPA_TXD0 AH6
IFPA_TXD1_N AH7
IFPA_TXD1 AH8
IFPA_TXD2_N AK8
IFPA_TXD2 AJ8
IFPA_TXD3_N AH5
IFPA_TXD3 AJ5
IFPB_TXC_N AL4
IFPB_TXC AK4
IFPB_TXD4_N AM5
IFPB_TXD4 AM6
IFPB_TXD5_N AL7
IFPB_TXD5 AM7
IFPB_TXD6_N AK5
IFPB_TXD6 AK6
IFPB_TXD7_N AL8
IFPB_TXD7 AK7
IFPA_PLLVDD
1D8V_S0
L7
BLM15AG221SN-GP
C70 SC4D7U6D3V5KX-3GP
C74 SC4700P50V2KX-1GP
C135 SC470P50V2KX-3GP
220ohm 100MHz
300mA 0.45ohm DC
IFPA_IOVDD
1D8V_S0
L25
BLM15AG221SN-GP
C637 SC4D7U6D3V5KX-3GP
C640 SC4700P50V2KX-1GP
C120 SC470P50V2KX-3GP
C639 SC4700P50V2KX-1GP
C130 SC470P50V2KX-3GP
45mA
IFPA_IOVDD
IFPB_IOVDD
45mA
R95 0R2J-2-GP
C127 SC8P250V2CC-GP
R83 0R2J-2-GP
C89 SC8P250V2CC-GP
C100 SC3D3P50V2CN-GP
C118 SC3D3P50V2CN-GP
C109 SC3D3P50V2CN-GP
C631 SC3D3P50V2CN-GP
C633 SC3D3P50V2CN-GP
C101 SC3D3P50V2CN-GP
VGA_TXACLK- 18
VGA_TXACLK+ 18
VGA_TXAOUT0- 18
VGA_TXAOUT0+ 18
VGA_TXAOUT1- 18
VGA_TXAOUT1+ 18
VGA_TXAOUT2- 18
VGA_TXAOUT2+ 18
VGA_TXBCLK- 18
VGA_TXBCLK+ 18
VGA_TXBOUT0- 18
VGA_TXBOUT0+ 18
VGA_TXBOUT1- 18
VGA_TXBOUT1+ 18
VGA_TXBOUT2- 18
VGA_TXBOUT2+ 18
U55I
9 OF 14
CLAMP F6
C113 SCD1U10V2KX-4GP
3D3V_S0
THERMALSENSOR_OBS V6
THERMDN J1
THERMDP K1
35 VGA_THERMDC
VGA_THERMDC
C84 SC2200P50V2KX-2GP
35 VGA_THERMDA
VGA_THERMDA
RN19 SRN10KJ-5-GP
VGA_TCK
TPAD28 TP46
TPAD28 TP49
TPAD28 TP109
VGA_TRST#
JTAG_TCK AJ11
JTAG_TMS AK11
JTAG_TDI AK12
JTAG_TDO AL12
JTAG_TRST# AL13
I2CS_SCL C1 I2CS_SCL
I2CS_SDA B1 I2CS_SDA
RN38 SRN2K2J-1-GP
RN9 SRN2K2J-1-GP
I2CC_SCL G2 LDDC_CLK
I2CC_SDA G1 LDDC_DATA
LDDC_CLK 18
LDDC_DATA 18
GPIO0 K3 HDMI_HDP
HDMI_HDP 16
GPIO1 H1
GPIO2 K5 LBKLT_CTL
GPIO3 G5 LCDVDD_EN
GPIO4 E2 PANEL_BKEN
GPIO5 J5 GFX_CORE_CNTRL
LBKLT_CTL 18
LCDVDD_EN 18
PANEL_BKEN 33
GFX_CORE_CNTRL 53
GPIO6 G6
GPIO7 K6
GPIO8 E1 NB8M_THERM#
GPIO9 D2 SW_VREF
GPIO10 H5
DRA_SYNC/GPIO11 F4
GPIO12 E3
GPIO13 U3
DRB_SYNC/GPIO14 U4
R292 0R2J-2-GP
THERMTRIP_VGA# 33
SW_VREF 48,51,52
R291 2K2R2J-2-GP
HDMI_CEC
HDMI_CEC 16
R385 10KR2J-3-GP PANEL_BKEN
R92 10KR2J-3-GP LCDVDD_EN
R85 10KR2J-3-GP LBKLT_CTL
R91 2K2R2J-2-GP SW_VREF
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA-LVDS/TV/CRT (3/3)
Size A3
Document Number Hawke-Intel
Rev -1
Date: Sunday, September 09, 2007
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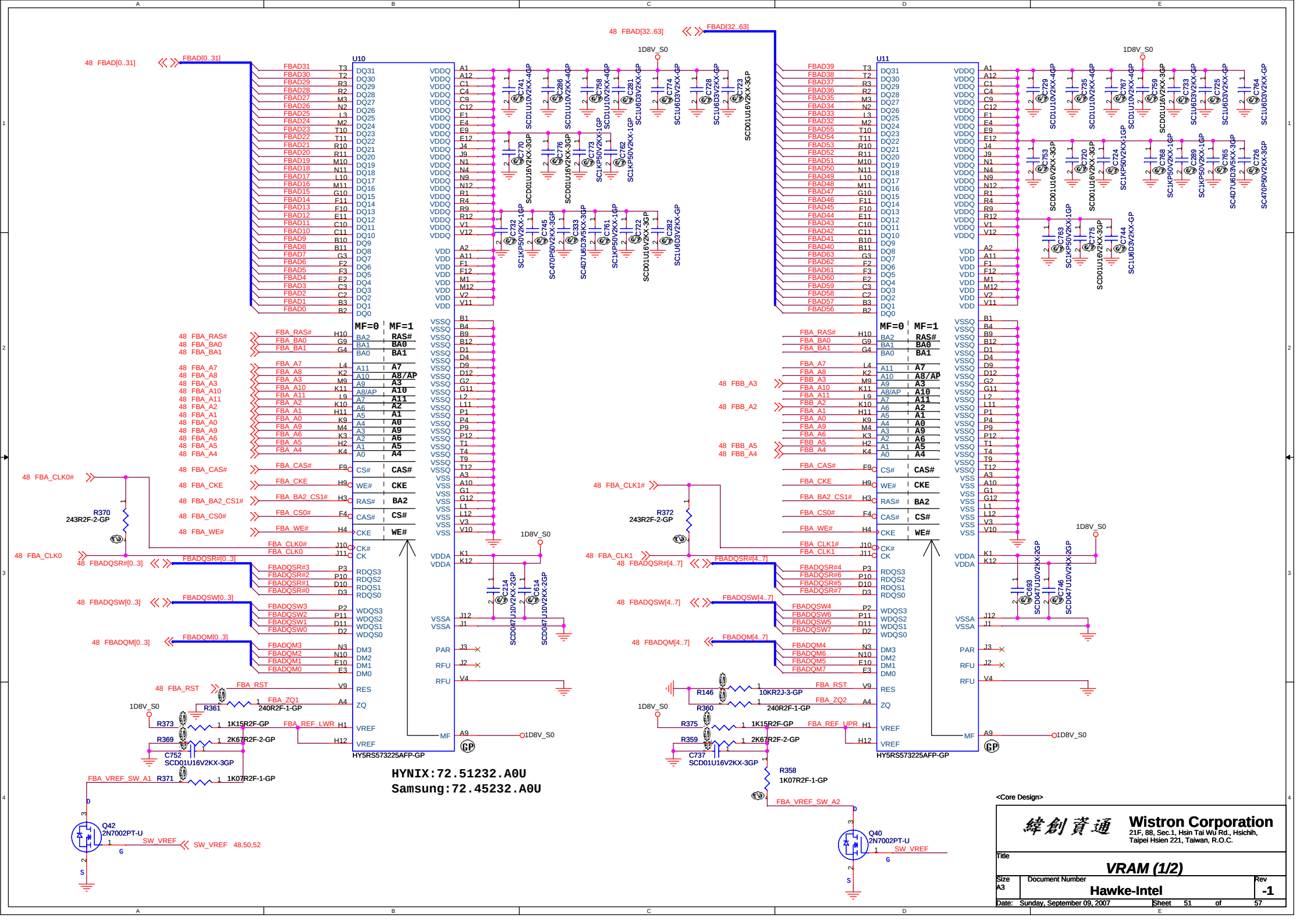
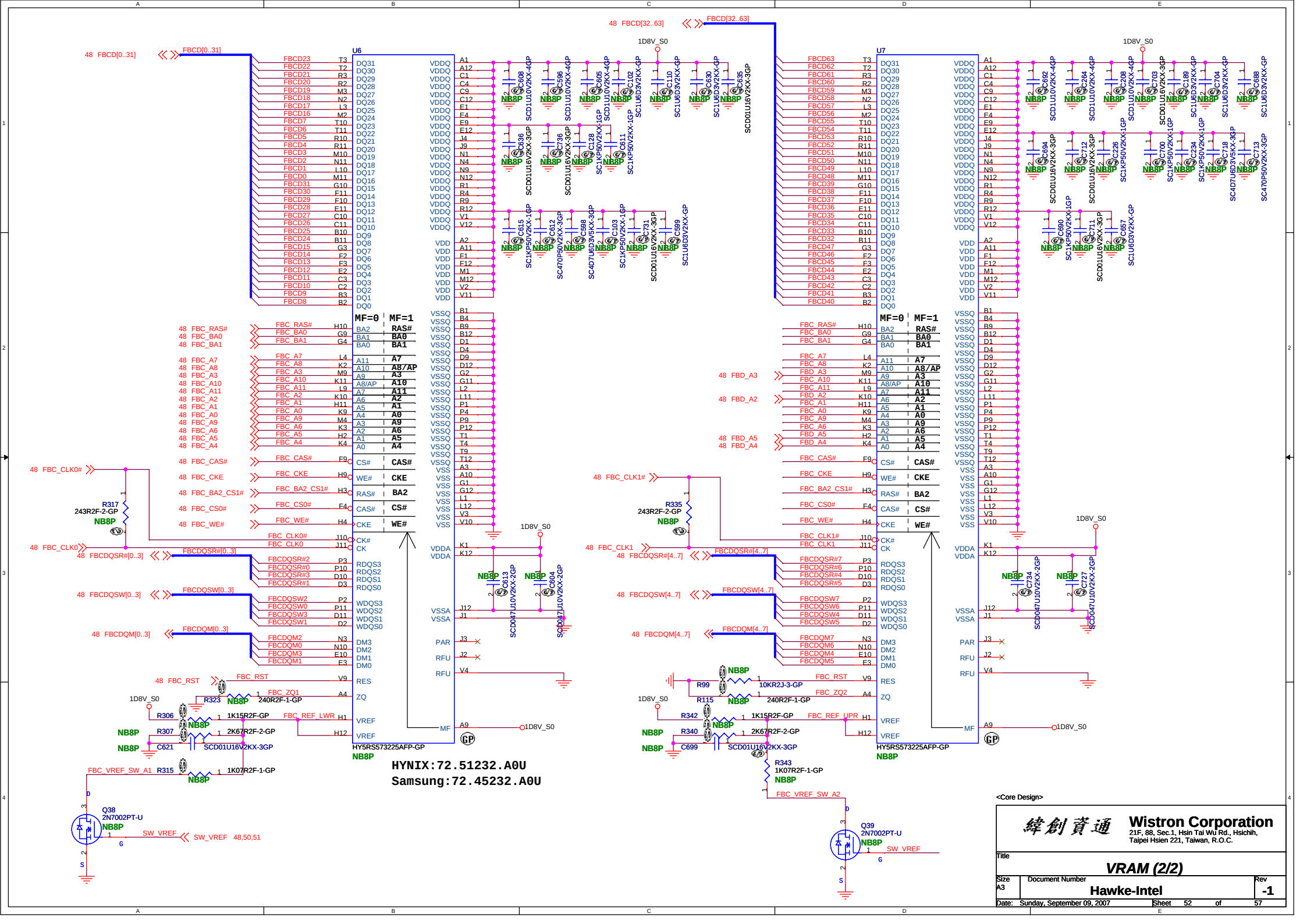
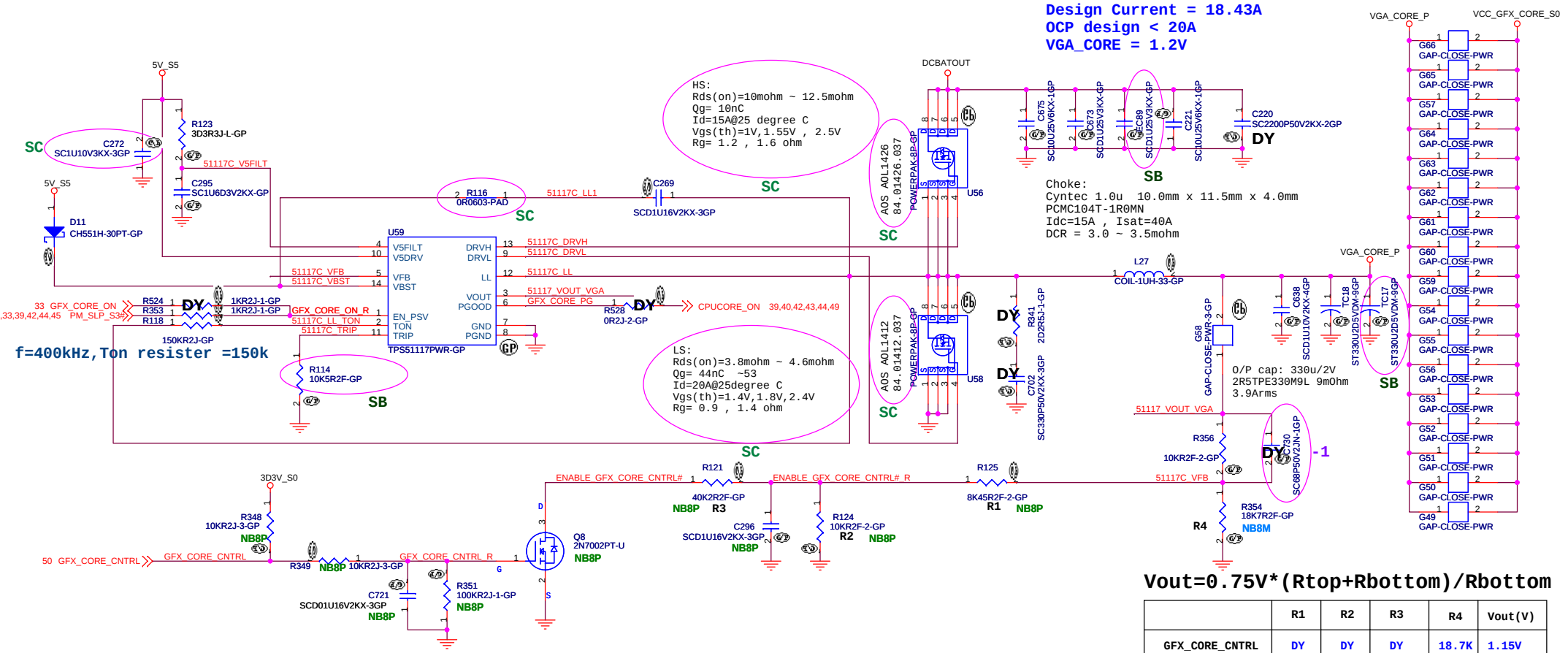

48 FBAD[0..31]
FBAD[0..31]
48 FBAD[32..63]
FBAD[32..63]
1D8V_S0
U10
U11
MF=0
MF=1
HY5RS573225AFP-GP
48 FBA_RAS#
48 FBA_BA0
48 FBA_BA1
48 FBA_A7
48 FBA_A8
48 FBA_A3
48 FBA_A10
48 FBA_A11
48 FBA_A2
48 FBA_A1
48 FBA_A0
48 FBA_A9
48 FBA_A6
48 FBA_A5
48 FBA_A4
48 FBA_CAS#
48 FBA_CKE
48 FBA_BA2_CS1#
48 FBA_CS0#
48 FBA_WE#
48 FBA_CLK0#
48 FBA_CLK0
48 FBADQSR#[0..3]
48 FBADQSW[0..3]
48 FBADQM[0..3]
48 FBA_RST
48 FBB_A3
48 FBB_A2
48 FBB_A5
48 FBB_A4
48 FBA_CLK1#
48 FBA_CLK1
48 FBADQSR#[4..7]
48 FBADQSW[4..7]
48 FBADQM[4..7]
R370
243R2F-2-GP
R372
243R2F-2-GP
R361
240R2F-1-GP
R373
1K15R2F-GP
R369
2K67R2F-2-GP
C752
SCD01U16V2KX-3GP
R371
1K07R2F-1-GP
FBA_VREF_SW_A1
Q42
2N7002PT-U
SW_VREF
SW_VREF 48,50,52
R146
10KR2J-3-GP
R360
240R2F-1-GP
R375
1K15R2F-GP
R359
2K67R2F-2-GP
C737
SCD01U16V2KX-3GP
R358
1K07R2F-1-GP
FBA_VREF_SW_A2
Q40
2N7002PT-U
HYNIX:72.51232.A0U
Samsung:72.45232.A0U
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM (1/2)
Size
A3
Document Number
Hawke-Intel
Rev
-1
Date: Sunday, September 09, 2007
Sheet 51 of 57


48 FBCD[0..31]
FBCD[0..31]
U6
MF=0
MF=1
HY5RS573225AFP-GP
NB8P
HYNIX:72.51232.A0U
Samsung:72.45232.A0U
48 FBCD[32..63]
FBCD[32..63]
U7
MF=0
MF=1
HY5RS573225AFP-GP
NB8P
1D8V_S0
Q38
2N7002PT-U
Q39
2N7002PT-U
SW_VREF
SW_VREF 48,50,51
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM (2/2)
Size
A3
Document Number
Hawke-Intel
Rev
-1
Date: Sunday, September 09, 2007
Sheet 52 of 57



	R1	R2	R3	R4	Vout(V)
GFX_CORE_CNTRL NA	DY	DY	DY	18.7K	1.15V
GFX_CORE_CNTRL Low	8.45K	10K	40.2K to FET	DY	1.15V
GFX_CORE_CNTRL High	8.45K	10K	40.2K to GND	DY	1.2V

<Core Design>

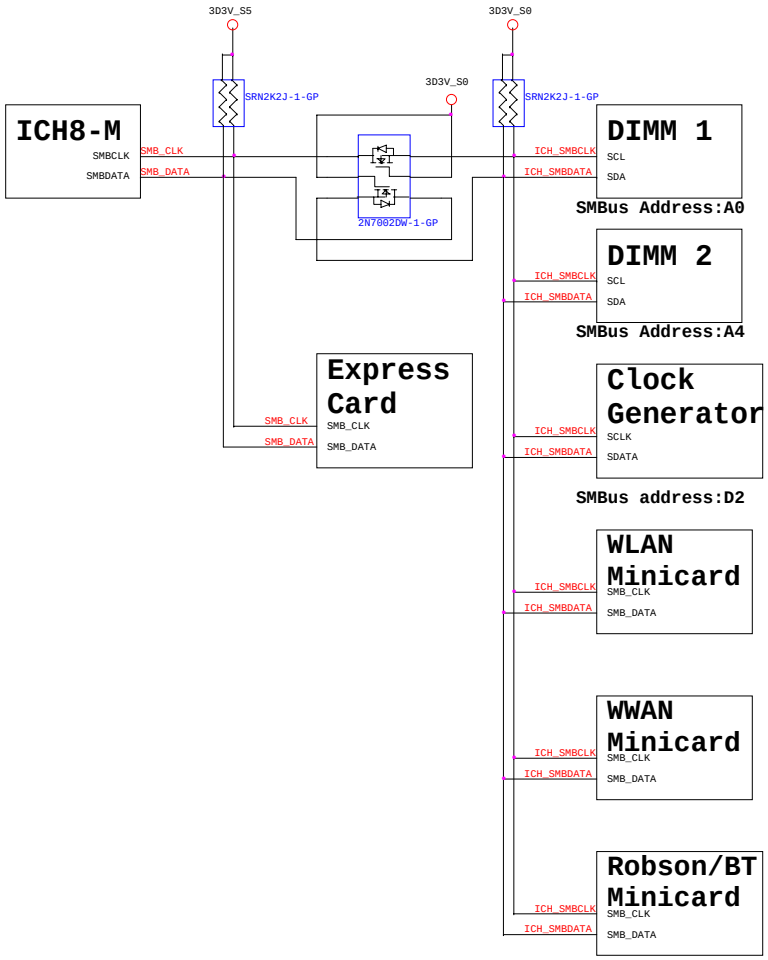
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC VGA_Core

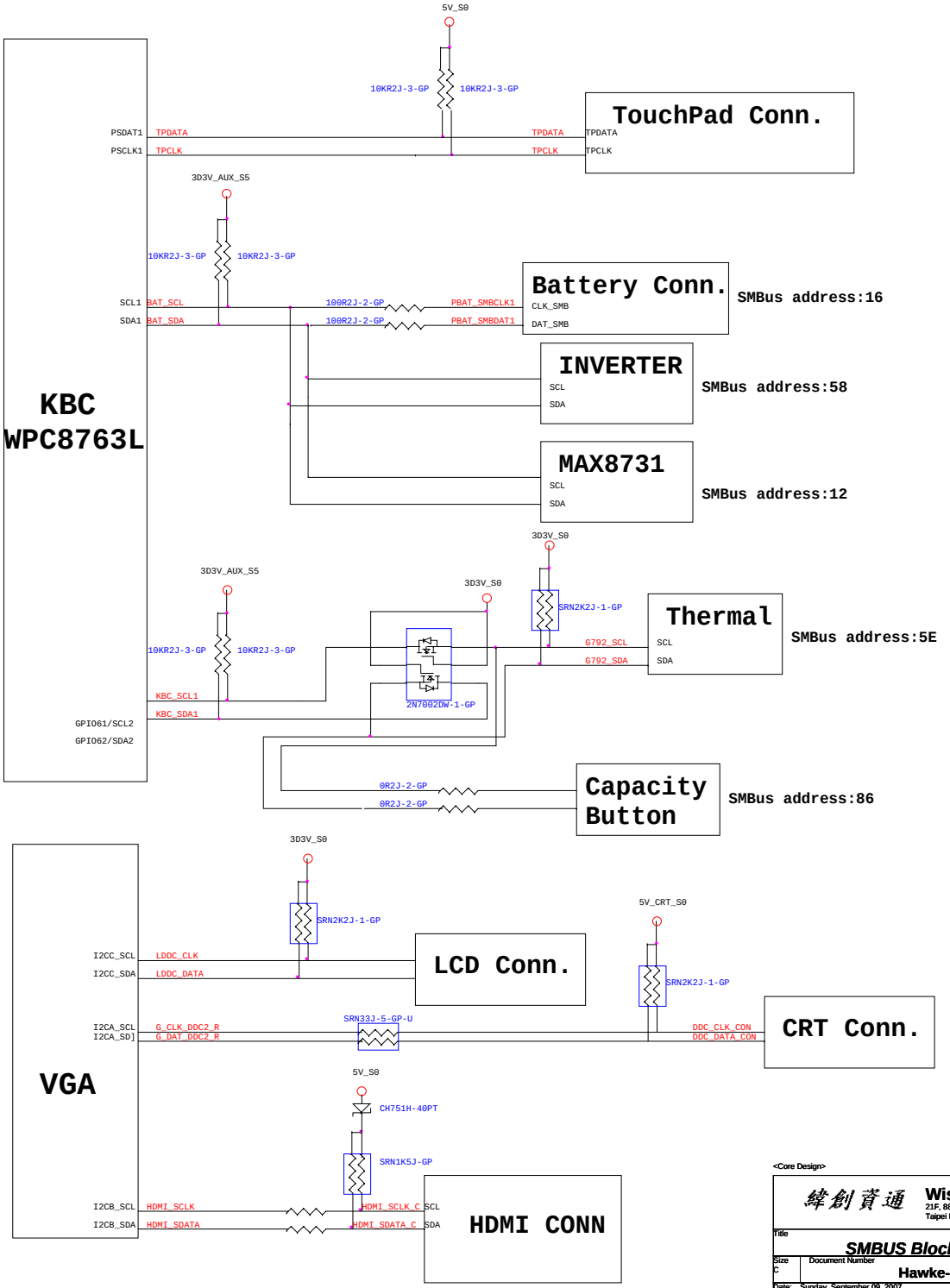
Size: A3 | Document Number: Hawke-Intel | Rev: -1

Date: Sunday, September 09, 2007 | Sheet 53 of 57

ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

Size	Document Number	Rev
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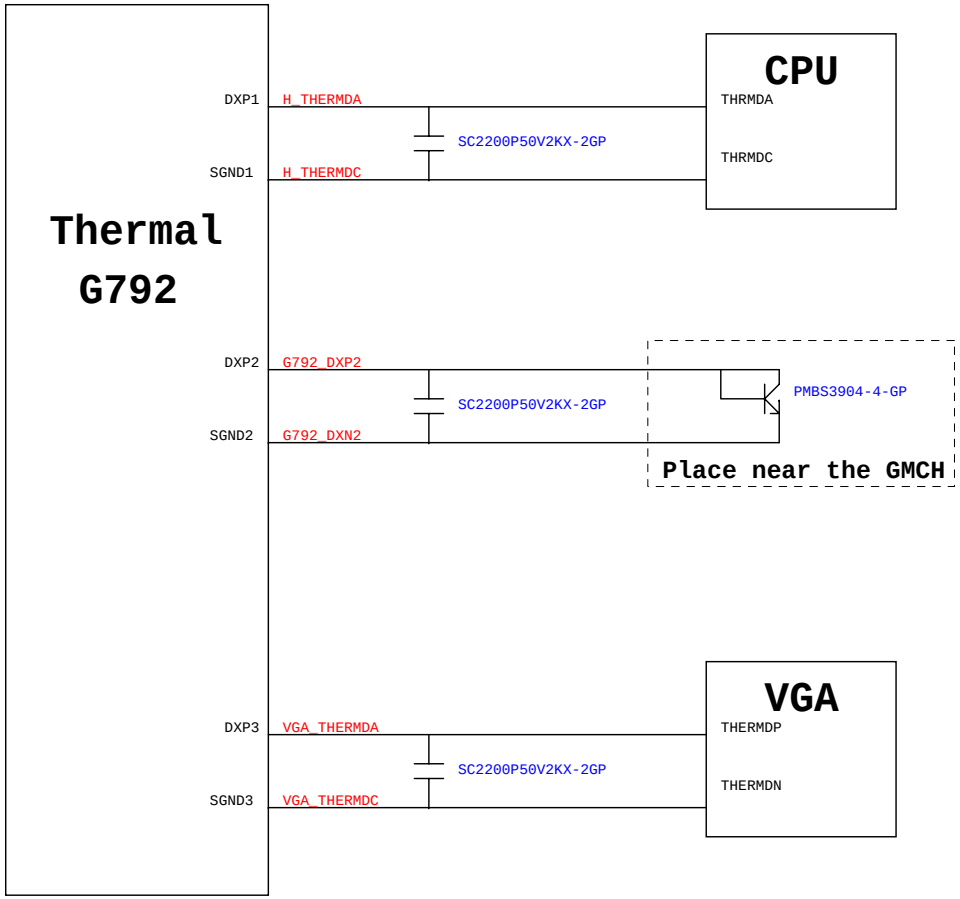
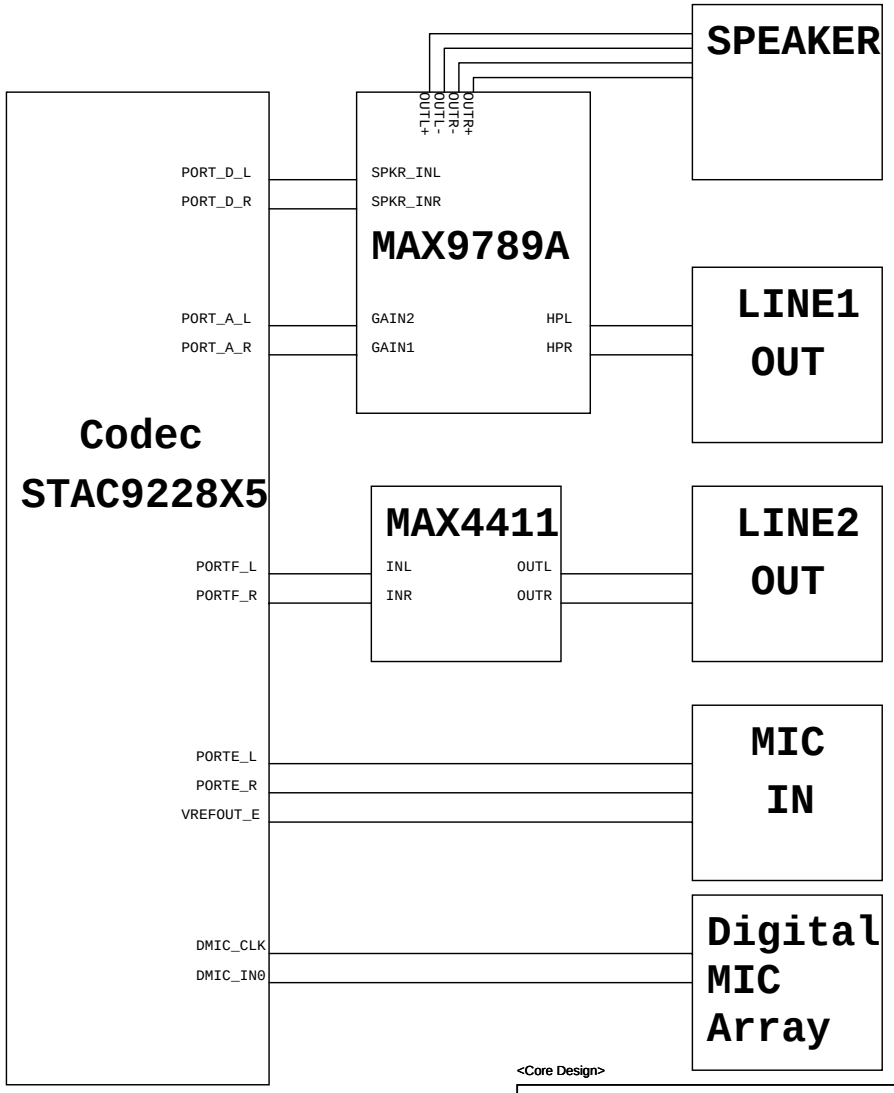
Thermal Block Diagram



Audio Block Diagram



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram		
Size: B	Document Number: Hawke-Intel	Rev: -1
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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	4	Changed R431 from 10K ohm to 2.2K ohm.	Follow M08 design.	EE
		2	4	Changed X4's CL from 20pF to 10pF and changed C392 and C399 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		3	4	Changed RN27, RN28, RN29 and RN31 from 0 ohm to 22 ohm.	To solved these clock signals' Slew Rate are over spec.	EE
		4	18	Changed LVDS connector from 42-pin to 40-pin.	By ME suggestion.	ME
		5	18,33	Connected the LCD1 pin 3 to GND and connected pin 6 to WPC8763's GPIO05 (pin 108 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the LCD cable PAID.	EE
		6	18	Added EC75-EC78 near CAMERA1.	By EMC team suggestion.	EMC
		7	20	Change C354 and C355 from 15pF to 12pF and changed X1 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		8	21	Added R526 10K ohm between GPIO26 and 3D3V_S0, removed R404.	To solved 3D3V_S0 has leakage when S3 and S5.	EE
		9	21	Added the reserved Q47, D31, R530, R531 and R532.	For test EC_RMRST#_R circuit.	EE
		10	21	Changed R442 from 22.6 ohm to 20 ohm.	To sloved the left side USB ports and Camera USB's eye diagram fail.	EE
		11	23	Changed HDD connector.	By ME suggestion.	ME
		12	25	Changed 1394 connector.	To used reverse type by ME suggestion.	ME
		13	25	Changed X5's CL from 20pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		14	25	Removed R466, U26, R192 and D19, and connected the net MC_PWR_CTRL_0 to U25 pin 4.	For these materials are no used.	EE
2007/07/06	X00 to X01	15	25	Populated C887, C888 and C894-C896.	By EMC team suggestion.	EMC
		16	26	Changed C387 and C390 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		17	27	Changed RJ1 connector.	By ME suggestion.	ME
		18	30	Changed U61 from 8Mbits to 16Mbits SPI ROM.	By customer requirement.	EE
		19	30	Added EC79-EC82 near CAP1.	By EMC team suggestion.	EMC
		20	30	Added EC83-EC88 near BT1.	By EMC team suggestion.	EMC
		21	30	Added EC90-EC91 near CN2 (Biometric).	By EMC team suggestion.	EMC
		22	31	Changed C880 and C881 from 0402 size to 0603 size.	Follow Thurman design.	EE
		23	32	Swaped the nets AUD_HP1_OUT_R1, AUD_HP1_OUT_L1 with AUD_AMP_GAIN1, AUD_AMP_GAIN2.	To sloved the HP1 hadn't output.	EE
		24	32	Changed R211 and R212 from 100K ohm to 10M ohm.	To sloved the AUD_HP1_EN and AUD_HP2_EN volatge level lower than 2V.	EE
		25	33	De-pop R396 and populated R395.	To changed the MB version id to SB.	EE
		26	33	Changed R391 and R405 from 10K ohm to 100K ohm.	To sloved the INSTANT_BTN# and SNIFFER_PWR_SW# can't work.	EE
		27	33	Added R527 100K ohm between WLAN/BT_BTN# and 3D3V_AUX_S5.	To sloved the WLAN/BT_BTN# can't work.	EE
		28	33	Changed X2 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		29	33,36	Changed KB1 from 25-pin to 27-pin connector, connected the KB1 pin 27 to GND and connected pin 26 to WPC8763's GPI92 (pin 99 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the KB cable PAID.	ME,EE
		30	33	Changed R408 and R389 from 10K ohm to 4.7K ohm.	By Vendor's FAE suggestion.	EE
		31	35	Changed FAN1 from 4-pin to 3-pin connector.	By ME suggestion.	ME
		32	36	Added R534, Q48 and R535 off SATA_LED# and Q23.	Supported the HDD LED is dim when sinffer switch press.	EE
		33	36	Connected LED2 pin A from 5V_S0 to 5V_S5.	To sloved the Power LED can't breath when system enter S3.	EE
		34	38	Changed C530 and C531 from 1206 size to 1210 size and populated C7.	To solved noise when battery full load.	Power
		35	39	Changed R477 from 12.1K ohm to 13.3K ohm and changed R468 from 12.1K ohm to 11.8K ohm.	To adjust 3.3V and 5V current limit by power team suggestion.	Power
		36	40	Changed R7 from 12.7K ohm to 11.8K ohm and changed R468 from 3.24K ohm to 3.65K ohm.	To adjust CPU Vcore current limit by power team suggestion.	Power
		37	42	Changed R135 from 12.1K ohm to 11K ohm .	To adjust 1.05V current limit by power team suggestion.	Power
		38	43	Populated C529.	By EMC team suggestion.	EMC
		39	46	Added more one hole H33.	By EMC team suggestion.	EMC
		40	46	Populated EC28 and EC31.	By EMC team suggestion.	EMC
		41	47	Added C900, C901, C904 10uF and TC26 100uF.	To sloved VGA Vcore had OVP when run 3Dmark.	Power
		42	53	Changed R135 from 12.1K ohm to 10.5K ohm .	To adjust CPU Vcore current limit by power team suggestion.	Power
		43	53	Added EC89 0.1uF between DCBATOUT and GND.	By EMC team suggestion.	EMC

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Title: ***HISTORY from X00 to X01***

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	4	Changed U22 from ICS 9LPRS365BKLFT to Realtek RTM875M-606-LF.	Changed clock gen symbol from ICS 9LPRS365BKLFT to Realtek RTM875M-606-LF.	EE
		2	15	Changed HDMI power rail from +5V_HDMI to 5V_S0.	Follow Thurman design.	EE
		3	17	Populated D4, D5, D6, D7 and D8.	By NV GPU ESD requirement.	EMC
		4	17	Changed L1, L2 and L4 from BLM18BA100SN1 to BLM18BB470SN1	To solve the ring on RGB singnal.	EE
		5	18,33	Added D32, connected pin 1 to LCDVDD_TST_EN, pin 2 to LCDVDD_EN and pin 3 to ENVDD. Changed R276 from 0 to 100k ohm and changed R276.1 to GND	Added LCDVDD_TST_EN from U17.27 to control U53.3	EE
		6	18	Disconnted LCD1 pin 3 and pin 10	To prevent the power short to GND.	EE
		7	21	Added R542 for ECSCI# need to pull up 3D3V_S0	To solve one of CPU core always loading 100%.	EE
		8	27	Added EC92 22pF between NEWCARD_CLKREQ# and GND	By EMC team suggestion.	EE
		9	27	Added note for transformer source part number.	By EMC team suggestion.	EE
		10	29	1.Changed D20 to U73 for Bluetooth Action circuit. 2.Reserved U73, R193 and R195, populated R194.	1.It can be used both BT module and BT mini-card. 2.Just keep BT module now.	EE
		11	29, 33	Connect MINI2 pin 20 to U17.24 (GPO47 of KBC).	Changed WWAN enable WiFi RF controlled by another GPIO pin (U17.24 is GPO47 of KBC).	EE
		12	30, 33	Rename SNIFFER_YELLOW# to SNIFFER_YELLOW, SNIFFER_BLUE# to SNIFFER_BLUE.	These pins are High active.	EE
		13	30	Disconnted SNIFFER_BD1 pin 8 and CAP1 pin 7.	To prevent power short to GND.	EE
2007/08/17	X01 to X02	14	30	Changed EC90 and EC91 from 22pF to MLVG0402220NV05BP.	By EMC team suggestion.	EMC
		15	32	Populated EC24, EC25, EC26 and EC27 and change to 1000pF.	By EMC team suggestion.	EMC
		16	32	Changed Q45 to U47 and added R543.	To add AUD_SPK_ENABLE# controlled by AMP_MUTE#.	EE
		17	32	Changed R197 from 0 ohm to 100K ohm and pull up to +5V_SPK_AMP, dispopulated R505 and populated R213.	To solve HP1, HP2 and Speaker have "BoBo" noisy when power on, off, enter S3.	EE
		18	33	Populated R396 and R398, dispopulated R395 and R399.	Change Board ID to version SC.	EE
		19	36	Populated Q48 and R534, dispopulated R535.	HDD LED should be dim when power on by Sniffer button.	EE
		20	36	Changed C275 and C276 from reserved 33pF to MLVG0402220NV05BP, and populated them	By EMC team suggestion.	EMC
		21	36	Changed KB EMI caps from 220pF to 180pF.	To solved the word has repeat symptom when key-in.	EE
		22	38	The U42 and U44 were swap the main source and 2nd source.	To prevented used AO4468 that SI4800BDY 2nd source on charger H/S and L/S MOS.	EE
		23	39	Populated R485 and dispopulated R489.	To changed 3V and 5V PWM to Skip mode.	EE
		24	42, 43, 53	Changed C329, C566 and C272 rated voltage from 6.3V to 10V.	For derating issues by power team requirment.	EE
		25	43, 53	Change the U56 and U39 from 2nd source to main source, and swap the U38 and U58's the main source and 2nd source	To combined U39 and U56 material item of BOM with CPU H/S MOS (U4 and U35).	EE
		26	20	Changed C354 and C355 from 12pF to 8.2pF.	For Negative Resistance of X1 isn't enough.	EE
		27	33	Changed C350 and C351 from 15pF to 10pF.	For Negative Resistance of X2 isn't enough.	EE

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