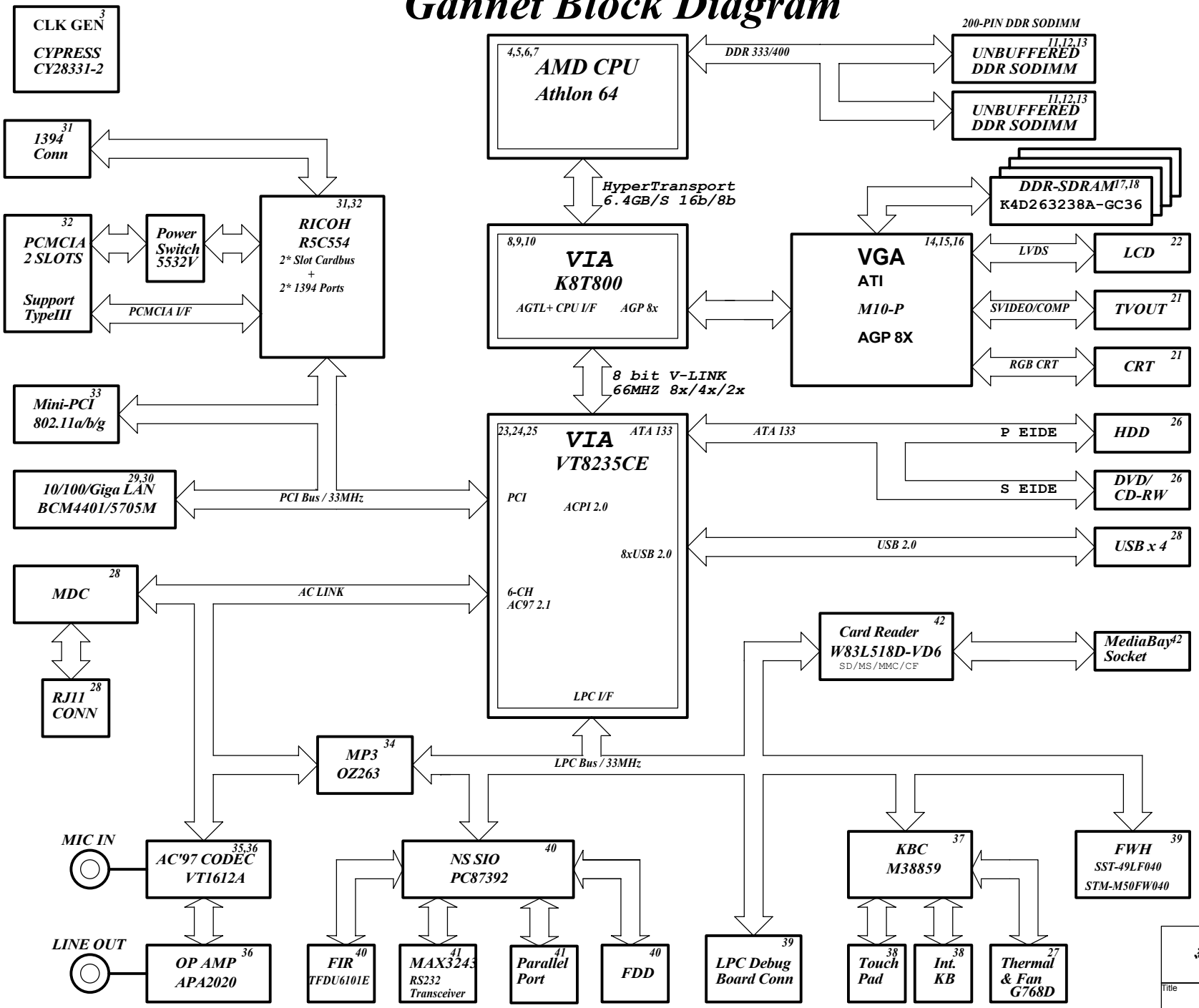
Gannet Block Diagram



PCB Layer Stackup

For High Speed Trace	L1: Signal 1 L2: GND L3: Signal 2 L4: VCC L5: Signal 3 L6: GND L7: Signal 4 L8: Signal 5
For Low Speed Trace	L1: Signal 1 L2: GND L3: Signal 2 L4: Signal 3 L5: VCC L6: GND L7: Signal 4 L8: Signal 5

Battery Charger 44

ATINY12/MAX1645

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC 45

MAX1999

INPUT	OUTPUT
DCBATOUT	5V_S5 +5V_UP_S5 3D3V_S5

DDR&VDDR DC/DC 46

MAX1715/CM8500

INPUT	OUTPUT
DCBATOUT	VGA VCORE 1D25V_SO VVGAEER

CPU V_CORE 47

Controller-HIP6301 Drive-ISL6207*2(2 Phase)

INPUT	OUTPUT
DCBATOUT	VCC_CORE

SYSTEM POWER 48,49

TPS5110/FDC653N/APL1117 G913C/LP2951ACM/FDS9412

INPUT	OUTPUT
5V_S3 3D3V_S5 DCBATOUT 2D5V_S3 VVGADDR	5V_S0 3D3V_S3 3D3V_S0 3D3V_LAN_S3 1D8V_S5 2D5V_S3 1D8V_S0 +5V_AUX_S5 2D5V_S0 1D5V_S0

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Title: Block Diagram

Size: A3 | Document Number: Gannet | Rev: -1

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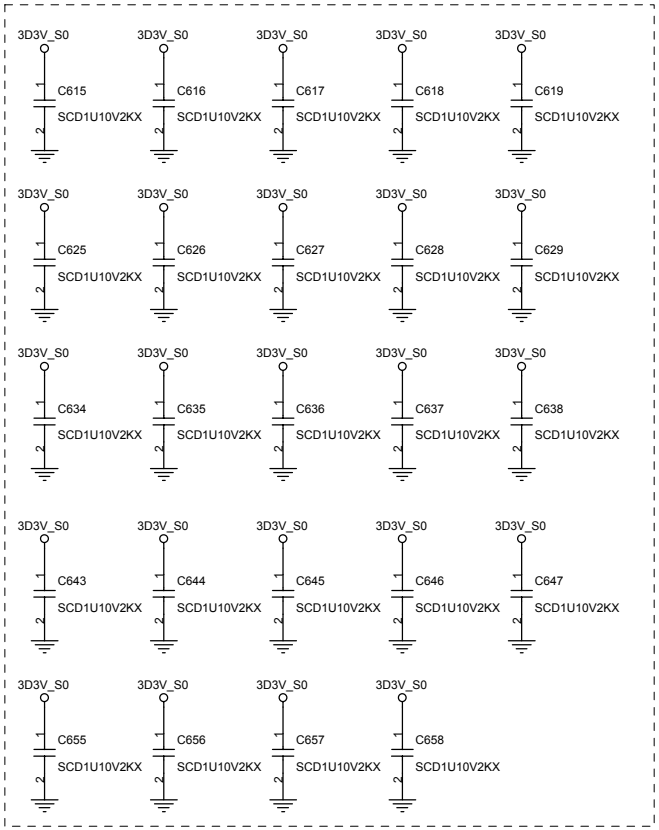
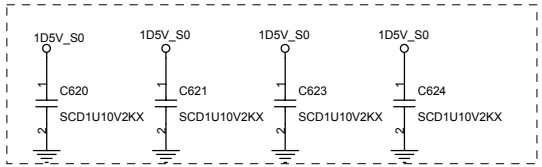
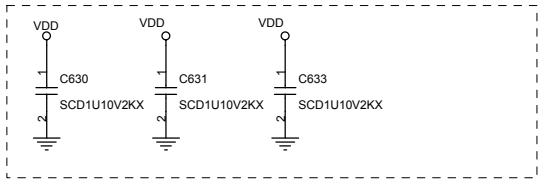
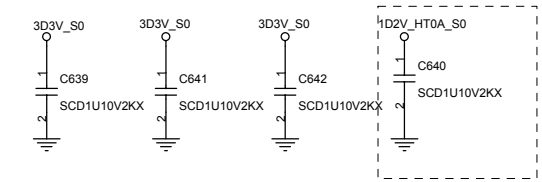
J8 REVISION HISTORY

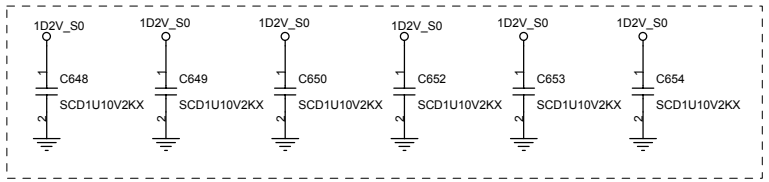
6/12 EMI Bypass Cap.

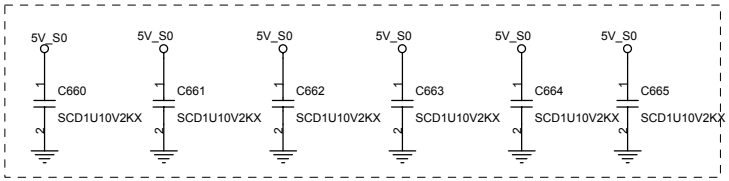


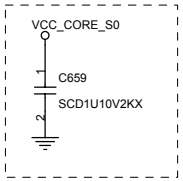












PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTF#	P_REQ#0/P_GNT#0
R5C554-CardBus A	AD22	P_INTB#	P_REQ#1/P_GNT#1
R5C554-CardBus B	AD22	P_INTC#	P_REQ#1/P_GNT#1
R5C554-IEEE 1394	AD22	P_INTD#	P_REQ#1/P_GNT#1
VGA-ATI M10-P		P_INTA#	
BCM-5705M	AD23	P_INTE#	P_REQ#2/P_GNT#2

16,46 1D2V_S0 — 1D2V_S0
4,8,10,50 1D2V_HT0A_S0 — 1D2V_HT0A_S0
4,6 1D2V_HT0B_S0 — 1D2V_HT0B_S0
29 1D2V_LAN_S5 — 1D2V_LAN_S5
5,6,7,12,13,46,50 1D25V_S3 — 1D25V_S3
9,10,14,16,20,49 1D5V_S0 — 1D5V_S0
15,16,49,50 1D8V_S0 — 1D8V_S0
15,16,17,18,46,49 VVGADDR — VVGADDR
6,8,9,10,16,19,20,23,24,25,31,48,50 2D5V_S0 — 2D5V_S0
5,6,7,10,11,13,46,48,49,50 2D5V_S3 — 2D5V_S3
6,24,25 2D5V_S5 — 2D5V_S5
3,8,9,10,11,14,16,19,20,21,22,23,24,25,27,28,29,31,32,33,34,35,36,37,38,39,40,41,42,43,47,48,49,51 3D3V_S0 — 3D3V_S0
10,22,28,34,37,48 3D3V_S3 — 3D3V_S3
22,23,24,25,27,29,34,37,43,45,48,50,51 3D3V_S5 — 3D3V_S5
19,21,22,23,24,25,26,27,28,30,32,33,35,36,37,38,39,40,41,42,43,46,47,48,50,51 5V_S0 — 5V_S0
37,46,48,49 5V_S3 — 5V_S3
27,45,48,50,51 5V_S5 — 5V_S5
34,43,49,50,51 +5V_AUX_S5 — +5V_AUX_S5
22,43,44,48,49 +5V_UP_S5 — +5V_UP_S5
22,27,44,45,46,47,48,49 DCBATOUT — DCBATOUT
7,47 VCC_CORE_S0 — VCC_CORE_S0
43,44 AD+ — AD+

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Title: **REVISION HISTORY**

Size	Document Number	Rev
A3	GANNET	-1

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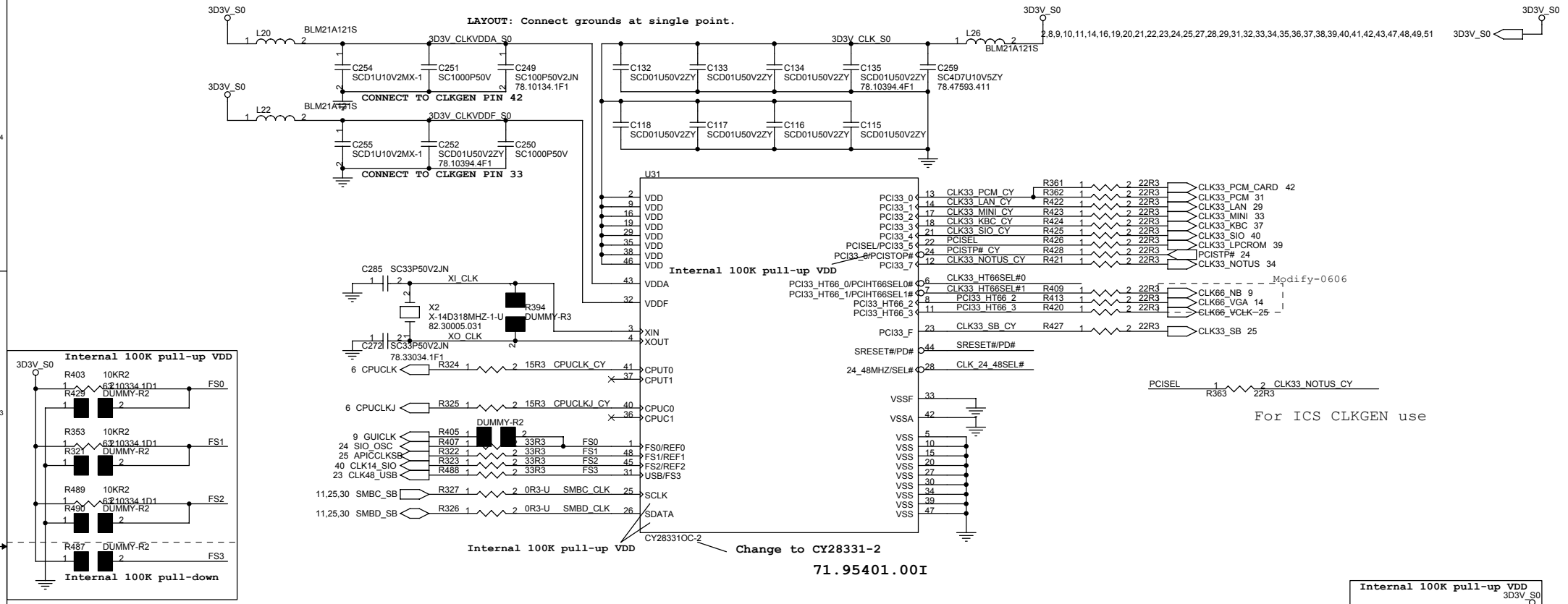

Input Configuration				Clock Generator Output				
FS3	FS2	FS1	FS0	PCI_HT#	CPU (MHz)	PCI33_HT66 (MHz)	PCI33 (MHz)	
0	0	0	0	X	Hi-Z	Hi-Z	Hi-Z	All output Tri-state
0	0	0	1	X	133.9	33.5 or 67.0	33.5	
0	0	1	0	X	166.9	33.4 or 66.8	33.4	
0	0	1	1	X	200.9	33.5 or 67.0	33.5	
0	1	0	0	X	100	33.3 or 66.7	33.3	
0	1	0	1	X	133.33	33.3 or 66.7	33.3	
0	1	1	0	X	166.66	33.3 or 66.7	33.3	
* 0	1	1	1	X	200	33.3 or 66.7	33.3	Normal Hammer operation
1	0	0	0	X	105.0	35.0 or 70.0	35.0	
1	0	0	1	X	110.0	36.7 or 73.3	36.7	
1	0	1	0	X	210.0	35.0 or 70.0	35.0	
1	0	1	1	X	240.0	30.0 or 60.0	30.00	
1	1	0	0	X	270.0	33.8 or 67.5	33.8	
1	1	0	1	X	233.3	27.2 or 58.3	27.2	
1	1	1	0	X	266.7	33.3 or 66.7	33.3	
1	1	1	1	X	300.0	37.5 or 75.0	37.5	

	PCISEL	PIN22
*	0	PCI33_6
	1	PCISTOP#

	24_48 SEL#	24_48MHz
*	0	48MHz
	1	24MHz

PCIHT66 SEL[1:0]#PCI33_HT66[3:0]					
SEL1	SEL0	PIN6	PIN7	PIN8	PIN11
* 0	0	HT66	HT66	HT66	HT66
0	1	HT66	HT66	HT66	PCI33
1	0	HT66	HT66	PCI33	PCI33
1	1	HT66	PCI33	PCI33	PCI33

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Title: ***CLKGEN_CY28331***

Size: A3 | Document Number: **Gannet** | Rev: -1

Date: Thursday, December 04, 2003 | Sheet 3 of 51

Clawhammer HT Interface

1D2V_HT0A_S0
2,8,10,50 1D2V_HT0A_S0
1D2V_HT0B_S0
6 1D2V_HT0B_S0

LAYOUT: Close to CPU within 1 inch #24665 PG:135

1D2V_HT0A_S0

C25 SCD22U10V3KX 78.22423.2B1
C27 SCD22U10V3KX 78.22423.2B1
C587 SCD22U10V3KX 78.22423.2B1
C588 SCD22U10V3KX 78.22423.2B1

Between CPU and NB

1D2V_HT0A_S0

C28 SCD22U10V3KX 78.22423.2B1
C29 SCD22U10V3KX 78.22423.2B1
C33 SCD22U10V3KX 78.22423.2B1
C34 SCD22U10V3KX 78.22423.2B1

11/11 add SCD22U for AMD suggest.

LAYOUT: Place bypass cap on topside of board near HTT power pins that are not connected directly to downstream HTT device, but connected internally to other HTT power pins.

1D2V_HT0B_S0
C576 SC4D7U10V5ZY 78.47593.411

HTT for CPU sideA Transmit power and NB sideA Receive power

HTT for CPU sideB Receive power and NB sideA Transmit power

1D2V_HT0A_S0
C586 SCD1U16V
1D2V_HT0B_S0
C578 SCD1U16V

U20A

	D29	VLDT0_A	VLDT0_B	AH29	
	D27	VLDT0_A	VLDT0_B	AH27	
	D25	VLDT0_A	VLDT0_B	AG28	
	C28	VLDT0_A	VLDT0_B	AG26	
	C26	VLDT0_A	VLDT0_B	AF29	
	B29	VLDT0_A	VLDT0_B	AE28	
	B27	VLDT0_A	VLDT0_B	AE25	
8 NB0CADOUT[15..0]	NB0CADOUT15	T25	L0_CADIN_H15	L0_CADOUT_H15	N26	CPUCADOUT15	CPUCADOUT[15..0] 8
8 NB0CADOUTJ[15..0]	NB0CADOUTJ15	R25	L0_CADIN_L15	L0_CADOUT_L15	N27	CPUCADOUTJ15	CPUCADOUTJ[15..0] 8
	NB0CADOUT14	U27	L0_CADIN_H14	L0_CADOUT_H14	L25	CPUCADOUT14	
	NB0CADOUTJ14	U26	L0_CADIN_L14	L0_CADOUT_L14	M25	CPUCADOUTJ14	
	NB0CADOUT13	V25	L0_CADIN_H13	L0_CADOUT_H13	L26	CPUCADOUT13	
	NB0CADOUTJ13	U25	L0_CADIN_L13	L0_CADOUT_L13	L27	CPUCADOUTJ13	
	NB0CADOUT12	W27	L0_CADIN_H12	L0_CADOUT_H12	J25	CPUCADOUT12	
	NB0CADOUTJ12	W26	L0_CADIN_L12	L0_CADOUT_L12	K25	CPUCADOUTJ12	
	NB0CADOUT11	AA27	L0_CADIN_H11	L0_CADOUT_H11	G25	CPUCADOUT11	
	NB0CADOUTJ11	AA26	L0_CADIN_L11	L0_CADOUT_L11	H25	CPUCADOUTJ11	
	NB0CADOUT10	AB25	L0_CADIN_H10	L0_CADOUT_H10	G26	CPUCADOUT10	
	NB0CADOUTJ10	AA25	L0_CADIN_L10	L0_CADOUT_L10	G27	CPUCADOUTJ10	
	NB0CADOUT9	AC27	L0_CADIN_H9	L0_CADOUT_H9	E25	CPUCADOUT9	
	NB0CADOUTJ9	AC26	L0_CADIN_L9	L0_CADOUT_L9	F25	CPUCADOUTJ9	
	NB0CADOUT8	AD25	L0_CADIN_H8	L0_CADOUT_H8	F26	CPUCADOUT8	
	NB0CADOUTJ8	AC25	L0_CADIN_L8	L0_CADOUT_L8	E27	CPUCADOUTJ8	
	NB0CADOUT7	T27	L0_CADIN_H7	L0_CADOUT_H7	N29	CPUCADOUT7	
	NB0CADOUTJ7	T28	L0_CADIN_L7	L0_CADOUT_L7	P29	CPUCADOUTJ7	
	NB0CADOUT6	V29	L0_CADIN_H6	L0_CADOUT_H6	M28	CPUCADOUT6	
	NB0CADOUTJ6	U29	L0_CADIN_L6	L0_CADOUT_L6	M27	CPUCADOUTJ6	
	NB0CADOUT5	V27	L0_CADIN_H5	L0_CADOUT_H5	L29	CPUCADOUT5	
	NB0CADOUTJ5	V28	L0_CADIN_L5	L0_CADOUT_L5	M29	CPUCADOUTJ5	
	NB0CADOUT4	Y29	L0_CADIN_H4	L0_CADOUT_H4	K28	CPUCADOUT4	
	NB0CADOUTJ4	W29	L0_CADIN_L4	L0_CADOUT_L4	K27	CPUCADOUTJ4	
	NB0CADOUT3	AB29	L0_CADIN_H3	L0_CADOUT_H3	H28	CPUCADOUT3	
	NB0CADOUTJ3	AA29	L0_CADIN_L3	L0_CADOUT_L3	H27	CPUCADOUTJ3	
	NB0CADOUT2	AB27	L0_CADIN_H2	L0_CADOUT_H2	G29	CPUCADOUT2	
	NB0CADOUTJ2	AB28	L0_CADIN_L2	L0_CADOUT_L2	H29	CPUCADOUTJ2	
	NB0CADOUT1	AD29	L0_CADIN_H1	L0_CADOUT_H1	F28	CPUCADOUT1	
	NB0CADOUTJ1	AC29	L0_CADIN_L1	L0_CADOUT_L1	F27	CPUCADOUTJ1	
	NB0CADOUT0	AD27	L0_CADIN_H0	L0_CADOUT_H0	F29	CPUCADOUT0	
	NB0CADOUTJ0	AD28	L0_CADIN_L0	L0_CADOUT_L0	F29	CPUCADOUTJ0	

Used SideB Power Plane

Used SideA Power Plane

1D2V_HT0B_S0

8 NB0HTTCLKOUT1	NB0HTTCLKOUT1	Y25	L0_CLKIN_H1	L0_CLKOUT_H1	J26	CPUHTTCLKOUT1	CPUHTTCLKOUT1 8
8 NB0HTTCLKOUTJ1	NB0HTTCLKOUTJ1	W25	L0_CLKIN_L1	L0_CLKOUT_L1	J27	CPUHTTCLKOUTJ1	CPUHTTCLKOUTJ1 8
8 NB0HTTCLKOUT0	NB0HTTCLKOUT0	Y27	L0_CLKIN_H0	L0_CLKOUT_H0	J29	CPUHTTCLKOUT0	CPUHTTCLKOUT0 8
8 NB0HTTCLKOUTJ0	NB0HTTCLKOUTJ0	Y28	L0_CLKIN_L0	L0_CLKOUT_L0	K29	CPUHTTCLKOUTJ0	CPUHTTCLKOUTJ0 8
R796 1 2 49D9R3F CPUHTTCTLIN1		R27	L0_CTLIN_H1	L0_CTLOUT_H1	N25	CPUHTTCTLOUT1	CPUHTTCTLOUT1 TP176
R795 1 2 49D9R3F CPUHTTCTLINJ1		R26	L0_CTLIN_L1	L0_CTLOUT_L1	P25	CPUHTTCTLOUTJ1	CPUHTTCTLOUTJ1 TP177
	NB0HTTCTLOUT	T29	L0_CTLIN_H0	L0_CTLOUT_H0	P28	CPUHTTCTLOUT0	CPUHTTCTLOUT0 8
8 NB0HTTCTLOUT	NB0HTTCTLOUTJ	R29	L0_CTLIN_L0	L0_CTLOUT_L0	P27	CPUHTTCTLOUTJ0	CPUHTTCTLOUTJ0 8

BGA754-SKT-U
62.10030.041

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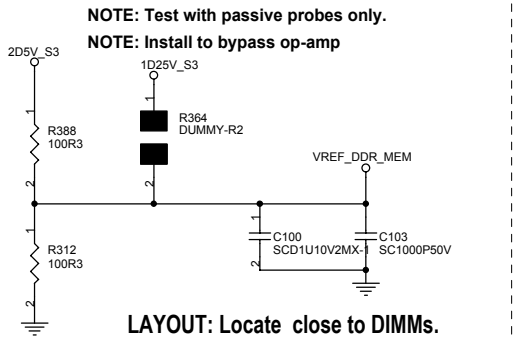
Title: ***CPU(1/4)_HyperTransport I/F***

Size: A3 | Document Number: **Gannet** | Rev: -1

Date: Thursday, December 04, 2003 | Sheet 4 of 51

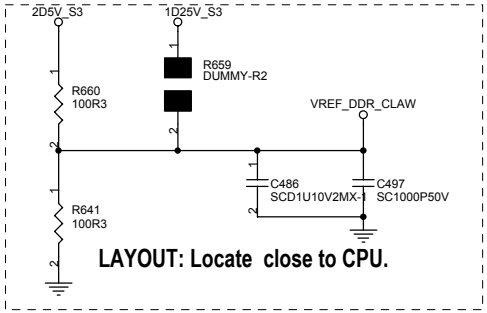
Clawhammer DDR Interface

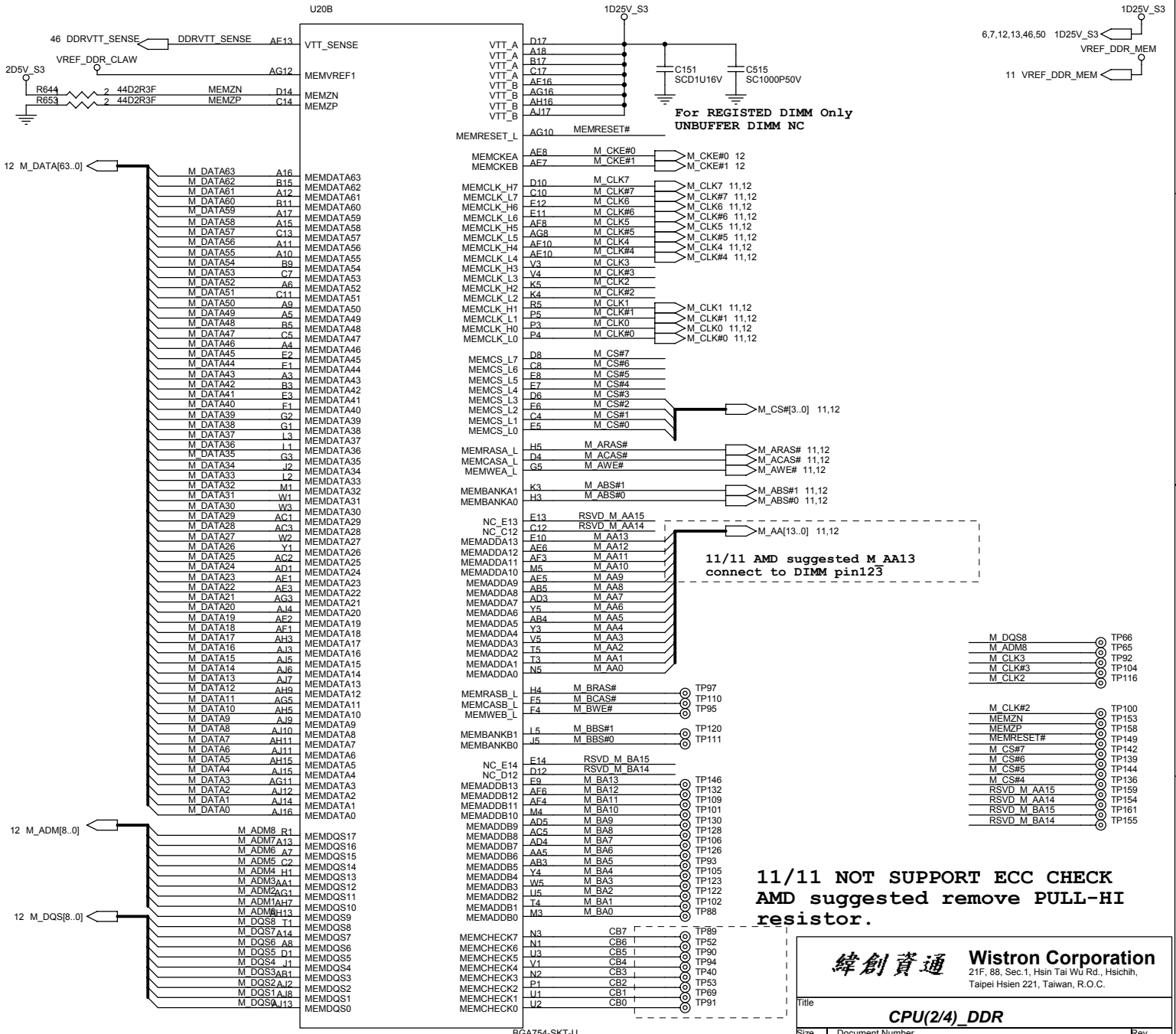
VREF_DDR_MEM



NOTE: Remove to bypass op-amp

VREF_DDR_CLAW





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Title: ***CPU(2/4)_DDR***

Size	Document Number	Rev
A3	**Gannet**	-1

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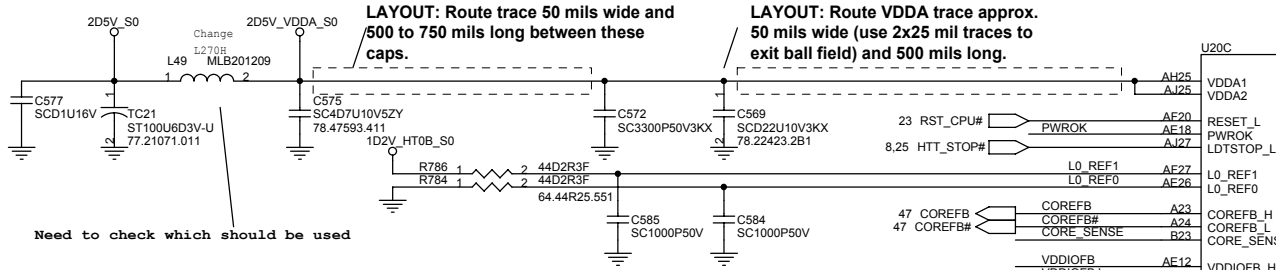
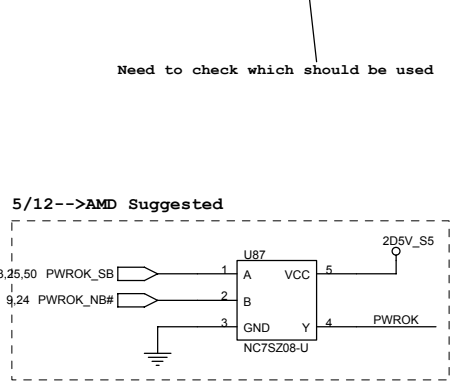
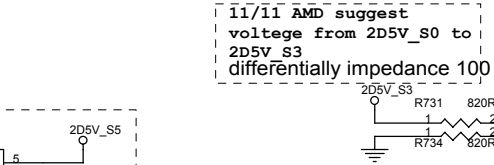
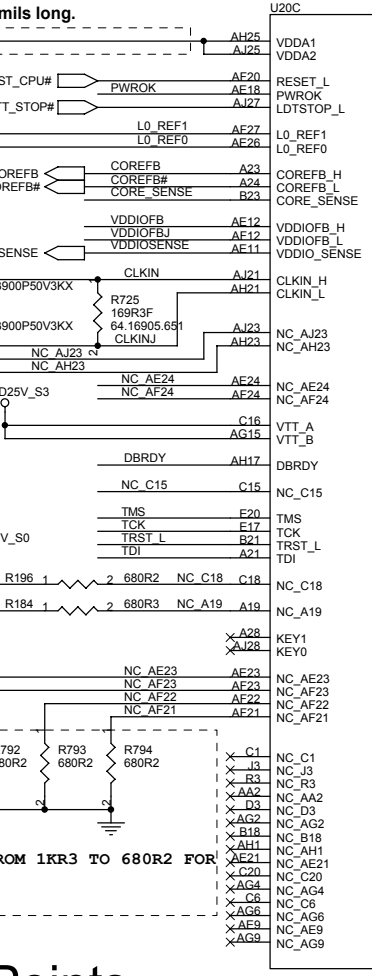
Clawhammer Control and Debug

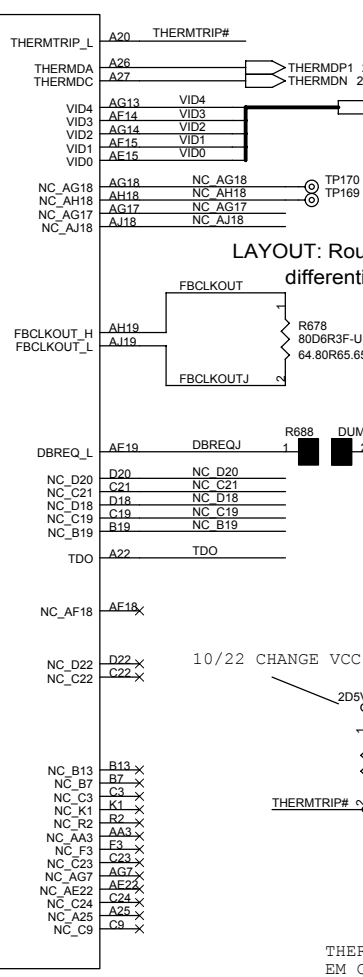
2D5V_VDDA_S0





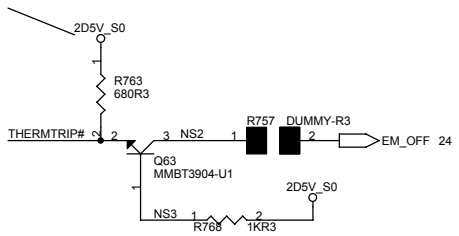






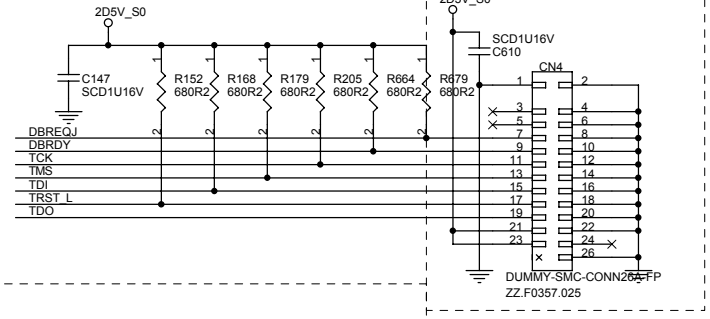
LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

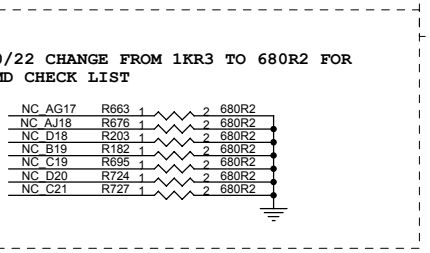
10/22 CHANGE VCC FROM 2D5V_S3 TO 2D5V_S0



THERMTRIPJ Level shift to VT8235
EM_OFF PIN near VT8235

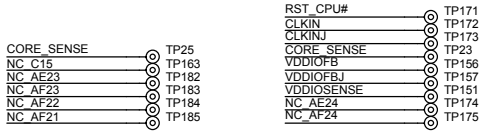
HDT Connectors

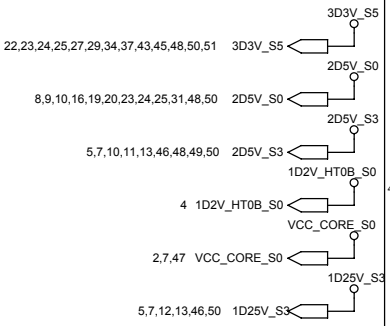




Validation Test Points

LAYOUT: Place close to the CPU.





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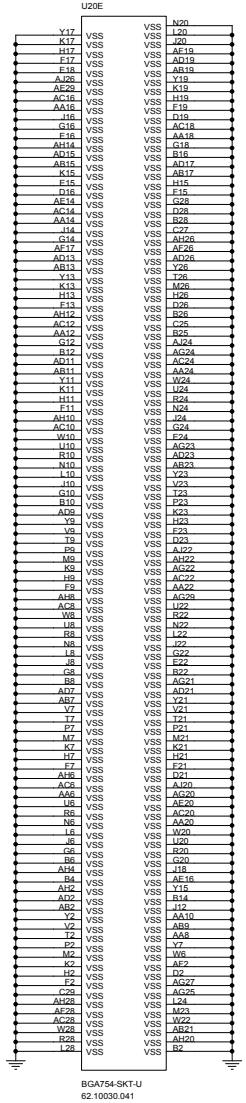
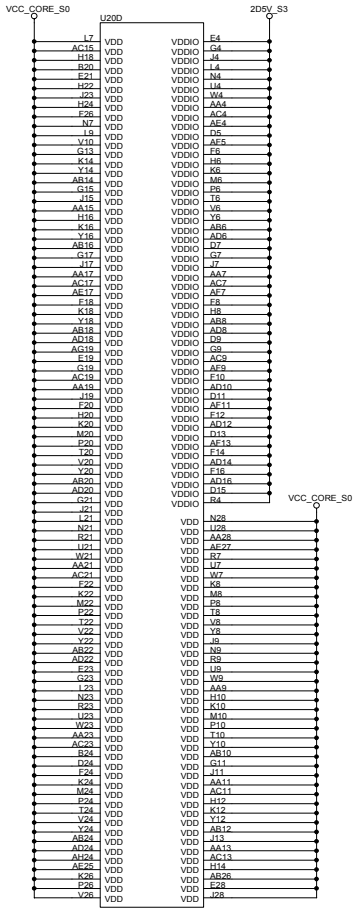
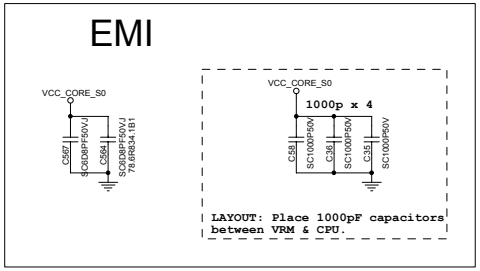
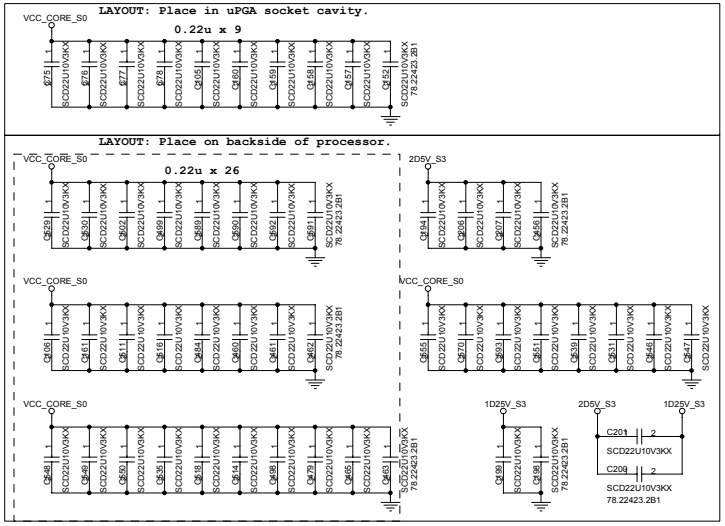
Title	***CPU(3/4)_Control & Debug***	
Size A3	Document Number **Gannet**	Rev -1
Date: Thursday, December 04, 2003	Sheet 6 of 51	

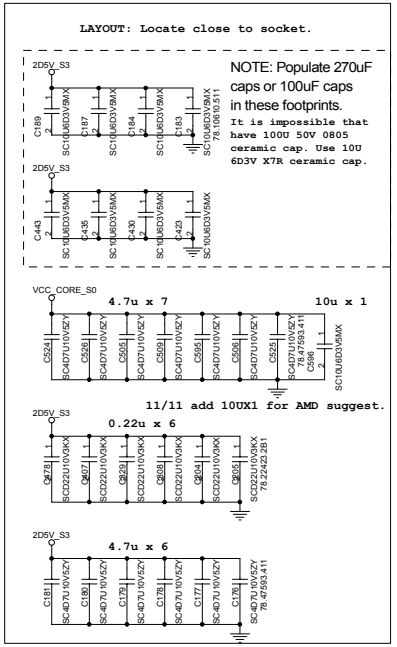
Clawhammer Power and Ground Connections

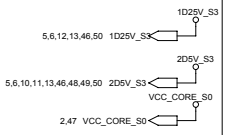




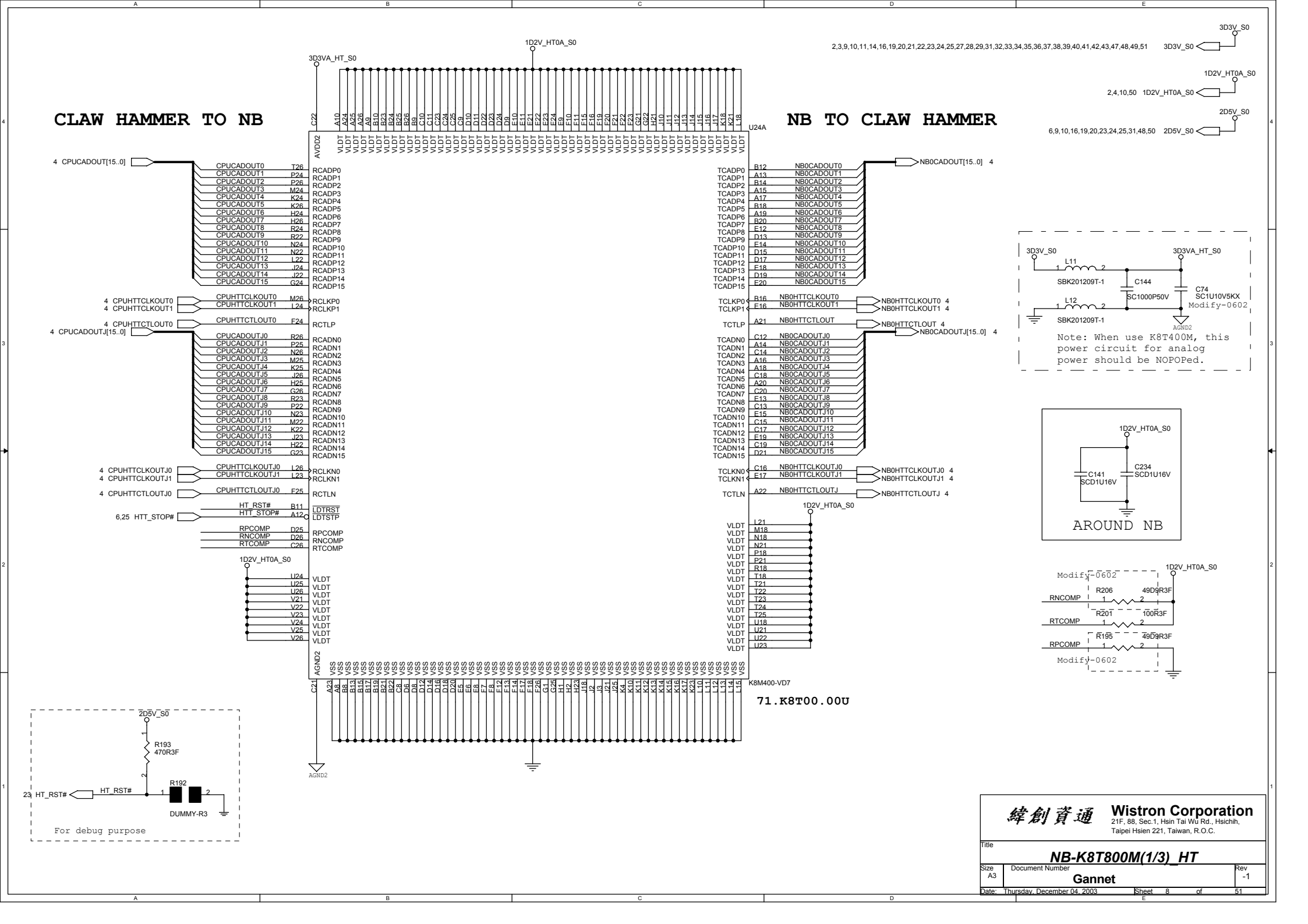


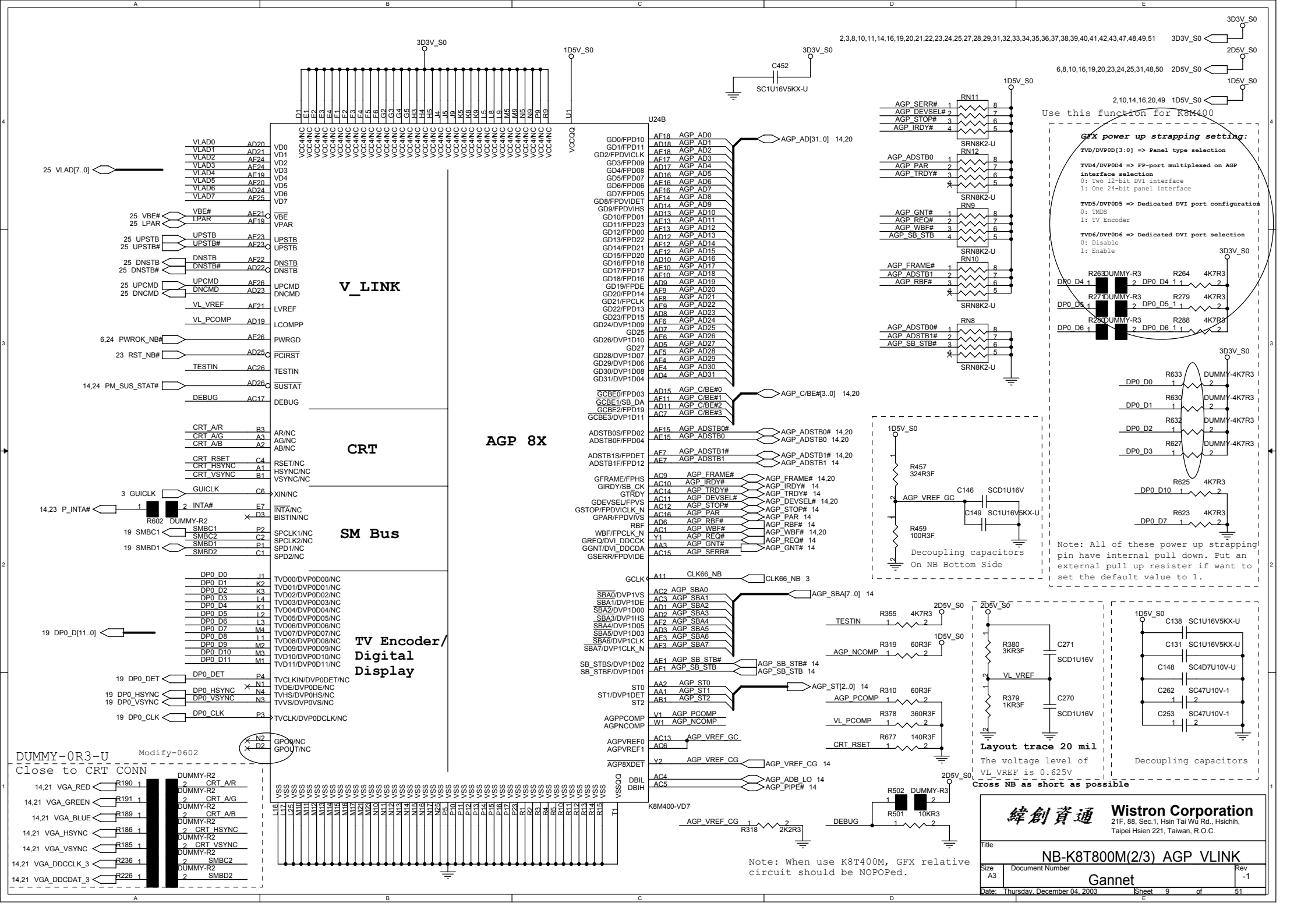






緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU(4/4)_Power***
Size: A2	Document Number: **Gannet**
Rev: -1	
Date: Thursday, December 04, 2003	Sheet 7 of 51


CLAW HAMMER TO NB
NB TO CLAW HAMMER
U24A
K8M400-VD7
71.K8T00.00U
AROUND NB
Note: When use K8T400M, this power circuit for analog power should be NOPOPed.
For debug purpose
Modify-0602
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
NB-K8T800M(1/3)_HT
Gannet
Size A3
Rev -1
Date: Thursday, December 04, 2003
Sheet 8 of 51



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: NB-K8T800M(2/3) AGP VLINK	
Size: A3	Document Number: Gannet	Rev: -1
Date: Thursday, December 04, 2003	Sheet 9 of 51	

Layout trace 20 mil

U24C

K8M400-VD7

Layout trace 20 mil

Note: When use K8T400M, these power circuit for GFX analog power should be NOPOPed.

NEAR N/B ON BOT SIDE

Power for NB Core and VLINK interface

LDO

VDD=1.5V for K8M400

VDD=2.5V for K8T400M(Default)

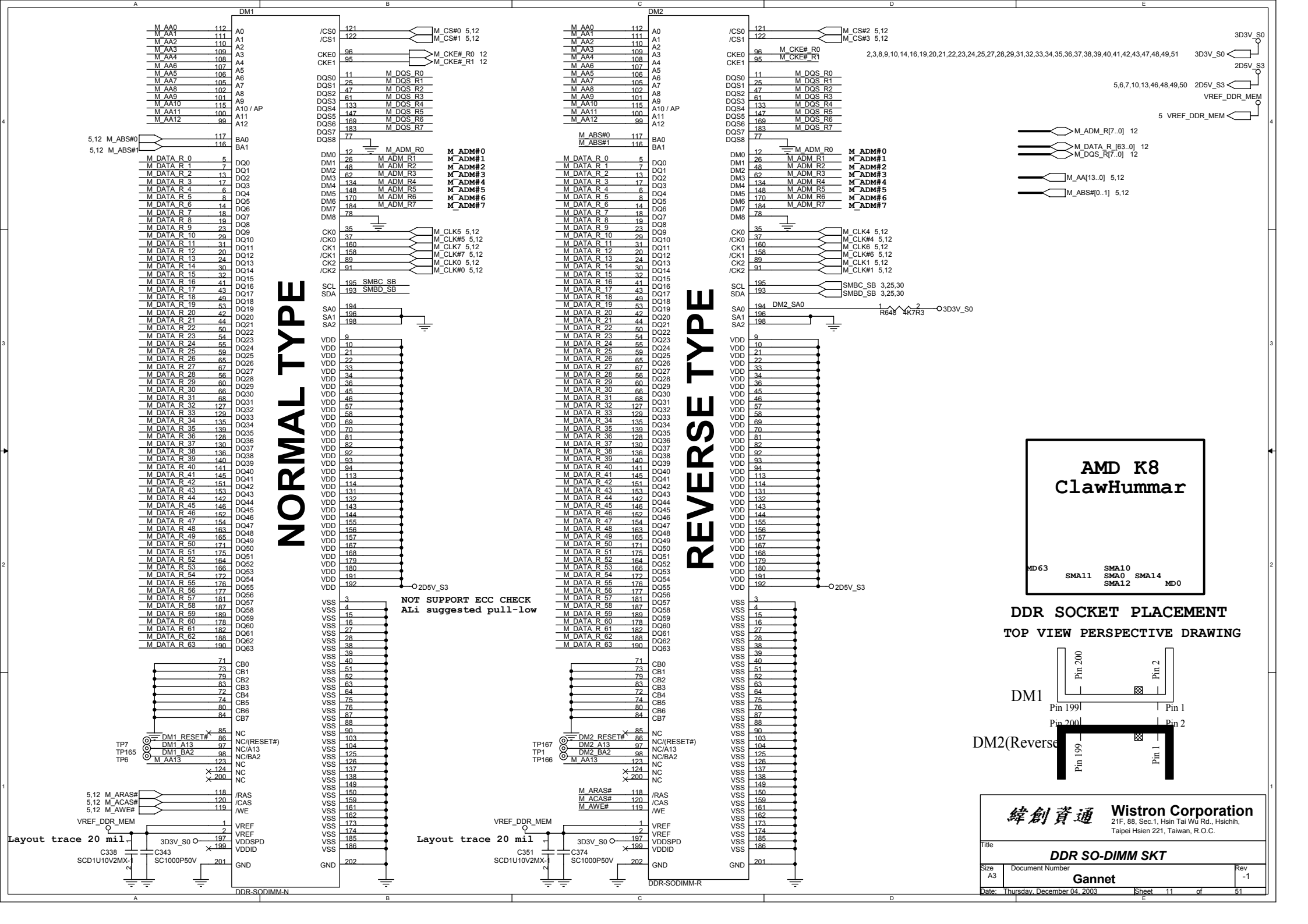
DUMMY

Layout trace 20 mil

VSUSNB=1.5V for K8M400
When R1=100, R2=500

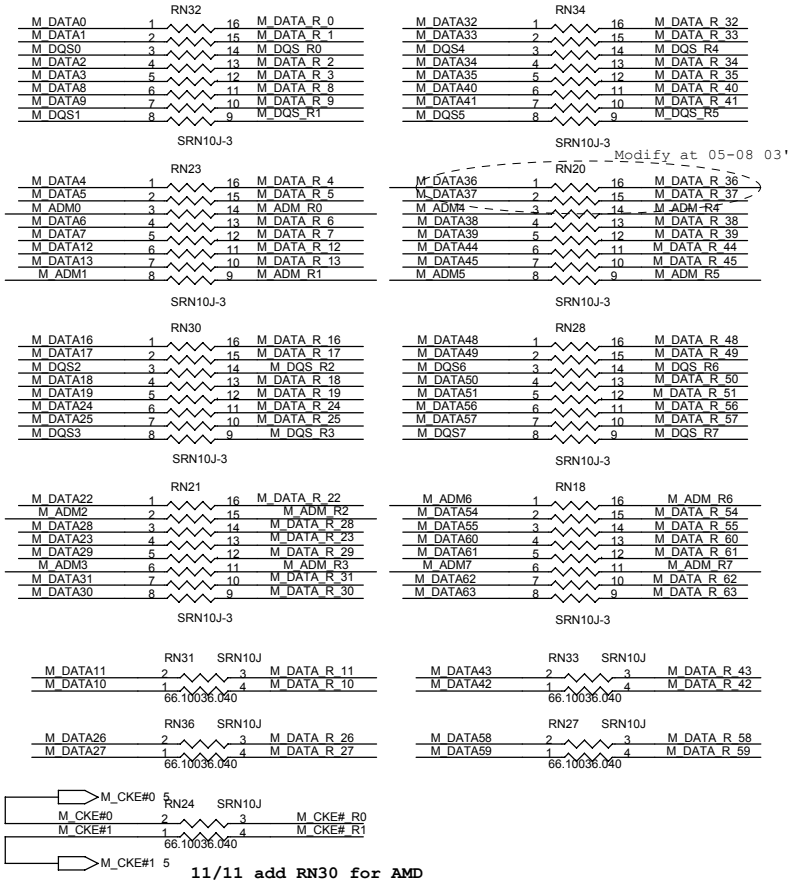
VSUSNB=2.5V for K8T400M
When R1=102, R2=100
(Default)

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**NB-K8T800M(3/3)_POWER**	
Size A3	Document Number **Gannet**	Rev -1
Date: Thursday, December 04, 2003	Sheet 10 of 51	

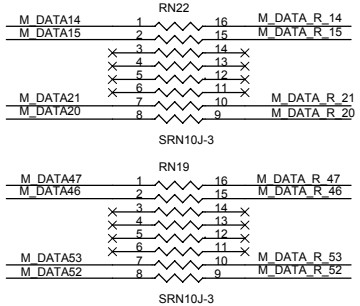

DM1
NORMAL TYPE
DDR-SODIMM-N
DM2
REVERSE TYPE
DDR-SODIMM-R
NOT SUPPORT ECC CHECK
ALi suggested pull-low
Layout trace 20 mil
Layout trace 20 mil
AMD K8
ClawHummar
DDR SOCKET PLACEMENT
TOP VIEW PERSPECTIVE DRAWING
DM1
DM2(Reverse)
Pin 200
Pin 2
Pin 199
Pin 1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR SO-DIMM SKT
Gannet
Thursday, December 04, 2003

SERIES DAMPING

PLACE RNs CLOSE TO FIRST DM (DM2), < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS



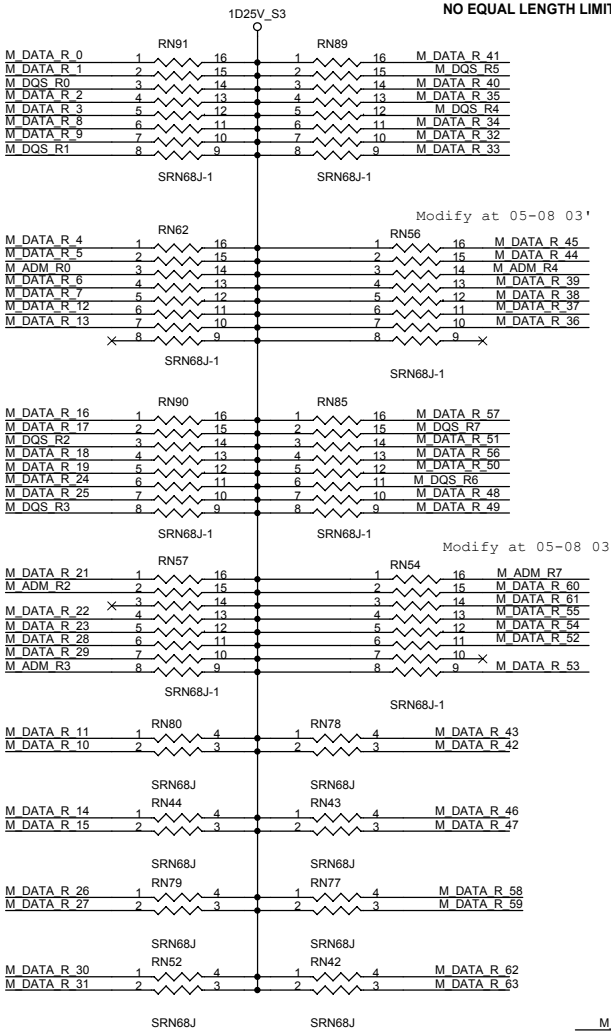
11/11 add RN30 for AMD suggest.



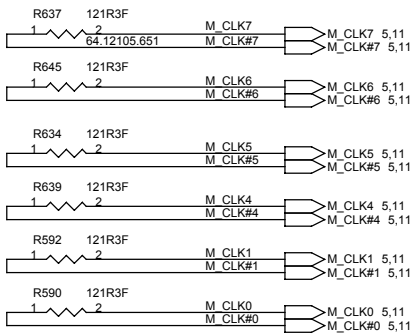
11 M_ADM_R[7..0]
5 M_ADM[8..0]

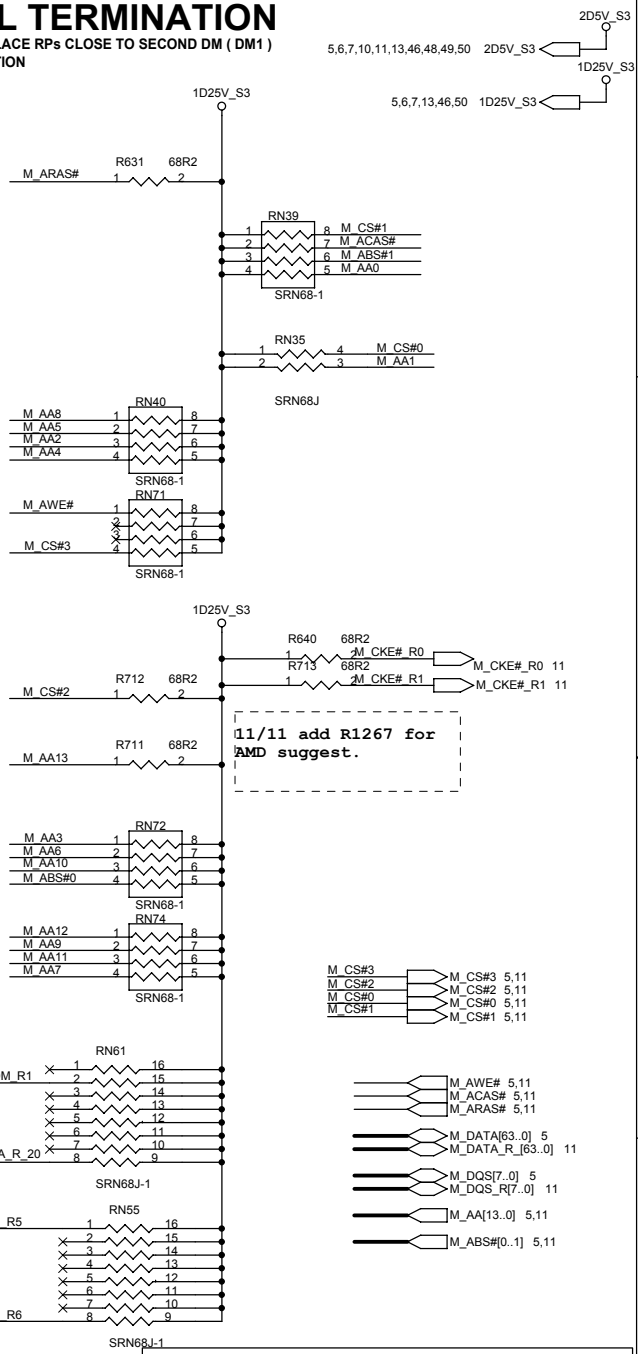
PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM1)
NO EQUAL LENGTH LIMITATION



PLACE BETWEEN DM1, DM2
CLOSE TO FIRST DM (DM 2) < 0.2", TO SECOND DM (DM1) < 1.1"
EQUAL LENGTH LIMITATION WITH SCK/SCK#





緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR DAMPING & TERMINATION***

Size: A3 | Document Number: **Gannet** | Rev: -1

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	100u	10u	4.7u	0.22u	0.1u	1000p	100p
1D25V_S3 TO GND	2	2	10	10	34	4	4

	220u	0.22u	0.1u
1D25V_S3 TO 2D5V_S3	1	10	34

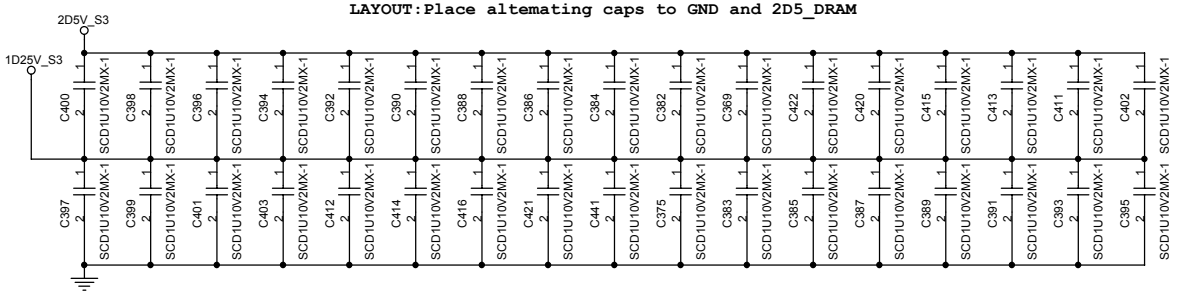
2D5V_S3

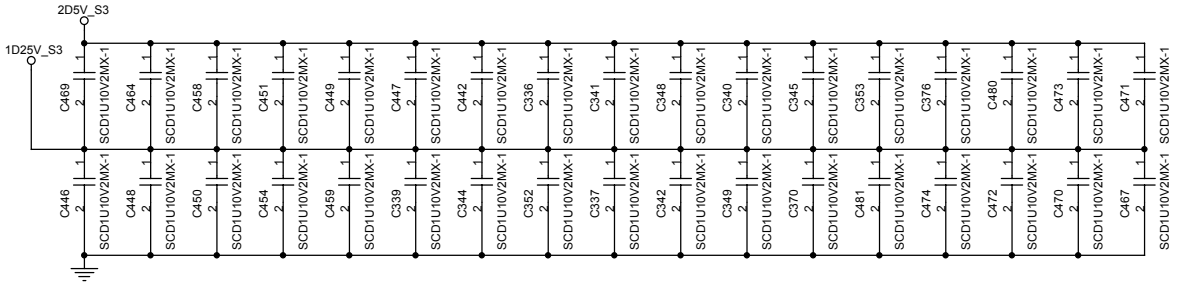
5,6,7,10,11,46,48,49,50 2D5V_S3

1D25V_S3

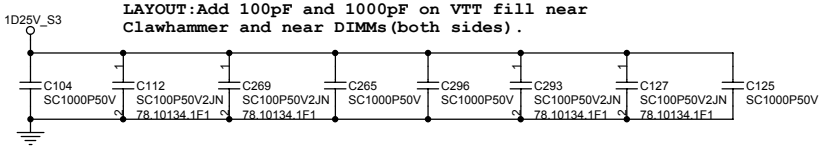
5,6,7,12,46,50 1D25V_S3

LAYOUT:Place altemating caps to GND and 2D5_DRAM

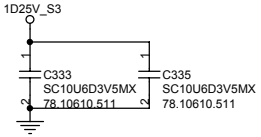




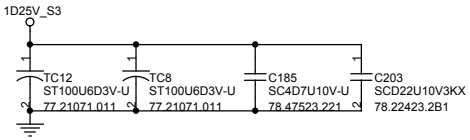
LAYOUT:Add 100pF and 1000pF on VTT fill near Clawhammer and near DIMMs(both sides).

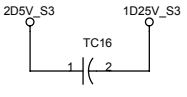


LAYOUT:Place one 10uF capacitor on each end of the VTT island.

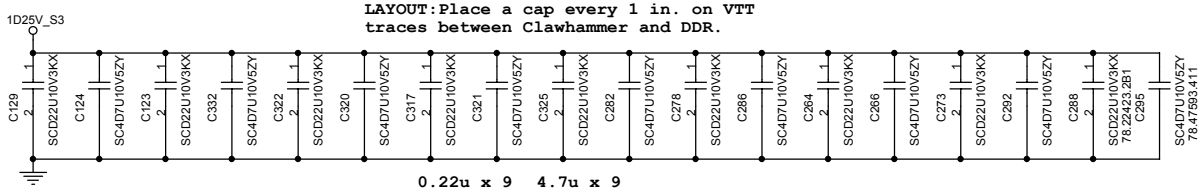


LAYOUT:Locate close to Clawhammer socket.



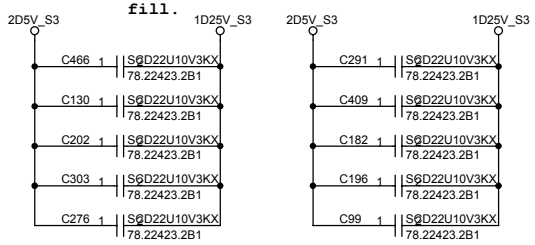


LAYOUT:Place a cap every 1 in. on VTT traces between Clawhammer and DDR.



0.22u x 9 4.7u x 9

LAYOUT:Place on backside, evenly spaced around VTT fill.



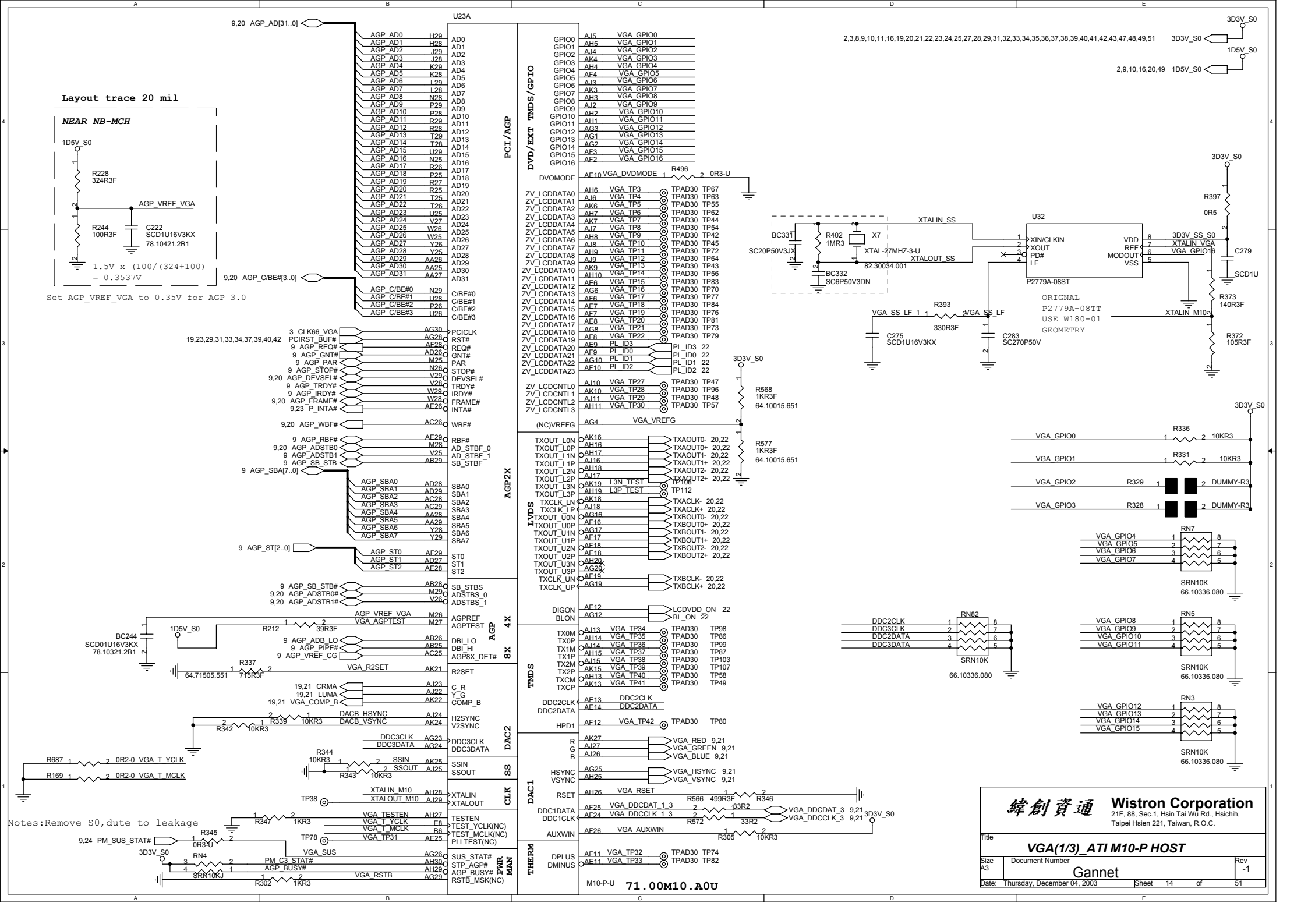
0.22u x 10

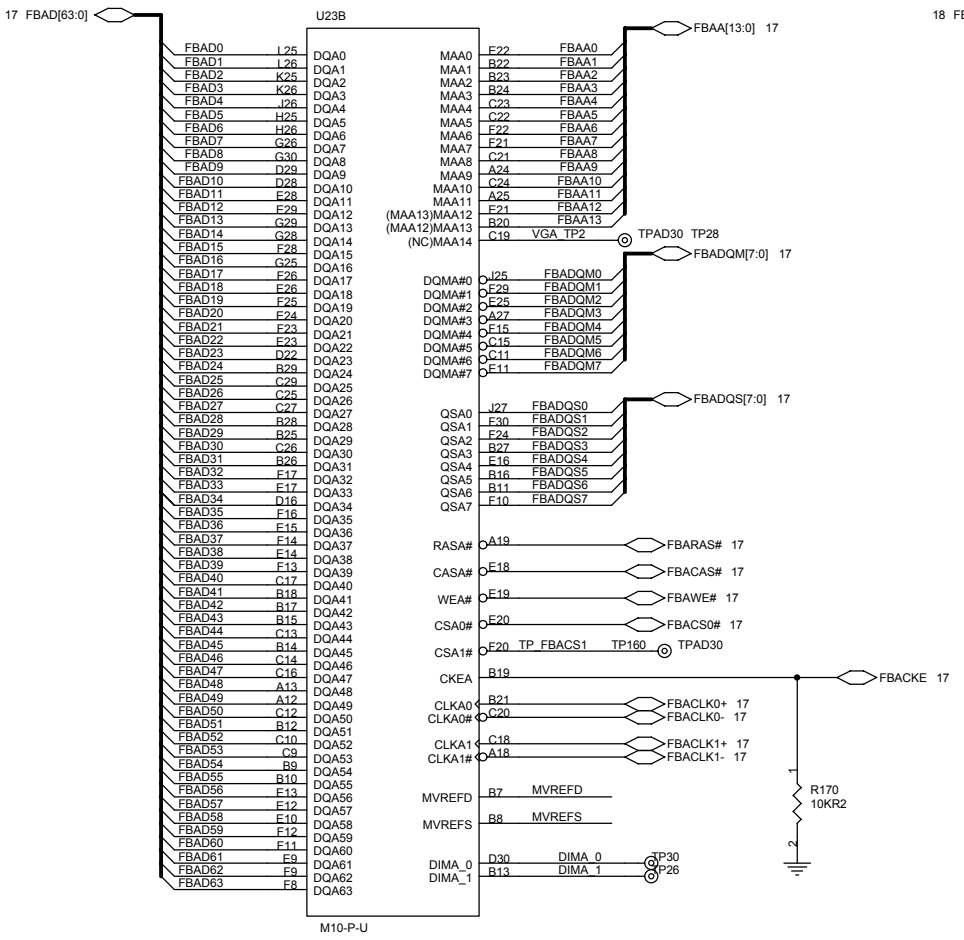
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

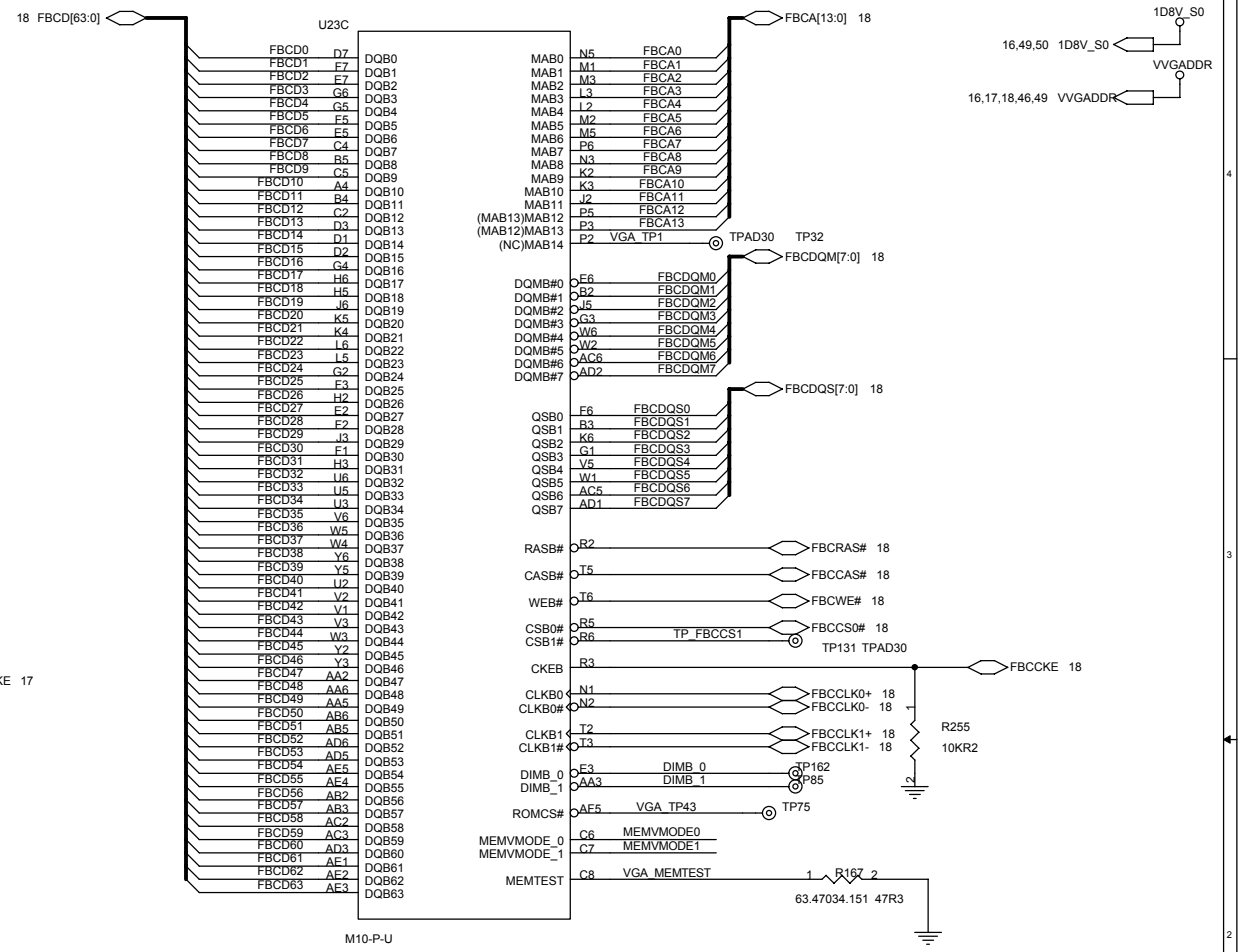
Title: ***DDR DECOUPLING***

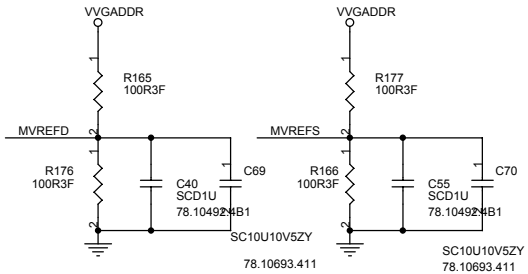
Size: A3 | Document Number: **Gannet** | Rev: -1

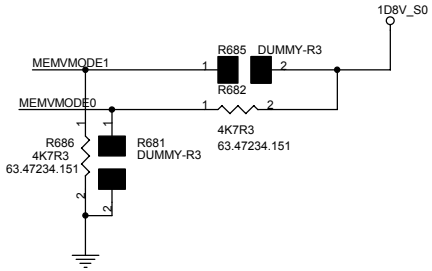
Date: Thursday, December 04, 2003 | Sheet 13 of 51


U23A
Layout trace 20 mil
NEAR NB-MCH
1D5V_S0
R228 324R3F
AGP_VREF_VGA
R244 100R3F
C222 SCD1U16V3KX 78.10421.2B1
1.5V x (100/(324+100)) = 0.3537V
Set AGP_VREF_VGA to 0.35V for AGP 3.0
PCI/AGP
AGP2X
AGP 4X
AGP 8X
DAC2
SS
CLK
PWR MAN
DVD/EXT TMDS/GPIO
LVDS
TMDS
DAC1
THERM
Notes:Remove S0,dute to leakage
M10-P-U
71.00M10.A0U
XTALIN_SS
XTALOUT_SS
XTAL-27MHZ-3-U
82.30034.001
U32
XIN/CLKIN
XOUT
PD#
LF
VDD
REF
MODOUT
VSS
P2779A-08ST
ORIGNAL
P2779A-08TT
USE W180-01
GEOMETRY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VGA(1/3)_ATI M10-P HOST
Gannet
Date: Thursday, December 04, 2003
Sheet 14 of 51









	MEMMODE0	MEMMODE1
2D5V VDDR1	1	0
1D8V VDDR1(ELPIDA)	0	1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
VGA(2/3) ATI M10-P MEM

Size	Document Number	Rev
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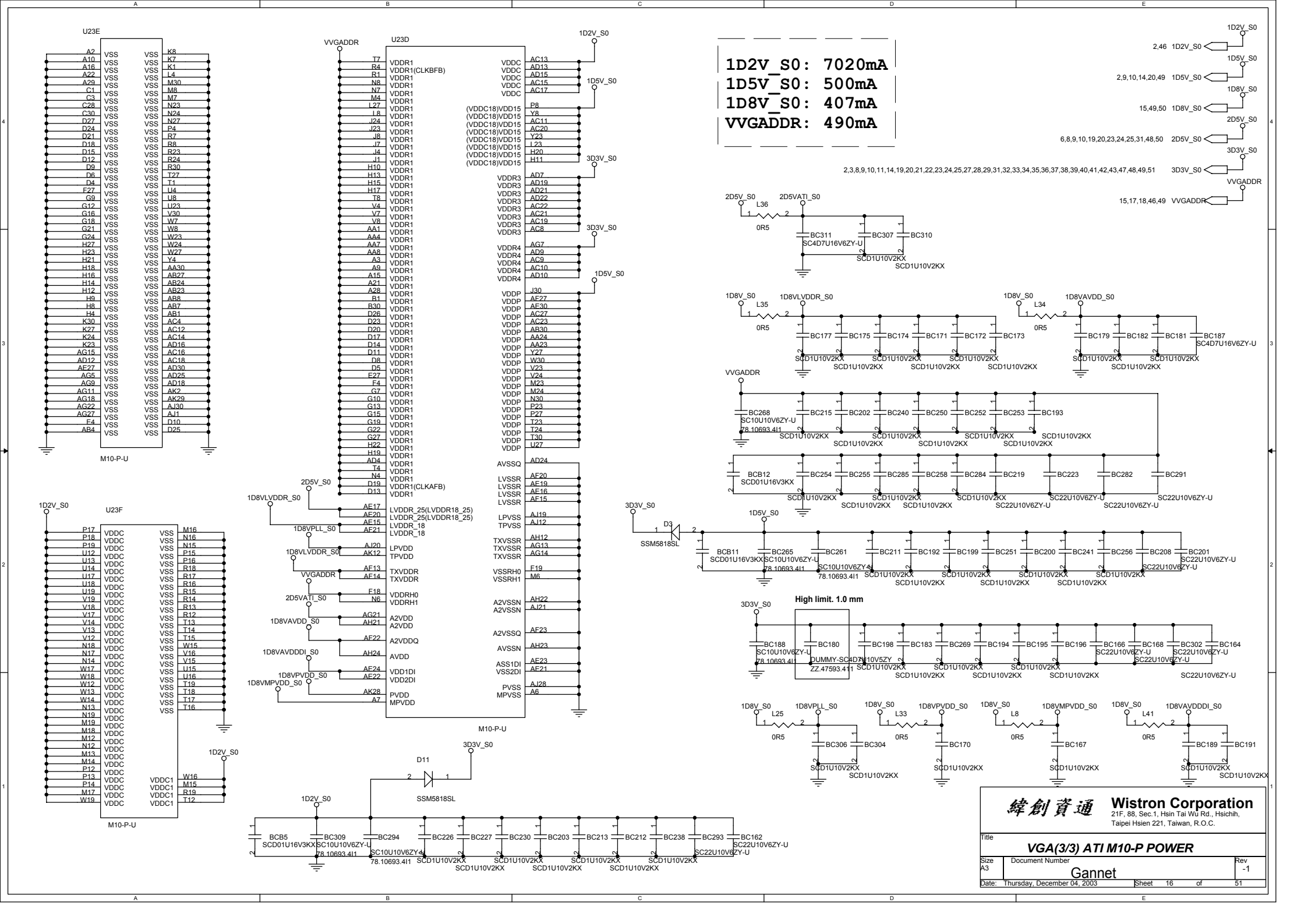
Date: Thursday, December 04, 2003 Sheet 15 of 51


1D2V_S0: 7020mA
1D5V_S0: 500mA
1D8V_S0: 407mA
VVGADDR: 490mA
U23E
M10-P-U
U23D
M10-P-U
U23F
M10-P-U
High limit. 1.0 mm
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VGA(3/3) ATI M10-P POWER
Size A3
Document Number
Gannet
Rev -1
Date: Thursday, December 04, 2003
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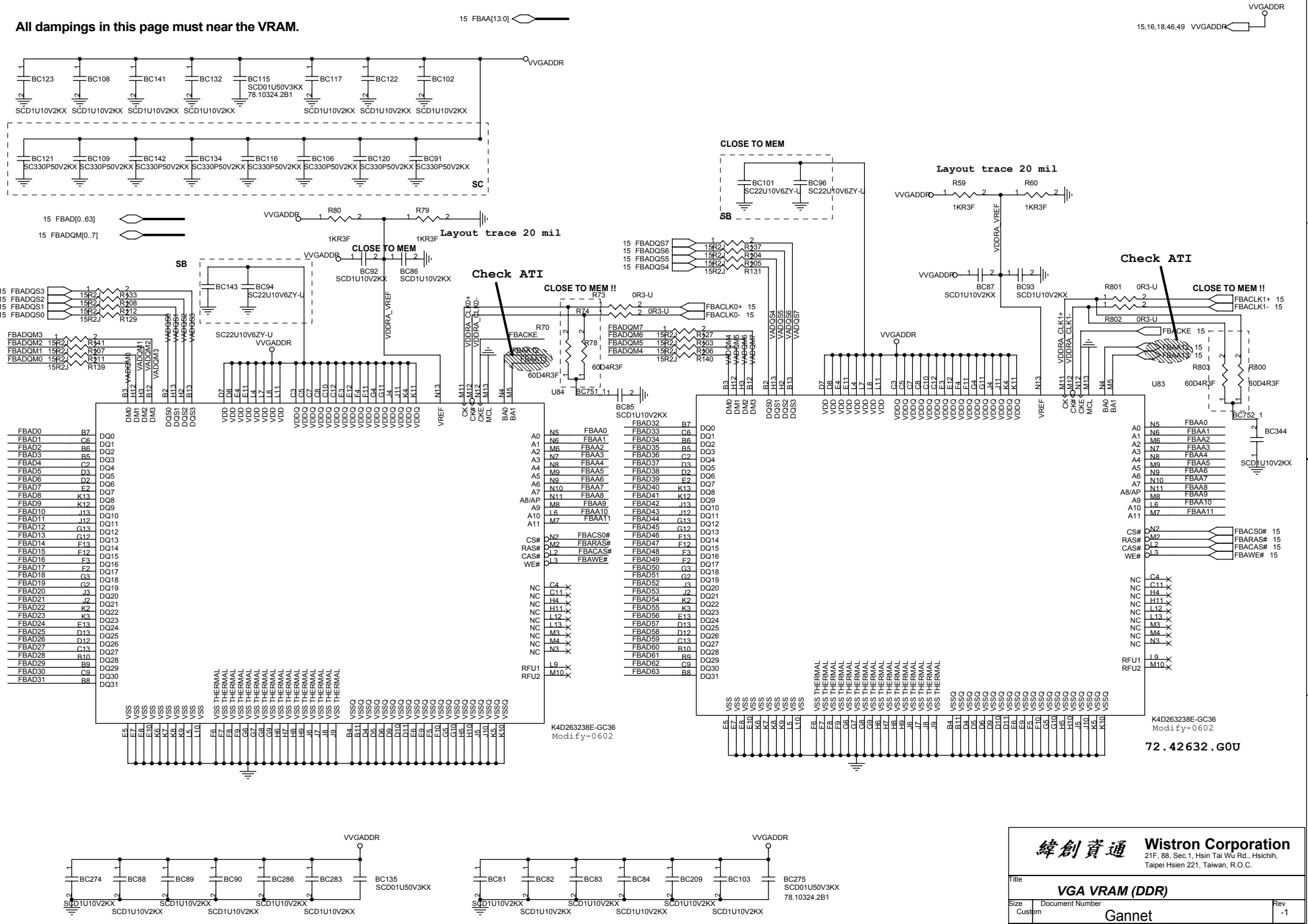
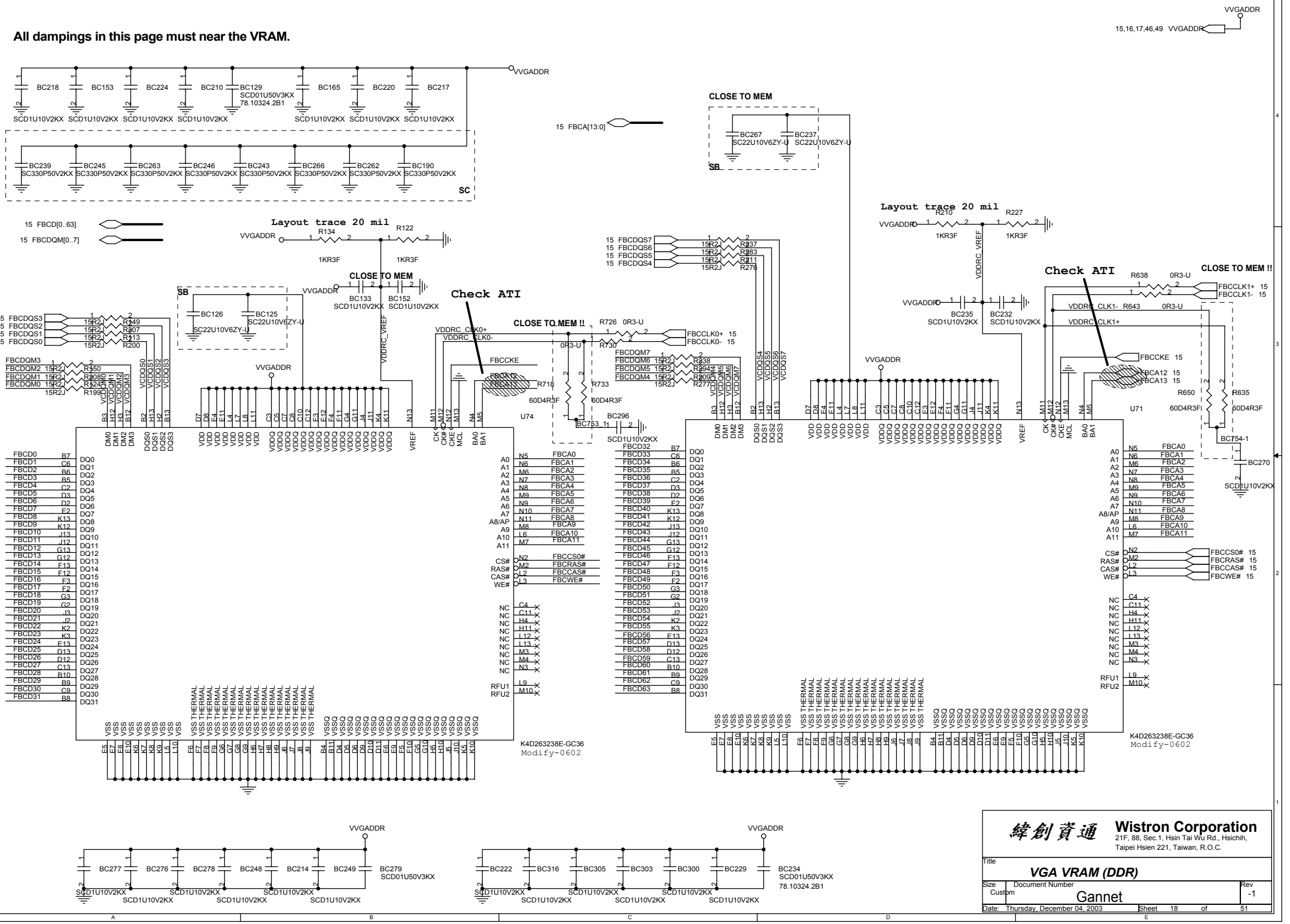
All dampings in this page must near the VRAM.

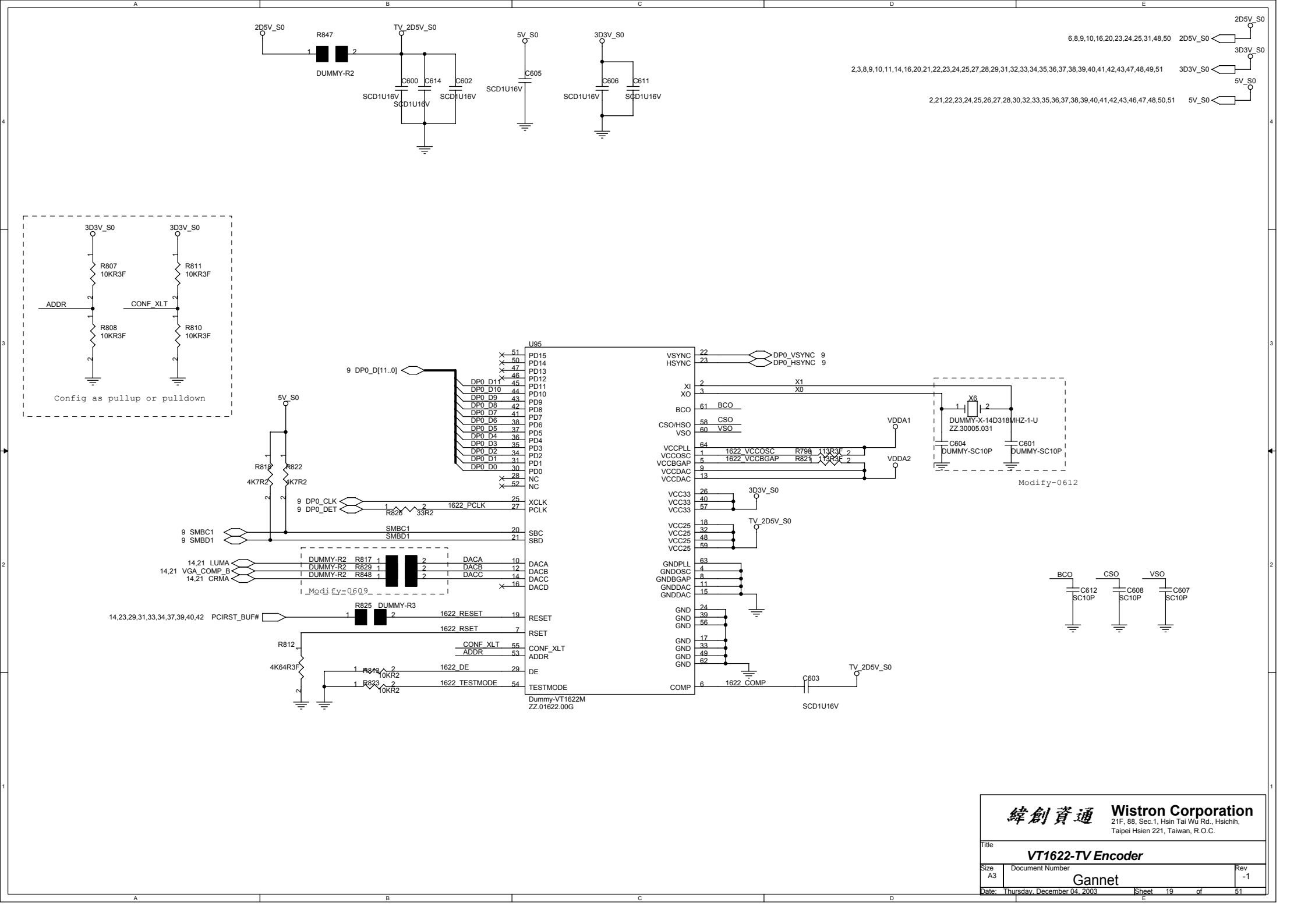


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***VGA VRAM (DDR)***		
Size: Custom	Document Number: Gannet		Rev: -1
Date: Thursday, December 04, 2003	Sheet 17 of 51		

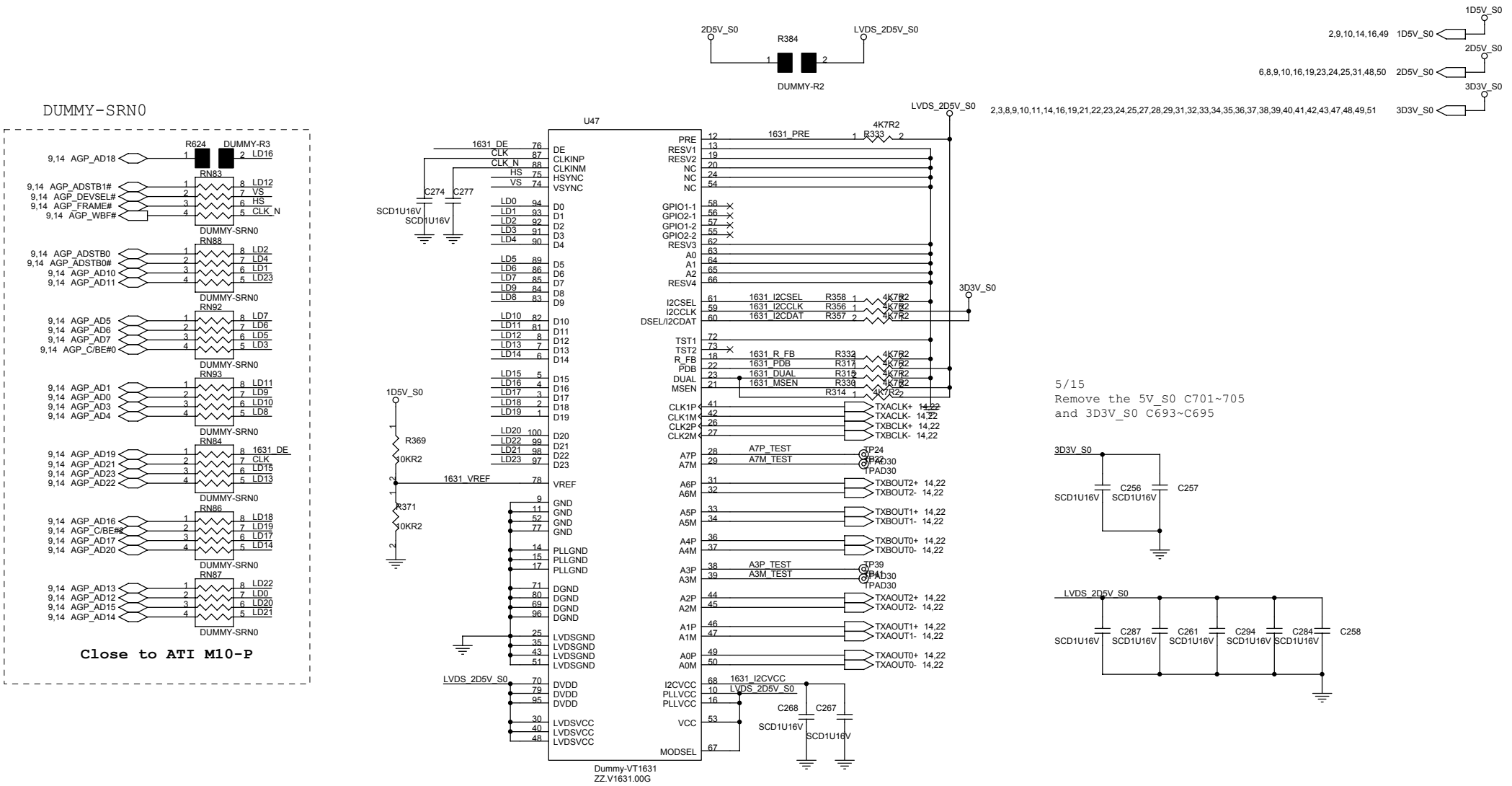
All dampings in this page must near the VRAM.



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***VGA VRAM (DDR)***		
Size: Custom	Document Number: Gannet		Rev: -1
Date: Thursday, December 04, 2003	Sheet 18 of 51		



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VT1622-TV Encoder***	
Size A3	Document Number Gannet	Rev -1
Date: Thursday, December 04, 2003	Sheet 19 of 51	



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VT1631-LVDS Transmitter***

Size	Document Number	Rev
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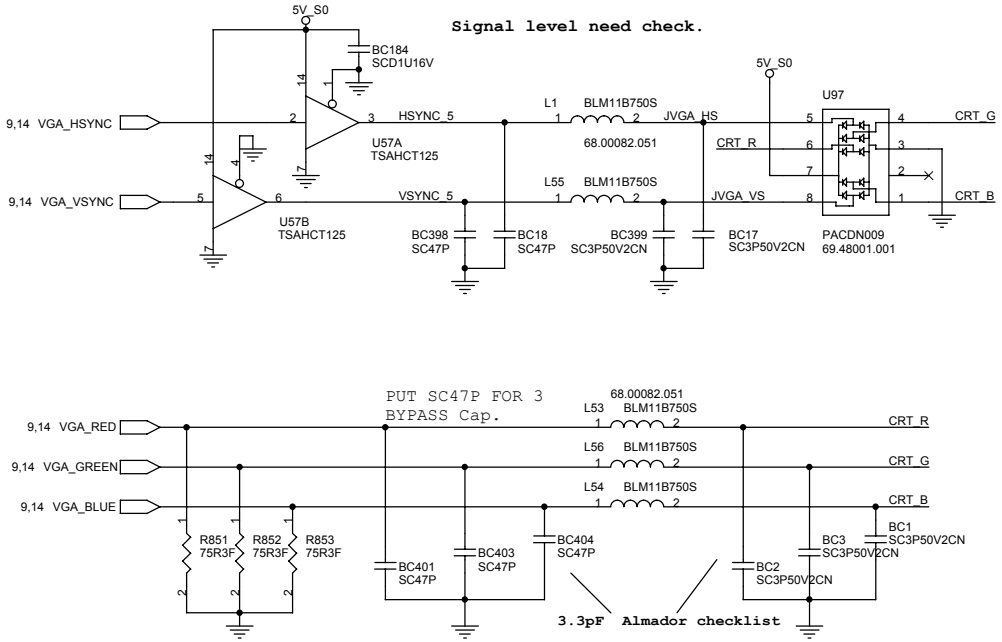
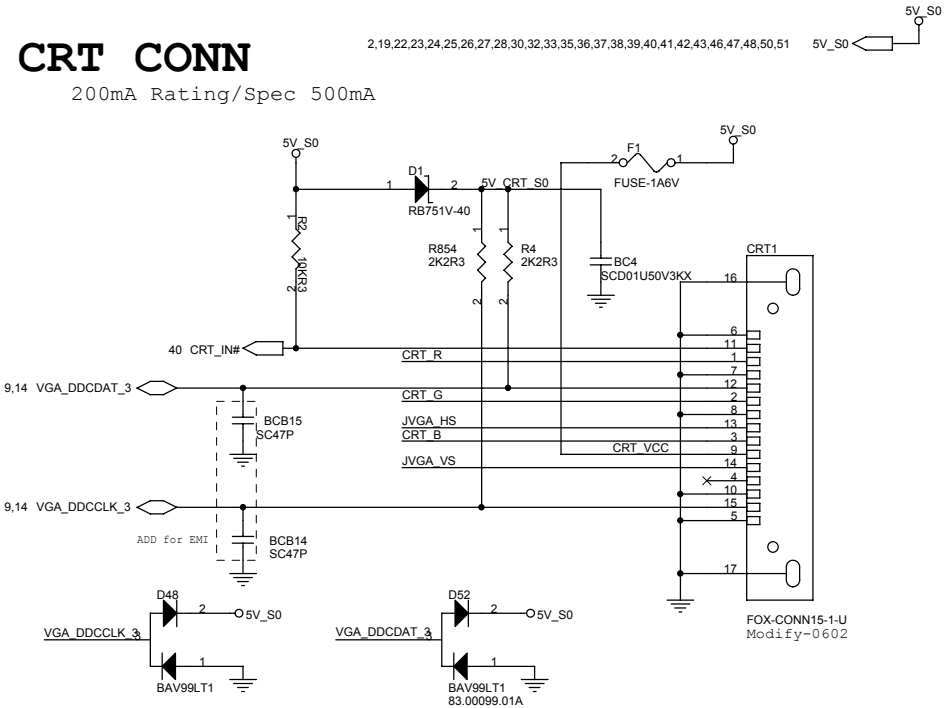
CRT



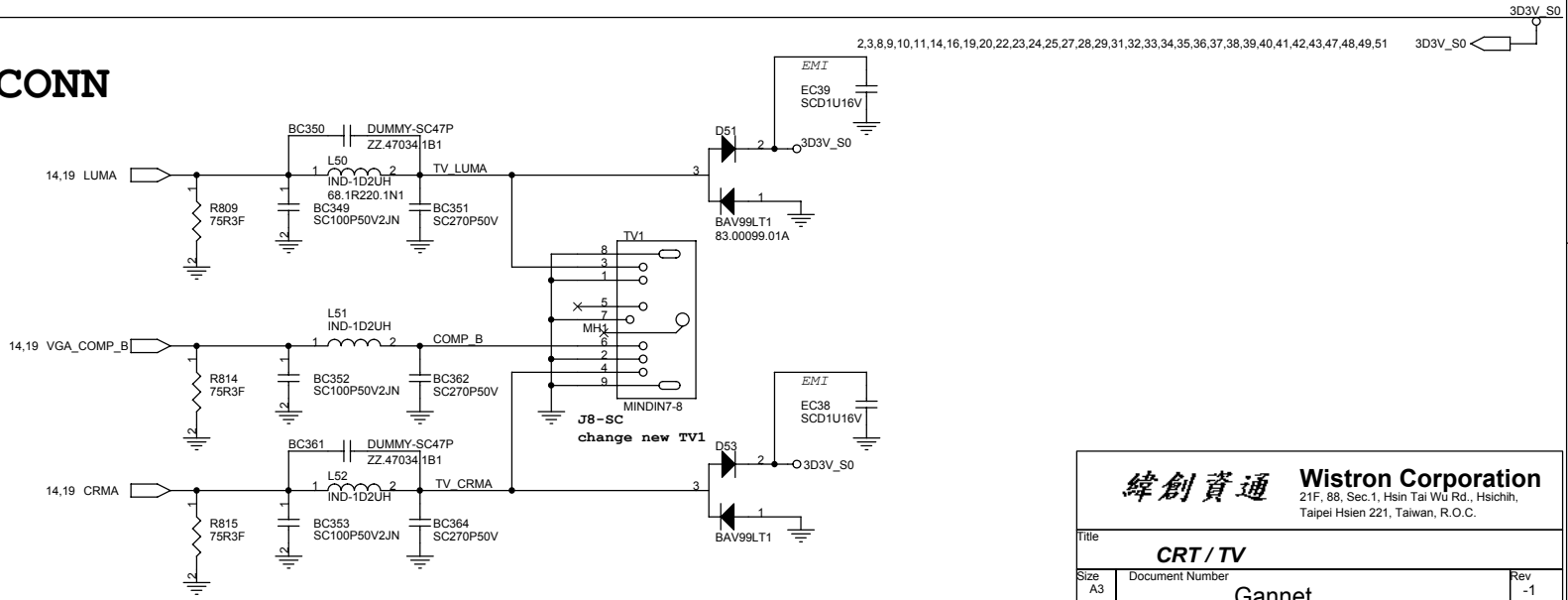
CRT CONN

200mA Rating/Spec 500mA



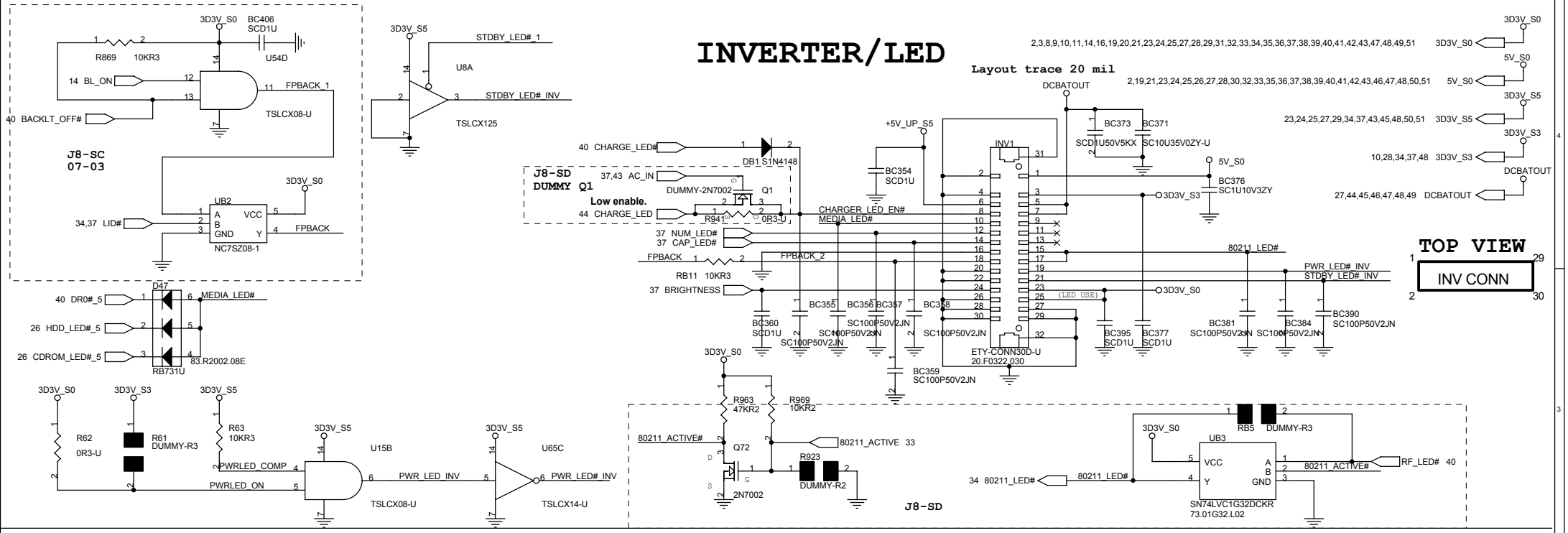
Layout Note:
Must be a ground return path between this ground and the ground on the VGA connector. 37.4_1% resistors must be placed after RGB pi filter ,near CRT connector.

TV CONN

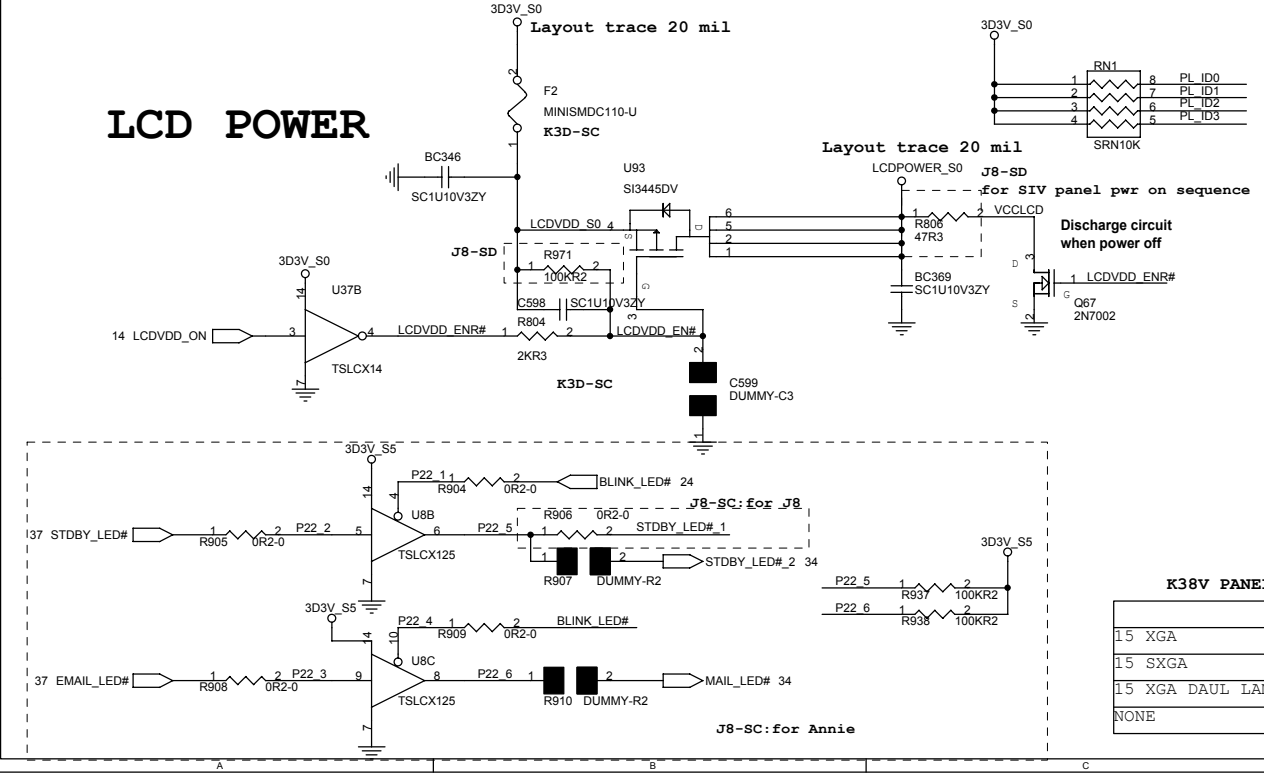


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT / TV***	
Size A3	Document Number Gannet	Rev -1
Date: Thursday, December 04, 2003	Sheet 21 of 51	

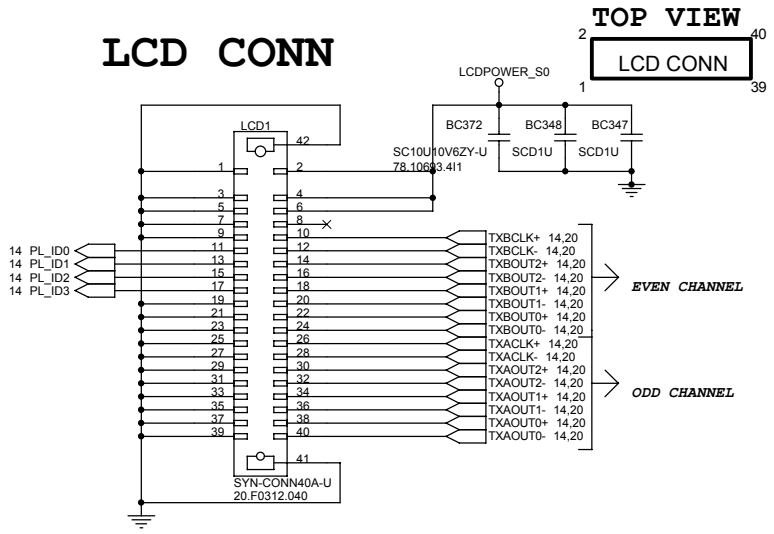
INVERTER/LED



LCD POWER



LCD CONN



K38V PANEL ID SETTING

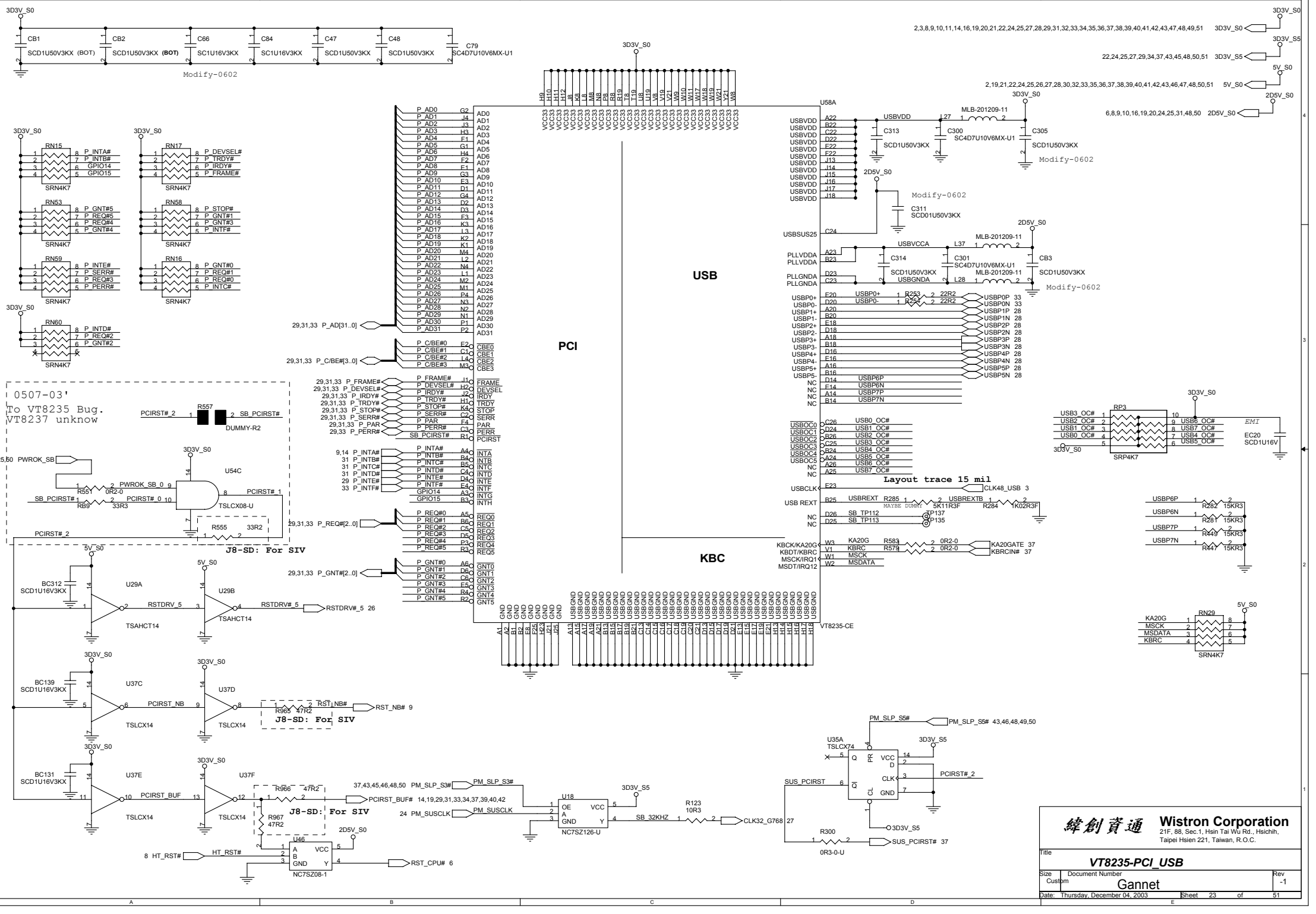
	PL_ID2	PL_ID1	PL_ID0
15 XGA	0	0	1
15 SXGA	0	1	0
15 XGA DAUL LAMP	0	1	1
NONE	1	1	1

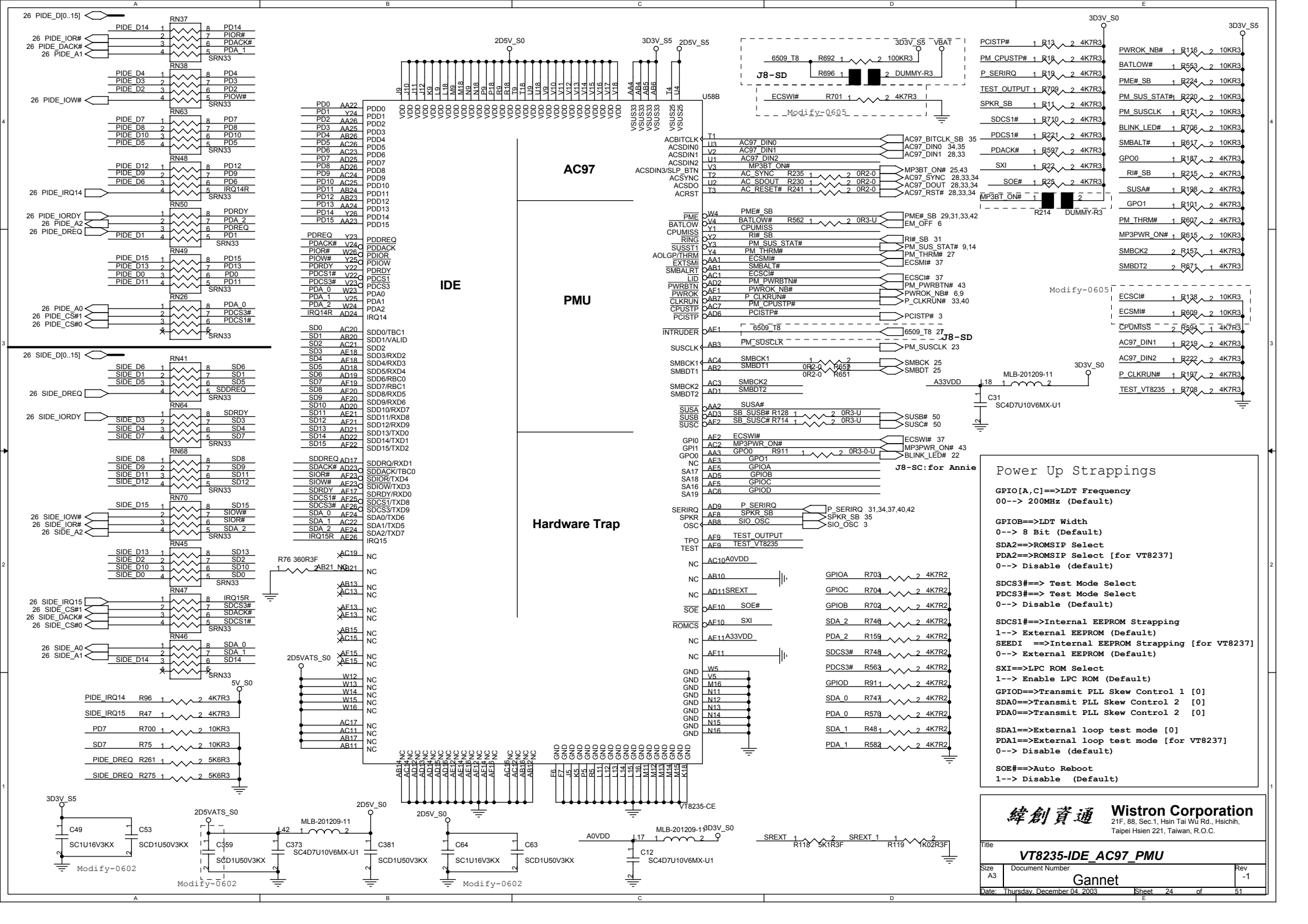
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

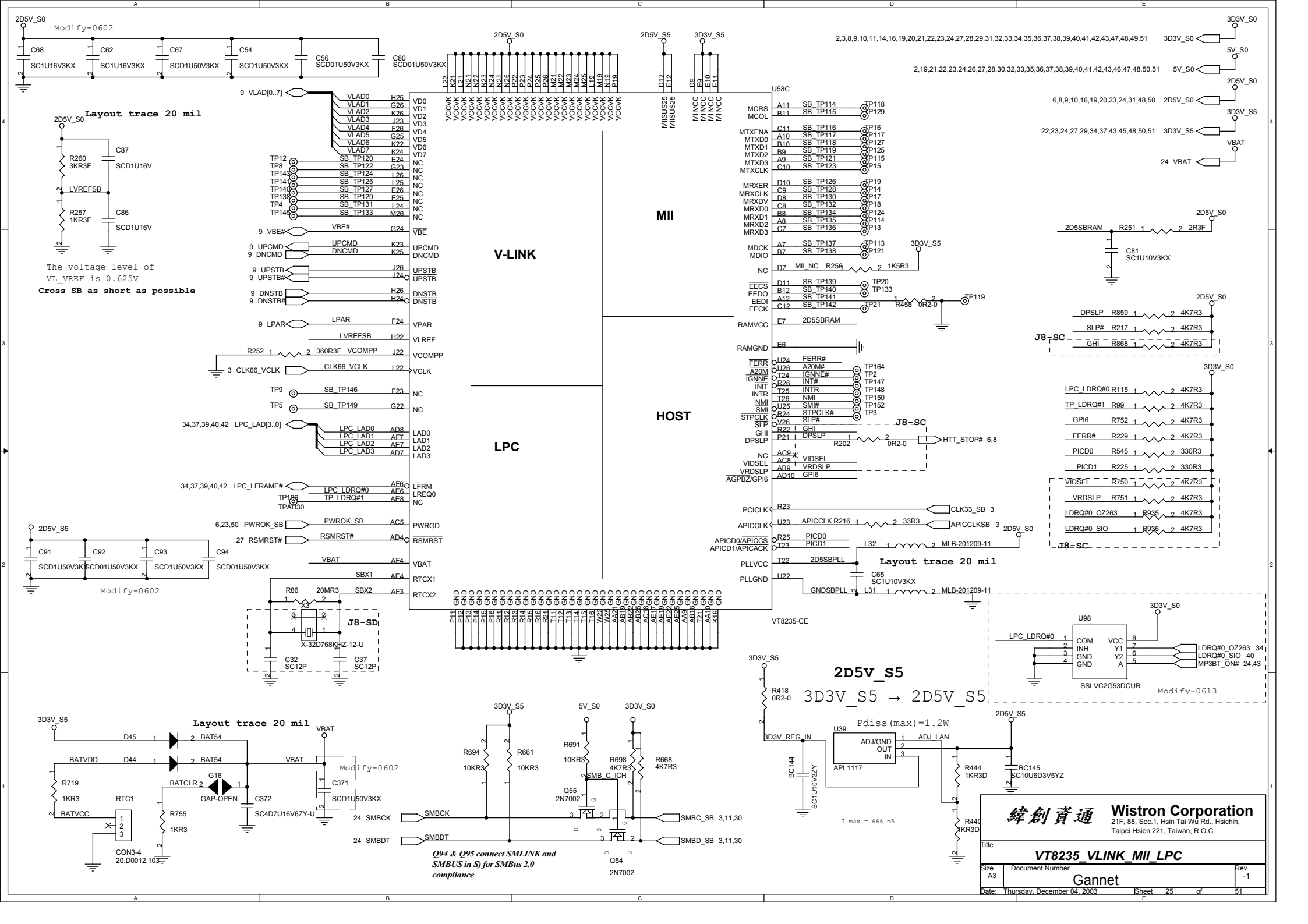
Title: **INV / LCD**

Size: A3 | Document Number: Gannet | Rev: -1

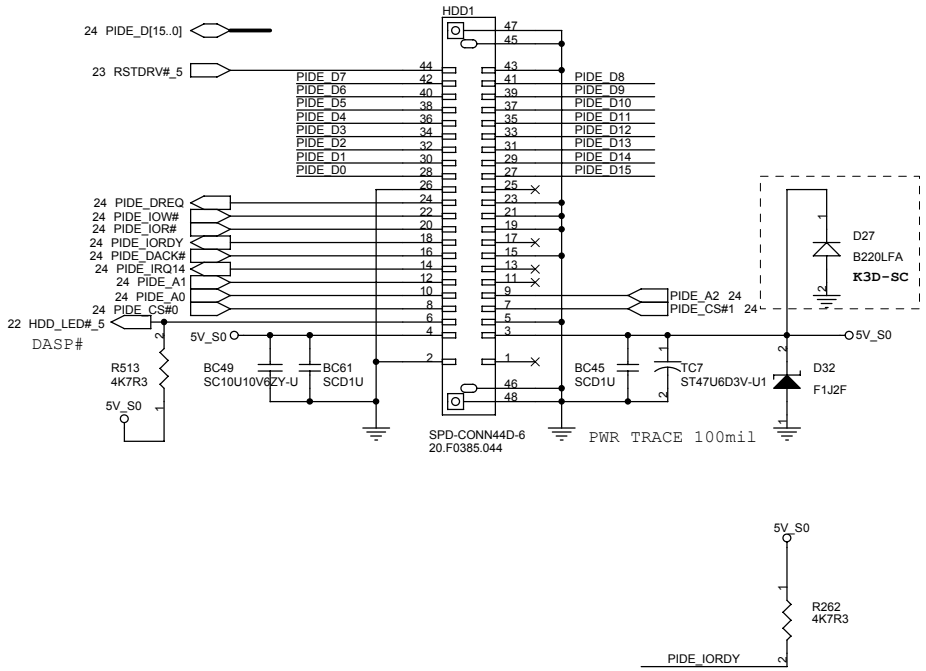
Date: Thursday, December 04, 2003 | Sheet 22 of 51


3D3V_S0
CB1
SCD1U50V3KX (BOT)
CB2
SCD1U50V3KX (BOT)
C66
SC1U16V3KX
C84
SC1U16V3KX
C47
SCD1U50V3KX
C48
SCD1U50V3KX
C79
SC4D7U10V6MX-U1
Modify-0602
2,3,8,9,10,11,14,16,19,20,21,22,24,25,27,28,29,31,32,33,34,35,36,37,38,39,40,41,42,43,47,48,49,51
3D3V_S5
22,24,25,27,29,34,37,43,45,48,50,51
5V_S0
2,19,21,22,24,25,26,27,28,30,32,33,35,36,37,38,39,40,41,42,43,46,47,48,50,51
2D5V_S0
6,8,9,10,16,19,20,24,25,31,48,50
RN15
P_INTA#
P_INTB#
GIO14
GIO15
SRN4K7
RN17
P_DEVSEL#
P_TRDY#
P_IRDY#
P_FRAME#
RN53
P_GNT#5
P_REQ#5
P_REQ#4
P_GNT#4
RN58
P_STOP#
P_GNT#1
P_GNT#3
P_INTF#
RN59
P_INTE#
P_SERR#
P_REQ#3
P_PERR#
RN16
P_GNT#0
P_REQ#1
P_REQ#0
P_INTC#
RN60
P_INTD#
P_REQ#2
P_GNT#2
29,31,33 P_AD[31..0]
29,31,33 P_C/BE#[3..0]
29,31,33 P_FRAME#
29,31,33 P_DEVSEL#
29,31,33 P_IRDY#
29,31,33 P_TRDY#
29,31,33 P_STOP#
29,31,33 P_SERR#
29,31,33 P_PAR
29,31,33 P_PERR#
9,14 P_INTA#
31 P_INTB#
31 P_INTC#
31 P_INTD#
29 P_INTE#
33 P_INTF#
GPIO14
GPIO15
29,31,33 P_REQ#[2..0]
29,31,33 P_GNT#[2..0]
PCI
USB
KBC
VT8235-CE
U58A
USBVDD
USBSUS25
PLLVDDA
PLLGNDA
USBVCCA
USBGNDA
USBP0+
USBP0-
USBP1+
USBP1-
USBP2+
USBP2-
USBP3+
USBP3-
USBP4+
USBP4-
USBP5+
USBP5-
USBOC0
USBOC1
USBOC2
USBOC3
USBOC4
USBOC5
USBCLK
USB REXT
KBCK/KA20G
KBDT/KBRC
MSCK/IRQ1
MSDT/IRQ12
C313
SCD1U50V3KX
C300
SC4D7U10V6MX-U1
C305
SCD1U50V3KX
C311
SCD01U50V3KX
C314
C301
SC4D7U10V6MX-U1
CB3
SCD1U50V3KX
MLB-201209-11
L37
L28
R253
R254
22R2
R285
R284
5K11R3F
1K02R3F
MAYBE DUMMY
TP137
TP135
TP112
TP113
R583
R579
0R2-0
KA20GATE 37
KBRCIN# 37
Layout trace 15 mil
CLK48_USB 3
USBREXT
USBREXTB
USBP0P 33
USBP0N 33
USBP1P 28
USBP1N 28
USBP2P 28
USBP2N 28
USBP3P 28
USBP3N 28
USBP4P 28
USBP4N 28
USBP5P 28
USBP5N 28
USBP6P
USBP6N
USBP7N
USB0_OC#
USB1_OC#
USB2_OC#
USB3_OC#
USB4_OC#
USB5_OC#
USB6_OC#
USB7_OC#
RP3
SRP4K7
EMI
EC20
SCD1U16V
USBP6P
USBP6N
USBP7P
USBP7N
R282
R281
R449
R447
15KR3
RN29
KA20G
MSCK
MSDATA
KBRC
SRN4K7
0507-03'
To VT8235 Bug.
VT8237 unknow
PCIRST#_2
R557
SB_PCIRST#
DUMMY-R2
PWROK_SB
U54C
R551
0R2-0
R89
33R3
TSLCX08-U
R555
33R2
J8-SD: For SIV
U29A
U29B
BC312
SCD1U16V3KX
TSAHCT14
RSTDRV_5
RSTDRV#_5
RSTDRV#_5 26
U37C
U37D
BC139
SCD1U16V3KX
TSLCX14
PCIRST_NB
RST_NB#
RST_NB# 9
R965
47R2
U37E
U37F
BC131
SCD1U16V3KX
PCIRST_BUF
R966
R967
PCIRST_BUF# 14,19,29,31,33,34,37,39,40,42
37,43,45,46,48,50 PM_SLP_S3#
PM_SLP_S3#
24 PM_SUSCLK
PM_SUSCLK
U18
NC7SZ126-U
R123
10R3
SB_32KHZ
CLK32_G768 27
U46
NC7SZ08-1
8 HT_RST#
HT_RST#
RST_CPU# 6
2D5V_S0
U35A
TSLCX74
PM_SLP_S5#
PM_SLP_S5# 43,46,48,49,50
SUS_PCIRST
PCIRST#_2
R300
0R3-0-U
SUS_PCIRST# 37
0507-03'
To VT8235 Bug.
VT8237 unknow
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VT8235-PCI_USB
Size
Custom
Document Number
Gannet
Rev
-1
Date: Thursday, December 04, 2003
Sheet 23 of 51

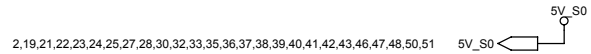

IDE
AC97
PMU
Hardware Trap
U58B
VT8235-CE
J8-SD
J8-SC:for Annie
Modify-0605
Modify-0602
Power Up Strappings
GPIO[A,C]==>LDT Frequency
00--> 200MHz (Default)
GPIOB==>LDT Width
0--> 8 Bit (Default)
SDA2==>ROMSIP Select
PDA2==>ROMSIP Select [for VT8237]
0--> Disable (default)
SDCS3#==> Test Mode Select
PDCS3#==> Test Mode Select
0--> Disable (Default)
SDCS1#==>Internal EEPROM Strapping
1--> External EEPROM (Default)
SEEDI ==>Internal EEPROM Strapping [for VT8237]
0--> External EEPROM (Default)
SXI==>LPC ROM Select
1--> Enable LPC ROM (Default)
GPIOD==>Transmit PLL Skew Control 1 [0]
SDA0==>Transmit PLL Skew Control 2 [0]
PDA0==>Transmit PLL Skew Control 2 [0]
SDA1==>External loop test mode [0]
PDA1==>External loop test mode [for VT8237]
0--> Disable (default)
SOE#==>Auto Reboot
1--> Disable (Default)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VT8235-IDE_AC97_PMU
Size A3
Document Number
Gannet
Rev -1
Date: Thursday, December 04, 2003
Sheet 24 of 51

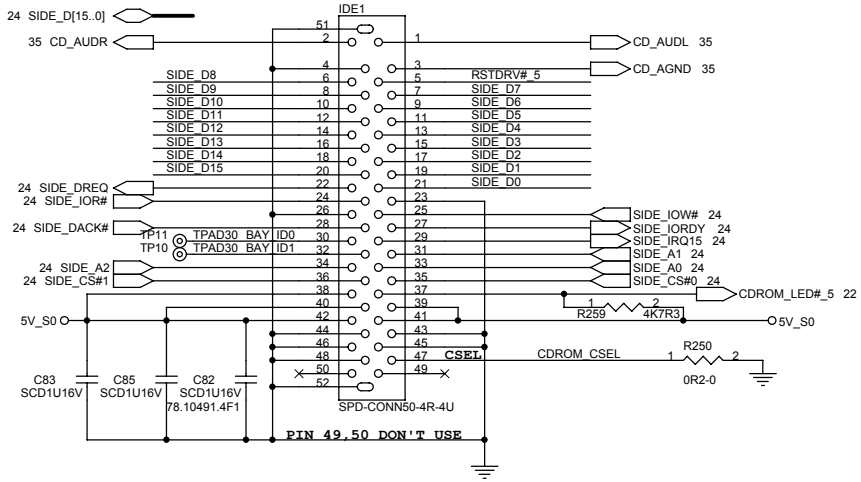

Modify-0602
Layout trace 20 mil
The voltage level of VL_VREF is 0.625V
Cross SB as short as possible
V-LINK
MII
LPC
HOST
VT8235-CE
2D5V_S5
3D5V_S5
Layout trace 20 mil
Modify-0602
Modify-0613
Pdiss(max)=1.2W
I max = 666 mA
Q94 & Q95 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
VT8235_VLINK_MII_LPC
Gannet
Thursday, December 04, 2003

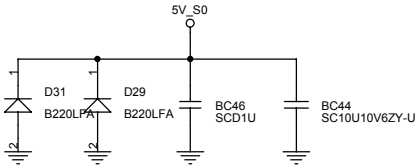
HDD

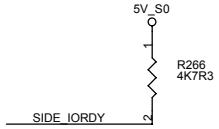


CDROM

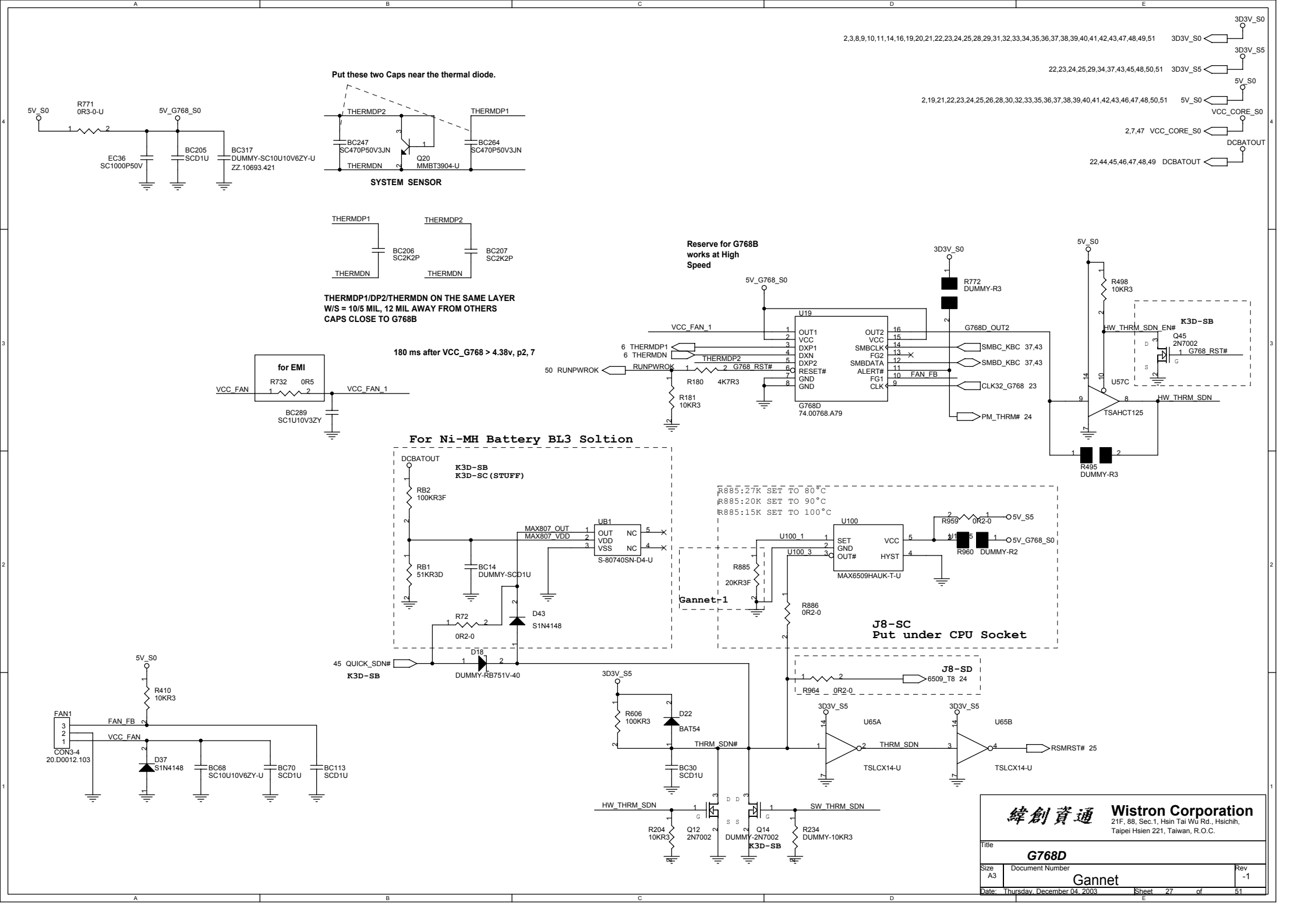






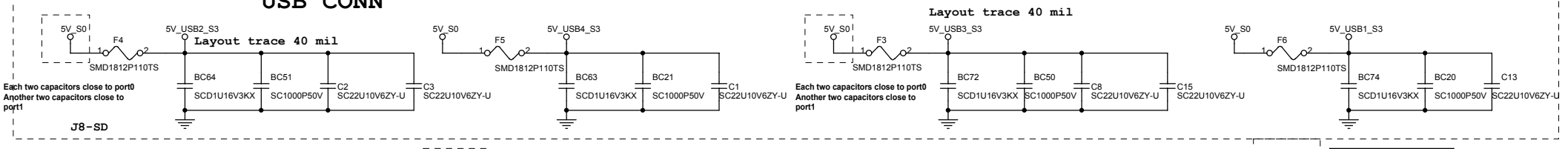


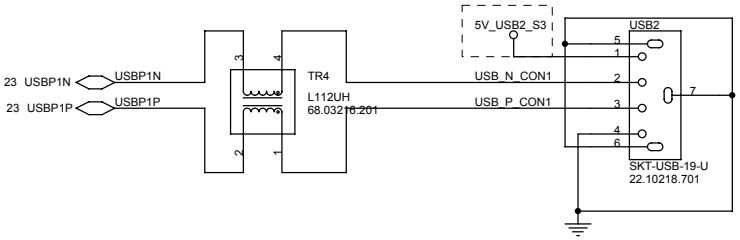
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD / CDROM***	
Size A3	Document Number Gannet	Rev -1
Date: Thursday, December 04, 2003	Sheet 26 of 51	



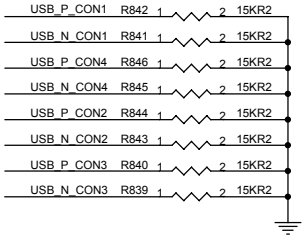
緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***G768D***
Size A3	Document Number: Gannet
Rev	-1
Date: Thursday, December 04, 2003	Sheet 27 of 51

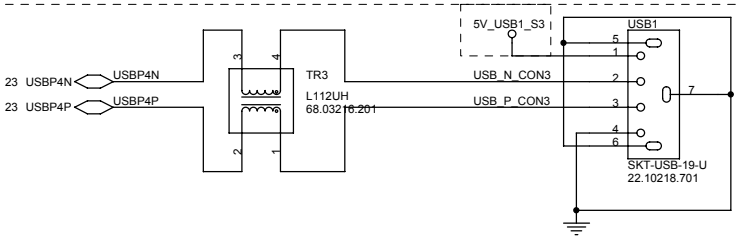
USB CONN



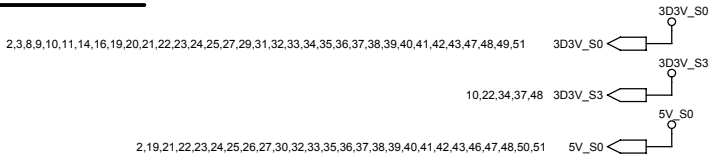


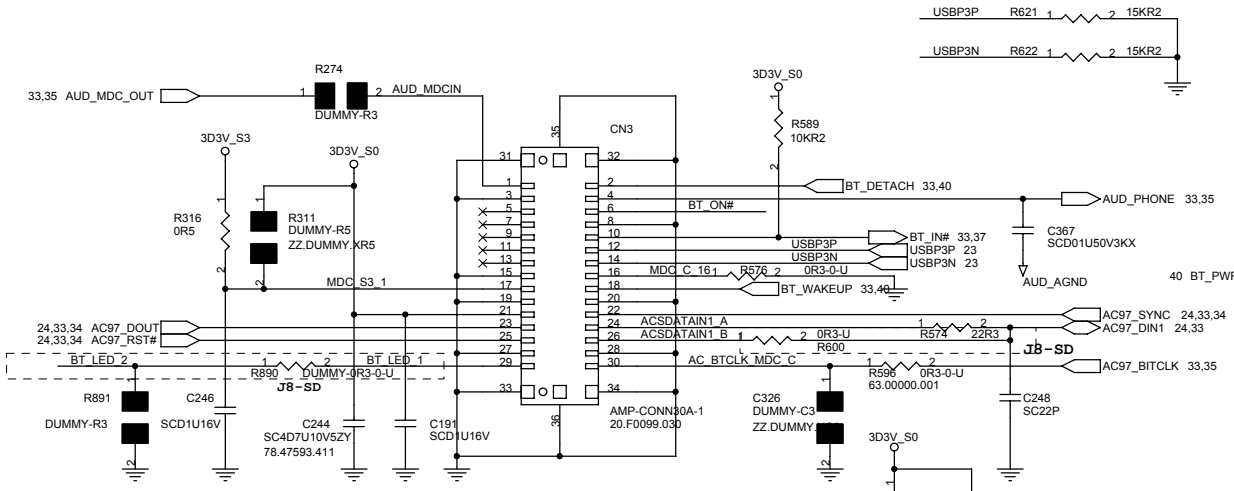
Modify at 05-08 03'

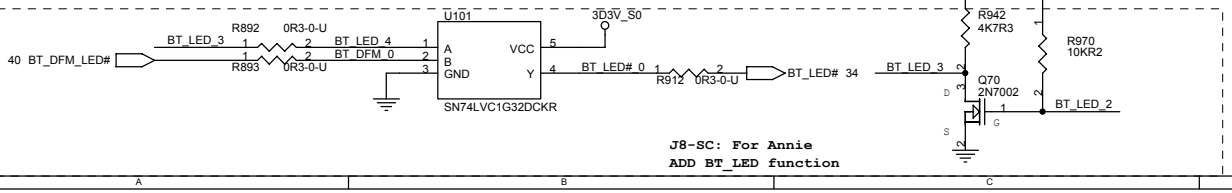




MDC Connector



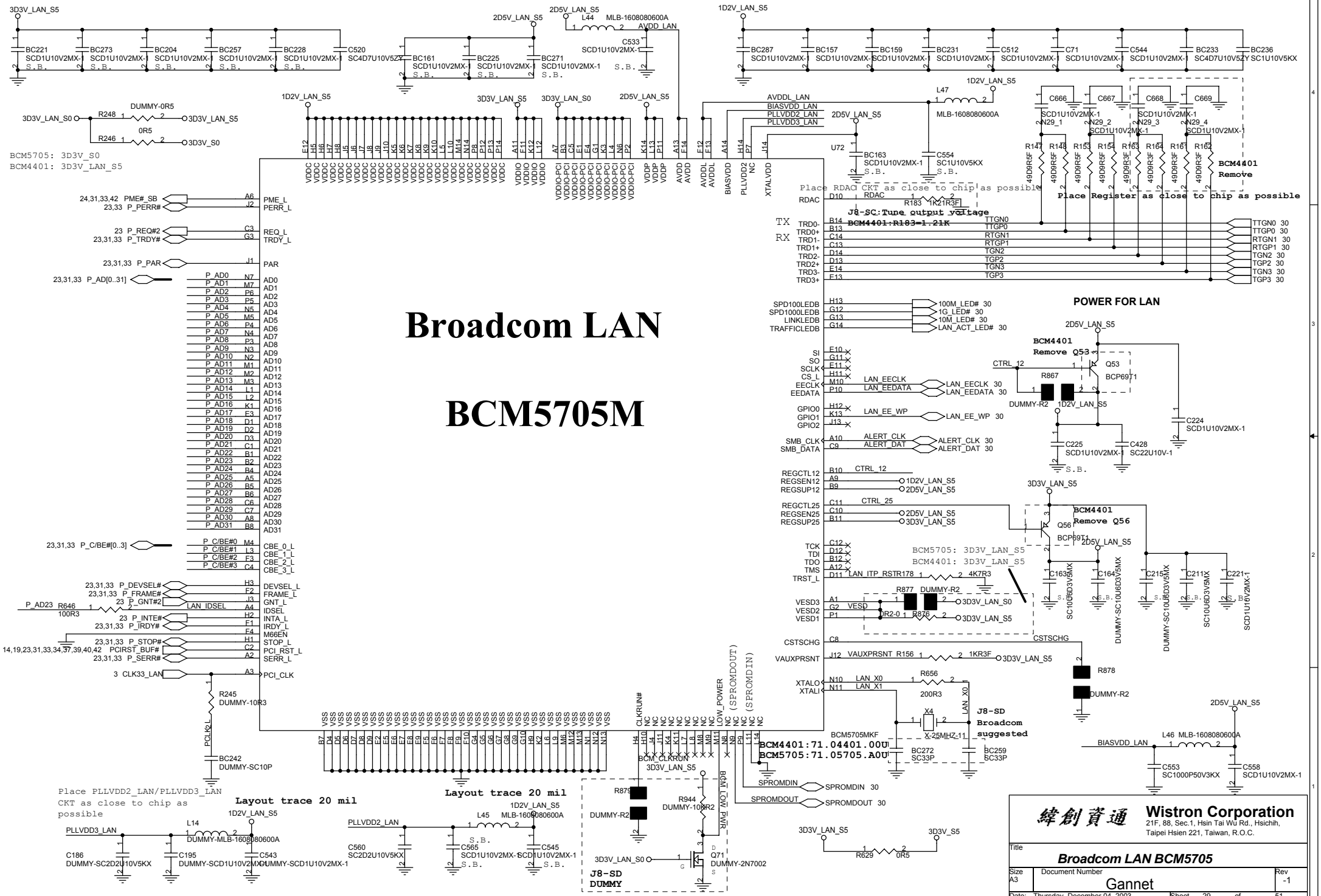




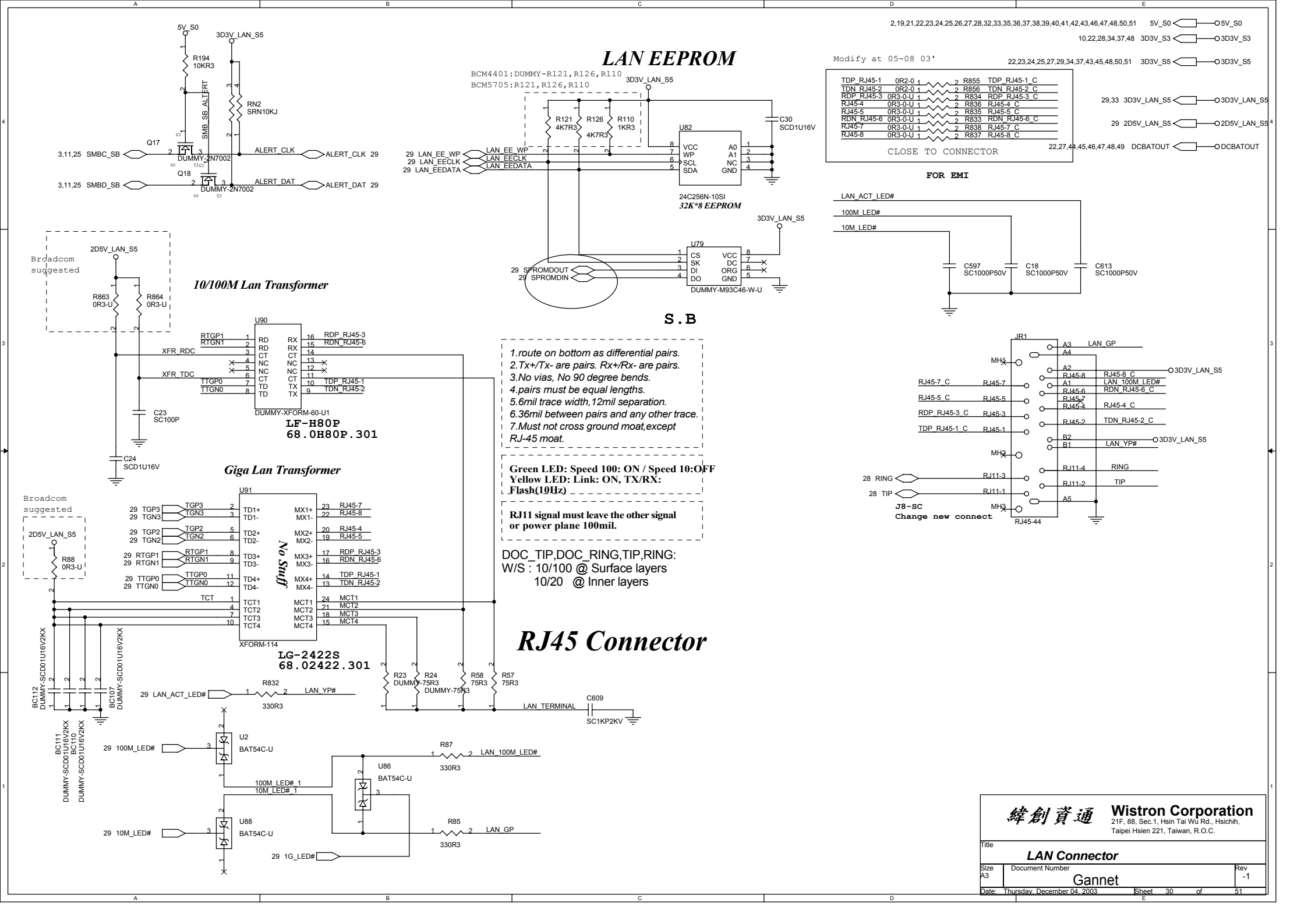
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB / MDC I/F and LAN***	
Size: Custom	Document Number: Gannet	Rev: -1
Date: Thursday, December 04, 2003	Sheet 28 of 51	

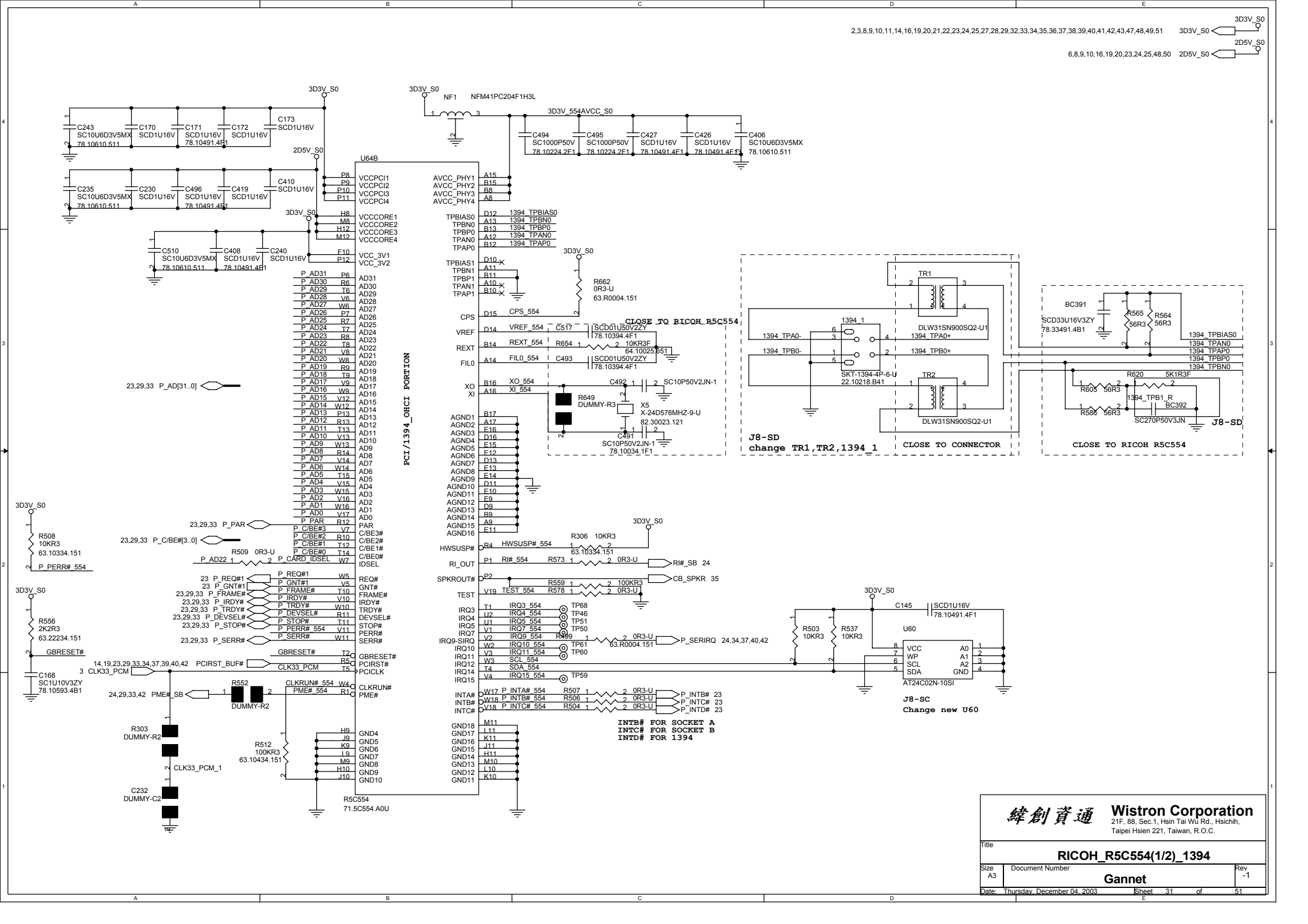
Broadcom LAN

BCM5705M

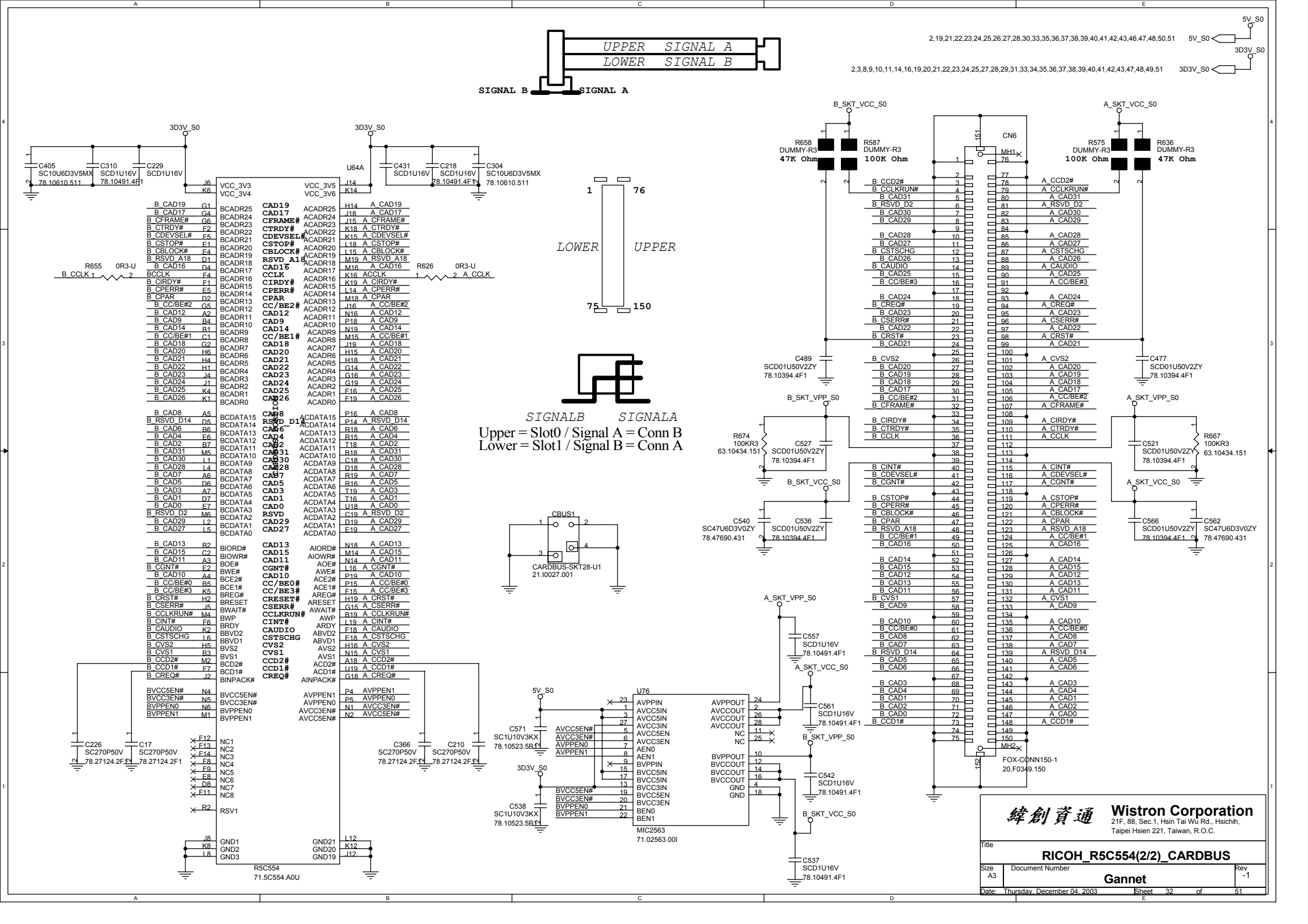


Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Broadcom LAN BCM5705	
Size: A3	Document Number: Gannet
Rev: -1	
Date: Thursday, December 04, 2003	Sheet 29 of 51


LAN EEPROM
BCM4401:DUMMY-R121,R126,R110
BCM5705:R121,R126,R110
3D3V_LAN_S5
R121 4K7R3
R126 4K7R3
R110 1KR3
C30 SCD1U16V
U82
VCC WP SCL SDA A0 A1 NC GND
29 LAN_EE_WP
29 LAN_EECLK
29 LAN_EEDATA
24C256N-10SI
32K*8 EEPROM
U79
CS SK DI DO VCC DC ORG GND
29 SPROMDOUT
29 SPROMDIN
DUMMY-M93C46-W-U
S.B
Modify at 05-08 03'
TDP_RJ45-1 0R2-0 R855 TDP_RJ45-1_C
TDN_RJ45-2 0R2-0 R856 TDN_RJ45-2_C
RDP_RJ45-3 0R3-0-U R834 RDP_RJ45-3_C
RJ45-4 0R3-0-U R836 RJ45-4_C
RJ45-5 0R3-0-U R835 RJ45-5_C
RDN_RJ45-6 0R3-0-U R833 RDN_RJ45-6_C
RJ45-7 0R3-0-U R838 RJ45-7_C
RJ45-8 0R3-0-U R837 RJ45-8_C
CLOSE TO CONNECTOR
FOR EMI
2,19,21,22,23,24,25,26,27,28,32,33,35,36,37,38,39,40,41,42,43,46,47,48,50,51 5V_S0
10,22,28,34,37,48 3D3V_S3
22,23,24,25,27,29,34,37,43,45,48,50,51 3D3V_S5
29,33 3D3V_LAN_S5
29 2D5V_LAN_S5
22,27,44,45,46,47,48,49 DCBATOUT
LAN_ACT_LED#
100M_LED#
10M_LED#
C597 SC1000P50V
C18 SC1000P50V
C613 SC1000P50V
5V_S0
3D3V_LAN_S5
R194 10KR3
RN2 SRN10KJ
SMB_SB_ALERT
Q17
Q18
DUMMY-2N7002
3,11,25 SMBC_SB
3,11,25 SMBD_SB
ALERT_CLK
ALERT_DAT
ALERT_CLK 29
ALERT_DAT 29
2D5V_LAN_S5
Broadcom suggested
R863 0R3-U
R864 0R3-U
10/100M Lan Transformer
U90
RTGP1 RTGN1 XFR_RDC XFR_TDC TTGP0 TTGN0
RD RX CT NC TD
RDP_RJ45-3
RDN_RJ45-6
TDP_RJ45-1
TDN_RJ45-2
C23 SC100P
C24 SCD1U16V
DUMMY-XFORM-60-U1
LF-H80P
68.0H80P.301
Giga Lan Transformer
U91
TGP3 TGN3 TGP2 TGN2 RTGP1 RTGN1 TTGP0 TTGN0 TCT
TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-
MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4-
MCT1 MCT2 MCT3 MCT4
RJ45-7 RJ45-8 RJ45-4 RJ45-5 RDP_RJ45-3 RDN_RJ45-6 TDP_RJ45-1 TDN_RJ45-2
No Stuff
XFORM-114
LG-2422S
68.02422.301
R88 0R3-U
BC112 DUMMY-SCD01U16V2KX
BC107 DUMMY-SCD01U16V2KX
BC111 DUMMY-SCD01U16V2KX
BC110 DUMMY-SCD01U16V2KX
R832 330R3
29 LAN_ACT_LED#
LAN_YP#
R23 DUMMY-75R3
R24 DUMMY-75R3
R58 75R3
R57 75R3
LAN_TERMINAL
C609 SC1KP2KV
U2 BAT54C-U
U86 BAT54C-U
U88 BAT54C-U
29 100M_LED#
29 10M_LED#
29 1G_LED#
R87 330R3
R85 330R3
LAN_100M_LED#
LAN_GP
100M_LED# 1
10M_LED# 1
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width,12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat,except RJ-45 moat.
Green LED: Speed 100: ON / Speed 10:OFF
Yellow LED: Link: ON, TX/RX: Flash(10Hz)
RJ11 signal must leave the other signal or power plane 100mil.
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers
RJ45 Connector
JR1
A3 LAN_GP
A4
A2 RJ45-8 RJ45-8_C
A1 LAN_100M_LED# RDN_RJ45-6_C
RJ45-6 RJ45-7
RJ45-4 RJ45-4_C
RJ45-2 TDN_RJ45-2_C
B2
B1 LAN_YP#
RJ11-4 RING
RJ11-2 TIP
A5
MH1 MH2 MH3
RJ45-7_C RJ45-5_C RDP_RJ45-3_C TDP_RJ45-1_C
RJ45-7 RJ45-5 RJ45-3 RJ45-1
RJ11-3 RJ11-1
28 RING
28 TIP
J8-SC
Change new connect
RJ45-44
3D3V_LAN_S5
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN Connector
Size A3
Document Number
Gannet
Rev -1
Date: Thursday, December 04, 2003
Sheet 30 of 51



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**RICOH_R5C554(1/2)_1394**	
Size A3	Document Number **Gannet**	Rev -1
Date: Thursday, December 04, 2003	Sheet 31 of 51	



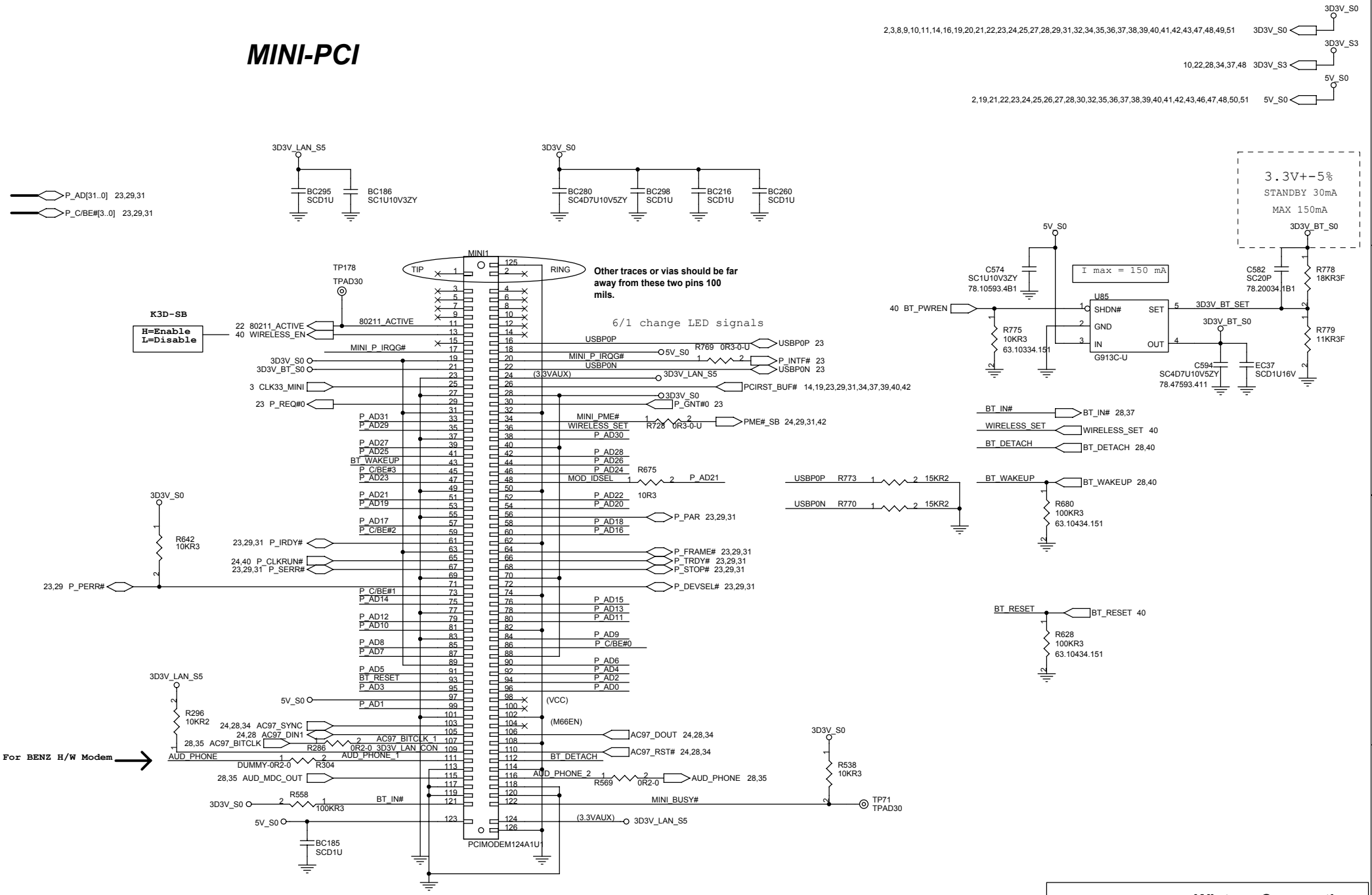
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RICOH_R5C554(2/2)_CARDBUS

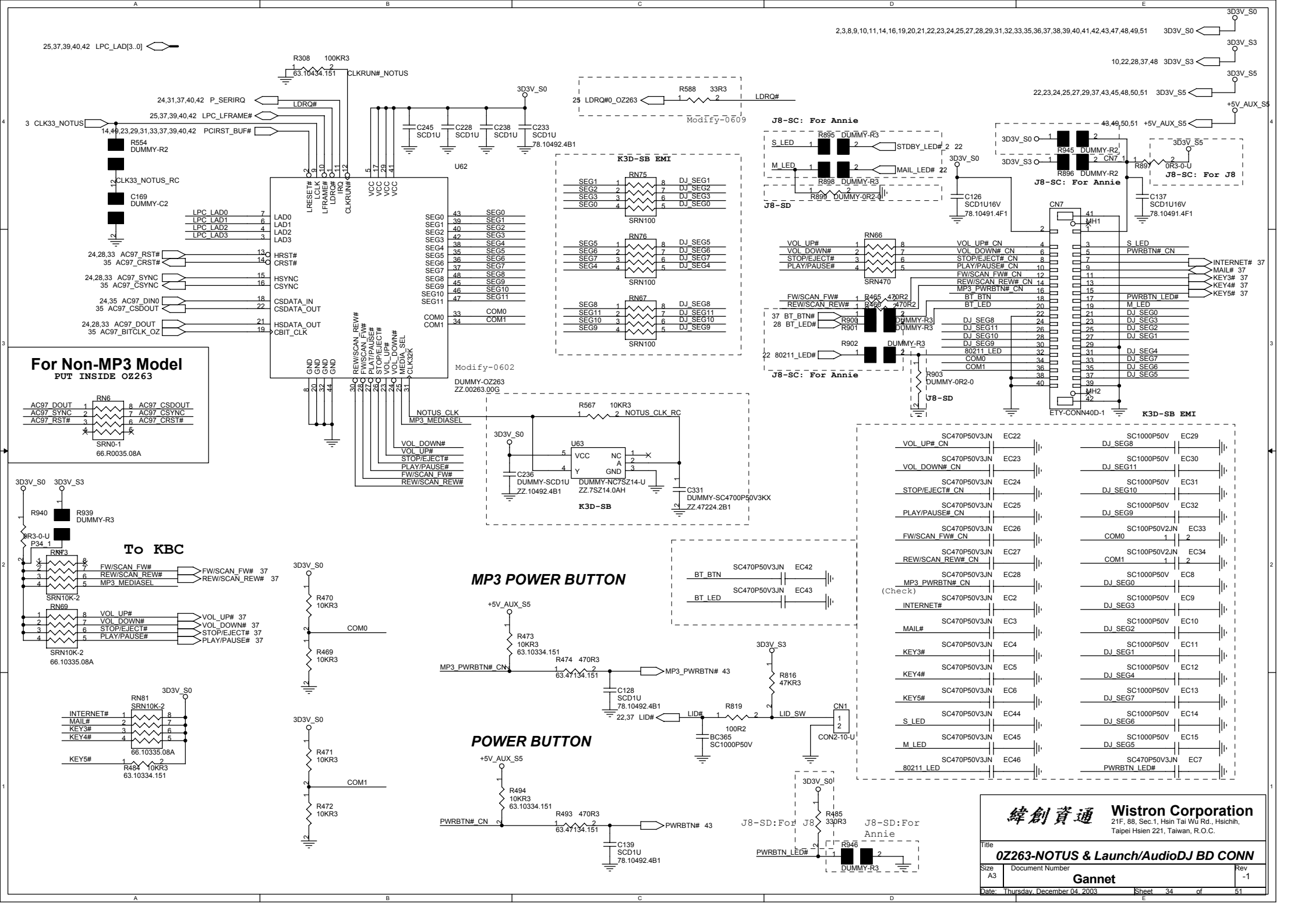
Size	Document Number	Rev
A3	Gannet	-1

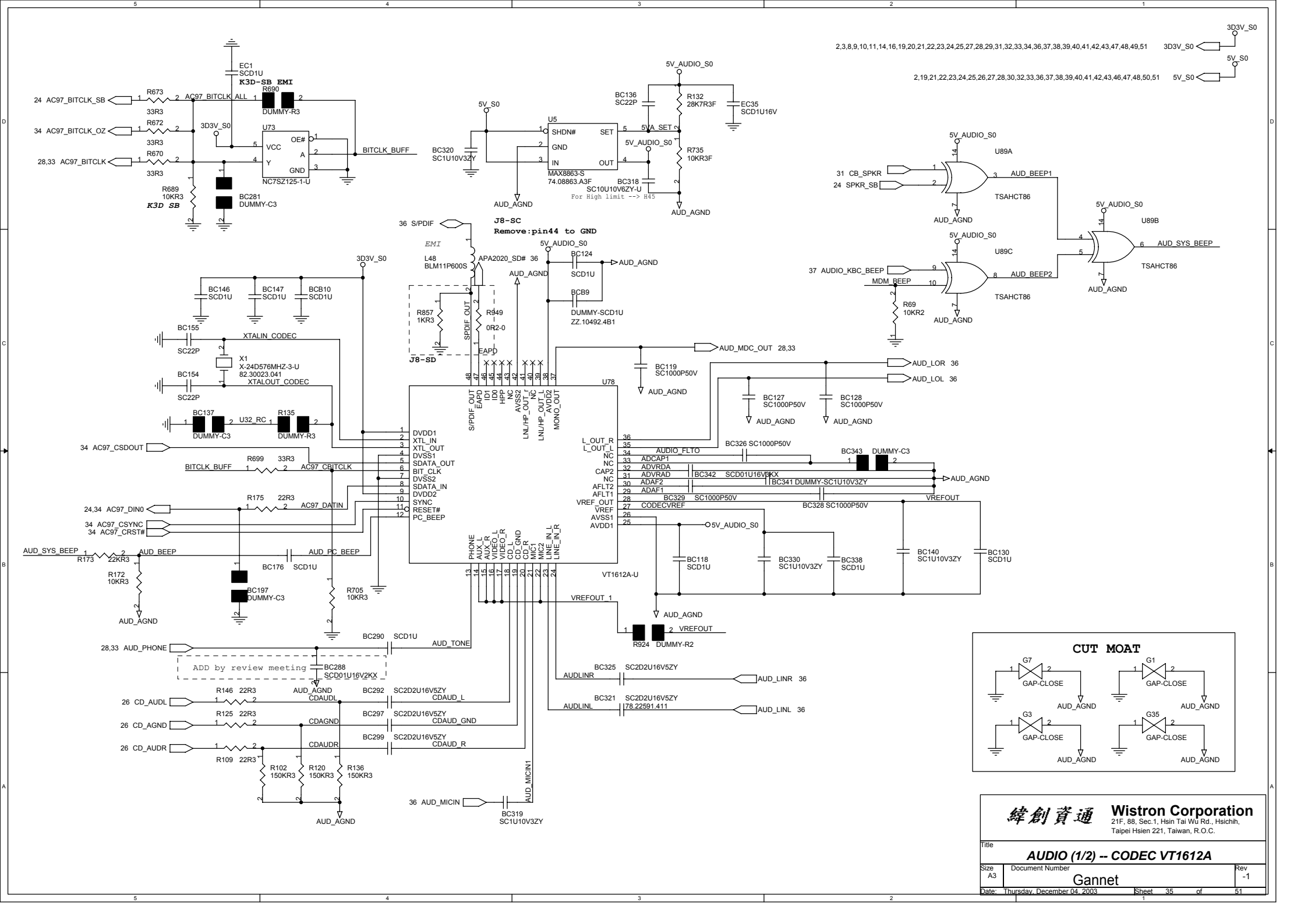
Date: Thursday, December 04, 2003 Sheet 32 of 51

MINI-PCI



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI-PCI***	
Size A3	Document Number Gannet	Rev -1
Date: Thursday, December 04, 2003	Sheet 33 of 51	


25,37,39,40,42 LPC_LAD[3..0]
R308 100KR3
63.10434.151
CLKRUN#_NOTUS
24,31,37,40,42 P_SERIRQ
LDRQ#
25,37,39,40,42 LPC_LFRAME#
3 CLK33_NOTUS
14,49,23,29,31,33,37,39,40,42 PCIRST_BUF#
R554
DUMMY-R2
CLK33_NOTUS_RC
C169
DUMMY-C2
U62
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LAD0
LAD1
LAD2
LAD3
24,28,33 AC97_RST#
35 AC97_CRST#
HRST#
CRST#
24,28,33 AC97_SYNC
35 AC97_CSYNC
HSYNC
CSYNC
24,35 AC97_DIN0
35 AC97_CSDOUT
CSDATA_IN
CSDATA_OUT
24,28,33 AC97_DOUT
35 AC97_BITCLK_OZ
HSDATA_OUT
CBIT_CLK
LRESET#
LCLK
LFRAME#
LDRQ#
IRQ
CLKRUN#
VCC
GND
SEG0
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG8
SEG9
SEG10
SEG11
COM0
COM1
REW/SCAN_REW#
FW/SCAN_FW#
PLAY/PAUSE#
STOP/EJECT#
VOL_UP#
VOL_DOWN#
MEDIA_SEL
CLK32K
Modify-0602
DUMMY-OZ263
ZZ.00263.00G
C245 SCD1U
C228 SCD1U
C238 SCD1U
C233 SCD1U
78.10492.4B1
3D3V_S0
25 LDRQ#0_OZ263
R588 33R3
LDRQ#
Modify-0609
K3D-SB EMI
RN75
RN76
RN67
SRN100
DJ_SEG0
DJ_SEG1
DJ_SEG2
DJ_SEG3
DJ_SEG4
DJ_SEG5
DJ_SEG6
DJ_SEG7
DJ_SEG8
DJ_SEG9
DJ_SEG10
DJ_SEG11
For Non-MP3 Model
PUT INSIDE OZ263
RN6
AC97_DOUT
AC97_SYNC
AC97_RST#
AC97_CSDOUT
AC97_CSYNC
AC97_CRST#
SRN0-1
66.R0035.08A
NOTUS_CLK
MP3_MEDIASEL
R567 10KR3
NOTUS_CLK_RC
U63
VCC
NC
A
Y
GND
C236
DUMMY-SCD1U
ZZ.10492.4B1
DUMMY-NC7SZ14-U
ZZ.7SZ14.0AH
C331
DUMMY-SC4700P50V3KX
ZZ.47224.2B1
K3D-SB
J8-SC: For Annie
J8-SD
S_LED
M_LED
STDBY_LED#
MAIL_LED#
R895 DUMMY-R3
R898 DUMMY-R3
R899 DUMMY-0R2-0
C126
SCD1U16V
78.10491.4F1
R945 DUMMY-R2
R896 DUMMY-R2
R897 0R3-0-U
J8-SC: For J8
C137
SCD1U16V
78.10491.4F1
CN7
MH1
MH2
ETY-CONN40D-1
RN66
SRN470
VOL_UP#
VOL_DOWN#
STOP/EJECT#
PLAY/PAUSE#
FW/SCAN_FW#
REW/SCAN_REW#
MP3_PWRBTN#
BT_BTN
BT_LED
80211_LED
COM0
COM1
R465 470R2
R466 470R2
R900 DUMMY-R3
R901 DUMMY-R3
R902 DUMMY-R3
R903 DUMMY-0R2-0
37 BT_BTN#
28 BT_LED#
22 80211_LED#
INTERNET# 37
MAIL# 37
KEY3# 37
KEY4# 37
KEY5# 37
PWRBTN_LED#
To KBC
RN73
SRN10K-2
RN69
66.10335.08A
R940
R939
DUMMY-R3
0R3-0-U
P34_1
FW/SCAN_FW# 37
REW/SCAN_REW# 37
VOL_UP# 37
VOL_DOWN# 37
STOP/EJECT# 37
PLAY/PAUSE# 37
RN81
INTERNET#
MAIL#
KEY3#
KEY4#
KEY5#
R484 10KR3
63.10334.151
R470 10KR3
R469 10KR3
R471 10KR3
R472 10KR3
COM0
COM1
MP3 POWER BUTTON
POWER BUTTON
+5V_AUX_S5
R473 10KR3 63.10334.151
R474 470R3 63.47134.151
MP3_PWRBTN# 43
MP3_PWRBTN#_CN
C128 SCD1U 78.10492.4B1
22,37 LID#
R816 47KR3
R819 100R2
BC365 SC1000P50V
LID_SW
CN1
CON2-10-U
R494 10KR3 63.10334.151
R493 470R3 63.47134.151
PWRBTN# 43
PWRBTN#_CN
C139 SCD1U 78.10492.4B1
R485 330R3
R946 DUMMY-R3
PWRBTN_LED#
J8-SD:For J8
J8-SD:For Annie
BT_BTN
BT_LED
SC470P50V3JN EC42
SC470P50V3JN EC43
SC470P50V3JN EC22
SC1000P50V EC29
SC470P50V3JN EC23
SC1000P50V EC30
SC470P50V3JN EC24
SC1000P50V EC31
SC470P50V3JN EC25
SC1000P50V EC32
SC470P50V3JN EC26
SC100P50V2JN EC33
SC470P50V3JN EC27
SC100P50V2JN EC34
SC470P50V3JN EC28
SC1000P50V EC8
(Check)
SC470P50V3JN EC2
SC1000P50V EC9
SC470P50V3JN EC3
SC1000P50V EC10
SC470P50V3JN EC4
SC1000P50V EC11
SC470P50V3JN EC5
SC1000P50V EC12
SC470P50V3JN EC6
SC1000P50V EC13
SC470P50V3JN EC44
SC1000P50V EC14
SC470P50V3JN EC45
SC1000P50V EC15
SC470P50V3JN EC46
SC470P50V3JN EC7
2,3,8,9,10,11,14,16,19,20,21,22,23,24,25,27,28,29,31,32,33,35,36,37,38,39,40,41,42,43,47,48,49,51 3D3V_S0
10,22,28,37,48 3D3V_S3
22,23,24,25,27,29,37,43,45,48,50,51 3D3V_S5
43,49,50,51 +5V_AUX_S5
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
0Z263-NOTUS & Launch/AudioDJ BD CONN
Size A3
Document Number
Gannet
Rev -1
Date: Thursday, December 04, 2003
Sheet 34 of 51



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO (1/2) -- CODEC VT1612A***	
Size A3	Document Number: Gannet	Rev -1
Date: Thursday, December 04, 2003	Sheet 35 of 51	

SA DV-2 U78 change from APA2020 to APA2020ARI-TR

J8-SC
Delete "Bo" sound

LINE IN

MIC PREAMP

LINE OUT

If R->L 避免 noise
1000P -> 100P

J8-SD: Remove EC40,EC41
MODIFY BY EMI

For depop

SB-31-5
Remove Q16,U30,BC200,R168,R167

SB-0724-1

K3D-SB

K3D-SB EMI

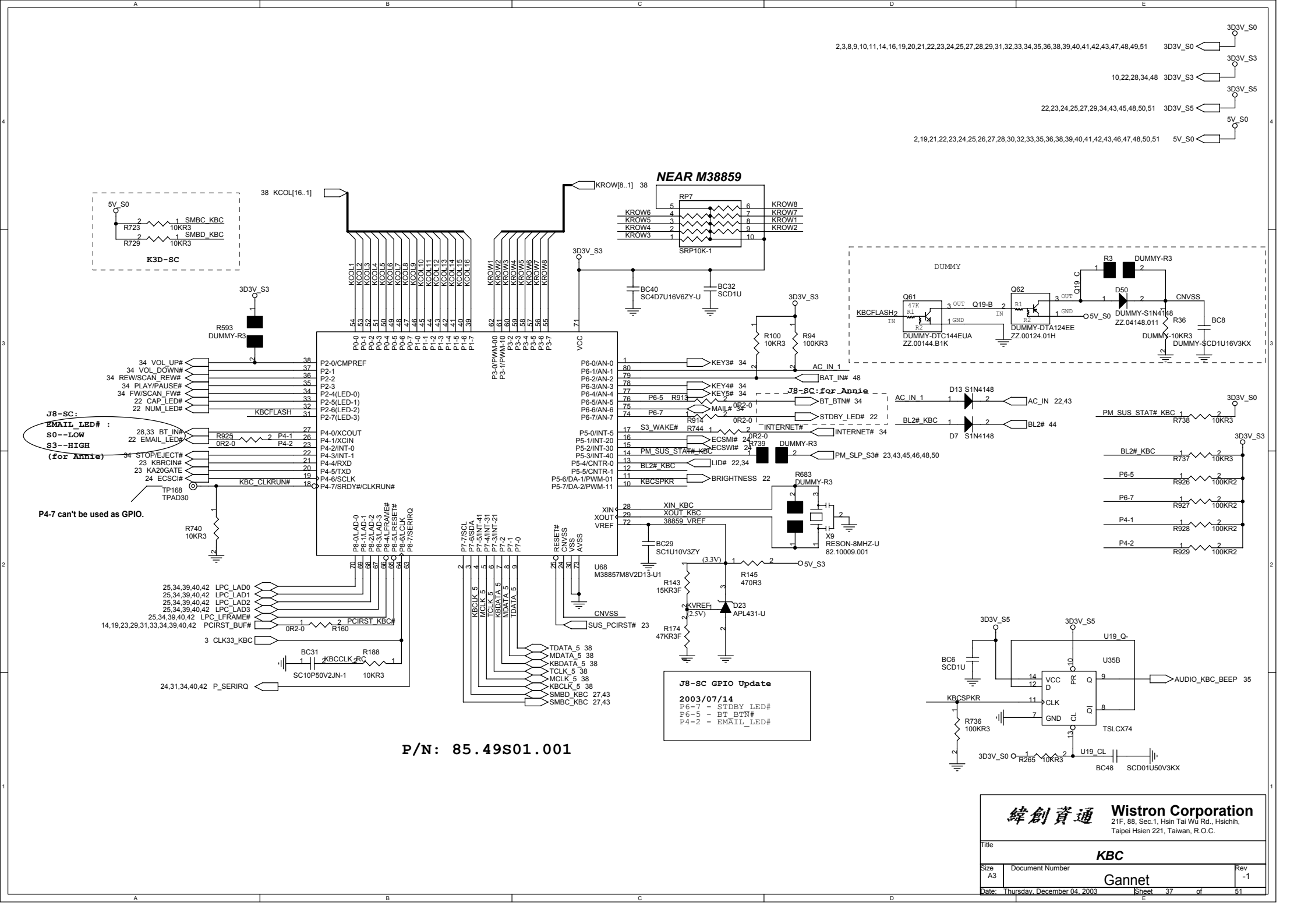
J8-SD

SB-31-4

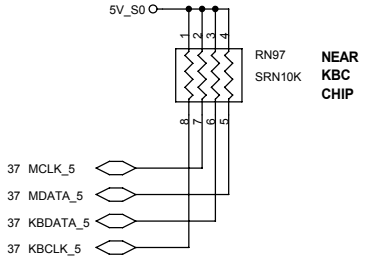
SB-31-3

For no S/PDIF,
P/N: 22.10257.001
FOXCONN

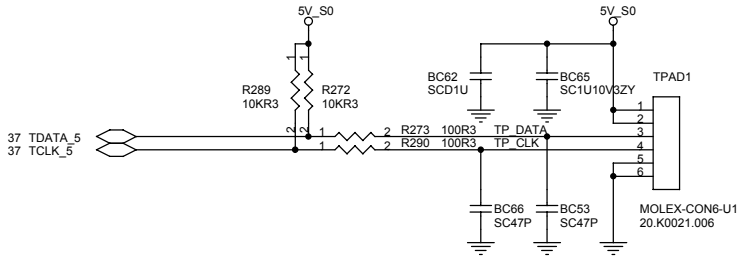
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO (2/2)***	
Size A3	Document Number Gannet	Rev -1
Date: Thursday, December 04, 2003	Sheet 36 of 51	


NEAR M38859
K3D-SC
J8-SC:
EMAIL_LED# :
S0--LOW
S3--HIGH
(for Annie)
P4-7 can't be used as GPIO.
J8-SC:for Annie
J8-SC GPIO Update
2003/07/14
P6-7 - STDBY_LED#
P6-5 - BT_BTN#
P4-2 - EMAIL_LED#
DUMMY
U68
M38857M8V2D13-U1
U19_Q-
U35B
TSLCX74
P/N: 85.49S01.001
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC
Gannet
Thursday, December 04, 2003
Sheet 37 of 51

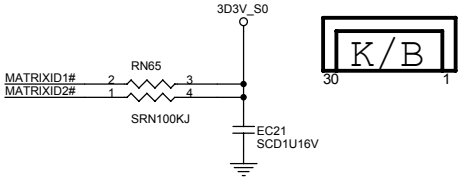
PS/2 CONN

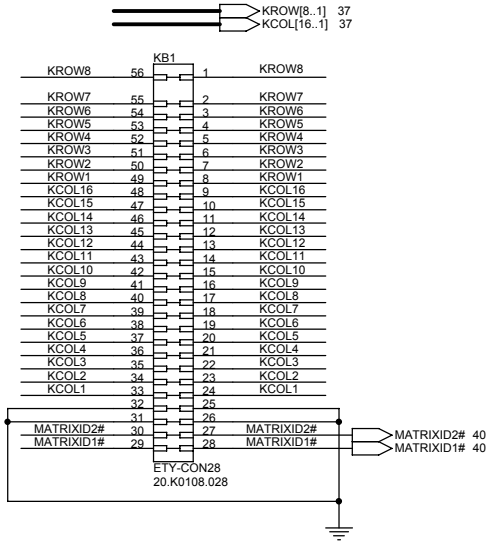


TOUCH PAD



Internal KeyBoard CONN



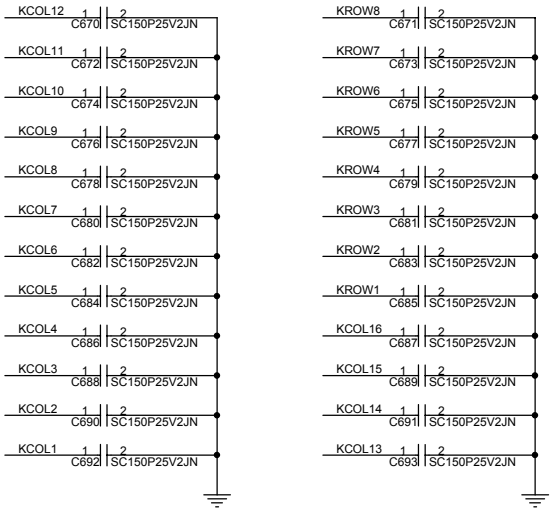


SB

Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

7/09 EMI Bypass cap.

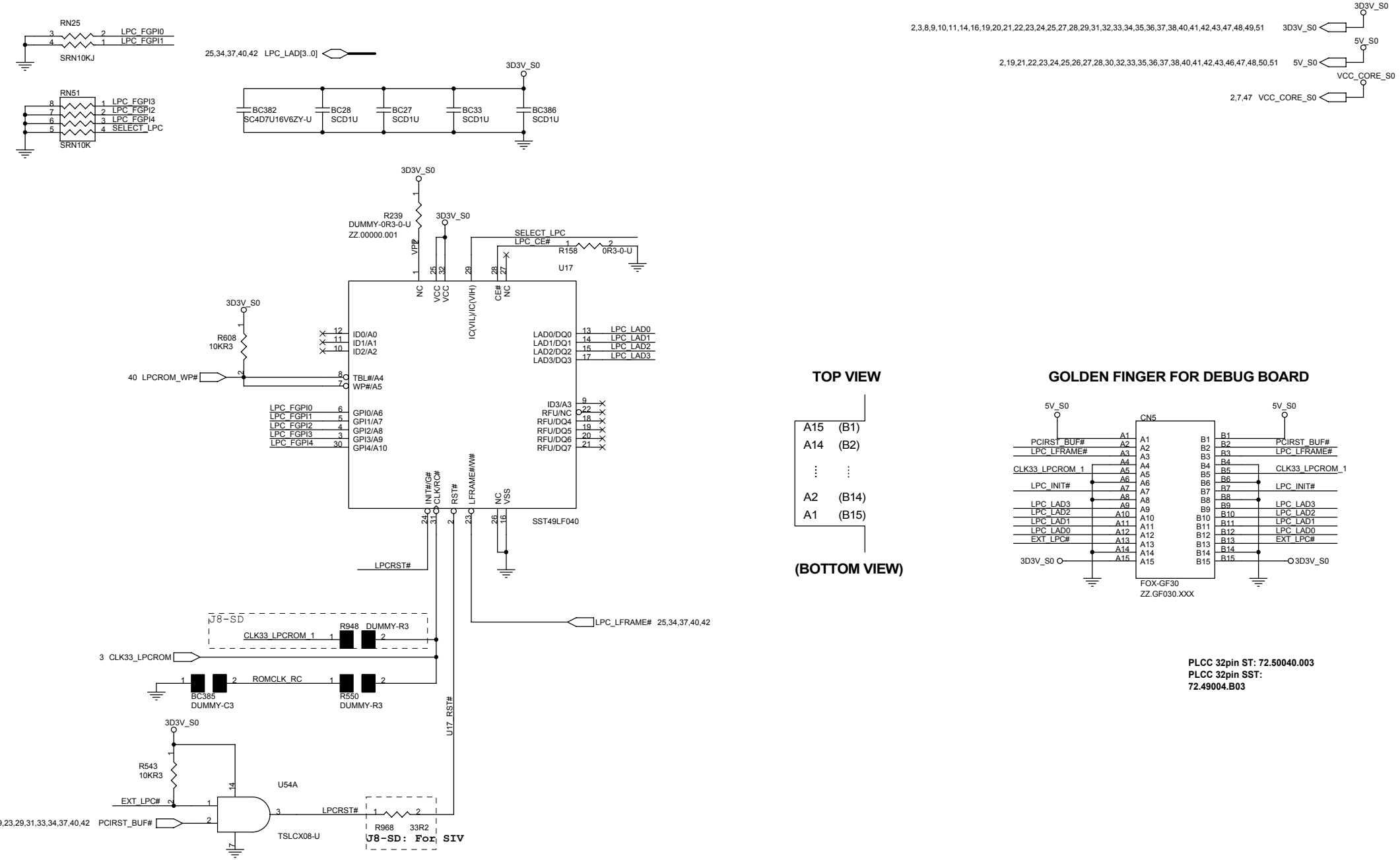


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

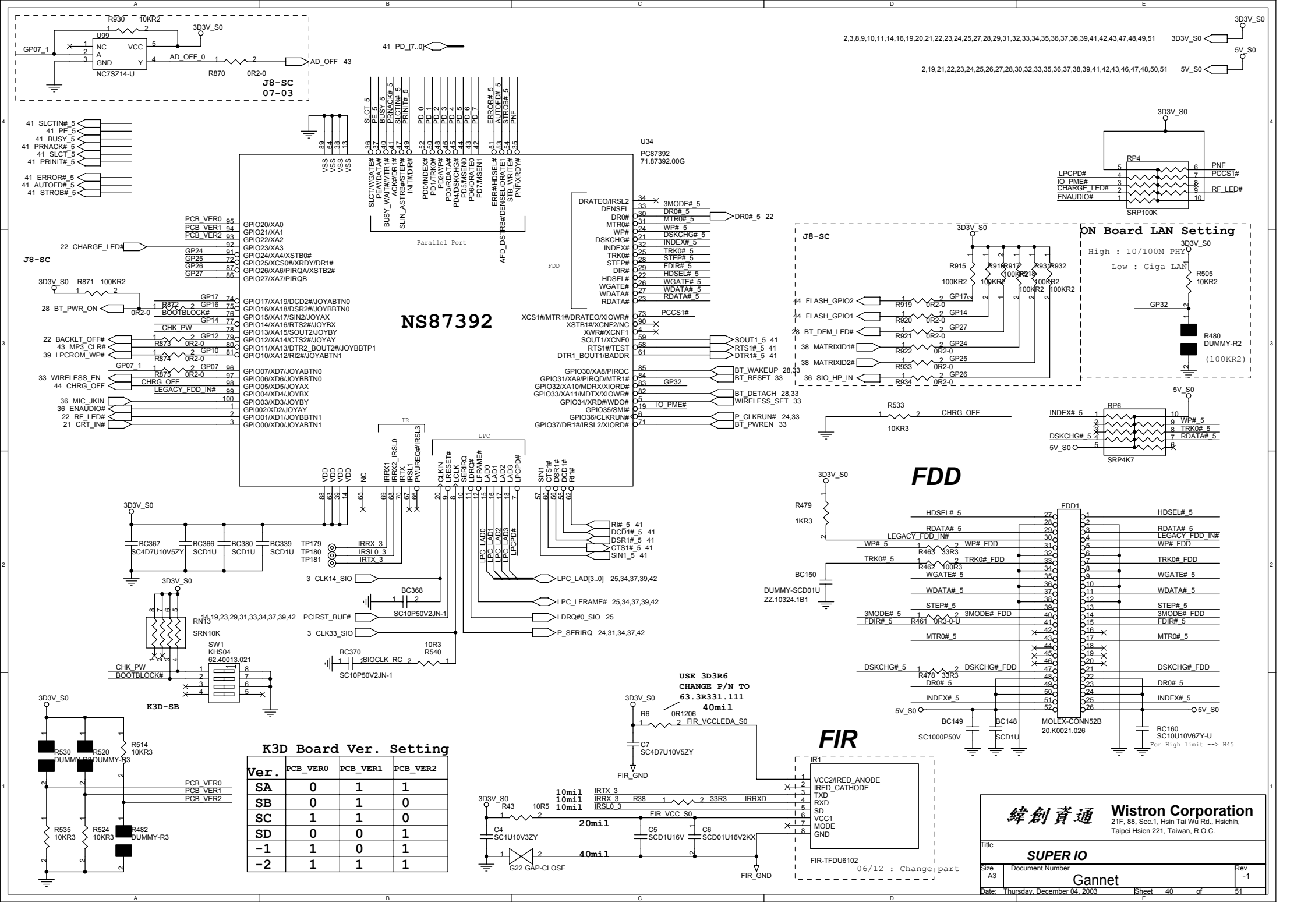
Title: ***PS2 / TOUCHPAD / KB CONN***

Size: A3 | Document Number: Gannet | Rev: -1

Date: Thursday, December 04, 2003 | Sheet 38 of 51



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LPCROM / DEBUG PORT***	
Size A3	Document Number Gannet	Rev -1
Date: Thursday, December 04, 2003	Sheet 39 of 51	


NS87392
J8-SC
07-03
J8-SC
K3D-SB
FDD
FIR
ON Board LAN Setting
High : 10/100M PHY
Low : Giga LAN
USE 3D3R6
CHANGE P/N TO
63.3R331.111
40mil
Parallel Port
FDD
LPC
IR
K3D Board Ver. Setting
Ver. | PCB_VER0 | PCB_VER1 | PCB_VER2
SA | 0 | 1 | 1
SB | 0 | 1 | 0
SC | 1 | 1 | 0
SD | 0 | 0 | 1
-1 | 1 | 0 | 1
-2 | 1 | 1 | 1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SUPER IO
Size A3
Document Number
Gannet
Rev -1
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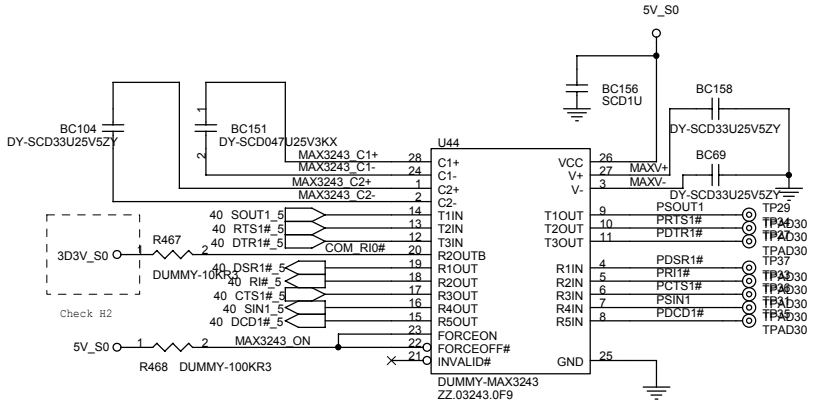
SERIAL PORT

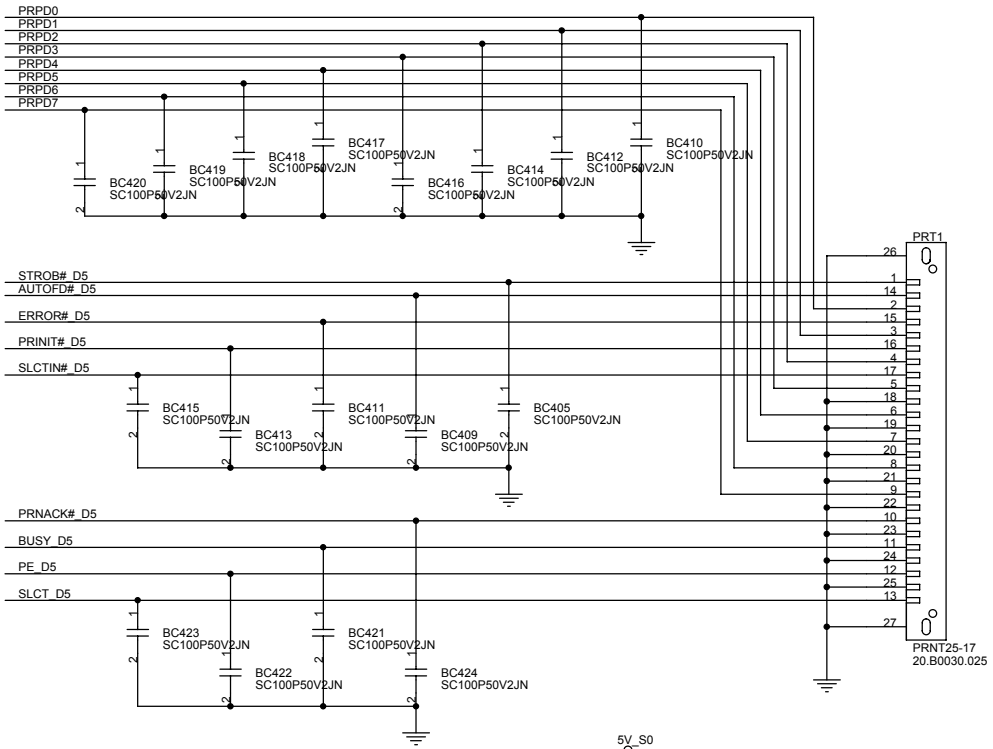


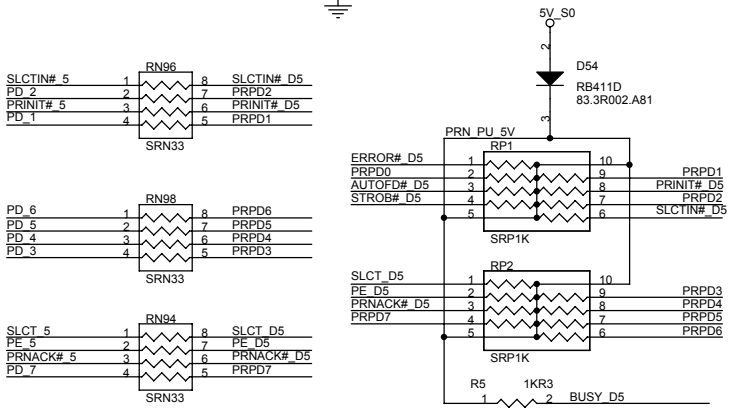
SA DV-3 Change MAX3243CDB TI to MAX3243 MAXIM

PRINTER PORT

2,3,8,9,10,11,14,16,19,20,21,22,23,24,25,27,28,29,31,32,33,34,35,36,37,38,39,40,42,43,47,48,49,51 — 3D3V_S0

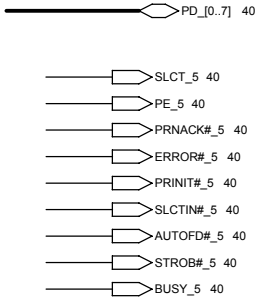
2,19,21,22,23,24,25,26,27,28,30,32,33,35,36,37,38,39,40,42,43,46,47,48,50,51 — 5V_S0





CHECK PULL HIGH

FROM SIO



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PORTS***

Size	Document Number	Rev
A3	Gannet	-1

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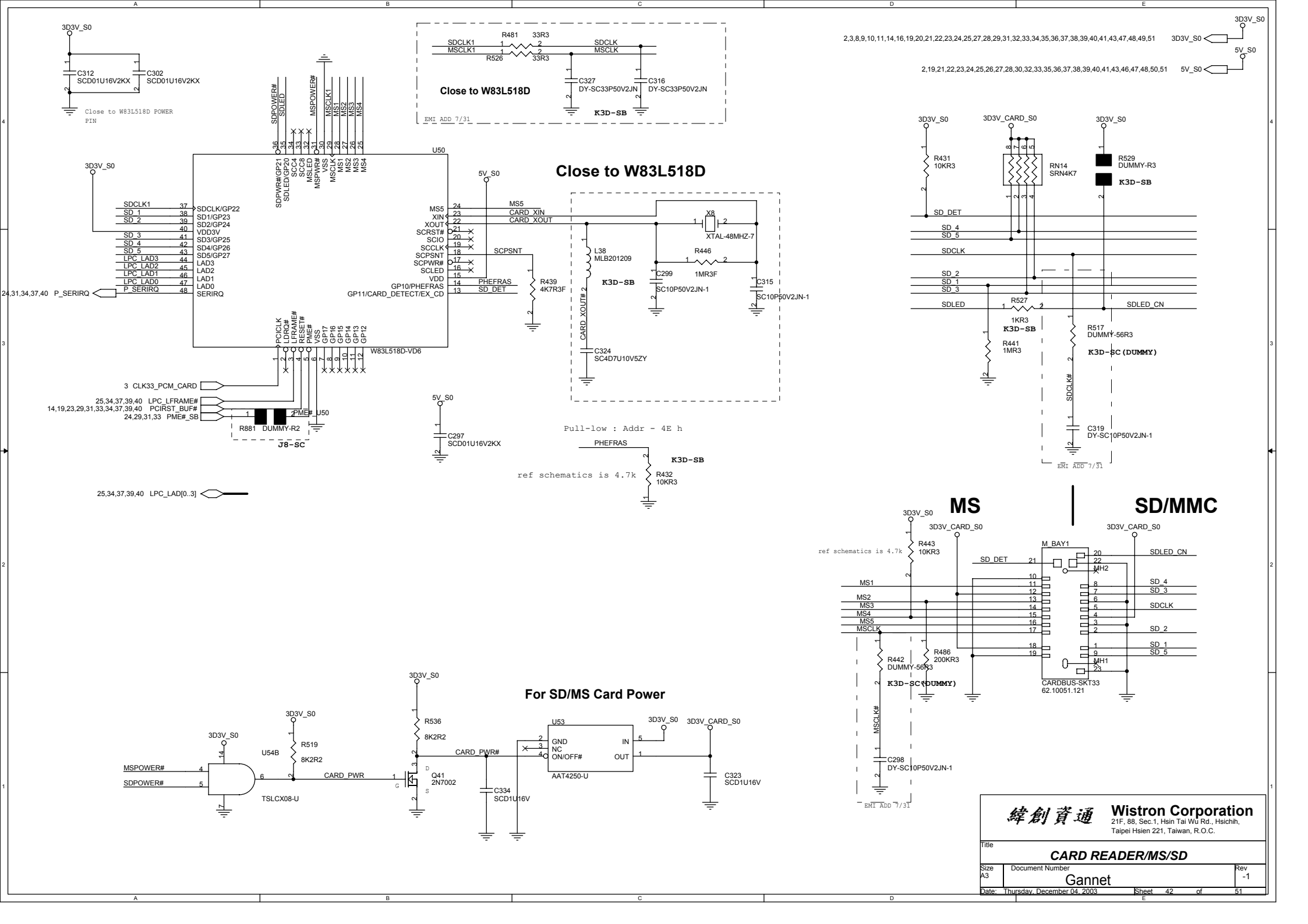

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CARD READER/MS/SD***	
Size A3	Document Number Gannet	Rev -1
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Change new part-0611

Origin: Fuse between Jack & inductor
F4:R451007, P/N: 69.47001.011

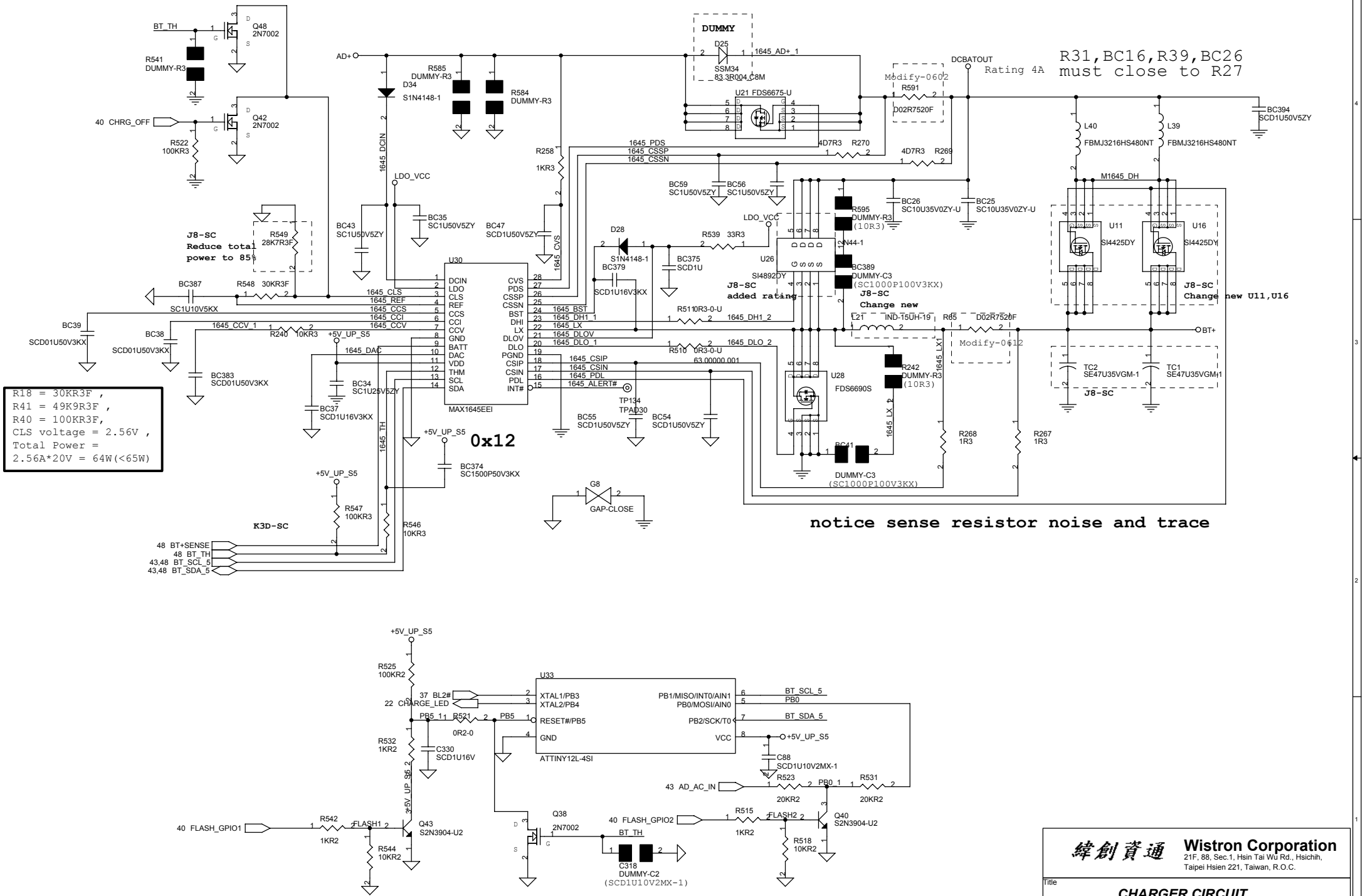
DCIN1
Layout trace 200 mil
AD_JACK+
L5 FBMJ3216HS480NT
LB1 FBMJ3216HS480NT
SC100P50V2JN
BC52
C14 SCD1U50V3KX 78.10424.2B1
DC-JACK49-U2
Layout trace 200 mil
ADJACK
BC76 SCD1U
U94
FDS6675-U
AD+
R787 56KR3 K3D-SB
Modify-0602
C580 SC1U10V3ZY
+5V_AUX_S5
AC_IN 22,37
R797 10KR3
R805 1KR3F N43-2
Q4 2N7002
Q66 2N7002
U49A
TSAHCT32 K3D-SB
AD_AC_IN 44
R464 DUMMY-R2
47,48 12VGATE_S0
0R2-0 R37
12VGATE_S0_1
+5V_UP_S5
R34 10KR3
R44 10KR3
27,37 SMBD_KBC
BT_SDA_5
BT_SDA_5 44,48
Q3 2N7002
27,37 SMBC_KBC
BT_SCL_5
BT_SCL_5 44,48
Q11 2N7002
AD_OFF# 2
R828 10KR3
40 AD_OFF
AD_OFF_1
Q68 2N7002
BC363 SC1U10V3ZY
R827 100KR3
Q2 DTA124EUA-U1
R33 100KR3
AD_SWITCH
C16 N43-1
SCD1U50V3KX
BC79 SCD1U50V5KX
R35 56KR3
R799 10KR3
Change to SIO GPIO07

3D3V_S5
+5V_AUX_S5
R360 22KR3
MP3_PRE#
C120 SCD1U
U38A TSAHCT74
R436 10KR2
R437 DUMMY-R2
MP3_PWERON
24 MP3PWR_ON#
D36 RB751V-40
K3D-SB
MP3_PWERON#
MP3_BTN
R299 1KR2
K3D-SB
MP3_PWRBTN
U55E TSAHCT14
MP3_PWRBTN#
C107 SCD1U
MP3_CL#
Q37 2N7002
PWR_CTL Logic BY Hardware

5V_S0
R375 10KR2
MP3_CLR
MP3_CLR# 40
Q24 DUMMY-2N7002 K3D-SB
Q26 DUMMY-2N7002
R349 22KR3
BC301 SCD1U16V
HI_PAUSE
Q23 2N7002
U52 NC7ST08-U
DL_ALL_PG
MP3_SLP_S3
U55A TSAHCT14
R500 10KR3
MP3_SLP_S3_1
U55F TSAHCT14
PM_SLP_S3#
PM_SLP_S3# 23,37,45,46,48,50
BC178 SC1U10V3ZY
J8-SC
R882 4K7R3
MP3BT_ON#

3D3V_S5
R880 4K7R3
24 PM_PWRBTN#
To SB
D10 S1N4148
PM_PWRBTN#_1
U55B TSAHCT14
PWRBTN_3
R483 47KR3
PWRBTN_2
BC169 SC1U10V3ZY K3D-SB
U49B TSAHCT32
PWRBTN_74
PM_SLP_S5#
PM_SLP_S5# 23,46,48,49,50
U38B TSAHCT74
U50_PR
R351 10KR3
U50_CL
R412 22KR3
BC138 SCD1U
Q29 2N7002
3D3V_S0
R307 10KR3
Q26
SB-40-1
U55C TSAHCT14
R528 47KR3
PWRBTN#
PWRBTN# 34
D40 S1N4148
MP3BT_ON
U61 NC7SZ125-U
MP3BT_ON#_1
MP3BT_ON# 24,25
MP3_PWRBTN# 34
R516 100KR3
12VGATE_S0
K3D-SC
Q22 2N7002
45,49 SHUTDOWN_S5
RB4
0R3-0-U
SHUTDOWN_S5
SD_S5
SD#_S5
U55D TSAHCT14
U49C TSAHCT32
AC_IN

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PWR CTL LOGIC / ADT / DC CONN***	
Size A3	Document Number Gannet	Rev -1
Date: Thursday, December 04, 2003	Sheet 43 of 51	


R31,BC16,R39,BC26
must close to R27
Rating 4A
DCBATOUT
Modify-0602
Modify-0612
J8-SC
Reduce total
power to 85%
J8-SC
added rating
J8-SC
Change new
J8-SC
Change new U11,U16
R18 = 30KR3F ,
R41 = 49K9R3F ,
R40 = 100KR3F,
CLS voltage = 2.56V ,
Total Power =
2.56A*20V = 64W(<65W)
0x12
K3D-SC
notice sense resistor noise and trace
MAX1645EEI
ATTINY12L-4SI
GAP-CLOSE
DUMMY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER CIRCUIT
Gannet
Size A3
Rev -1
Date: Thursday, December 04, 2003
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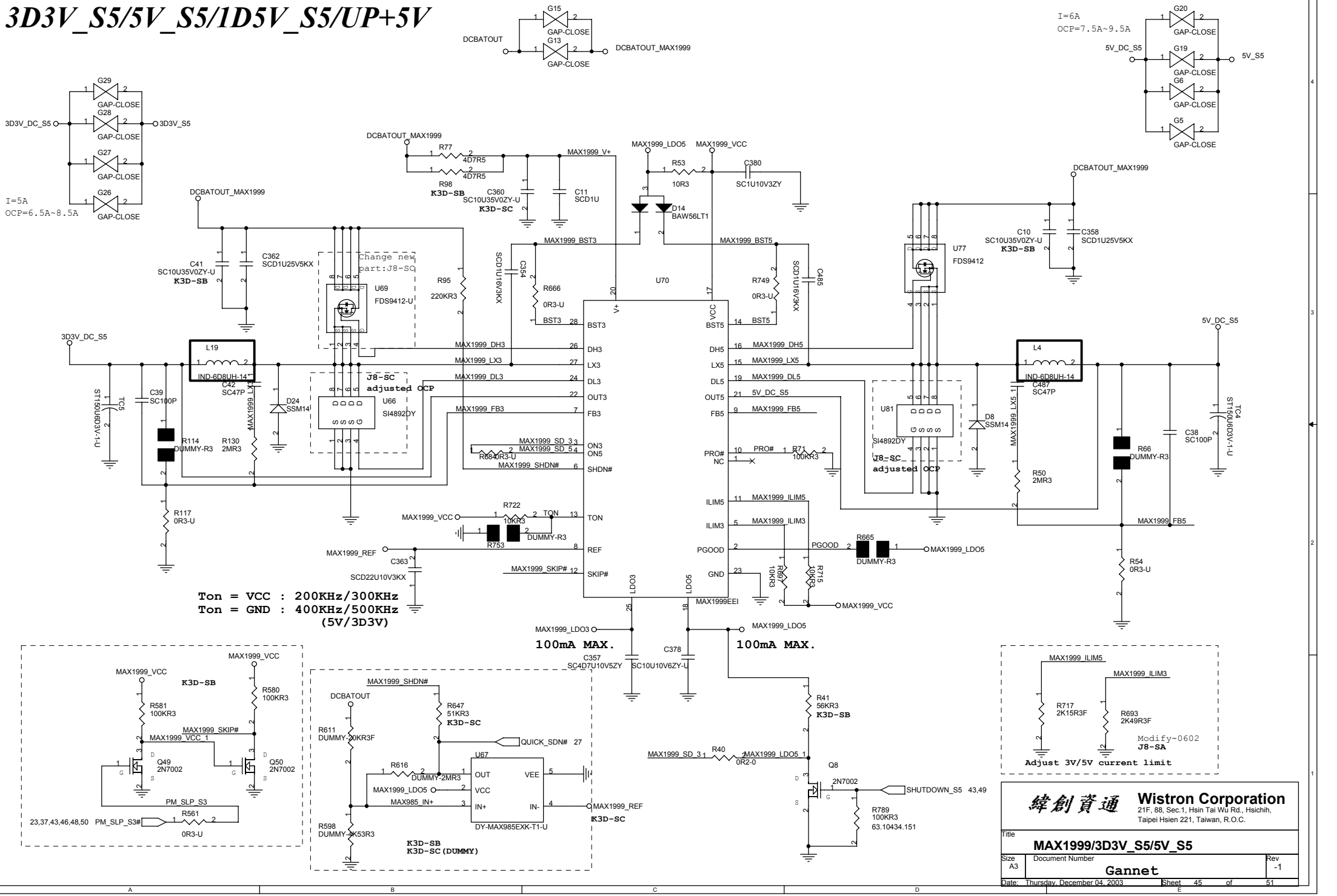
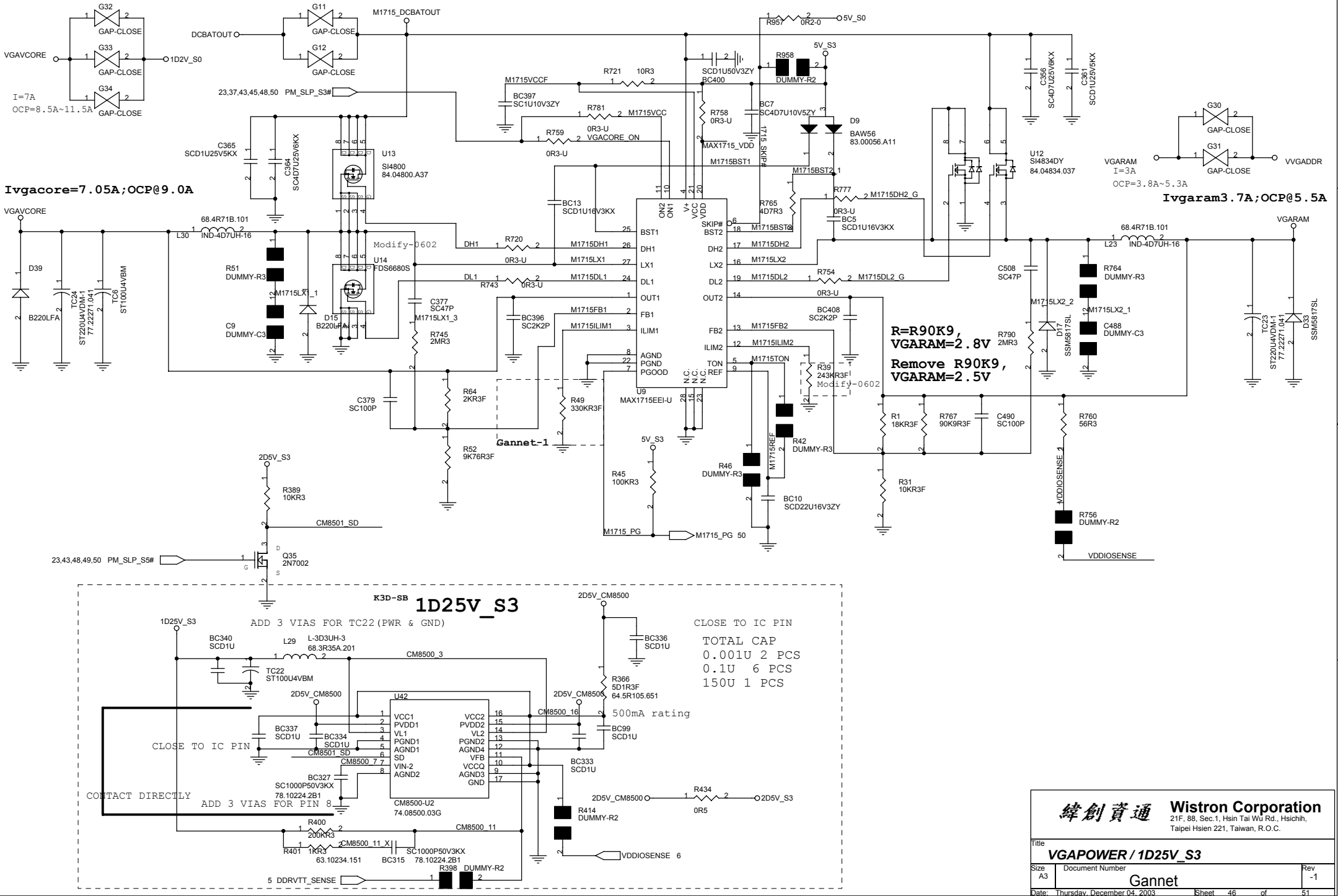
SYSTEM DC/DC
3D3V_S5/5V_S5/1D5V_S5/UP+5V



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**MAX1999/3D3V_S5/5V_S5**	
Size A3	Document Number **Gannet**	Rev -1
Date: Thursday, December 04, 2003	Sheet 45 of 51	

VGAPOWER / 1D25V_S0 / Charger Connector



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VGAPOWER / 1D25V_S3***	
Size A3	Document Number: Gannet	Rev: -1
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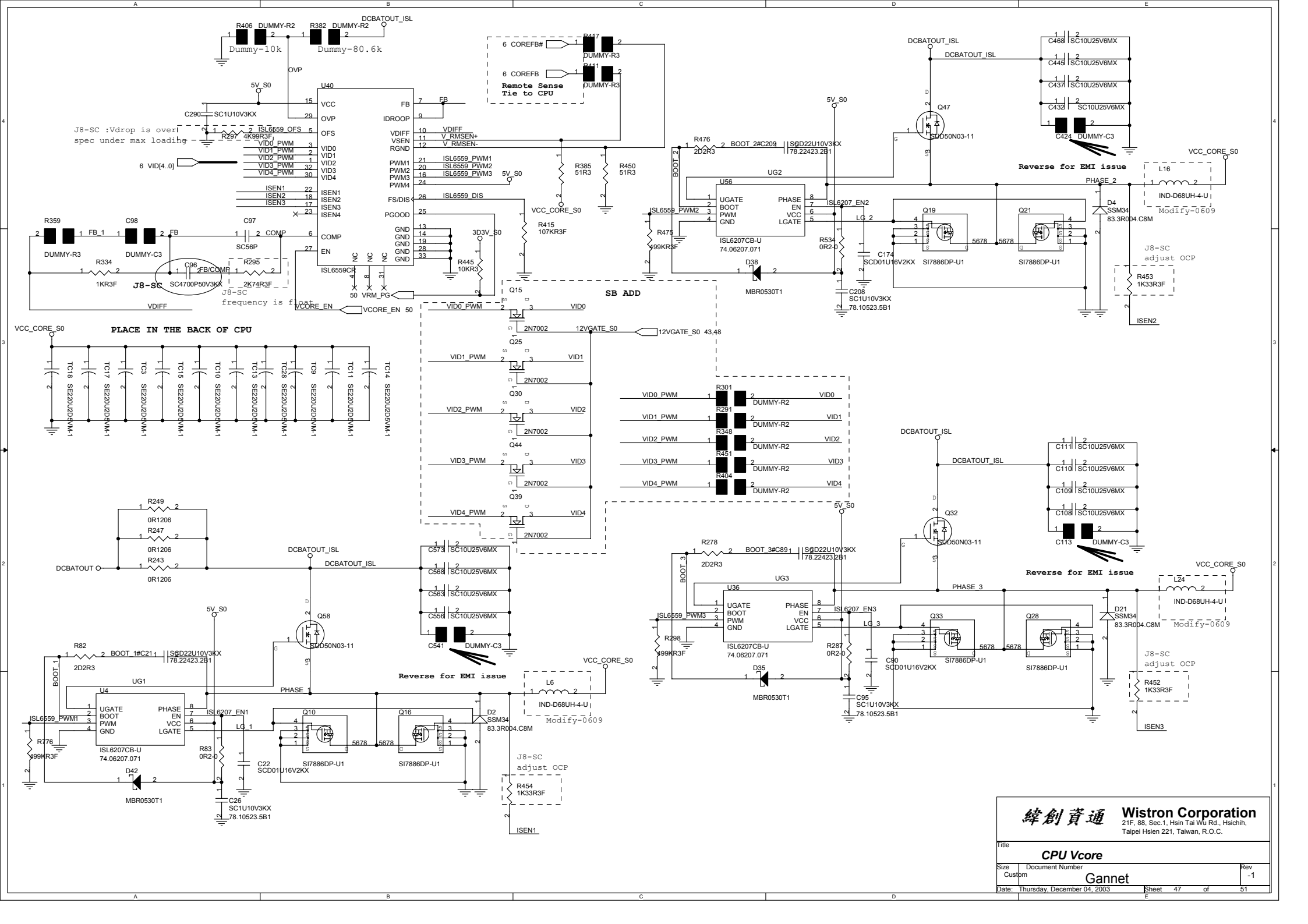

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Title: CPU Vcore	
Size: Custom	Document Number: Gannet
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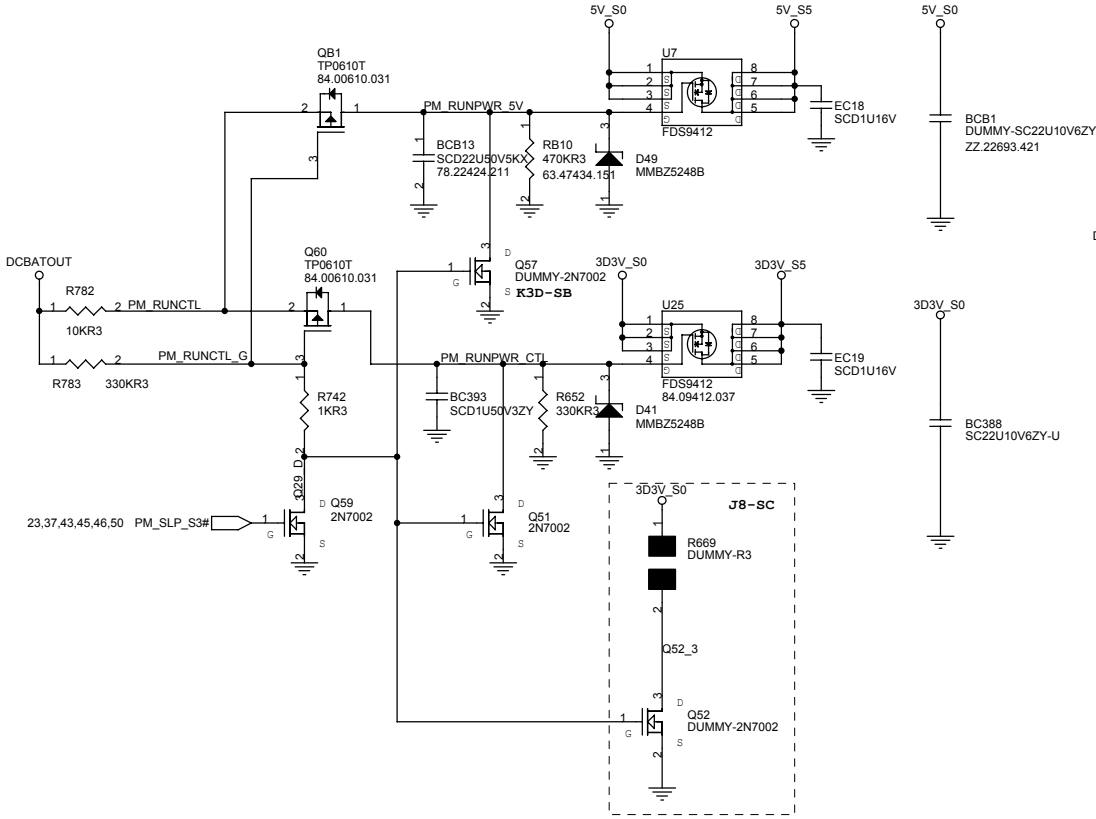

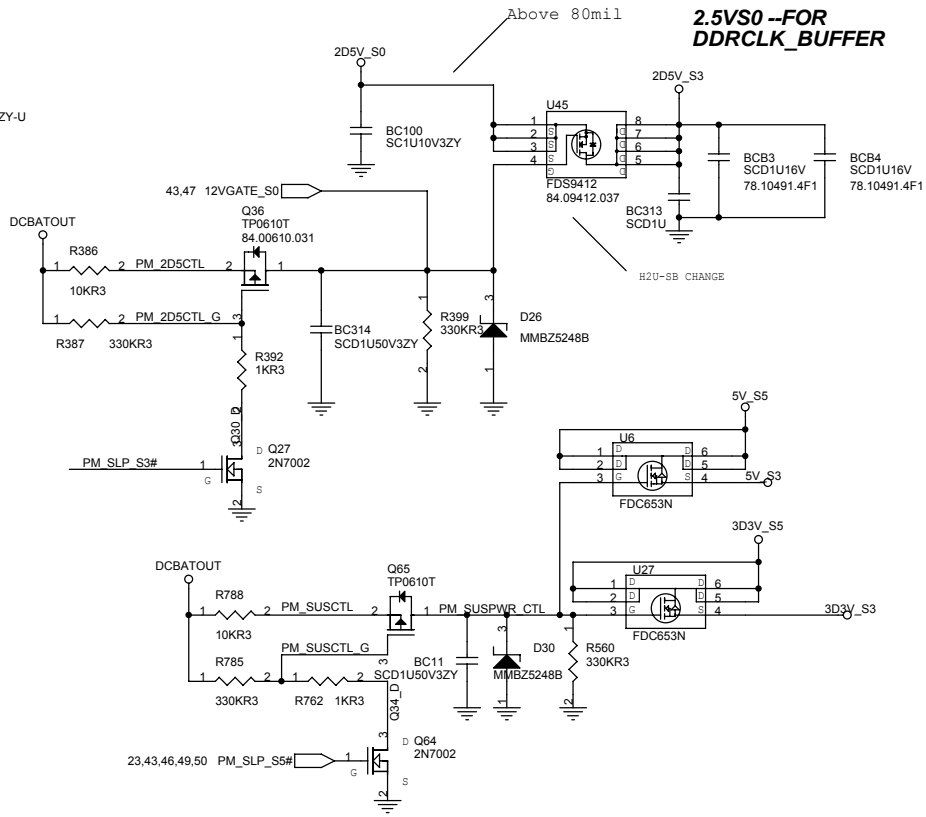

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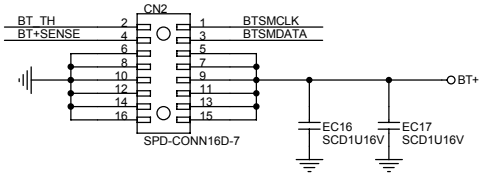
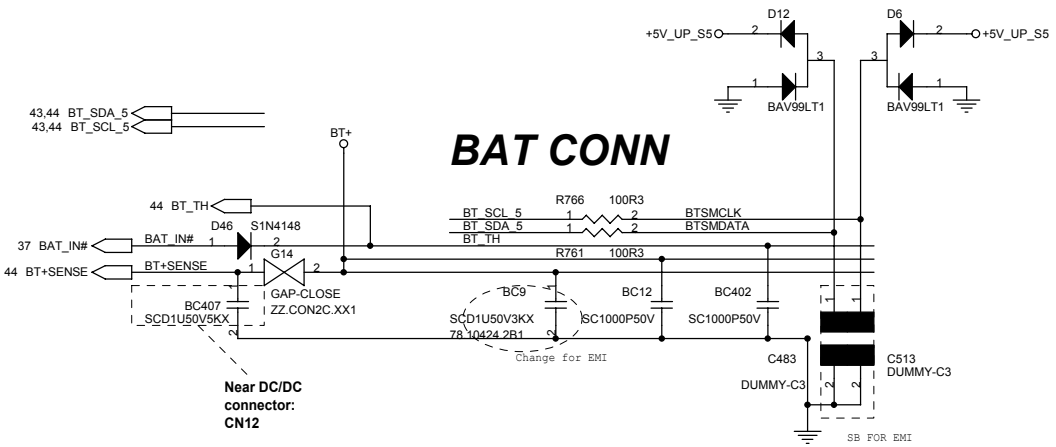


BAT CONN



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Title: DC/DC (1/2) -- 5V / 3.3V / 2.5V

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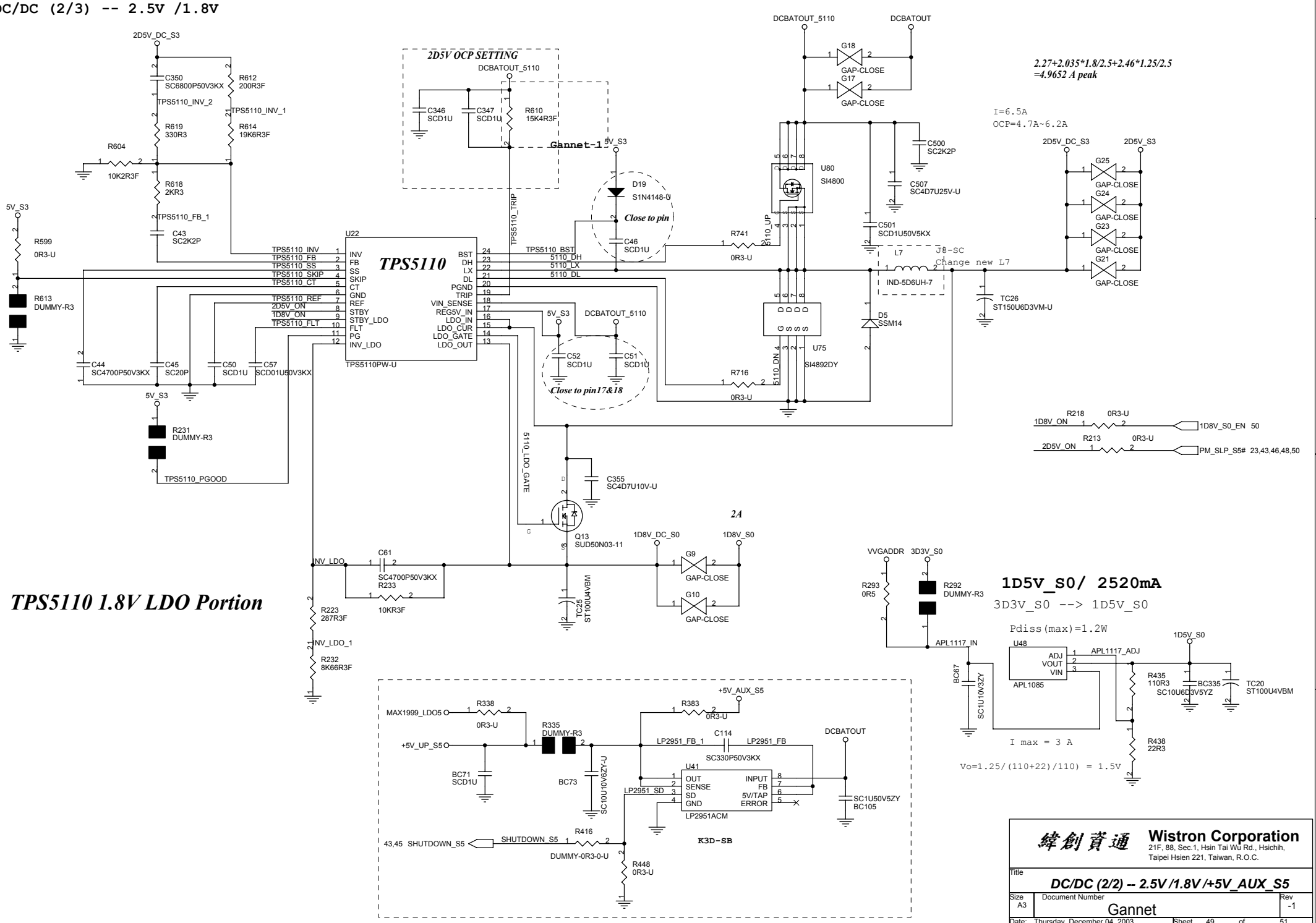
DC/DC (2/3) -- 2.5V /1.8V



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Title	DC/DC (2/2) -- 2.5V /1.8V /+5V_AUX_S5	
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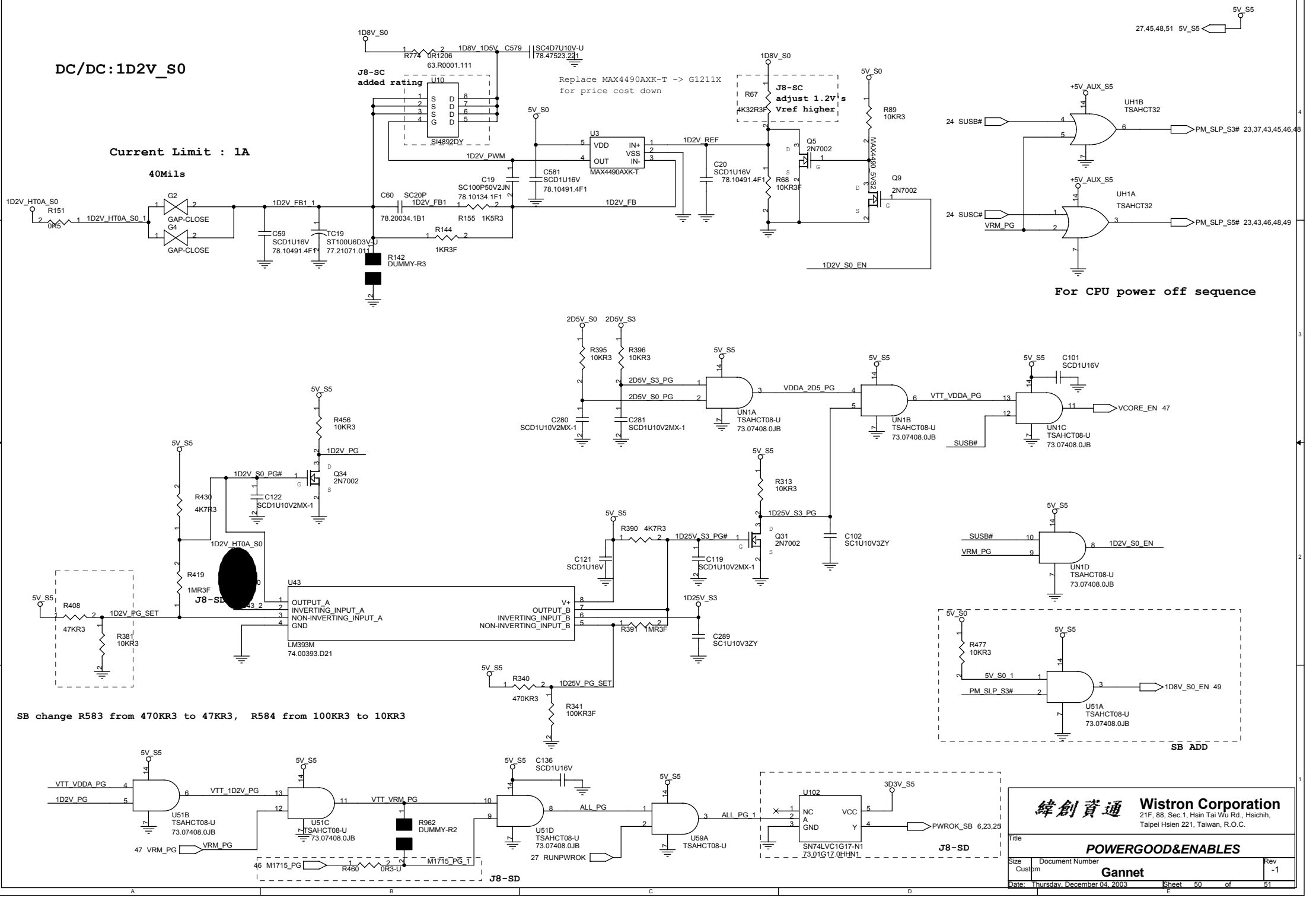
DC/DC:1D2V_S0

Current Limit : 1A

40Mils



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Title: ***POWERGOOD&ENABLES***

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Custom	Gannet	-1
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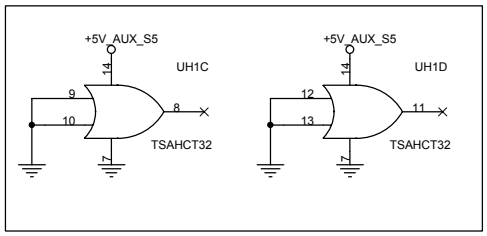

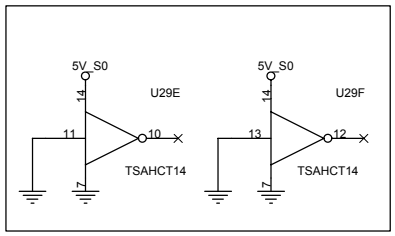

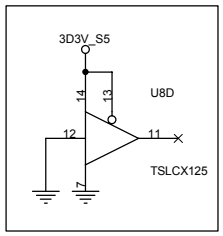

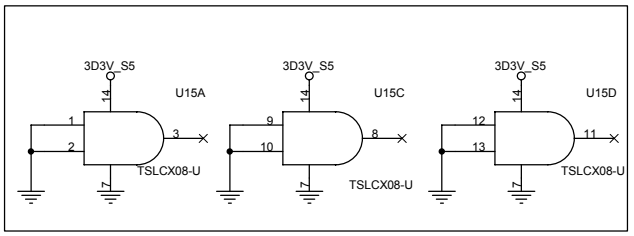

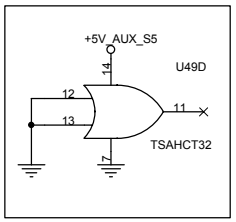

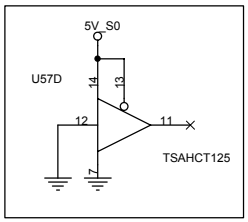

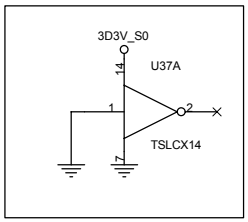

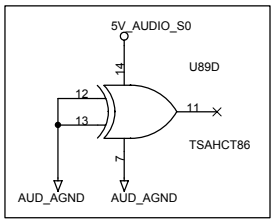

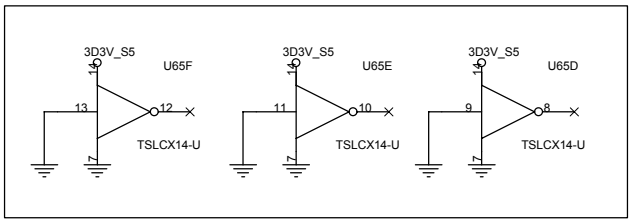

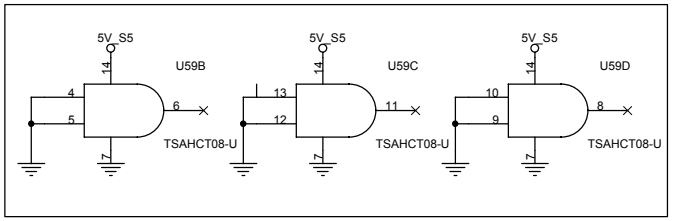

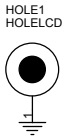

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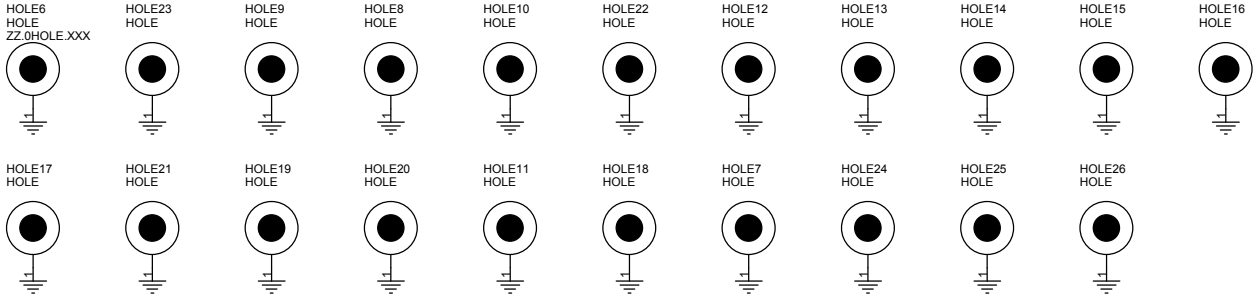
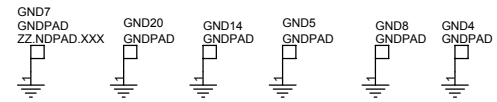
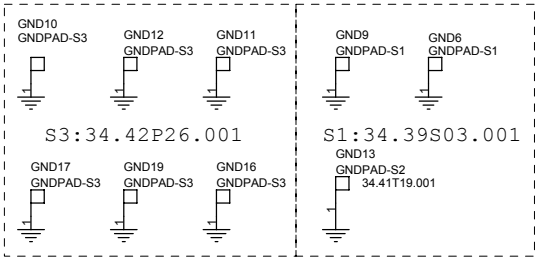
LCD Stand Off
P/N:
34.41T01.001

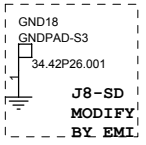
DC/DC Stand Off
P/N:
34.41T02.001

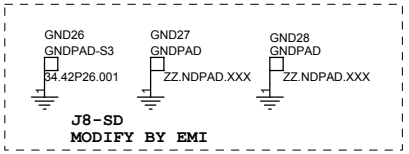
SPARE GATES











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Title: ***MISC***

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