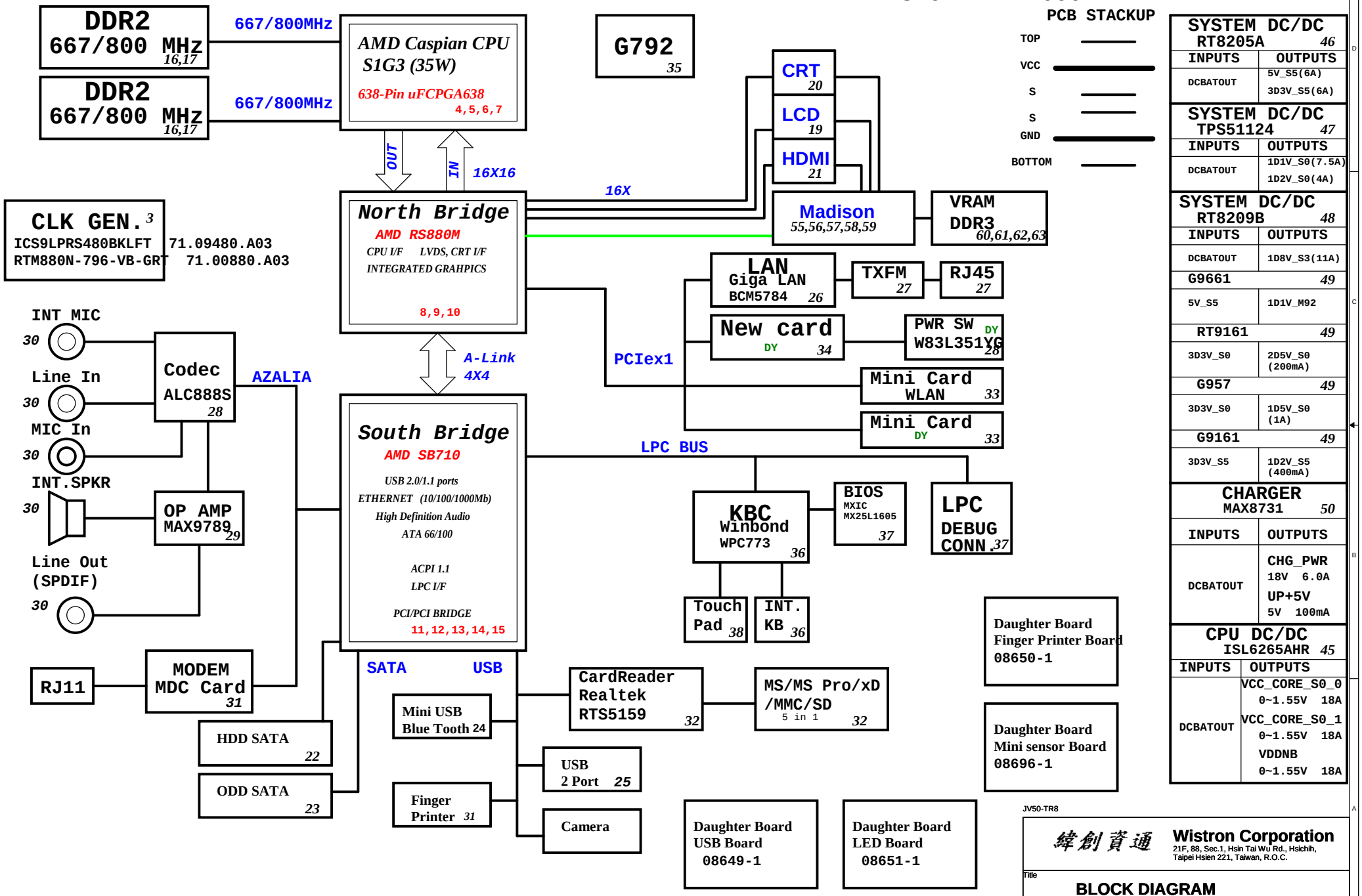
JV50-TR_8VRAM Block Diagram

Project code: 91.4FN01.001
PCB P/N : 48.4FN02.001
REVISION : 09927-1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8205A 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC RT8209B 48	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)
G9661 49	
5V_S5	1D1V_M92
RT9161 49	
3D3V_S0	2D5V_S0 (200mA)
G957 49	
3D3V_S0	1D5V_S0 (1A)
G9161 49	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 05, 2009 Sheet 1 of 63

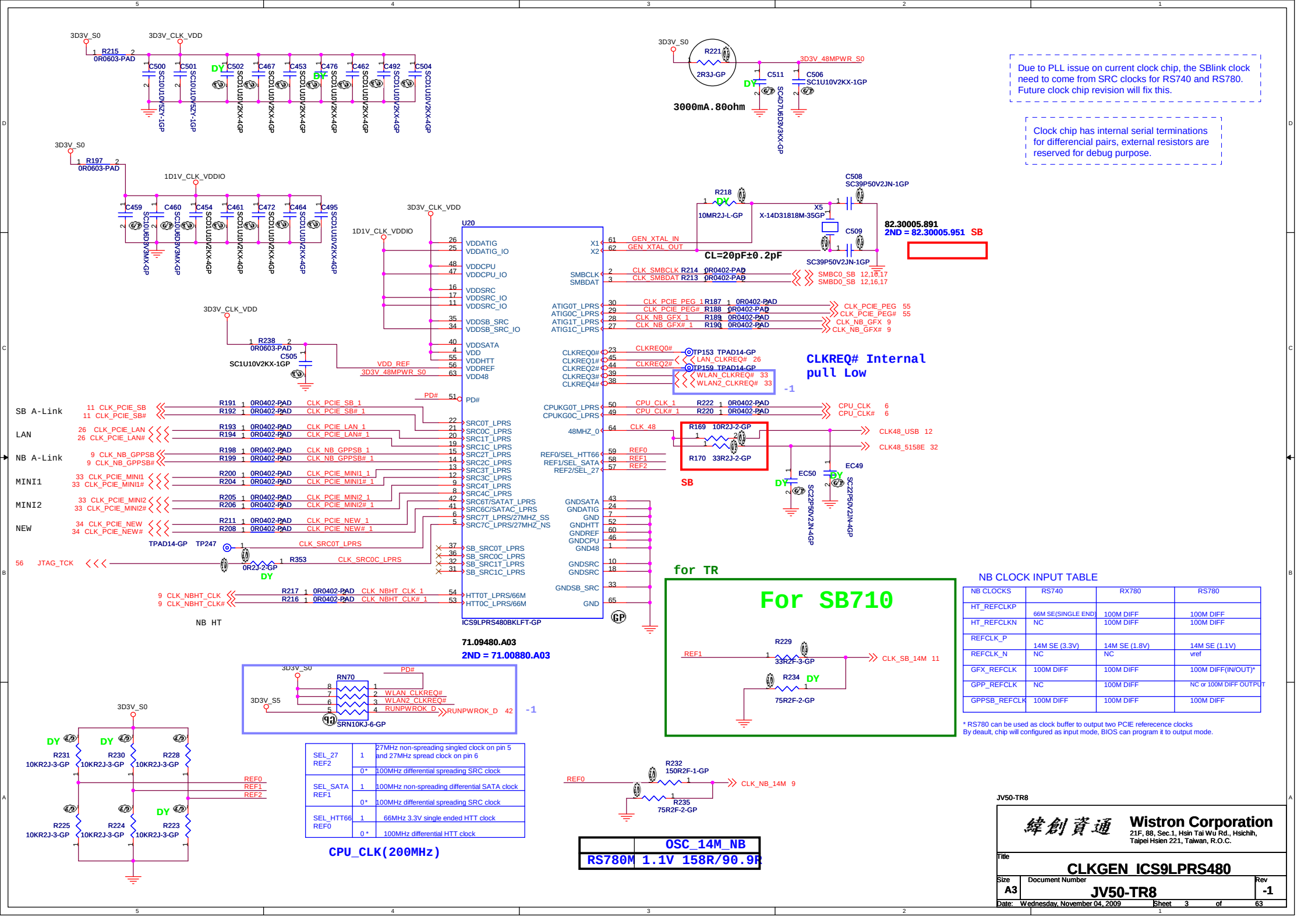
JV50-TR8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB/PCIE Routing**

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 05, 2009 Sheet 2 of 63



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

JV50-TR8

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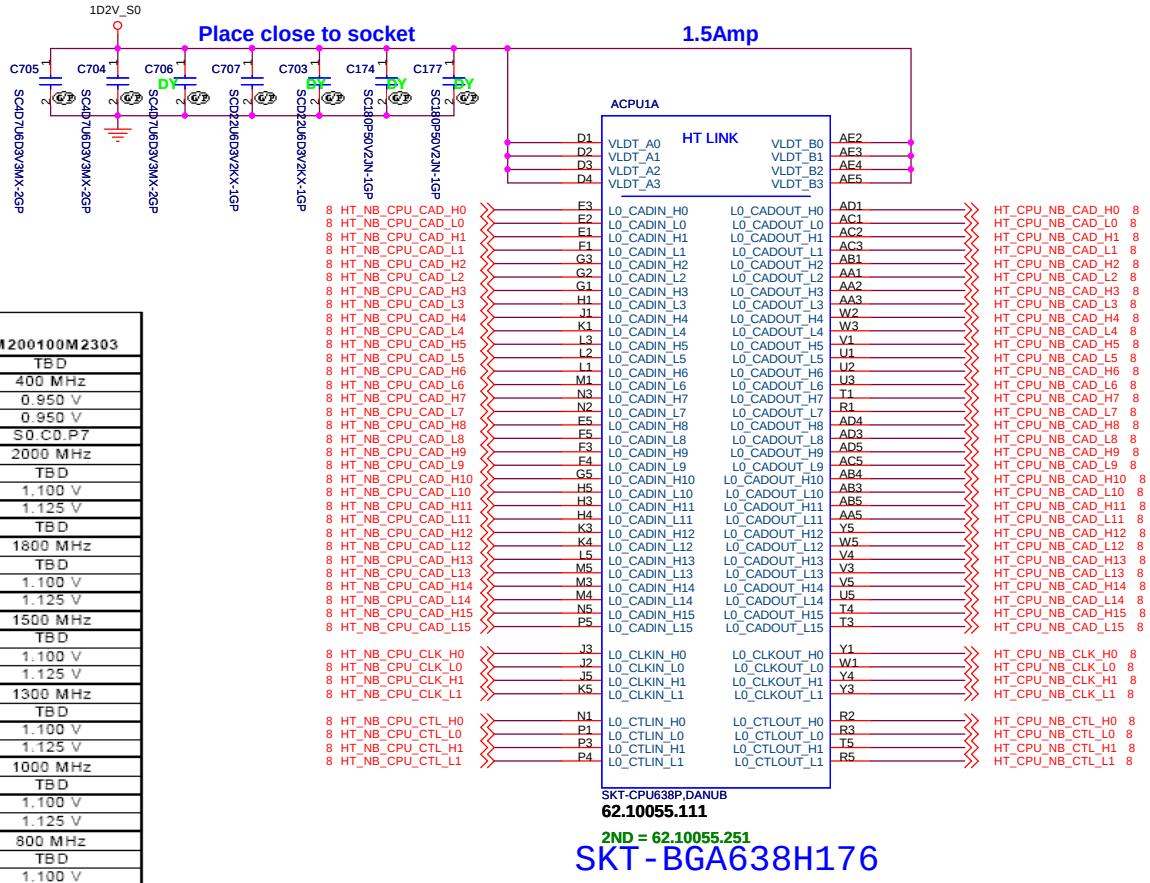
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS9LPRS480

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Wednesday, November 04, 2009 Sheet 3 of 63



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

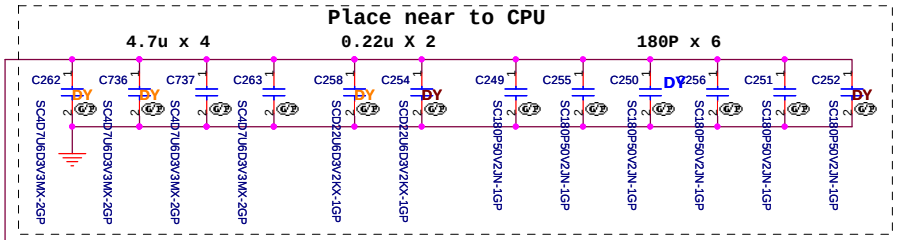
JV50-TR8

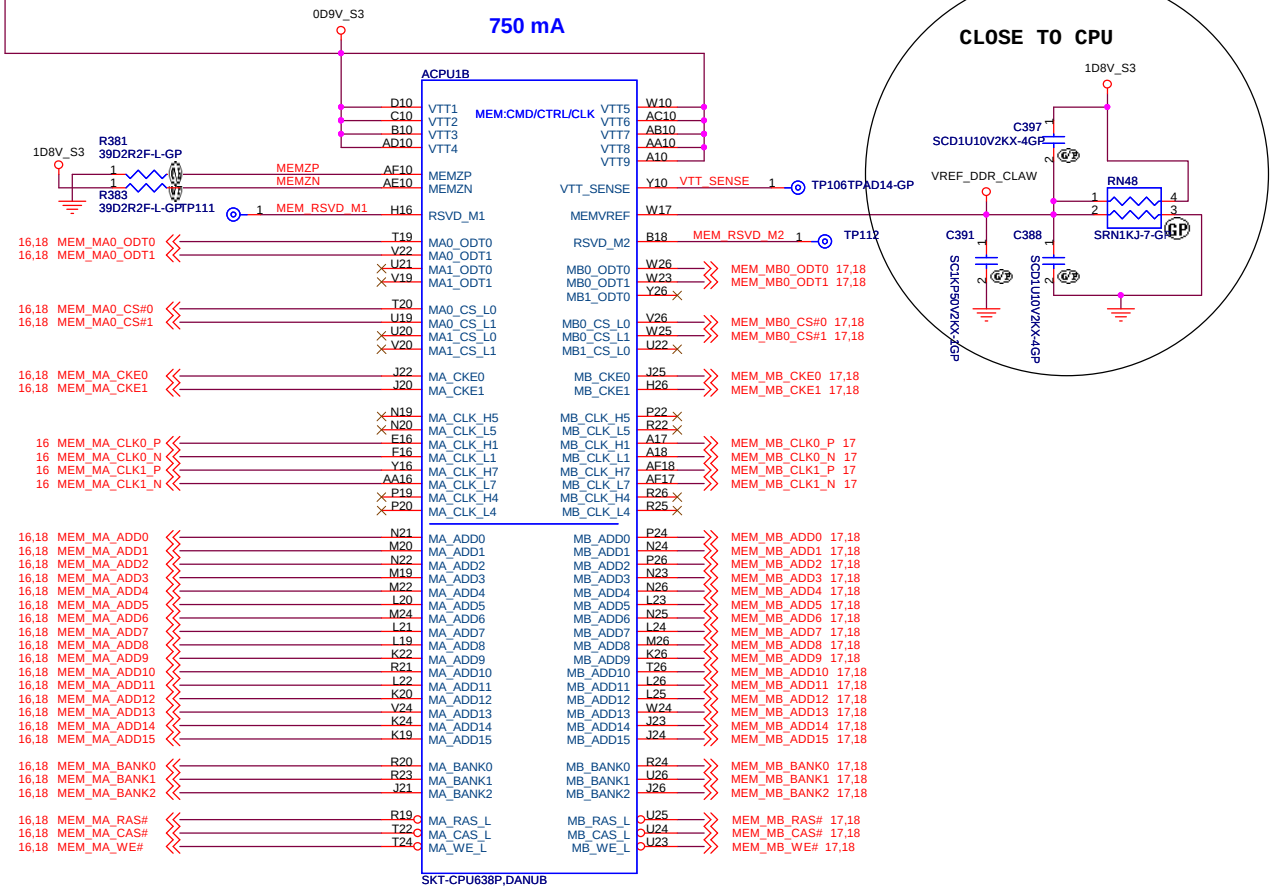
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_HT_LINK I/F (1/4)

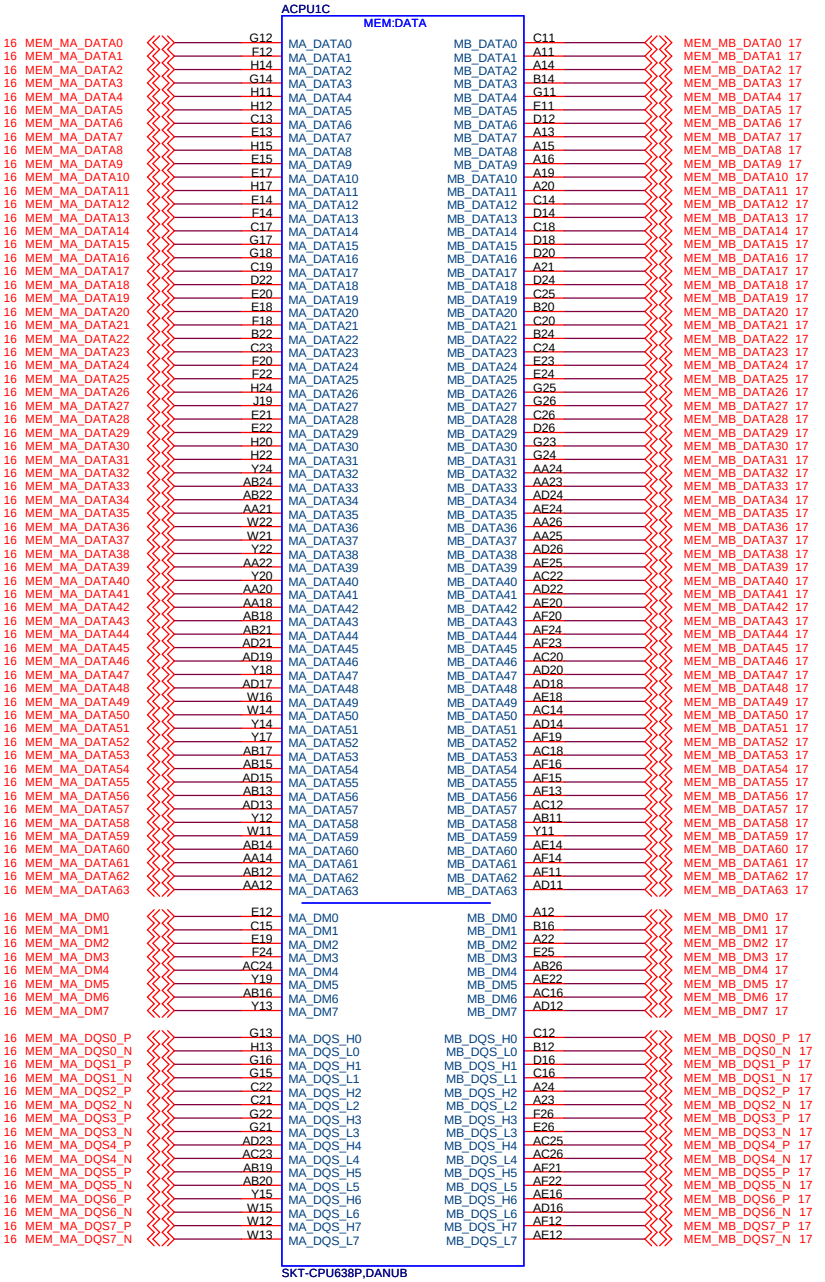
Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 4 of 63





62.10055.111



JV50-TR8

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU_DDR_(2/4)		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 5 of 63	

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

for TR

for TR

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

Near CPU PIN

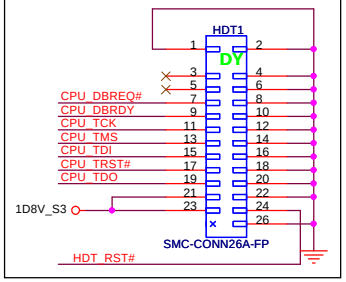
-1_20091021

CPU exceeds to 125℃

84.T3904.C11
2ND = 84.03904.L06

SKT-CPU638P,DANUB

HDT Connectors



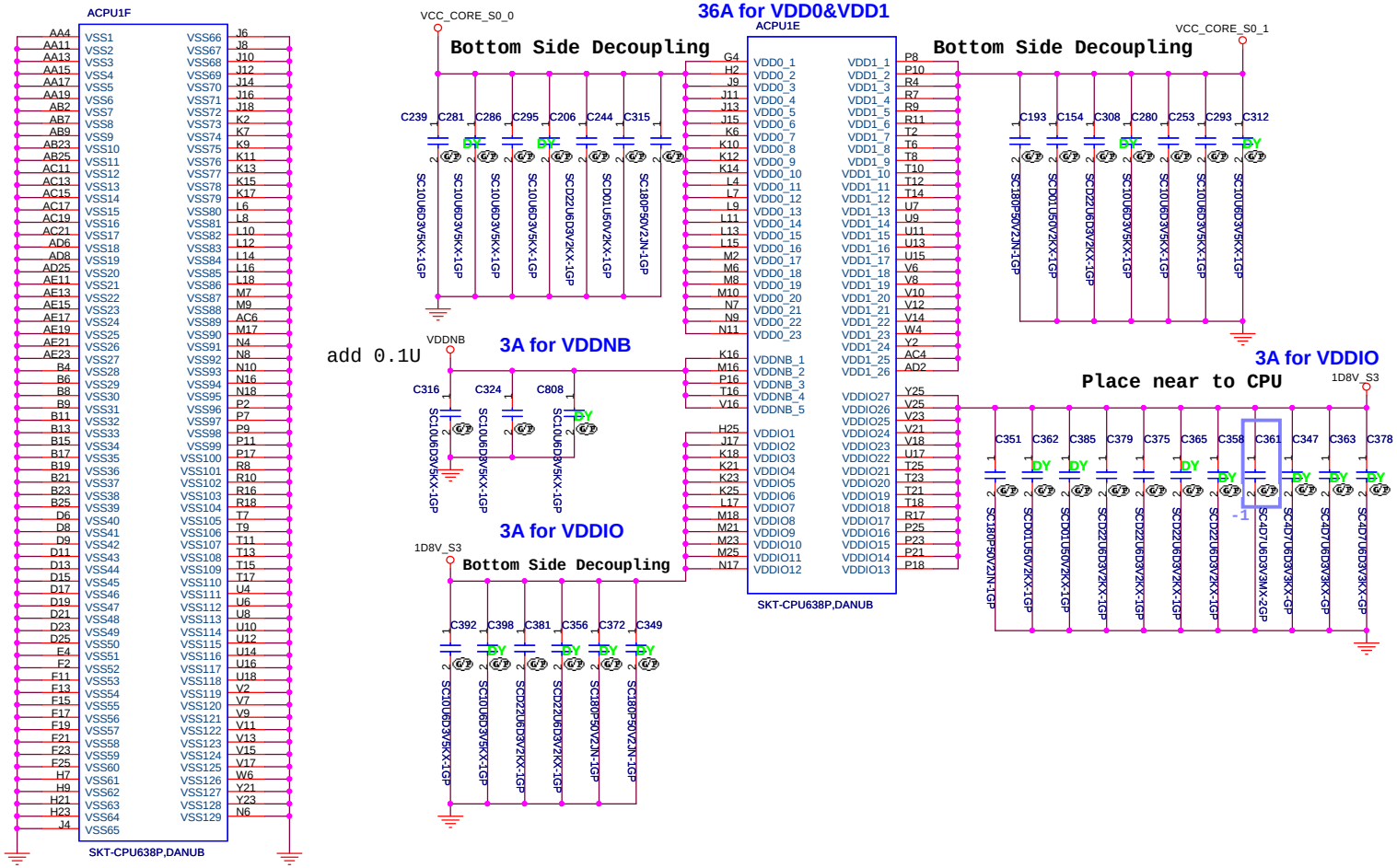
JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)

Size	Document Number	Rev
A3	JV50-TR8	-1

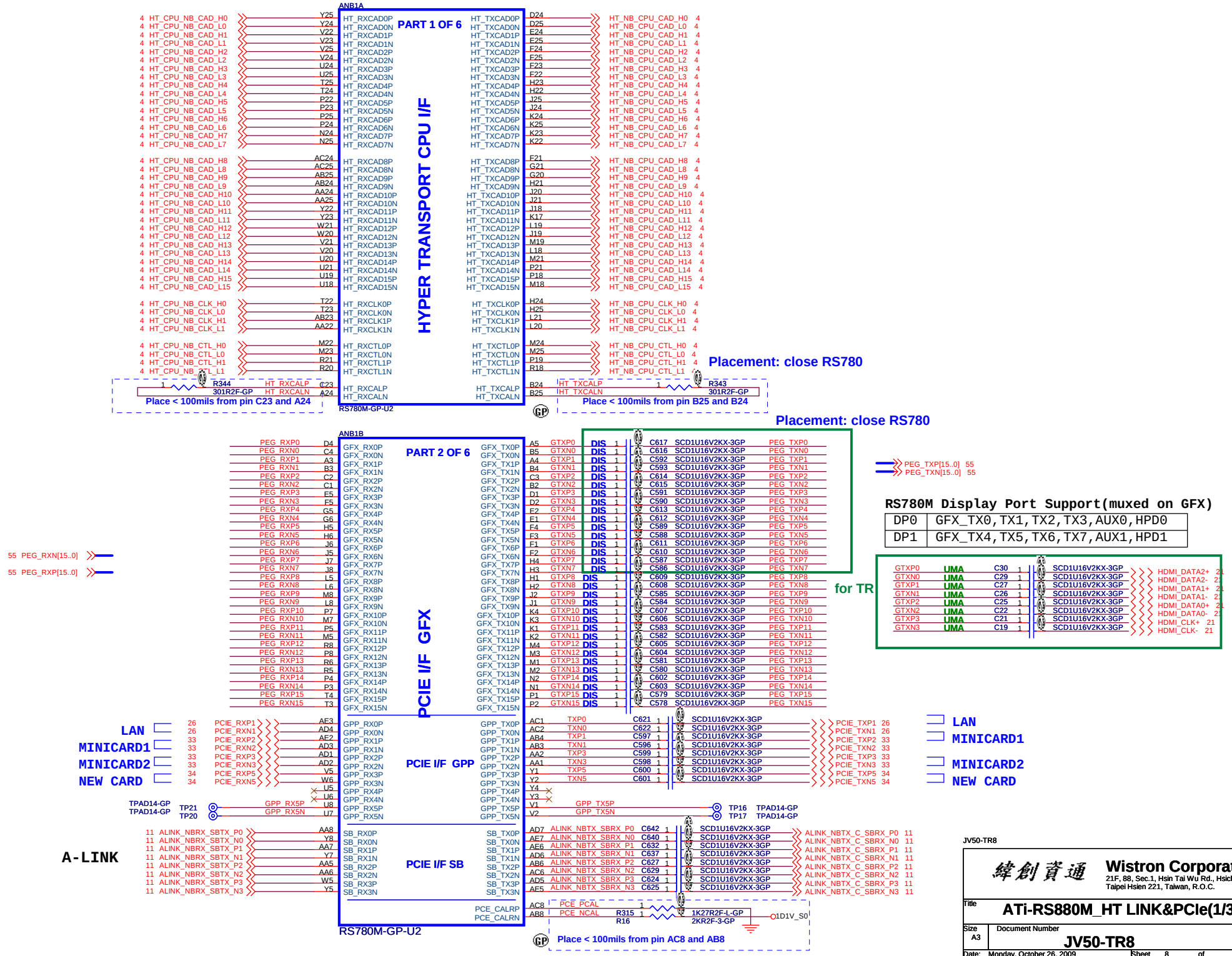
Date: Monday, October 26, 2009 Sheet 6 of 63

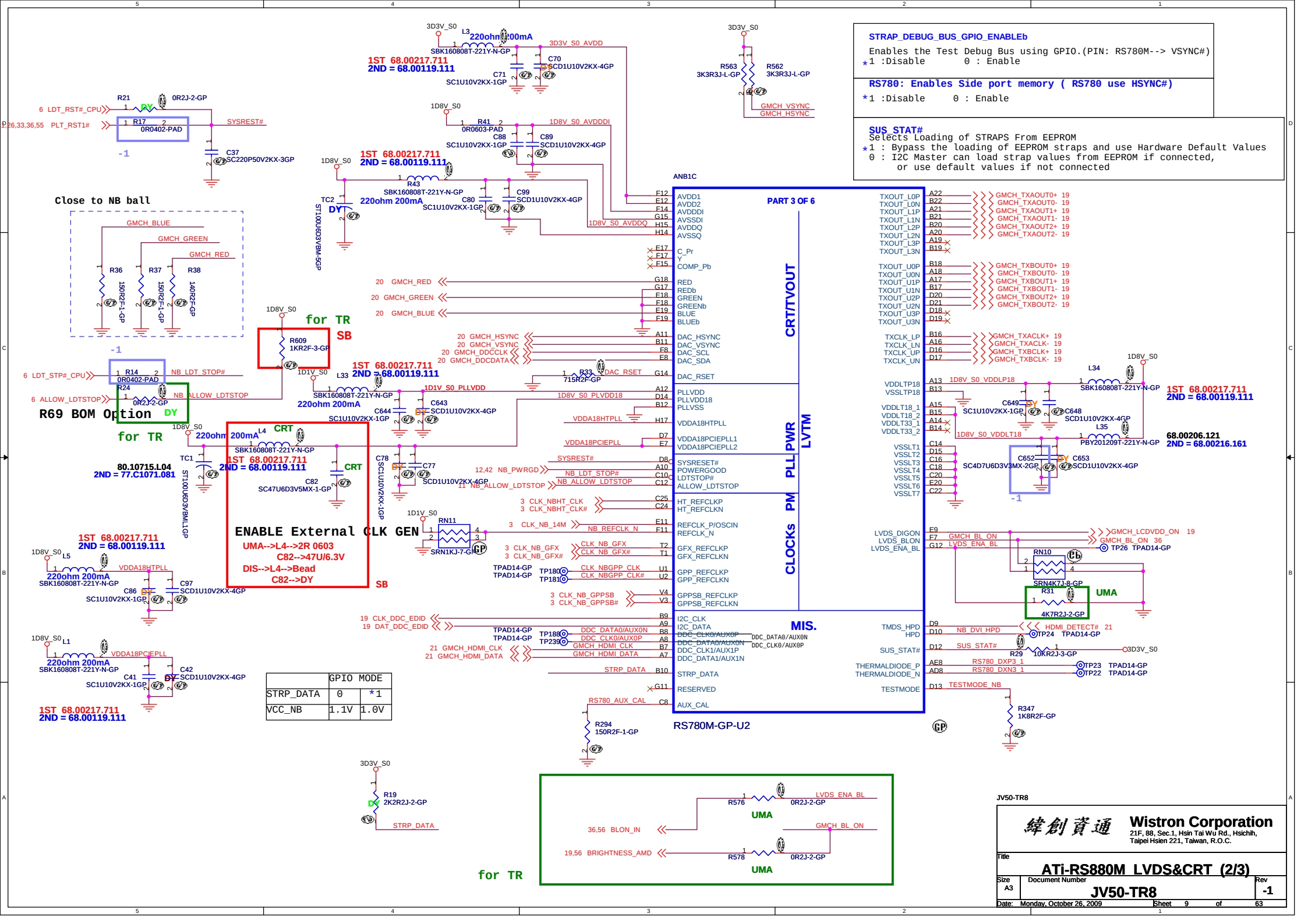


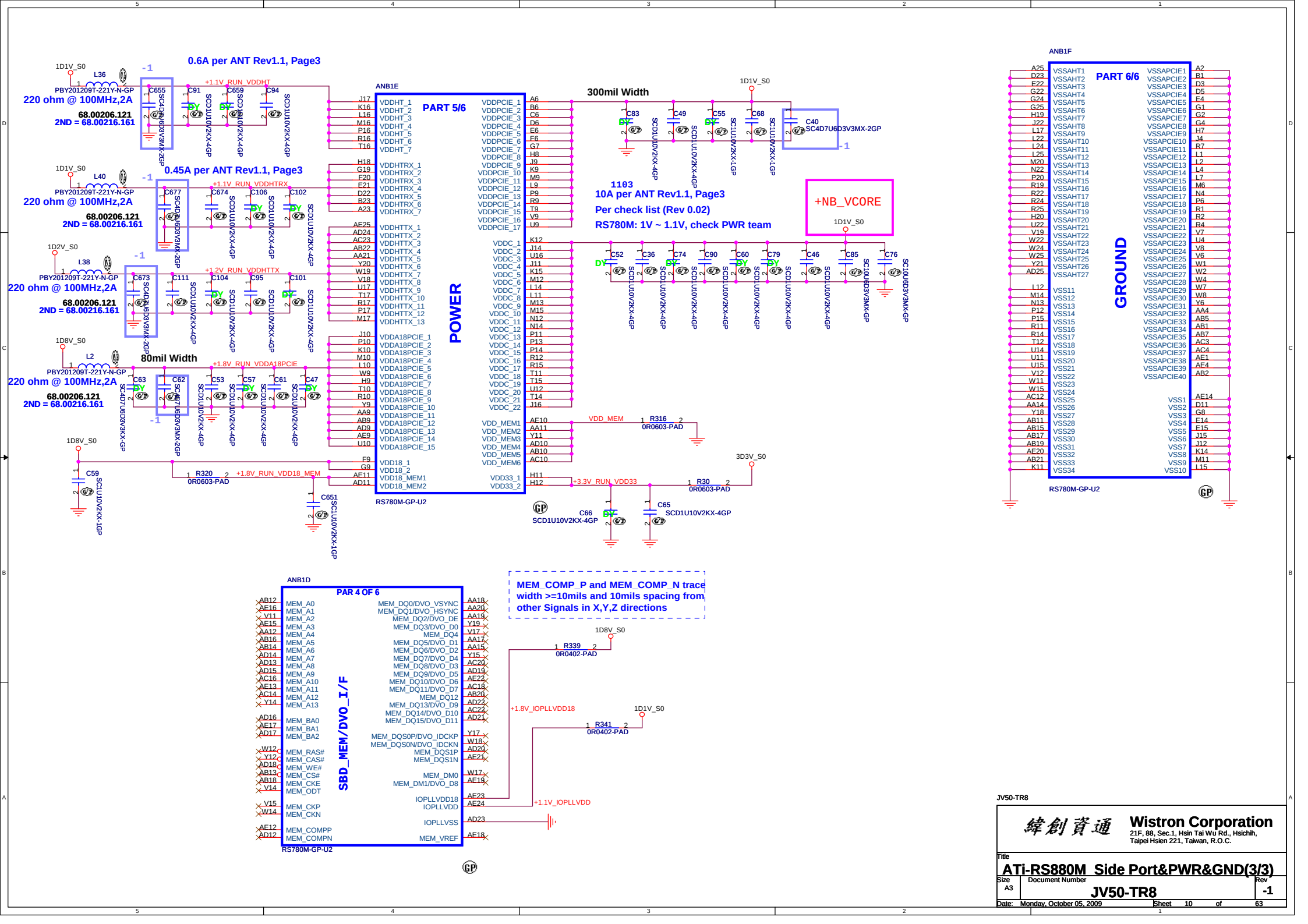
JV50-TR8

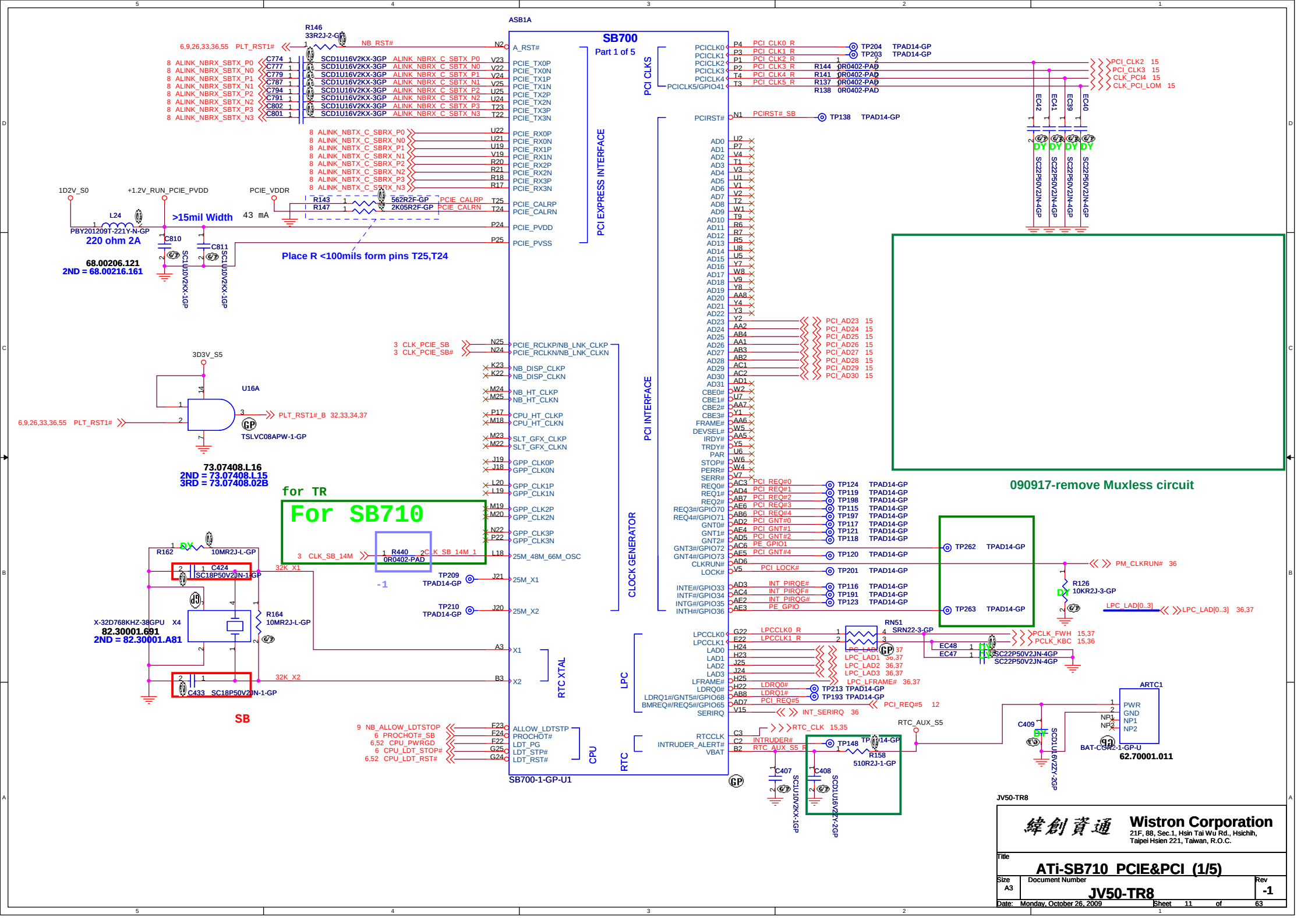
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

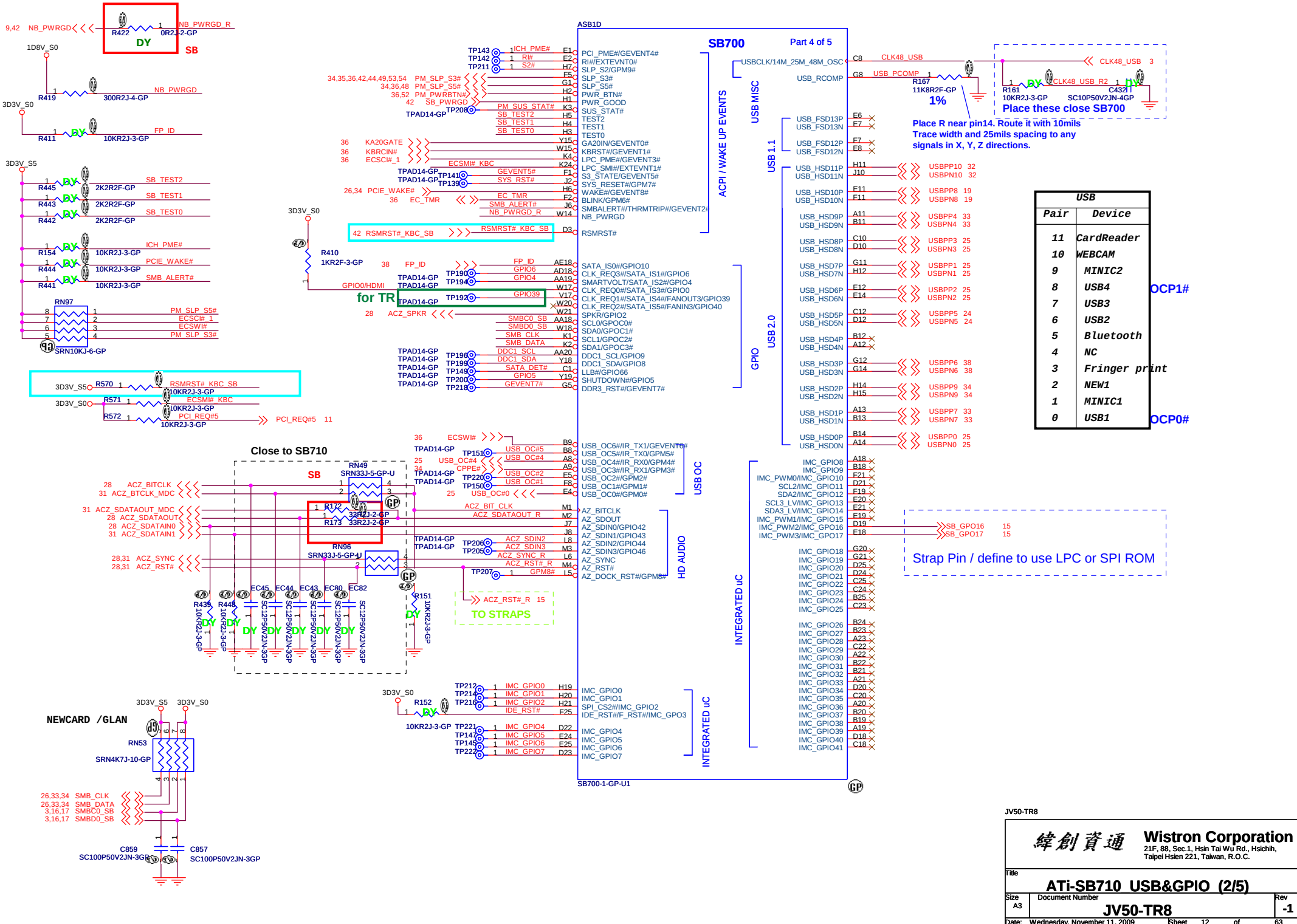
Title	CPU_Power_(4/4)	
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 05, 2009	Sheet 7 of 63	


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Placement: close RS780
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
R344 301R2F-GP
R343 301R2F-GP
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
for TR
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
LAN
MINICARD1
MINICARD2
NEW CARD
A-LINK
Place < 100mils from pin AC8 and AB8
R315 1K27R2F-L-GP
R16 2KR2F-3-GP
1D1V_S0
JV50-TR8
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_HT LINK&PCIe(1/3)
Size A3
Document Number JV50-TR8
Rev -1
Date: Monday, October 26, 2009
Sheet 8 of 63


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
Close to NB ball
R69 BOM Option
for TR
ENABLE External CLK GEN
UMA-->L4-->2R 0603
C82-->47U/6.3V
DIS-->L4-->Bead
C82-->DY
SB
ANB1C
PART 3 OF 6
CRT/TVOUT
PLL/PWR
LVTM
CLOCKs
PM
MIS.
RS780M-GP-U2
GPIO MODE
STRP_DATA 0 *1
VCC_NB 1.1V 1.0V
UMA
for TR
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M LVDS&CRT (2/3)
Size A3
Document Number JV50-TR8
Rev -1
Date: Monday, October 26, 2009
Sheet 9 of 63


0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
1103
10A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
ANB1E
PART 5/6
POWER
RS780M-GP-U2
ANB1F
PART 6/6
GROUND
RS780M-GP-U2
ANB1D
PAR 4 OF 6
SBD_MEM/DVO_I/F
RS780M-GP-U2
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
220 ohm @ 100MHz,2A
68.00206.121
2ND = 68.00216.161
+1.1V_RUN_VDDHT
+1.1V_RUN_VDDHTRX
+1.2V_RUN_VDDHTTX
+1.8V_RUN_VDDA18PCIE
+1.8V_RUN_VDD18_MEM
+3.3V_RUN_VDD33
VDD_MEM
+1.8V_IOPLLVDD18
+1.1V_IOPLLVDD
1D1V_S0
1D2V_S0
1D8V_S0
3D3V_S0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
JV50-TR8
ATi-RS880M_Side Port&PWR&GND(3/3)
Size A3
Document Number JV50-TR8
Rev -1
Date: Monday, October 05, 2009
Sheet 10 of 63


ASB1A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB700-1-GP-U1
R146 33R2J-2-GP
NB_RST#
PLT_RST1#
6,9,26,33,36,55
SCD1U16V2KX-3GP
ALINK_NBRX_C_SBTX_P0
ALINK_NBRX_C_SBTX_N0
ALINK_NBRX_C_SBTX_P1
ALINK_NBRX_C_SBTX_N1
ALINK_NBRX_C_SBTX_P2
ALINK_NBRX_C_SBTX_N2
ALINK_NBRX_C_SBTX_P3
ALINK_NBRX_C_SBTX_N3
ALINK_NBTX_C_SBRX_P0
ALINK_NBTX_C_SBRX_N0
ALINK_NBTX_C_SBRX_P1
ALINK_NBTX_C_SBRX_N1
ALINK_NBTX_C_SBRX_P2
ALINK_NBTX_C_SBRX_N2
ALINK_NBTX_C_SBRX_P3
ALINK_NBTX_C_SBRX_N3
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
1D2V_S0
+1.2V_RUN_PCIE_PVDD
PCIE_VDDR
L24
PBY201209T-221Y-N-GP
220 ohm 2A
>15mil Width
43 mA
R143 562R2F-GP
R147 2K05R2F-GP
PCIE_CALRP
PCIE_CALRN
PCIE_PVDD
PCIE_PVSS
C810
C811
SC1U10V2KX-1GP
68.00206.121
2ND = 68.00216.161
Place R <100mils form pins T25,T24
3D3V_S5
U16A
TSLVC08APW-1-GP
PLT_RST1#_B 32,33,34,37
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
CLK_PCIE_SB
CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
for TR
For SB710
CLK_SB_14M
R440 0R0402-PAD
CLK_SB_14M_1
25M_48M_66M_OSC
25M_X1
25M_X2
TP209 TPAD14-GP
TP210 TPAD14-GP
R162 10MR2J-L-GP
C424 SC18P50V2JN-1GP
32K_X1
32K_X2
X-32D768KHZ-38GPU X4
82.30001.691
2ND = 82.30001.A81
R164 10MR2J-L-GP
C433 SC18P50V2JN-1-GP
SB
X1
X2
ALLOW_LDTSTP
PROCHOT#_SB
CPU_PWRGD
CPU_LDT_STOP#
CPU_LDT_RST#
LDT_PG
LDT_STP#
LDT_RST#
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCI_CLK0_R
PCI_CLK1_R
PCI_CLK2_R
PCI_CLK3_R
PCI_CLK4_R
PCI_CLK5_R
TP204 TPAD14-GP
TP203 TPAD14-GP
R144 0R0402-PAD
R141 0R0402-PAD
R137 0R0402-PAD
R138 0R0402-PAD
PCI_CLK2 15
PCI_CLK3 15
CLK_PCI4 15
CLK_PCI_LOM 15
EC42
EC41
EC39
EC40
SC22P50V2JN-4GP
PCIRST#
PCIRST#_SB
TP138 TPAD14-GP
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
PCI_AD23 15
PCI_AD24 15
PCI_AD25 15
PCI_AD26 15
PCI_AD27 15
PCI_AD28 15
PCI_AD29 15
PCI_AD30 15
CBE0#
CBE1#
CBE2#
CBE3#
FRAME#
DEVSEL#
IRDY#
TRDY#
PAR
STOP#
PERR#
SERR#
REQ0#
REQ1#
REQ2#
REQ3#/GPIO70
REQ4#/GPIO71
GNT0#
GNT1#
GNT2#
GNT3#/GPIO72
GNT4#/GPIO73
CLKRUN#
LOCK#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_REQ#4
PCI_GNT#0
PCI_GNT#1
PCI_GNT#2
PE_GPIO1
PCI_GNT#4
PCI_LOCK#
TP124 TPAD14-GP
TP119 TPAD14-GP
TP198 TPAD14-GP
TP115 TPAD14-GP
TP197 TPAD14-GP
TP117 TPAD14-GP
TP121 TPAD14-GP
TP118 TPAD14-GP
TP120 TPAD14-GP
TP201 TPAD14-GP
TP262 TPAD14-GP
TP263 TPAD14-GP
PM_CLKRUN# 36
R126 10KR2J-3-GP
LPC_LAD[0..3]
INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
PE_GPIO
TP116 TPAD14-GP
TP191 TPAD14-GP
TP123 TPAD14-GP
LPCCLK0
LPCCLK1
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#/GNT5#/GPIO68
BMREQ#/REQ5#/GPIO65
SERIRQ
LPCCLK0_R
LPCCLK1_R
RN51 SRN22-3-GP
PCLK_FWH 15,37
PCLK_KBC 15,36
EC48
EC47
SC22P50V2JN-4GP
LPC_LAD0 36,37
LPC_LAD1 36,37
LPC_LAD2 36,37
LPC_LAD3 36,37
LPC_LFRAME# 36,37
LDRQ0#
LDRQ1#
PCI_REQ#5
TP213 TPAD14-GP
TP193 TPAD14-GP
INT_SERIRQ 36
PCI_REQ#5 12
RTCCLK
INTRUDER_ALERT#
VBAT
RTC_CLK 15,35
INTRUDER#
RTC_AUX_S5_R
TP148 TPAD14-GP
R158 510R2J-1-GP
RTC_AUX_S5
C407 SC1U10V2KX-1GP
C408 SCD1U16V2ZY-2GP
C409 SCD1U16V2ZY-2GP
ARTC1
PWR
GND
NP1
NP2
BAT-CON2-1-GP-U
62.70001.011
090917-remove Muxless circuit
JV50-TR8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 PCIE&PCI (1/5)
Size A3
Document Number JV50-TR8
Rev -1
Date: Monday, October 26, 2009
Sheet 11 of 63



JV50-TR8

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**ATi-SB710 USB&GPIO (2/5)**	
Size A3	Document Number **JV50-TR8**	Rev **-1**
Date: Wednesday, November 11, 2009	Sheet 12 of 63	

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB710

SATA HDD
SATA ODD

SB700
Part 2 of 5
ASB1B
SB700-1-GP-U1

SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR

Very Close to SB710

1ST 82.30020.851
2ND = 82.30020.791
SB

93 mA

>15mil Width

Dummy CKG select

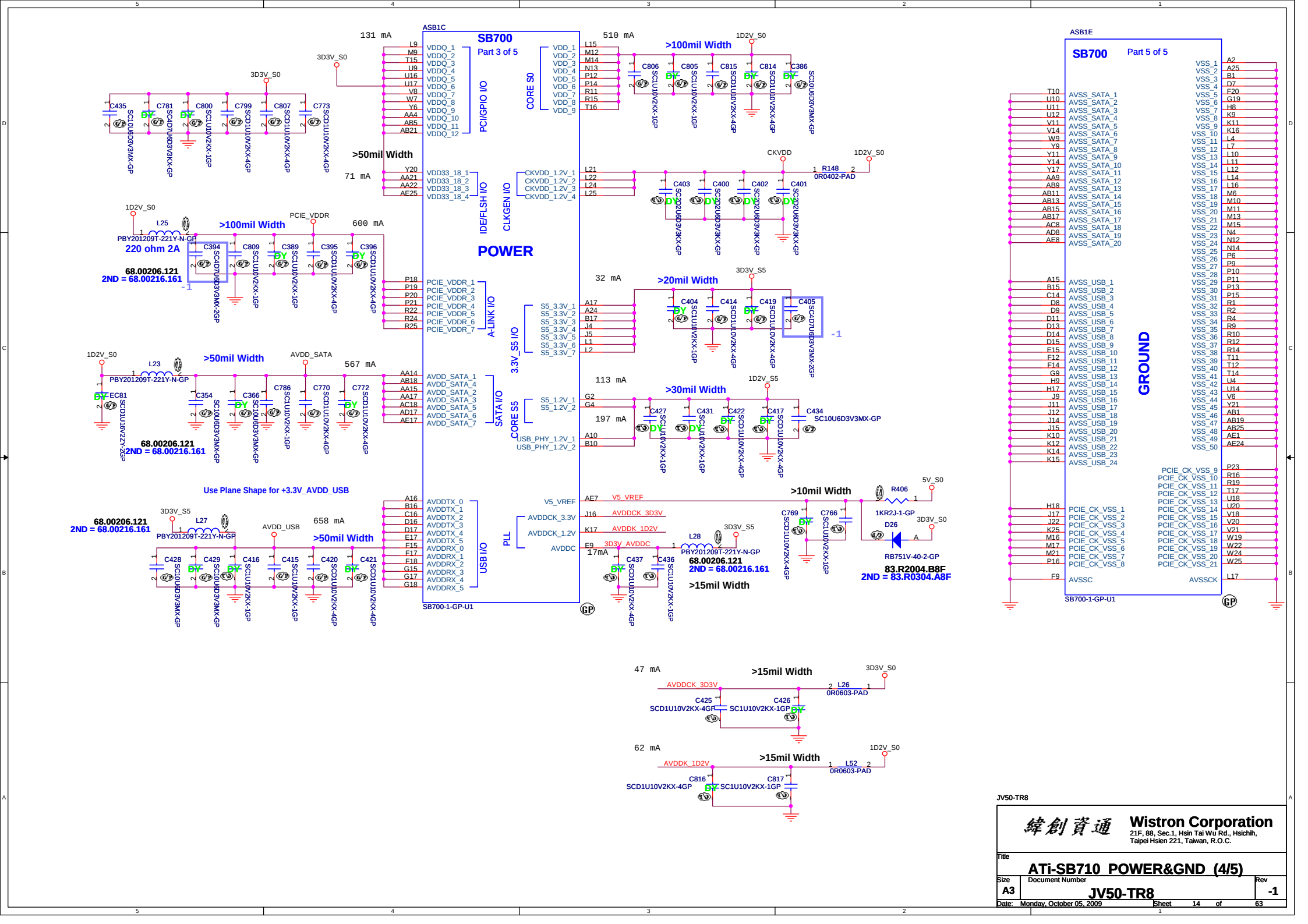
CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

Layout connect to Cap then GND

JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 SATA-IDE (3/5)
Size: A3
Document Number: JV50-TR8
Rev: -1
Date: Monday, October 26, 2009
Sheet 13 of 63



JV50-TR8

緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

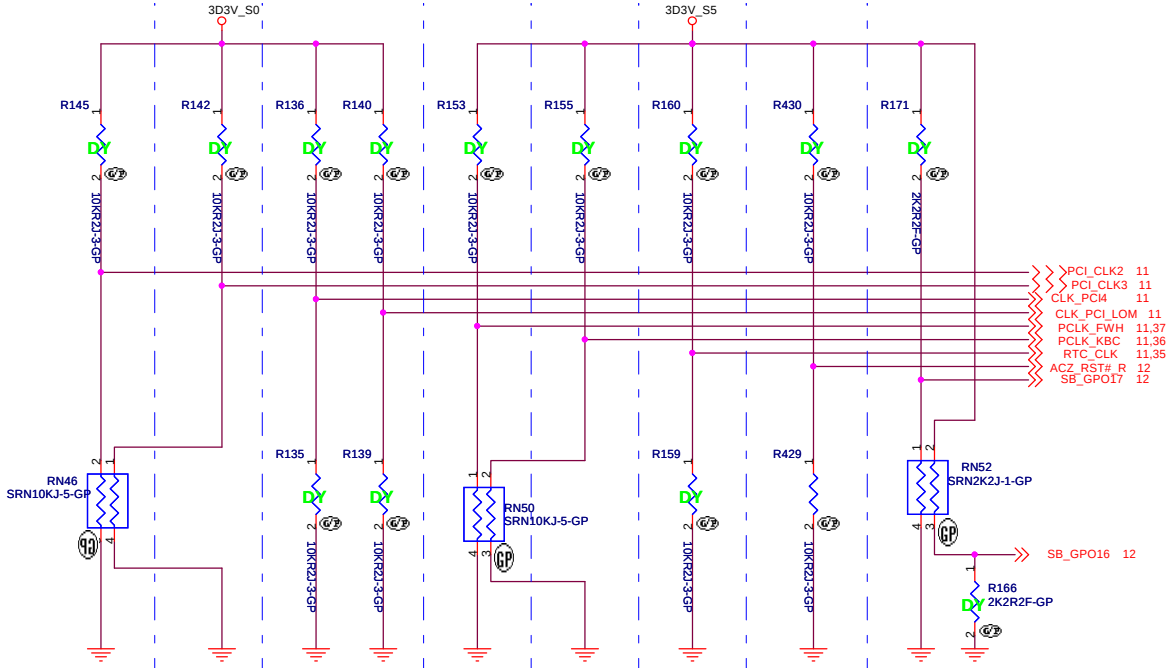
Title: **ATi-SB710 POWER&GND (4/5)**

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 05, 2009 Sheet 14 of 63

REQUIRED STRAPS

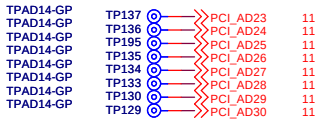
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

JV50-TR8

緯創資通 Wistron Corporation
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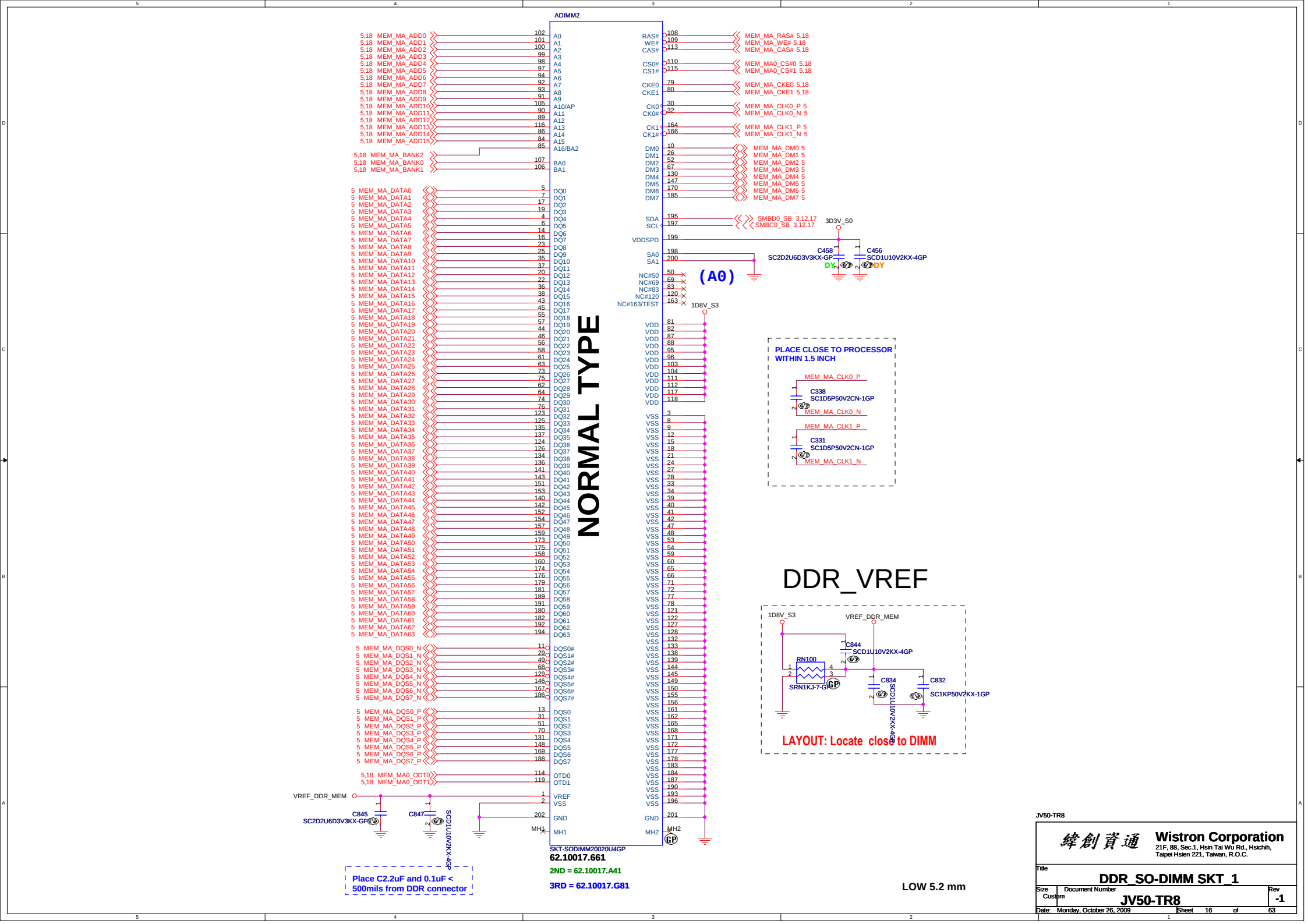
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 STRAPPING (5/5)

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 15 of 63



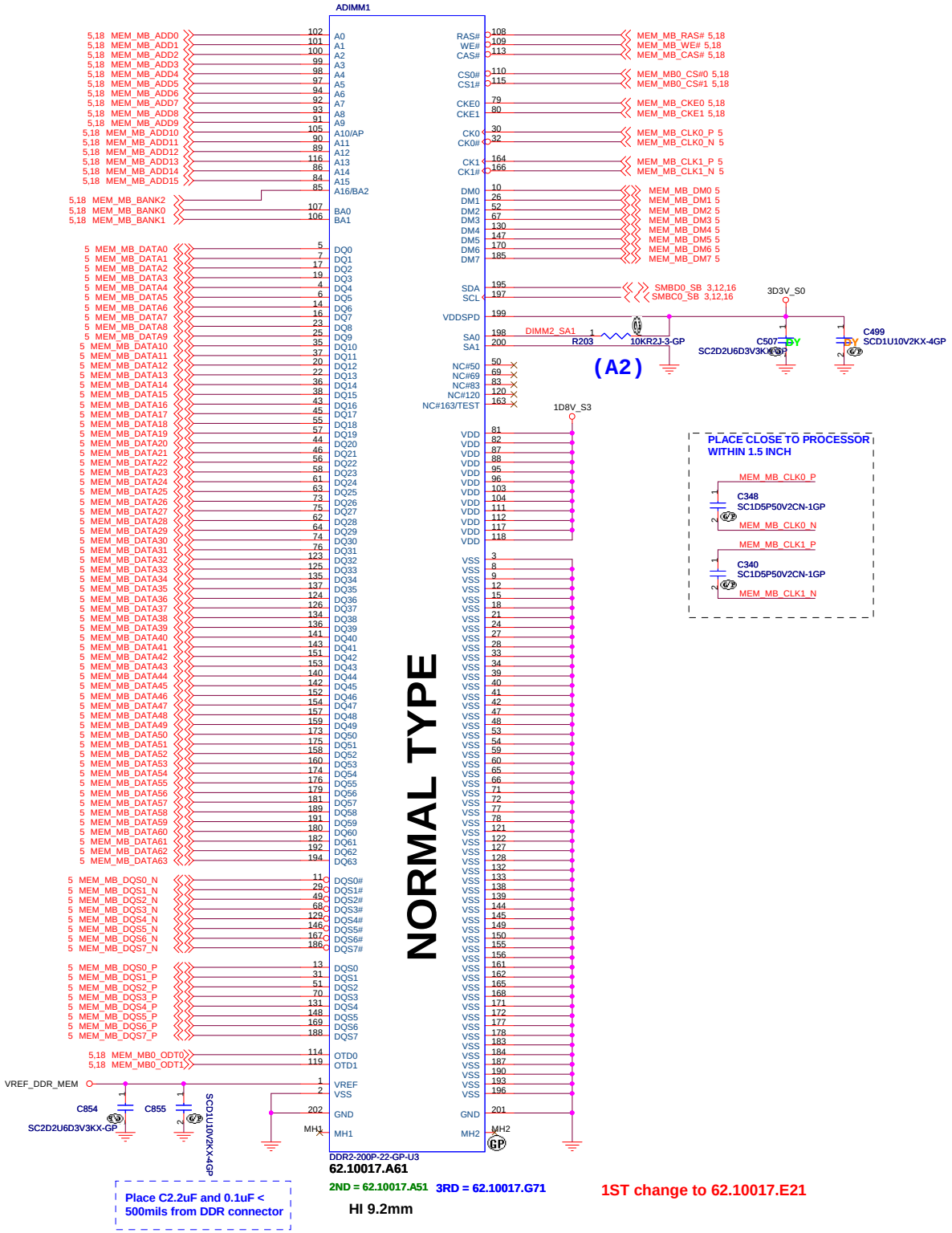
JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size: Custom | Document Number: JV50-TR8 | Rev: -1

Date: Monday, October 26, 2009 | Sheet 16 of 63



JV50-TR8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

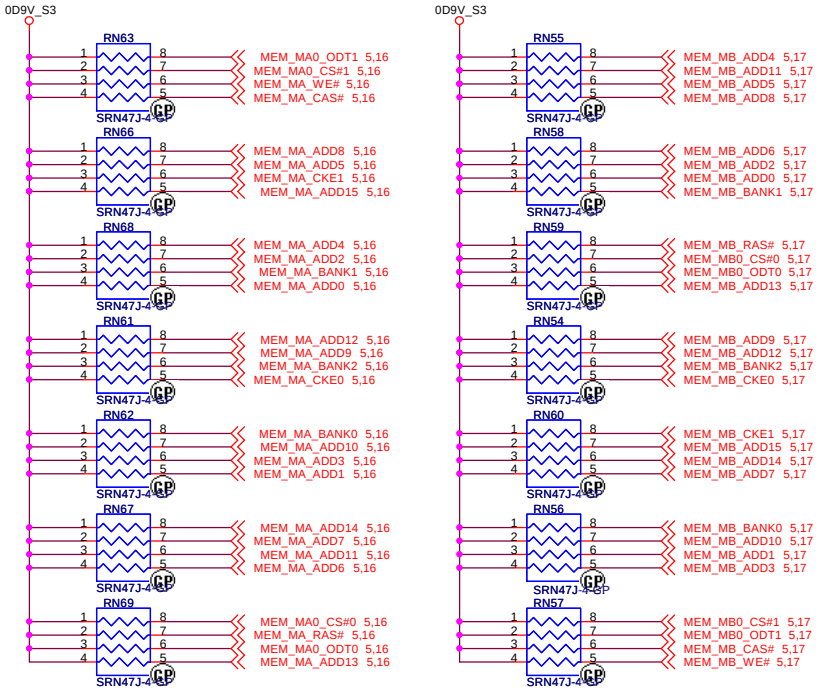
Title: **DDR_SO-DIMM SKT_2**

Size	Document Number	Rev
Custom	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 17 of 63

PARALLEL TERMINATION

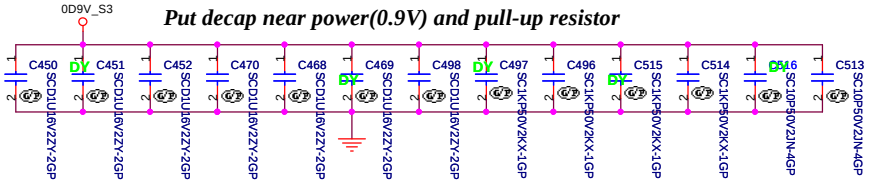
Put decap near power(0.9V) and pull-up resistor



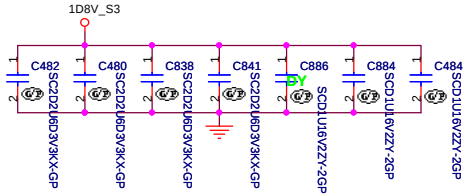
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

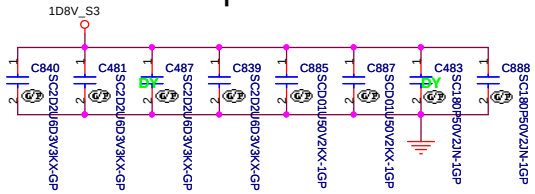


Place these Caps near DM1



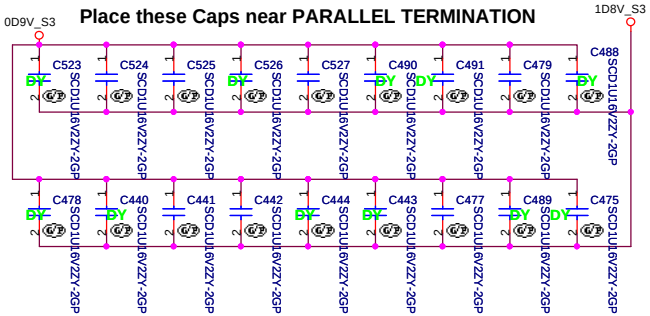
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



JV50-TR8

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR_DAMPING & TERMINATION**

Size	Document Number	Rev
A3	JV50-TR8	-1

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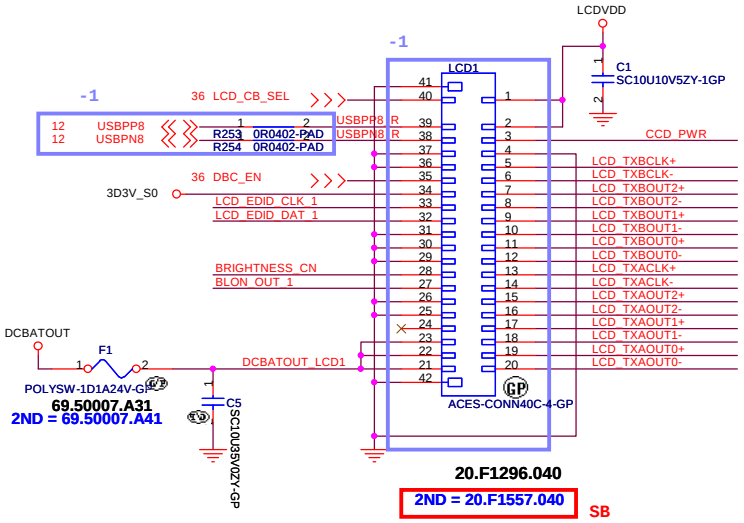
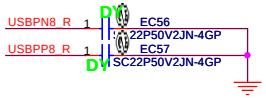
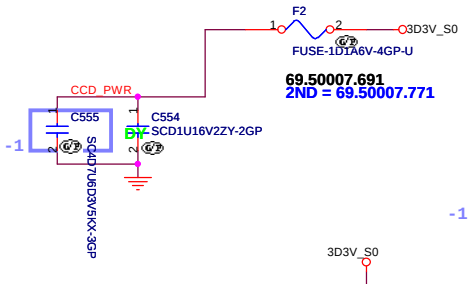
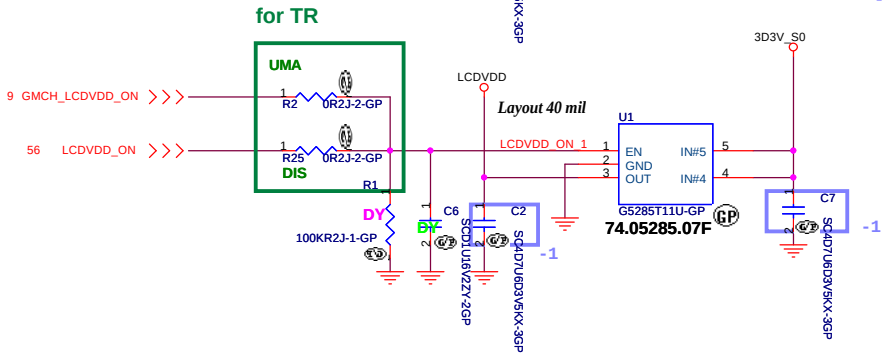
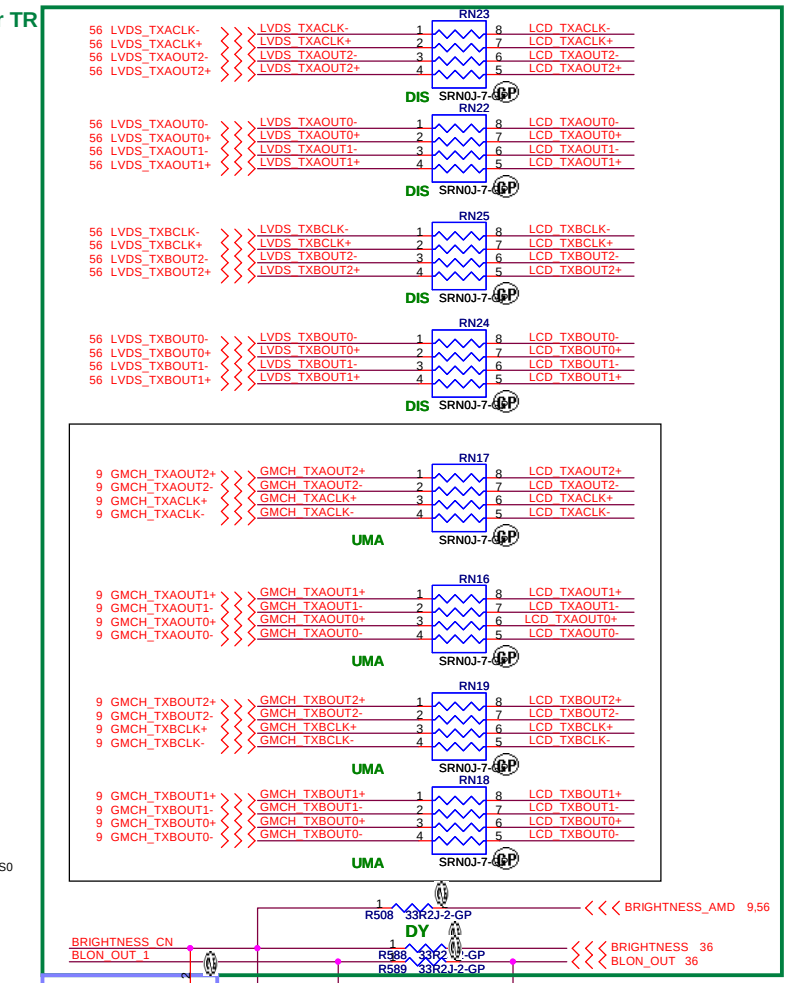
LCD/INVERTER/CCD CONN











Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN		
Size: A3	Document Number: JV50-TR8	Rev: -1
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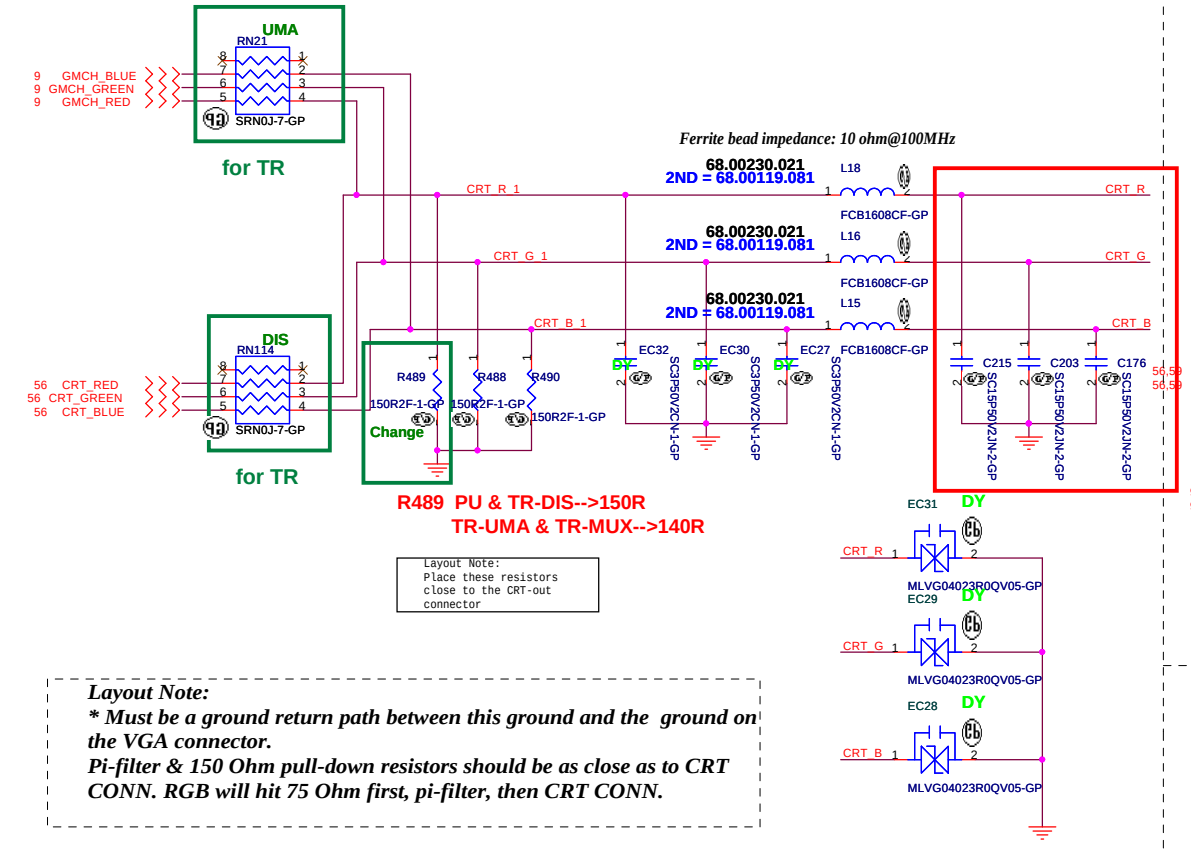
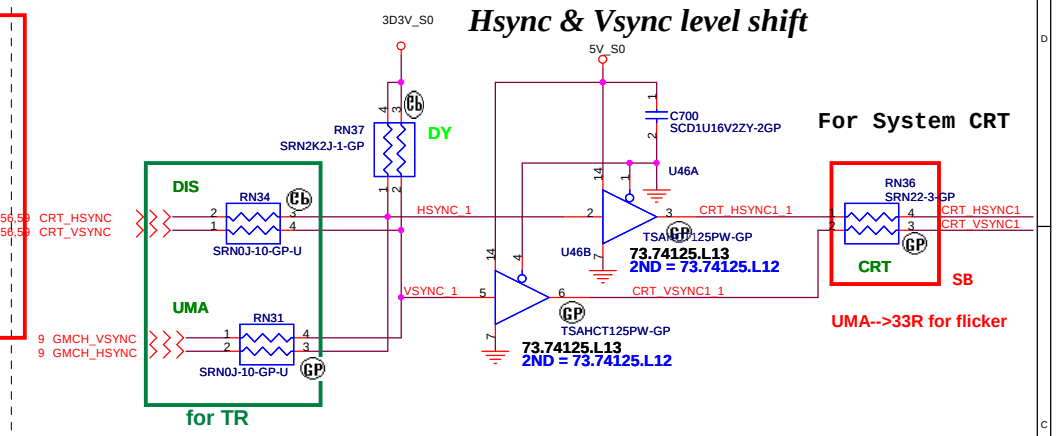
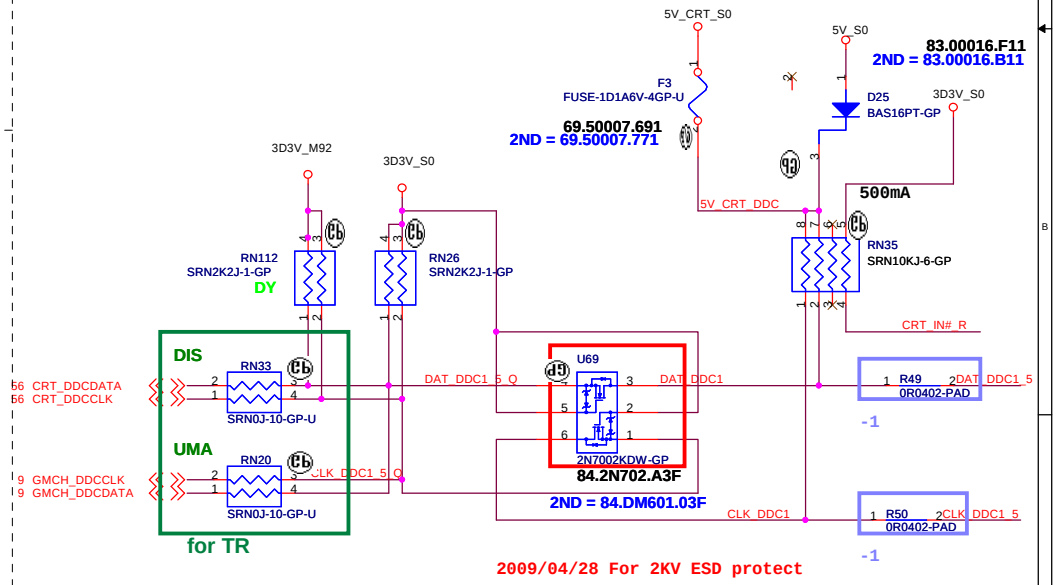
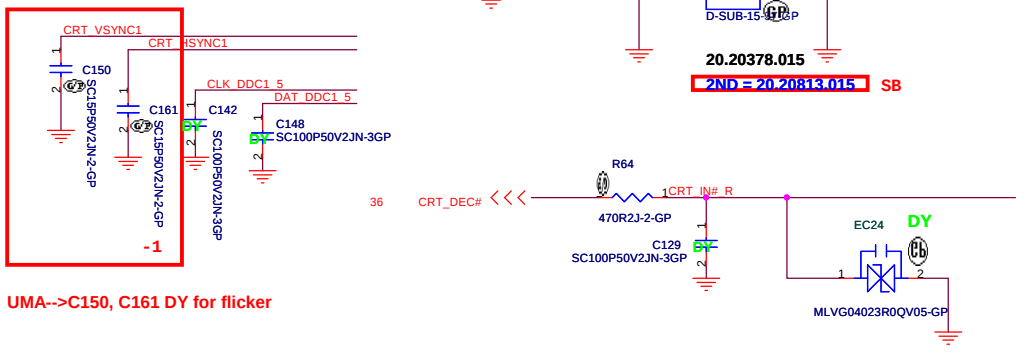


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





CRT I/F & CONNECTOR



JV50-TR8

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
	JV50-TR8	-1

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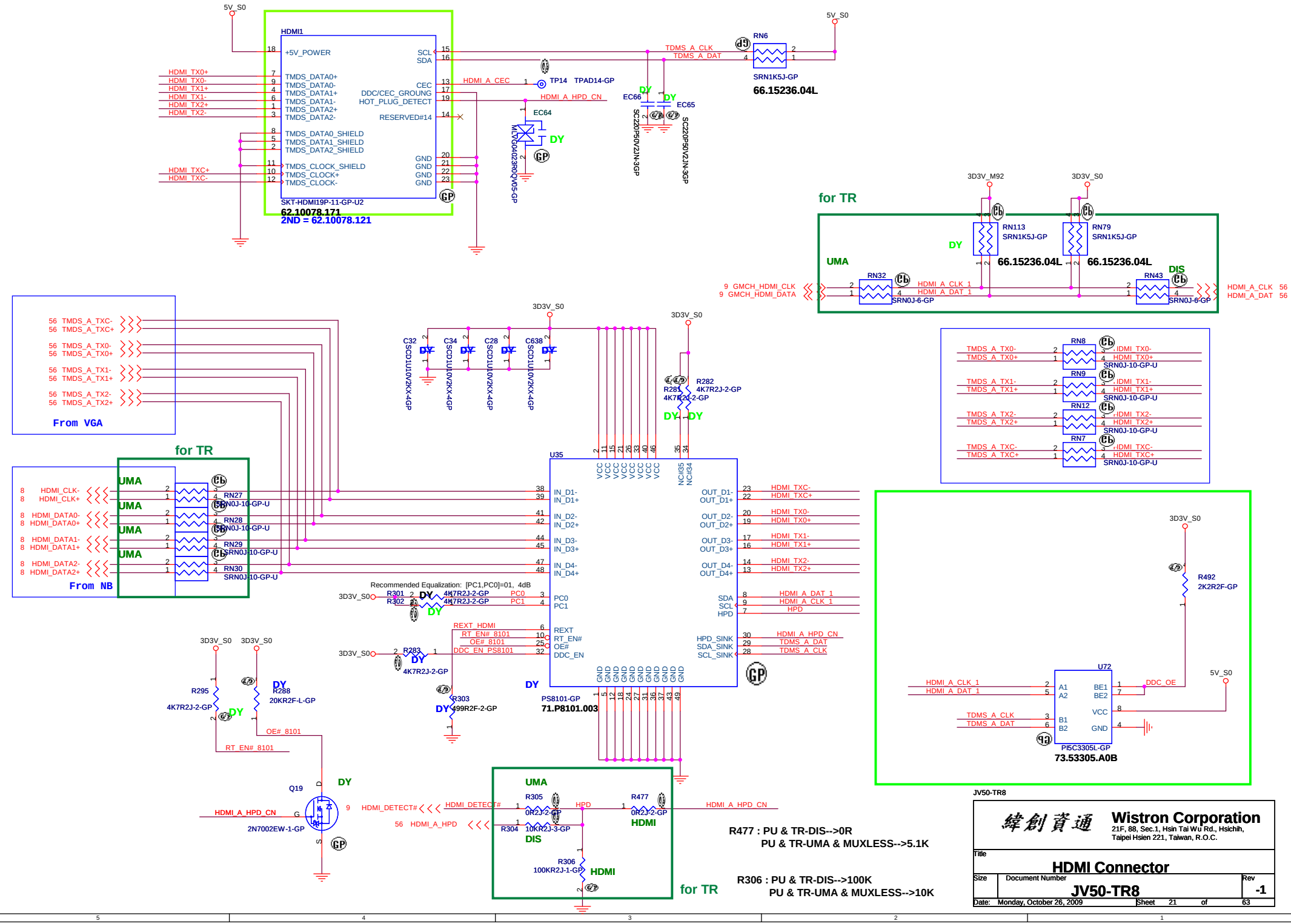
HDMI1
SKT-HDMI19P-11-GP-U2
62.10078.171
2ND = 62.10078.121
RN6
SRN1K5J-GP
66.15236.04L
TP14 TPAD14-GP
EC64
EC65
EC66
MLTG0402R30QV05-GP
SC220P50V2JN-3GP
for TR
UMA
DIS
RN113
RN79
RN32
RN43
SRN0J-6-GP
From VGA
From NB
RN27
RN28
RN29
RN30
SRN0J-10-GP-U
RN8
RN9
RN12
RN7
SRN0J-10-GP-U
U35
PS8101-GP
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
R282
4K7R2J-2-GP
R288
20KR2F-L-GP
R303
499R2F-2-GP
Q19
2N7002EW-1-GP
R305
R304
10KR2J-3-GP
R306
100KR2J-1-GP
R477
0R2J-2-GP
HDMI
R492
2K2R2F-GP
U72
PI5C3305L-GP
73.53305.A0B
R477 : PU & TR-DIS-->0R
PU & TR-UMA & MUXLESS-->5.1K
R306 : PU & TR-DIS-->100K
PU & TR-UMA & MUXLESS-->10K
JV50-TR8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
HDMI Connector
Size
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Date: Monday, October 26, 2009
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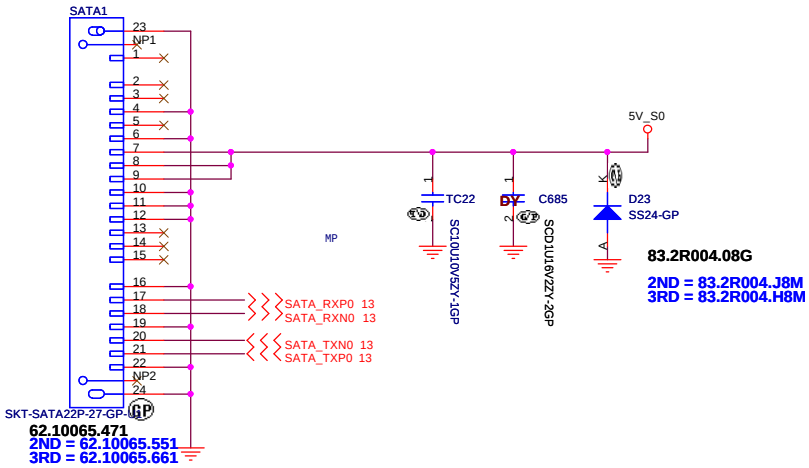
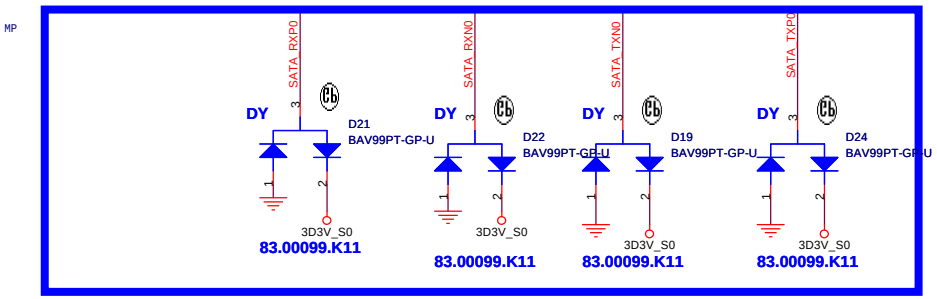
SATA Connector

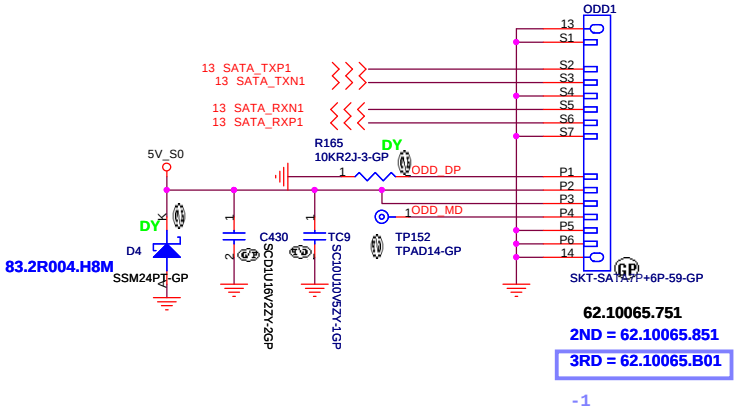


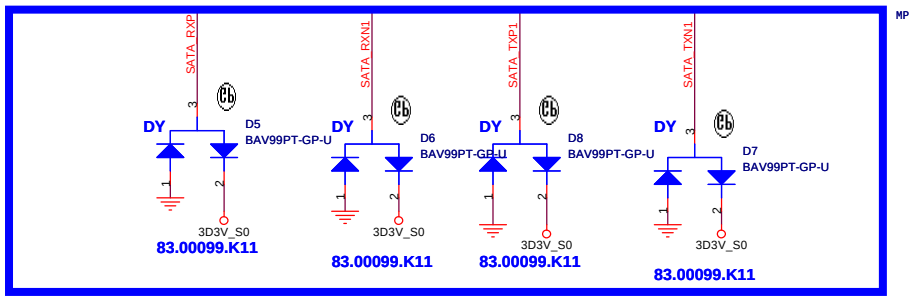


JV50-TR8

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: HDD		
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 22 of 63	

SATA ODD Connector





JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ODD

Size | Document Number: JV50-TR8 | Rev: -1

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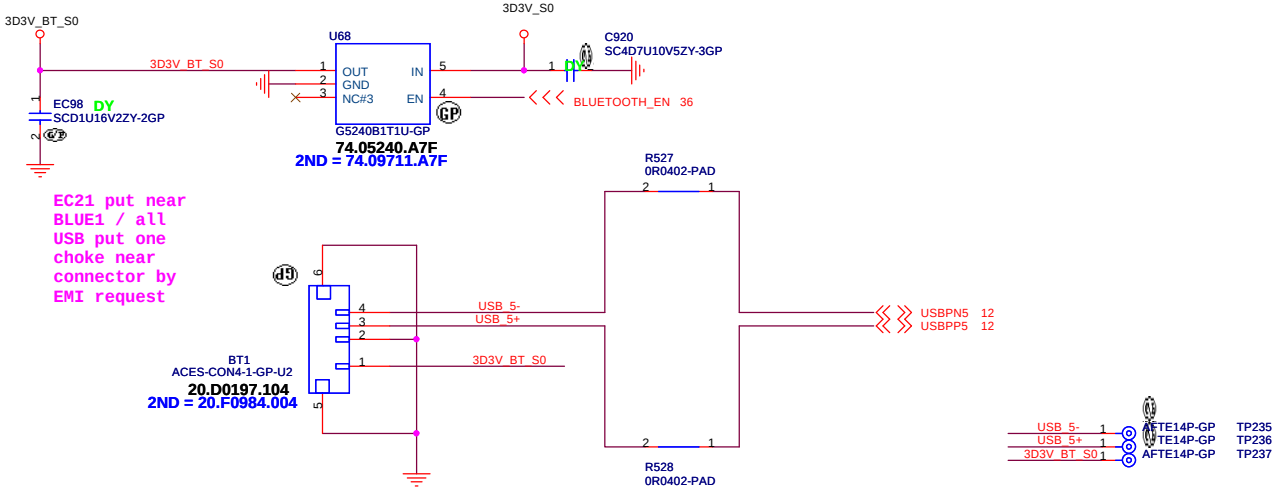
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



JV50-TR8

緯創資通 **Wistron Corporation**
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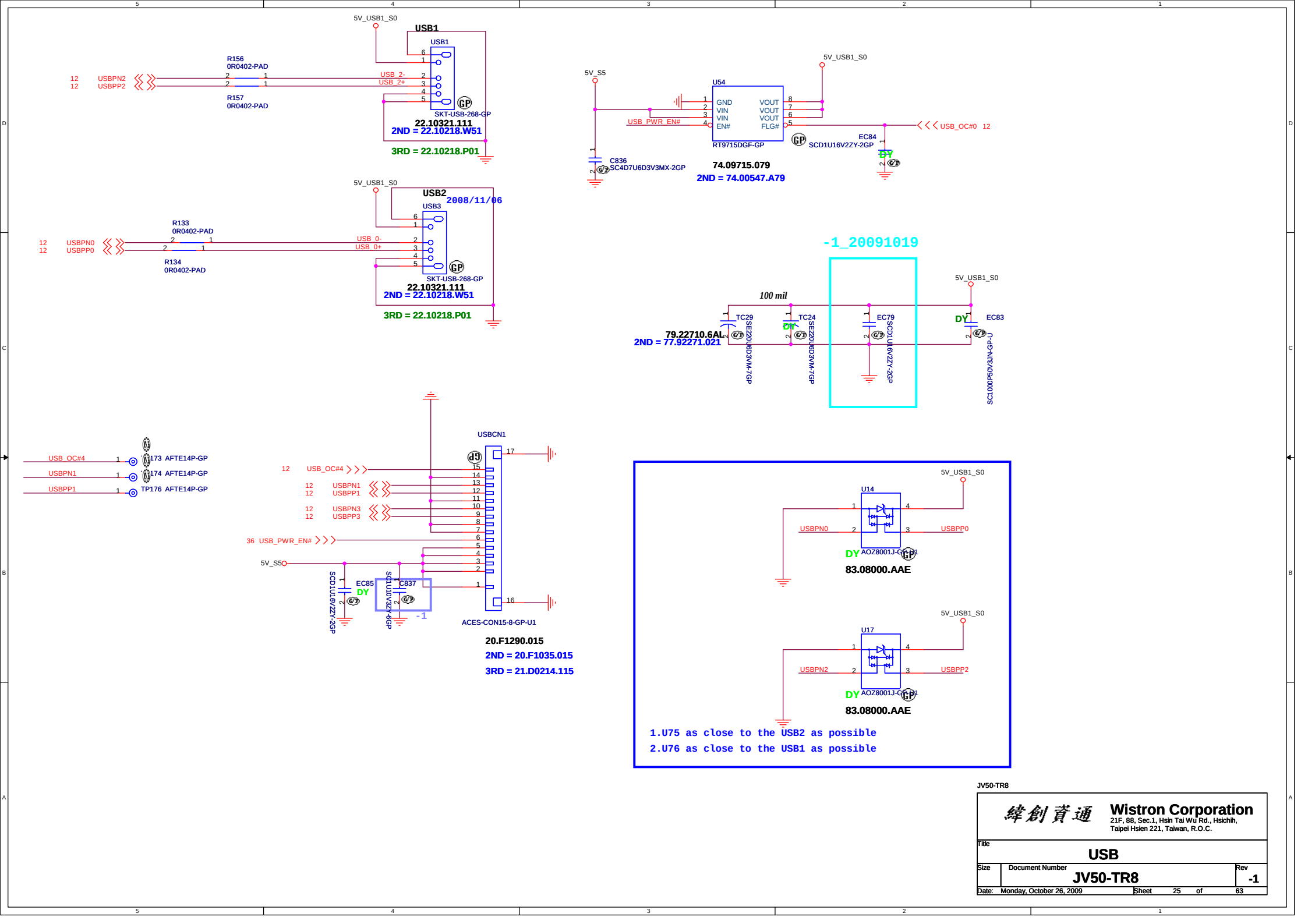
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BLUETOOTH		
Size	Document Number	Rev
	JV50-TR8	**-1**
Date: Thursday, November 12, 2009	Sheet 24 of 63	



JV50-TR8

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **USB**		
Size	Document Number: **JV50-TR8**	Rev: **-1**
Date: Monday, October 26, 2009	Sheet 25 of 63	

CO-Layout BCM5764 and BCM5784
modify BOM :71.05784.M03

U4
BCM5784MKMLG-GP
71.05784.M03

U3
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01

82.30020.851
2ND = 82.30020.791

1ST 84.DCP69.01B
2ND = 84.00069.B1B

Place PLLVDD/AVDDL
CKT as close to chip as
possible

JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BCM5784MKMLG

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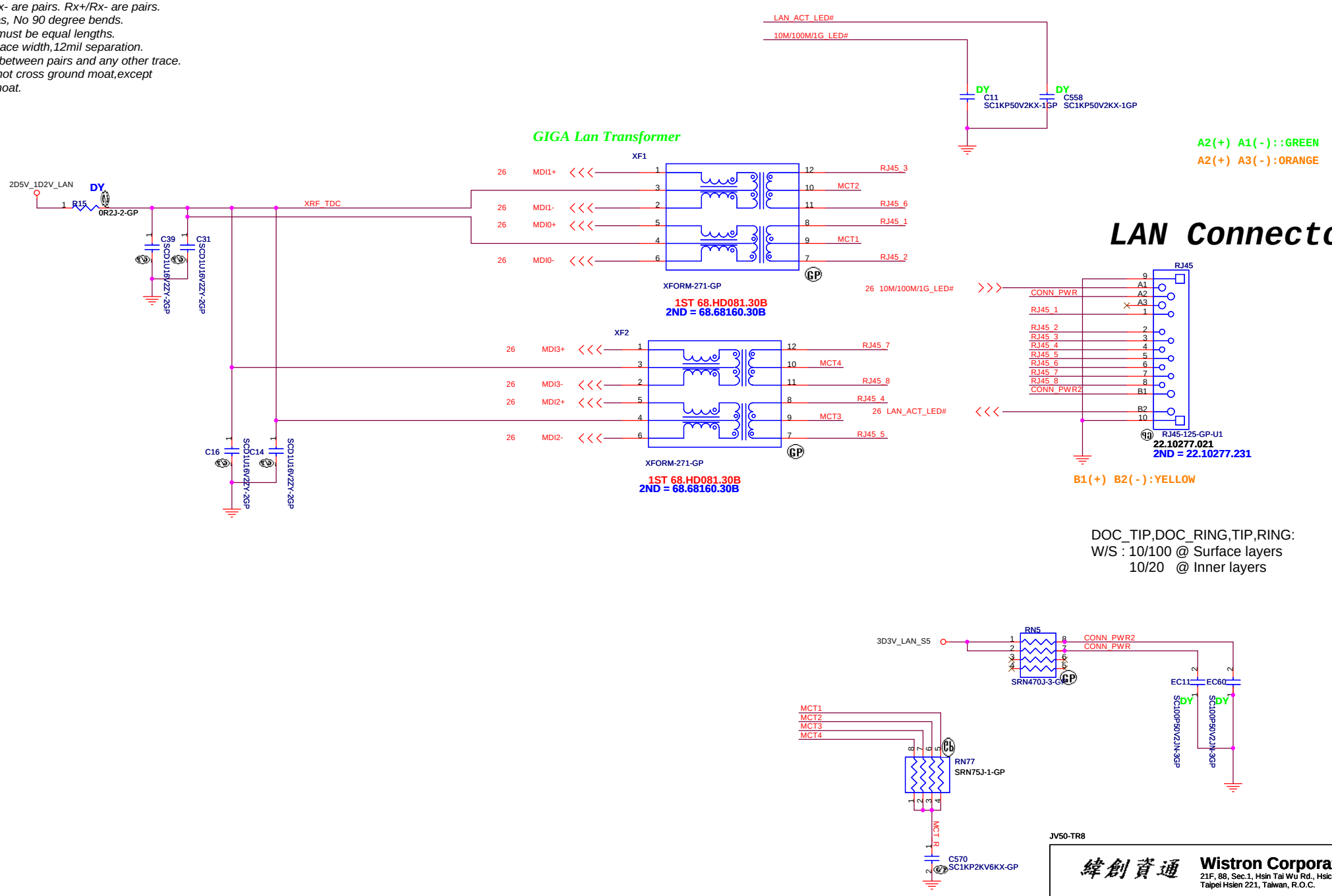
LAN Connector

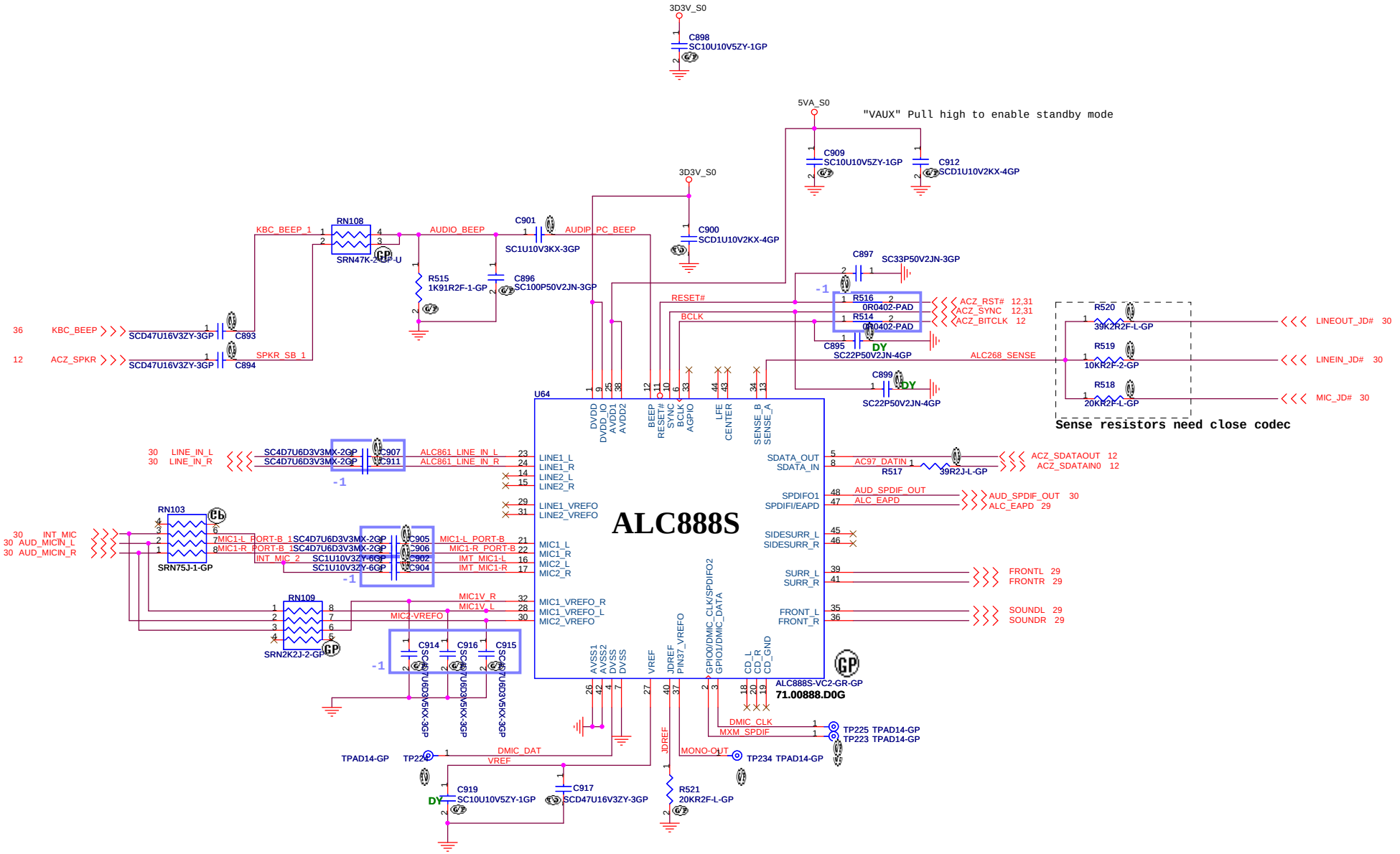
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



JV50-TR8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LAN CONN		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 27 of 63	



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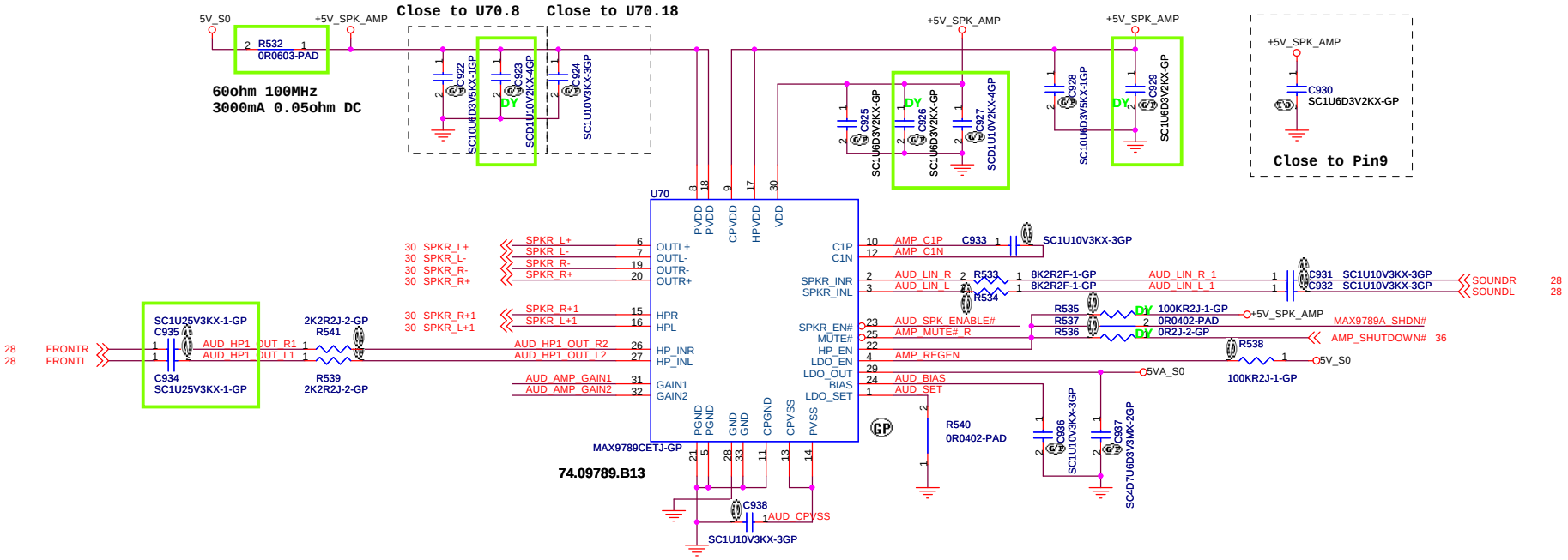
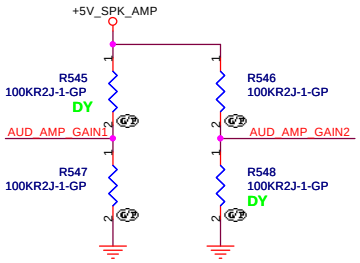
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Azalia codec ALC888**	
Size A3	Document Number **JV50-TR8**	Rev **-1**
Date: Monday, October 26, 2009	Sheet 28 of 63	

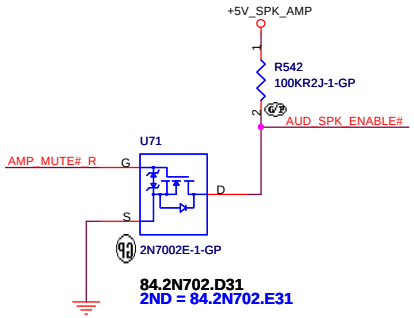


GAIN SETTING

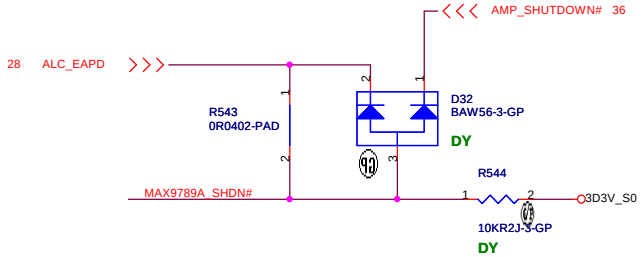


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown



84.2N702.D31
2ND = 84.2N702.E31



JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP

Size	Document Number	Rev
	JV50-TR8	-1

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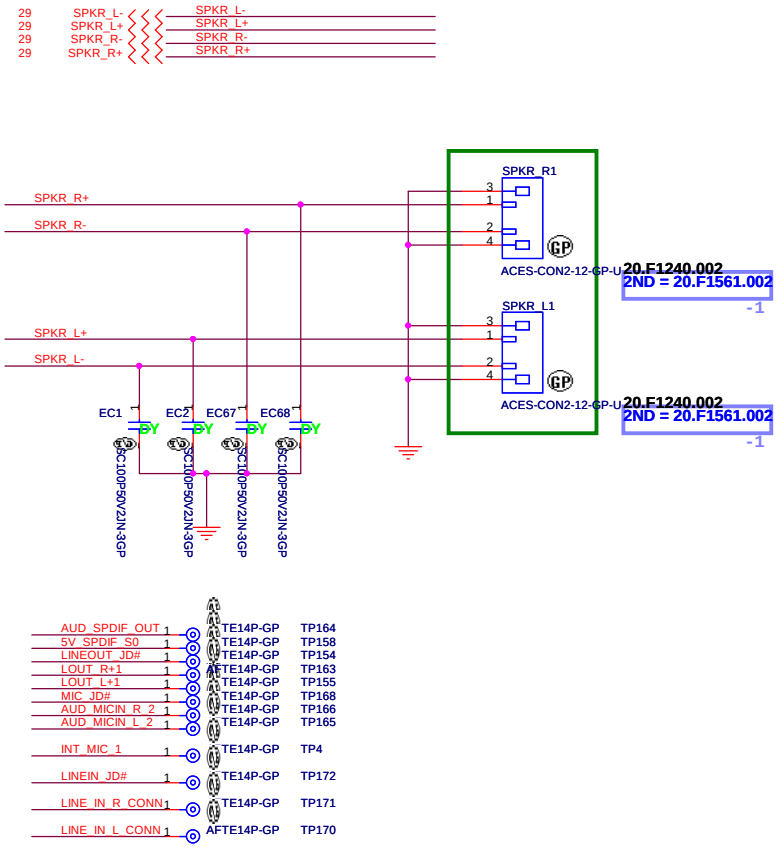
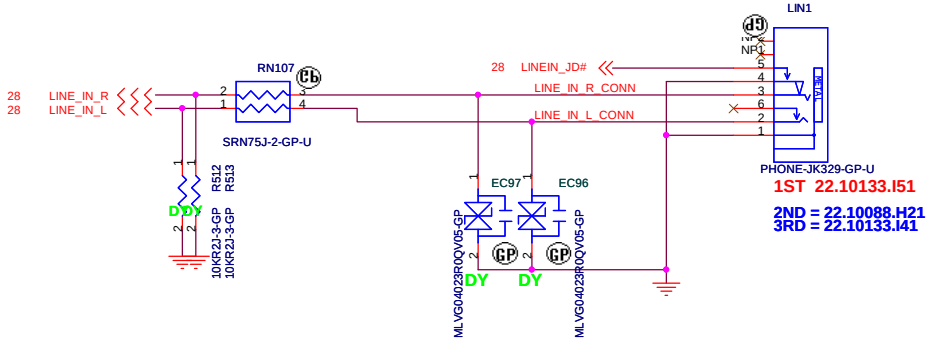
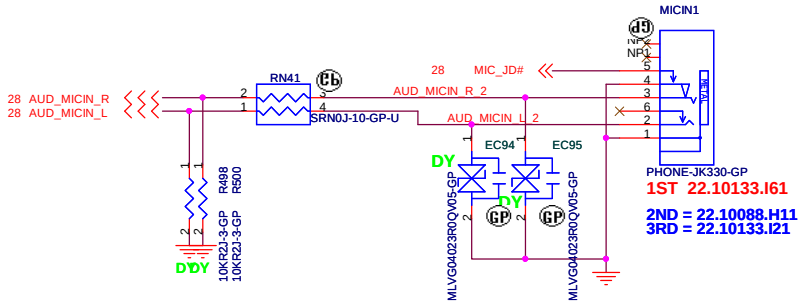
Internal Speaker



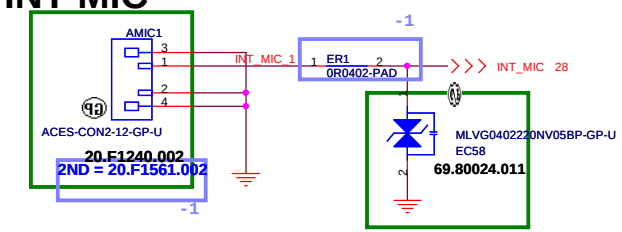
LINE IN



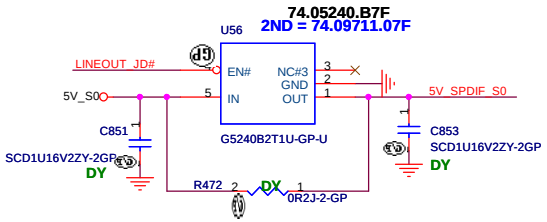
MIC IN

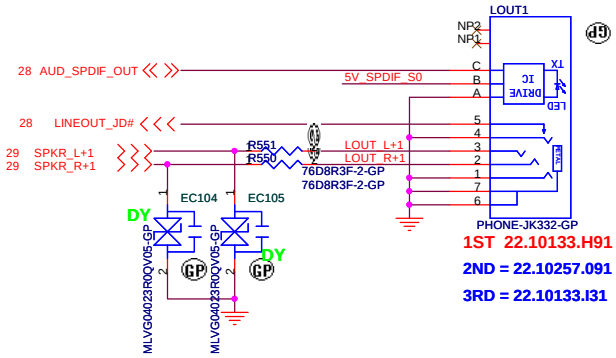


INT MIC



LINE OUT





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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO JACK		
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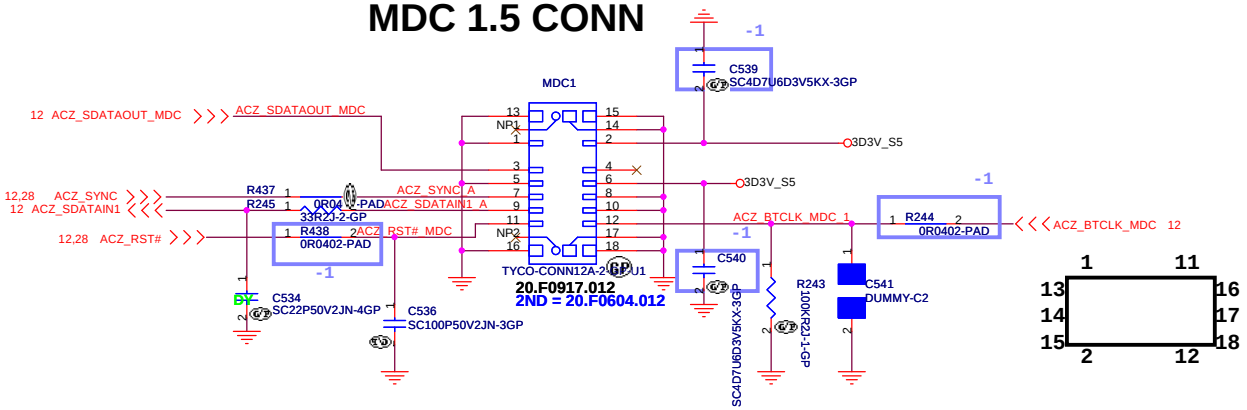
MDC 1.5 CONN



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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC		
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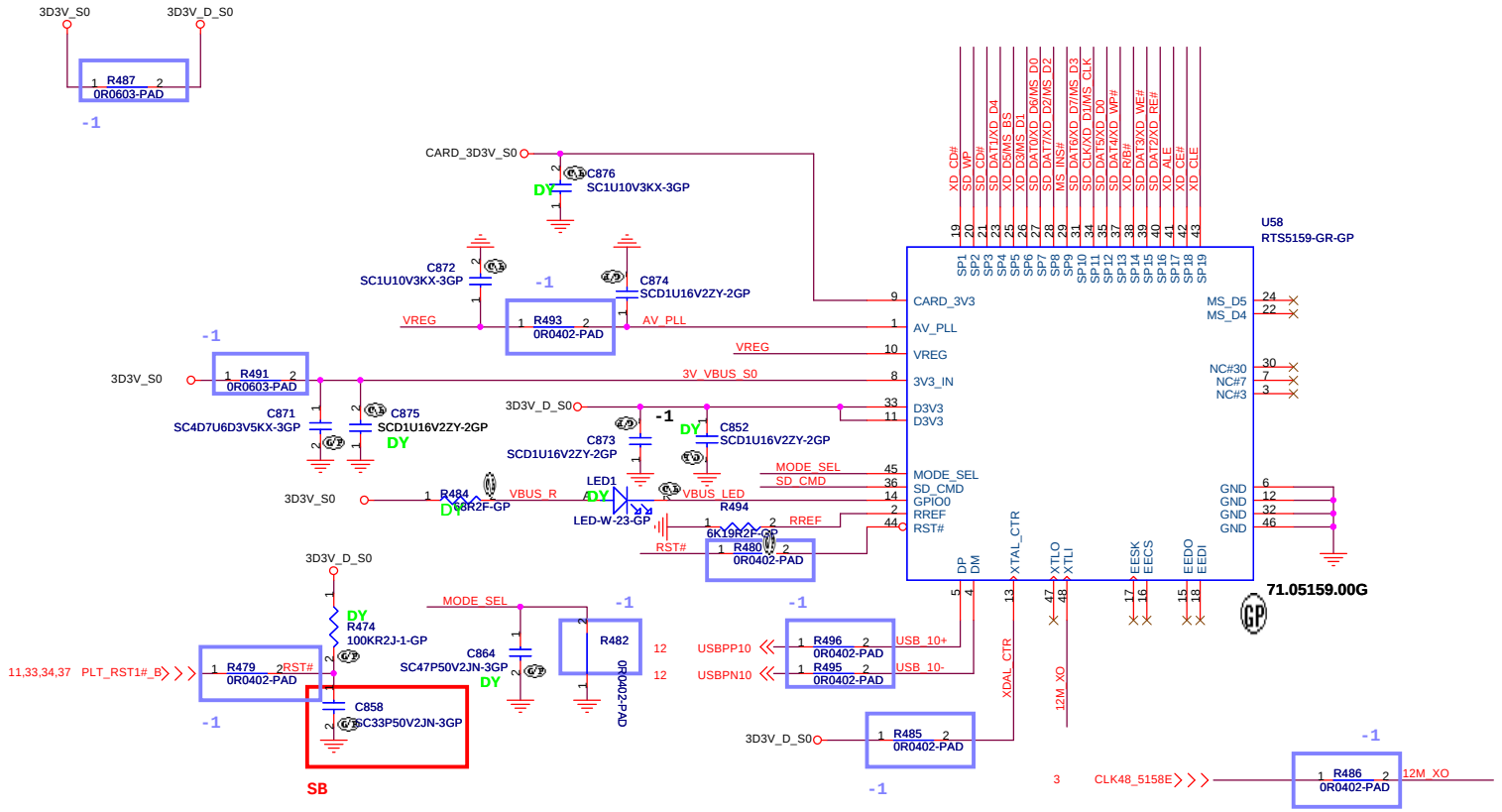
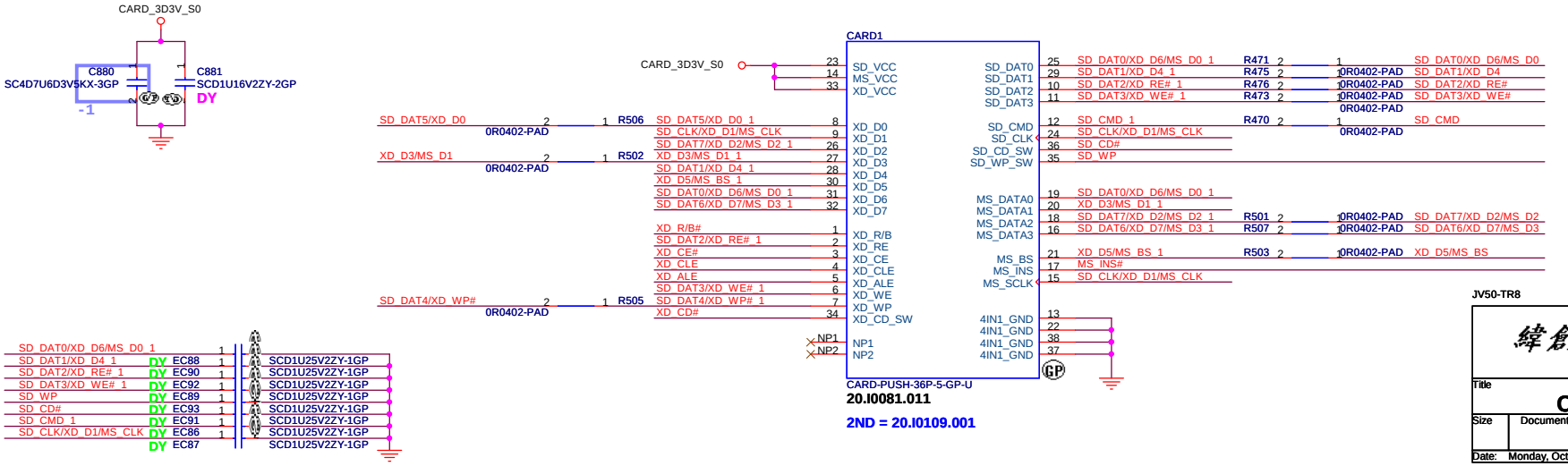
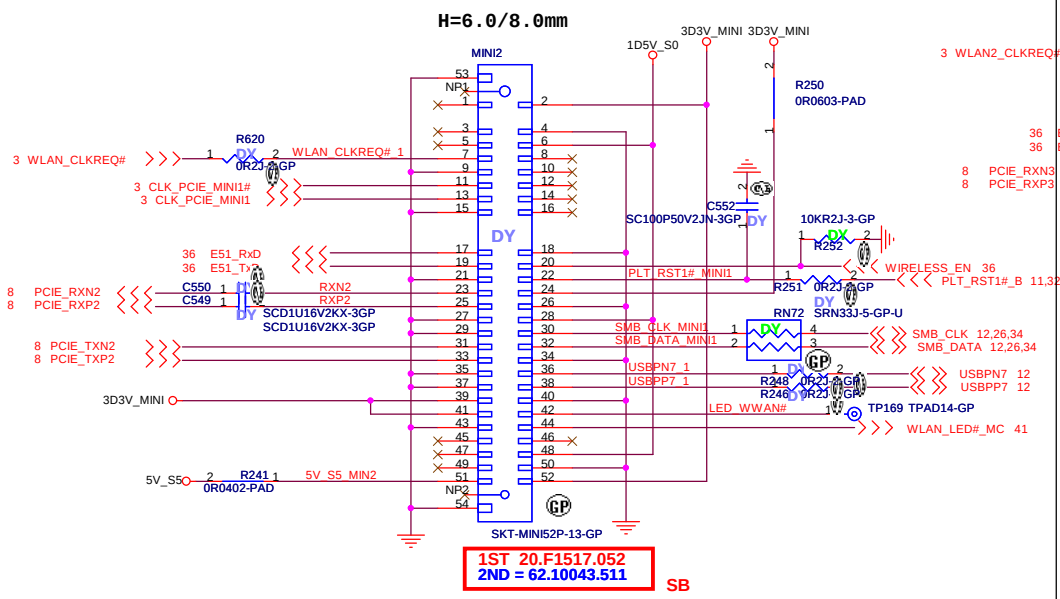
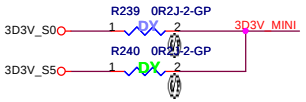


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)

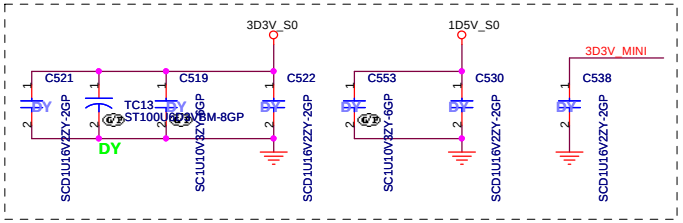


Mini Card Connector(WLAN)

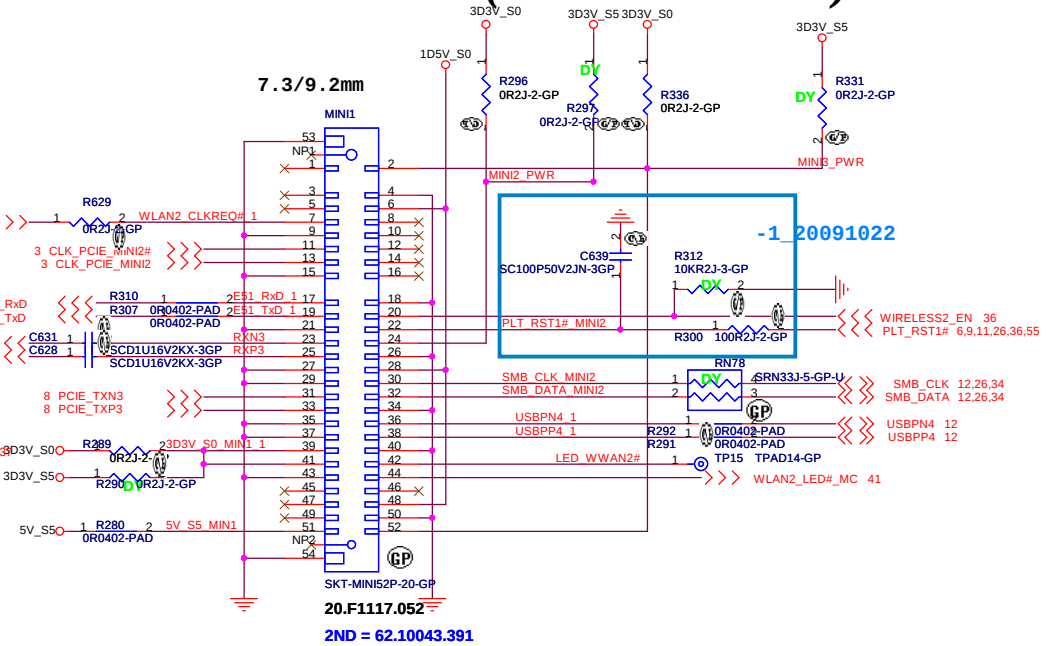




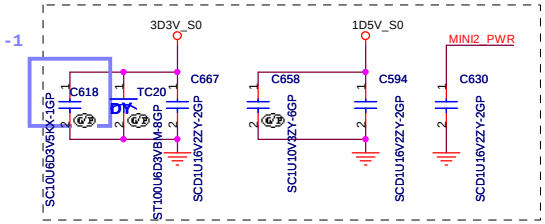
Place near MINI2



Mini Card Connector(Robson2 and 3G)



Place near MINI1



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Title: MINI CARD		
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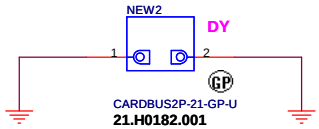
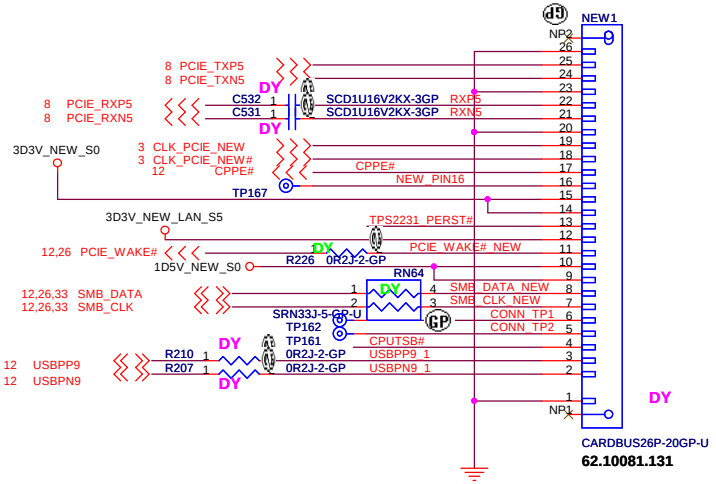
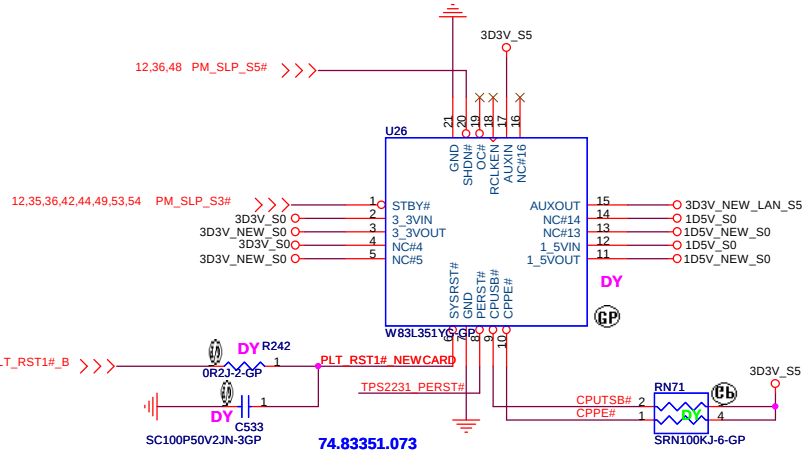
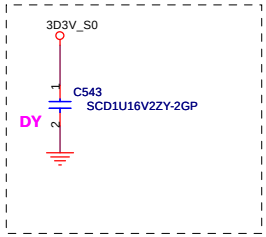
NEWCARD Connector



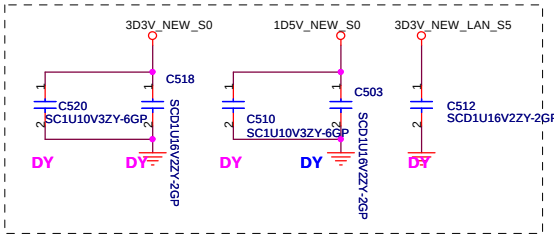




Place them Near to Chip



Place them Near to Connector



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Title: NEW CARD		
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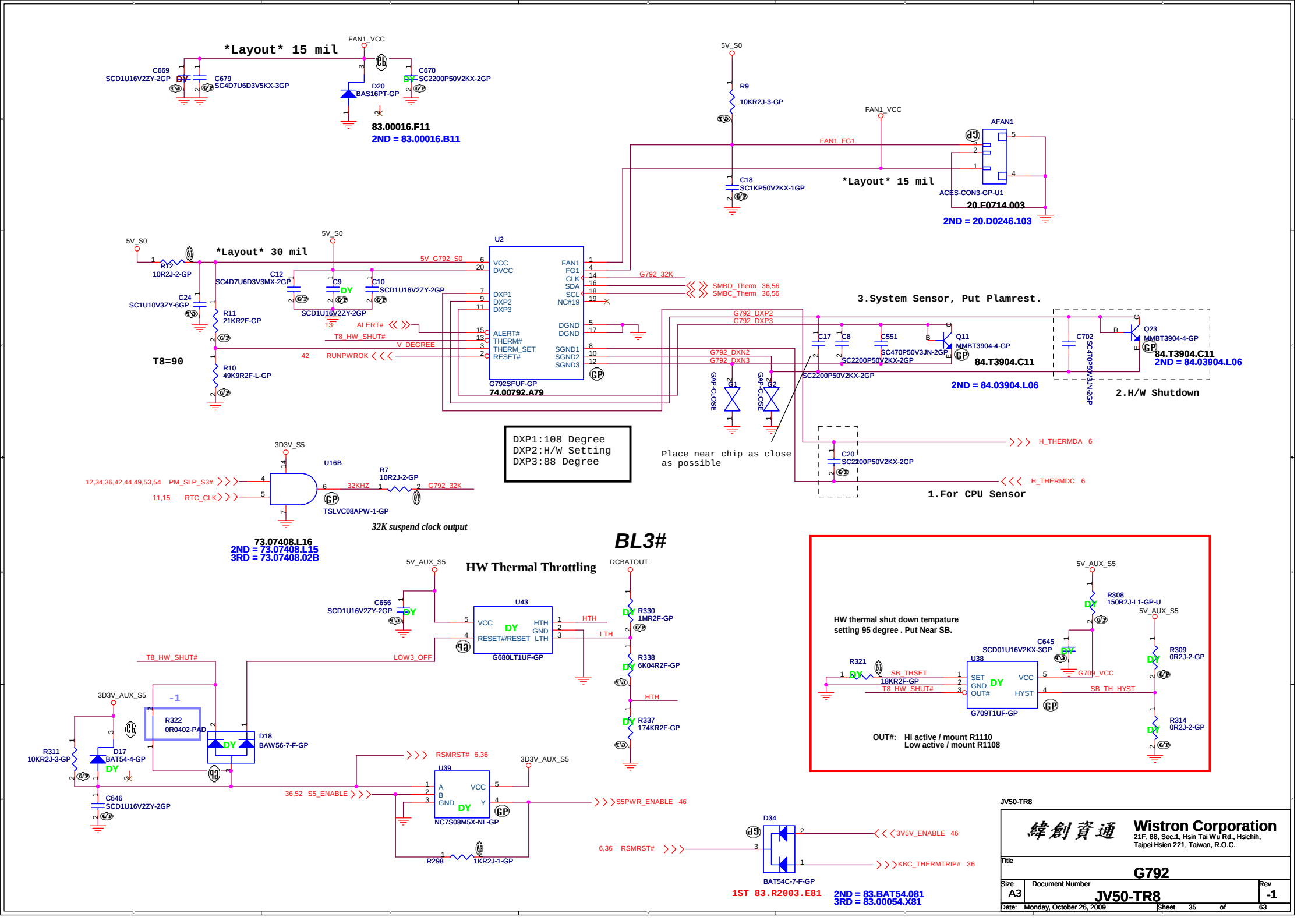

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Title: G792

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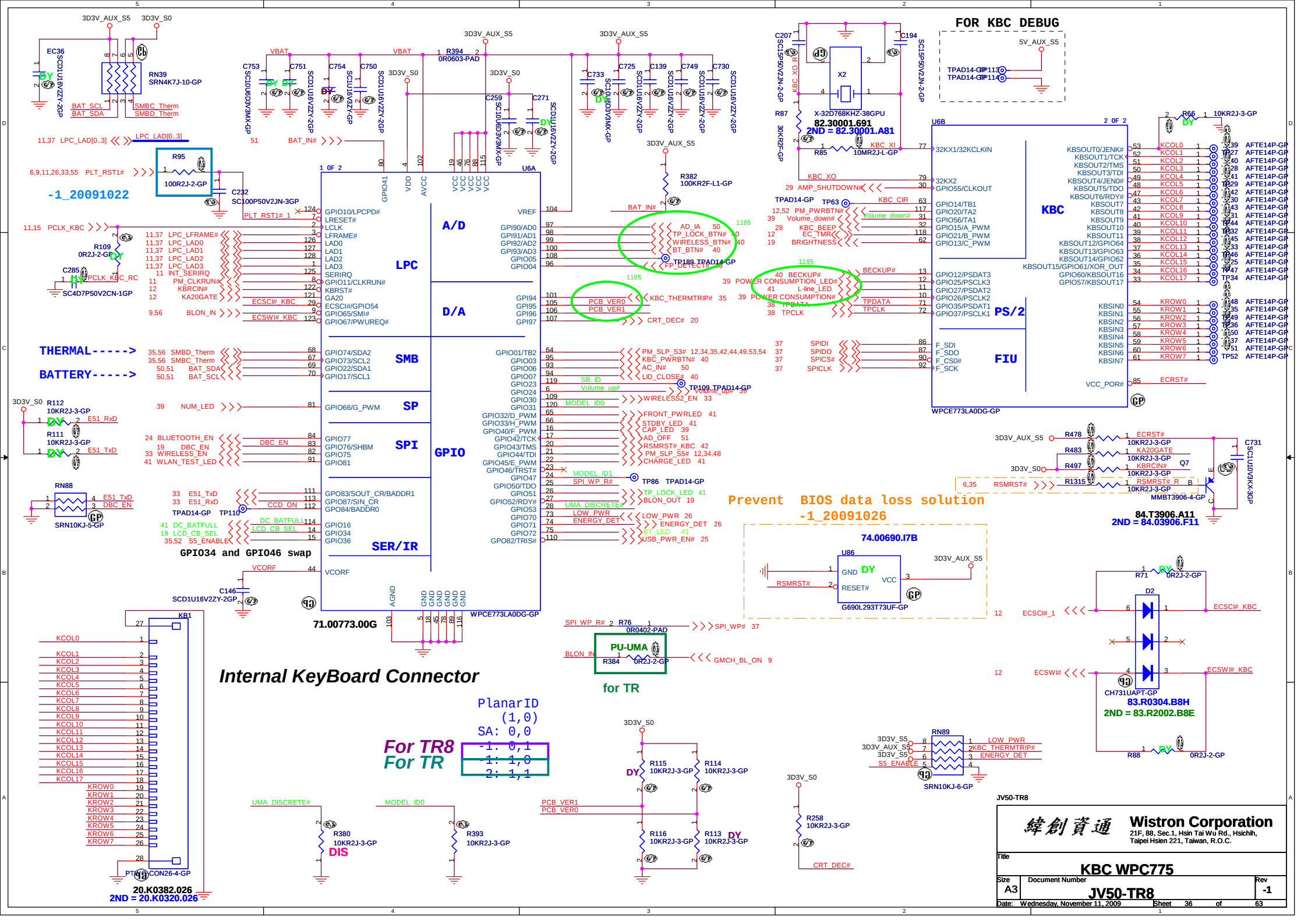
FOR KBC DEBUG
U6A
1 OF 2
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
U6B
2 OF 2
KBC
PS/2
FIU
WPCE773LA0DG-GP
71.00773.00G
-1_20091022
GPIO034 and GPIO046 swap
THERMAL----->
BATTERY----->
Prevent BIOS data loss solution
-1_20091026
74.00690.I7B
G690L293T73UF-GP
Internal KeyBoard Connector
KB1
20.K0382.026
2ND = 20.K0320.026
PlanarID
(1,0)
SA: 0,0
-1: 0,1
-1: 1,0
2: 1,1
For TR8
For TR
PU-UMA
for TR
DIS
82.30001.691
2ND = 82.30001.A81
84.T3906.A11
2ND = 84.03906.F11
CH731UAPT-GP
83.R0304.B8H
2ND = 83.R2002.B8E
SRN10KJ-5-GP
SRN10KJ-6-GP
MMBT3906-4-GP
JV50-TR8
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KBC WPC775
Size A3
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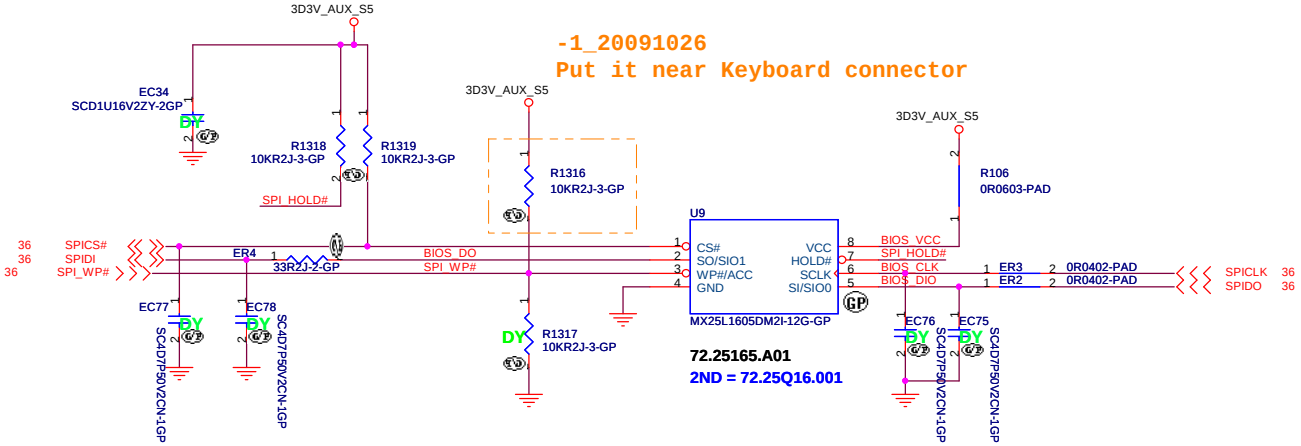
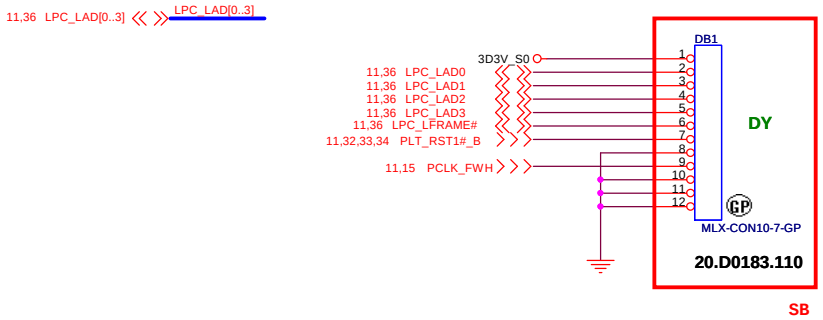


16M Bits
SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



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Taipei Hsien 221, Taiwan, R.O.C.

Title		
BIOS		
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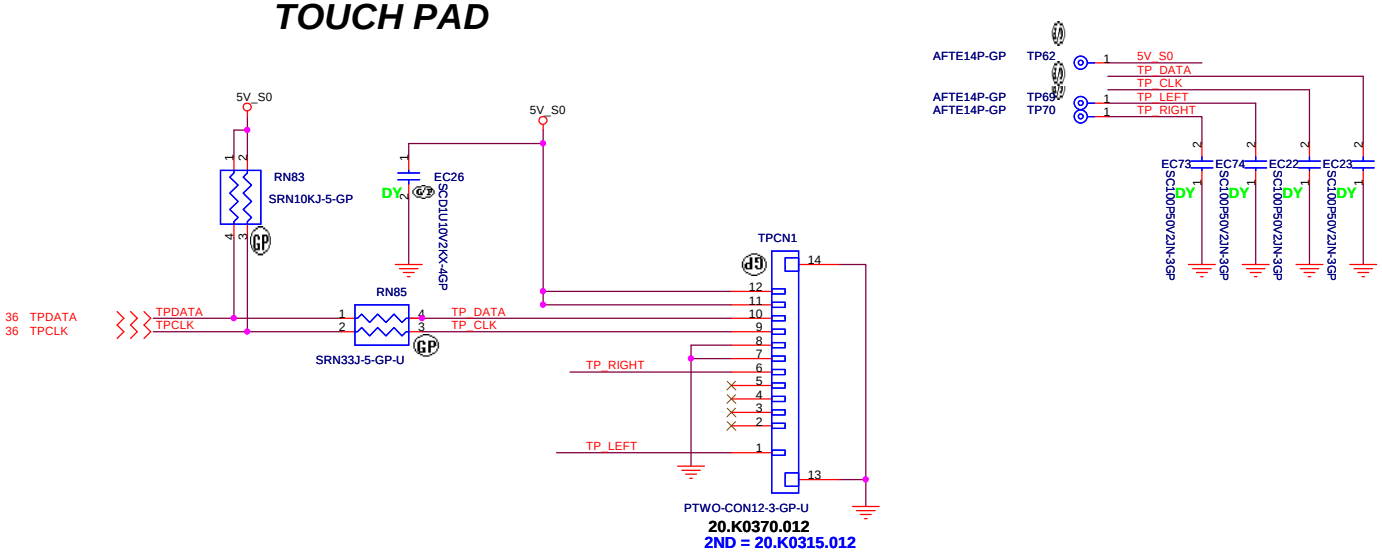
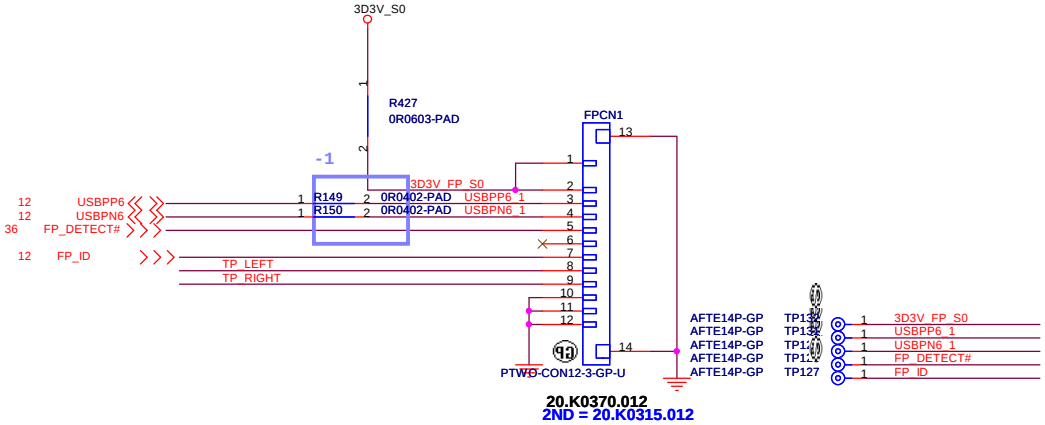
TOUCH PAD



Finger printer



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Title: **Touch PAD/Finger printer**

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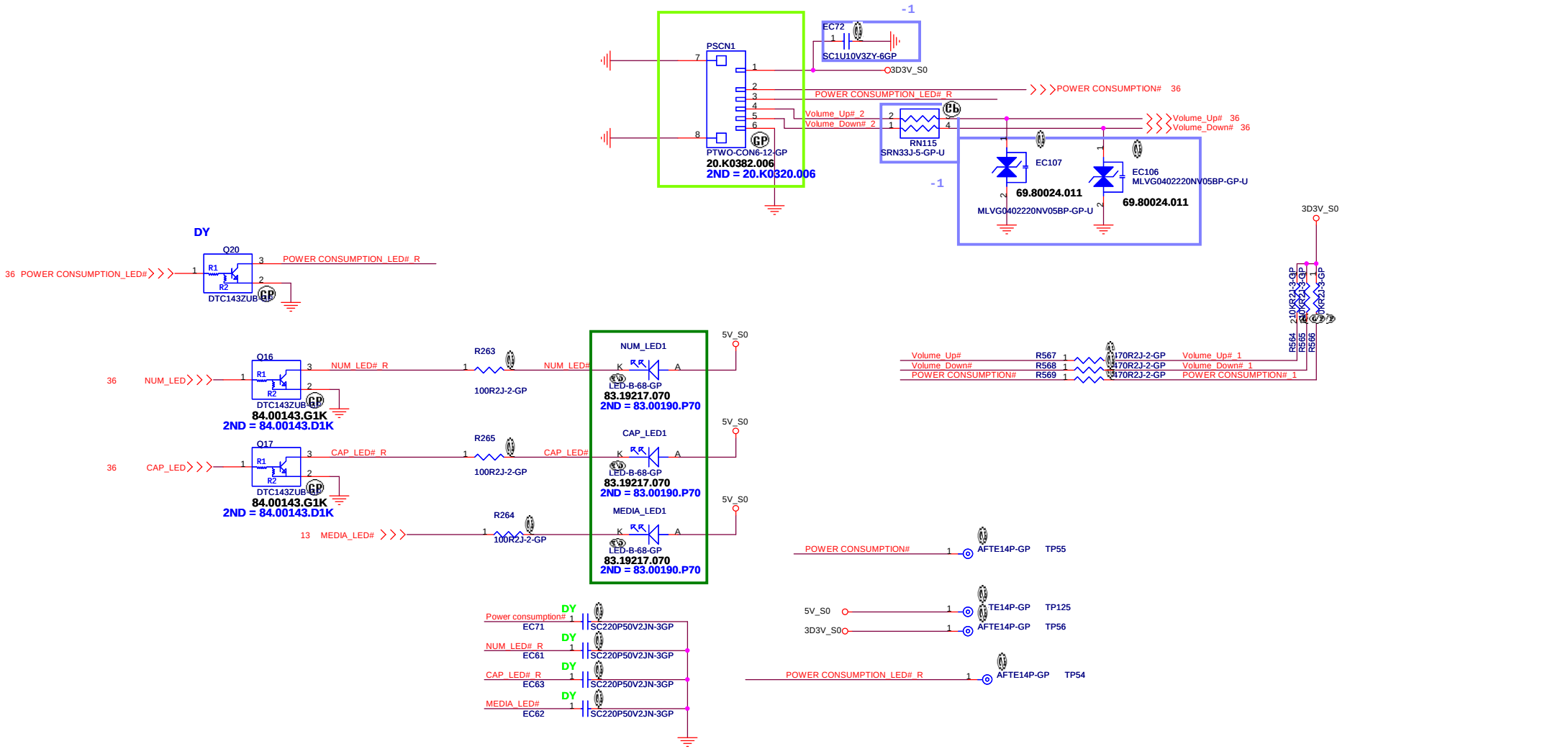

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Title: **LAUNCH BOARD**

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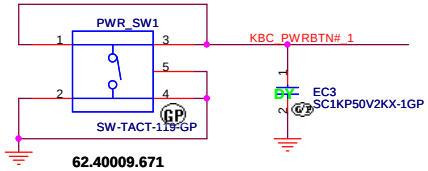
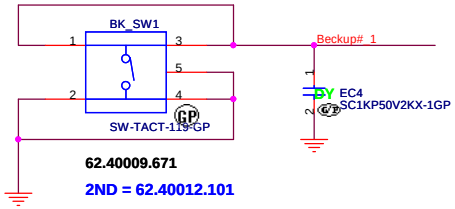
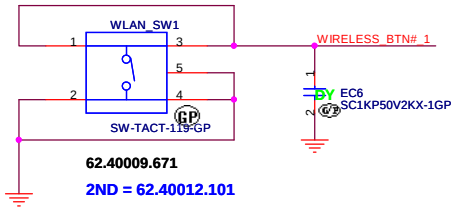
Power Button



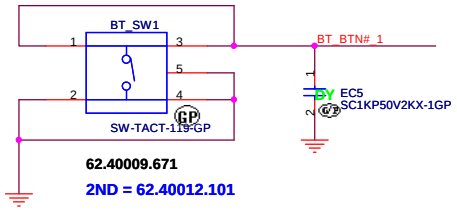
Beckup Button



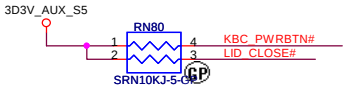
WIRELESS Button

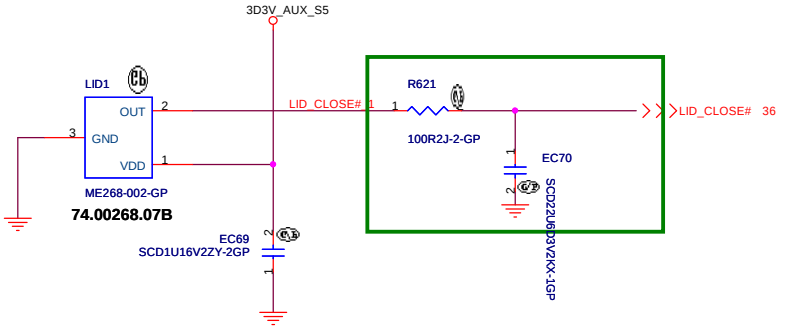


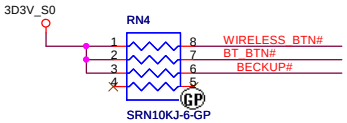
BT/3G Button

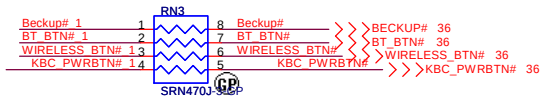


Cover Up Switch

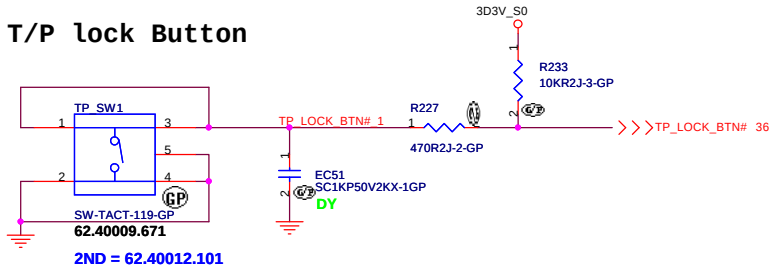








T/P lock Button



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Title: SWITCH		
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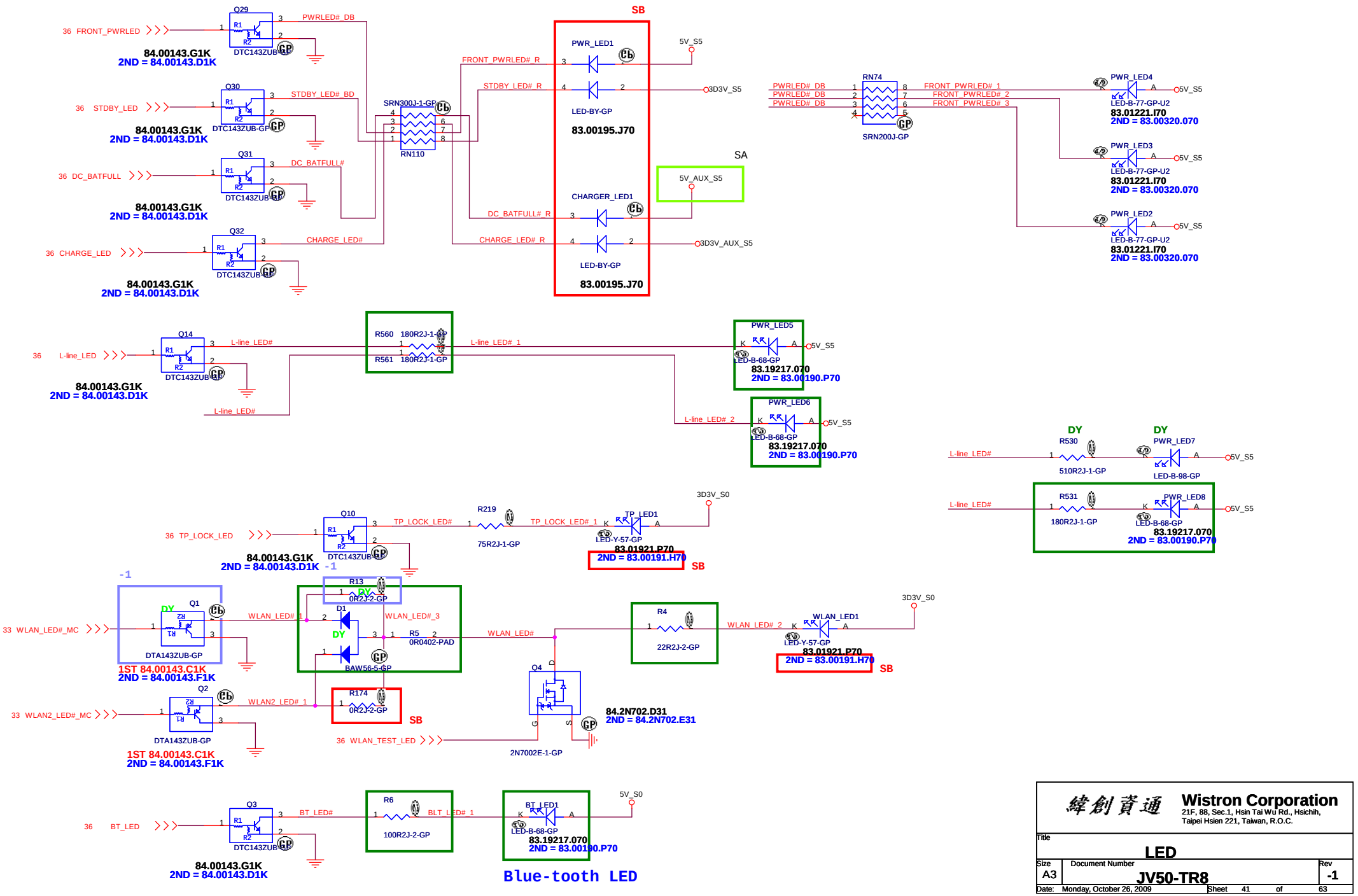

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Title: LED		
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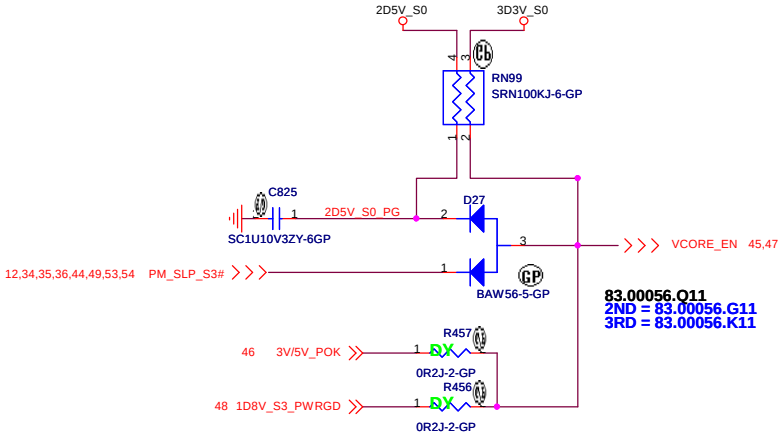

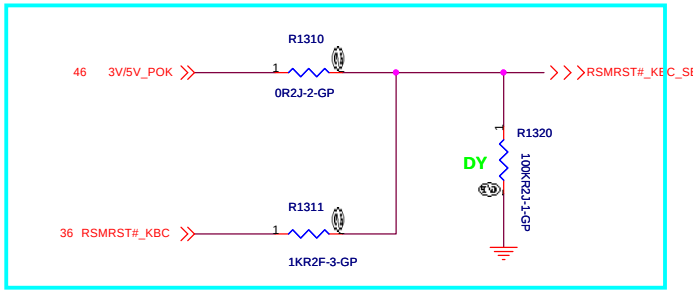

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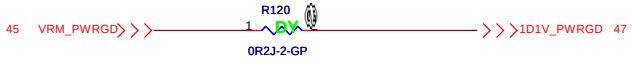

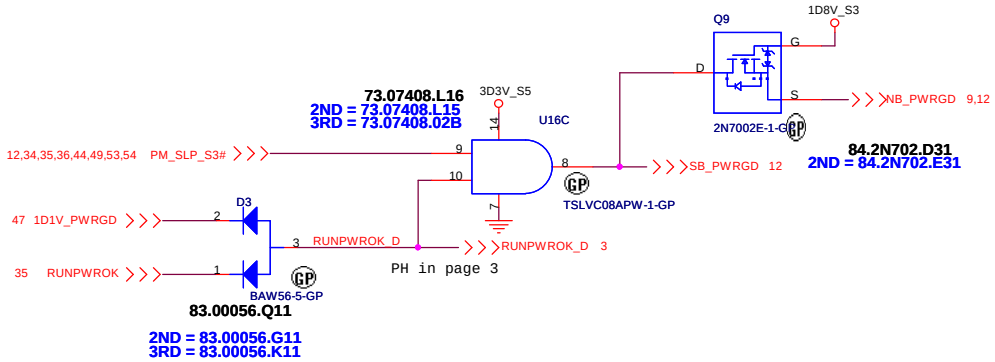

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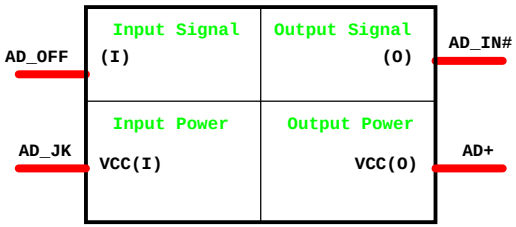
Adapter



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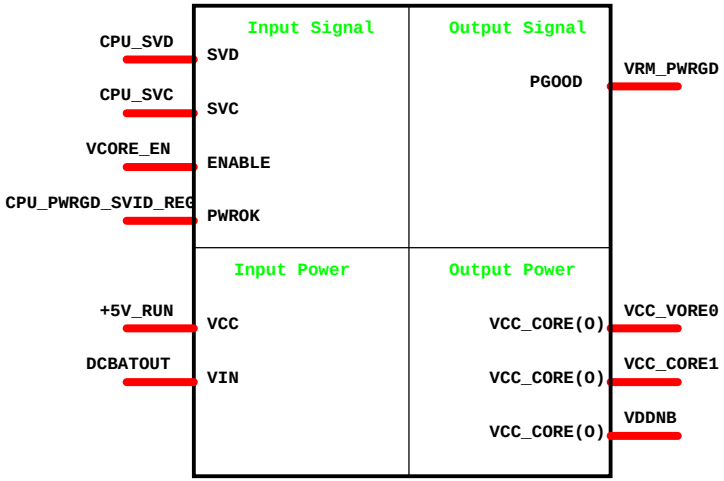

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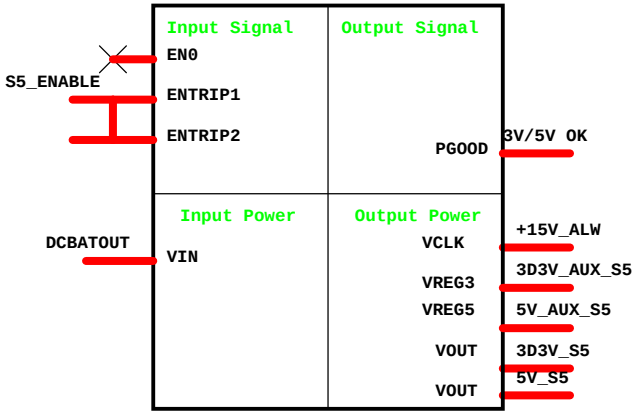

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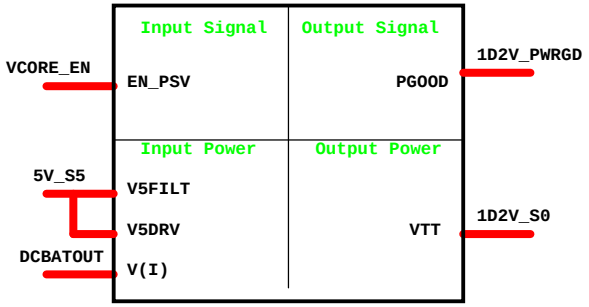

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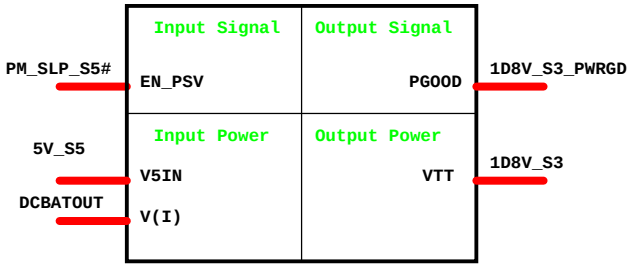

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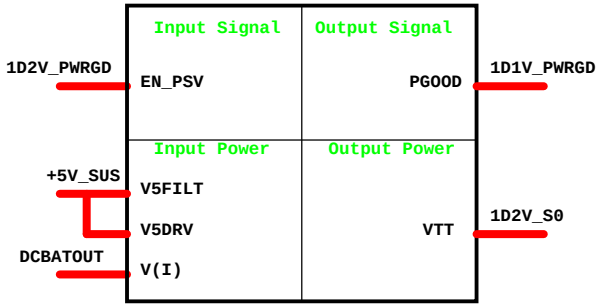
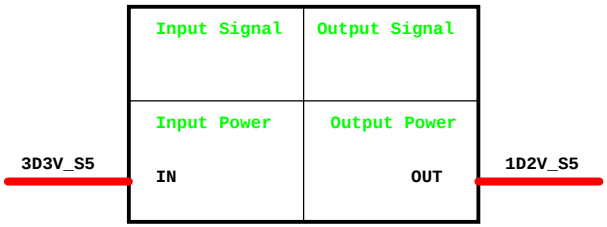
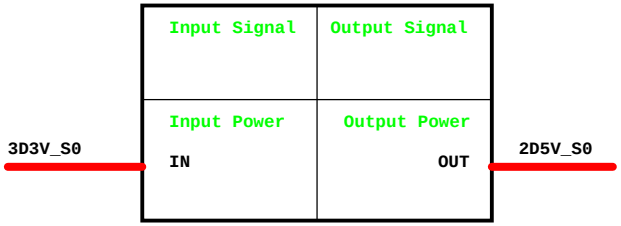


1D2V LDO G9161



2D5V LDO R9161



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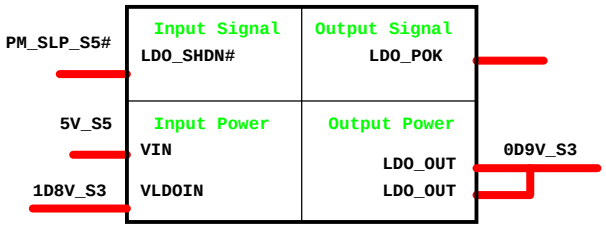

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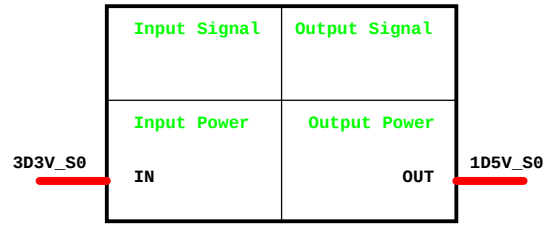
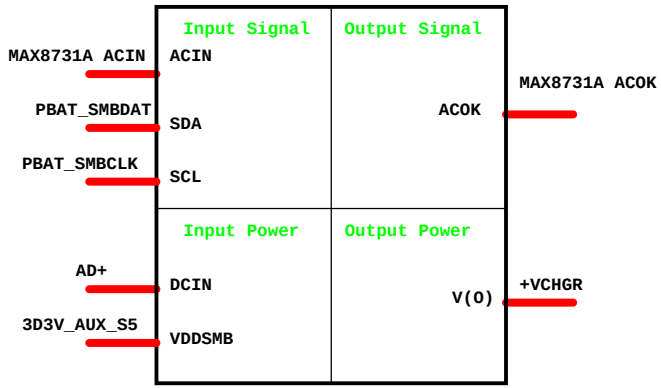


CHARGER MAX8731



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Title: **Power Block Diagram**

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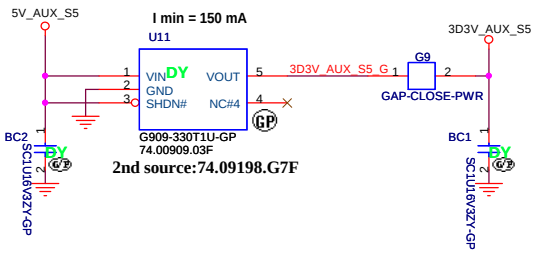
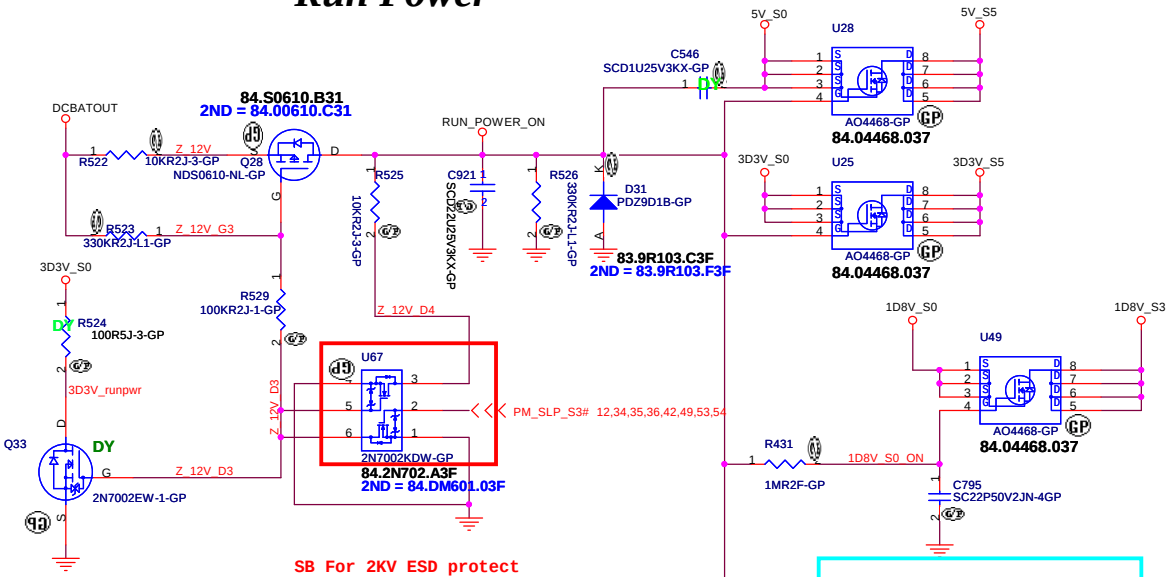
Date: Monday, October 05, 2009 Sheet 43 of 63

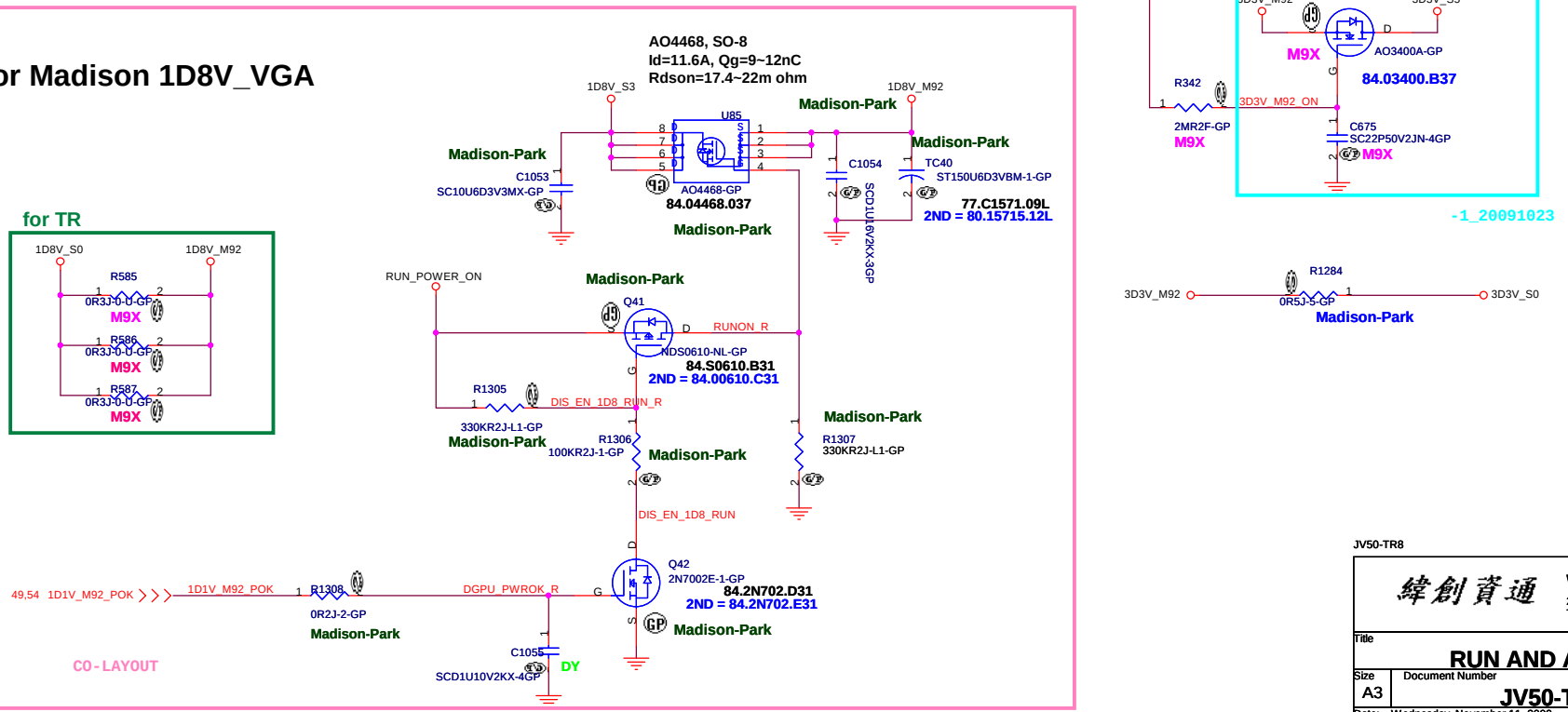
Aux Power 3D3V_AUX_S5



Run Power

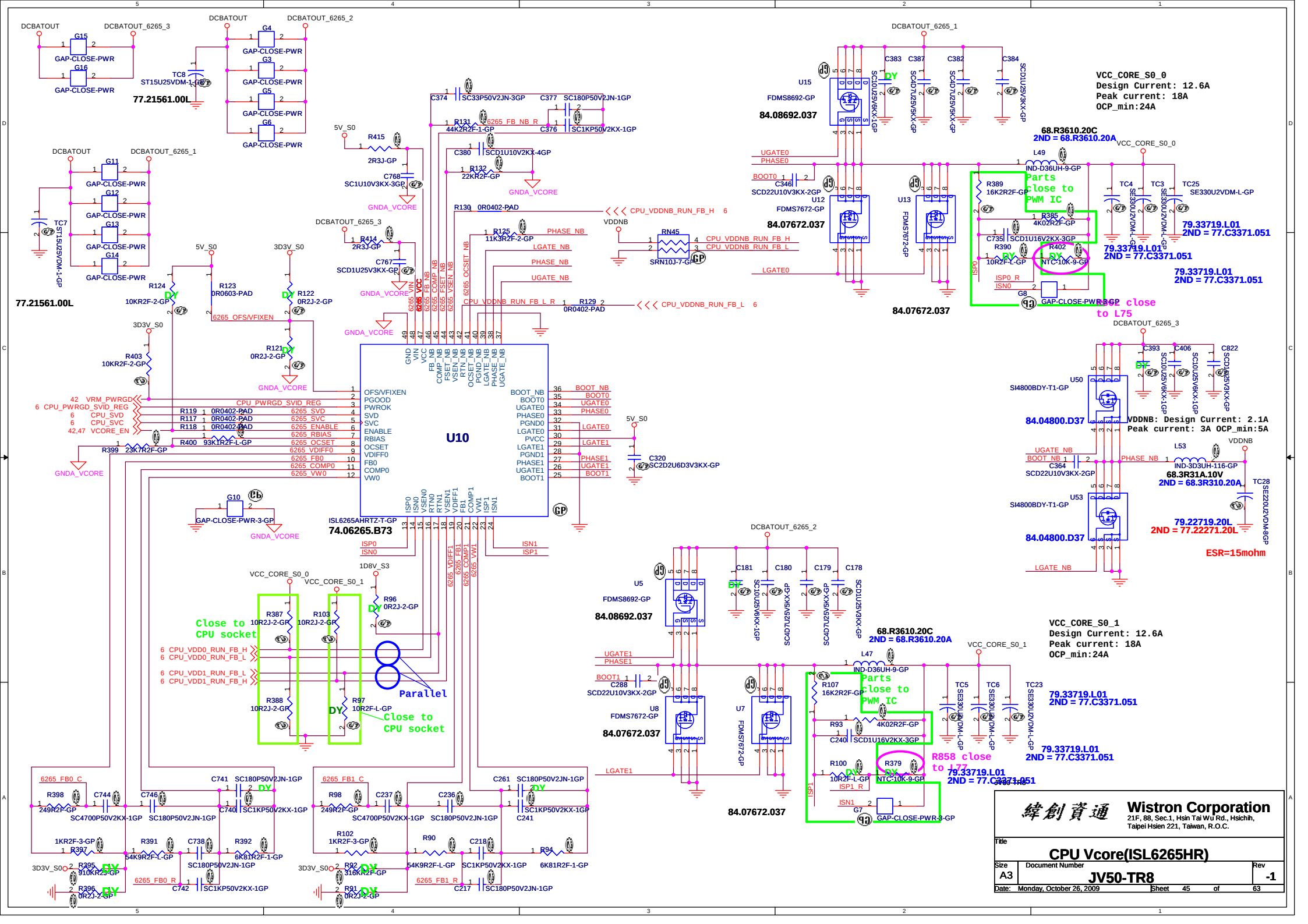


For Madison 1D8V_VGA



JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RUN AND AUX POWER		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Wednesday, November 11, 2009	Sheet 44 of 63	


U10
ISL6265AHRTZ-T-GP
74.06265.B73
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
Parts close to PWM IC
Close to CPU socket
Parallel
R858 close to L77
R379 close to L75
ESR=15mohm
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JV50-TR8
Rev -1
Monday, October 26, 2009
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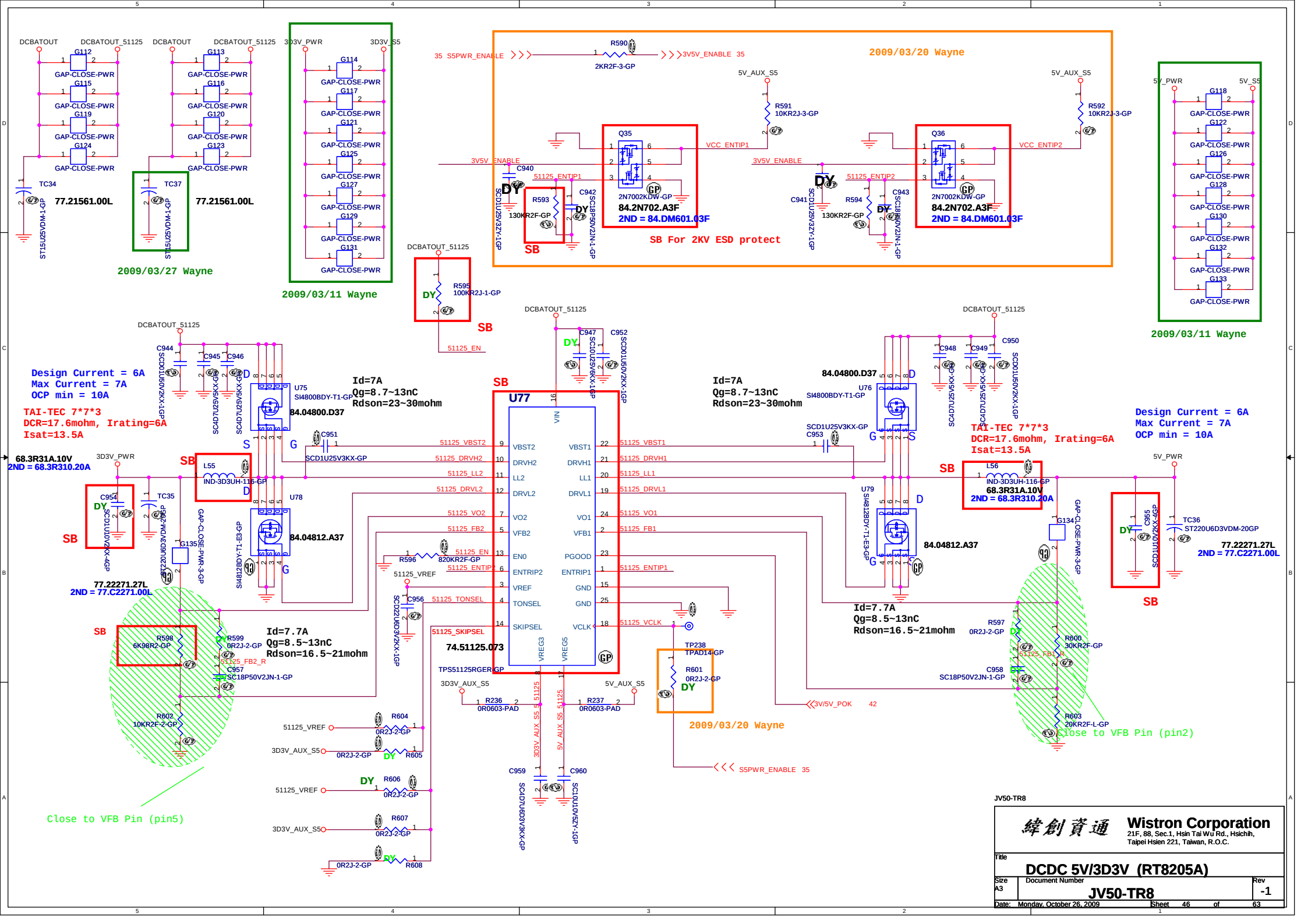
DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_PWR
5V_S5
5V_AUX_S5
35 S5PWR_ENABLE
3V5V_ENABLE 35
R590
2KR2F-3-GP
2009/03/20 Wayne
R591
10KR2J-3-GP
R592
10KR2J-3-GP
Q35
Q36
VCC_ENTIP1
VCC_ENTIP2
3V5V_ENABLE
C940
51125_ENTIP1
51125_ENTIP2
R593
130KR2F-GP
C942
SCD1U25V3ZY-1GP
SCD1U25V3KX-GP
SC18P50V2JN-1-GP
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
SB
SB For 2KV ESD protect
C941
R594
C943
DY
GP
G114
G117
G121
G125
G127
G129
G131
2009/03/11 Wayne
G118
G122
G126
G128
G130
G132
G133
GAP-CLOSE-PWR
TC34
TC37
77.21561.00L
ST15U25VDM-1-GP
2009/03/27 Wayne
G112
G113
G115
G116
G119
G120
G123
G124
R595
100KR2J-1-GP
51125_EN
Design Current = 6A
Max Current = 7A
OCP min = 10A
TAI-TEC 7*7*3
DCR=17.6mohm, Irating=6A
Isat=13.5A
68.3R31A.10V
2ND = 68.3R310.20A
C944
C945
C946
C947
C948
C949
C950
C952
SCD1U50V2KX-1GP
SC4D7U25V5KX-GP
U75
SI4800BDY-T1-GP
84.04800.D37
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
U76
U77
U78
U79
C951
C953
L55
L56
IND-3D3UH-116-GP
C954
C955
TC35
TC36
ST220U6D3VDM-20GP
77.22271.27L
2ND = 77.C2271.00L
SI4812BDY-T1-E3-GP
84.04812.A37
G135
G134
GAP-CLOSE-PWR-3-GP
R596
820KR2F-GP
51125_VREF
C956
SCD22U6D3V2KX-1GP
51125_TONSEL
51125_SKIPSEL
74.51125.073
TPS51125RGER-GP
VIN
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
GND
VCLK
VREG3
VREG5
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_ENTIP1
51125_VCLK
R597
0R2J-2-GP
R598
6K98R2-GP
R599
0R2J-2-GP
R600
30KR2F-GP
R601
0R2J-2-GP
R602
10KR2F-2-GP
R603
20KR2F-L-GP
C957
SC18P50V2JN-1-GP
C958
TP238
TPAD14-GP
R604
R605
R606
R607
R608
C959
C960
SCD1U10V2KX-4GP
SCD1U10V2ZY-1GP
R236
R237
0R0603-PAD
3D3V_AUX_S5
5V_AUX_S5
3V/5V_POK 42
S5PWR_ENABLE 35
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
JV50-TR8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (RT8205A)
Size
A3
Document Number
JV50-TR8
Rev
-1
Date: Monday, October 26, 2009
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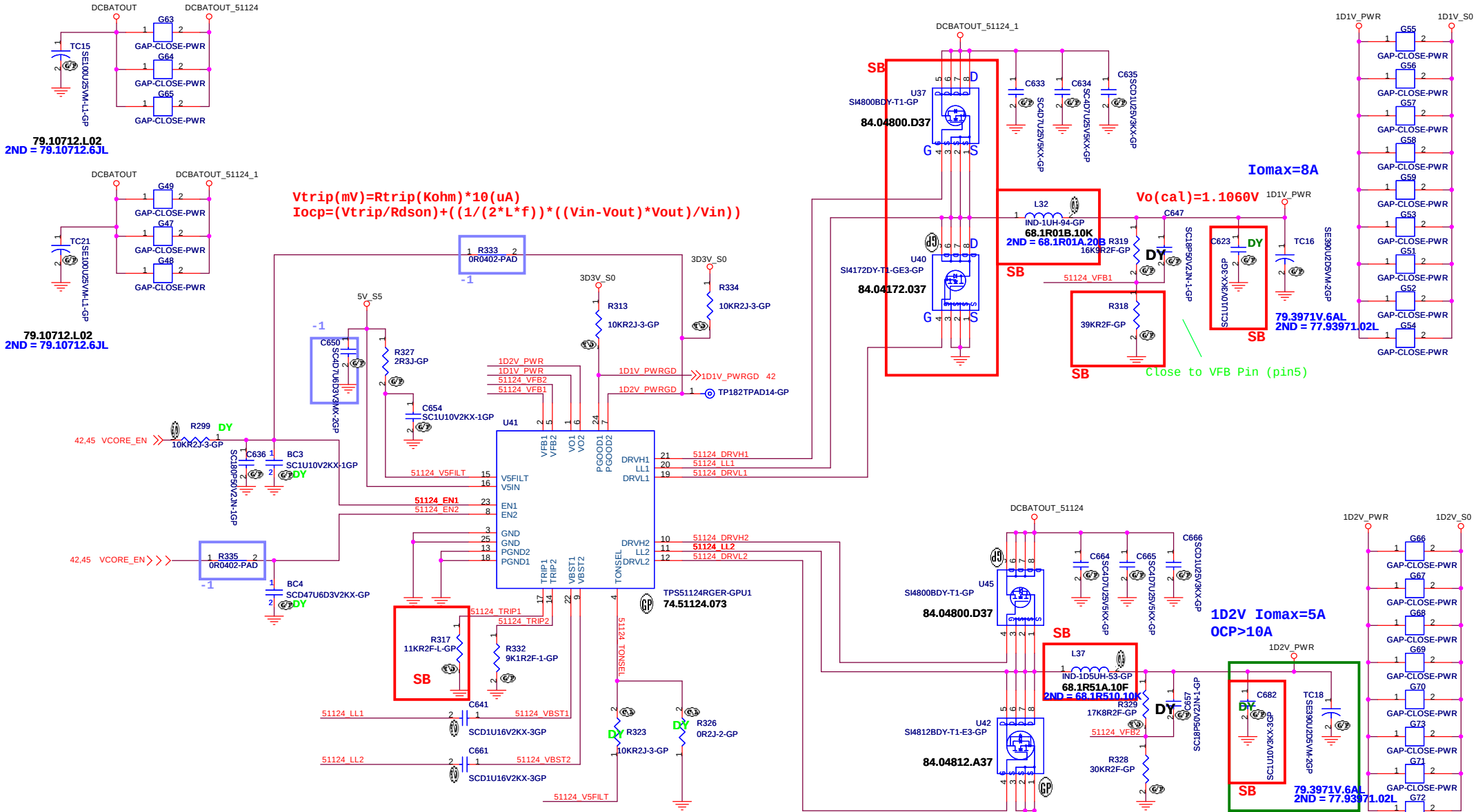

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

Size	Document Number	Rev
A3	JV50-TR8	-1

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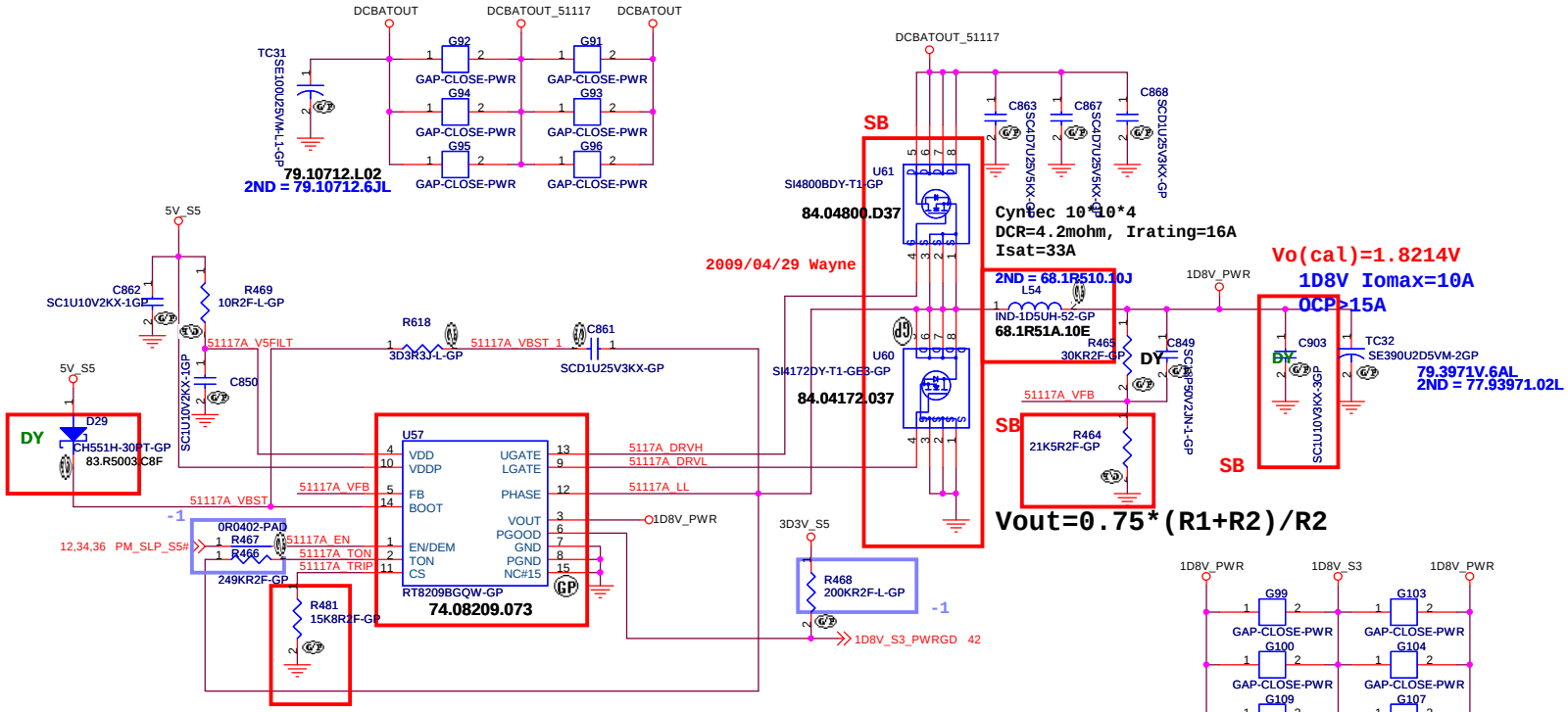

JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DCDC_1D8V_RT8209B/LDO 0D9V		
Size: A3	Document Number: JV50-TR8	Rev: -1
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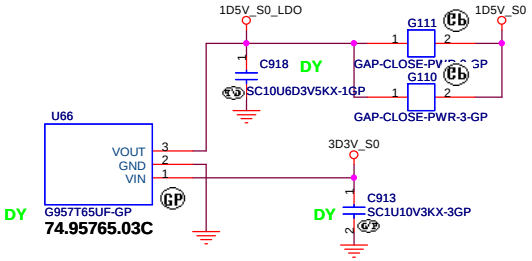
G957

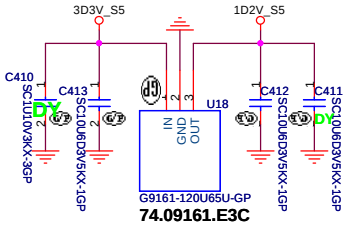
1D5V_S0
Iomax=1A



For MINI Card.NEW Card power SW

G9161

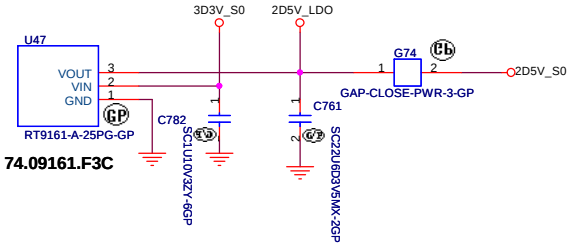
1D2V_S5
Iomax=400mA



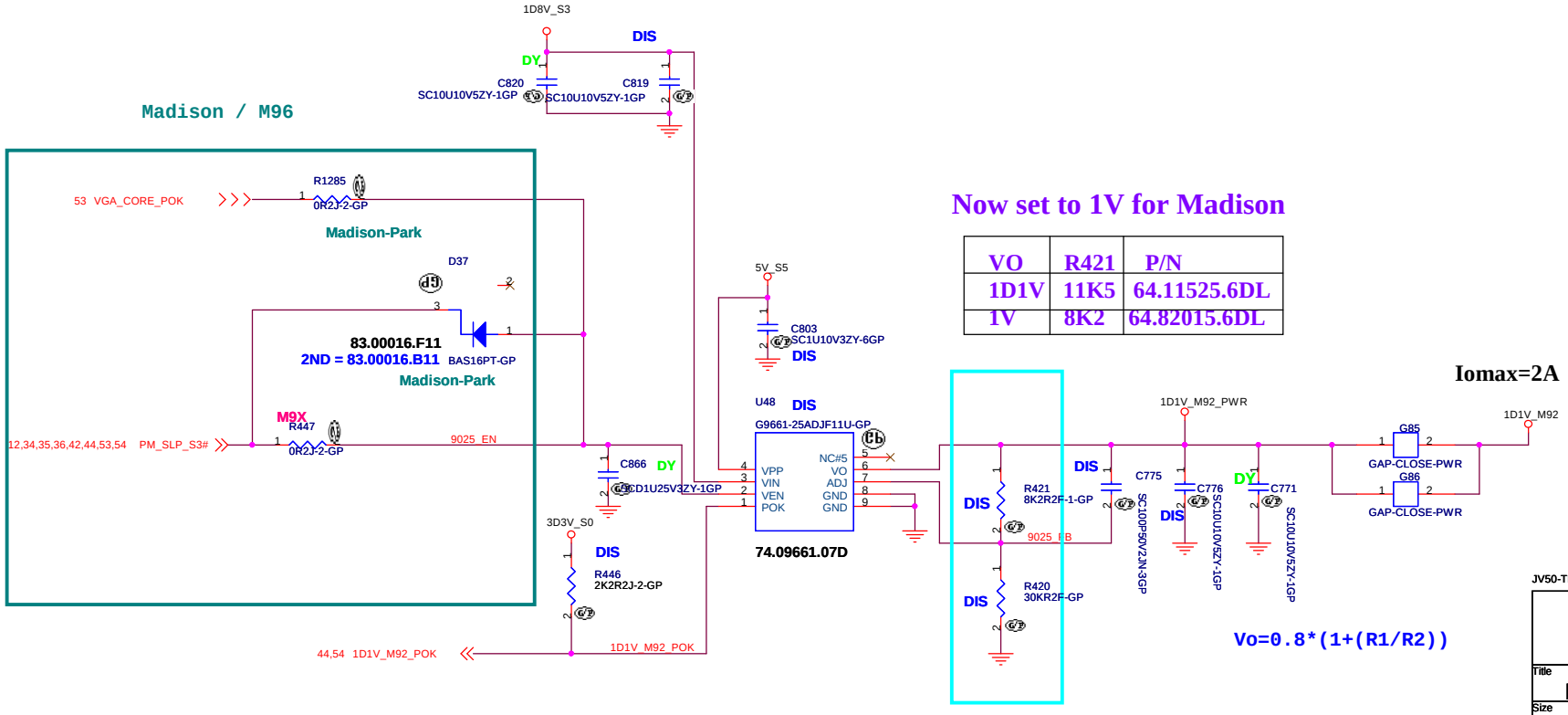
Place near to SB710

RT9161A

2D5V
Iomax=0.2A



Place near to CPU



JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 2D5V/1D5V/1D2V_S5/1V_VGA

Size: A3 | Document Number: JV50-TR8 | Rev: -1

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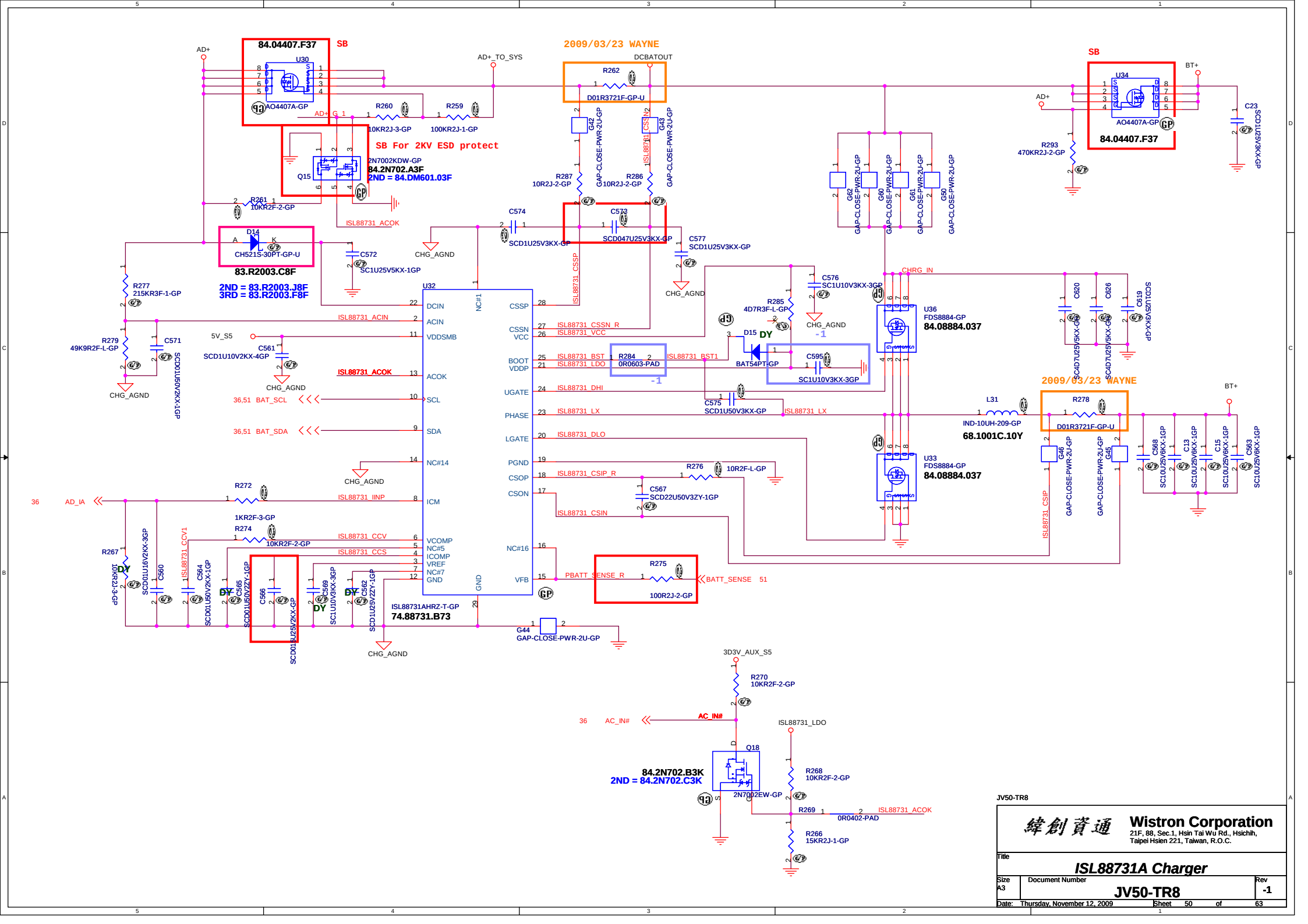
84.04407.F37
SB
U30
AO4407A-GP
AD+
AD+_TO_SYS
2009/03/23 WAYNE
DCBATOUT
R262
D01R3721F-GP-U
SB For 2KV ESD protect
Q15
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
R260
10KR2J-3-GP
R259
100KR2J-1-GP
R261
10KR2F-2-GP
ISL88731_ACOK
D14
CH521S-30PT-GP-U
83.R2003.C8F
2ND = 83.R2003.J8F
3RD = 83.R2003.F8F
C572
SC1U25V5KX-1GP
CHG_AGND
C574
SCD1U25V3KX-GP
C573
SCD047U25V3KX-GP
C577
SCD1U25V3KX-GP
R287
10R2J-2-GP
R286
10R2J-2-GP
GAP-CLOSE-PWR-2U-GP
ISL88731_CSSP
ISL88731_CSSN
G42
G43
G62
G60
G61
G50
U34
AO4407A-GP
84.04407.F37
BT+
R293
470KR2J-2-GP
C23
SCD1U25V5KX-GP
R277
215KR3F-1-GP
R279
49K9R2F-L-GP
C571
SCD1U50V2KX-1GP
5V_S5
C561
SCD1U10V2KX-4GP
U32
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731_ACIN
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST
ISL88731_LDO
ISL88731_BST1
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
ISL88731_IINP
ISL88731_CCV
ISL88731_CCS
PBATT_SENSE_R
ISL88731AHRZ-T-GP
74.88731.B73
R284
0R0603-PAD
R285
4D7R3F-L-GP
D15
BAT54PT-GP
DY
C595
SC1U10V3KX-3GP
C576
SC1U10V3KX-3GP
C575
SCD1U50V3KX-GP
CHRG_IN
U36
FDS8884-GP
84.08884.037
U33
FDS8884-GP
84.08884.037
L31
IND-10UH-209-GP
68.1001C.10Y
2009/03/23 WAYNE
R278
D01R3721F-GP-U
C620
C626
C619
SC4D7U25V5KX-GP
C568
C13
C15
C563
SC10U25V6KX-1GP
R272
1KR2F-3-GP
R274
10KR2F-2-GP
R267
10KR2J-3-GP
C560
C564
C565
C566
C569
C562
SCD01U16V2KX-3GP
SCD01U50V2KX-1GP
SCD01U50V2ZY-1GP
SCD01U25V2KX-GP
SC1U10V3KX-3GP
SCD1U25V2ZY-1GP
R276
10R2F-L-GP
C567
SCD22U50V3ZY-1GP
R275
100R2J-2-GP
BATT_SENSE
G44
GAP-CLOSE-PWR-2U-GP
G46
G45
GAP-CLOSE-PWR-2U-GP
3D3V_AUX_S5
R270
10KR2F-2-GP
AC_IN#
Q18
2N7002EW-GP
84.2N702.B3K
2ND = 84.2N702.C3K
R268
10KR2F-2-GP
R269
0R0402-PAD
R266
15KR2J-1-GP
JV50-TR8
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
JV50-TR8
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-1
Date: Thursday, November 12, 2009
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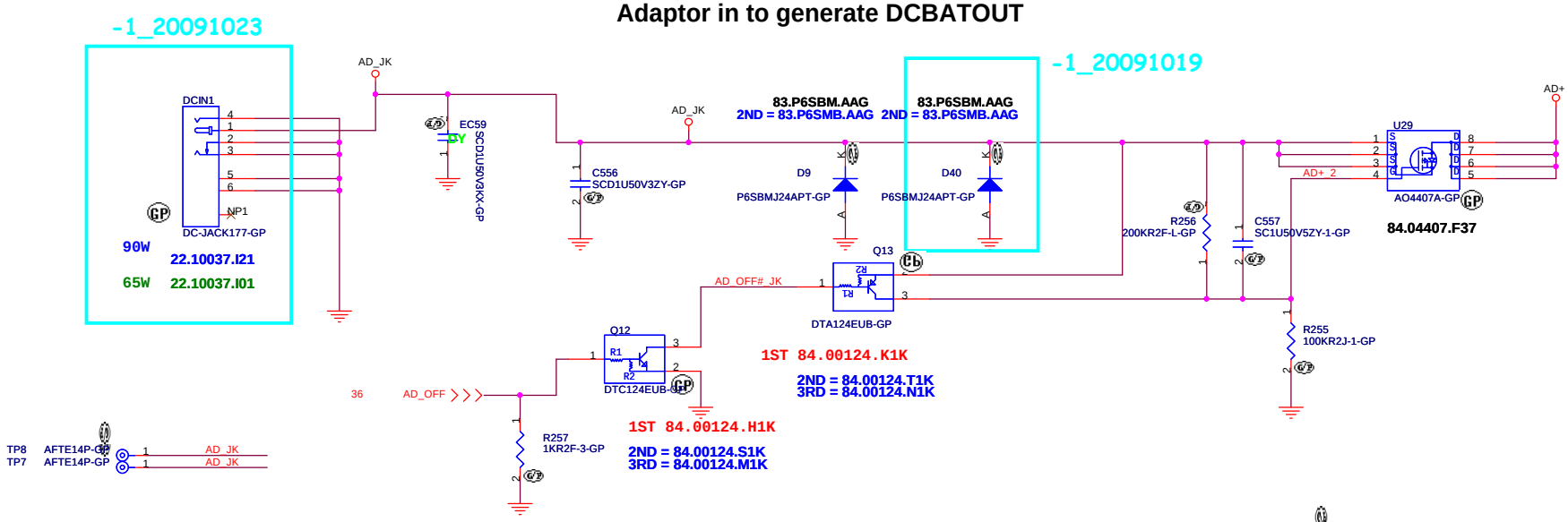
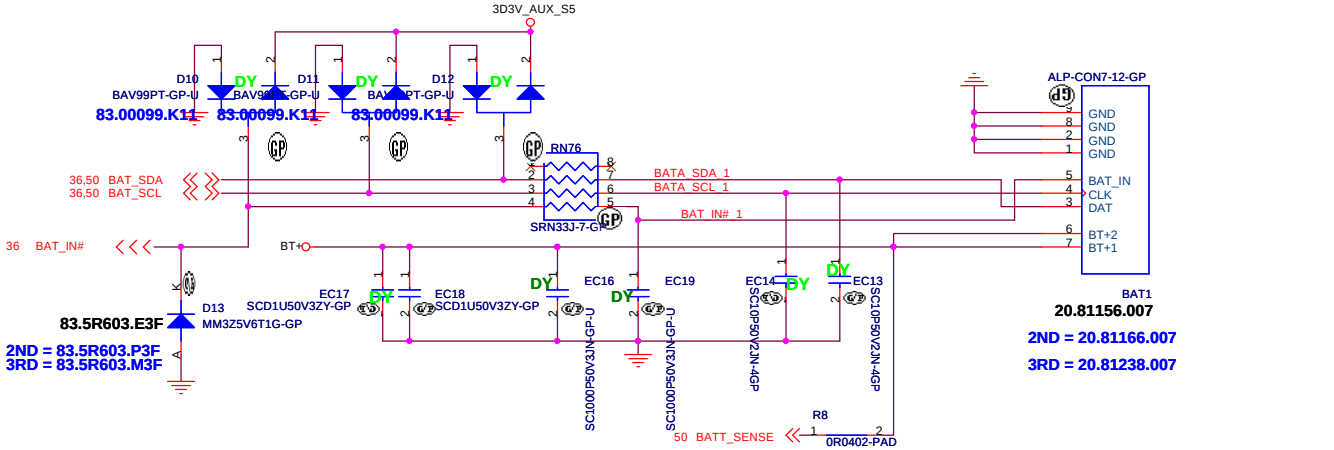
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AD/BATT CONN	
Size	Document Number JV50-TR8	Rev -1
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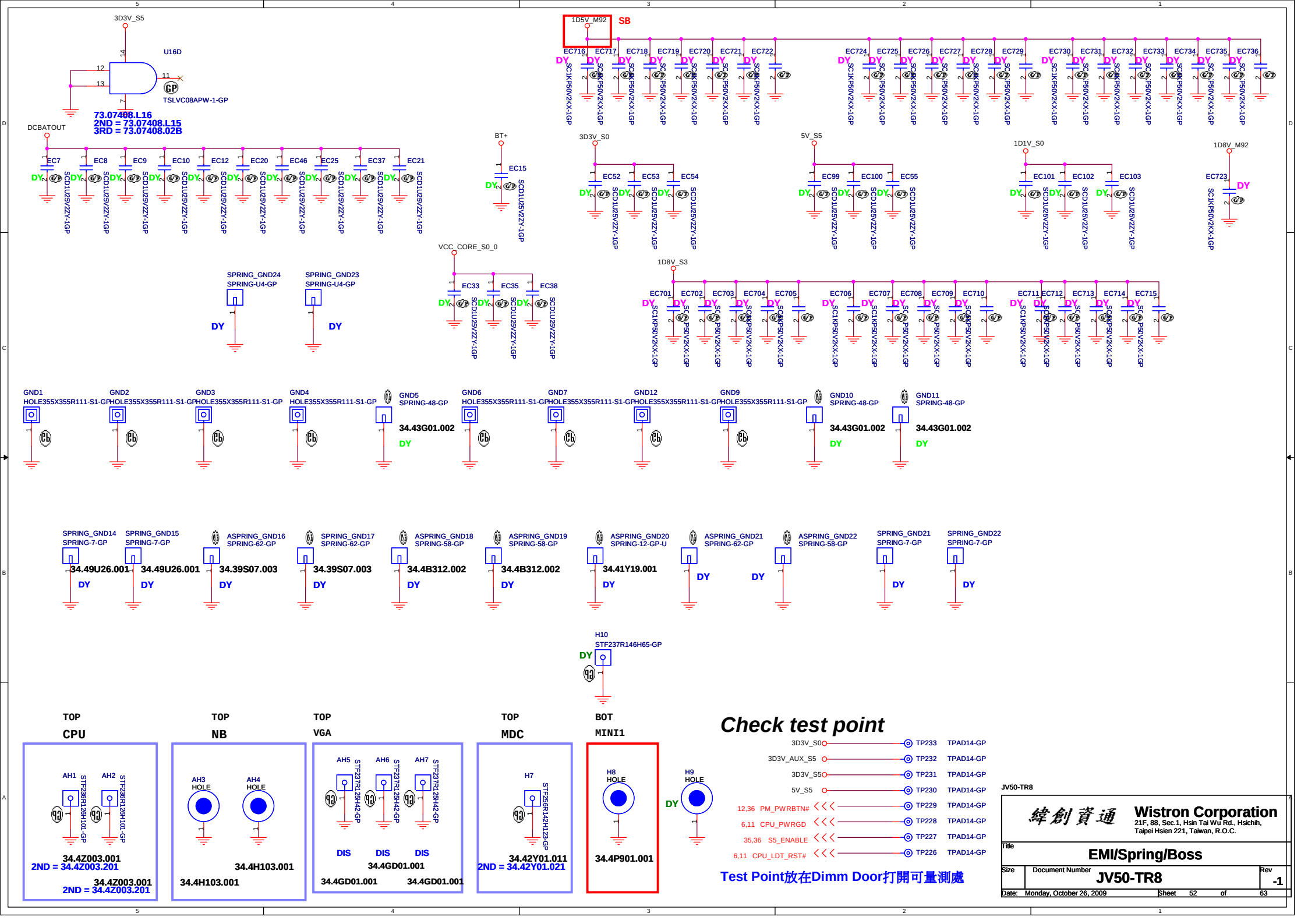
3D3V_S5
U16D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
DCBATOUT
EC7 EC8 EC9 EC10 EC12 EC20 EC46 EC25 EC37 EC21
SCD1U25V2ZY-1GP
BT+
EC15
VCC_CORE_S0_0
EC33 EC35 EC38
1D5V_M92
SB
EC716 EC717 EC718 EC719 EC720 EC721 EC722
EC724 EC725 EC726 EC727 EC728 EC729 EC730 EC731 EC732 EC733 EC734 EC735 EC736
SC1KP50V2KX-1GP
3D3V_S0
EC52 EC53 EC54
5V_S5
EC99 EC100 EC55
1D1V_S0
EC101 EC102 EC103
1D8V_M92
EC723
SC1KP50V2KX-1GP
1D8V_S3
EC701 EC702 EC703 EC704 EC705 EC706 EC707 EC708 EC709 EC710 EC711 EC712 EC713 EC714 EC715
SC1KF50V2KX-1GP
SC4K7F50V2KX-1GP
SC6P50V2KX-1GP
SPRING_GND24
SPRING-U4-GP
SPRING_GND23
SPRING-U4-GP
GND1 HOLE355X355R111-S1-GP
GND2 HOLE355X355R111-S1-GP
GND3 HOLE355X355R111-S1-GP
GND4 HOLE355X355R111-S1-GP
GND5 SPRING-48-GP
34.43G01.002
GND6 HOLE355X355R111-S1-GP
GND7 HOLE355X355R111-S1-GP
GND12 HOLE355X355R111-S1-GP
GND9 HOLE355X355R111-S1-GP
GND10 SPRING-48-GP
34.43G01.002
GND11 SPRING-48-GP
34.43G01.002
SPRING_GND14 SPRING-7-GP
34.49U26.001
SPRING_GND15 SPRING-7-GP
34.49U26.001
ASPRING_GND16 SPRING-62-GP
34.39S07.003
SPRING_GND17 SPRING-62-GP
34.39S07.003
ASPRING_GND18 SPRING-58-GP
34.4B312.002
ASPRING_GND19 SPRING-58-GP
34.4B312.002
ASPRING_GND20 SPRING-12-GP-U
34.41Y19.001
ASPRING_GND21 SPRING-62-GP
ASPRING_GND22 SPRING-58-GP
SPRING_GND21 SPRING-7-GP
SPRING_GND22 SPRING-7-GP
H10 STF237R146H65-GP
DY
TOP
CPU
AH1 STF236R126H101-GP
AH2 STF236R126H101-GP
34.4Z003.001
2ND = 34.4Z003.201
34.4Z003.001
2ND = 34.4Z003.201
TOP
NB
AH3 HOLE
AH4 HOLE
34.4H103.001
34.4H103.001
TOP
VGA
AH5 STF237R125H42-GP
AH6 STF237R125H42-GP
AH7 STF237R125H42-GP
DIS DIS DIS
34.4GD01.001
34.4GD01.001 34.4GD01.001
TOP
MDC
H7 STF256R142H123-GP
34.42Y01.011
2ND = 34.42Y01.021
BOT
MINI1
H8 HOLE
34.4P901.001
H9 HOLE
DY
Check test point
3D3V_S0 TP233 TPAD14-GP
3D3V_AUX_S5 TP232 TPAD14-GP
3D3V_S5 TP231 TPAD14-GP
5V_S5 TP230 TPAD14-GP
12,36 PM_PWRBTN# TP229 TPAD14-GP
6,11 CPU_PWRGD TP228 TPAD14-GP
35,36 S5_ENABLE TP227 TPAD14-GP
6,11 CPU_LDT_RST# TP226 TPAD14-GP
Test Point放在Dimm Door打開可量測處
JV50-TR8
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
JV50-TR8
Rev
-1
Date: Monday, October 26, 2009
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RT8209E for VGA

Iomax=23A, OCP>40A

DCBATOUT
DCBATOUT_8209E_VGA
G136 GAP-CLOSE-PWR
G138 GAP-CLOSE-PWR
G140 GAP-CLOSE-PWR
G142 GAP-CLOSE-PWR
5V_S5
C1037 DIS SC1U10V2KX-3GP
R1286 DIS 10R2F-L-GP
C1041 DIS SC1U10V2KX-1GP
D36 DY B0530WS-7-F-GP
R1287 3D3R3J-L-GP DIS
8209A_R_BOOT_VGA
C1038 SCD1U16V2KX-3GP DIS
U81 DIS RT8209EGQW-GP
8209A_VDD_VGA
RT8209_FB_VGA
8209A_BOOT
8209A_EN/DEM_VGA
8209A_TON_VGA
8209A_CS_VGA
8209A_HGATE_VGA
8209A_LGATE_VGA
8209A_PHASE_VGA
8209A_PGOOD_VGA
VGA_CORE_PWR
R1288 8K2R2F-1-GP DIS
R1290 220KR2F-GP DIS
-1_20091021
3D3V_S0
R1291 10KR2J-3-GP DIS
R1292 0R0402-PAD-1-GP
VGA_CORE_POK 49
C1042 SC100P50V2JN-3GP DIS
12,34,35,36,42,44,49,54 PM_SLP_S3#
R1289 10KR2J-3-GP M9X
D38 BAS16PT-GP
83.00016.F11
2ND = 83.00016.B11
Madison-Park
R1293 10KR2J-3-GP Madison-Park
3D3V_M92
C1043 16KR3F-GP DIS
U80 SIR474DP-T1-GE3-GP DIS
U82 SIR460DP-T1-GE3-GP DIS
U83 SIR460DP-T1-GE3-GP DIS
C1039 C1040 C1056 SC10U25V5KX-GP DIS
DCBATOUT_8209E_VGA
L62 IND-D45UH-14-GP DIS
-1_20091021
VGA_CORE_PWR
TC38 TC39 SE330U2VDM-L-GP DIS
79.33719.L01
79.33719.L01
VCC_GFX_CORE
G137 G139 G141 G143 G144 G145 G146 G147 G148 G149 G150 G151 G152 G153 G154 G155 G156 G157 G158 G159 G160 G161 GAP-CLOSE-PWR

Vout=0.75*(1+Rh/Rl)

DY C1044 SC47P50V2JN-3GP
R1294 10KR2F-2-GP DIS
RT8209_FB_VGA
R1295 49K9R2F-L-GP DIS
R1296 110KR2F-L-GP DY
NV_VID1_Q
Q39 84.2N702.B3K
2ND = 84.2N702.C3K
2N7002EW-GP
R1298 NV_VID1 DY 10KR2J-3-GP
PWRCNTL_1 56
C1046 SCD1U10V2KX-4GP DY
R1297 73K2R2F-GP DIS
NV_VID0_Q
Q40 2N7002EW-GP
84.2N702.B3K
2ND = 84.2N702.C3K
-1_20091019
3D3V_S0
R1309 100KR2J-1-GP DIS
NV_VID0_R
Q45 MMBT2222A-3-GP
R1299 NV_VID0 DIS 10KR2J-3-GP
PWRCNTL_0 56
C1045 SCD1U10V2KX-4GP DIS

M92 XT			
R1295	37.4K	R1297	30K
VGA_CORE	1.20V		

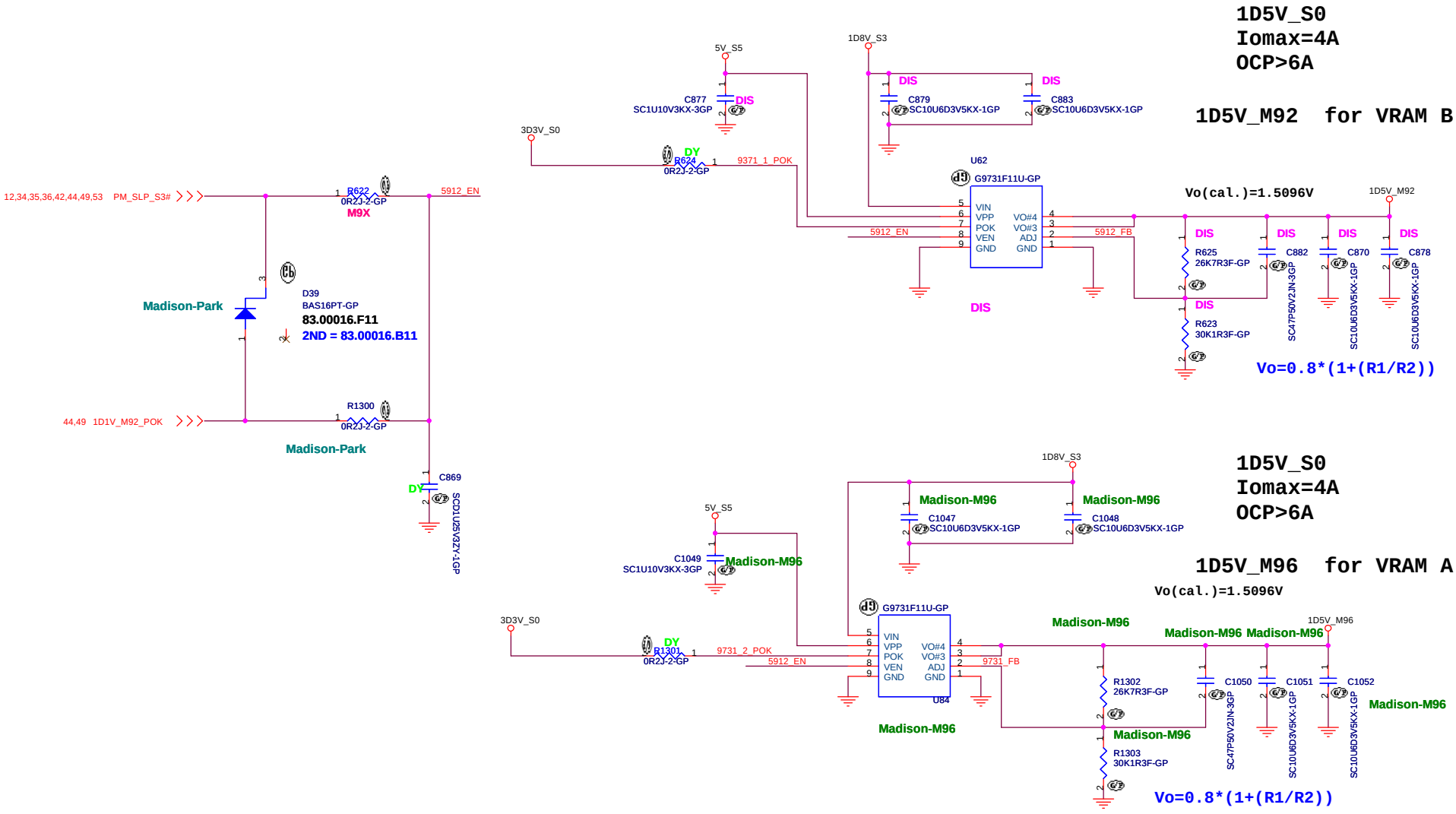
30k(64.30025.6DL)
73.2k(64.73225.6DL)
37.4k (64.37425.6DL)

	Madison Pro	Park XT	M96 Pro
R1297	73.2K	36.5K	30K
VGA_CORE	1.00V	1.12V	1.15V

	Madison Pro	Park XT	M96 Pro	M92-XT
PWRCNTL_0				
0	1.00V	1.12V	1.15V	1.20V
1	0.90V	0.90V	0.90V	0.95V

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E VGA CORE
Size: A3
Document Number: JV50-TR8
Rev: -1
Date: Thursday, November 12, 2009
Sheet 53 of 63



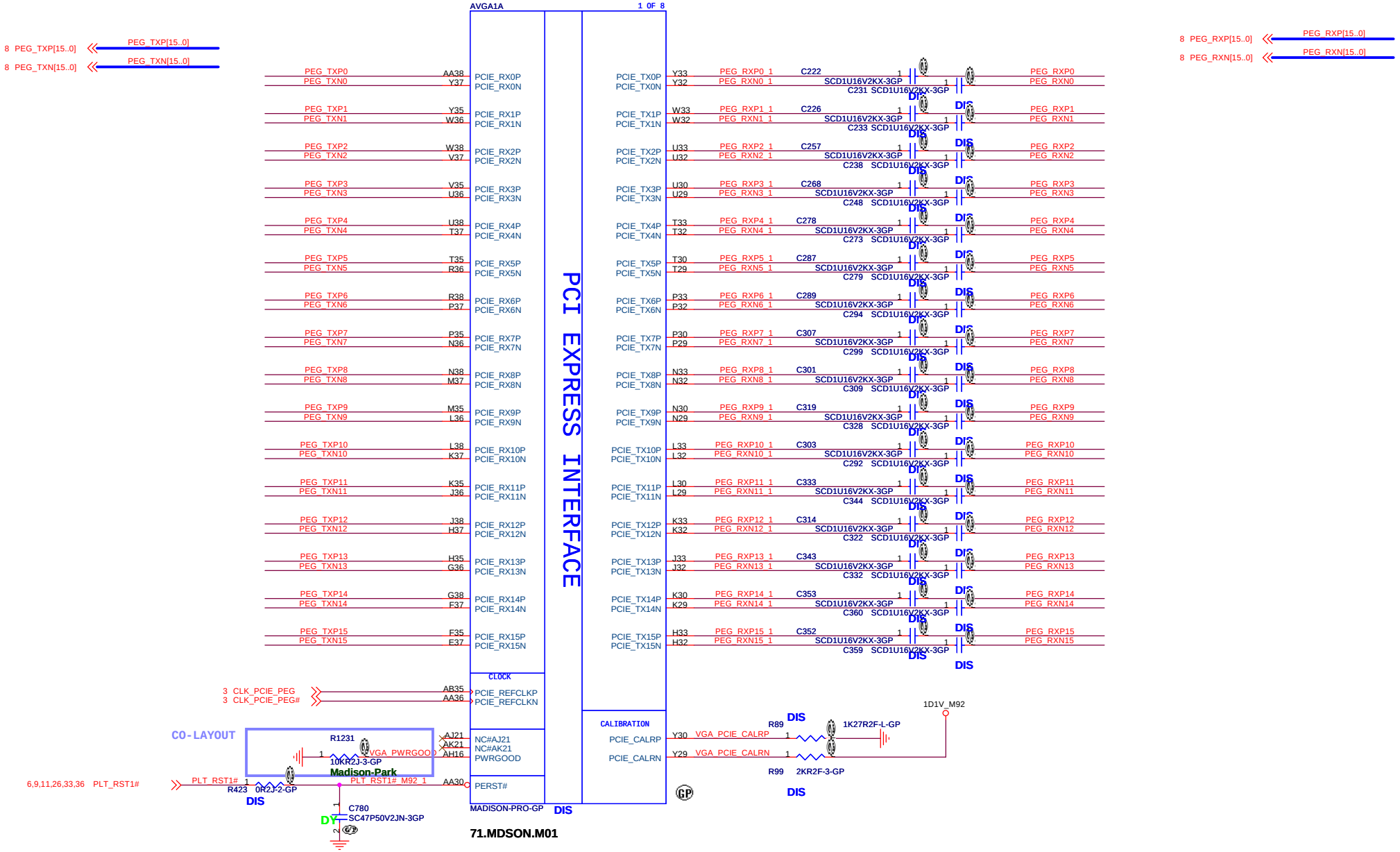
JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G9731_1D5V_VRAM POWER

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Wednesday, November 11, 2009 Sheet 54 of 63



DIS / UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Madison PCIE**	
Size: A3	Document Number: **JV71-TR**	Rev: **-1**
Date: Monday, October 26, 2009	Sheet 55 of 63	

Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request

DVPDATA [3:0]
0100 1GB GDDR3 Hynix-H5TQ1G63BFR-12C (800MHz)
1000 1GB GDDR3 Samsung-K4W1G1646E-HC12 (800MHz)
1100 1GB GDDR3 ATI (800MHz)

It's strap for GDDR3-136ball
Need to Clarify

Back Bias (body bias) which minimizes
power consumption in battery modes.
PD = Disable
PU = Enable

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

For Thermal sensor

for TR

71.MDSON.M01

71.MDSON.M01

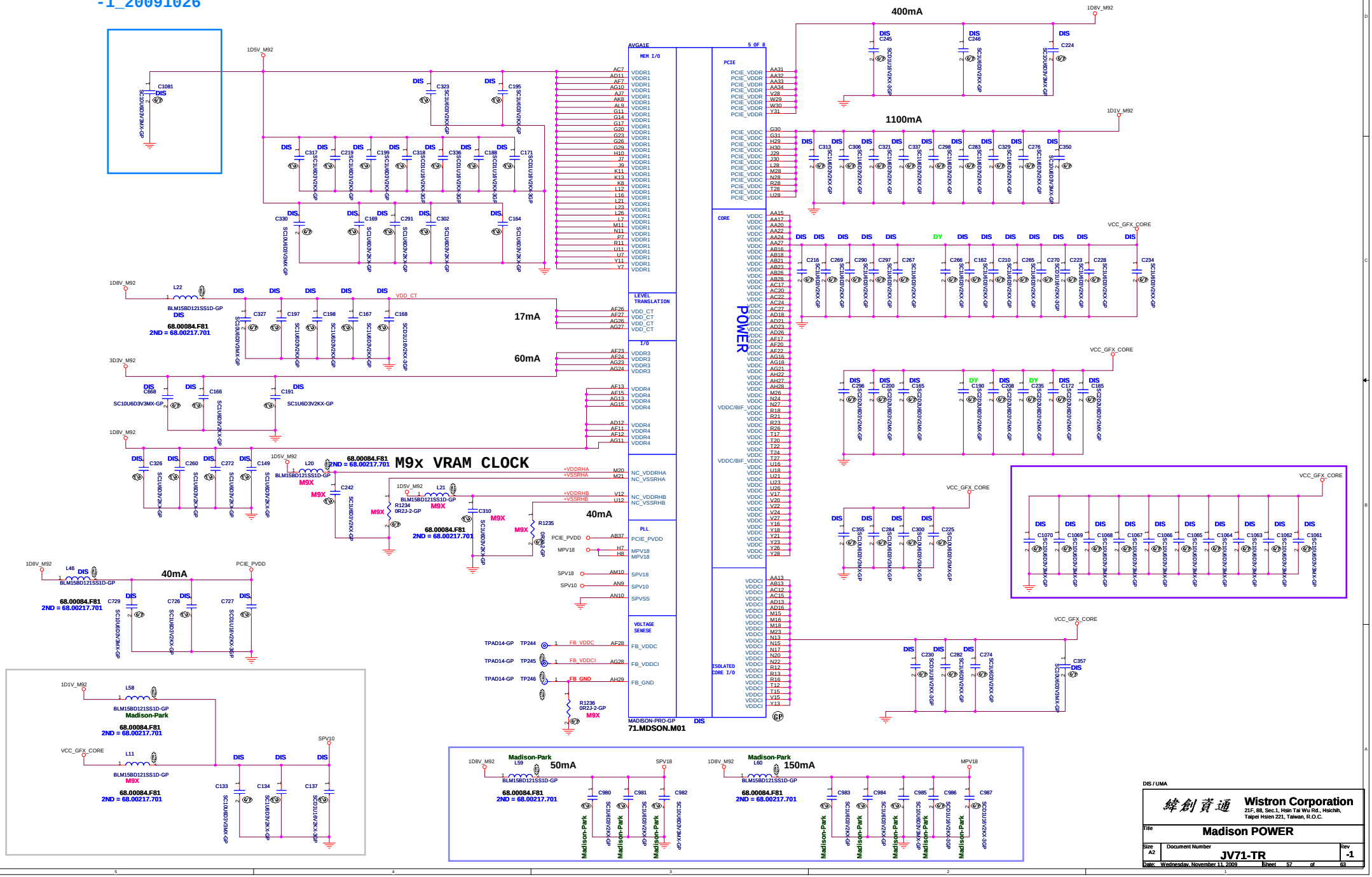
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

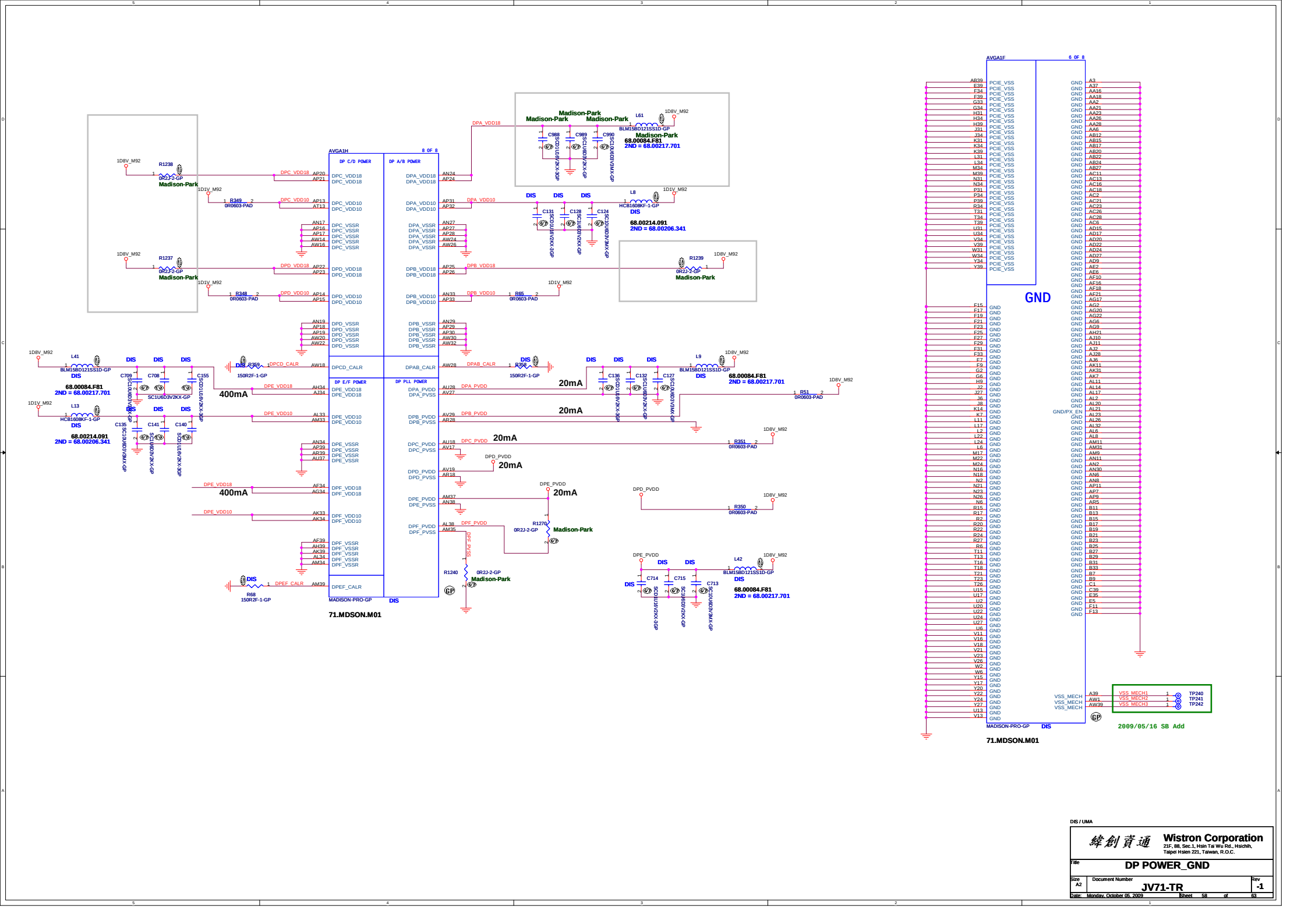
Title: Madison IO

Size: A2 | Document Number: JV71-TR | Rev: -1

Date: Wednesday, November 11, 2009 | Sheet 56 of 63

-1_20091026


400mA
1100mA
17mA
60mA
40mA
M9x VRAM CLOCK
50mA
150mA
AVGA1E
MEM I/O
PCIE
CORE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
ISOLATED CORE I/O
POWER
MADISON-PRO-GP
71.MDSON.M01
Madison-Park
68.00084.F81
2ND = 68.00217.701
Wistron Corporation
Madison POWER
JV71-TR


AVGA1H
8 OF 8
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
MADISON-PRO-GP
DIS
71.MDSON.M01
Madison-Park
68.00084.F81
2ND = 68.00217.701
68.00214.091
2ND = 68.00206.341
20mA
400mA
AVGA1F
6 OF 8
GND
MADISON-PRO-GP
71.MDSON.M01
2009/05/16 SB Add
DIS / UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DP POWER_GND
Size A2
Document Number
JV71-TR
Rev -1
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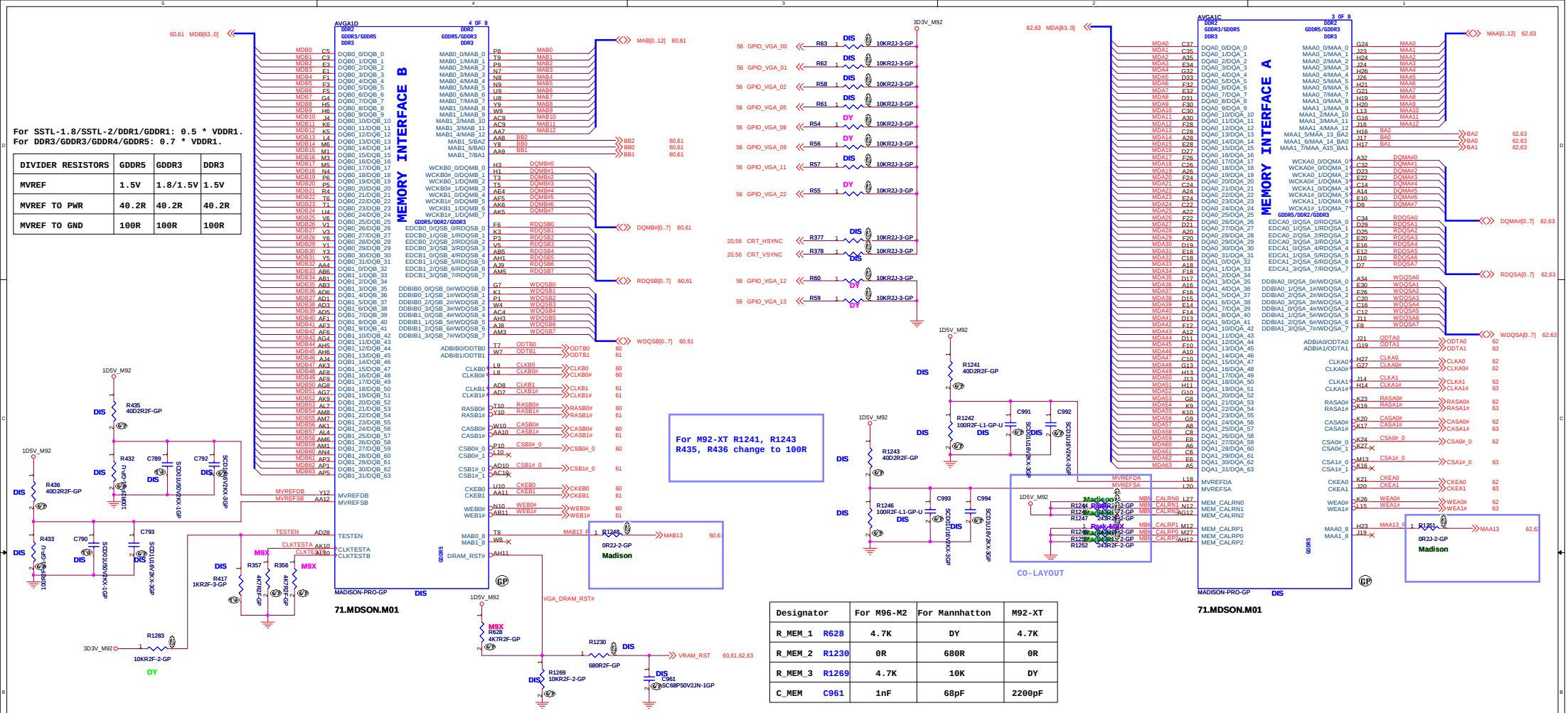
For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



Designator		For M96-M2	For Mannhatton	M92-XT
R_MEM_1	R628	4.7K	DY	4.7K
R_MEM_2	R1230	0R	680R	0R
R_MEM_3	R1269	4.7K	10K	DY
C_MEM	C961	1nF	68pF	2200pF

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
V 256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison Memory / Straps

Size	Document Number	Rev
A2	JV71-TR	-1

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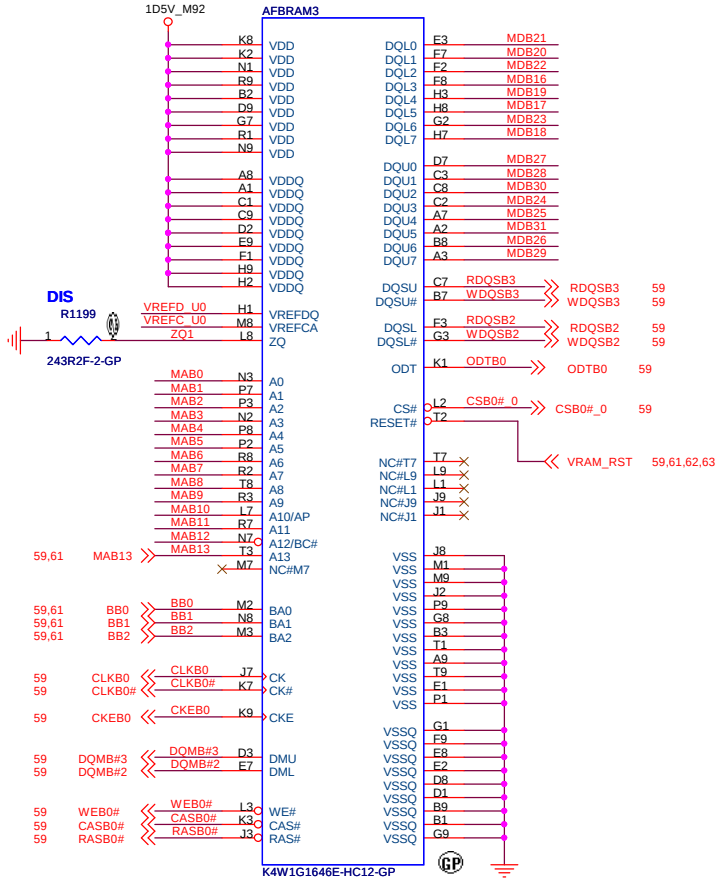
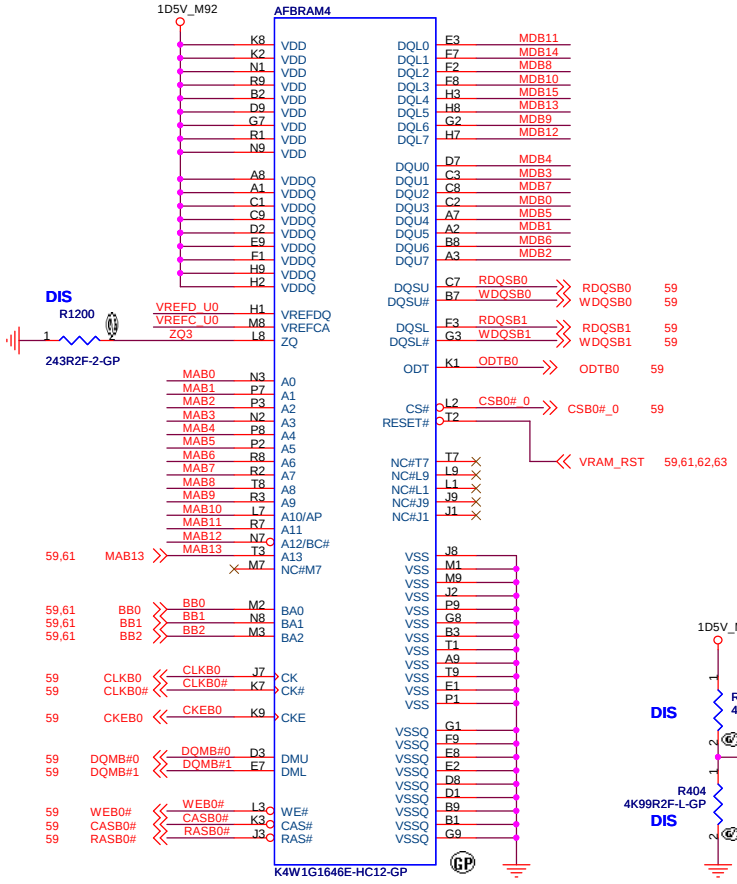
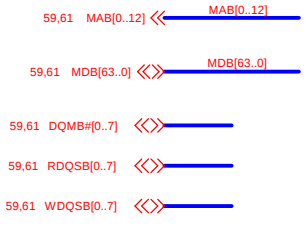
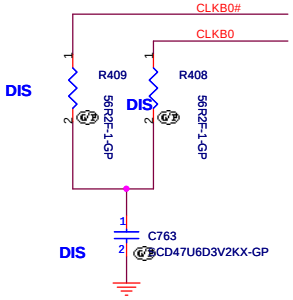
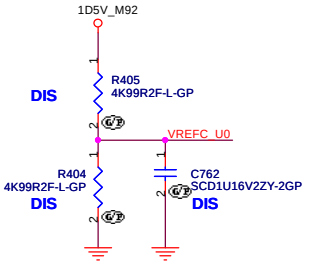
GDDR3

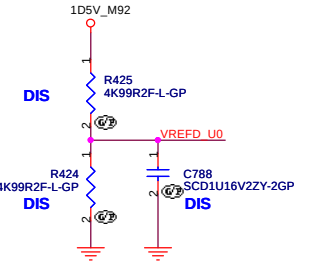












DIS

72.41164.H0U

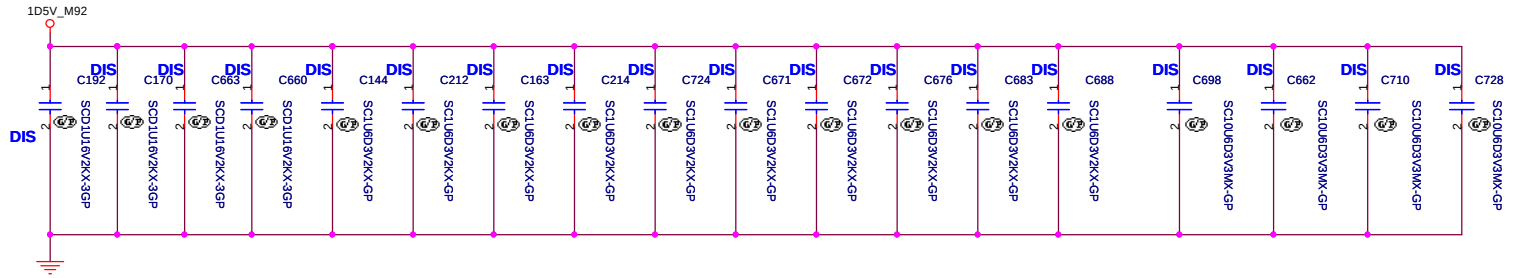
2ND = 72.51G63.C0U

SAMSUNG 1ST=72.41164.H0U
HYUNIX 2ND=72.51G63.C0U

DIS

72.41164.H0U

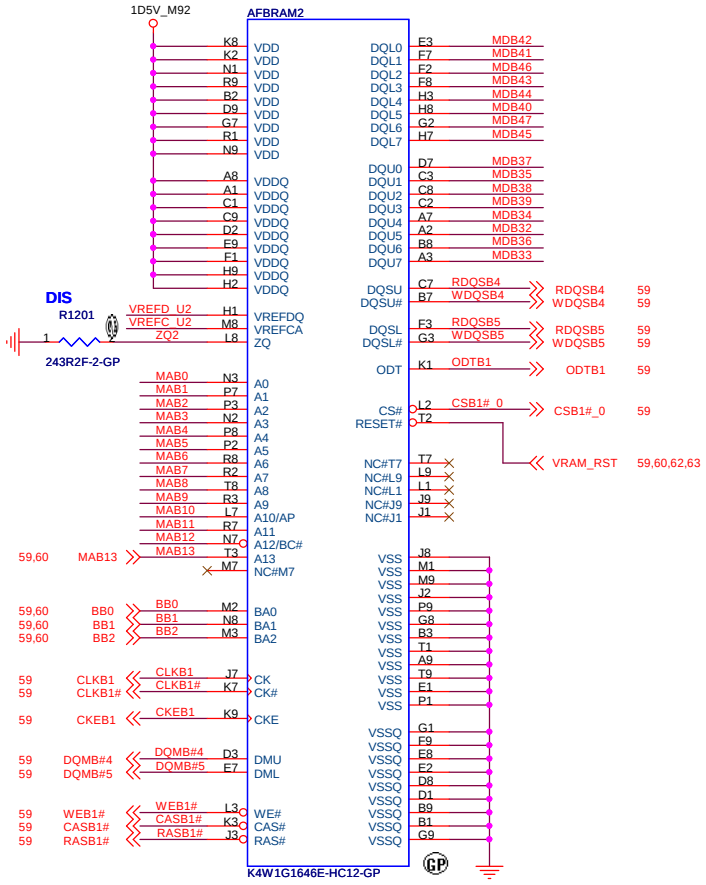
2ND = 72.51G63.C0U

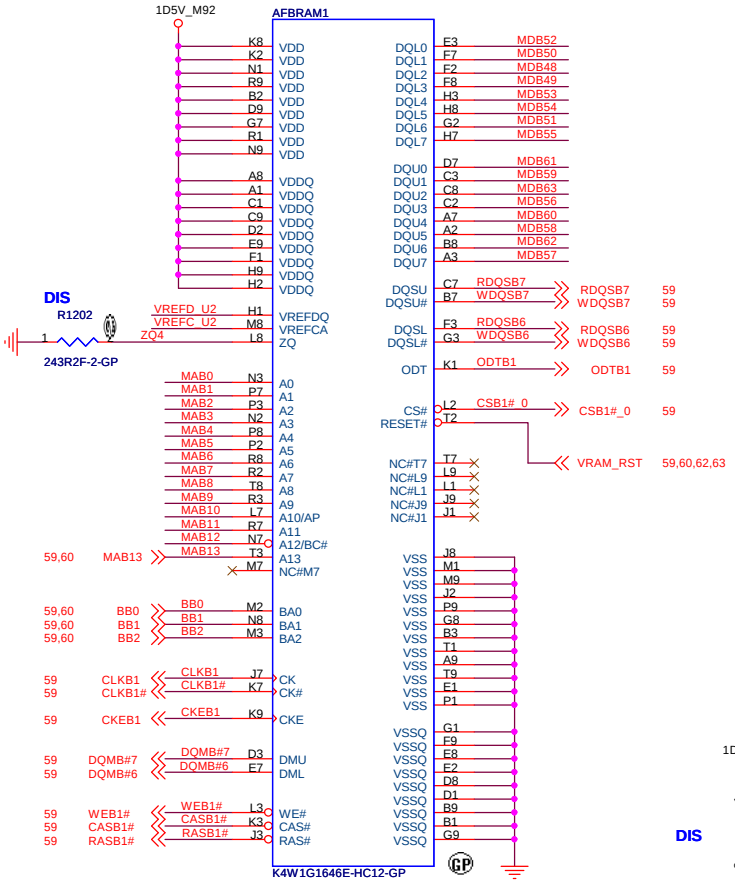


JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 DDR3 B0		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 60 of 63	

GDDR3





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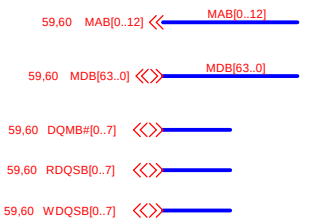
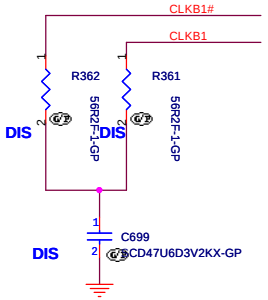
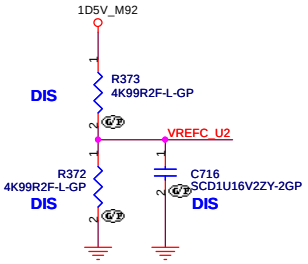
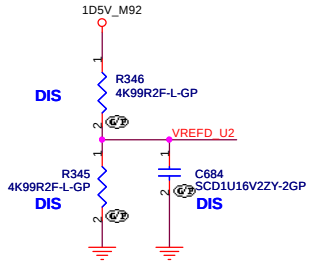
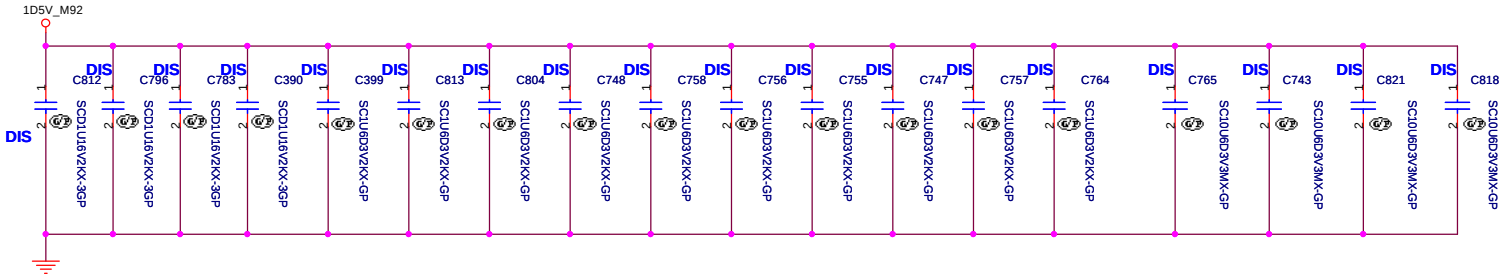
HYUNIX 2ND=72.51G63.C0U









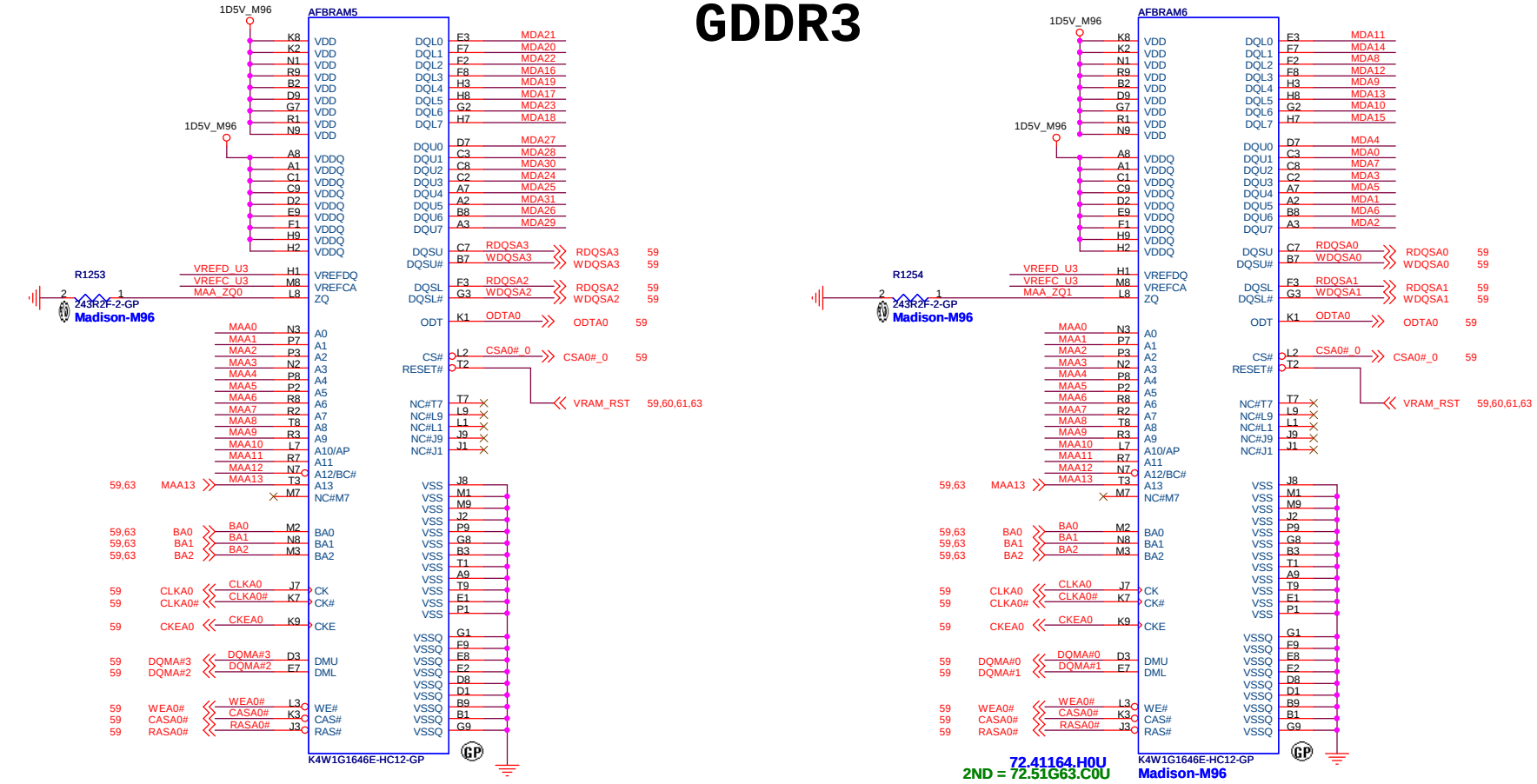


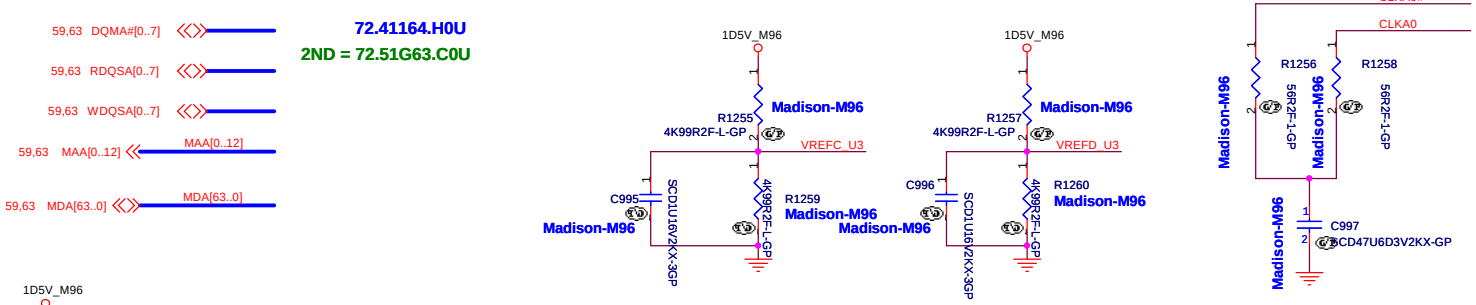
JV50-TR8

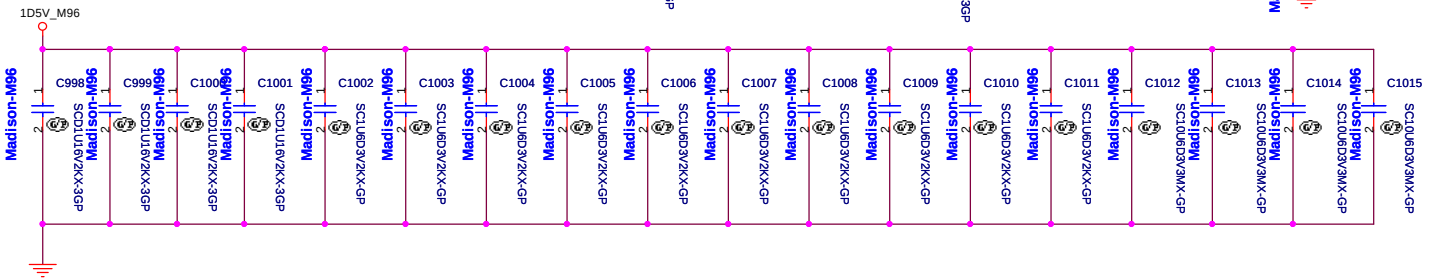
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	M92 DDR3 B1	
Size A3	Document Number JV50-TR8	Rev -1
Date: Monday, October 26, 2009	Sheet 61 of 63	

GDDR3







JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 DDR3 A0		
Size: A3	Document Number: JV50-TR8	Rev: -1
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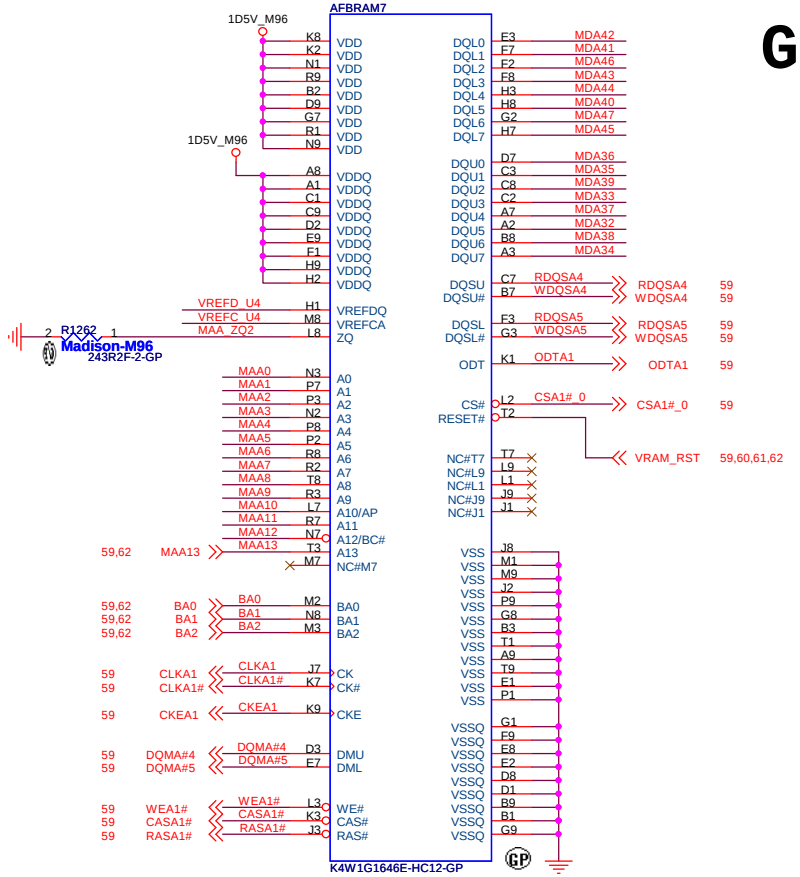
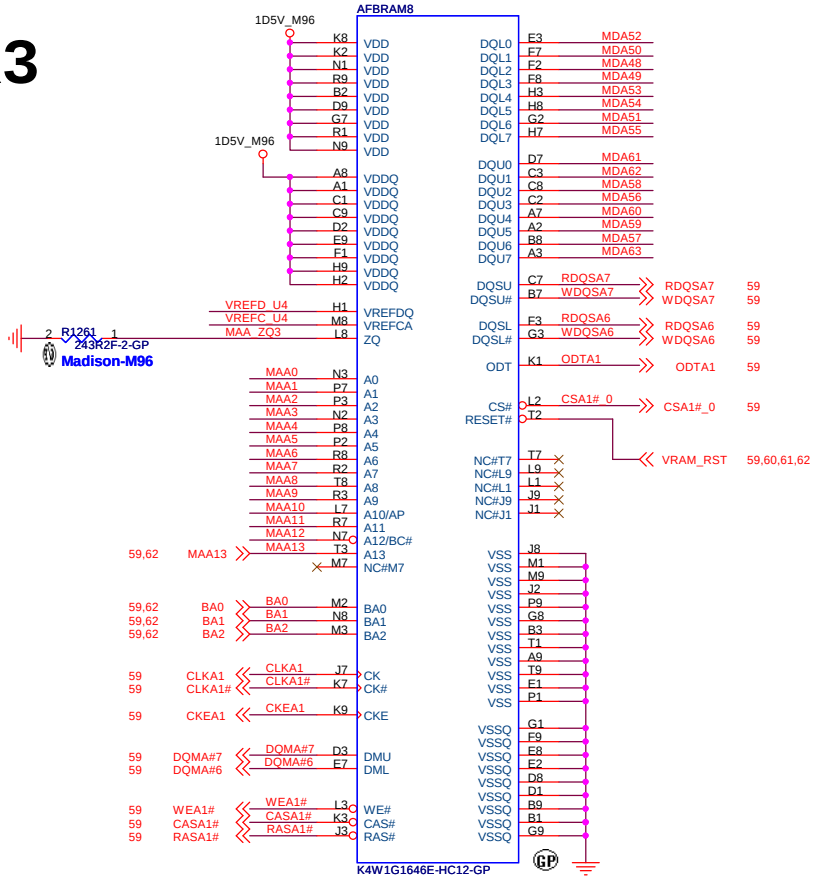
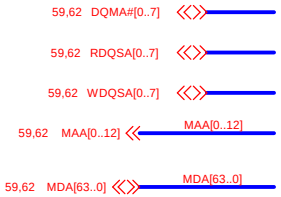
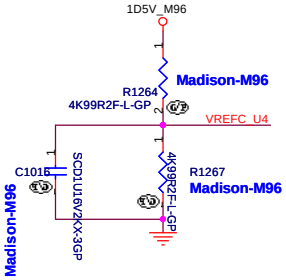
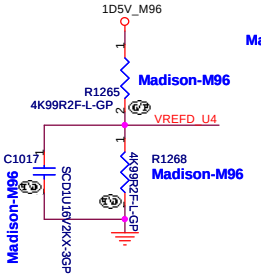
GDDR3

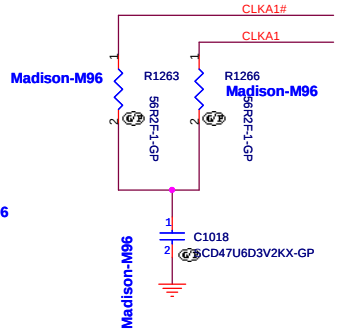


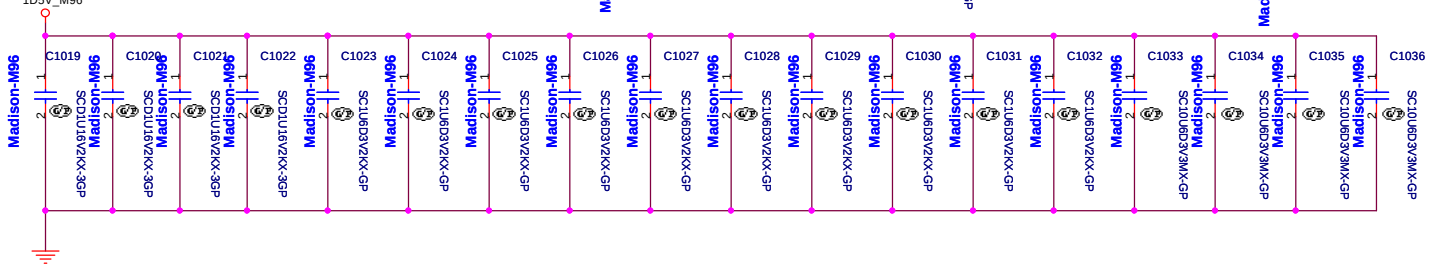












JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 DDR3 A1		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 63 of 63	