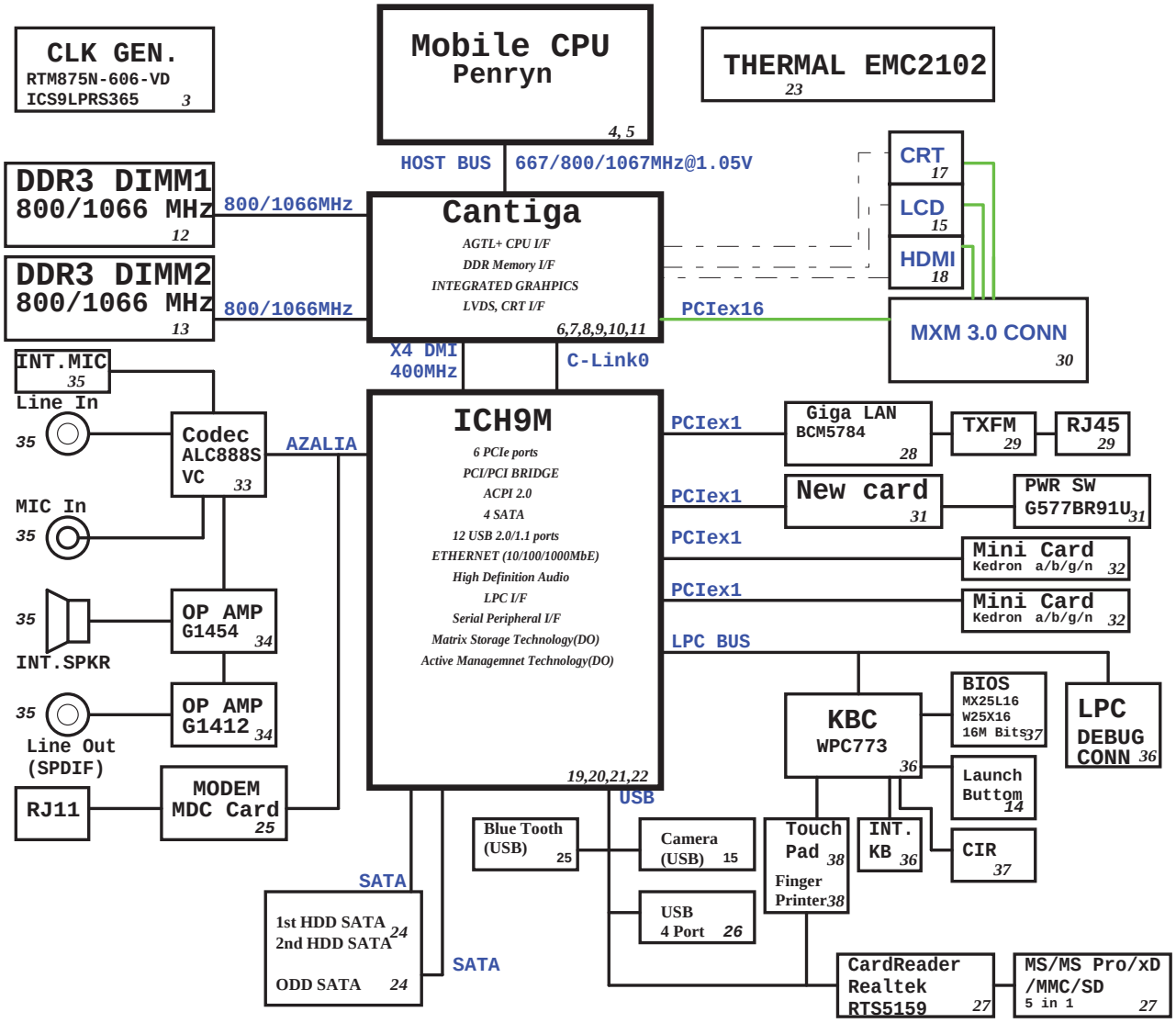
SJM80_MV/JV80_MV Block Diagram

Project code: 91.4DW01.001
PCB P/N : 48.4DW01.0SB
REVISION : 09221 -1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 43

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 45

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D5V_S3

RT9026 44

1D5V_S3	DDR_VREF_S3 DDR_VREF_S3_1

AO4468 44

1D5V_S3	1D5V_S0

GFXCORE DC/DC ISL6263A 46

INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V

CPU DC/DC ISL6266A 42

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER MAX8731A 47

INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

SJM80 UMA ONLY SB

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Title: BLOCK DIAGRAM
Size: Custom | Document Number: SJM80/JV80 | Rev: -1
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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

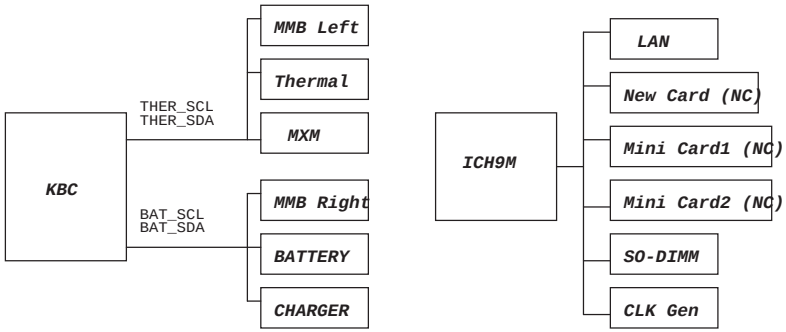
PCIE Routing

LANE1	LAN Broadcom 5784
LANE2	MiniCard WLAN
LANE3	MiniCard TV
LANE4	NC
LANE5	NewCard
LANE6	NC

USB Table

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINI1 (WL)
4	CCD
5	NEW CARD
6	FP
7	BT
8	NC
9	USB1
10	MINI2
11	CARD READER

SMBus



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Title: Reference

Size A3 | Document Number: SJM80/JV80 | Rev -1

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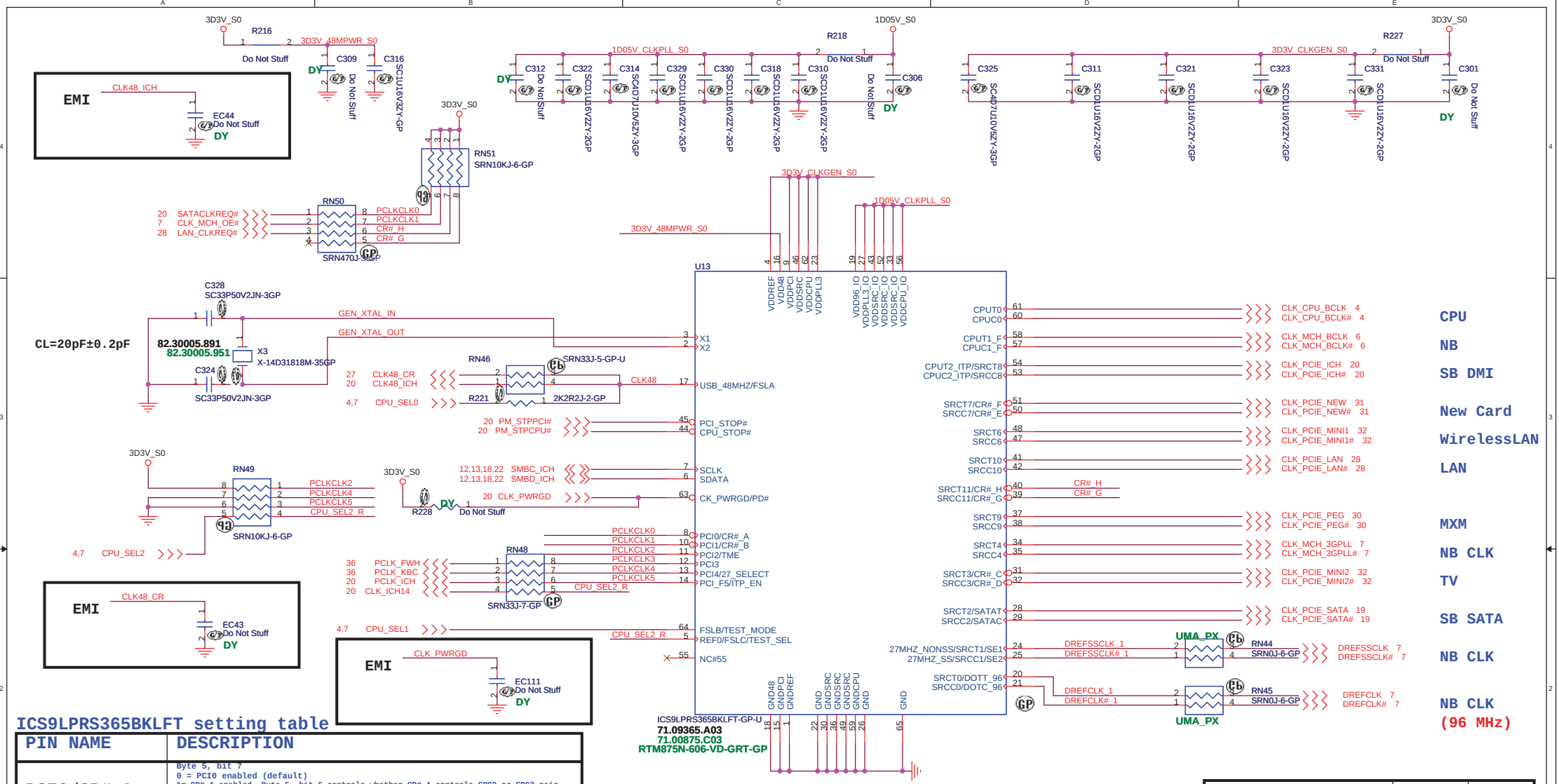

ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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Title: Clock Generator

Size | Document Number: SJM80/JV80 | Rev: -1

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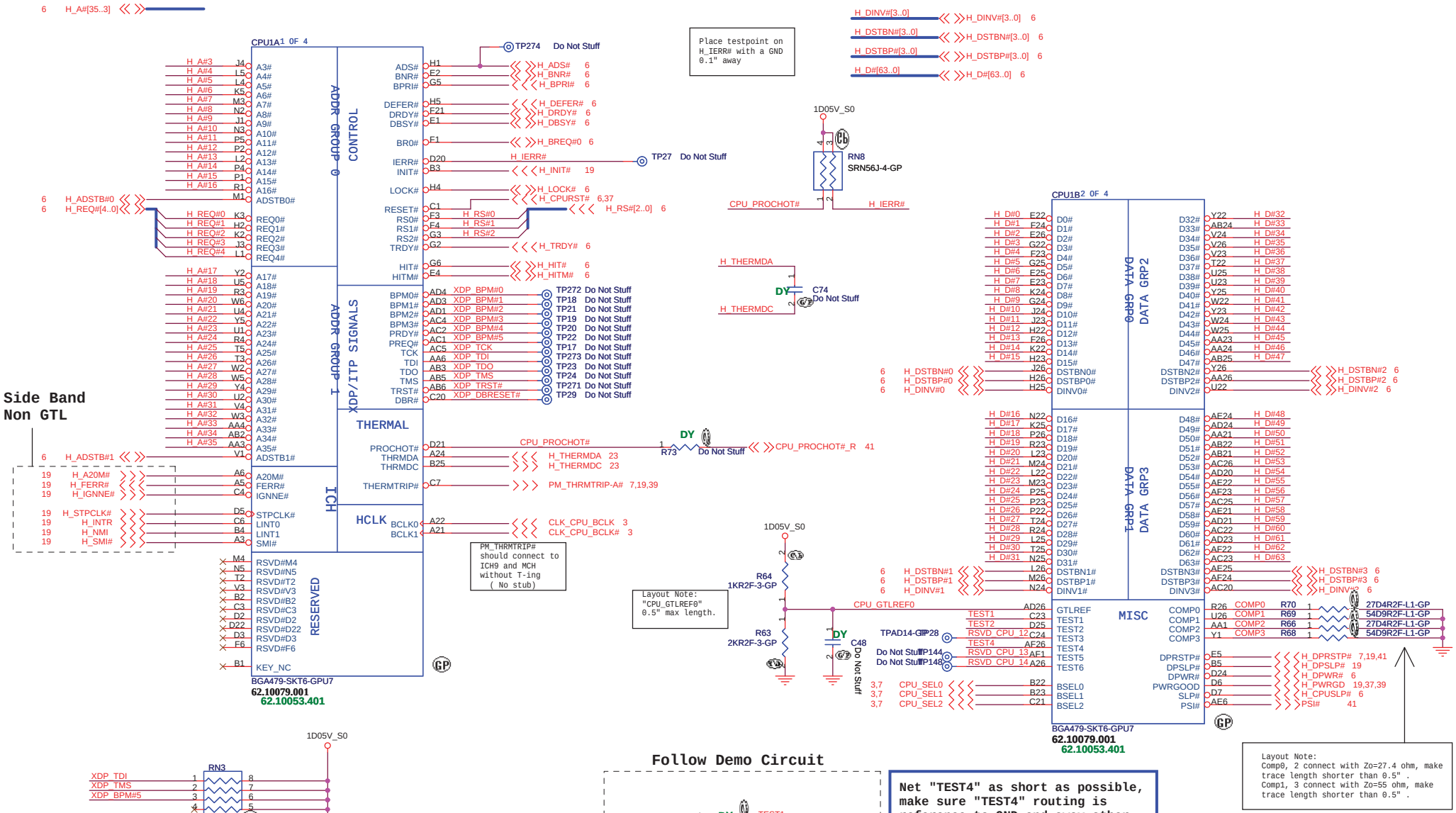

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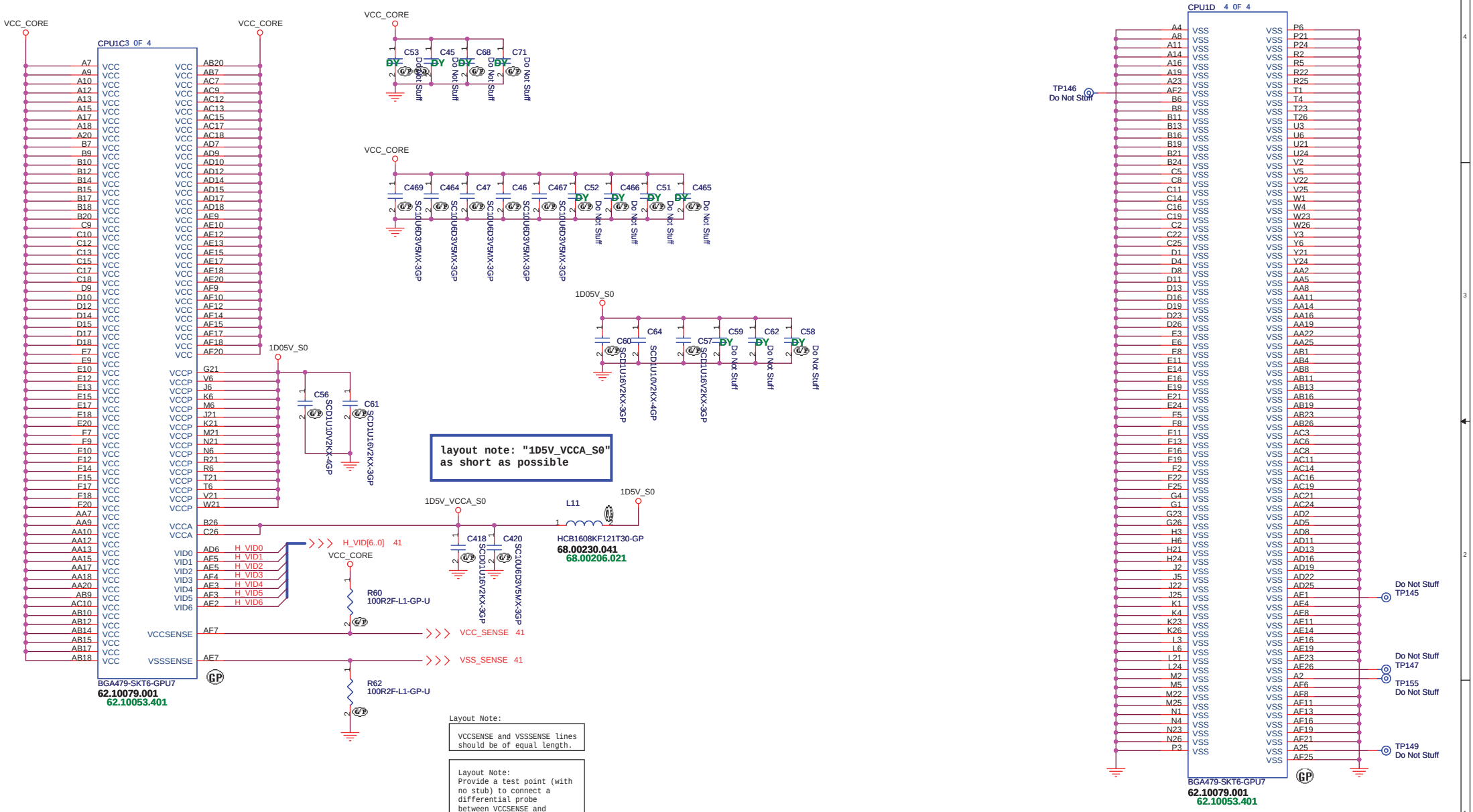

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Title: CPU (2 of 2)

Size | Document Number: SJM80/JV80 | Rev: -1

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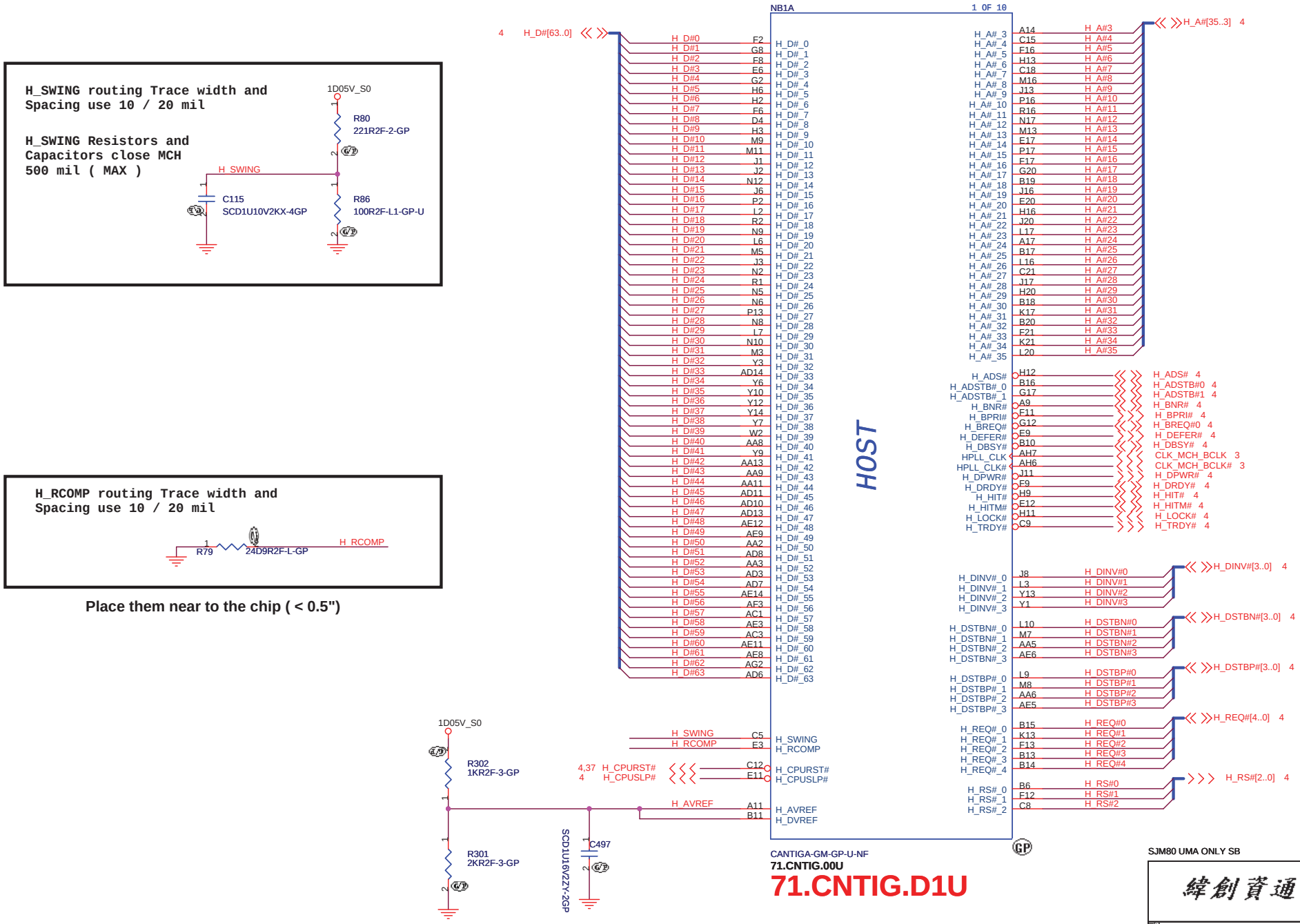

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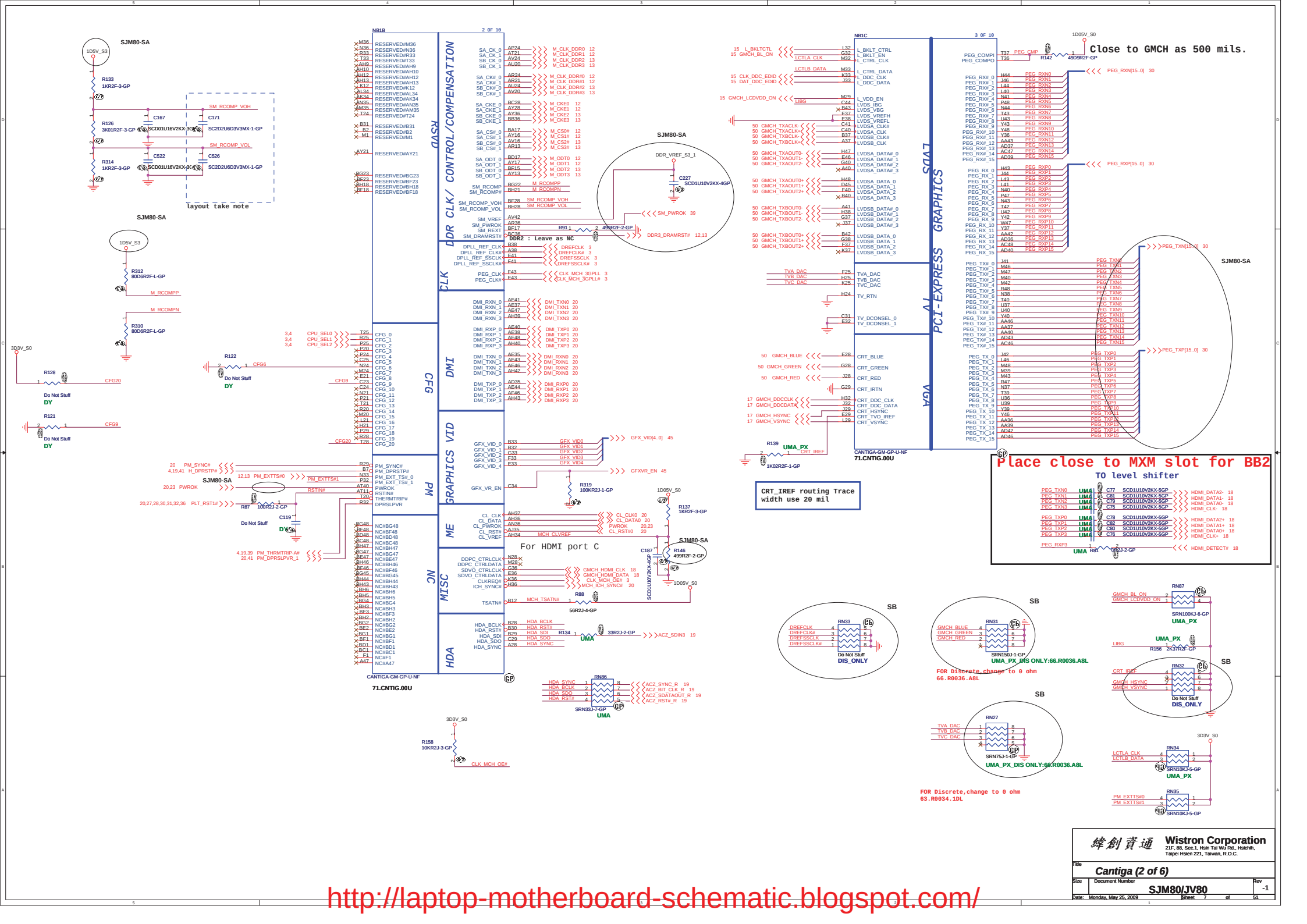

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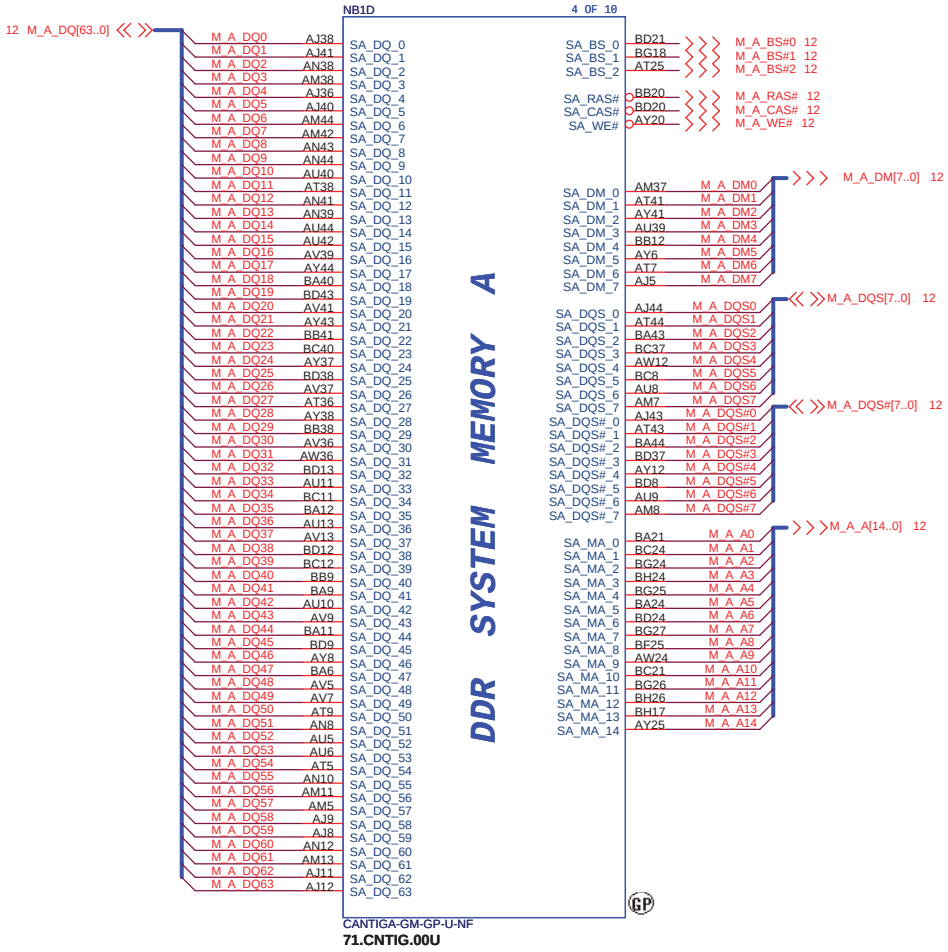

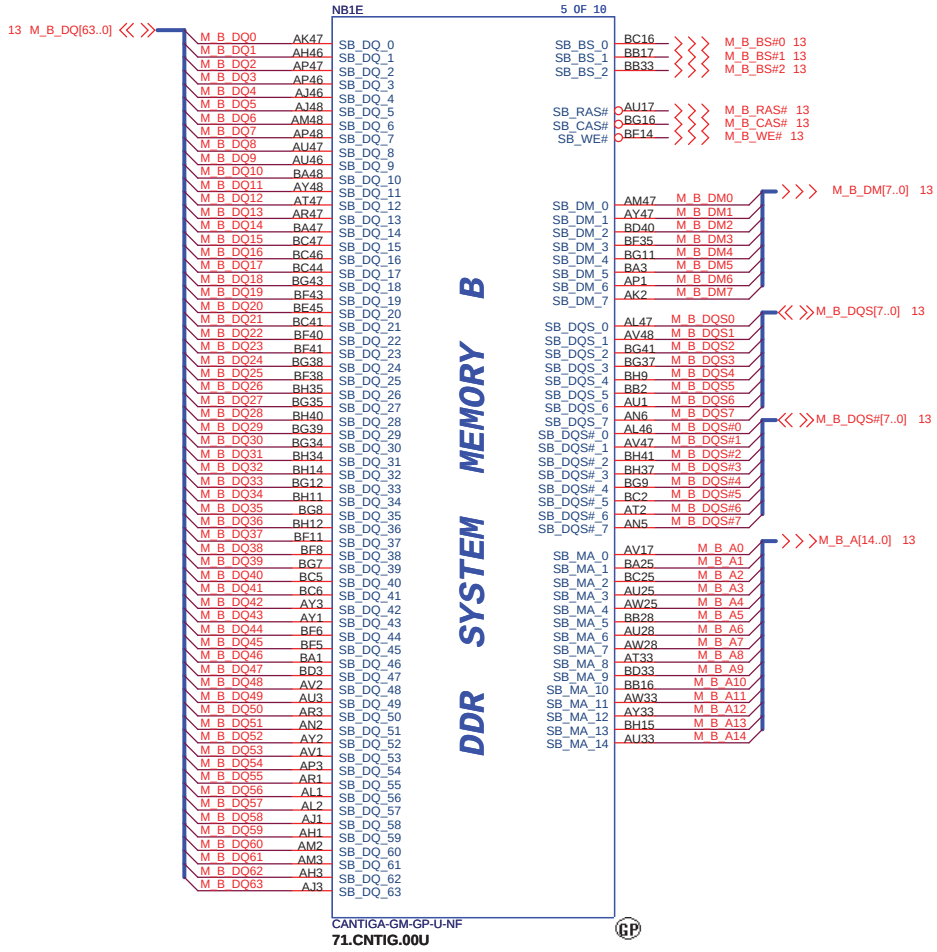

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Title	Cantiga (3 of 6)
Size	
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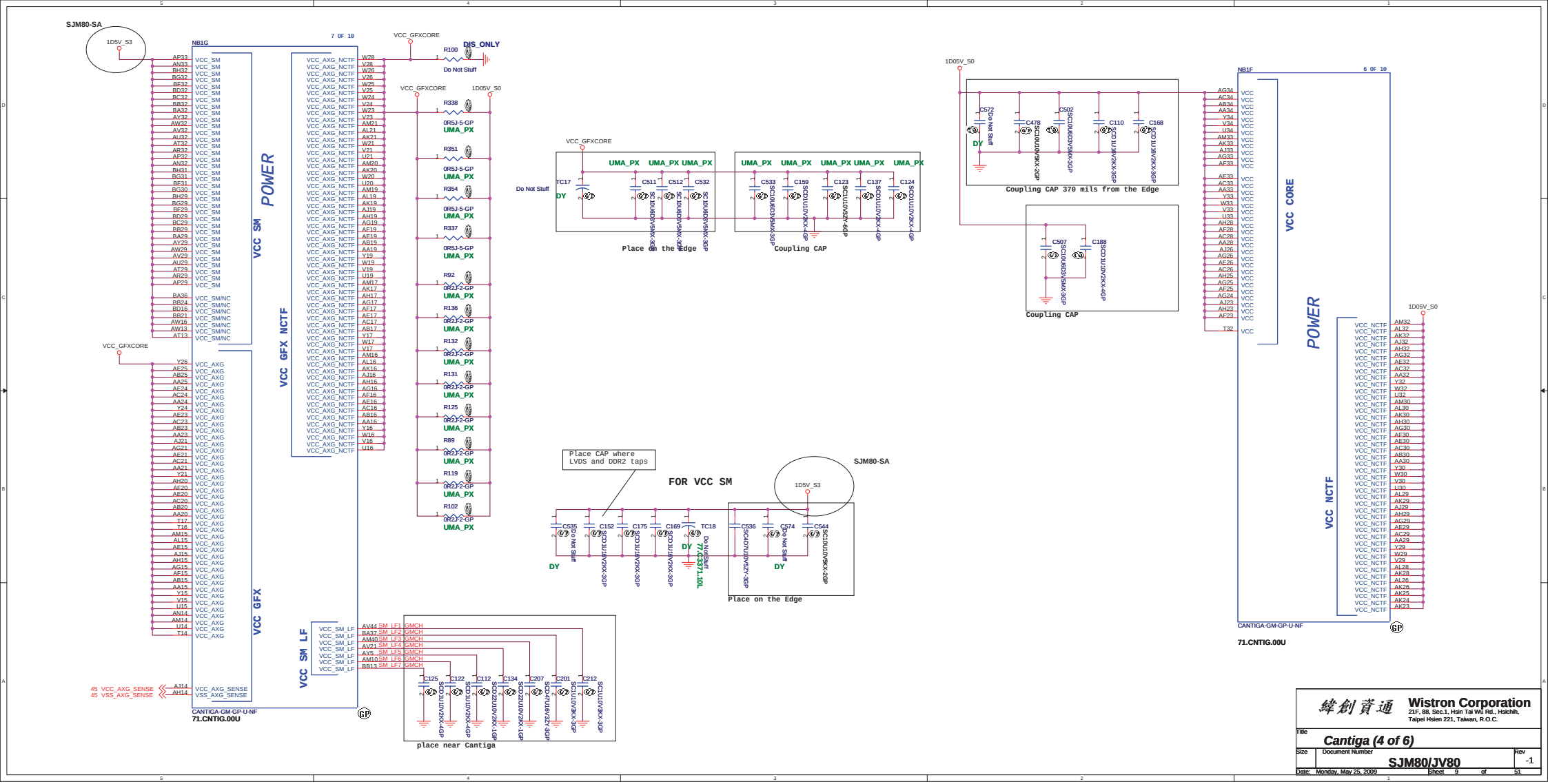

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Title: Cantiga (4 of 6)

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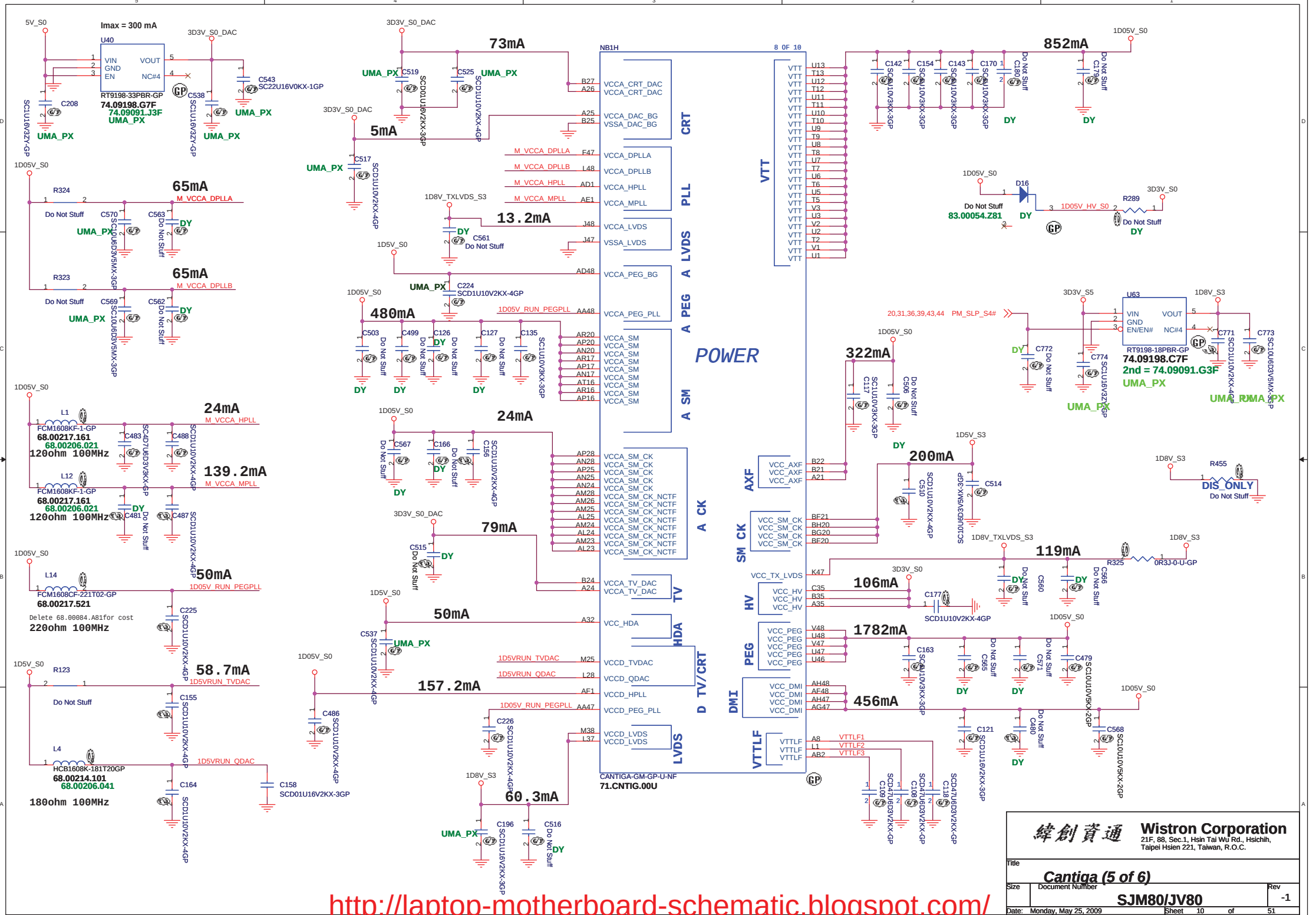

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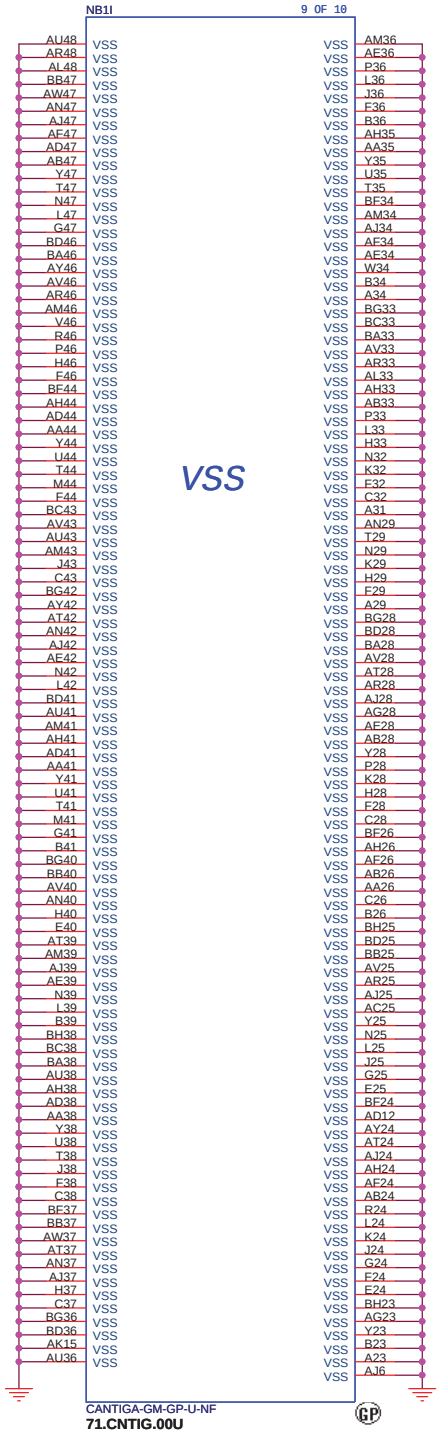

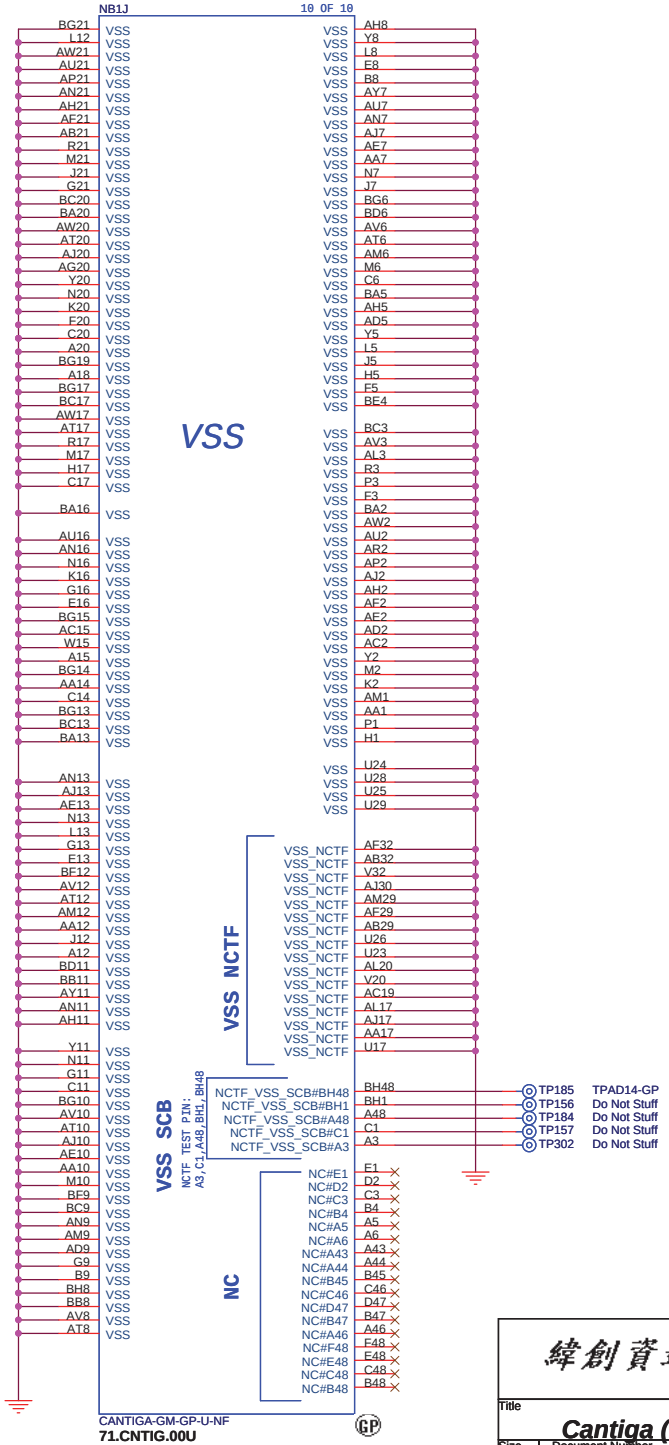

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Title		
Cantiga (6 of 6)		
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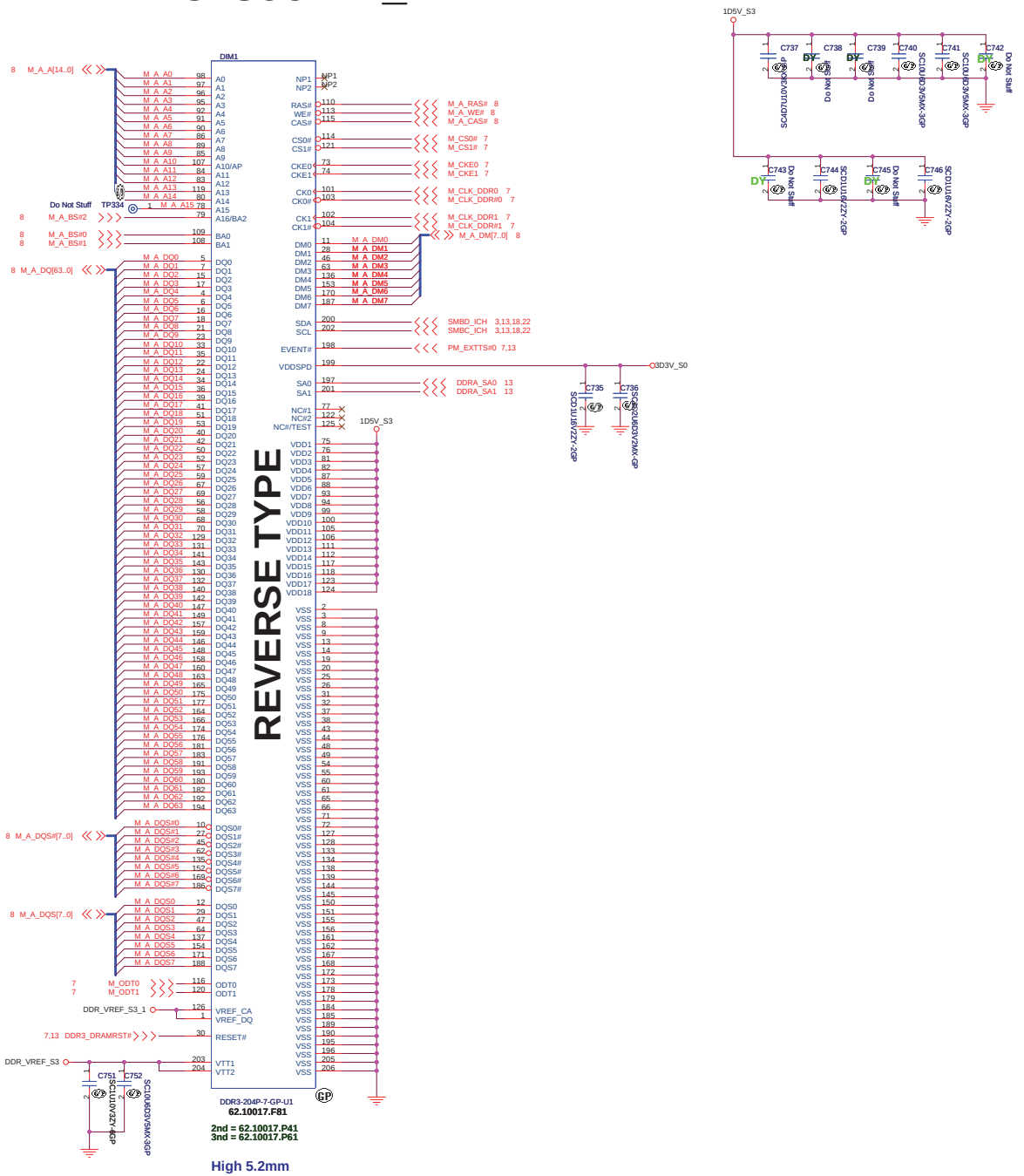
DDR3 SOCKET_1



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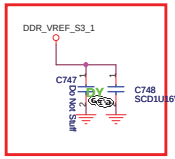

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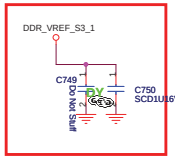

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Title: DDR3 Socket

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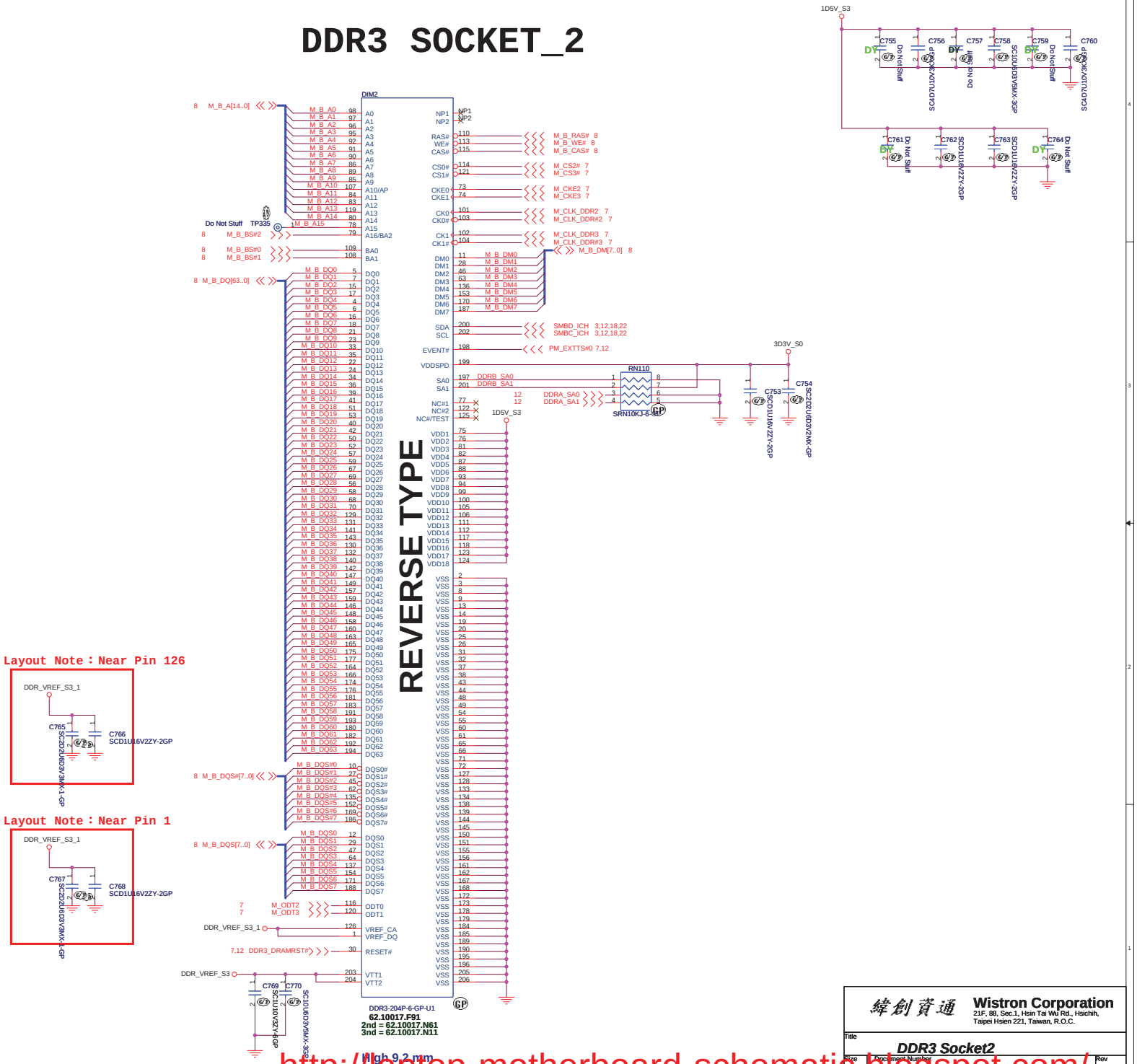
DDR3 SOCKET_2



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Title: DDR3 Socket2			
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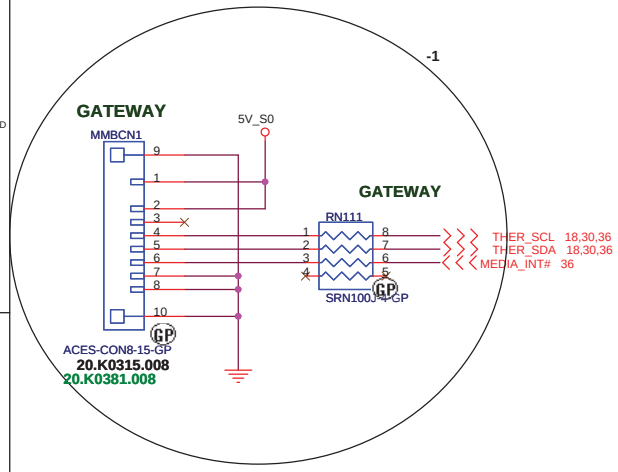
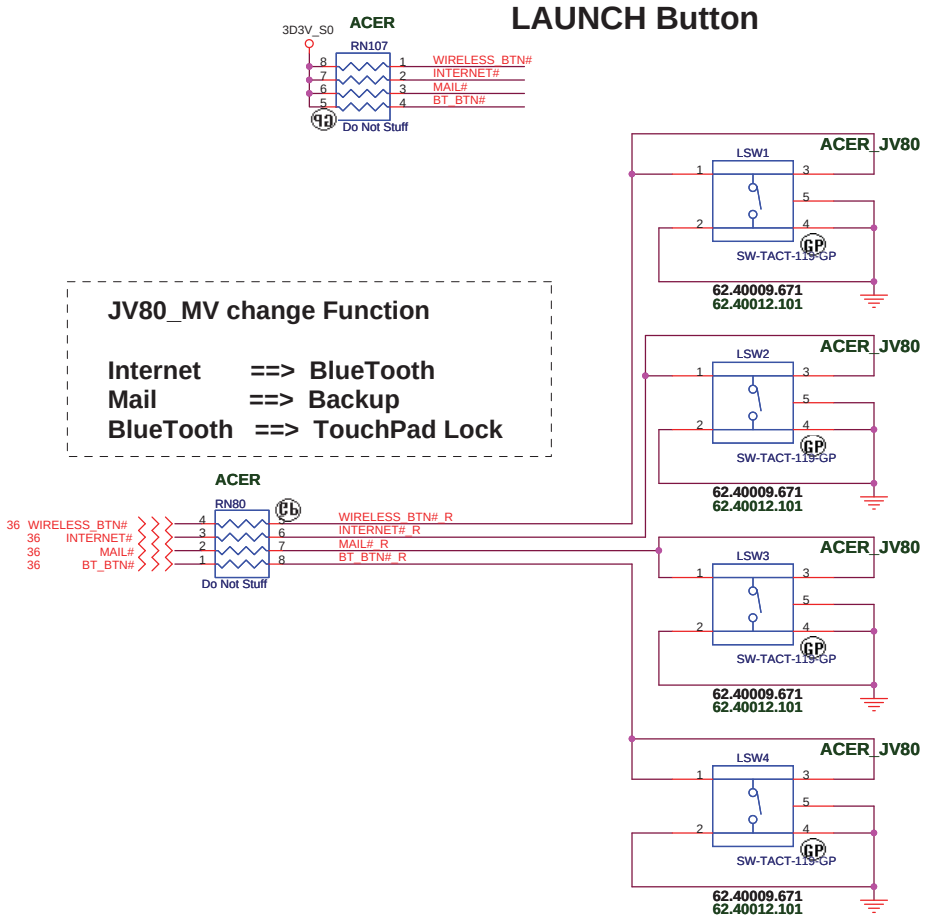
MMB Lounch For GATEWAY



LAUNCH Button



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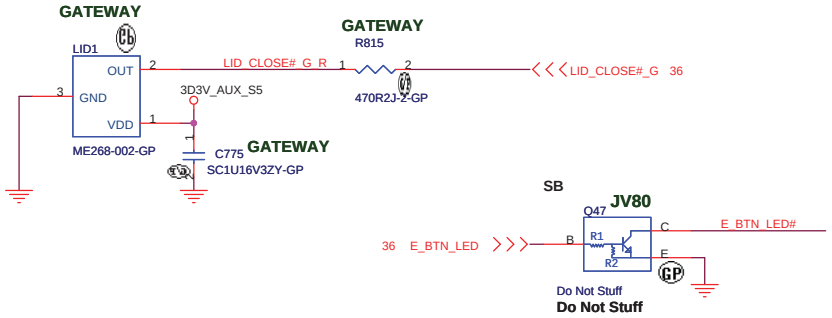
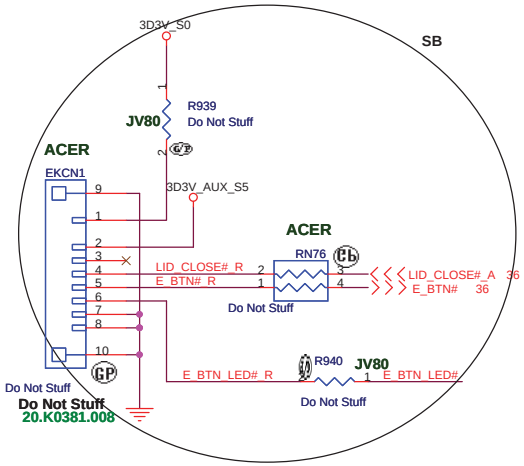
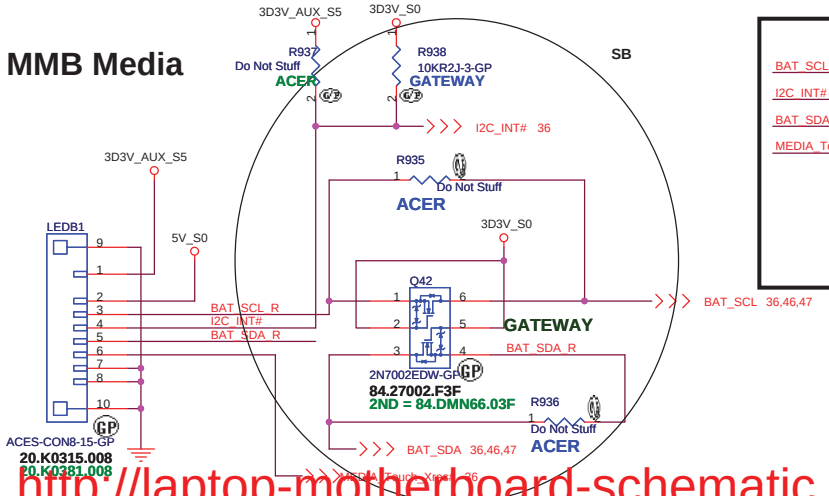
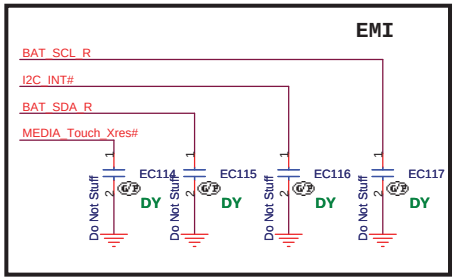


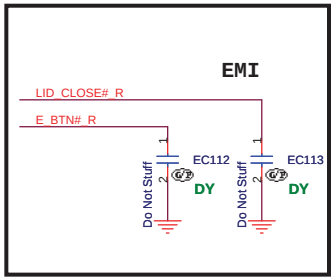
E-KEY Button



MMB Media







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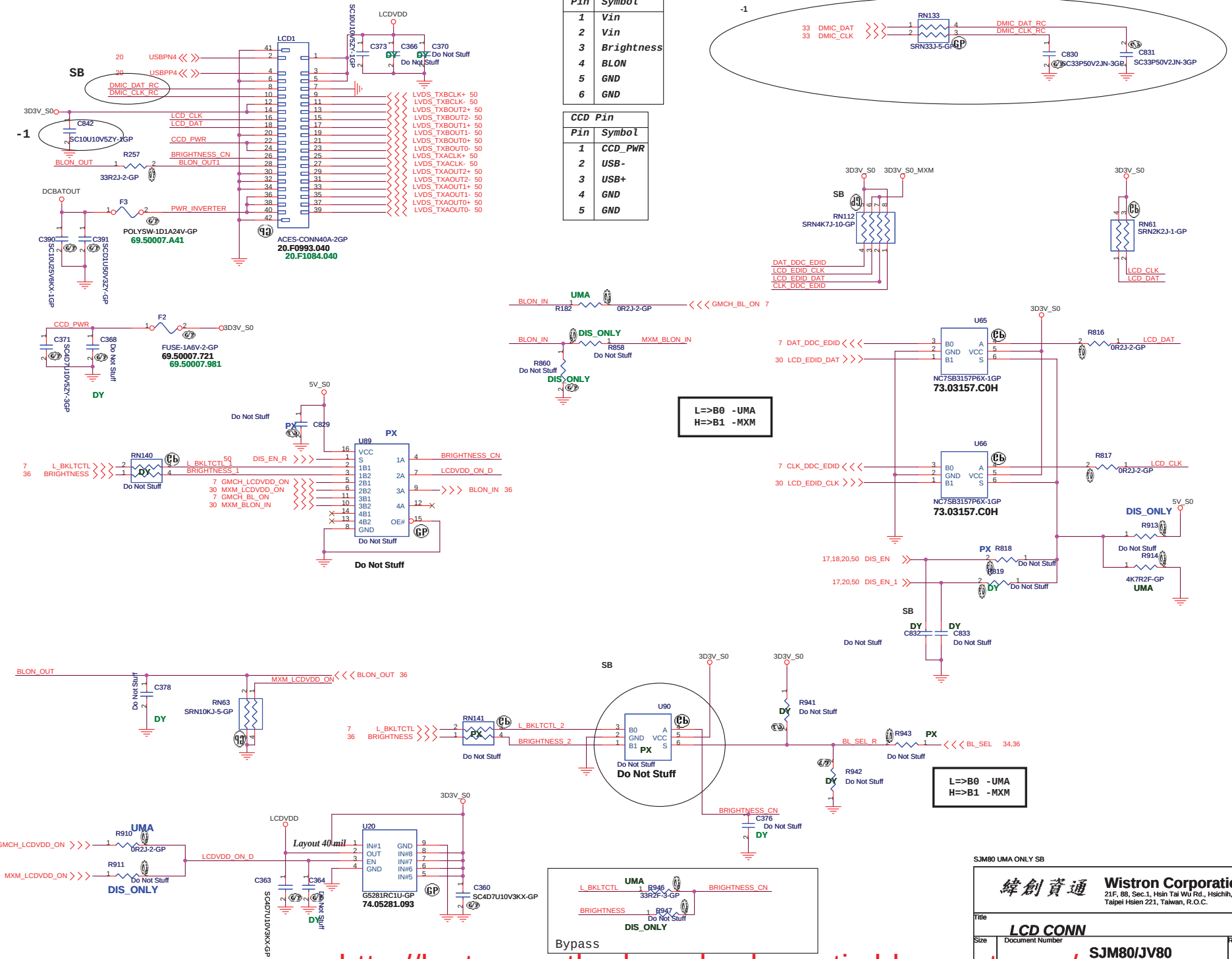
LCD/INVERTER/CCD CONN

EMI request RN133 22R change 33R
C830/C831 22P change 33P

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



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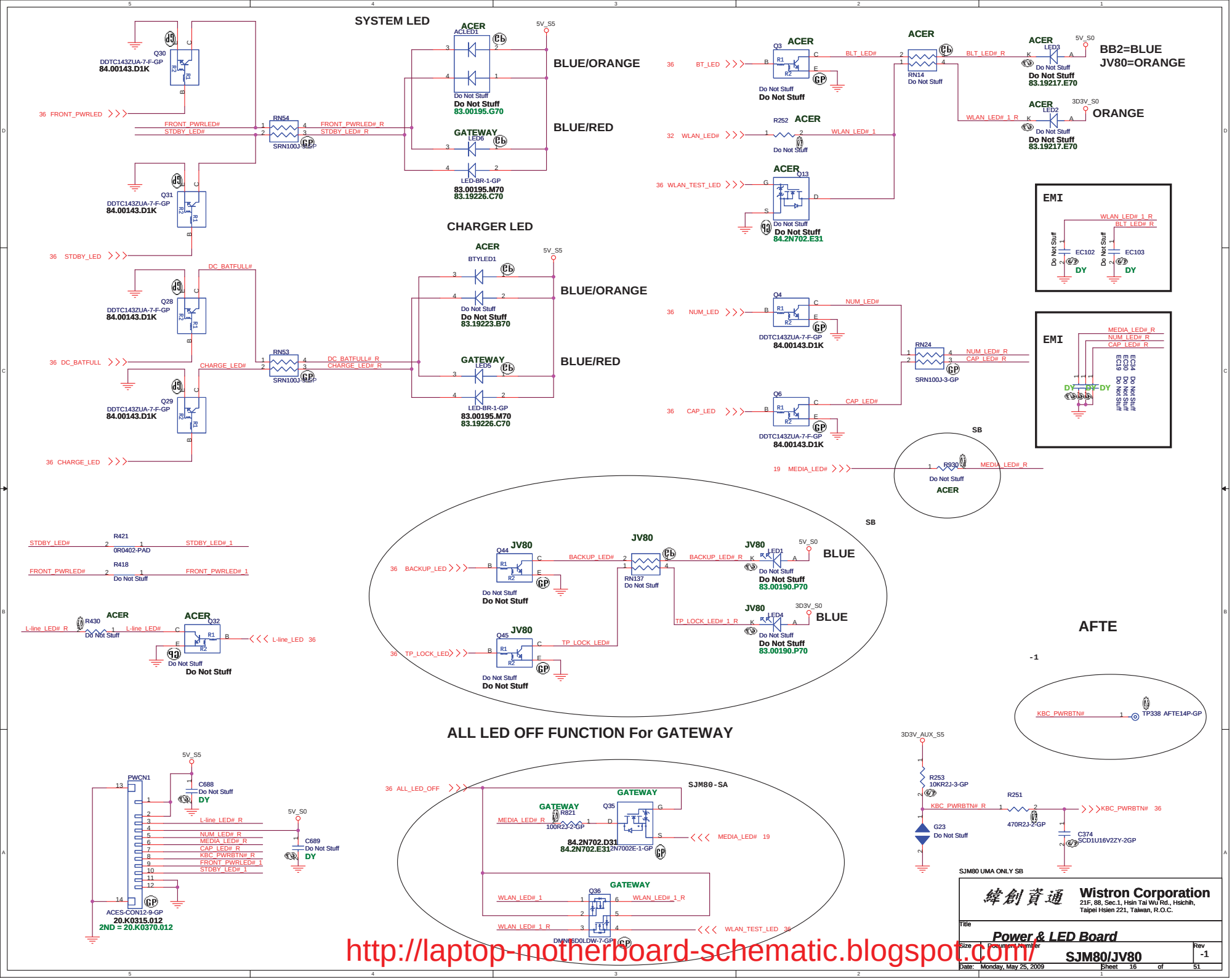

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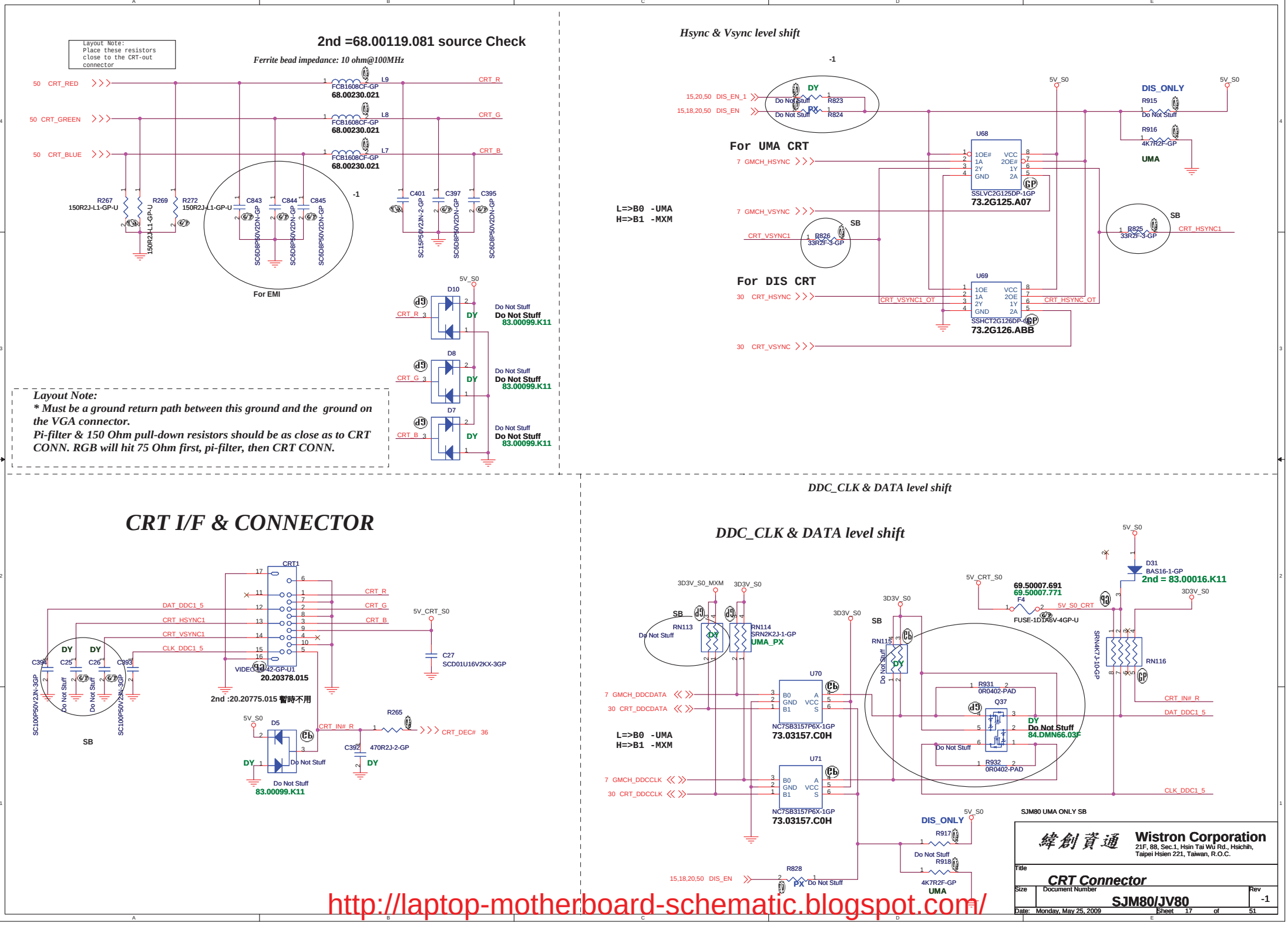

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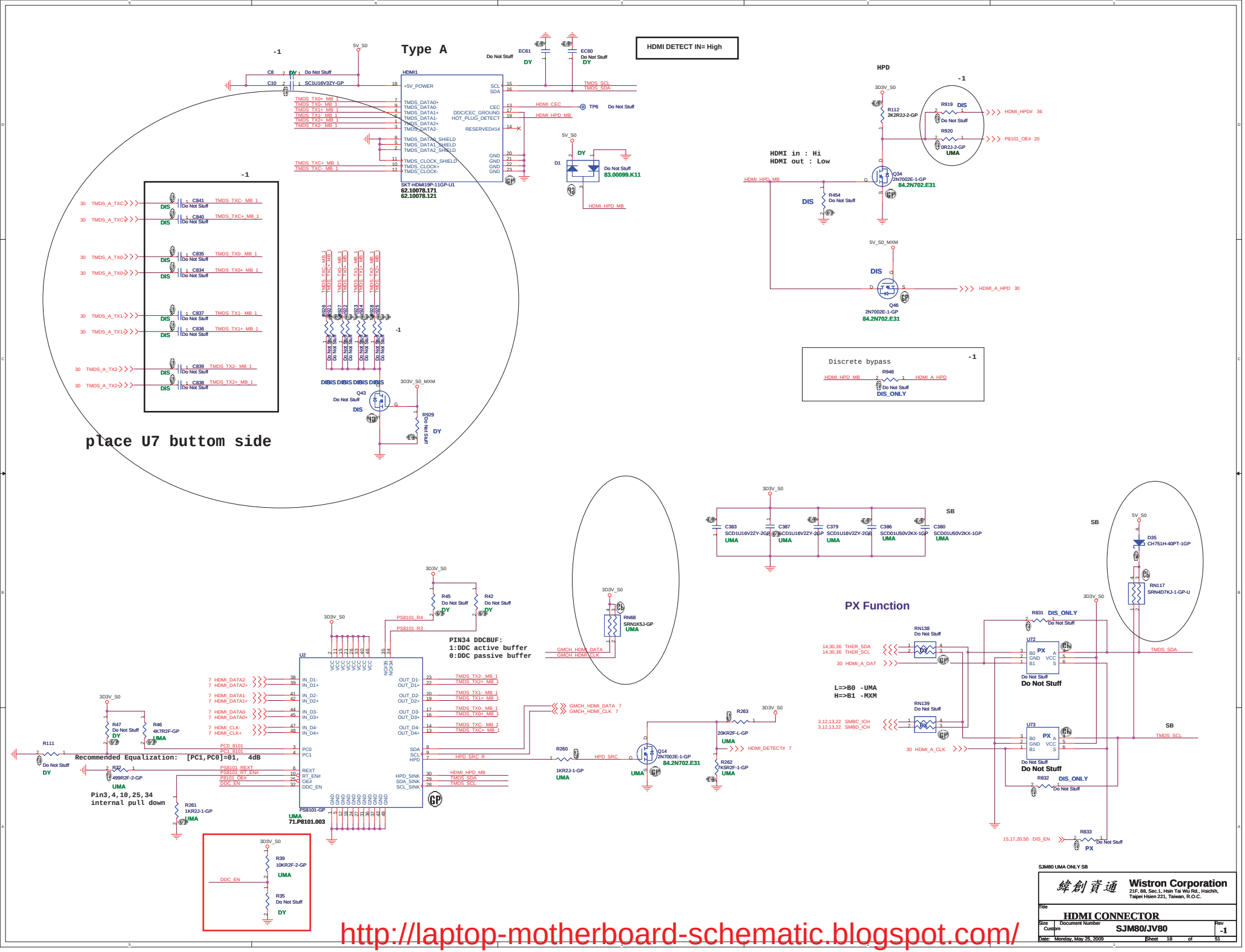

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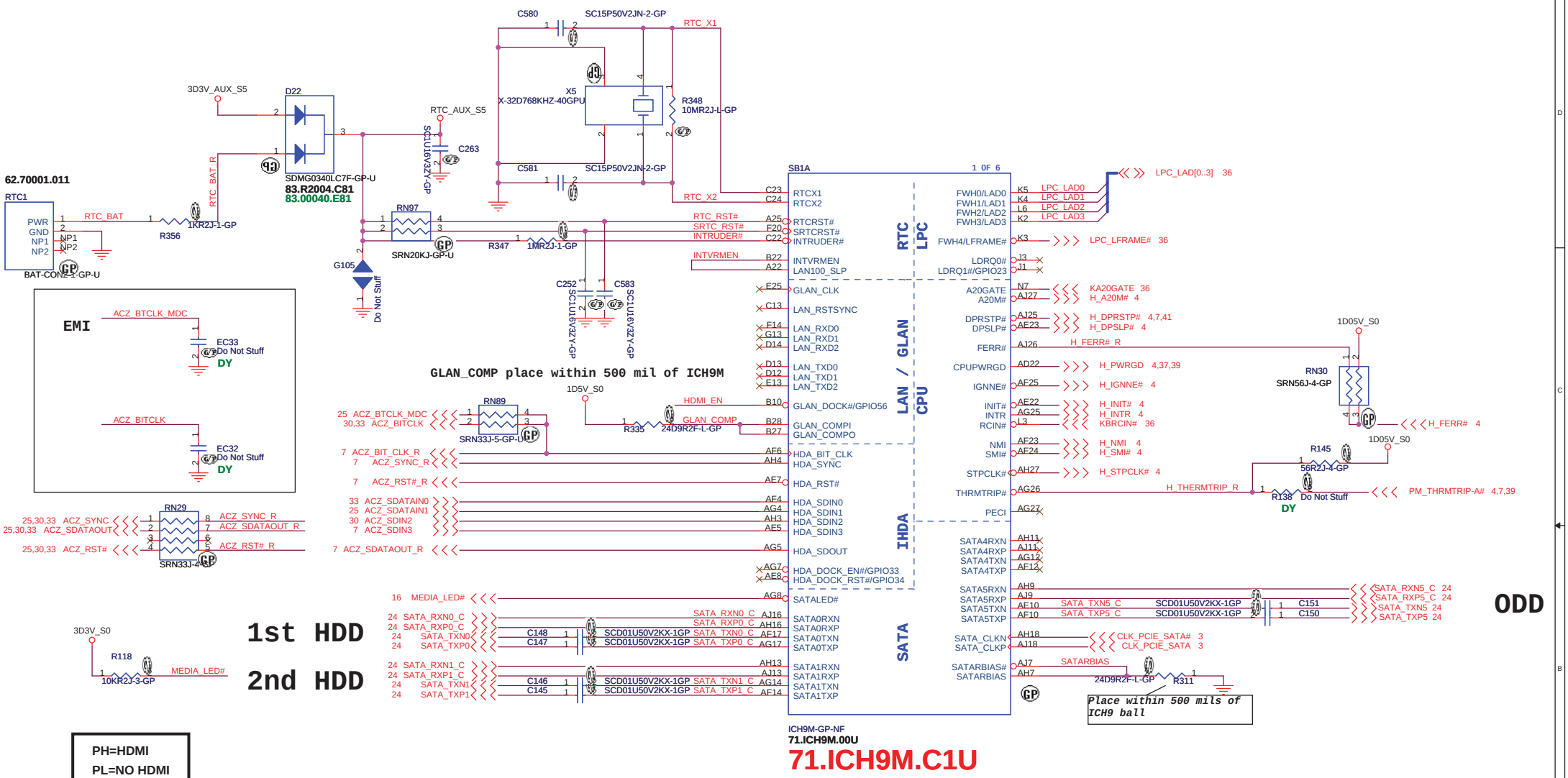

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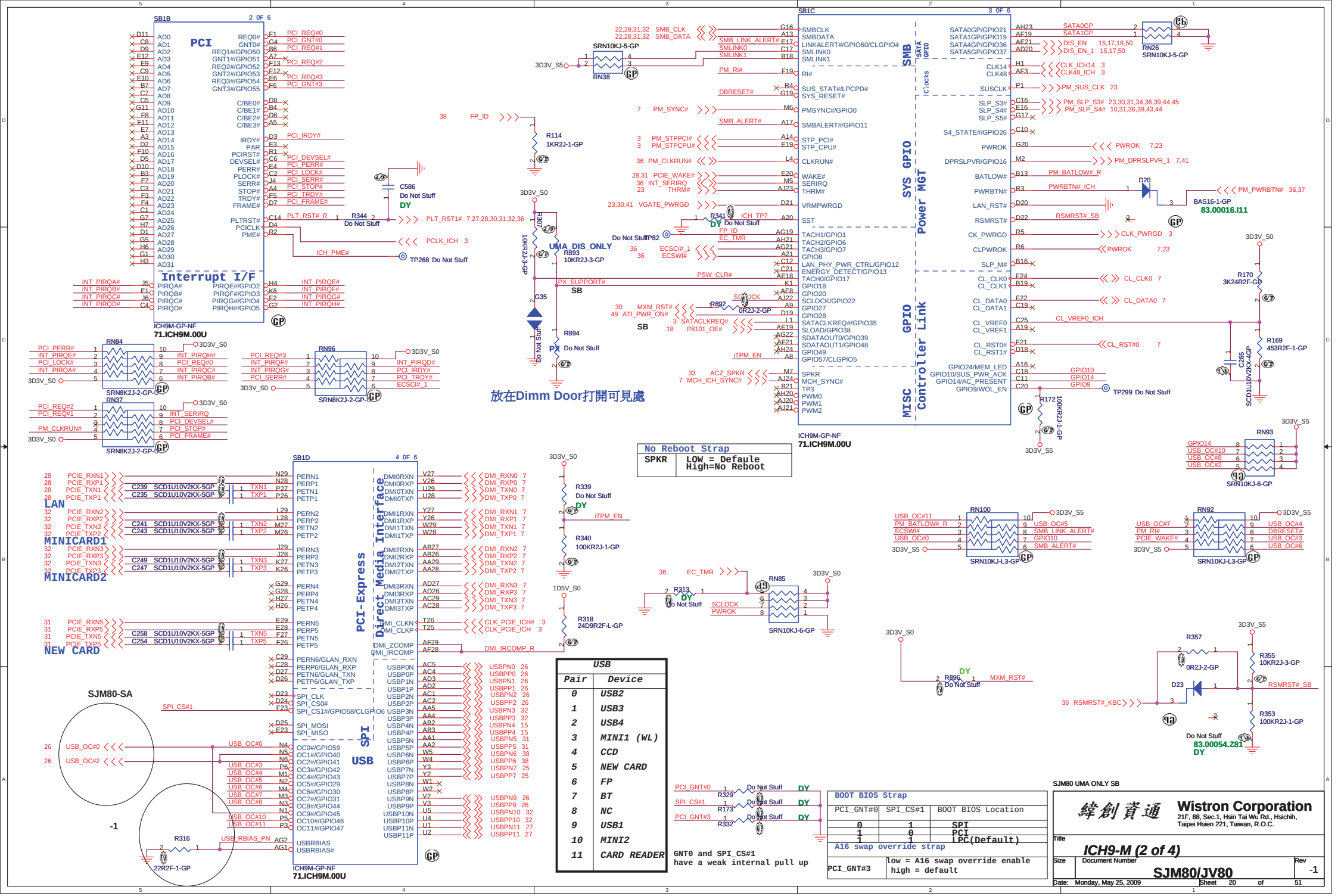

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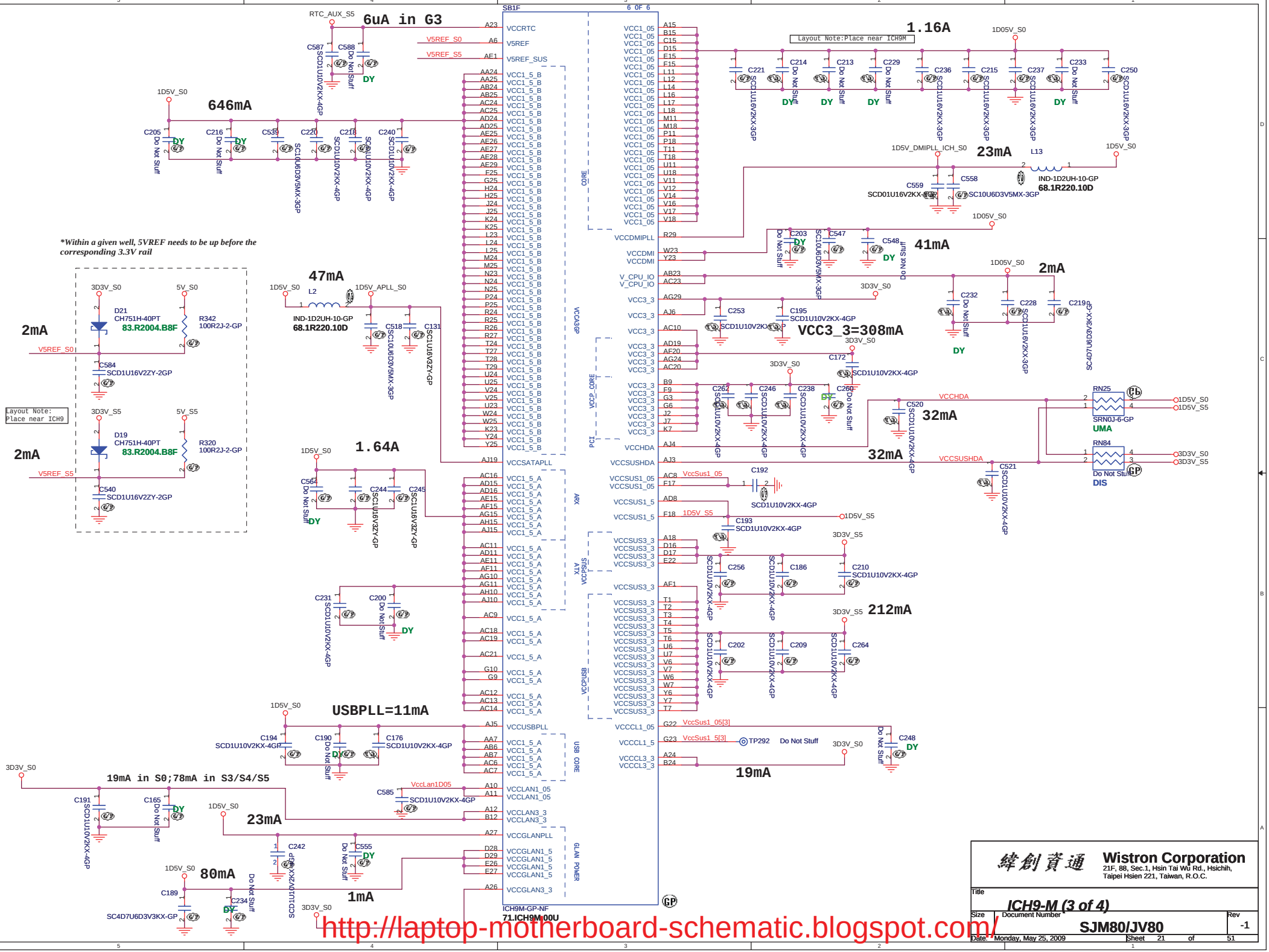

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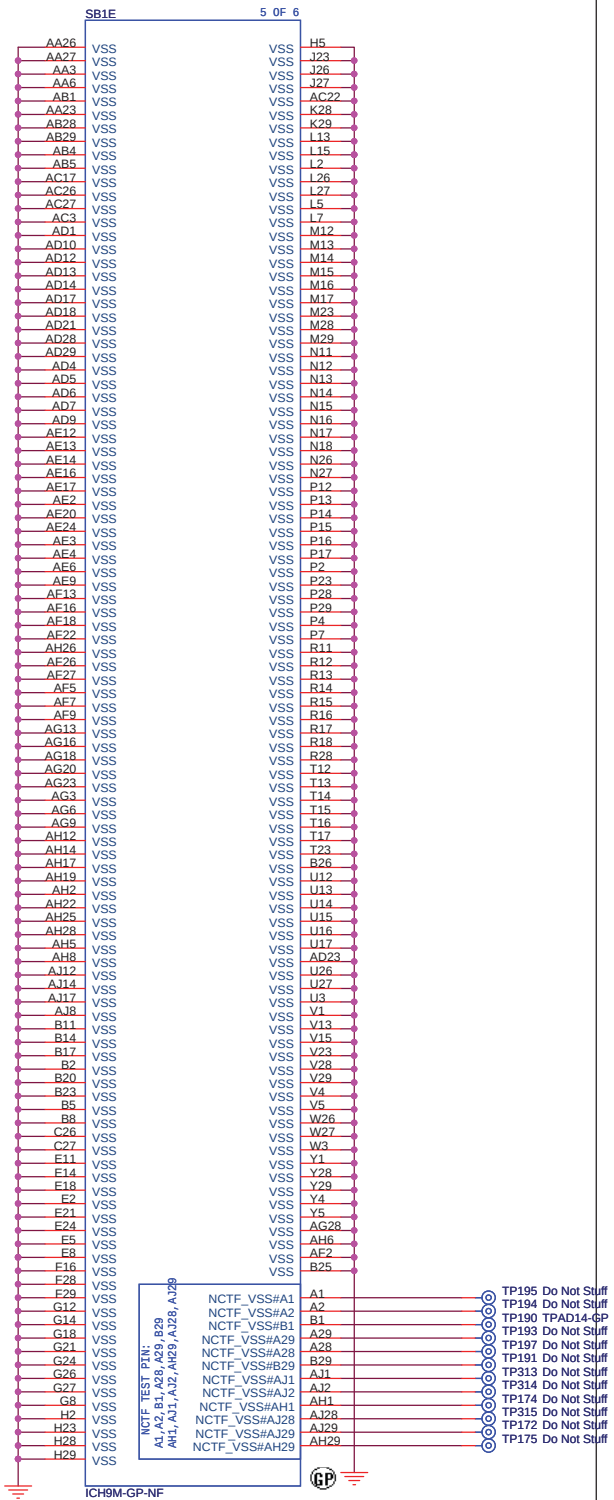
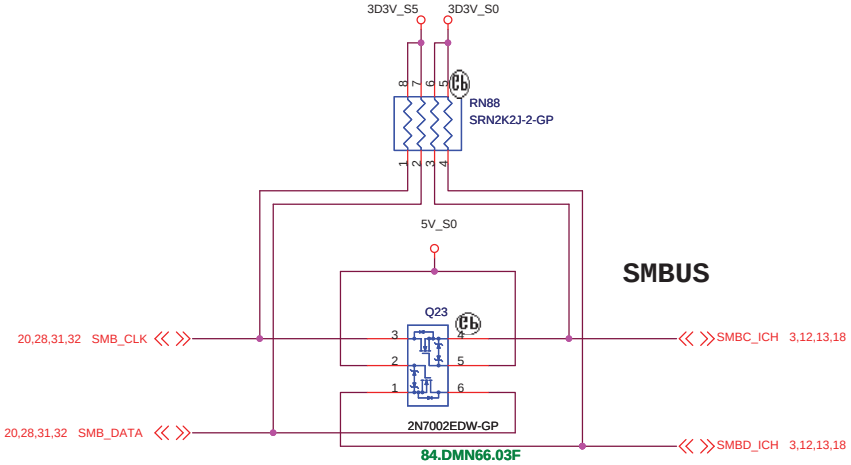




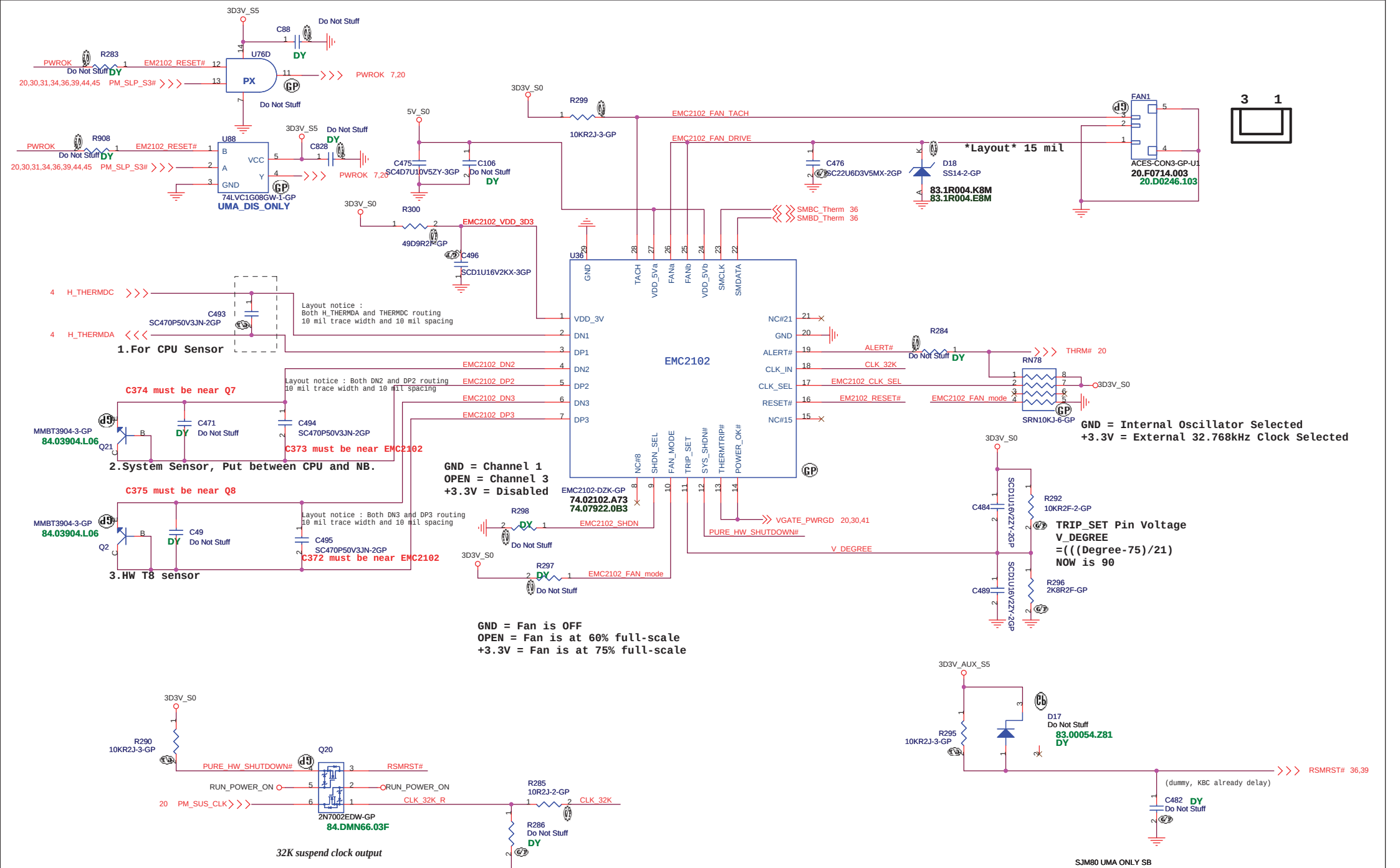
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ICH9-M (4 of 4)*

Size | Document Number: **SJM80/JV80** | Rev: -1

Date: Monday, May 25, 2009 | Sheet 22 of 51

http://laptop-motherboard-schematic.blogspot.com/



SJM80 UMA ONLY SB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size | Document Number: SJM80/JV80 | Rev: -1

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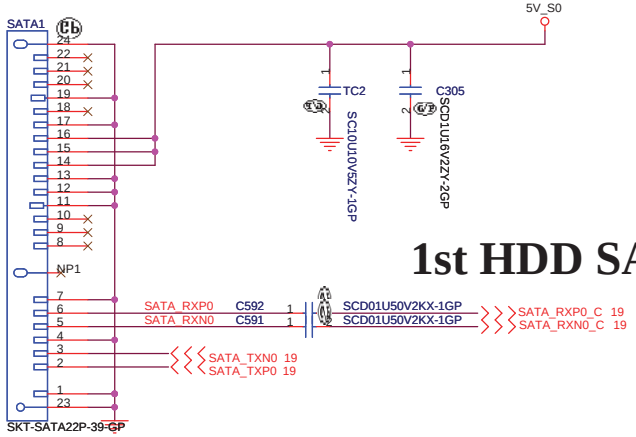
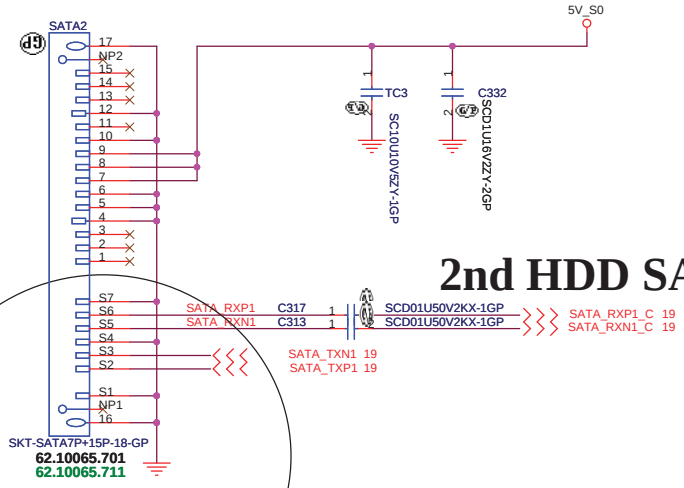
http://laptop-motherboard-schematic.blogspot.com/



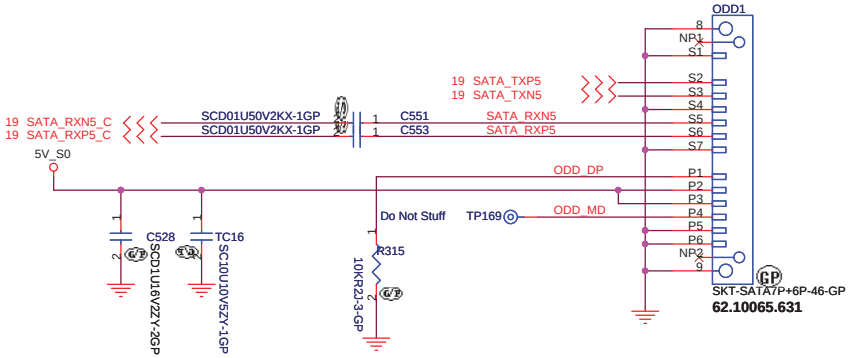
1st HDD SATA Connector



2nd HDD SATA Connector

SB 不打Main source

SATA ODD Connector



SJM80 UMA ONLY SB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***HDD & ODD***
Size / Document Number	**SJM80/JV80**
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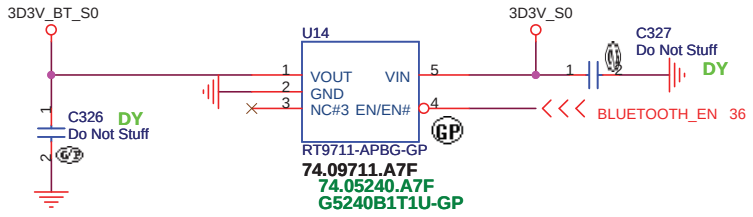
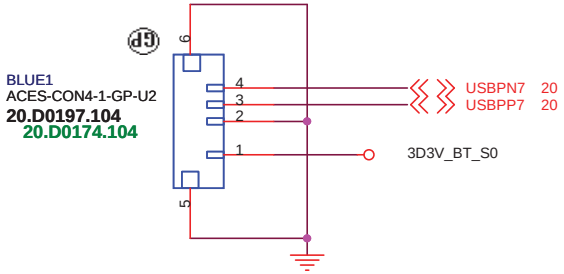
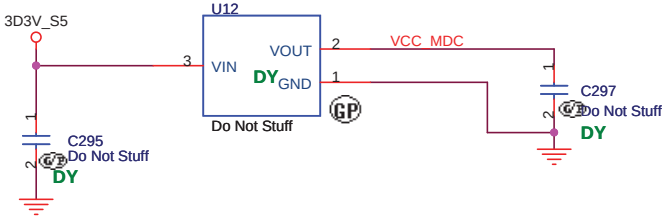
http://laptop-motherboard-schematic.blogspot.com/

BLUETOOTH MODULE

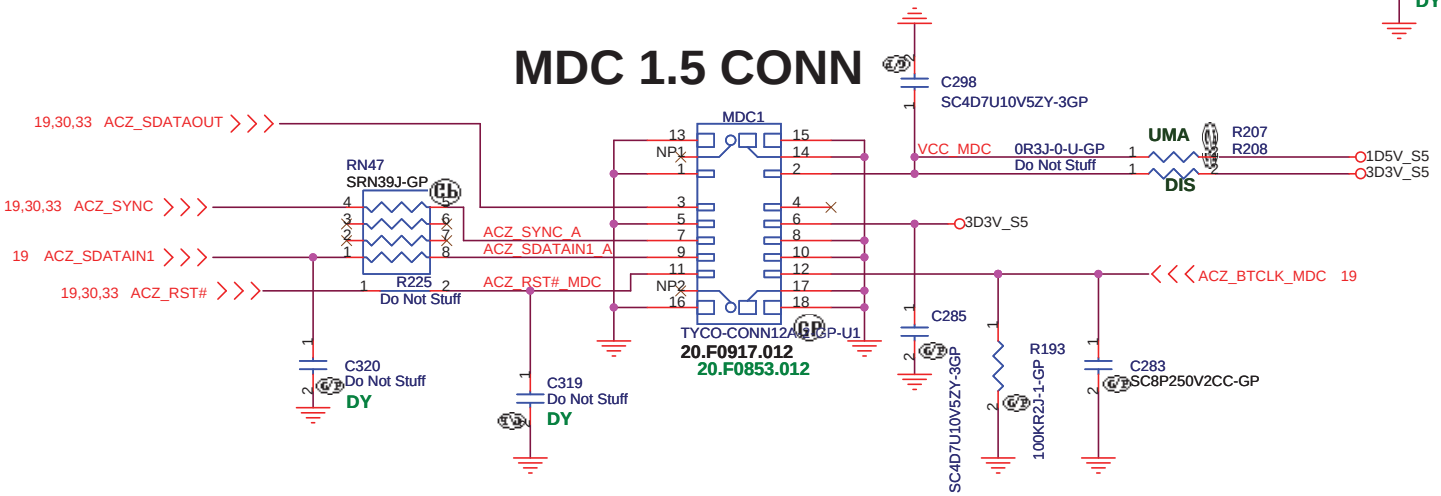
1.5A / High Active Voltage 2V

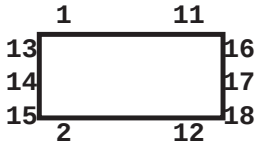






MDC 1.5 CONN

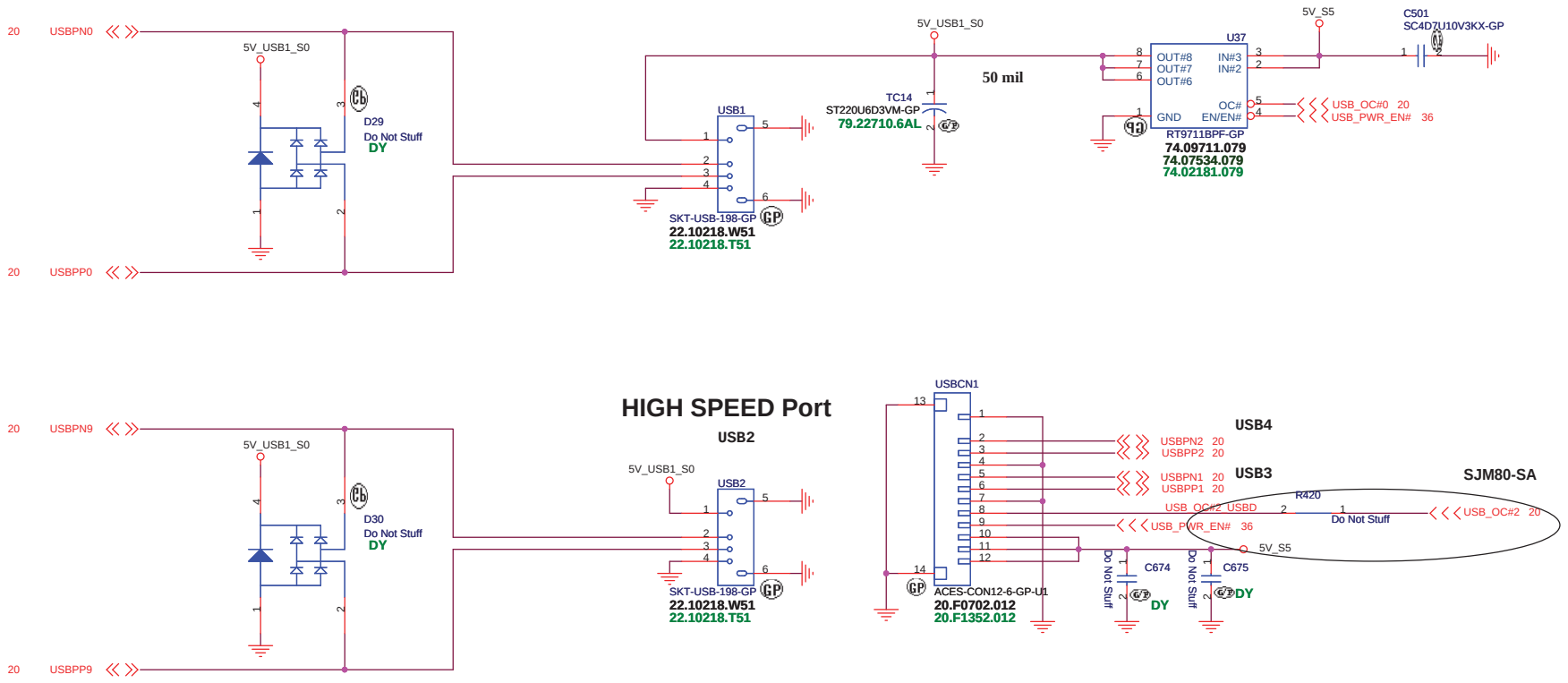




SJM80 UMA ONLY SB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BLUETOOTH & MDC***	
Size	Document Number **SJM80/JV80**	Rev -1
Date: Monday, May 25, 2009	Sheet 25 of 51	

http://laptop-motherboard-schematic.blogspot.com/



SJM80 UMA ONLY SB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB connector**

Size	Document Number	Rev
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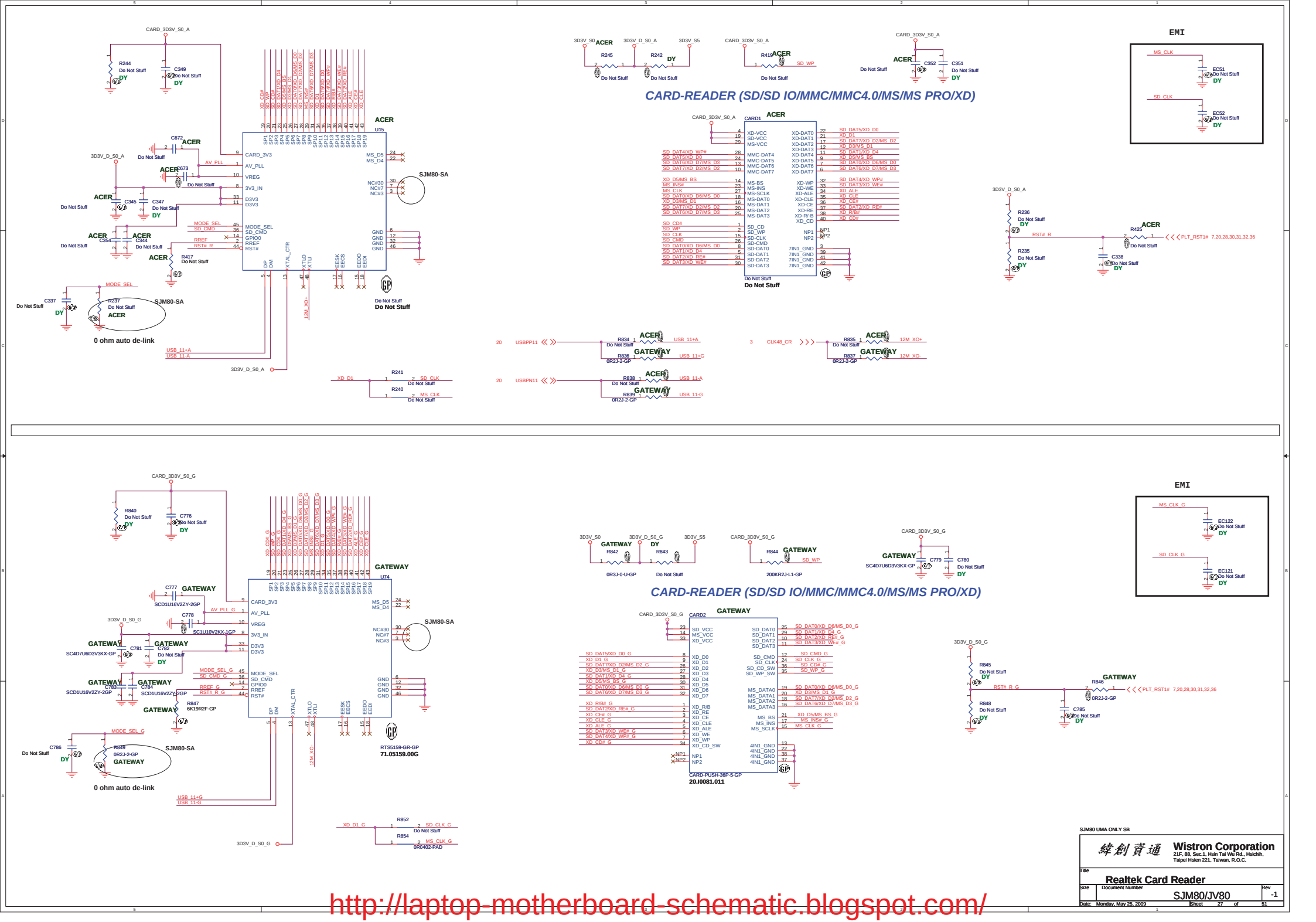
http://laptop-motherboard-schematic.blogspot.com/



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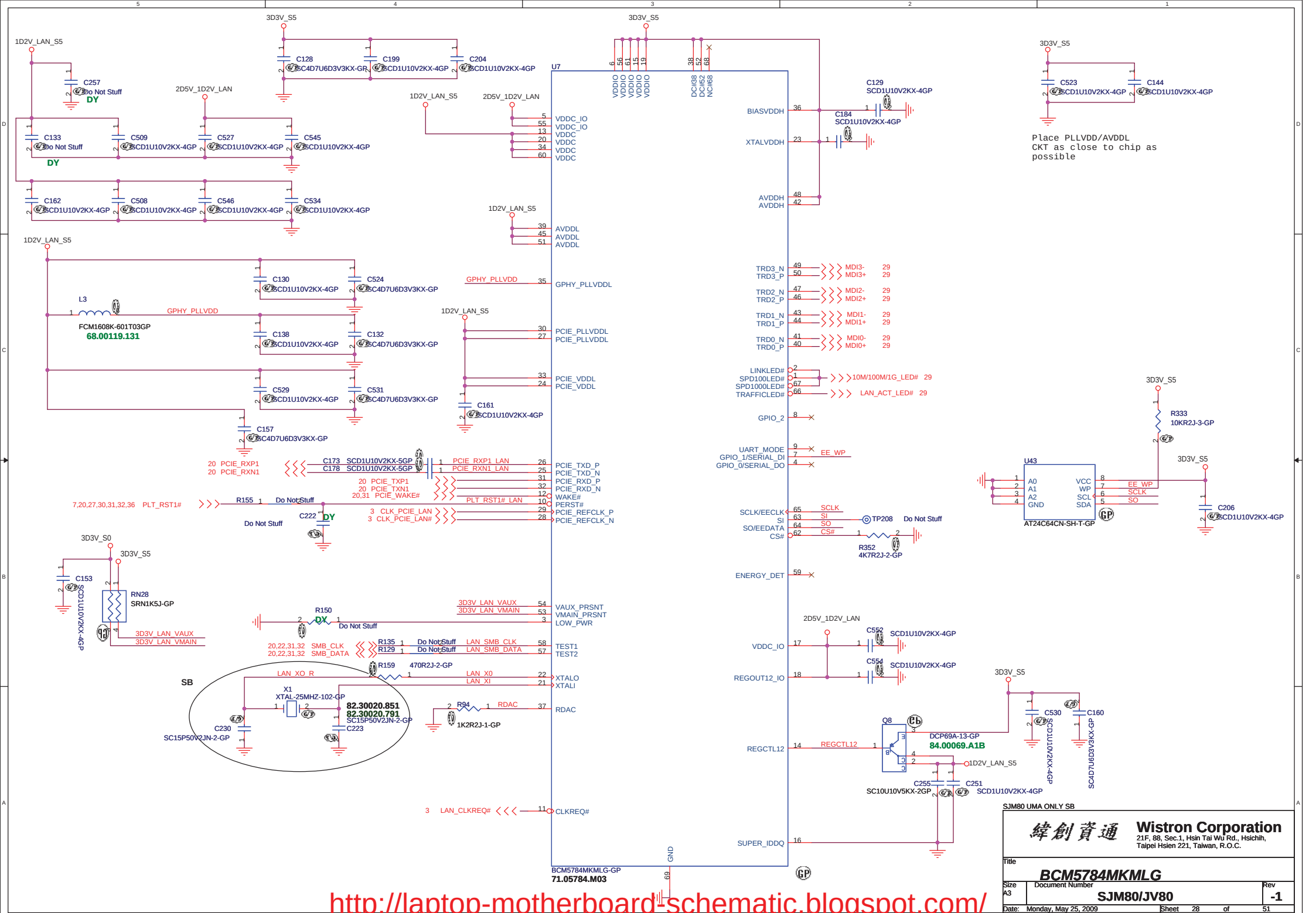
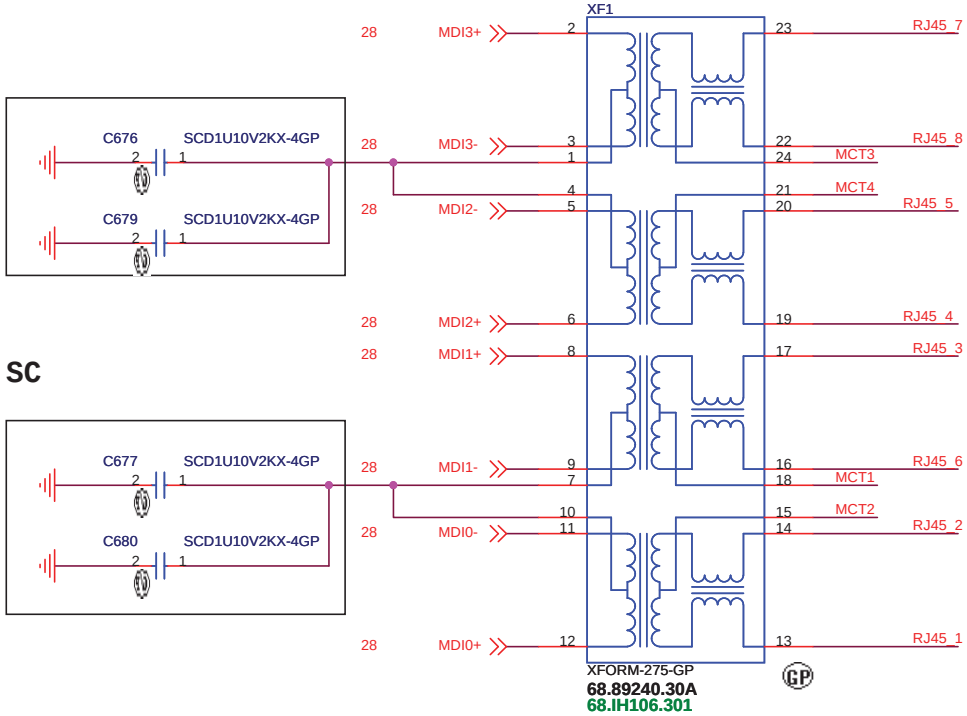


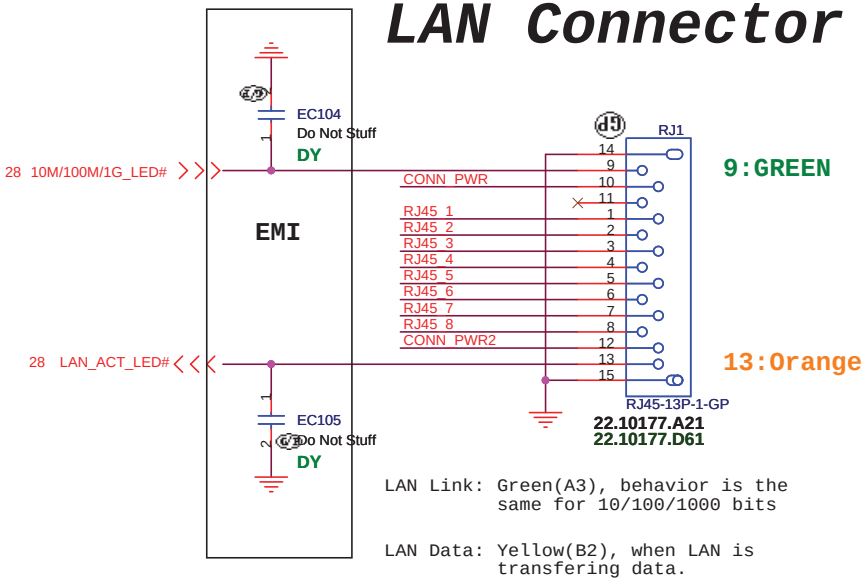
http://laptop-motherboard-schematic.blogspot.com/

LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

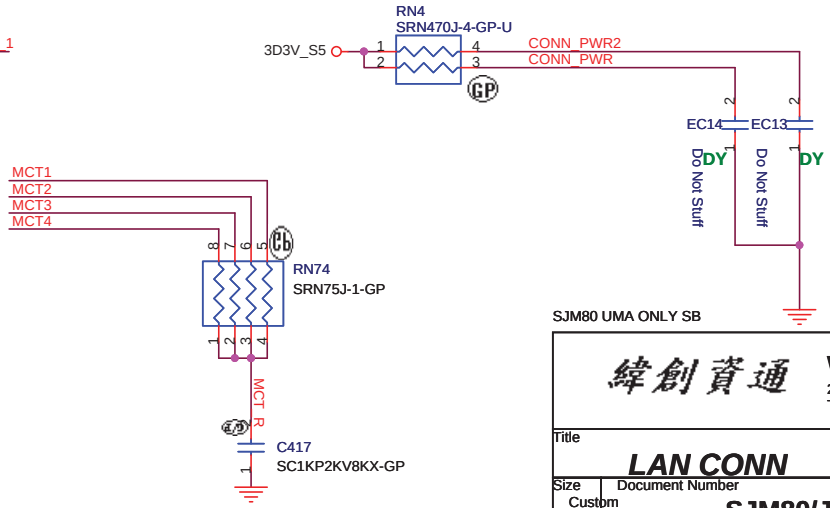


LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.



SJM80 UMA ONLY SB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LAN CONN**	
Size Custom	Document Number **SJM80/JV80**	Rev **-1**
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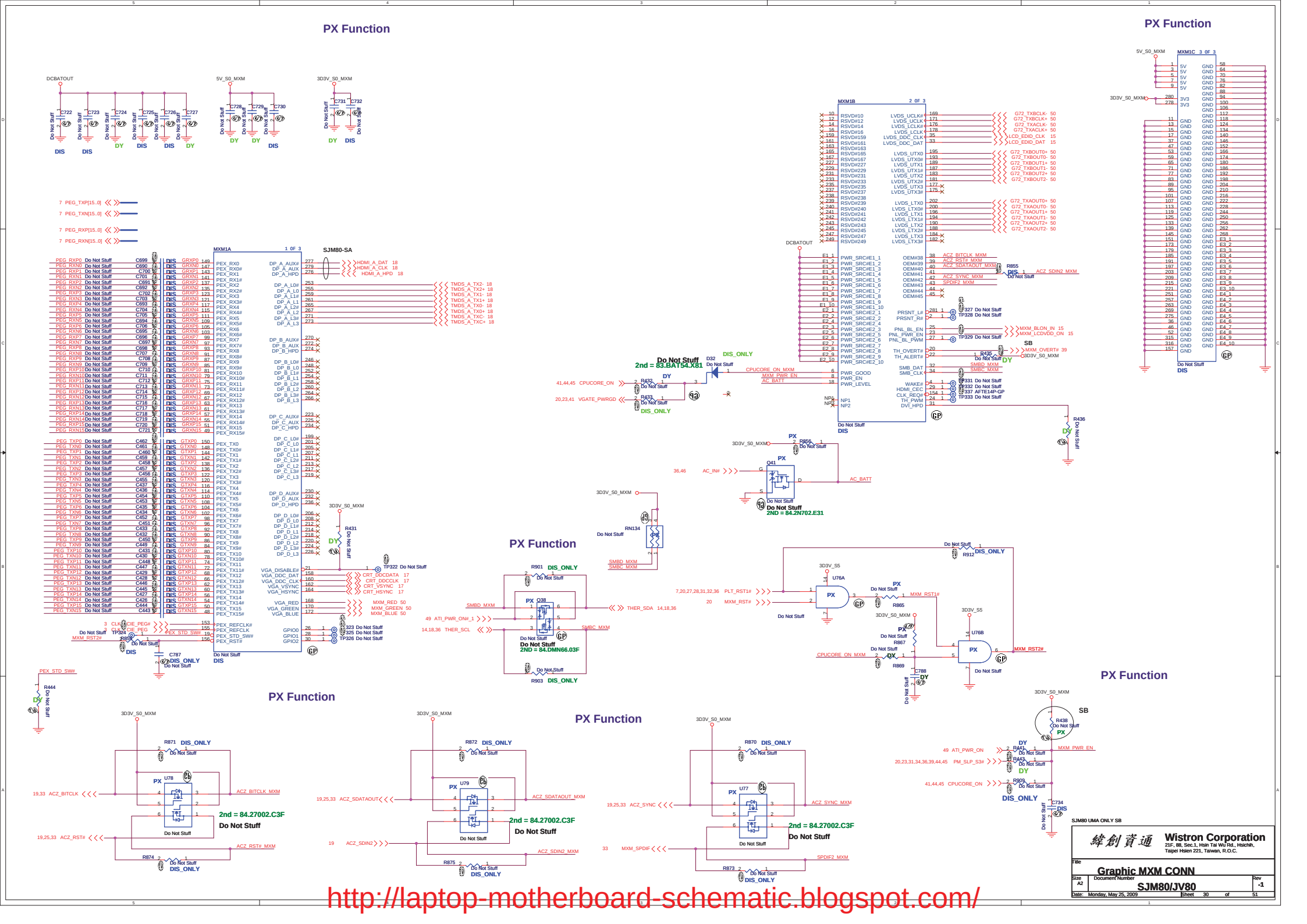
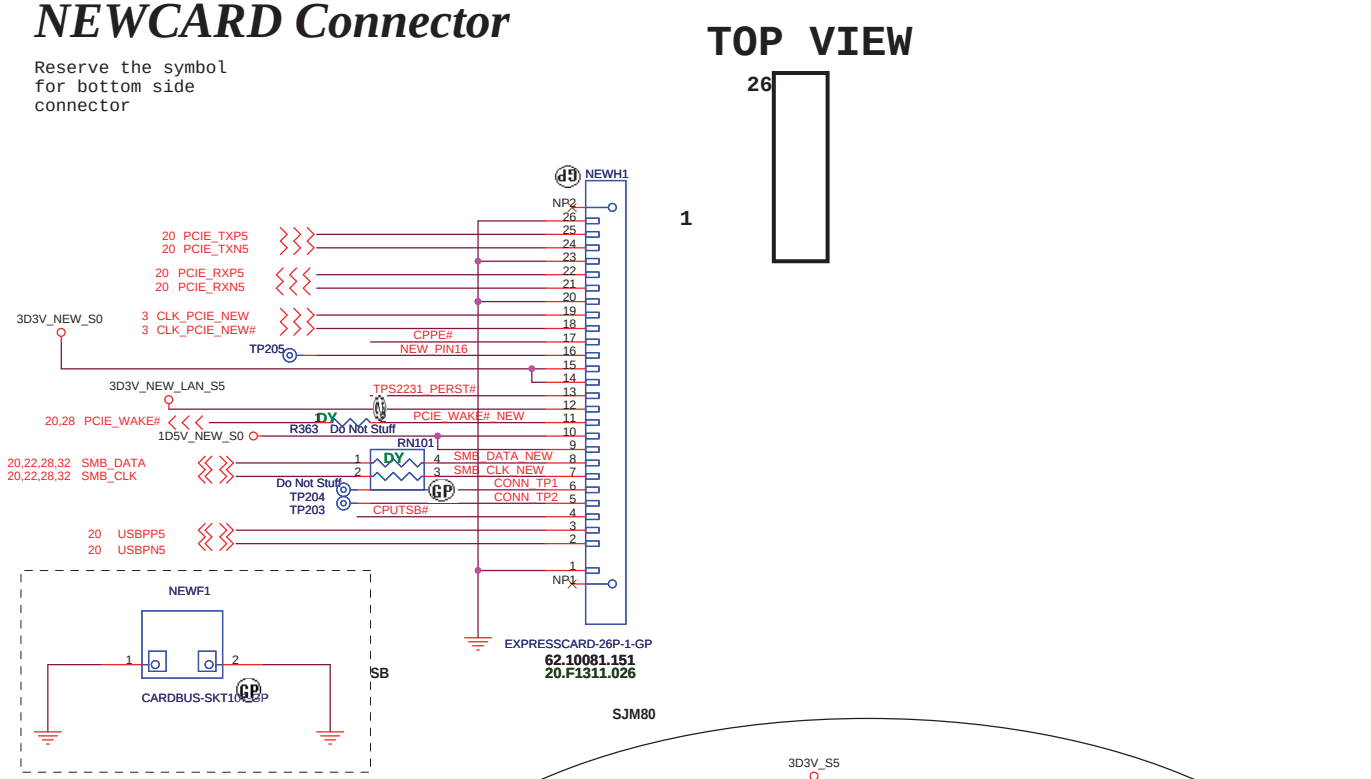
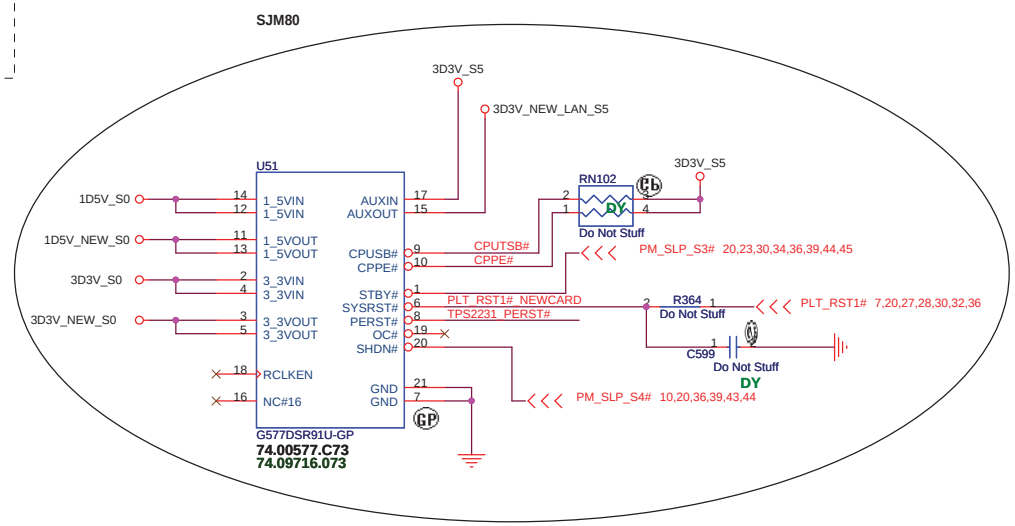


http://laptop-motherboard-schematic.blogspot.com/

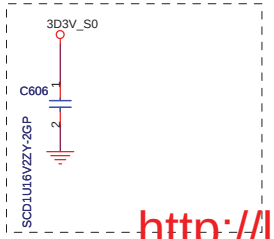
NEWCARD Connector

Reserve the symbol
for bottom side
connector

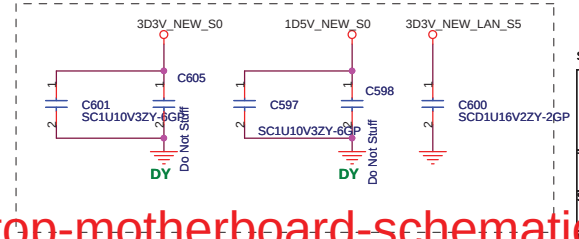




Place them Near to Chip



Place them Near to Connector



SJM80 UMA ONLY SB

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
NEW CARD		
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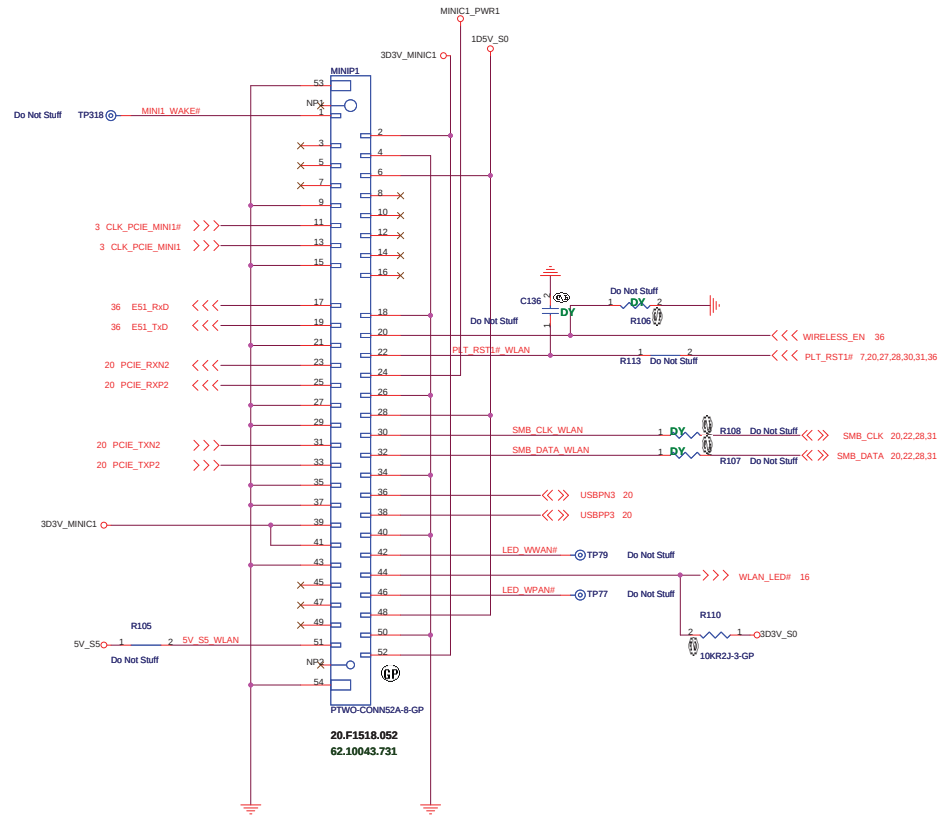
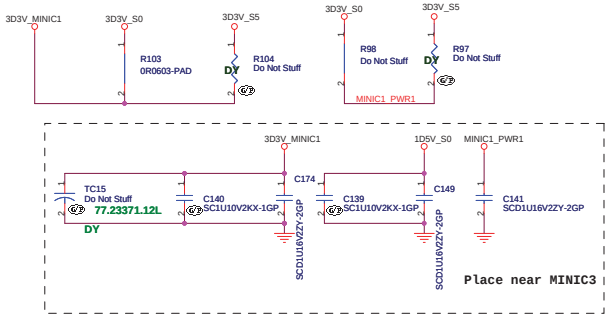
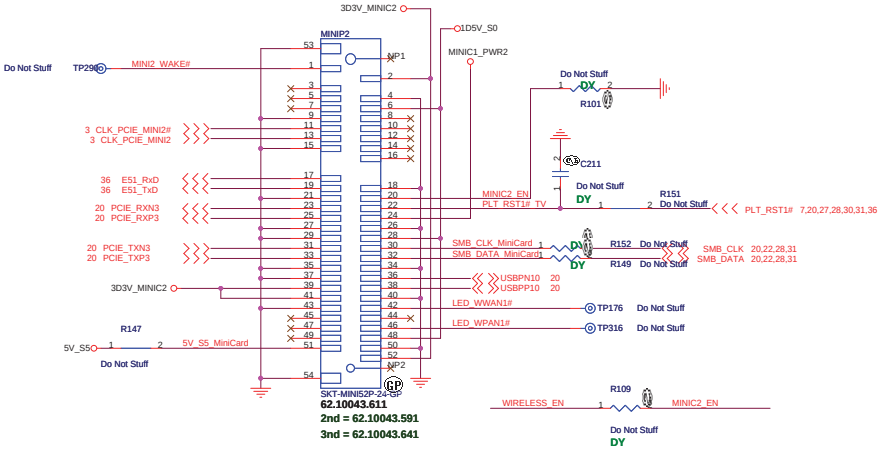
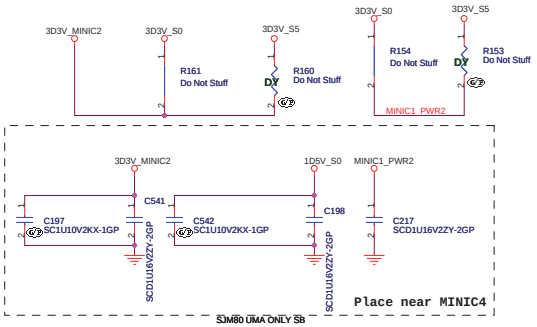
Mini Card Connector(WLAN)









SJM80 UMA ONLY Sb

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	MINI CARD
Size / Document Number	SJM80UMA80
Rev	-1
Custom	
Date: Monday, May 25, 2009	Sheet 32 of 51

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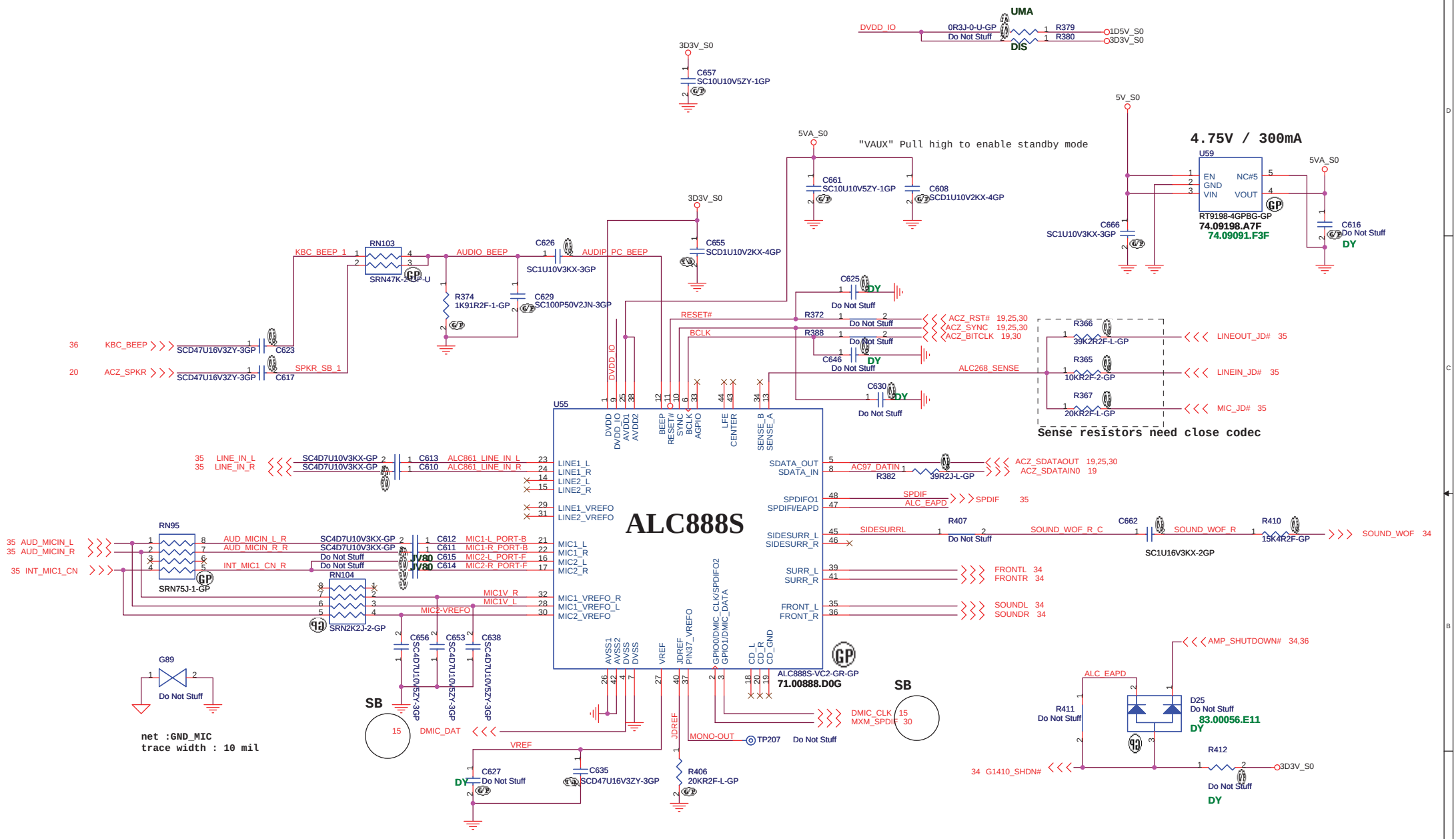

SJM80 UMA ONLY SB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Azalia codec ALC888***	
Size A3	Document Number **SJM80/JV80**	Rev **-1**
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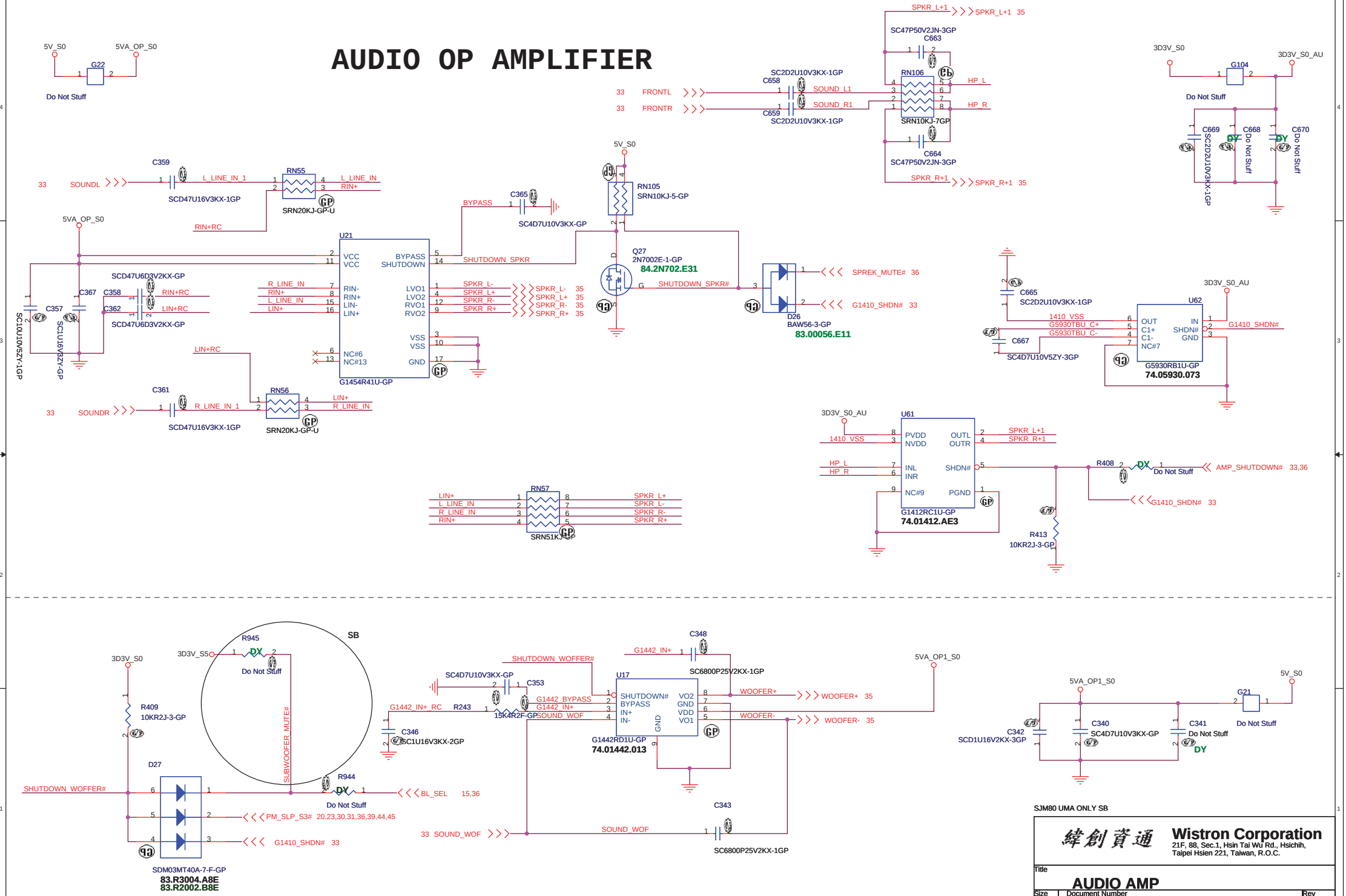
AUDIO OP AMPLIFIER



SJM80 UMA ONLY SB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO AMP	
Size	Document Number: SJM80/JV80	Rev: -1
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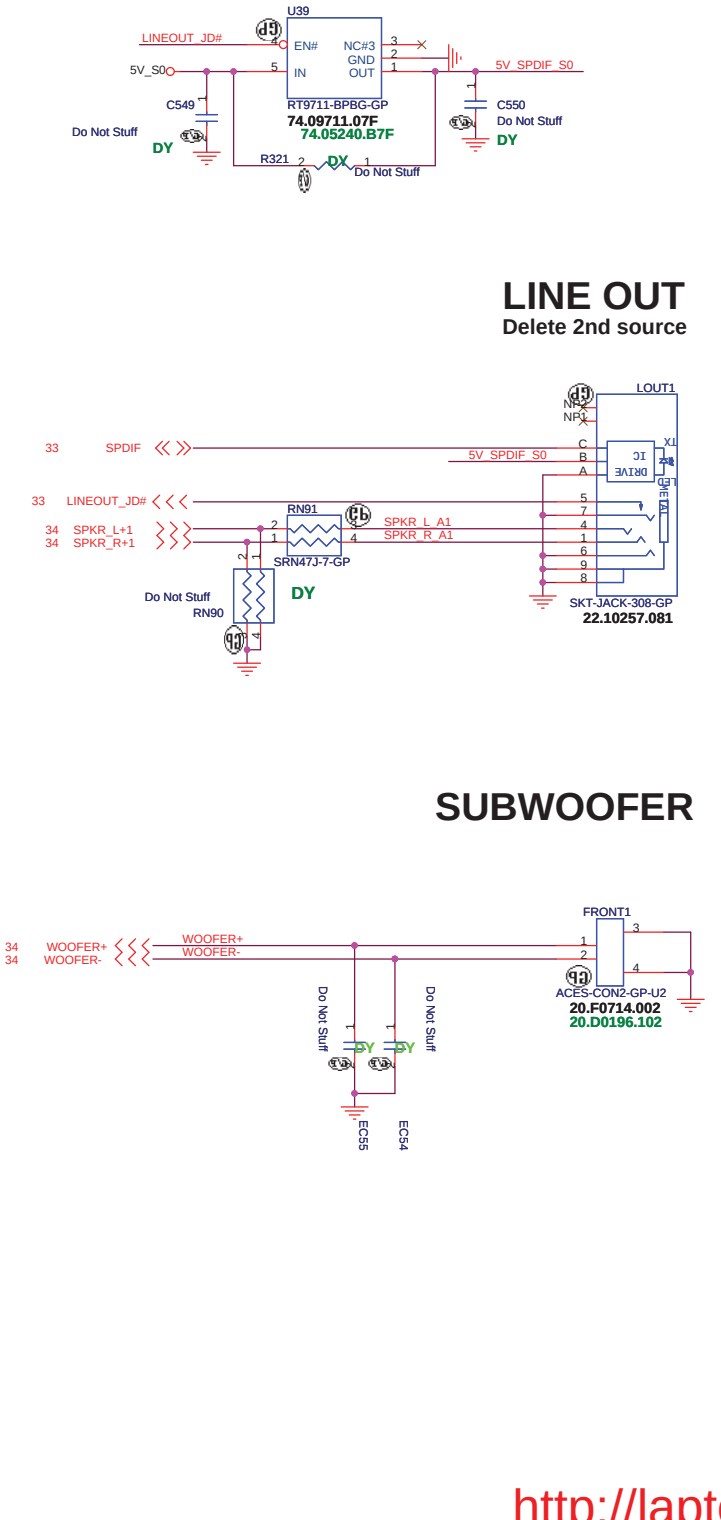

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO JACK**

Size	Document Number	Rev
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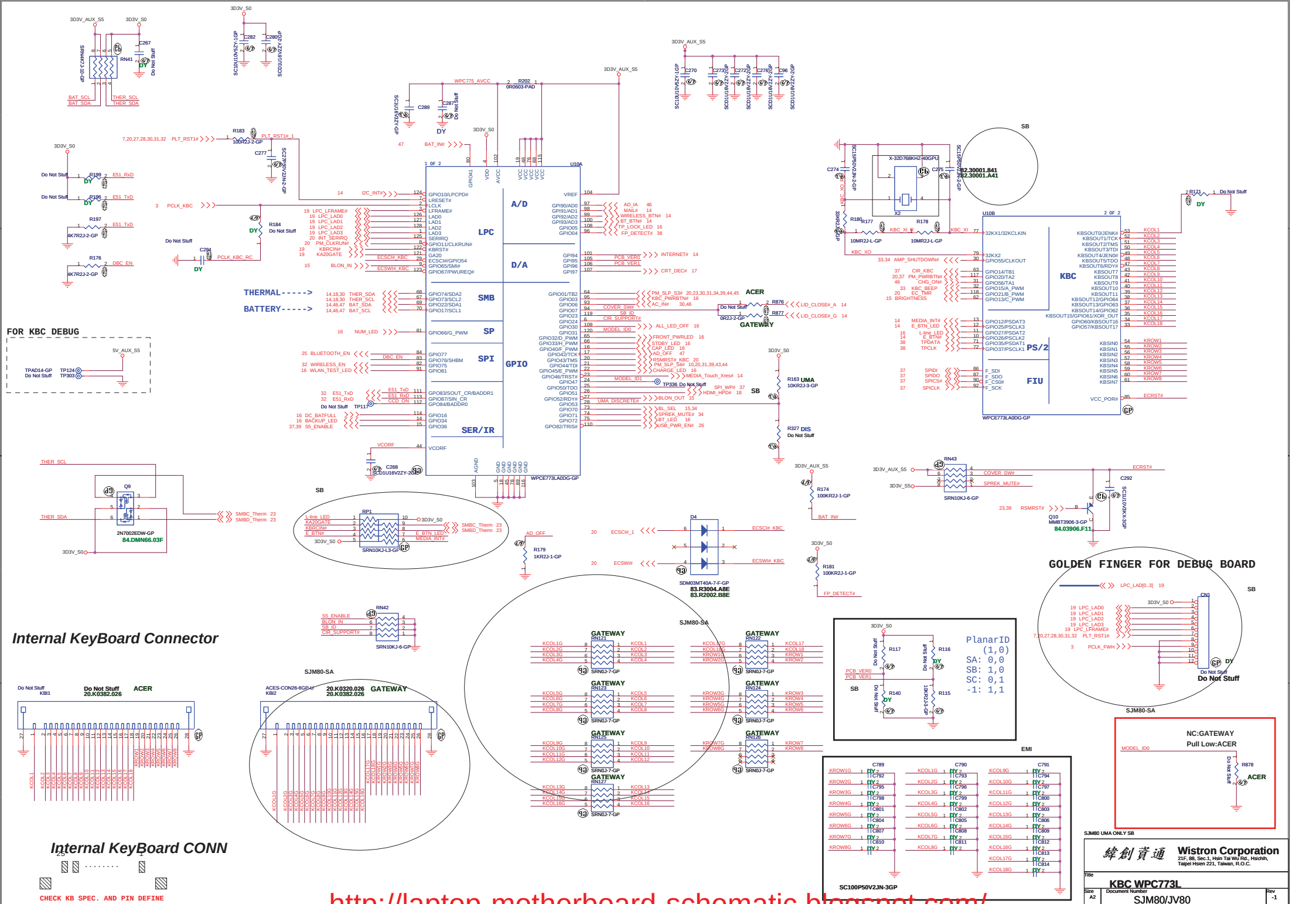

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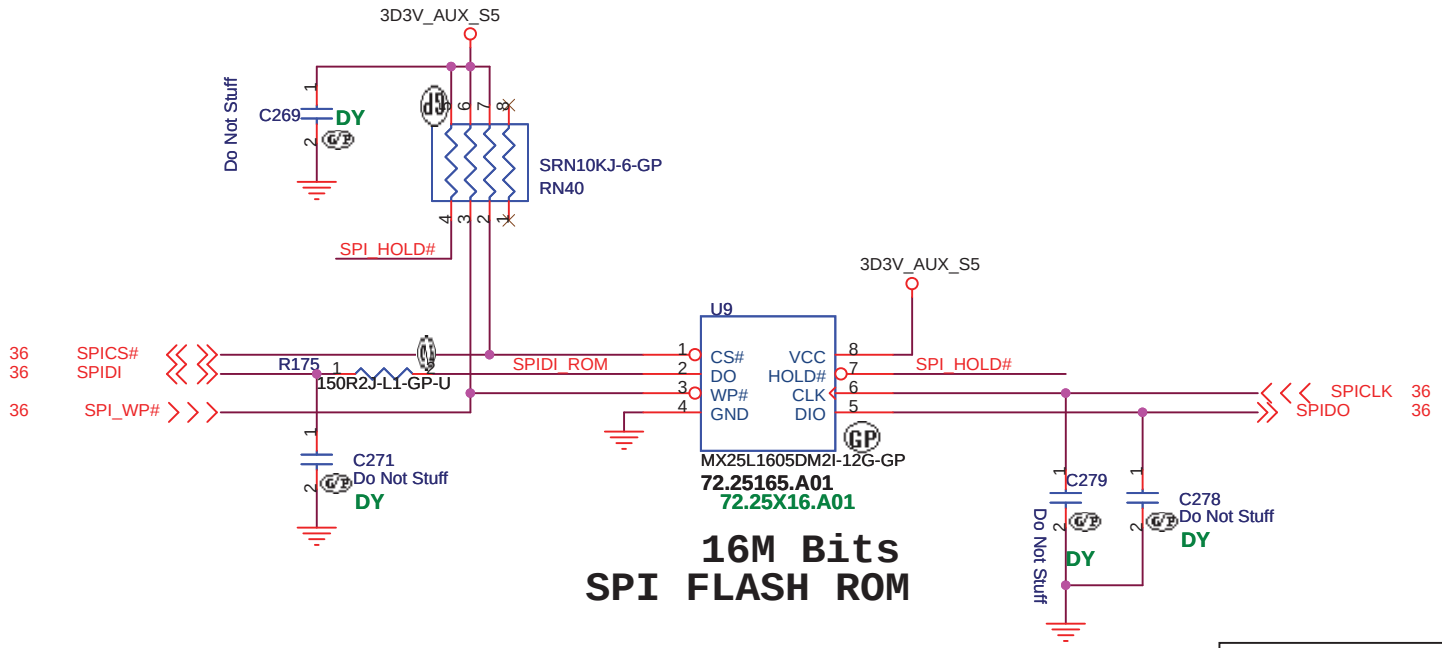
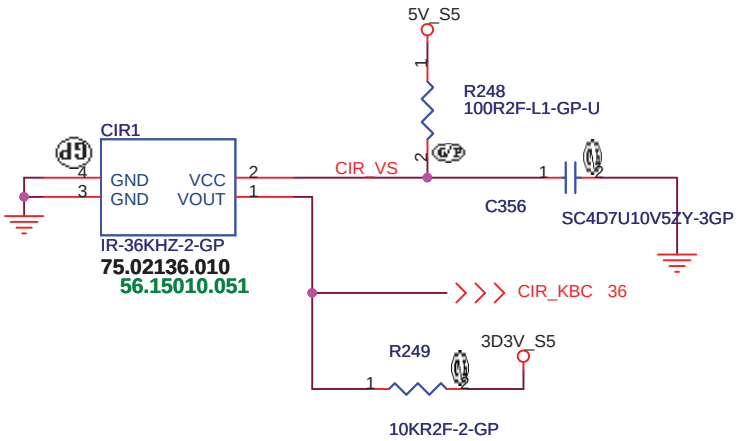


16M Bits
SPI FLASH ROM

CIR Module



Check test point

Test Point放在Dimm Door打開可量測處

SJM80 UMA ONLY SB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BIOS		
Size	Document Number	Rev
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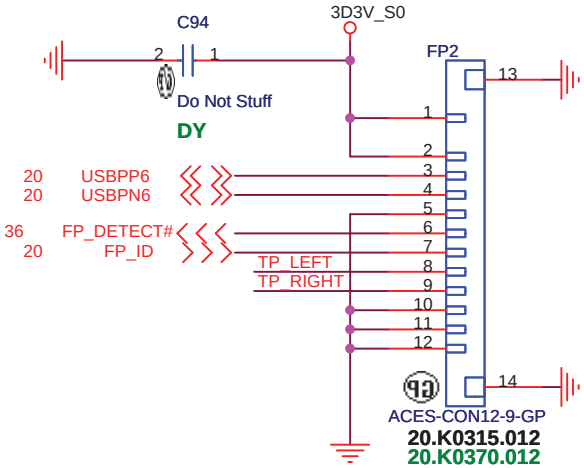
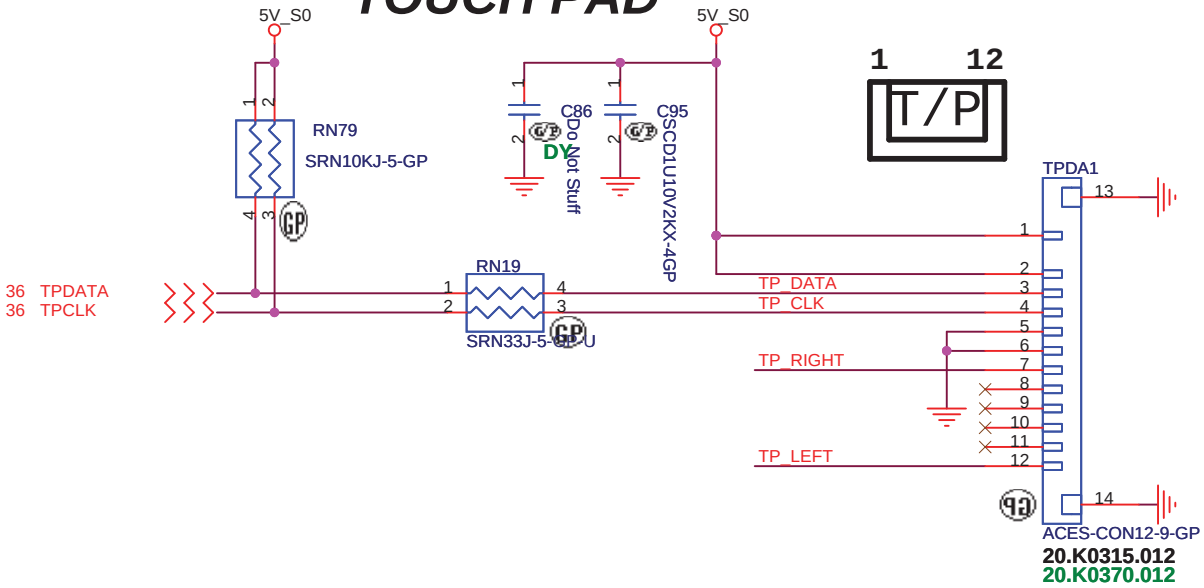
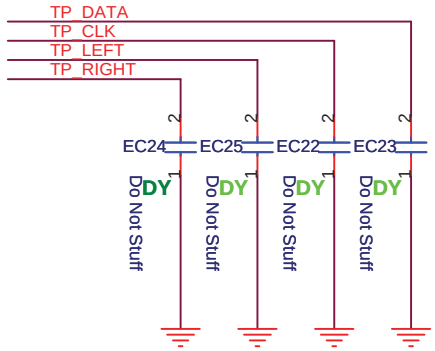
Finger printer



TOUCH PAD





SJM80 UMA ONLY SB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Finger Printer and Touch PAD

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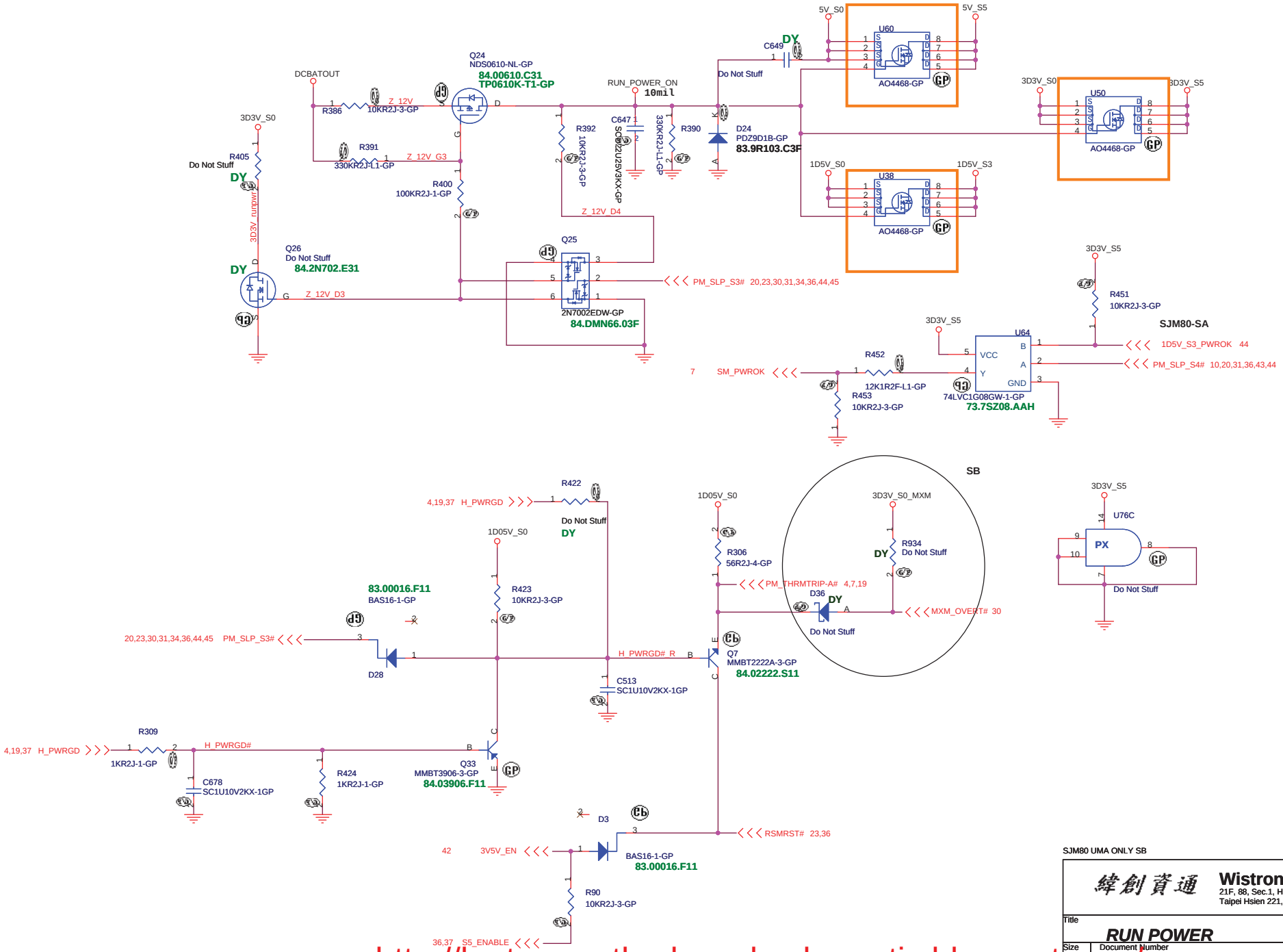
Run Power



SJM80 UMA ONLY SB

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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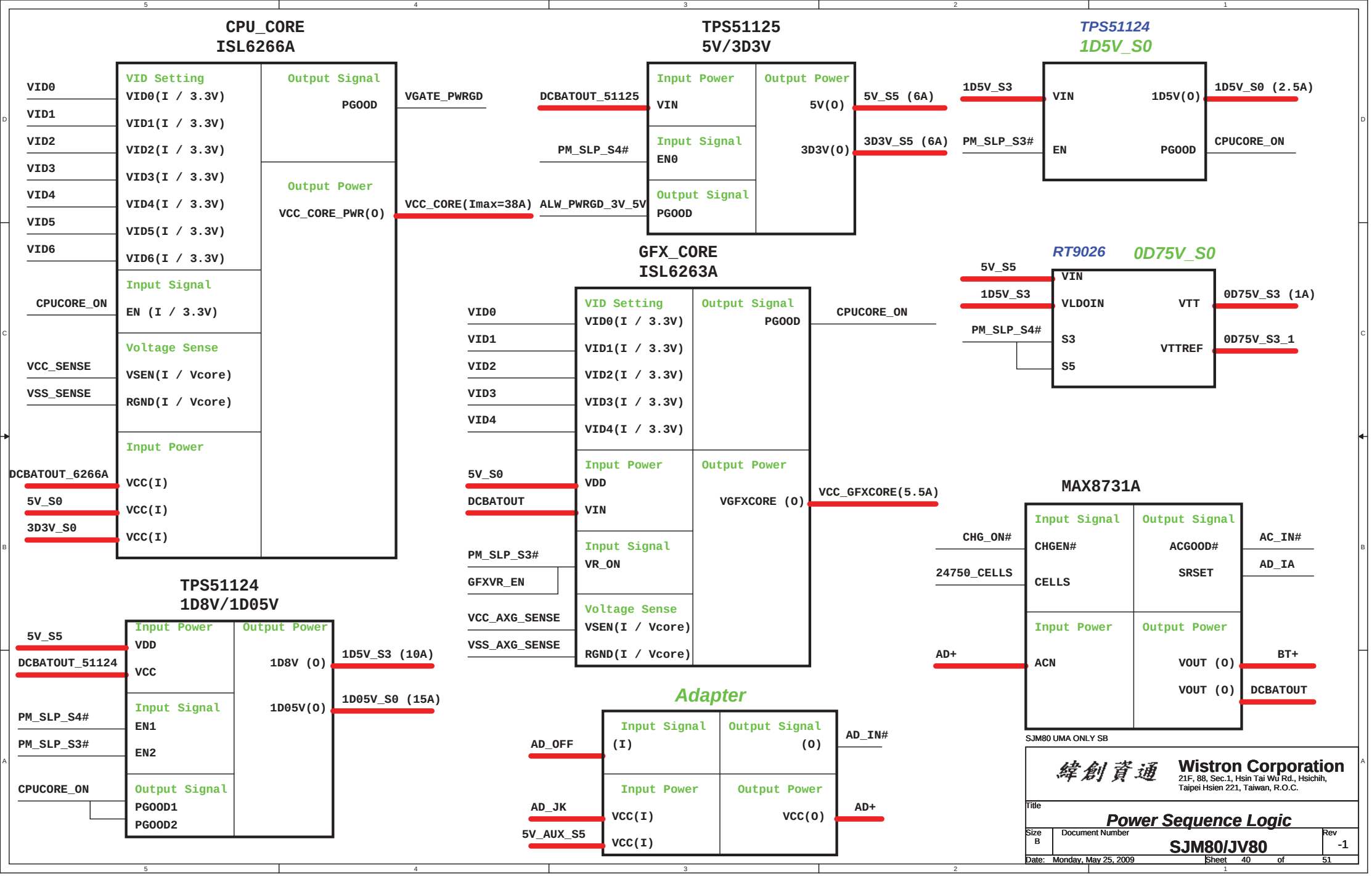
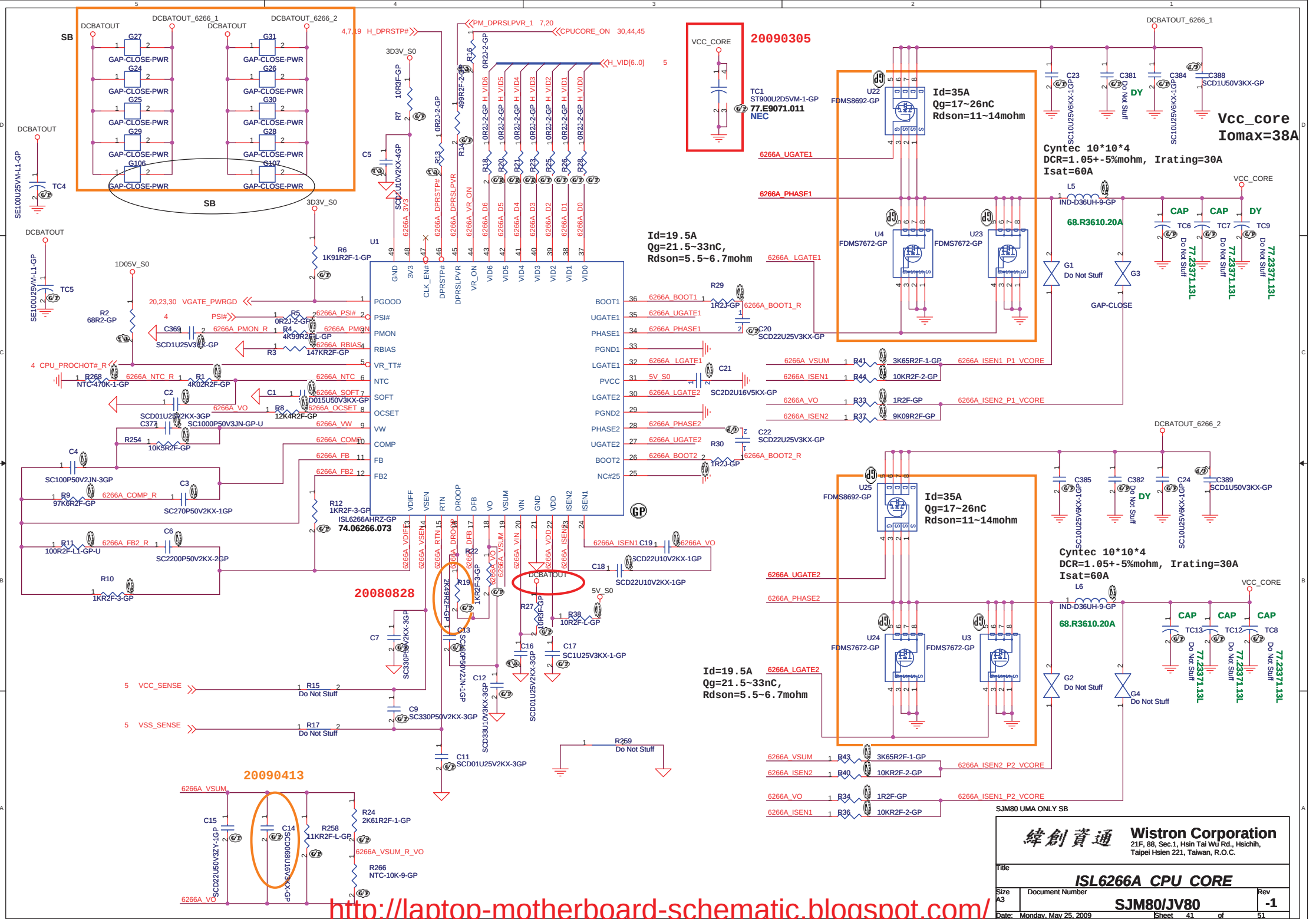
Title		
RUN POWER		
Size	Document Number	Rev
	SJM80/JV80	-1
Date: Monday, May 25, 2009	Sheet 39 of 51	

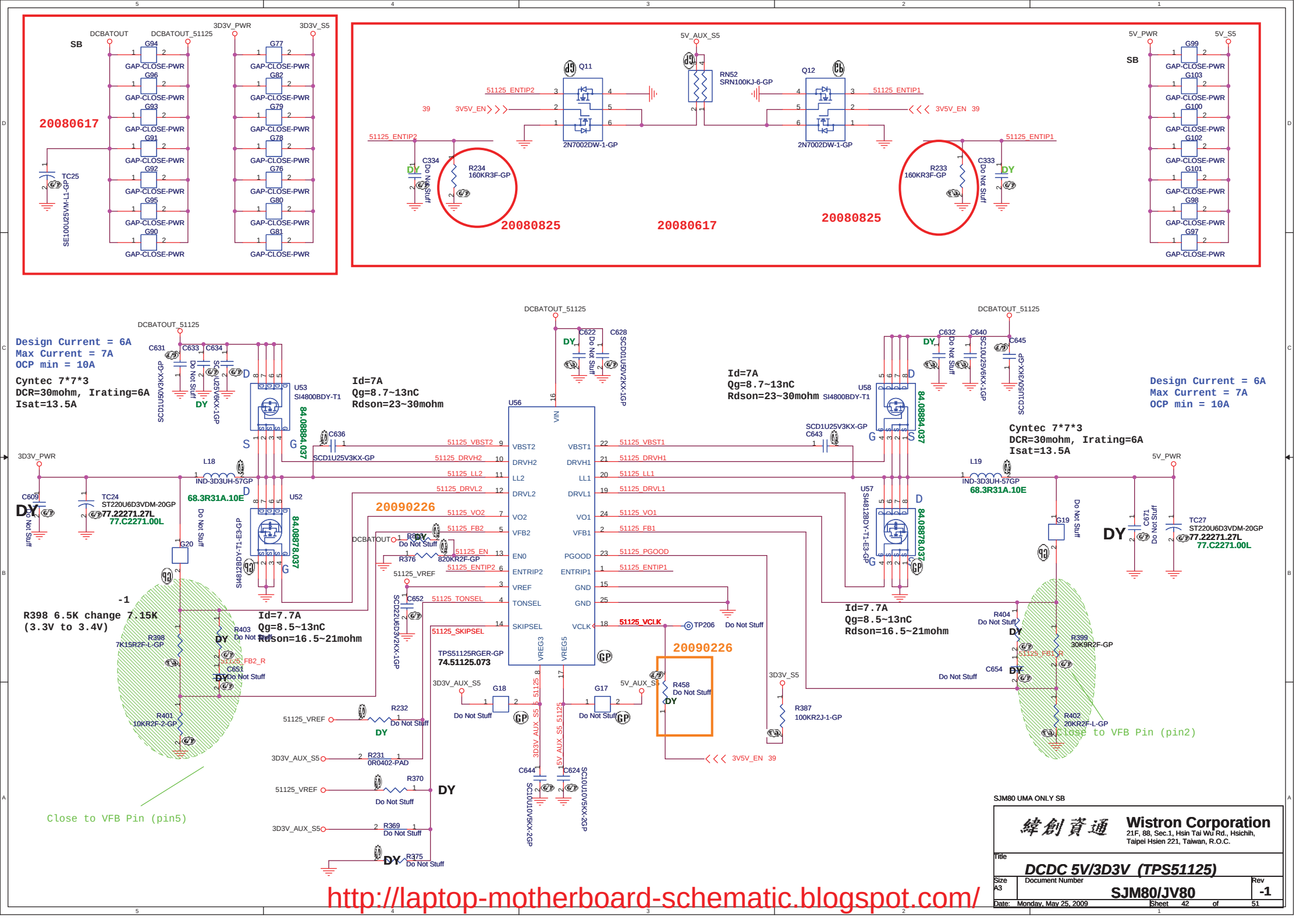
http://laptop-motherboard-schematic.blogspot.com/



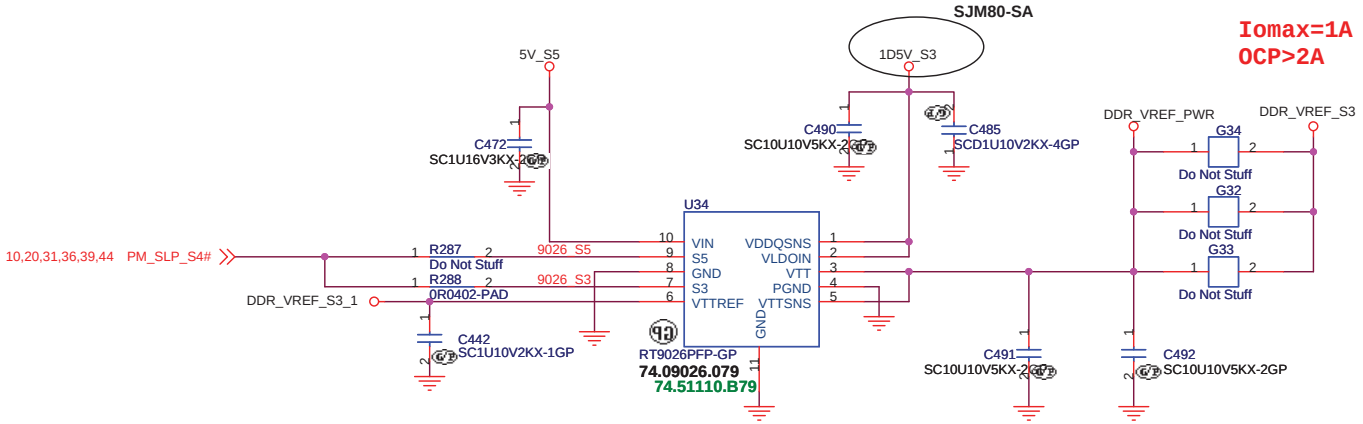
http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/


SJM80 UMA ONLY SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (TPS51125)
Size A3
Document Number
SJM80/JV80
Rev -1
Date: Monday, May 25, 2009
Sheet 42 of 51
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
R398 6.5K change 7.15K
(3.3V to 3.4V)
TPS51125RGER-GP
74.51125.073
20080617
20080825
20090226
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
http://laptop-motherboard-schematic.blogspot.com/

SJM80-SA



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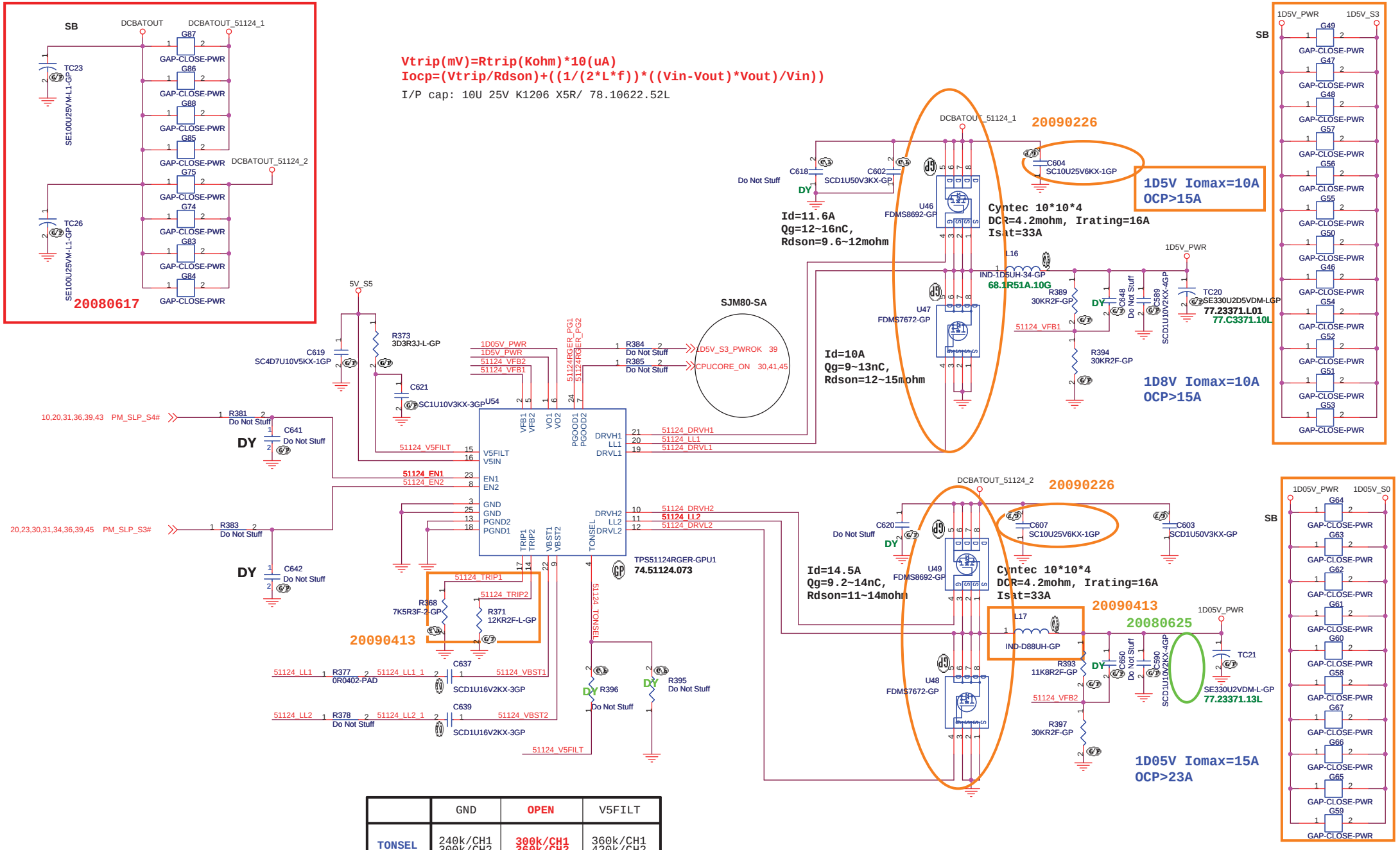
Title	***1D5V & 0D75V***	
Size Custom	Document Number **SJM80/JV80**	Rev **-1**
Date: Monday, May 25, 2009	Sheet 43 of 51	

http://laptop-motherboard-schematic.blogspot.com/



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

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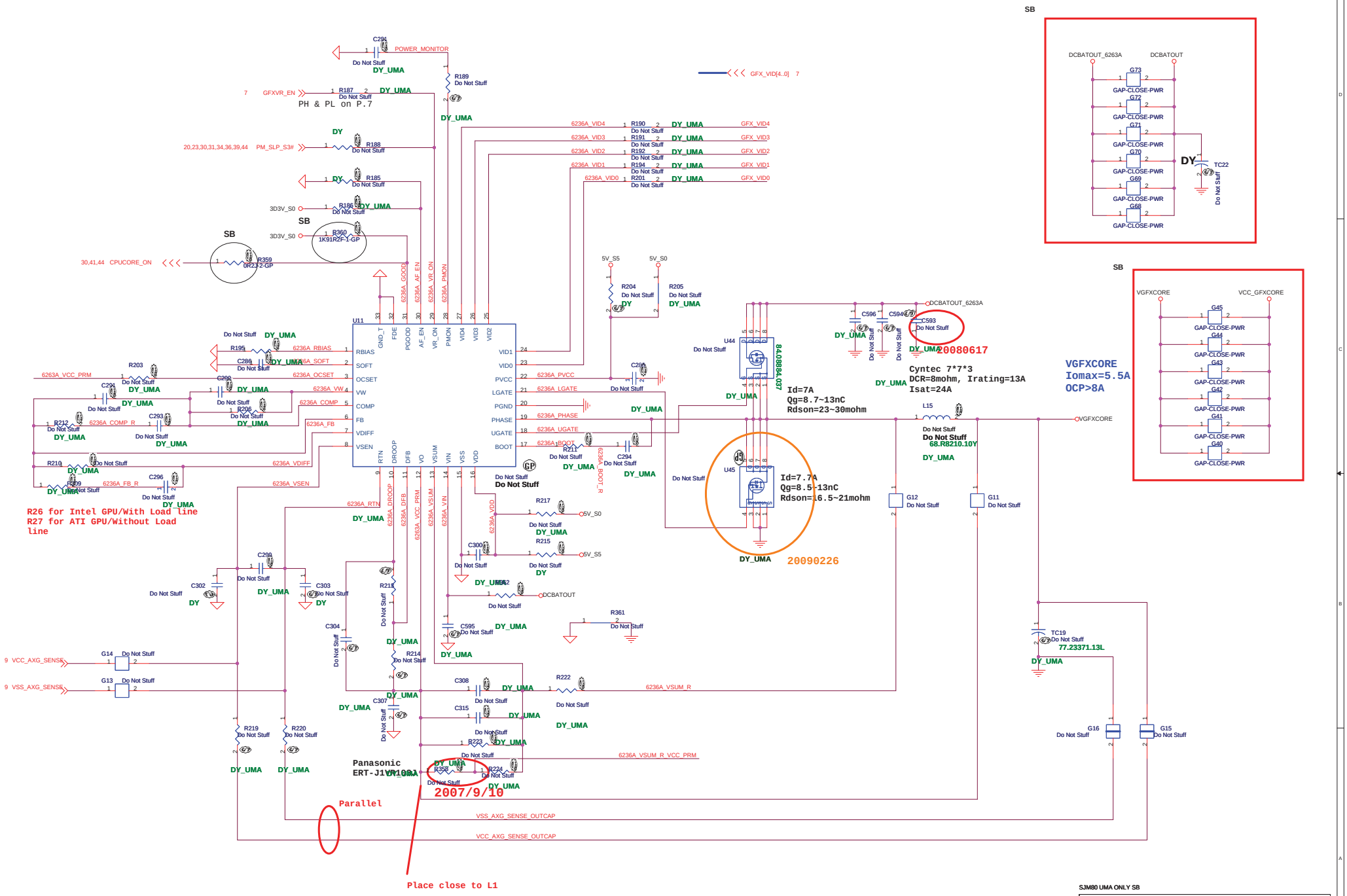
Title: TPS51124 1D5V 1D05V

Size: A3 | Document Number: SJM80/JV80 | Rev: -1

Date: Monday, May 25, 2009 | Sheet 44 of 51

http://laptop-motherboard-schematic.blogspot.com/



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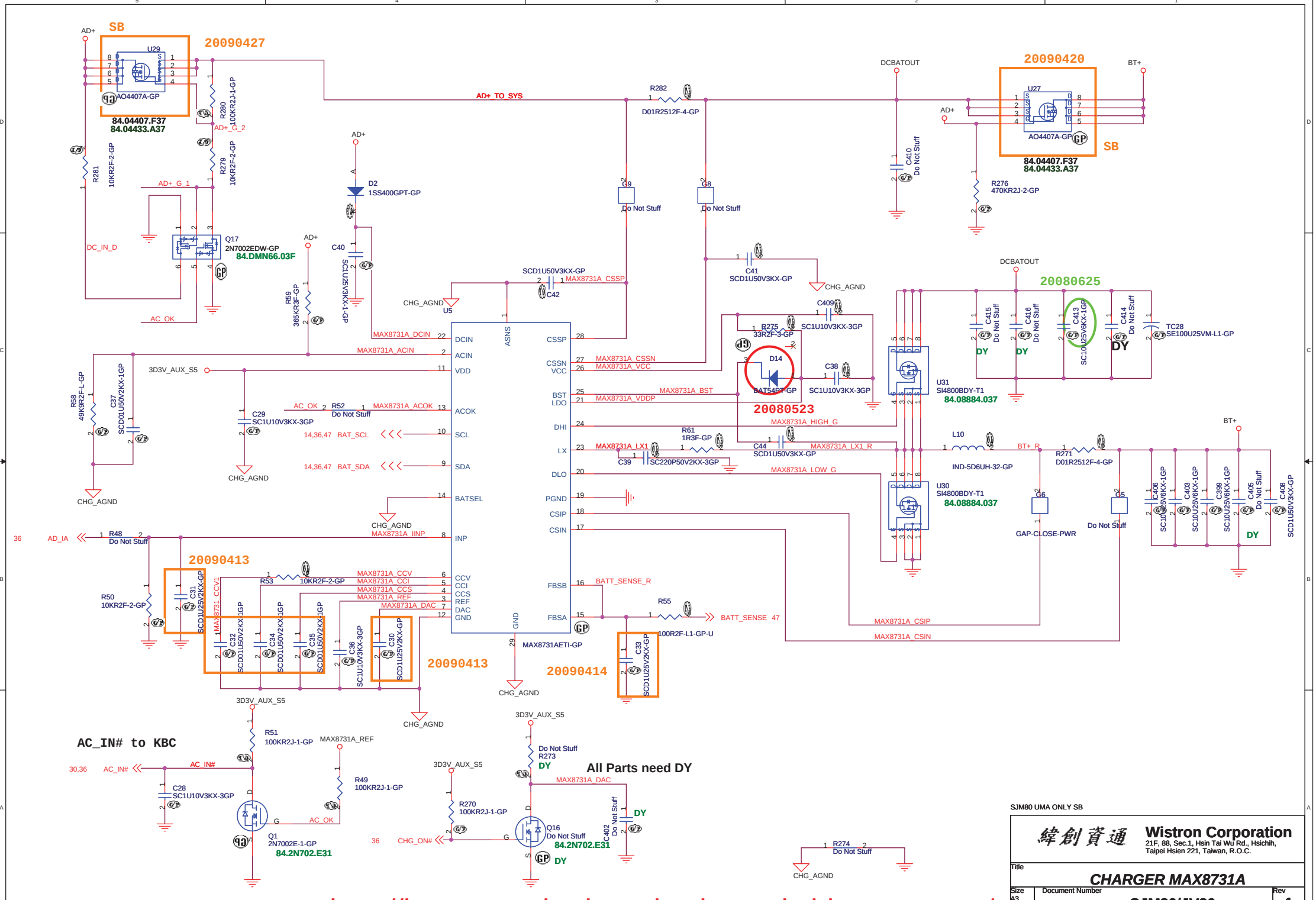
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6263A_GFX CORE

Size: C | Document Number: SJM80/JV80 | Rev: -1

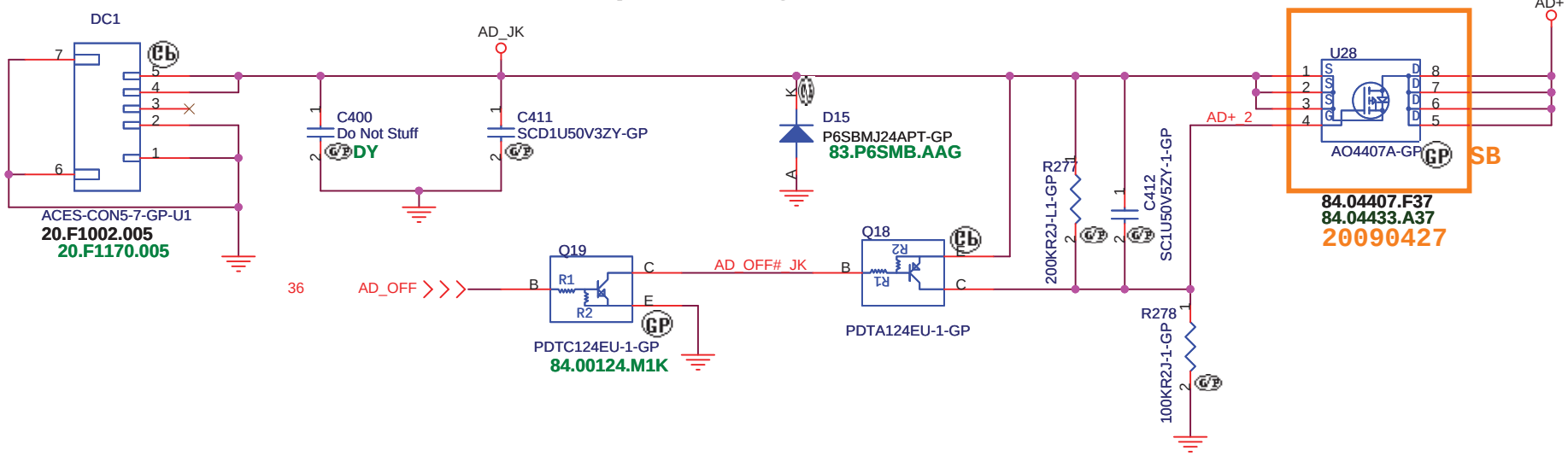
Date: Monday, May 25, 2009 | Sheet 45 of 51

http://laptop-motherboard-schematic.blogspot.com/

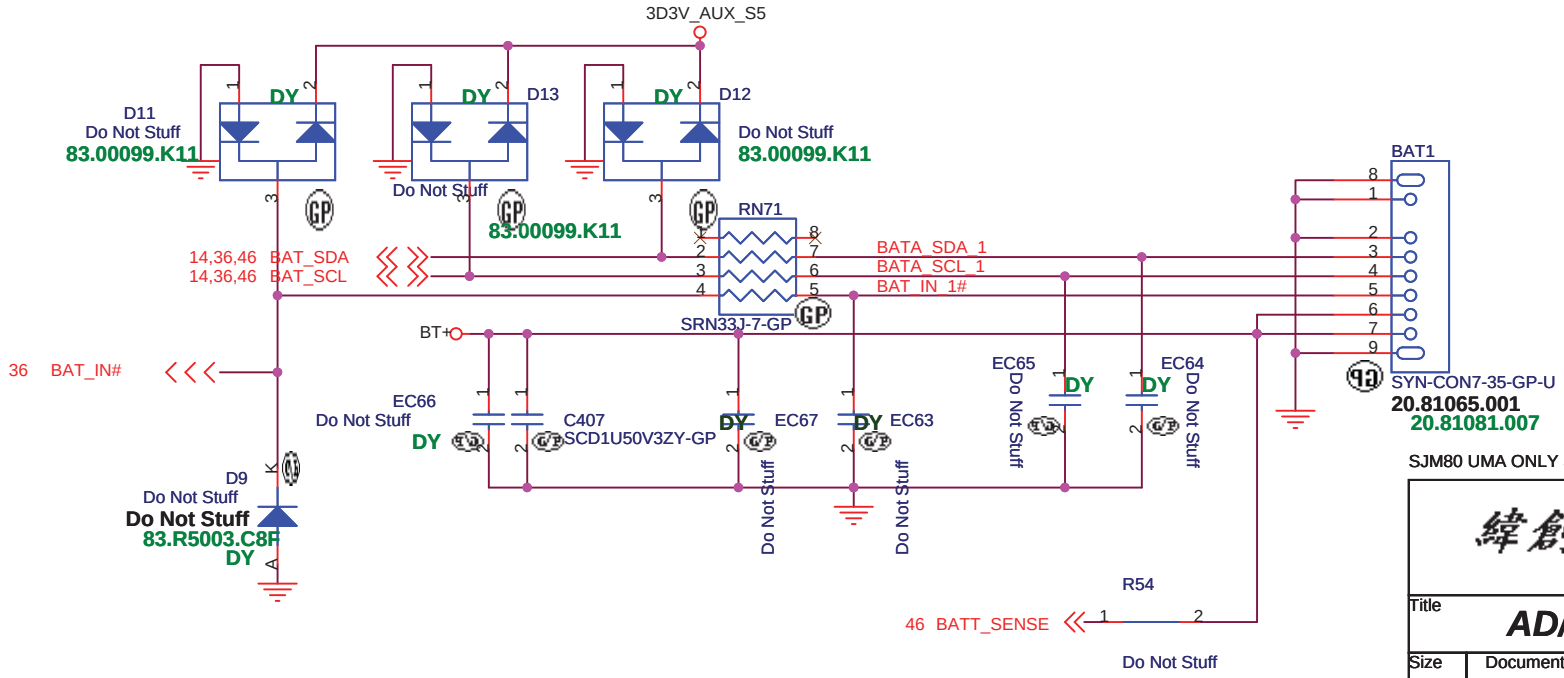


http://laptop-motherboard-schematic.blogspot.com/

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AD/BATT CONN***	
Size	Document Number **SJM80/JV80**	Rev -1
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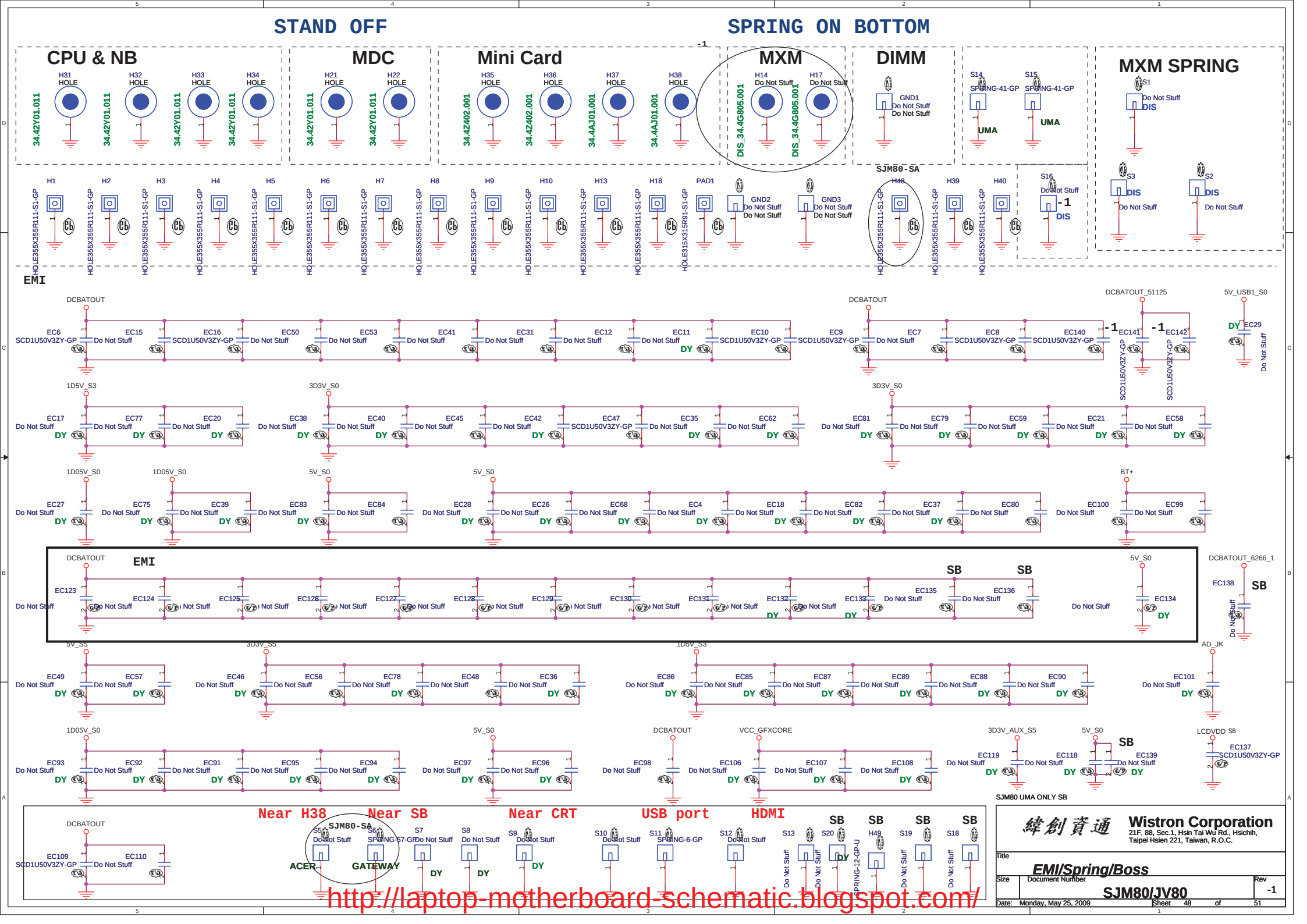
http://laptop-motherboard-schematic.blogspot.com/


STAND OFF
SPRING ON BOTTOM
CPU & NB
MDC
Mini Card
MXM
DIMM
MXM SPRING
EMI
Near H38
Near SB
Near CRT
USB port
HDMI
SJM80 UMA ONLY SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
SJM80/JV80
Rev
-1
Date: Monday, May 25, 2009
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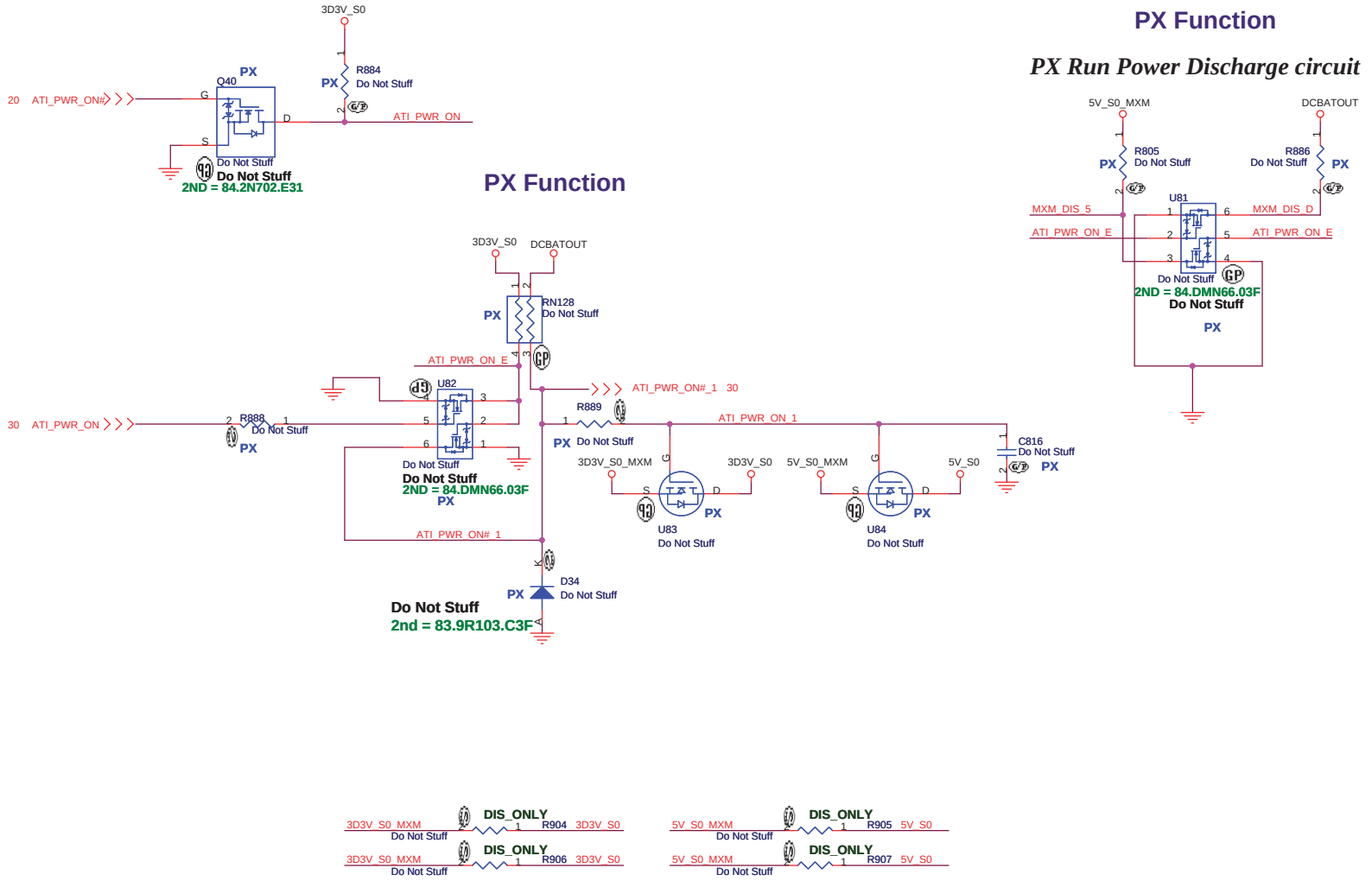

SJM80 UMA ONLY SB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PX Run Power***	
Size	Document Number **SJM80/JV80**	Rev -1
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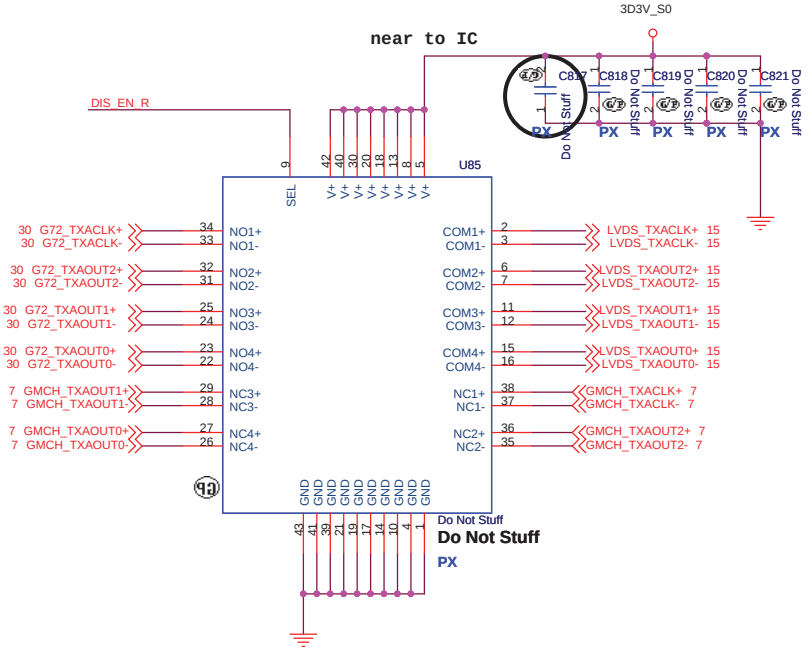
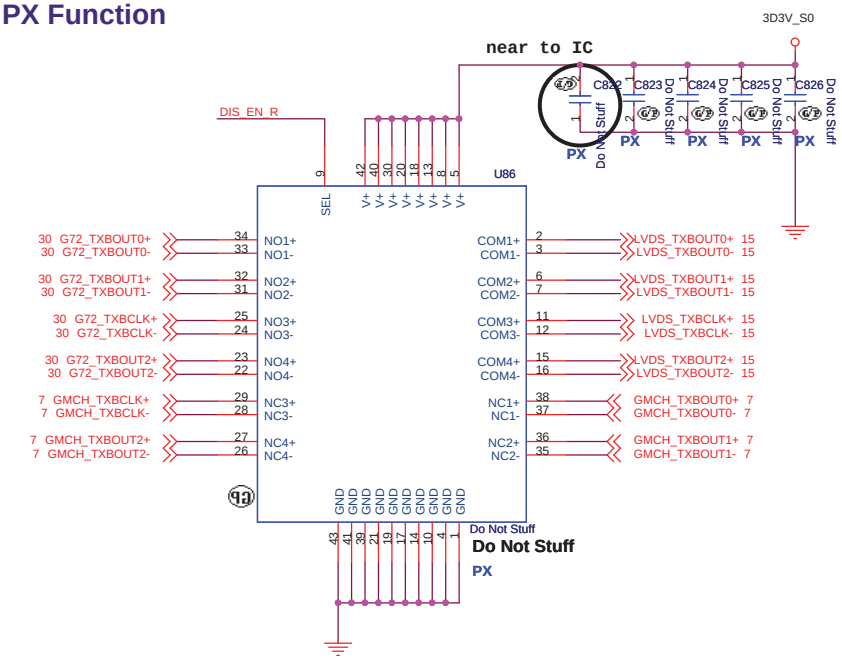
PX Function

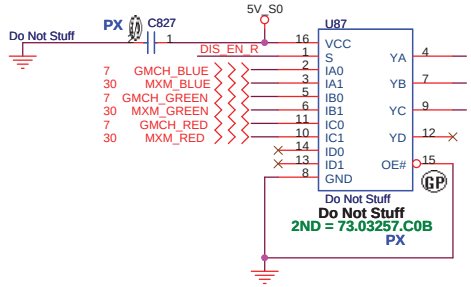


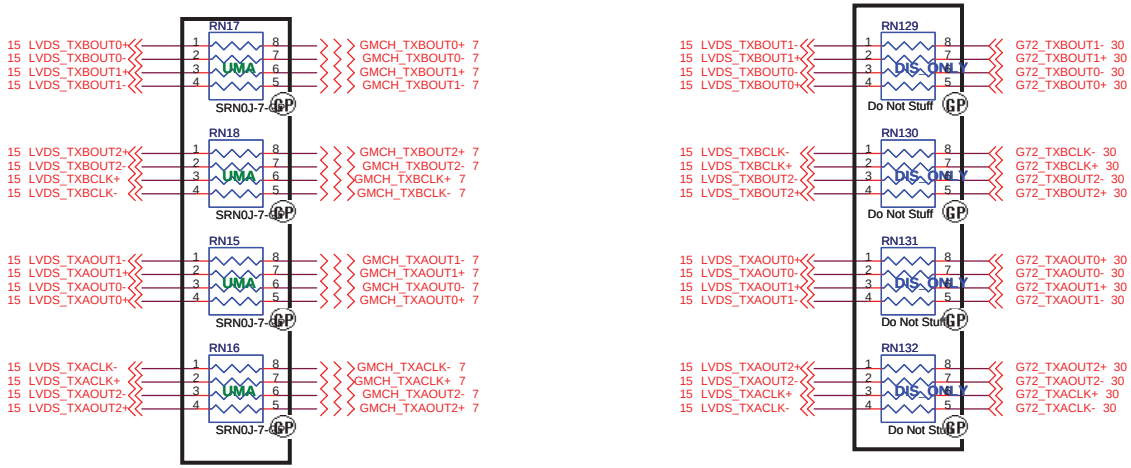


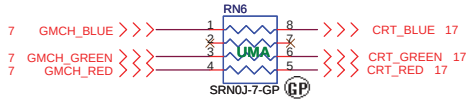
$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

DIS_EN_R Low = UMA
DIS_EN_R High = DIS

PX Function







SJM80 UMA ONLY SB

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *PX Switch*

Size | Document Number: SJM80/JV80 | Rev: -1

Date: Monday, May 25, 2009 | Sheet 50 of 51

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SJM80 Schematic EC Tracking Record LAB 0325 , 2009
EC #/ Page / Description / Part Affected

EC SB03/26/change R359 R360 上件(for PX function)
EC SB03/26/change RN27 RN31 RN32 RN33 上件(for PX function)
EC SC03/30 change REAR1,REAR2 Net name
EC SB03/31 add digital Mic function
EC SB04/03 change Brightness setting from NB
EC SB04/03 modify MMB BD add switch
EC SB04/06 Change LAN Crystal setting
EC SB04/07 Close Power GAP
EC SB04/07 Change PCB Version
EC SB04/13 Keep JV80 GPIO and Function Key
EC SB04/20 add R946 R947 for BRIGHTNESS Bypass
EC -105/03 change C834~C841 to 0 ohm for HDMI no display design
EC -105/03 add R948 for DIS ONLY HDP
EC -105/03 change R823 to R824 for CRT no display
EC -105/13 change MXM Card Stand off part number
EC -105/19 MMBCN1 power 3D3V change 5V (for MMB LED light display)
EC -105/19 Modify HDMI hot plug schematic Location Q46
EC -105/20 change R316 to 22R2 (For USB eye diagram)
EC -105/20 change R398 6.5k to 7.1K increase 3.3V to 3.4V
EC -105/21 Q46 HDMI hot plug change power 3D3V_S0_MXM to 5V_S0
EC -105/22 add Cap for EMI at CRT RGB

EC -1 01/20/Change R316 to 22D6R2F(For USB eye diagram)

SJM80 UMA ONLY SB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EC Tracking Record
Size | Document Number: SJM80/JV80 | Rev: -1
Date: Monday, May 25, 2009 | Sheet 51 of 51

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