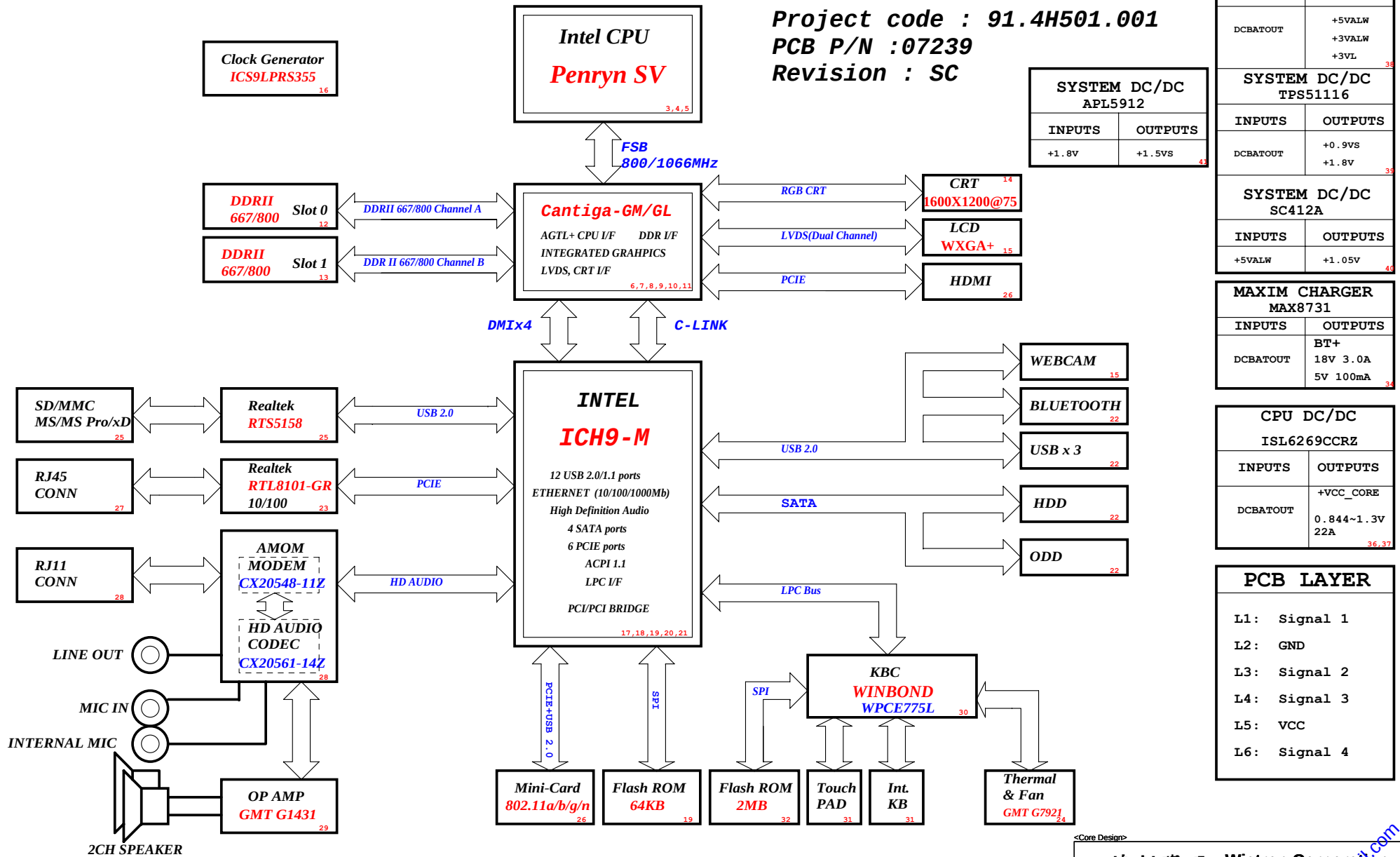


Warrior Intel UMA Block Diagram

Project code : 91.4H501.001

PCB P/N : 07239

Revision : SC



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

Title

Block Diagram .

Size

Document Number

Warrior	SC
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Date: Friday, January 04, 2008

Sheet 1 of 42

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1. Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: Offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Configurable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPT, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

PCIE Routing page 19

LANE1	LAN
LANE2	MiniCard WLAN

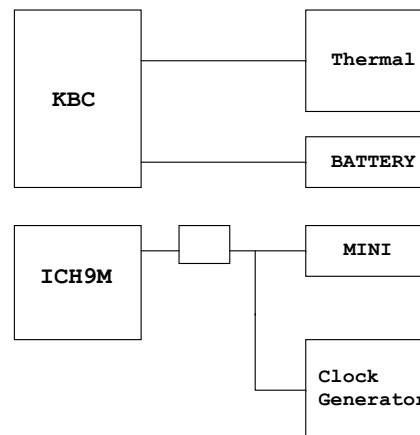
USB Table page 19

USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

ICH9 Integrated pull-up and pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLEPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determine by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

SMBus



Cantiga chipset and ICH9M I/O controller
Hub strapping configuration

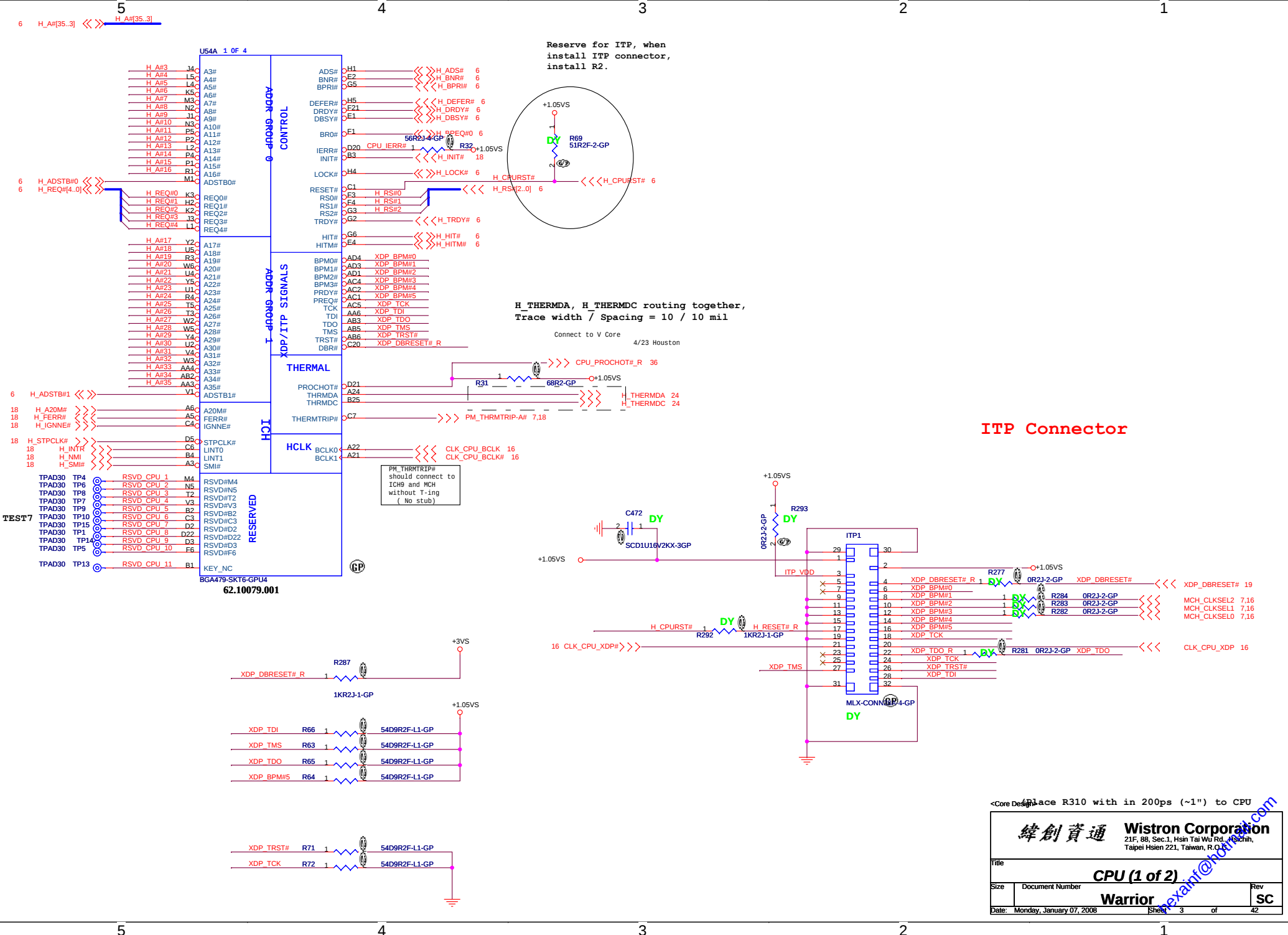
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (Default)
CFG9	PCIe Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) 11 = Disabled (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: {3->0, 2->1, 1->2 and 0->3} DMI x2 mode [MCH->ICH]: {3->0, 2->1}
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIe disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

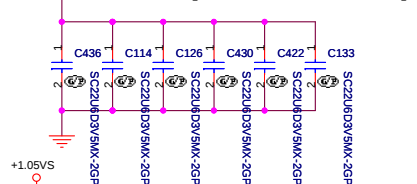
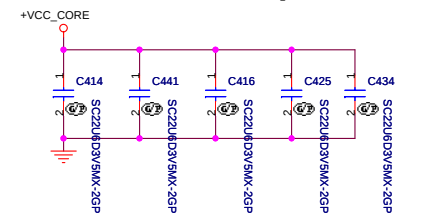
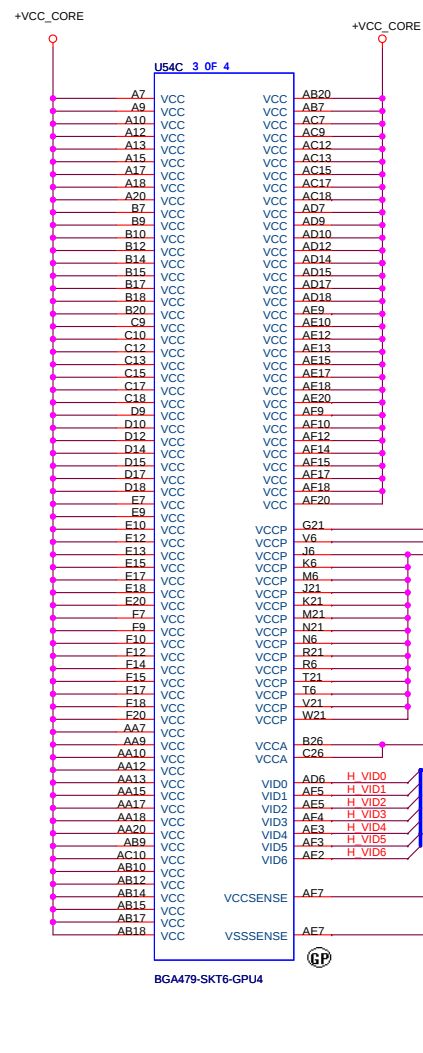
<Core Design>

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Table of Content Warrior	
Size A3	Document Number
Date: 2008.04.04	Sheet 2 of 12





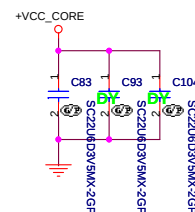
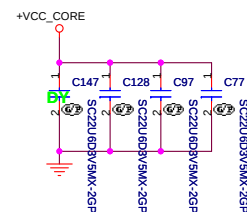
Layout Note:
Comp0, 2 connect with $Z_0=27.4\ \Omega$, make
trace length shorter than 0.5λ .
Comp1, 3 connect with $Z_0=55\ \Omega$, make
trace length shorter than 0.5λ .

[illegible]

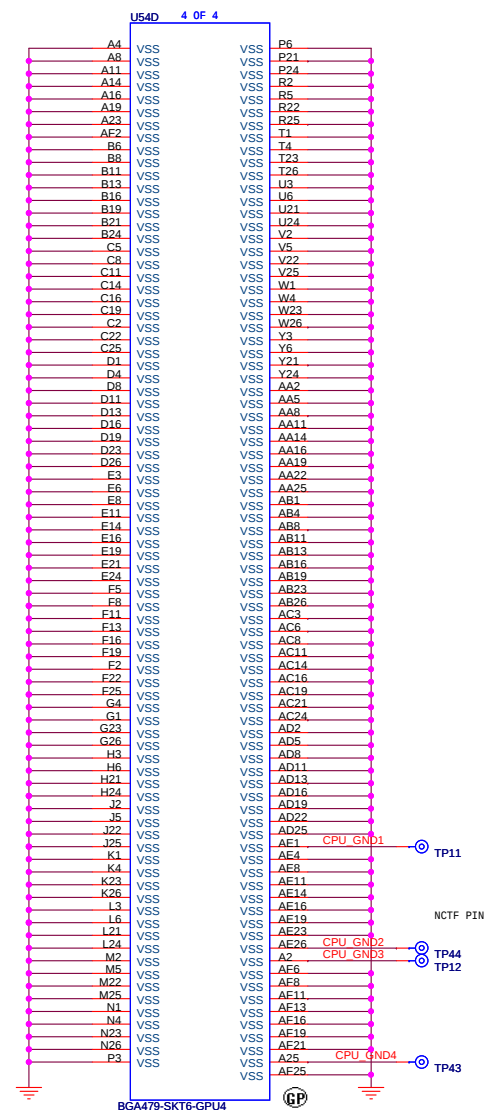
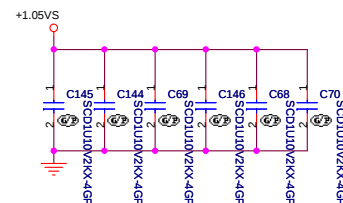
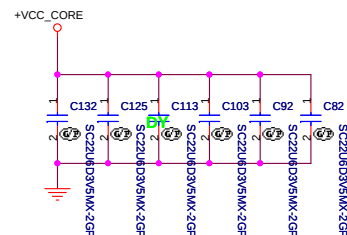
Layout Note:

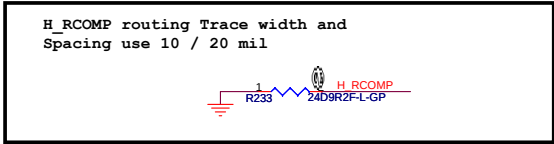
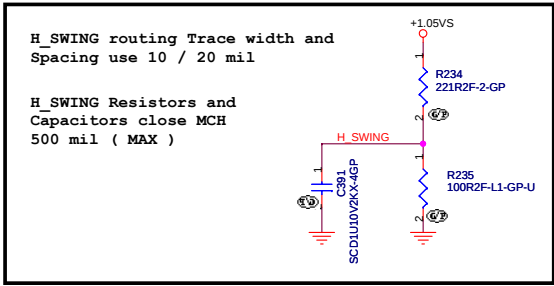
VCCSENSE and VSSSENSE lines should be of equal length.

Please these inside socket
cavity on L8(North side Secondary)

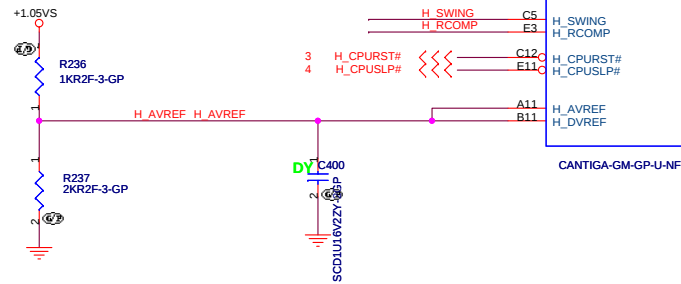


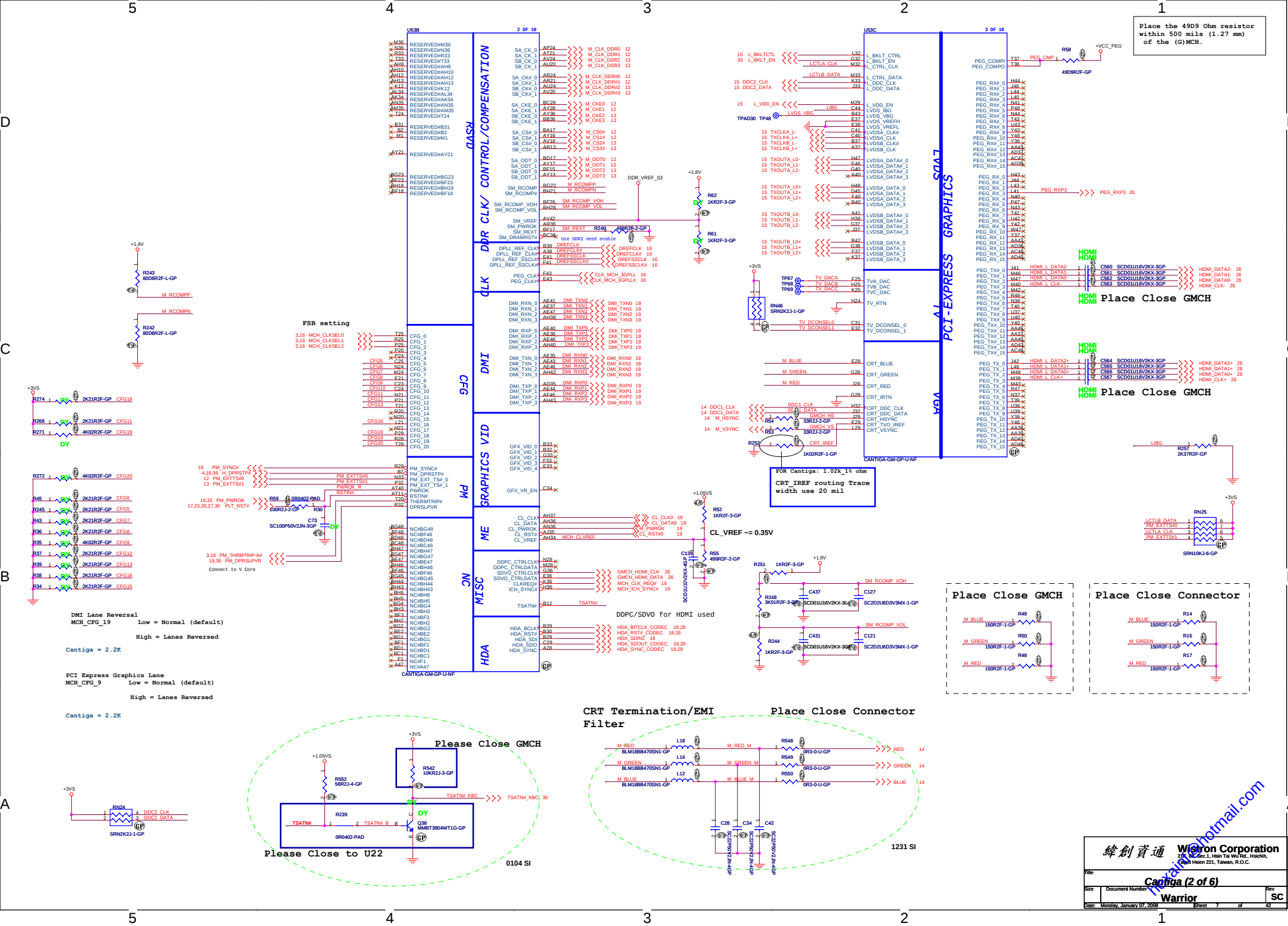
Please these inside socket
cavity on L8 (South side Primary)





Place them near to the chip (< 0.5")





Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

Place Close GMCH

Place Close GMCH

FOR Cantiga: 1.02k_14 ohm
CRT_IREF routing Trace width use 20 mil

Place Close GMCH

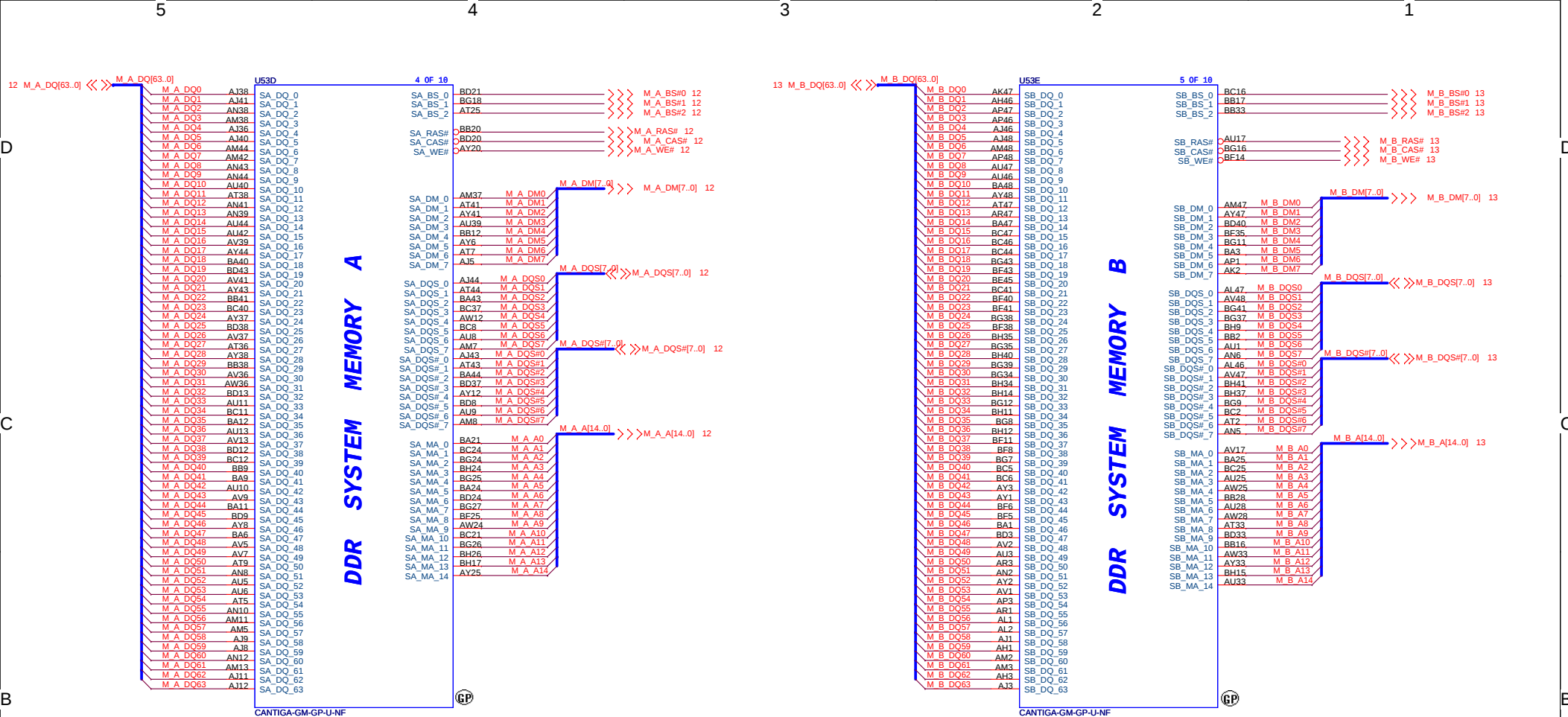
Place Close Connector

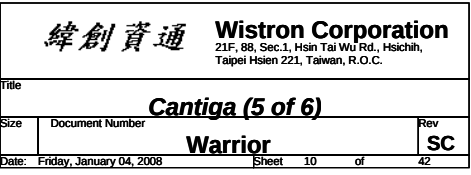
CRT Termination/EMI Filter

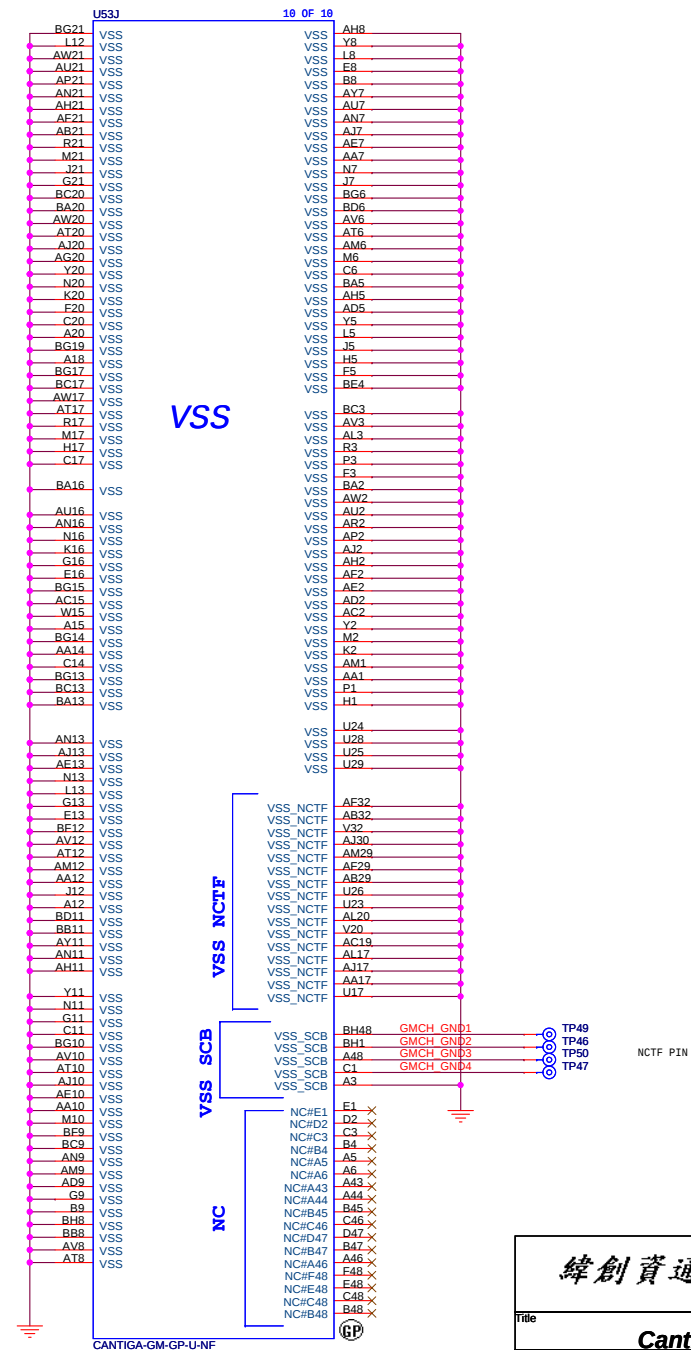
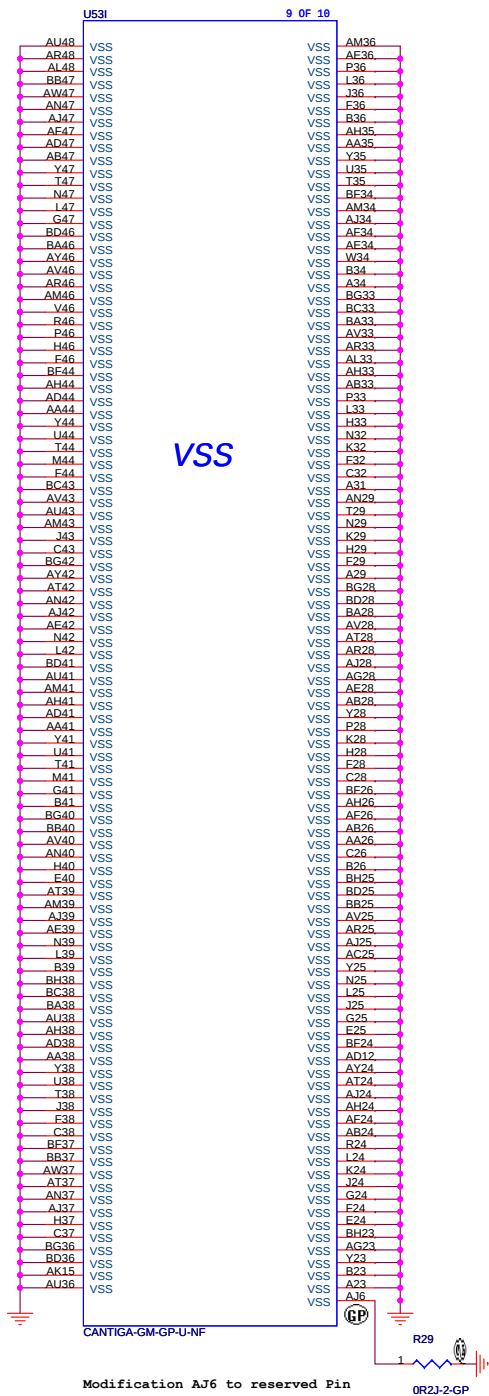
Place Close Connector

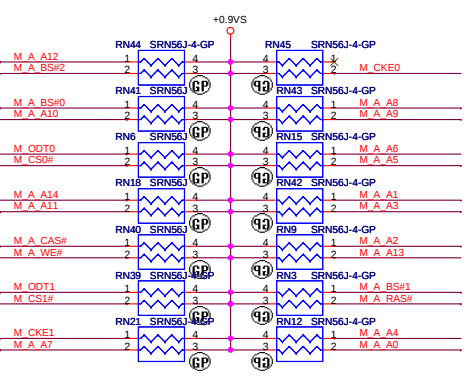
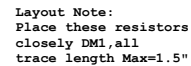
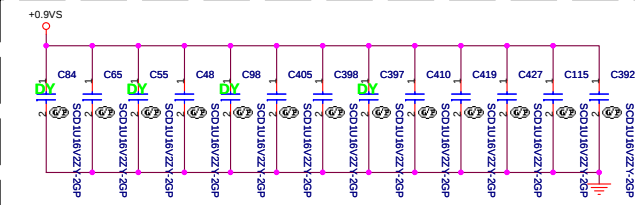
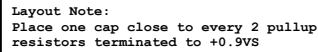
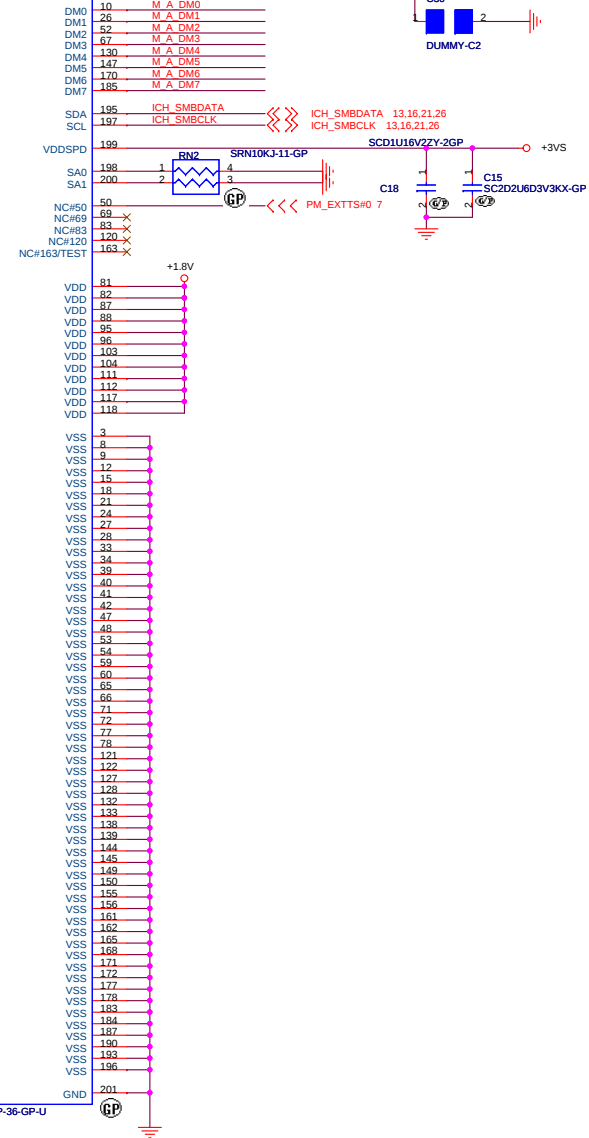
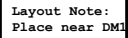
Please Close GMCH

Please Close to U22



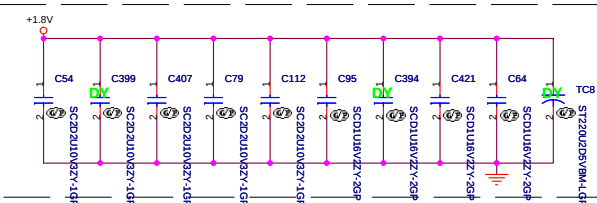




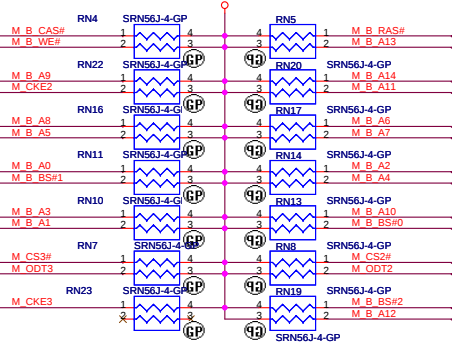
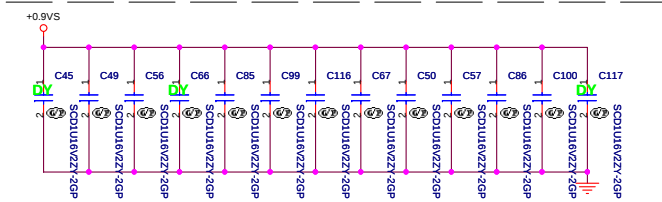


DM2 use 62.10017.E11

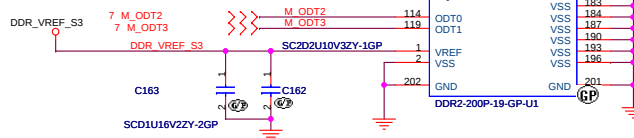
Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistors
closely DM2, all
trace length Max=1.5"

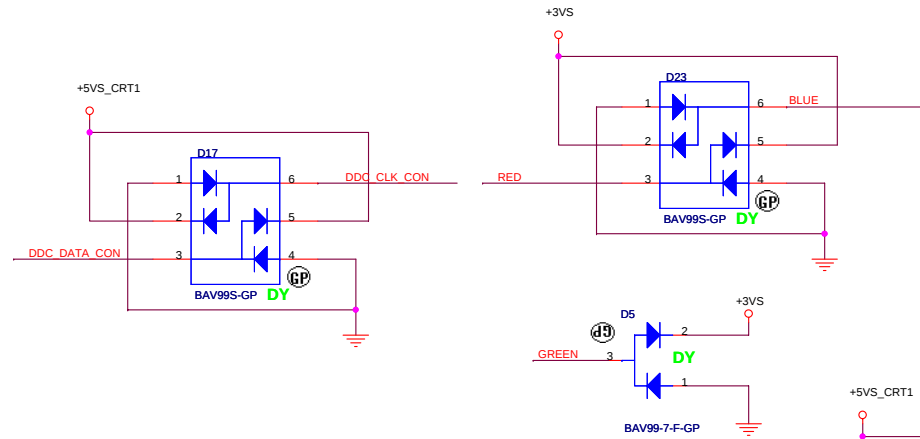


DM1 use 62.10017.B51

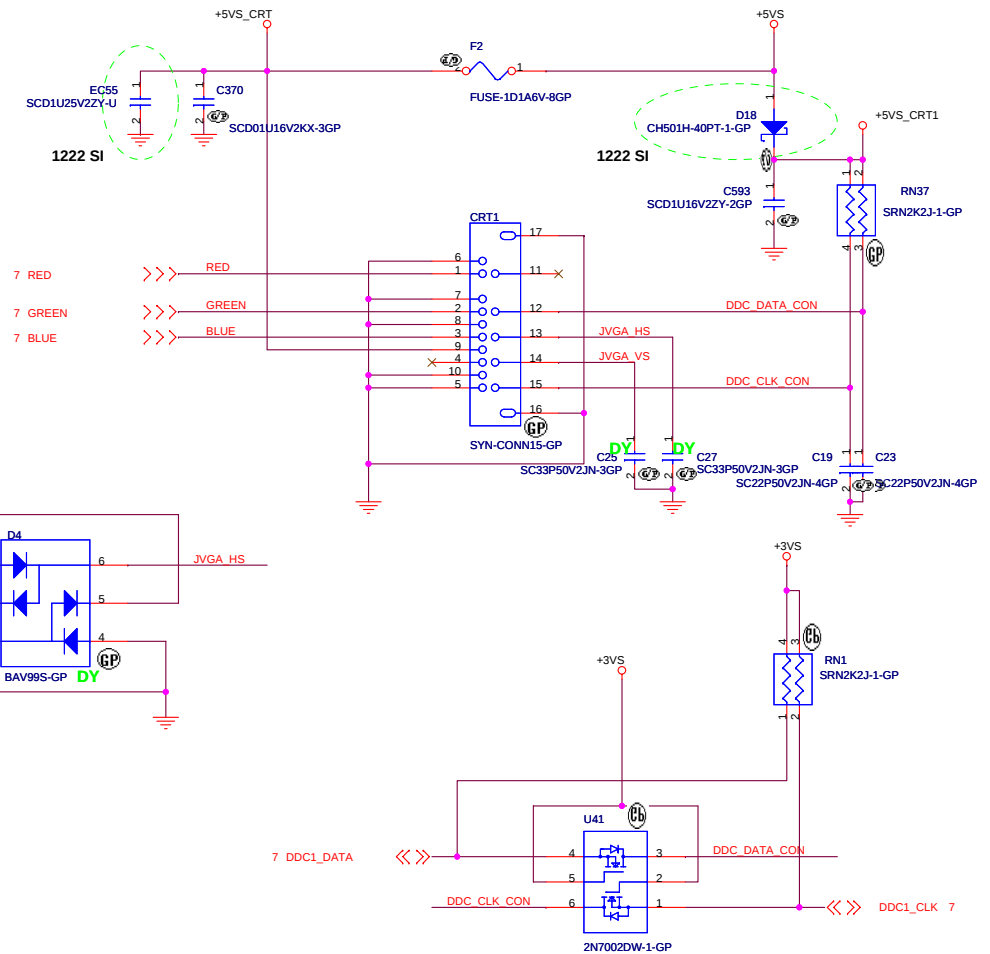
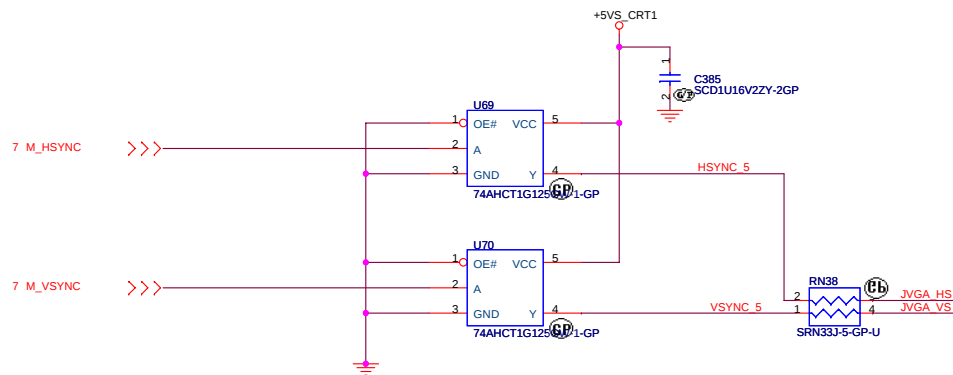
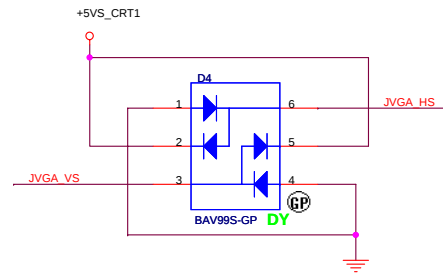
1206 SI

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CRT I/F & CONNECTOR



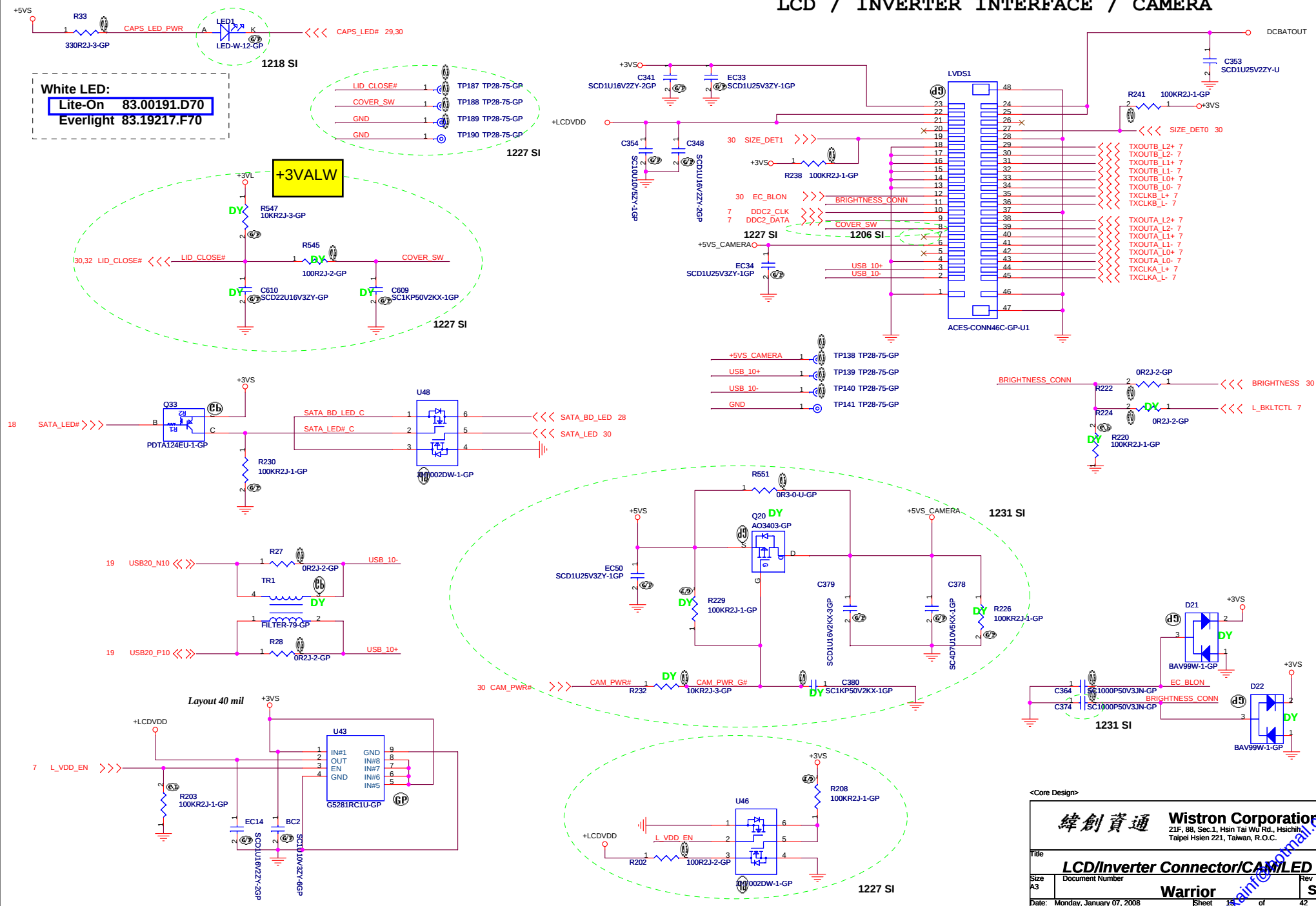
Layout Note:
 * Must be a ground return path between this ground and the ground on the VGA connector.
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

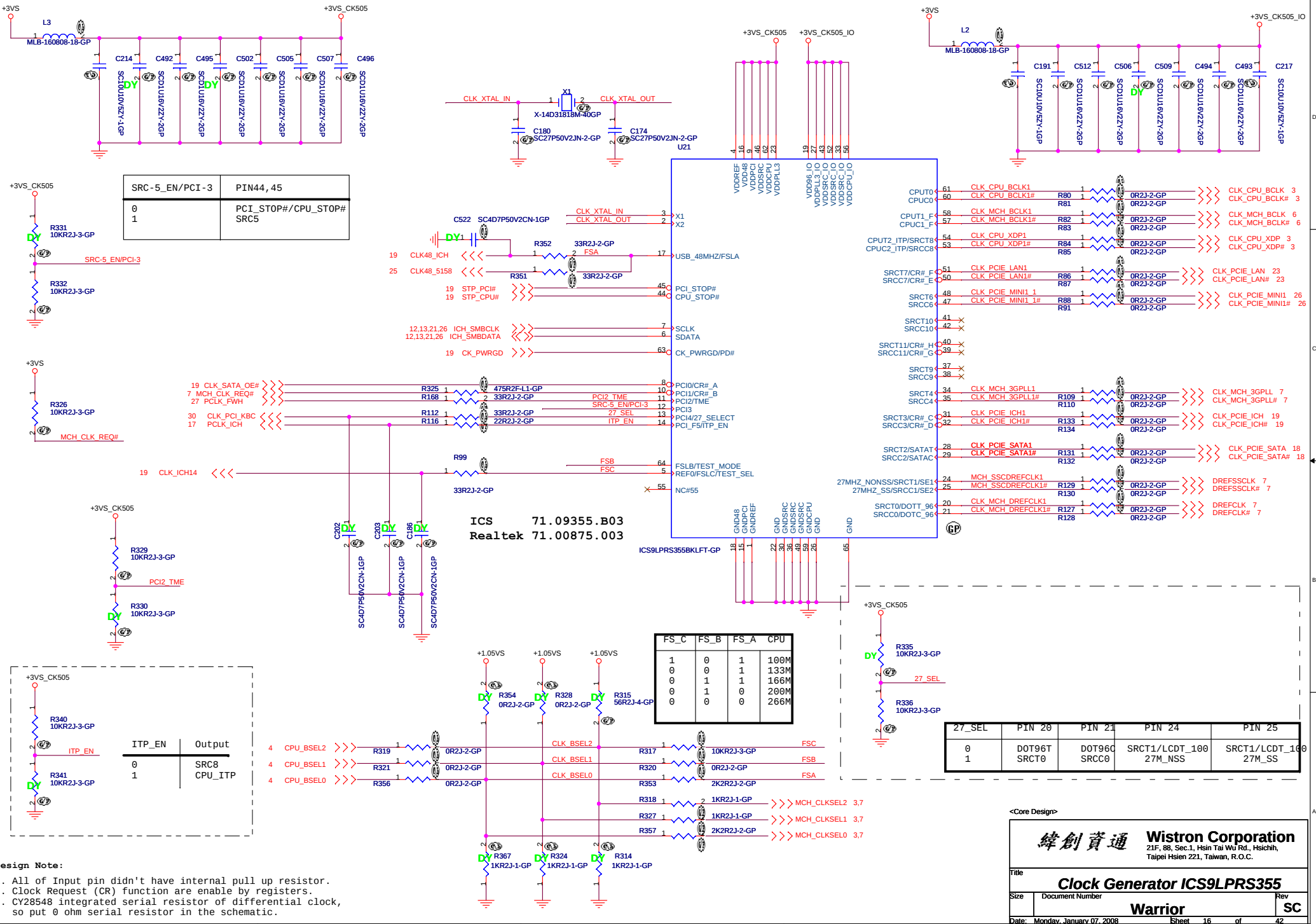


5V @ ext. CRT side

<Core Design>			
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title CRT Connector			
Size A3	Document Number	Rev	SC
Date: Monday, January 07, 2008		Sheet 14 of 42	

LCD / INVERTER INTERFACE / CAMERA





Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

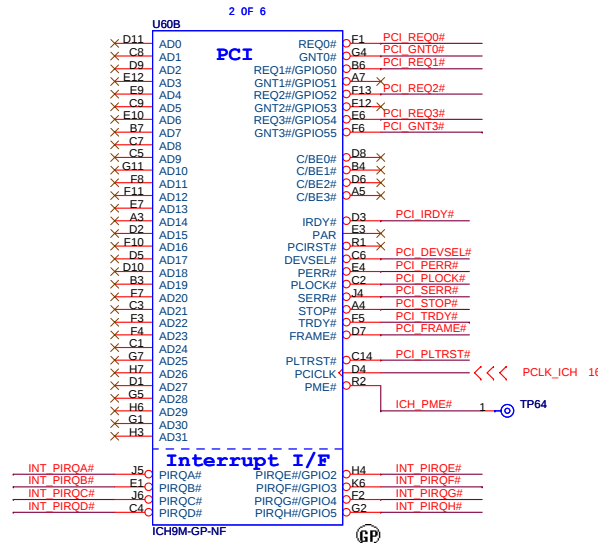
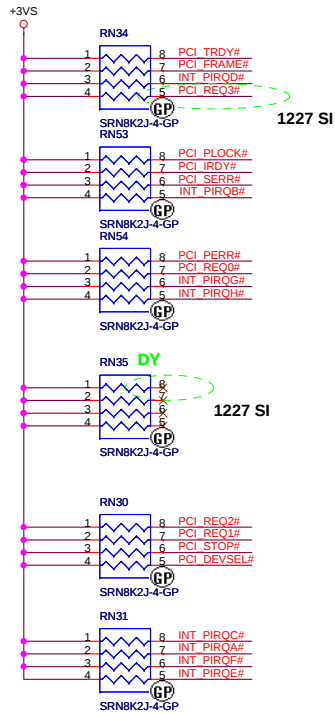
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Clock Generator ICS9LPRS355

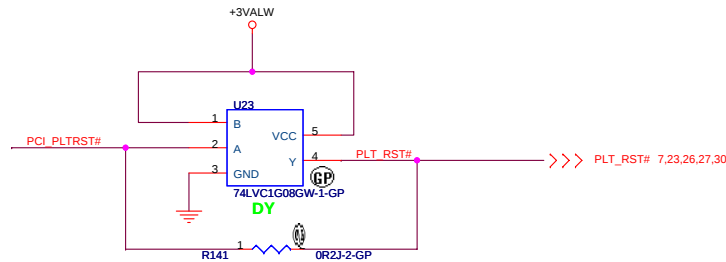
Size Document Number
Warrior

Date: Monday, January 07, 2008 Sheet 16 of 42

Rev
SC

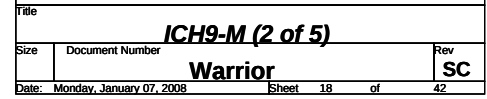


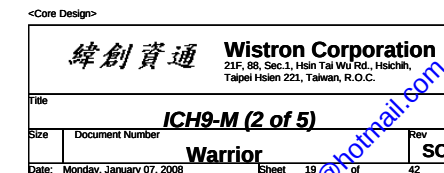
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	



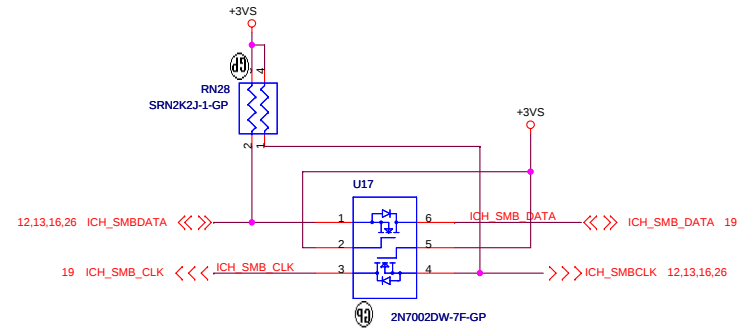
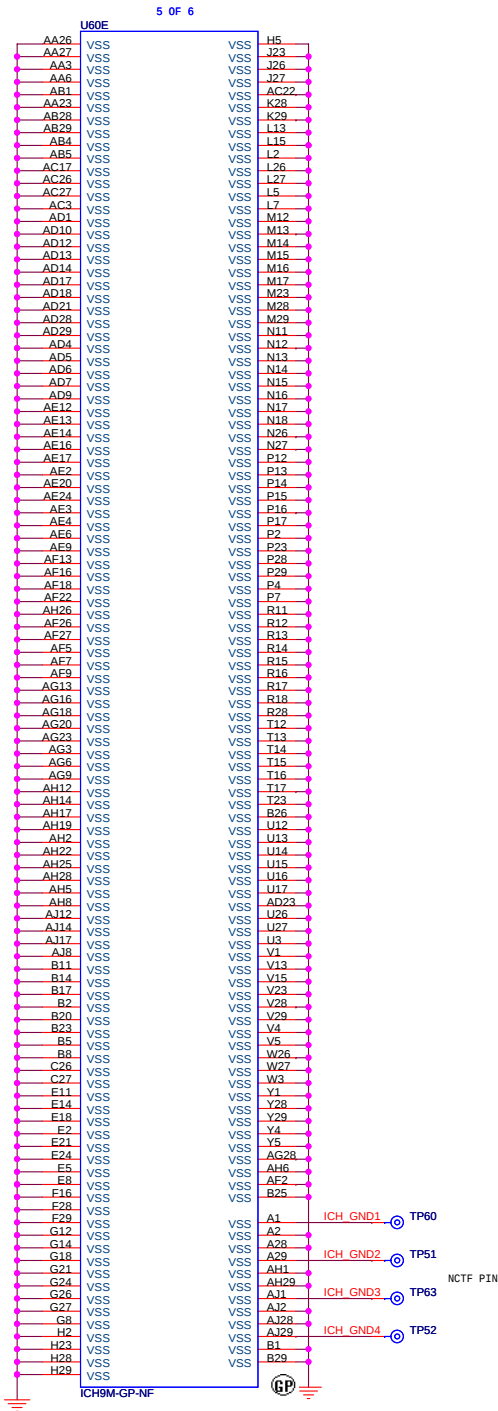
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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiao Taipei Hsien 221, Taiwan, R.O.C.	
Title: ICH9-M (1 of 5)			
Size	Document Number		Rev
Warrior		SC	
Date:	Monday, January 07, 2008	Sheet	42





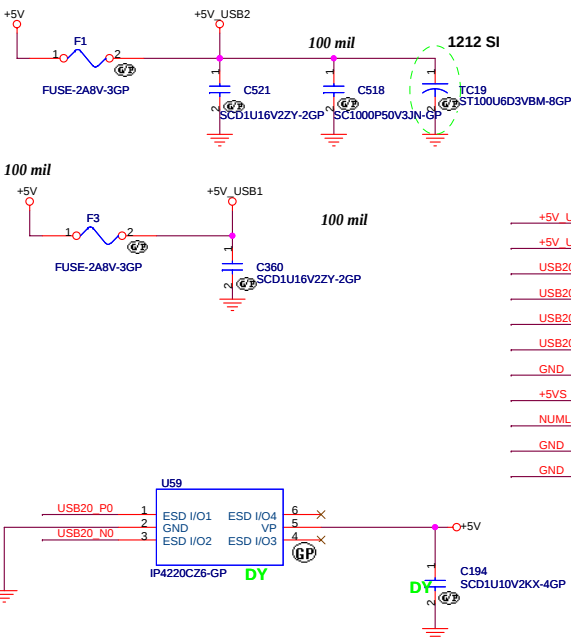




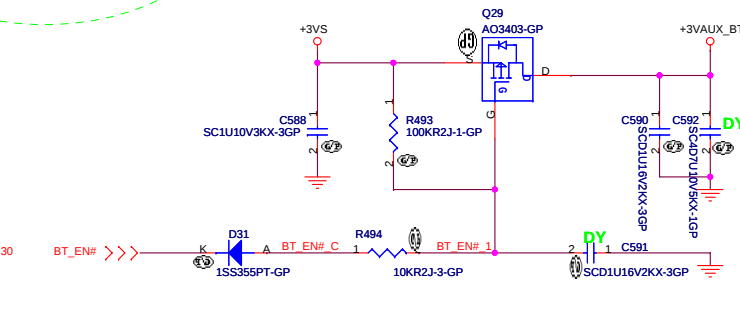
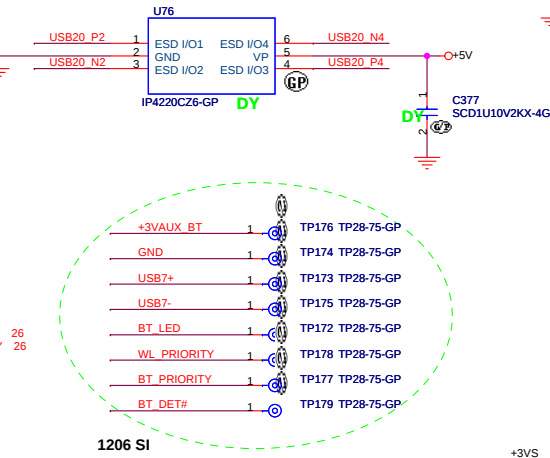
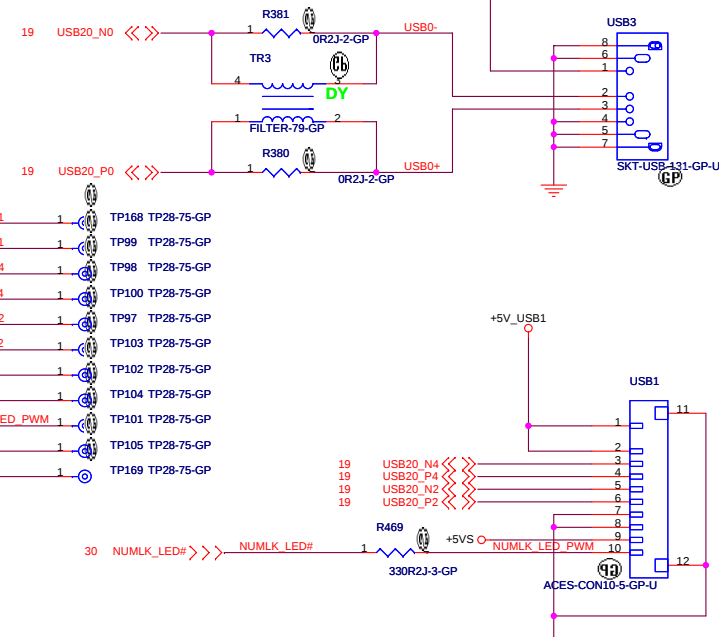
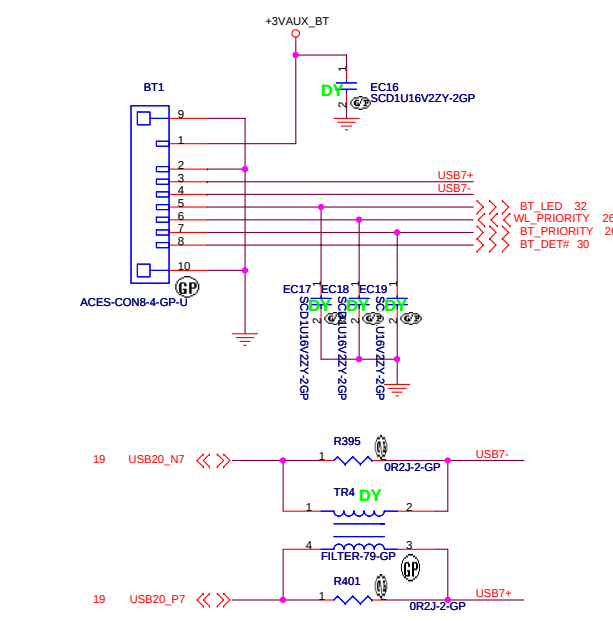
SMBUS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title ICH9-M (4 of 4)	
Size	Document Number Warrior
Date: Monday, January 07, 2008	Rev SC Sheet 21 of 42

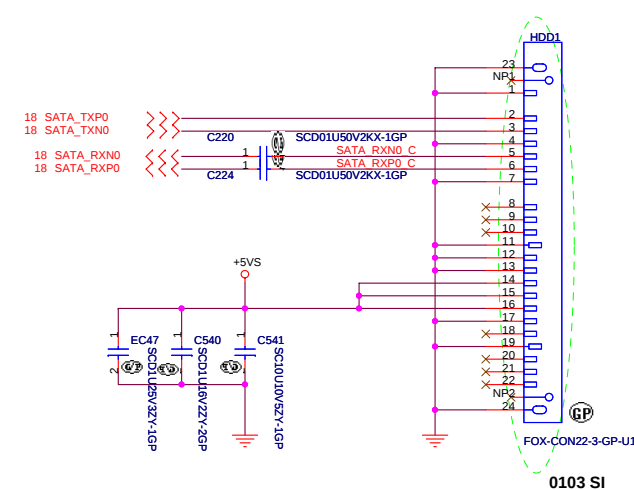
USB PORT



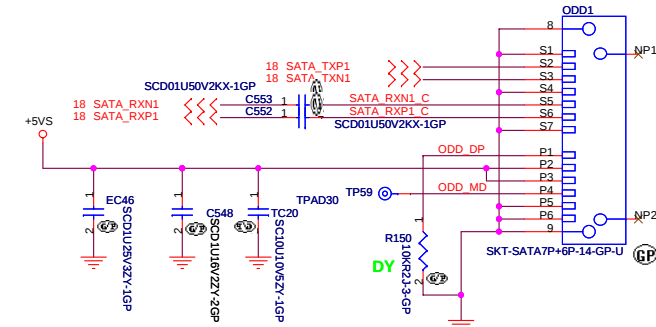
BLUETOOTH



SATA HD Connector



ODD Connector



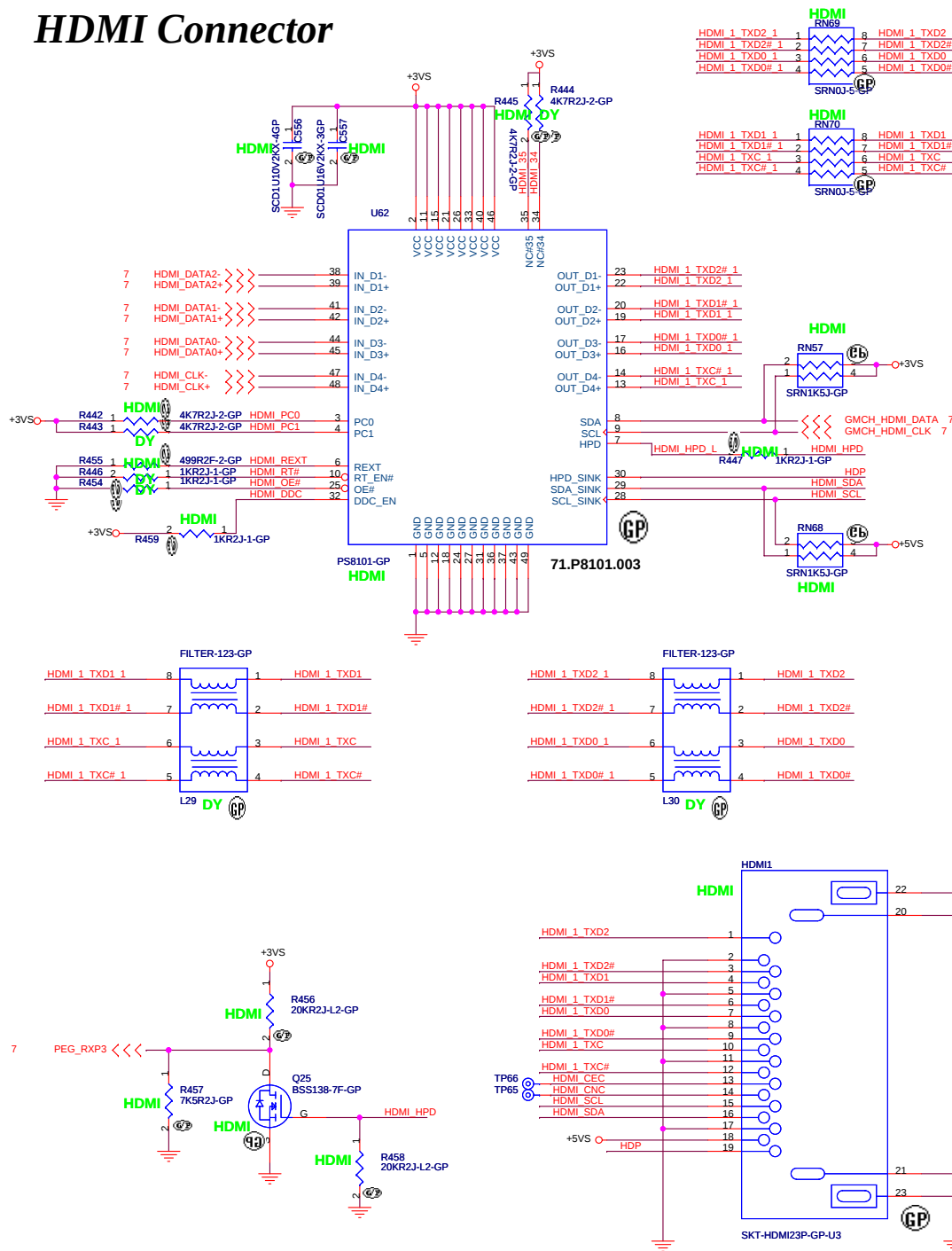
MAX 150mA

<Core Design>

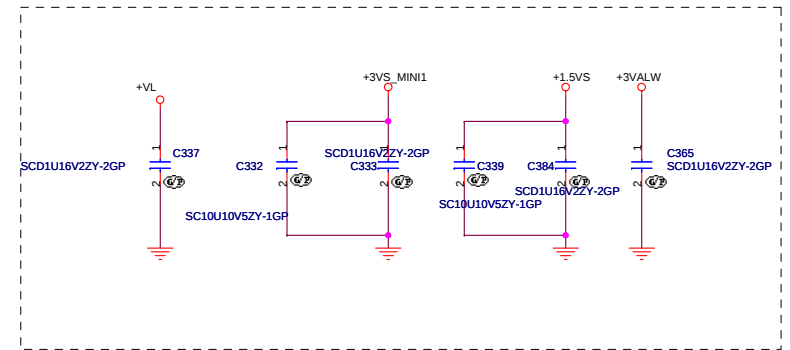
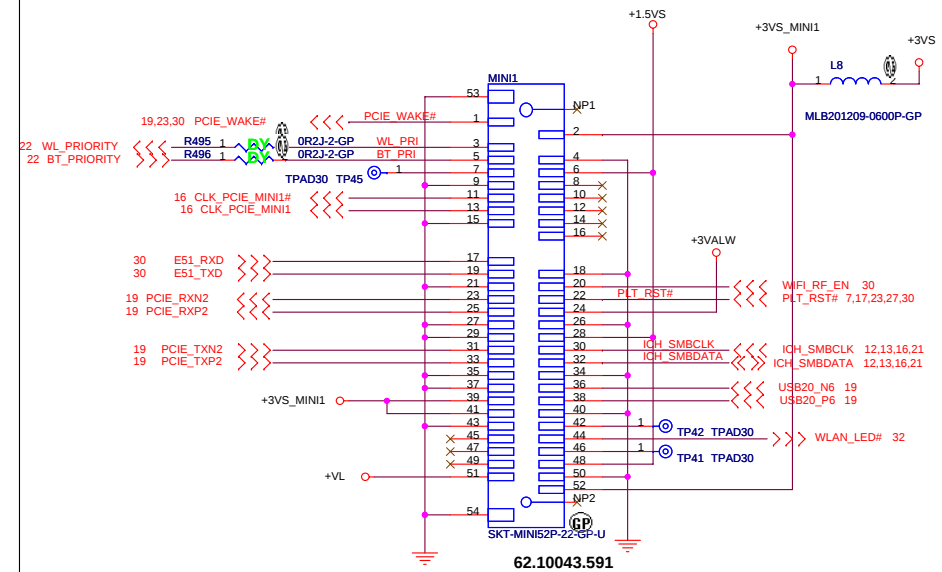
緯創資通 Wistron Corporation		
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Title		
HDD/CDROM/USB/BT		
Size	Document Number	Rev
A3	Warrior	SC
Date	Monday, January 07, 2008	Sheet 22 of 42

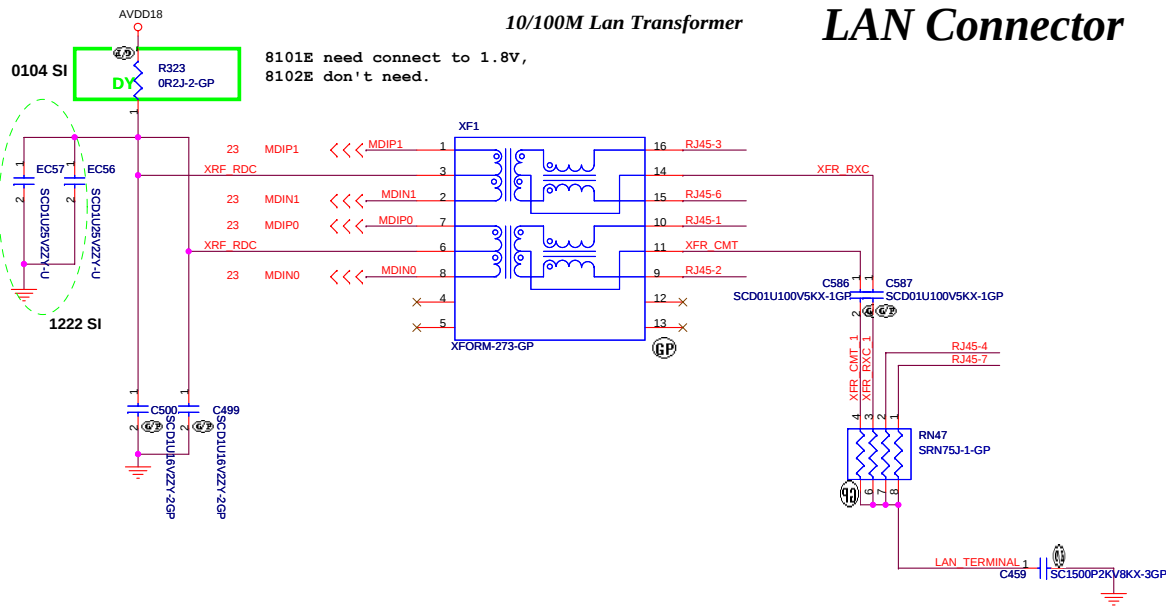


HDMI Connector



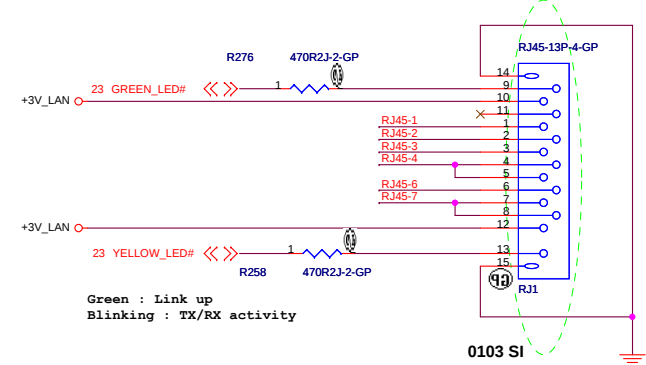
Mini Card Connector1(802.11a/b/g)





- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



Remark:

Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.

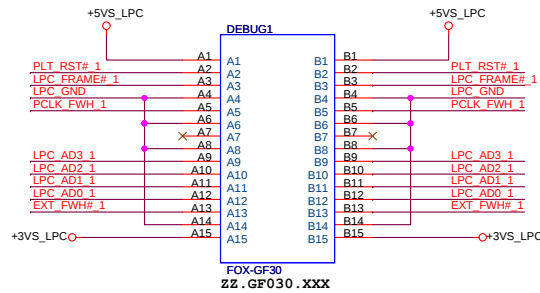
Golden Finger for Debug Board

TOP VIEW (A)

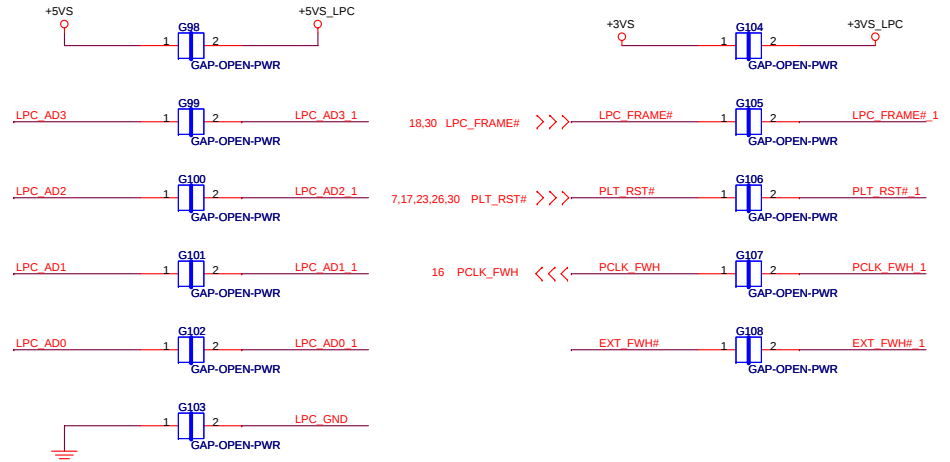
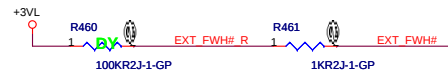
A15 (B1)
A14 (B2)
:
:
:
A2 (B14)
A1 (B15)

BOTTOM VIEW (B)

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPE17 Elec. P3-46



Please put near board edge.

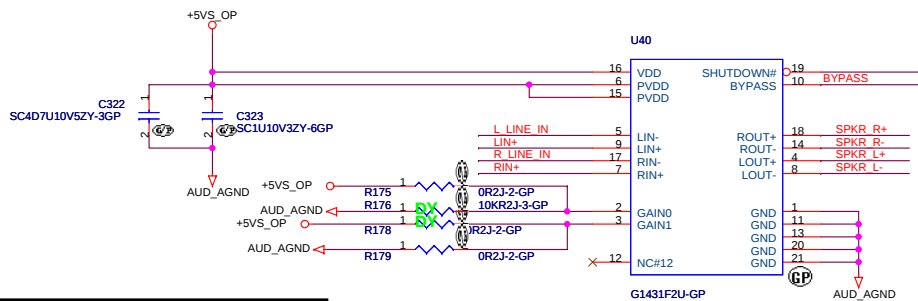


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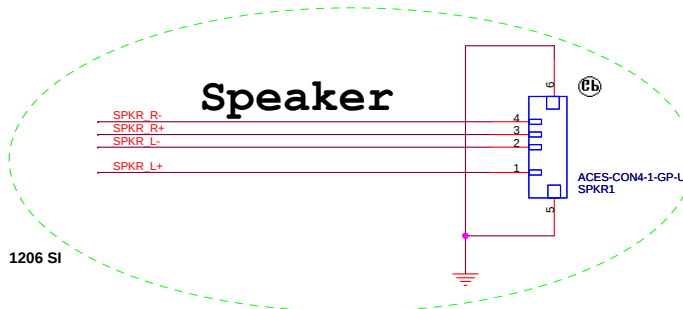
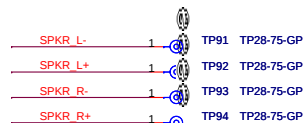
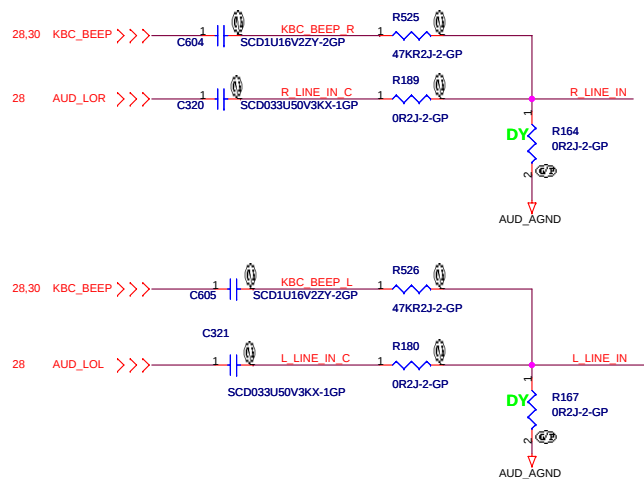
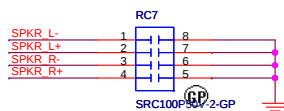
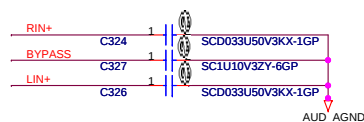
緯創資通

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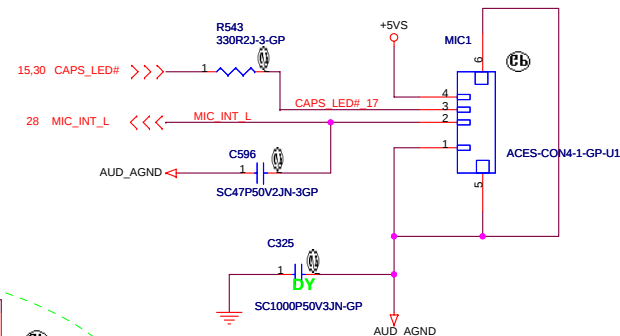
Title	LAN CONN/Debug		
Size	Document Number	Rev	SC
A3			
Date:	Monday, January 07, 2008	Sheet	27 of 42



GAIN0	GAIN1	Av (dB)
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0	1	10
1	0	15.6
1	1	21.6



MIC



<Core Design>

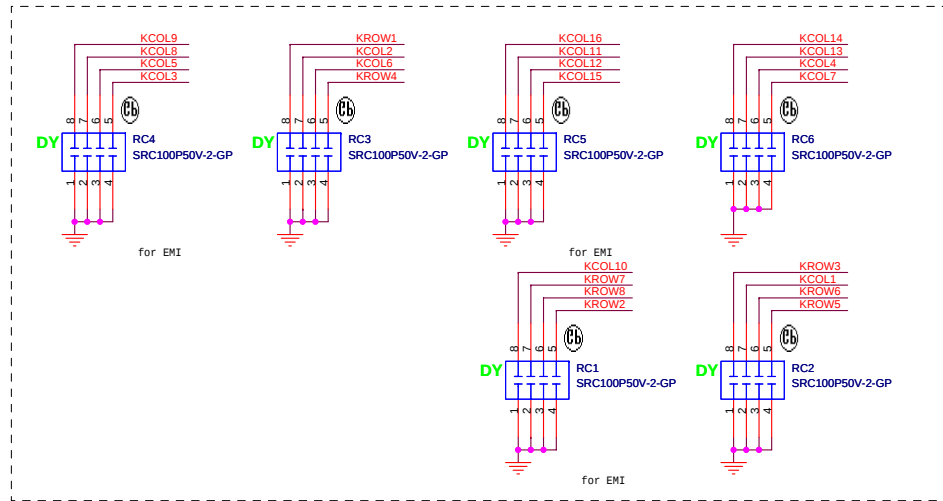
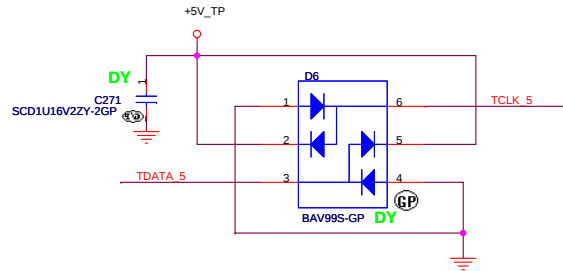
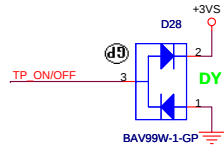
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Keelung, Taipei Hsien 221, Taiwan, R.O.C.	
AUDIO AMP/SPEAKER	
Title Size A3 Date: Monday, January 07, 2008	Document Number Rev SC

Internal KeyBoard Connector

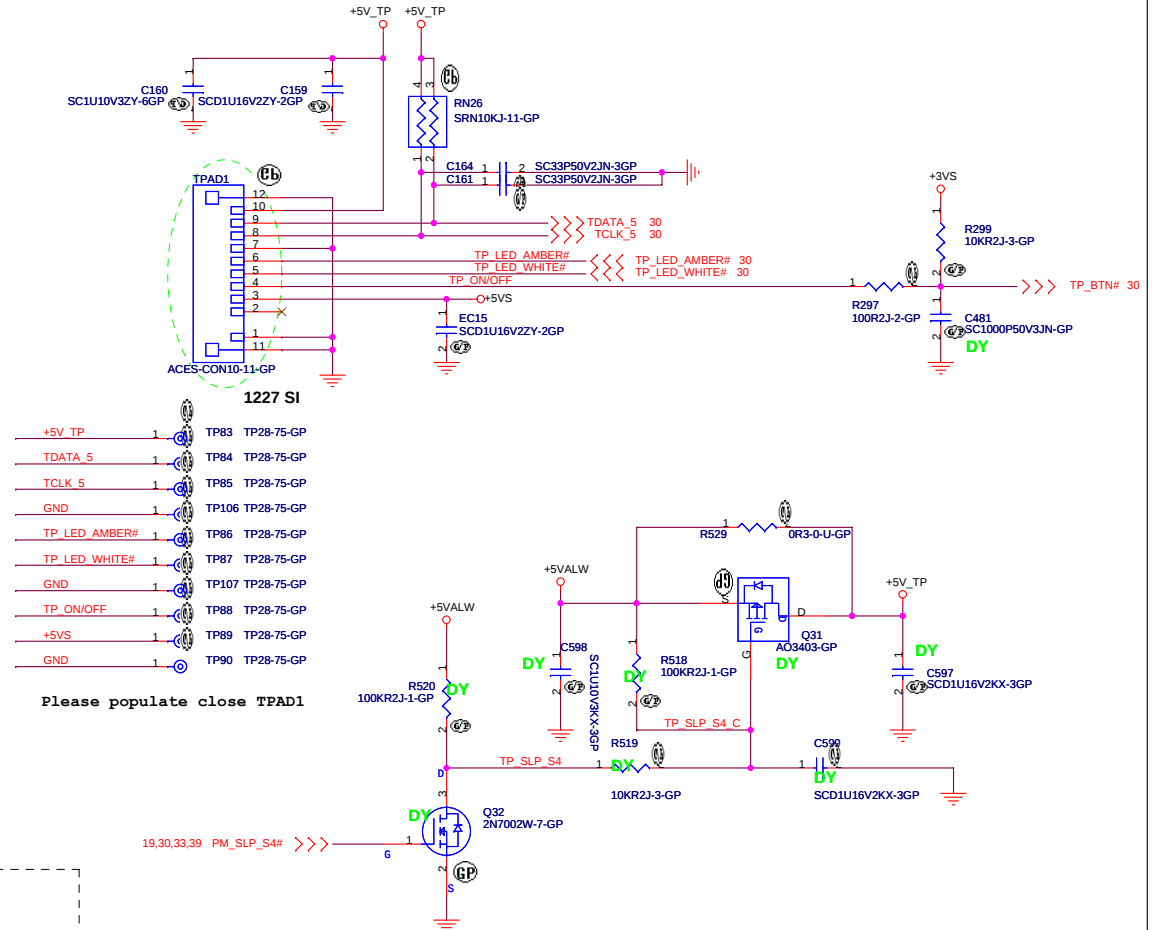
30 KROW[1..8] <<< <<<
30 KCOL[1..18] <<< <<<

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



TouchPad Connector

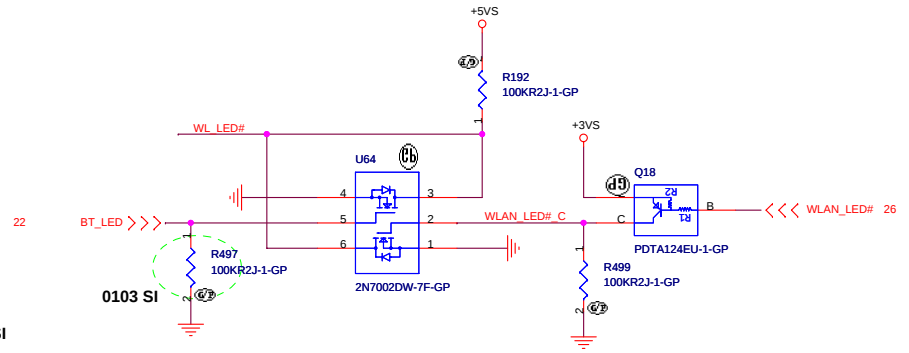
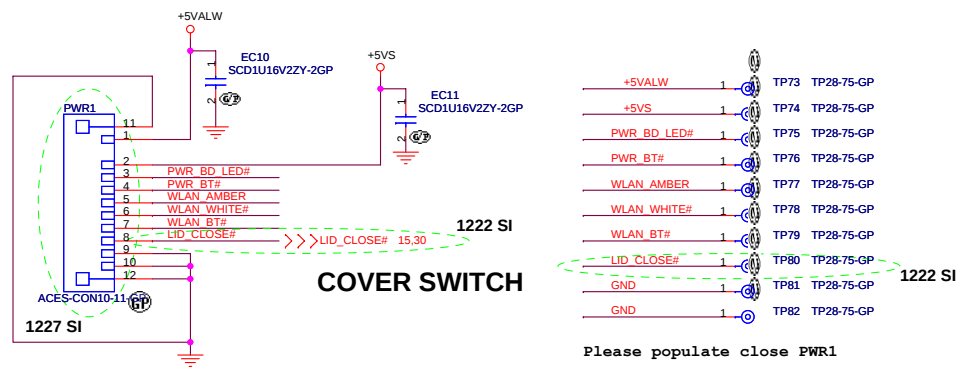
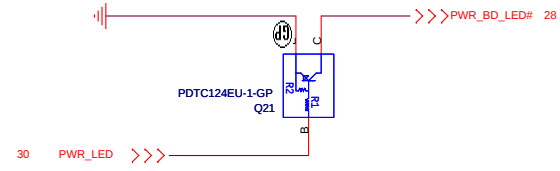
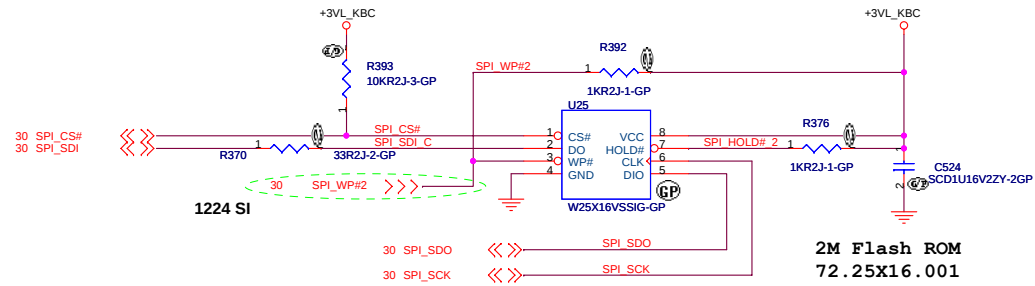


Please populate close TPAD1

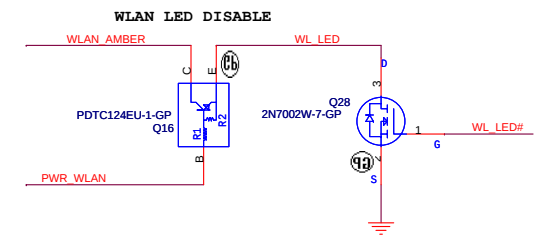
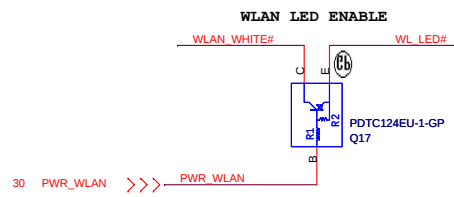
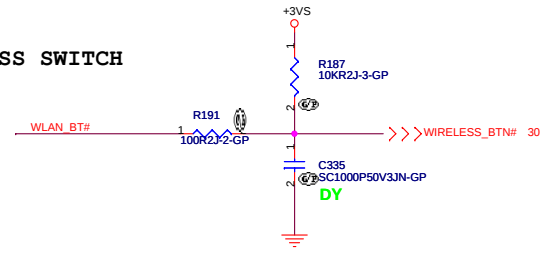
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Taipei Hsien 221, Taiwan, R.O.C.

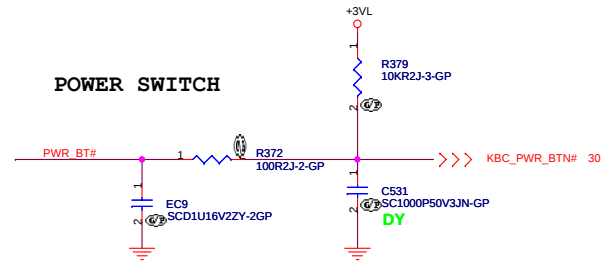
Title	KeyBoard-CONN		
Size A3	Document Number	Warrior	Rev SC
Date: Monday, January 07, 2008	Sheet	of	42



WIRELESS SWITCH



POWER SWITCH



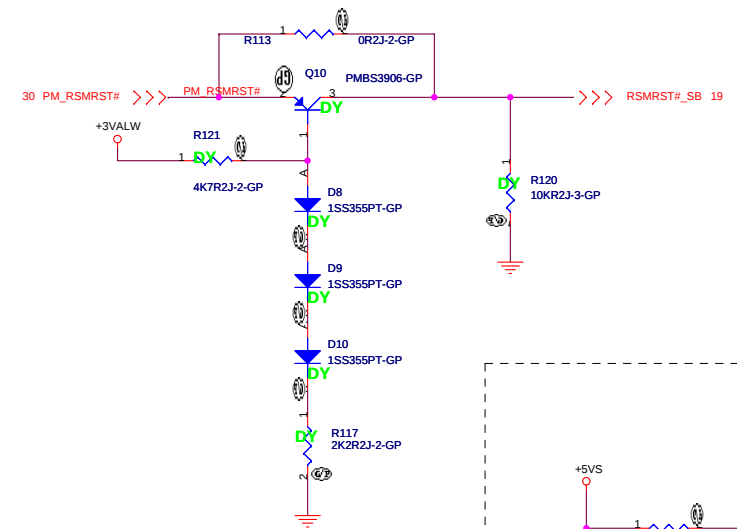
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **FWH and CONN.**

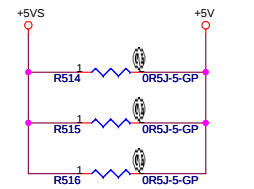
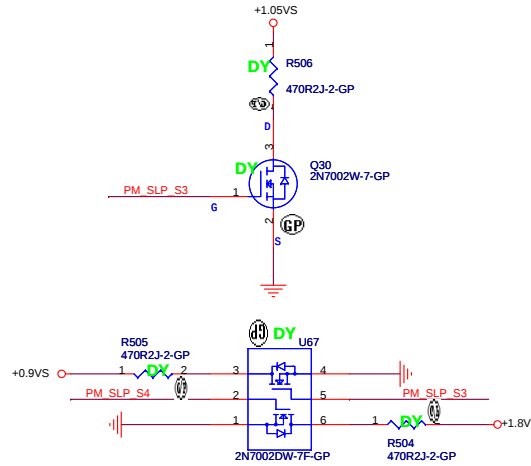
Size A3 Document Number: **Warrior** Rev: **SC**

Date: Monday, January 07, 2008 Sheet 32 of 42



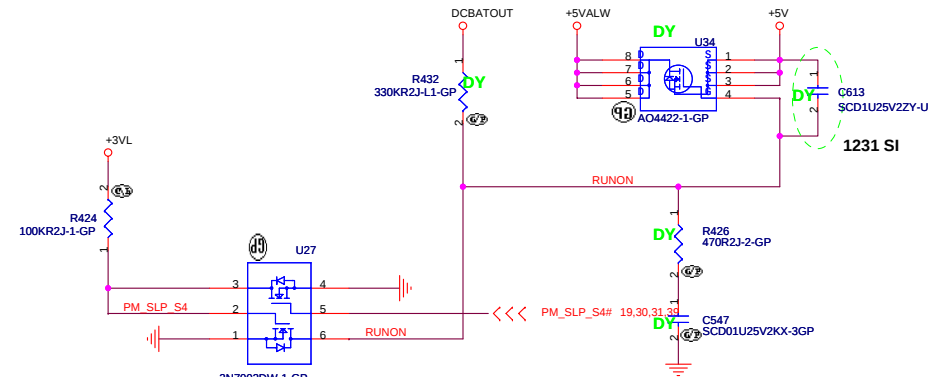
The top diagram shows a circuit for a PM SLP signal connected to +3VS. A 470R2J-2-GP resistor (R501) is connected between the +1.5VS supply and the gate of a 2N7002DW-7F-GP MOSFET (U65). The MOSFET's source is connected to ground, and its drain is connected to the PM SLP_S3 signal line. A 470R2J-2-GP resistor (R500) is connected between the PM SLP_S3 signal line and the +3VS supply. The MOSFET is labeled with a blue 'DY' and a blue 'd39'.

The bottom diagram shows a similar circuit for a PM SLP signal connected to +5V. A 470R2J-2-GP resistor (R503) is connected between the +5VS supply and the gate of a 2N7002DW-7F-GP MOSFET (U66). The MOSFET's source is connected to ground, and its drain is connected to the PM SLP_S4 signal line. A 470R2J-2-GP resistor (R502) is connected between the PM SLP_S4 signal line and the +5V supply. The MOSFET is labeled with a blue 'DY' and a blue 'd39'.



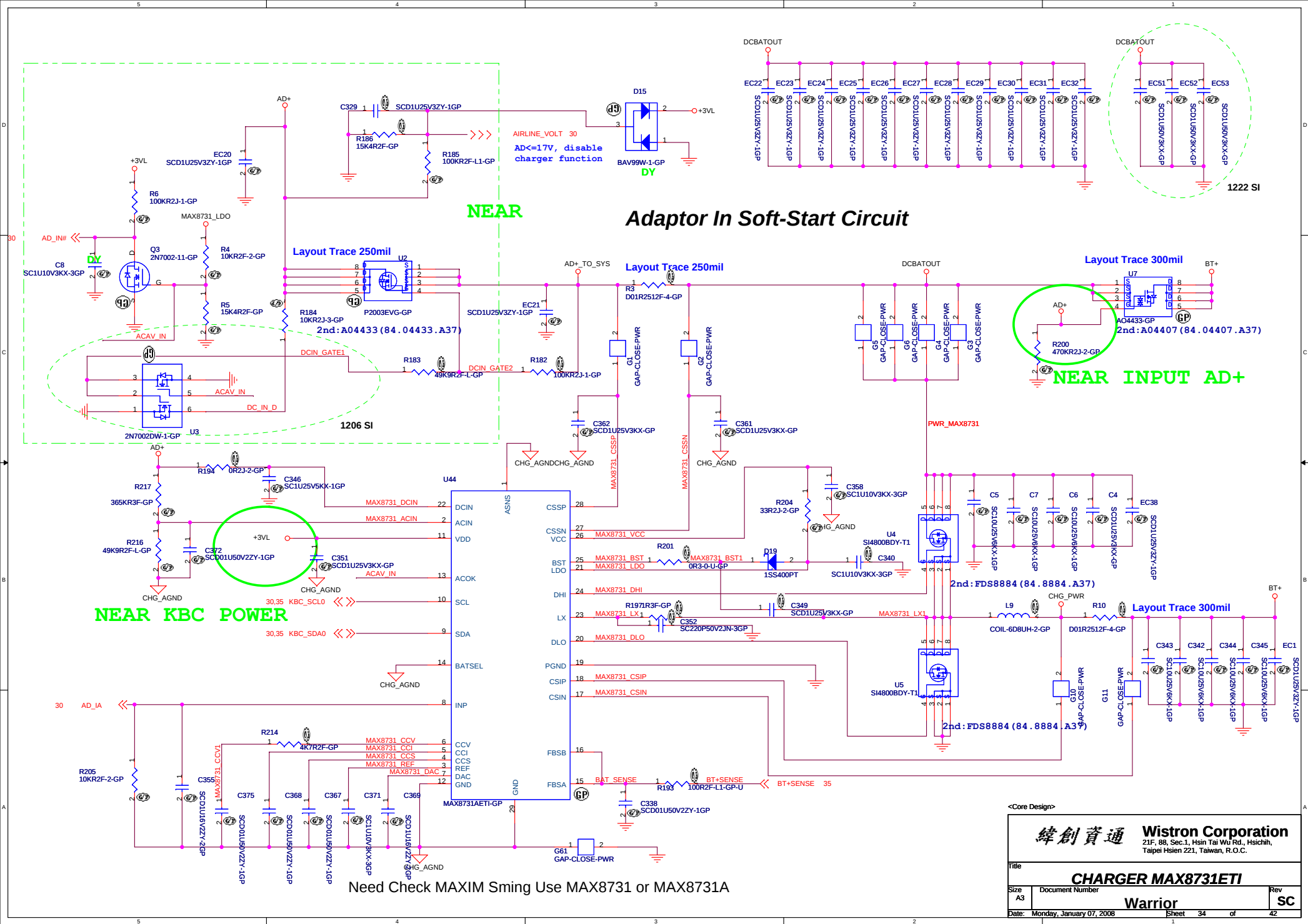
Populate close U34

+5VALW to +5V Transfer

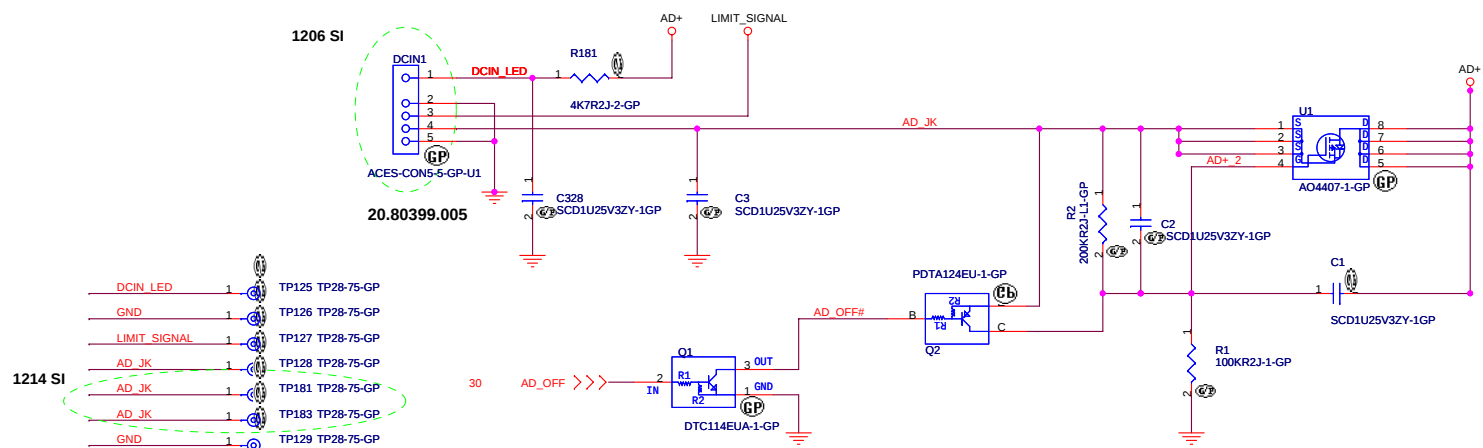
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Taipei Hsien 221, Taiwan, R.O.C.

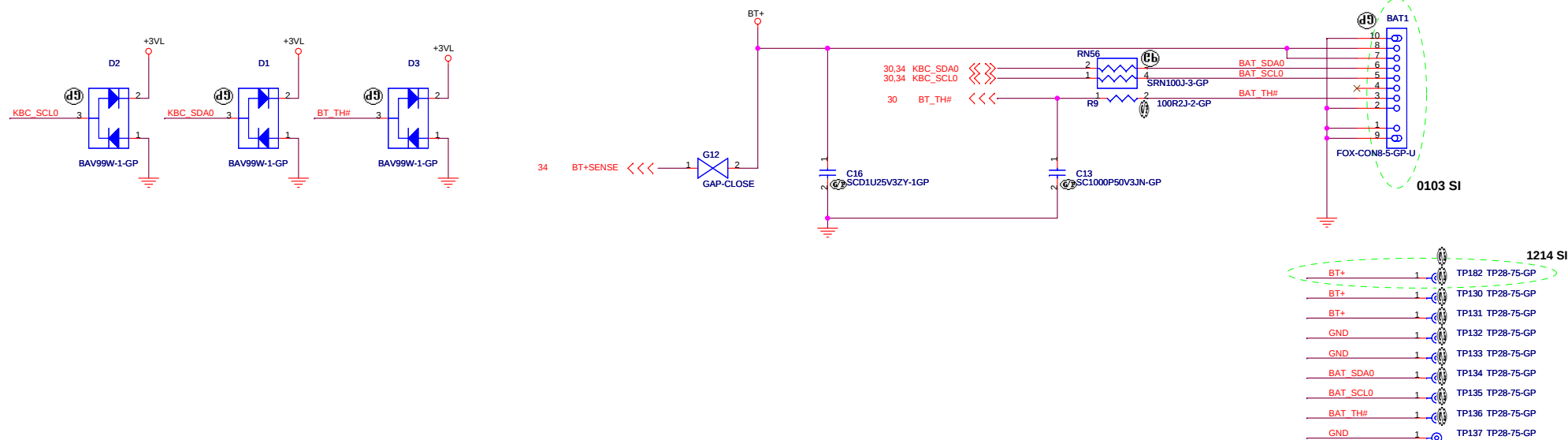
Title			
PWRPLANE Warrior			
Size A3	Document Number		Rev SC
Date: Monday, January 07, 2008		Sheet 33 of	42



Adaptor in to generate DCBATOUT



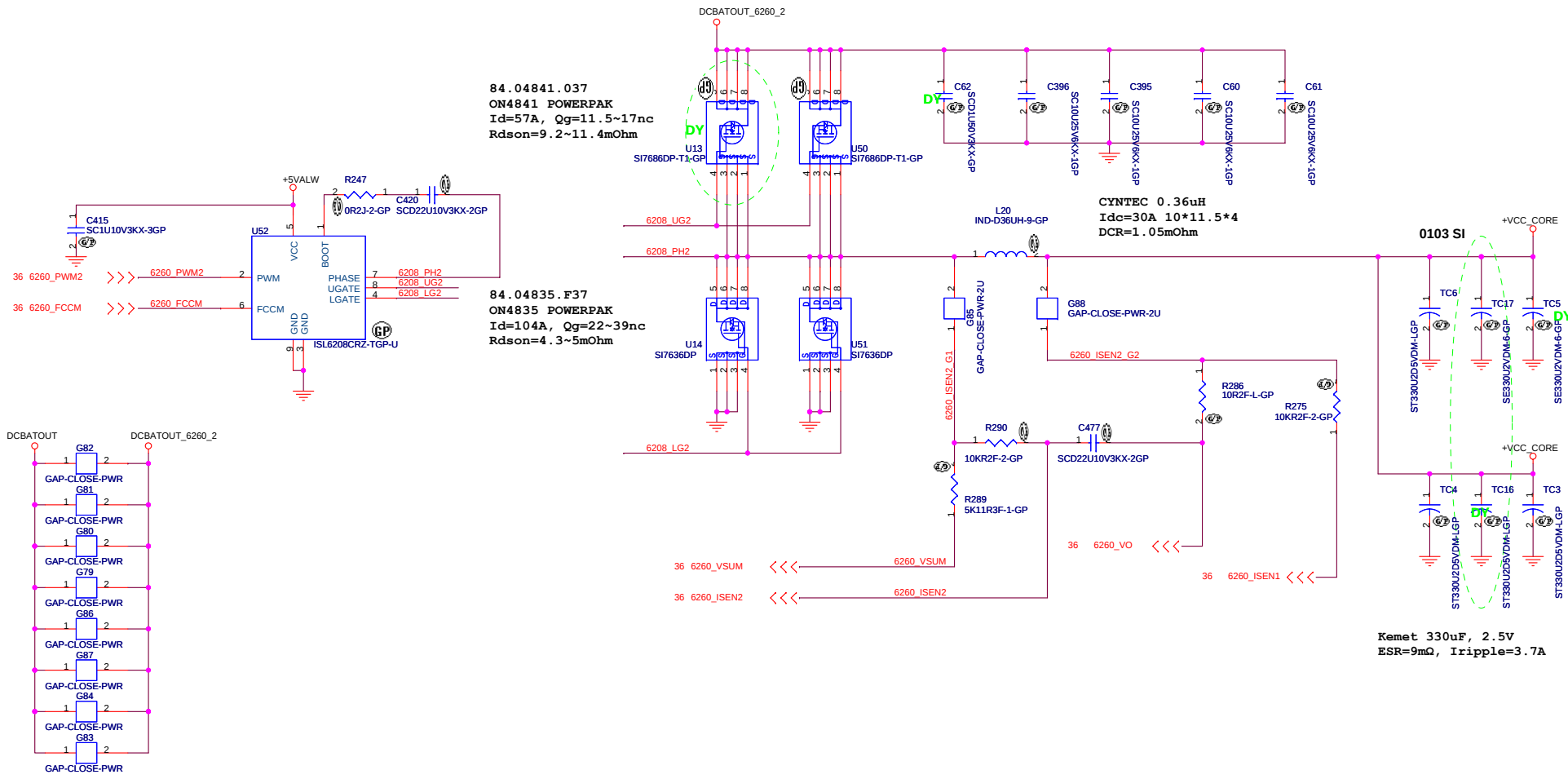
BATTERY CONNECTOR



<Core Design>

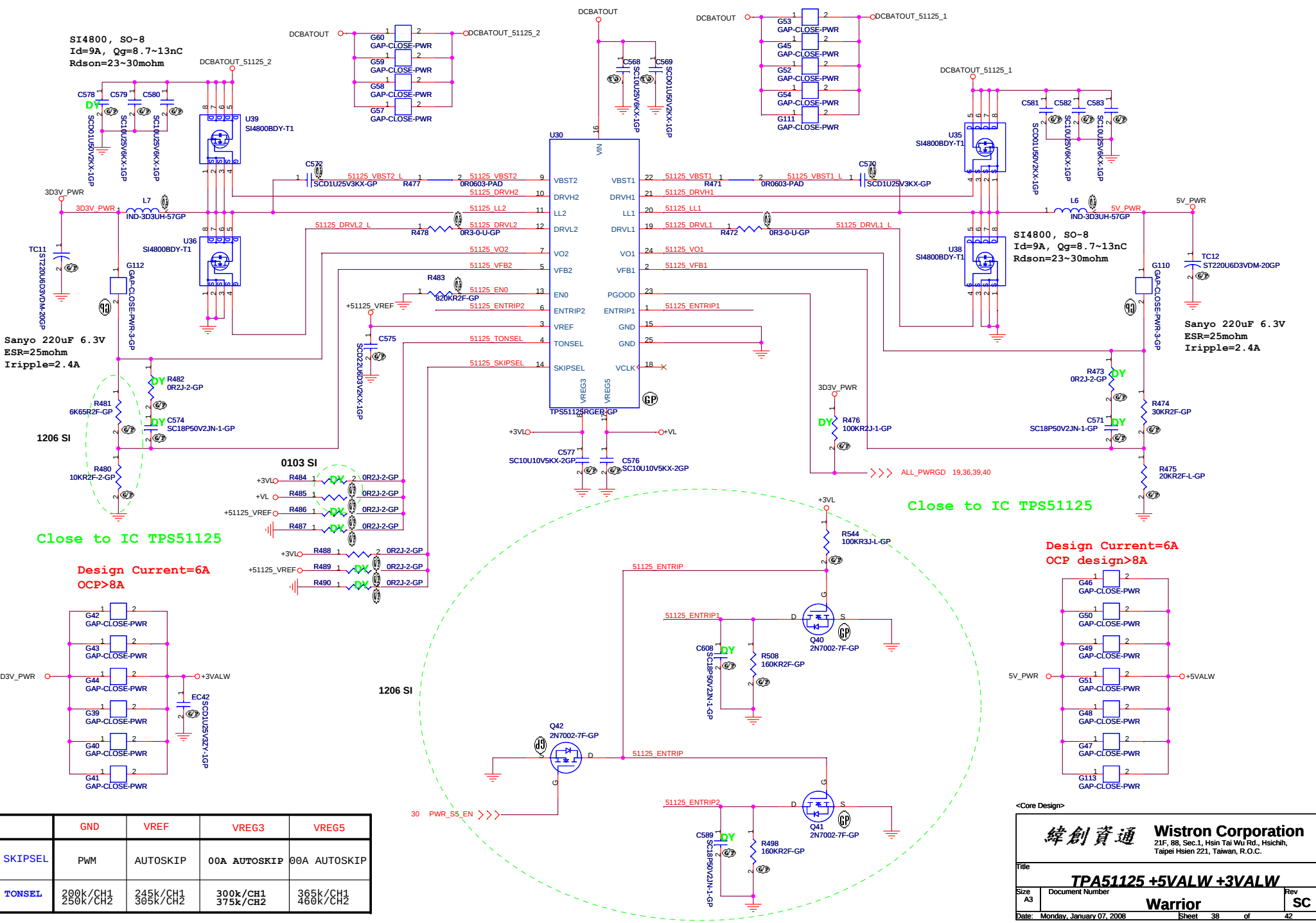
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Title			AD/BATT CONN		
Size	Document Number				Rev
A3	Warrior				SD



Kemet 330uF, 2.5V
ESR=9mΩ, Iripple=3.7A

SI4800, SO-8
Id=9A, Qg=8.7~13nC
Rdson=23~30mohm



Close to IC TPS51125

Design Current=6A
OCP>8A

Close to IC TPS51125

Design Current=6A
OCP design>8A

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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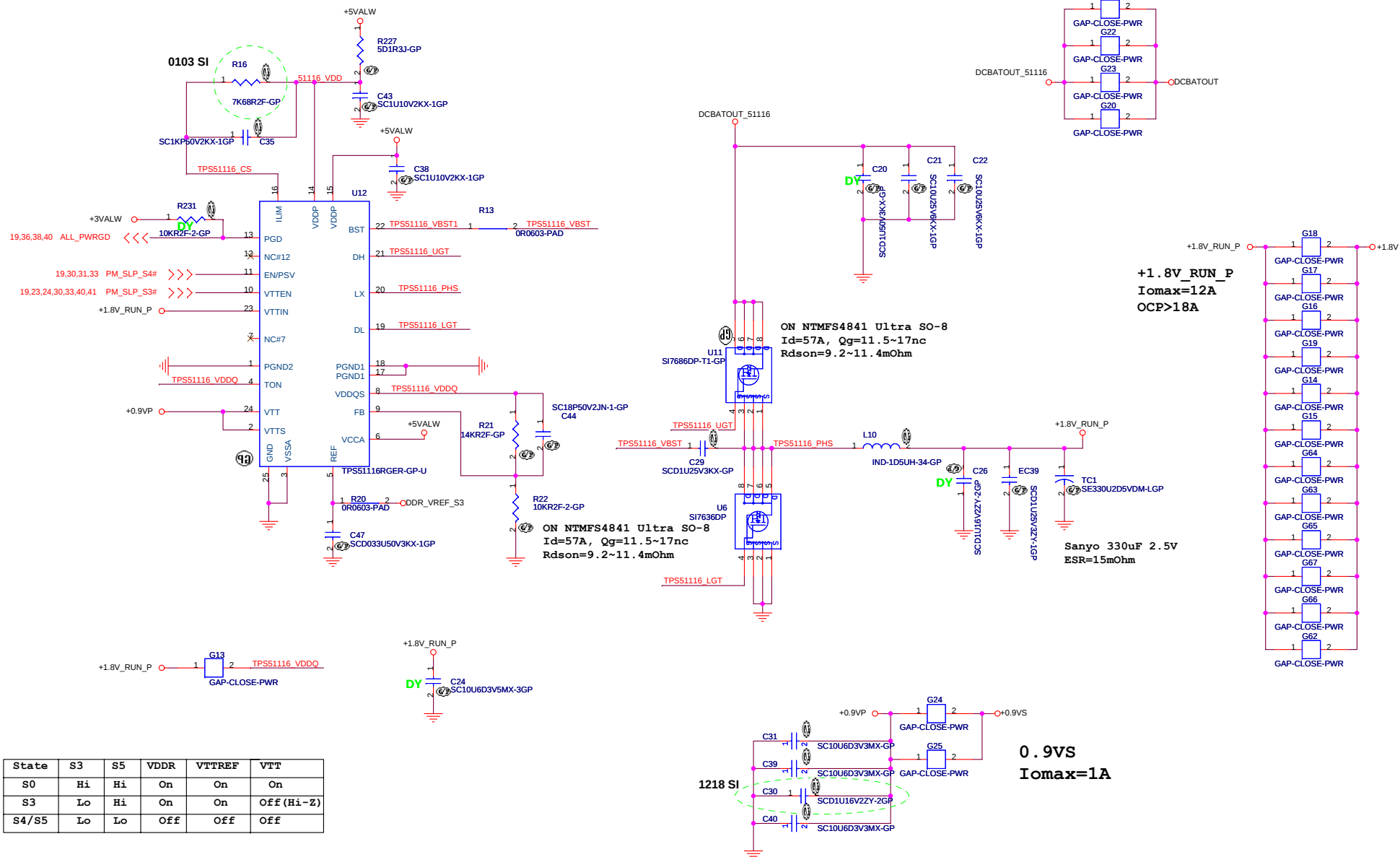
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

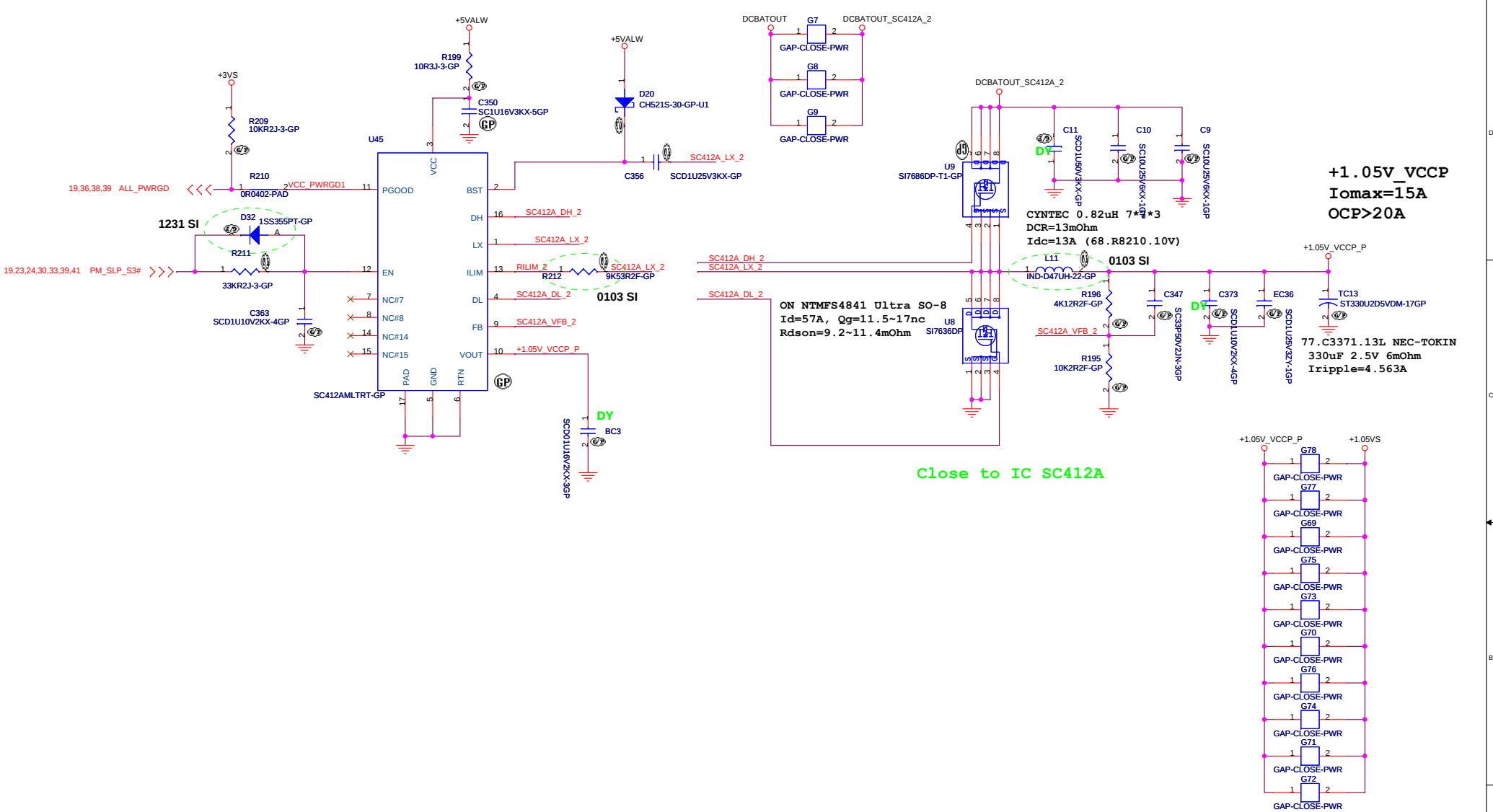
Title: **TPA51125 +5VALW +3VALW**

Size A3 Document Number **Warrior** Rev **SC**

Date: Monday, January 07, 2008 Sheet 38 of 42

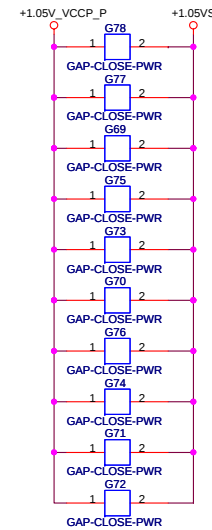
TI TPS51116 for 1D8V and 0D9V





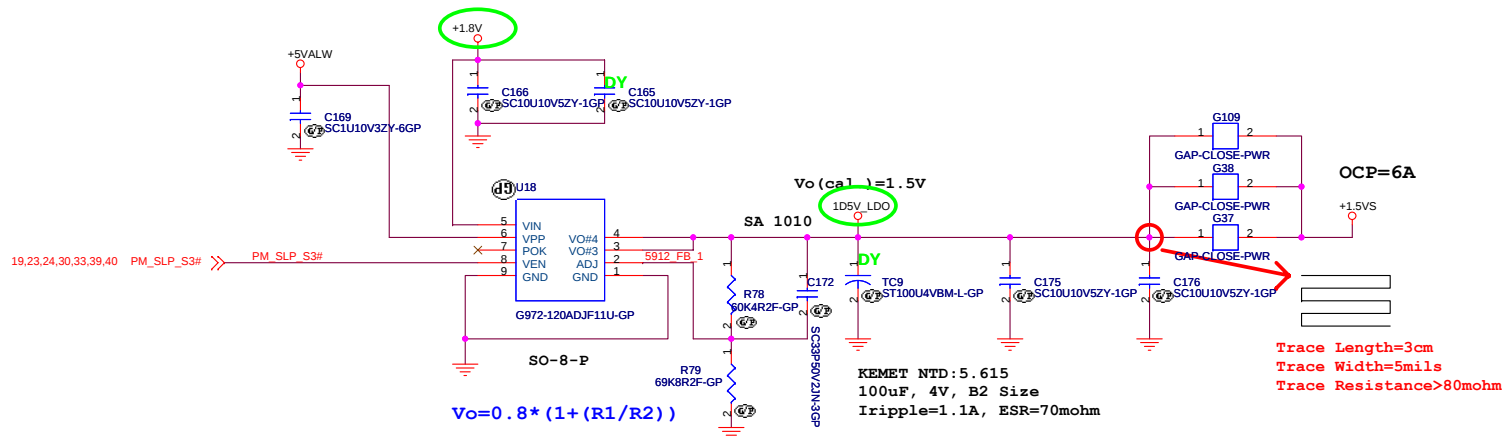
+1.05V_VCCP
I_{omax}=15A
OCP>20A

Close to IC SC412A



<Core Design>

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Title SC412A +1.05VS		
Size A3	Document Number Warrior	Rev SC
Date: Monday, January 07, 2008 Sheet 40 of 42		



<Core Design>

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Title

GMT 1D5V LDO

Size
A3

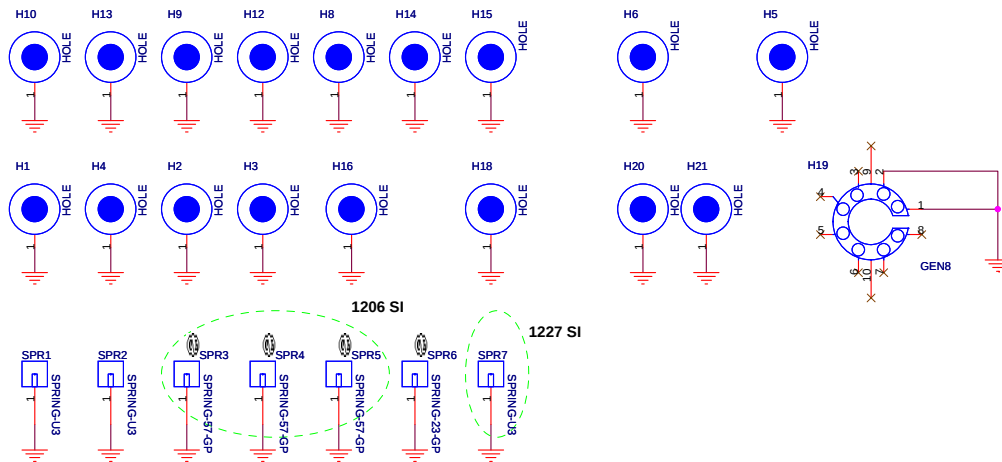
Document Number

Warrior

Rev
SC

Date: Monday, January 07, 2008

Sheet 41 of 42



SPR1-2: 34.40U07.001
 SPR3-5: 34.42T14.002
 SPR6 : 34.39S07.003
 SPR7 : 34.40U07.001

<Core Design>

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Title	MISC
Size A3	Document Number
Date: Monday, January 07, 2008	Rev SC
Sheet 42 of 42	