Leopard Block Diagram

Project code: 91.49Q01.001
PCB P/N : 48.49Q01.021
REVISION : 04216-4 FF

CLK GEN 3
ICS954206AG

4,5 Mobile CPU
Dothan

DDR1*2 333MHz 11,12

Host BUS 400/533MHz

1394 Conn 26

PCMCIA 1 SLOT 24

Power Switch TPS2220A 22

22,23 PCI 7411
CARDBUS
1394
SD/MS/MMC/SM

SD/MS 6 in 1 Card Slost 24

6,7,8,9,10 Alviso
GM/GML

LVDS
LCD 14

SVIDEO/COMP
TVOUT 13

RGB CRT
CRT

DAUGHTER BOARD

DMI I/F 100MHz

Mini-PCI 29
802.11a/b/g

16,17,18,19 ICH6-M

BLUE THUMB

USB 2.0
USB x 2
USB x 2 30

RJ45 CONN 26

10/100 RTL8100C 25,26

PCI BUS

P IDE
MASTER
HDD 21

SLAVE
DVD/ CD-RW 21

RJ11 CONN 25

MODEM 30
MDC Card

AC97-LINK

PCI EXPRESS/ USB2.0
EXPRESSCARD 21

LPC Bus

MIC IN 13

AC'97 CODEC 27
AD1981B

LINE OUT

Docking 13

OP AMP 28
G1420BF3U

SPEAKER 2CH

KBC 31
NS97551

X-BUS

LPC Debug Conn 33

Power Switch TPS2231 21

Comsumer IR 29

Touch Pad 31

Int. KB 31

Thermal & Fan 19
G768D

FlashRom 32
4Mb (512kB)

SYSTEM DC/DC 36 MAX1999	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC 37 TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 2D5V_S3

MAXIM CHARGER 34 MAX1909	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC 35 MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

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Taipei Hsien 221, Taiwan, R.O.C.

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ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_2D5V= 2.5 Voltage power up on system work(S0 state)
2D5V_S3= 2.5 Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 1.25 Voltage suspend to RAM(S3 state)
1D25V_S0= 1.25 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

38,39,40,41 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,16,18,36,40,41 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,40,41 CORE_GMCH_S0 — CORE_GMCH_S0
12,39 1D25V_S0 — 1D25V_S0
7,11,40 DDR_VREF_S3 — DDR_VREF_S3
5,7,9,17,18,21,38,39,41 1D5V_S0 — 1D5V_S0
18,39 1D5V_S5 — 1D5V_S5
5 1D5V_VCCA_S0 — 1D5V_VCCA_S0
4,5,36 VCC_CORE_S0 — VCC_CORE_S0
7,9,15,18,40 2D5V_S0 — 2D5V_S0
7,9,10,11,12,38,39,40,41 2D5V_S3 — 2D5V_S3
3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V_S0 — 3D3V_S0
13,14,30,40 3D3V_S3 — 3D3V_S3
17,18,19,21,25,29,31,35,37,39,40 3D3V_S5 — 3D3V_S5
25,41 3D3V_LAN_S5 — 3D3V_LAN_S5
16,20,31,32,34,35,36,37 3D3V_AUX — 3D3V_AUX
28 5VA_OP_S0 — 5VA_OP_S0
13,14,18,19,20,21,23,27,28,29,32,36,39,40,41 5V_S0 — 5V_S0
13,14,26,30,32,37,38,40,41 5V_S3 — 5V_S3
14,18,20,36,38 5V_S5 — 5V_S5
14,15,35,37,38,39 5V_AUX — 5V_AUX
14,35,37,38,39,40,41 DCBATOUT — DCBATOUT
13,34,35,41 AD+ — AD+
31,34,35,41 BT+ — BT+

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0#/GNT0#
Cardbus Controller TI7411	AD22	(CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG#	REQ1#/GNT1#
LAN	AD23	P_INTE#	REQ2#/GNT2#
Blue Thumb	AD24		

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Title: ITP
Size: A3 | Document Number: Leopard | Rev: -4
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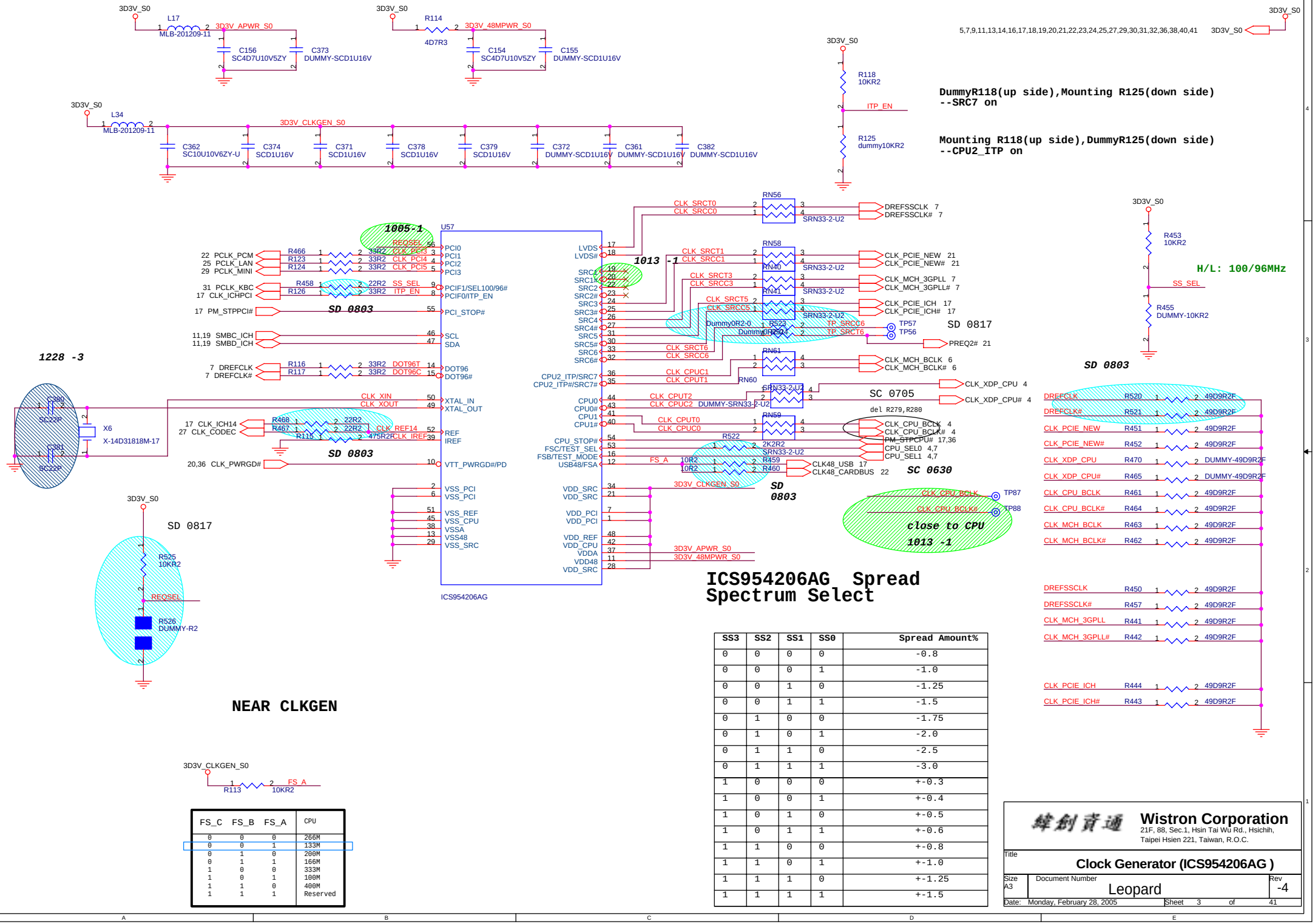
3D3V_S0
L17
MLB-201209-11
3D3V_APWR_S0
C156
SC4D7U10V5ZY
C373
DUMMY-SCD1U16V
R114
4D7R3
3D3V_48MPWR_S0
C154
SC4D7U10V5ZY
C155
DUMMY-SCD1U16V
L34
MLB-201209-11
3D3V_CLKGEN_S0
C362
SC10U10V6ZY-U
C374
SCD1U16V
C371
SCD1U16V
C378
SCD1U16V
C379
SCD1U16V
C372
DUMMY-SCD1U16V
C361
DUMMY-SCD1U16V
C382
DUMMY-SCD1U16V
5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41
R118
10KR2
ITP_EN
R125
dummy10KR2
DummyR118(up side),Mounting R125(down side)
--SRC7 on
Mounting R118(up side),DummyR125(down side)
--CPU2_ITP on
1005-1
U57
REQSEL
PCI0
PCI1
PCI2
PCI3
PCIF1/SEL100/96#
PCIF0/ITP_EN
PCI_STOP#
SCL
SDA
DOT96
DOT96#
XTAL_IN
XTAL_OUT
REF
IREF
VTT_PWRGD#/PD
VSS_PCI
VSS_PCI
VSS_REF
VSS_CPU
VSSA
VSS48
VSS_SRC
LVDS
LVDS#
SRC1
SRC1#
SRC2
SRC2#
SRC3
SRC3#
SRC4
SRC4#
SRC5
SRC5#
SRC6
SRC6#
CPU2_ITP/SRC7
CPU2_ITP#/SRC7#
CPU0
CPU0#
CPU1
CPU1#
CPU_STOP#
FSC/TEST_SEL
FSB/TEST_MODE
USB48/FSA
VDD_SRC
VDD_SRC
VDD_PCI
VDD_PCI
VDD_REF
VDD_CPU
VDDA
VDD48
VDD_SRC
ICS954206AG
22 PCLK_PCM
25 PCLK_LAN
29 PCLK_MINI
R466 33R2 CLK_PCI3
R123 33R2 CLK_PCI4
R124 33R2 CLK_PCI5
31 PCLK_KBC
17 CLK_ICHPCI
R458 22R2 SS_SEL
R126 33R2 ITP_EN
17 PM_STPPCI#
SD 0803
11,19 SMBC_ICH
11,19 SMBD_ICH
7 DREFCLK
7 DREFCLK#
R116 33R2 DOT96T
R117 33R2 DOT96C
CLK_XIN
CLK_XOUT
17 CLK_ICH14
27 CLK_CODEC
R468 22R2
R467 22R2
R115 475R2F
CLK_REF14
CLK_IREF
SD 0803
20,36 CLK_PWRGD#
1228 -3
C380
SC22P
C381
SC22P
X6
X-14D31818M-17
3D3V_S0
SD 0817
R525
10KR2
REQSEL
R526
DUMMY-R2
NEAR CLKGEN
3D3V_CLKGEN_S0
R113
10KR2
FS_A
FS_C FS_B FS_A CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved
1013 -1
CLK_SRCT0
CLK_SRCC0
CLK_SRCT1
CLK_SRCC1
CLK_SRCT3
CLK_SRCC3
CLK_SRCT5
CLK_SRCC5
CLK_SRCT6
CLK_SRCC6
CLK_CPUC1
CLK_CPUT1
CLK_CPUT2
CLK_CPUC2
CLK_CPUT0
CLK_CPUC0
FS_A
3D3V_CLKGEN_S0
3D3V_APWR_S0
3D3V_48MPWR_S0
RN56
SRN33-2-U2
DREFSSCLK 7
DREFSSCLK# 7
RN58
RN40
RN41
CLK_PCIE_NEW 21
CLK_PCIE_NEW# 21
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
CLK_PCIE_ICH 17
CLK_PCIE_ICH# 17
Dummy0R2-0
R523
Dummy0R2-0
R524
TP_SRCC6
TP_SRCT6
TP57
TP56
SD 0817
PREQ2# 21
RN61
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
RN60
DUMMY-SRN33-2-U2
SC 0705
CLK_XDP_CPU 4
CLK_XDP_CPU# 4
del R279,R280
RN59
CLK_CPU_BCLK 4
CLK_CPU_BCLK# 4
PM_STPCPU# 17,36
CPU_SEL0 4,7
CPU_SEL1 4,7
R522
2K2R2
10R2
10R2
R459
R460
CLK48_USB 17
CLK48_CARDBUS 22
SC 0630
SD 0803
CLK_CPU_BCLK
CLK_CPU_BCLK#
TP87
TP88
close to CPU
1013 -1
3D3V_S0
R453
10KR2
H/L: 100/96MHz
SS_SEL
R455
DUMMY-10KR2
SD 0803
DREFCLK R520 49D9R2F
DREFCLK# R521 49D9R2F
CLK_PCIE_NEW R451 49D9R2F
CLK_PCIE_NEW# R452 49D9R2F
CLK_XDP_CPU R470 DUMMY-49D9R2F
CLK_XDP_CPU# R465 DUMMY-49D9R2F
CLK_CPU_BCLK R461 49D9R2F
CLK_CPU_BCLK# R464 49D9R2F
CLK_MCH_BCLK R463 49D9R2F
CLK_MCH_BCLK# R462 49D9R2F
DREFSSCLK R450 49D9R2F
DREFSSCLK# R457 49D9R2F
CLK_MCH_3GPLL R441 49D9R2F
CLK_MCH_3GPLL# R442 49D9R2F
CLK_PCIE_ICH R444 49D9R2F
CLK_PCIE_ICH# R443 49D9R2F
ICS954206AG Spread Spectrum Select
SS3 SS2 SS1 SS0 Spread Amount%
0 0 0 0 -0.8
0 0 0 1 -1.0
0 0 1 0 -1.25
0 0 1 1 -1.5
0 1 0 0 -1.75
0 1 0 1 -2.0
0 1 1 0 -2.5
0 1 1 1 -3.0
1 0 0 0 +-0.3
1 0 0 1 +-0.4
1 0 1 0 +-0.5
1 0 1 1 +-0.6
1 1 0 0 +-0.8
1 1 0 1 +-1.0
1 1 1 0 +-1.25
1 1 1 1 +-1.5
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Title
Clock Generator (ICS954206AG)
Size A3
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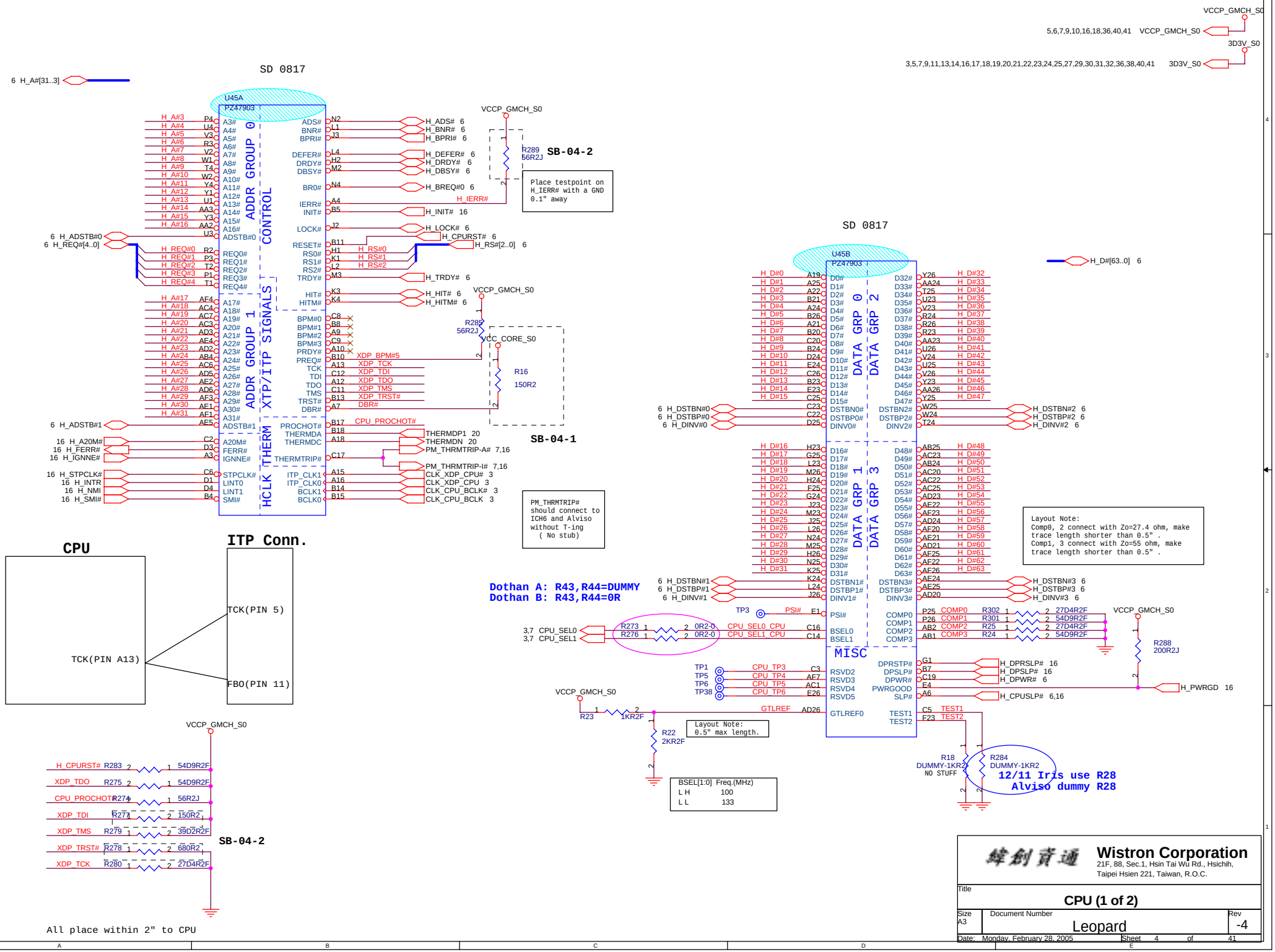
SD 0817
U45A
PZ47903
ADDR GROUP 0
ADDR GROUP 1
XTP/ITP SIGNALS
HCLK THERM CONTROL
SB-04-2
SB-04-1
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)
SD 0817
U45B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Dothan A: R43,R44=DUMMY
Dothan B: R43,R44=0R
Layout Note: 0.5" max length.
BSEL[1:0] Freq.(MHz)
L H 100
L L 133
12/11 Iris use R28
Alviso dummy R28
CPU
ITP Conn.
TCK(PIN A13)
TCK(PIN 5)
TBO(PIN 11)
SB-04-2
All place within 2" to CPU
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CPU (1 of 2)
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SD 0817

VCC_CORE_S0

U45C

PZ47903

1.8V is for Dothan A2 before.

1D5V OR 1D8V
Intel suggest Dothan A2 or later only use 1.5V

1D5V_VCCA_S0

C15 SCD01U25V2KX

C10 SC10U10V6ZY-U

TP_VCCA1 TP2
TP_VCCA2 TPAD30
TP_VCCA3 TP39

VCCP_GMCH_S0

SB-05-01

CPU_D10 R286 1 2 0R2-0

AA11	VCC0	VCC59	G5		
AA13	VCC1	VCC60	H22		
AA15	VCC2	VCC61	H6		
AA17	VCC3	VCC62	J21		
AA19	VCC4	VCC63	J5		
AA21	VCC5	VCC64	K22		
AA5	VCC6	VCC65	U5		
AA7	VCC7	VCC66	V22		
AA9	VCC8	VCC67	V6		
AB10	VCC9	VCC68	W21		
AB12	VCC10	VCC69	W5		
AB14	VCC11	VCC70	Y22		
AB16	VCC12	VCC71	Y6		
AB18	VCC13				
AB20	VCC14	VCCA0	F26		
AB22	VCC15	VCCA1	B1		
AB6	VCC16	VCCA2	N1		
AB8	VCC17	VCCA3	AC26		
AC11	VCC18				
AC13	VCC19	VCCP0	D10		
AC15	VCC20	VCCP1	D12		
AC17	VCC21	VCCP2	D14		
AC19	VCC22	VCCP3	D16		
AC9	VCC23	VCCP4	E11		
AD10	VCC24	VCCP5	E13		
AD12	VCC25	VCCP6	E15		
AD14	VCC26	VCCP7	F10		
AD16	VCC27	VCCP8	F12		
AD18	VCC28	VCCP9	F14		
AD8	VCC29	VCCP10	F16		
AE11	VCC30	VCCP11	K6		
AE13	VCC31	VCCP12	L21		
AE15	VCC32	VCCP13	L5		
AE17	VCC33	VCCP14	M22		
AE19	VCC34	VCCP15	M6		
AE9	VCC35	VCCP16	N21		
AF10	VCC36	VCCP17	N5		
AF12	VCC37	VCCP18	P22		
AF14	VCC38	VCCP19	P6		
AF16	VCC39	VCCP20	R21		
AF18	VCC40	VCCP21	R5		
AF8	VCC41	VCCP22	T22		
D18	VCC42	VCCP23	T6		
D20	VCC43	VCCP24	U21		
D22	VCC44				
D6	VCC45	VCCQ0	P23		
D8	VCC46	VCCQ1	W4		
E17	VCC47				
E19	VCC48	VID0	E2	H_VID0	36
E21	VCC49	VID1	F2	H_VID1	36
E5	VCC50	VID2	F3	H_VID2	36
E7	VCC51	VID3	G3	H_VID3	36
E9	VCC52	VID4	G4	H_VID4	36
F18	VCC53	VID5	H4	H_VID5	36
F20	VCC54				
F22	VCC55				
F6	VCC56	VCCSENSE	AE7	TP_VCCSENSE	
F8	VCC57				
G21	VCC58	VSSSENSE	AE6	TP_VSSSENSE	

R34 DUMMY-54D9R2F NO STUFF

R33 DUMMY-54D9R2F NO STUFF

Layout Note:

VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

U45D

PZ47903

A2	VSS0	VSS97	D13		
A5	VSS1	VSS98	D15		
A8	VSS2	VSS99	D17		
A11	VSS3	VSS100	D19		
A14	VSS4	VSS101	D21		
A17	VSS5	VSS102	D23		
A20	VSS6	VSS103	D26		
A23	VSS7	VSS104	E3		
A26	VSS8	VSS105	E6		
AA1	VSS9	VSS106	E8		
AA4	VSS10	VSS107	E10		
AA6	VSS11	VSS108	E12		
AA8	VSS12	VSS109	E14		
AA10	VSS13	VSS110	E16		
AA12	VSS14	VSS111	E18		
AA14	VSS15	VSS112	E20		
AA16	VSS16	VSS113	E22		
AA18	VSS17	VSS114	E25		
AA20	VSS18	VSS115	F1		
AA22	VSS19	VSS116	F4		
AA25	VSS20	VSS117	F5		
AB3	VSS21	VSS118	F7		
AB5	VSS22	VSS119	F9		
AB7	VSS23	VSS120	F11		
AB9	VSS24	VSS121	F13		
AB11	VSS25	VSS122	F15		
AB13	VSS26	VSS123	F17		
AB15	VSS27	VSS124	F19		
AB17	VSS28	VSS125	F21		
AB19	VSS29	VSS126	F24		
AB21	VSS30	VSS127	G2		
AB23	VSS31	VSS128	G6		
AB26	VSS32	VSS129	G22		
AC2	VSS33	VSS130	G23		
AC5	VSS34	VSS131	G26		
AC8	VSS35	VSS132	H3		
AC10	VSS36	VSS133	H5		
AC12	VSS37	VSS134	H21		
AC14	VSS38	VSS135	H25		
AC16	VSS39	VSS136	J1		
AC18	VSS40	VSS137	J4		
AC21	VSS41	VSS138	J6		
AC24	VSS42	VSS139	J22		
AD1	VSS43	VSS140	J24		
AD4	VSS44	VSS141	K2		
AD7	VSS45	VSS142	K5		
AD9	VSS46	VSS143	K21		
AD11	VSS47	VSS144	K23		
AD13	VSS48	VSS145	K26		
AD15	VSS49	VSS146	L3		
AD17	VSS50	VSS147	L6		
AD19	VSS51	VSS148	L22		
AD22	VSS52	VSS149	L25		
AD25	VSS53	VSS150	M1		
AE3	VSS54	VSS151	M4		
AE6	VSS55	VSS152	M5		
AE8	VSS56	VSS153	M21		
AE10	VSS57	VSS154	M24		
AE12	VSS58	VSS155	N3		
AE14	VSS59	VSS156	N6		
AE16	VSS60	VSS157	N22		
AE18	VSS61	VSS158	N23		
AE20	VSS62	VSS159	N26		
AE23	VSS63	VSS160	P2		
AE26	VSS64	VSS161	P5		
AF2	VSS65	VSS162	P21		
AF5	VSS66	VSS163	P24		
AF9	VSS67	VSS164	R1		
AF11	VSS68	VSS165	R4		
AF13	VSS69	VSS166	R6		
AF15	VSS70	VSS167	R22		
AF17	VSS71	VSS168	R25		
AF19	VSS72	VSS169	T3		
AF21	VSS73	VSS170	T5		
AF24	VSS74	VSS171	T21		
B3	VSS75	VSS172	T23		
B6	VSS76	VSS173	T26		
B9	VSS77	VSS174	U2		
B12	VSS78	VSS175	U6		
B16	VSS79	VSS176	U22		
B19	VSS80	VSS177	U24		
B22	VSS81	VSS178	V1		
B25	VSS82	VSS179	V4		
C1	VSS83	VSS180	V5		
C4	VSS84	VSS181	V21		
C7	VSS85	VSS182	V25		
C10	VSS86	VSS183	W3		
C13	VSS87	VSS184	W6		
C15	VSS88	VSS185	W22		
C18	VSS89	VSS186	W23		
C21	VSS90	VSS187	W26		
C24	VSS91	VSS188	Y2		
D2	VSS92	VSS189	Y5		
D5	VSS93	VSS190	Y21		
D7	VSS94	VSS191	Y24		
D9	VSS95				
D11	VSS96				

SD 0817

VCC_CORE_S0
4,36 VCC_CORE_S0

VCCP_GMCH_S0
4,6,7,9,10,16,18,36,40,41 VCCP_GMCH_S0

3D3V_S0
3,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V_S0

PUMA SC

1D5V_VCCA_S0

Imax = 120 mA

3D3V_S0

U44
SHDN# GND IN SET OUT
DY-G913C-U

BC53 dummySC1U10V3ZY

BC54 DummySC22P

BC2 DummySC1U10V3ZY

1D5V_VCCA_SET

R295 Dummy12K7R3F ZZ.12725.651

R296 Dummy49K9R2F

1D5V_VCCA_S0 1D5V_S0

R17 0R2-0

0.1u *10 150u *1

VCCP_GMCH_S0

C18 C19 C27 C33 C22 C11 C28 C34 C20 C26 SCD1U10V2MX-1

SD 0817

TC1 ST100U6D3VM-U NO STUFF

VCC_CORE_S0

C16 C17 C21 C23 C29 C31 C32 C36 C37 C38 C39 SC10U6D3V5MX

C44 C276 C277 C279 C280 C281 C282 C283 C284 DYSC100U6V3ZY-L

1013 -1

鋒創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU (2 of 2)	
Size A3	Document Number Leopard	Rev -4
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12/12 Trace 10 mil wide with 20 mil spacing

H_XRCOMP — R69 24D9R2F — H_YRCOMP — R87 24D9R2F

VCCP_GMCH_S0 — R70 54D9R2F — H_XSCOMP — VCCP_GMCH_S0 — R89 54D9R2F — H_YSCOMP

VCCP_GMCH_S0 — R67 221R3F — H_XSWING — R68 100R2F — C73 SCD1U16V

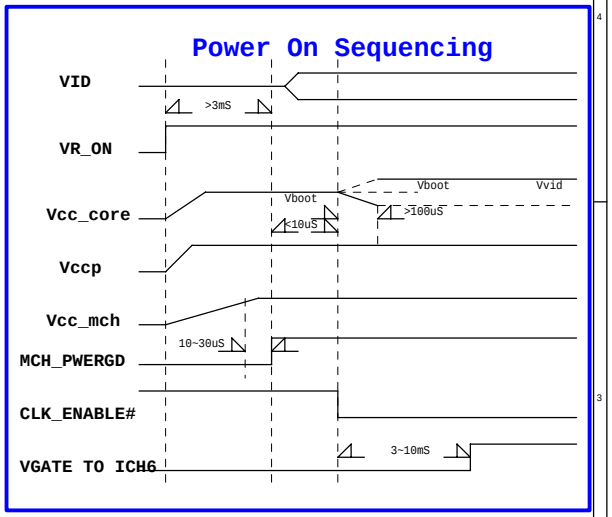
VCCP_GMCH_S0 — R86 221R3F — H_YSWING — R88 100R2F — C91 SCD1U16V

12/12 Trace 10 mil wide with 20 mil spacing

CORE_GMCH_S0
9,10,40,41 CORE_GMCH_S0

VCCP_GMCH_S0
4,5,7,9,10,16,18,36,40,41 VCCP_GMCH_S0

Power On Sequencing



Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 **101 = FSB400** others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	Reserved	0 = DDR2 **1 = DDR1 (Default)**
CFG7	CPU Strap	0 = Reserved **1 = Dothan (Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes **1 = Normal (Default)**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation (Default)**
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V (Default)** 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V (Default)** 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present(Default)** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

4 H_D#[63..0] — H_A#[31..3] 4

U17A — HOST — ALVISO-GM

HXRCOMP HXSCOMP HXSWING HYRCOMP HYSCOMP HYSWING

H_ADS# 4 — H_ADSTB#0 4 — H_ADSTB#1 4 — H_VREF — H_BNR# 4 — H_BPRI# 4 — H_BREQ#0 4 — H_CPURST# 4

VCCP_GMCH_S0 — R336 100R2F — C303 SCD1U10V2KX — R337 200R2F

2/10 HM1-SC Intel Sightings issue 54489

CLK_MCH_BCLK# 3 — CLK_MCH_BCLK 3

H_DBSY# 4 — H_DEFER# 4 — H_DINV#[3..0] 4 — H_DPWR# 4 — H_DRDY# 4 — H_DSTBN#[3..0] 4 — H_DSTBP#[3..0] 4

TP_H_EDRDY# — TP42 — H_HIT# 4 — H_HITM# 4 — H_LOCK# 4 — TP_H_PCREQ# — TP9 — H_REQ#[4..0] 4

H_RS#[2..0] 4

SC 0630

R311 — H_CPUSLP# 4,16 — H_CPUSLP_GMCH — H_TRDY# 4

CORE_GMCH_S0 — R391 DUMMY-0R2-0 — H_DPWR#

For Banias/Celeron-M:R93=DUMMY
For Dothan A:R93=DUMMY
For Dothan B:R93=0R

ALVISO-GM:71.0GMCH.08U
ALVISO-PM:71.0GMCH.0BU
ALVISO-GML:71.0GMCH.0JU

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Title: GMCH (1 of 5)
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Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die

9,15,18,40 2D5V_S0 — 2D5V_S0
9,10,11,12,38,39,40,41 2D5V_S3 — 2D5V_S3
5,9,17,18,21,38,39,41 1D5V_S0 — 1D5V_S0
6,9,10,40,41 CORE_GMCH_S0 — CORE_GMCH_S0
11,40 DDR_VREF_S3 — DDR_VREF_S3

U17B

17 DMI_TXN[3..0] — DMI_TXN0 AA31, DMI_TXN1 AB35, DMI_TXN2 AC31, DMI_TXN3 AD35 — DMIRXN0, DMIRXN1, DMIRXN2, DMIRXN3
17 DMI_TXP[3..0] — DMI_TXP0 Y31, DMI_TXP1 AA35, DMI_TXP2 AB31, DMI_TXP3 AC35 — DMIRXP0, DMIRXP1, DMIRXP2, DMIRXP3
17 DMI_RXN[3..0] — DMI_RXN0 AA33, DMI_RXN1 AB37, DMI_RXN2 AC33, DMI_RXN3 AD37 — DMITXN0, DMITXN1, DMITXN2, DMITXN3
17 DMI_RXP[3..0] — DMI_RXP0 Y33, DMI_RXP1 AA37, DMI_RXP2 AB33, DMI_RXP3 AC37 — DMITXP0, DMITXP1, DMITXP2, DMITXP3

DMI

11 CLK_DDR0 — AM33 SM_CK0
11 CLK_DDR1 — AL1 SM_CK1
AE11 SM_CK2
11 CLK_DDR3 — AJ34 SM_CK3
11 CLK_DDR4 — AF6 SM_CK4
AC10 SM_CK5
11 CLK_DDR0# — AN33 SM_CK0#
11 CLK_DDR1# — AK1 SM_CK1#
AE10 SM_CK2#
11 CLK_DDR3# — AJ33 SM_CK3#
11 CLK_DDR4# — AF5 SM_CK4#
AD10 SM_CK5#

11,12 M_CKE0_R# — AP21 SM_CKE0
11,12 M_CKE1_R# — AM21 SM_CKE1
11,12 M_CKE2_R# — AH21 SM_CKE2
11,12 M_CKE3_R# — AK21 SM_CKE3

11,12 M_CS0_R# — AN16 SM_CS0#
11,12 M_CS1_R# — AM14 SM_CS1#
11,12 M_CS2_R# — AH15 SM_CS2#
11,12 M_CS3_R# — AG16 SM_CS3#

Layout Note: Route as short as possible

M_OCDCOMP0 — AF22 SM_OCDCOMP0
M_OCDCOMP1 — AF16 SM_OCDCOMP1
R405 40D2R2F, R404 40D2R2F

AP14 SM_ODT0
AL15 SM_ODT1
AM11 SM_ODT2
AN10 SM_ODT3

DDR_VREF_S3
M_RCOMPN — AK10 SMRCOMPN
M_RCOMPP — AK11 SMRCOMPP
AF37 SMVREF0
AD1 SMVREF1
SMXSLEW — AE27 SMXSLEWIN
AE28 SMXSLEWOUT
SMYSLEW — AF9 SMYSLEWIN
AF10 SMYSLEWOUT
C109 SCD1U10V2MX-1

DDR MUXING

CFG0 G16 CFG0
CFG1 H13 CFG1
CFG2 G14 — R534 1 2 1KR2
CFG3 F16
CFG4 F15
CFG5 G15
CFG6 E16
CFG7 D17
CFG8 J16
CFG9 D15
CFG10 E15
CFG11 D14
CFG12 E14
CFG13 H12
CFG14 C14
CFG15 H15
CFG16 J15
CFG17 H14
CFG18 G22
CFG19 G23
CFG20 D23

CFG/RSVD

RSVD21 G25 — TP48
RSVD22 G24 — TP44
RSVD23 J17 — TP43
RSVD24 A31 — TP11
RSVD25 A30 — TP10
RSVD26 D26 — TP47
RSVD27 D25 — TP45

SD 0817

BM_BUSY# J23 — PM_BMBUSY# 17
EXT_TS0# J21 — PM_EXTTS#0
EXT_TS1# H22 — PM_EXTTS#1
THRMTRIP# F5 — PM_THRMTRIP-A# 4,16
PWROK AD30 — PWROK 20
RSTIN# AE29 — RST1# 1 2 R406 100R2 — PLT_RST1# 19,21

PM

DREF_CLKN A24 — DREFCLK# 3
DREF_CLKP A23 — DREFCLK 3
DREF_SSCLKN C37 — DREFSSCLK# 3
DREF_SSCLKP D37 — DREFSSCLK 3

CLK

NC1 AP37 GMCH_TP3 — TP20
NC2 AN37 GMCH_TP4 — TP18
NC3 AP36 GMCH_TP5 — TP19
NC4 AP2 GMCH_TP6 — TP15
NC5 AP1 GMCH_TP7 — TP16
NC6 AN1 GMCH_TP8 — TP17
NC7 B1 GMCH_TP9 — TP7
NC8 A2 GMCH_TP10 — TP8
NC9 B37 GMCH_TP11 — TP14
NC10 A36 GMCH_TP12 — TP13
NC11 A37 GMCH_TP13 — TP12

NC

ALVISO-GM

Intel suggest NC Due to votusly DVO

U17G

TP46 SDVO_DAT H24
TP49 SDVO_CLK H25
3 CLK_MCH_3GPLL# AB29
3 CLK_MCH_3GPLL AC29

SDVOCTRL_DATA
SDVOCTRL_CLK
GCLKN
GCLKP

MISC

13 COMP_VGA — A15 TVDAC_A
13 LUMA_VGA — C16 TVDAC_B
13 CRMA_VGA — A17 TVDAC_C
J18 TV_REFSET
B15 TV_IRTNA
B16 TV_IRTNB
B17 TV_IRTNC

R373 1 2 TV_REFSET
4K99R2F
SD 0817

R53 150R2F, R54 150R2F, R55 150R2F
SB-07-01

TV

15 GMCH_DDCCLK — E24 DDCCLK
15 GMCH_DDCDATA — E23 DDCDATA

Trace impendance 50ohm Less than 0.5", trace impendance 37.5ohm

15 VGA_BLUE — E21 BLUE
15 VGA_GREEN — D21 BLUE#
15 VGA_RED — C20 GREEN
B20 GREEN#
A19 RED
B19 RED#
H21 VSYNC
G21 HSYNC
J20 REFSET

R59 1 2 Dummy150R2F
R57 1 2 Dummy150R2F
R56 1 2 Dummy150R2F
1228 -3
13 VGA_VSYNC — R60 1 2 39R2J
13 VGA_HSYNC — R58 1 2 39R2J
R374 1 2 255R2F
SB-07-01

VGA

LBKLT_CRTL E25 LBKLT_CRTL
LBKLT_EN F25 LBKLT_EN
LCTLA_CLK C23 LCTLA_CLK
LCTLB_DATA C22 LCTLB_DATA
LDDC_CLK F23 LDDC_CLK
LDDC_DATA F22 LDDC_DATA
VDD_EN F26 VDD_EN
LIBG C33 LIBG
LVBG C31 LVBG
L_VREFH F28 LVREFH
L_VREFL F27 LVREFL

31 BL_ON — LBKLT_CRTL
14 LCDVDD_ON — LIBG
TP41 L_LVBG
TP51 L_VREFH
TP50 L_VREFL
NO_STUFF

LVDS

PCI-EXPRESS GRAPHICS

EXP_COMPI D36
EXP_ICOMPO D34
PEG_COMP 2 R71 1 24D9R2F — 1D5V_S0

EXP_RXN0 E30
EXP_RXN1 F34
EXP_RXN2 G30
EXP_RXN3 H34
EXP_RXN4 J30
EXP_RXN5 K34
EXP_RXN6 L30
EXP_RXN7 M34
EXP_RXN8 N30
EXP_RXN9 P34
EXP_RXN10 R30
EXP_RXN11 T34
EXP_RXN12 U30
EXP_RXN13 V34
EXP_RXN14 W30
EXP_RXN15 Y34

EXP_RXP0 D30
EXP_RXP1 E34
EXP_RXP2 F30
EXP_RXP3 G34
EXP_RXP4 H30
EXP_RXP5 J34
EXP_RXP6 K30
EXP_RXP7 L34
EXP_RXP8 M30
EXP_RXP9 N34
EXP_RXP10 P30
EXP_RXP11 R34
EXP_RXP12 T30
EXP_RXP13 U34
EXP_RXP14 V30
EXP_RXP15 W34

EXP_TXN0 E32
EXP_TXN1 F36
EXP_TXN2 G32
EXP_TXN3 H36
EXP_TXN4 J32
EXP_TXN5 K36
EXP_TXN6 L32
EXP_TXN7 M36
EXP_TXN8 N32
EXP_TXN9 P36
EXP_TXN10 R32
EXP_TXN11 T36
EXP_TXN12 U32
EXP_TXN13 V36
EXP_TXN14 W32
EXP_TXN15 Y36

EXP_TXP0 D32
EXP_TXP1 E36
EXP_TXP2 F32
EXP_TXP3 G36
EXP_TXP4 H32
EXP_TXP5 J36
EXP_TXP6 K32
EXP_TXP7 L36
EXP_TXP8 M32
EXP_TXP9 N36
EXP_TXP10 P32
EXP_TXP11 R36
EXP_TXP12 T32
EXP_TXP13 U36
EXP_TXP14 V32
EXP_TXP15 W36

ALVISO-GM

PUMA SC
SB-07-02

2D5V_S0
RN39 SRN2K2
LCTLA_CLK 1 8
LCTLB_DATA 2 7
LDDC_CLK 3 6
LDDC_DATA 4 5

14 TXACLK- — B30 LACLKN
14 TXACLK+ — B29 LACLKP
14 TXBCLK- — C25 LBCLKN
14 TXBCLK+ — C24 LBCLKP

14 TXAOUT0- — B34 LADATAN0
14 TXAOUT1- — B33 LADATAN1
14 TXAOUT2- — B32 LADATAN2

14 TXAOUT0+ — A34 LADATAP0
14 TXAOUT1+ — A33 LADATAP1
14 TXAOUT2+ — B31 LADATAP2

14 TXBOUT0- — C29 LBDATAN0
14 TXBOUT1- — D28 LBDATAN1
14 TXBOUT2- — C27 LBDATAN2

14 TXBOUT0+ — C28 LBDATAP0
14 TXBOUT1+ — D27 LBDATAP1
14 TXBOUT2+ — C26 LBDATAP2

BL_ON R382 1 2 100KR2
LBKLT_CRTL R381 1 2 100KR2
LIBG R379 1 2 1K5R2F

2D5V_S0
R375 10KR2 1 2 PM_EXTTS#0
R378 10KR2 1 2 PM_EXTTS#1

When Low 2.2K Ohm

R350 1 2 DUMMY-R2 CFG3
R348 1 2 DUMMY-R2 CFG4
R343 1 2 DUMMY-R2 CFG5
R351 1 2 DUMMY-R2 CFG6
R352 1 2 DUMMY-R2 CFG7
R340 1 2 DUMMY-R2 CFG8
R347 1 2 DUMMY-R2 CFG9
R349 1 2 DUMMY-R2 CFG10
R52 1 2 DUMMY-R2 CFG11
R345 1 2 DUMMY-R2 CFG12
R338 1 2 DUMMY-R2 CFG13
R346 1 2 DUMMY-R2 CFG14
R342 1 2 DUMMY-R2 CFG15
R339 1 2 DUMMY-R2 CFG16
R341 1 2 DUMMY-R2 CFG17

When High 1K Ohm

2D5V_S0
R380 1 2 DUMMY-R2 CFG18
R376 1 2 DUMMY-R2 CFG19
R377 1 2 DUMMY-R2 CFG20

FOR DDR1

2D5V_S3
R403 80D6R2F
M_RCOMPN
M_RCOMPP
R429 80D6R2F

VCCP_GMCH_S0
Ref ALVISO EDS-1 Page 115
SD 0817
Epr Dothan-B
R344 10KR2, R49 10KR2, R50 1KR2
SB-07-03
CFG2 — CPU_SEL0 3,4
CFG1 — CPU_SEL1 3,4
CFG0
R48 DummyK7R2, R51 DummyK7R2

CFG(2..1)	FREQ.(MHz)
10	400
00	533
11	Reserved

CFG2=0(R51):133MHZ
CFG2=1(R50):100MHZ

3D3V_S0
RN38 SRN4D7KJ
14 EDID_CLK
14 EDID_DAT
LDDC_CLK
LDDC_DATA
2D5V_S0
U14 2N7002DW
SC 0701

PUMA SC

Strapping

CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors

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Title: GMCH (2 of 5)
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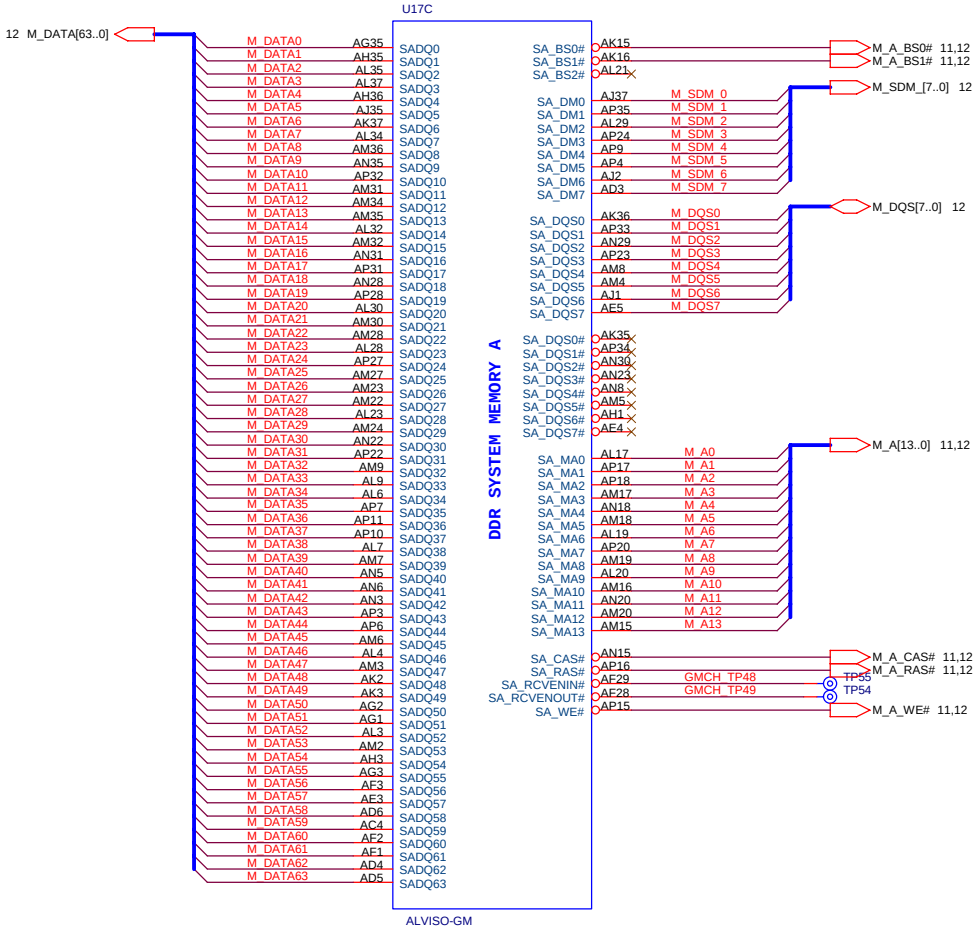
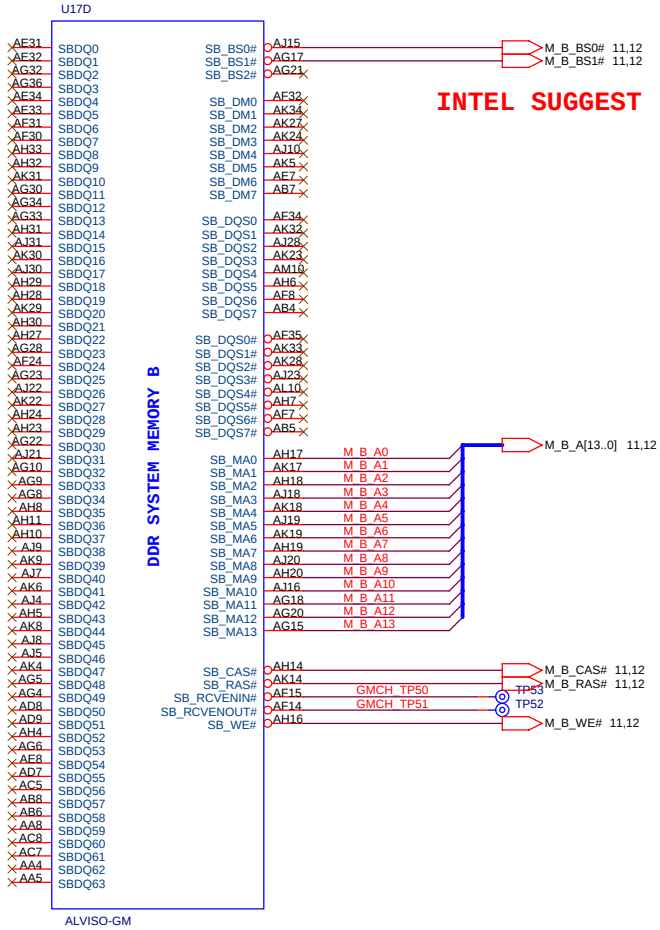
SUPPORT DDR333 ONLY





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Title: GMCH (3 of 5)		
Size: A3	Document Number: Leopard	Rev: -4
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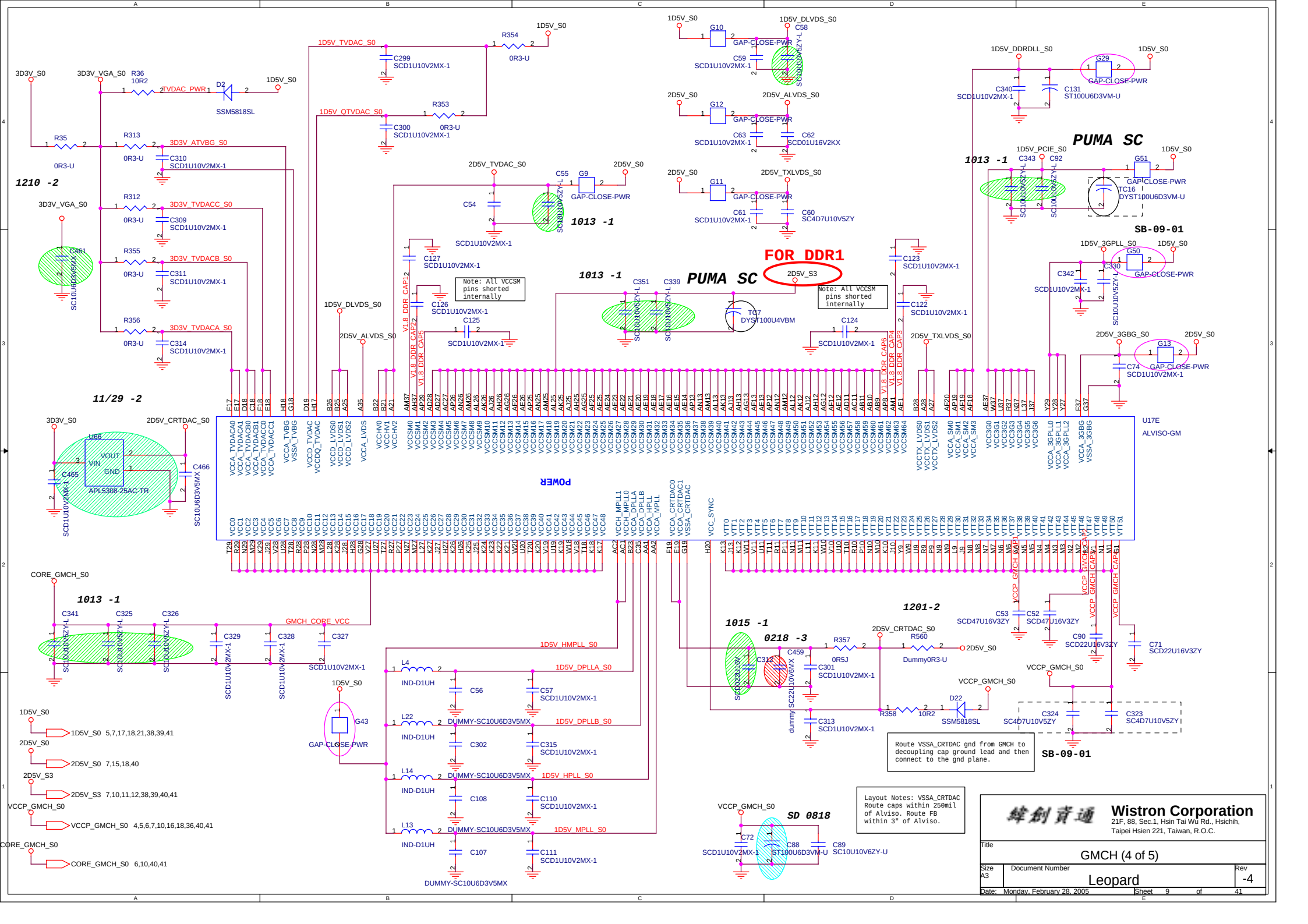
PUMA SC
FOR DDR1
POWER
1210 -2
1013 -1
11/29 -2
1015 -1
0218 -3
1201-2
SD 0818
SB-09-01
Note: All VCCSM pins shorted internally
Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.
Layout Notes: VSSA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
U17E
ALVISO-GM
Wistron Corporation
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GMCH (4 of 5)
Leopard
-4
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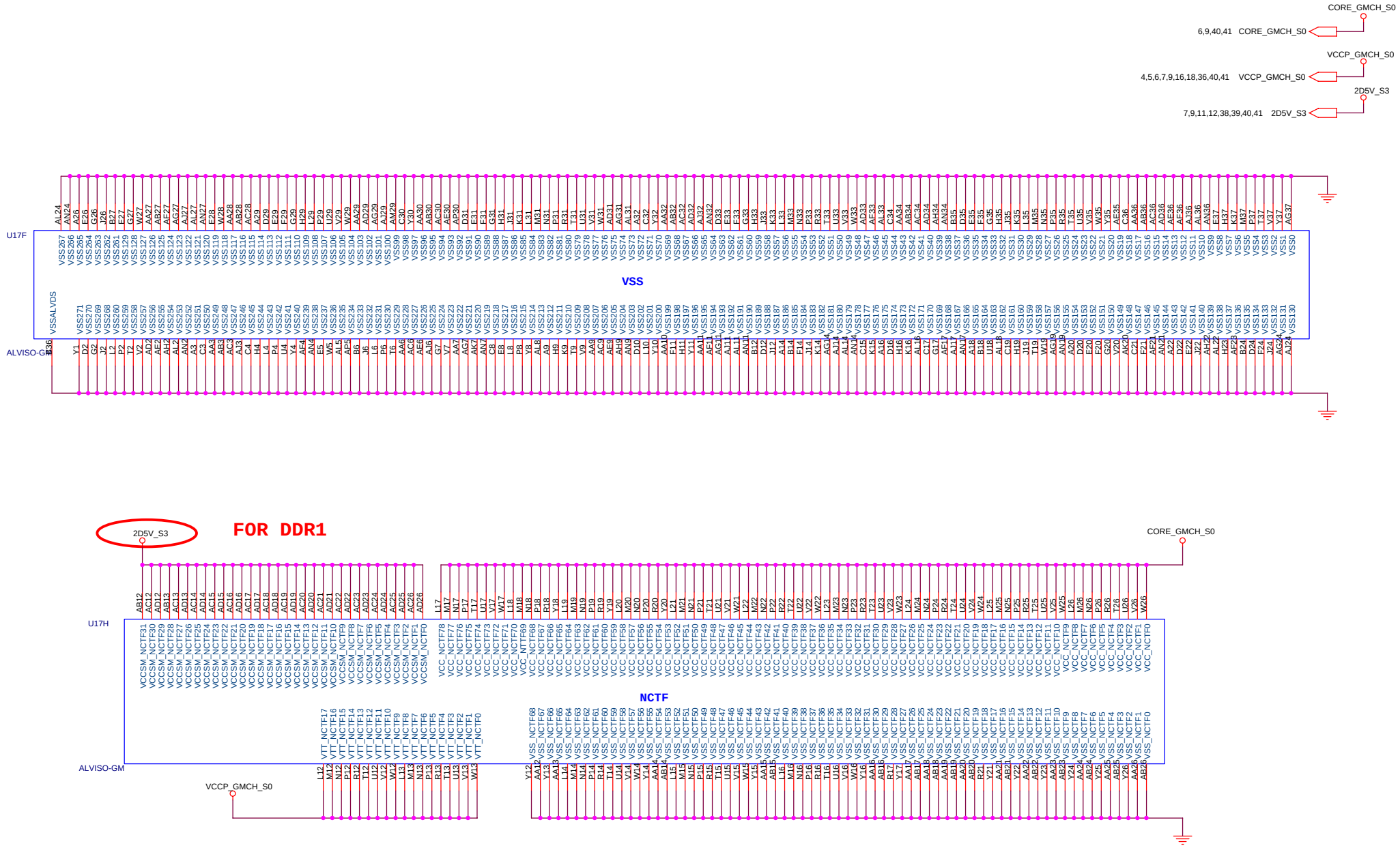

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Title: GMCH (5 of 5)

Size: A3 | Document Number: Leopard | Rev: -4

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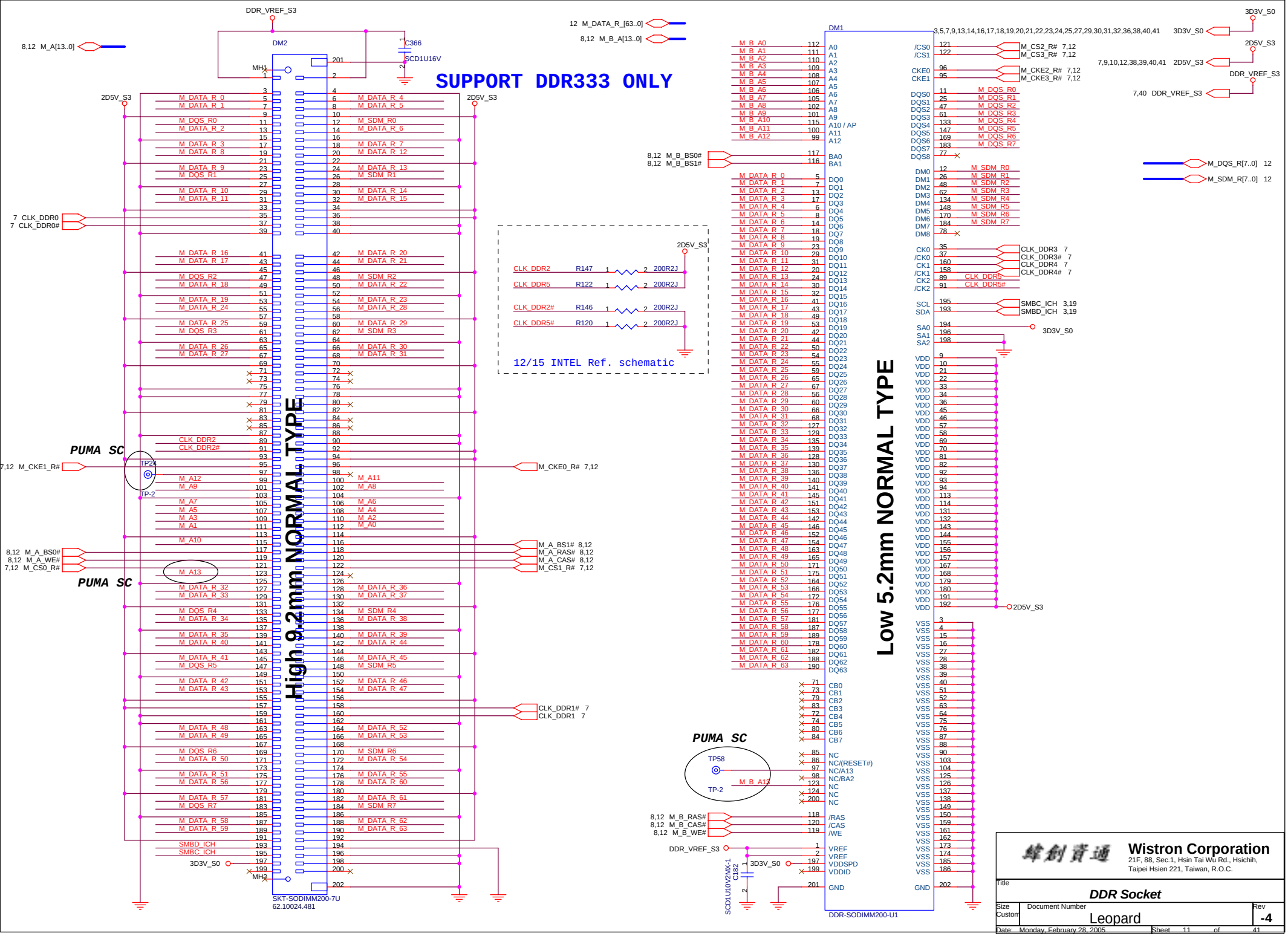
SUPPORT DDR333 ONLY
High 9.2mm NORMAL TYPE
Low 5.2mm NORMAL TYPE
PUMA SC
PUMA SC
PUMA SC
12/15 INTEL Ref. schematic
DM2
DM1
SKT-SODIMM200-7U
62.10024.481
DDR-SODIMM200-U1
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR Socket
Size
Custom
Document Number
Leopard
Rev
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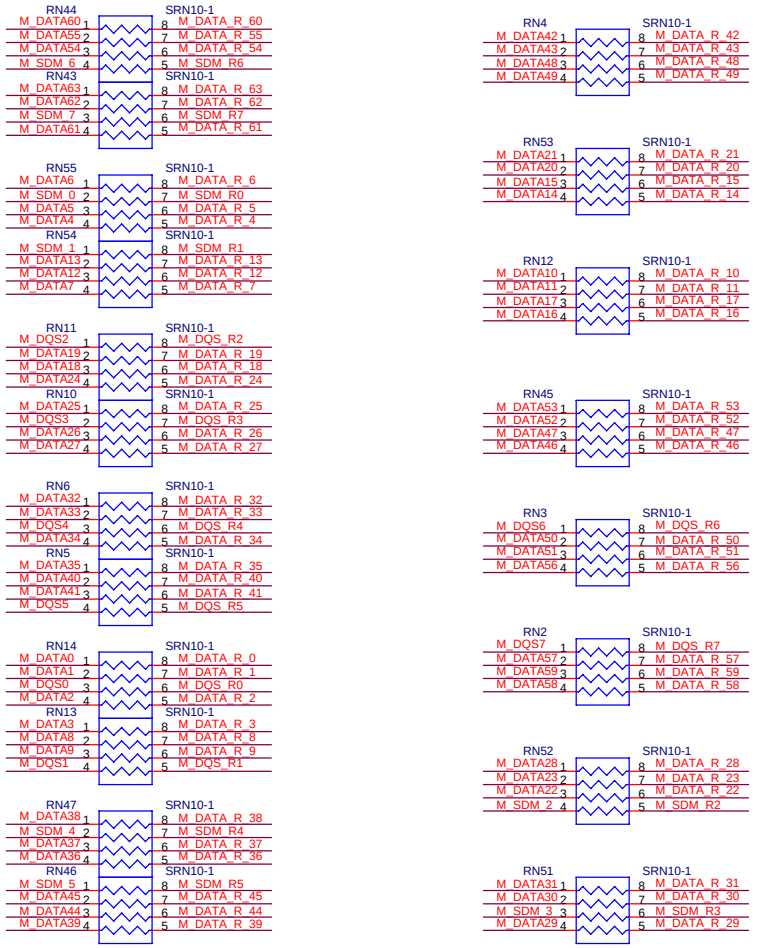
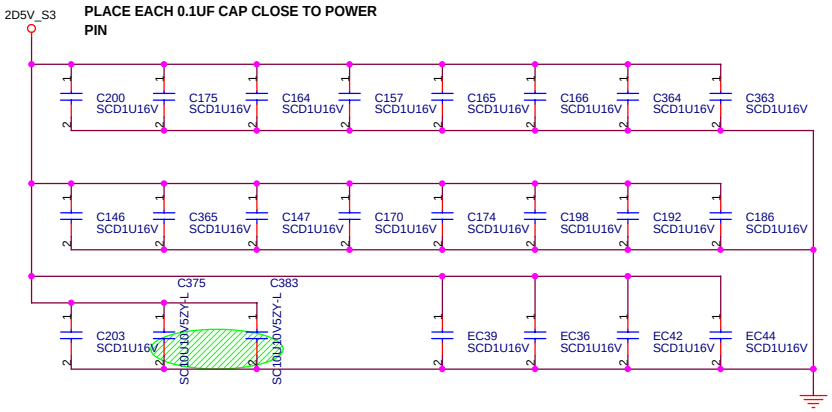
SERIES DAMPING

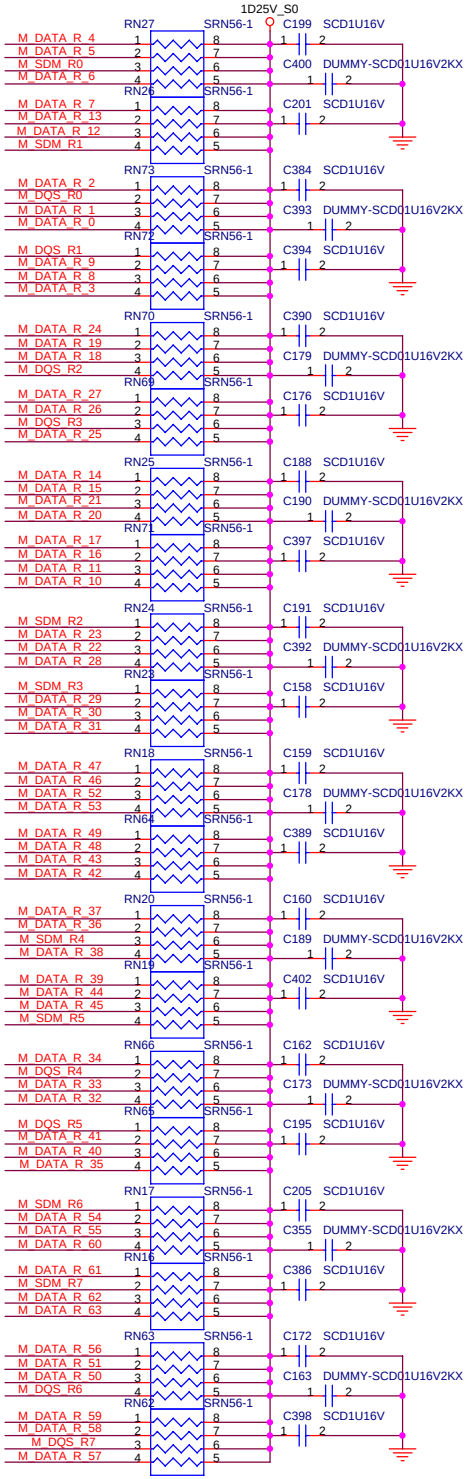
PUMA-SC

Change RN to small size



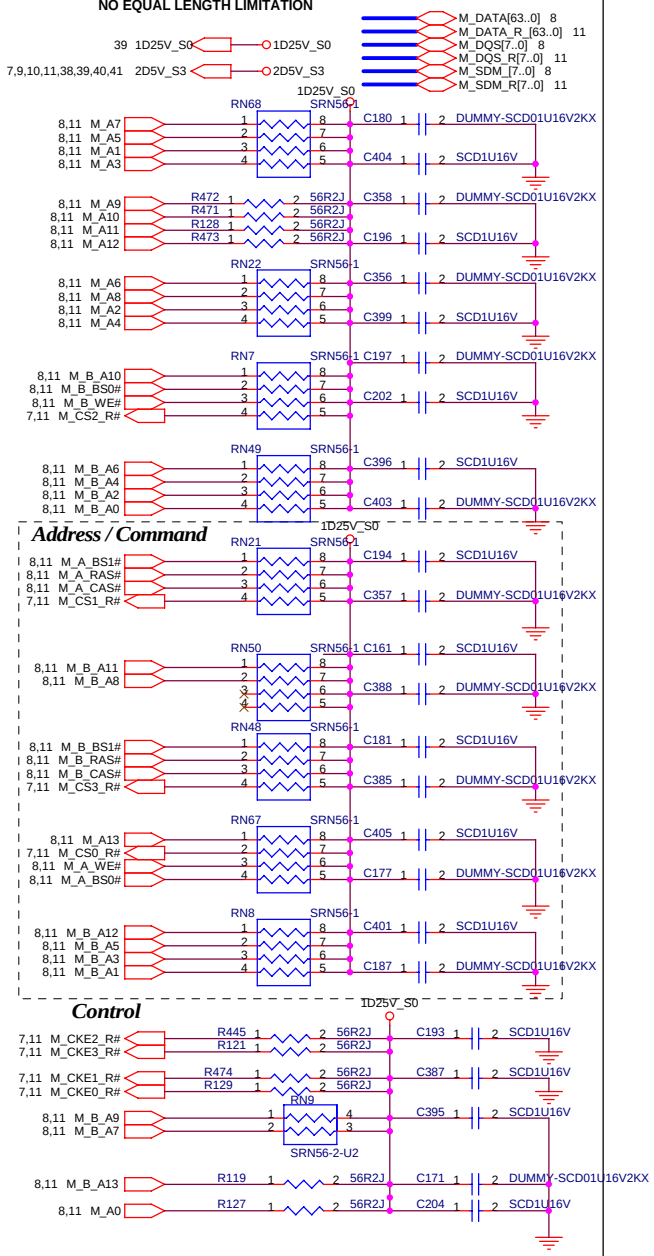
PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN





PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION



鋒創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR Serial/Terminator Resistor***

Size	Document Number	Rev
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Docking Connector

Digital Signal CONN

CN5 — JST-CON20 — 1005-1

USB_P_CON0, USB_N_CON0, 5V_S3, USB_P_CON1, USB_N_CON1, 5V_S3, CRMA_CN5, LUMA_CN5, 5V_S0, DDC_DATA 15, DDC_CLK 15, JVGA_HS 7, JVGA_VS 7, 5V_S0, CRT_R 15, CRT_G 15, CRT_B 15

LINE-OUT

PUMA SC

LUMA_CN5 — L12 BLM11B750S — LUMA
CRMA_CN5 — L15 BLM11B750S — CRMA

SD 0817

BC12 SC33P50V2CN, BC13 SC33P50V2CN, C99 DUMMY-SC3P50V2CN, C102 DUMMY-SC3P50V2CN, R94 150R2F, R91 150R2F

VOL_UP_DK# — D29 DummyBAV99LT1
VOL_DWN_DK# — D30 DummyBAV99LT1

1015 -1

Close to Docking CN

Analog Signal CONN

1006 -1

CN6 — MOLEX-CON10-1

MIC_PR, EXT_MIC_1 27, EXT_MIC_2 27, HP_OUT_R 27, HP_OUT_L 27, EARPHONE 28, LID_SW 14, AUD_AGND, 3D3V_S0

R432 47KR2 63.47334.1D1 — EARPHONE

MIC-IN

17 USB_PN6 — USB_N_CON6
17 USB_PP6 — USB_P_CON6
17 USB_PN0 — USB_N_CON0
17 USB_PP0 — USB_P_CON0
USB_N_CON1 — USB_PN1 17
USB_P_CON1 — USB_PP1 17

3D3V_S3 — D31 BAV99LT1 — LID_SW

11/29 -2

26 BC0EX1 — R495 — DUMMY-R2 — ICH_PME# 17,25,29
26 BC0EX2 — R225 — DUMMY-R2 — PCI_AD24 17,22,25,29

Please close to ICH6

HP suggest

0218 -3

5V_S0 — R309 10KR2 — PR_INSERT# — PR_INSERT# 31
DOCK_PRESENT — R63 47R2 — Q17 MMBT3904-U1
R64 dummy2K2R2 — PR_PRESENT#

5V_S3 — F3 FUSE-2A8V — 5V_DOCK
C306 SC4D7U10V5ZY, C305 SCD1U16V, TC15 DUMMY-ST47U6D3V-U1

100 mil

PUMA SC

1209 -2

5V_S3, AD+, 5V_S0, DCBATOUT_BEAD, 5V_S0
C337 SCD1U16V, C70 SCD1U25V3KX, C458 SCD1U16V, C69 SCD1U25V3KX, C338 SCD1U16V

1011 -1 — 27 SPDIF_OUT — L19 BLM18PG600SN1 — SPDIF — C51 SC470P25V2KN
C464 SC470P25V2KN
EC124 DUMMY-SCD1U16V — AUD_AGND

PUMA SC

15 CIR — R259 0R2-0 — CIR_KBC 31
CIR_PR — 0R2-0

CIR,CIR_PR,CIR_KBC are connect togather. default setting 12/12

CN12 — FOX-CONN58D-U3

3/15 HM1-SD

PR_PRESENT#, RJ45-4 26, RJ45-5 26, RJ45-1 26, RJ45-2 26, MIC_PR, AUD_AGND, DK_SPKR_R+ 28, DK_SPKR_L+ 28, VOL_UP_DK# 31, USB_N_CON6, USB_P_CON6, IR_OUT, TP40, R333 0R2-0, COMP_PR, LUMA_PR, CRMA_PR, CIR_PR, VOL_DWN_DK# 31, 5V_DOCK, DCBATOUT_BEAD, R65 1KR2, AD+

1209 -2

RJ45-7 26, RJ45-8 26, RJ45-3 26, RJ45-6 26, JACK_DETECT# 28, SPDIF, 5V_Dock_S0, R43 0R2-0, 5V_S0, MUTE_LED 14,31, 1394_TPA1P_PR 26, 1394_TPA1N_PR 26, 1394_TPB1P_PR 26, 1394_TPB1N_PR 26, DOCK_PRESENT, 5V_DOCK, AD+

SD 0812

SD 0812 HM1-SD FOR EMI

JACK_DETECT# EC8, MUTE_LED EC11, AUD_AGND EC93, MIC_PR EC95, DK_SPKR_R+ EC94, DK_SPKR_L+ EC1021, COMP_PR EC100, VOL_UP_DK# EC1011, VOL_DWN_DK# EC1031, DOCK_PRESENT EC20, PR_PRESENT# EC92, BT_LED EC19 — SCD1U16V / SC1000P16V2KX — BT_LED 14,26

3D3V_S0 — 3,5,7,9,11,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41
5V_S0 — 14,18,19,20,21,23,27,28,29,32,36,39,40,41
5V_S3 — 14,26,30,32,37,38,40,41
DCBATOUT — 14,35,37,38,39,40,41
5V_AUX — 14,15,35,37,38,39

INPUT	FUNCTION
LOW	B0
HIGH	B1

Place near the GMCH

U7 NC7SB3157P6X-U — LUMA_VGA 7
U8 NC7SB3157P6X-U — CRMA_VGA 7
PR_INSERT#

SD 0817

LUMA_PR — L26 IND-1D2UH — LUMA_PR_1 — C290 SC47P50V2JN, C297 SC47P50V2JN, R334 150R2F
CRMA_PR — L24 IND-1D2UH — CRMA_PR_1 — C299 SC47P50V2JN, C307 SC47P50V2JN
COMP_PR — L25 IND-1D2UH — C295 SC47P50V2JN, C298 SC47P50V2JN, R335 150R2F, R372 150R2F

SB-13-01

R536 0R2-0 — COMP_VGA 7

Place near the DOCK

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Board to board conn/ Docking

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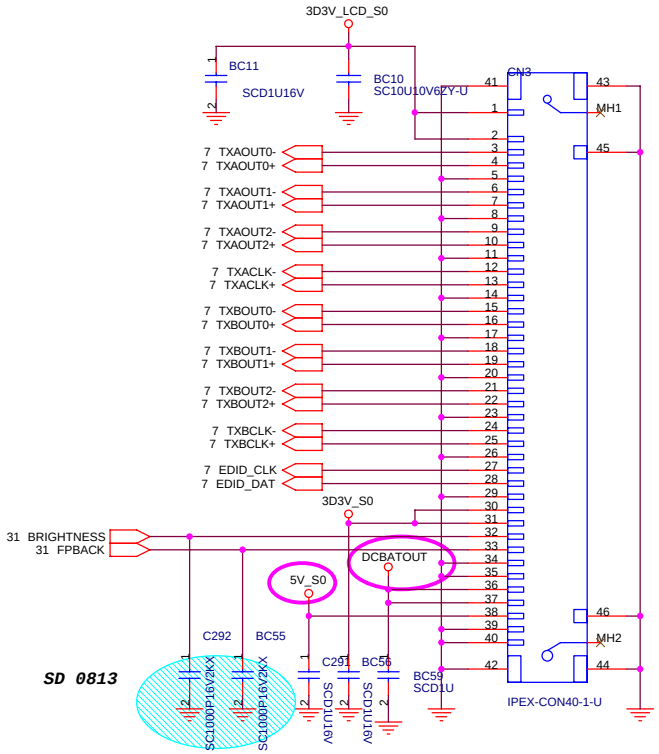
INVERTER/LCD

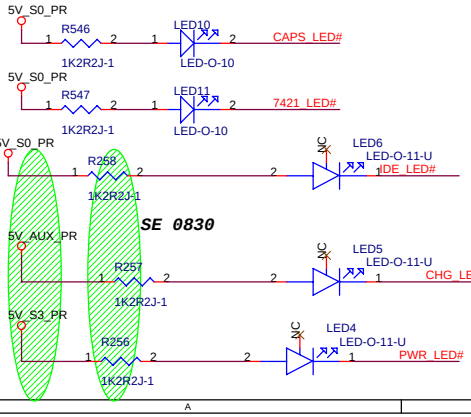


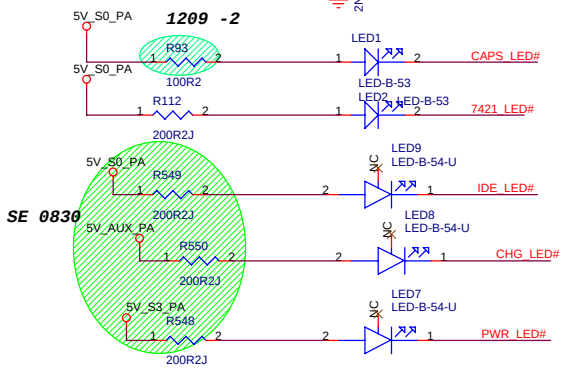
		PWR	CHR	HDD	IR	CAPS	7421
PR Botton		Amber LED4	Amber LED5	Amber LED6	U42	Amber LED1	Amber LED2
PA Top		Blue LED8	Blue LED7	Blue LED9	U64	Blue LED1	Blue LED2

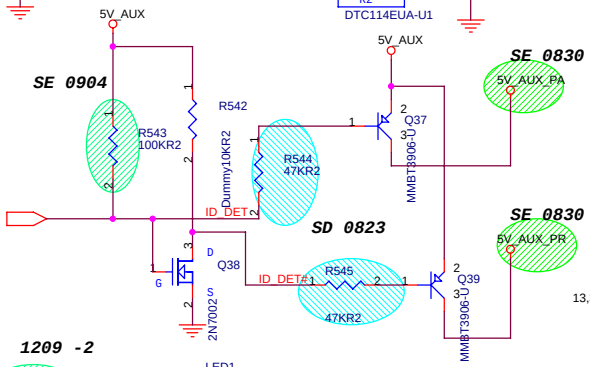
SC 0705

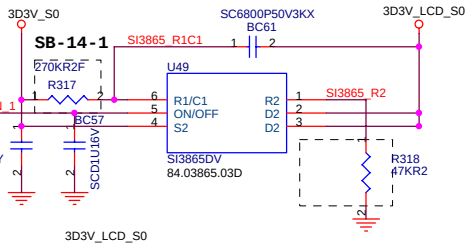
change R from 100 to 200 ohm

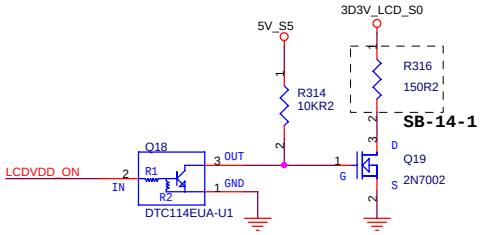
PUMA SC

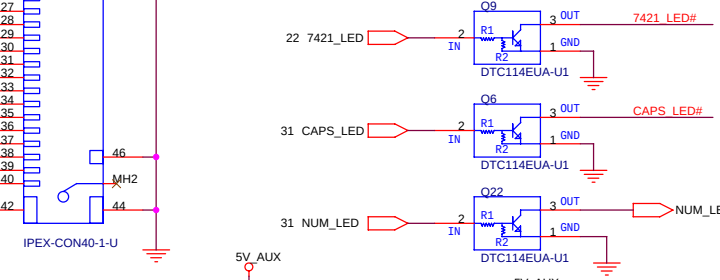


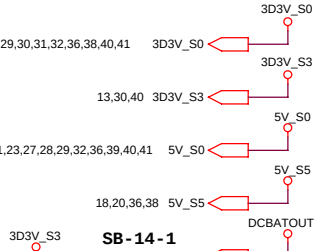


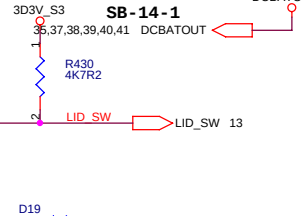


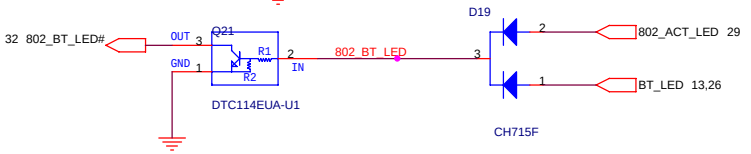


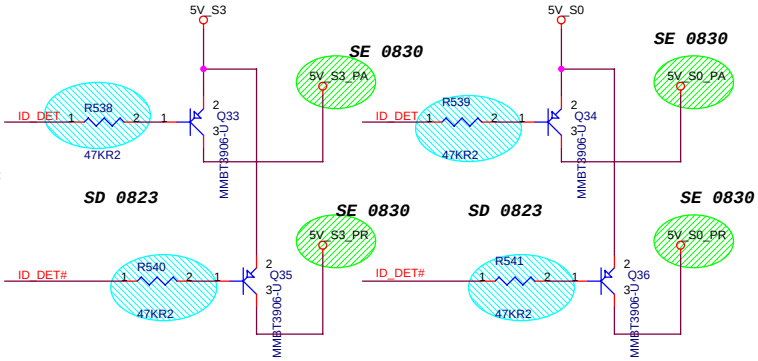


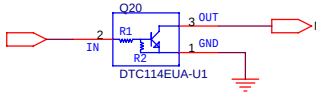


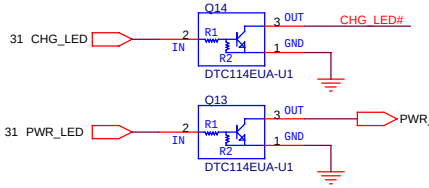












鋒創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Inverter/LCD***	
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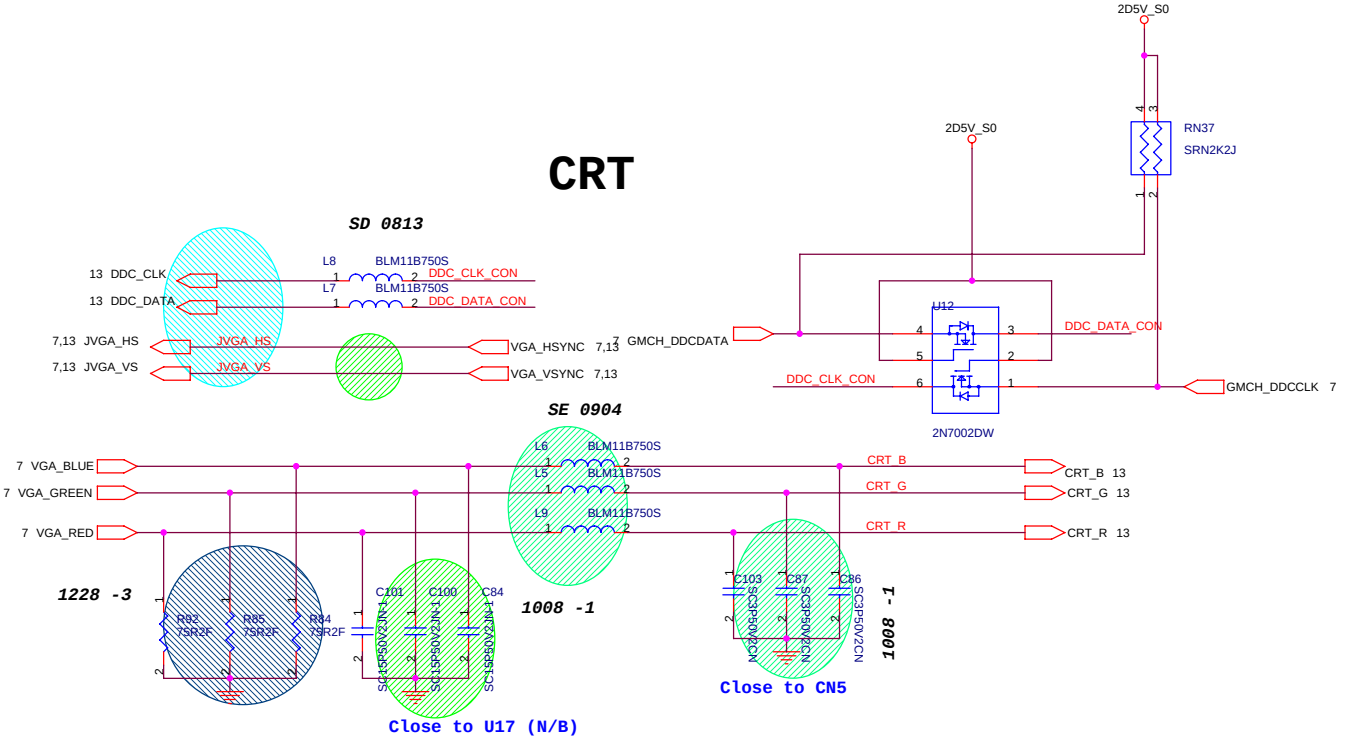
PA & PR diffent parts

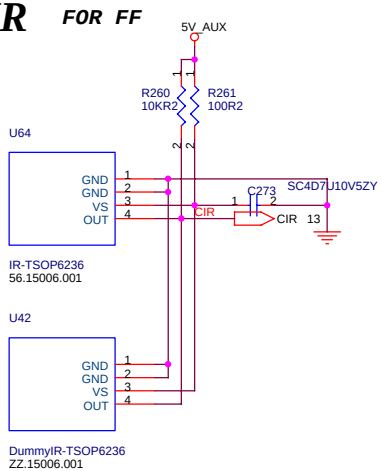
	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED2	83.00190.Y70	83.00190.W70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	Dummy	83.00110.D70
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
LED9	83.00110.E70	Dummy
U64	56.15006.001	Dummy
U42	Dummy	56.15006.001
R256	63.20134.1D1	63.12234.1D1
R257	63.20134.1D1	63.12234.1D1
R258	63.20134.1D1	63.12234.1D1
R93	63.20134.1D1	63.12234.1D1
R112	63.20134.1D1	63.12234.1D1
CBUS1	21.H0088.001	21.H0088.001
R176	63.10334.1D1	Dummy
R177	Dummy	63.10334.1D1

CRT



010804 Modified on Astro ID request

CIR FOR FF



鋒創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CRT/ CIR	
Size A3	Document Number: Leopard	Rev -4
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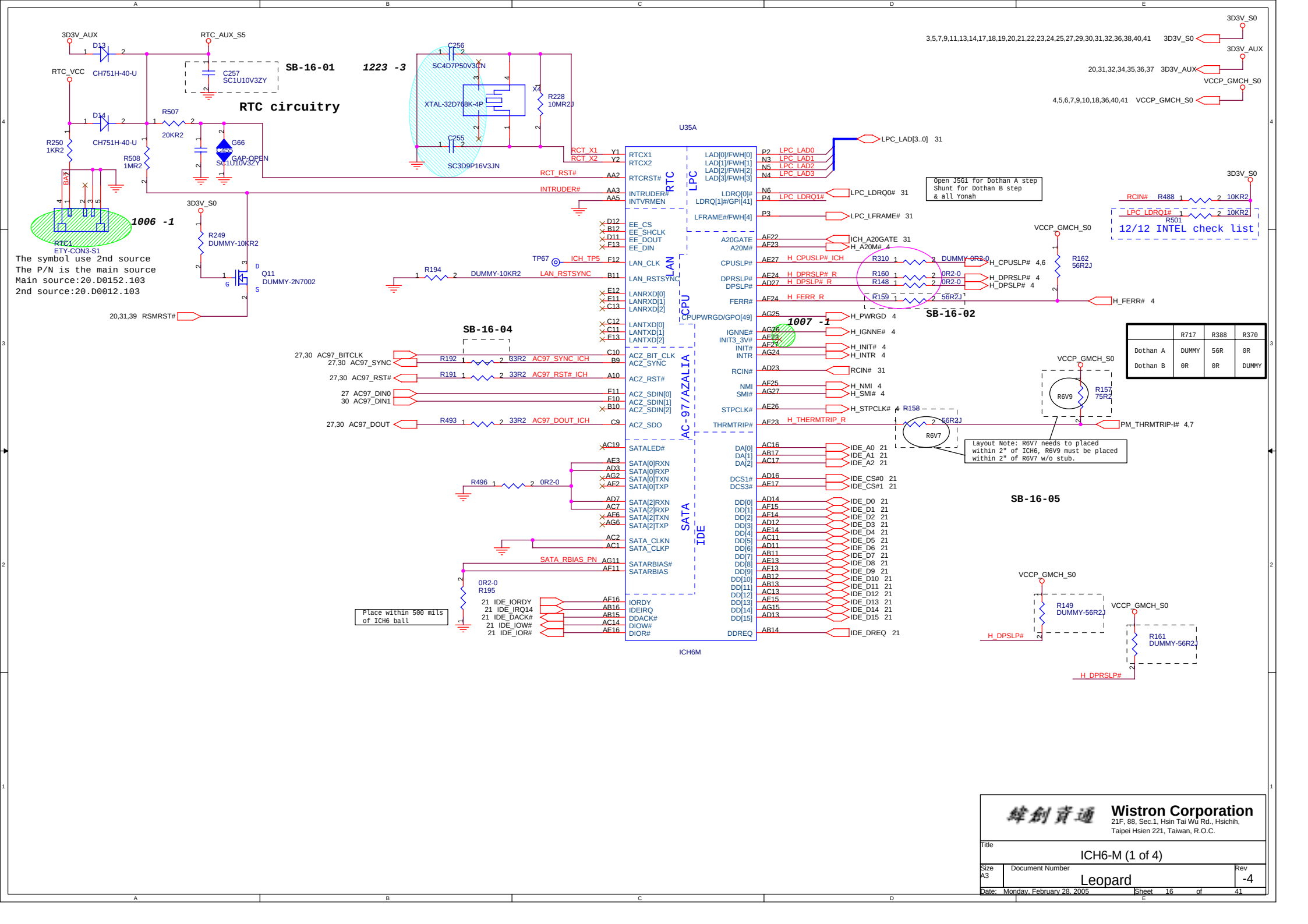
RTC circuitry
SB-16-01
1223 -3
1006 -1
1007 -1
SB-16-02
SB-16-04
SB-16-05
The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103
12/12 INTEL check list
Open J5G1 for Dothan A step
Shunt for Dothan B step
& all Yonah
Layout Note: R6V7 needs to placed within 2" of ICH6, R6V9 must be placed within 2" of R6V7 w/o stub.
Place within 500 mils of ICH6 ball
U35A
ICH6M
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
Dothan A
Dothan B
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH6-M (1 of 4)
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U35B

U35C

PCIE AC coupling caps
need to be within 250 mils of the driver.

Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.

Place within 500 mils of ICH

ICH6M

ICH6 Pullups

PUMA Board Version Setting

Ver.	PCB_VER0	PCB_VER1
DB	0	0
SI	0	1
PV	1	0
MV	1	1

ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

HM1-SB
To avoide leakage current

Intel 22.6 ohm 1%

1D5V_S0 1D5V_S0 5,7,9,18,21,38,39,41
3D3V_S5 3D3V_S5 18,19,21,25,29,31,35,37,39,40
3D3V_S0 3D3V_S0 3,5,7,9,11,13,14,16,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41

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Title: ICH6-M (2 of 4)

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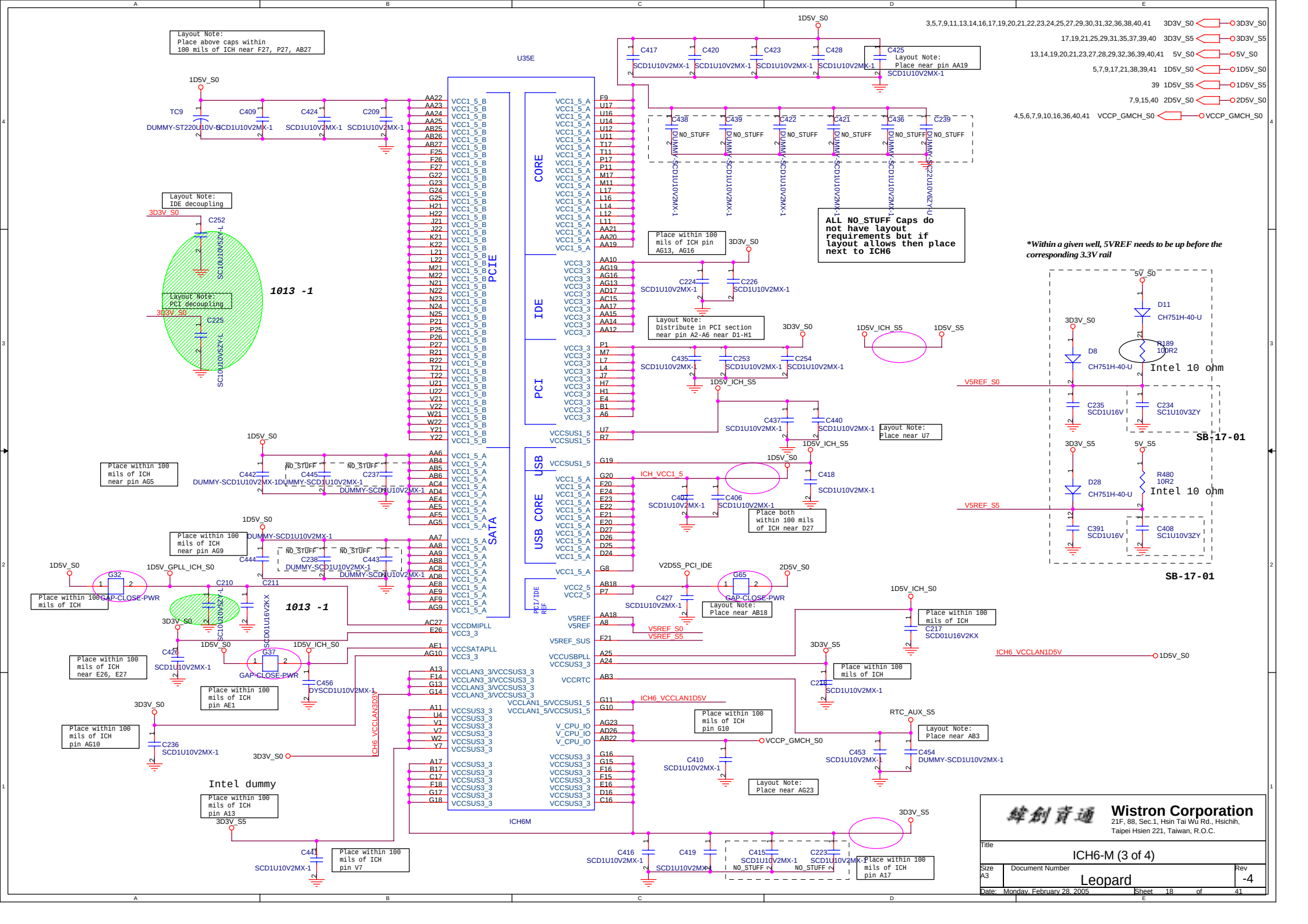
Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27
U35E
PCIE
SATA
CORE
IDE
PCI
USB
USB CORE
PCI/IDE REF
ICH6M
1D5V_S0
3D3V_S0
3D3V_S5
5V_S0
5V_S5
2D5V_S0
1D5V_ICH_S5
1D5V_ICH_S0
1D5V_S5
1D5V_GPLL_ICH_S0
V2D5S_PCI_IDE
VCCP_GMCH_S0
RTC_AUX_S5
ICH6_VCCLAN1D5V
ICH6_VCCLAN3D3V
V5REF_S0
V5REF_S5
3,5,7,9,11,13,14,16,17,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V_S0
17,19,21,25,29,31,35,37,39,40 3D3V_S5
13,14,19,20,21,23,27,28,29,32,36,39,40,41 5V_S0
5,7,9,17,21,38,39,41 1D5V_S0
39 1D5V_S5
7,9,15,40 2D5V_S0
4,5,6,7,9,10,16,36,40,41 VCCP_GMCH_S0
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Intel 10 ohm
SB-17-01
Intel dummy
1013 -1
Wistron Corporation
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Title
ICH6-M (3 of 4)
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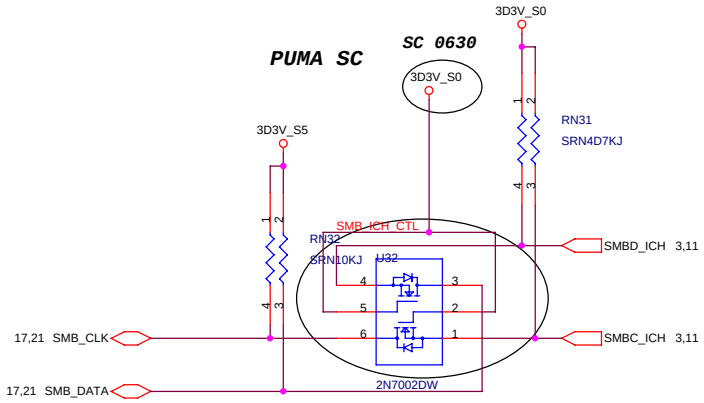
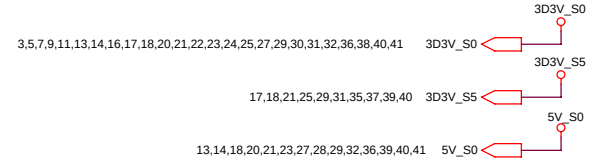
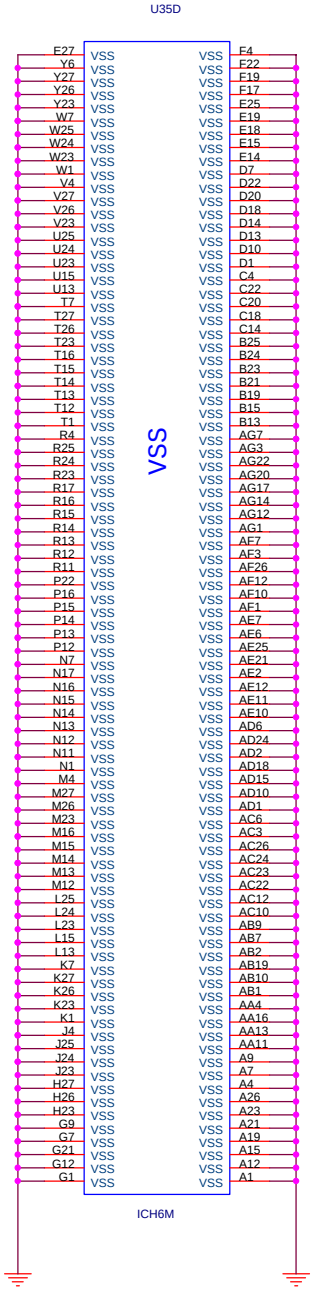
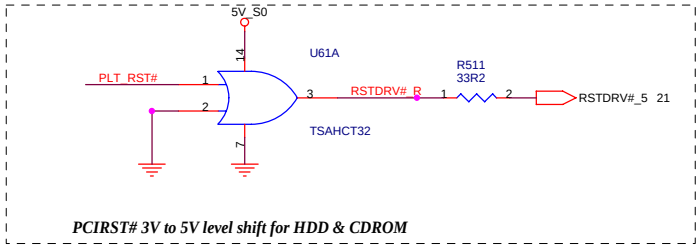
SMBUS(ICH6 ---> SODIMM,CLKGEN)



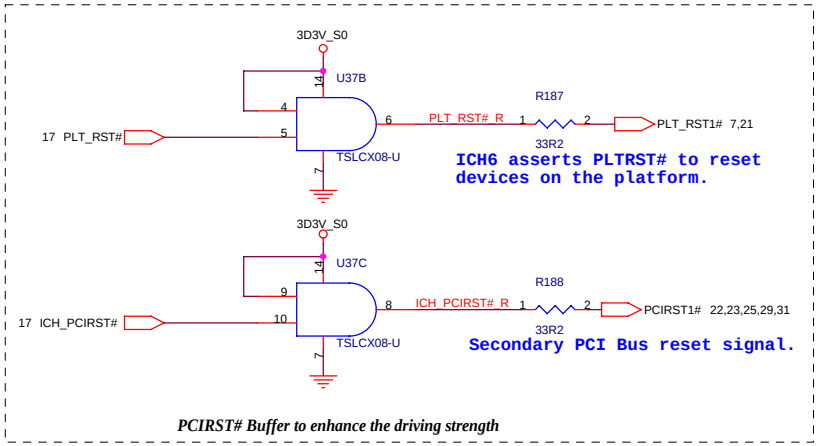




PUMA SC



PCIRST# 3V to 5V level shift for HDD & CDROM



PCIRST# Buffer to enhance the driving strength

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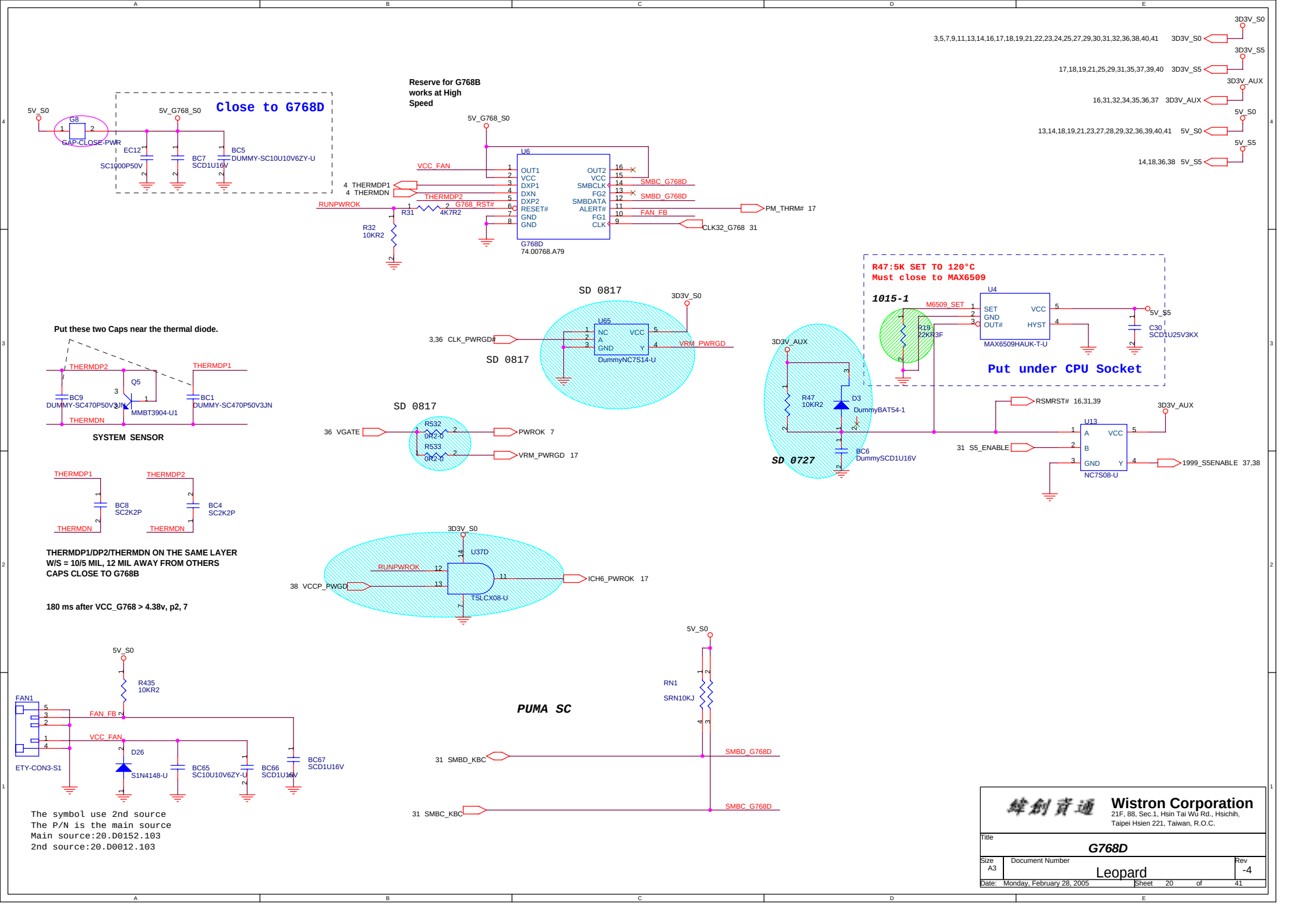
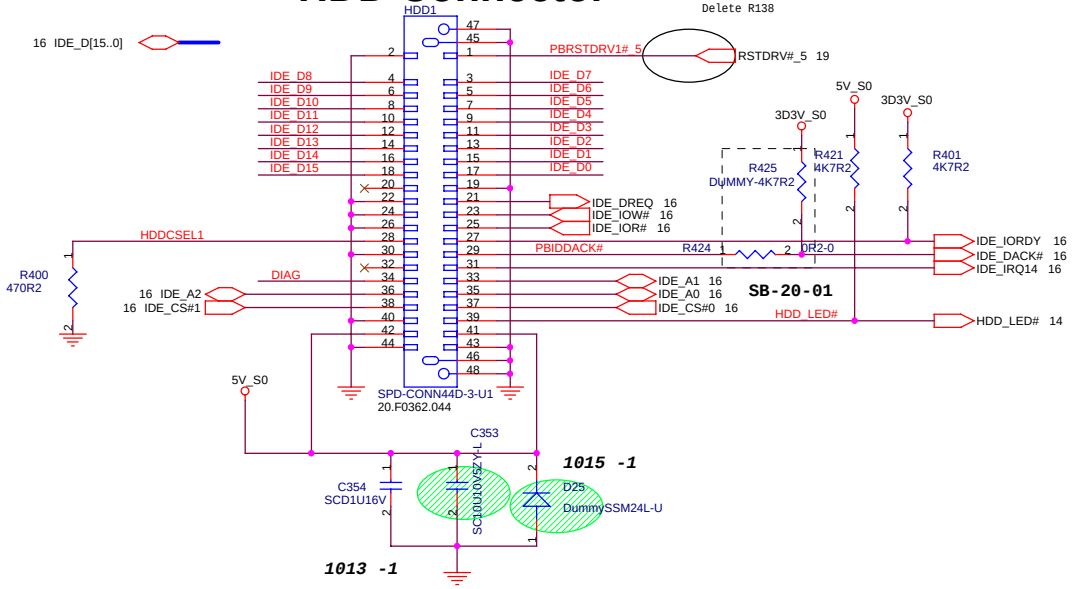
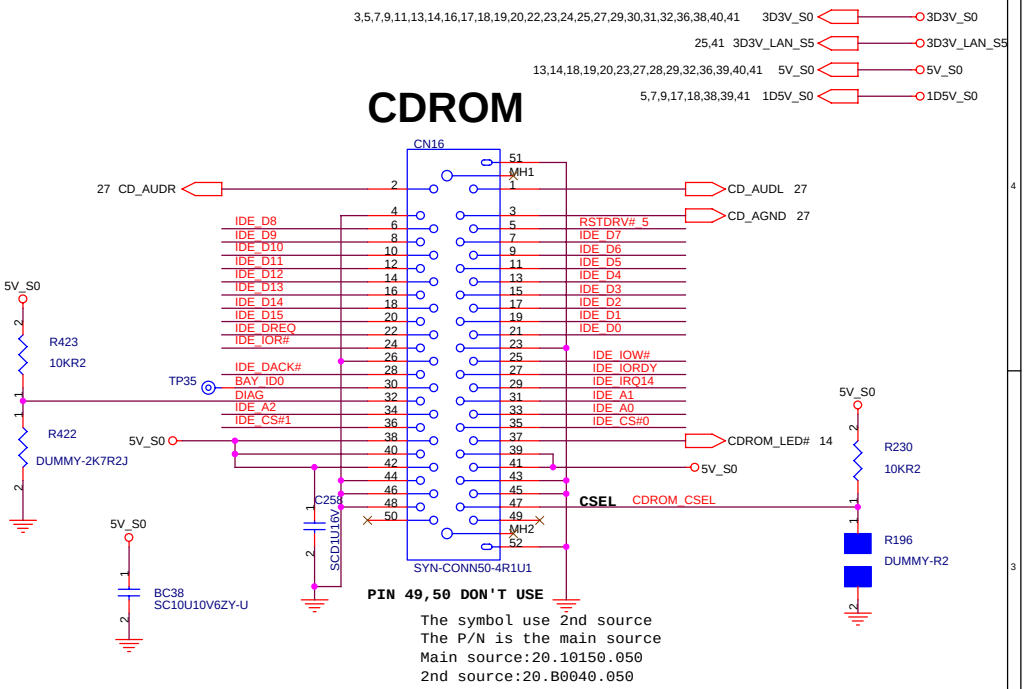

Close to G768D
5V_S0
5V_G768_S0
G8
GAP-CLOSE-PWR
EC12
SC1000P50V
BC7
SCD1U16V
BC5
DUMMY-SC10U10V6ZY-U
Reserve for G768B
works at High
Speed
5V_G768_S0
U6
VCC_FAN
4 THERMDP1
4 THERMDN
THERMDP2
RUNPWROK
R31
4K7R2
G768_RST#
R32
10KR2
OUT1
VCC
DXP1
DXN
DXP2
RESET#
GND
GND
OUT2
VCC
SMBCLK
FG2
SMBDATA
ALERT#
FG1
CLK
SMBC_G768D
SMBD_G768D
FAN_FB
PM_THRM# 17
CLK32_G768 31
G768D
74.00768.A79
3D3V_S0
3,5,7,9,11,13,14,16,17,18,19,21,22,23,24,25,27,29,30,31,32,36,38,40,41
3D3V_S5
17,18,19,21,25,29,31,35,37,39,40
3D3V_AUX
16,31,32,34,35,36,37
5V_S0
13,14,18,19,21,23,27,28,29,32,36,39,40,41
5V_S5
14,18,36,38
Put these two Caps near the thermal diode.
THERMDP2
THERMDP1
Q5
BC9
DUMMY-SC470P50V3JN
MMBT3904-U1
BC1
DUMMY-SC470P50V3JN
THERMDN
SYSTEM SENSOR
THERMDP1
THERMDP2
BC8
SC2K2P
BC4
SC2K2P
THERMDN
THERMDN
THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B
180 ms after VCC_G768 > 4.38v, p2, 7
SD 0817
3D3V_S0
3,36 CLK_PWRGD#
U65
NC
A
GND
VCC
Y
VRM_PWRGD
DummyNC7S14-U
SD 0817
SD 0817
36 VGATE
R532
0R2-0
R533
0R2-0
PWROK 7
VRM_PWRGD 17
3D3V_S0
U37D
RUNPWROK
38 VCCP_PWGD
TSLCX08-U
ICH6_PWROK 17
R47:5K SET TO 120°C
Must close to MAX6509
1015-1
U4
M6509_SET
SET
GND
OUT#
VCC
HYST
MAX6509HAUK-T-U
R19
22KR3F
5V_S5
C30
SCD1U25V3KX
Put under CPU Socket
3D3V_AUX
R47
10KR2
D3
DummyBAT54-1
BC6
DummySCD1U16V
SD 0727
RSMRST# 16,31,39
3D3V_AUX
U13
A
B
GND
VCC
Y
NC7S08-U
31 S5_ENABLE
1999_S5ENABLE 37,38
5V_S0
R435
10KR2
FAN1
FAN_FB
VCC_FAN
D26
S1N4148-U
BC65
SC10U10V6ZY-U
BC66
SCD1U16V
BC67
SCD1U16V
ETY-CON3-S1
PUMA SC
5V_S0
RN1
SRN10KJ
31 SMBD_KBC
SMBD_G768D
31 SMBC_KBC
SMBC_G768D
The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103
鋒創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G768D
Size
A3
Document Number
Leopard
Rev
-4
Date: Monday, February 28, 2005
Sheet 20 of 41

HDD Connector

SC 0712
Delete R138



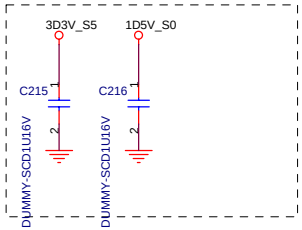
CDROM



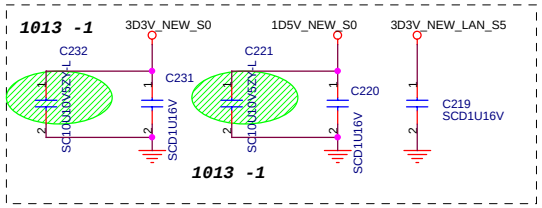
The symbol use 2nd source
The P/N is the main source
Main source:20.10150.050
2nd source:20.B0040.050

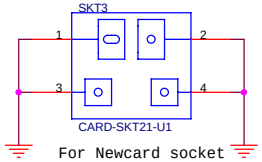
NEWCARD Connector

Place them Near to Chip



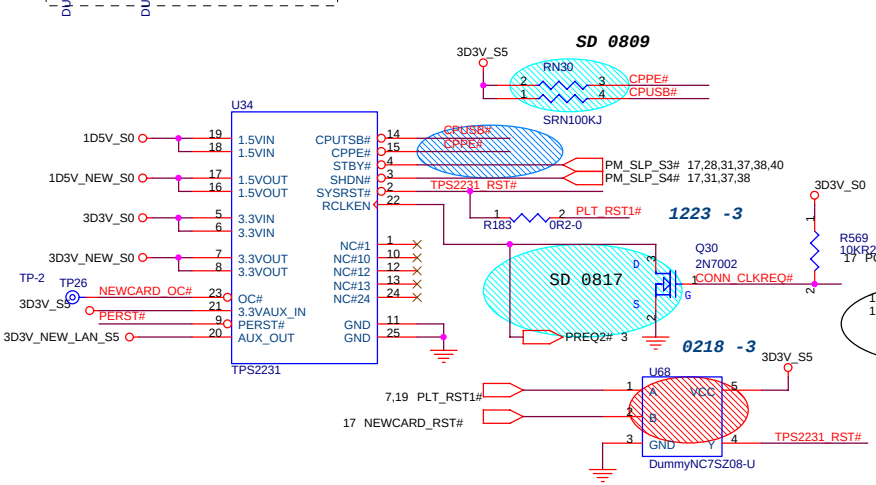
Place them Near to Connector

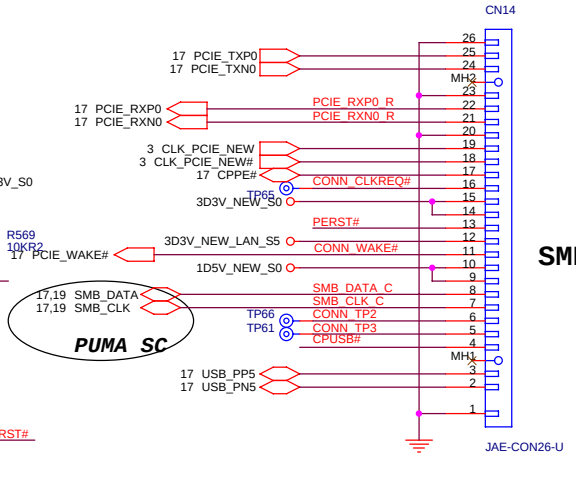




For Newcard socket

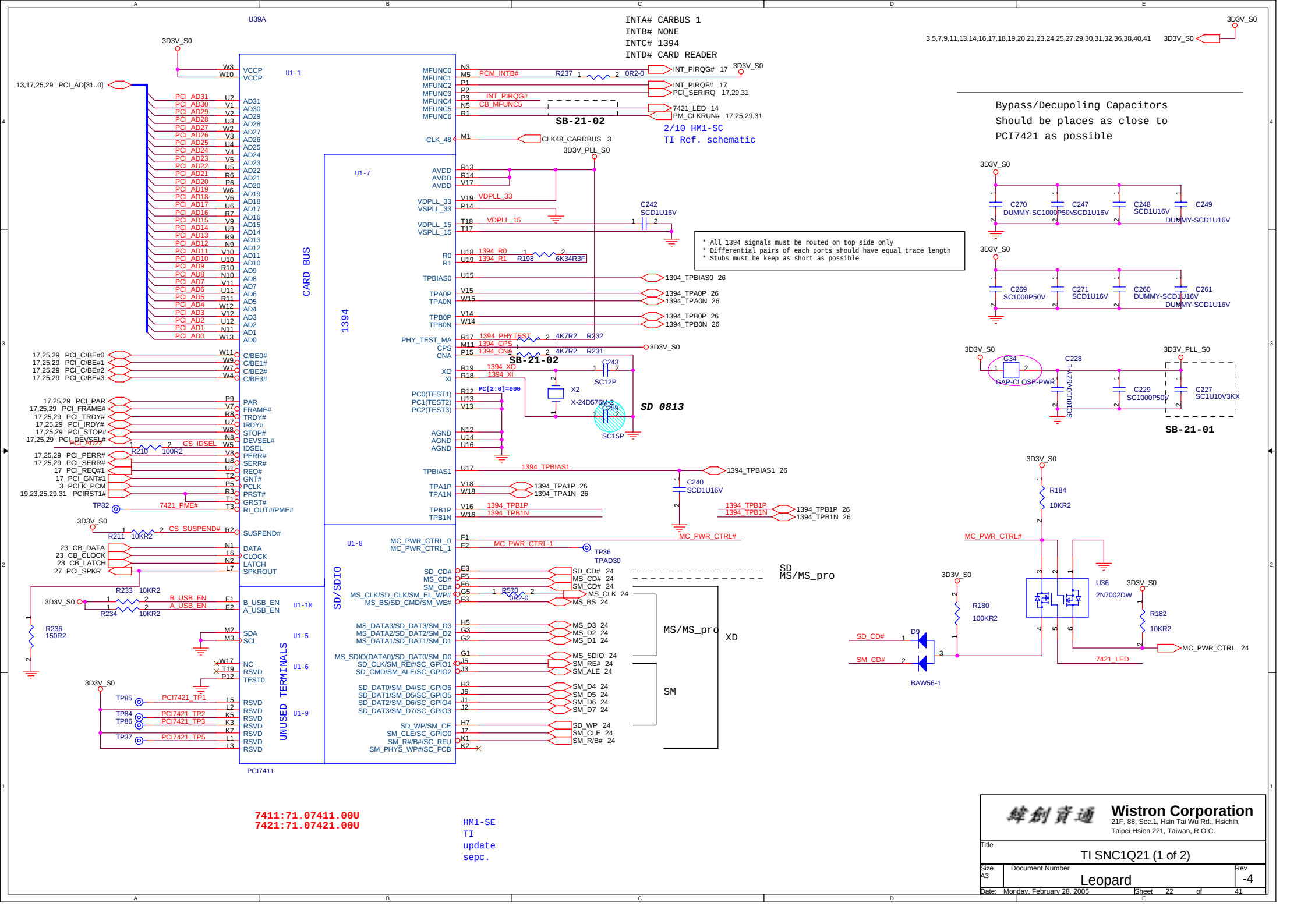
SD 0809



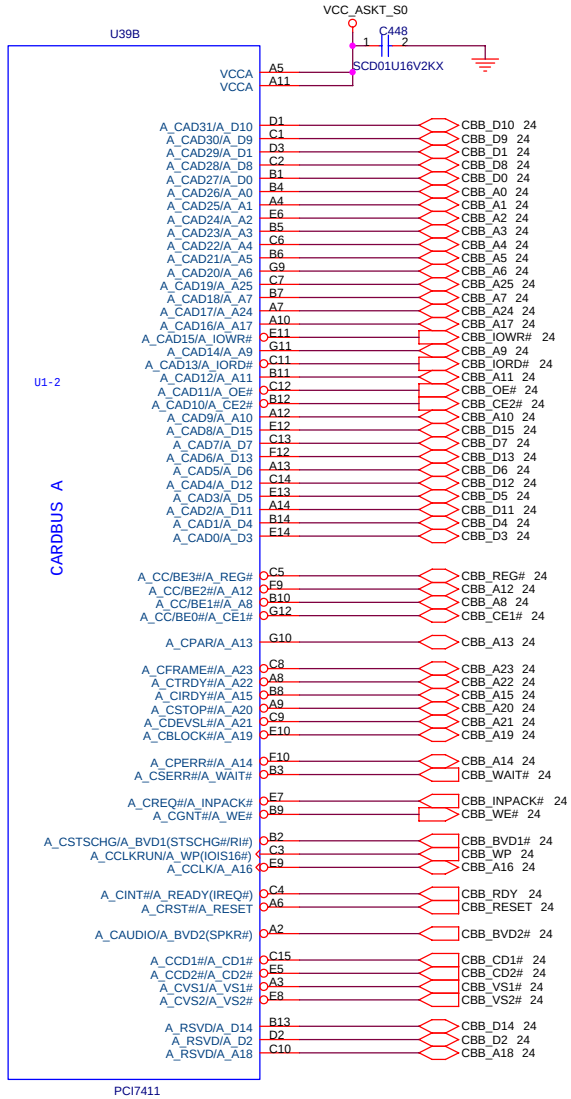


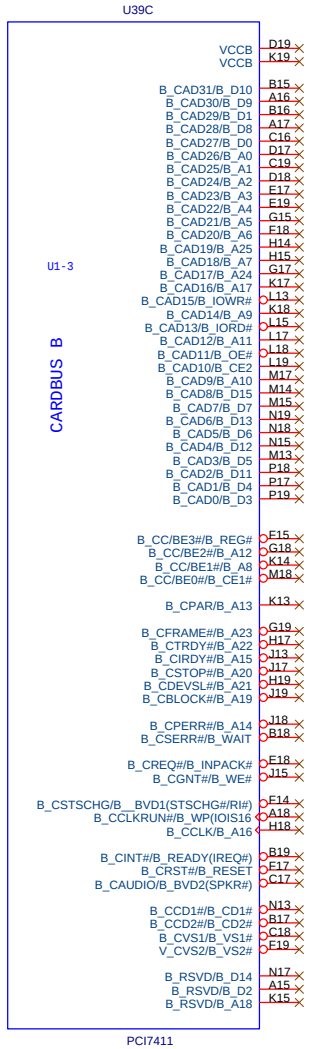
SMBUS(ICH6--NEWCARD,LAN)

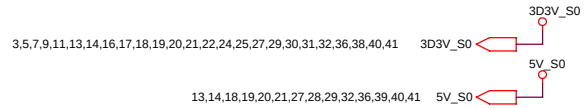
Wistron Corporation	鋒創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: HDD / CDROM/NEWCARD	
Size: A3	Document Number: Leopard
Rev: -4	
Date: Monday, February 28, 2005	Sheet 21 of 41

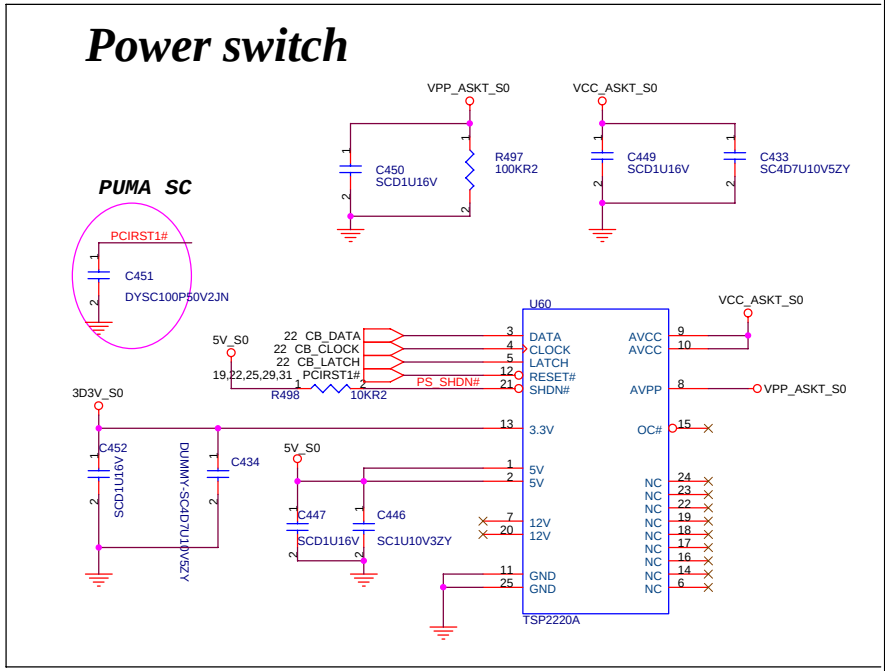


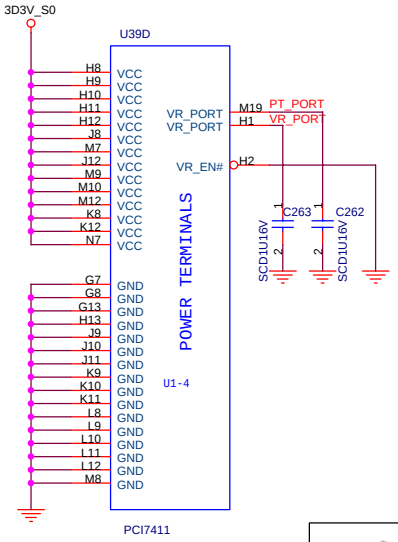
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TI SNC1Q21 (1 of 2)
Size A3	Document Number: Leopard
Rev	-4
Date: Monday, February 28, 2005	Sheet 22 of 41





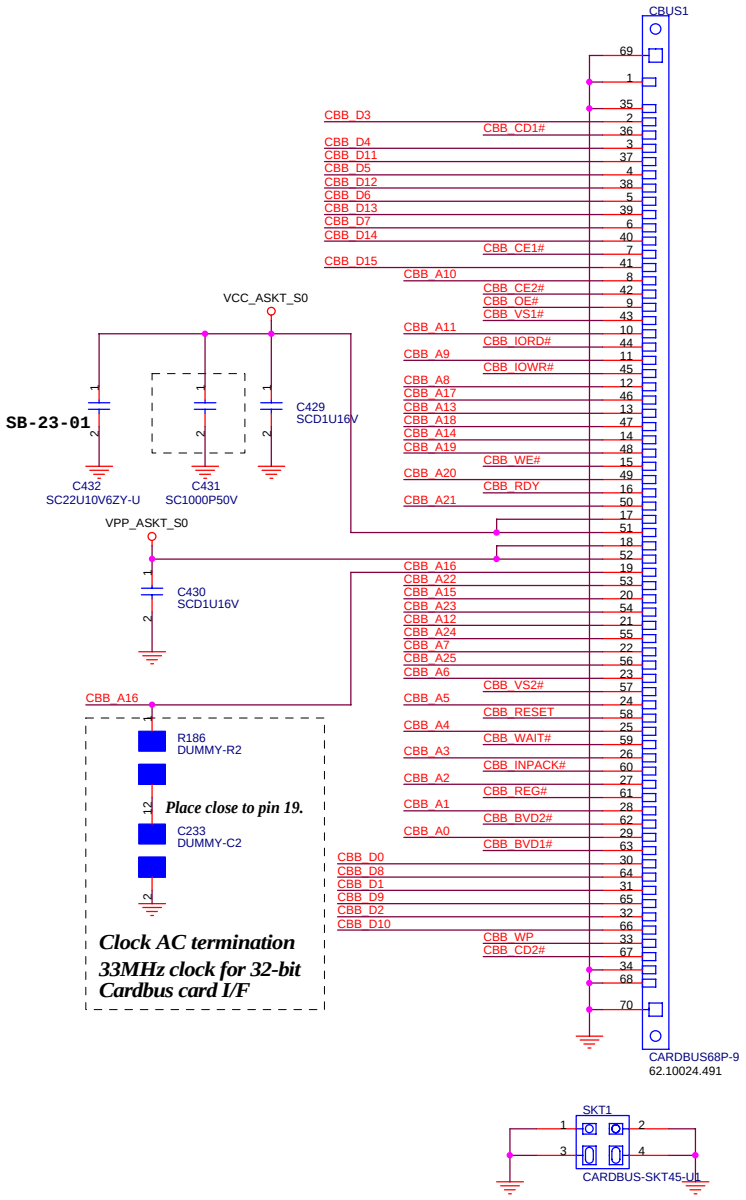






鋒創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: TI PCI7411 GHK (2 of 2)		
Size: A3	Document Number: Leopard	Rev: -4
Date: Monday, February 28, 2005	Sheet 23 of 41	

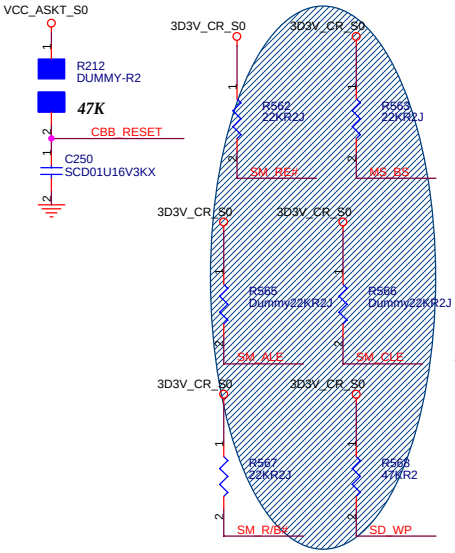
PCMCIA Socket



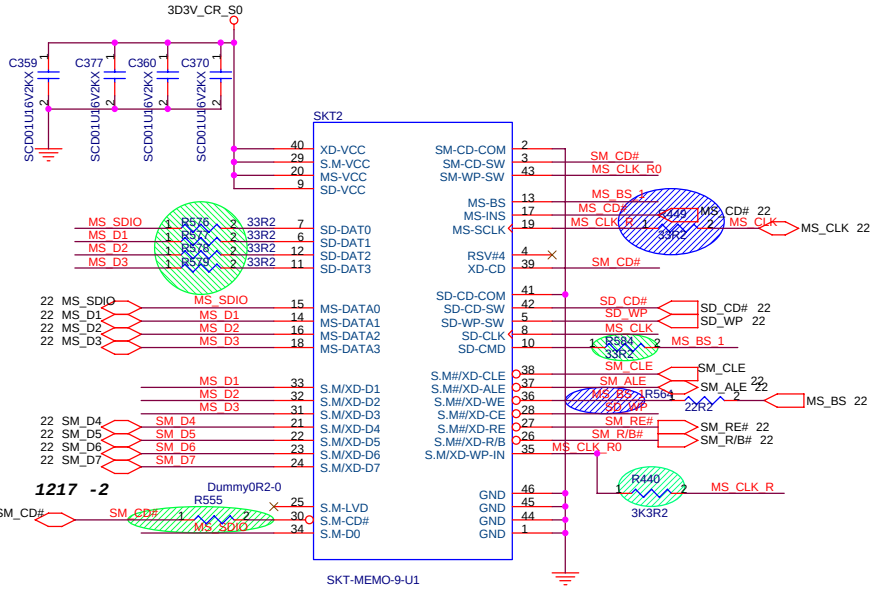
Cardbus I/F

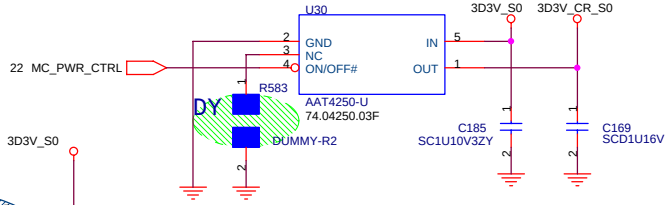
CBB_D[0..15] 23
CBB_A[0..25] 23
CBB_IORD# 23
CBB_IOWR# 23
CBB_OE# 23
CBB_WE# 23
CBB_REG# 23
CBB_RDY 23
CBB_WP 23
CBB_RESET 23
CBB_WAIT# 23
CBB_INPACK# 23
CBB_CE1# 23
CBB_CE2# 23
CBB_BVD1# 23
CBB_BVD2# 23
CBB_CD1# 23
CBB_CD2# 23
CBB_VS1# 23
CBB_VS2# 23

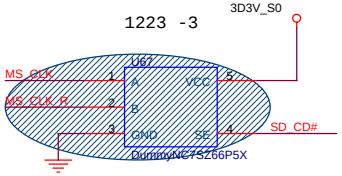
3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,25,27,29,30,31,32,36,38,40,41 3D3V_S0
14,35,37,38,39,40,41 DCBATOUT



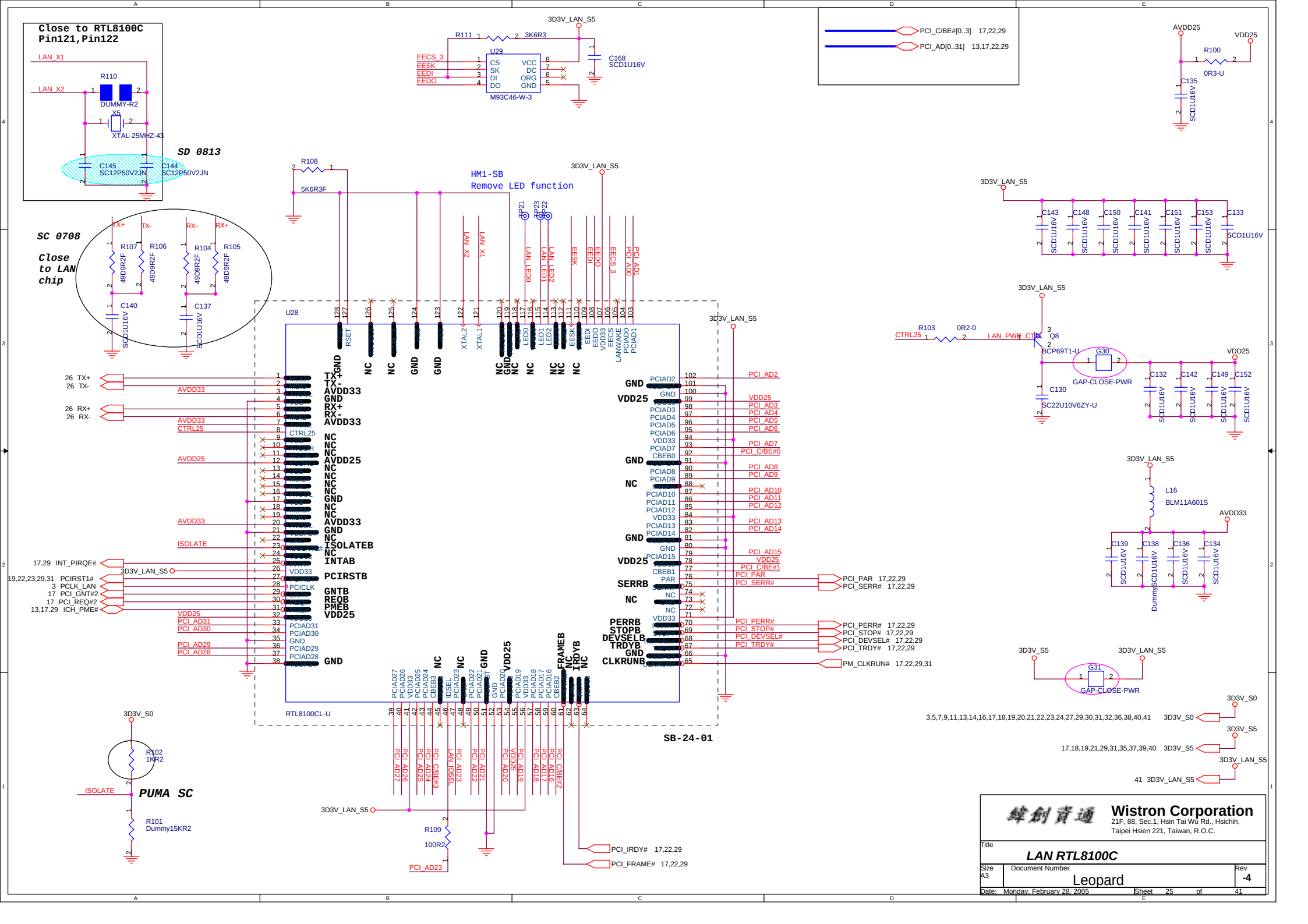
6 in 1 Connector







緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCMCIA SLOT/ CARDBUS SKT	
Size A3	Document Number Leopard	Rev -4
Date: Monday, February 28, 2005	Sheet 24 of 41	



鋒創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN RTL8100C

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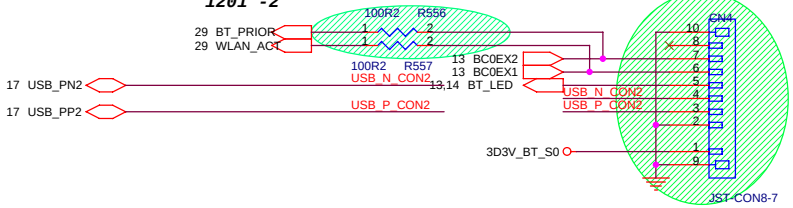
PUMA SC

Blue thumb

Place on bottom side
From NEW!

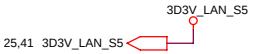
1201 -2

1004-1

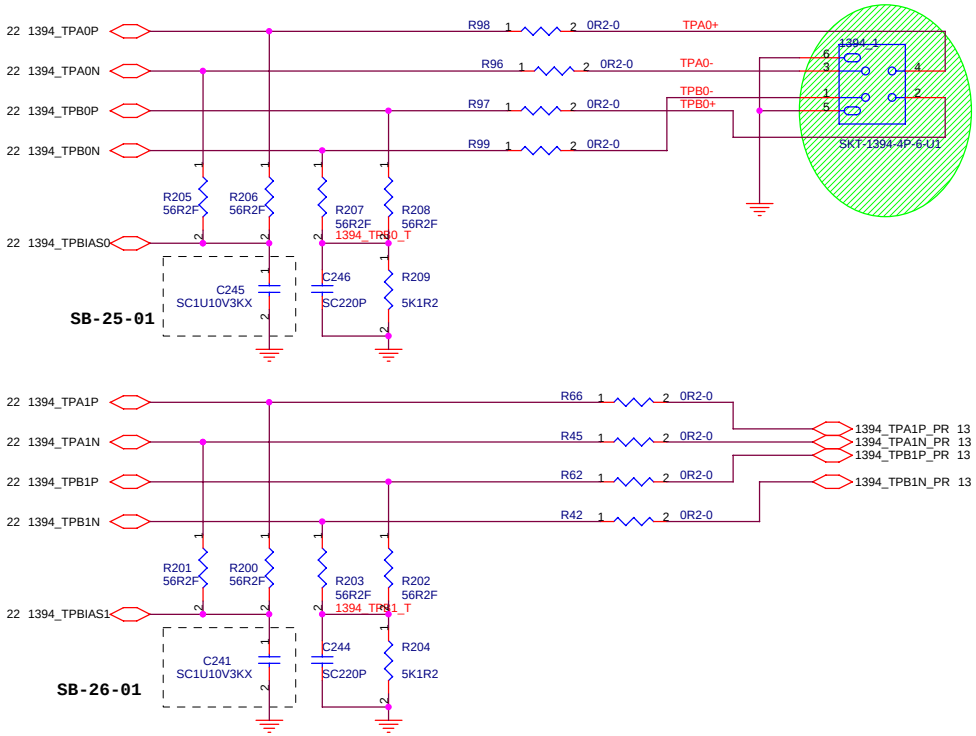


BC0EX2 connect to PCI_AD22 on main board.
BC0EX1 connect to ICH_PME# on main board.

1394 Connector

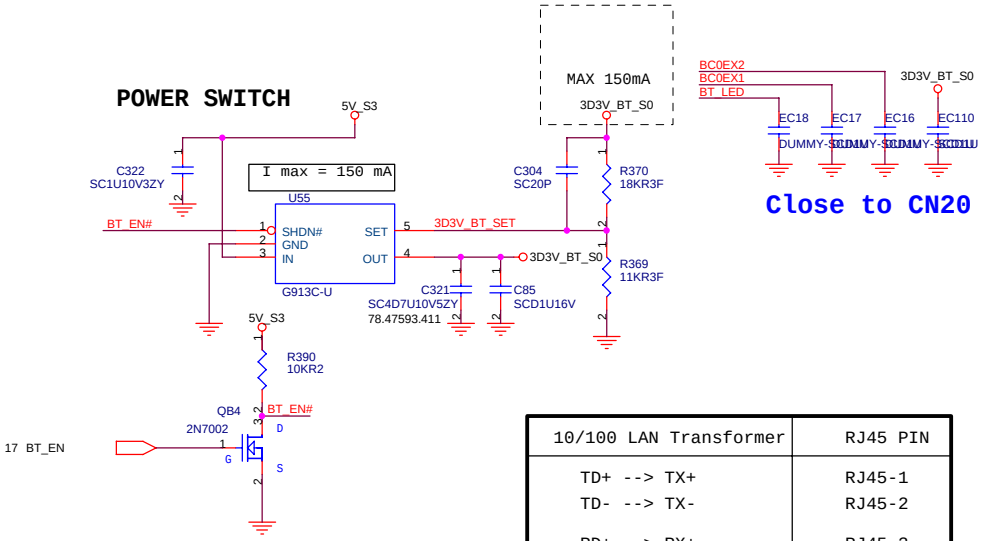


1006 -1



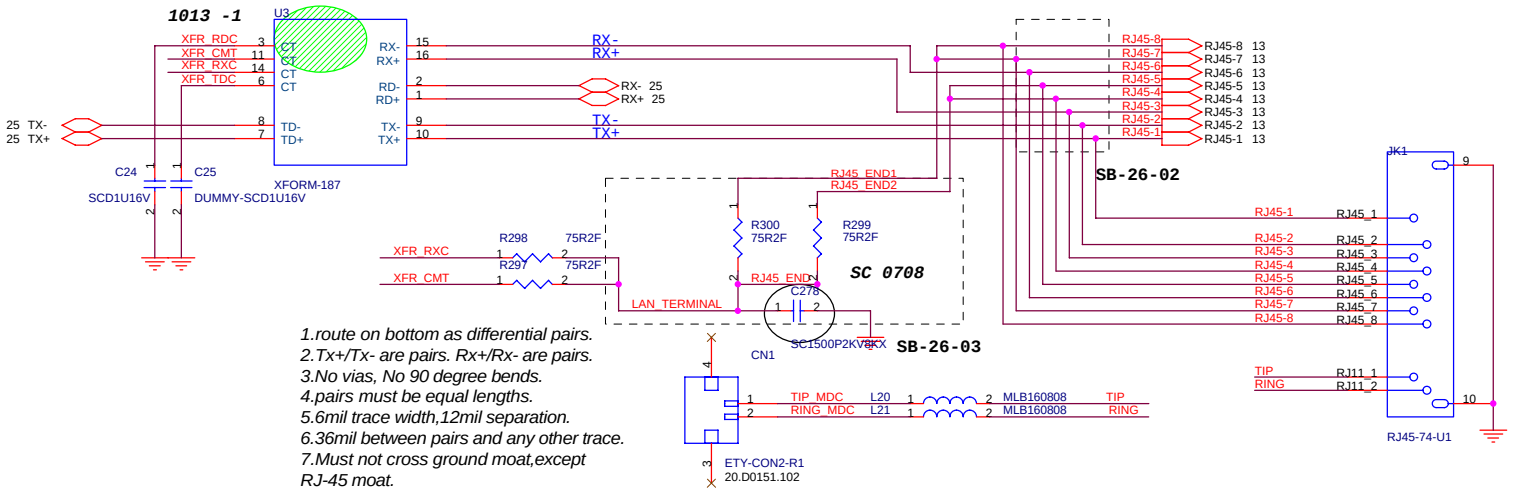
These components near to chip side.

POWER SWITCH



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

10/100M Lan Transformer



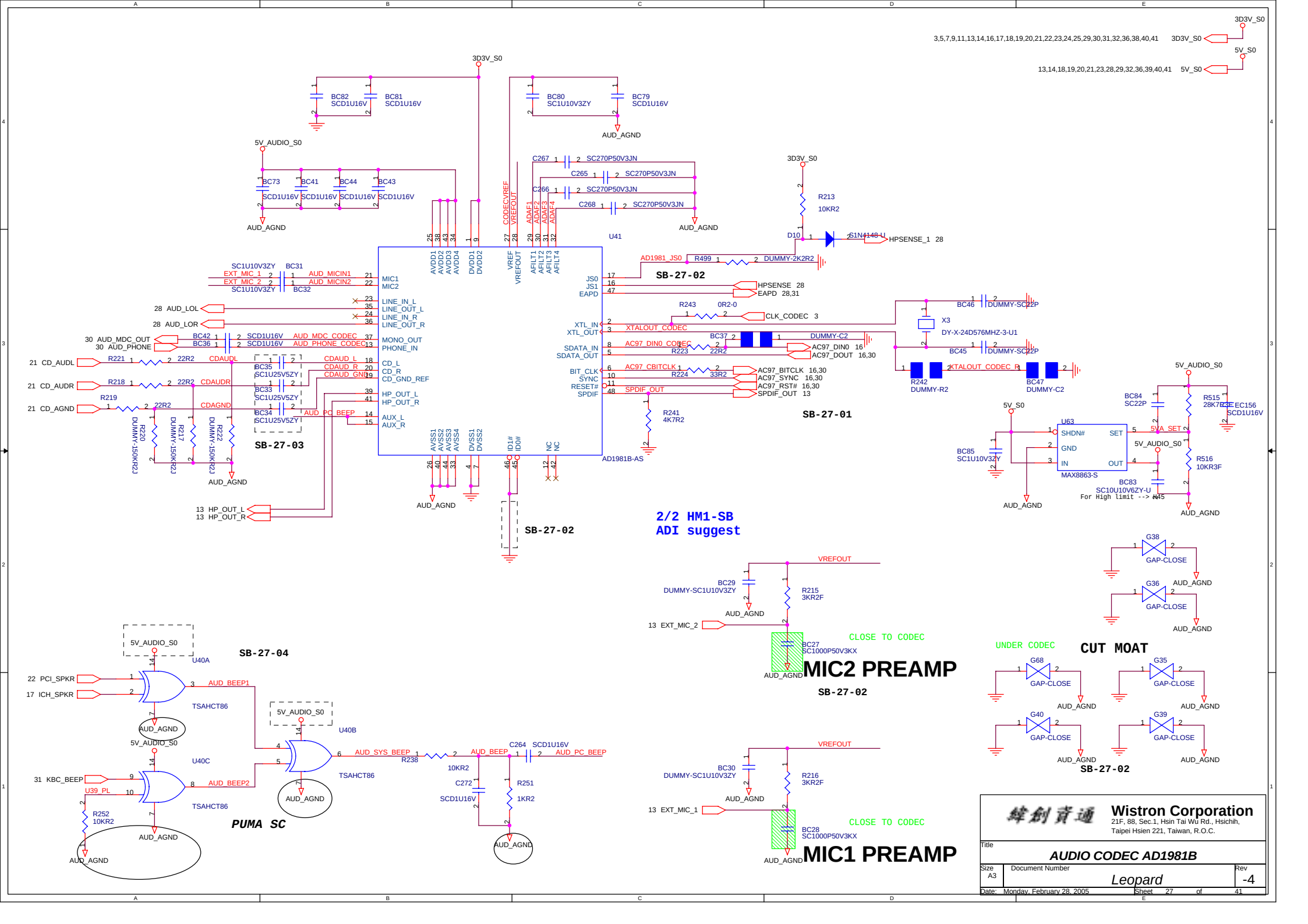
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

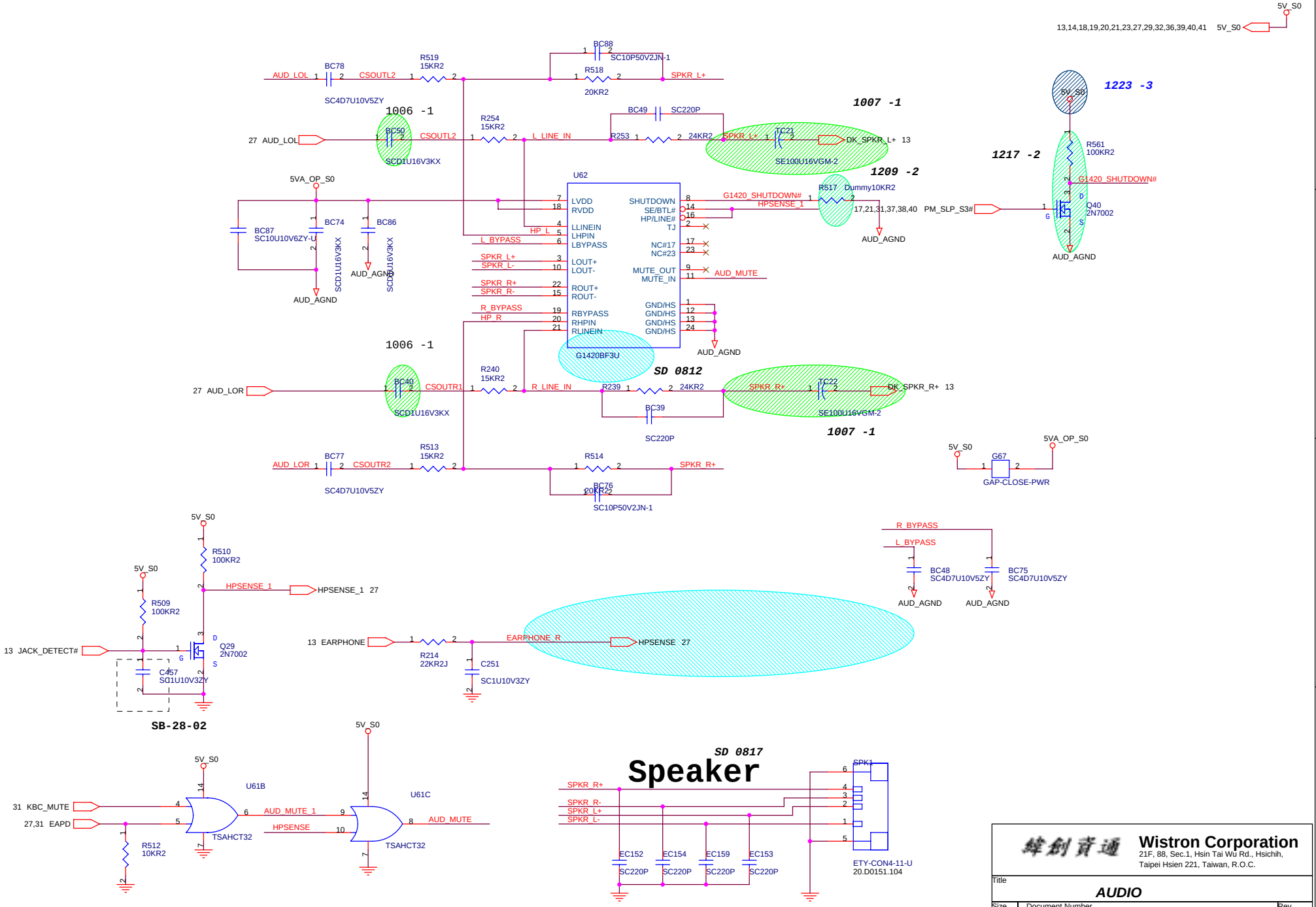
鋒創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN / 1394 Connector***

Size: A3 | Document Number: Leopard | Rev: -4

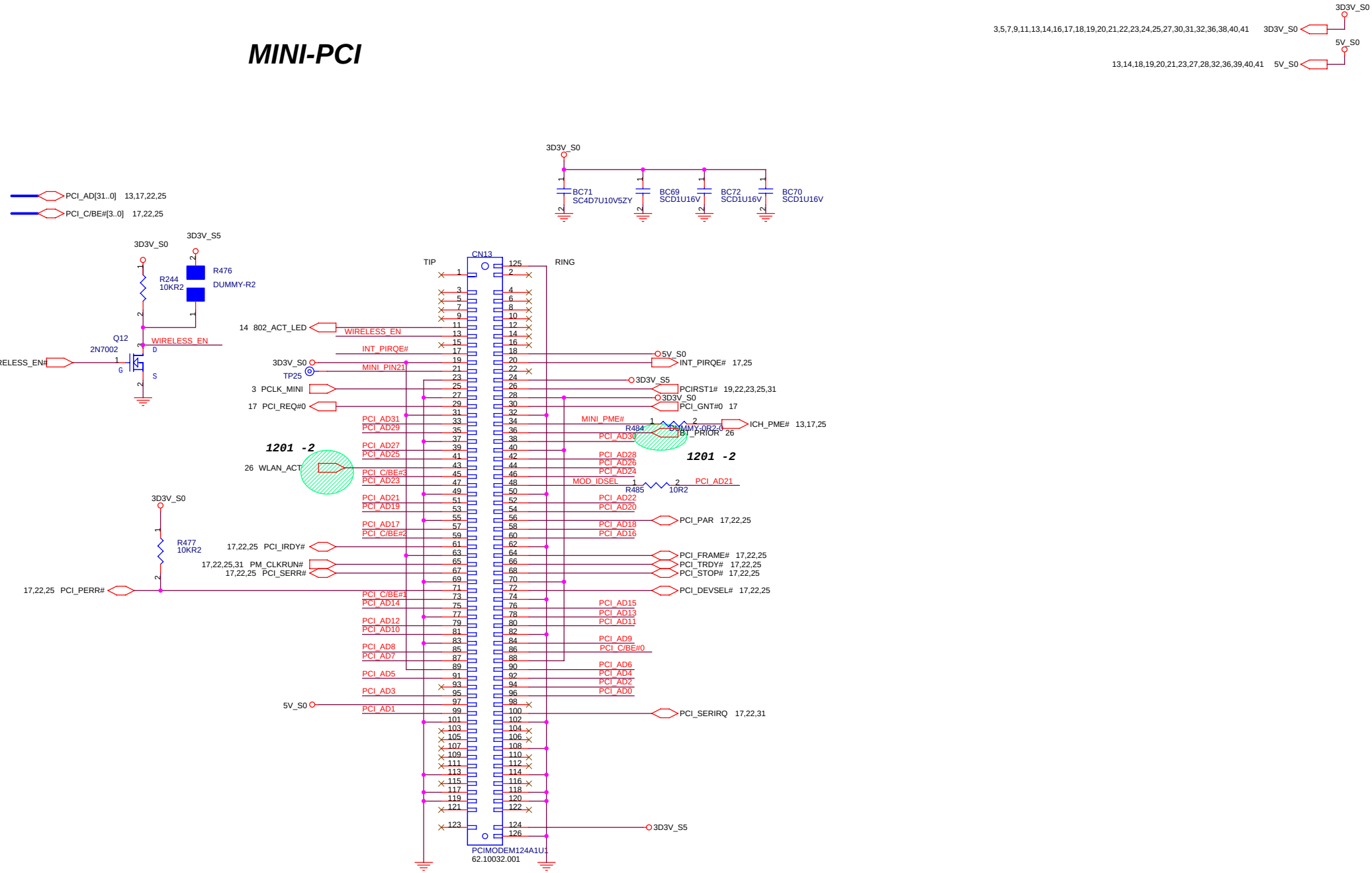
Date: Monday, February 28, 2005 | Sheet 26 of 41


3D3V_S0
5V_S0
5V_AUDIO_S0
AUD_AGND
U41
AD1981B-AS
SB-27-01
SB-27-02
SB-27-03
SB-27-04
2/2 HM1-SB
ADI suggest
MIC2 PREAMP
MIC1 PREAMP
CLOSE TO CODEC
CUT MOAT
UNDER CODEC
PUMA SC
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC AD1981B
Leopard
-4
Monday, February 28, 2005



鋒創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO***	
Size A3	Document Number Leopard	Rev -4
Date: Monday, February 28, 2005	Sheet 28 of 41	

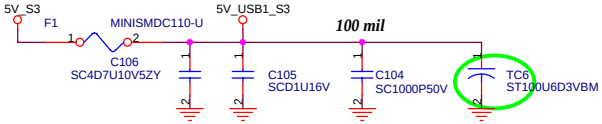
MINI-PCI

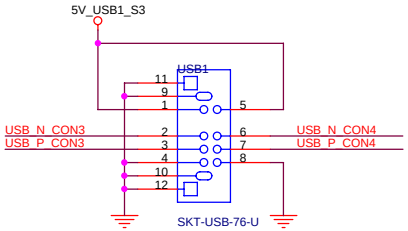


The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031

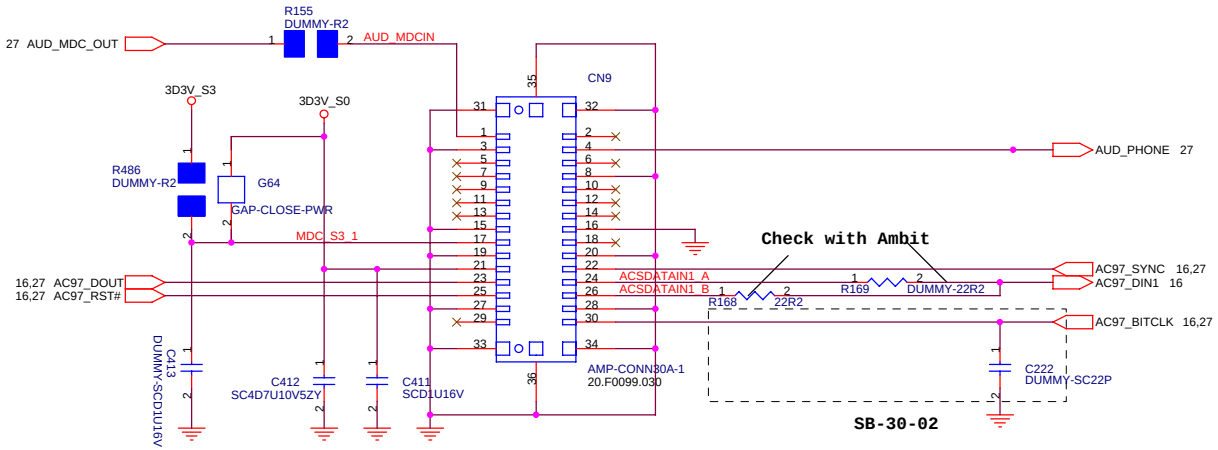
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI-PCI***	
Size A3	Document Number: Leopard	Rev: -4
Date: Monday, February 28, 2005	Sheet 29 of 41	

USB POWER





MDC Connector



Wistron Corporation
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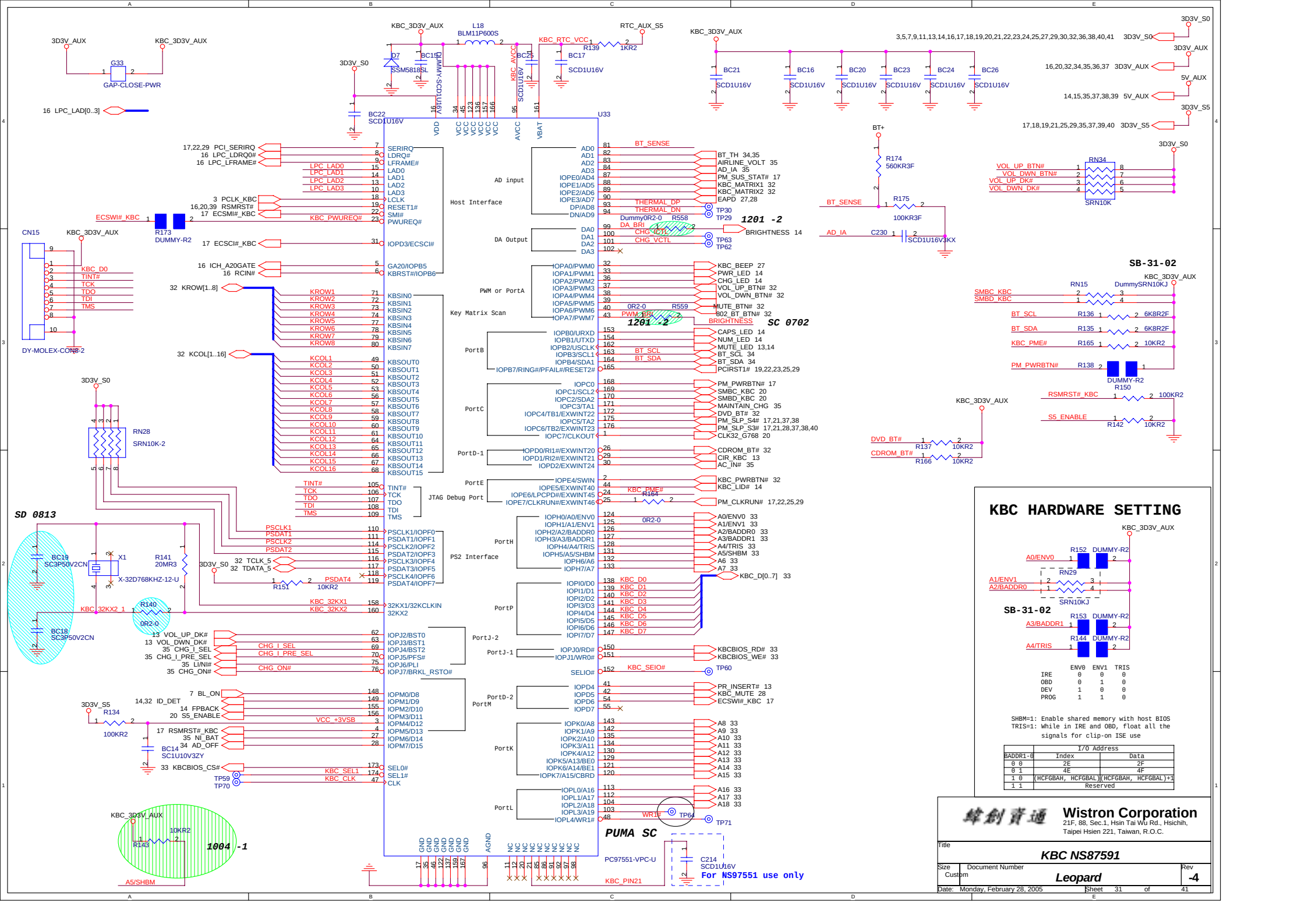
Title: ***USB / MDC CONN.***

Size: A3 | Document Number: Leopard | Rev: -4

Date: Monday, February 28, 2005 | Sheet 30 of 41


U33
PUMA SC
SD 0813
SB-31-02
SB-31-02
SC 0702
1201 -2
1201 -2
1004 -1
KBC HARDWARE SETTING
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC NS87591
Leopard
-4
Monday, February 28, 2005
Sheet 31 of 41
For NS97551 use only
SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use

INTERNAL KEYBOARD CONNECTOR

KROW[1..8] 31 KCOL[1..16] 31

CN7

ETY-CON24-1
20.K0170.001

25	1	KROW2	
	2	KROW8	
	3	KROW7	
	4	KCOL10	
	5	KROW5	
	6	KROW6	
	7	KCOL1	
	8	KROW3	
	9	KROW4	
	10	KCOL6	
	11	KCOL2	
	12	KROW1	
	13	KCOL3	
	14	KCOL5	
	15	KCOL8	
	16	KCOL9	
	17	KCOL7	
	18	KCOL4	
	19	KCOL13	
	20	KCOL14	
	21	KCOL15	
	22	KCOL12	
	23	KCOL11	
26	24	KCOL16	

3D3V_S0
R319 10KR2
802_BT_BTN#

3D3V_S0
R321 10KR2
MUTE_BTN#

KBC_3D3V_AUX
R178 dummy10KR2
R177 dummy10KR2
R179 10KR2
R176 10KR2
KBC_MATRIX2 31
KBC_MATRIX1 31

the matrix table for PCB

KBC_MATRIX2,KBC_MATRIX1

	PA	PR
FF	00	01
DF	10	11

	NONE Quick Play	Quick Play
MATRIXID1#	0	1

1012 -1

KCOL9 KCOL8 KCOL5 KCOL3
RC4 SRC150P
KROW1 KCOL2 KCOL6 KROW4
RC3 SRC150P
KCOL14 KCOL13 KCOL4 KCOL7
RC2 SRC150P
KCOL16 KCOL11 KCOL12 KCOL15
RC1 SRC150P
for EMI
KROW3 KCOL1 KROW6 KROW5
RC6 SRC150P
KCOL10 KROW7 KROW8 KROW2
RC5 SRC150P
for EMI

SB-32-01

3D3V_S0
3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,36,38,40,41 3D3V_S0
3D3V_AUX
16,20,31,34,35,36,37 3D3V_AUX
5V_S0
13,14,18,19,20,21,23,27,28,29,36,39,40,41 5V_S0

LAUNCH Board

POWER BUTTON

3D3V_AUX
R303 10KR2
31 KBC_PWRBTN#
R322 470R2
PWRBTN#
BC58 SCD1U16V
31 DVD_BT#
31 CDROM_BT#
DVD_BT#
CDROM_BT#
EC89 SC1000P16V2KX
EC88 SC1000P16V2KX

5V_S3
SCD1U10V2MX-1 C289
CN2
14 PWR_LED#
14 MUTE_LED#
14 802_BT_LED#
31 VOL_UP_BTN#
31 VOL_DWN_BTN#
31 802_BT_BTN#
14,31 ID_DET
14 NUM_LED#
31 MUTE_BTN#
5V_S0
C290 SCD1U10V2MX-1
1005-1
JST-CON20

SD 0813

3D3V_S0
D32
VOL_UP_BTN#
DummyBAV99LT1
3D3V_S0
D33
VOL_DWN_BTN#
DummyBAV99LT1

11/29 -2

SD 0813

VOL_DWN_BTN#
VOL_UP_BTN#
802_BT_LED#
MUTE_LED#
PWR_LED#
NUM_LED#
EC87 EC82 EC83 EC84 EC85 EC86
SC1000P16V2KX

TouchPad Connector

5V_S3
R433 10KR2
R434 10KR2
31 TDATA_5
31 TCLK_5
PUMA_SC 0628
CN8
BC63 DUMMY-SC47P50V2JN
BC64 DUMMY-SC47P50V2JN
BC68 DUMMY-SC1U10V8ZY
DUMMY-SCD1U16V
ETY-CON8-5
20.K0121.008

鋒創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *KEYBOARD/TOUCH PAD/Launch key*
Size: A3 | Document Number: *Leopard* | Rev: -4
Date: Monday, February 28, 2005 | Sheet 32 of 41

3D3V_S0

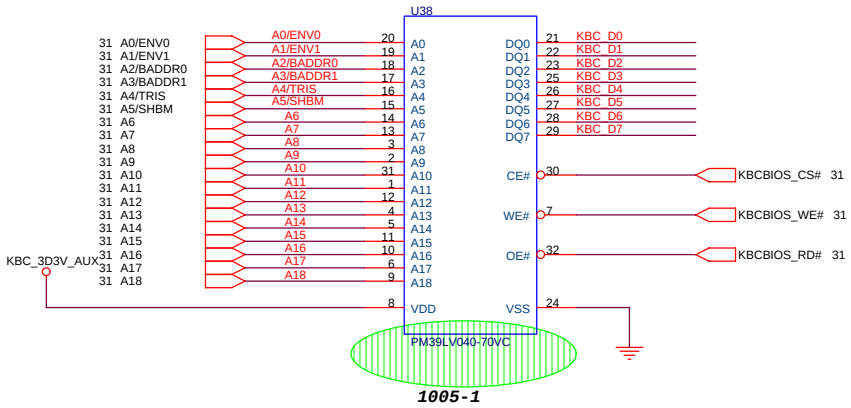
3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V_S0

5V_S0

13,14,18,19,20,21,23,27,28,29,32,36,39,40,41 5V_S0

KBC_D[0..7] 31

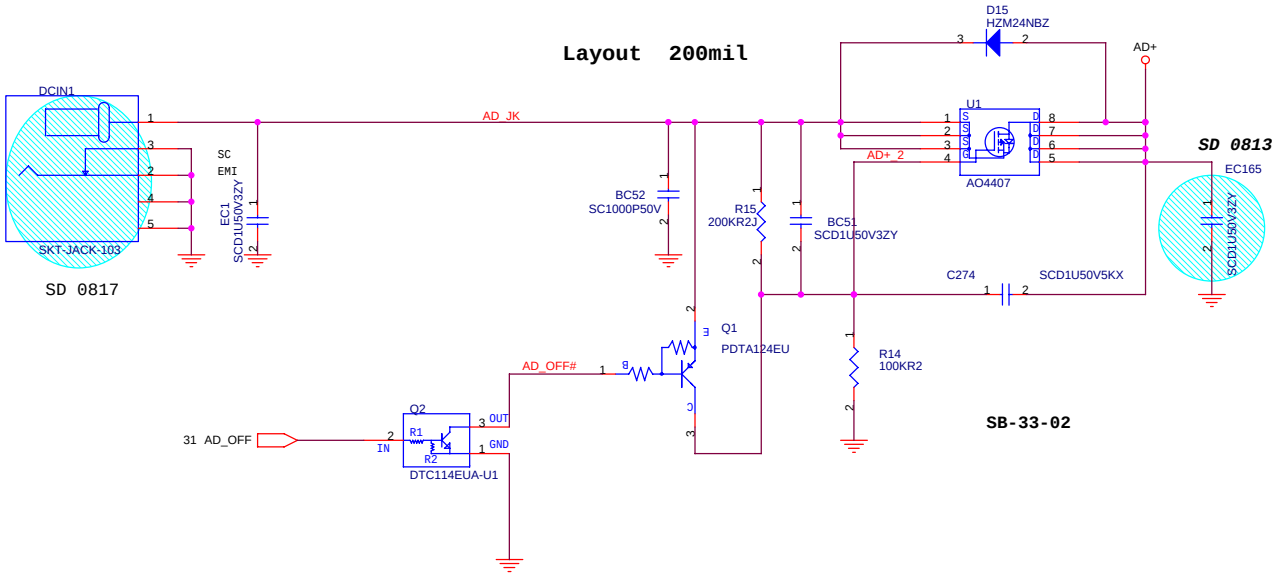
512KB Flash

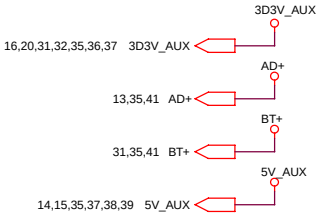


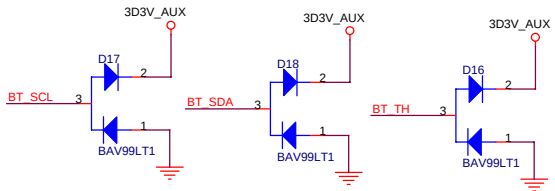
1005-1

偉創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BIOS/GF***	
Size A3	Document Number ***Leopard***	Rev ***-4***
Date: Monday, February 28, 2005	Sheet 33 of 41	

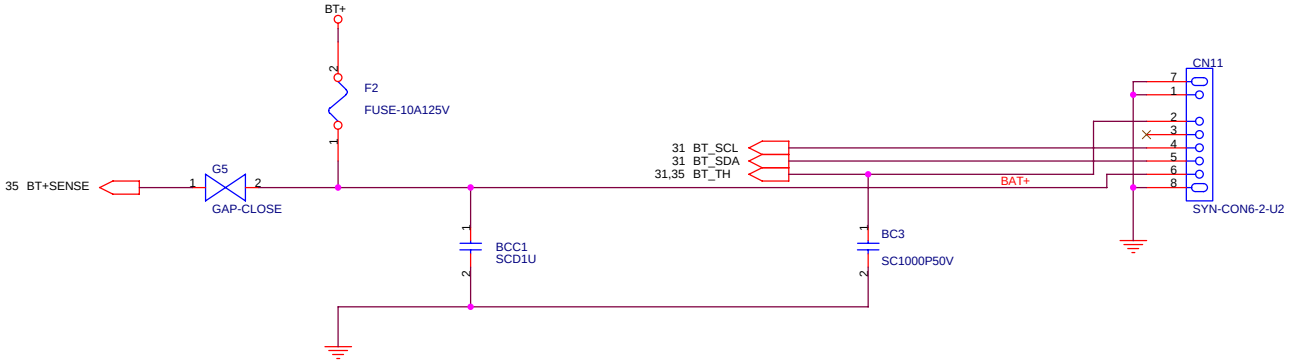
Adaptor in to generate DCBATOUT



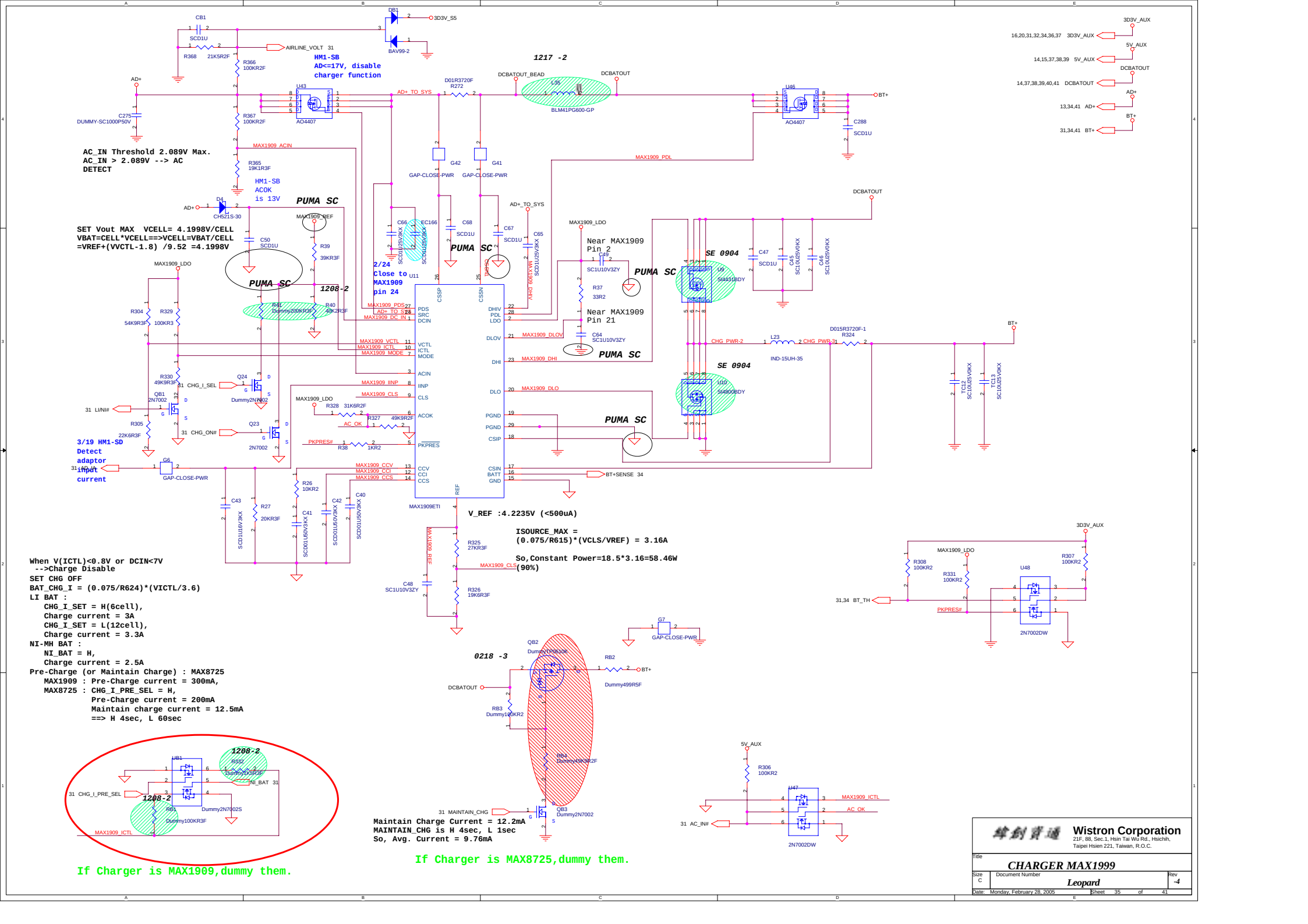




BATTERY CONNECTOR



鋒創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Adaptor/ Bettery conn.***		
Size: A3	Document Number: Leopard	Rev: -4
Date: Monday, February 28, 2005	Sheet 34 of 41	


HM1-SB
AD<=17V, disable
charger function
1217 -2
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC
DETECT
HM1-SB
ACOK
is 13V
PUMA SC
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
1208-2
2/24
Close to
MAX1909
pin 24
Near MAX1909
Pin 2
Near MAX1909
Pin 21
SE 0904
3/19 HM1-SD
Detect
adaptor
input
current
V_REF :4.2235V (<500uA)
ISOURCE_MAX =
(0.075/R615)*(VCLS/VREF) = 3.16A
So,Constant Power=18.5*3.16=58.46W
(90%)
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
SET CHG OFF
BAT_CHG_I = (0.075/R624)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3A
CHG_I_SET = L(12cell),
Charge current = 3.3A
NI-MH BAT :
NI_BAT = H,
Charge current = 2.5A
Pre-Charge (or Maintain Charge) : MAX8725
MAX1909 : Pre-Charge current = 300mA,
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 200mA
Maintain charge current = 12.5mA
==> H 4sec, L 60sec
0218 -3
Maintain Charge Current = 12.2mA
MAINTAIN_CHG is H 4sec, L 1sec
So, Avg. Current = 9.76mA
If Charger is MAX1909,dummy them.
If Charger is MAX8725,dummy them.
Wistron Corporation
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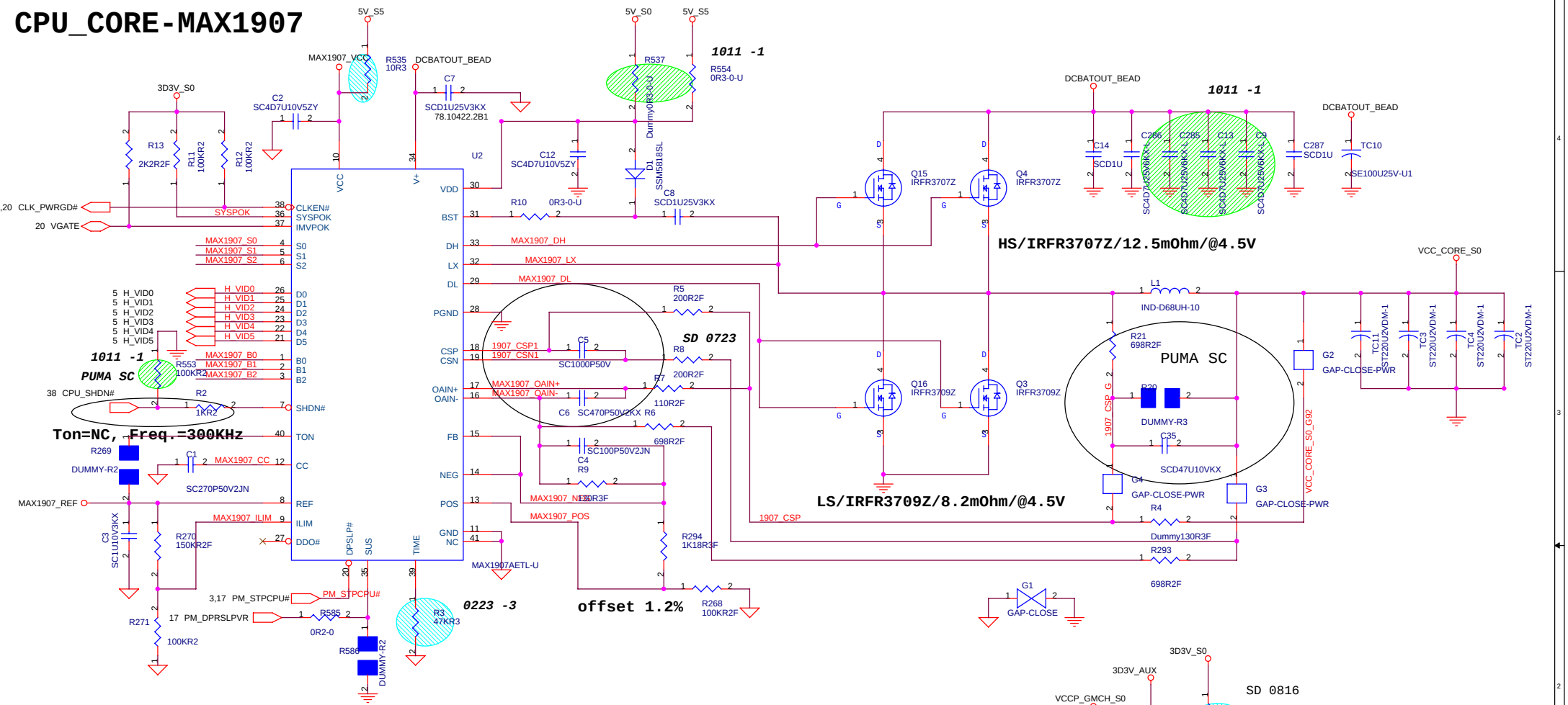
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX1999
Leopard
Monday, February 28, 2005
Sheet 35 of 41

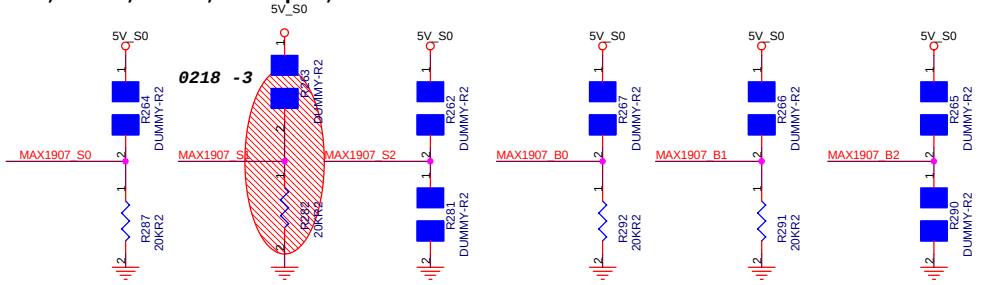
CPU_CORE-MAX1907



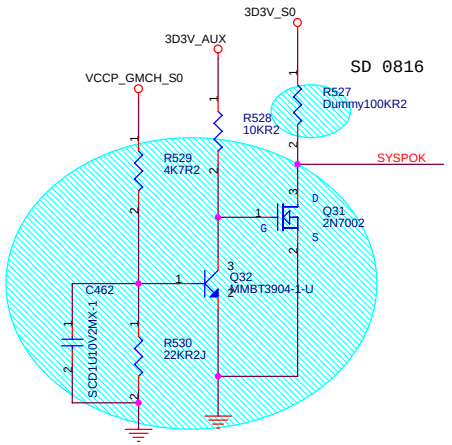
OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940



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Title: *IMVP IV-CPU POWER-MAX1907*

Size: A3 | Document Number: *Leopard* | Rev: -4

Date: Monday, February 28, 2005 | Sheet 36 of 41

SYSTEM DC/DC 3D3V_S5 / 5V_S5

3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V_S0 → 3D3V_S0
17,18,19,21,25,29,31,35,39,40 3D3V_S5 → 3D3V_S5
16,20,31,32,34,35,36 3D3V_AUX → 3D3V_AUX
14,18,20,36,38 5V_S5 → 5V_S5
14,15,35,38,39 5V_AUX → 5V_AUX
14,35,38,39,40,41 DCBATOUT → DCBATOUT

3V = 4Arms, OCP>6A

5V = 5Arms, OCP>6.8A

*Sanyo / 6*7.7 / CV-AX*

DCBATOUT
R83 4D7R5
C80 SC1U25V5ZY
C81 SCD1U
C120
C121 SCD1U
SC4D7U25V-U
5V_AUX
MAX1999_VCC
R387
47R2
C319 SC1U10V3ZY
D21 BAW56LT1
MAX1999_V+
MAX1999_BST3
MAX1999_BST5
C336 SCD1U50V3KX
R399 0R3-U
R362 0R3-U
C303 SCD1U50V3KX
CLOSE TO CMOS
U24 AO4422
U54
U16 AO4422
C82 SC4D7U25V-U
C83 SC4D7U25V-U
C98 SCD1U
3D3V_DC_S5
5V_DC_S3
L30 IND-8UH-2
L28 IND-8UH-2
MAX1999_BST3R
MAX1999_BST5R
MAX1999_DH3
MAX1999_LX3
MAX1999_DL3
MAX1999_FB3
MAX1999_ON3
MAX1999_ON5
MAX1999_SHDN#
MAX1999_DH5
MAX1999_LX5
MAX1999_DL5
MAX1999_FB5
MAX1999_PRO#
MAX1999_ILIM
U25 AO4422
U19 AO4422
Rds(on) = 24 mohm
C96 SC47P50V2JN
C79 SC47P50V2JN
R81 2MR3
R79 15K4R3
C77 SC100P50V2JN
TC14 ST150U6D3VDM-9
TC19 ST220U4VDM-L3
C78 SC100P50V2JN
R80 6K98R3F
R90 2MR3
R385 100KR2
R82 10KR3F
R78 10KR3F
These components should be located near by MAX1977
20,38 1999_S5ENABLE
17,21,31,38 PM_SLP_S4#
1KR2 R393
1KR2 R386
D6 dummy1SS400
D5 dummy1SS400
39 BL3#
MAX1999_REF
Vref = 2V
C316 SCD22U10V3KX
3V_LDO=100mA
MAX1999_LDO3
MAX1999_LDO5
5V_LDO=100mA
MAX1999EEI
R77 300KR3
R75 200KR3
G44 GAP-CLOSE-PWR
C318 SC2D2U6D3V3MX-1
R384 300KR2J
MAX1999_SKIP#
C320 SC1U10V3KX
G45 GAP-CLOSE-PWR
EC167 SCD1U25V3KX
R76 300KR3
R74 150KR3
Q26 DTC115EE-U
17,21,28,31,38,40 PM_SLP_S3#
PM_SLP_S3# high = PWM
PM_SLP_S3# low = Ultrasonic
SKIP# > 2.4V : PWM mode
SKIP# = GND(,0.8V) : SKIP MODE
SKIP# = REF (1.7V~2.3V)/FloatING
Ultrasonic MODE(25KHz min)
5V_S5 spec. = 10mA
C317 DUMMY-C2
C331 DUMMY-C2
G21 GAP-CLOSE

```
ILIM5: 5V * 200K / (200K+300K) = 2.0V
       200mV / 24 = 8.3A
        OCP point = 8.3A +1/2Iripple

ILIM3: 5V * 200K / (200K+300K) = 2.0V
       200mV / 24 = 8.3A
        OCP point = 8.3A +1/2Iripple
       OCP point = 20A +1/2Iripple
```

ILIM=Vcc 100mV*
ILIM=Vref 200mV*
OCP= 0.1Vth/Rds(on) + 0.5Iripple

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*DC/DC 3V_S5/5V_S5*	
Size A3	Document Number *Leopard*	Rev *-4*
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TI TPS5130 for 2.5V, 1.5V, 1.05V.

(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)

For 1.5V
SETTING=1.517V

SD 0811

R413 680R2
C348 SC4700P50V2KX
PWM_1D5V
SC 0722
R416 10KR3F
R410 7K87R2F
R409 3K9R2F
SD 0823
C349 SC4700P50V2KX
5130_INV1
5130_FB1

For 1.05V
SETTING=1.061V

R398 80K6R3F
R396 680R2
C333 SC5600P25V2KX
PWM_1D05V
R395 20KR2F
R397 2K7R2J
C334 SC3300P50V2KX
5130_INV3
5130_FB3

For 2.5V
SETTING=2.516V

R411 680R2
C347 SC5600P25V2KX
PWM_2D5V
R415 10K2R3F
R412 20KR2F
R414 2KR2F
SC 0722
C350 SC3300P50V2KX
5130_INV2
5130_FB2

SD 0811
5130_FLT
C116 SCD01U16V3KX

5V_AUX
R360 100KR2
U51 2N7002DW
PM_SLP_S3#
5130_SS_STBY1
SD 0812
C119 SC1500P50V3KX

5V_AUX
R359 100KR2
U50 2N7002DW
PM_SLP_S4# 17,21,31,37
5130_SS_STBY2
C118 SC4700P50V3KX

5V_AUX
R361 100KR2
U53 2N7002DW
PM_SLP_S3#
5130_SS_STBY3
SD 0812
C335 SC1500P50V3KX

5130_FB1
5130_SS_STBY1
5130_INV2
5130_FB2
5130_SS_STBY2
5130_PWM_SEL
5130_CT
5130_REF
STBY_REF
R392 1KR3
20,37 1999_S5ENABLE

TPS5130

FB1
SS_STBY1
INV2
FB2
SS_STBY2
PWM_SEL
CT
GND
REF
STBY_VREF5
STBY_VREF3.3
STBY_LDO

INV1 FLT LH1 OUT1_U LL1 OUT1_D OUTGND1 TRIP1 VIN_SENSE12 TRIP2 OUTGND2 OUT2_D
U23

LL2
OUT2_U
LH2
VIN
VREF3.3
VREF5
REG5V_IN
LDO_IN
LDO_CUR
LDO_GATE
LDO_OUT
INV_LDO

SS_STBY3 FB3 INV3 PGOUT PG_DELAY TRIP3 VIN_SENSE3 LH3 OUT3_U LL3 OUT3_D OUTGND3
TPS5130PT-U

5130_CT
C117 SC47P50V2JN
5130_REF
C97 SCD1U16V3KX

5130_SS_STBY3
5130_FB3
5130_INV3

5V_DC_S5
D24 BAW56 83.00056.A11
5130_LH1
C115 SCD1U50V5KX
5130_LL1
5130_LL1 39
5130_OUT1U
5130_OUT1D
5130_OUT1U 39
5130_OUT1D 39
5130_TRIP1
5130_TRIP2
DCBATOUT
5130_OUT2D
5130_OUT2D 39
5130_FLT
5130_INV1

5130_LH2
C114 SCD1U50V5KX
5130_LL2
5130_LL2 39
close to IC

DCBATOUT
C344 SCD1U
5130_OUT2U
5130_OUT2U 39
5V_DC_S5
5V_S5
G52 GAP-CLOSE-PWR
C93 SC4D7U10V5ZY

R552 0R2-0
1006 -1
C463 SCD1U
5V_S3

For 1.5V
SETTING=1.505V

C95 SC1000P25V
5130_OUT3D
5130_LL3
5130_OUT3U
5130_OUT3D 39
5130_OUT3U 39
5130_LH3
C94 SCD1U50V5KX
5130_LL3 39
5V_DC_S5
D23 BAT54-1
DCBATOUT

SD 0820
3D3V_S0
R170 10KR2
20 VCCP_PWGD
PM_SLP_S3#
5130_TRIP3
3D3V_S0
U37A
TSLCX08-U
CPU_SHDN# 36

HW Thermal Throttling

OCP_1.05V
SD 0811
R408 15KR3
DCBATOUT
5130_TRIP1
C346 SCD1U16V3KX
close to IC

OCP_2.5V
R407 20KR3
DCBATOUT
5130_TRIP2
C345 SCD1U16V3KX
close to IC

OCP_1D5V
R394 20KR3
DCBATOUT
5130_TRIP3
C332 SCD1U16V3KX
close to IC

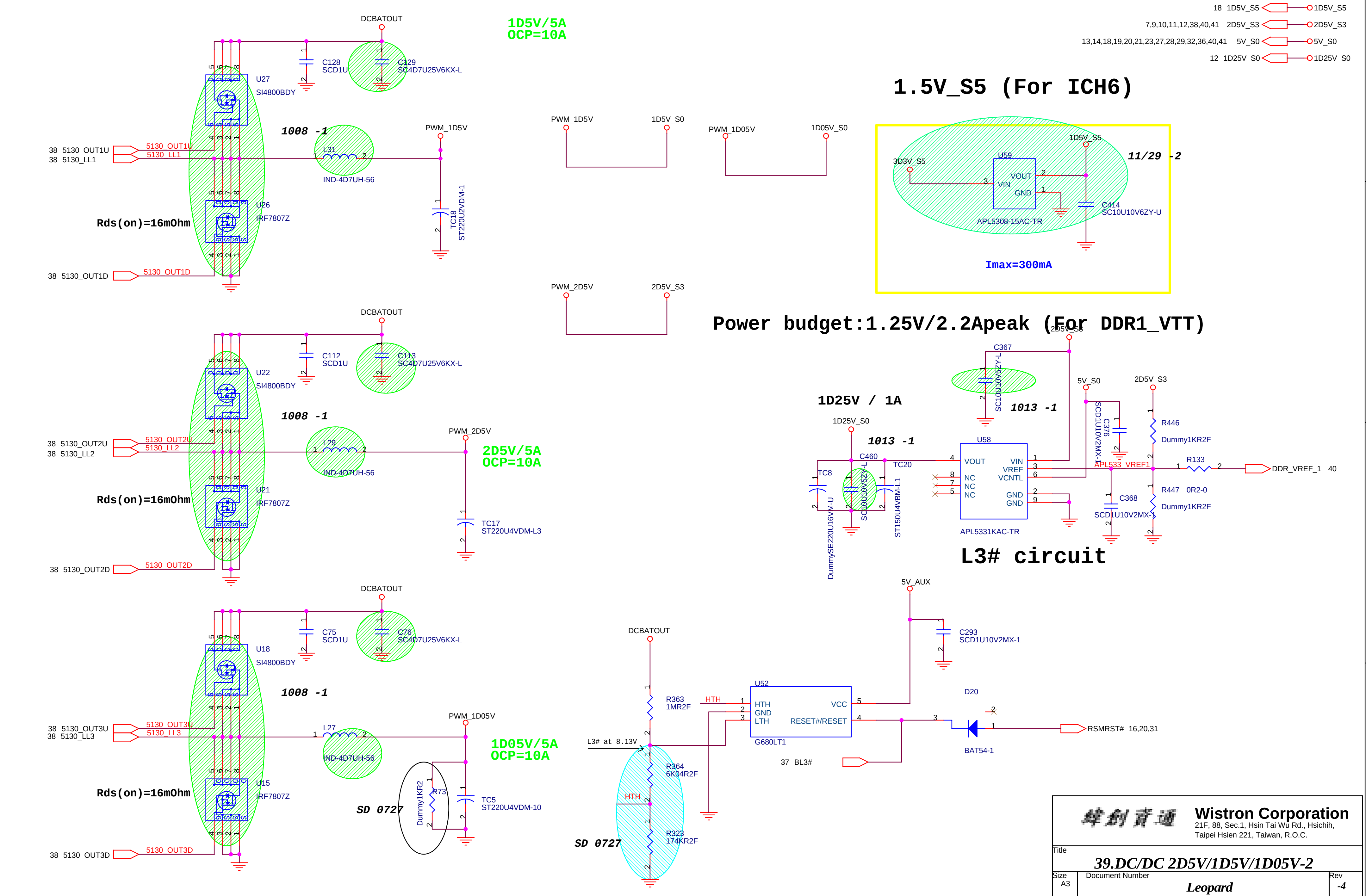
G28 GAP-CLOSE

5V_AUX
R383 300KR2J
5130_PWM_SEL
17,21,28,31,37,40 PM_SLP_S3#
Q25 DTC115EE-U
R1
R2
IN
OUT
GND

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DC/DC 2D5V/1D5V/1D05V
Size A3	Document Number Leopard
Rev	-4
Date: Monday, February 28, 2005	Sheet 38 of 41

TI TPS5130 for 2.5V, 1.5V, 1.05V

(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)



Wistron Corporation

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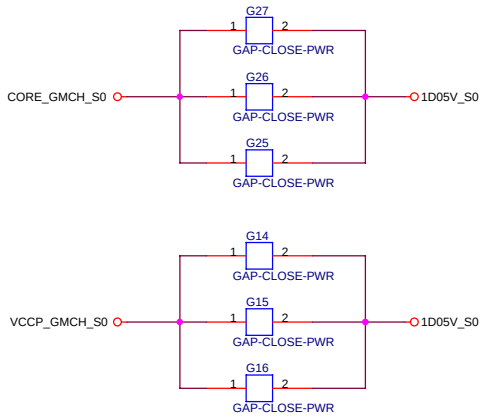
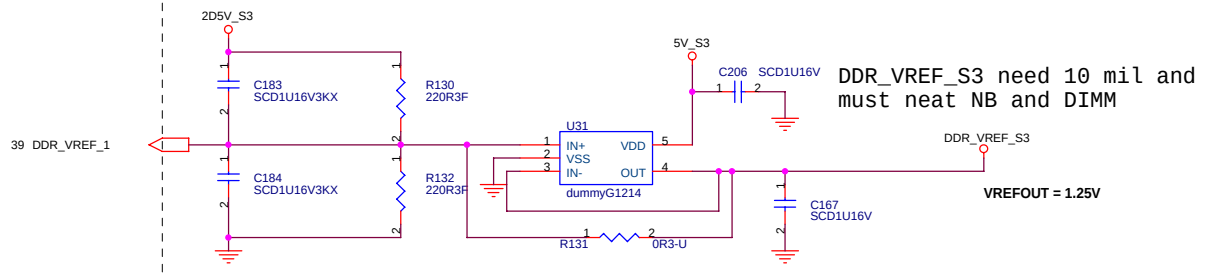
Taipei Hsien 221, Taiwan, R.O.C.

Title		
39.DC/DC 2D5V/1D5V/1D05V-2		
Size: A3	Document Number: Leopard	Rev: -4
Date: Monday, February 28, 2005	Sheet 39 of 41	

FOR GMCH Power



3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,41 3D3V_S0 — 3D3V_S0
13,14,30 3D3V_S3 — 3D3V_S3
17,18,19,21,25,29,31,35,37,39 3D3V_S5 — 3D3V_S5
13,14,18,19,20,21,23,27,28,29,32,36,39,41 5V_S0 — 5V_S0
13,14,26,30,32,37,38,41 5V_S3 — 5V_S3
14,18,20,36,38 5V_S5 — 5V_S5
7,9,15,18 2D5V_S0 — 2D5V_S0
7,9,10,11,12,38,39,41 2D5V_S3 — 2D5V_S3
7,11 DDR_VREF_S3 — DDR_VREF_S3
14,35,37,38,39,41 DCBATOUT — DCBATOUT
38,39,41 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,16,18,36,41 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,41 CORE_GMCH_S0 — CORE_GMCH_S0

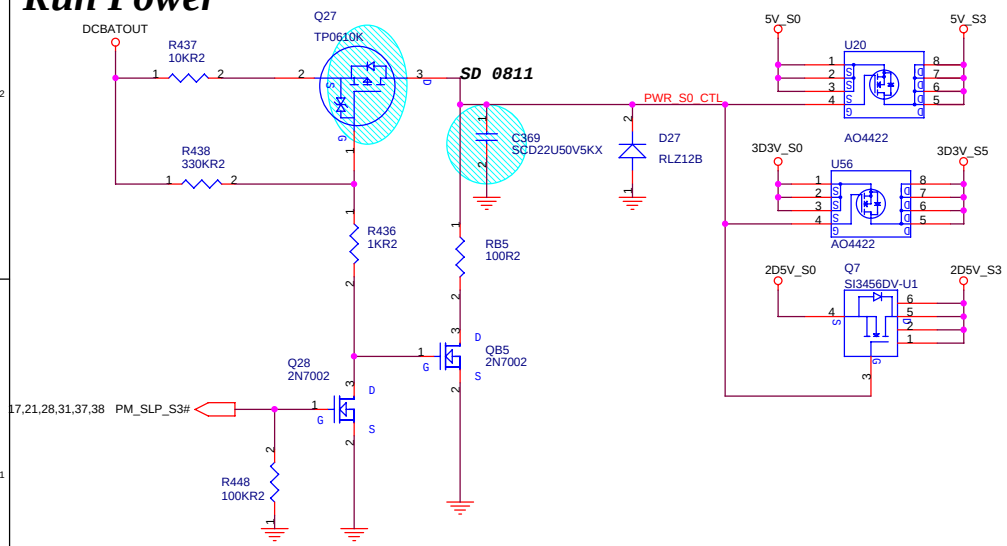


DDR_VREF_S3 need 10 mil and must neat NB and DIMM

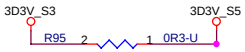
FOR DDR Power

Run Power

0223 -3



Suspend Power



鋒創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PWRPLANE&RESETLOGIC		
Size: A3	Document Number: Leopard	Rev: -4
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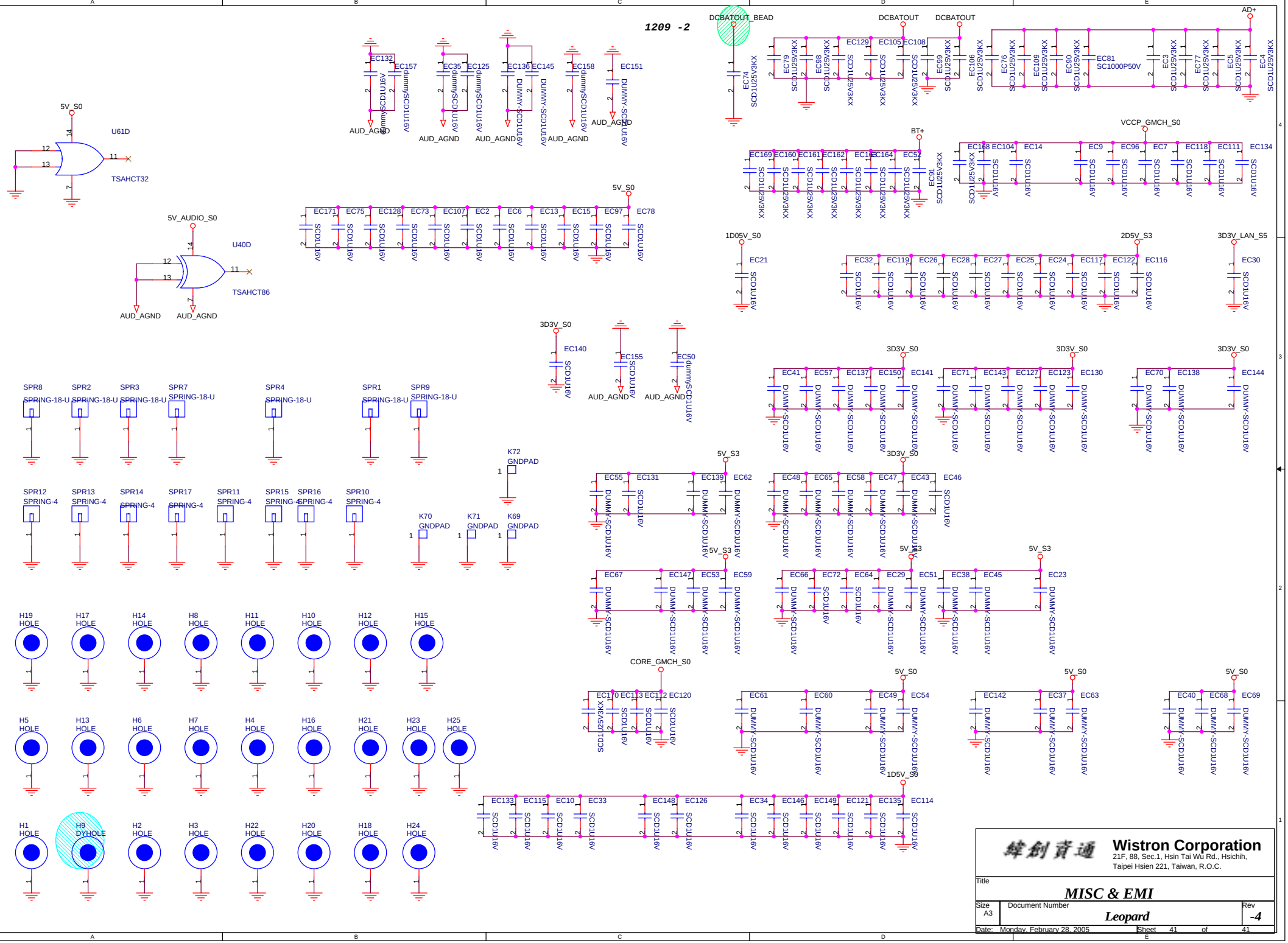

鋒創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***MISC & EMI***		
Size A3	Document Number ***Leopard***	Rev ***-4***	
Date: Monday, February 28, 2005	Sheet 41 of 41		