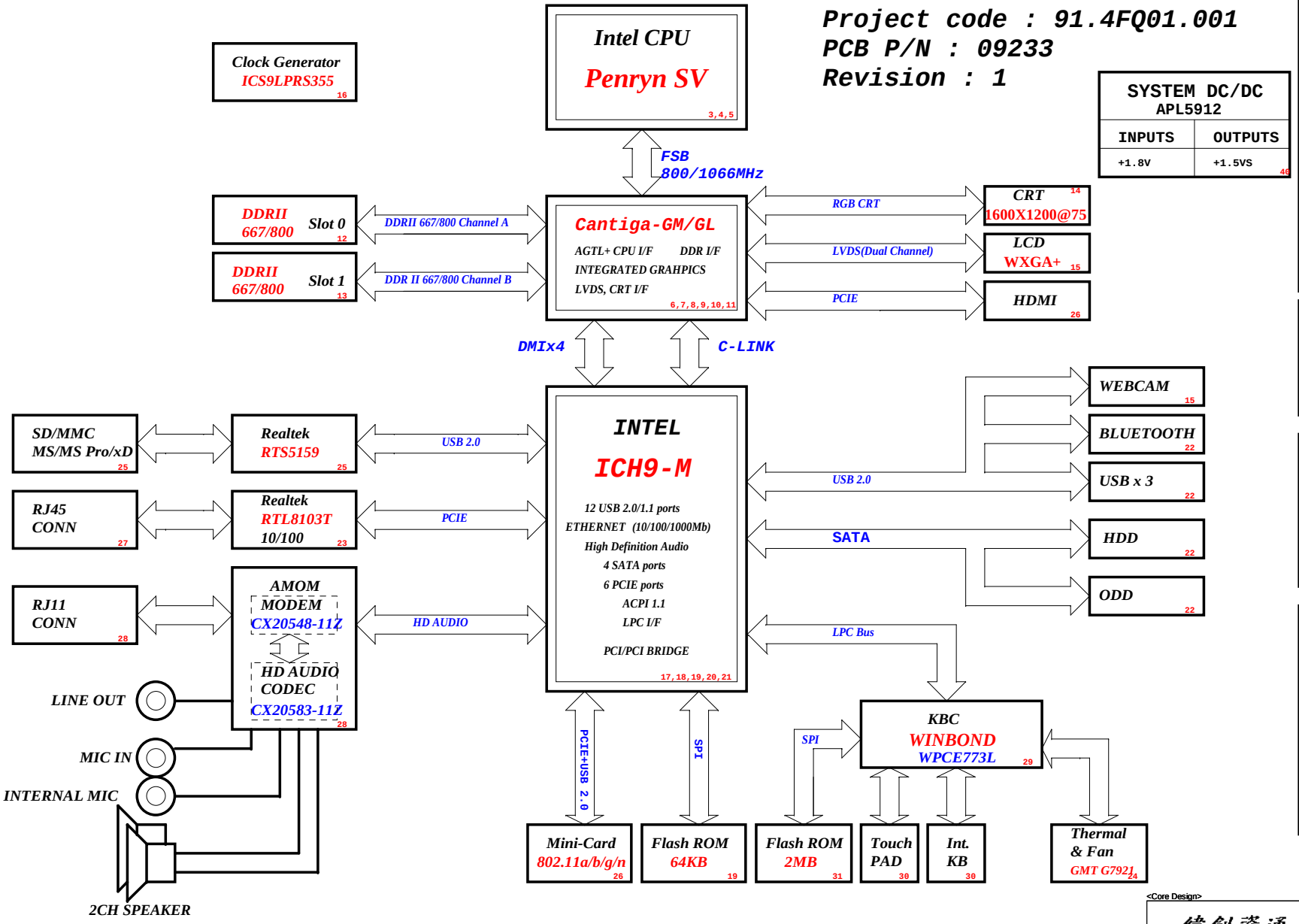
HBU16-1.2 Intel UMA Block Diagram

Project code : 91.4FQ01.001
PCB P/N : 09233
Revision : 1



SYSTEM DC/DC
APL5912

INPUTS	OUTPUTS
+1.8V	+1.5VS 40

SYSTEM DC/DC
TPS51125

INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 37

SYSTEM DC/DC
TPS51116

INPUTS	OUTPUTS
DCBATOUT	+0.9VS +1.8V 38

SYSTEM DC/DC
RT8209

INPUTS	OUTPUTS
+5VALW	+1.05V 39

MAXIM CHARGER
MAX8731

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 33

CPU DC/DC
ISL6269CCRZ

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 22A 35,36

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size	Document Number	Rev
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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

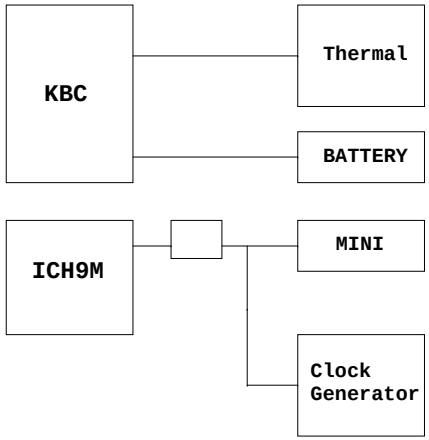
PCIE Routing page 19

LANE1	**LAN**
LANE2	**MiniCard WLAN**

USB Table page 19

USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

SMBus



<Core Design>

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Title: ***Table of Content***

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Reserve for ITP, when install ITP connector, install R69.

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

ITP Connector

1st: 62.10079.001
2nd: 62.10053.401

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Title: CPU (1 of 2)

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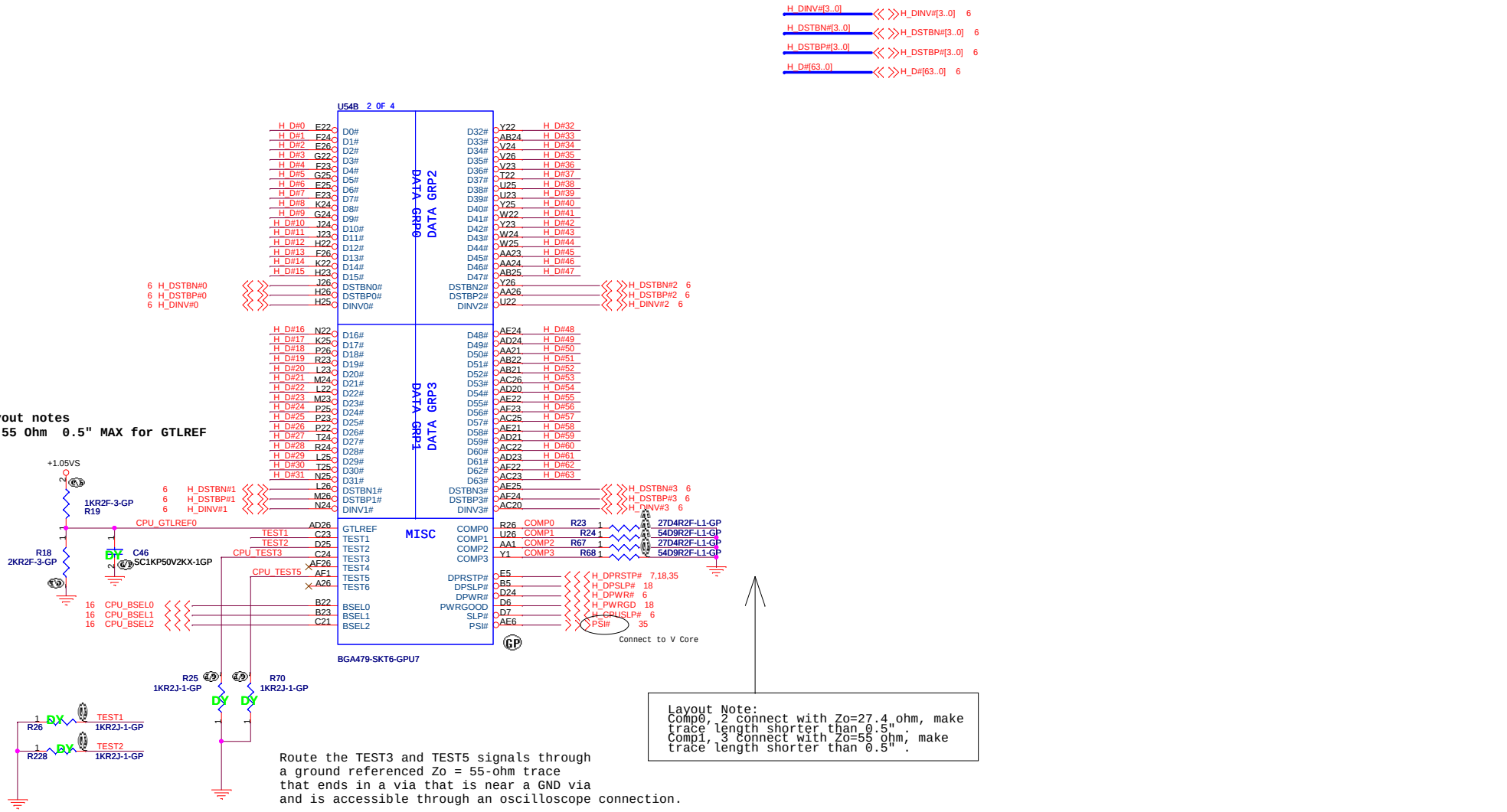

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Title	***CPU (3 of 2)***	
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Please these inside socket cavity on L8(North side Secondary)

Please these inside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(North side Primary)

Please these outside socket cavity on L8(North side Secondary)

Please these outside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(South side Primary)

Please these inside socket cavity on L8(North side Secondary)

layout note: "1D5V_VCCA_S0" as short as possible

Layout Note:
Place as close as possible to the CPU VCCA pin.

Connect to V Core

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

U54C 3 0F 4

BGA479-SKT6-GPU7

U54D 4 0F 4

BGA479-SKT6-GPU7

TC14 ST220U2D5VBM-LGP

R225 0R0603-PAD

R56 100R2F-L1-GP-U

R57 100R2F-L1-GP-U

TP11 TPAD14-GP

TP44 TPAD14-GP

TP12 TPAD14-GP

TP43 TPAD14-GP

NCTF PIN

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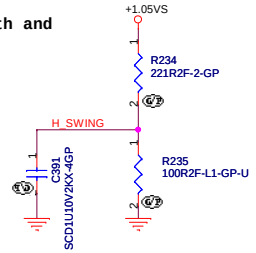
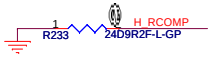
H_SWING routing Trace width and Spacing use 10 / 20 mil

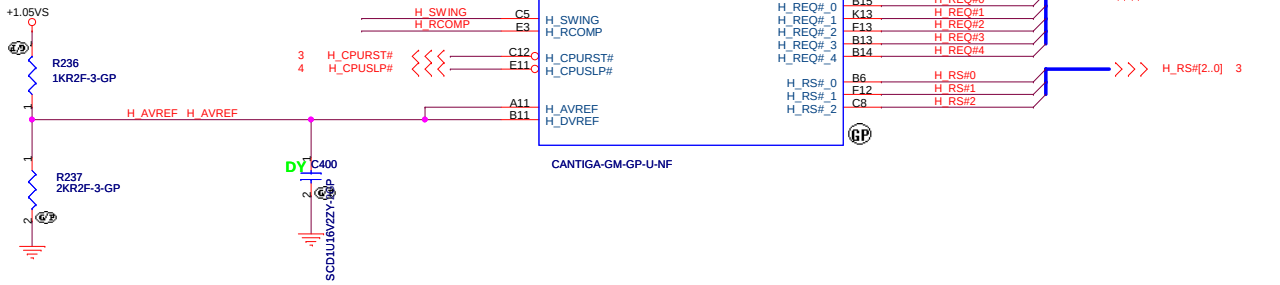
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Title: Cantiga (1 of 6)

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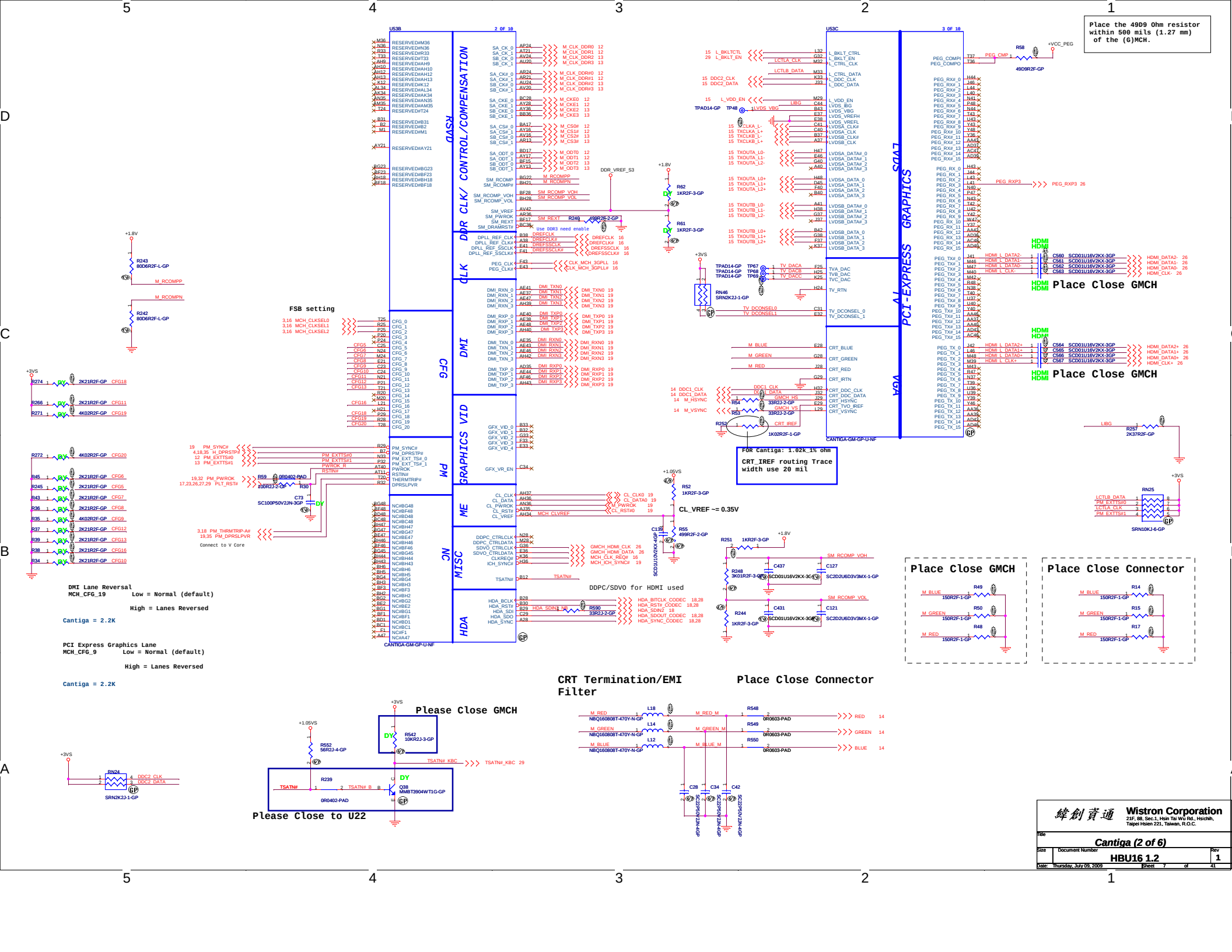
Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.
FSB setting
DMI Lane Reversal
MCH_CFG_19 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K
PCI Express Graphics Lane
MCH_CFG_9 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K
FOR Cantiga: 1.02k_1% ohm
CRT_IREF routing Trace width use 20 mil
CL_VREF ~= 0.35V
DDPC/SDVO for HDMI used
CRT Termination/EMI Filter
Place Close GMCH
Place Close Connector
Please Close GMCH
Please Close to U22
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Cantiga (2 of 6)
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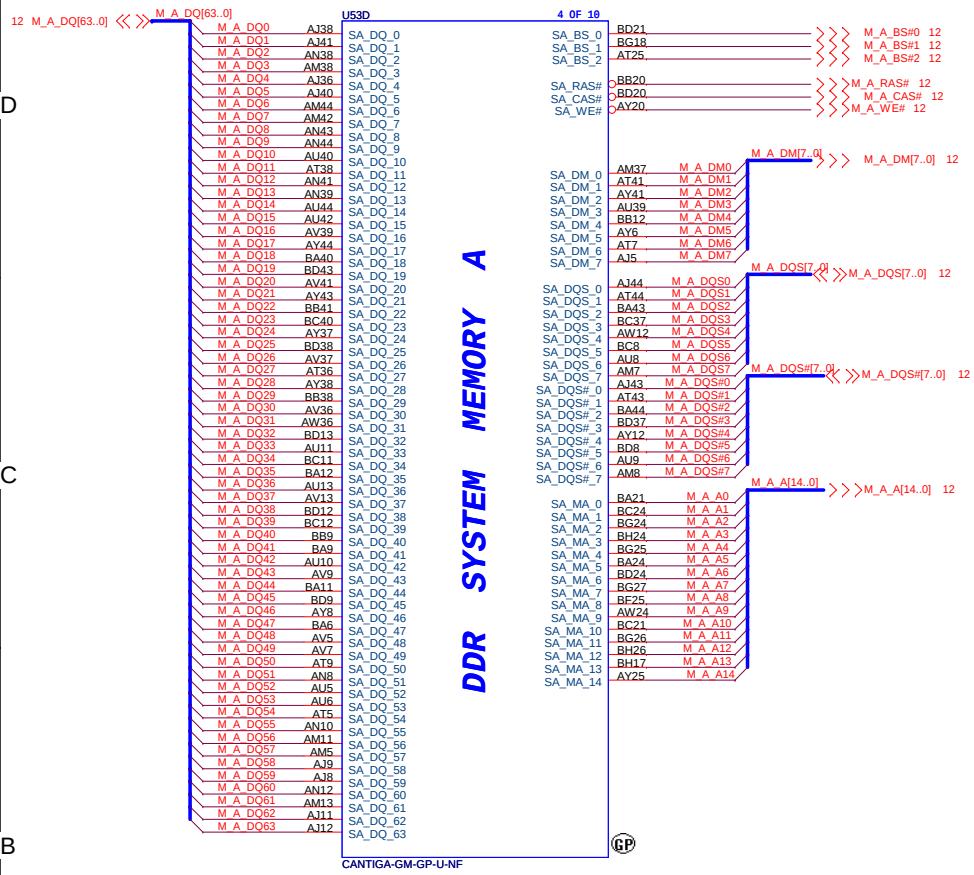

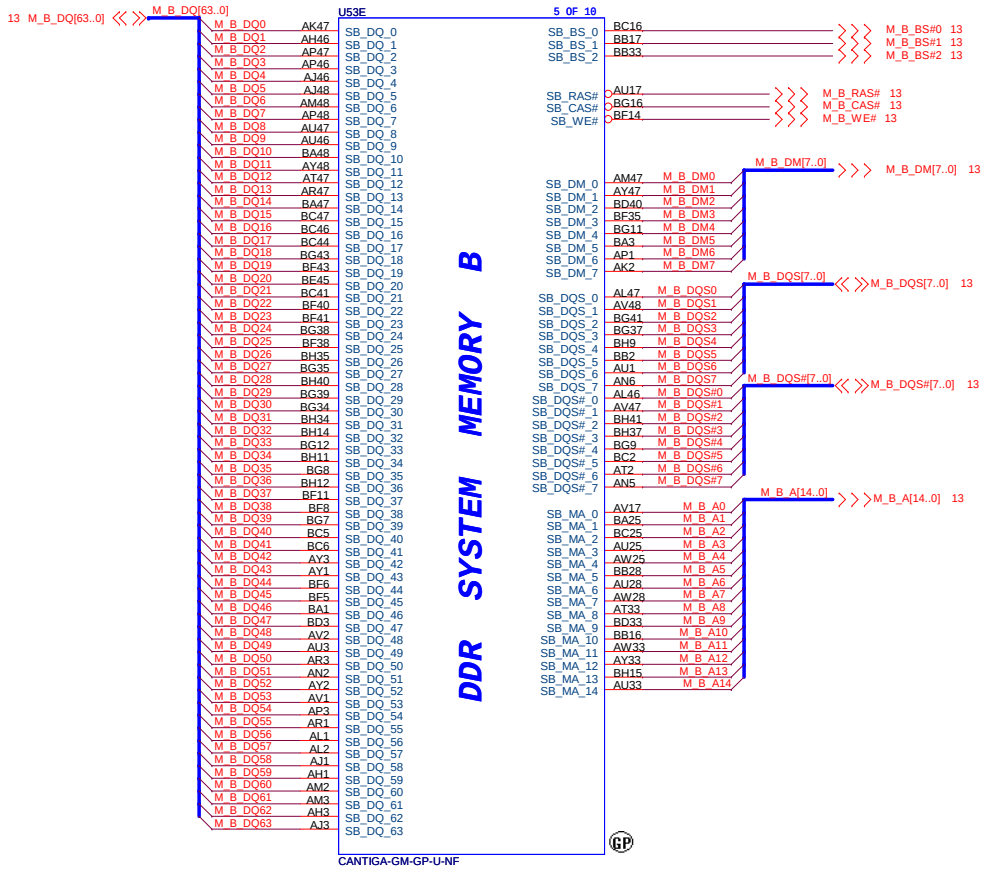

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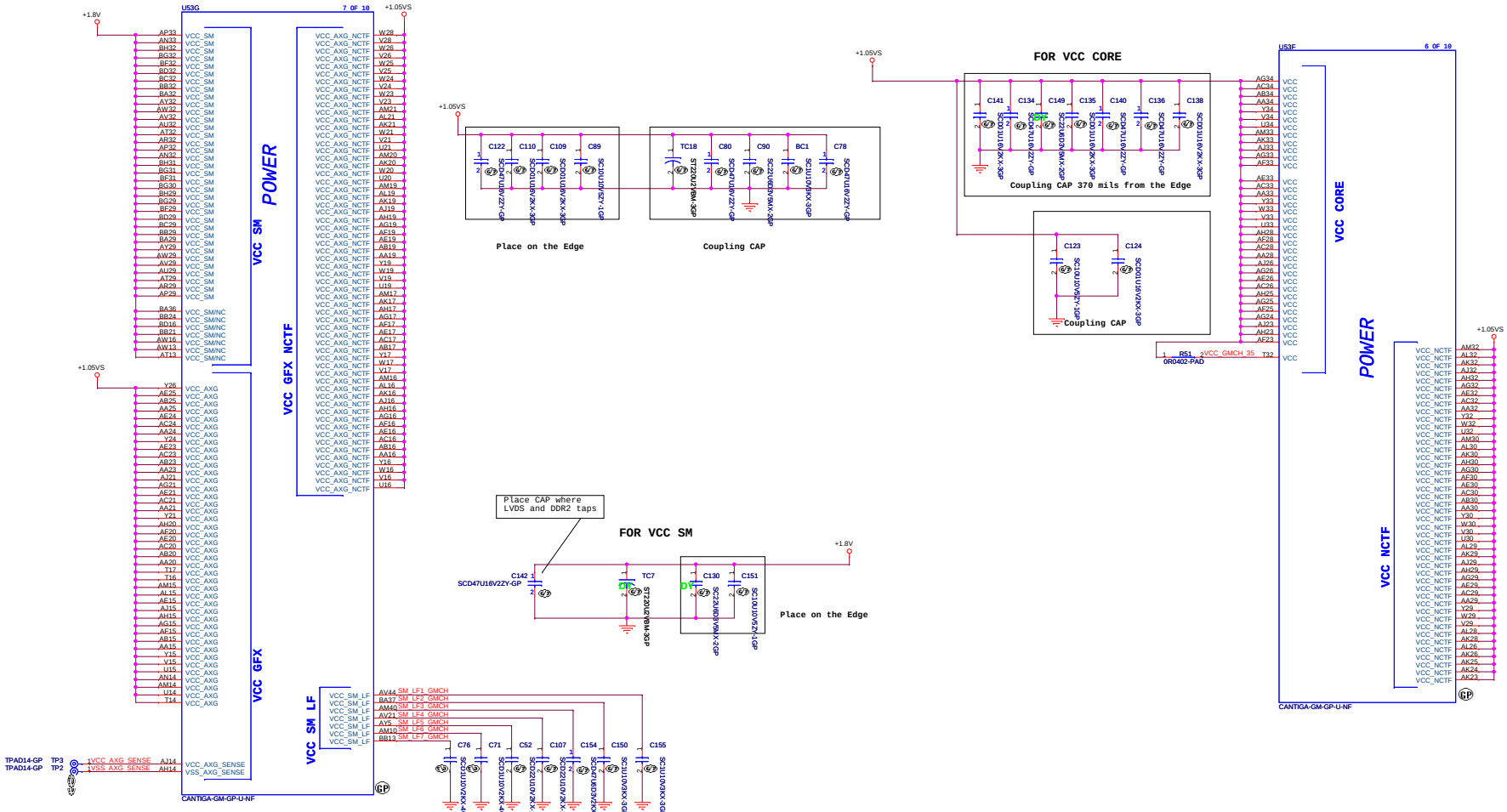

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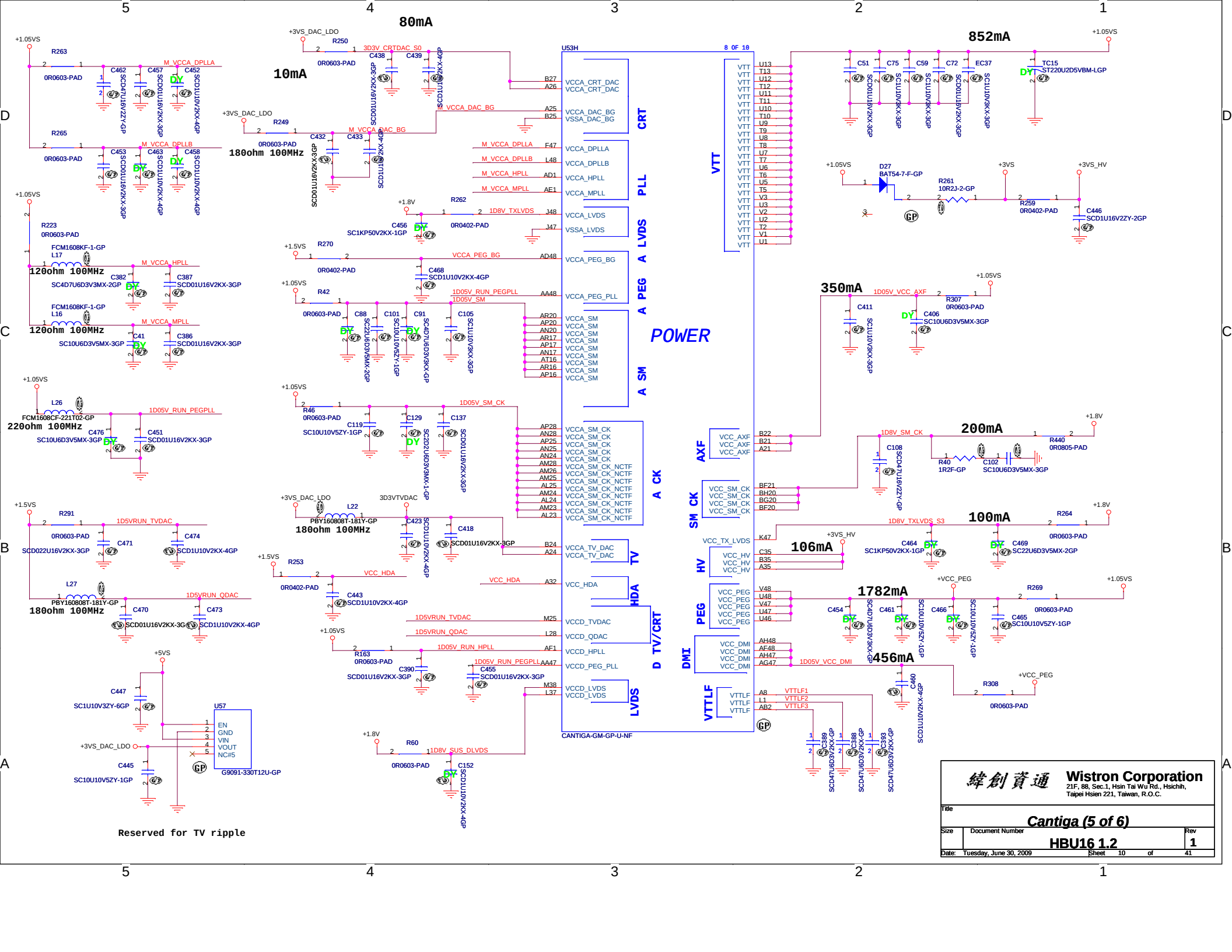
80mA
10mA
852mA
350mA
200mA
100mA
106mA
1782mA
456mA
180ohm 100MHz
120ohm 100MHz
220ohm 100MHz
U53H
8 OF 10
CANTIGA-GM-GP-U-NF
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
Reserved for TV ripple
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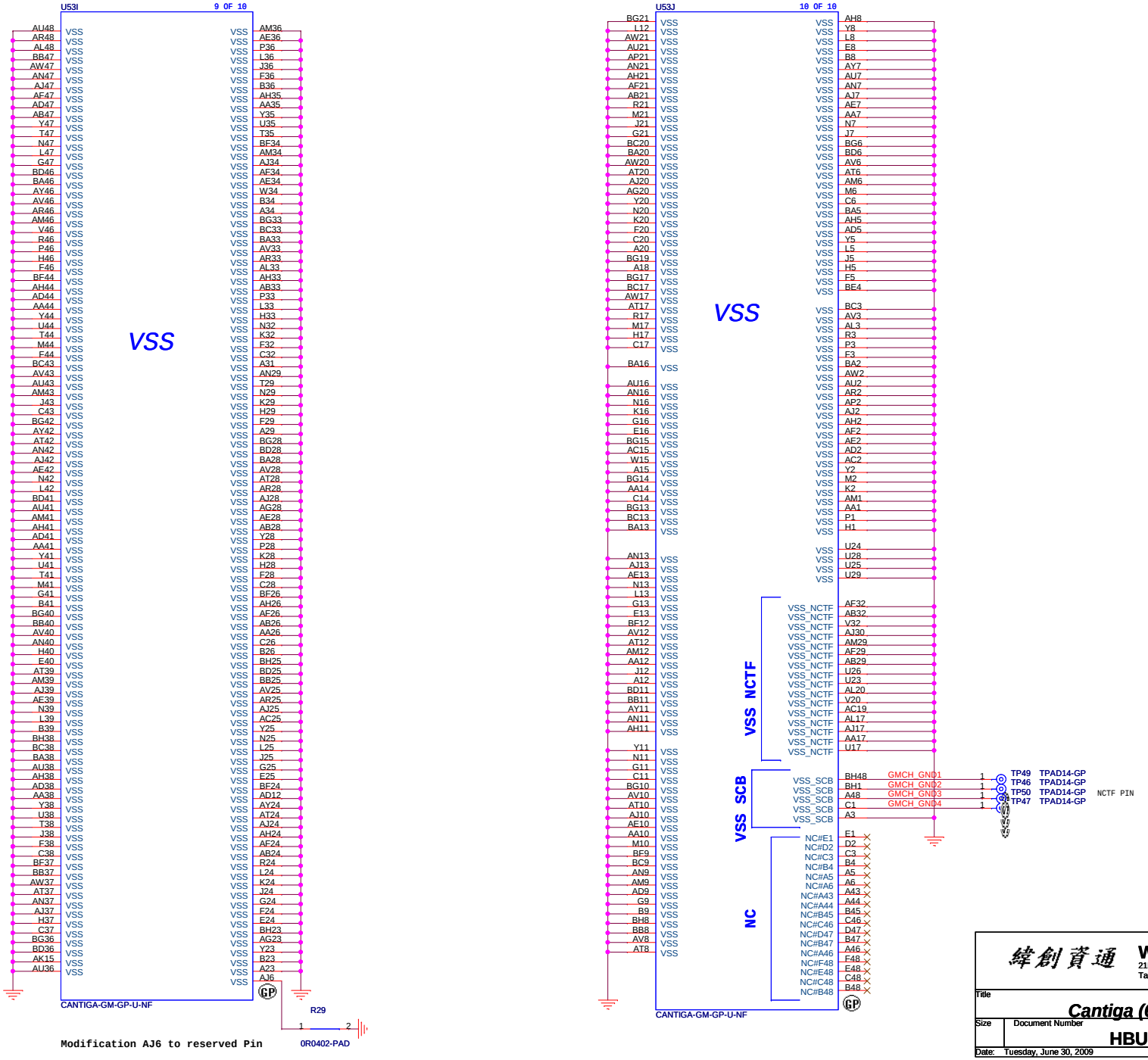

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Title: ***Cantiga (6 of 6)***

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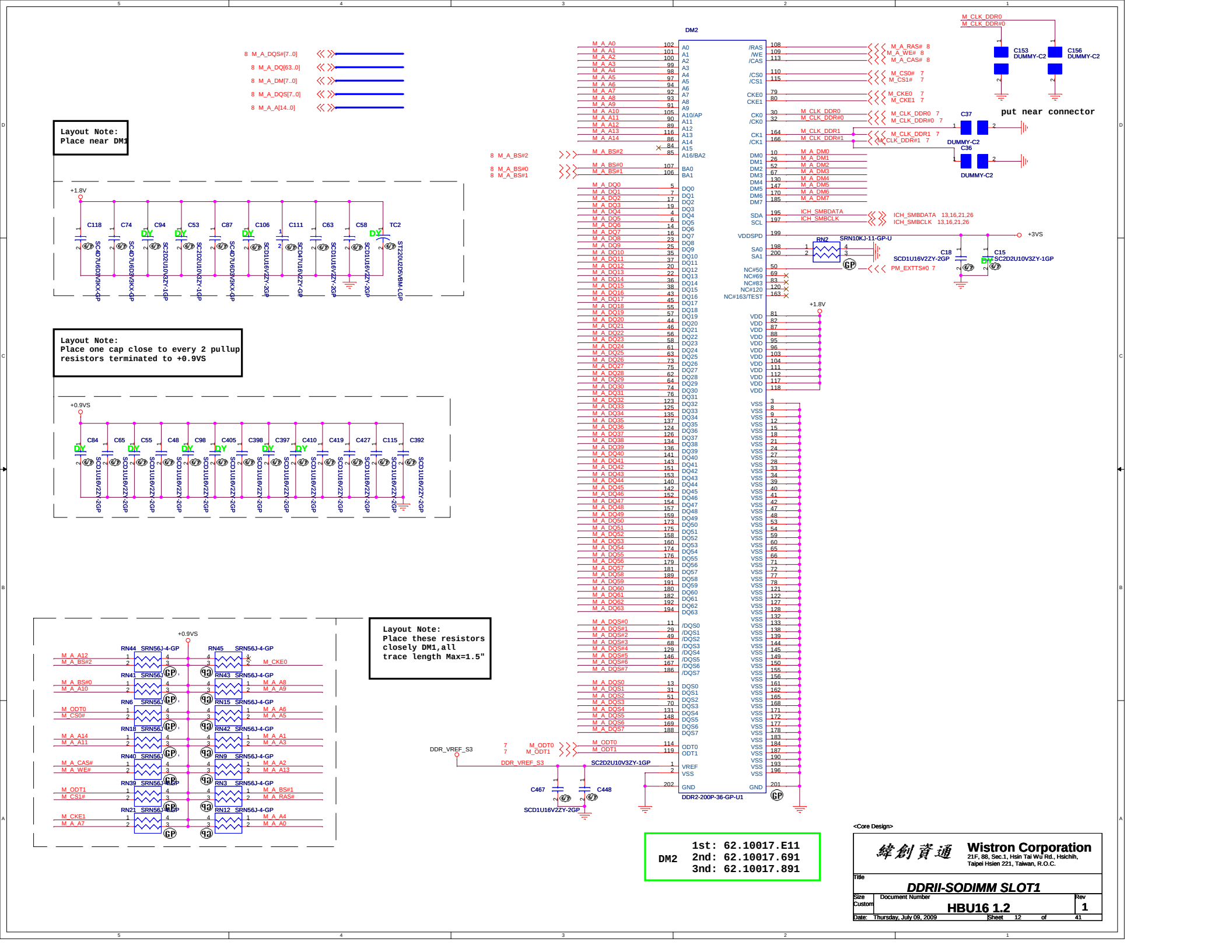

DM2 1st: 62.10017.E11
2nd: 62.10017.691
3nd: 62.10017.891

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Title: DDRII-SODIMM SLOT1

Size: Custom | Document Number: HBU16 1.2 | Rev: 1

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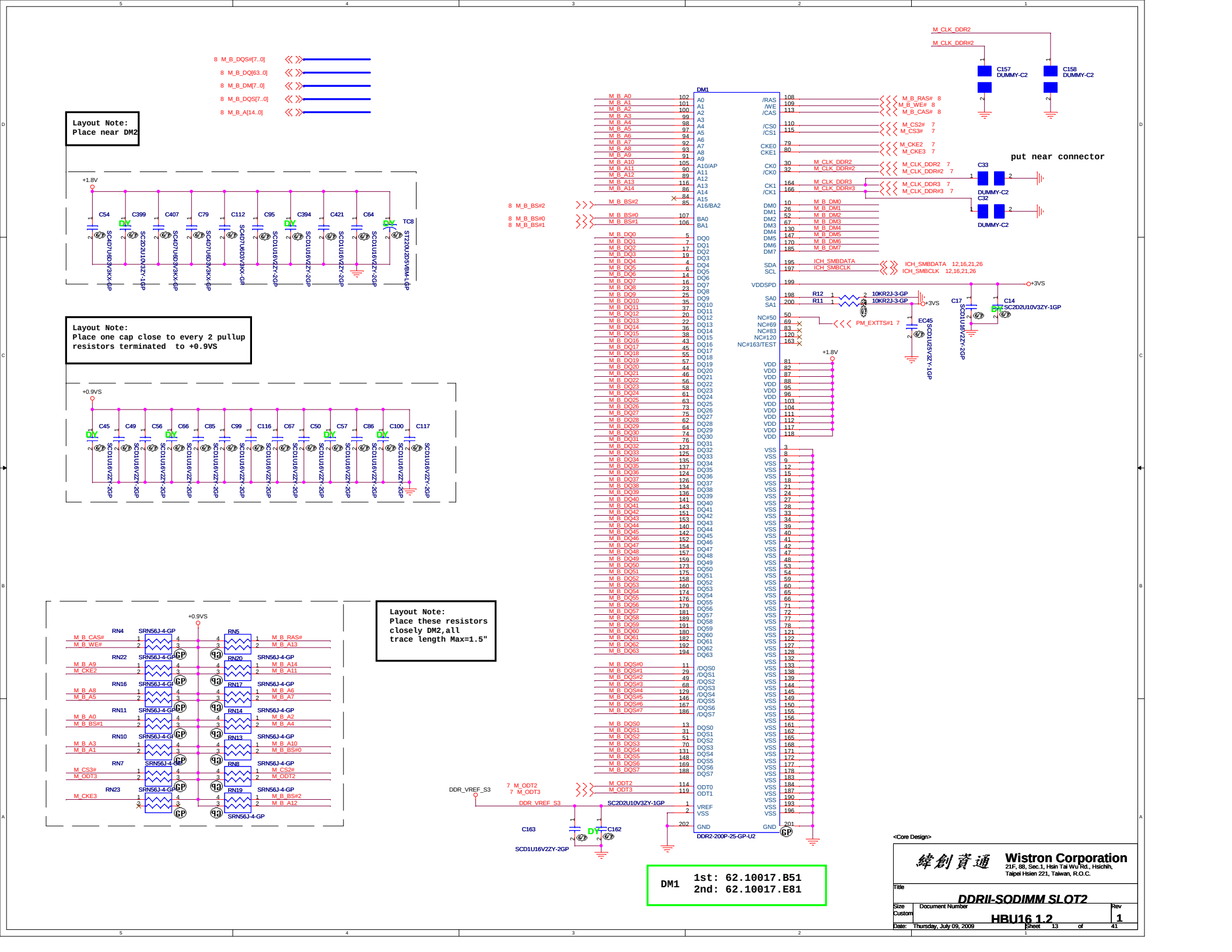
8 M_B_DQS#[7..0]
8 M_B_DQ[63..0]
8 M_B_DM[7..0]
8 M_B_DQS[7..0]
8 M_B_A[14..0]
Layout Note:
Place near DM2
+1.8V
C54 C399 C407 C79 C112 C95 C394 C421 C64 TC8
DY
SC4D7U6D3V3KX-6P
SC2D2U10N3ZY-1GP
SC4D7U6D3V3KX-GR
SC1U16V4ZY-2GP
SC2D2U6D3V9BM-LGP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
+0.9VS
C45 C49 C56 C66 C85 C99 C116 C67 C50 C57 C86 C100 C117
SC1U16V2ZY-2GP
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
+0.9VS
RN4 RN22 RN16 RN11 RN10 RN7 RN23
RN5 RN20 RN17 RN14 RN13 RN8 RN19
SRN56J-4-GP
M_B_CAS# M_B_WE# M_B_A9 M_CKE2 M_B_A8 M_B_A5 M_B_A0 M_B_BS#1 M_B_A3 M_B_A1 M_CS3# M_ODT3 M_CKE3
M_B_RAS# M_B_A13 M_B_A14 M_B_A11 M_B_A6 M_B_A7 M_B_A2 M_B_A4 M_B_A10 M_B_BS#0 M_CS2# M_ODT2 M_B_BS#2 M_B_A12
DM1
DDR2-200P-25-GP-U2
M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14
M_B_BS#2
M_B_BS#0 M_B_BS#1
M_B_DQ0 M_B_DQ1 M_B_DQ2 M_B_DQ3 M_B_DQ4 M_B_DQ5 M_B_DQ6 M_B_DQ7 M_B_DQ8 M_B_DQ9 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ13 M_B_DQ14 M_B_DQ15 M_B_DQ16 M_B_DQ17 M_B_DQ18 M_B_DQ19 M_B_DQ20 M_B_DQ21 M_B_DQ22 M_B_DQ23 M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ27 M_B_DQ28 M_B_DQ29 M_B_DQ30 M_B_DQ31 M_B_DQ32 M_B_DQ33 M_B_DQ34 M_B_DQ35 M_B_DQ36 M_B_DQ37 M_B_DQ38 M_B_DQ39 M_B_DQ40 M_B_DQ41 M_B_DQ42 M_B_DQ43 M_B_DQ44 M_B_DQ45 M_B_DQ46 M_B_DQ47 M_B_DQ48 M_B_DQ49 M_B_DQ50 M_B_DQ51 M_B_DQ52 M_B_DQ53 M_B_DQ54 M_B_DQ55 M_B_DQ56 M_B_DQ57 M_B_DQ58 M_B_DQ59 M_B_DQ60 M_B_DQ61 M_B_DQ62 M_B_DQ63
M_B_DQS#0 M_B_DQS#1 M_B_DQS#2 M_B_DQS#3 M_B_DQS#4 M_B_DQS#5 M_B_DQS#6 M_B_DQS#7
M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7
M_ODT2 M_ODT3
DDR_VREF_S3
SC2D2U10V3ZY-1GP
C163 C162
SCD1U16V2ZY-2GP
/RAS /WE /CAS /CS0 /CS1 CKE0 CKE1 CK0 /CK0 CK1 /CK1 SDA SCL VDDSPD SA0 SA1 NC#50 NC#69 NC#83 NC#120 NC#163/TEST VDD VSS VREF GND
M_B_RAS# 8
M_B_WE# 8
M_B_CAS# 8
M_CS2# 7
M_CS3# 7
M_CKE2 7
M_CKE3 7
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR2 7
M_CLK_DDR#2 7
M_CLK_DDR3
M_CLK_DDR#3
M_CLK_DDR3 7
M_CLK_DDR#3 7
M_B_DM0 M_B_DM1 M_B_DM2 M_B_DM3 M_B_DM4 M_B_DM5 M_B_DM6 M_B_DM7
ICH_SMBDATA
ICH_SMBCLK
ICH_SMBDATA 12,16,21,26
ICH_SMBCLK 12,16,21,26
+3VS
R12 R11 10KR2J-3-GP
PM_EXTTS#1 7
EC45 SCD1U25V2KY-1GP
C17 SCD1U16V2ZY-2GP
C14 SC2D2U10V3ZY-1GP
+1.8V
C157 C158 DUMMY-C2
C33 C32 DUMMY-C2
put near connector
DM1 1st: 62.10017.B51
2nd: 62.10017.E81
<Core Design>
緯創資通
Wistron Corporation
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Title
DDRII-SODIMM SLOT2
Size Custom
Document Number HBU16 1.2
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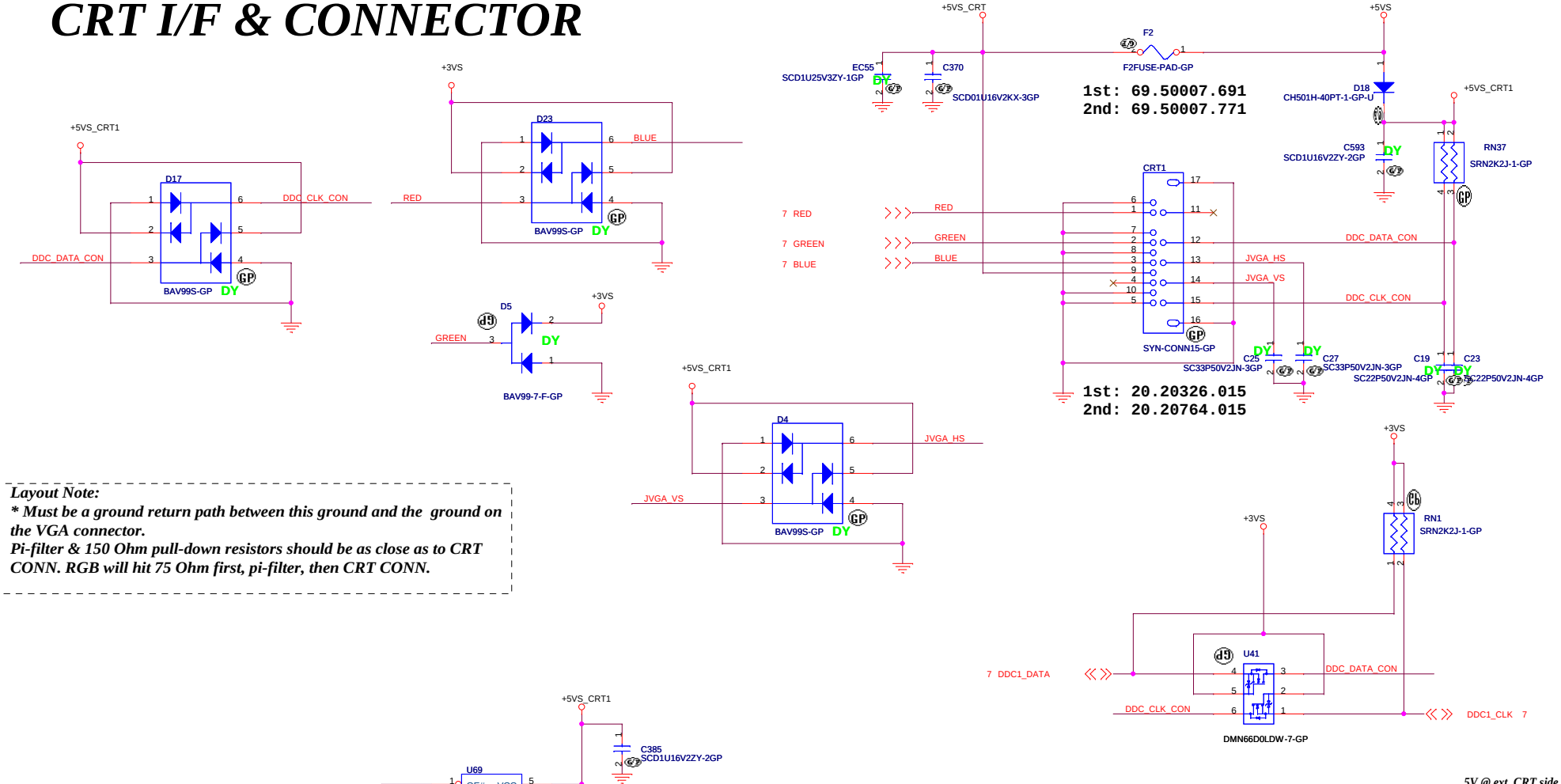
CRT I/F & CONNECTOR



Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

5V @ ext. CRT side

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **CRT Connector**		
Size: A3	Document Number: **HBU16 1.2**	Rev: **1**
Date: Thursday, July 09, 2009	Sheet 14 of 41	

LCD / INVERTER INTERFACE / CAMERA

+5VS
R33 330R2J-3-GP
CAPS_LED_PWR
LED1 LED-W-12-GP-U
CAPS_LED# 28,29

White LED:
Lite-On 83.00191.D70
Everlight 83.19217.F70

LID_CLOSE# TP187 TP28-75-GP
COVER_SW TP188 TP28-75-GP
GND TP189 TP28-75-GP
GND TP190 TP28-75-GP

+3VL
R547 10KR2J-3-GP
29,31 LID_CLOSE#
R545 100R2J-2-GP
C610 SCD22U10V2KX-1GP
C609 SC1KP50V2KX-1GP

+3VS
C341 SCD1U16V2ZY-2GP
EC33 SCD1U25V3ZY-1GP
+LCDVDD
C354 SC10U10V5ZY-1GP
C348 SCD1U16V2ZY-2GP
29 SIZE_DET1
R238 100KR2J-1-GP
29 EC_BLON
7 DDC2_CLK
7 DDC2_DATA
BRIGHTNESS_CONN
COVER_SW
+5VS_CAMERA
EC34 SCD1U25V3ZY-1GP
USB_10+
USB_10-
LVDS1 ACES-CONN46C-2-GP-U
DCBATOUT
C353 SCD1U25V3KX-GP
R241 100KR2J-1-GP
SIZE_DET0 29
TXOUTB_L2+ 7
TXOUTB_L2- 7
TXOUTB_L1+ 7
TXOUTB_L1- 7
TXOUTB_L0+ 7
TXOUTB_L0- 7
TXCLKB_L+ 7
TXCLKB_L- 7
TXOUTA_L2+ 7
TXOUTA_L2- 7
TXOUTA_L1+ 7
TXOUTA_L1- 7
TXOUTA_L0+ 7
TXOUTA_L0- 7
TXCLKA_L+ 7
TXCLKA_L- 7

	SIZE_DET0 (Pin27)	SIZE_DET1 (Pin19)
15.4"	1	1
17.0"	0	1
15.6"	1	0
16.0"	0	0

+5VS_CAMERA TP138 TP28-75-GP
USB_10+ TP139 TP28-75-GP
USB_10- TP140 TP28-75-GP
GND TP141 TP28-75-GP

1st: 20.F1296.046
2nd: 20.F1270.046

+3VS
18 SATA_LED#
Q33 PDTA124EU-1-GP
R230 100KR2J-1-GP
SATA_BD_LED_C
SATA_LED# C
U48 DMN66D0LDW-7-GP
SATA_BD_LED 28
SATA_LED 29

R27 0R0402-PAD
19 USB20_N10
USB_10-
R28 0R0402-PAD
19 USB20_P10
USB_10+

R551 0R0603-PAD
+5VS
Q20 AO3403-GP
EC50 SCD1U25V3ZY-1GP
R229 100KR2J-1-GP
+5VS_CAMERA
C379 SCD1U16V2ZY-2GP
C378 SC4D7U10V5ZY-3GP
R226 100KR2J-1-GP
29 CAM_PWR#
CAM_PWR#
R232 10KR2J-3-GP
CAM_PWR_G#
C380 SC1KP50V2KX-1GP

BRIGHTNESS_CONN
0R0402-PAD
R222
BRIGHTNESS 29
R224 0R2J-2-GP
L_BKLTCTL 7
R220 100KR2J-1-GP

+3VS
D21 BAV99W-1-GP
EC_BLON
C364 SC1KP50V2KX-1GP
C374 SC1KP50V2KX-1GP
BRIGHTNESS_CONN
D22 BAV99W-1-GP
0630 -1

Layout 40 mil
+3VS
+LCDVDD
7 L_VDD_EN
R203 100KR2J-1-GP
U43 G5281RC1U-GP
EC14 SCD1U16V2ZY-2GP
BC2 SC10U10V3ZY-6GP

+3VS
R208 100KR2J-1-GP
U46 DMN66D0LDW-7-GP
+LCDVDD
L_VDD_EN
R202 100R2J-2-GP

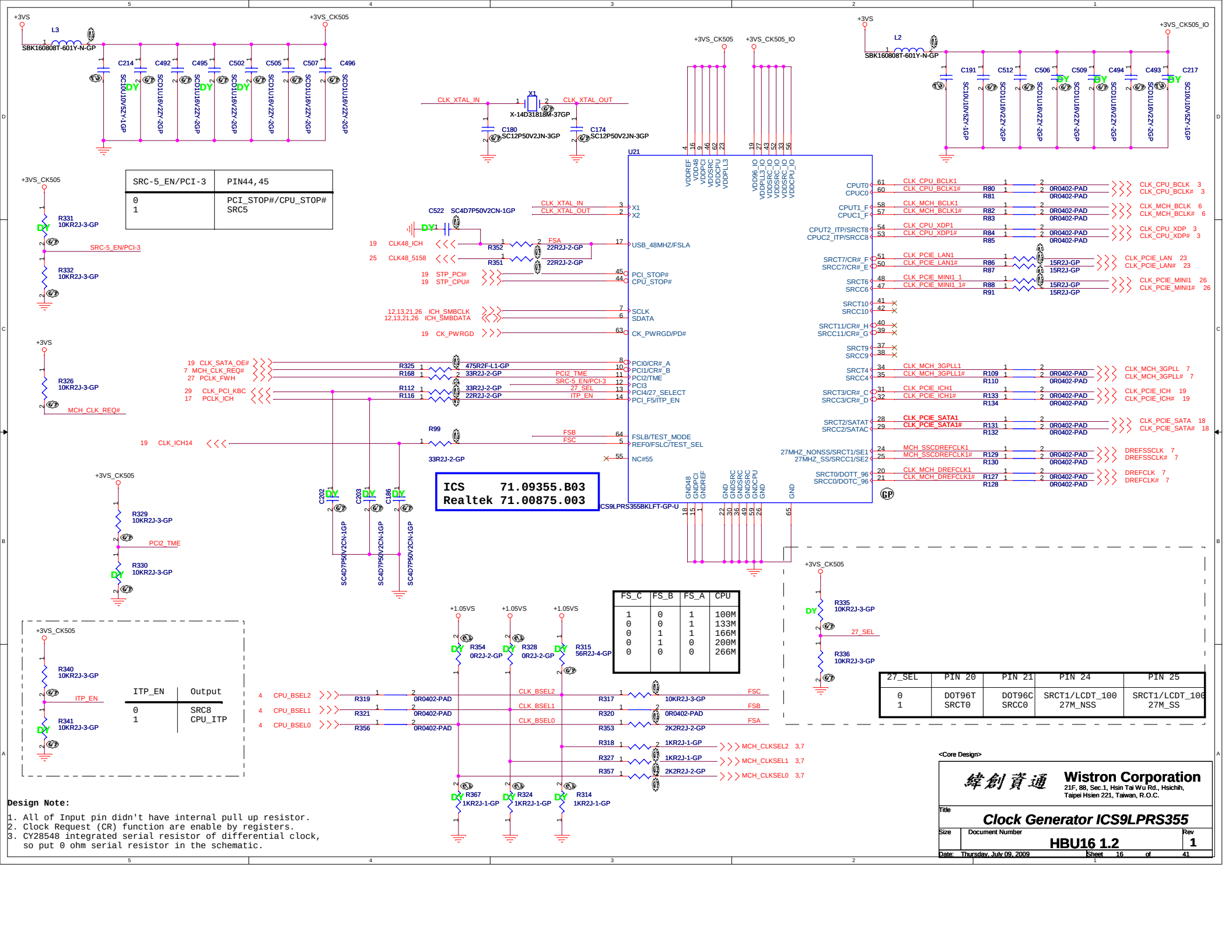
<Core Design>

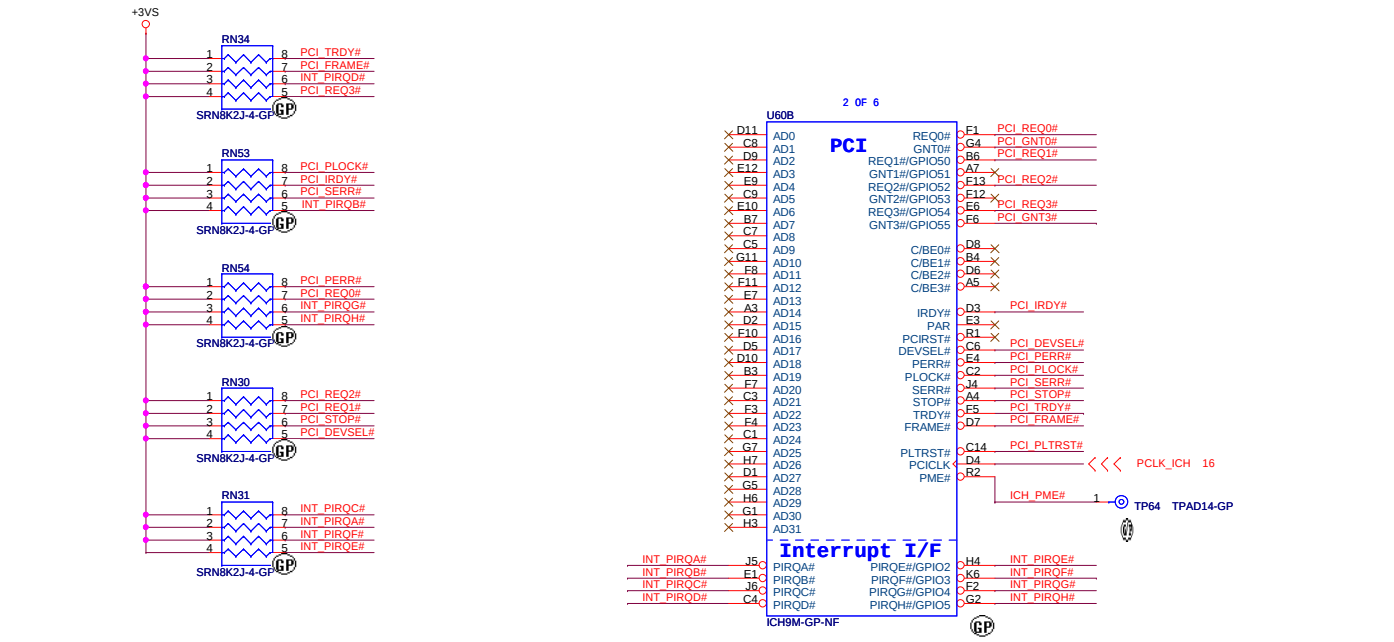
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

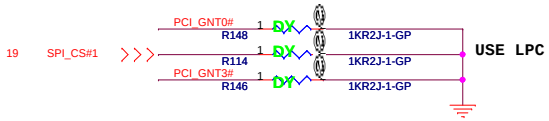
Title: ***LCD/Inverter Connector/CAM/LED***

Size	Document Number	Rev
A3	HBU16 1.2	1

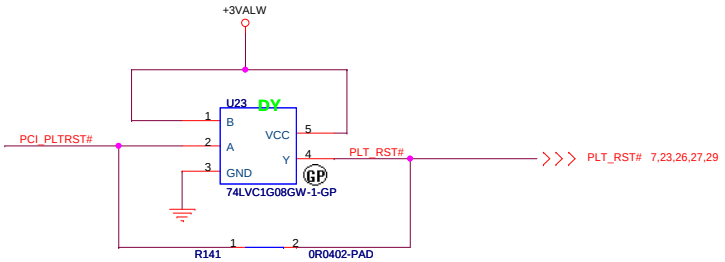
Date: Thursday, July 09, 2009 Sheet 15 of 41


+3VS
L3
SBK160808T-601Y-N-GP
+3VS_CK505
C214
C492
C495
C502
C505
C507
C496
SCD1U16V2ZY-1GP
SCD1U16V2ZY-2GP
DY
+3VS_CK505_IO
L2
C191
C512
C506
C509
C494
C493
C217
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
CLK_XTAL_IN
CLK_XTAL_OUT
X1
X-14D31818M-37GP
C180
SC12P50V2JN-3GP
C174
SC12P50V2JN-3GP
U21
VDDREF
VDD48
VDDPCI
VDDSRC
VDDCPU
VDDPLL3
VDD96_IO
VDDPLL3_IO
VDDSRC_IO
VDDCPU_IO
SRC-5_EN/PCI-3
PIN44,45
0
PCI_STOP#/CPU_STOP#
1
SRC5
R331
10KR2J-3-GP
R332
10KR2J-3-GP
C522
SC4D7P50V2CN-1GP
CLK48_ICH
CLK48_5158
R352
R351
22R2J-2-GP
FSA
USB_48MHZ/FSLA
STP_PCI#
STP_CPU#
PCI_STOP#
CPU_STOP#
ICH_SMBCLK
ICH_SMBDATA
SCLK
SDATA
CK_PWRGD
CK_PWRGD/PD#
R326
10KR2J-3-GP
MCH_CLK_REQ#
CLK_SATA_OE#
MCH_CLK_REQ#
PCLK_FWH
CLK_PCI_KBC
PCLK_ICH
R325
R168
R112
R116
475R2F-L1-GP
33R2J-2-GP
22R2J-2-GP
PCI2_TME
SRC-5_EN/PCI-3
27_SEL
ITP_EN
PCI0/CR#_A
PCI1/CR#_B
PCI2/TME
PCI3
PCI4/27_SELECT
PCI_F5/ITP_EN
CLK_ICH14
R99
FSB
FSC
FSLB/TEST_MODE
REF0/FSLC/TEST_SEL
NC#55
ICS 71.09355.B03
Realtek 71.00875.003
CS9LPRS355BKLFT-GP-U
R329
10KR2J-3-GP
R330
10KR2J-3-GP
C202
C203
C186
SC4D7P50V2CN-1GP
CPUT0
CPUC0
CPUT1_F
CPUC1_F
CPUT2_ITP/SRCT8
CPUC2_ITP/SRCC8
SRCT7/CR#_F
SRCC7/CR#_E
SRCT6
SRCC6
SRCT10
SRCC10
SRCT11/CR#_H
SRCC11/CR#_G
SRCT9
SRCC9
SRCT4
SRCC4
SRCT3/CR#_C
SRCC3/CR#_D
SRCT2/SATAT
SRCC2/SATAC
27MHZ_NONSS/SRCT1/SE1
27MHZ_SS/SRCC1/SE2
SRCT0/DOTT_96
SRCC0/DOTC_96
CLK_CPU_BCLK
CLK_CPU_BCLK#
CLK_MCH_BCLK
CLK_MCH_BCLK#
CLK_CPU_XDP
CLK_CPU_XDP#
CLK_PCIE_LAN
CLK_PCIE_LAN#
CLK_PCIE_MINI1_1
CLK_PCIE_MINI1_1#
CLK_MCH_3GPLL1
CLK_MCH_3GPLL1#
CLK_PCIE_ICH1
CLK_PCIE_ICH1#
CLK_PCIE_SATA1
CLK_PCIE_SATA1#
MCH_SSCDREFCLK1
MCH_SSCDREFCLK1#
CLK_MCH_DREFCLK1
CLK_MCH_DREFCLK1#
R80
R81
R82
R83
R84
R85
R86
R87
R88
R91
R109
R110
R133
R134
R131
R132
R129
R130
R127
R128
0R0402-PAD
15R2J-GP
CLK_CPU_BCLK 3
CLK_CPU_BCLK# 3
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
CLK_CPU_XDP 3
CLK_CPU_XDP# 3
CLK_PCIE_LAN 23
CLK_PCIE_LAN# 23
CLK_PCIE_MINI1 26
CLK_PCIE_MINI1# 26
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
CLK_PCIE_ICH 19
CLK_PCIE_ICH# 19
CLK_PCIE_SATA 18
CLK_PCIE_SATA# 18
DREFSSCLK 7
DREFSSCLK# 7
DREFCLK 7
DREFCLK# 7
GP
GND48
GNDPCI
GNDREF
GND
GNDSRC
GNDCPU
R335
10KR2J-3-GP
R336
10KR2J-3-GP
27_SEL
27_SEL
PIN 20
PIN 21
PIN 24
PIN 25
0
DOT96T
SRCT0
DOT96C
SRCC0
SRCT1/LCDT_100
27M_NSS
SRCT1/LCDT_100
27M_SS
1
R340
10KR2J-3-GP
ITP_EN
R341
10KR2J-3-GP
ITP_EN
Output
0
SRC8
1
CPU_ITP
+1.05VS
R354
0R2J-2-GP
R328
0R2J-2-GP
R315
56R2J-4-GP
FS_C
FS_B
FS_A
CPU
1
0
1
100M
0
0
1
133M
0
1
1
166M
0
1
0
200M
0
0
0
266M
CPU_BSEL2
CPU_BSEL1
CPU_BSEL0
R319
R321
R356
R317
R320
R353
10KR2J-3-GP
0R0402-PAD
2K2R2J-2-GP
FSC
FSB
FSA
R318
R327
R357
1KR2J-1-GP
2K2R2J-2-GP
MCH_CLKSEL2 3,7
MCH_CLKSEL1 3,7
MCH_CLKSEL0 3,7
R367
R324
R314
1KR2J-1-GP
Design Note:
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock,
so put 0 ohm serial resistor in the schematic.
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator ICS9LPRS355
Size
Document Number
HBU16 1.2
Rev
1
Date: Thursday, July 09, 2009
Sheet 16 of 41





BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	



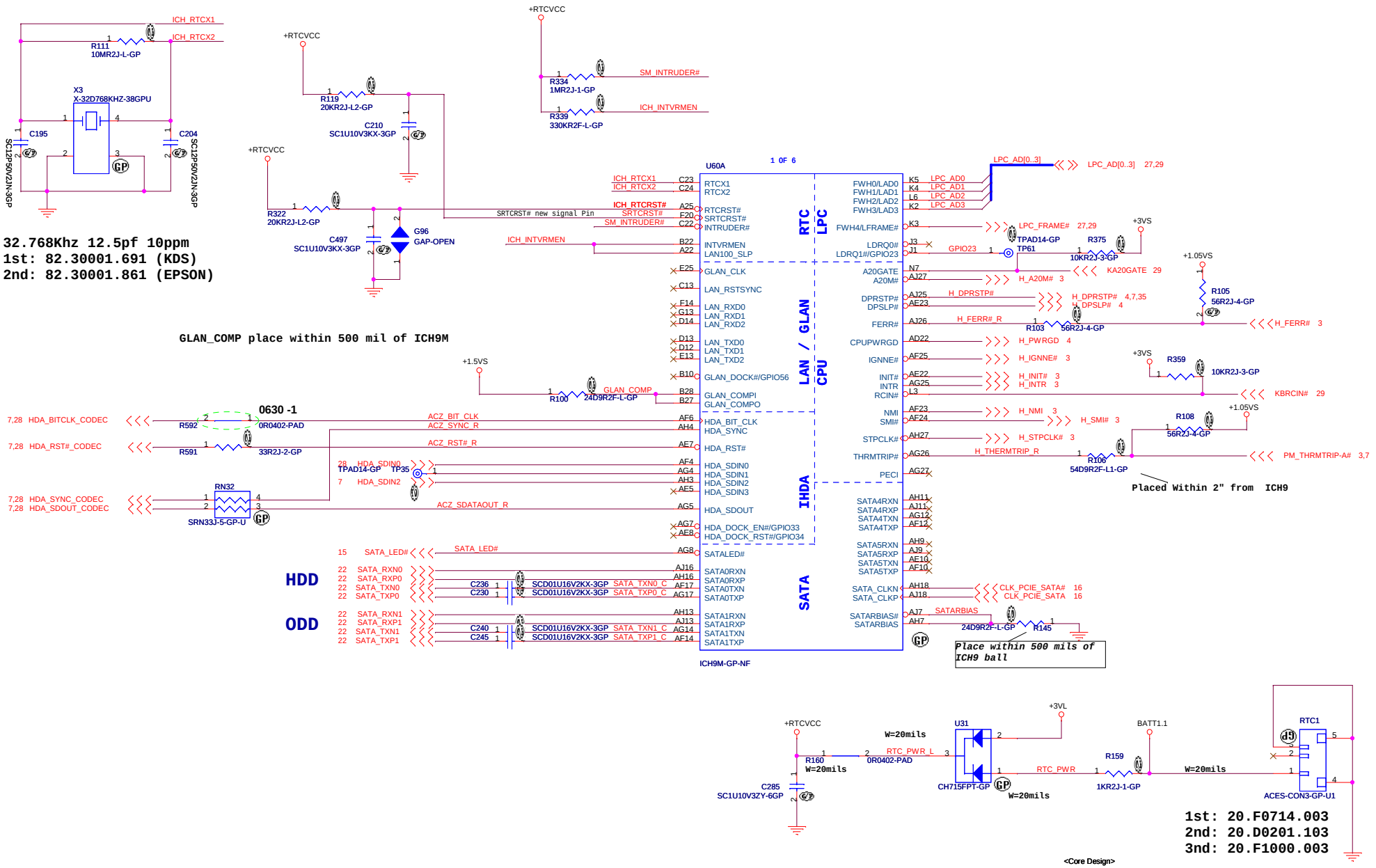
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (1 of 5)

Size | Document Number: HBU16 1.2 | Rev: 1

Date: Thursday, July 09, 2009 | Sheet 17 of 41



integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

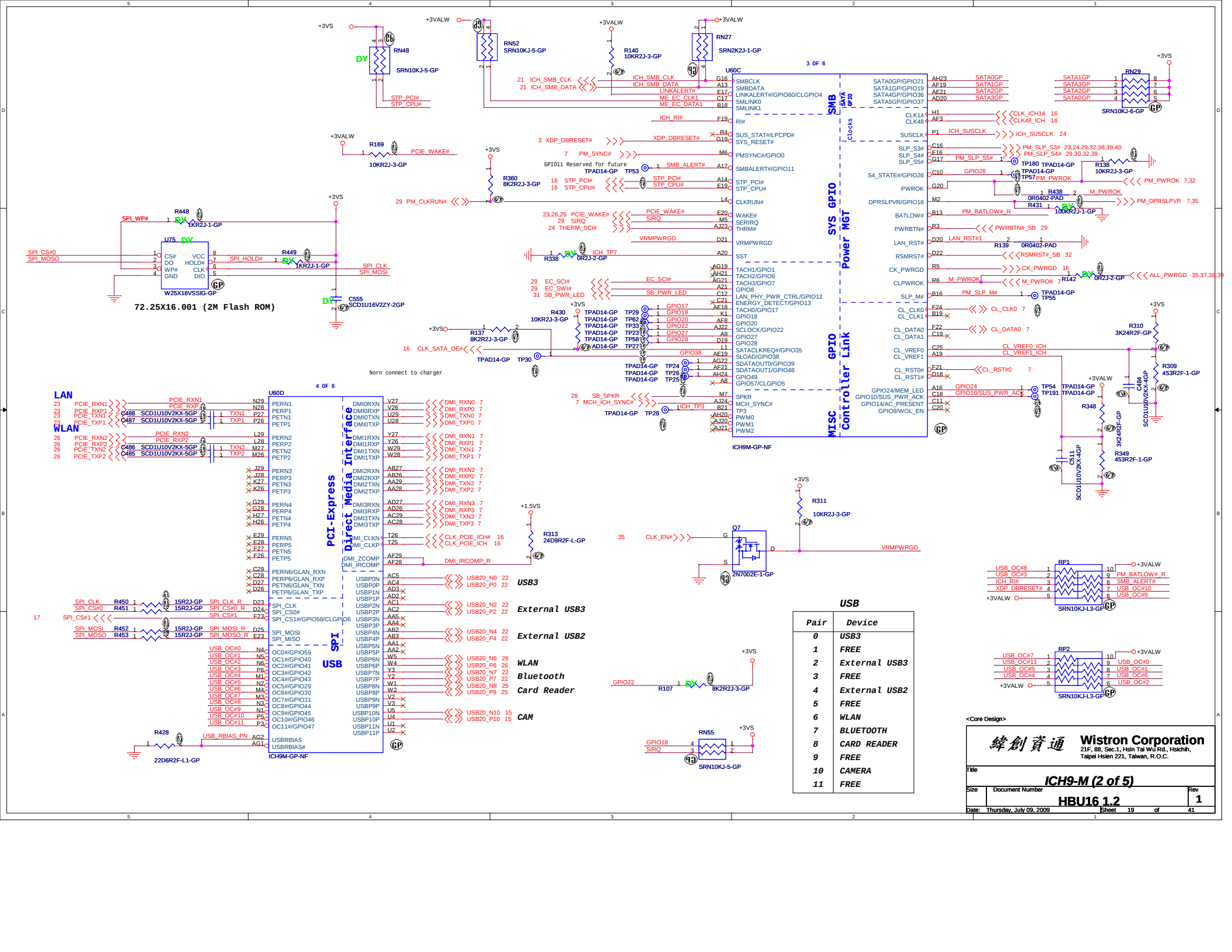
<Core Design>

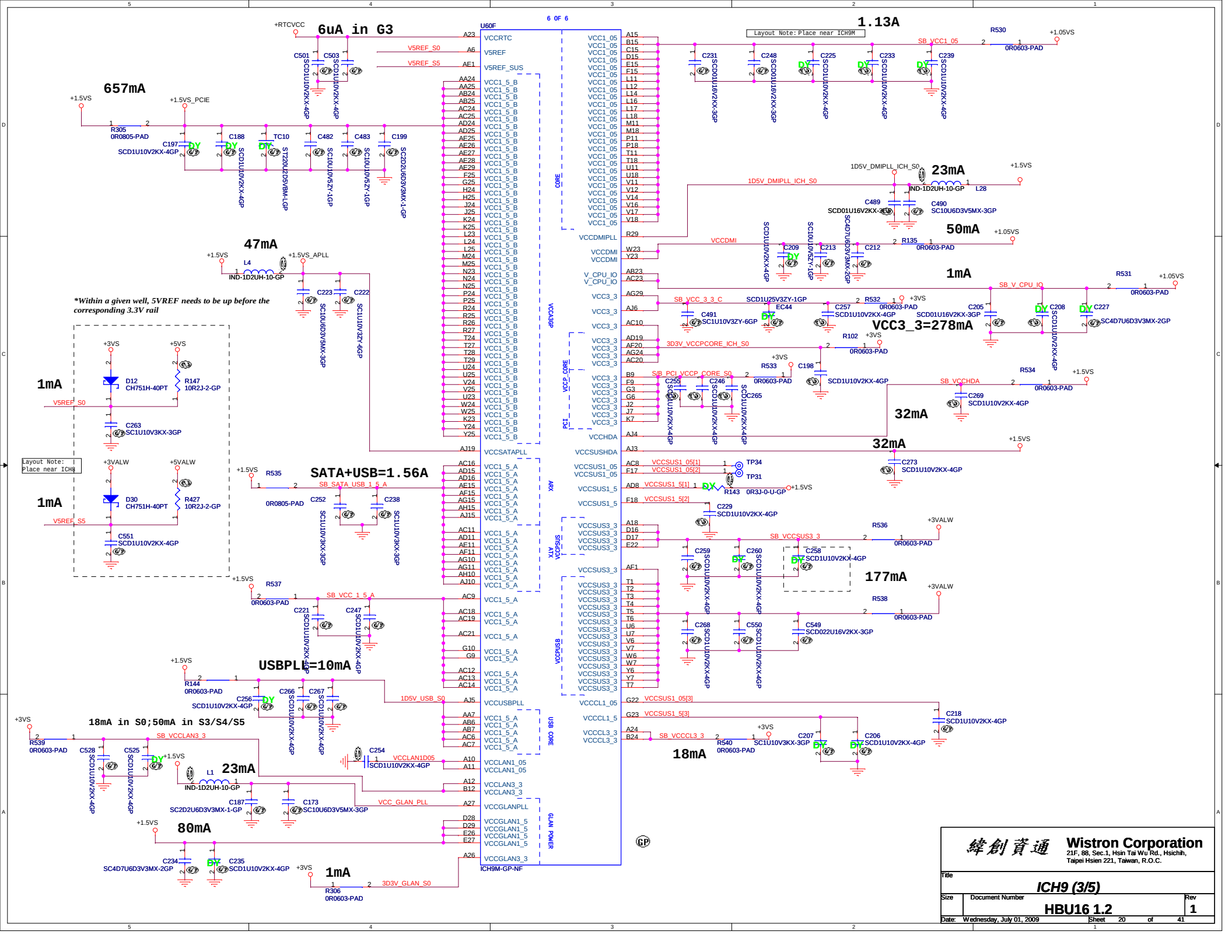
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

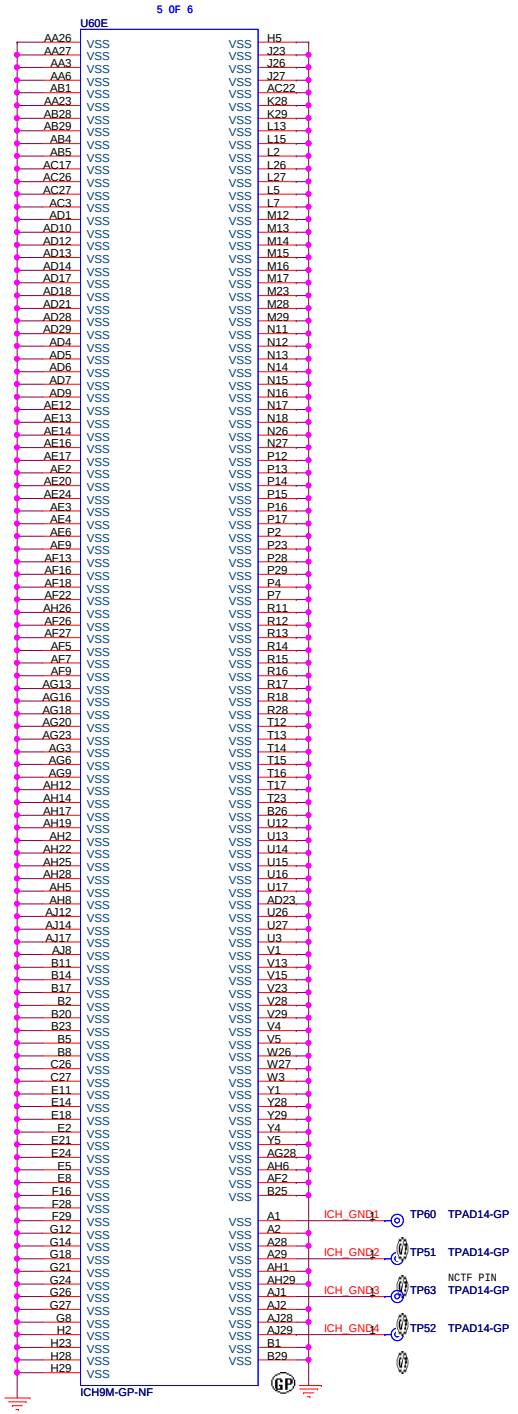
Title: ICH9-M (2 of 5)

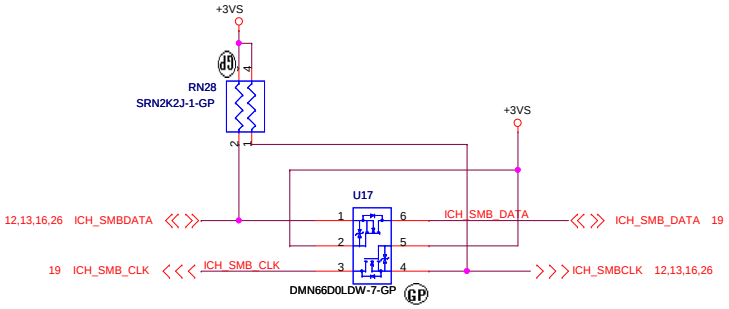
Size	Document Number	Rev
	HBU16 1.2	1

Date: Thursday, July 09, 2009 Sheet 18 of 41


U60C
3 OF 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
U60D
4 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
LAN
WLAN
Norn connect to charger
72.25X16.001 (2M Flash ROM)
W25X16VSSIG-GP
USB3
External USB3
External USB2
WLAN
Bluetooth
Card Reader
CAM
USB
Pair
Device
0
USB3
1
FREE
2
External USB3
3
FREE
4
External USB2
5
FREE
6
WLAN
7
BLUETOOTH
8
CARD READER
9
FREE
10
CAMERA
11
FREE
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 5)
Size
Document Number
HBU16 1.2
Rev
1
Date: Thursday, July 09, 2009
Sheet 19 of 41


6 OF 6
U60F
ICH9M-GP-NF
6uA in G3
657mA
47mA
1mA
1mA
SATA+USB=1.56A
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
1.13A
23mA
50mA
1mA
VCC3_3=278mA
32mA
32mA
177mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH9M
Layout Note: Place near ICH9
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9 (3/5)
Size
Document Number
HBU16 1.2
Rev
1
Date: Wednesday, July 01, 2009
Sheet 20 of 41





SMBUS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ICH9-M (4 of 4)*

Size	Document Number	Rev
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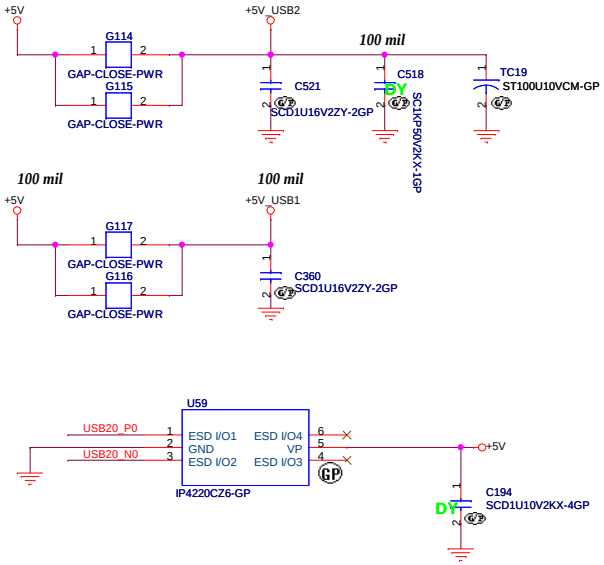
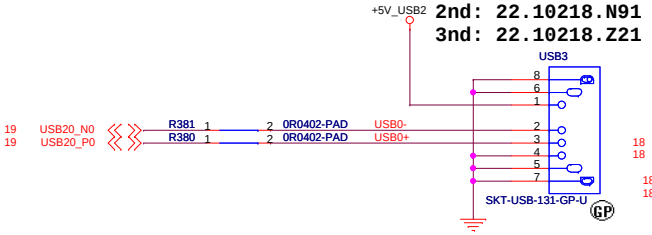
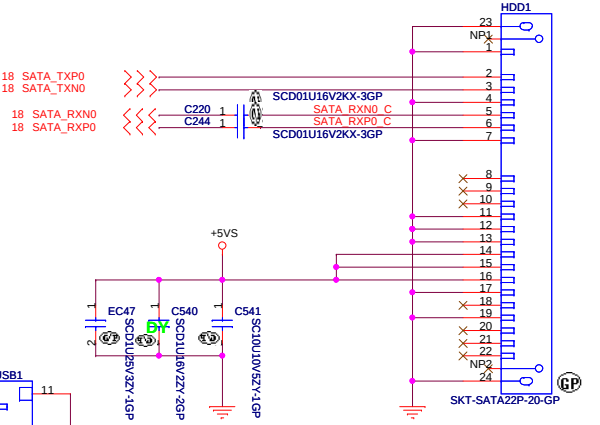
USB PORT



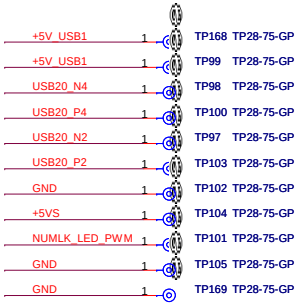
1st: 22.10218.N21
2nd: 22.10218.N91
3nd: 22.10218.Z21

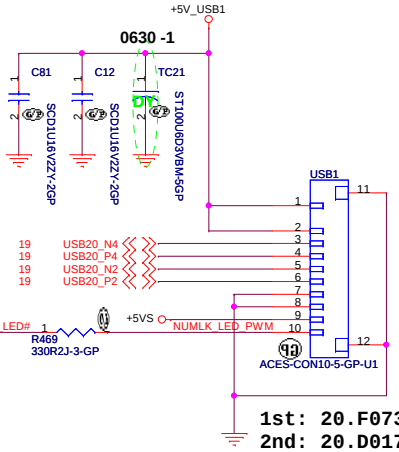


SATA HDD Connector

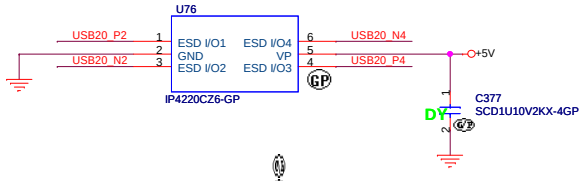


1st: 62.10065.261
2nd: 62.10065.511

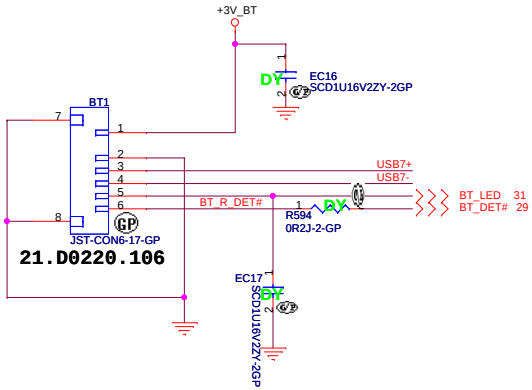


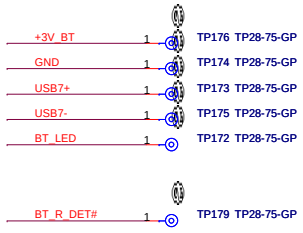


1st: 20.F0735.010
2nd: 20.D0174.110
3nd: 20.F0984.010



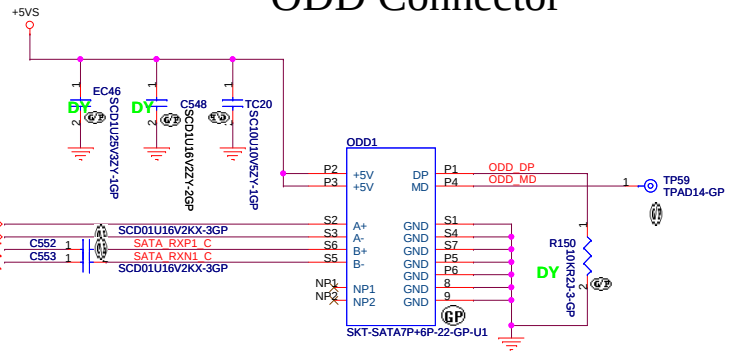
BLUETOOTH



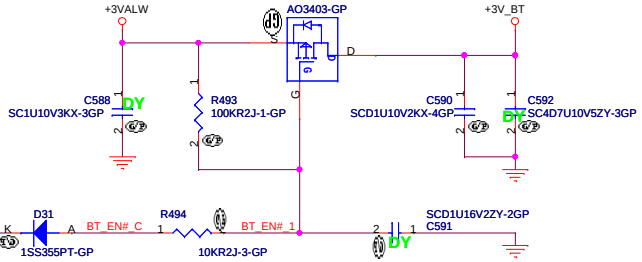


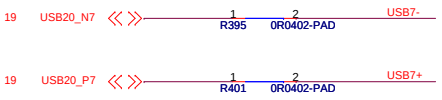
MAX 150mA

ODD Connector



1st: 62.10065.351
2nd: 62.10065.421
3nd: 62.10065.521





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/CDROM/USB/BT

Size	Document Number	Rev
A3	HBU16 1.2	1

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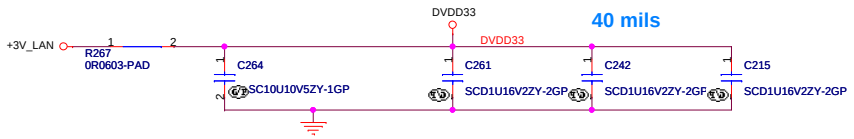
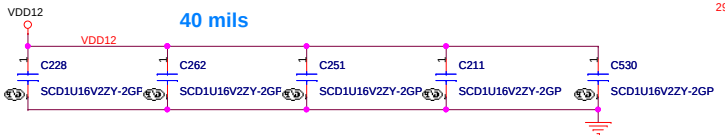
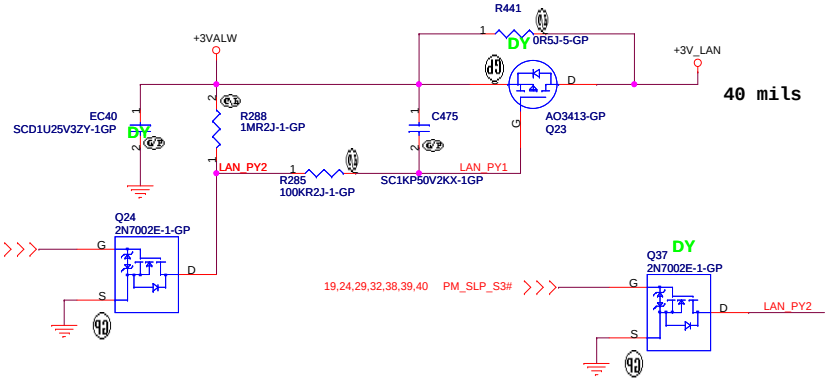
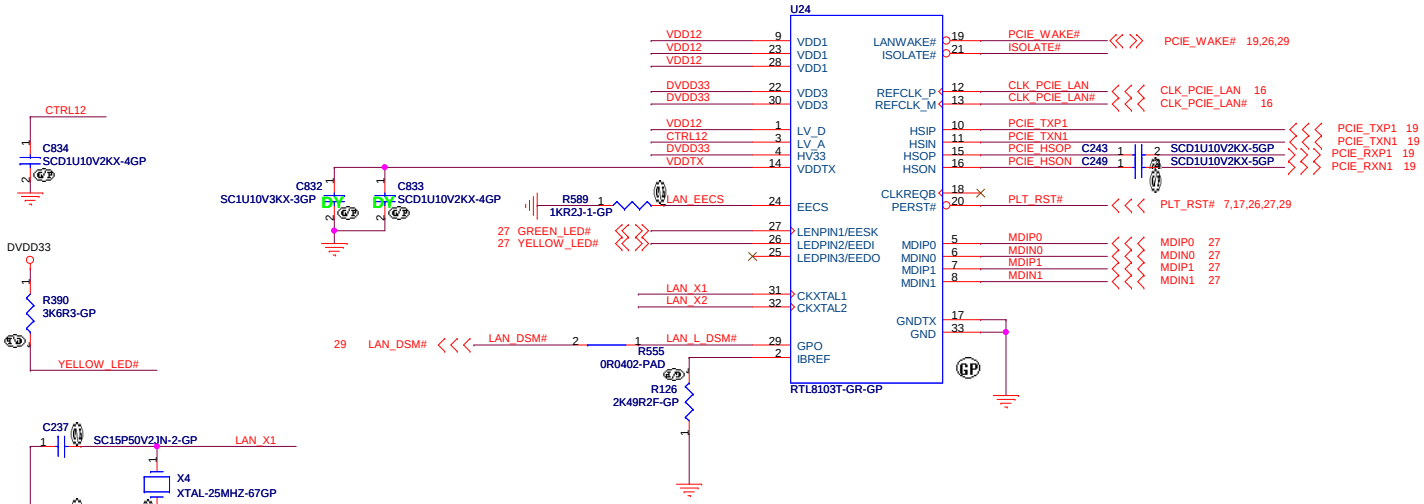
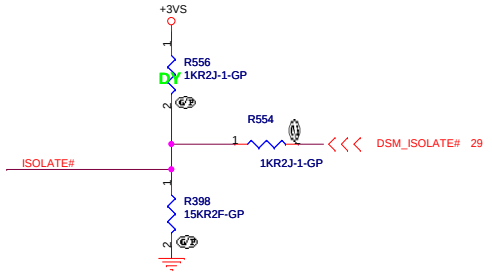






EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED1 : LINK (Green)
=> LED2 : ACT (Yellow)
(BOTH 10/100 AND GIGA CHIP)





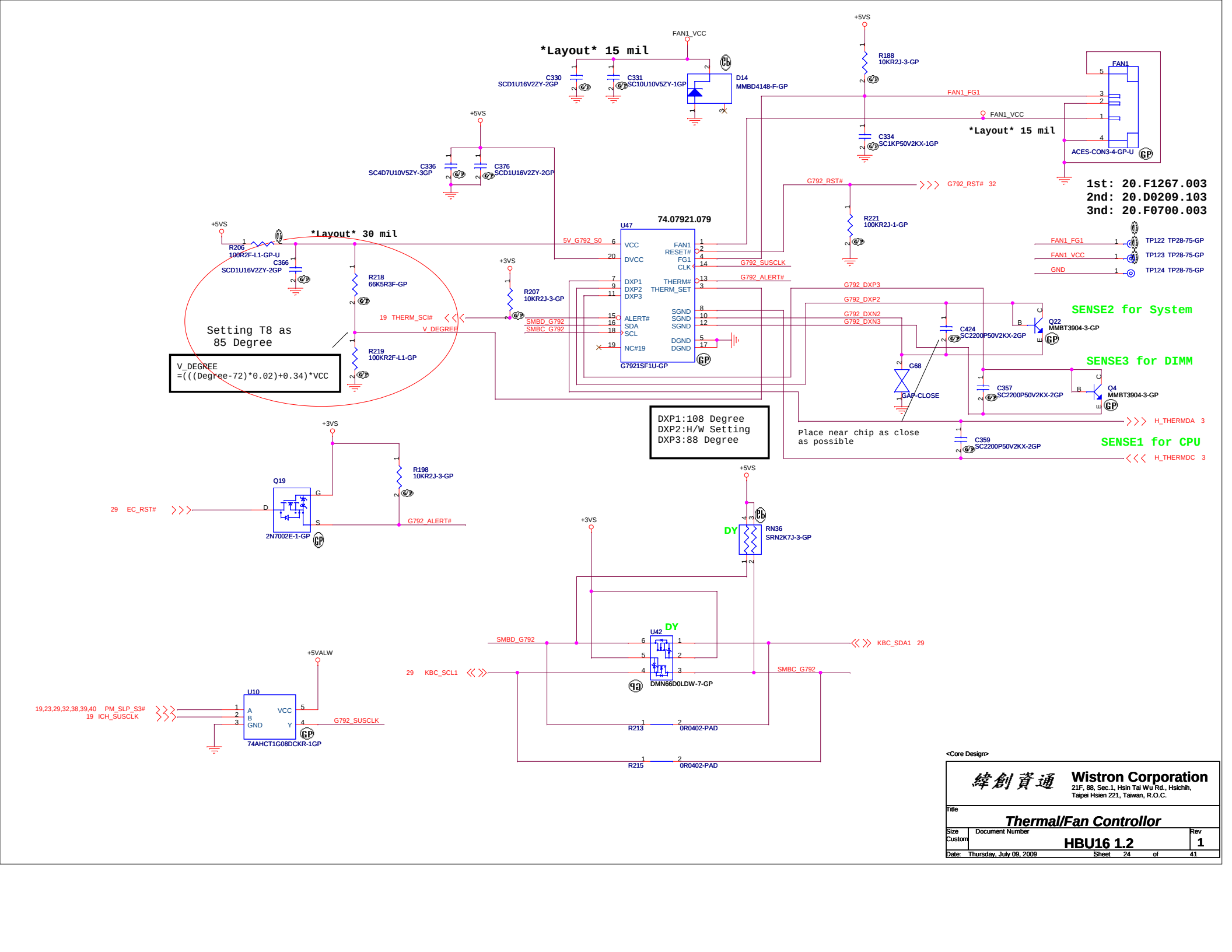
<Core Design>

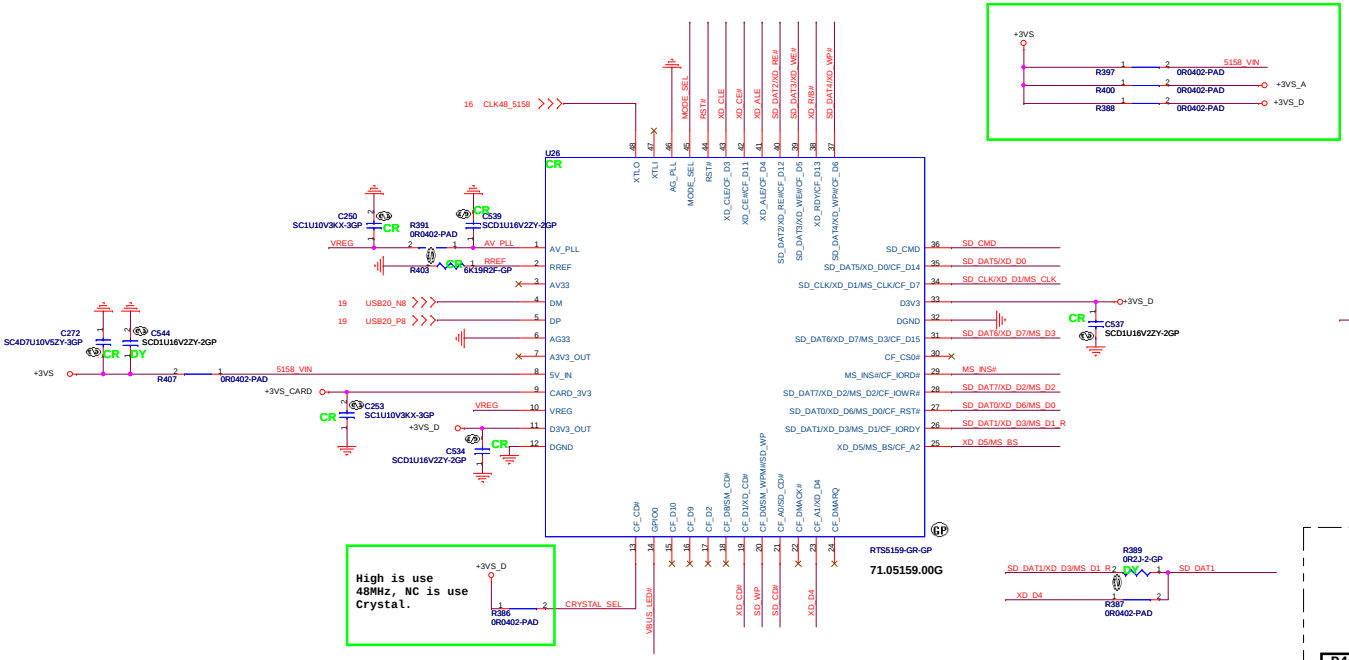
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

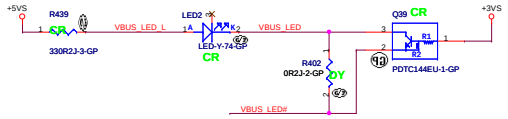
Title: **RTL8103T**

Size	Document Number	Rev
A3	HBU16 1.2	1

Date: Thursday, July 09, 2009 Sheet 23 of 41


Layout 15 mil
FAN1_VCC
C330
SCD1U16V2ZY-2GP
C331
SC10U10V5ZY-1GP
D14
MMBD4148-F-GP
+5VS
R188
10KR2J-3-GP
FAN1
FAN1_FG1
FAN1_VCC
Layout 15 mil
C334
SC1KP50V2KX-1GP
ACES-CON3-4-GP-U
C336
SC4D7U10V5ZY-3GP
C376
SCD1U16V2ZY-2GP
1st: 20.F1267.003
2nd: 20.D0209.103
3nd: 20.F0700.003
G792_RST#
G792_RST# 32
R221
100KR2J-1-GP
74.07921.079
U47
5V_G792_S0
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
SDA
SCL
NC#19
FAN1
RESET#
FG1
CLK
THERM#
THERM_SET
SGND
SGND
SGND
DGND
DGND
G792_SUSCLK
G792_ALERT#
G7921SF1U-GP
FAN1_FG1
FAN1_VCC
GND
TP122 TP28-75-GP
TP123 TP28-75-GP
TP124 TP28-75-GP
Layout 30 mil
R206
100R2F-L1-GP-U
C366
SCD1U16V2ZY-2GP
R218
66K5R3F-GP
R219
100KR2F-L1-GP
19 THERM_SCI#
V_DEGREE
R207
10KR2J-3-GP
SMBD_G792
SMBC_G792
Setting T8 as
85 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
G792_DXP3
G792_DXP2
G792_DXN2
G792_DXN3
SENSE2 for System
C424
SC2200P50V2KX-2GP
Q22
MMBT3904-3-GP
SENSE3 for DIMM
G68
GAP-CLOSE
C357
SC2200P50V2KX-2GP
Q4
MMBT3904-3-GP
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close
as possible
H_THERMDA 3
C359
SC2200P50V2KX-2GP
SENSE1 for CPU
H_THERMDC 3
R198
10KR2J-3-GP
Q19
29 EC_RST#
G792_ALERT#
2N7002E-1-GP
DY
RN36
SRN2K7J-3-GP
U42
SMBD_G792
KBC_SDA1 29
29 KBC_SCL1
SMBC_G792
DMN66D0LDW-7-GP
R213
0R0402-PAD
R215
0R0402-PAD
+5VALW
U10
19,23,29,32,38,39,40 PM_SLP_S3#
19 ICH_SUSCLK
G792_SUSCLK
74AHCT1G08DCKR-1GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Custom
Document Number
HBU16 1.2
Rev
1
Date: Thursday, July 09, 2009
Sheet 24 of 41



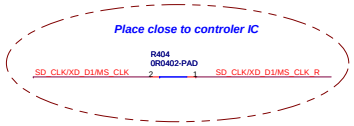


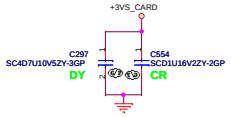
R405	C542	USB Auto De-link (*1)	MS Formatter (*2)	Description
0	NC	Yes	No	Recommended
NC	Install	Yes	Yes	
NC	NC	No	No	Compatible with RTS5158E

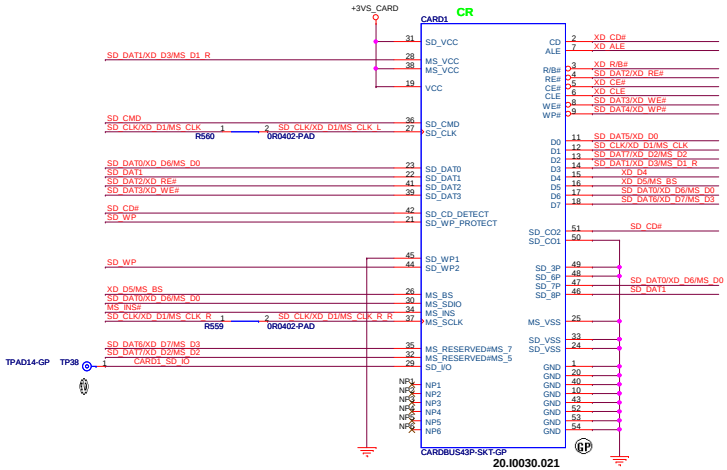
***1. USB Auto De-link mode:** If user remove memory card from socket, RTS5159 will terminate USB bus connection and enter power saving state.

***2. MS Formatter:** MSPRO, MSPRO DUO, MSPRO-HG or MSPRO-HG DUO card will be formatted as factory default setting if user formatted these card types under "Vista" OS.

4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)







<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

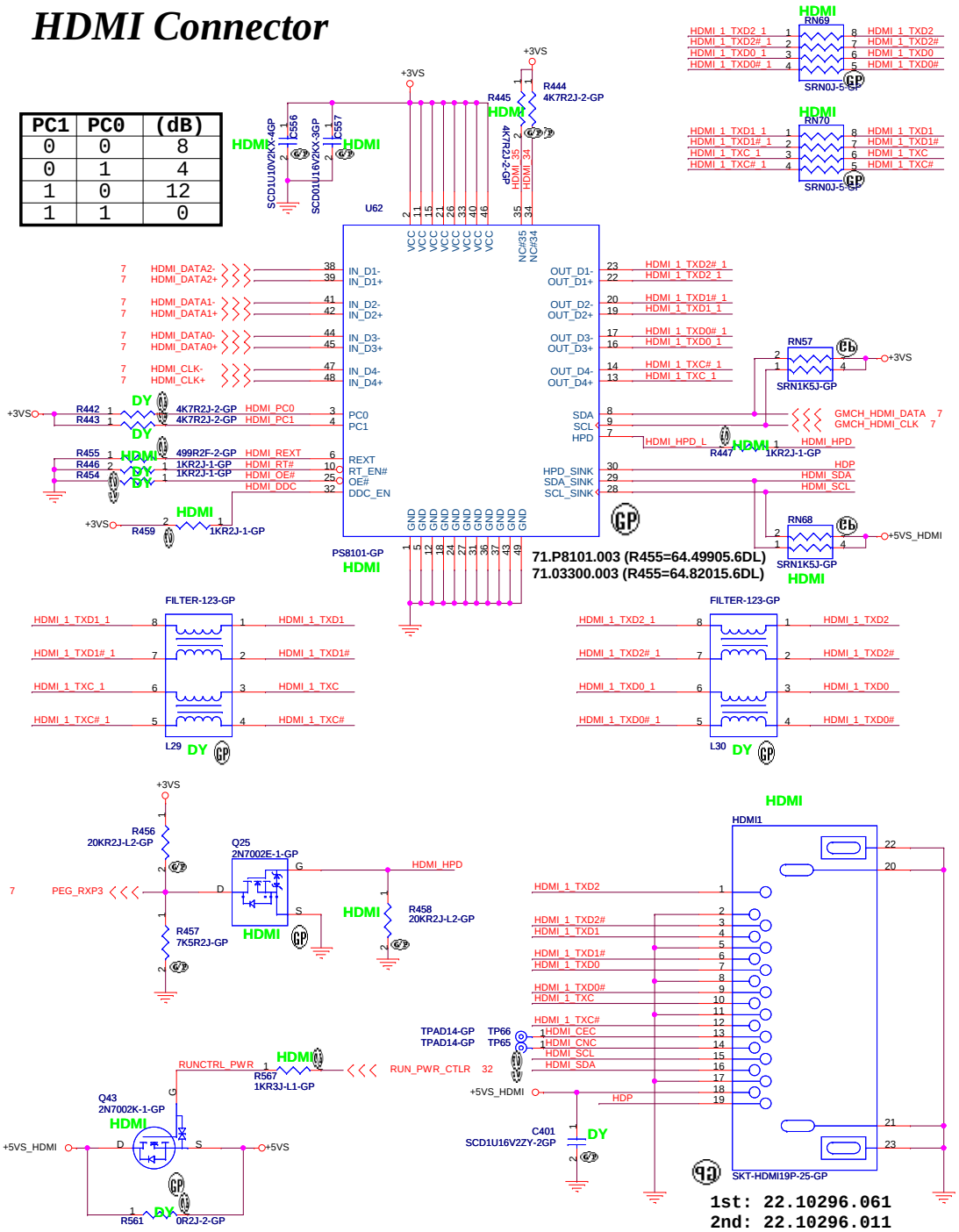
Title: **USB CardReader Controller-RTS5159**

Size	Document Number	Rev
	HBU16 1.2	1

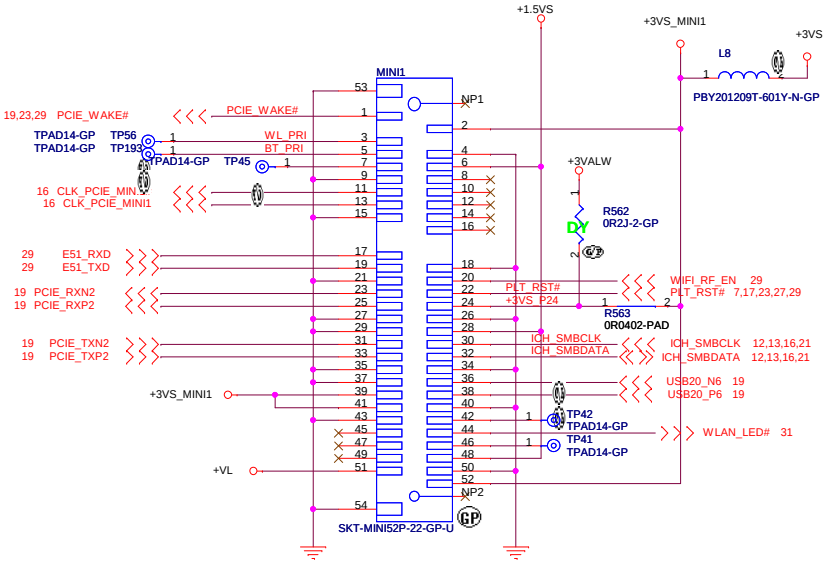
Date: Thursday, July 09, 2009 Sheet 25 of 41

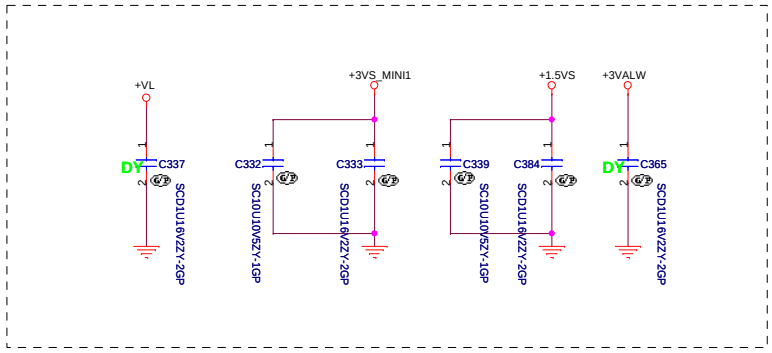
HDMI Connector

PC1	PC0	(dB)
0	0	8
0	1	4
1	0	12
1	1	0



Mini Card Connector1(802.11a/b/g)





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD/HDMI CONN .**

Size	Document Number	Rev
A3	HBU16 1.2	1

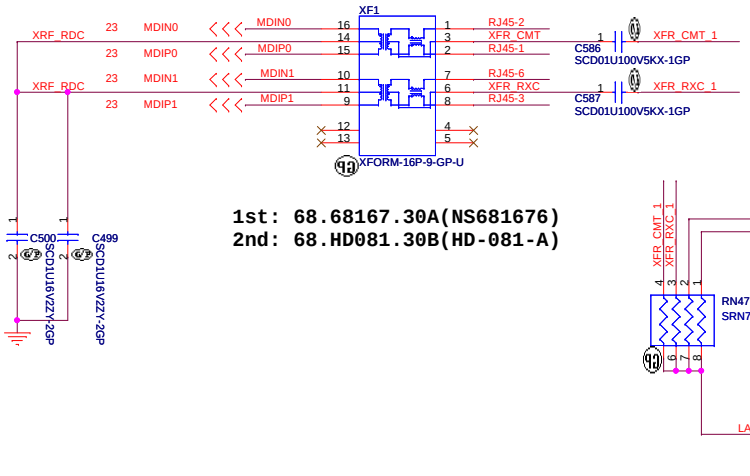
Date: Thursday, July 09, 2009 Sheet 26 of 41

LAN Connector

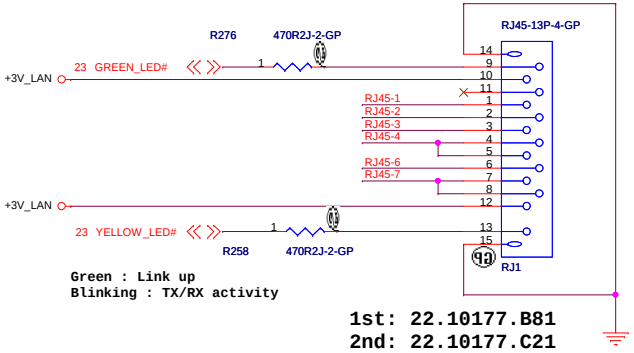
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW

10/100M Lan Transformer



1st: 68.68167.30A(NS681676)
2nd: 68.HD081.30B(HD-081-A)



Green : Link up
Blinking : TX/RX activity

1st: 22.10177.B81
2nd: 22.10177.C21

Remark:
Add trace width to 20mils for RJ1 pin4, 5 and pin 7, 8.

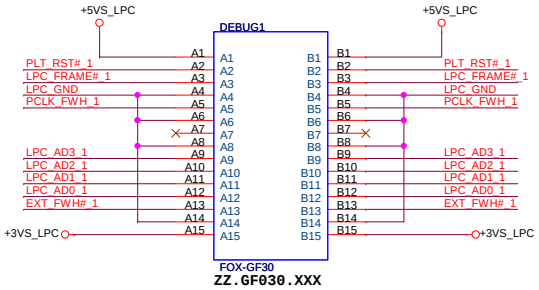
Golden Finger for Debug Board

TOP VIEW (A)

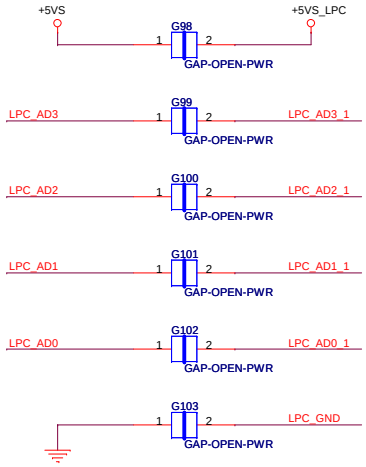
A15	(B1)
A14	(B2)
:	:
A2	(B14)
A1	(B15)

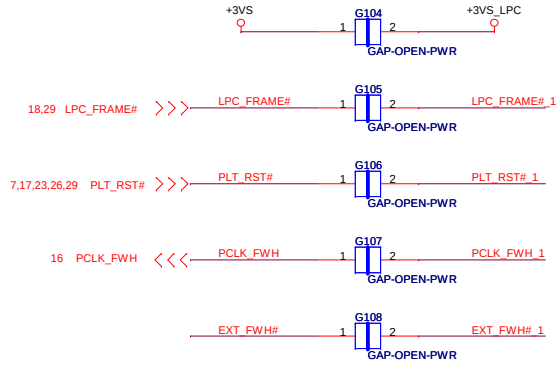
BOTTOM VIEW (B)

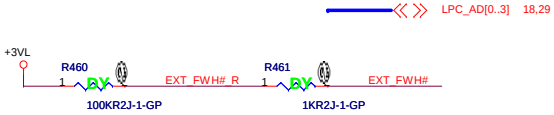
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



Please put near board edge.







CLOSE TO TRANSFORMER

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN CONN/Debug***

Size	Document Number	Rev
A3	**HBU16 1.2**	1

Date: Thursday, July 09, 2009 Sheet 27 of 41

PC BEEP GAIN CONTROL

GAIN	R568
-46 dB	DY
-18 dB	Install

SPDIF/BEEPGAIN is an input used to set the PC Beep gain while the device is in reset.

Default gain is -46 dB without populating the 10-Kohm pull-up resistor.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5VS_AUD to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.

2.5A (100mils)

Note:
In order for the audio codec to Wake on Jack, the CODEC VAUX pin (VAUX_3.3, pin2&6) must be powered by a rail that is not removed unless AC power is removed.

Close to Modem

Close to U32.

Close to U32.

Close to SPKR1.

0703 -1

0630 -1

0709 -1

1st: 83.R2003.E81
2nd: 83.BAT54.081
3nd: 83.00054.Q81

1st: 20.K0320.015
2nd: 20.K0343.015

Speaker

1st: 20.D0197.104
2nd: 20.F0984.004
3nd: 20.D0209.104

MIC

1st: 20.D0197.104
2nd: 20.F0984.004
3nd: 20.F0689.004

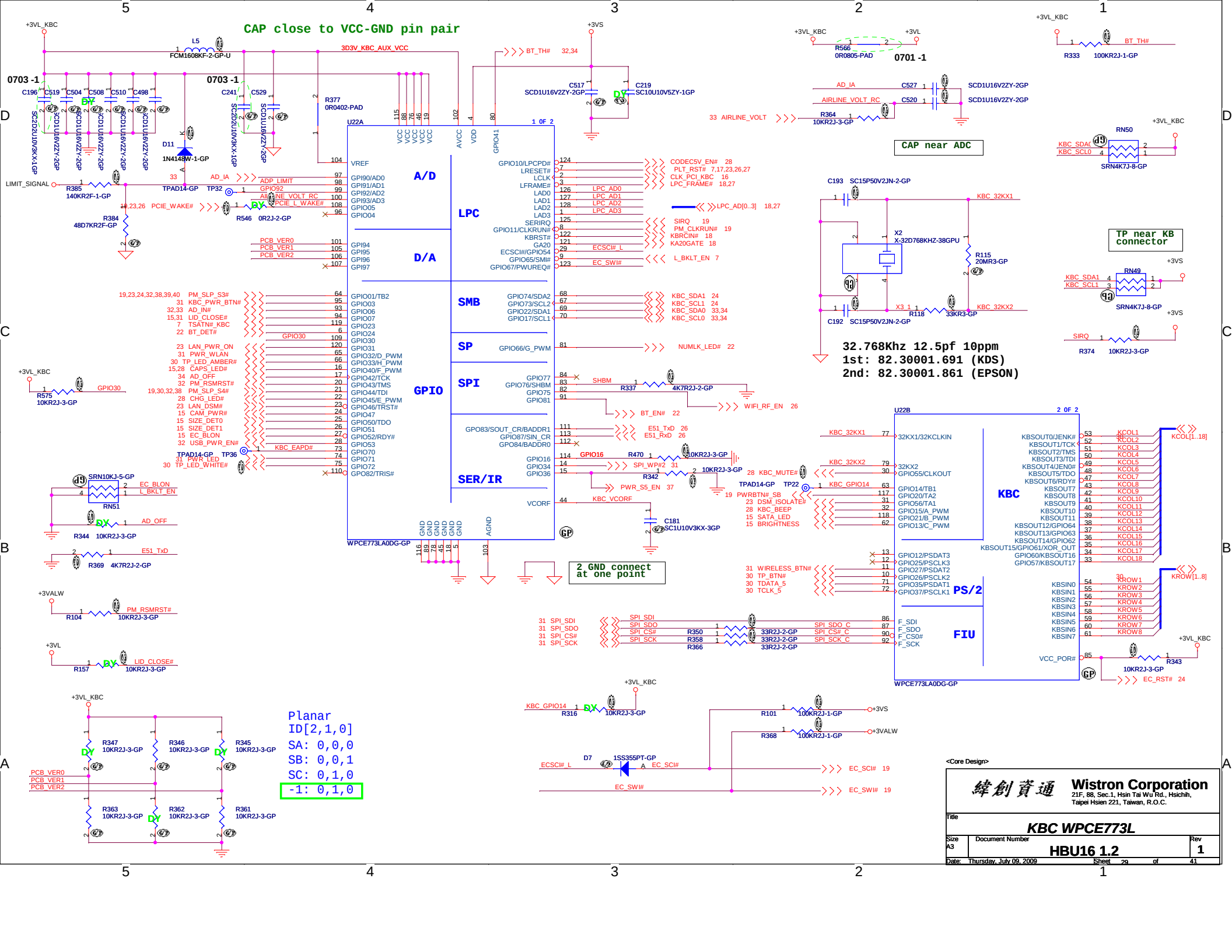
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

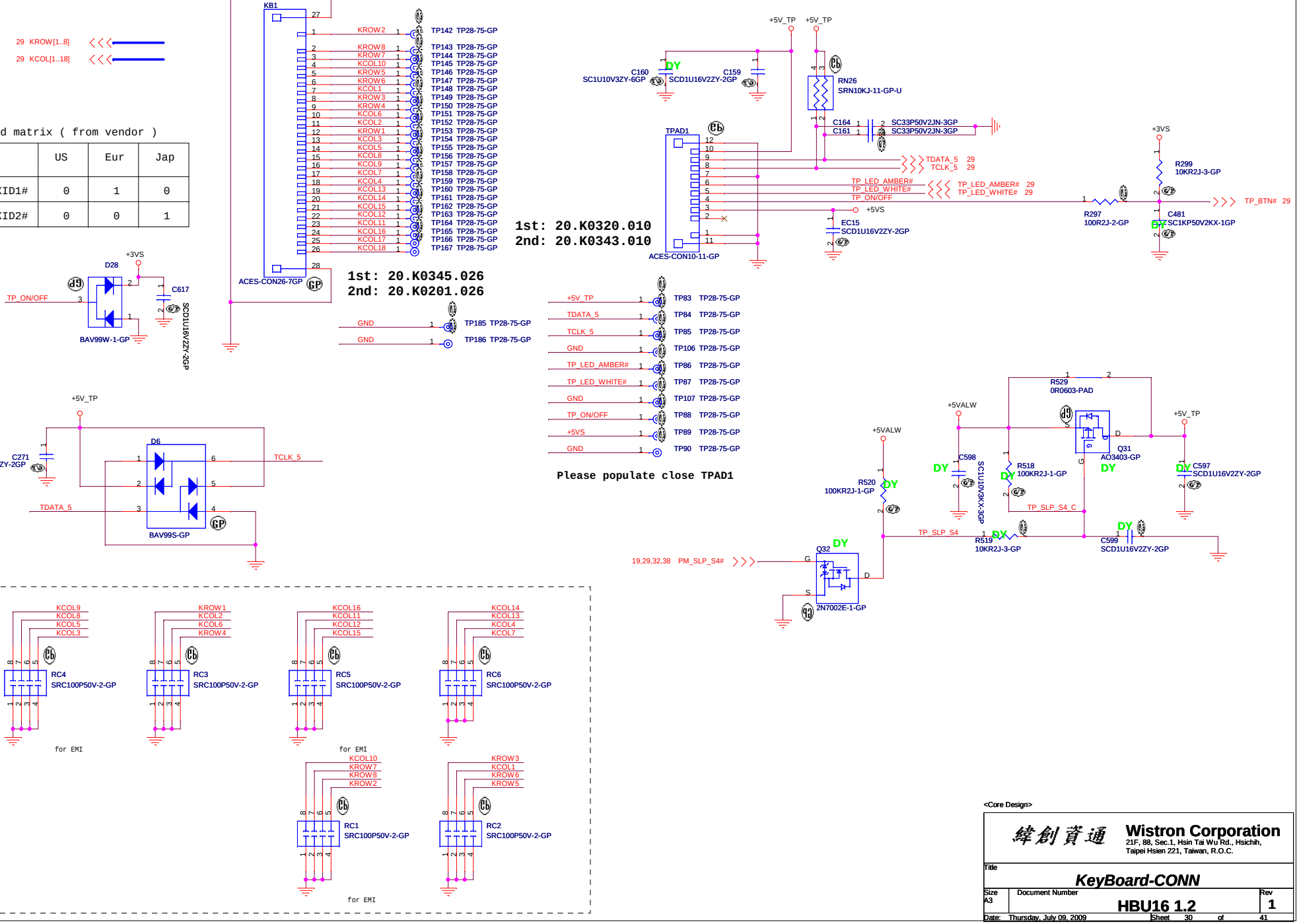
Title: AUDIO CODEC CX20583-11Z

Size: Custom | Document Number: HBU16 1.2 | Rev: 1

Date: Thursday, July 09, 2009 | Sheet 28 of 41


CAP close to VCC-GND pin pair
CAP near ADC
TP near KB connector
32.768Khz 12.5pf 10ppm
1st: 82.30001.691 (KDS)
2nd: 82.30001.861 (EPSON)
2 GND connect at one point
Planar ID[2,1,0]
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
-1: 0,1,0
U22A
U22B
WPCE773LA0DG-GP
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPCE773L
HBU16 1.2
Thursday, July 09, 2009

Internal KeyBoard Connector



Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

TouchPad Connector

1st: 20.K0320.010
2nd: 20.K0343.010

Please populate close TPAD1

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard-CONN

Size	Document Number	Rev
A3	HBU16 1.2	1

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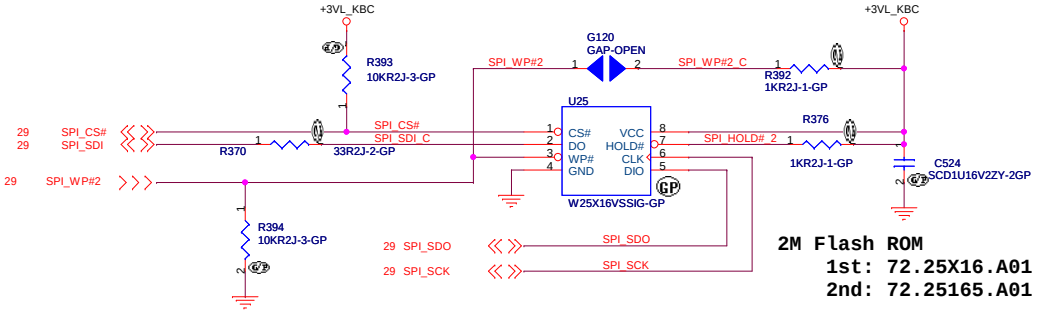
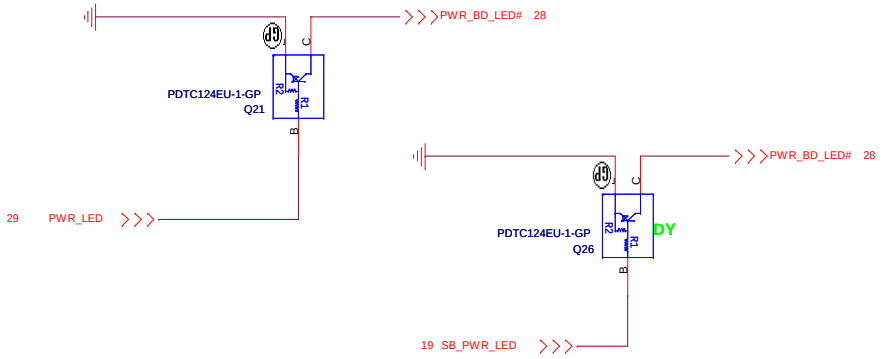
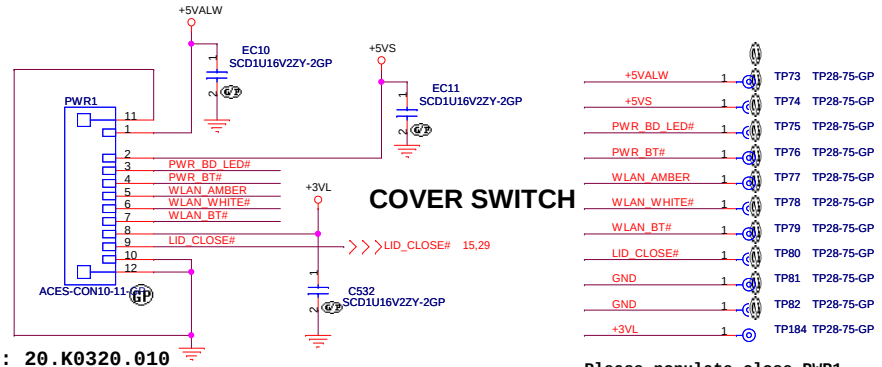


2M Flash ROM
1st: 72.25X16.A01
2nd: 72.25165.A01

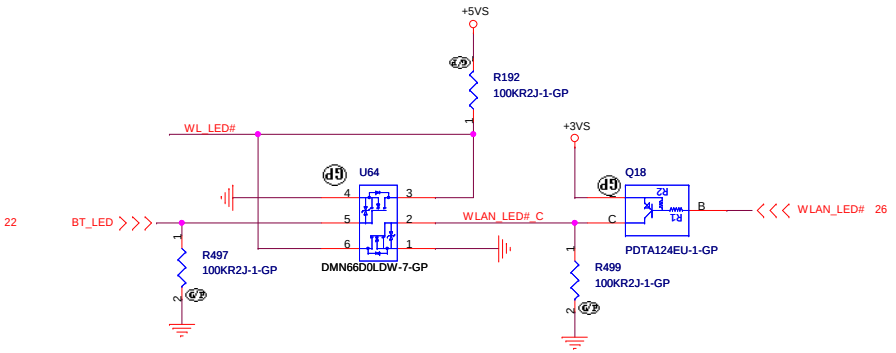




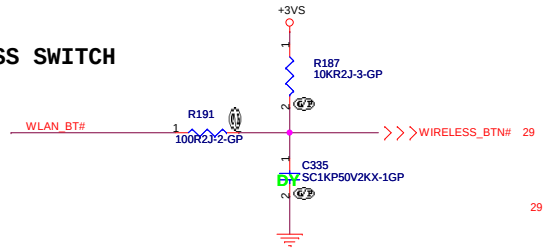
COVER SWITCH

1st: 20.K0320.010
2nd: 20.K0343.010

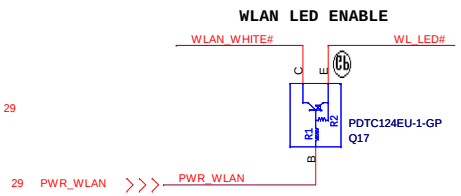
Please populate close PWR1



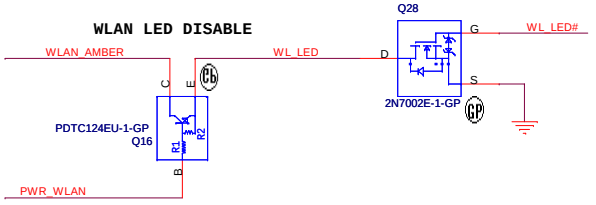
WIRELESS SWITCH

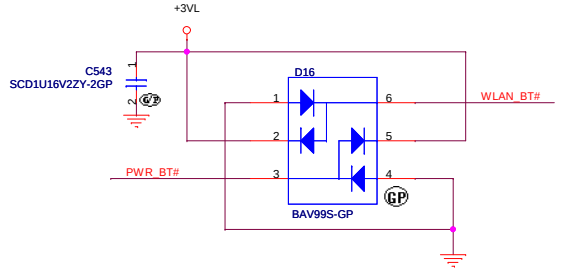


WLAN LED ENABLE

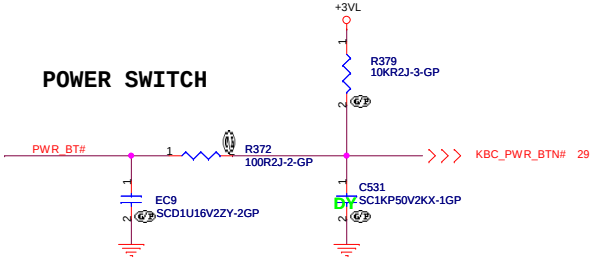


WLAN LED DISABLE





POWER SWITCH



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***FWH and CONN.***

Size	Document Number	Rev
A3	**HBU16 1.2**	1

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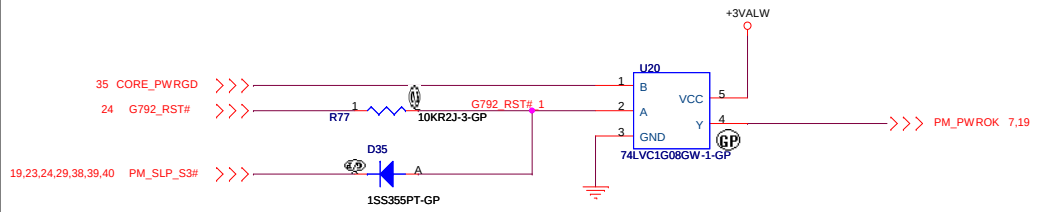
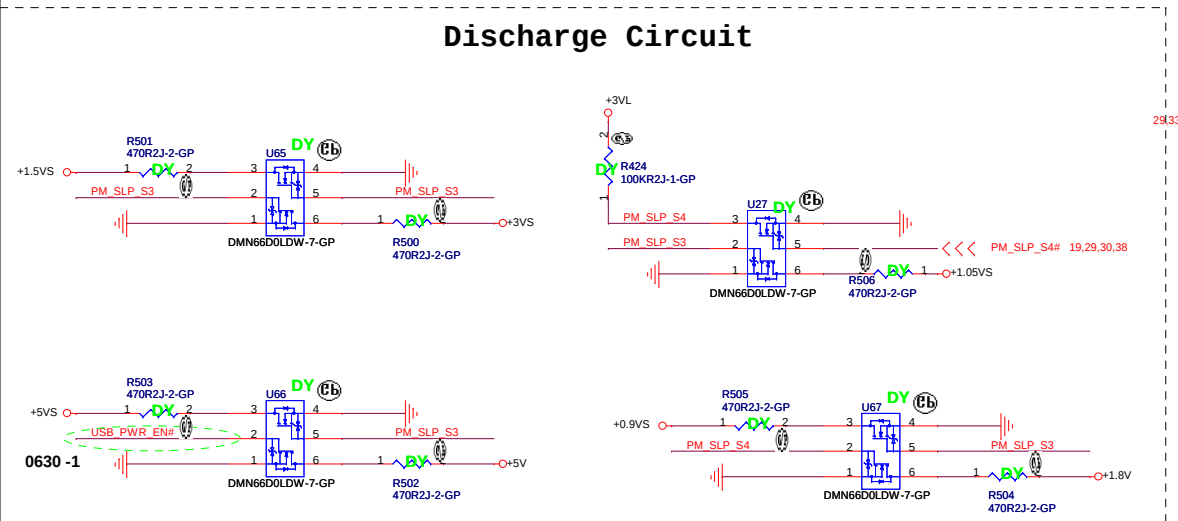
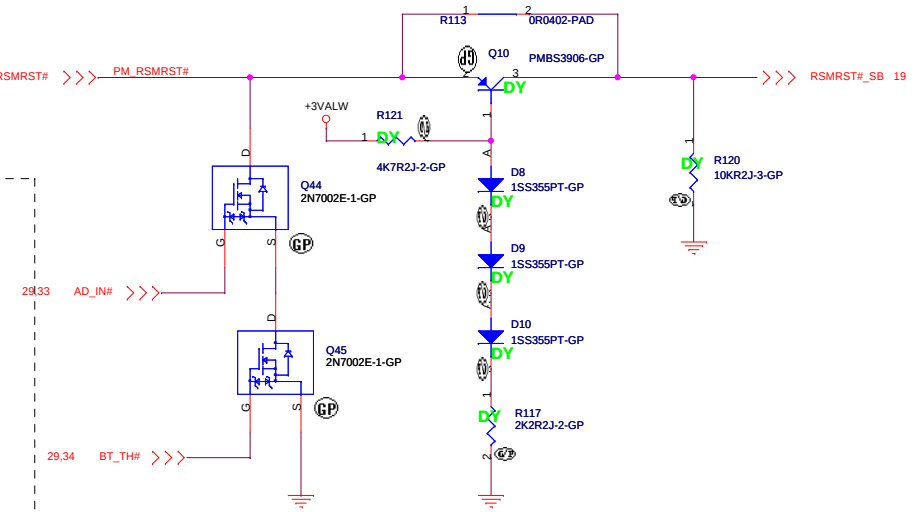
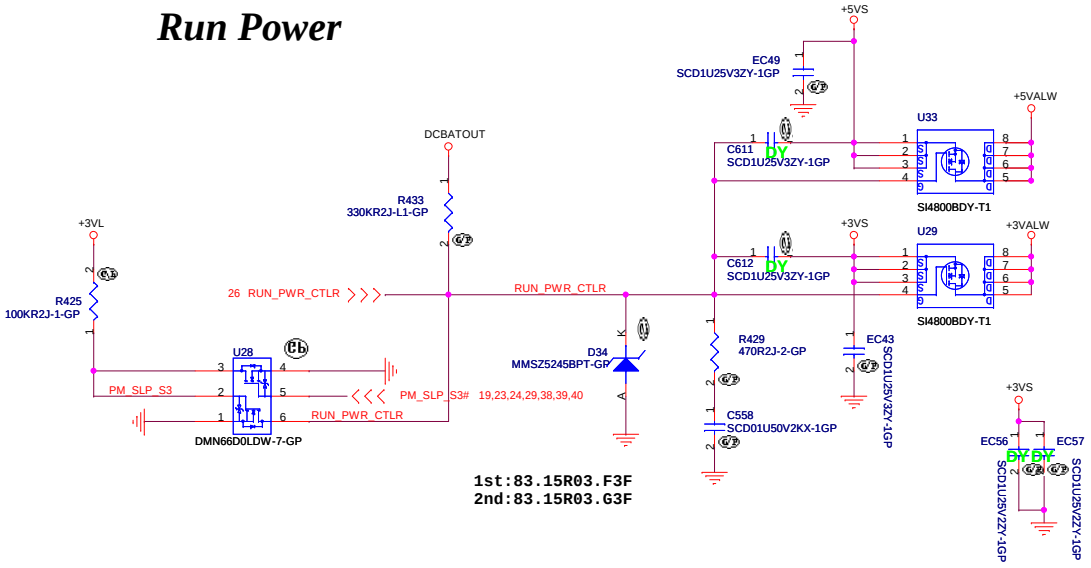






+5VALW to +5VS Transfer
+3VALW to +3VS Transfer

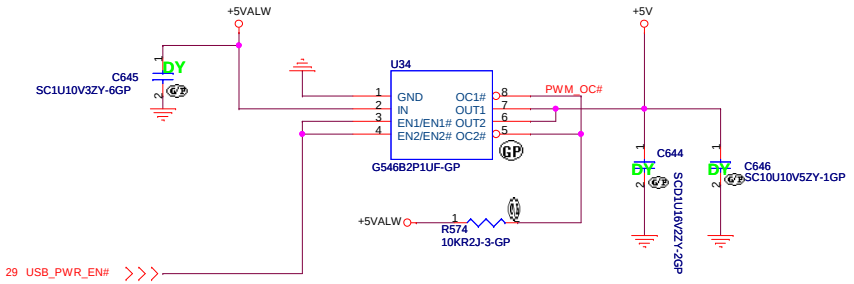
Run Power



1st:83.15R03.F3F
2nd:83.15R03.G3F

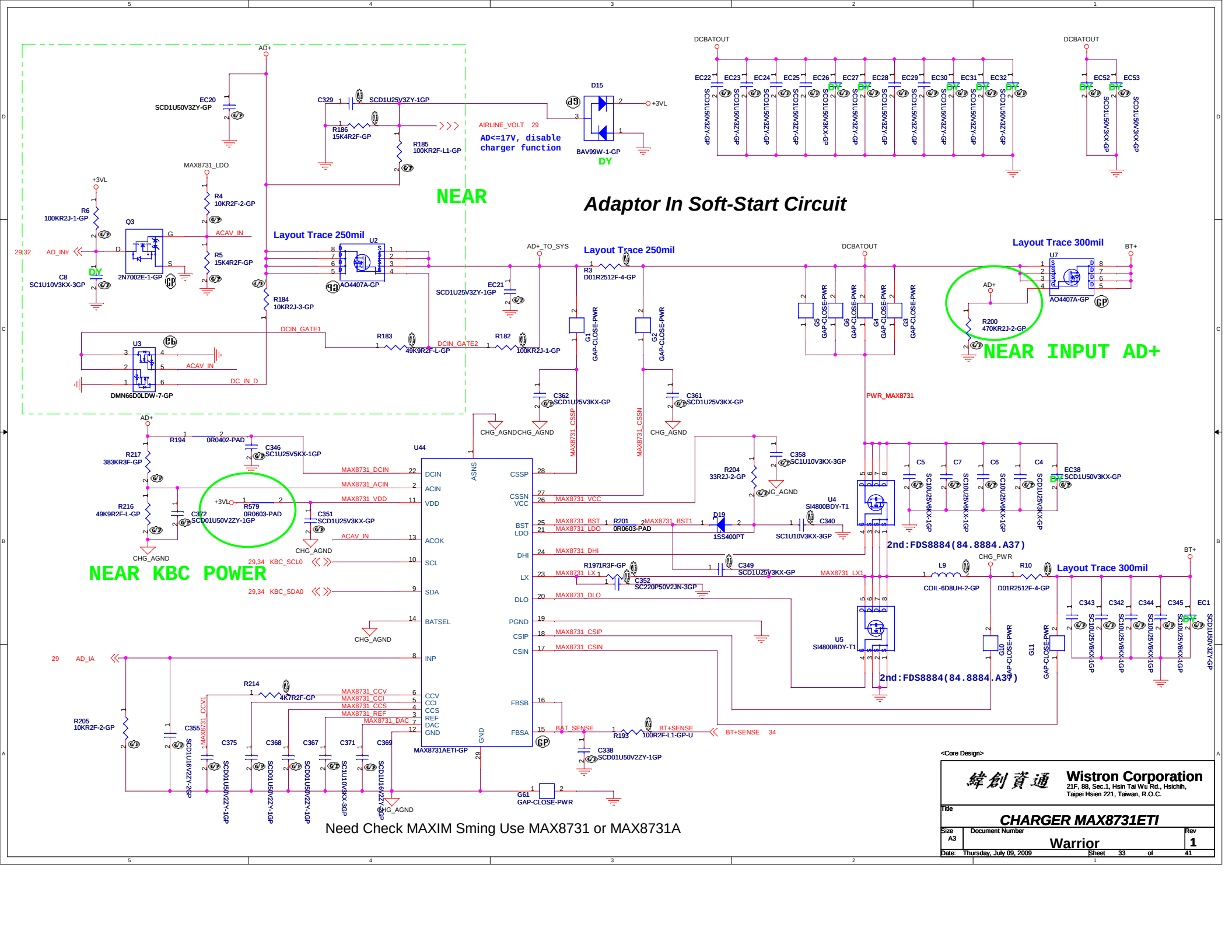
+5VALW to +5V Transfer

G546B2P1 Low active, 1.5A per channel

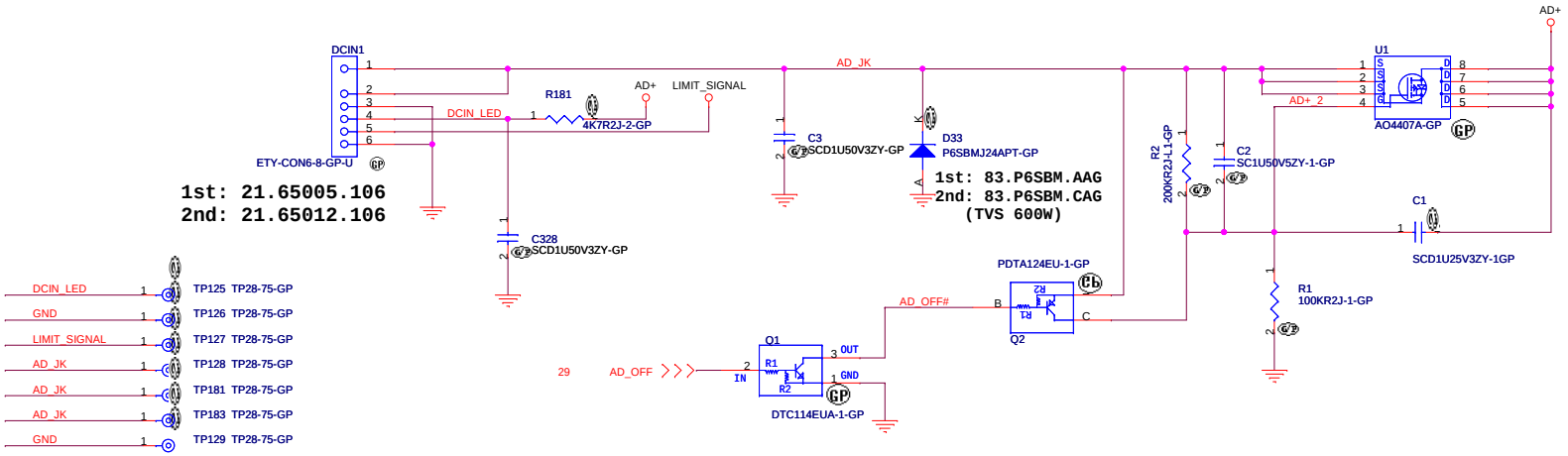


<Core Design>

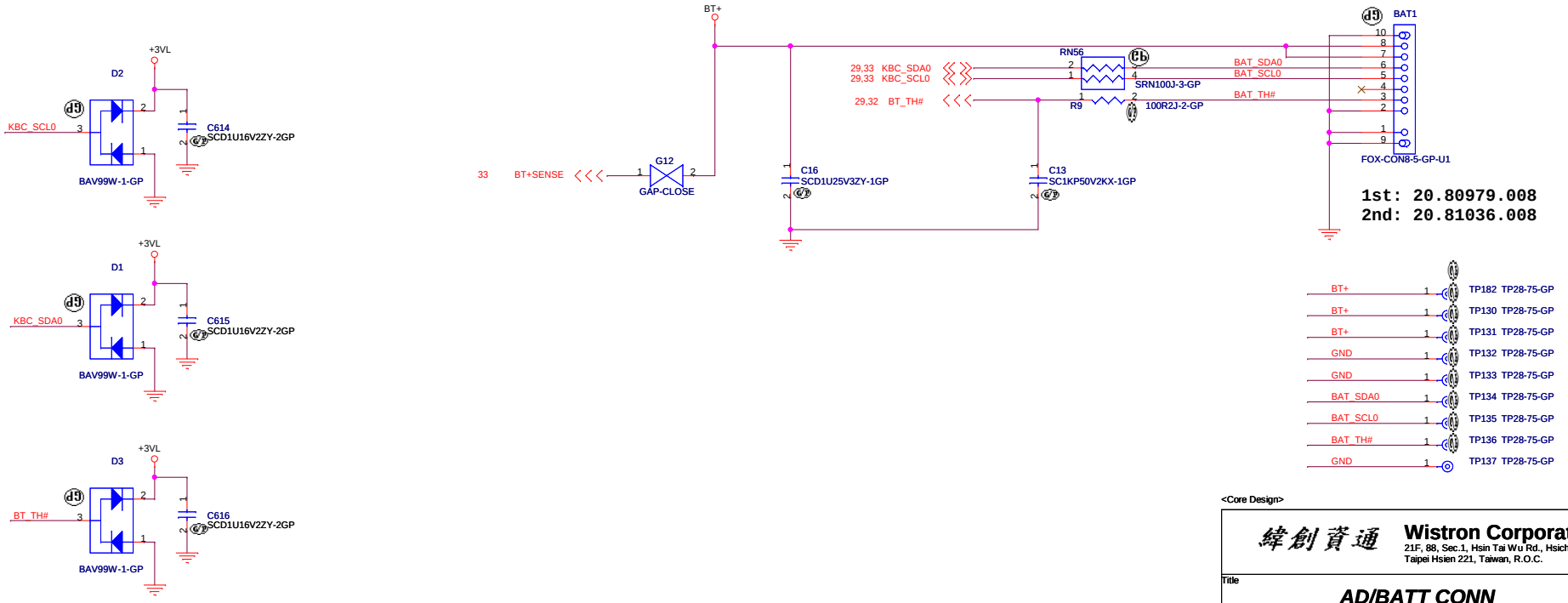
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PWRPLANE***	
Size A3	Document Number **HBU16 1.2**	Rev **1**
Date: Thursday, July 09, 2009	Sheet 32 of 41	


Adaptor In Soft-Start Circuit
NEAR
AD<=17V, disable charger function
Layout Trace 250mil
Layout Trace 300mil
NEAR INPUT AD+
NEAR KBC POWER
2nd:FDS8884(84.8884.A37)
Need Check MAXIM Sming Use MAX8731 or MAX8731A
MAX8731AETI-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8731ETI
Warrior
Thursday, July 09, 2009

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title: **AD/BATT CONN**

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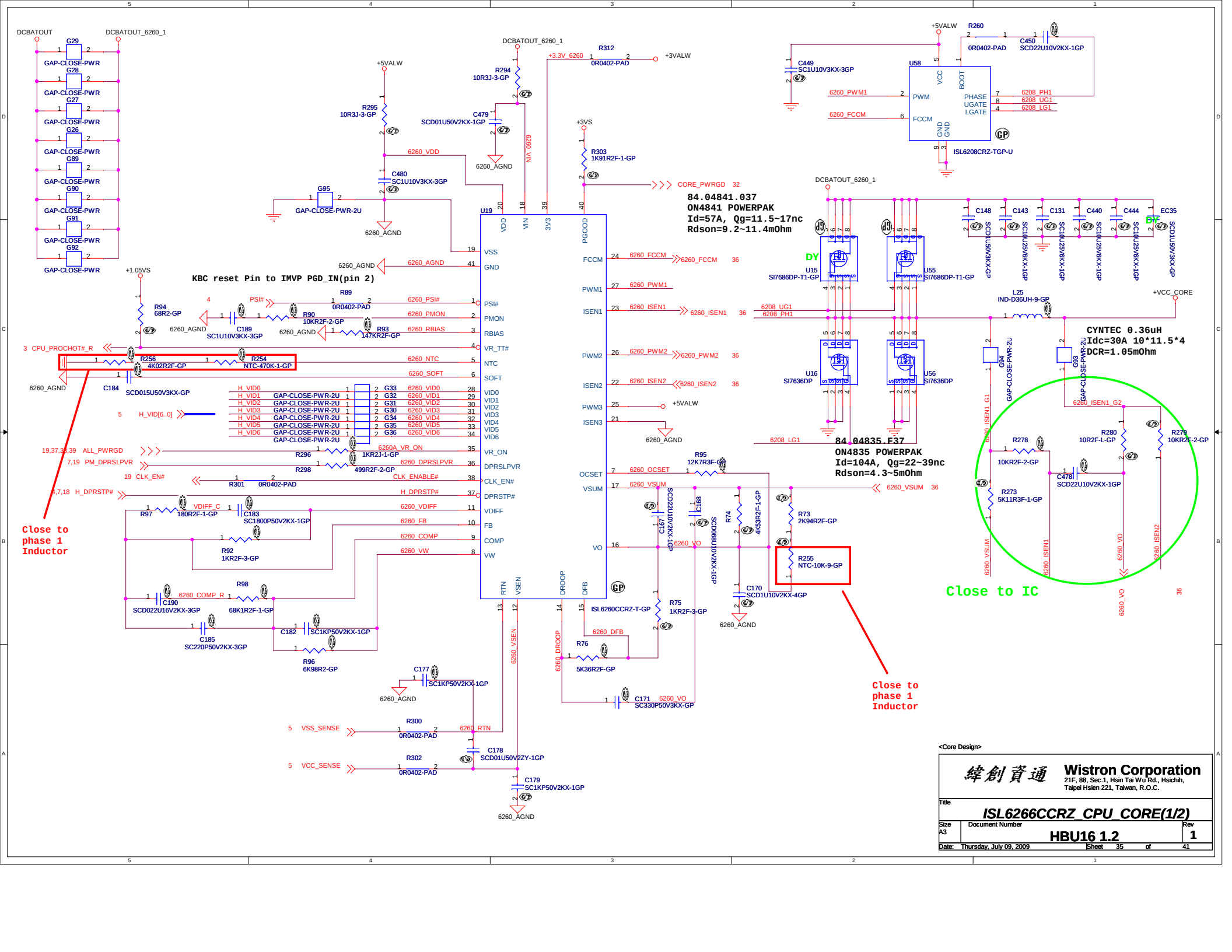
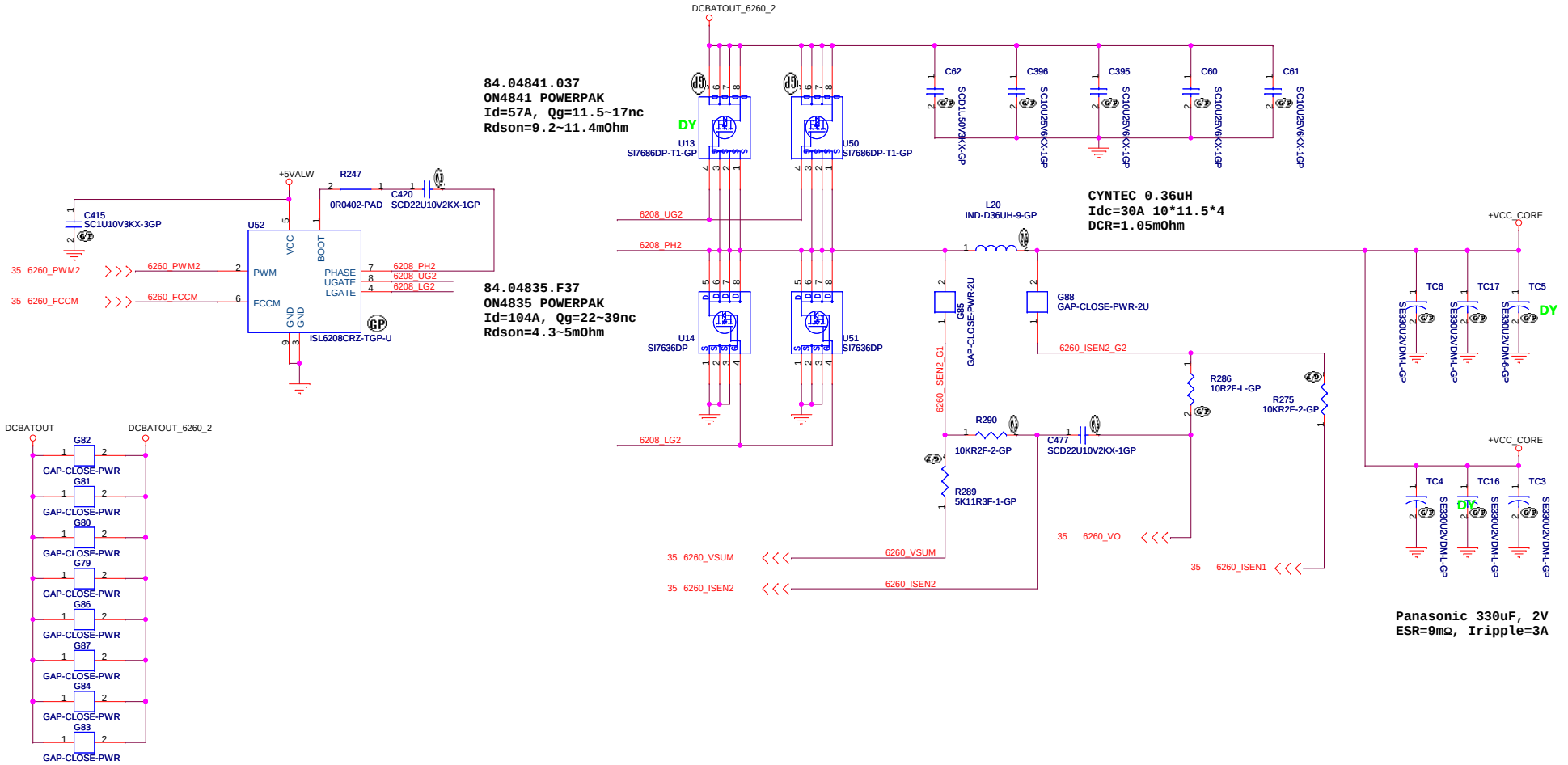

DCBATOUT
DCBATOUT_6260_1
GAP-CLOSE-PWR
+5VALW
+3VALW
+3VS
+1.05VS
6260_AGND
U19
ISL6260CCRZ-T-GP
KBC reset Pin to IMVP PGD_IN(pin 2)
84.04841.037
ON4841 POWERPAK
Id=57A, Qg=11.5~17nc
Rdson=9.2~11.4mOhm
84.04835.F37
ON4835 POWERPAK
Id=104A, Qg=22~39nc
Rdson=4.3~5mOhm
CYNTEC 0.36uH
Idc=30A 10*11.5*4
DCR=1.05mOhm
Close to phase 1 Inductor
Close to phase 1 Inductor
Close to IC
ISL6208CRZ-TGP-U
SI7686DP-T1-GP
SI7636DP
+VCC_CORE
CORE_PWRGD
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266CCRZ_CPU_CORE(1/2)
HBU16 1.2
Thursday, July 09, 2009



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Title	***ISL6260CCRZ_CPU_CORE(2/2)***
Size: A3	Document Number: **HBU16 1.2** Rev: **1**
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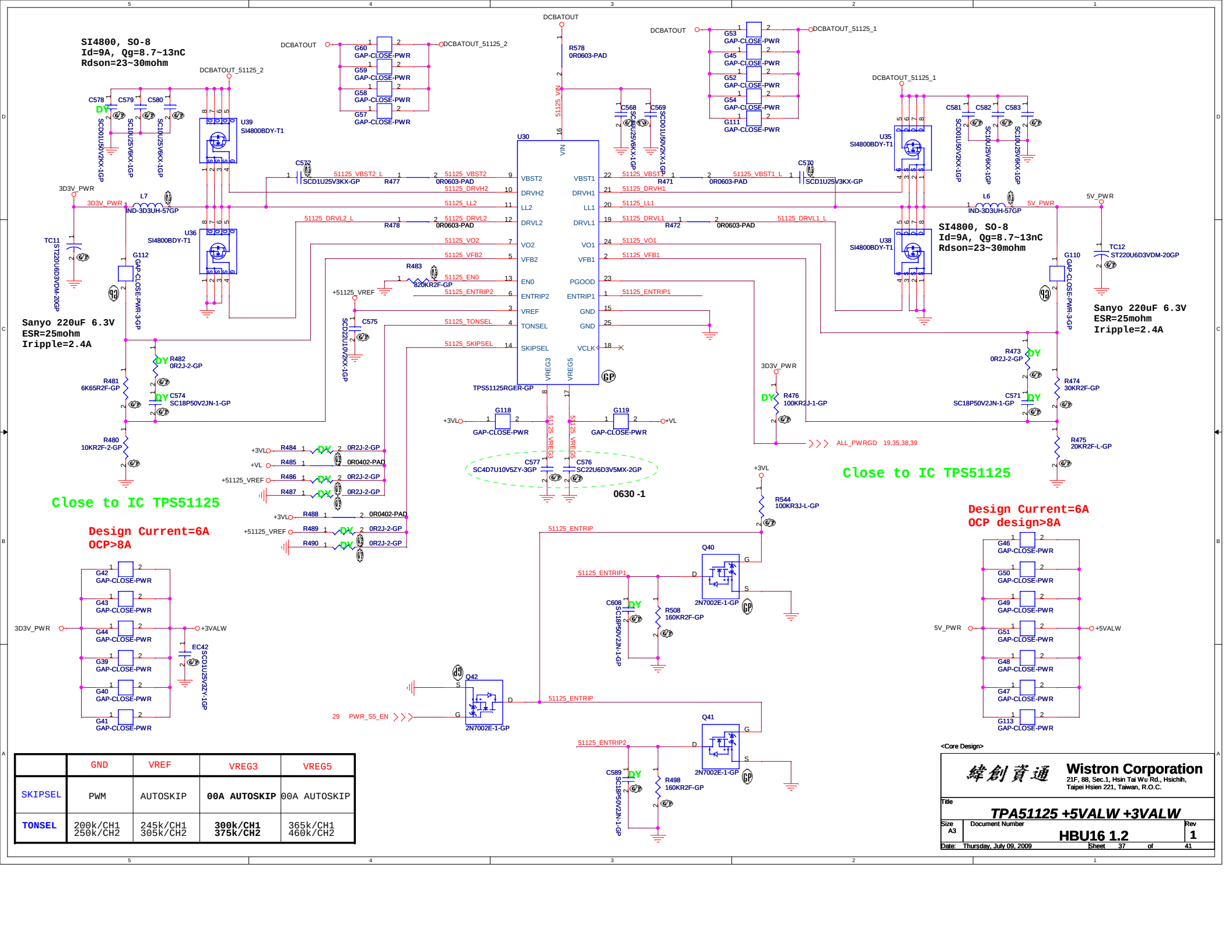

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	**00A AUTOSKIP**	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	**300k/CH1** **375k/CH2**	365k/CH1 460k/CH2

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Title: TPA51125 +5VALW +3VALW

Size: A3 | Document Number: HBU16 1.2 | Rev: 1

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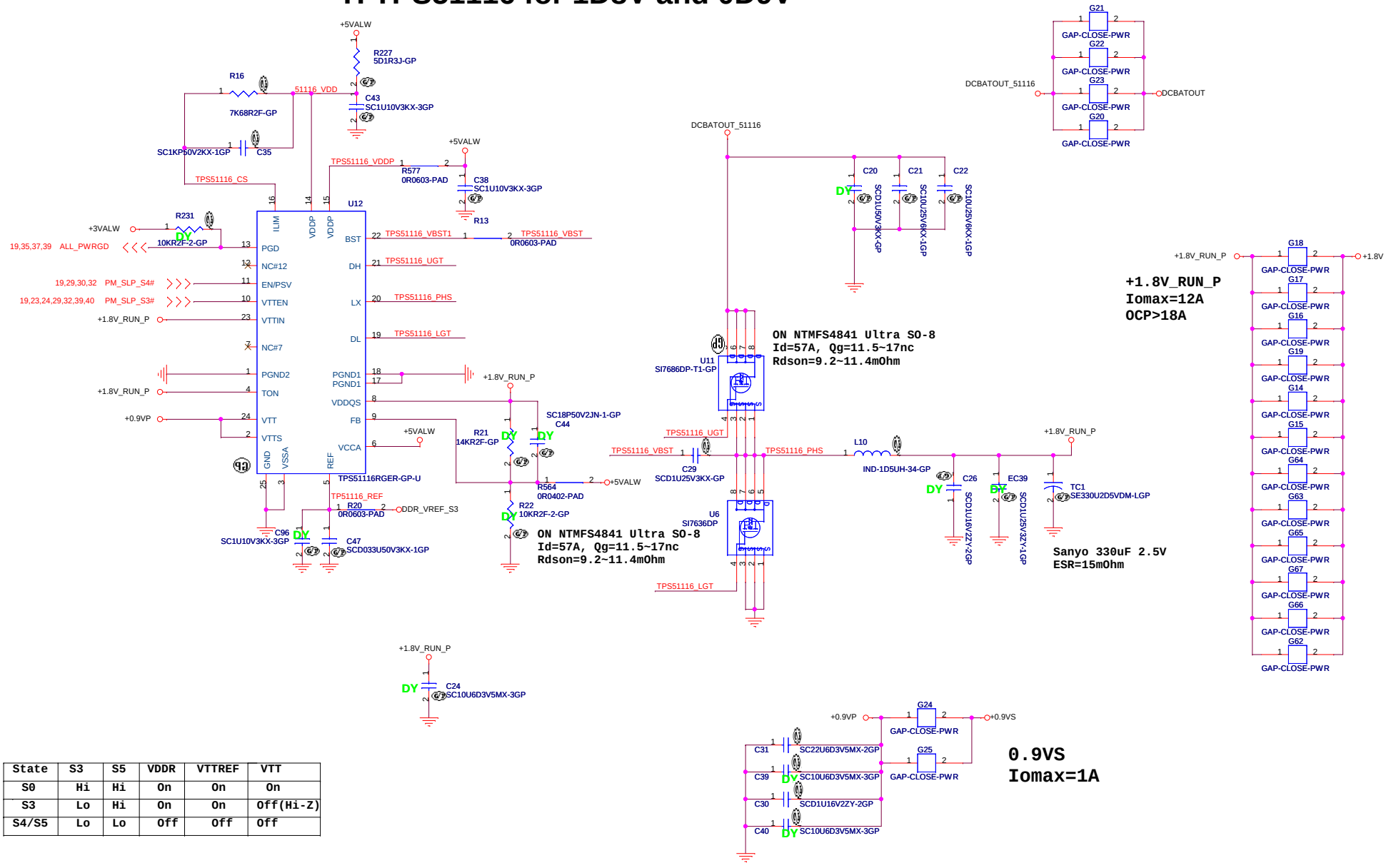
TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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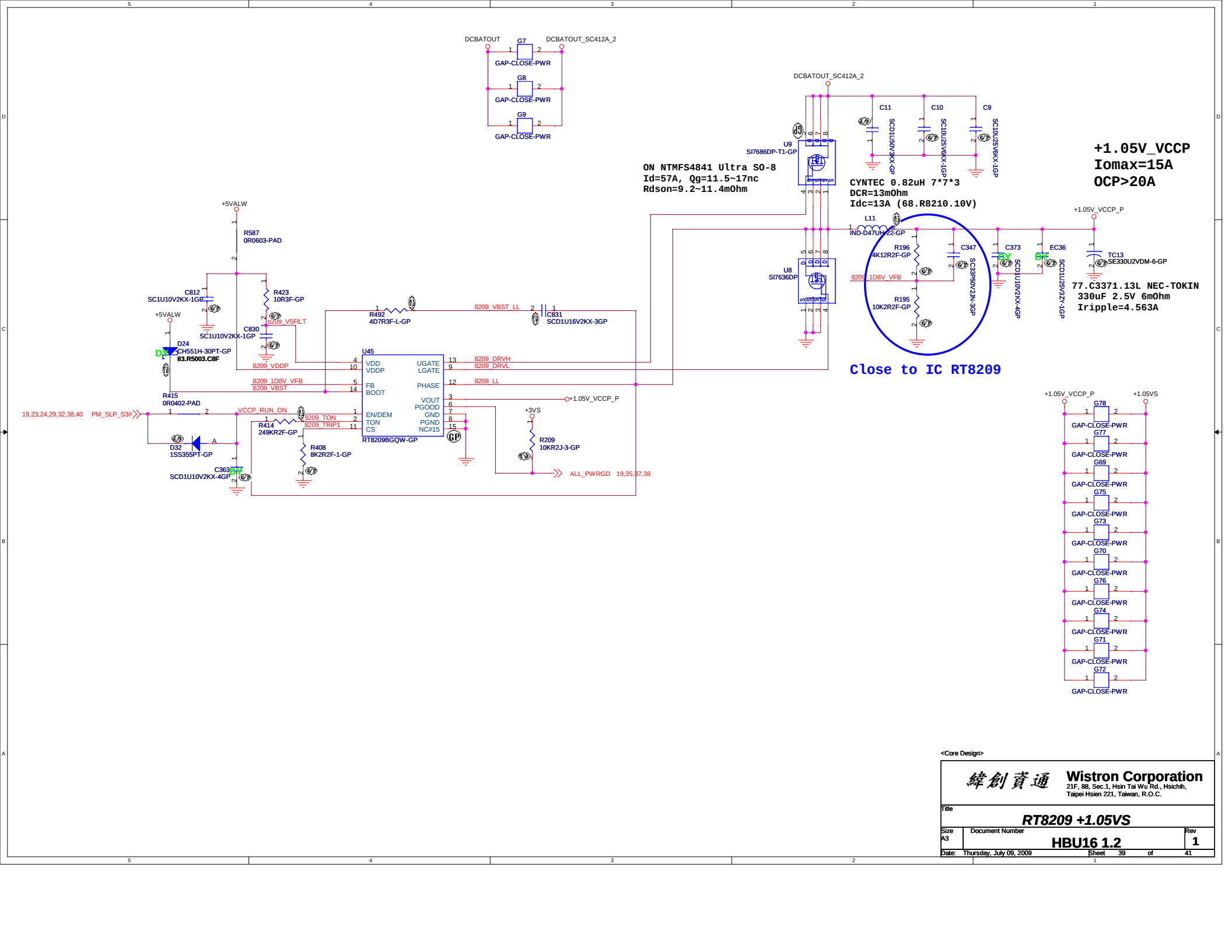
Title: TPS51116 1D8V/0D9V

Size: A3 | Document Number: HBU16 1.2 | Rev: 1

Date: Thursday, July 09, 2009 | Sheet 38 of 41



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Title: RT8209 +1.05VS

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A3	HBU16 1.2	1

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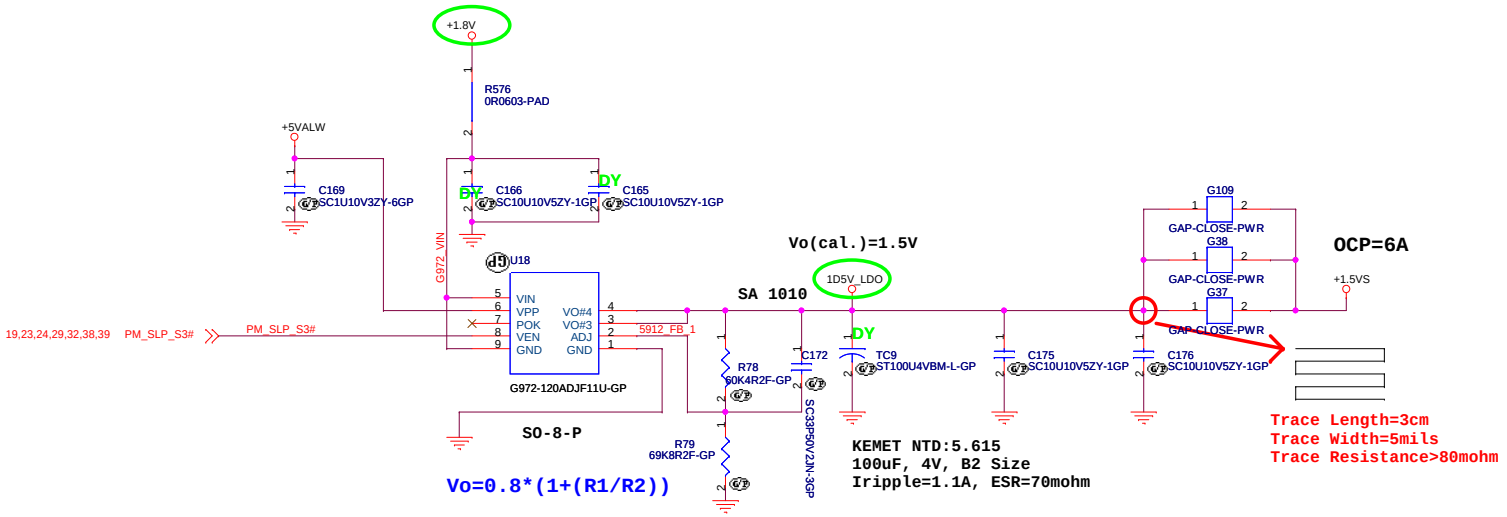

1st: 74.00972.031(GMT)
2nd: 74.05912.A71(Anpac)

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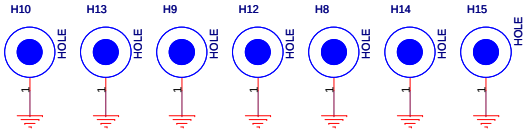
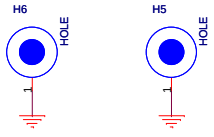
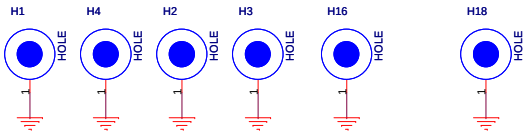
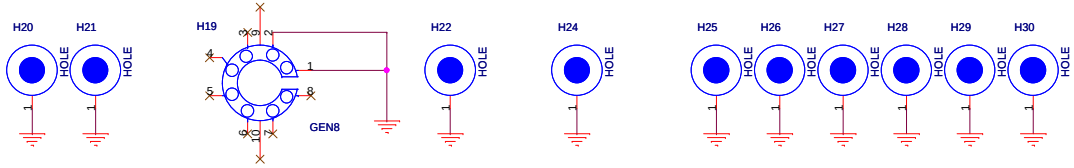
Taipei Hsien 221, Taiwan, R.O.C.

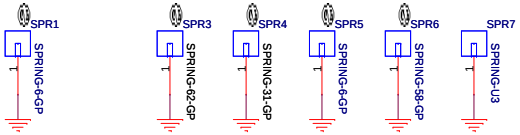
Title	GMT_1D5V_LDO	
Size: A3	Document Number: HBU16 1.2	Rev: 1
Date: Thursday, July 09, 2009	Sheet 40 of 41	











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SPR6: 34.4B312.002, 34.4B312.101
SPR7: 34.40U07.001, 34.40U07.101

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Title: ***MISC***

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A3	HBU16 1.2	1

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