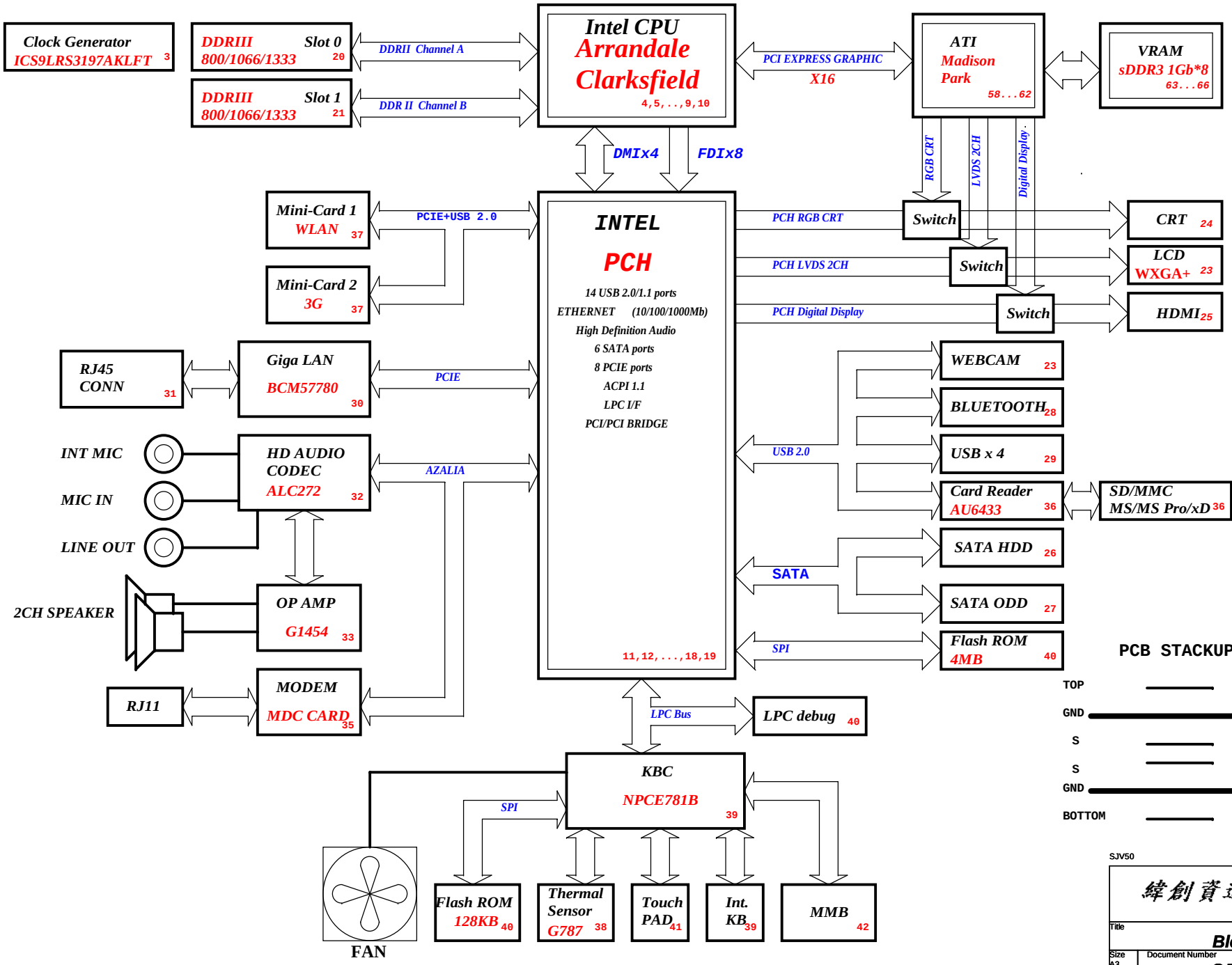
# SJV50-CP Block Diagram

Project code: 91.4GH01.001
PCB P/N : 48.4GH01.0SB
REVISION : 09284-SB




## PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

## CPU DC/DC
ISL62882

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | VCC_CORE 45,46 |

## SYSTEM DC/DC
TPS51123

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | 5V_S5<br>3D3V_S5 47 |

## SYSTEM DC/DC
TPS51117

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | 1D5V_S3 48 |

## SYSTEM DC/DC
TPS51117

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | 1D05V_S0 48 |

## SYSTEM DC/DC
TPS51117

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | 1D05V_VTT 49 |

## RT9025

| INPUTS | OUTPUTS |
|---|---|
| 3D3V_S0 | 1D8V_S0 50 |

## G2997

| INPUTS | OUTPUTS |
|---|---|
| 1D5V_S3 | 0D75_S0 50 |

## SYSTEM DC/DC
ISL62881

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | VCC_GFXCORE 52 |

## SYSTEM DC/DC
TPS51117

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | +VGA_CORE 53 |

## CHARGER
ISL88731A

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | BT+ 51 |

SJV50

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Title: Block Diagram

| Size | Document Number | Rev |
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# PCH Strapping

| Name | Schematics Notes |
|---|---|
| SPKR | **Reboot option at power-up**<br>**Default Mode:** Internal weak Pull-down.<br>**No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. |
| INIT3_3V# | Weak internal pull-down. Do not pull high. |
| GNT3#/ GPIO55 | **Default Mode:** Internal pull-up.<br>**Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor). |
| INTVRMEN | **High (1) = Integrated VRM is enabled**<br>**Low (0) = Integrated VRM is disabled** |
| GNT0#, GNT1# | **Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required.<br>**Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.<br>**Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. |
| GNT2#/ GPIO53 | **Default - Internal pull-up.**<br>**Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops). |
| GPIO33 | **Default:** Do not pull low.<br>**Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor. |
| SPI_MOSI | **Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor<br>**Disable iTPM:** Left floating, no pull-down required. |
| NV_ALE | **Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.<br>**Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor. |
| NC_CLE | Weak internal pull-up. Do not pull low. |
| HAD_DOCK_EN# /GPIO[33] | **Low (0):** Flash Descriptor Security will be overridden.<br>**High (1) :** Flash Descriptor Security will be in effect. |
| HDA_SDO | Weak internal pull-down. Do not pull high. |
| HDA_SYNC | Weak internal pull-down. Do not pull high. |
| GPIO15 | Weak internal pull-down. Do not pull high. |
| GPIO8 | Weak internal pull-up. Do not pull low. |
| GPIO27 | **Default = Do not connect (floating)**<br>High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.<br>Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails. |

# Processor Strapping

| Pin Name | Strap Description | Configuration (Default value for each bit is 1 unless specified otherwise) | Default Value |
|---|---|---|---|
| CFG[4] | **Embedded DisplayPort Presence** | **1:** Disabled - No Physical Display Port attached to Embedded DisplayPort.<br>**0:** Enabled - An external Display Port device is connected to the Embedded Display Port. | **1** |
| CFG[3] | **PCI-Express Static Lane Reversal** | **1:** Normal Operation.<br>**0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ... | **1** |
| CFG[0] | **PCI-Express Configuration Select** | **1:** Single PCI-Express Graphics<br>**0:** Bifurcation enabled | **1** |
| CFG[7] | **Reserved - Temporarily used for early Clarksfield samples.** | **Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor<br>**Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].<br>For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality. | **0** |

# PCIE Routing

| | |
|---|---|
| LANE1 | LAN |
| LANE2 | MiniCard WLAN |
| | |

# USB Table

| Pair | Device |
|---|---|
| 0 | USB3 |
| 1 | USB2 |
| 2 | USB4 |
| 3 | MINICARD1 |
| 4 | WECAM |
| 5 | Touch Panel (X) |
| 6 | NC |
| 7 | NC |
| 8 | NC |
| 9 | USB1(HS) |
| 10 | Finger Print (X) |
| 11 | Blue Tooth |
| 12 | MINIC2 |
| 13 | Cardreader |

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Title: **Table of Content**

| Size | Document Number | Rev |
|---|---|---|
| A3 | SJV50-CP | SB |

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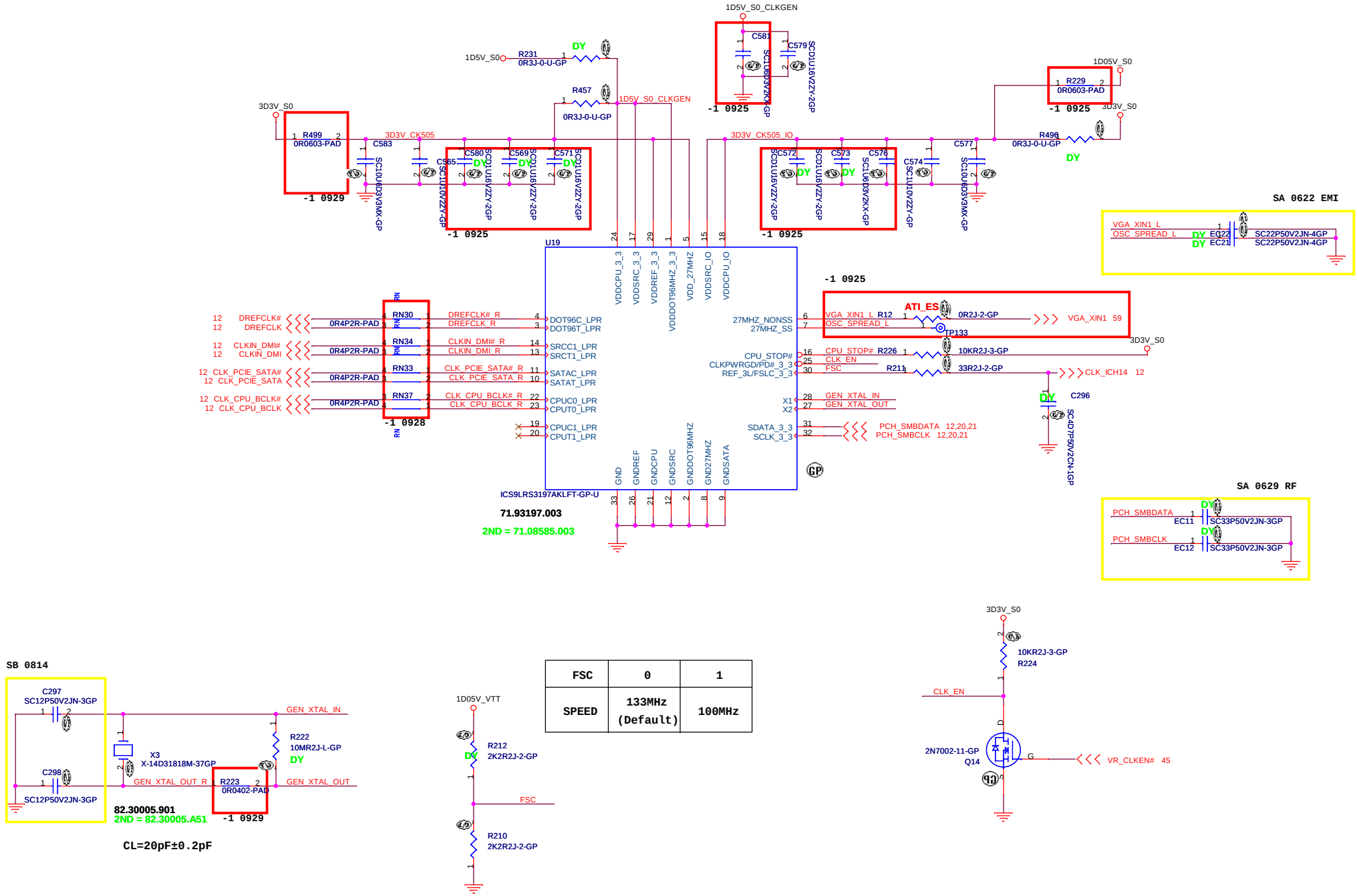


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Title: **Clock Generator**

| Size | Document Number | Rev |
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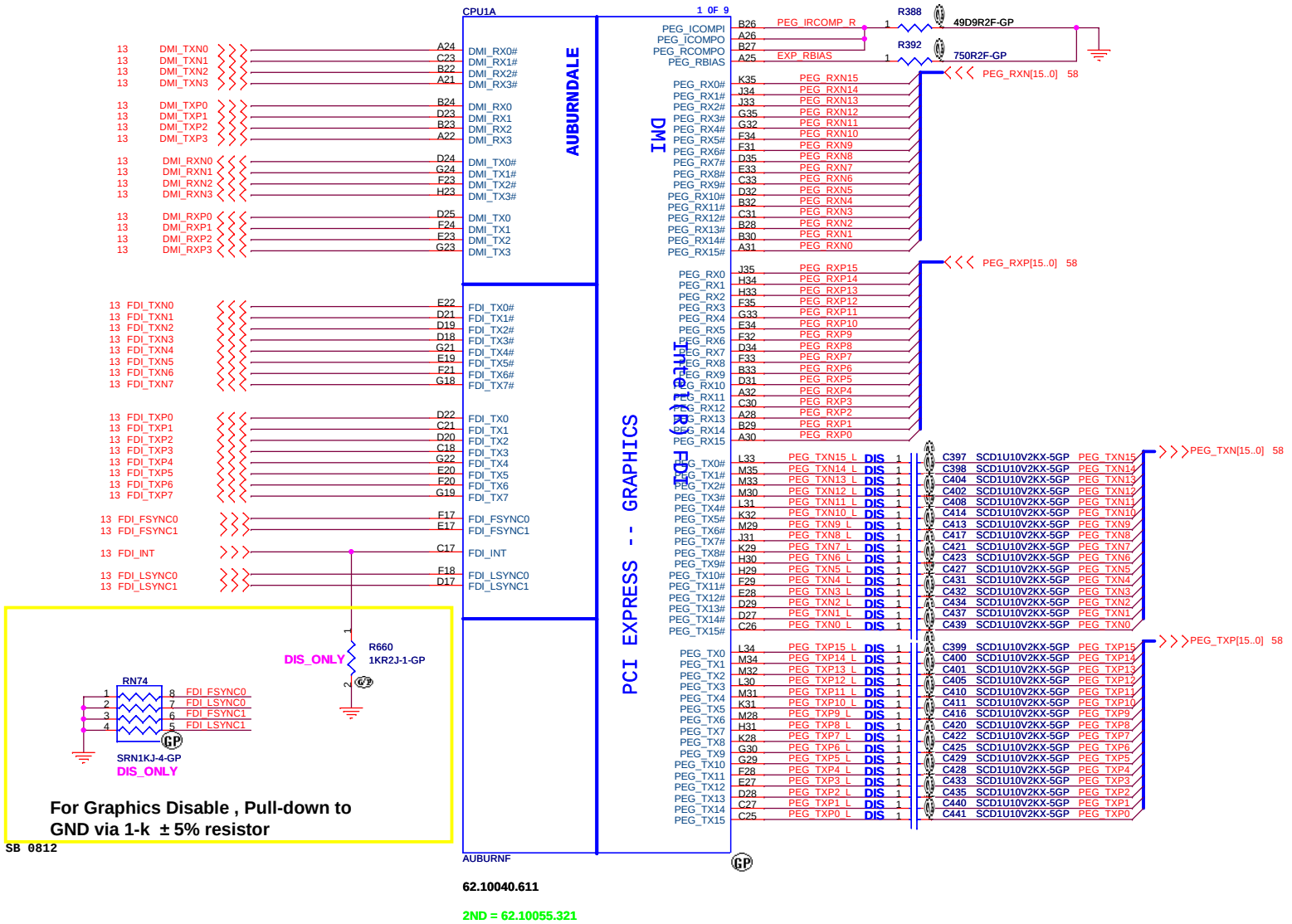


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| | |
|---|---|
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| Title | ***CPU (1/7)*** |
| Size A3 | Document Number **SJV50-CP** Rev **SB** |
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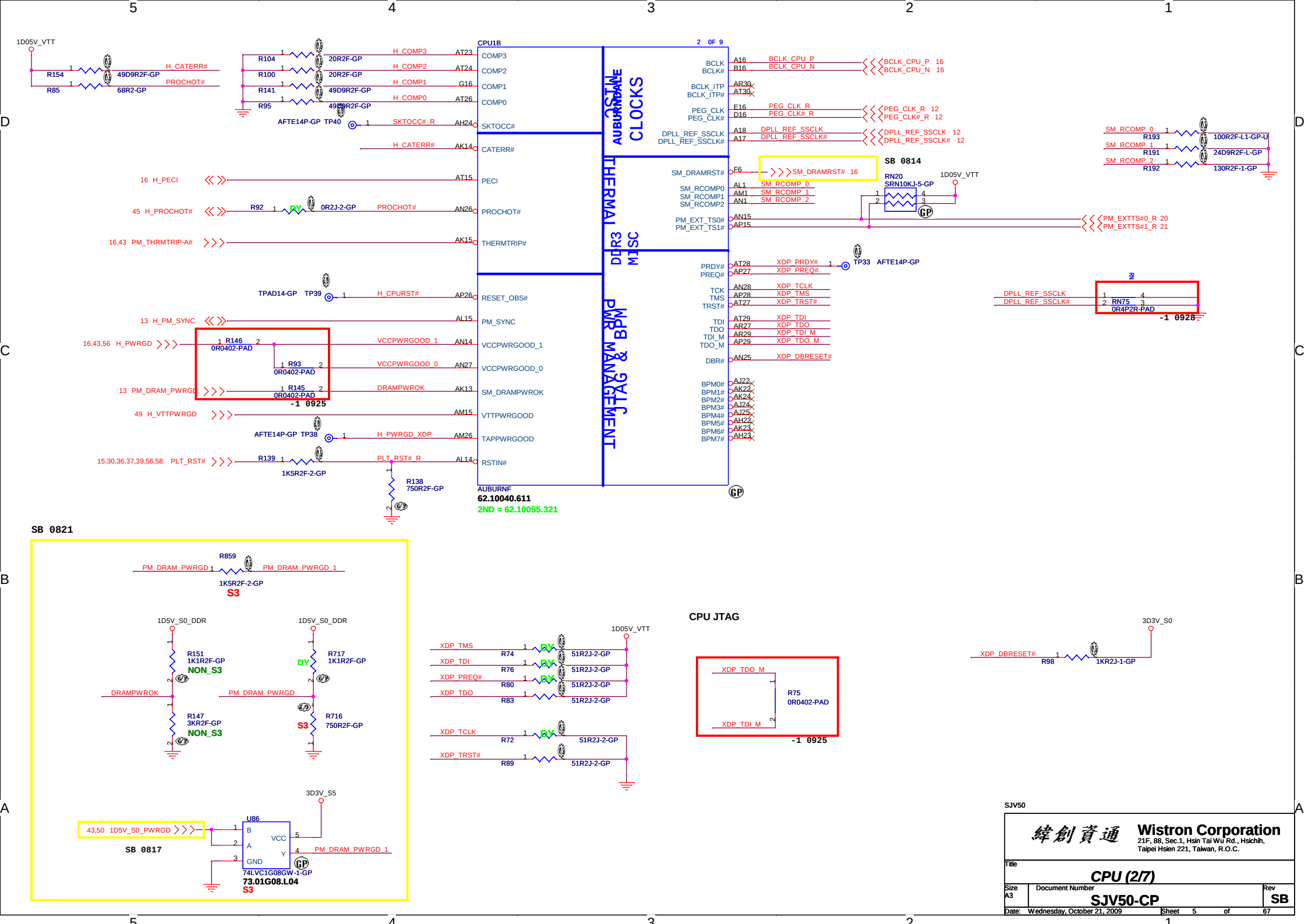
CPU1B
2 OF 9
AUBURNDALE
CLOCKS
THERMAL
DDR3
MISC
PWR MANAGEMENT
JTAG
COMP3
COMP2
COMP1
COMP0
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
RESET_OBS#
PM_SYNC
VCCPWRGOOD_1
VCCPWRGOOD_0
SM_DRAMPWROK
VTTPWRGOOD
TAPPWRGOOD
RSTIN#
AUBURNF
62.10040.611
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BCLK
BCLK#
BCLK_ITP
BCLK_ITP#
PEG_CLK
PEG_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PM_EXT_TS0#
PM_EXT_TS1#
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
TDI_M
TDO_M
DBR#
BPM0#
BPM1#
BPM2#
BPM3#
BPM4#
BPM5#
BPM6#
BPM7#
SB 0814
RN20
SRN10KJ-5-GP
1D05V_VTT
TP33
AFTE14P-GP
TPAD14-GP TP39
AFTE14P-GP TP38
AFTE14P-GP TP40
R104
R100
R141
R95
R154
R85
R92
R146
R93
R145
R139
R138
R859
R151
R147
R717
R716
R74
R76
R80
R83
R72
R89
R75
R98
SB 0821
S3
NON_S3
DY
U86
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SB 0817
CPU JTAG
XDP_TMS
XDP_TDI
XDP_PREQ#
XDP_TDO
XDP_TCLK
XDP_TRST#
XDP_TDO_M
XDP_TDI_M
XDP_DBRESET#
-1 0925
-1 0928
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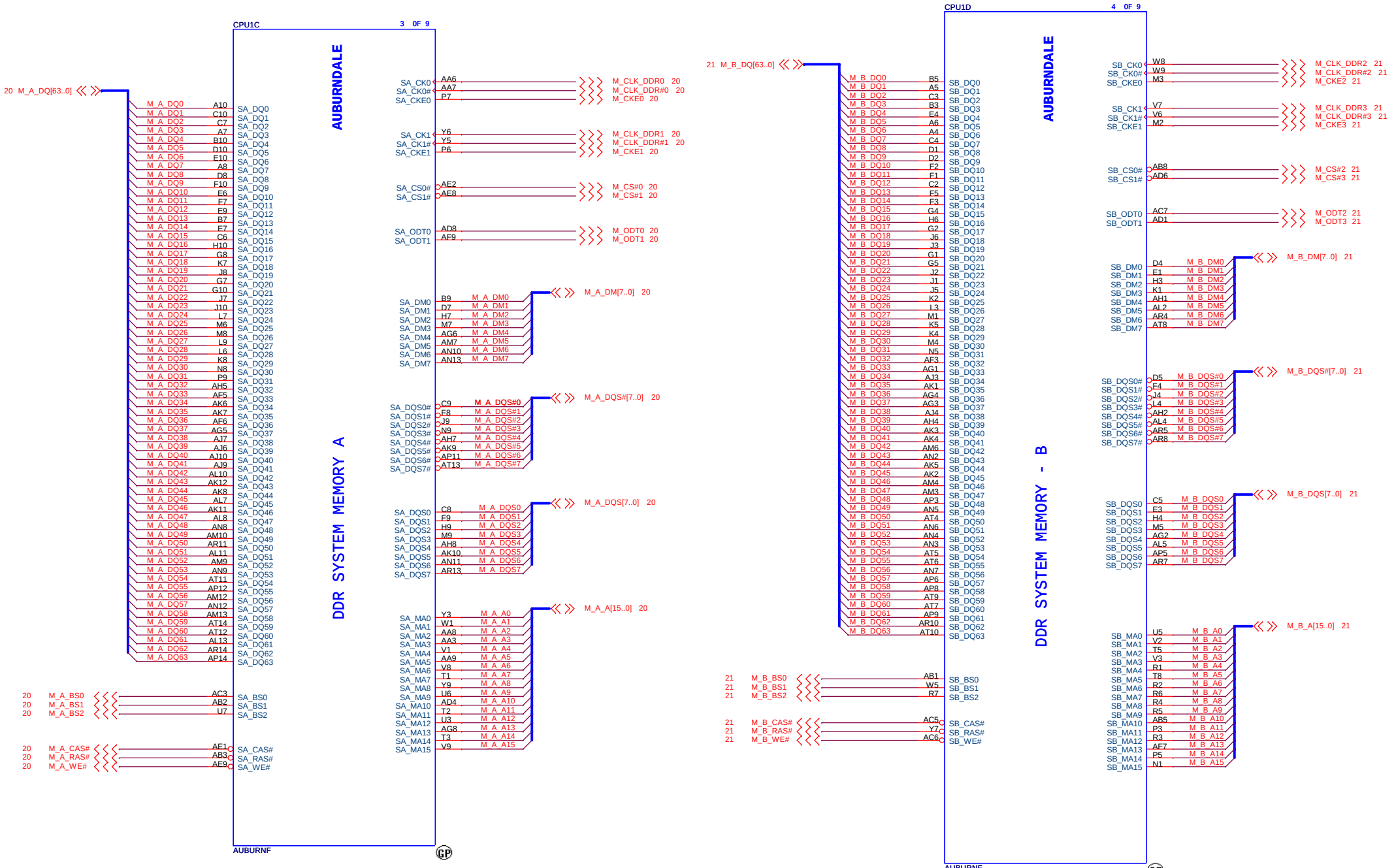
CPU1C
3 0F 9
AUBURNDALE
DDR SYSTEM MEMORY A
AUBURNF
20 M_A_DQ[63..0]
M_A_DQ0 A10
M_A_DQ1 C10
M_A_DQ2 C7
M_A_DQ3 A7
M_A_DQ4 B10
M_A_DQ5 D10
M_A_DQ6 E10
M_A_DQ7 A8
M_A_DQ8 D8
M_A_DQ9 F10
M_A_DQ10 E6
M_A_DQ11 F7
M_A_DQ12 E9
M_A_DQ13 B7
M_A_DQ14 E7
M_A_DQ15 C6
M_A_DQ16 H10
M_A_DQ17 G8
M_A_DQ18 K7
M_A_DQ19 J8
M_A_DQ20 G7
M_A_DQ21 G10
M_A_DQ22 J7
M_A_DQ23 J10
M_A_DQ24 L7
M_A_DQ25 M6
M_A_DQ26 M8
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M_A_DQ35 AK7
M_A_DQ36 AF6
M_A_DQ37 AG5
M_A_DQ38 AJ7
M_A_DQ39 AJ6
M_A_DQ40 AJ10
M_A_DQ41 AJ9
M_A_DQ42 AL10
M_A_DQ43 AK12
M_A_DQ44 AK8
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M_A_DQ46 AK11
M_A_DQ47 AL8
M_A_DQ48 AN8
M_A_DQ49 AM10
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M_A_DQ53 AN9
M_A_DQ54 AT11
M_A_DQ55 AP12
M_A_DQ56 AM12
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M_A_DQ58 AM13
M_A_DQ59 AT14
M_A_DQ60 AT12
M_A_DQ61 AL13
M_A_DQ62 AR14
M_A_DQ63 AP14
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20 M_A_BS1
20 M_A_BS2
AC3 AB2 U7
SA_BS0 SA_BS1 SA_BS2
20 M_A_CAS#
20 M_A_RAS#
20 M_A_WE#
AE1 AB3 AE9
SA_CAS# SA_RAS# SA_WE#
SA_CK0 AA6
SA_CK0# AA7
SA_CKE0 P7
M_CLK_DDR0 20
M_CLK_DDR#0 20
M_CKE0 20
SA_CK1 Y6
SA_CK1# Y5
SA_CKE1 P6
M_CLK_DDR1 20
M_CLK_DDR#1 20
M_CKE1 20
SA_CS0# AE2
SA_CS1# AE8
M_CS#0 20
M_CS#1 20
SA_ODT0 AD8
SA_ODT1 AF9
M_ODT0 20
M_ODT1 20
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SA_DM2 H7 M_A_DM2
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SA_DM6 AN10 M_A_DM6
SA_DM7 AN13 M_A_DM7
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SA_DQS1# F8 M_A_DQS#1
SA_DQS2# J9 M_A_DQS#2
SA_DQS3# N9 M_A_DQS#3
SA_DQS4# AH7 M_A_DQS#4
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SA_MA2 AA8 M_A_A2
SA_MA3 AA3 M_A_A3
SA_MA4 V1 M_A_A4
SA_MA5 AA9 M_A_A5
SA_MA6 V8 M_A_A6
SA_MA7 T1 M_A_A7
SA_MA8 Y9 M_A_A8
SA_MA9 U6 M_A_A9
SA_MA10 AD4 M_A_A10
SA_MA11 T2 M_A_A11
SA_MA12 U3 M_A_A12
SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15
M_A_A[15..0] 20
2ND = 62.10055.321
62.10040.611
CPU1D
4 0F 9
AUBURNDALE
DDR SYSTEM MEMORY - B
AUBURNF
SJV50
21 M_B_DQ[63..0]
M_B_DQ0 B5
M_B_DQ1 A5
M_B_DQ2 C3
M_B_DQ3 B3
M_B_DQ4 E4
M_B_DQ5 A6
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M_B_DQ7 C4
M_B_DQ8 D1
M_B_DQ9 D2
M_B_DQ10 F2
M_B_DQ11 F1
M_B_DQ12 C2
M_B_DQ13 E5
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M_B_DQ16 H6
M_B_DQ17 G2
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M_B_DQ35 AK1
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M_B_DQ38 AJ4
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M_B_DQ41 AK4
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M_B_DQ44 AK5
M_B_DQ45 AK2
M_B_DQ46 AM4
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M_B_DQ49 AN5
M_B_DQ50 AT4
M_B_DQ51 AN6
M_B_DQ52 AN4
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M_B_DQ54 AT5
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M_B_DQ58 AP8
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M_B_DQ60 AT7
M_B_DQ61 AP9
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21 M_B_BS0
21 M_B_BS1
21 M_B_BS2
AB1 W5 R7
SB_BS0 SB_BS1 SB_BS2
21 M_B_CAS#
21 M_B_RAS#
21 M_B_WE#
AC5 Y7 AC6
SB_CAS# SB_RAS# SB_WE#
SB_CK0 W8
SB_CK0# W9
SB_CKE0 M3
M_CLK_DDR2 21
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M_CKE2 21
SB_CK1 V7
SB_CK1# V6
SB_CKE1 M2
M_CLK_DDR3 21
M_CLK_DDR#3 21
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SB_CS1# AD6
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M_CS#3 21
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M_ODT2 21
M_ODT3 21
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SB_DQS4# AH2 M_B_DQS#4
SB_DQS5# AL4 M_B_DQS#5
SB_DQS6# AR5 M_B_DQS#6
SB_DQS7# AR8 M_B_DQS#7
M_B_DQS#[7..0] 21
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SB_DQS2 H4 M_B_DQS2
SB_DQS3 M5 M_B_DQS3
SB_DQS4 AG2 M_B_DQS4
SB_DQS5 AL5 M_B_DQS5
SB_DQS6 AP5 M_B_DQS6
SB_DQS7 AR7 M_B_DQS7
M_B_DQS[7..0] 21
SB_MA0 U5 M_B_A0
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SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AE7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15
M_B_A[15..0] 21
2ND = 62.10055.321
62.10040.611
緯創資通
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (3/7)
Size A3
Document Number
SJV50-CP
Rev SB
Date: Wednesday, October 21, 2009
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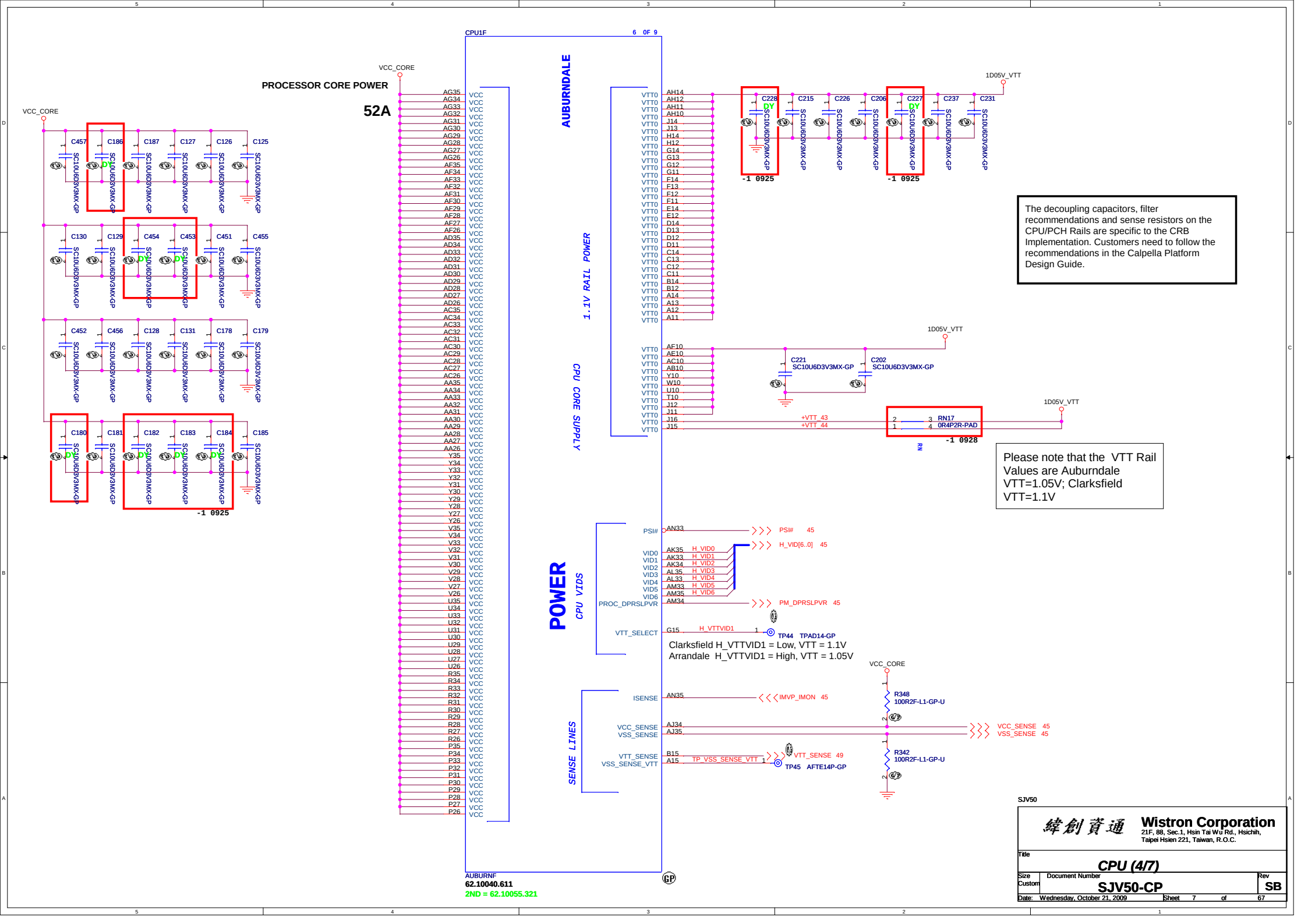
PROCESSOR CORE POWER
52A
VCC_CORE
CPU1F
6 0F 9
AUBURNDALE
1.1V RAIL POWER
CPU CORE SUPPLY
POWER
CPU VIDS
SENSE LINES
1D05V_VTT
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
AUBURNF
62.10040.611
2ND = 62.10055.321
SJV50
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Taipei Hsien 221, Taiwan, R.O.C.
CPU (4/7)
SJV50-CP
SB
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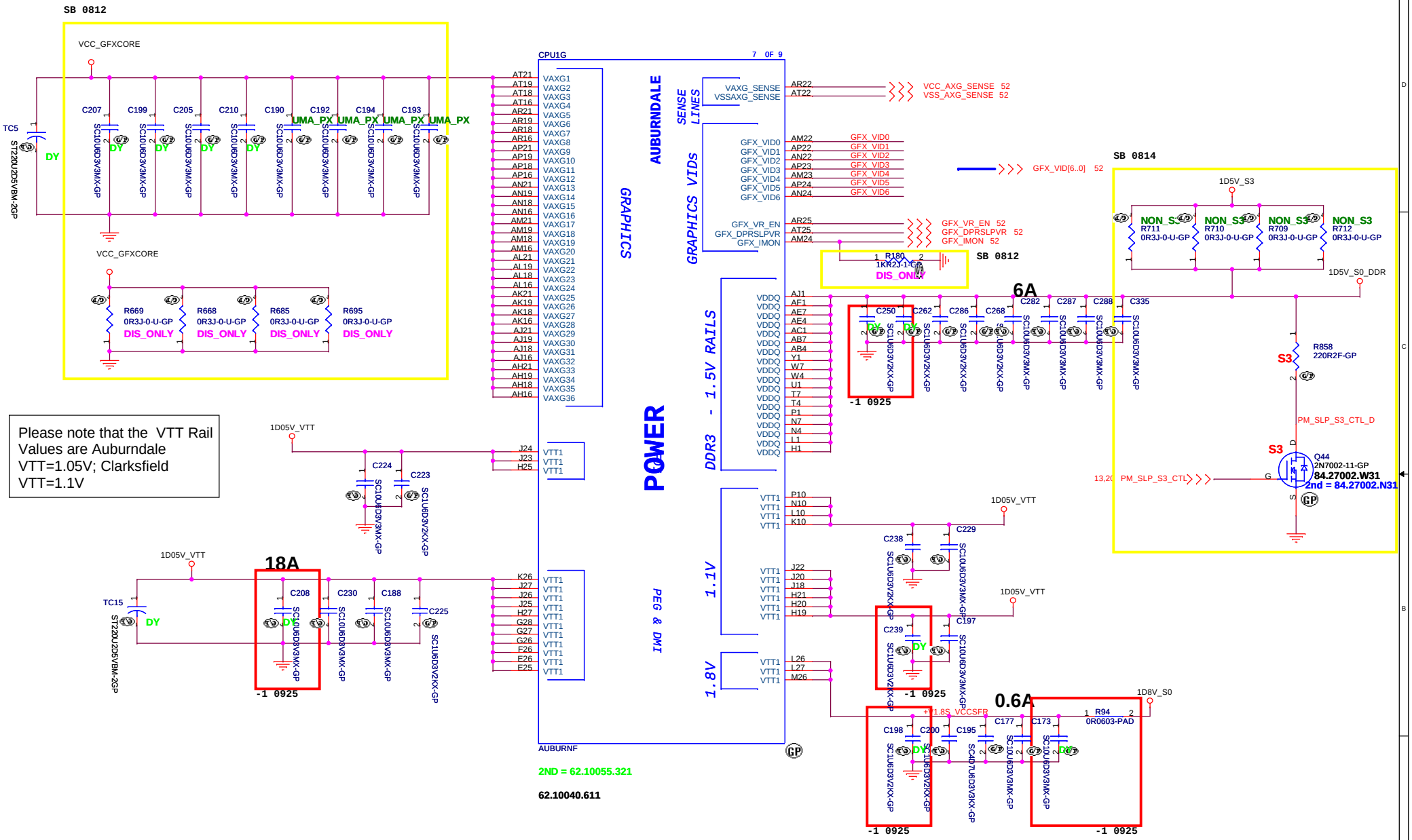


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Title: **CPU (5/7)**

| Size | Document Number | Rev |
|---|---|---|
| A3 | SJV50-CP | SB |

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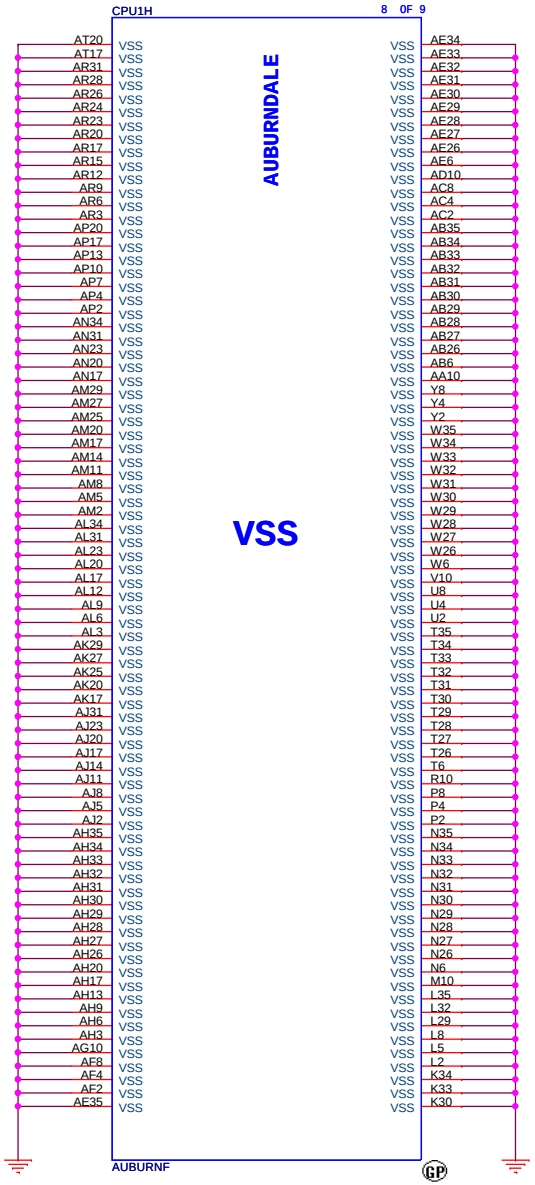
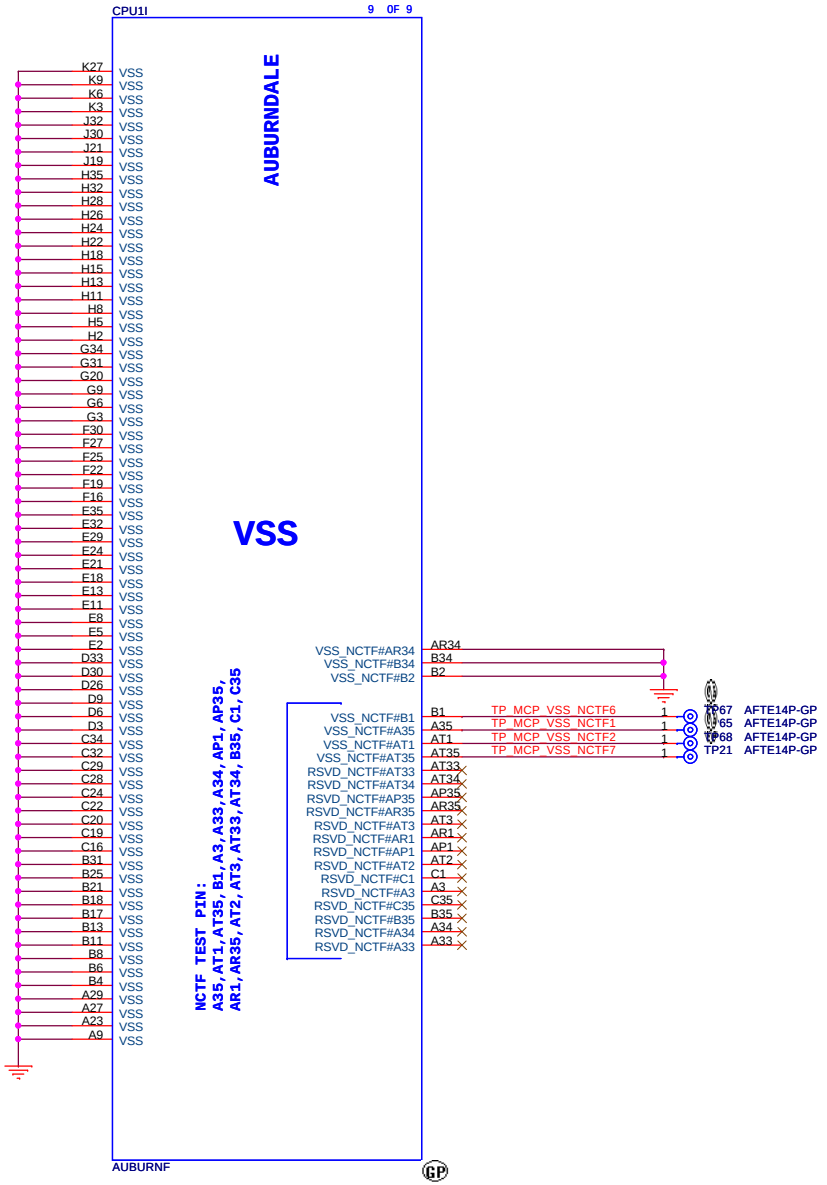



2ND = 62.10055.321

62.10040.611




2ND = 62.10055.321

62.10040.611

SJV50

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Title: ***CPU (6/7)***

| Size | Document Number | Rev |
|---|---|---|
| A3 | **SJV50-CP** | **SB** |

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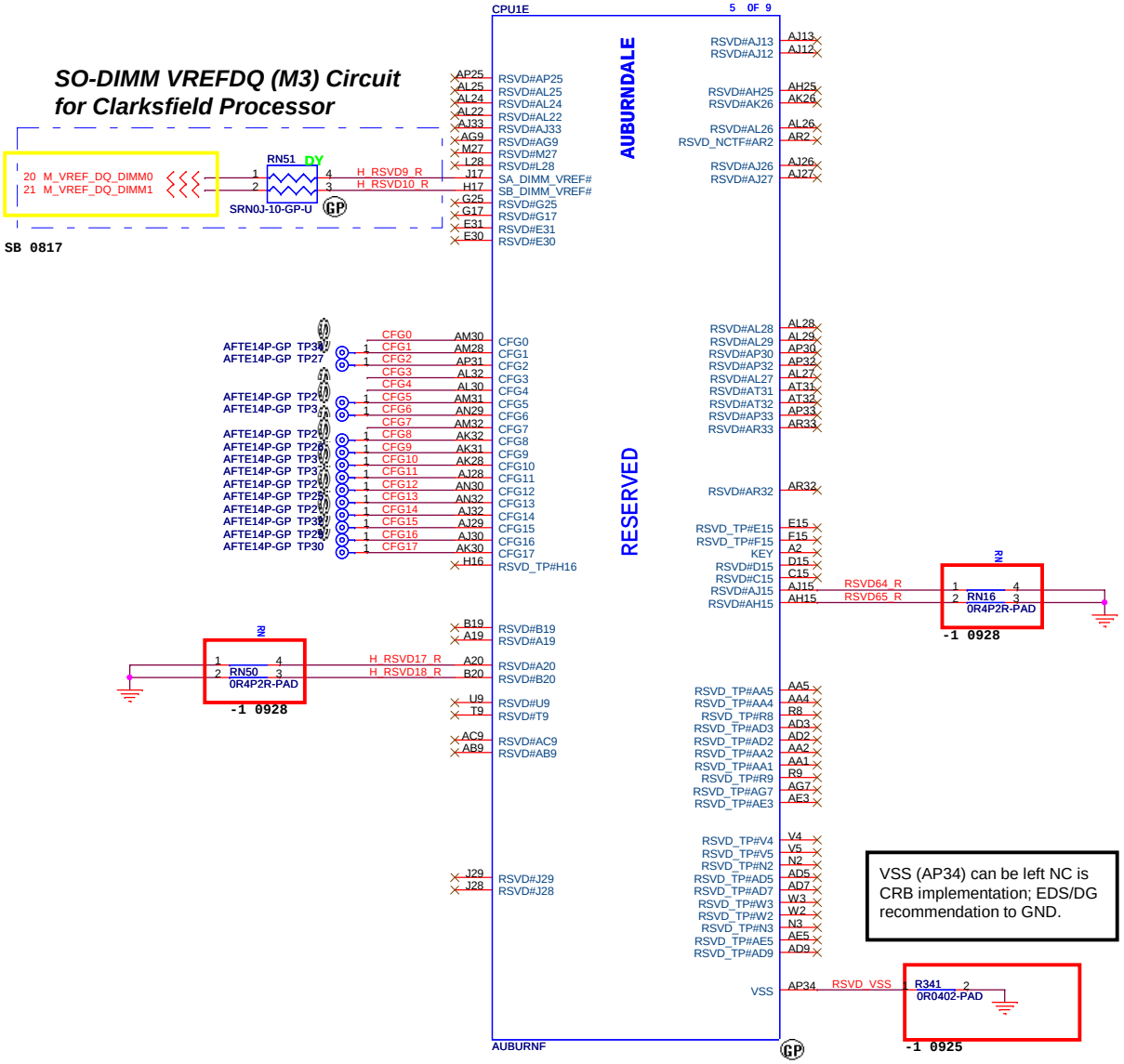
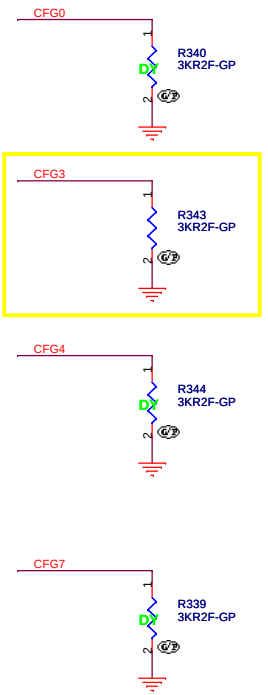
## SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor




| PCI-Express Configuration Select | |
|---|---|
| CFG0 | 1:Single PEG<br>0:Bifurcation enabled |

| CFG3 - PCI-Express Static Lane Reversal | |
|---|---|
| CFG3 | 1 :Normal Operation<br>0 :Lane Numbers Reversed<br>15 -> 0, 14 -> 1, ... |

| CFG4 - Display Port Presence | |
|---|---|
| CFG4 | 1:Disabled; No Physical Display Port attached to Embedded Display Port<br>0:Enabled; An external Display Port device is connected to the Embedded Display Port |

| CFG7(Reserved) - Temporarily used for early Clarksfield samples. | |
|---|---|
| CFG7 | Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.<br><br>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].<br>For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality. |

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| Size | Document Number | Rev |
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| integrated VccSus1_05,VccSus1_5,VccCL1_5 | |
|---|---|
| INTVRMEN | High=Enable Low=Disable |
| integrated VccLan1_05VccCL1_05 | |
| LAN100_SLP | High=Enable Low=Disable |

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

ICH_RTCX1
ICH_RTCX2
R443 10MR2J-L-GP
X6
X-32D768KHZ-34GPU
82.30001.661
C554 SC7P50V2DN-2GP
C549 SC7P50V2DN-2GP

RTC_AUX_S5
RN22 SRN20KJ-GP-U
C263 SC1U6D3V2KX-GP
C281 SC1U6D3V2KX-GP
G57 GAP-OPEN

SA 0629 RF
ACZ_RST# DY EC14 SC33P50V2JN-3GP
ACZ_SYNC DY EC18 SC33P50V2JN-3GP
ACZ_BIT_CLK DY EC16 SC33P50V2JN-3GP
ACZ_SDATAOUT DY EC17 SC33P50V2JN-3GP

SB 0825
32 ACZ_RST#_AUDIO
32 ACZ_SYNC_AUDIO
32 ACZ_BITCLK_AUDIO
32 ACZ_SDATAOUT_AUDIO
R397 10R2J-2-GP
R423 10R2J-2-GP
R420 10R2J-2-GP
R422 47R2J-2-GP
ACZ_RST#
ACZ_SYNC
ACZ_BIT_CLK
ACZ_SDATAOUT

35 ACZ_RST#_MDC
35 ACZ_SYNC_MDC
35 ACZ_BTCLK_MDC
35 ACZ_SDATAOUT_MDC
R398 33R2J-2-GP
R424 33R2J-2-GP
R419 33R2J-2-GP
R421 33R2J-2-GP

NO REBOOT STRAP
3D3V_S0
R465 DY 1KR2J-1-GP ACZ_SPKR

| No Reboot Strap R23 | |
|---|---|
| HDA_SPKR | Low = Default<br>High = No Reboot |

-1 0925
3D3V_S5
PCH_JTAG_TMS R493 DY 200R2J-L1-GP
PCH_JTAG_TDO R485 DY 200R2J-L1-GP
PCH_JTAG_TDI R492 DY 200R2J-L1-GP
PCH_JTAG_RST# R490 DY 10KR2J-3-GP
PCH_JTAG_TMS R477 DY 100R2J-2-GP
PCH_JTAG_TDO R486 DY 100R2J-2-GP
PCH_JTAG_TDI R487 DY 100R2J-2-GP
PCH_JTAG_RST# R491 DY 51R2F-2-GP
PCH_JTAG_TCK R227 51R2F-2-GP
When unused all JTAG pins may be NC

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
3D3V_S0 R480 DY 8K2R2J-3-GP SPI_MOSI_R

SA 0709 EMI
ACZ_BTCLK_MDC
ACZ_BITCLK_AUDIO
DY EC13 SC22P50V2JN-4GP
DY EC15 SC22P50V2JN-4GP

RTC_AUX_S5
R189 1MR2J-1-GP SM_INTRUDER#
R188 330KR2F-L-GP ICH_INTVRMEN

SRTCRST# new signal Pin

PCH1A 1 OF 10
RTC: RTCX1 B13 ICH_RTCX1; RTCX2 D13 ICH_RTCX2; RTCRST# C14 ICH_RTCRST#; SRTCRST# D17 SRTCRST#; INTRUDER# A16 SM_INTRUDER#; INTVRMEN A14 ICH_INTVRMEN
LPC: FWH0/LAD0 D33 LPC_LAD0 39; FWH1/LAD1 B33 LPC_LAD1 39; FWH2/LAD2 C32 LPC_LAD2 39; FWH3/LAD3 A32 LPC_LAD3 39; FWH4/LFRAME# C34 LPC_LFRAME# 39; LDRQ0# A34; LDRQ1#/GPIO23 F34 PCH_GPIO23 — TP47 AFTE14P-GP; SERIRQ AB9 INT_SERIRQ — INT_SERIRQ 39
IHDA: HDA_BCLK A30 ACZ_BIT_CLK; HDA_SYNC D29 ACZ_SYNC; SPKR P1 32 ACZ_SPKR; HDA_RST# C30 ACZ_RST#; HDA_SDIN0 G30 32 ACZ_SDATAIN0; HDA_SDIN1 F30 35 ACZ_SDATAIN1 — AFTE14P-GP TP48; HDA_SDIN2 E32 HDA_SDIN2; HDA_SDIN3 F32; HDA_SDO B29 ACZ_SDATAOUT
SATA: HDA_DOCK_EN#/GPIO33 H32 HDA_DOCK_EN#; HDA_DOCK_RST#/GPIO13 J30
JTAG: JTAG_TCK M3 PCH_JTAG_TCK; JTAG_TMS K3 PCH_JTAG_TMS; JTAG_TDI K1 PCH_JTAG_TDI; JTAG_TDO J2 PCH_JTAG_TDO; TRST# J4 PCH_JTAG_RST#
SPI: SPI_CLK BA2; SPI_CS0# AV3; SPI_CS1# AY3; SPI_MOSI AY1; SPI_MISO AV1
IBEXPEAK-M-GP-NF

-1 0925
39 ME_UNLOCK# — R171 0R0402-PAD — HDA_DOCK_EN#
R172 8K2R2J-3-GP DY

40 PCH_SPI_CLK — PCH_SPI_CLK R481 15R2J-GP SPI_CLK_R
40 PCH_SPI_CS#0 — PCH_SPI_CS#0 R478 15R2J-GP SPI_CS#0_R
40 PCH_SPI_MOSI — PCH_SPI_MOSI R479 15R2J-GP SPI_MOSI_R
40 SPI_MOSO_R — SPI_MOSO_R

SATA: SATA0RXN AK7 SATA_RXN0 26; SATA0RXP AK6 SATA_RXP0 26; SATA0TXN AK11 SATA_TXN0 26; SATA0TXP AK9 SATA_TXP0 26 — HDD
SATA1RXN AH6; SATA1RXP AH5; SATA1TXN AH9; SATA1TXP AH8
SATA2RXN AF11; SATA2RXP AF9; SATA2TXN AF7; SATA2TXP AF6
SATA3RXN AH3; SATA3RXP AH1; SATA3TXN AF3; SATA3TXP AF1
SATA4RXN AD9 SATA_RXN4 27; SATA4RXP AD8 SATA_RXP4 27; SATA4TXN AD6 SATA_TXN4 27; SATA4TXP AD5 SATA_TXP4 27 — ODD
SATA5RXN AD3; SATA5RXP AD1; SATA5TXN AB3; SATA5TXP AB1
SATAICOMPO AF16; SATAICOMPI AF15 — SATAICOMP — R187 37D4R2F-GP — 1D05V_S0
SATALED# T3 SATA_LED# — SATA_LED# 42
SATA0GP/GPIO21 Y9 SATA_DET#0_R
SATA1GP/GPIO19 V1 SATA_DET#1_R

RN39 SRN10KJ-7GP 3D3V_S0
SATA_LED#
SATA_DET#0_R
INT_SERIRQ
SATA_DET#1_R

RTC_AUX_S5 -1 0925
R244 0R0603-PAD RTC_PWR_L
C311 SC1U10V2ZY-GP
D10 BAS40CW-GP
83.00040.E81
2nd = 83.00040.M81
3D3V_AUX_S5
RTC_PWR R239 1KR2J-1-GP
RTC_BAT
RTC1 PWR GND NP1 NP2
BAT-CON2-1-GP-U
62.70001.011

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Title: PCH (1/9)
Size: A3 | Document Number: SJV50-CP | Rev: SB
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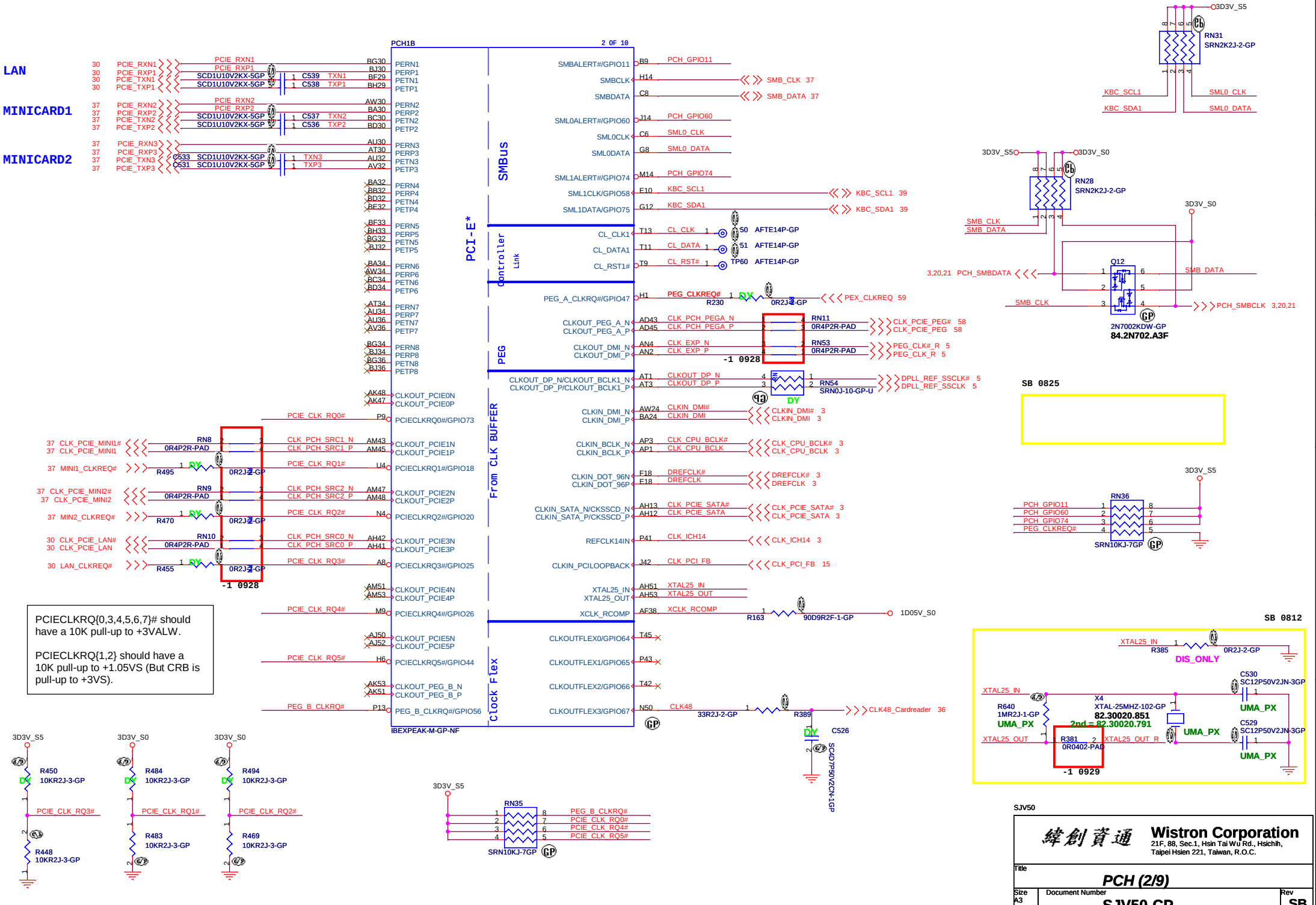
LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
SB 0825
SB 0812
-1 0928
-1 0929
2N7002KDW-GP
84.2N702.A3F
SRN10KJ-7GP
SRN2K2J-2-GP
SRN0J-10-GP-U
0R4P2R-PAD
0R2J-2-GP
90D9R2F-1-GP
33R2J-2-GP
SC47P50V2CN-1GP
SC12P50V2JN-3GP
XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30020.791
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PCH (2/9)
SJV50-CP
Wednesday, October 21, 2009
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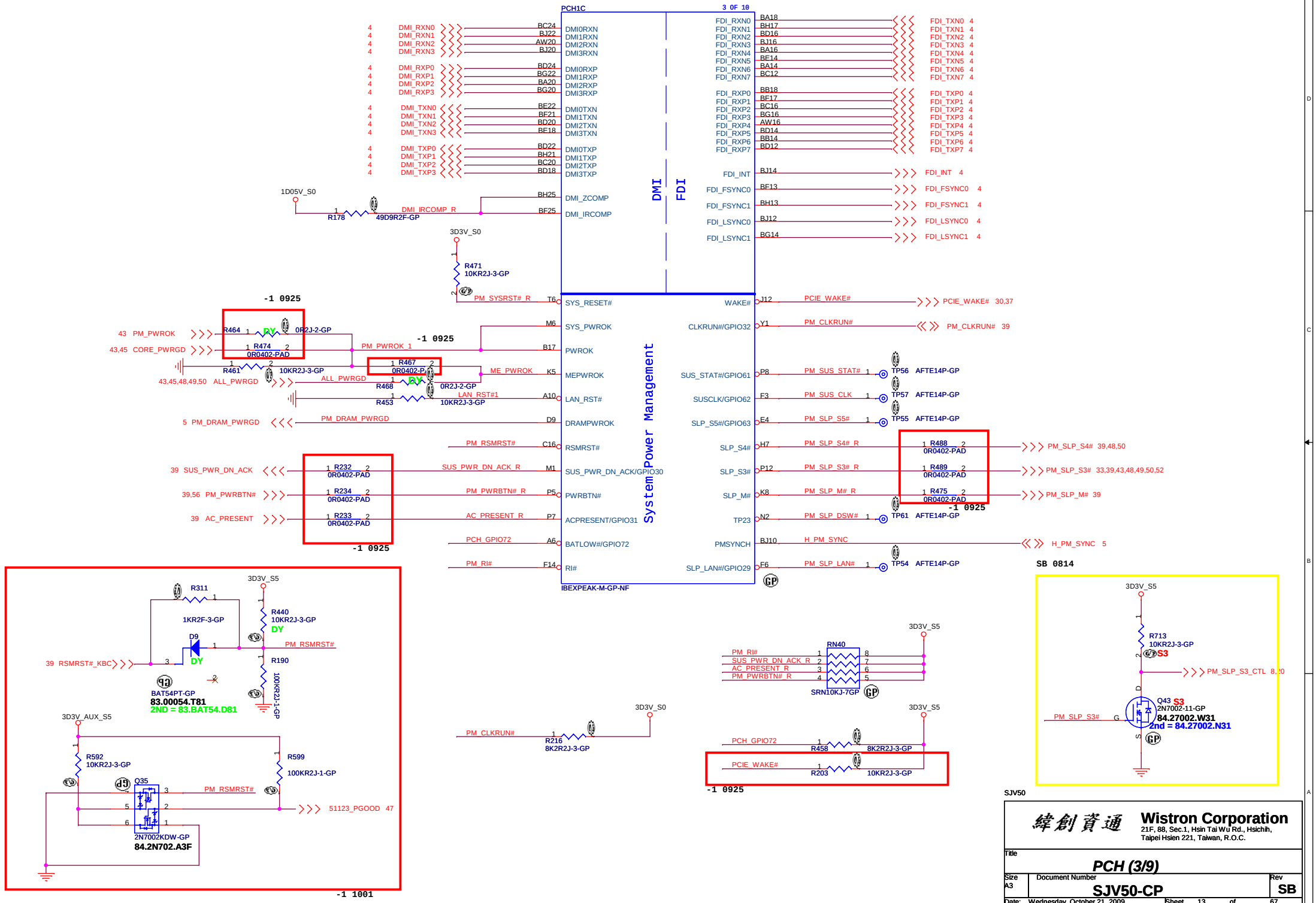
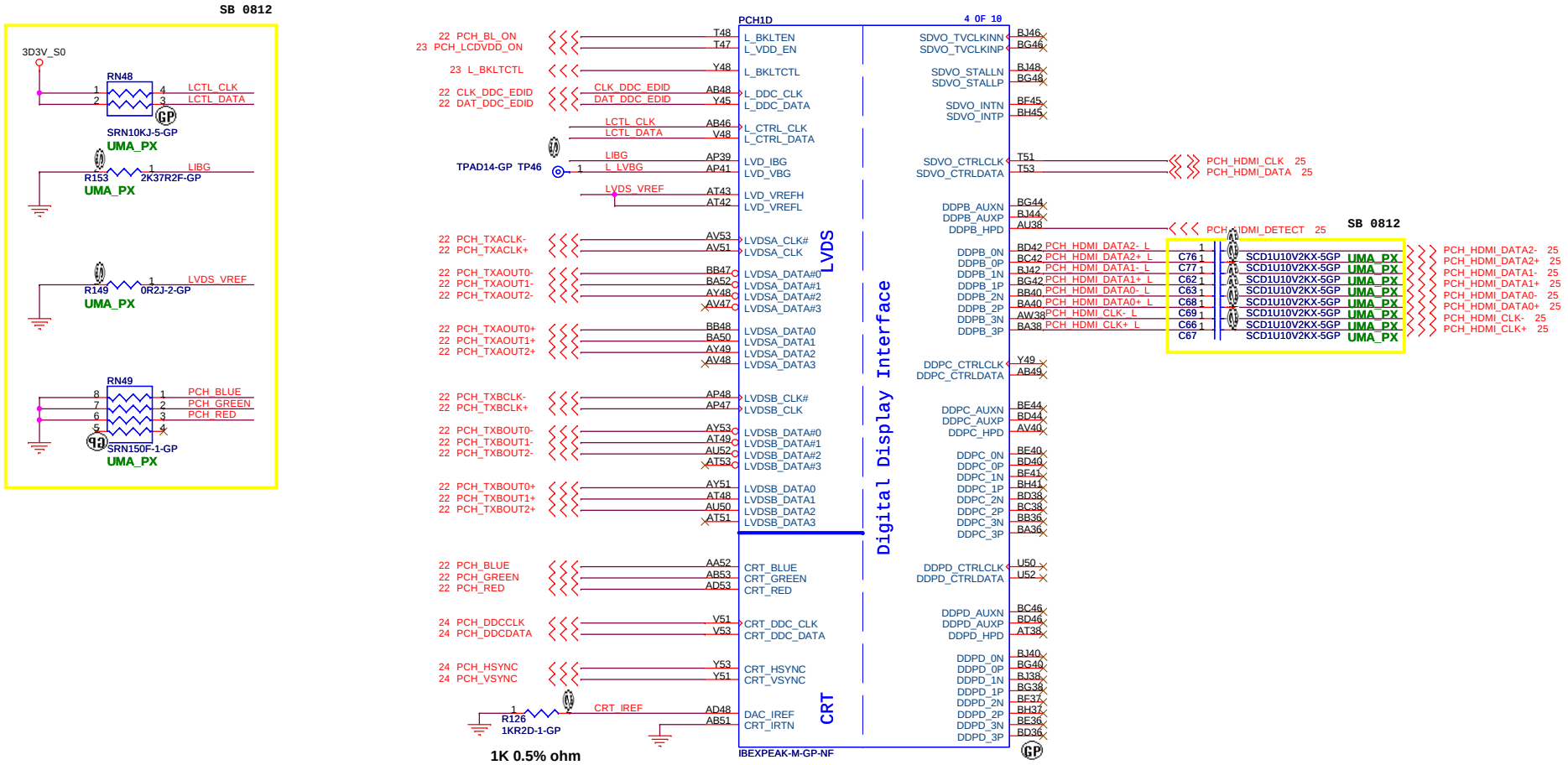



| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | ***PCH (3/9)*** | |
| Size A3 | Document Number **SJV50-CP** | Rev **SB** |
| Date: Wednesday, October 21, 2009 | Sheet 13 of 67 | |

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| | | |
|---|---|---|
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| Title | ***PCH (4/9)*** | |
| Size<br>A3 | Document Number<br>**SJV50-CP** | Rev<br>**SB** |
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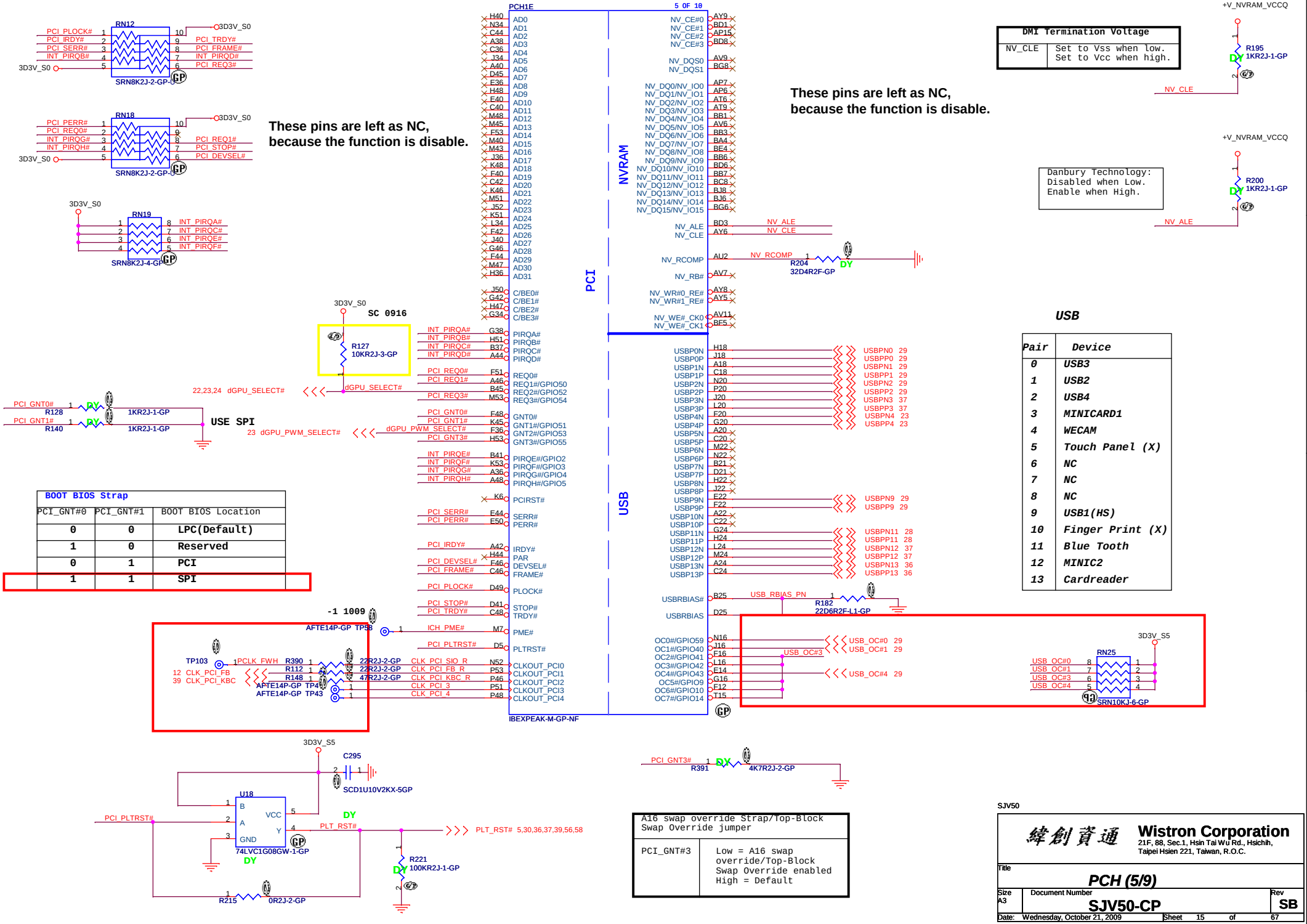


| DMI Termination Voltage | |
|---|---|
| NV_CLE | Set to Vss when low.<br>Set to Vcc when high. |

| BOOT BIOS Strap | | |
|---|---|---|
| PCI_GNT#0 | PCI_GNT#1 | BOOT BIOS Location |
| 0 | 0 | LPC(Default) |
| 1 | 0 | Reserved |
| 0 | 1 | PCI |
| 1 | 1 | SPI |

**USB**

| Pair | Device |
|---|---|
| 0 | USB3 |
| 1 | USB2 |
| 2 | USB4 |
| 3 | MINICARD1 |
| 4 | WECAM |
| 5 | Touch Panel (X) |
| 6 | NC |
| 7 | NC |
| 8 | NC |
| 9 | USB1(HS) |
| 10 | Finger Print (X) |
| 11 | Blue Tooth |
| 12 | MINIC2 |
| 13 | Cardreader |

| A16 swap override Strap/Top-Block Swap Override jumper | |
|---|---|
| PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled<br>High = Default |

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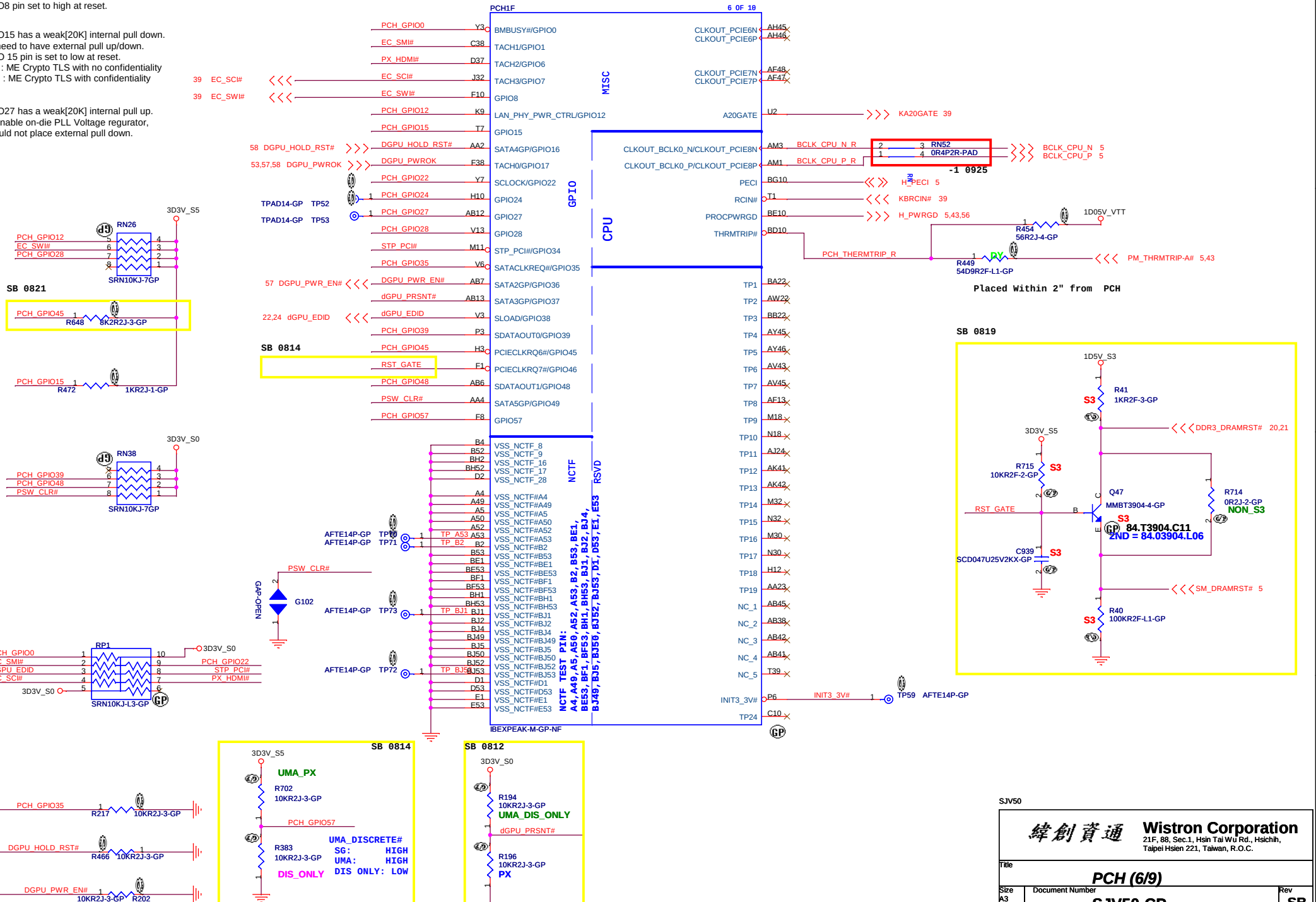
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

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Title: PCH (6/9)

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|---|---|---|
| A3 | SJV50-CP | SB |

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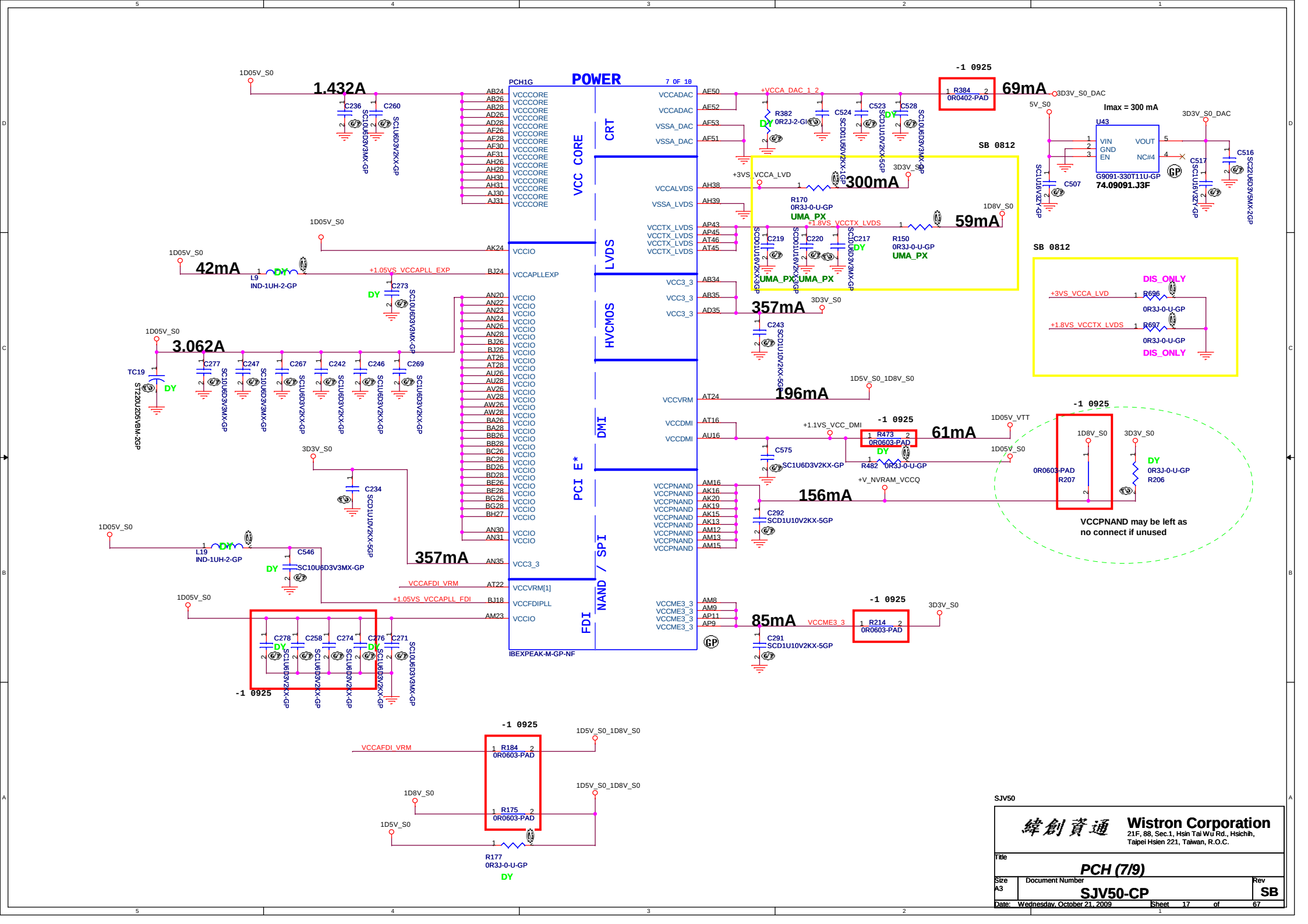
POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
42mA
357mA
357mA
196mA
156mA
85mA
69mA
300mA
59mA
61mA
-1 0925
SB 0812
Imax = 300 mA
G9091-330T11U-GP
74.09091.J3F
DIS_ONLY
VCCPNAND may be left as no connect if unused
IBEXPEAK-M-GP-NF
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SJV50
PCH (7/9)
SJV50-CP
Rev SB
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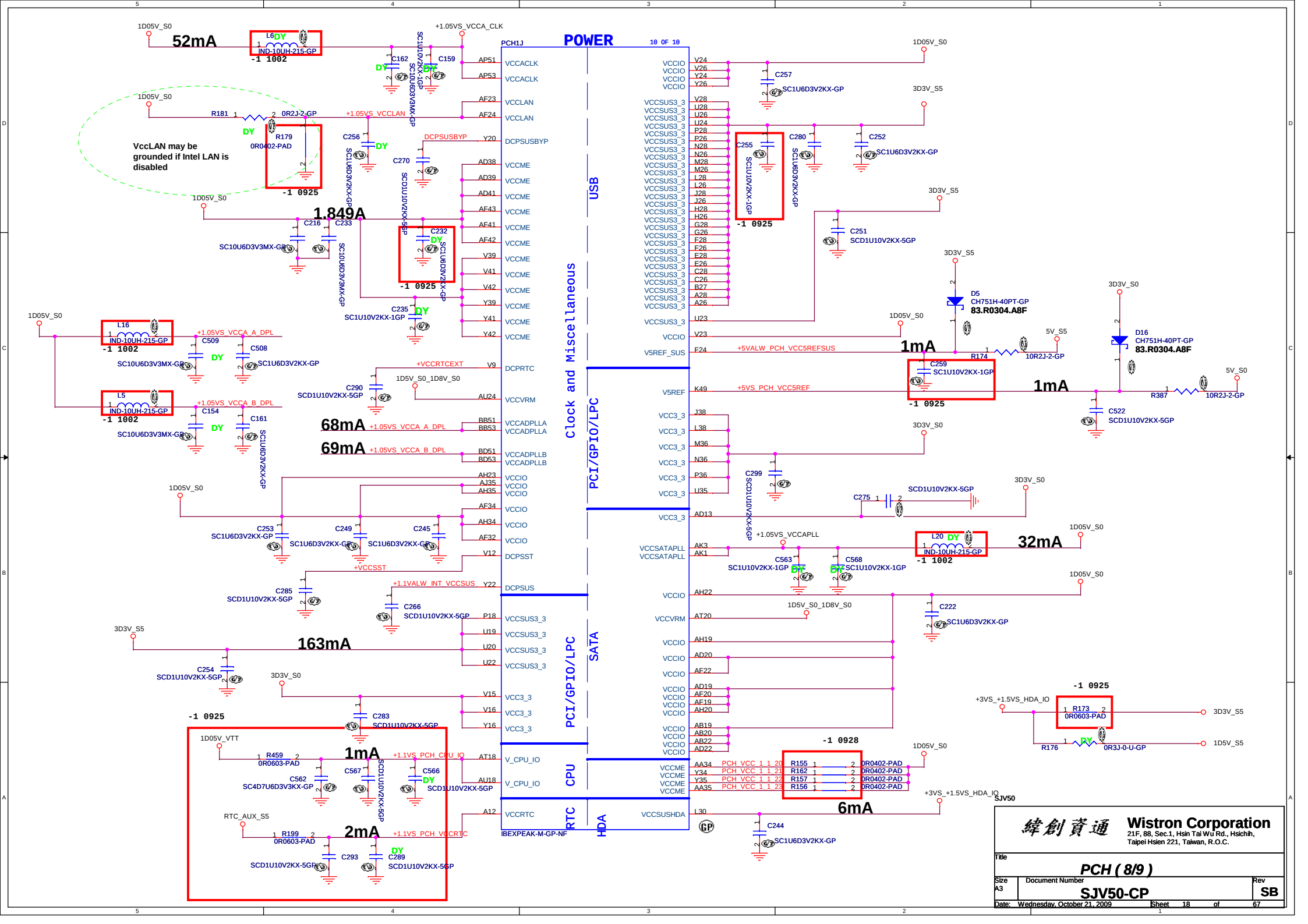
POWER
10 OF 10
PCH1J
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
52mA
1.849A
163mA
68mA
69mA
1mA
2mA
6mA
32mA
VccLAN may be grounded if Intel LAN is disabled
-1 1002
-1 0925
-1 0928
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Title
PCH ( 8/9 )
Size A3
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Date: Wednesday, October 21, 2009
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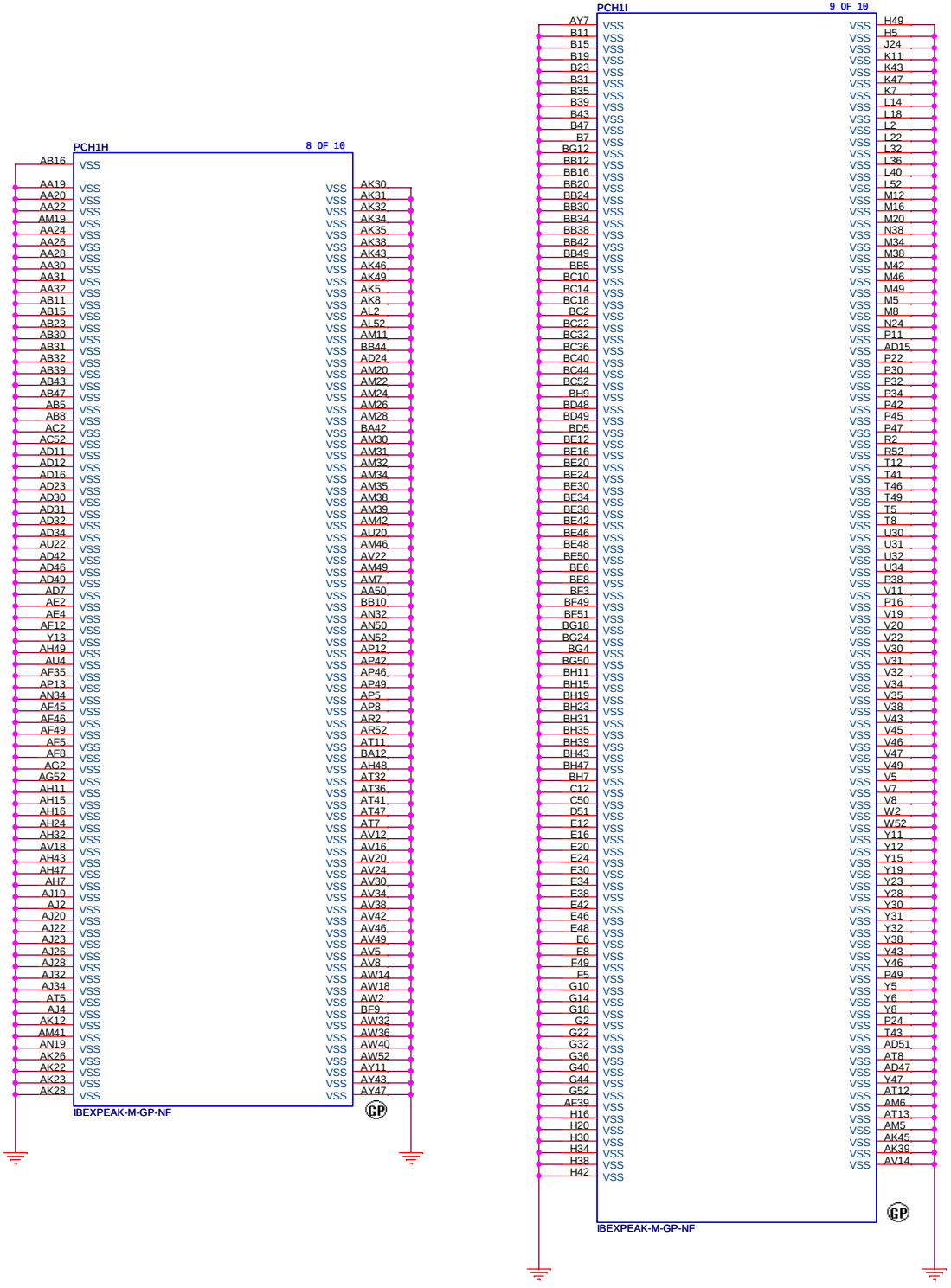


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Title: ***PCH ( 9/9 )***

| Size | Document Number | Rev |
|---|---|---|
| A3 | SJV50-CP | SB |

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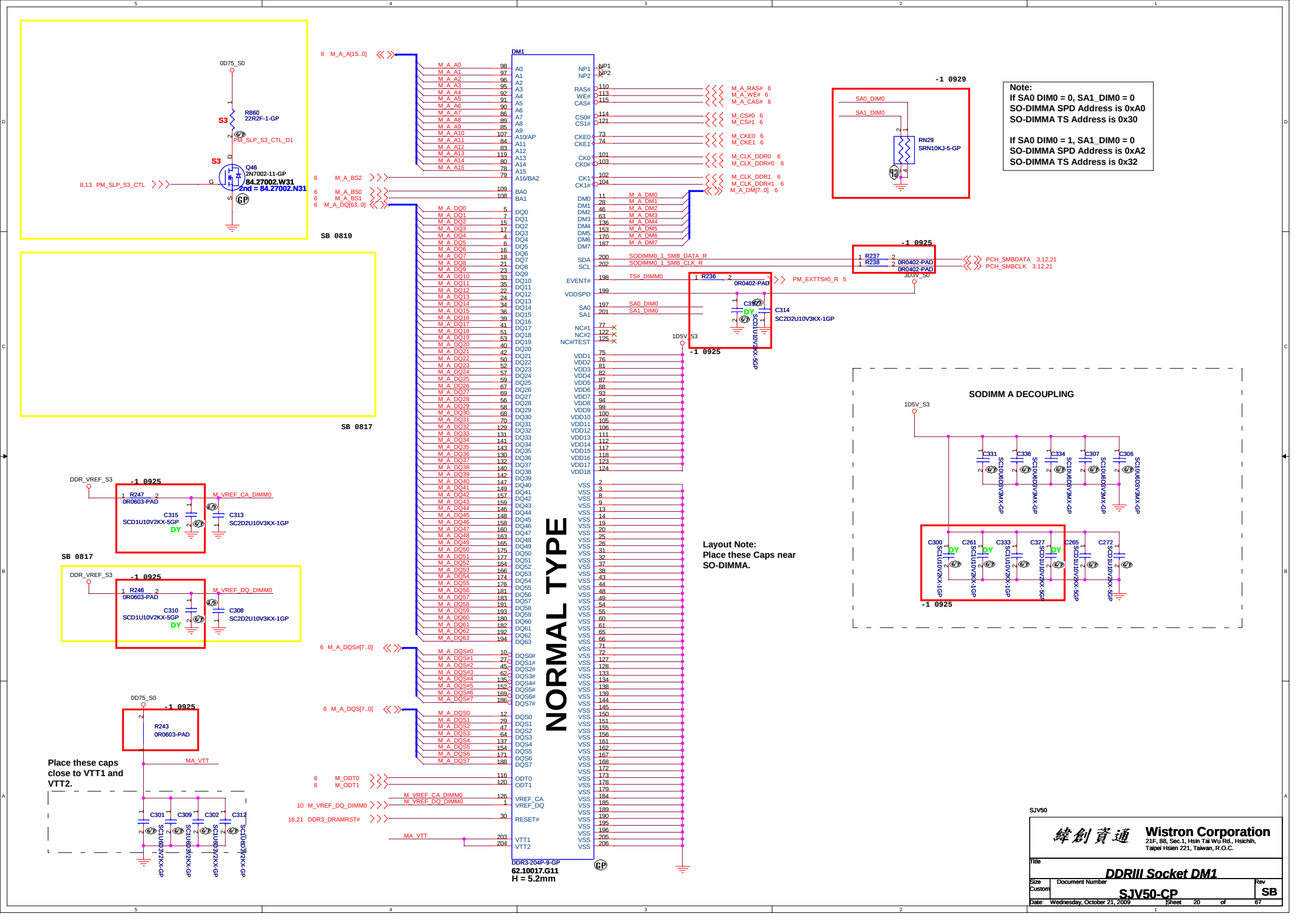
0D75_S0
R860
22R2F-1-GP
S3
PM_SLP_S3_CTL_D1
Q46
2N7002-11-GP
84.27002.W31
2nd = 84.27002.N31
8,13 PM_SLP_S3_CTL
SB 0819
SB 0817
DM1
NORMAL TYPE
DDR3-204P-9-GP
62.10017.G11
H = 5.2mm
-1 0929
SA0_DIM0
SA1_DIM0
RN29
SRN10KJ-5-GP
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
-1 0925
R237
R238
0R0402-PAD
PCH_SMBDATA 3,12,21
PCH_SMBCLK 3,12,21
3D3V_S0
R236
PM_EXTTS#0_R 5
C314
SC2D2U10V3KX-1GP
SCD1U10V2KX-5GP
1D5V_S3
SODIMM A DECOUPLING
C331
C336
C334
C307
C306
SCD10U6D3V3MX-GP
C300
C261
C333
C327
C265
C272
SCD1U10V2KX-1GP
SCD1U10V2KX-5GP
DY
Layout Note:
Place these Caps near
SO-DIMMA.
DDR_VREF_S3
R247
0R0603-PAD
C315
C313
SC2D2U10V3KX-1GP
M_VREF_CA_DIMM0
R246
C310
C308
M_VREF_DQ_DIMM0
R243
MA_VTT
Place these caps
close to VTT1 and
VTT2.
C301
C309
C302
C317
SCD10U6D3V2KX-5GP
M_A_A[15..0]
M_A_BS2
M_A_BS0
M_A_BS1
M_A_DQ[63..0]
M_A_DQS#[7..0]
M_A_DQS[7..0]
M_ODT0
M_ODT1
M_VREF_CA_DIMM0
M_VREF_DQ_DIMM0
16,21 DDR3_DRAMRST#
M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6
M_CS#0 6
M_CS#1 6
M_CKE0 6
M_CKE1 6
M_CLK_DDR0 6
M_CLK_DDR#0 6
M_CLK_DDR1 6
M_CLK_DDR#1 6
M_A_DM[7..0] 6
SODIMM0_1_SMB_DATA_R
SODIMM0_1_SMB_CLK_R
TS#_DIMM0
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM1
Size
Custom
Document Number
SJV50-CP
Rev
SB
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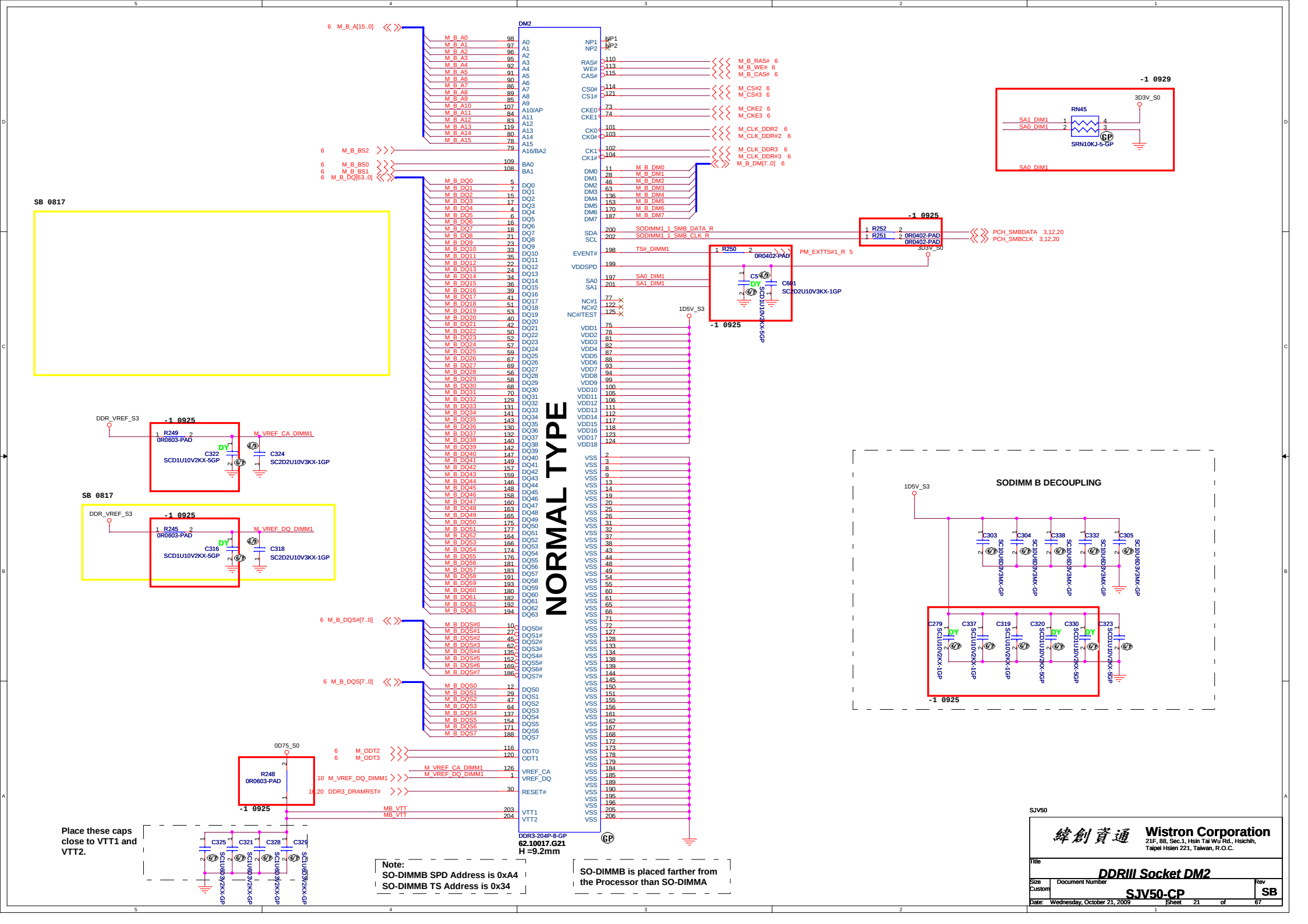
DM2
NORMAL TYPE
DDR3-204P-8-GP
62.10017.G21
H =9.2mm
SB 0817
SB 0817
-1 0925
-1 0929
SODIMM B DECOUPLING
Place these caps close to VTT1 and VTT2.
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
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DDRIII Socket DM2
SJV50-CP
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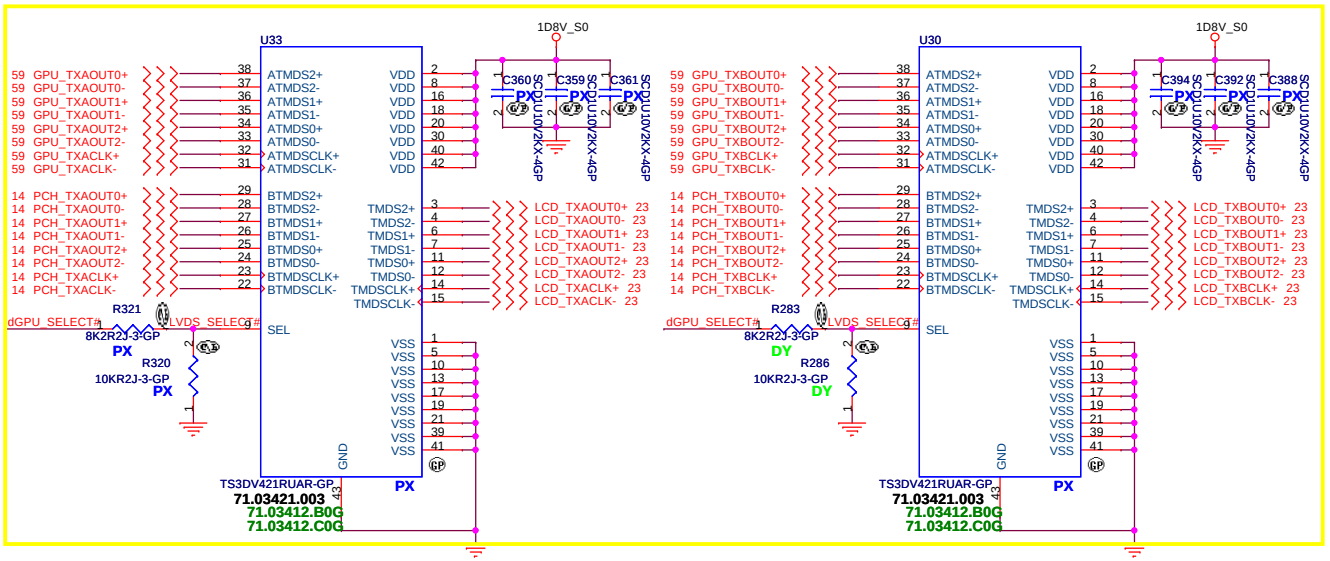
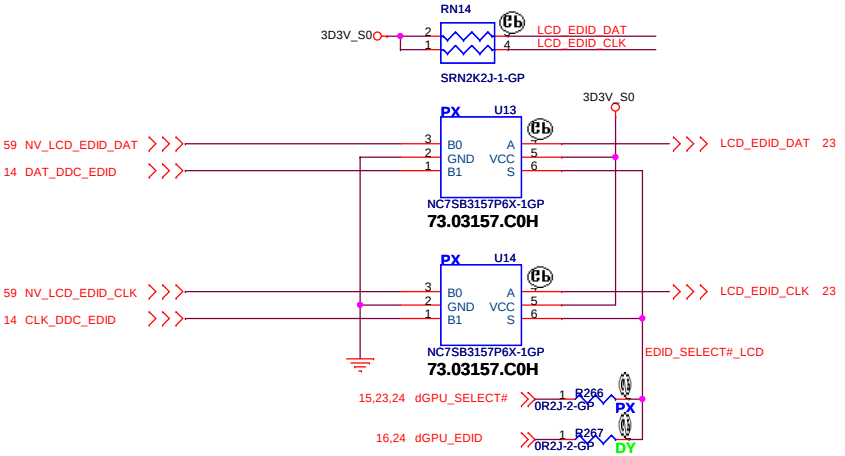
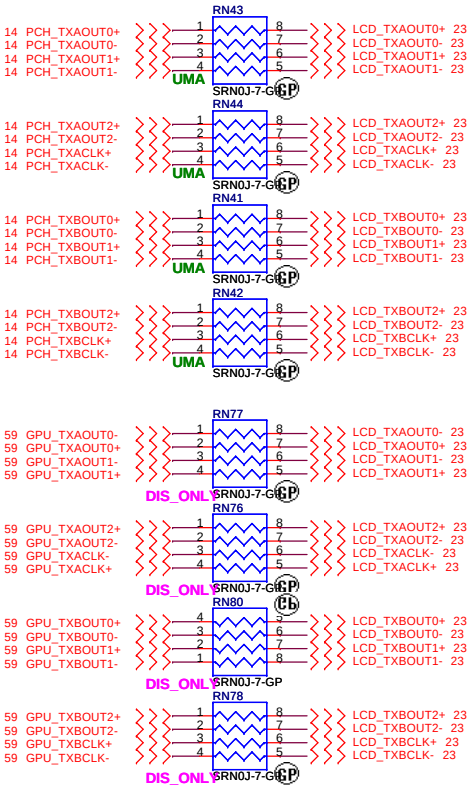
67

SB 0812



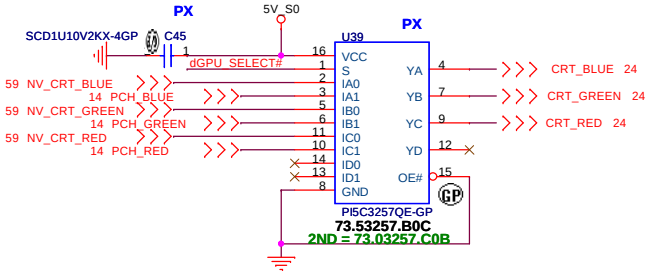



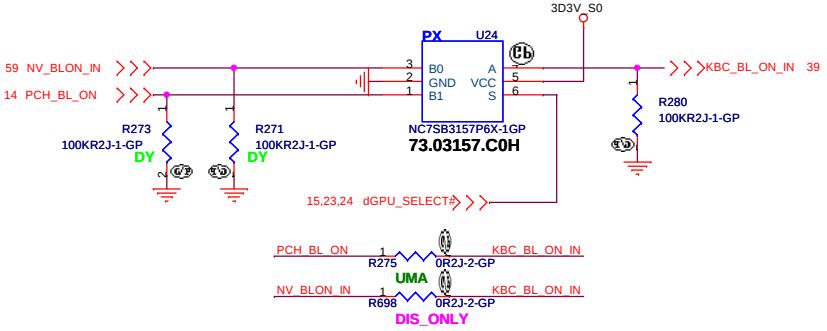



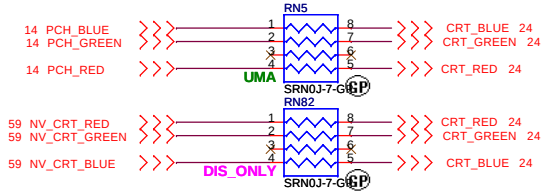

## FUNCTION TABLE

| SEL | FUNCTION | OUTPUT |
|---|---|---|
| L | TMDSn+ = ATMDSn+<br>TMDSn- = ATMDSn-<br>TMDSCLK+ = ATMDSCLK+<br>TMDSCLK- = ATMDSCLK-<br>BTMDSn+ = High Impedance<br>BTMDSn- = High Impedance<br>BTMDSCLK+ = High Impedance<br>BTMDSCLK- = High Impedance | TMDSn+<br>TMDSn-<br>TMDSCLK+<br>TMDSCLK- |
| H | TMDSn+ = BTMDSn+<br>TMDSn- = BTMDSn-<br>TMDSCLK+ = BTMDSCLK+<br>TMDSCLK- = BTMDSCLK-<br>ATMDSn+ = High Impedance<br>ATMDSn- = High Impedance<br>ATMDSCLK+ = High Impedance<br>ATMDSCLK- = High Impedance | TMDSn+<br>TMDSn-<br>TMDSCLK+<br>TMDSCLK- |

| $\overline{E}$ | S | YA | YB | YC | YD | Function |
|---|---|---|---|---|---|---|
| H | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Disable |
| L | L | IA0 | IB0 | IC0 | ID0 | S = 0 |
| L | H | IA1 | IB1 | IC1 | ID1 | S = 1 |

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Title: PX_SWITCH

| Size | Document Number | Rev |
|---|---|---|
| A3 | | SB |

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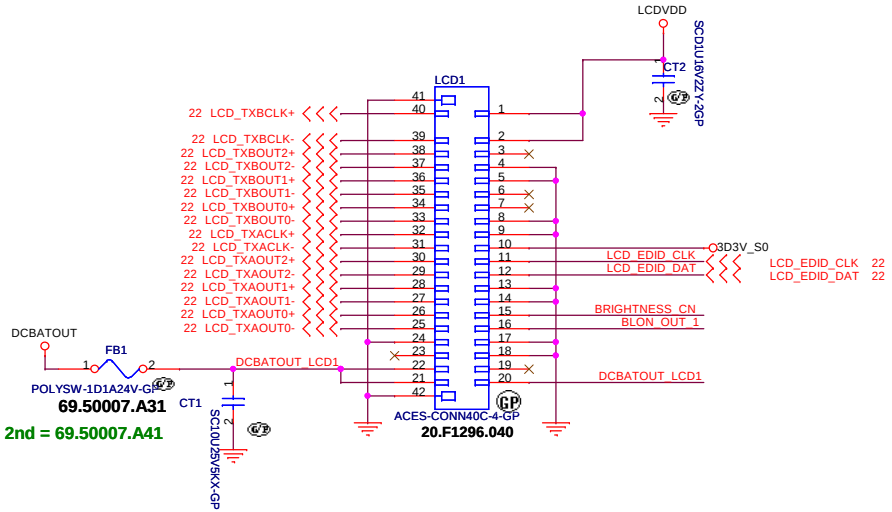
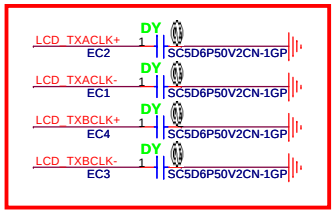
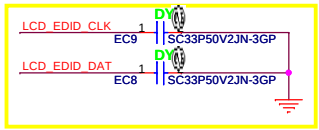
# LCD/INVERTER/CCD CONN



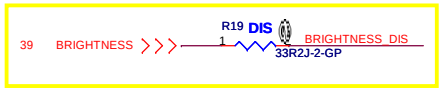




modify by RF

SA 0629 RF

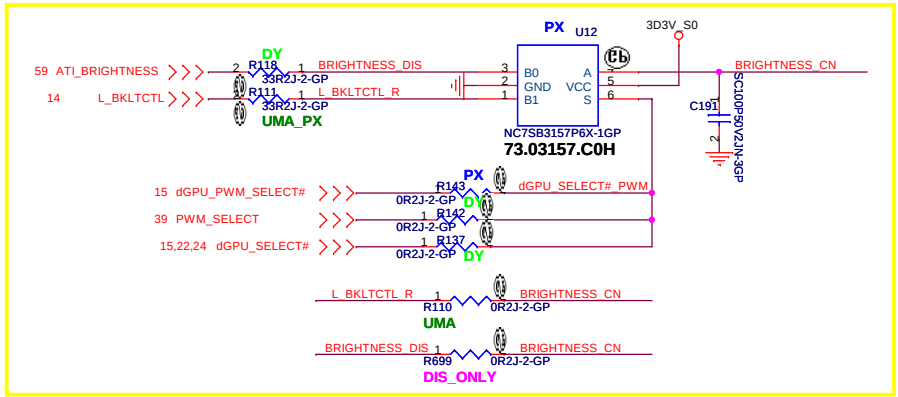


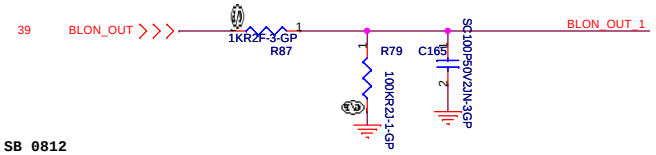

SC 0911



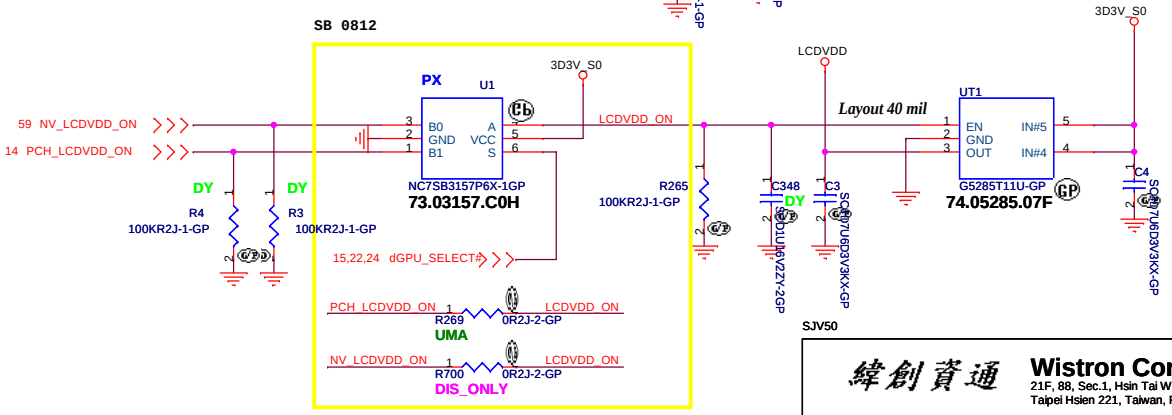

Reserve direct connector to KBC

SC 0911

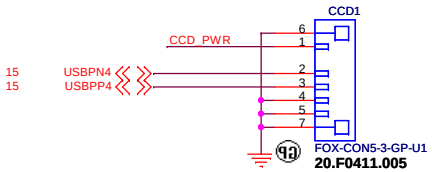


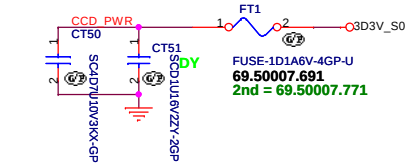




SB 0812

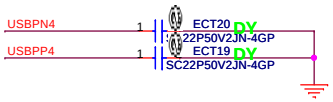


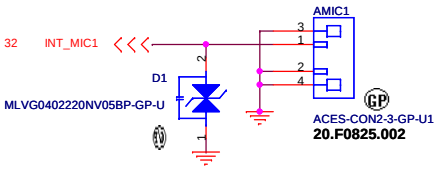

## CCD




## Internal Mic





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Title: LCD CONN

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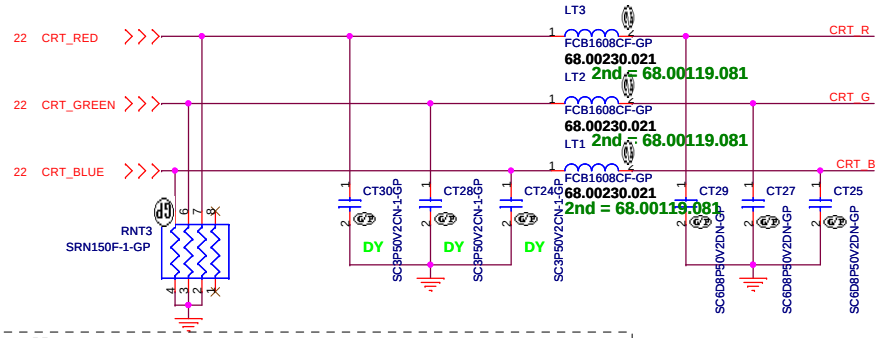
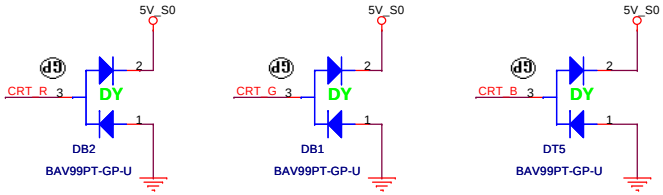
Layout Note:
Place these resistors close to the CRT-out connector



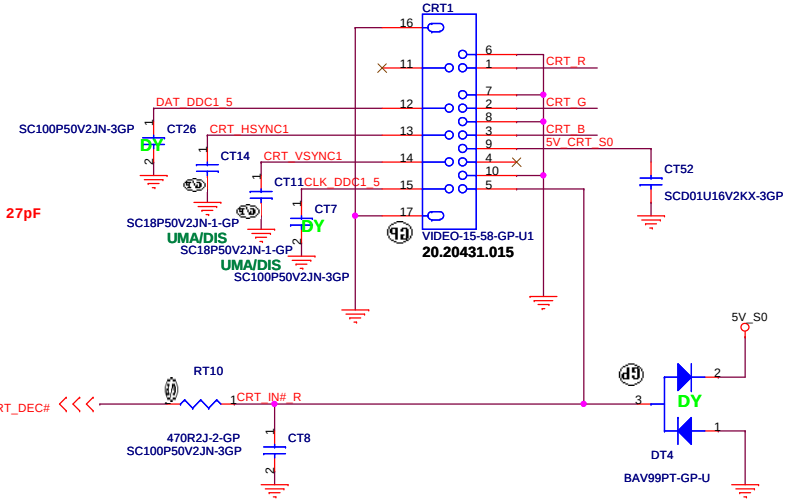

*Layout Note:*
** Must be a ground return path between this ground and the ground on the VGA connector.*
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.*

500mA




# CRT I/F & CONNECTOR

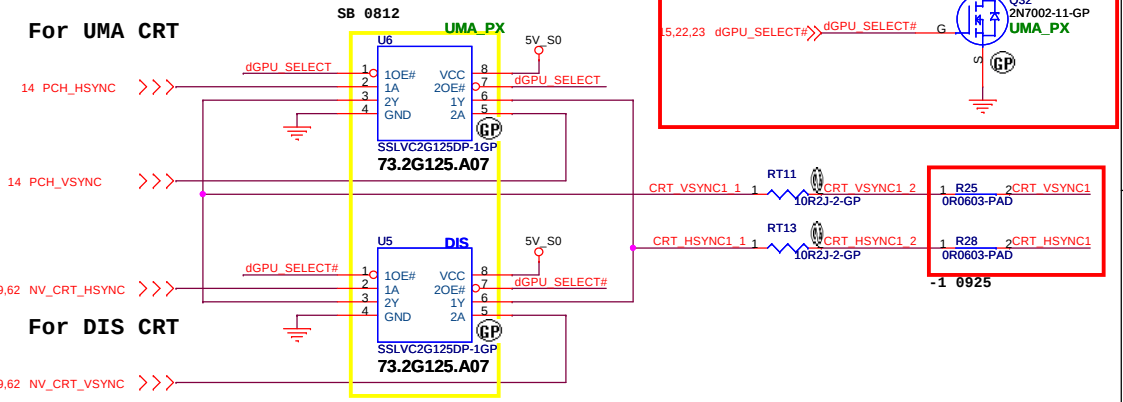
CT87 and CT43
FOR UMA,change to 27pF
(78.27034.1FL)



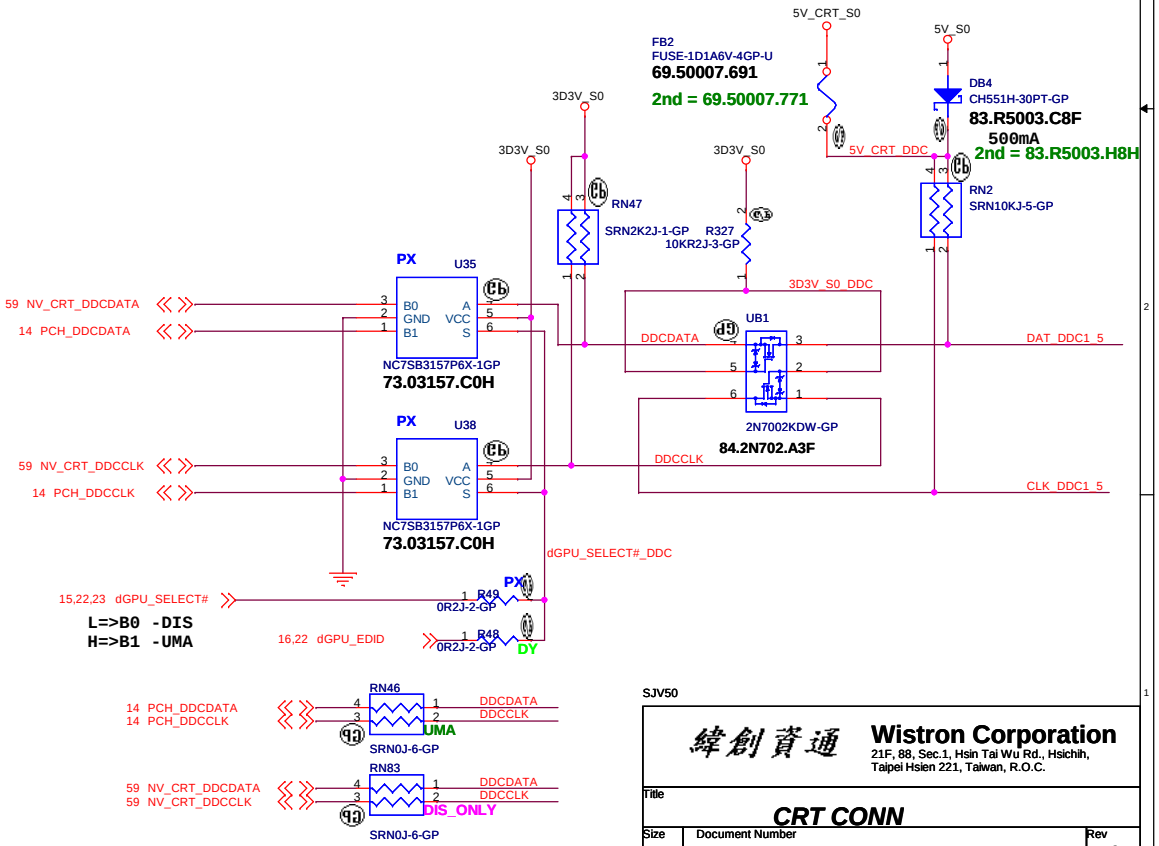

6 1 7 2 8 3 9 4 10 5

## Hsync & Vsync level shift

L=>B0 -UMA
H=>B1 -DIS




## DDC_CLK & DATA level shift

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Title: **CRT CONN**

| Size | Document Number | Rev |
|---|---|---|
| | SJV50-CP | SB |

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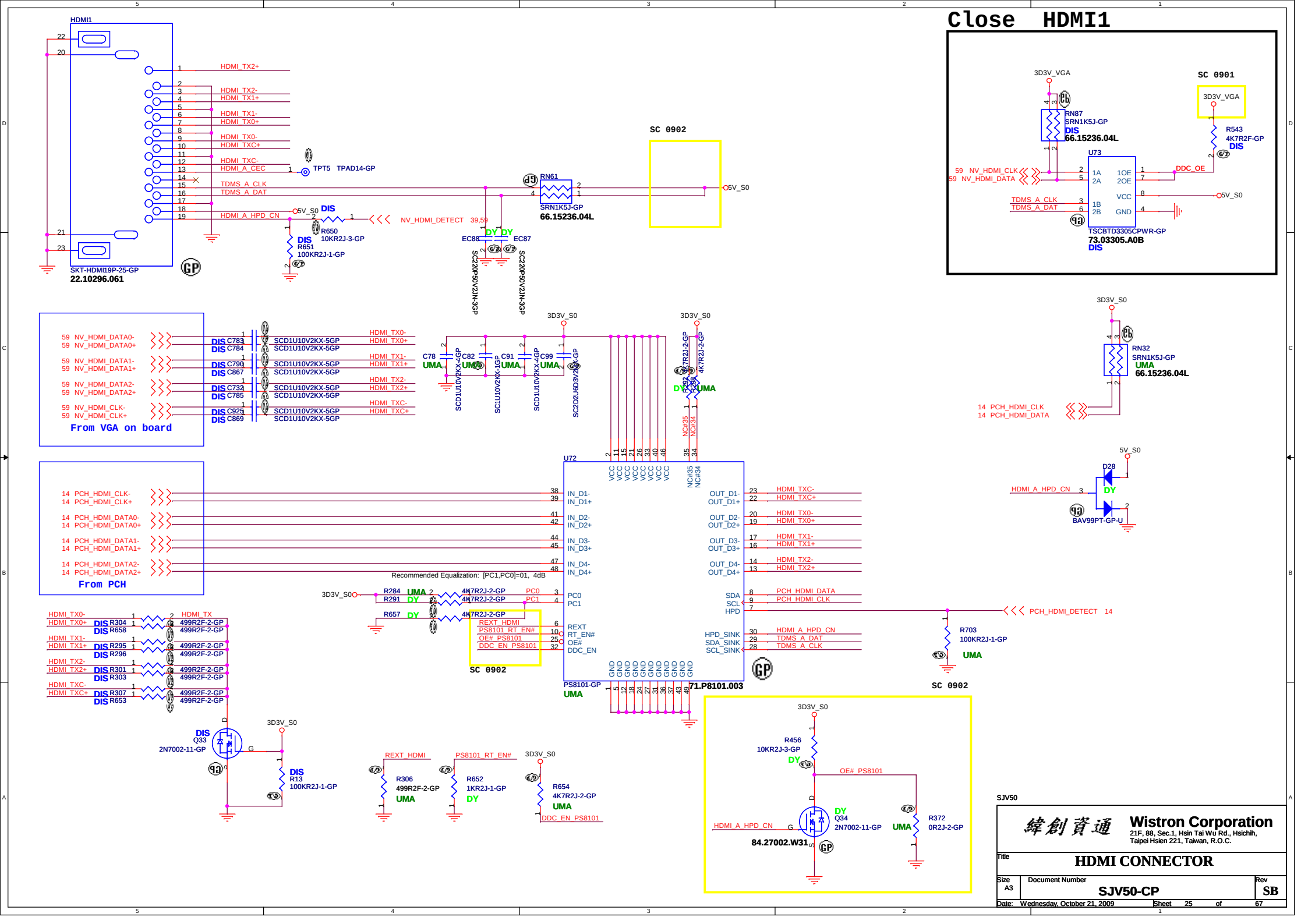
Close HDMI1
HDMI1
SKT-HDMI19P-25-GP
22.10296.061
HDMI_TX2+
HDMI_TX2-
HDMI_TX1+
HDMI_TX1-
HDMI_TX0+
HDMI_TX0-
HDMI_TXC+
HDMI_TXC-
HDMI_A_CEC
TPT5 TPAD14-GP
TDMS_A_CLK
TDMS_A_DAT
HDMI_A_HPD_CN
5V_S0
DIS
R650 10KR2J-3-GP
R651 100KR2J-1-GP
NV_HDMI_DETECT 39,59
RN61
SRN1K5J-GP
66.15236.04L
SC 0902
EC88
EC87
SC220P50V2JN-3GP
From VGA on board
59 NV_HDMI_DATA0-
59 NV_HDMI_DATA0+
59 NV_HDMI_DATA1-
59 NV_HDMI_DATA1+
59 NV_HDMI_DATA2-
59 NV_HDMI_DATA2+
59 NV_HDMI_CLK-
59 NV_HDMI_CLK+
C783
C784
C790
C867
C732
C785
C925
C869
SCD1U10V2KX-5GP
3D3V_S0
C78
C82
C91
C99
UMA
SC1U10V2KX-1GP
SCD1U10V2KX-4GP
SC2D2U6D3V2KX-GP
4K7R2J-2-GP
From PCH
14 PCH_HDMI_CLK-
14 PCH_HDMI_CLK+
14 PCH_HDMI_DATA0-
14 PCH_HDMI_DATA0+
14 PCH_HDMI_DATA1-
14 PCH_HDMI_DATA1+
14 PCH_HDMI_DATA2-
14 PCH_HDMI_DATA2+
U72
PS8101-GP
71.P8101.003
IN_D1-
IN_D1+
IN_D2-
IN_D2+
IN_D3-
IN_D3+
IN_D4-
IN_D4+
OUT_D1-
OUT_D1+
OUT_D2-
OUT_D2+
OUT_D3-
OUT_D3+
OUT_D4-
OUT_D4+
SDA
SCL
HPD
HPD_SINK
SDA_SINK
SCL_SINK
PC0
PC1
REXT
RT_EN#
OE#
DDC_EN
Recommended Equalization: [PC1,PC0]=01, 4dB
R284
R291
R657
4K7R2J-2-GP
REXT_HDMI
PS8101_RT_EN#
OE#_PS8101
DDC_EN_PS8101
SC 0902
PCH_HDMI_DETECT 14
R703
100KR2J-1-GP
UMA
SC 0901
3D3V_VGA
RN87
SRN1K5J-GP
DIS
66.15236.04L
R543
4K7R2F-GP
U73
TSCBTD3305CPWR-GP
73.03305.A0B
DDC_OE
RN32
14 PCH_HDMI_CLK
14 PCH_HDMI_DATA
D28
BAV99PT-GP-U
HDMI_TX0-
HDMI_TX0+
HDMI_TX1-
HDMI_TX1+
HDMI_TX2-
HDMI_TX2+
HDMI_TXC-
HDMI_TXC+
R304
R658
R295
R296
R301
R303
R307
R653
499R2F-2-GP
Q33
2N7002-11-GP
R13
100KR2J-1-GP
R306
499R2F-2-GP
R652
1KR2J-1-GP
R654
4K7R2J-2-GP
R456
10KR2J-3-GP
Q34
2N7002-11-GP
R372
0R2J-2-GP
84.27002.W31
SJV50
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Title
HDMI CONNECTOR
Size A3
Document Number SJV50-CP
Rev SB
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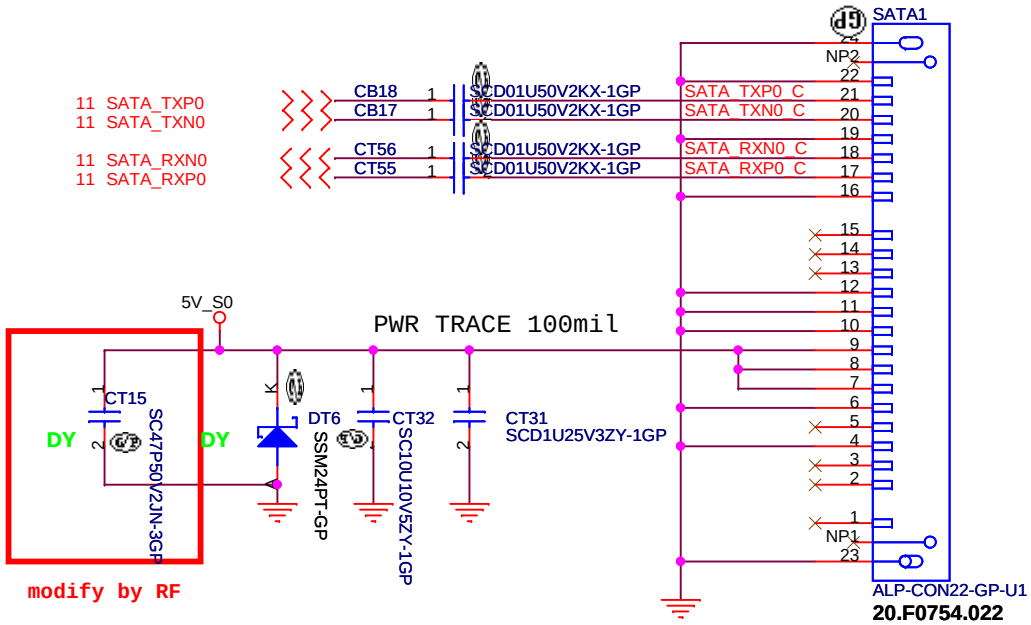
# SATA Connector

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| | |
|---|---|
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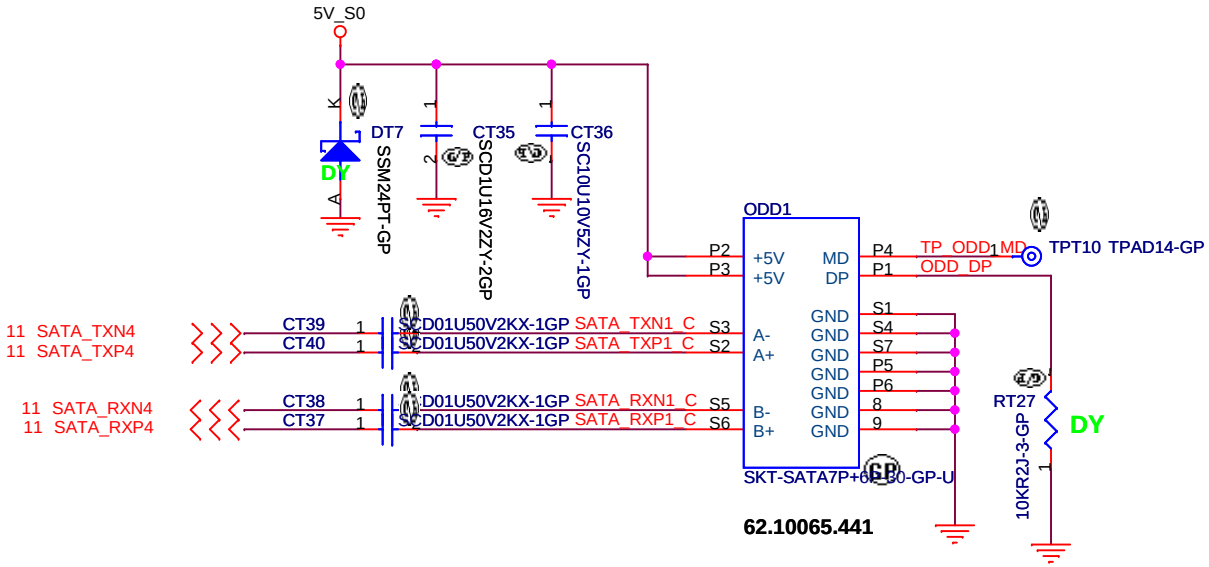
| Title | ***HDD CONN*** |
| Size | Document Number: **SJV50-CP** — Rev: SB |
| Date: Wednesday, October 21, 2009 | Sheet 26 of 67 |

# ODD Connector

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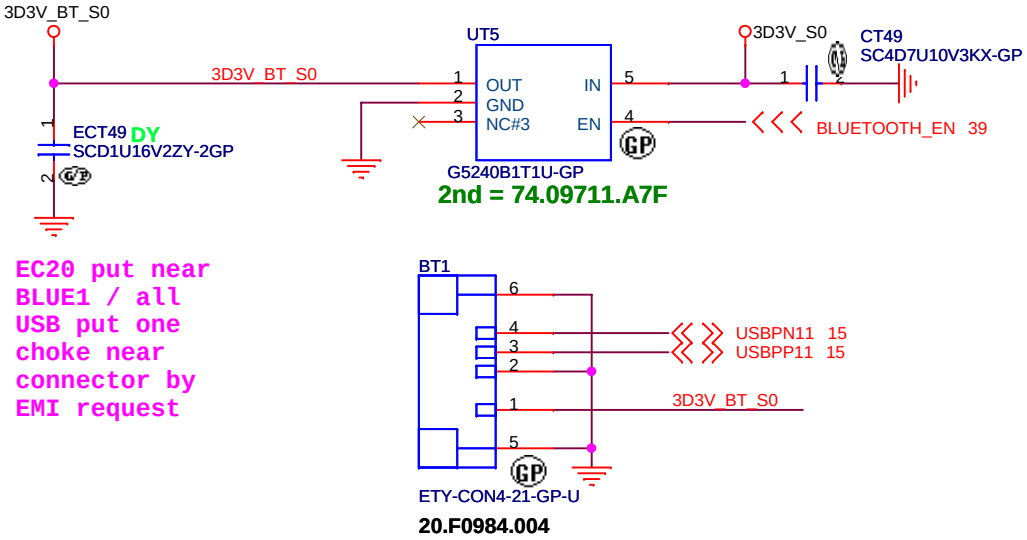
| | | |
|---|---|---|
| Title | ODD | |
| Size | Document Number SJV50-CP | Rev SB |
| Date: Wednesday, October 21, 2009 | Sheet 27 of 67 | |

# BLUETOOTH MODULE

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Title: BLUETOOTH

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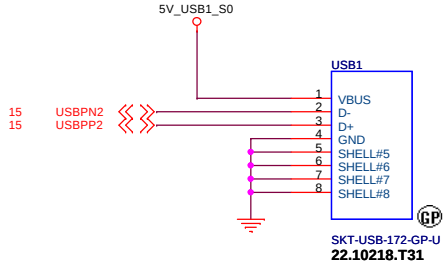


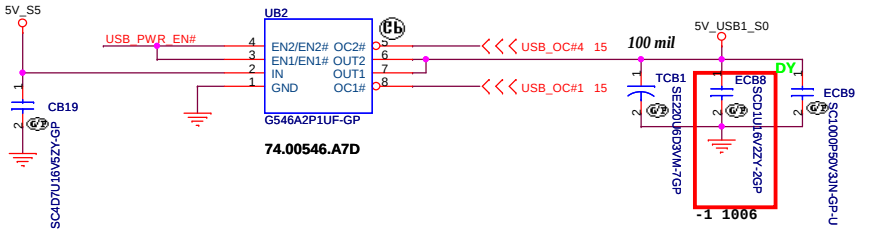


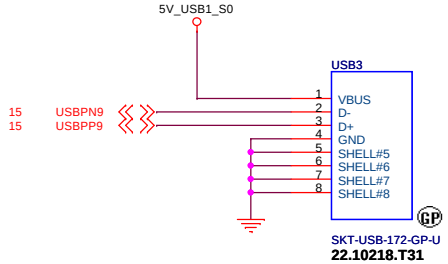


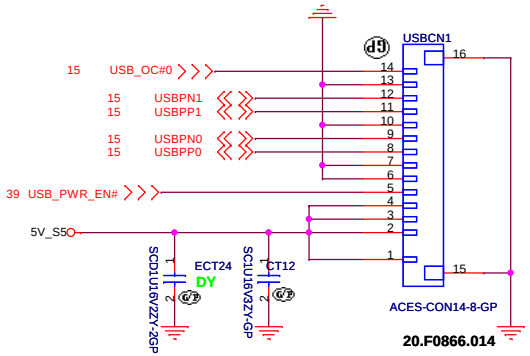


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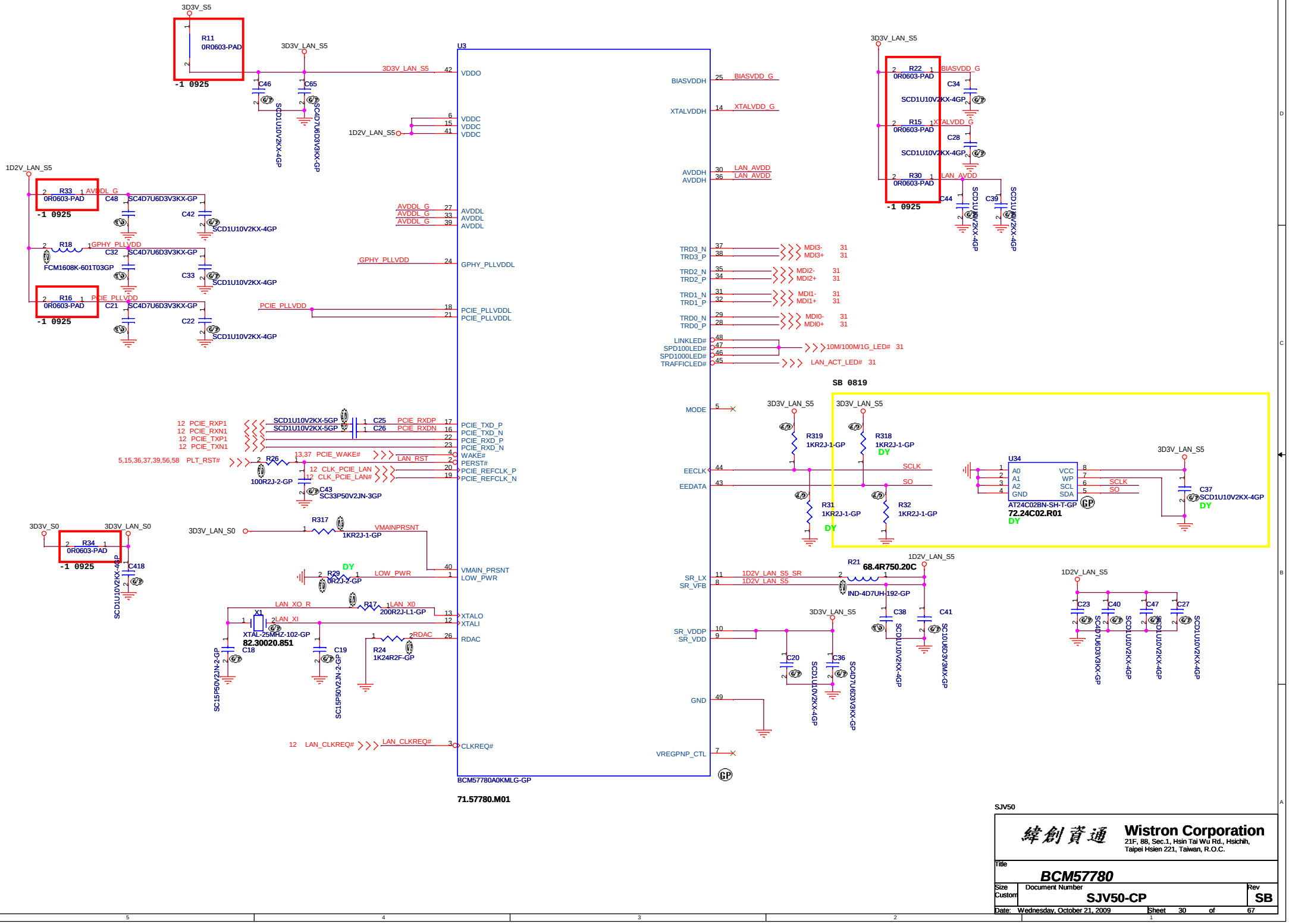
| | | |
|---|---|---|
| Title | *USB CONN* | |
| Size | Document Number SJV50-CP | Rev SB |
| Date: Wednesday, October 21, 2009 | Sheet 29 of 67 | |

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| | | |
|---|---|---|
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| Title: ***BCM57780*** | | |
| Size: Custom | Document Number: **SJV50-CP** | Rev: **SB** |
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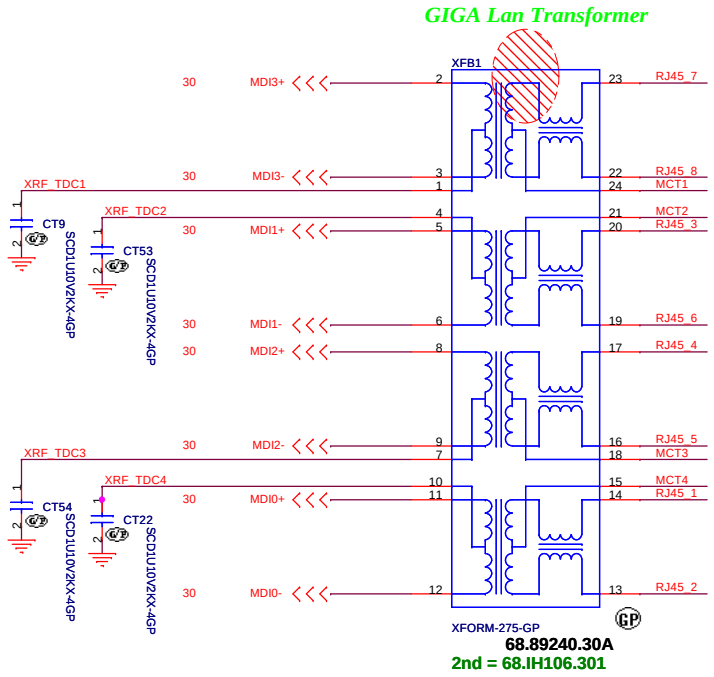
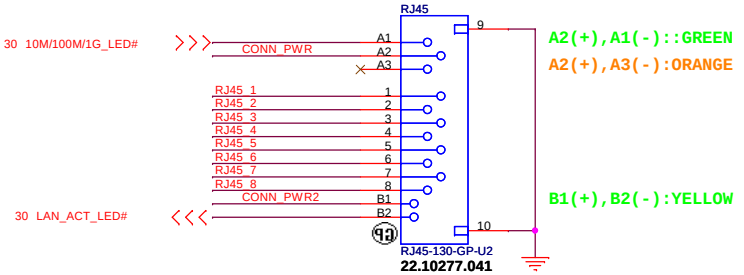
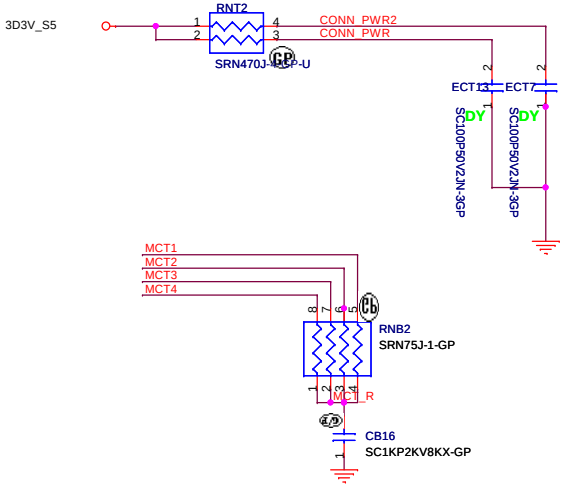
# LAN Connector

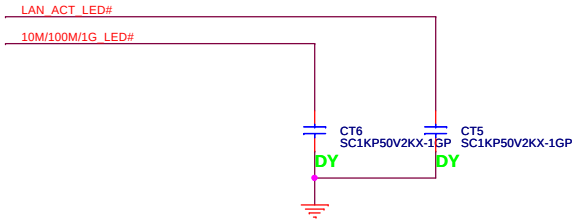
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

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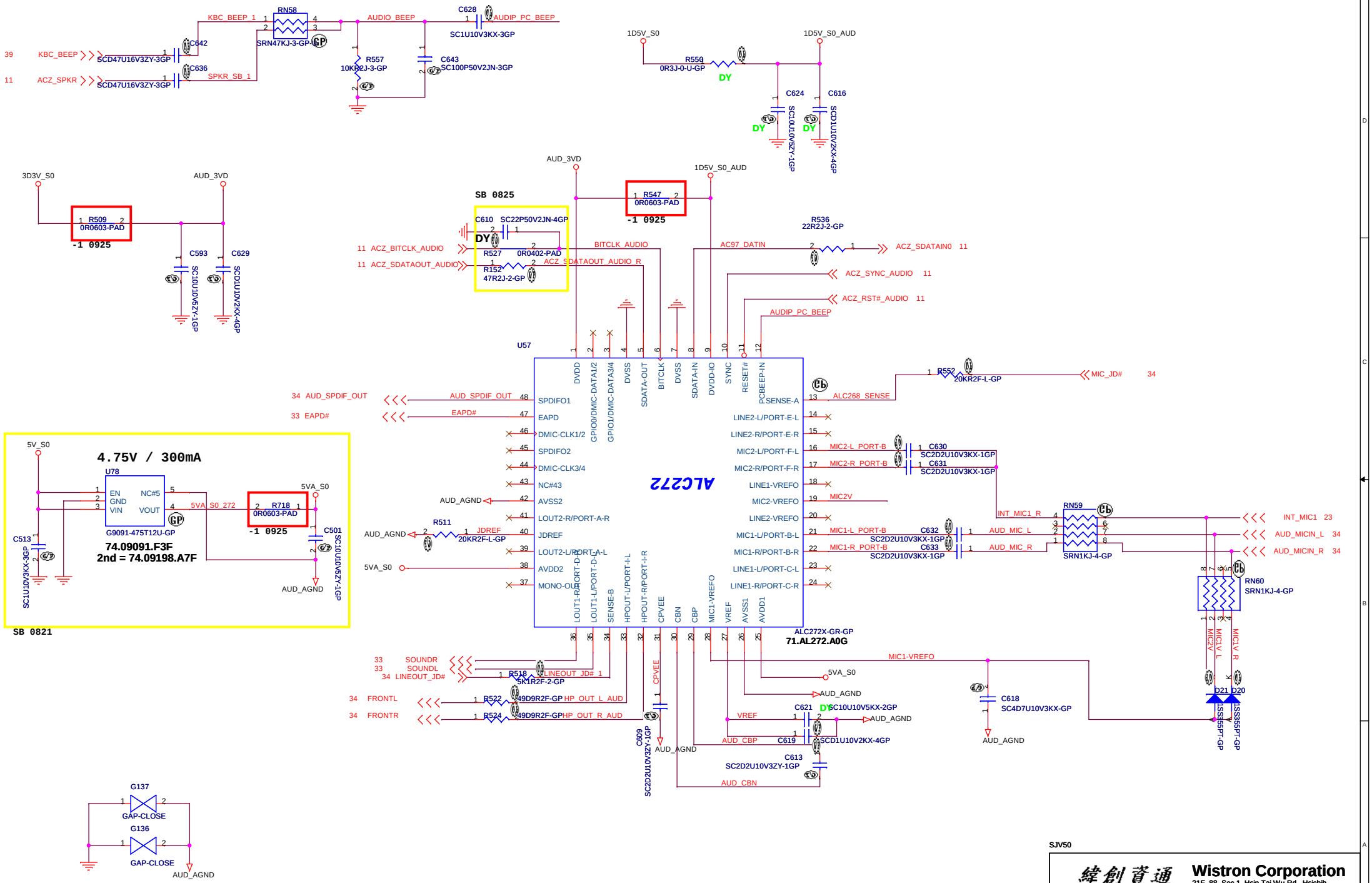
| | | |
|---|---|---|
| Title: **LAN CONN** | | |
| Size: A3 | Document Number: SJV50-CP | Rev: SB |
| Date: Wednesday, October 21, 2009 | Sheet 31 of 67 | |

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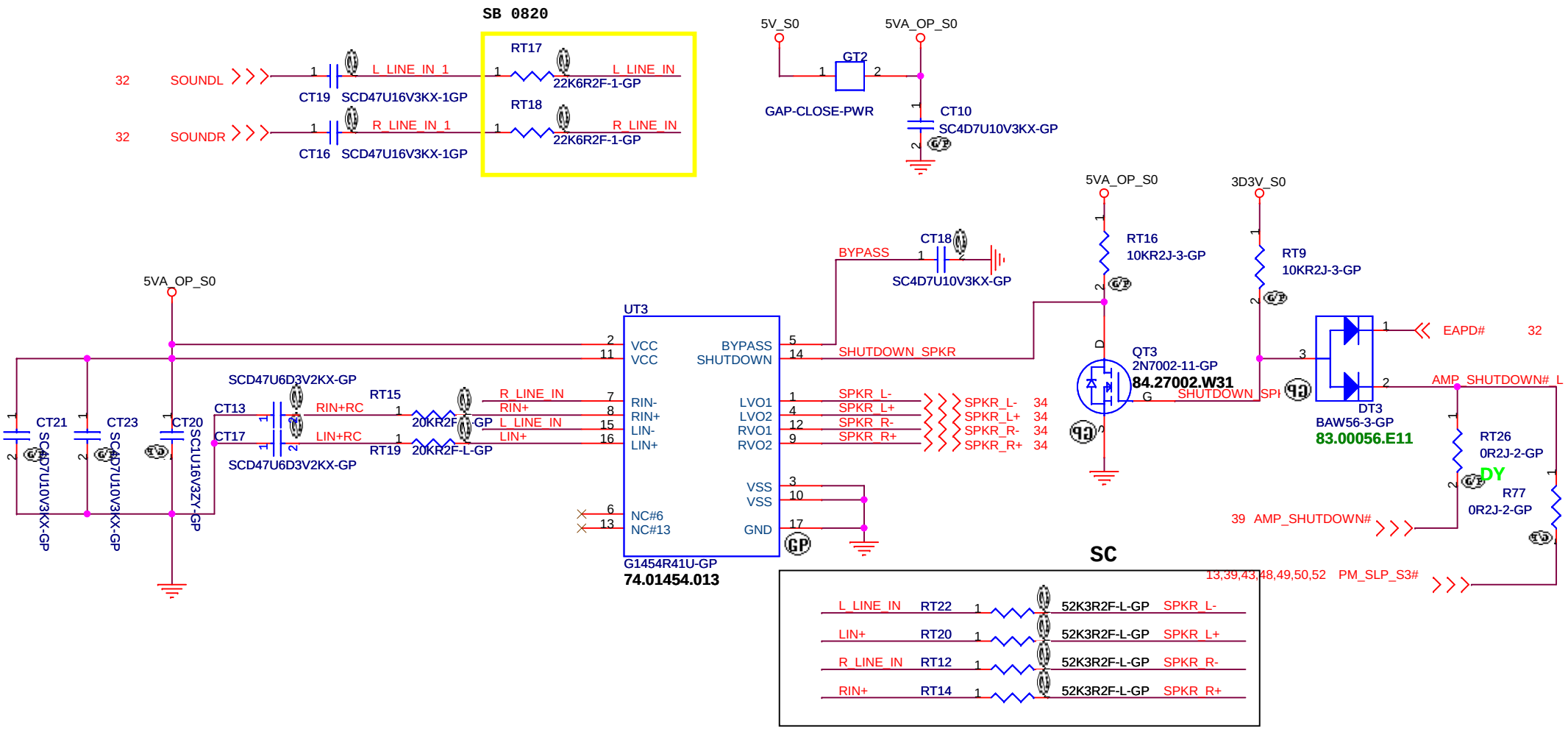
| | | |
|---|---|---|
| Title | *Azalia codec ALC272* | |
| Size A3 | Document Number SJV50-CP | Rev SB |
| Date: Wednesday, October 21, 2009 | Sheet 32 of 67 | |

# AUDIO OP AMPLIFIER

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| | | |
|---|---|---|
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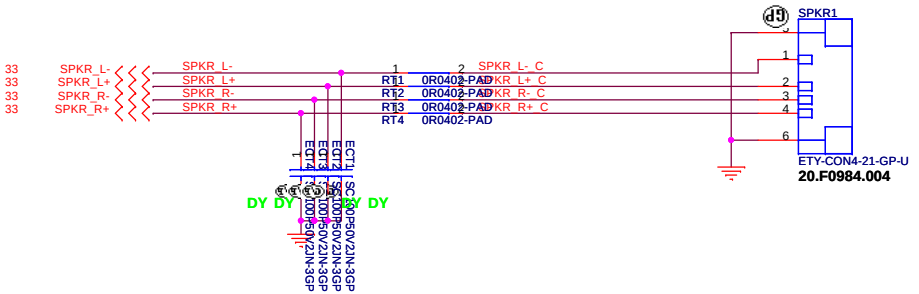
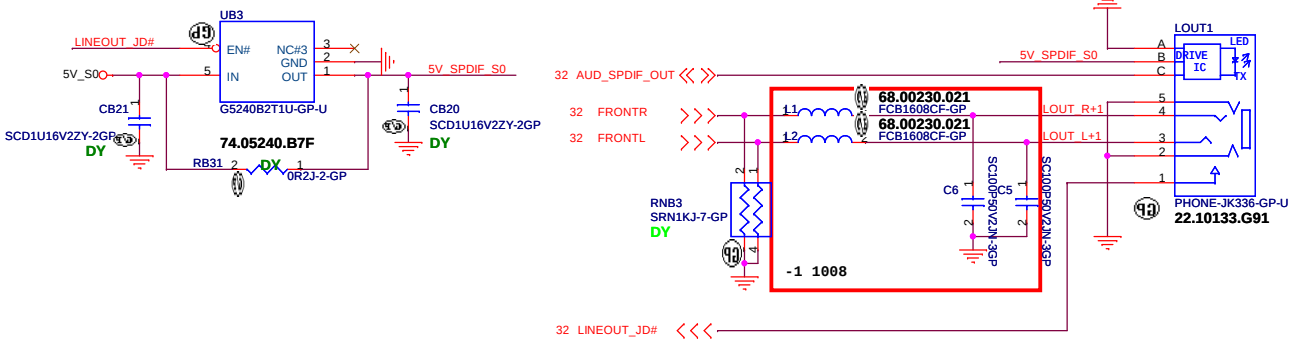
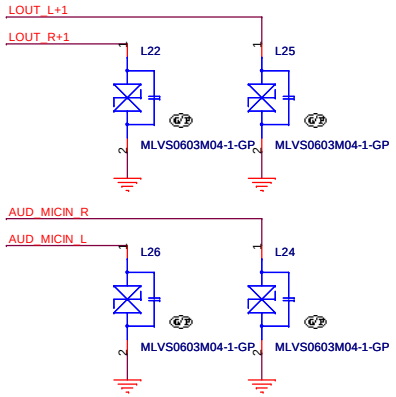
| Title | *AUDIO AMP AND JACK* | |
| Size | Document Number<br>SJV50-CP | Rev<br>SB |
| Date: Wednesday, October 21, 2009 | Sheet 33 of 67 | |

# Internal Speaker

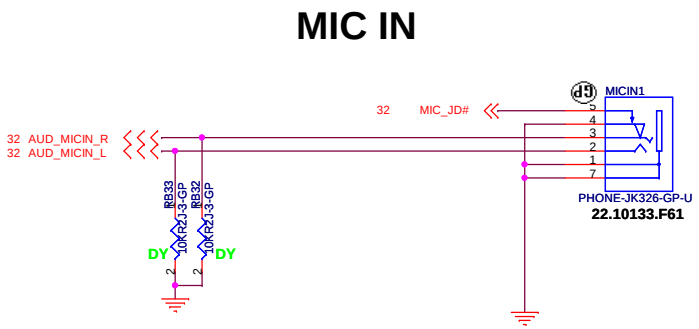


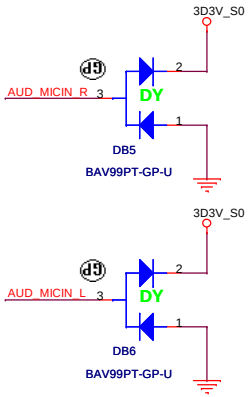

# LINE OUT




# MIC IN




SJV50

| | | |
|---|---|---|
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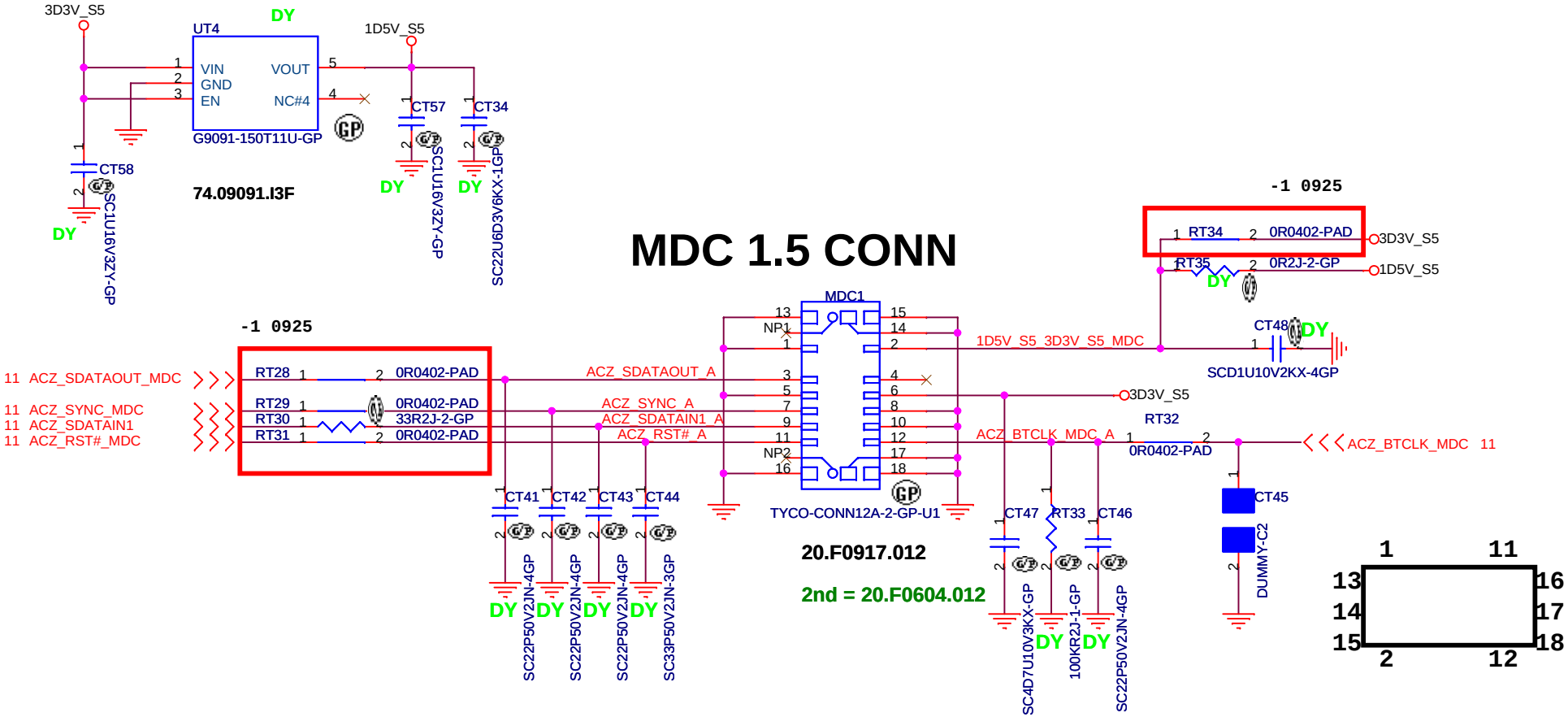
| Title: *AUDIO jack* | | |
| Size | Document Number: SJV50-CP | Rev: SB |
| Date: Wednesday, October 21, 2009 | Sheet 34 of 67 | |

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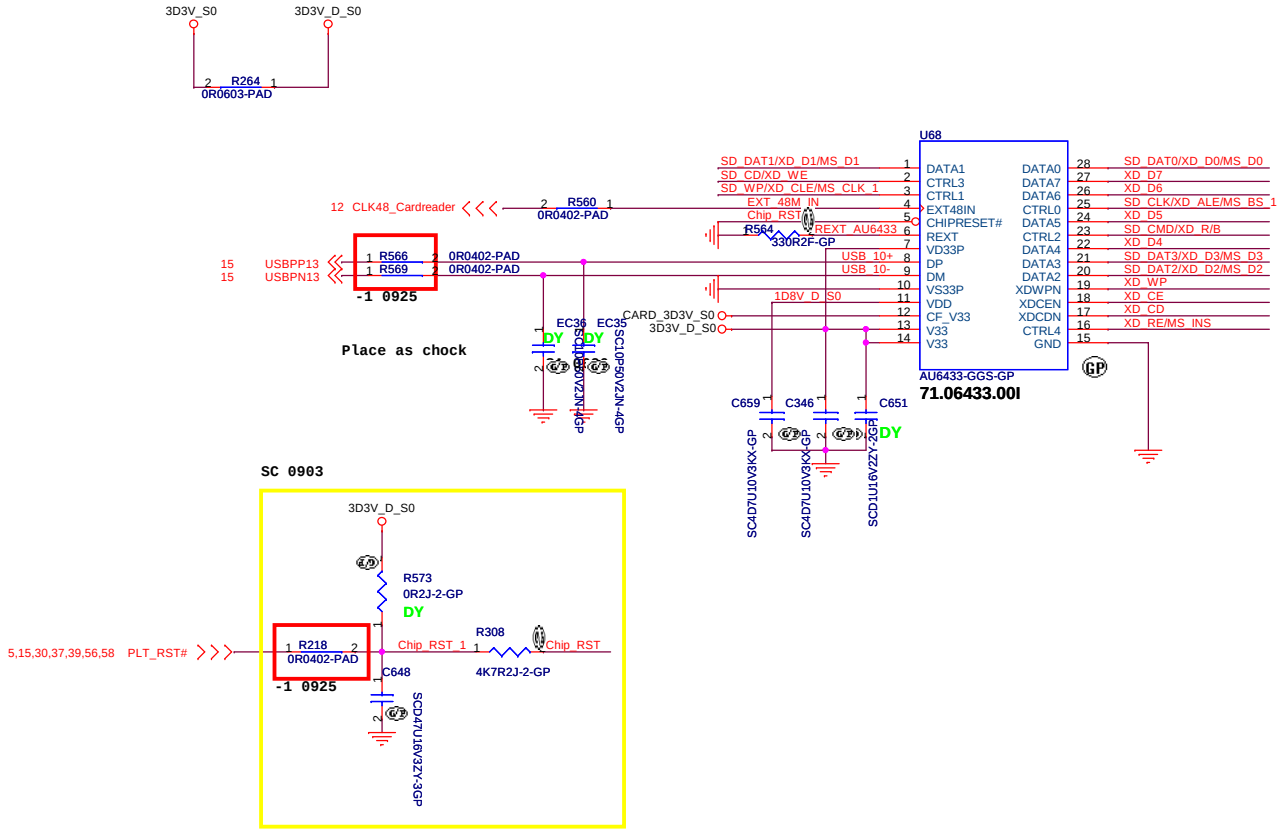
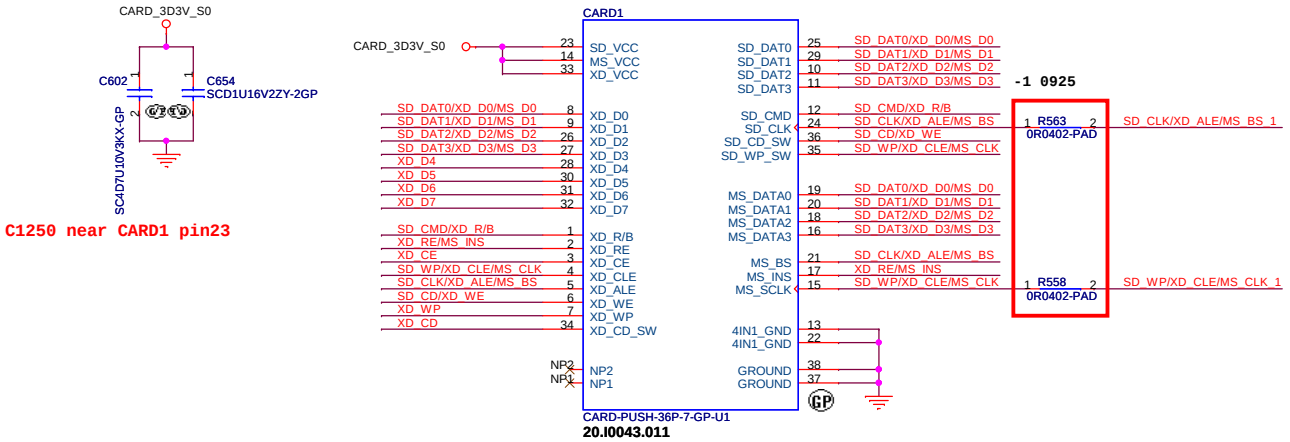
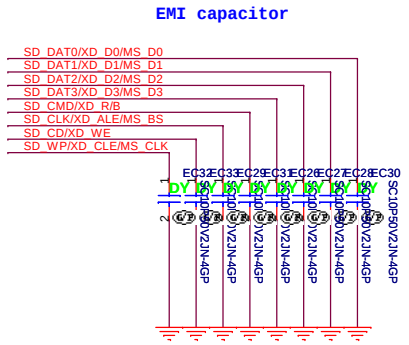
| | | |
|---|---|---|
| Title | MDC | |
| Size | Document Number: SJV50-CP | Rev: SB |
| Date: Wednesday, October 21, 2009 | Sheet 35 of 67 | |




# 5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)

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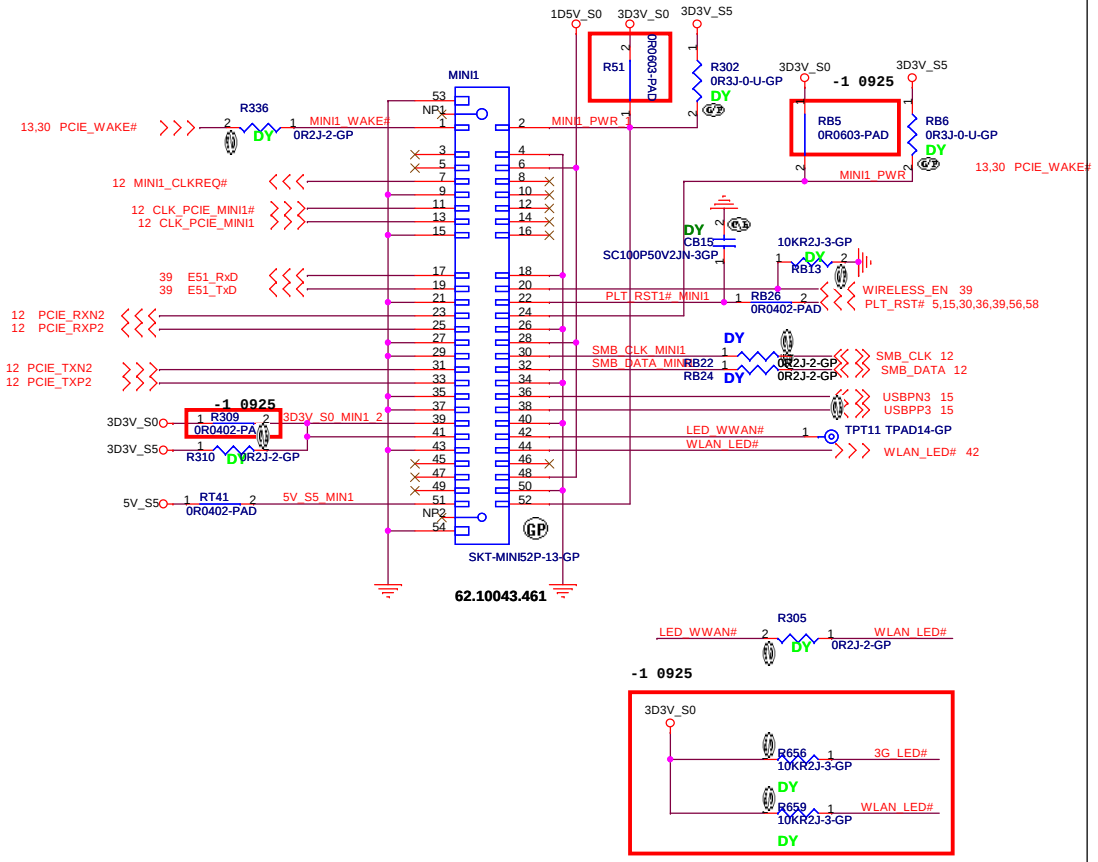
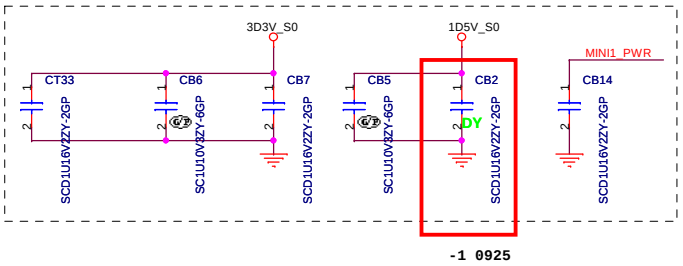
| | | |
|---|---|---|
| Title | Cardreader | |
| Size | Document Number | Rev |
| | SJV50-CP | SB |
| Date: Wednesday, October 21, 2009 | Sheet 36 of 67 | |

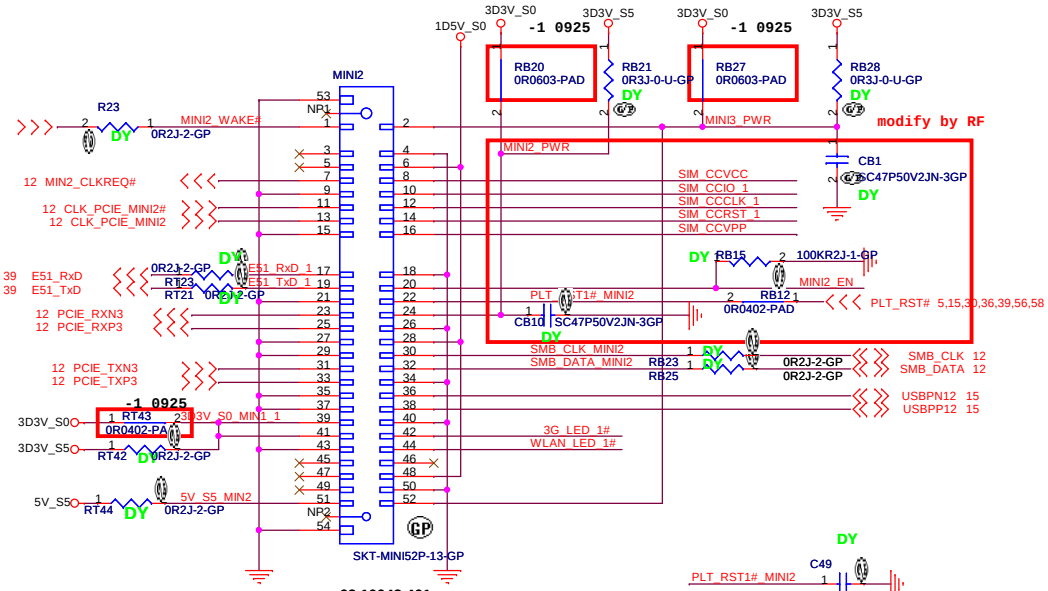
# Mini Card Connector(WLAN) Half Card
## Support debug-card



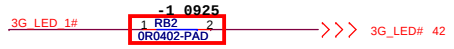

Place near MINI1




# Mini Card Connector(Robson2 and 3G)

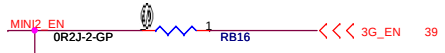



**3G**



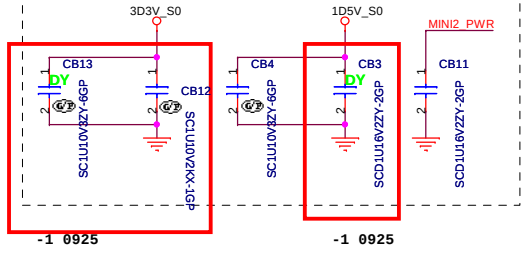

**NO_3G**

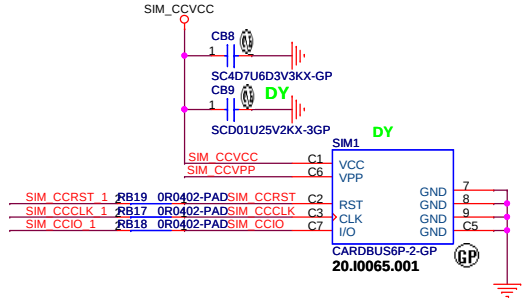

**3G**




**NO_3G**


Place near MINIC2

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| | | |
|---|---|---|
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| Title: MINI CARD | | |
| Size: A3 | Document Number: SJV50-CP | Rev: SB |
| Date: Wednesday, October 21, 2009 | Sheet 37 of 67 | |

for T8 thermal diode

84.T3904.C11

2nd = 84.03904.P11

Q3 MMBT3904-4-GP

C118 SC2200P50V2KX-2GP

G787_DP2

G787_DN2

C1252 & C1254 CLOSE TO G787

for system thermal diode

84.T3904.C11

2nd = 84.03904.P11

Q15 MMBT3904-4-GP

C326 SC2200P50V2KX-2GP

G787_DP1

G787_DN1

3D3V_S0

3D3V_AUX_S5

RN23 SRN10KJ-7GP

-1 0929

RSMRST#_CTRL

Q11

RSMRST#

PURE_HW_SHUTDOWN#

2N7002-11-GP

2ND = 84.27002.N31

D7 BAT54PT-GP

2ND = 83.BAT54.D81

83.00054.T81

DY

C544 SCD1U16V2ZY-2GP

RSMRST# 39,43

(dummy, KBC already delay)

5V_S0

R426 100R2J-2-GP

C532 SCD1U16V2KX-3GP

5V_S0_THERMAL

U15

VCC DVCC DP2DN3 DN2DP3 DXP1 SGND1 NC#1 NC#3 NC#12 SDA SCL THERM_SET THERM# ALERT# TEST GND

G787S11U-GP

74.00787.0B9

C147 SC10U6D3V3MX-GP

G787_DP2 G787_DN2 G787_DP1 G787_DN1

SMBD_THERM 39,42,59

SMBC_THERM 39,42,59

THERM_SET

PURE_HW_SHUTDOWN#

ALERT#

R183 10KR2J-3-GP

3D3V_S0

TP28

TP49 TPAD14-GP

R429 21KR2F-GP

R430 49K9R2F-L-GP

T8=90C

THERM_SET = [(Tset-72) x 0.02+0.34] x VCC

-1 0925

39 FAN_TACH1

R350 0R2J-2-GP DY

R351 10KR2J-3-GP DY

D15 RB551V30-GP

83.R5003.H8H

2ND = 83.5R003.08F

FAN_TACH1_D

39 FAN1_PWM

R106 0R0402-PAD

SCD1U16V2ZY-2GR

EC7 DY

SC 0902

FAN1_PWM_R

FAN1

For CPU FAN

C450 SC10U10V2ZY-1GP

D14 RB551V30-GP

2ND = 83.5R003.08F

83.R5003.H8H

ACES-CON4-GP-U1

20.F0714.004

2ND = 20.D0196.104

SJV50

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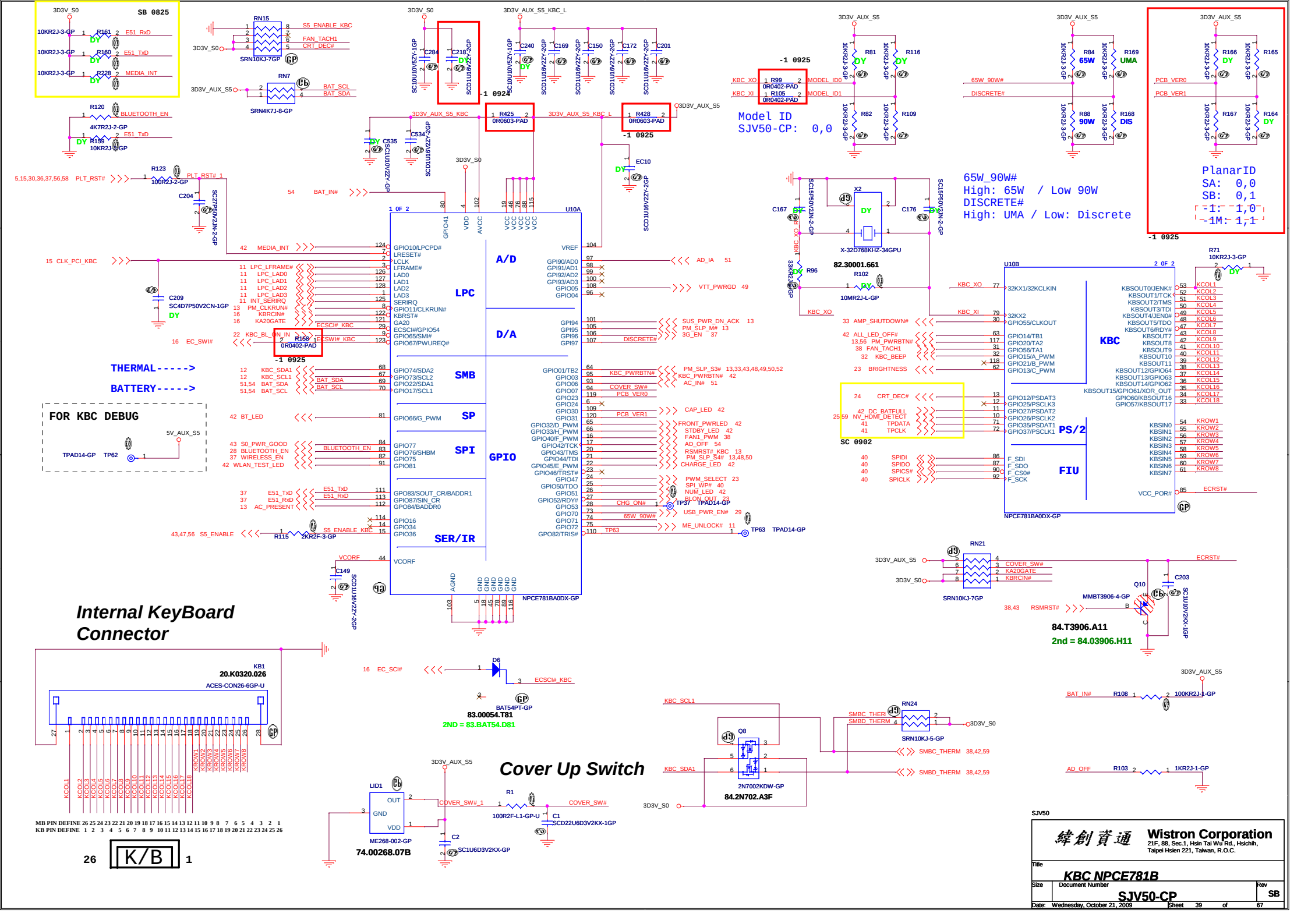
Title: Thermal/Fan Connector

Size | Document Number: SJV50-CP | Rev: SB

Date: Wednesday, October 21, 2009 | Sheet 38 of 67


SB 0825
U10A
NPCE781BA0DX-GP
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
U10B
KBC
PS/2
FIU
SC 0902
-1 0925
-1 0924
Model ID
SJV50-CP: 0,0
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
THERMAL----->
BATTERY----->
FOR KBC DEBUG
Internal KeyBoard Connector
Cover Up Switch
84.T3906.A11
2nd = 84.03906.H11
83.00054.T81
2ND = 83.BAT54.D81
74.00268.07B
84.2N702.A3F
82.30001.661
X-32D768KHZ-34GPU
20.K0320.026
ACES-CON26-6GP-U
ME268-002-GP
SRN10KJ-7GP
SRN4K7J-8-GP
SRN10KJ-5-GP
BAT54PT-GP
2N7002KDW-GP
MMBT3906-4-GP
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC NPCE781B
SJV50-CP
SB
Wednesday, October 21, 2009
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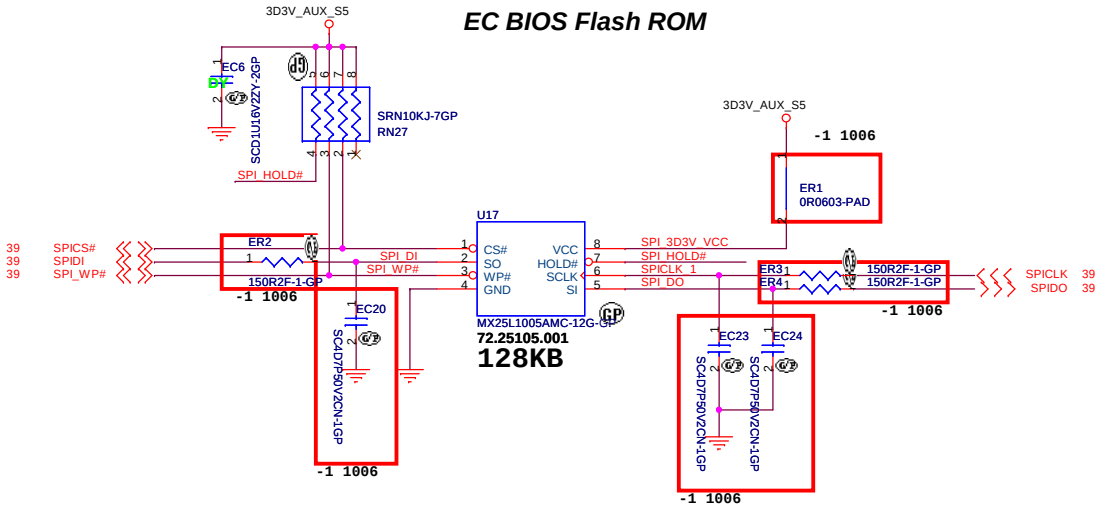
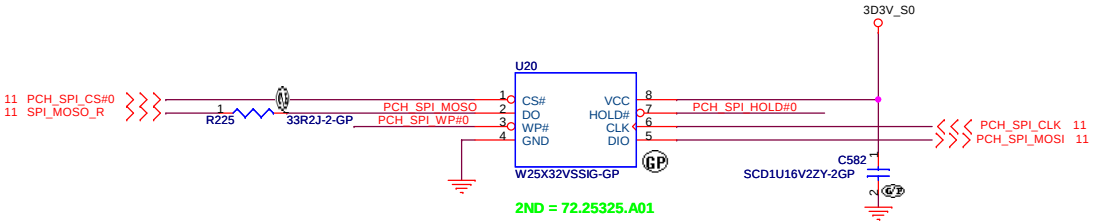
## EC BIOS Flash ROM



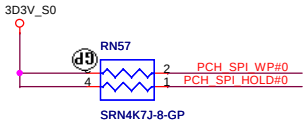

## System BIOS Flash ROM




**32M Bits**

## GOLDEN FINGER FOR DEBUG BOARD

-1 1009

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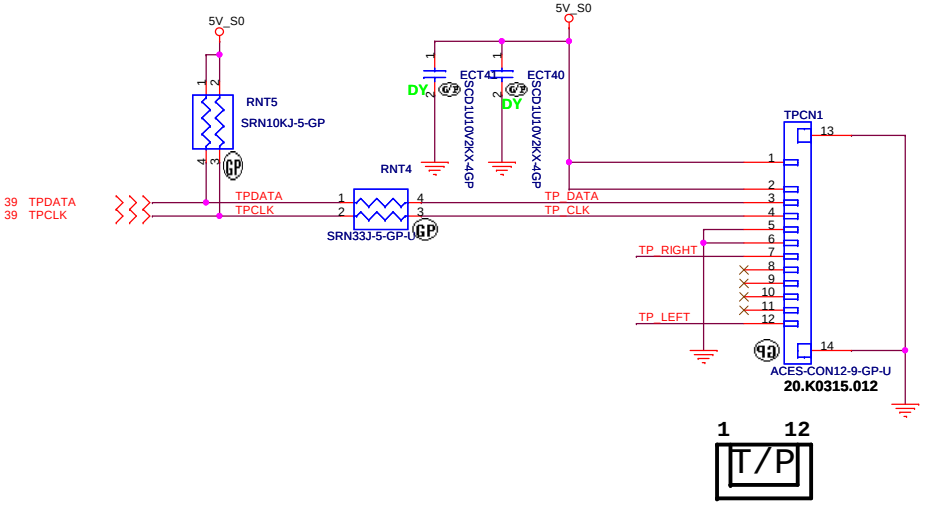
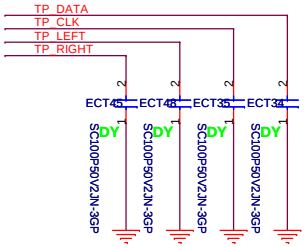
Title: **BIOS**

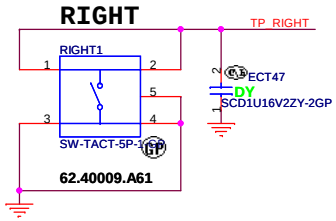
Size | Document Number: **SJV50-CP** | Rev: **SB**

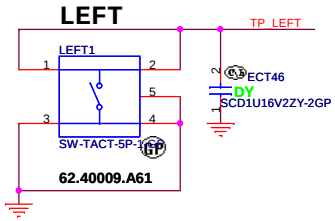
Date: Wednesday, October 21, 2009 | Sheet 40 of 67

# TOUCH PAD



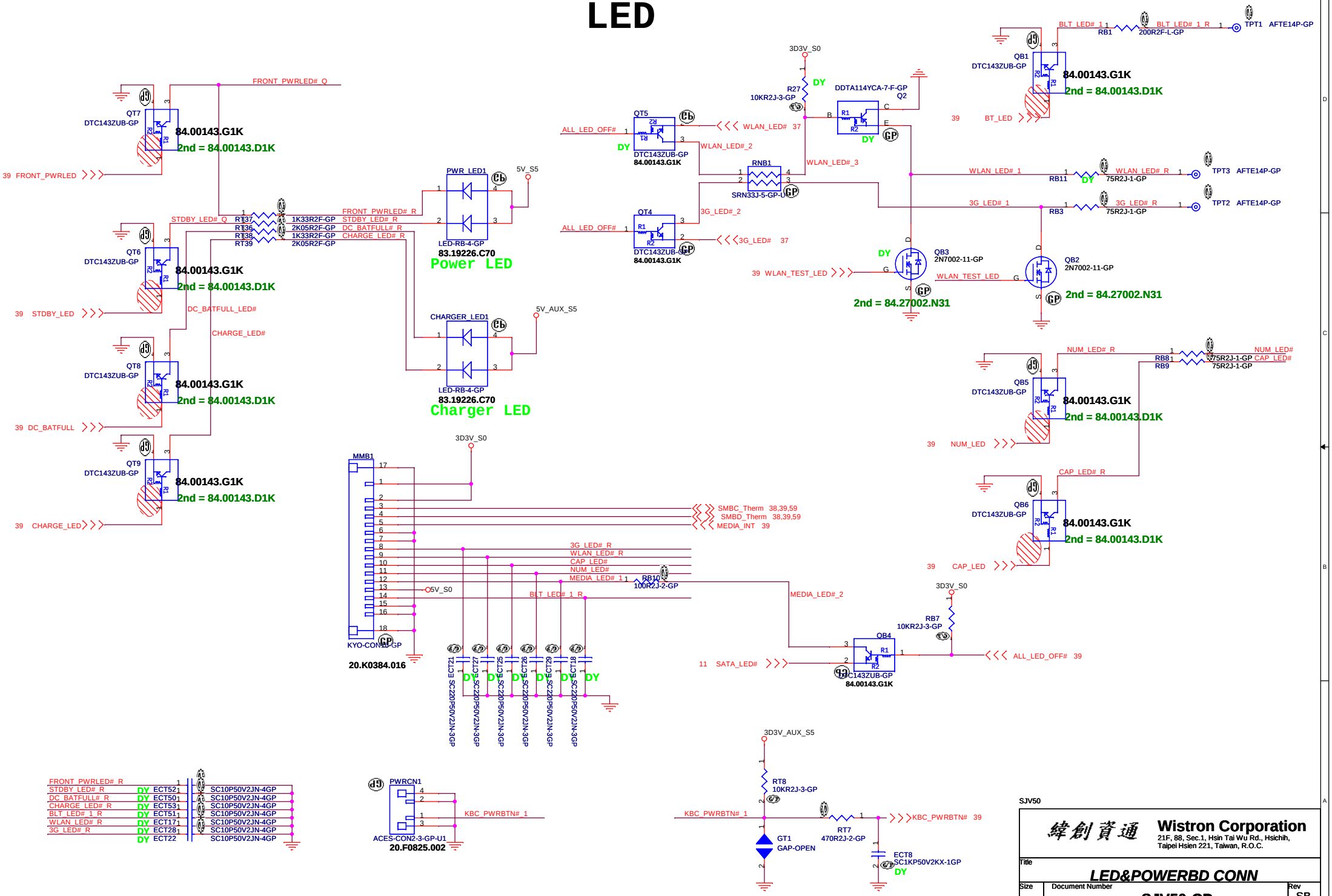




SJV50

| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: Touch PAD and FP | | |
| Size | Document Number: SJV50-CP | Rev: SB |
| Date: Wednesday, October 21, 2009 | Sheet 41 of 67 | |

# LED

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| | |
|---|---|
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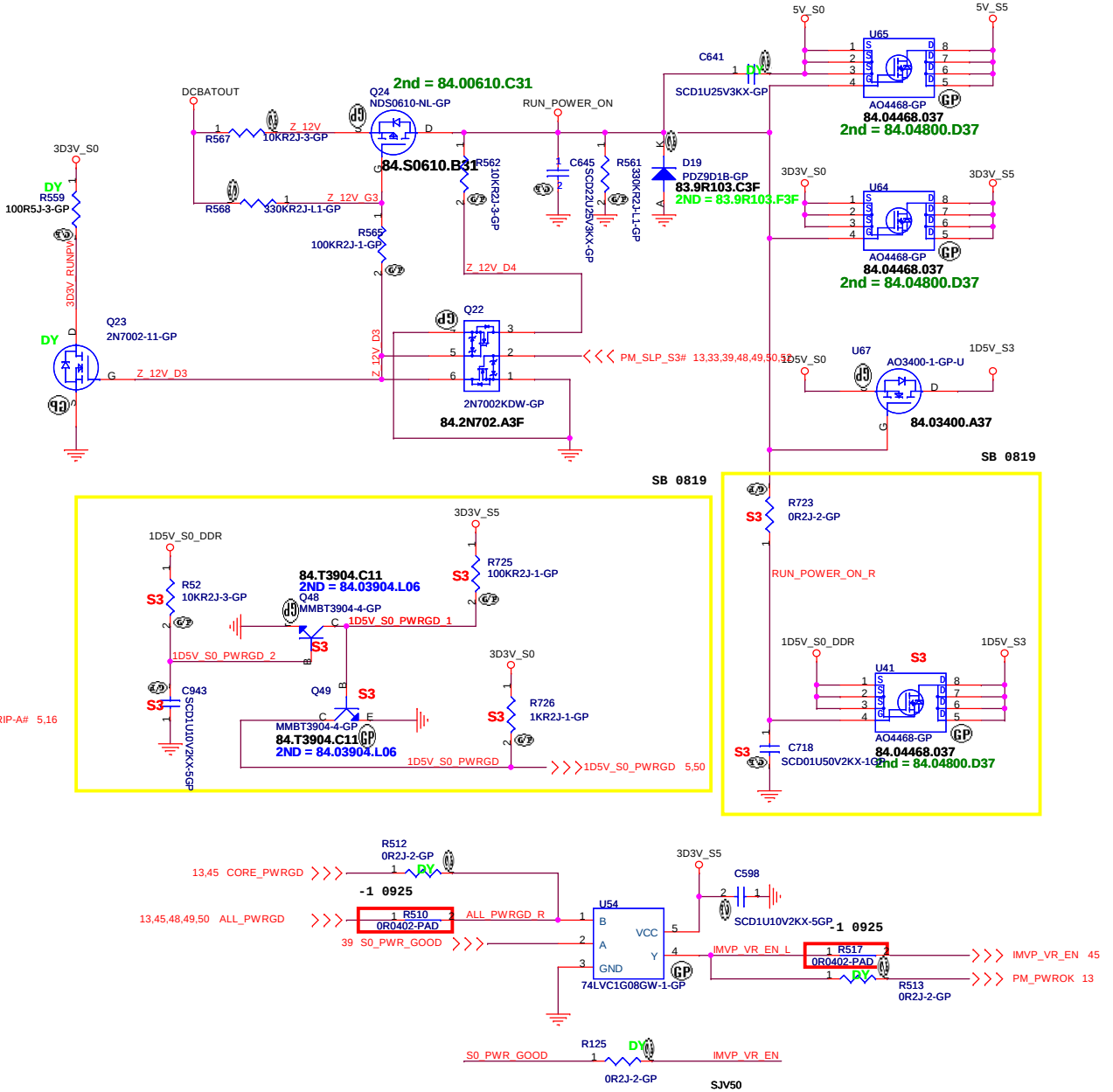
| Title | LED&POWERBD CONN |
| Size | Document Number: SJV50-CP |
| Rev | SB |
| Date: Wednesday, October 21, 2009 | Sheet 42 of 67 |

# Run Power

-1 1001

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Title: RUN POWER and 3D3V_AUX_S5

| Size | Document Number | Rev |
|---|---|---|
| | SJV50-CP | SB |

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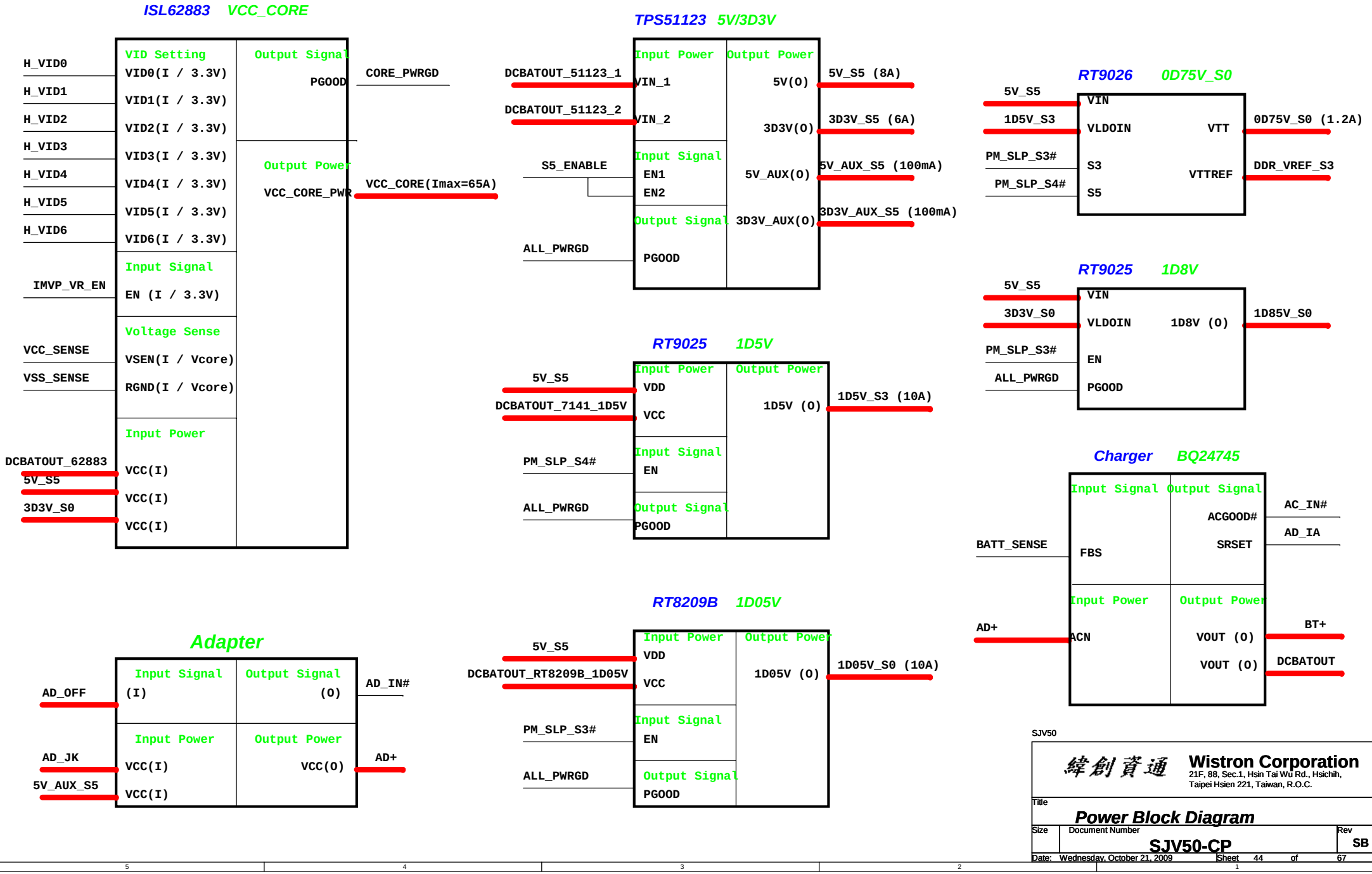


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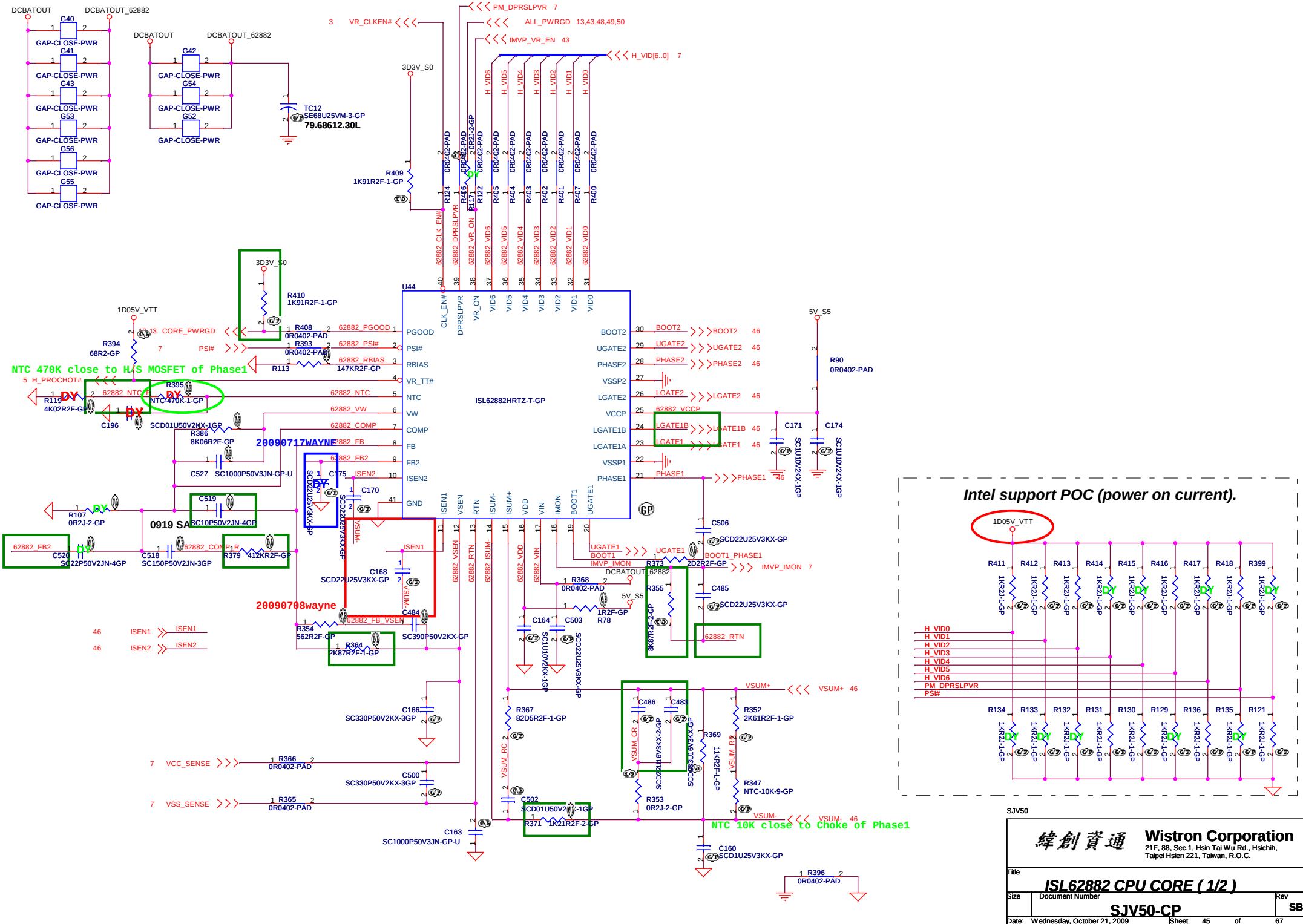
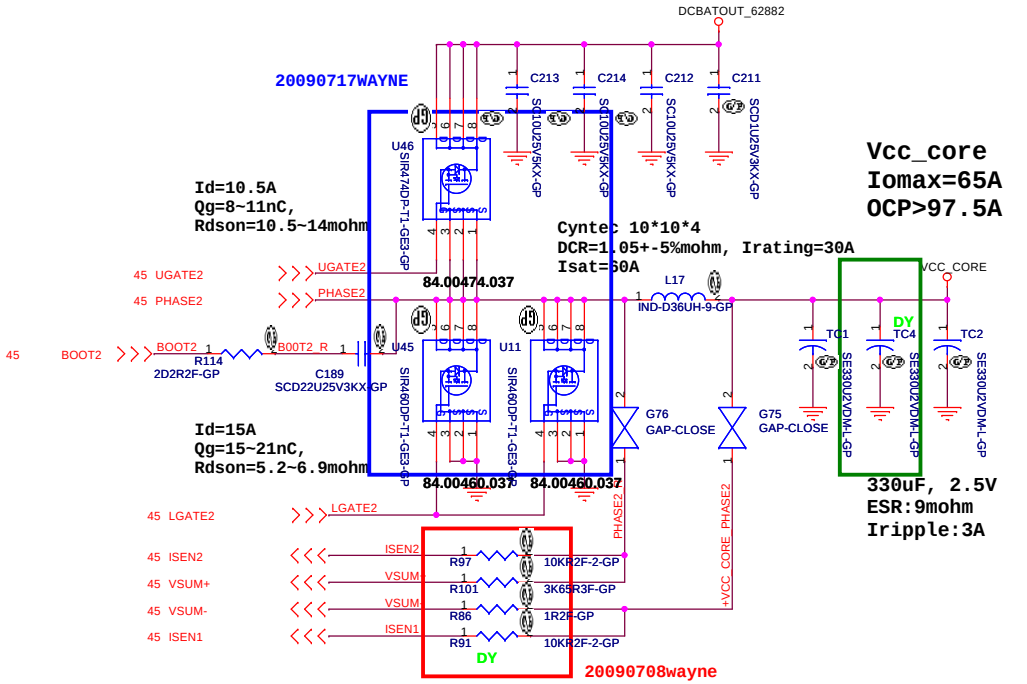
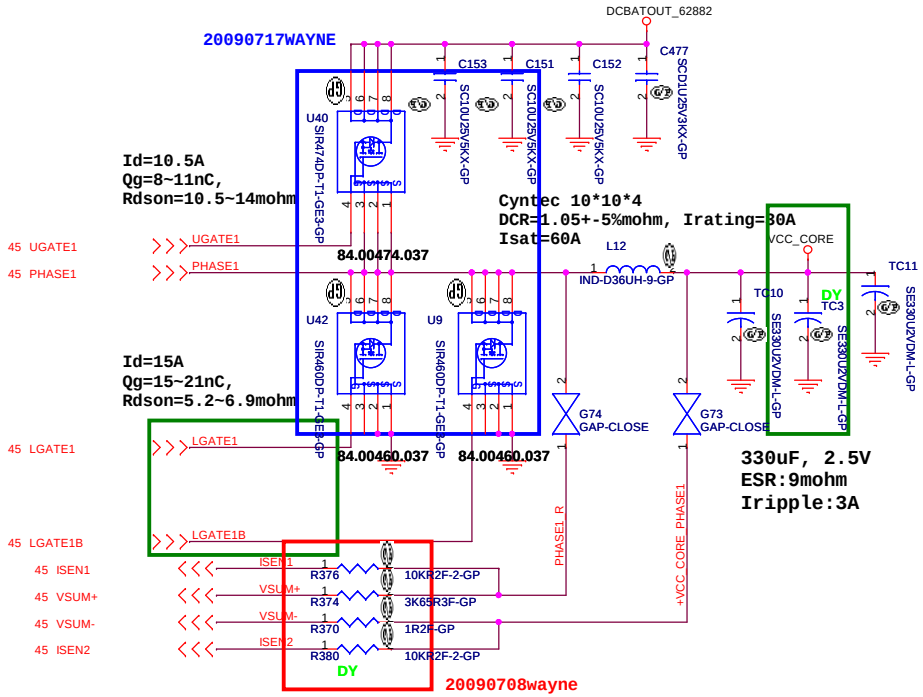
Title: **Power Block Diagram**

| Size | Document Number | Rev |
|---|---|---|
| | SJV50-CP | SB |

Date: Wednesday, October 21, 2009 Sheet 44 of 67


ISL62882HRTZ-T-GP
U44
NTC 470K close to H/S MOSFET of Phase1
NTC 10K close to Choke of Phase1
20090717WAYNE
20090708wayne
0919 SA
Intel support POC (power on current).
PM_DPRSLPVR 7
ALL_PWRGD 13,43,48,49,50
IMVP_VR_EN 43
H_VID[6..0] 7
VR_CLKEN# 3
3D3V_S0
1D05V_VTT
5V_S5
CORE_PWRGD 13
PSI# 7
H_PROCHOT# 5
VCC_SENSE 7
VSS_SENSE 7
IMVP_IMON 7
VSUM+ 46
VSUM- 46
ISEN1 46
ISEN2 46
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL62882 CPU CORE ( 1/2 )
SJV50-CP
Wednesday, October 21, 2009
Sheet 45 of 67



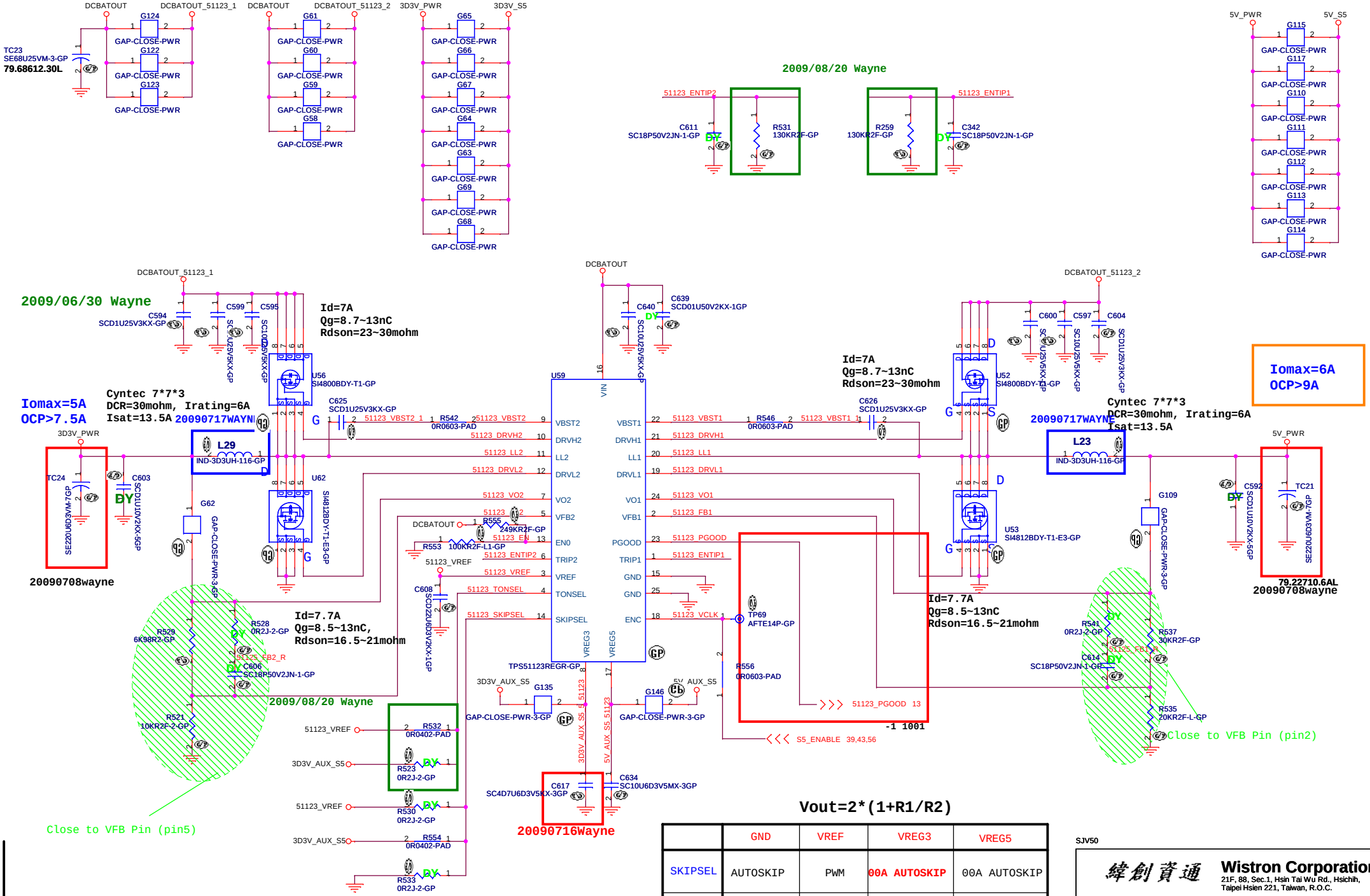

SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ISL62882 CPU CORE ( 1/2 )*

| Size | Document Number | Rev |
|---|---|---|
| | SJV50-CP | SB |

Date: Wednesday, October 21, 2009 Sheet 46 of 67




| | GND | VREF | VREG3 | VREG5 |
|---|---|---|---|---|
| SKIPSEL | AUTOSKIP | PWM | 00A AUTOSKIP | 00A AUTOSKIP |
| TONSEL | 200k/CH1<br>250k/CH2 | 245k/CH1<br>305k/CH2 | 300k/CH1<br>375k/CH2 | 365k/CH1<br>460k/CH2 |

SJV50

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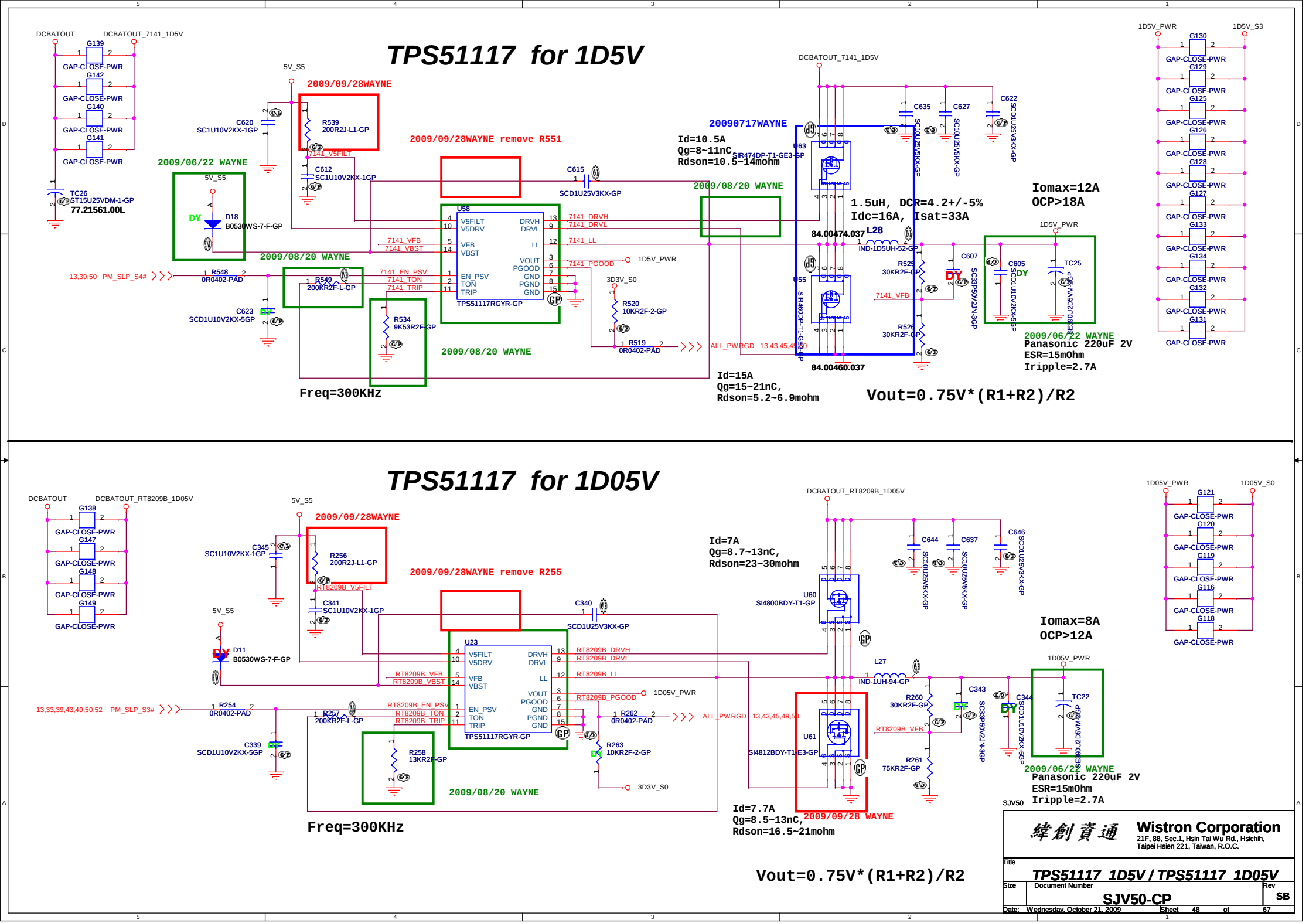
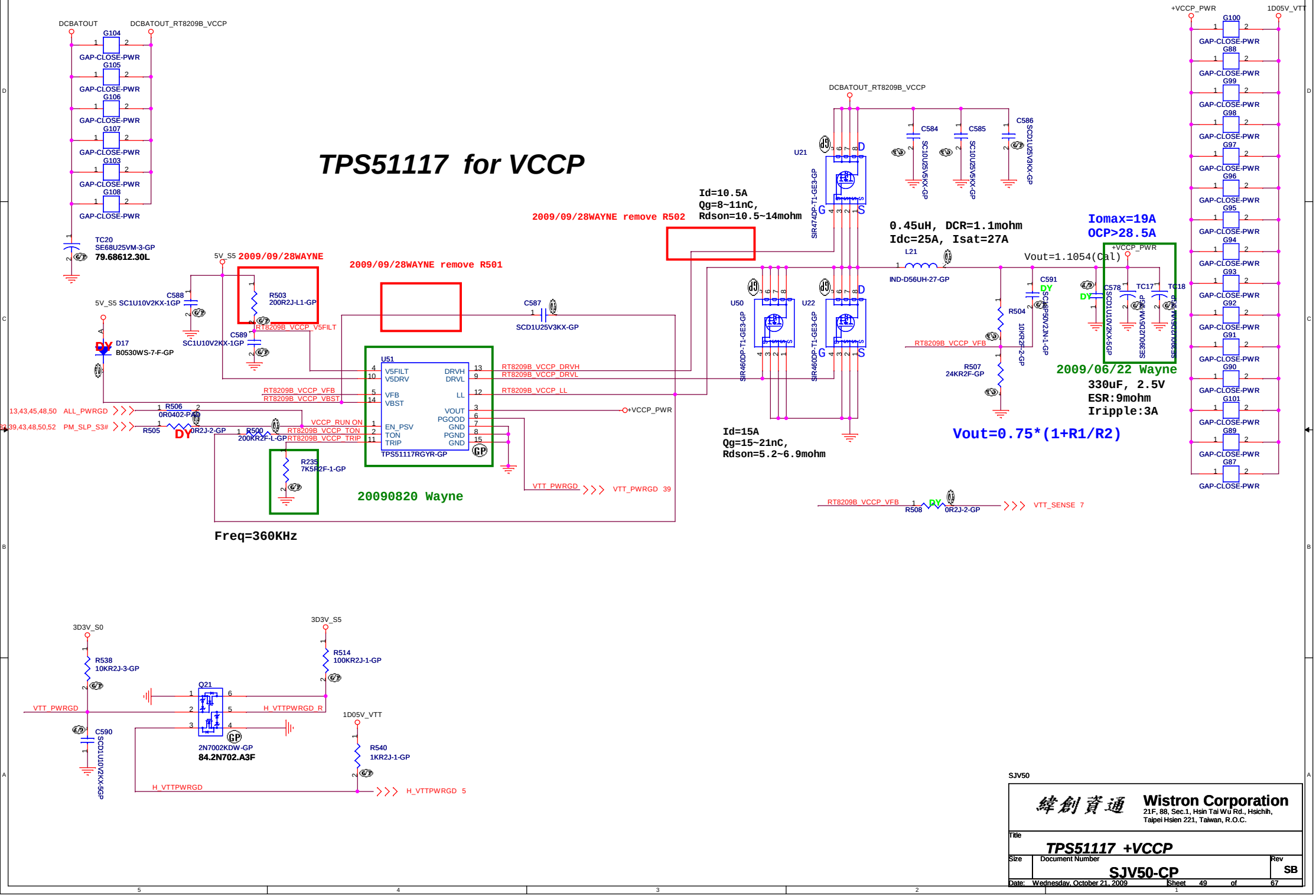
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51123 5V/3D3V

Size | Document Number: SJV50-CP | Rev: SB

Date: Wednesday, October 21, 2009 | Sheet 47 of 67


TPS51117 for 1D5V
DCBATOUT
DCBATOUT_7141_1D5V
5V_S5
2009/09/28WAYNE
2009/09/28WAYNE remove R551
2009/06/22 WAYNE
2009/08/20 WAYNE
20090717WAYNE
Id=10.5A
Qg=8~11nC
Rdson=10.5~14mohm
1.5uH, DCR=4.2+/-5%
Idc=16A, Isat=33A
Iomax=12A
OCP>18A
Panasonic 220uF 2V
ESR=15mOhm
Iripple=2.7A
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
Freq=300KHz
Vout=0.75V*(R1+R2)/R2
TPS51117RGYR-GP
1D5V_PWR
1D5V_S3
TPS51117 for 1D05V
DCBATOUT_RT8209B_1D05V
2009/09/28WAYNE remove R255
Id=7A
Qg=8.7~13nC,
Rdson=23~30mohm
Iomax=8A
OCP>12A
Id=7.7A
Qg=8.5~13nC,
Rdson=16.5~21mohm
2009/09/28 WAYNE
1D05V_PWR
1D05V_S0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51117_1D5V / TPS51117_1D05V
SJV50-CP
Wednesday, October 21, 2009




SJV50

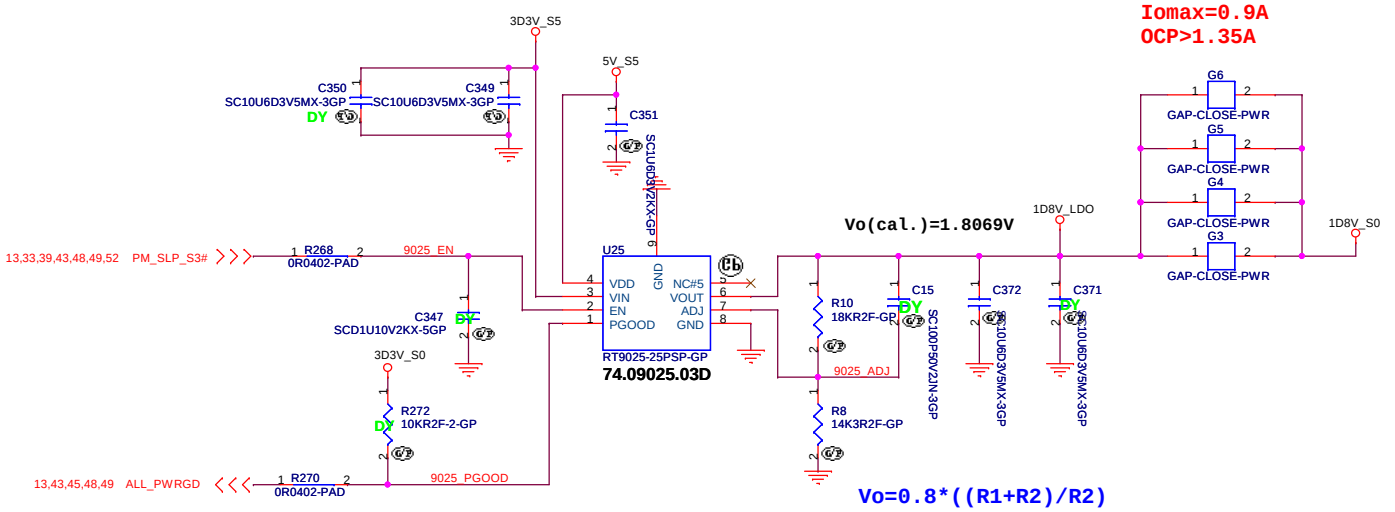
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51117 +VCCP***

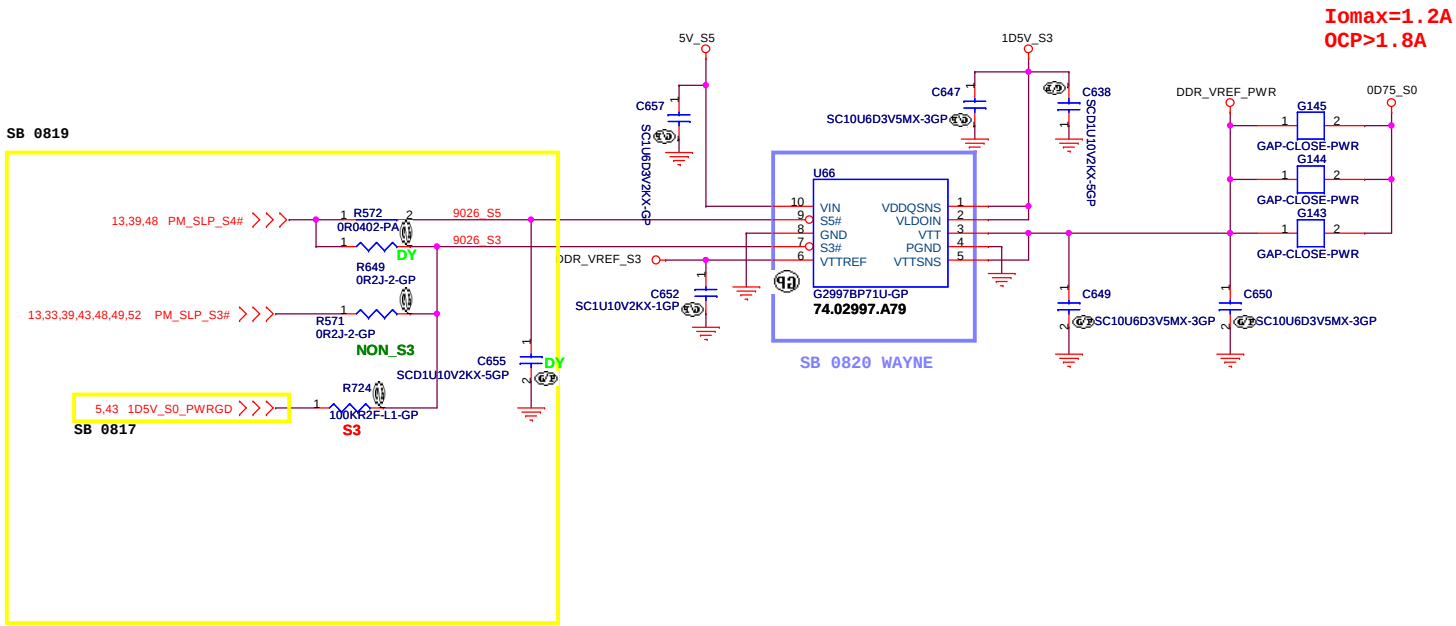
Size | Document Number: **SJV50-CP** | Rev: **SB**

Date: Wednesday, October 21, 2009 | Sheet 49 of 67

# RT9025 for 1D8V_S0




# G2997 for 0D75V_S3



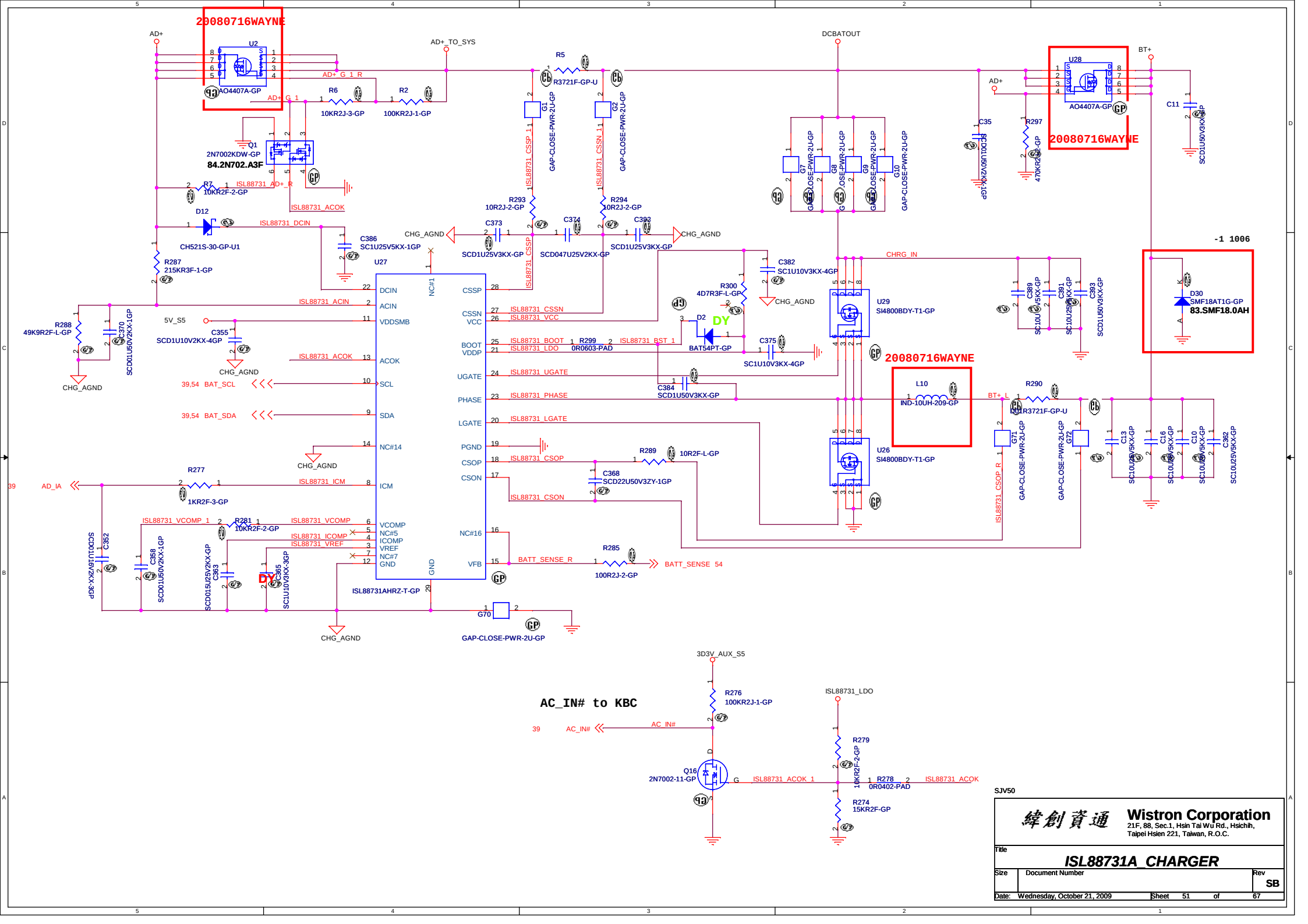

SJV50

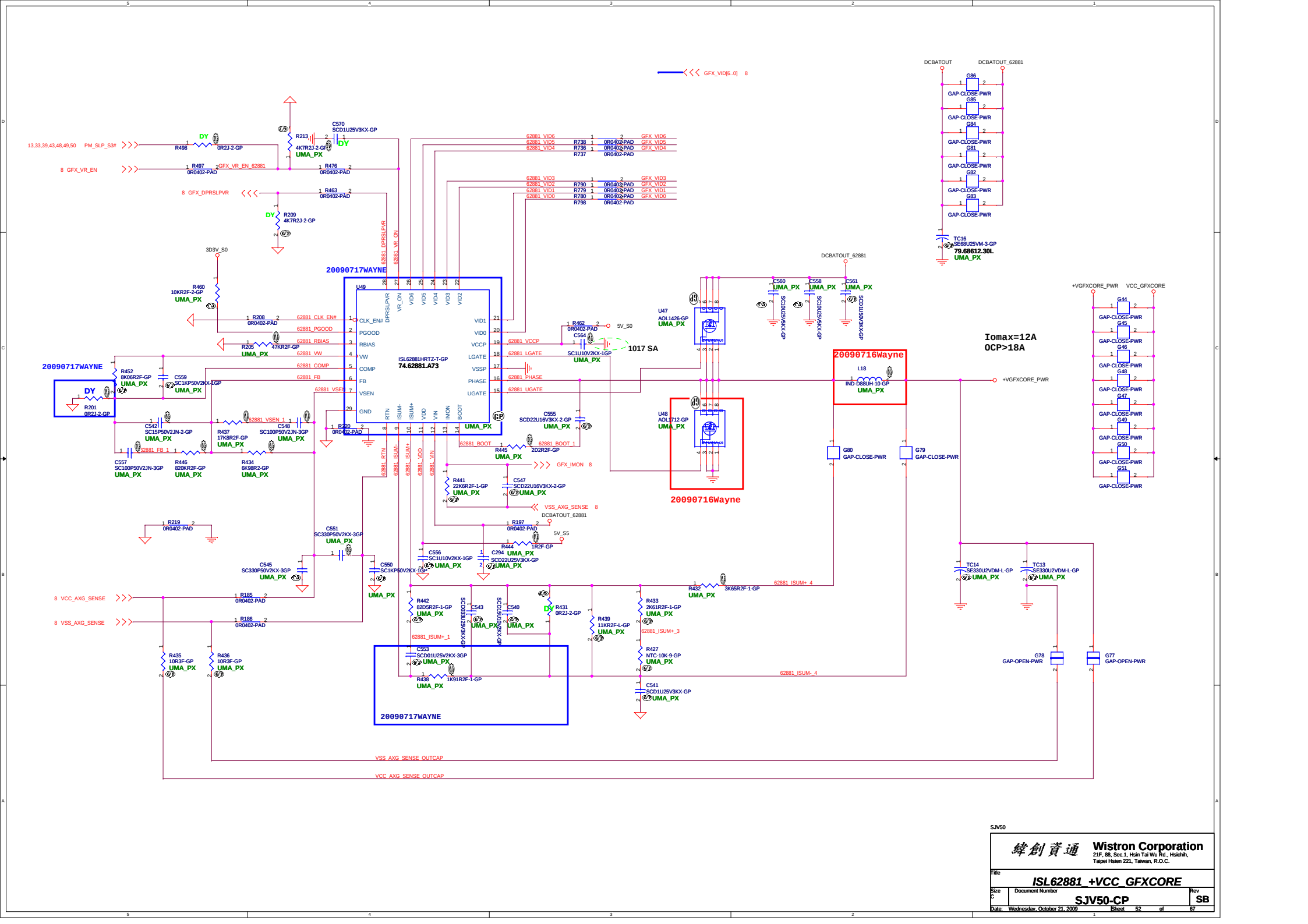
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

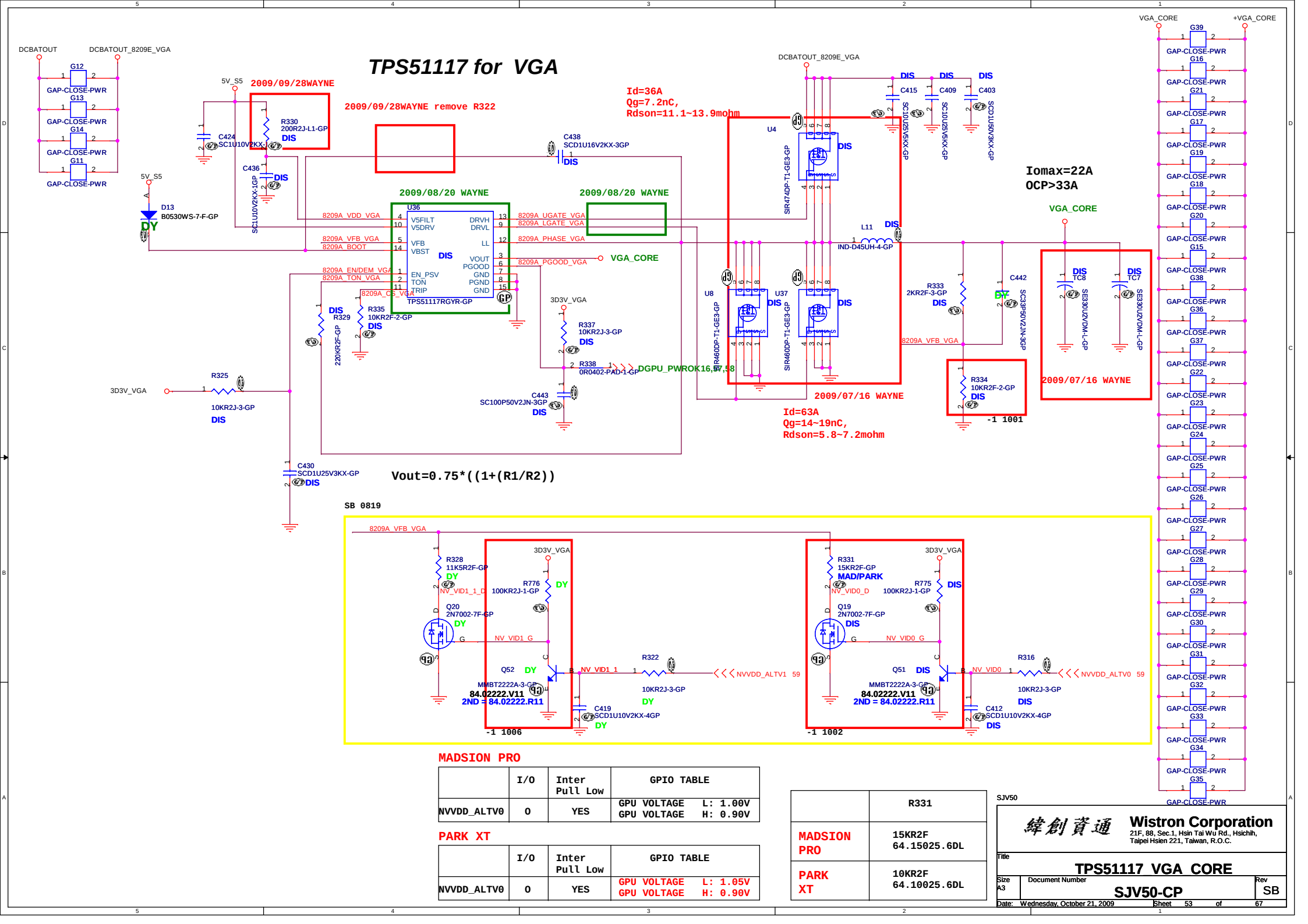
Title: RT9025_1D8V/G2997_0D75

Size | Document Number: SJV50-CP | Rev: SB

Date: Wednesday, October 21, 2009 | Sheet 50 of 67


20080716WAYNE
U2
AO4407A-GP
AD+
AD+_TO_SYS
AD+_G_1_R
AD+_G_1
R6
10KR2J-3-GP
R2
100KR2J-1-GP
R5
R3721F-GP-U
Q1
2N7002KDW-GP
84.2N702.A3F
R7
10KR2F-2-GP
ISL88731_AD+_R
ISL88731_ACOK
D12
CH521S-30-GP-U1
ISL88731_DCIN
C386
SC1U25V5KX-1GP
R287
215KR3F-1-GP
U27
ISL88731AHRZ-T-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
R288
49K9R2F-L-GP
C370
SCD01U50V2KX-1GP
CHG_AGND
5V_S5
C355
SCD1U10V2KX-4GP
39,54 BAT_SCL
39,54 BAT_SDA
R277
1KR2F-3-GP
39 AD_IA
ISL88731_VCOMP_1
R281
10KR2F-2-GP
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
C352
C358
SCD01U50V2KX-1GP
C363
SCD015U25V2KX-GP
C365
SC1U10V3KX-3GP
DY
ISL88731_ACIN
ISL88731_ICM
ISL88731_CSSP_1
ISL88731_CSSN_1
ISL88731_CSSP
ISL88731_CSSN
ISL88731_VCC
ISL88731_BOOT
ISL88731_LDO
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
ISL88731_CSOP
ISL88731_CSON
ISL88731_BST_1
R293
10R2J-2-GP
R294
10R2J-2-GP
C373
SCD1U25V3KX-GP
C374
SCD047U25V2KX-GP
C393
SCD1U25V3KX-GP
CHG_AGND
GAP-CLOSE-PWR-2U-GP
G1
G2
G70
R299
0R0603-PAD
D2
BAT54PT-GP
DY
C375
SC1U10V3KX-4GP
C384
SCD1U50V3KX-GP
R300
4D7R3F-L-GP
C382
SC1U10V3KX-4GP
R289
10R2F-L-GP
C368
SCD22U50V3ZY-1GP
R285
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 54
DCBATOUT
U28
AO4407A-GP
20080716WAYNE
C35
SCD1U50V2KX-1GP
R297
470KR2J-GP
C11
SCD1U50V3KX-GP
BT+
CHRG_IN
U29
SI4800BDY-T1-GP
U26
SI4800BDY-T1-GP
20080716WAYNE
L10
IND-10UH-209-GP
BT+_L
R290
0R3721F-GP-U
C389
SC10U25V5KX-GP
C391
SC10U25V5KX-GP
C393
SCD1U50V3KX-GP
G71
G72
GAP-CLOSE-PWR-2U-GP
ISL88731_CSOP_R
C13
C16
C10
C362
SC10U25V5KX-GP
-1 1006
D30
SMF18AT1G-GP
83.SMF18.0AH
AC_IN# to KBC
3D3V_AUX_S5
R276
100KR2J-1-GP
39 AC_IN#
Q16
2N7002-11-GP
ISL88731_ACOK_1
R279
10KR2F-2-GP
R278
0R0402-PAD
ISL88731_ACOK
R274
15KR2F-GP
ISL88731_LDO
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A_CHARGER
Size
Document Number
Rev
SB
Date: Wednesday, October 21, 2009
Sheet 51 of 67


GFX_VID[6..0] 8
DCBATOUT
DCBATOUT_62881
GAP-CLOSE-PWR
TC16 SFE68U25VM-3-GP 79.68612.30L UMA_PX
13,33,39,43,48,49,50 PM_SLP_S3#
8 GFX_VR_EN
8 GFX_DPRSLPVR
3D3V_S0
20090717WAYNE
U49
ISL62881HRTZ-T-GP
74.62881.A73
UMA_PX
62881_VID6
62881_VID5
62881_VID4
62881_VID3
62881_VID2
62881_VID1
62881_VID0
GFX_VID6
GFX_VID5
GFX_VID4
GFX_VID3
GFX_VID2
GFX_VID1
GFX_VID0
62881_DPRSLPVR
62881_VR_ON
62881_CLK_EN#
62881_PGOOD
62881_RBIAS
62881_VW
62881_COMP
62881_FB
62881_VSEN
62881_VCCP
62881_LGATE
62881_PHASE
62881_UGATE
62881_BOOT
62881_BOOT_1
5V_S0
1017 SA
U47 AOL1426-GP
U48 AOL1712-GP
20090716Wayne
L18 IND-D88UH-10-GP
+VGFXCORE_PWR
Iomax=12A
OCP>18A
GFX_IMON 8
VSS_AXG_SENSE 8
62881_ISUM+_4
62881_ISUM-_4
62881_ISUM+_1
62881_ISUM+_3
8 VCC_AXG_SENSE
8 VSS_AXG_SENSE
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
5V_S5
+VGFXCORE_PWR
VCC_GFXCORE
GAP-OPEN-PWR
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62881_+VCC_GFXCORE
Size C
Document Number
SJV50-CP
Rev SB
Date: Wednesday, October 21, 2009
Sheet 52 of 67




## MADSION PRO

| | I/O | Inter Pull Low | GPIO TABLE |
|---|---|---|---|
| NVVDD_ALTV0 | O | YES | GPU VOLTAGE L: 1.00V<br>GPU VOLTAGE H: 0.90V |

## PARK XT

| | I/O | Inter Pull Low | GPIO TABLE |
|---|---|---|---|
| NVVDD_ALTV0 | O | YES | GPU VOLTAGE L: 1.05V<br>GPU VOLTAGE H: 0.90V |

| | R331 |
|---|---|
| MADSION PRO | 15KR2F<br>64.15025.6DL |
| PARK XT | 10KR2F<br>64.10025.6DL |

SJV50

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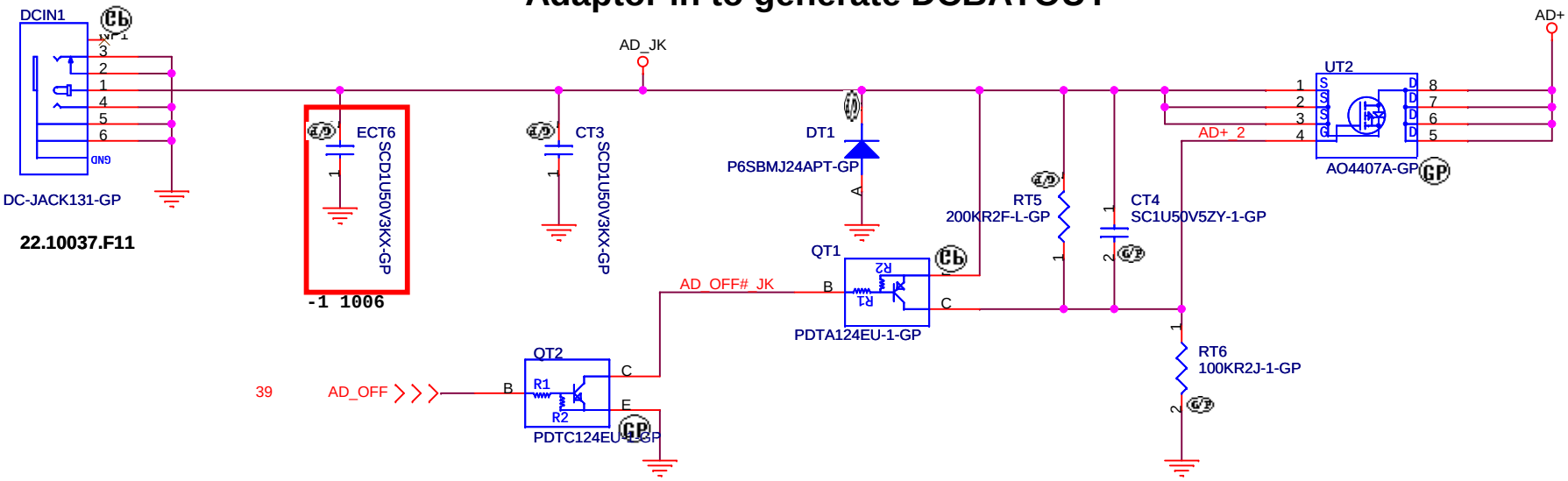
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51117 VGA CORE

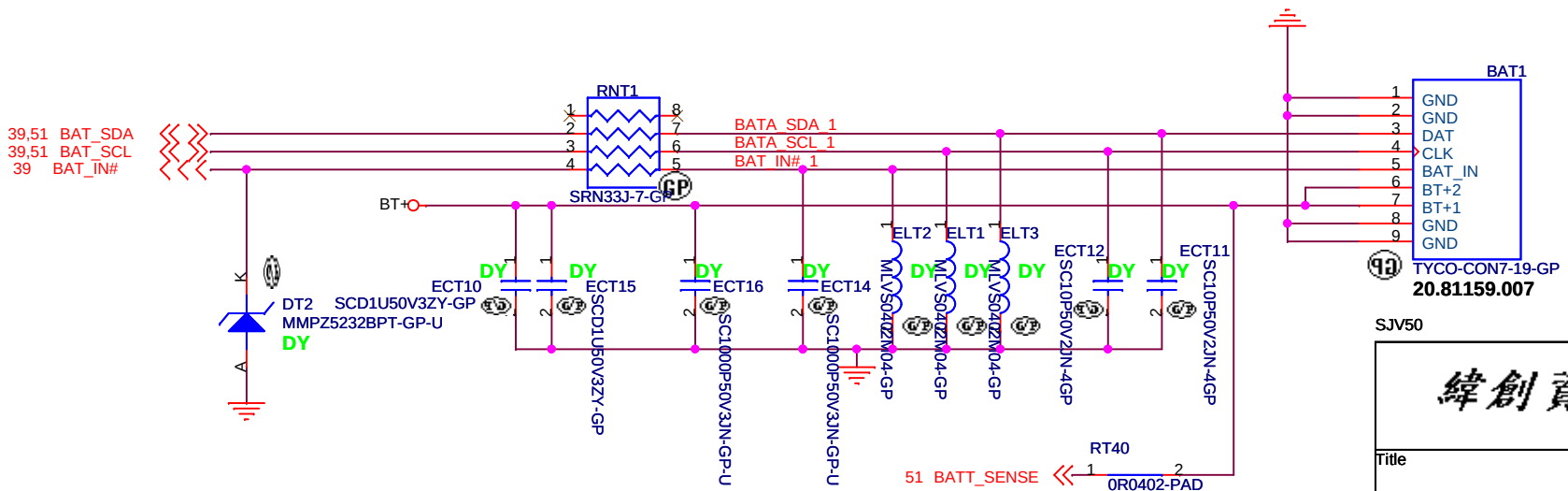
Size: A3 | Document Number: SJV50-CP | Rev: SB

Date: Wednesday, October 21, 2009 | Sheet 53 of 67

# Adaptor in to generate DCBATOUT




# BATTERY CONNECTOR




SJV50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Taipei Hsien 221, Taiwan, R.O.C.


Title: AD/BATT CONN

| Size | Document Number | Rev |
|---|---|---|
| | SJV50-CP | SB |

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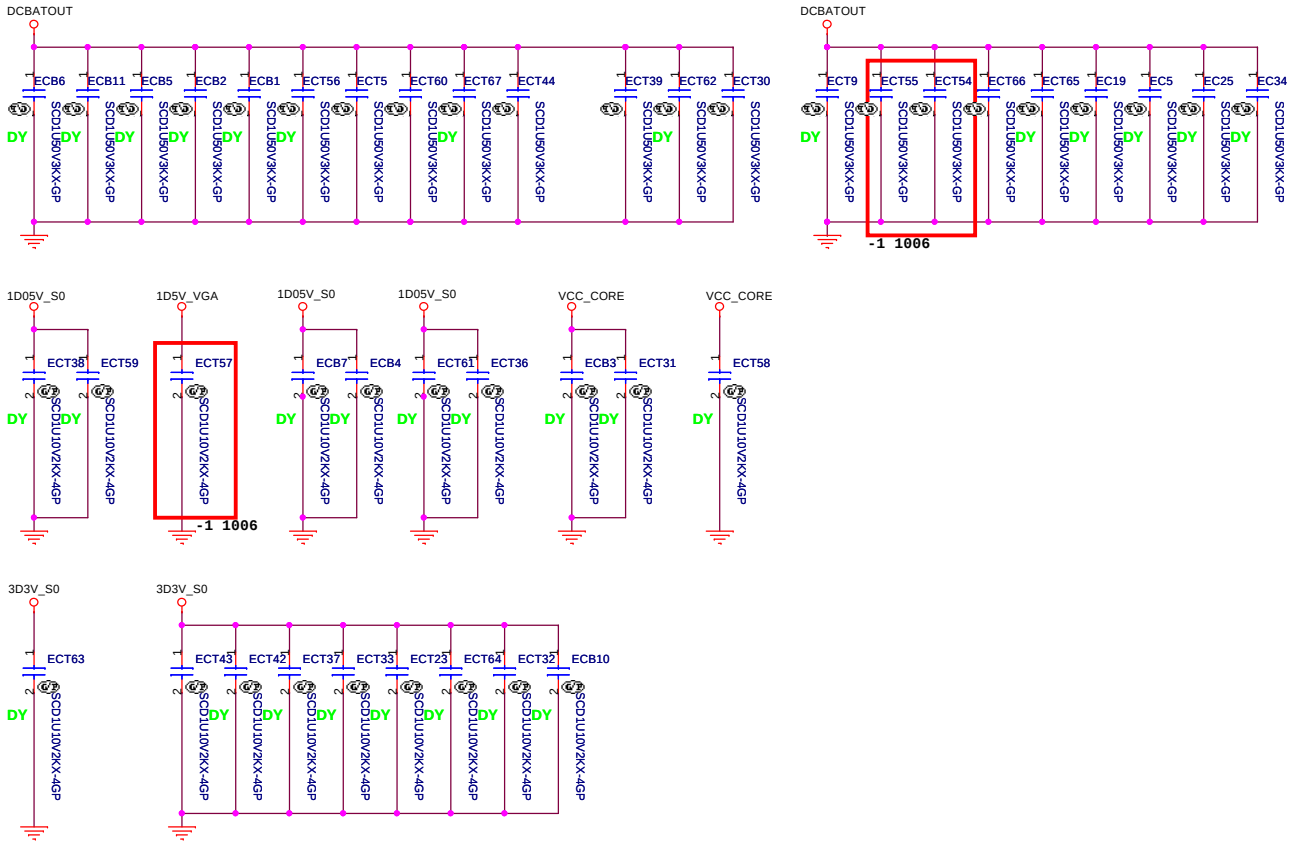


## CPU

H1 H2 H3

ZZ.00PAD.801 HOLE2542-GP

34.42Y01.021 34.42Y01.021 34.42Y01.021

## NB

H4

ZZ.00PAD.801 HOLE2542-GP

34.42Y01.021

## VGA

H5 H6

ZZ.00PAD.801 HOLE2542-GP

34.42Y01.021 34.42Y01.021

## MDC

H7 HOLE H8 HOLE

ZZ.0HOLE.XXX

34.42Y01.021 34.42Y01.021

## MINICARD

HB1 HOLE H20 HOLE

34.4B804.001 DY

H14

ZZ.00PAD.801 HOLE2542-GP

34.42Y01.021

GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9

HOLE355X355R111-S1-GP HOLE315X315R91-S1-GP

GNDT1 HOLE

ZZ.0HOLE.XXX

SPRING_GND3 SPRING-58-GP

34.4B312.002

SJV50

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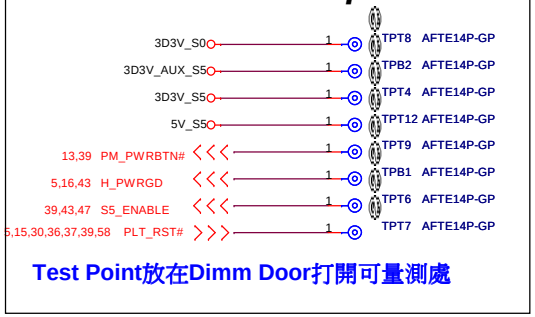
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size | Document Number: SJV50-CP | Rev: SB

Date: Wednesday, October 21, 2009 | Sheet 55 of 67

# Check test point




**Test Point放在Dimm Door打開可量測處**

SJV50

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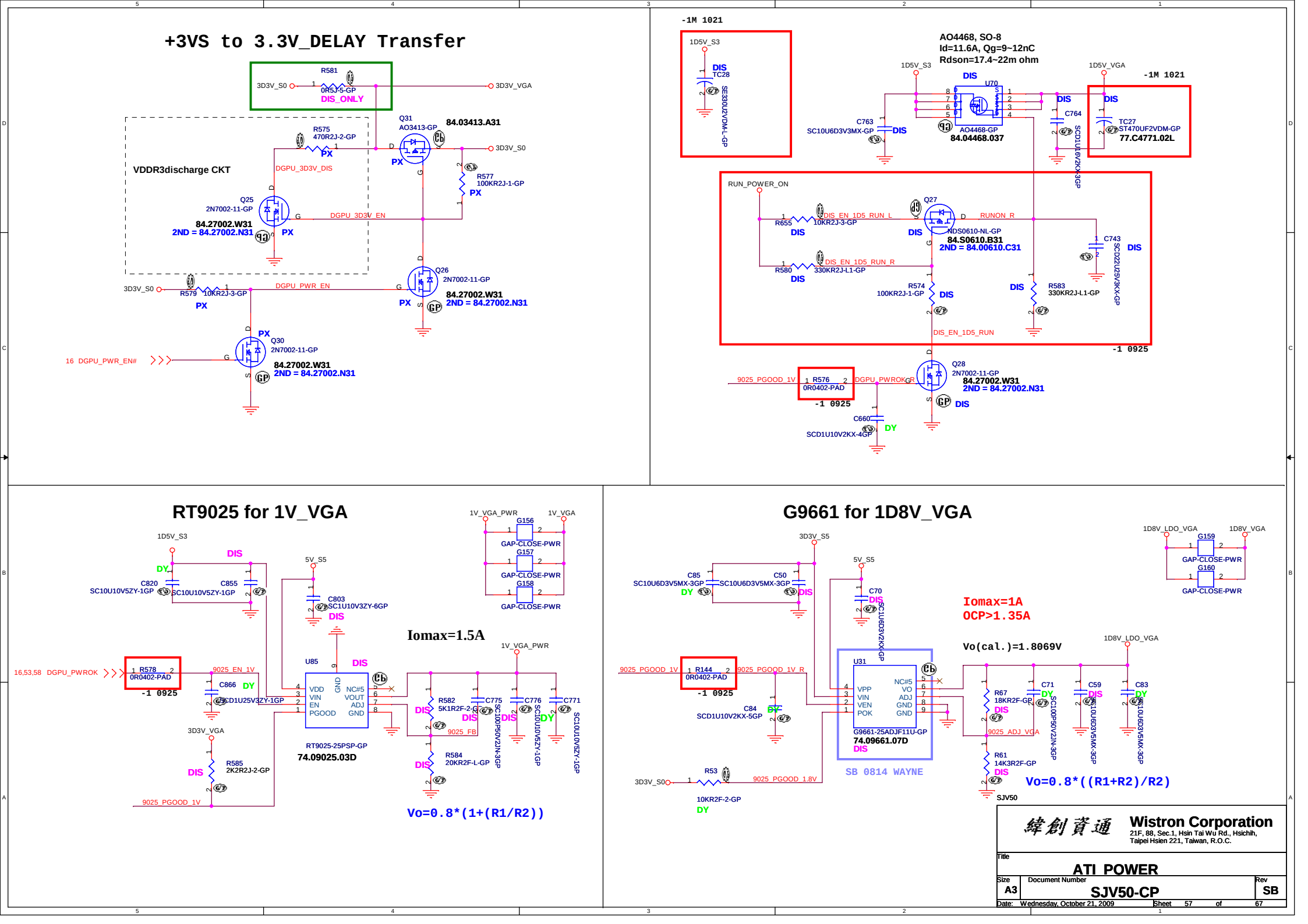
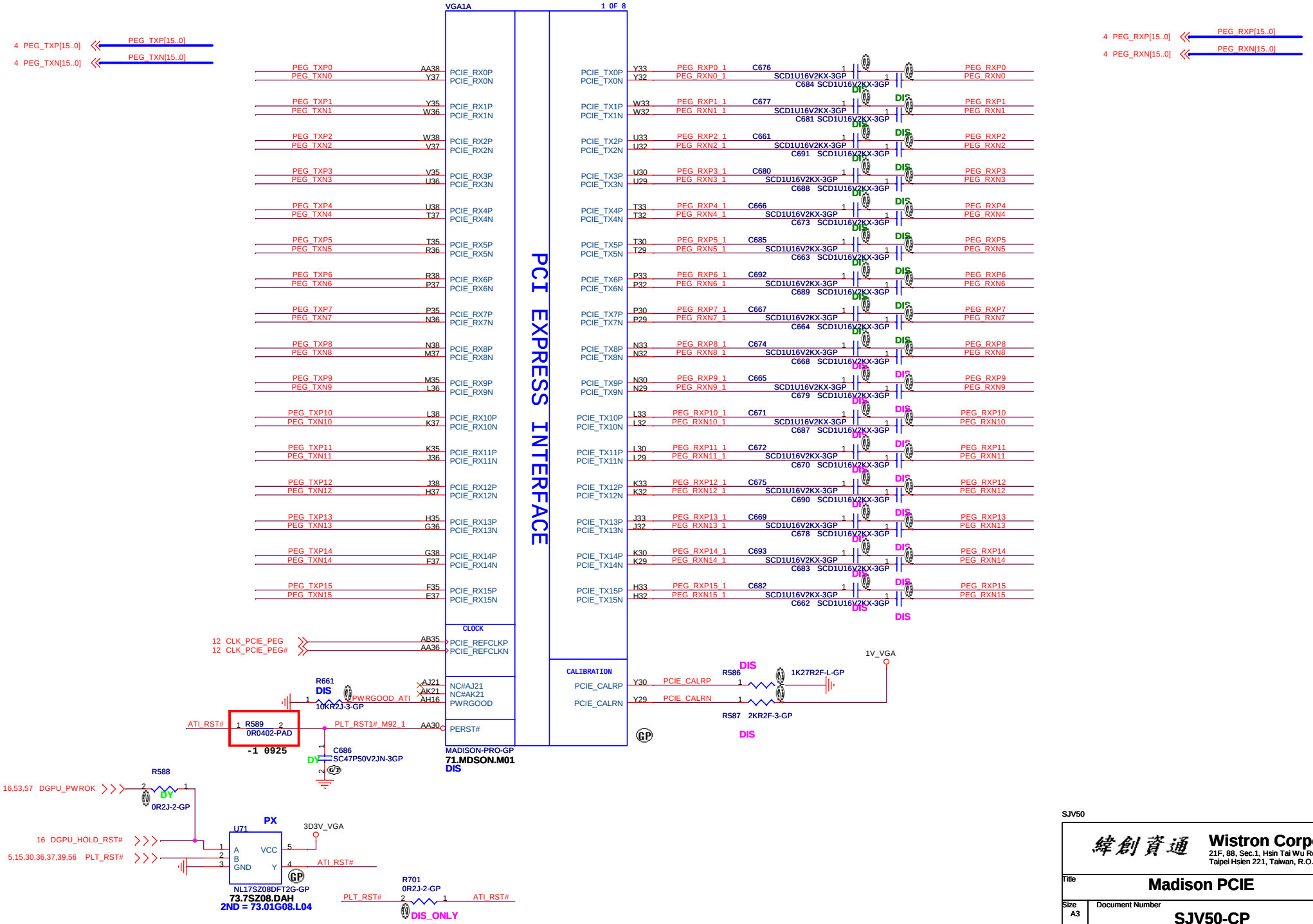
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title: ***AFTE_TP*** | | |
| Size: A3 | Document Number: **SJV50-CP** | Rev: **SB** |
| Date: Wednesday, October 21, 2009 | Sheet 56 of 67 | |


+3VS to 3.3V_DELAY Transfer
R581
3D3V_S0
0R5J-5-GP
DIS_ONLY
3D3V_VGA
VDDR3discharge CKT
Q31
AO3413-GP
84.03413.A31
R575
470R2J-2-GP
PX
DGPU_3D3V_DIS
R577
100KR2J-1-GP
Q25
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
DGPU_3D3V_EN
R579
10KR2J-3-GP
DGPU_PWR_EN
Q26
2N7002-11-GP
Q30
16 DGPU_PWR_EN#
-1M 1021
1D5V_S3
DIS
TC28
SE330U2VDM-L-GP
AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm
U70
AO4468-GP
84.04468.037
C763
SC10U6D3V3MX-GP
C764
SCD1U16V2KX-3GP
1D5V_VGA
TC27
ST470UF2VDM-GP
77.C4771.02L
RUN_POWER_ON
R655
10KR2J-3-GP
DIS_EN_1D5_RUN_L
Q27
NDS0610-NL-GP
84.S0610.B31
2ND = 84.00610.C31
RUNON_R
C743
SCD22U25V3KX-GP
R580
330KR2J-L1-GP
DIS_EN_1D5_RUN_R
R574
100KR2J-1-GP
R583
330KR2J-L1-GP
DIS_EN_1D5_RUN
-1 0925
9025_PGOOD_1V
R576
0R0402-PAD
DGPU_PWROKR
Q28
2N7002-11-GP
C660
SCD1U10V2KX-4GP
RT9025 for 1V_VGA
1D5V_S3
C820
SC10U10V5ZY-1GP
C855
SC10U10V5ZY-1GP
5V_S5
C803
SC1U10V3ZY-6GP
1V_VGA_PWR
1V_VGA
G156
GAP-CLOSE-PWR
G157
G158
Iomax=1.5A
16,53,58 DGPU_PWROK
R578
0R0402-PAD
9025_EN_1V
C866
SCD1U25V3ZY-1GP
U85
VDD
VIN
EN
PGOOD
GND
NC#5
VOUT
ADJ
RT9025-25PSP-GP
74.09025.03D
R582
5K1R2F-2-GP
C775
C776
C771
SC100P50V2JN-3GP
SC10U10V5ZY-1GP
9025_FB
R584
20KR2F-L-GP
3D3V_VGA
R585
2K2R2J-2-GP
9025_PGOOD_1V
Vo=0.8*(1+(R1/R2))
G9661 for 1D8V_VGA
3D3V_S5
C85
SC10U6D3V5MX-3GP
C50
SC10U6D3V5MX-3GP
C70
SC1U6D3V2KX-GP
Iomax=1A
OCP>1.35A
Vo(cal.)=1.8069V
1D8V_LDO_VGA
1D8V_VGA
G159
G160
R144
0R0402-PAD
9025_PGOOD_1V_R
U31
VPP
VIN
VEN
POK
NC#5
VO
ADJ
GND
G9661-25ADJF11U-GP
74.09661.07D
C84
SCD1U10V2KX-5GP
SB 0814 WAYNE
R53
10KR2F-2-GP
9025_PGOOD_1.8V
R67
18KR2F-GP
C71
C59
C83
SC10U6D3V5MX-3GP
9025_ADJ_VGA
R61
14K3R2F-GP
Vo=0.8*((R1+R2)/R2)
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI POWER
Size
A3
Document Number
SJV50-CP
Rev
SB
Date: Wednesday, October 21, 2009
Sheet 57 of 67




SJV50

| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | **Madison PCIE** | |
| Size A3 | Document Number **SJV50-CP** | Rev **SB** |
| Date: Wednesday, October 21, 2009 | Sheet 58 of 67 | |

Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)

It's strap for GDDR3-136ball
Need to Clarify

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

For Thermal sensor

SB 0811

SB 0814

SB 0817

SB 0819

SC 0902

-1 0930

-1 0929

-1 0925

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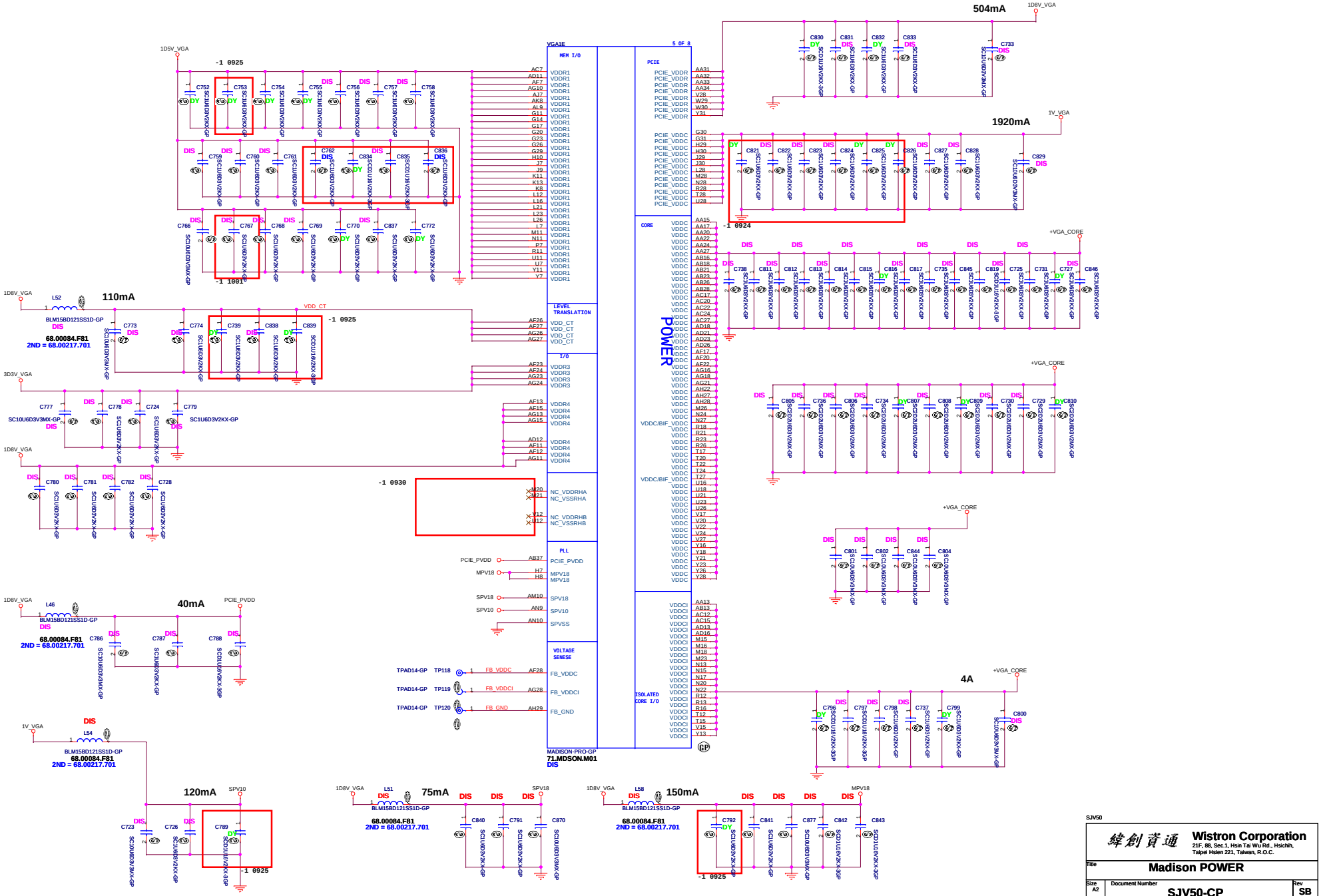
Title: Madison IO

Size: A2 | Document Number: SJV50-CP | Rev: SB

Date: Wednesday, October 21, 2009 | Sheet 59 of 67




SJV50

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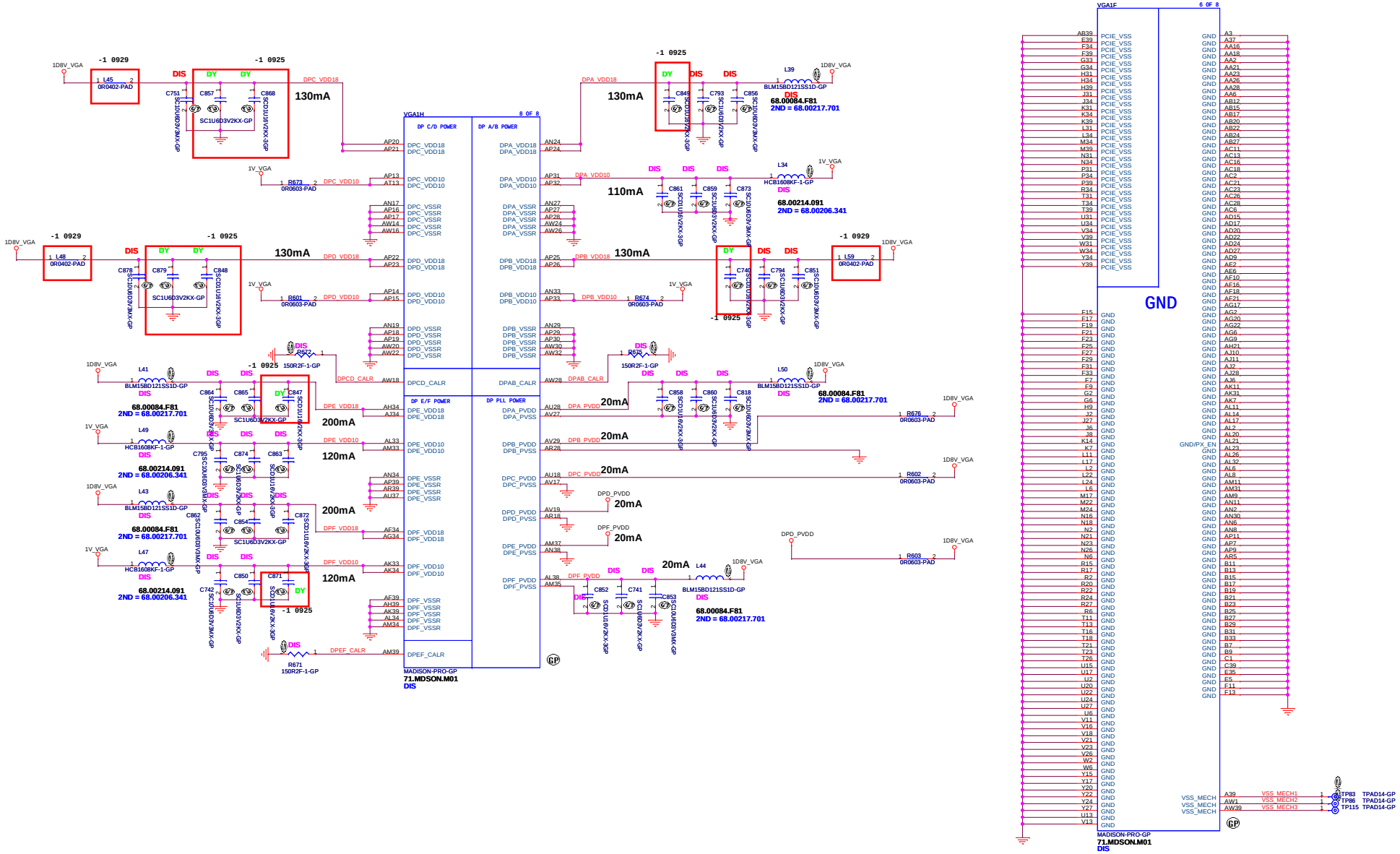
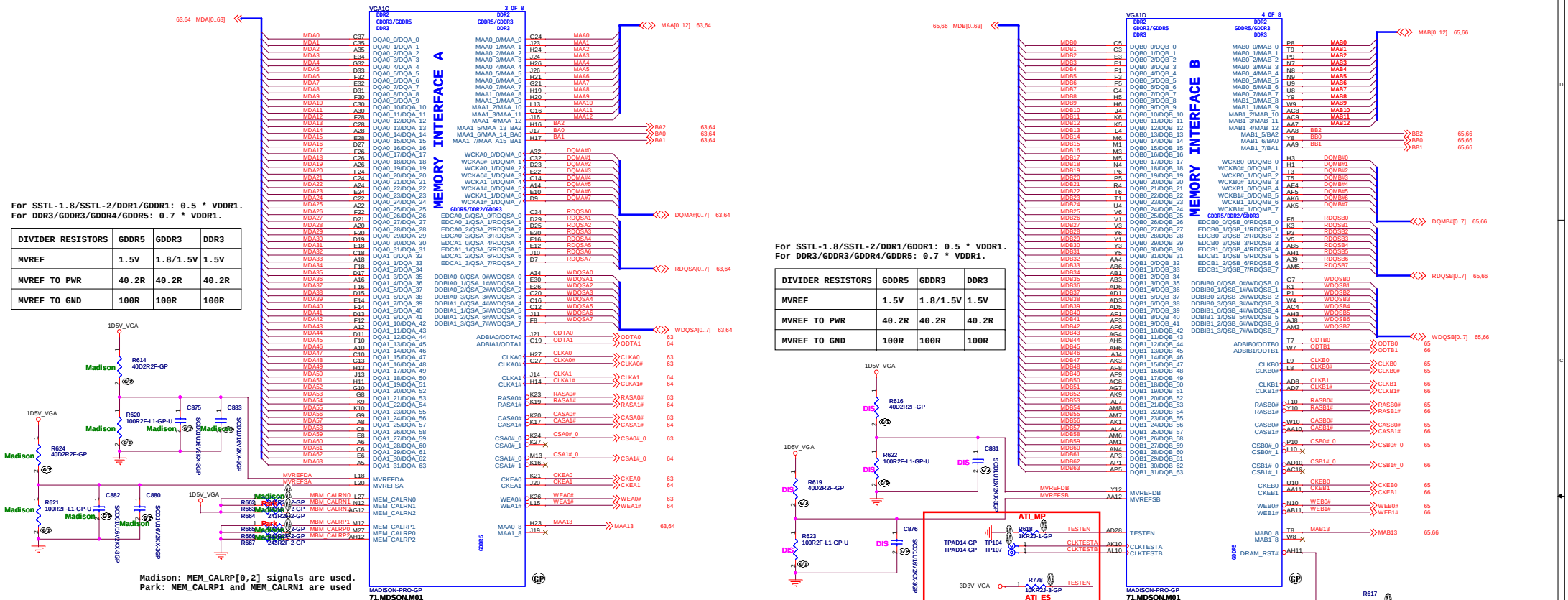
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Madison POWER**

| Size | Document Number | Rev |
|---|---|---|
| A2 | SJV50-CP | SB |

Date: Wednesday, October 21, 2009 Sheet 60 of 67


VGA1H
8 OF 8
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
MADISON-PRO-GP
71.MDSON.M01
DIS
130mA
110mA
200mA
120mA
20mA
68.00084.F81
2ND = 68.00217.701
68.00214.091
2ND = 68.00206.341
SC1U6D3V2KX-GP
150R2F-1-GP
0R0402-PAD
0R0603-PAD
HCB1608KF-1-GP
BLM15BD121SS1D-GP
VGA1F
6 OF 8
GND
PCIE_VSS
VSS_MECH
MADISON-PRO-GP
71.MDSON.M01
DIS
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DP POWER_GND
Size A2
Document Number
SJV50-CP
Rev SB
Date: Wednesday, October 21, 2009
Sheet 61 of 67




| STRAPS | PIN | DESCRIPTION | RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE |
|---|---|---|---|
| TX_PWRS_ENB (Internal PD) | GPIO0 | PCIE FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing | X |
| TX_DEEMPH_EN (Internal PD) | GPIO1 | Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled | X |
| RESERVED | GPIO8 | RESERVED | 0 |
| BIF_VGA_DIS | GPIO9 | VGA ENABLED | 0 |
| RESERVED | GPIO21 | RESERVED | 0 |
| BIOS_ROM_EN | GPIO22_ROMCSB | ENABLE EXTERNAL BIOS ROM | 0 |
| VIP_DEVICE_STRAP_ENA (Internal PD) | GPIO[13,12,11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size | X X X |
| RSVD | V2SYNC | | 0 |
| RSVD | H2SYNC | | 0 |
| AUD[1] AUD[0] (Internal PD) | VGA_HSYNC VGA_VSYNC | AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI ( if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI | X X |

## AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

| If BIOS_ROM_EN (GPIO22) = 0 | | If BIOS_ROM_EN (GPIO22) = 1 | | |
|---|---|---|---|---|
| Size of the primary memory apertures | GPIO[13,12,11] | Manufacturer | Part Number | GPIO[13,12,11] |
| V 128MB | x000 | ST Microelectronics | M25P05A | 0100 |
| 256MB | x001 | | M25P10A | 0101 |
| 64MB | x010 | | M25P20 | 0101 |
| 32MB | x | | M25P40 | 0101 |
| 512MB | x | | M25P80 | 0101 |
| 1GB | x | Chingis (formerly PMC) | Pm25LV512A | 0100 |
| 2GB | x | | Pm25LV010A | 0101 |
| 4GB | x | | | |

| Designator | For M97-M2 | For Mannhatton |
|---|---|---|
| R_MEM_1 | 10K | 10K |
| R_MEM_2 | 40R/Short | 680R |
| R_MEM_3 | DY | DY |
| C_MEM | 2.2nF | 68pF |

SJV50

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison Memory / Straps

Size: A2 | Document Number: SJV50-CP | Rev: SB

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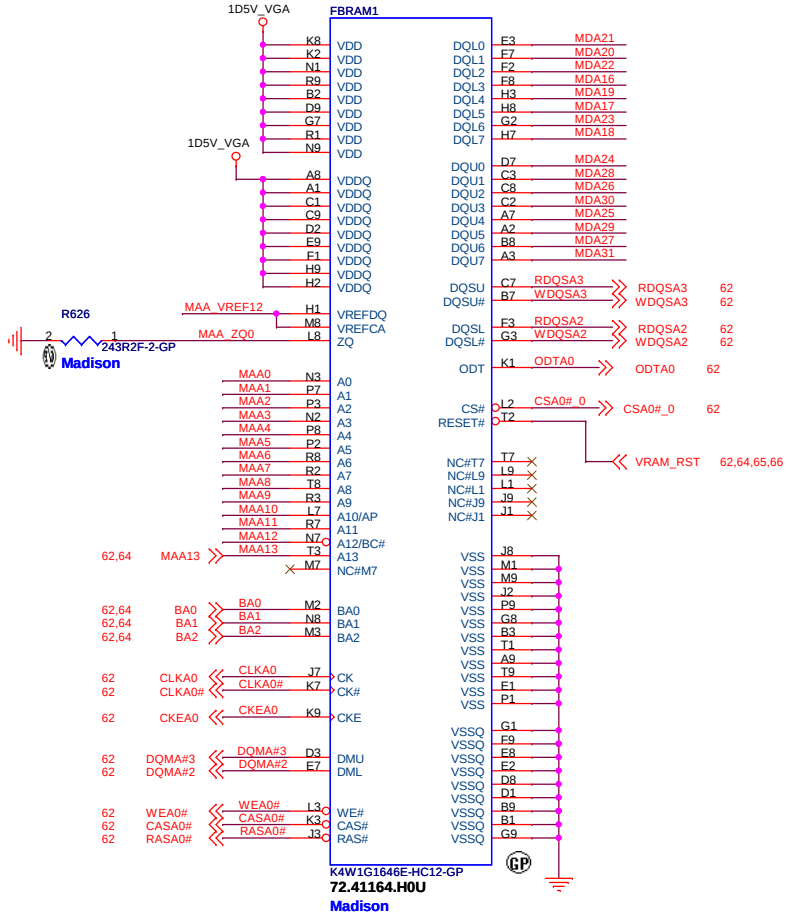
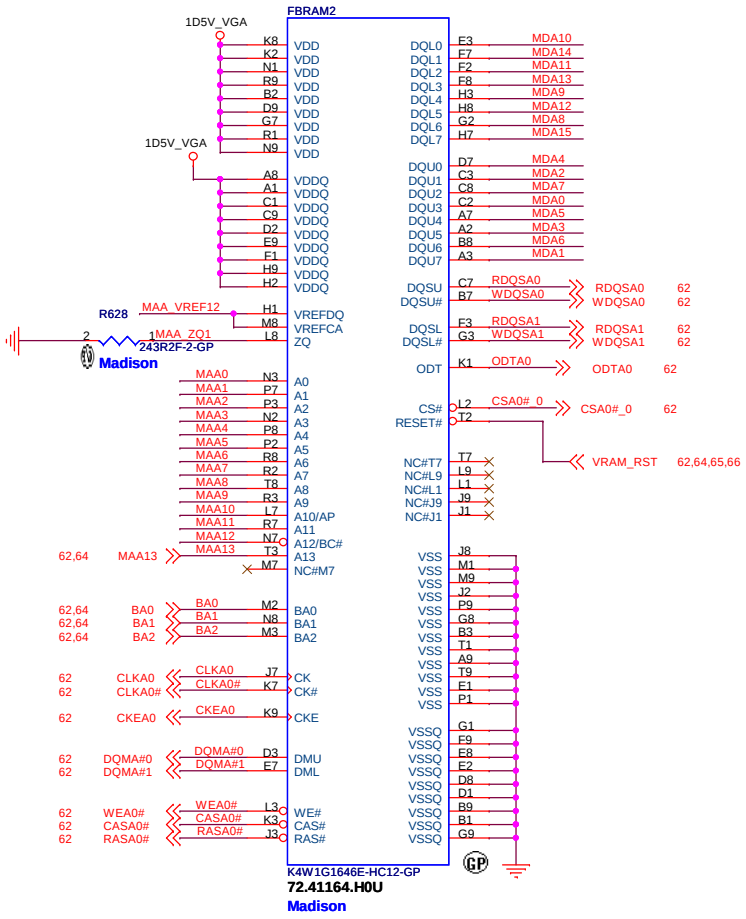
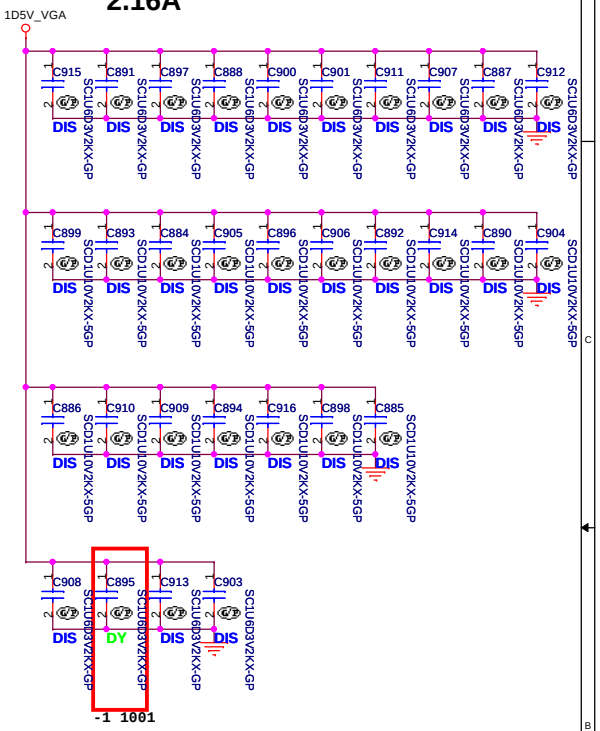
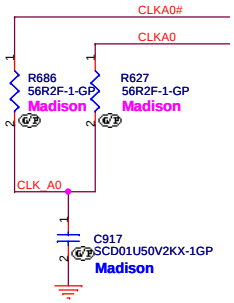
# DDR3

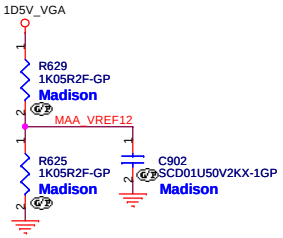



**SAMSUNG: 72.41164.H0U**
**HYNIX: 72.51G63.C0U**




62,64 DQMA#[0..7]

62,64 RDQSA[0..7]

62,64 WDQSA[0..7]

62,64 MAA[0..12] MAA[0..12]

62,64 MDA[0..63] MDA[0..63]

| | |
|---|---|
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| Title: *VRAM(1/4)* | |
| Size: A3 | Document Number: SJV50-CP |
| Rev: SB | |
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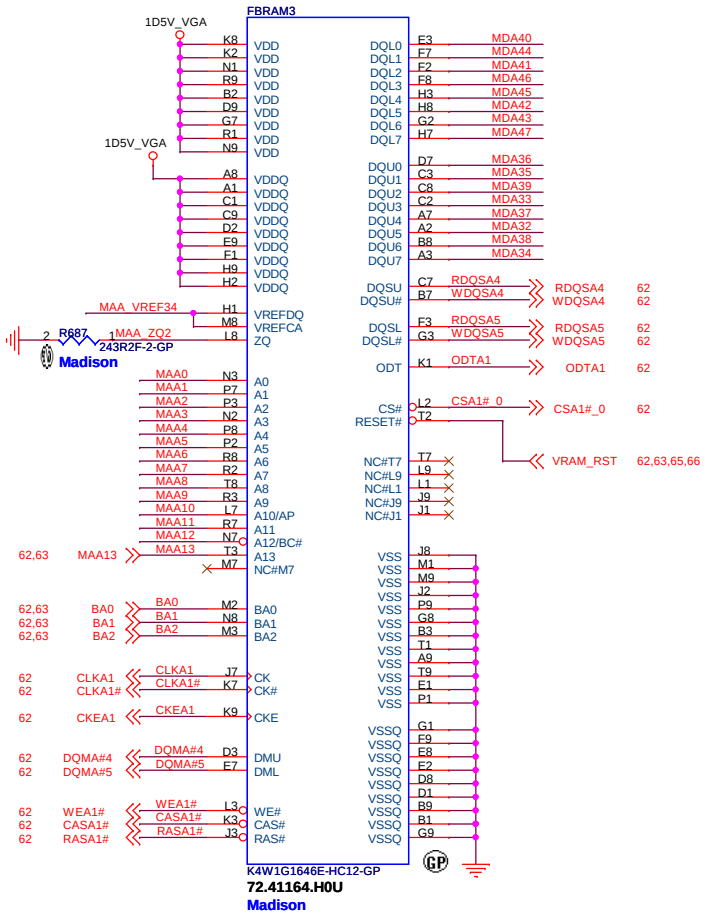
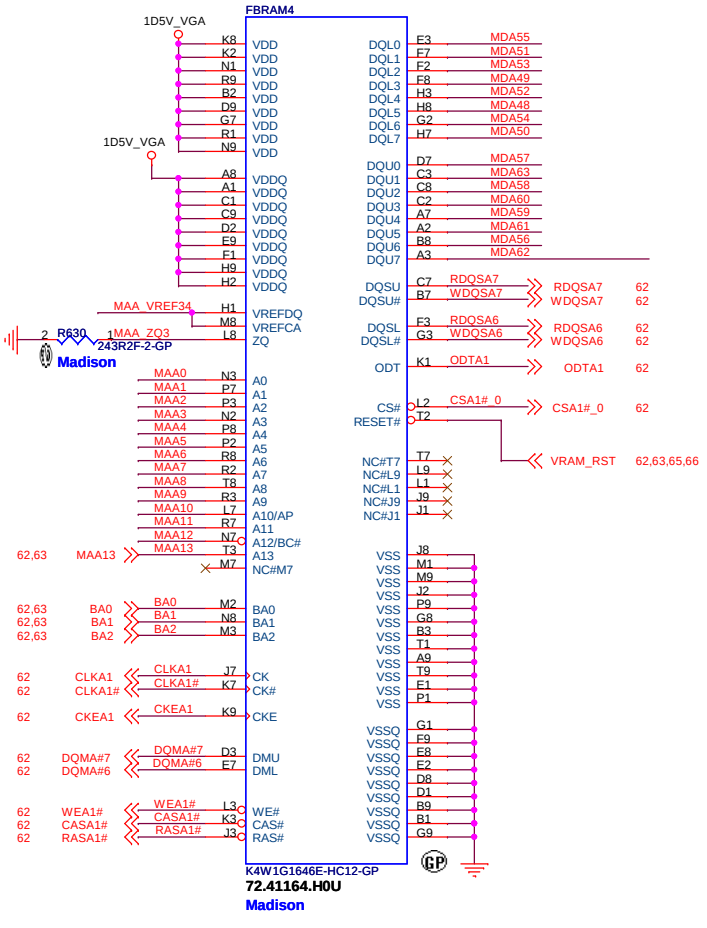
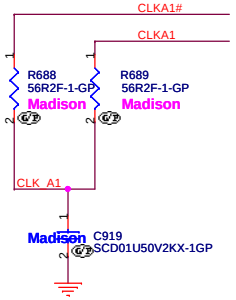
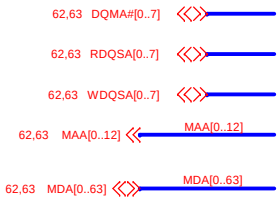
# DDR3

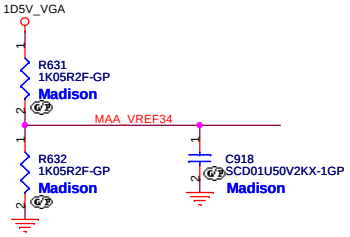



**SAMSUNG: 72.41164.H0U**
**HYNIX: 72.51G63.C0U**

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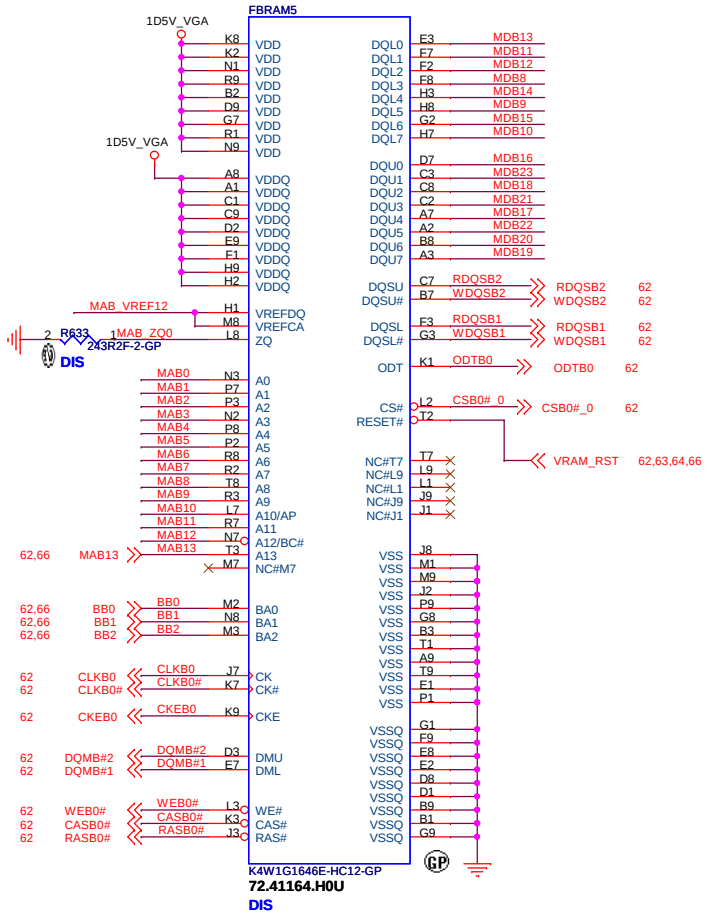
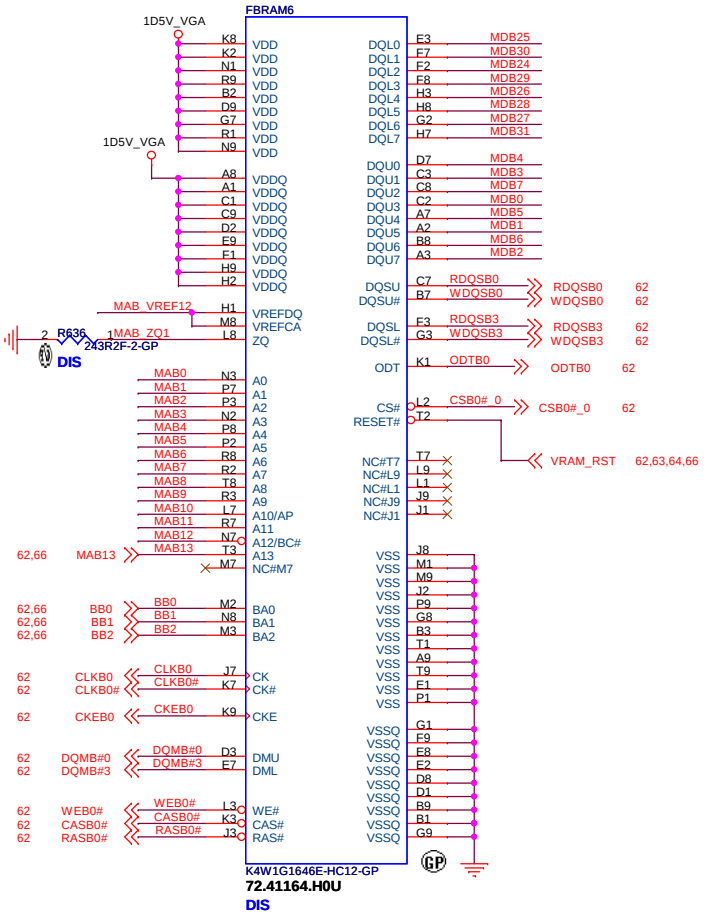
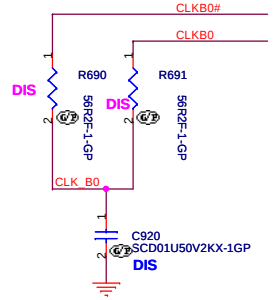
| Title: *VRAM(2/4)* | | |
| Size: A3 | Document Number: SJV50-CP | Rev: SB |
| Date: Wednesday, October 21, 2009 | Sheet 64 of 67 | |

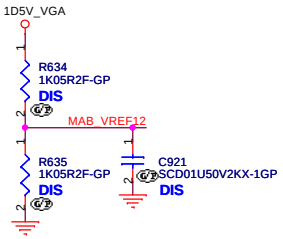
# DDR3

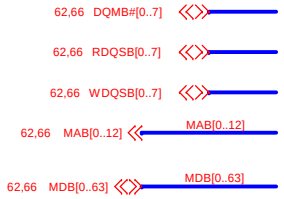



**SAMSUNG: 72.41164.H0U**
**HYNIX: 72.51G63.C0U**

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| Title: *VRAM(3/4)* | | |
| Size: A3 | Document Number: SJV50-CP | Rev: SB |
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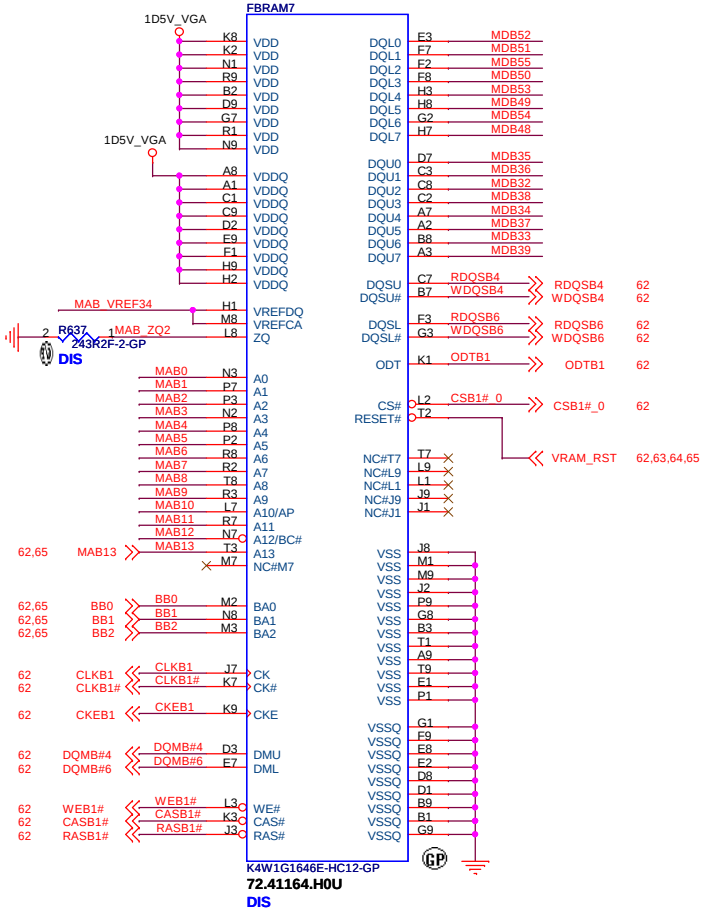
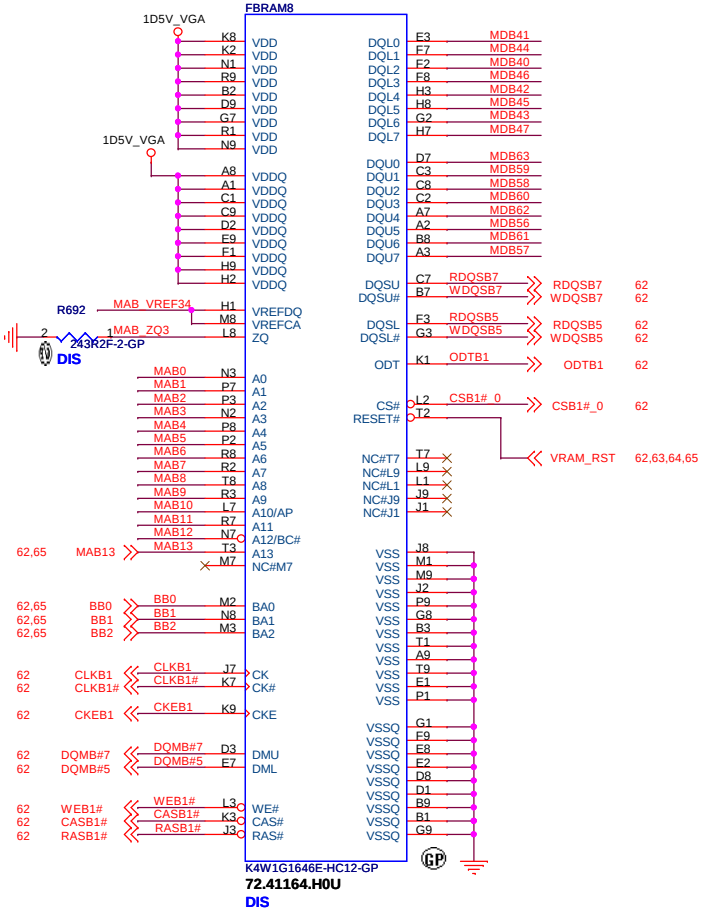
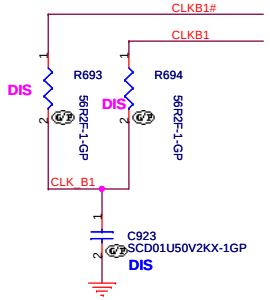
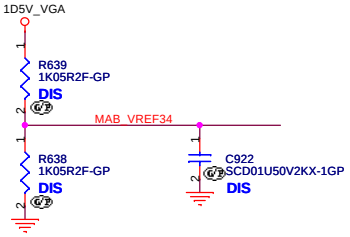
# DDR3




**SAMSUNG: 72.41164.H0U**
**HYNIX: 72.51G63.C0U**




62,65 DQMB#[0..7]

62,65 RDQSB[0..7]

62,65 WDQSB[0..7]

62,65 MAB[0..12] MAB[0..12]

62,65 MDB[0..63] MDB[0..63]

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| Title: ***VRAM(4/4)*** | | |
| Size: A3 | Document Number: **SJV50-CP** | Rev: SB |
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SB
0812
Page57-66: change GPU
Page24: swap U5 & U6
Page15: change R112 to 22ohm
Page43: D8 change to 83.00016.B11 83.00016.K11 83.00016.F11
Page25: change PS8325 to PS8271
Page4: add R660 RN74 for DIS_ONLY
Page8: add R180 R668 R669 R685 R695 for DIS_ONLY
Page8: change C190 C192 C193 C194 to UMA_PX
Page5: add RN75 for DIS_ONLY
Page52: change GFX to UMA_PX
Page12: change R385 to DIS_ONLY and X4 C529 C530 to UMA_PX and add R381 R640
Page14: change RN48 RN49 R149 R153 C62 C63 C66 C67 C68 C69 C76 C77 to UMA_PX
Page16: cahgne R194 to UMA_DIS_ONLY and change R196 to PX
Page17: change R150 R170 C219 C220 to UMA_PX and add R696 R697 for DIS_ONLY
Page22: change U30 U33 R320 R321 C359 C360 C361 C388 C392 C394 to PX
Page22: add RN76 RN77 RN78 RN80 for DIS_ONLY
Page22: change U13 U14 R266 to PX and add RN81 for DIS_ONLY
Page22: change U24 to PX and add R698 for DIS_ONLY
Page22: change U39 C45 to PX and add RN82 for DIS_ONLY
Page23: change U12 R143 to PX and change R111 to UMA_PX and add R699 for DIS_ONLY
Page23: change U1 to PX and add R700 for DIS_ONLY
Page24: change U6 to UMA_PX
Page24: change U35 U38 R49 to PX and add RN83 for DIS_ONLY
Page40: change R84 to 65W and change R88 to 90W
0814
Page50: DY R571 and add R649
Page59: add R774 DY
Page53: change R334 to 7.5K(64.75015.6DL) and add Q51 R775
Page53: change R331 to 15K(64.15025.6DL) DY and change R322 R328 C419 DY
Page3: change C297 C298 from 27p to 12p
Page32: codec co-layout
Page11: change 1D05V_S0 to 3D3V_S5
Page5,8,10,13,16,20,21,43,50: System Level Implemention to Reduce S3 State Power On
0817
Page59: swap SWAP NV_HDMI_DATA0+/- and NV_HDMI_DATA2+/-
Page43: add Q48, R725, R726, R52 and C943 for 1D5V_S0_PWRGD level shift
Page5: change U86 pin1,2 connection to 1D5V_S0_PWRGD
Page50: change R724 pin1 connection to 1D5V_S0_PWRGD
Page32: R778 option ALC271
Page10: RN51 DY, change netname M_VREF_DQ_DIMM0, M_VREF_DQ_DIMM1
Page20: del R67 U80 R791 R65 R66; R289 C403 C402 no-option , off-page M_VREF_DQ_DIMM0
Page21: del R67 U80 R791 R65 R66; R289 C403 C402 no-option , off-page M_VREF_DQ_DIMM0
0819
Page43: U41 change to 84.04468.037
Page59: change VGA_XIN1 connect to VGA1B.AW34
Page53: R331 DIS, Q51 DY to keep +VGA_CORE 1.05V
Page59: change RN79 to R378
Page23: change R19 pin2 connecot to BRIGHTNESS_DIS
Page5: RN75 mount
Page20: del R718 RN84
Page24: U6 change to 73.2G125.A07 UMA_PX(the same as U5), and modify enable to High active
Page43: Q48 change to Q48 and Q49
Page16: Q47 change to BJT 84.T3904.C11
Page50: del Q45
Page16: C939 change to 47nF
Page30: U34 R318 C37 DY, R32 mount
0820
Page33: change RT17 RT18 to 22K for gain
Page63-66: swap the signals of VRAM
Page47: change R542 R546 to 63.00000.00L
0821
Page43: change part reference C593 to C718
Page32: change codec co-layout to ALC272
Page5: change R151.1 to 1D5V_S0_DDR
Page16: change RN32 to R648 single resister
Page47: R532 mount,R523 DY
Page47: change R531,R259 to 64.13035.6DL
Page48: change R539 to 64.10R05.55L
Page48: change R549 to 64.20035.6DL
Page48: change R534 to 64.95315.6DL
Page48: change U23,U58 to 74.51117.073
Page48: Delete R543
Page48: change R258 to 64.13025.6DL
Page49: change U51 to 74.51117.073
Page49: change R235 to 64.75015.6DL
Page53: change U36 to 74.51117.073
Page53: Delete R326
Page50: change U66 to 74.02997.A79
Page33: delete R708
0824
Page52: change U49 to 74.62881.A73
0825
Page12: delete R228
Page32: add R152
Page11: change R422 to 63.47034.1DL
Page39: add R228 DY
0827
Page25: delete D3
0916
Page15: change R127 to 63.10334.1DL mount

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Title: HISTORY

| Size | Document Number | Rev |
|---|---|---|
| A2 | SJV50-CP | SB |

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