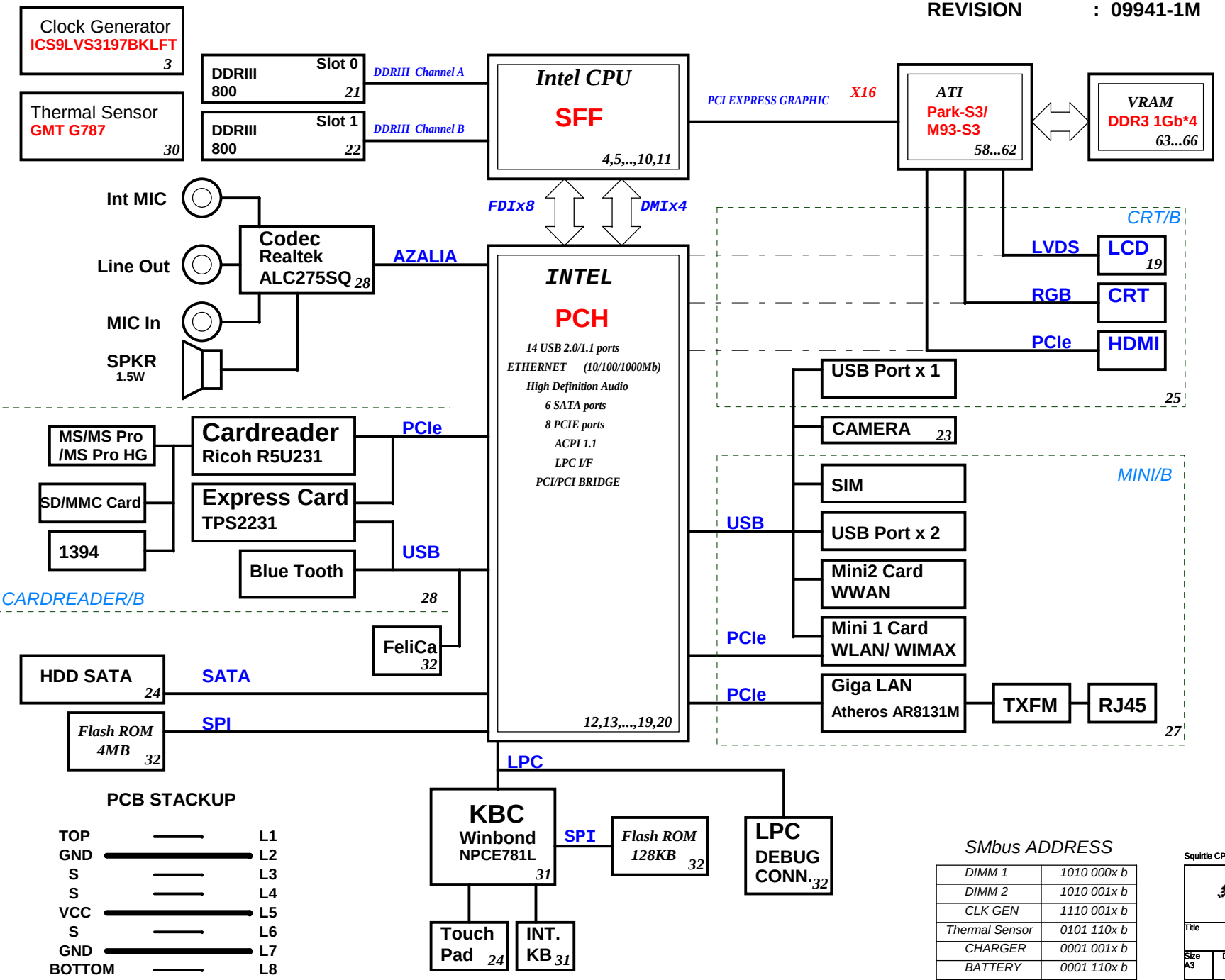
CADIZ-CP Block Diagram

PROJECT CODE : 91.4JH01.001
PCB P/N : 48.4JH01.01M
REVISION : 09941-1M



PCB STACKUP

TOP		L1
GND		L2
S		L3
S		L4
VCC		L5
S		L6
GND		L7
BOTTOM		L8

SMbus ADDRESS

DIMM 1	1010 000x b
DIMM 2	1010 001x b
CLK GEN	1110 001x b
Thermal Sensor	0101 110x b
CHARGER	0001 001x b
BATTERY	0001 110x b

SYSTEM DC/DC
RT8223 37

INPUTS	OUTPUTS
DCBATOUT	5V_S5(9A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5

RT8209 39

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(20A)

RT8209 38

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(13.5A)

RT9026 36

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 1.2A

CHARGER
BQ24751 32

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC
ADP3211 36

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 27A

VGA/ GFX Core
ADP3211 40

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE/ VCC_GFXCORE 11A

Squirtle CP DIS SAMSUNG

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: BLOCK DIAGRAM

Size	Document Number	Rev
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Date: Saturday, April 24, 2010 Sheet 1 of 57

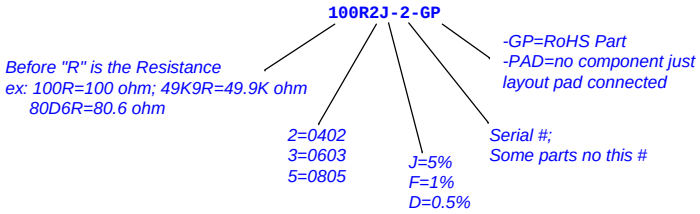
PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

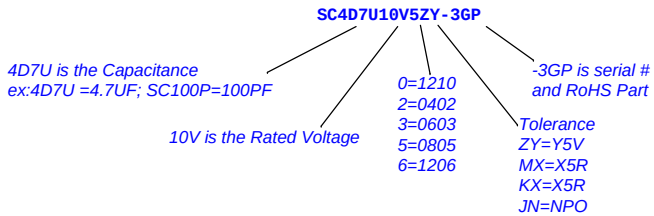
Processor Strapping

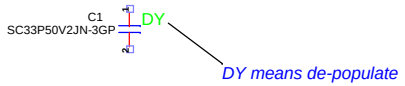
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

Resistor



Capacitor





Squirtle CP DIS SAMSUNG

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **Reference**

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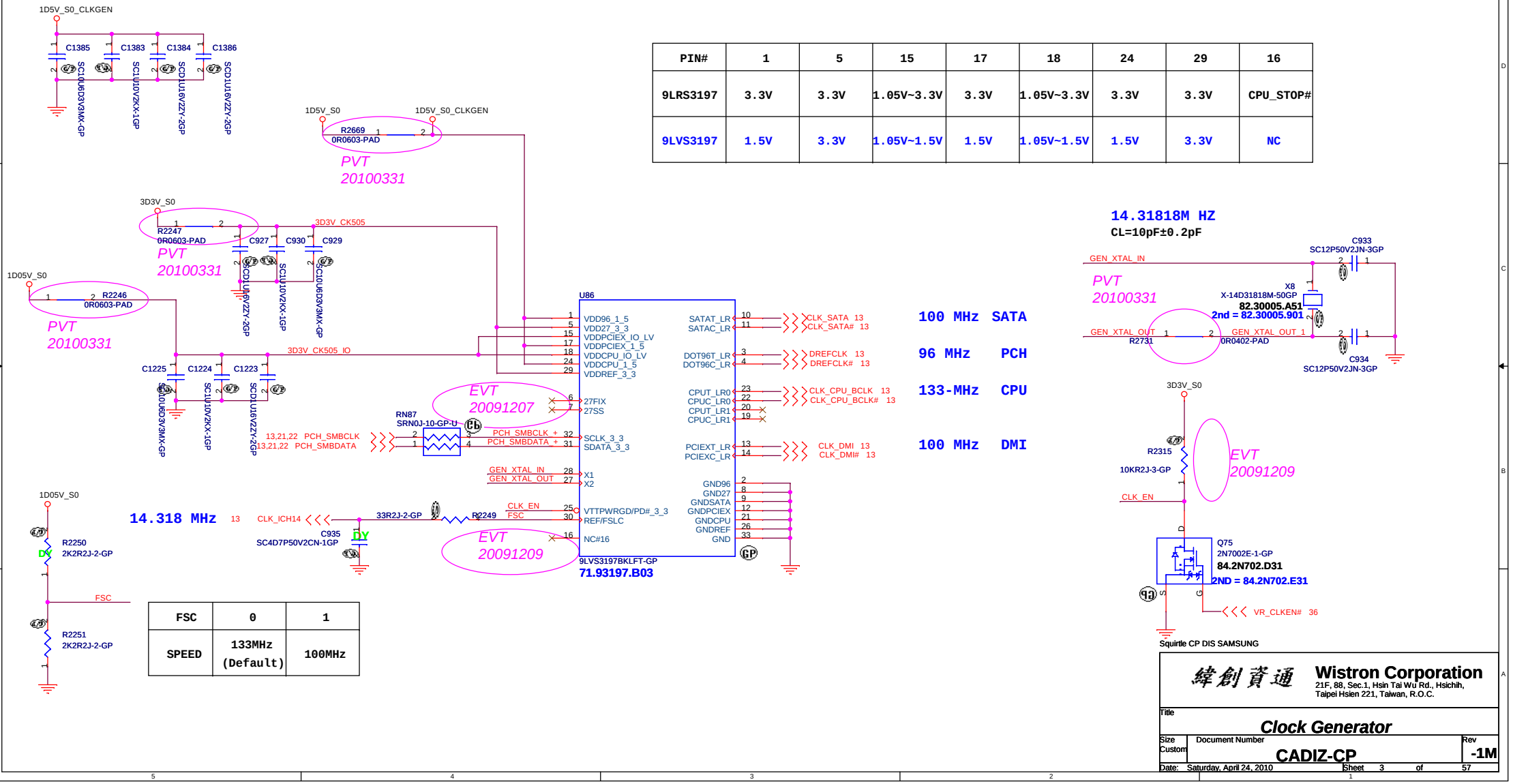

PIN#	1	5	15	17	18	24	29	16
9LRS3197	3.3V	3.3V	1.05V~3.3V	3.3V	1.05V~3.3V	3.3V	3.3V	CPU_STOP#
9LVS3197	1.5V	3.3V	1.05V~1.5V	1.5V	1.05V~1.5V	1.5V	3.3V	NC

FSC	0	1
SPEED	133MHz (Default)	100MHz

Wistron Corporation
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Title: Clock Generator

Size: Custom | Document Number: CADIZ-CP | Rev: -1M

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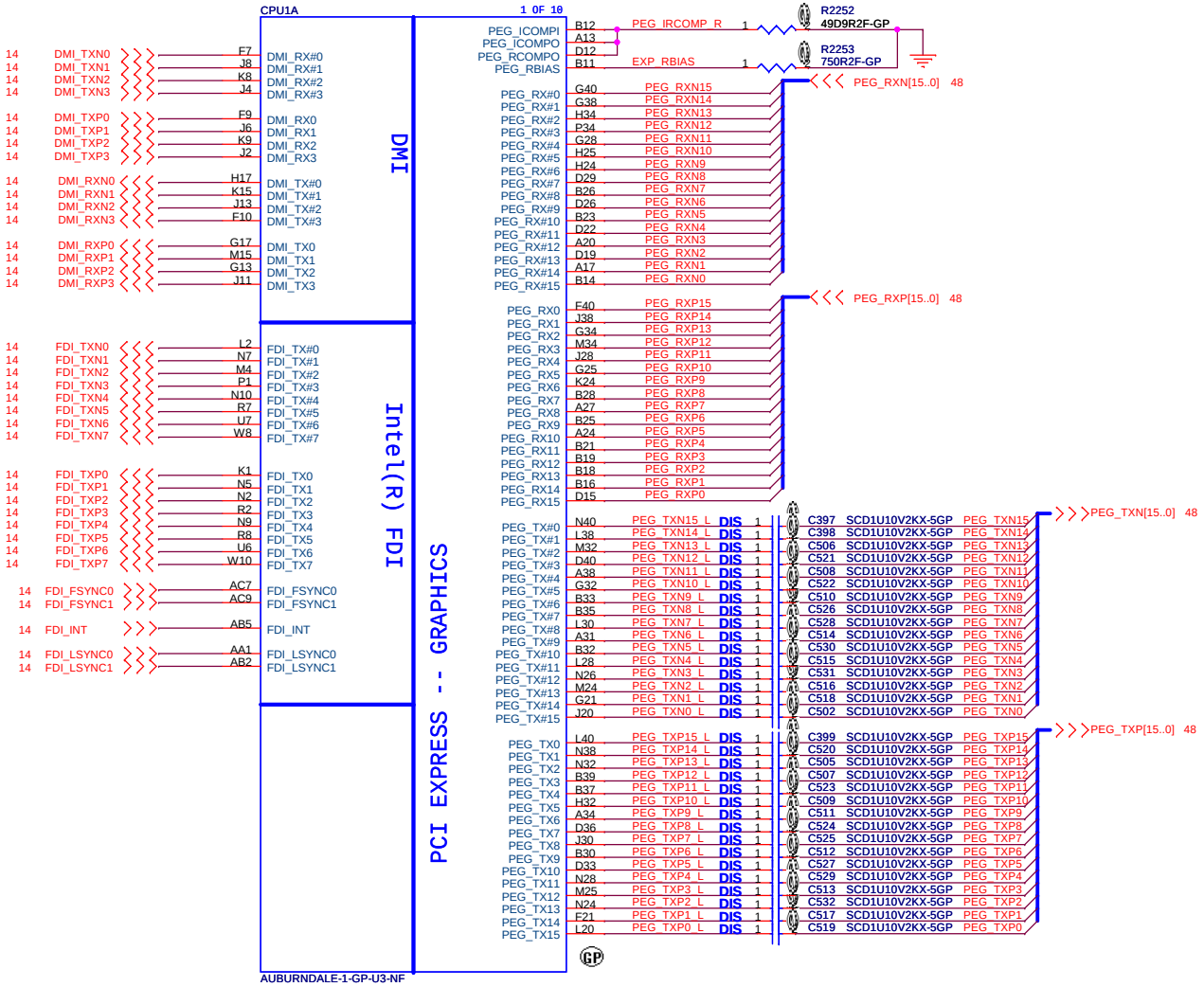

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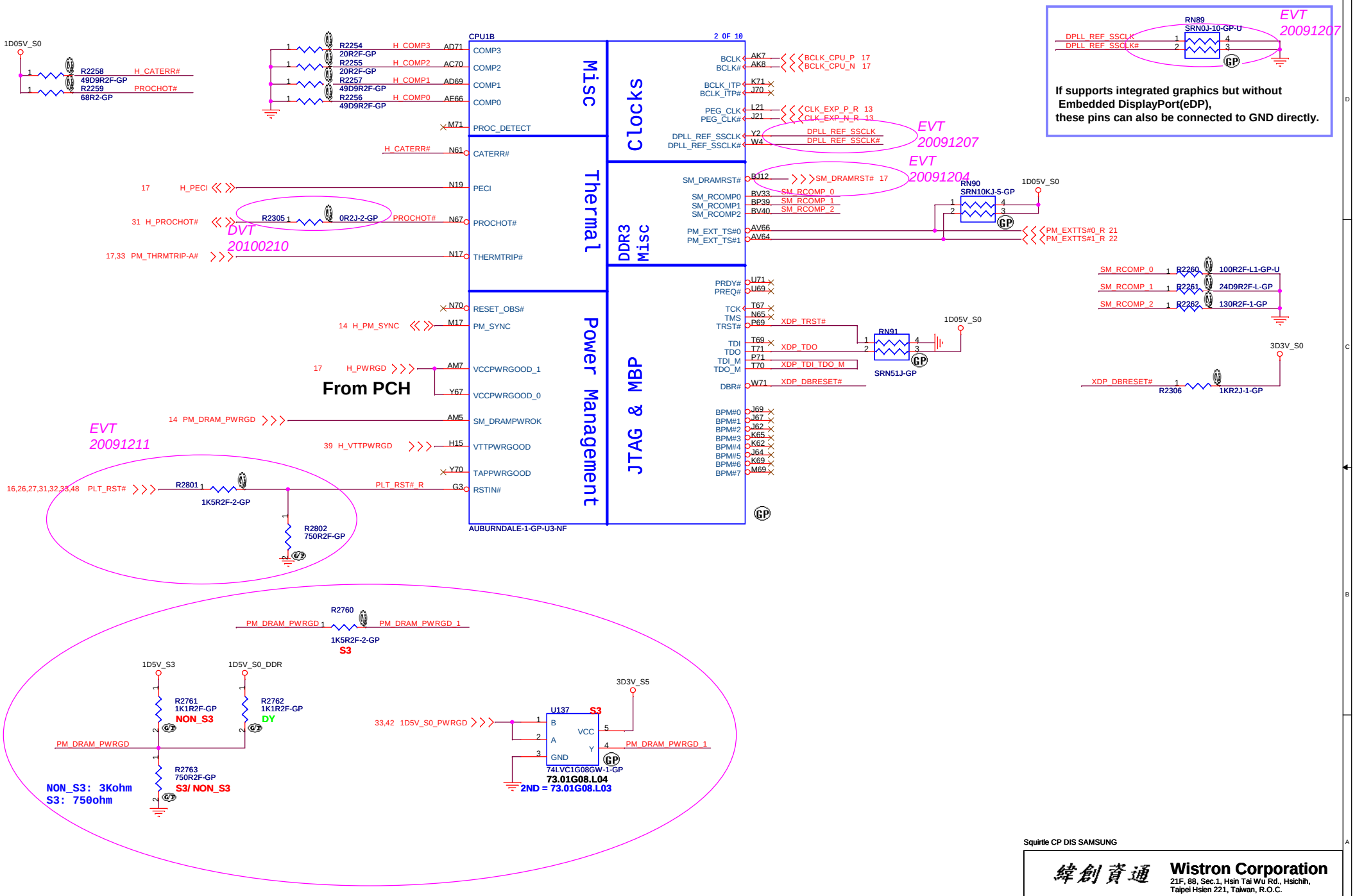
Title	CPU SFF 1 of 8(DMI/FDI/PEG)	
Size A3	Document Number CADIZ-CP	Rev -1M
Date: Saturday, April 24, 2010	Sheet 4 of 57	



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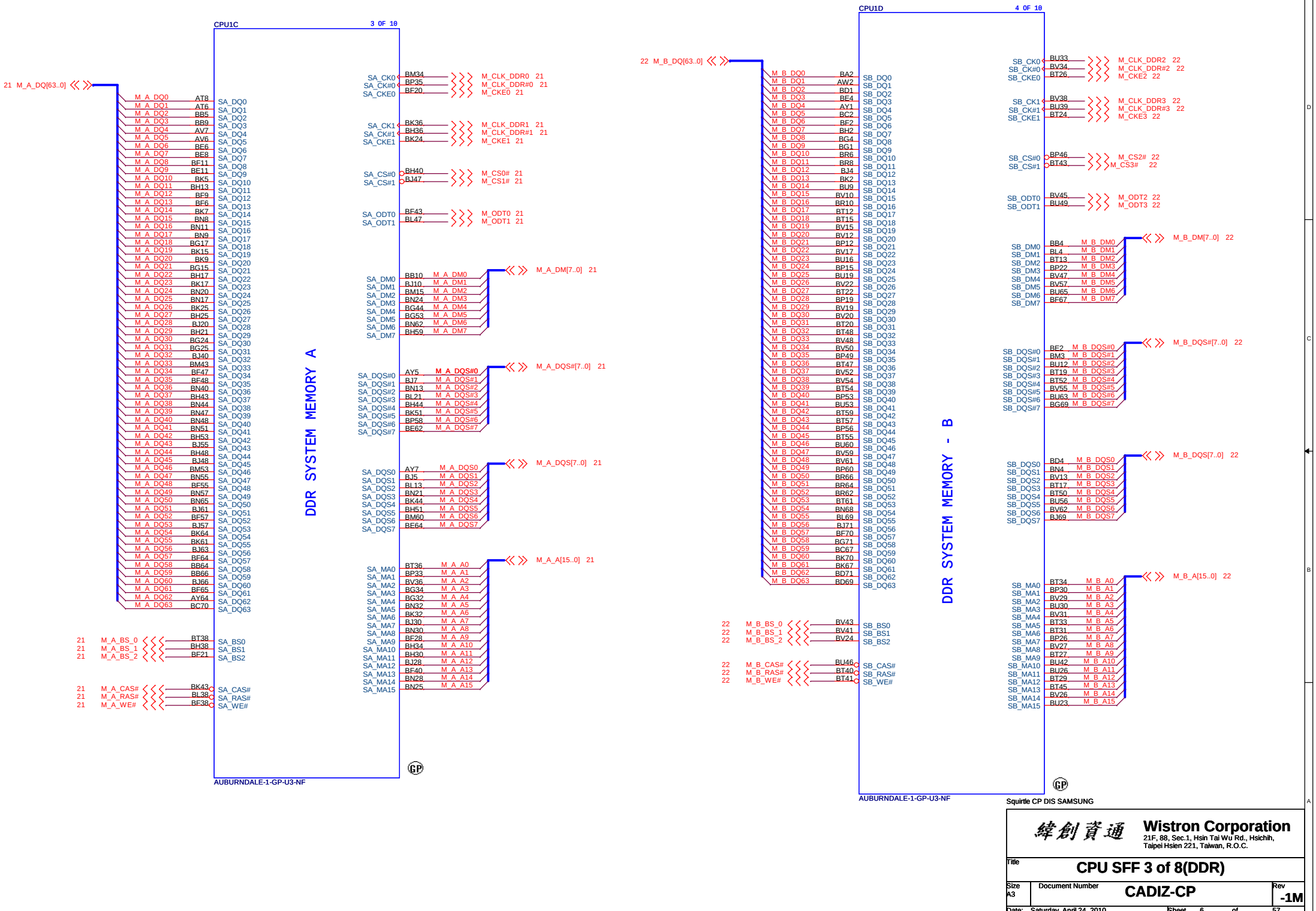
Title: CPU SFF 2 of 8(CLK/Thermal)

Size	Document Number	Rev
A3	CADIZ-CP	-1M

Date: Saturday, April 24, 2010 Sheet 5 of 57


CPU1C
3 OF 10
DDR SYSTEM MEMORY A
AUBURNDALE-1-GP-U3-NF
CPU1D
4 OF 10
DDR SYSTEM MEMORY - B
AUBURNDALE-1-GP-U3-NF
Squirtle CP DIS SAMSUNG
Wistron Corporation
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Title
CPU SFF 3 of 8(DDR)
Size
A3
Document Number
CADIZ-CP
Rev
-1M
Date: Saturday, April 24, 2010
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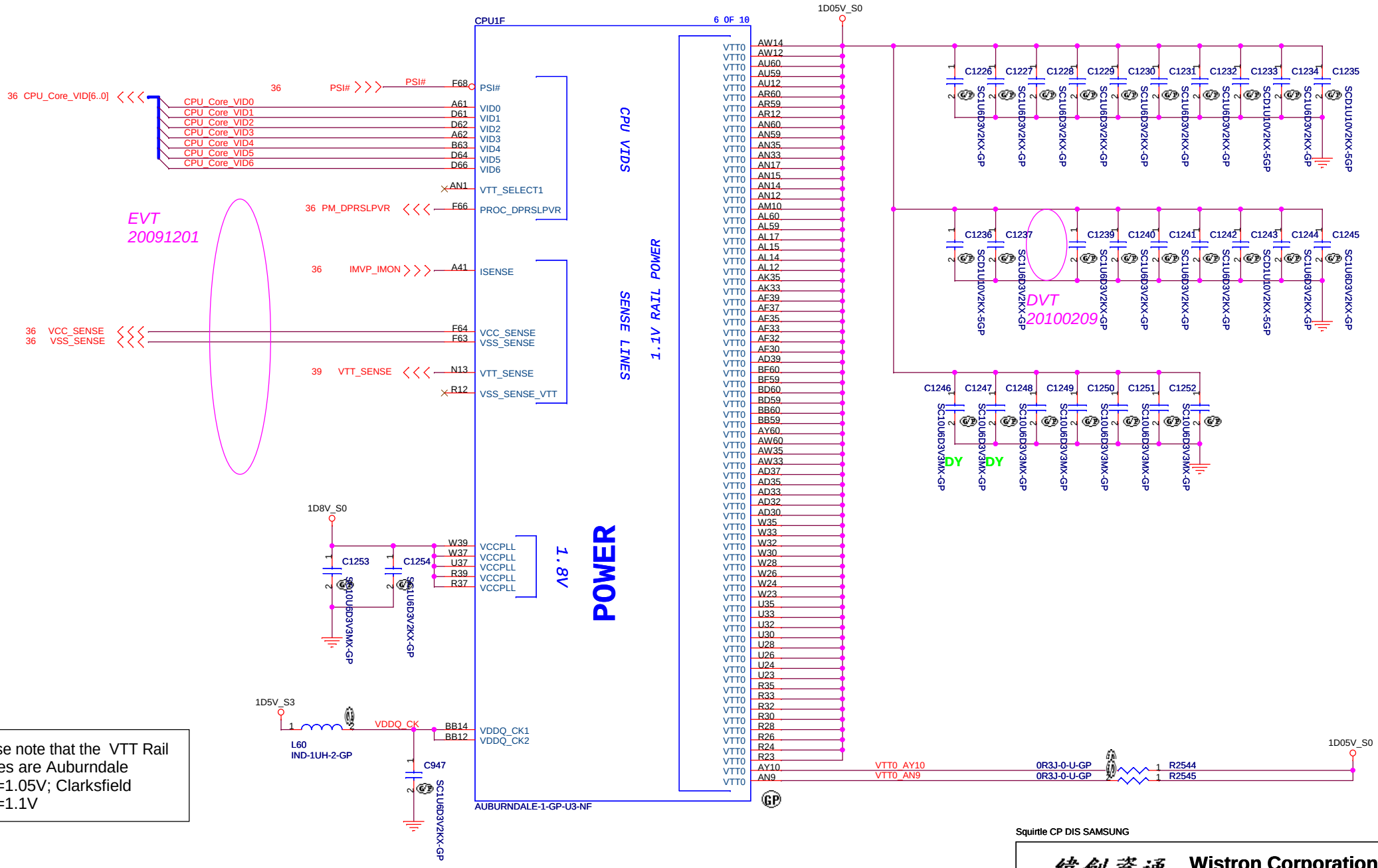

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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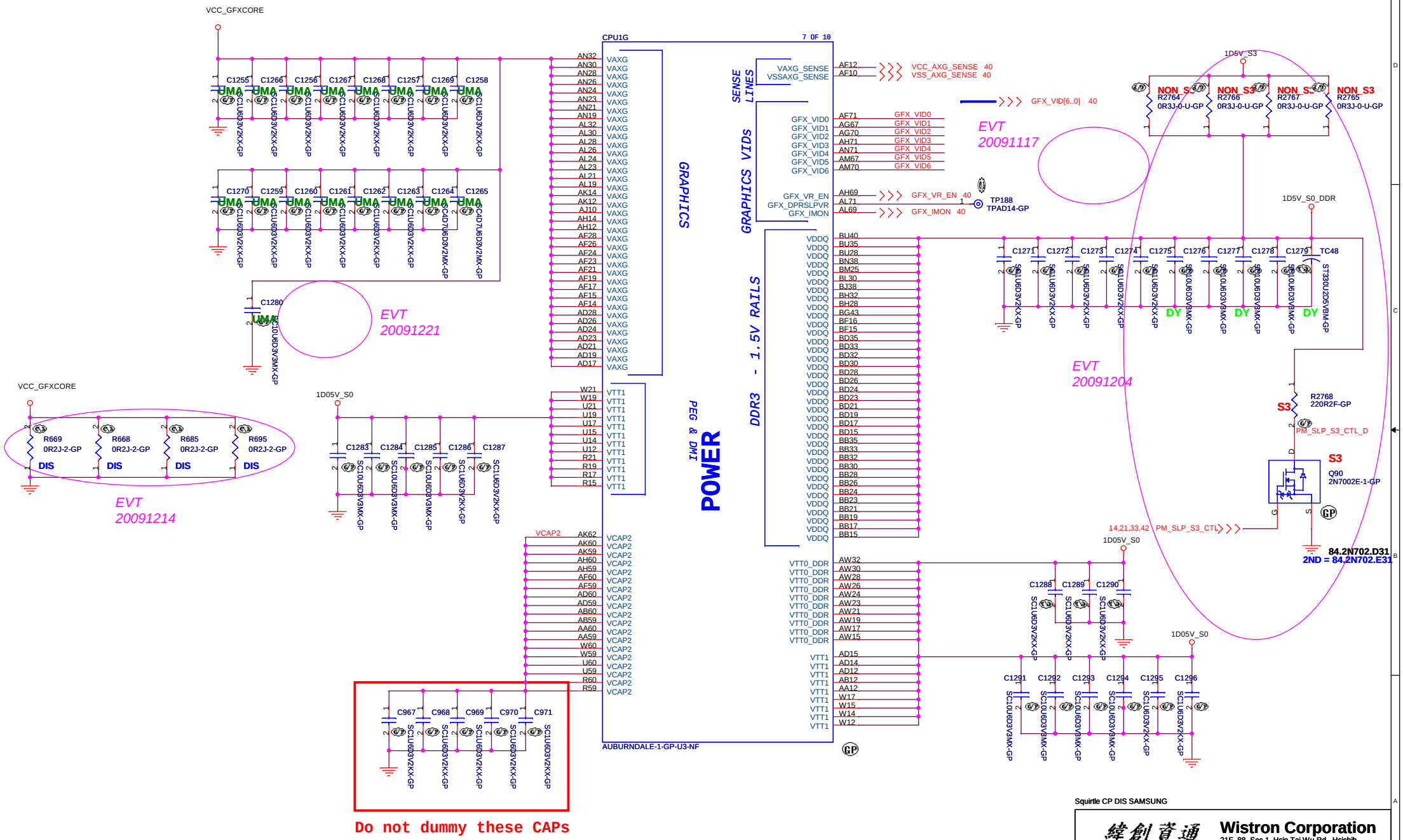
Title	CPU SFF 4 of 8(POWER/VTT)		
Size: Custom	Document Number: CADIZ-CP		Rev: -1M
Date: Saturday, April 24, 2010	Sheet 7 of 57		


VCC_GFXCORE
CPU1G
7 OF 10
GRAPHICS
PEG & DMI
POWER
DDR3 - 1.5V RAILS
GRAPHICS VIDs
SENSE LINES
AUBURNDALE-1-GP-U3-NF
VAXG_SENSE
VSSAXG_SENSE
VCC_AXG_SENSE 40
VSS_AXG_SENSE 40
GFX_VID[6..0] 40
GFX_VID0
GFX_VID1
GFX_VID2
GFX_VID3
GFX_VID4
GFX_VID5
GFX_VID6
GFX_VR_EN
GFX_DPRSLPVR
GFX_IMON
GFX_VR_EN 40
GFX_IMON 40
TP188
TPAD14-GP
1D5V_S3
1D5V_S0_DDR
1D05V_S0
VCAP2
VTT0_DDR
VTT1
VDDQ
NON_S3
R2764
R2766
R2767
R2765
0R3J-0-U-GP
R2768
220R2F-GP
PM_SLP_S3_CTL_D
PM_SLP_S3_CTL
14,21,33,42
Q90
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
R669
R668
R685
R695
0R2J-2-GP
DIS
EVT
20091221
EVT
20091117
EVT
20091204
EVT
20091214
Do not dummy these CAPs
Squirtle CP DIS SAMSUNG
Wistron Corporation
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Title
CPU SFF 5 of 8(PWR/DDR/GFX/)
Size
A3
Document Number
CADIZ-CP
Rev
-1M
Date: Saturday, April 24, 2010
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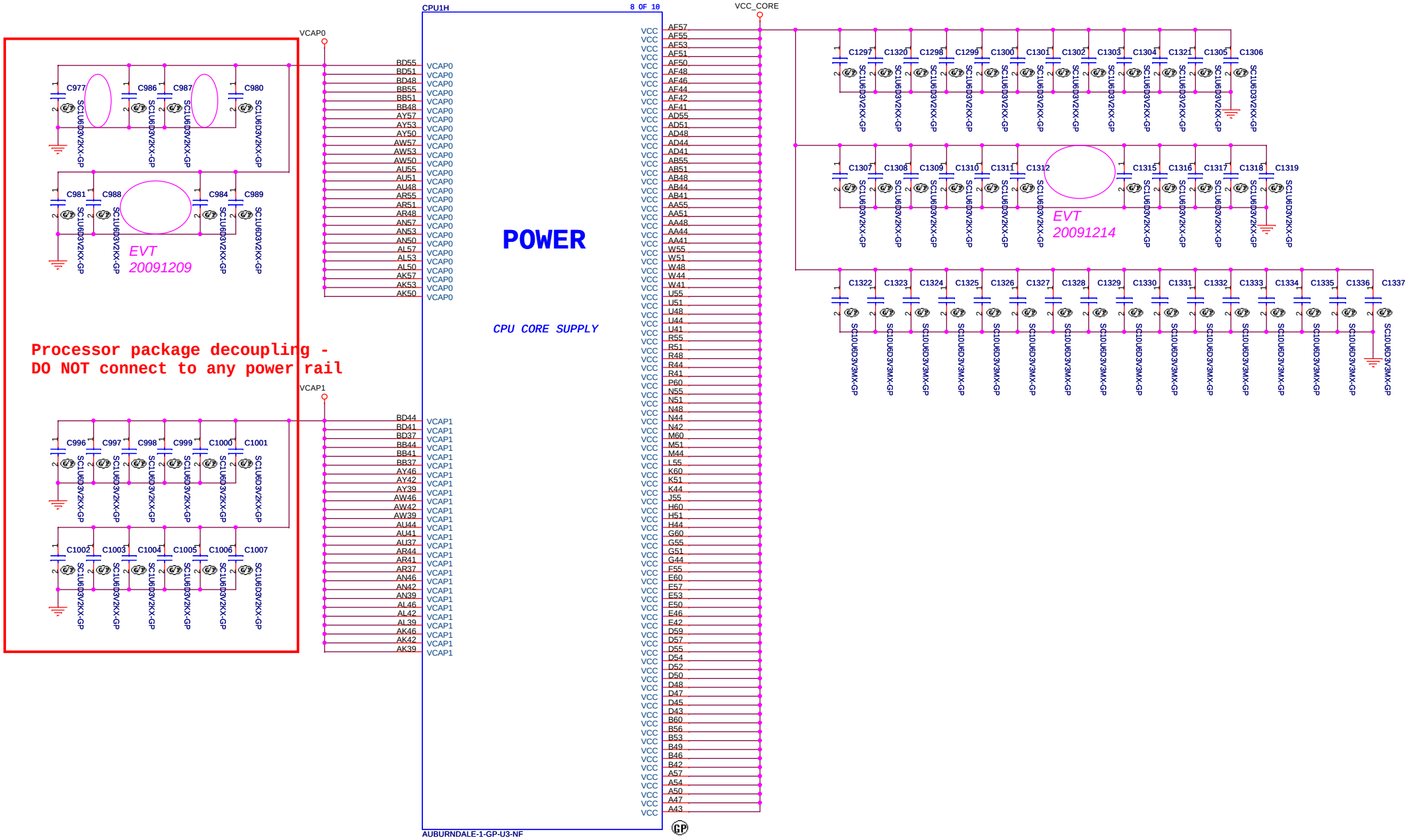

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Title	CPU SFF 6 of 8(CPUCORE)	
Size A3	Document Number CADIZ-CP	Rev -1M
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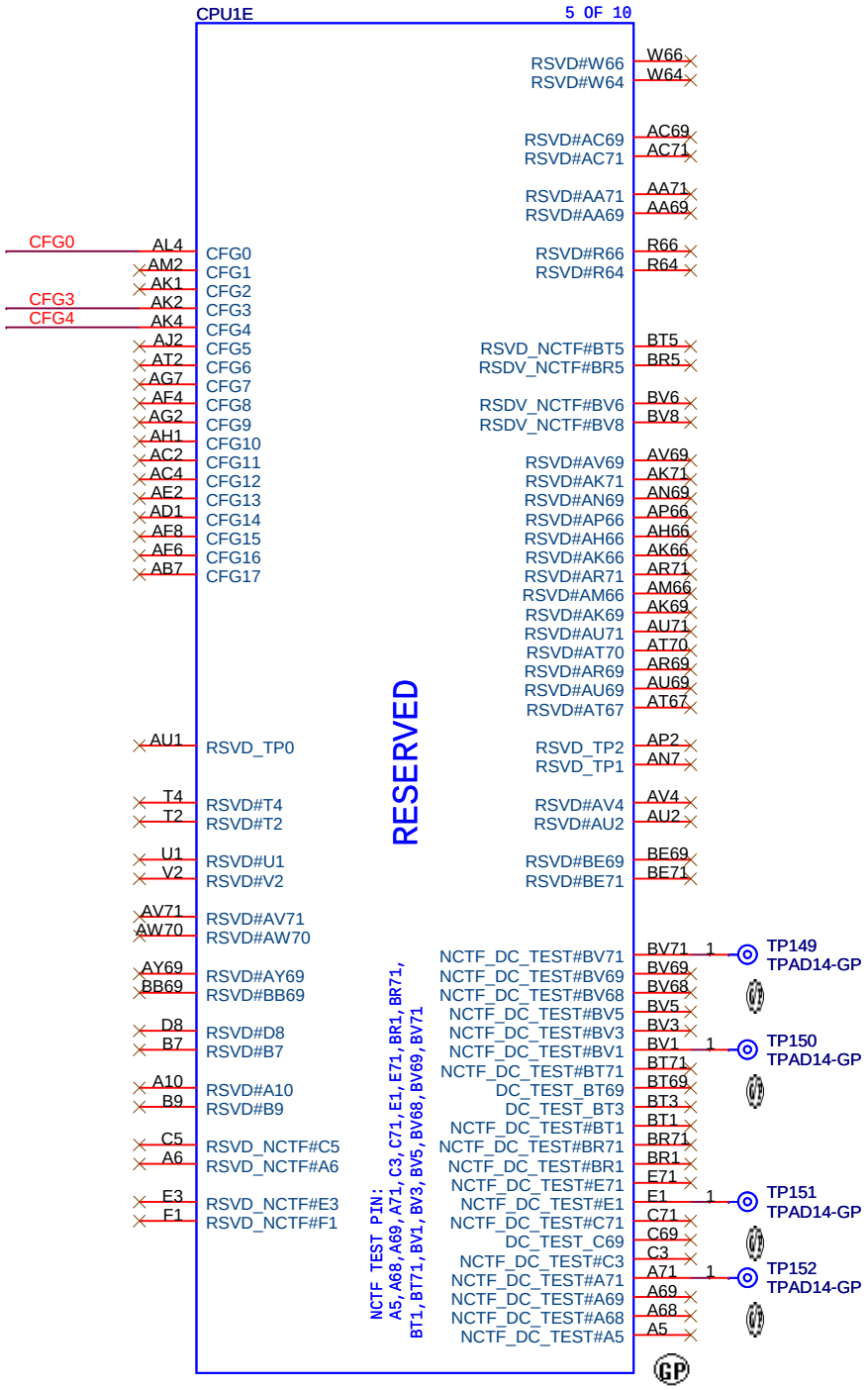

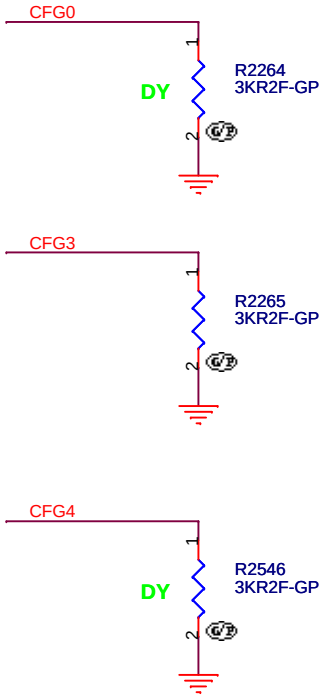

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

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Title: **CPU SFF 7 of 8(RESERVED)**

Size	Document Number	Rev
A4	CADIZ-CP	-1M

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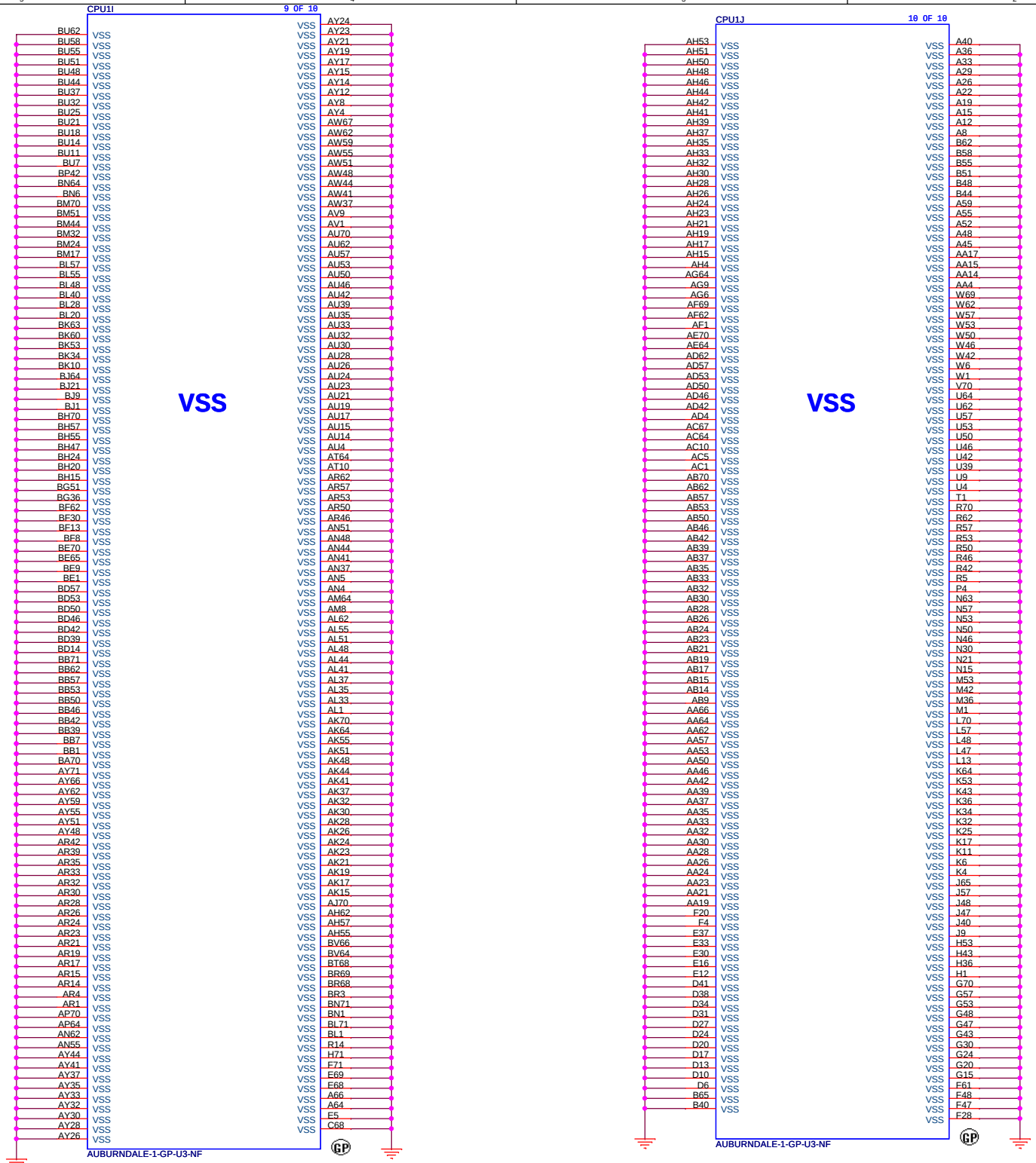

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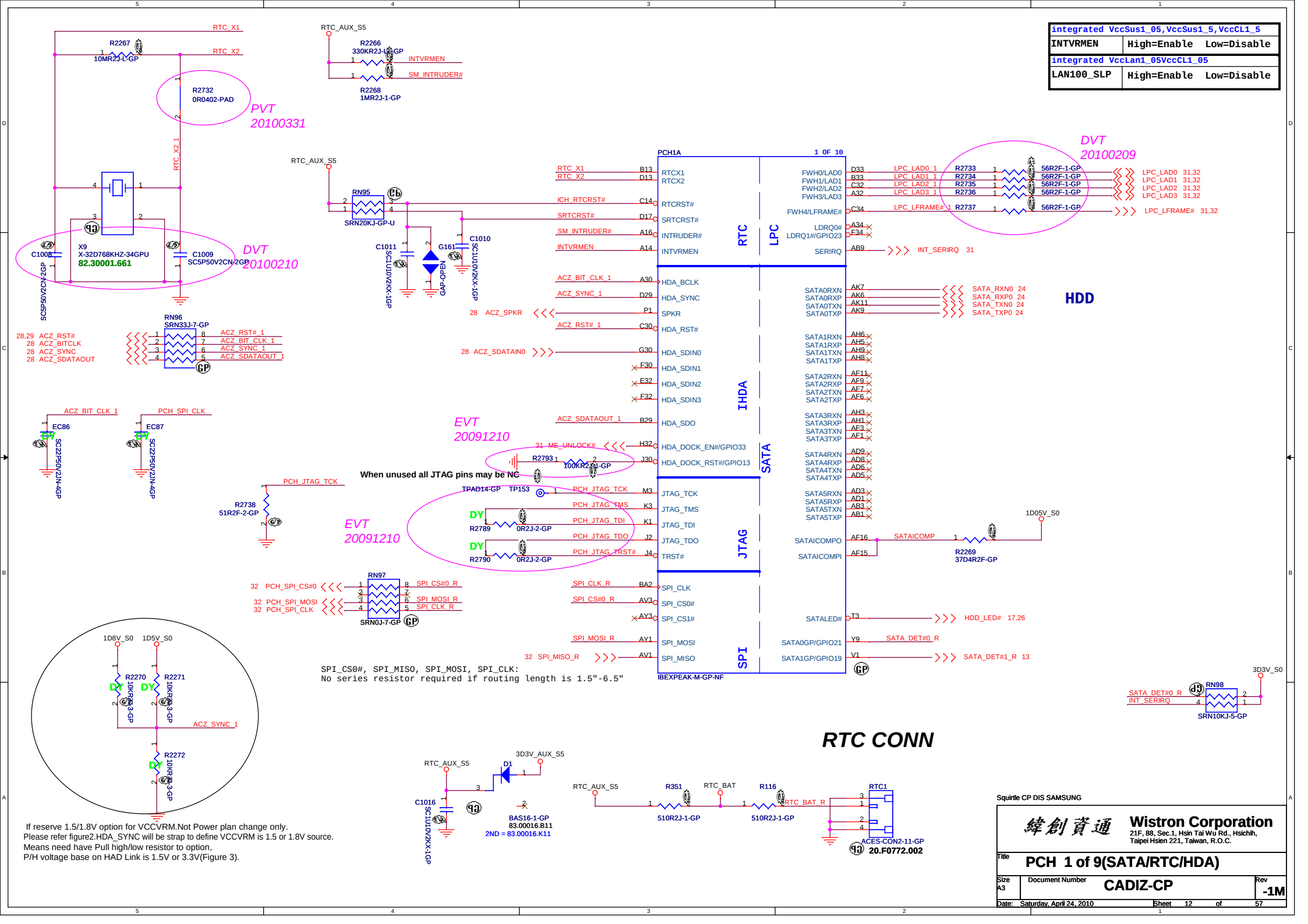
Title	CPU SFF 8 of 8(VSS)	
Size A3	Document Number CADIZ-CP	Rev -1M
Date: Saturday, April 24, 2010	Sheet 11 of 57	


integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
IBEXPEAK-M-GP-NF
HDD
RTC CONN
When unused all JTAG pins may be NC
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"
If reserve 1.5/1.8V option for VCCVRM.Not Power plan change only.
Please refer figure2.HDA_SYNC will be strap to define VCCVRM is 1.5 or 1.8V source.
Means need have Pull high/low resistor to option,
P/H voltage base on HAD Link is 1.5V or 3.3V(Figure 3).
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Title PCH 1 of 9(SATA/RTC/HDA)
Size A3
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Sheet 12 of 57

MINICARD1-WLAN

CARDREADER

LAN

ExpressCard

EVT 20091120

PCH1B

2 OF 10

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

IBEXPEAK-M-GP-NF

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

EVT 20091207

EVT 20091201

DVT 20100210

PVT 20100331

PVT 20100401

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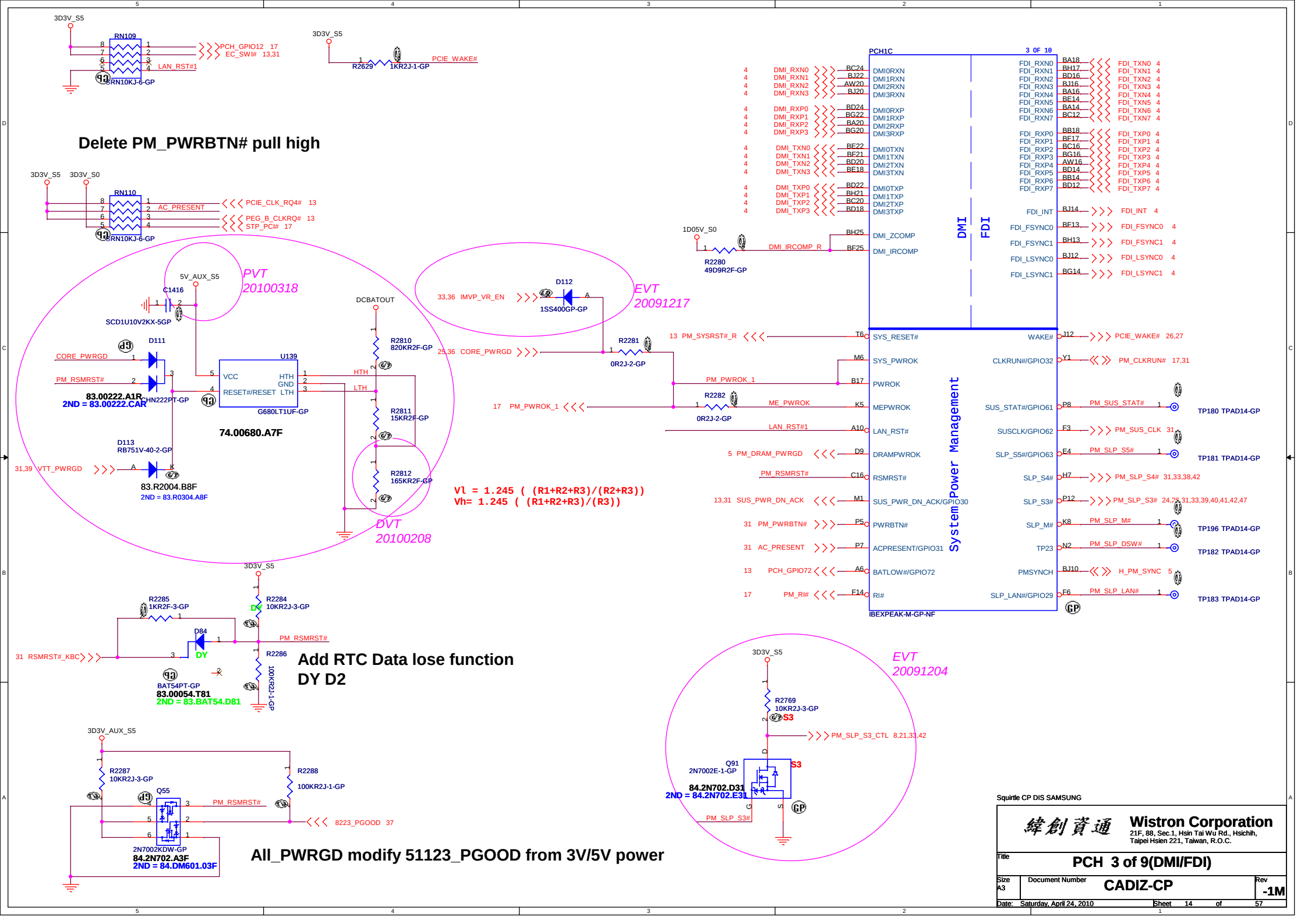
Title: PCH 2 of 9(PCIE/CLK/SMB)			
Size: A3	Document Number: CADIZ-CP		Rev: -1M
Date: Saturday, April 24, 2010	Sheet 13 of 57		


Delete PM_PWRBTN# pull high
PVT 20100318
DVT 20100208
EVT 20091217
EVT 20091204
Vl = 1.245 ((R1+R2+R3)/(R2+R3))
Vh= 1.245 ((R1+R2+R3)/(R3))
Add RTC Data lose function
DY D2
All_PWRGD modify 51123_PGOOD from 3V/5V power
PCH1C
IBEXPEAK-M-GP-NF
DMI
FDI
System Power Management
Squirtle CP DIS SAMSUNG
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PCH 3 of 9(DMI/FDI)
CADIZ-CP
-1M
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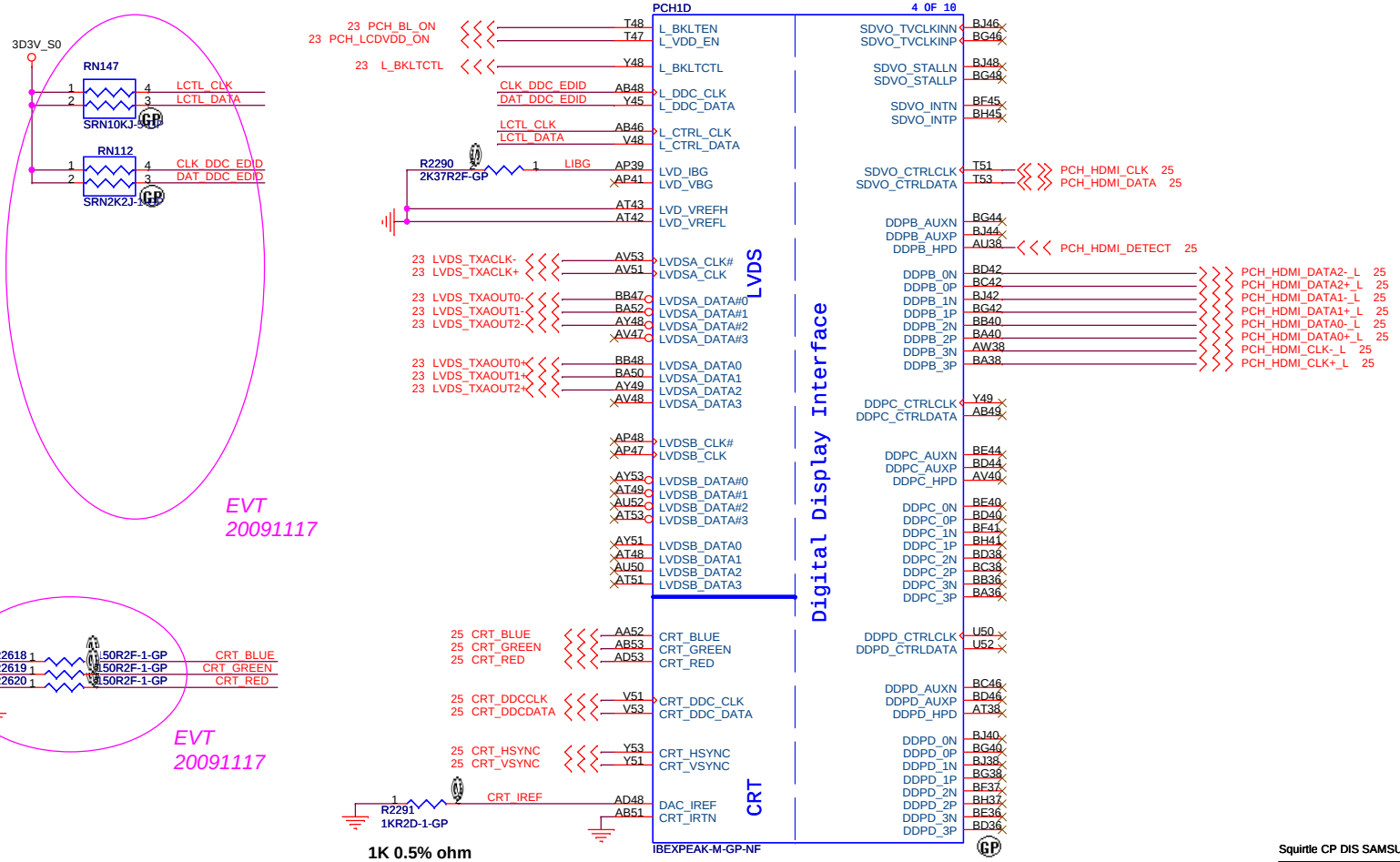
57

Panel backlight enable control for LVDS -
used to gate power into the backlight circuit



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Title: **PCH 4 of 9(LVDS/CRT/DP)**

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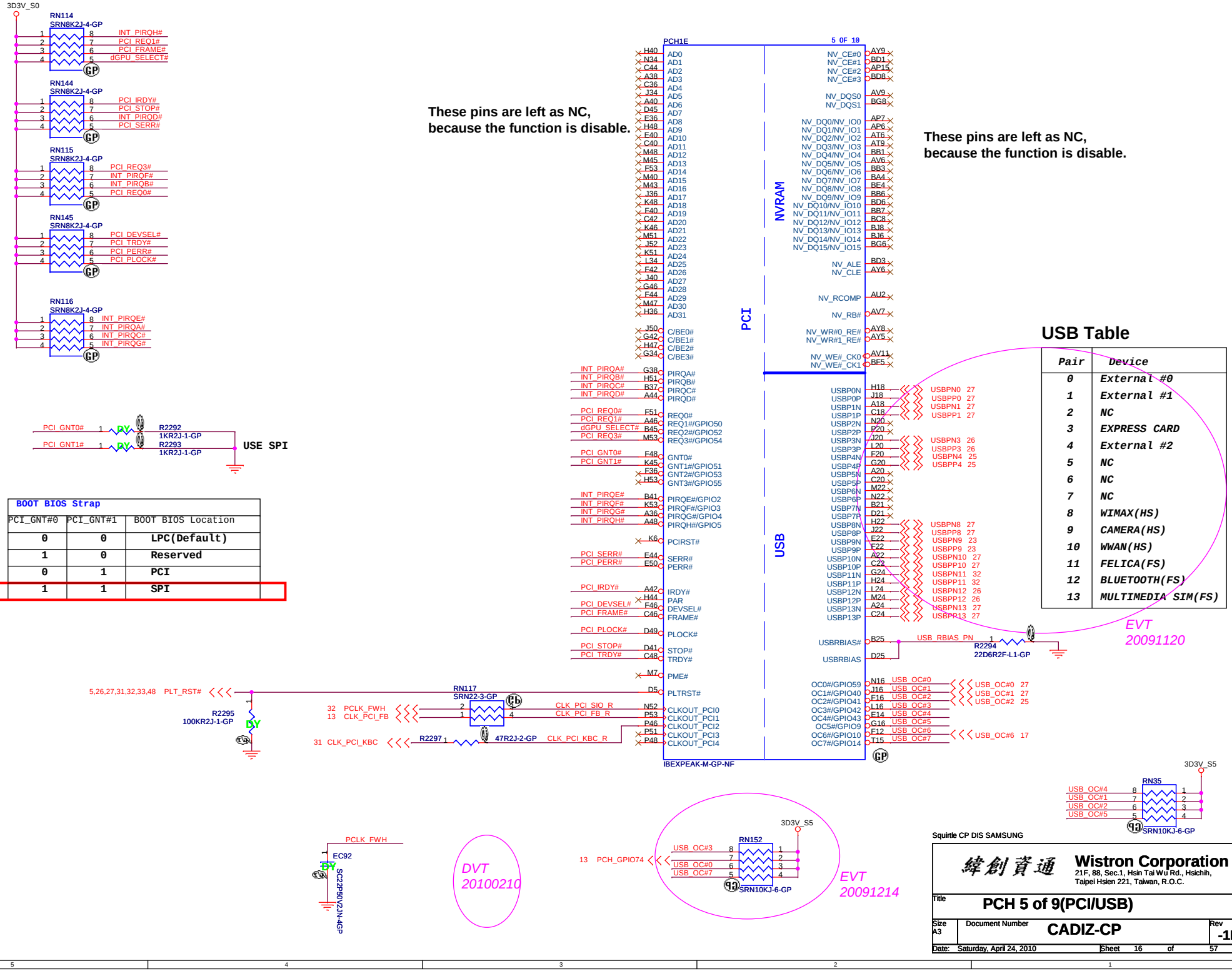
3D3V_S0
RN114
SRN8K2J-4-GP
INT_PIRQH#
PCI_REQ1#
PCI_FRAME#
dGPU_SELECT#
RN144
SRN8K2J-4-GP
PCI_IRDY#
PCI_STOP#
INT_PIRQD#
PCI_SERR#
RN115
SRN8K2J-4-GP
PCI_REQ3#
INT_PIRQF#
INT_PIRQB#
PCI_REQ0#
RN145
SRN8K2J-4-GP
PCI_DEVSEL#
PCI_TRDY#
PCI_PERR#
PCI_PLOCK#
RN116
SRN8K2J-4-GP
INT_PIRQE#
INT_PIRQA#
INT_PIRQC#
INT_PIRQG#
PCI_GNT0#
PCI_GNT1#
R2292
1KR2J-1-GP
R2293
1KR2J-1-GP
USE SPI
BOOT BIOS Strap
PCI_GNT#0 PCI_GNT#1 BOOT BIOS Location
0 0 LPC(Default)
1 0 Reserved
0 1 PCI
1 1 SPI
These pins are left as NC, because the function is disable.
PCH1E
5 OF 10
PCI
NVRAM
USB
IBEXPEAK-M-GP-NF
These pins are left as NC, because the function is disable.
USB Table
Pair Device
0 External #0
1 External #1
2 NC
3 EXPRESS CARD
4 External #2
5 NC
6 NC
7 NC
8 WIMAX(HS)
9 CAMERA(HS)
10 WWAN(HS)
11 FELICA(FS)
12 BLUETOOTH(FS)
13 MULTIMEDIA SIM(FS)
EVT 20091120
USB_RBIAS_PN
R2294
22D6R2F-L1-GP
RN117
SRN22-3-GP
R2295
100KR2J-1-GP
R2297
47R2J-2-GP
PLT_RST#
PCLK_FWH
CLK_PCI_KBC
CLK_PCI_SIO_R
CLK_PCI_FB_R
CLK_PCI_KBC_R
EC92
SC2259V2JN-4GP
DVT 20100210
RN152
SRN10KJ-6-GP
PCH_GPIO74
EVT 20091214
RN35
SRN10KJ-6-GP
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緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH 5 of 9(PCI/USB)
Size A3
Document Number
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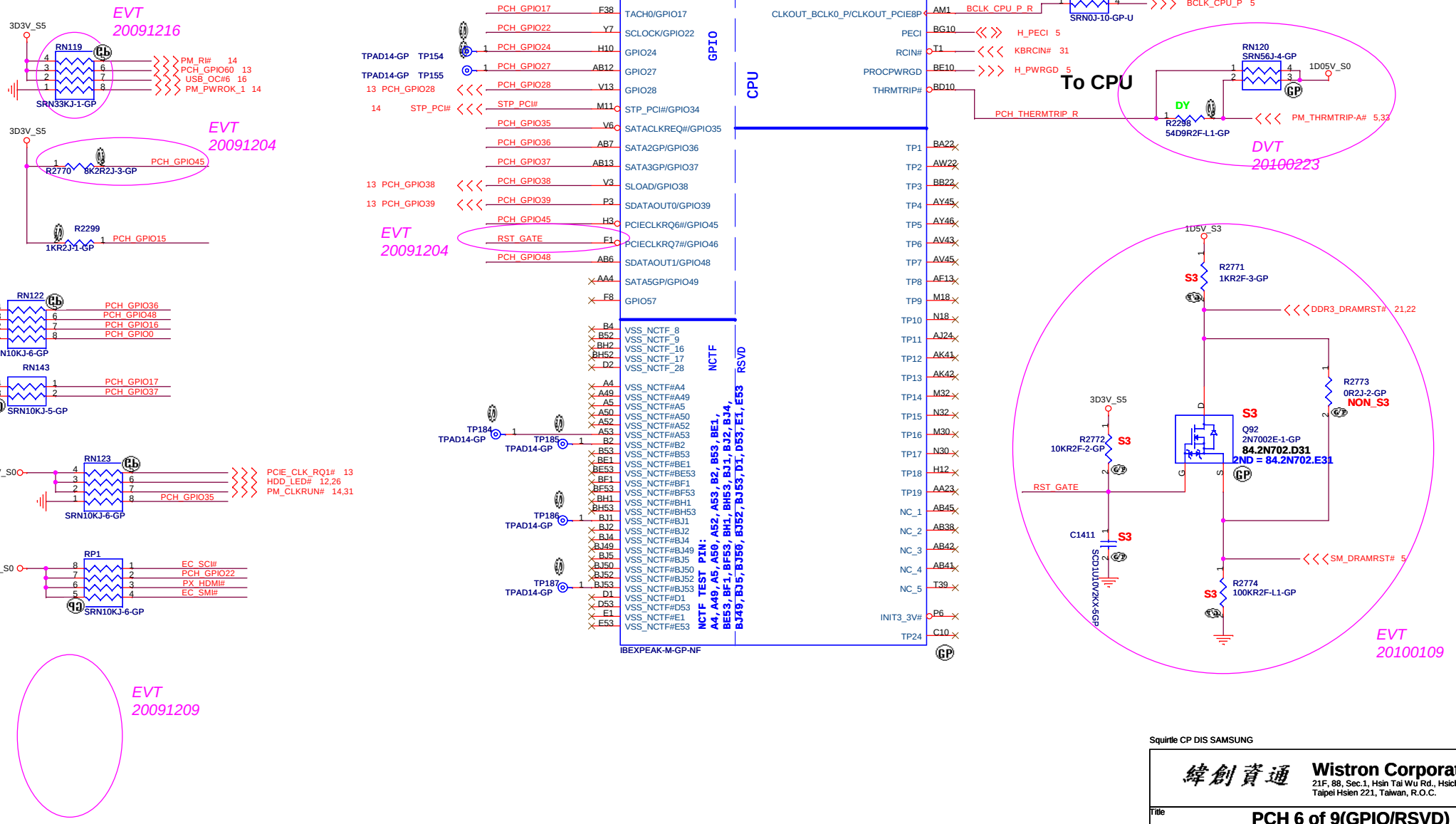
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



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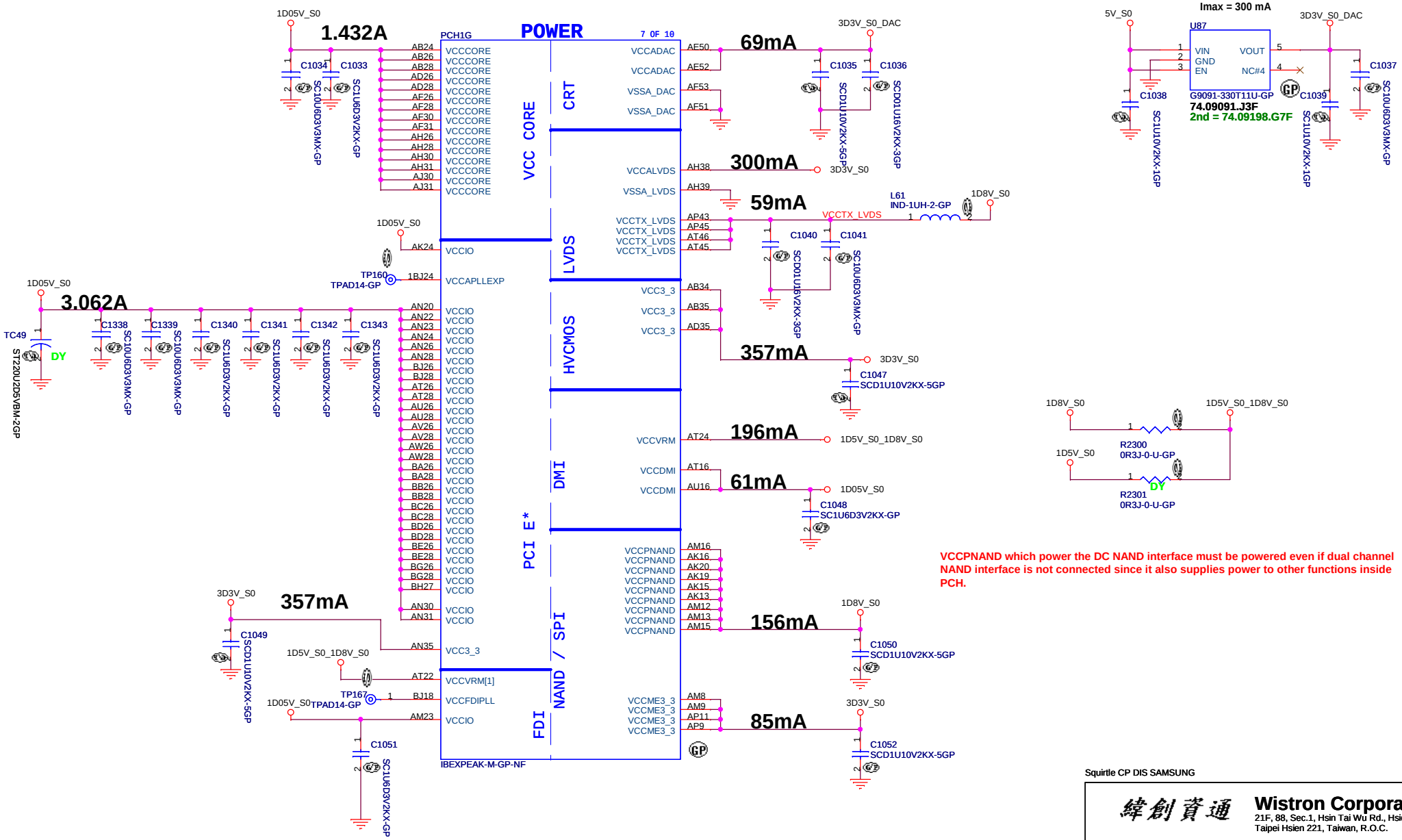
Title	PCH 6 of 9(GPIO/RSVD)	
Size A3	Document Number CADIZ-CP	Rev -1M
Date: Saturday, April 24, 2010	Sheet 17 of 57	

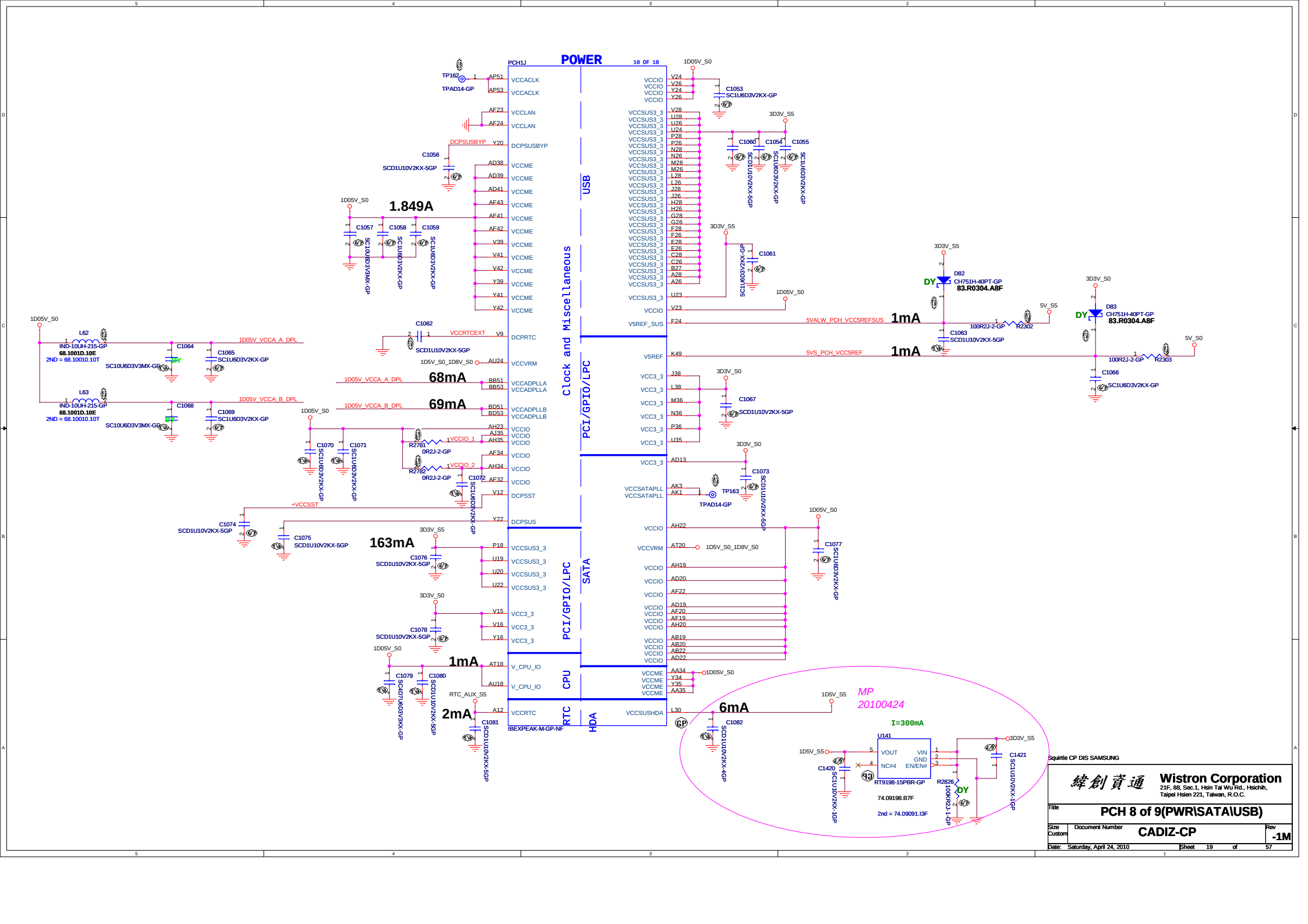


VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH 7 of 9(PWR/VCORE/LVDS)	
Size: Custom	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 18 of 57	


POWER
PCH1J
10 OF 10
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
1.849A
68mA
69mA
163mA
1mA
2mA
6mA
1mA
1mA
1D05V_S0
3D3V_S5
3D3V_S0
5V_S5
5V_S0
1D05V_VCCA_A_DPL
1D05V_VCCA_B_DPL
5VALW_PCH_VCC5REFSUS
5VS_PCH_VCC5REF
+VCCSST
RTC_AUX_S5
I=300mA
MP
20100424
Squirtle CP DIS SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH 8 of 9(PWR\SATA\USB)
Size
Custom
Document Number
CADIZ-CP
Rev
-1M
Date: Saturday, April 24, 2010
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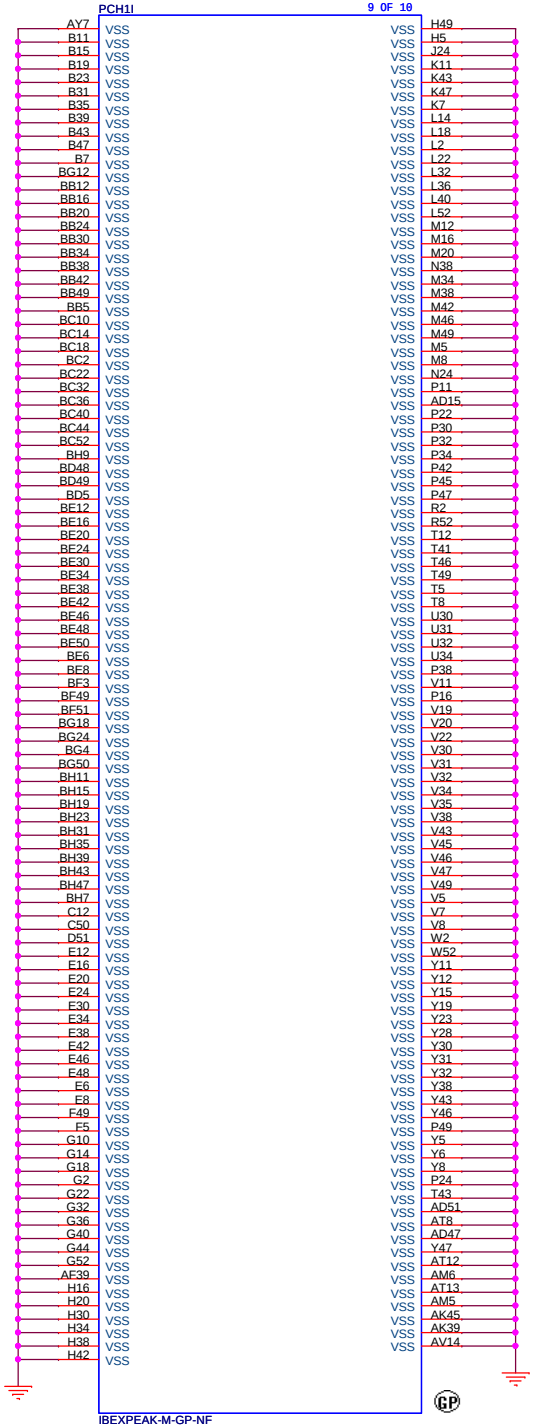

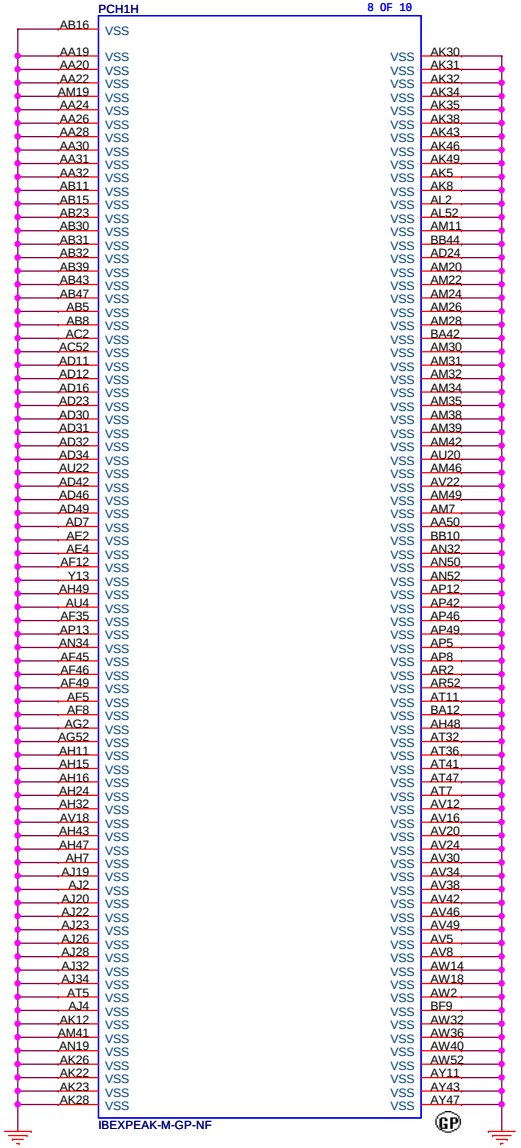

Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH 9 of 9(VSS)**

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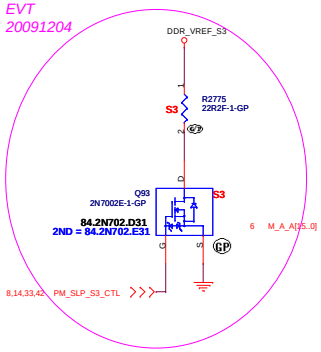
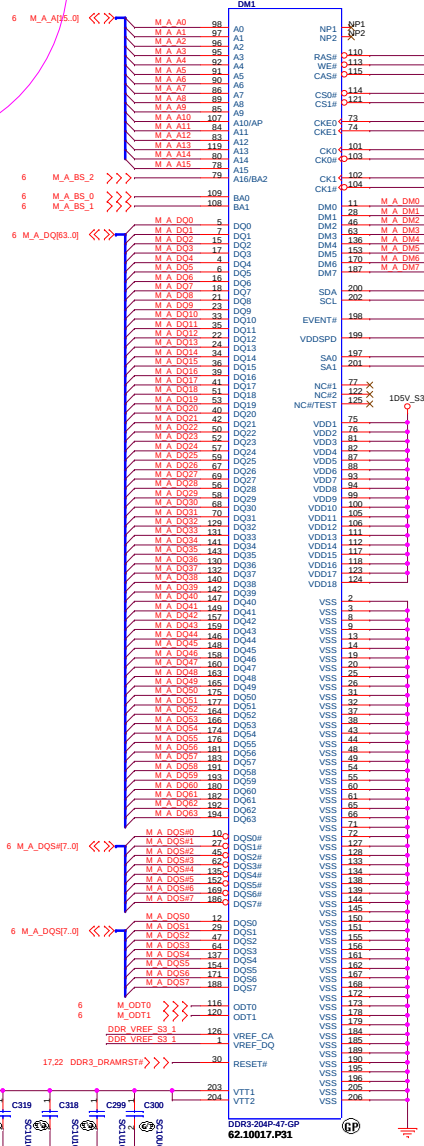
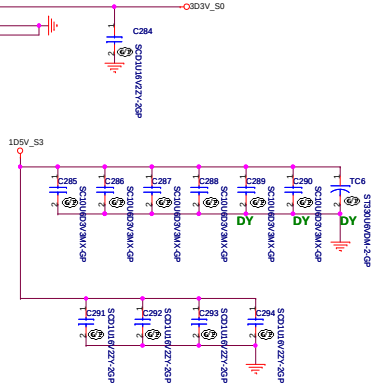
EVT
20091204

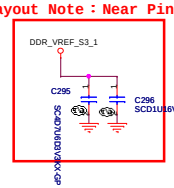
DDR3 SOCKET_1



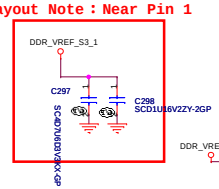


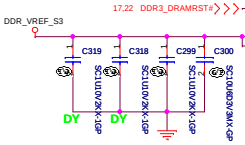


Layout Note：Near Pin 126



Layout Note：Near Pin 1





緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***DDR3 Socket1***
Size	Document Number: **CADIZ-CP** Rev: -1M
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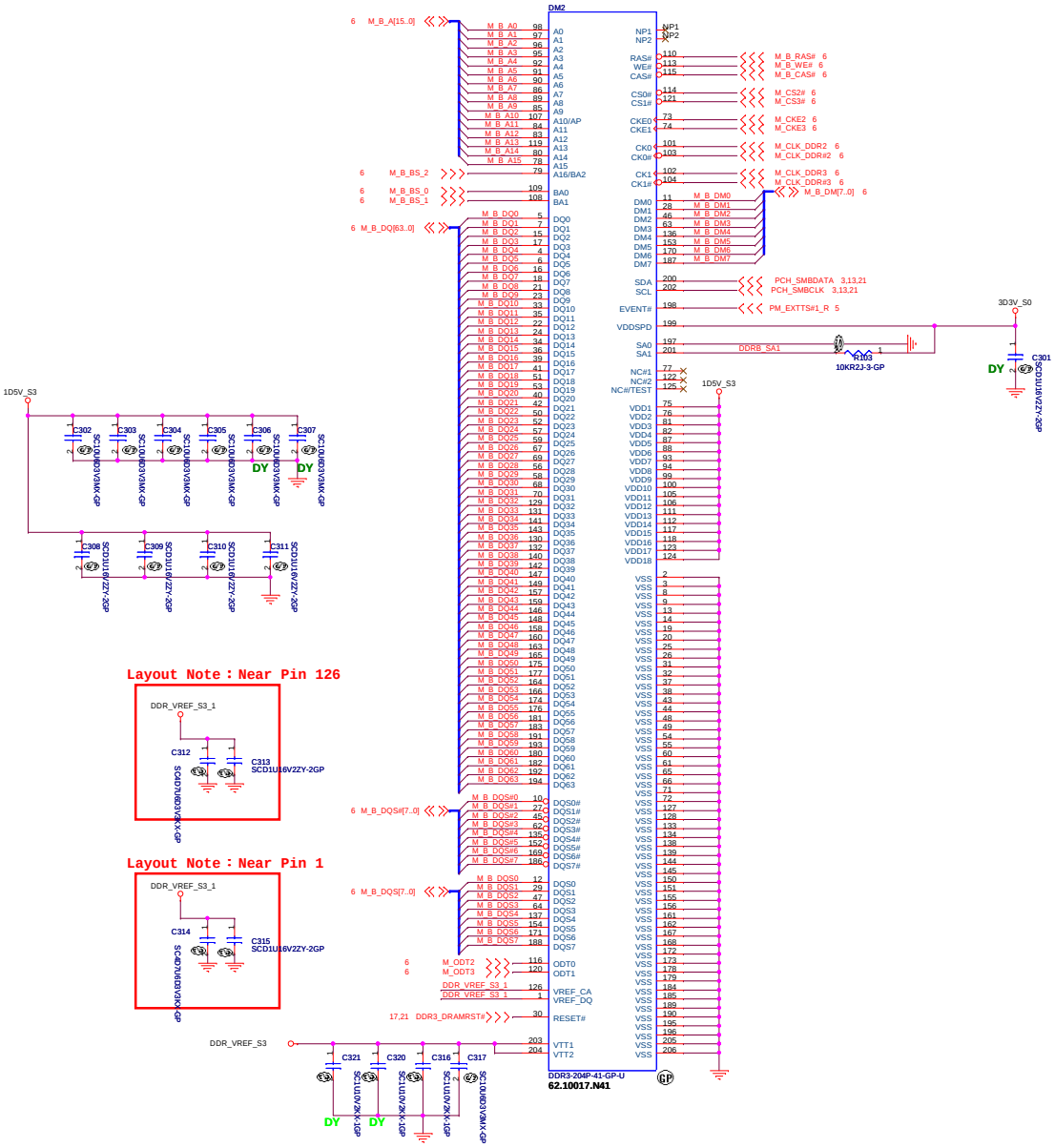
DDR3 SOCKET_2



Wistron Corporation	緯創資通
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Title: DDR3 Socket2	
Size	Document Number: CADIZ-CP
Rev: -1M	
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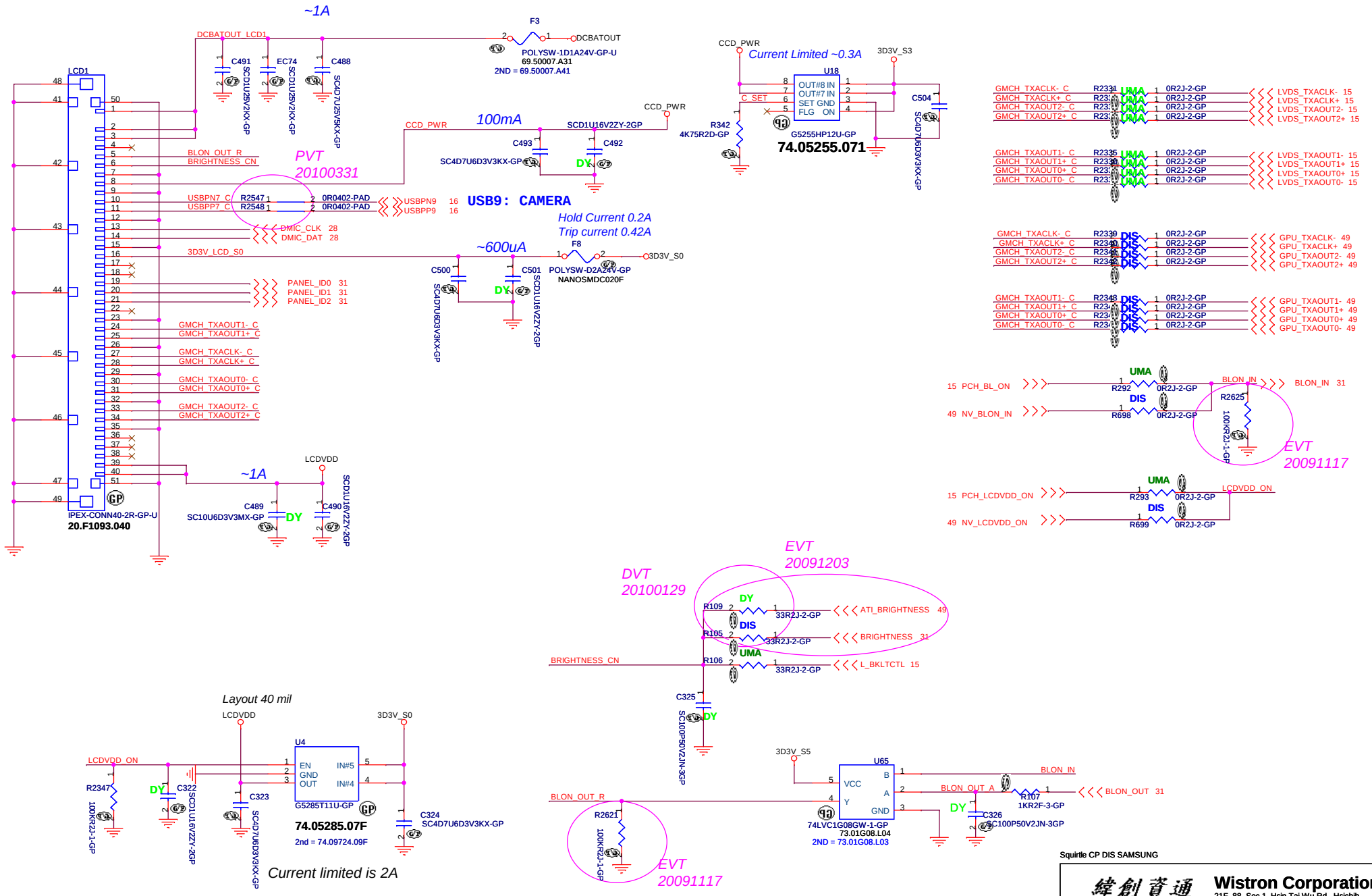
LCD/CCD CONN



Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD CONN	
Size	Document Number: CADIZ-CP	Rev: -1M
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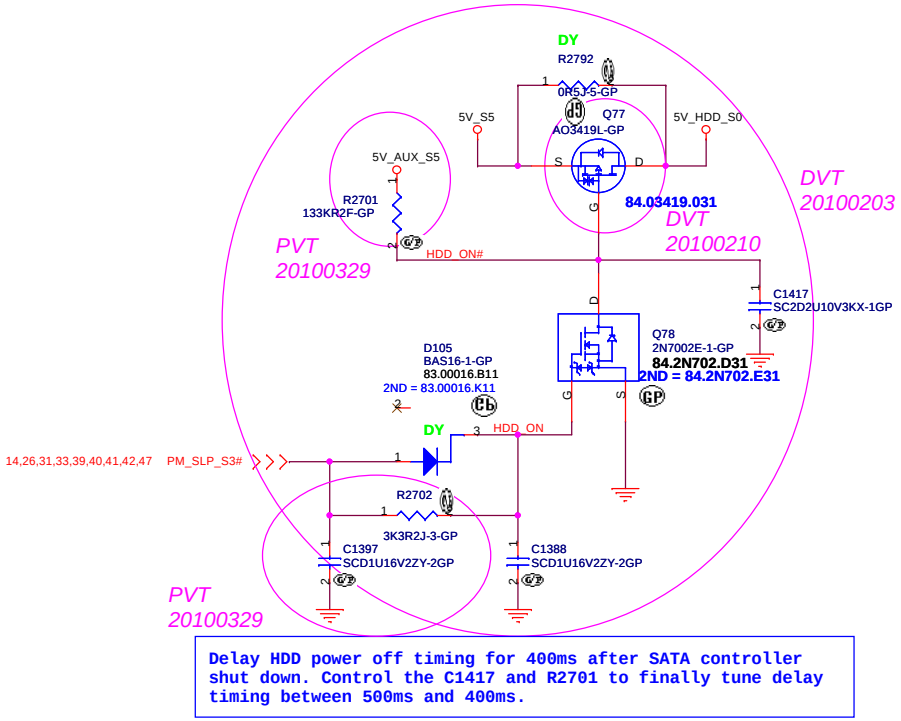
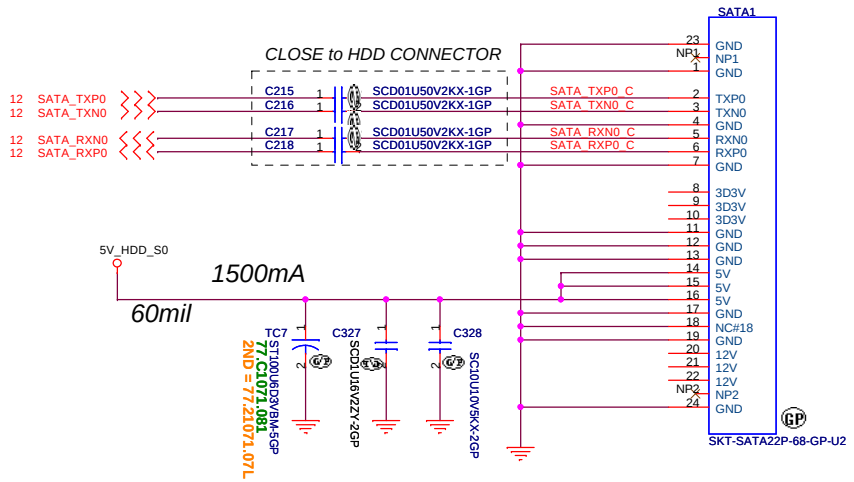
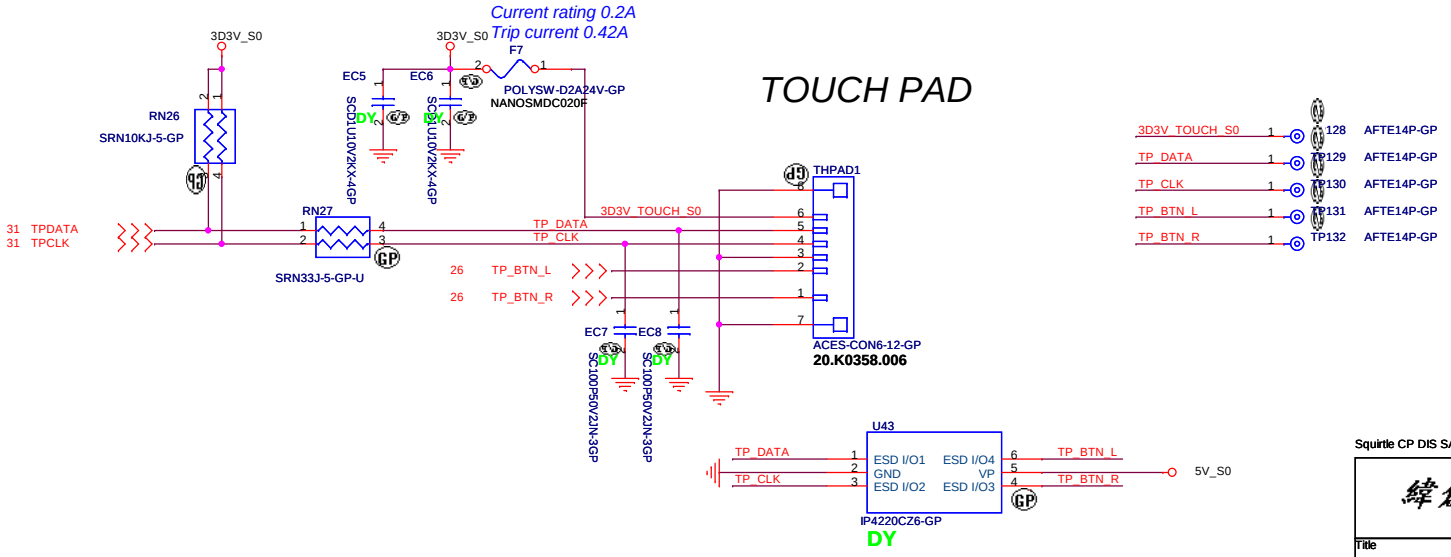


Delay HDD power off timing for 400ms after SATA controller shut down. Control the C1417 and R2701 to finally tune delay timing between 500ms and 400ms.

HDD Connector



TOUCH PAD



Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD CONN & TOUCHPAD**

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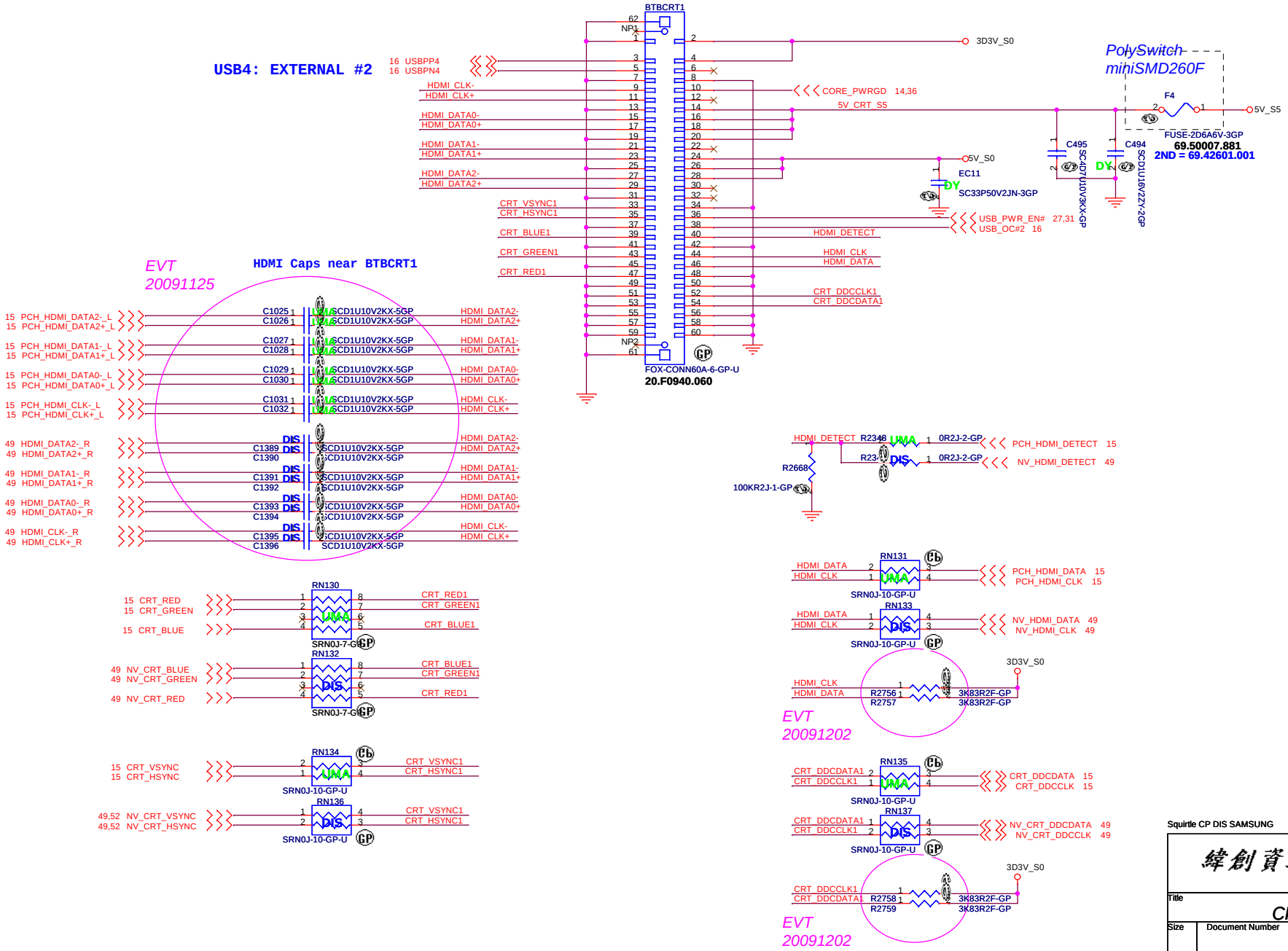
USB4: EXTERNAL #2
16 USBPP4
16 USBPN4
BTBCRT1
FOX-CONN60A-6-GP-U
20.F0940.060
3D3V_S0
5V_S0
5V_CRT_S5
5V_S5
CORE_PWRGD 14,36
HDMI_CLK-
HDMI_CLK+
HDMI_DATA0-
HDMI_DATA0+
HDMI_DATA1-
HDMI_DATA1+
HDMI_DATA2-
HDMI_DATA2+
CRT_VSYNC1
CRT_HSYNC1
CRT_BLUE1
CRT_GREEN1
CRT_RED1
HDMI_DETECT
HDMI_CLK
HDMI_DATA
CRT_DDCCLK1
CRT_DDCDATA1
USB_PWR_EN# 27,31
USB_OC#2 16
PolySwitch
miniSMD260F
F4
FUSE-2D6A6V-3GP
69.50007.881
2ND = 69.42601.001
C495
C494
EC11
SC33P50V2JN-3GP
SC4D7U10V3KX-GP
SC01U16V2ZY-2GP
EVT
20091125
HDMI Caps near BTBCRT1
SCD1U10V2KX-5GP
R2668
100KR2J-1-GP
R2348
R2349
0R2J-2-GP
PCH_HDMI_DETECT 15
NV_HDMI_DETECT 49
RN130
RN131
RN132
RN133
RN134
RN135
RN136
RN137
SRN0J-7-GP
SRN0J-10-GP-U
R2756
R2757
R2758
R2759
3K83R2F-GP
EVT
20091202
EVT
20091202
Squirtle CP DIS SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT BD CONN
Size
Document Number
CADIZ-CP
Rev
-1M
Date: Saturday, April 24, 2010
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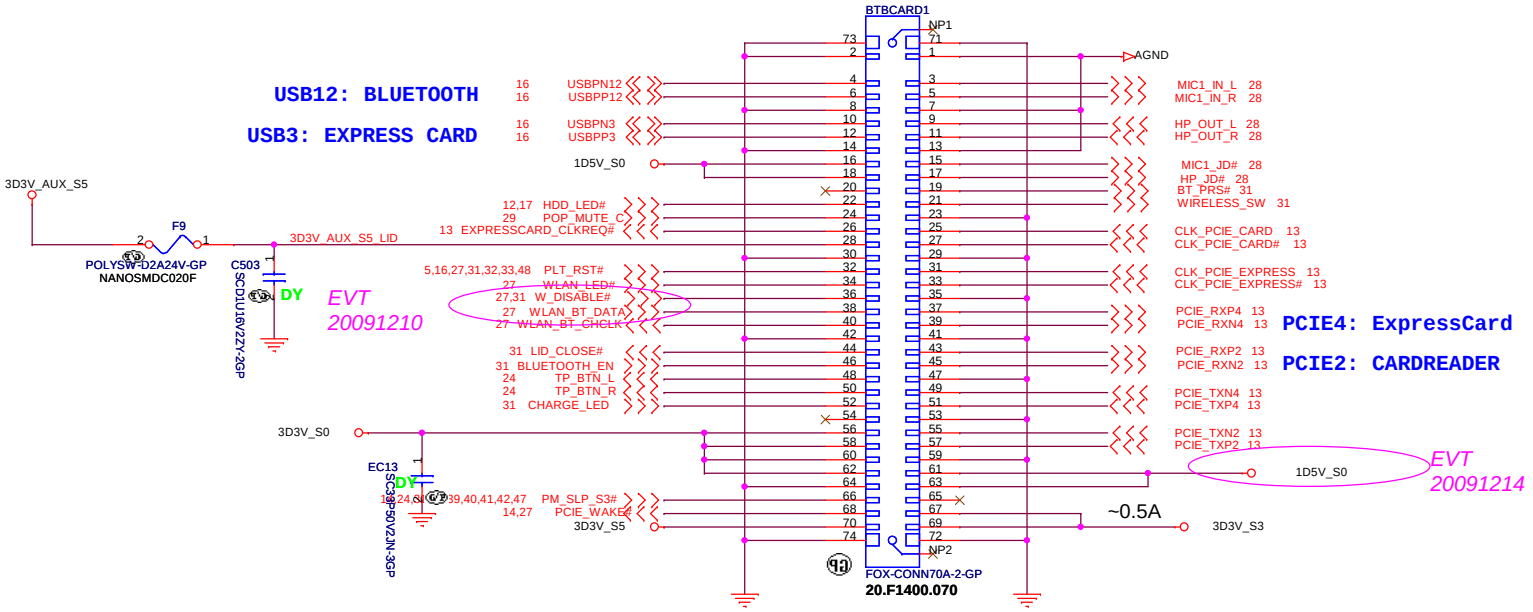

Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CARDREADER BD CONN		
Size	Document Number: CADIZ-CP	Rev: -1M
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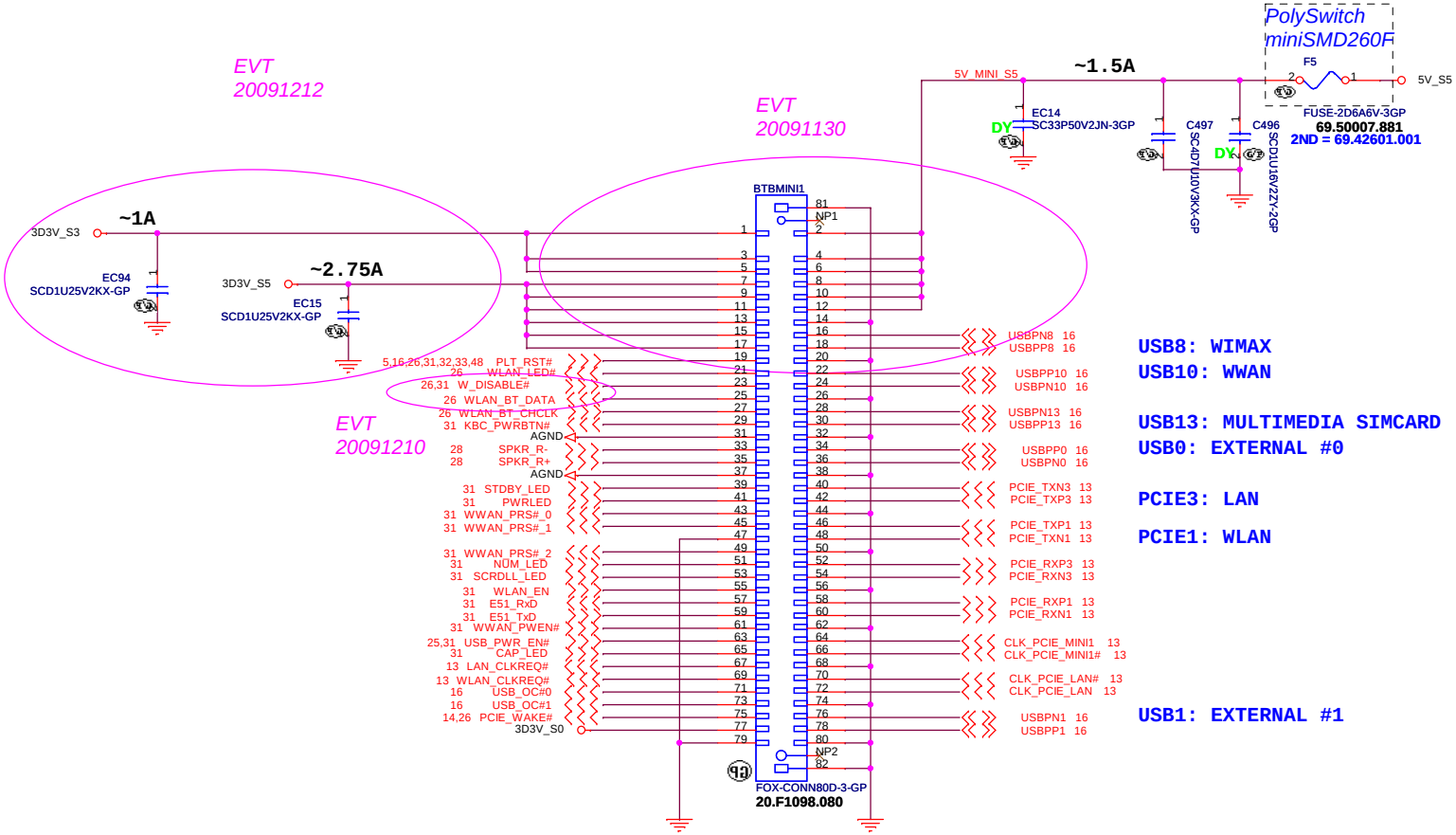

Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI BD CONN

Size	Document Number	Rev
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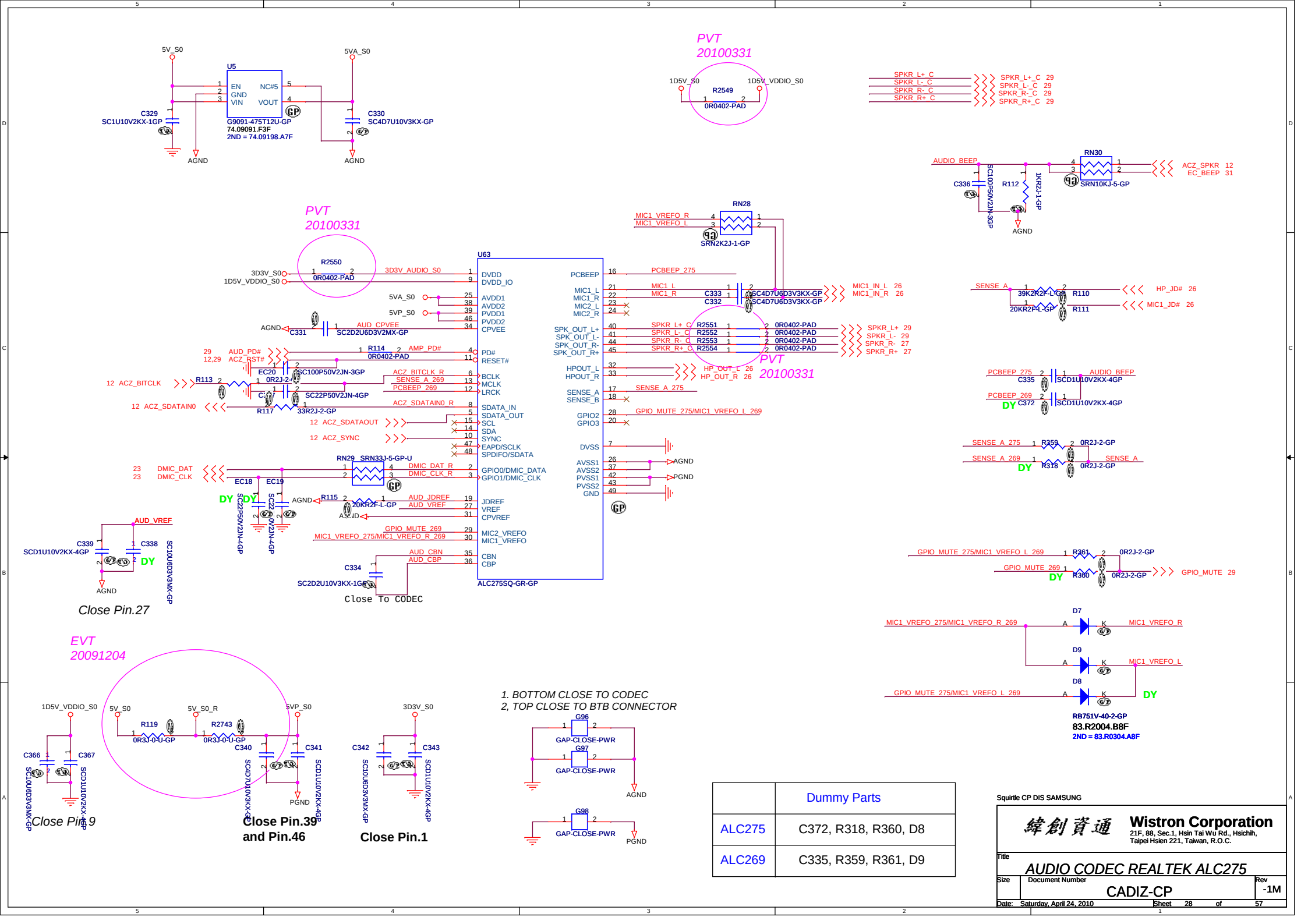

	Dummy Parts
ALC275	C372, R318, R360, D8
ALC269	C335, R359, R361, D9

Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO CODEC REALTEK ALC275*

Size	Document Number	Rev
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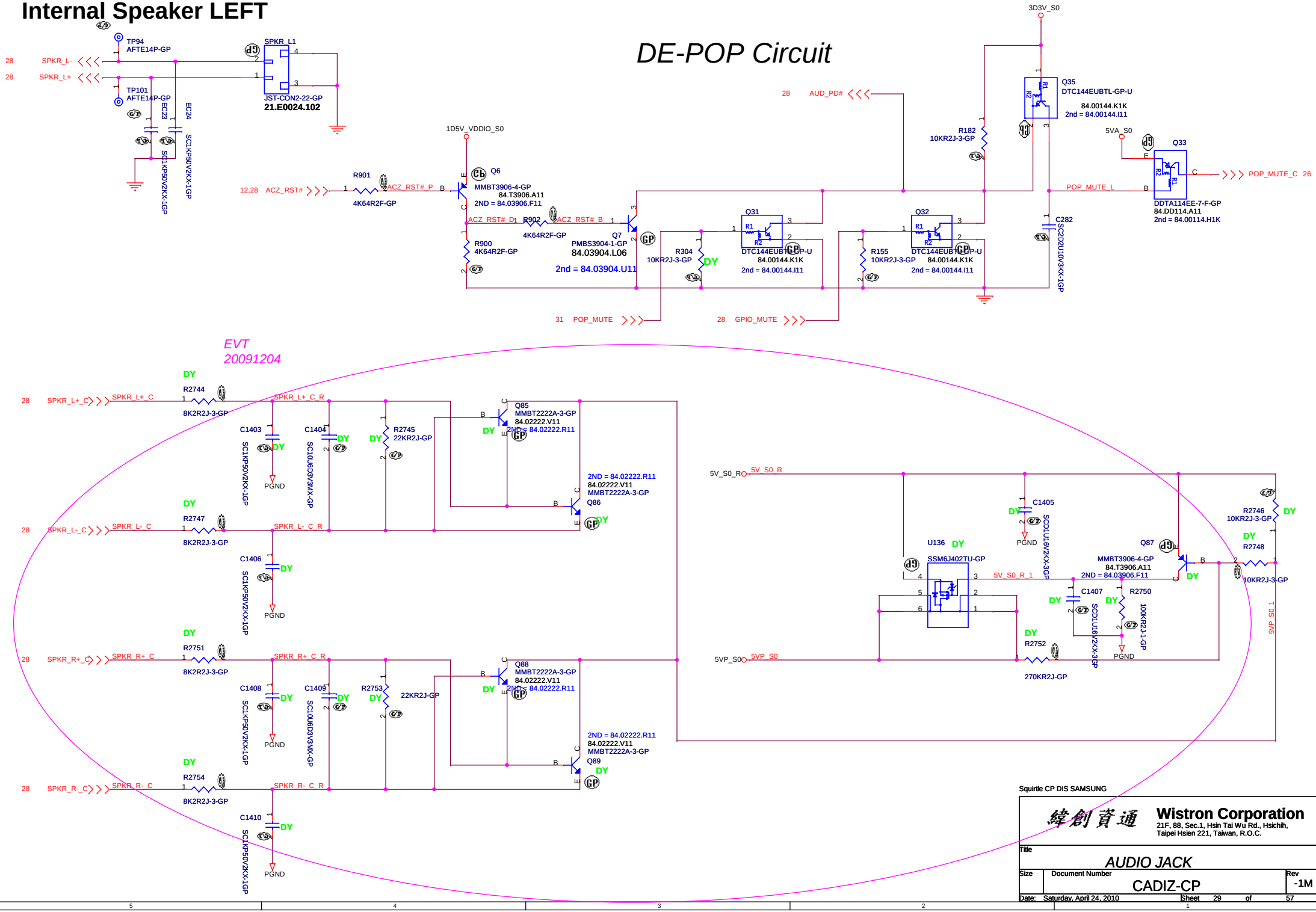
Internal Speaker LEFT



Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO JACK	
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for T8 thermal diode

84.03904.L06
2nd = 84.03904.U11
Q3 PMBS3904-1-GP
C118 SC2200P50V2KX-2GP
G787_DP2
G787_DN2

C1252 & C1254 CLOSE TO G787

for system thermal diode

84.03904.L06
2nd = 84.03904.U11
Q15 PMBS3904-1-GP
C346 SC2200P50V2KX-2GP
G787_DP1
G787_DN1

EVT
20091201

49 GPU_TEMP+ R2712 0R2J-2-GP G787_DN2
DIS

49 GPU_TEMP- R2713 0R2J-2-GP G787_DP2
DIS

5V_S0
R426 100R2J-2-GP
C533 SCD1U16V2KX-3GP
C147 SC10U6D3V3MX-GP DY

5V_S0_THERMAL

U15
VCC
THERM# PURE_HW_SHUTDOWN#
THERM_SET THERM_SET
DXP1 G787_DP1
DP2DN3 G787_DP2
DN2DP3 G787_DN2
ALERT# ALERT# R291 10KR2J-3-GP 3D3V_S0
SDA SMBD_THERM 31
SCL SMBC_THERM 31
TEST TPAD14-GP TP49 TP28
SGND1 G787_DN1
NC#8 NC#9 NC#12 NC#15
GND GND
G787R41U-GP
74.00787.0B3

R429 21KR2F-GP
R430 49K9R2F-L-GP

T8=90C
THERM_SET = [(Tset-72) x 0.02+0.34] x VCC

5V_FAN_S0
C344 SC4D7U10V3KX-GP
C345 SCD1U16V2ZY-2GP

5V_FAN_S0 136 AFTE14P-GP
FAN_PWM TP137 AFTE14P-GP
FAN_TACH 138 AFTE14P-GP
FAN_PRS# TP139 AFTE14P-GP

ps. FAN1 POWER TRACE WIDTH ~15 MIL
Max current is 235mA;
Stopped is ~10mA

31 FAN_PWM1 R358 0R2J-2-GP
SCD1U16V2ZY-2GP DY EC9 FAN_PWM

FAN1
FAN_PWM
FAN_TACH
31 FAN_PRS#
EC81 SC220P50V2JN-3GP
EC35 SC220P50V2JN-3GP
MLX-CON5-12-GP
20.F0693.005

5V_S0
R350 DY 0R2J-2-GP
R355 10KR2J-3-GP
D23 RB551V30-GP
31 FAN_TACH1 FAN_TACH
83.R5003.H8H
2ND = 83.5R003.08F

5V_S0 5V_FAN_S0
Q47 AO3413-GP
84.03413.A31
2nd = 84.02130.031
R73 100KR2J-1-GP
FAN_OFF
Q13 2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
31 FAN_OFF#

3D3V_S0
R125 10KR2J-3-GP
PURE_HW_SHUTDOWN#
Q4 2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
RSMRST# 31,33

Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor
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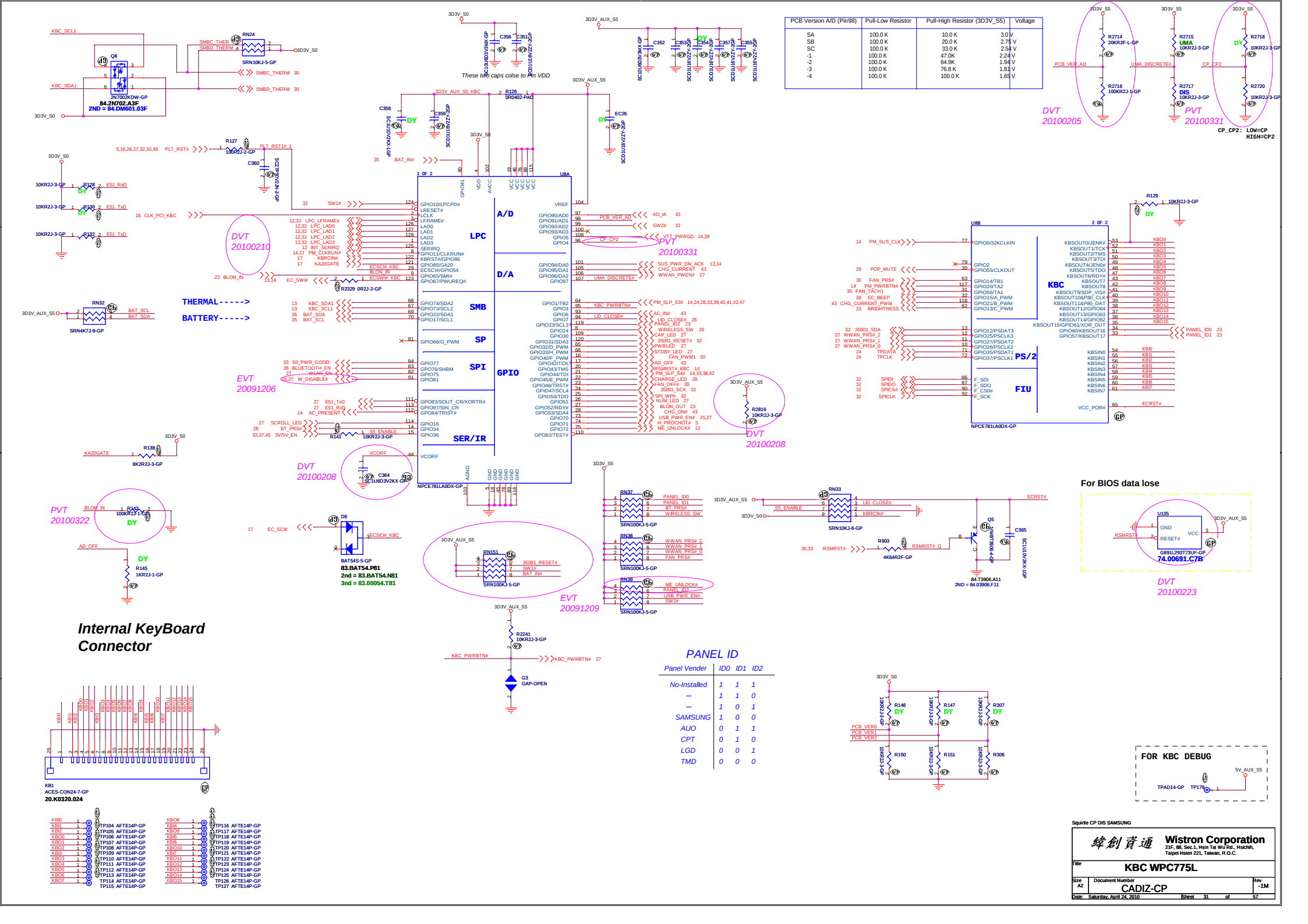
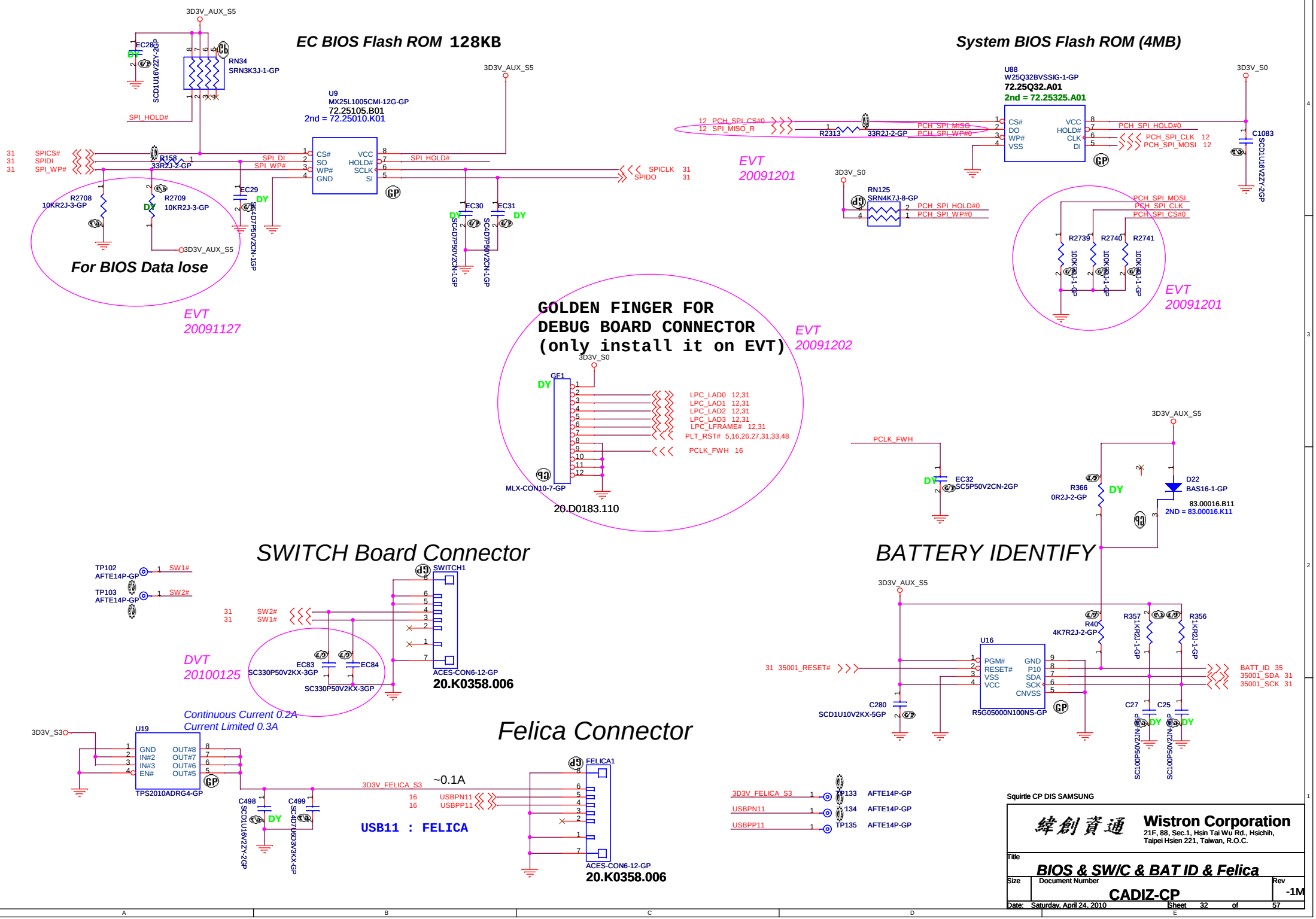
Date: Saturday, April 24, 2010 Sheet 30 of 57


PCB Version A/D (Pin98) | Pull-Low Resistor | Pull-High Resistor (3D3V_S5) | Voltage
SA 100.0 K 10.0 K 3.0 V
SB 100.0 K 20.0 K 2.75 V
SC 100.0 K 33.0 K 2.54 V
-1 100.0 K 47.0K 2.24 V
-2 100.0 K 64.9K 1.94 V
-3 100.0 K 76.8 K 1.81 V
-4 100.0 K 100.0 K 1.65 V
These two caps colse to Pin VDD
DVT 20100205
PVT 20100331
CP_CP2: LOW=CP HIGH=CP2
DVT 20100210
PVT 20100331
EVT 20091206
DVT 20100208
DVT 20100208
PVT 20100322
EVT 20091209
DVT 20100208
DVT 20100223
For BIOS data lose
THERMAL - - - - - >
BATTERY - - - - - >
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
U8A
NPCE781LA0DX-GP
U8B
KBC
PS/2
FIU
NPCE781LA0DX-GP
Internal KeyBoard Connector
KB1
ACES-CON24-7-GP
20.K0320.024
PANEL ID
Panel Vender | ID0 | ID1 | ID2
No-Installed 1 1 1
— 1 1 0
— 1 0 1
SAMSUNG 1 0 0
AUO 0 1 1
CPT 0 1 0
LGD 0 0 1
TMD 0 0 0
FOR KBC DEBUG
Squirtle CP DIS SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775L
CADIZ-CP
Saturday, April 24, 2010


EC BIOS Flash ROM 128KB
3D3V_AUX_S5
RN34
SRN3K3J-1-GP
SCD1U16V2ZY-2GP
SPI_HOLD#
U9
MX25L1005CMI-12G-GP
72.25105.B01
2nd = 72.25010.K01
31 SPICS#
31 SPIDI
31 SPI_WP#
R158
33R2J-2-GP
SPI_DI
SPI_WP#
CS#
SO
WP#
GND
VCC
HOLD#
SCLK
SI
SPI_HOLD#
SPICLK 31
SPIDO 31
R2708
10KR2J-3-GP
R2709
10KR2J-3-GP
EC29
SC4D7P50V2CN-1GP
EC30
EC31
For BIOS Data lose
EVT
20091127
System BIOS Flash ROM (4MB)
U88
W25Q32BVSSIG-1-GP
72.25Q32.A01
2nd = 72.25325.A01
3D3V_S0
12 PCH_SPI_CS#0
12 SPI_MISO_R
R2313
33R2J-2-GP
PCH_SPI_MISO
PCH_SPI_WP#0
CS#
DO
WP#
VSS
VCC
HOLD#
CLK
DI
PCH_SPI_HOLD#0
PCH_SPI_CLK 12
PCH_SPI_MOSI 12
C1083
SCD1U16V2ZY-2GP
EVT
20091201
RN125
SRN4K7J-8-GP
PCH_SPI_HOLD#0
PCH_SPI_WP#0
PCH_SPI_MOSI
PCH_SPI_CLK
PCH_SPI_CS#0
R2739
R2740
R2741
100KR2J-1-GP
EVT
20091201
GOLDEN FINGER FOR
DEBUG BOARD CONNECTOR
(only install it on EVT)
EVT
20091202
GF1
MLX-CON10-7-GP
LPC_LAD0 12,31
LPC_LAD1 12,31
LPC_LAD2 12,31
LPC_LAD3 12,31
LPC_LFRAME# 12,31
PLT_RST# 5,16,26,27,31,33,48
PCLK_FWH 16
20.D0183.110
PCLK_FWH
EC32
SC5P50V2CN-2GP
R366
0R2J-2-GP
D22
BAS16-1-GP
83.00016.B11
2ND = 83.00016.K11
SWITCH Board Connector
TP102
AFTE14P-GP
TP103
AFTE14P-GP
SW1#
SW2#
SWITCH1
ACES-CON6-12-GP
20.K0358.006
EC83
EC84
SC330P50V2KX-3GP
DVT
20100125
Continuous Current 0.2A
Current Limited 0.3A
BATTERY IDENTIFY
R40
4K7R2J-2-GP
R357
2KR2J-1-GP
R356
2KR2J-1-GP
U16
R5G05000N100NS-GP
PGM#
RESET#
VSS
VCC
GND
P10
SDA
SCK
CNVSS
35001_RESET#
BATT_ID 35
35001_SDA 31
35001_SCK 31
C280
SCD1U10V2KX-5GP
C27
C25
SC100P50V2JN-2GP
Felica Connector
3D3V_S3
U19
TPS2010ADRG4-GP
GND
IN#2
IN#3
EN#
OUT#8
OUT#7
OUT#6
OUT#5
C498
C499
SCD1U16V2ZY-2GP
SC47D1P50V3KX-GP
3D3V_FELICA_S3
~0.1A
USBPN11
USBPP11
USB11 : FELICA
FELICA1
ACES-CON6-12-GP
20.K0358.006
TP133
TP134
TP135
AFTE14P-GP
Squirtle CP DIS SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BIOS & SW/C & BAT ID & Felica
Size
Document Number
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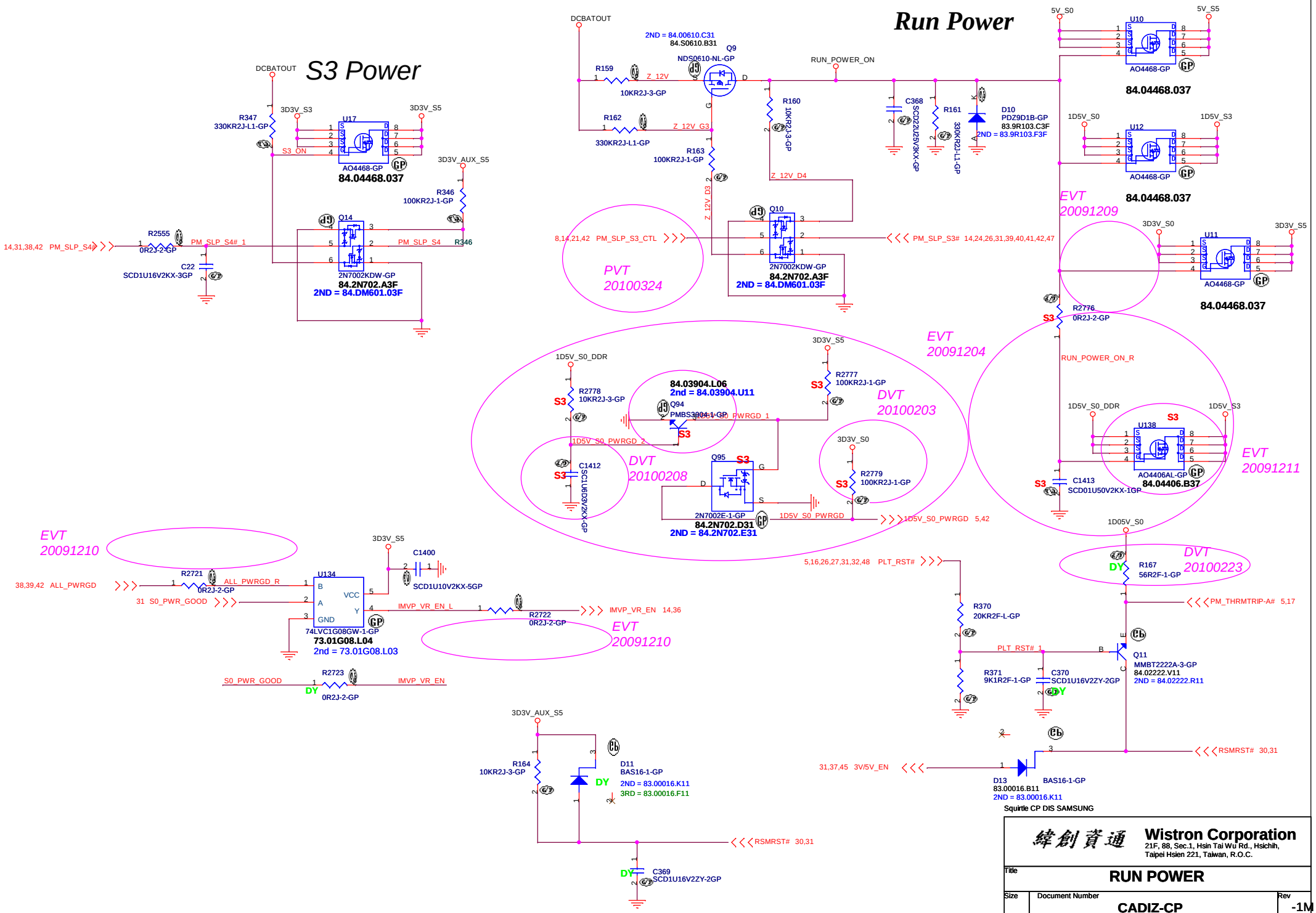
S3 Power
Run Power
DCBATOUT
R347
330KR2J-L1-GP
3D3V_S3
U17
AO4468-GP
84.04468.037
3D3V_S5
S3_ON
3D3V_AUX_S5
R346
100KR2J-1-GP
Q14
R2555
0R2J-2-GP
14,31,38,42 PM_SLP_S4#
PM_SLP_S4# 1
PM_SLP_S4
C22
SCD1U16V2KX-3GP
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
2ND = 84.00610.C31
84.S0610.B31
Q9
NDS0610-NL-GP
RUN_POWER_ON
R159
10KR2J-3-GP
Z_12V
R162
330KR2J-L1-GP
Z_12V_G3
R163
100KR2J-1-GP
R160
10KR2J-3-GP
C368
SCD22U25V3KX-GP
R161
330KR2J-L1-GP
D10
PDZ9D1B-GP
83.9R103.C3F
2ND = 83.9R103.F3F
Z_12V_D4
Z_12V_D3
Q10
8,14,21,42 PM_SLP_S3_CTL
PM_SLP_S3# 14,24,26,31,39,40,41,42,47
PVT
20100324
5V_S0
5V_S5
U10
AO4468-GP
84.04468.037
1D5V_S0
1D5V_S3
U12
AO4468-GP
84.04468.037
EVT
20091209
3D3V_S0
3D3V_S5
U11
AO4468-GP
84.04468.037
R2776
0R2J-2-GP
S3
RUN_POWER_ON_R
EVT
20091204
1D5V_S0_DDR
R2778
10KR2J-3-GP
84.03904.L06
2nd = 84.03904.U11
Q94
PMBS3904-1-GP
1D5V_S0_PWRGD_1
1D5V_S0_PWRGD_2
C1412
SC1U6D3V2KX-GP
DVT
20100208
3D3V_S5
R2777
100KR2J-1-GP
DVT
20100203
Q95
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
3D3V_S0
R2779
100KR2J-1-GP
1D5V_S0_PWRGD
1D5V_S0_PWRGD 5,42
1D5V_S0_DDR
1D5V_S3
U138
AO4406AL-GP
84.04406.B37
C1413
SCD01U50V2KX-1GP
EVT
20091211
EVT
20091210
38,39,42 ALL_PWRGD
R2721
0R2J-2-GP
ALL_PWRGD_R
31 S0_PWR_GOOD
U134
74LVC1G08GW-1-GP
73.01G08.L04
2nd = 73.01G08.L03
3D3V_S5
C1400
SCD1U10V2KX-5GP
IMVP_VR_EN_L
R2722
0R2J-2-GP
IMVP_VR_EN 14,36
EVT
20091210
S0_PWR_GOOD
R2723
DY
0R2J-2-GP
IMVP_VR_EN
1D05V_S0
DVT
20100223
R167
56R2F-1-GP
PM_THRMTRIP-A# 5,17
5,16,26,27,31,32,48 PLT_RST#
R370
20KR2F-L-GP
PLT_RST# 1
R371
9K1R2F-1-GP
C370
SCD1U16V2ZY-2GP
Q11
MMBT2222A-3-GP
84.02222.V11
2ND = 84.02222.R11
RSMRST# 30,31
31,37,45 3V/5V_EN
D13
BAS16-1-GP
83.00016.B11
2ND = 83.00016.K11
3D3V_AUX_S5
R164
10KR2J-3-GP
D11
BAS16-1-GP
2ND = 83.00016.K11
3RD = 83.00016.F11
RSMRST# 30,31
C369
SCD1U16V2ZY-2GP
Squirtle CP DIS SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RUN POWER
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CPU_CORE
ADP3211

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6261A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

Output Power
VCC_CORE_PWR(O)

VR_PWROK
VCC_CORE(Imax=27A)

RT8209 1D05V_S0

DCBATOUT_8202_1D05V
ALL_PWRGD

VIN
EN
1D5V(O)
PGOOD

1D05V_S0 (20A)
CPUCORE_ON

RT8209 1D5V_S3

DCBATOUT_8202_1D5V
PM_SLP_S4#

VIN
EN
1D5V(O)
PGOOD

1D5V_S3 (13.5A)
S3_PWRGD

GFX_CORE/ VGA_CORE
ADP3211

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT_3211

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

Output Power
VGFXCORE (O)

CPUCORE_ON
VCC_GFXCORE(11A)
+VGA_CORE(11A)

RT9026 0D75V_S0

5V_S5
1D5V_S3
PM_SLP_S3#
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D75V_S3 (1.2A)
0D75V_S3_1

APL5930 1V_VGA

5V_S5
1D5V_S3
VGACORE_PWROK

VIN
VLDOIN
EN
VTT
PGOOD

1V_VGA (2.5A)
1V_VGA_PWRGD

5V/3D3V
RT8223

DCBATOUT_51123
S5_ENABLE
ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (5A)
5V_AUX_S5
3D3V_AUX_S5

Charger BQ24751

CHG_ON#
AD+

Input Signal
CHGEN#

Input Power
ACDET

Output Signal
ACGOOD#
SRSET
BAT

Output Power
VOUT (O)
VOUT (O)

AC_IN#
CHG_CURRENT
BATT_SENSE
BT+
DCBATOUT

G9661 1D8V_VGA

5V_S5
3D3V_S5
1V_VGA_PWRGD

VIN
VLDOIN
EN
VTT
PGOOD

1D8V_VGA (1.3A)
9025_PGOO_1.8V

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence Logic

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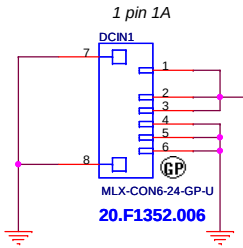
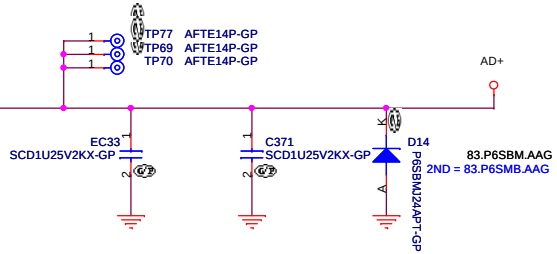
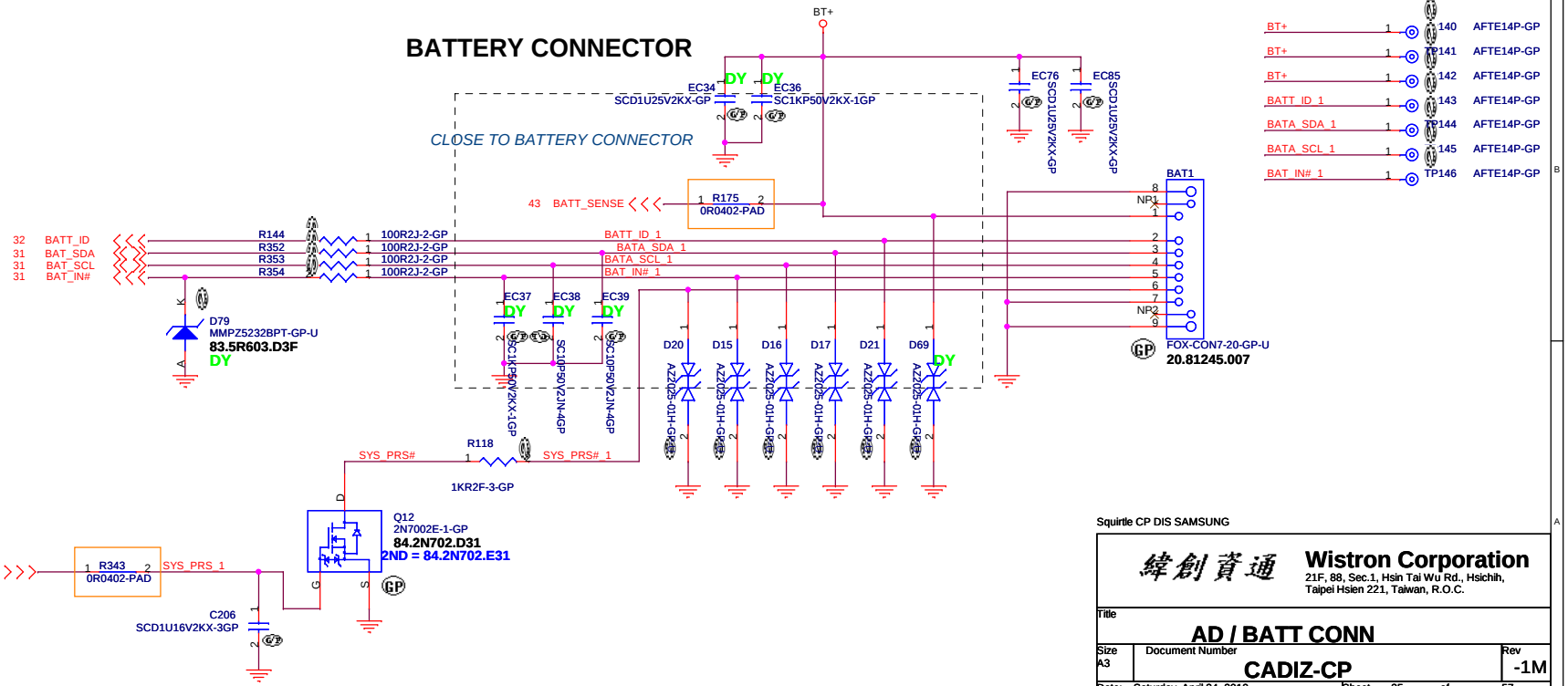
DC IN Connector



Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AD / BATT CONN		
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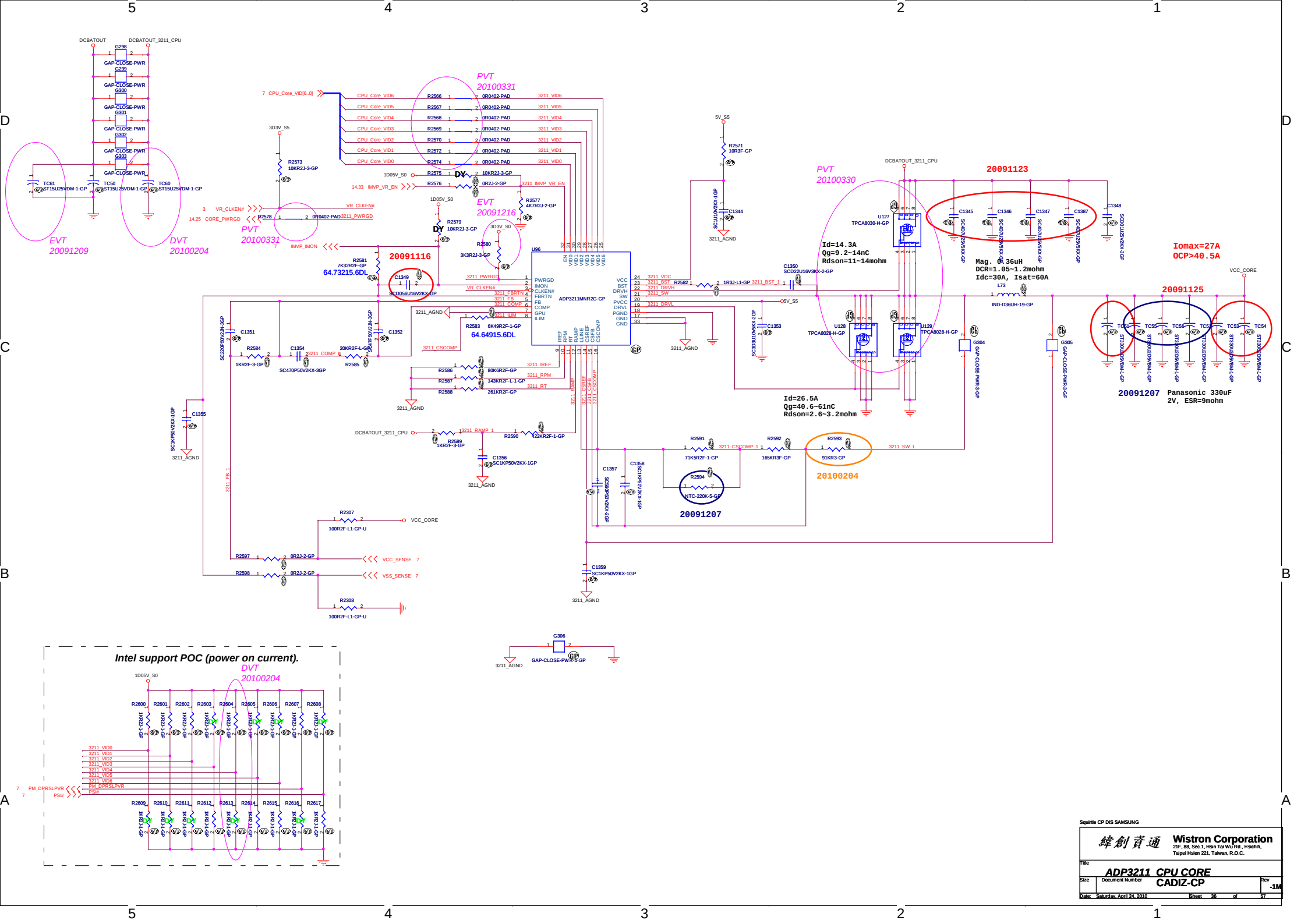

Squirtle CP DIS SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP3211 CPU CORE

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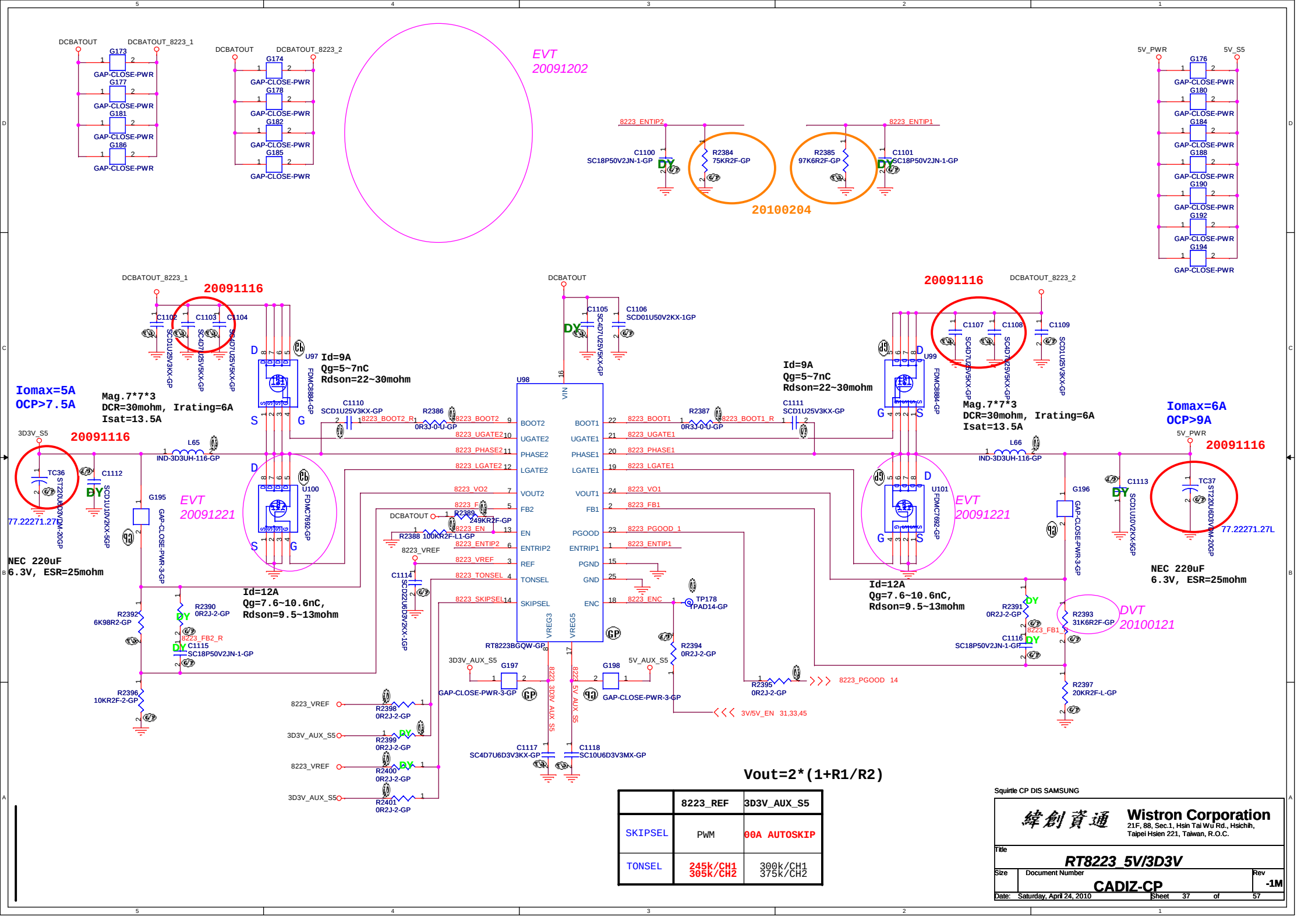
DCBATOUT
DCBATOUT_8223_1
G173
G177
G181
G186
GAP-CLOSE-PWR
DCBATOUT_8223_2
G174
G178
G182
G185
EVT
20091202
8223_ENTIP2
C1100
SC18P50V2JN-1-GP
R2384
75KR2F-GP
R2385
97K6R2F-GP
C1101
8223_ENTIP1
20100204
5V_PWR
5V_S5
G176
G180
G184
G188
G190
G192
G194
20091116
Iomax=5A
OCP>7.5A
Mag.7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=9A
Qg=5~7nC
Rdson=22~30mohm
U97
FDMC8884-GP
U99
C1102
C1103
C1104
SCD1U25V3KX-GP
SC4D7U25V5KX-GP
C1105
C1106
SCD01U50V2KX-1GP
C1107
C1108
C1109
3D3V_S5
L65
IND-3D3UH-116-GP
L66
TC36
ST220U6D3VDM-20GP
77.22271.27L
C1112
SCD1U10V2KX-5GP
G195
GAP-CLOSE-PWR-3-GP
NEC 220uF
6.3V, ESR=25mohm
U98
RT8223BGQW-GP
VIN
BOOT2
UGATE2
PHASE2
LGATE2
VOUT2
FB2
EN
ENTRIP2
REF
TONSEL
SKIPSEL
VREG3
BOOT1
UGATE1
PHASE1
LGATE1
VOUT1
FB1
PGOOD
ENTRIP1
PGND
GND
ENC
VREG5
C1110
R2386
0R3J-0-U-GP
R2387
C1111
8223_BOOT2
8223_UGATE2
8223_PHASE2
8223_LGATE2
8223_VO2
8223_FB2
8223_EN
8223_ENTIP2
8223_VREF
8223_TONSEL
8223_SKIPSEL
8223_BOOT1
8223_UGATE1
8223_PHASE1
8223_LGATE1
8223_VO1
8223_FB1
8223_PGOOD_1
8223_ENTIP1
8223_ENC
U100
U101
FDMC7692-GP
EVT
20091221
R2389
249KR2F-GP
R2388
100KR2F-L1-GP
C1114
SCD22U6D3V2KX-1GP
TP178
TPAD14-GP
R2390
0R2J-2-GP
R2392
6K98R2-GP
8223_FB2_R
C1115
SC18P50V2JN-1-GP
R2396
10KR2F-2-GP
Id=12A
Qg=7.6~10.6nC,
Rdson=9.5~13mohm
R2391
R2393
31K6R2F-GP
C1116
R2397
20KR2F-L-GP
DVT
20100121
G196
GAP-CLOSE-PWR-3-GP
C1113
TC37
R2394
0R2J-2-GP
R2395
0R2J-2-GP
8223_PGOOD 14
3V/5V_EN 31,33,45
3D3V_AUX_S5
5V_AUX_S5
G197
G198
C1117
SC4D7U6D3V3KX-GP
C1118
SC10U6D3V3MX-GP
R2398
R2399
R2400
R2401
Vout=2*(1+R1/R2)
8223_REF
3D3V_AUX_S5
SKIPSEL
PWM
00A AUTOSKIP
TONSEL
245k/CH1
305k/CH2
300k/CH1
375k/CH2
Squirtle CP DIS SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8223_5V/3D3V
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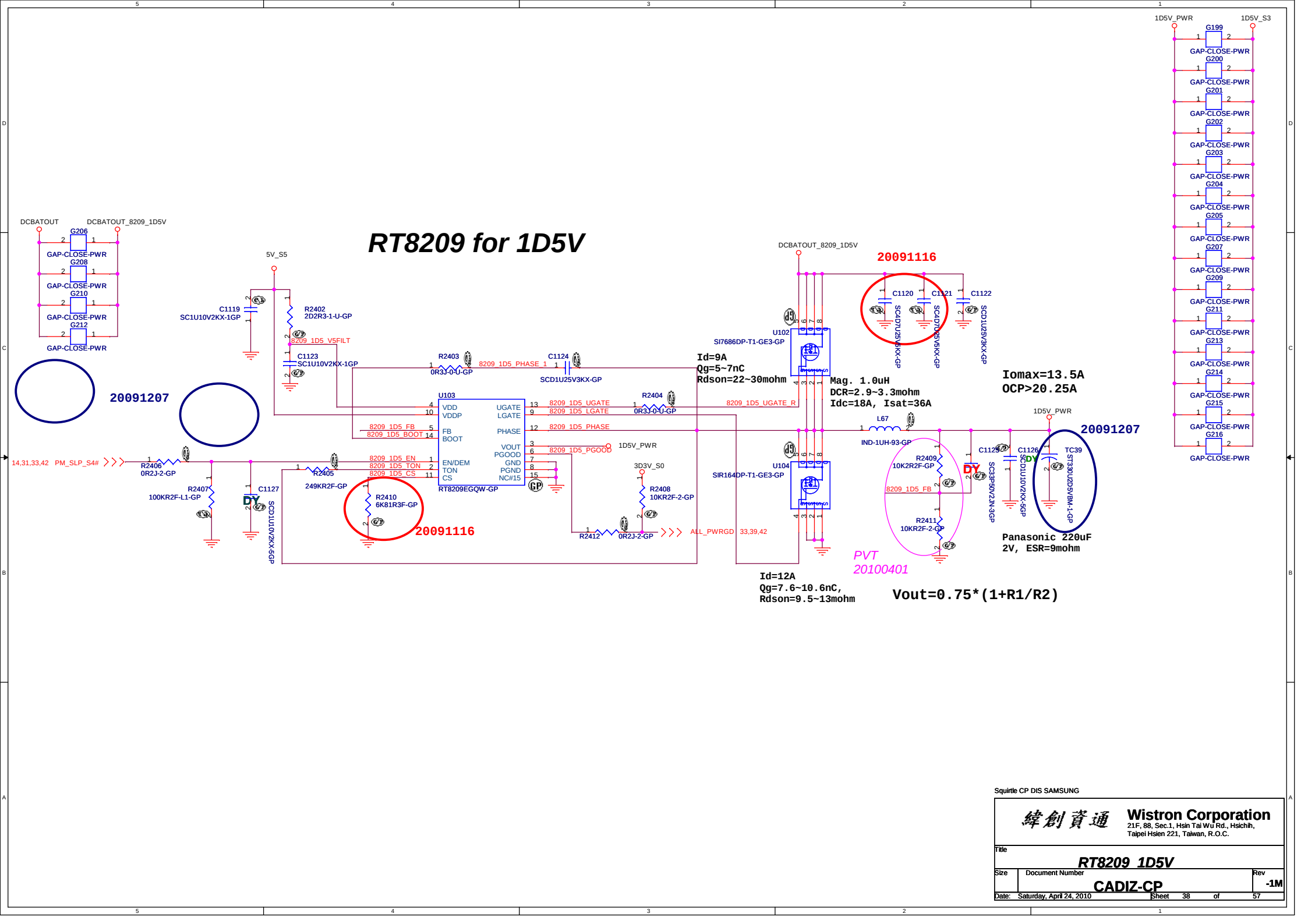

Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8209_1D5V		
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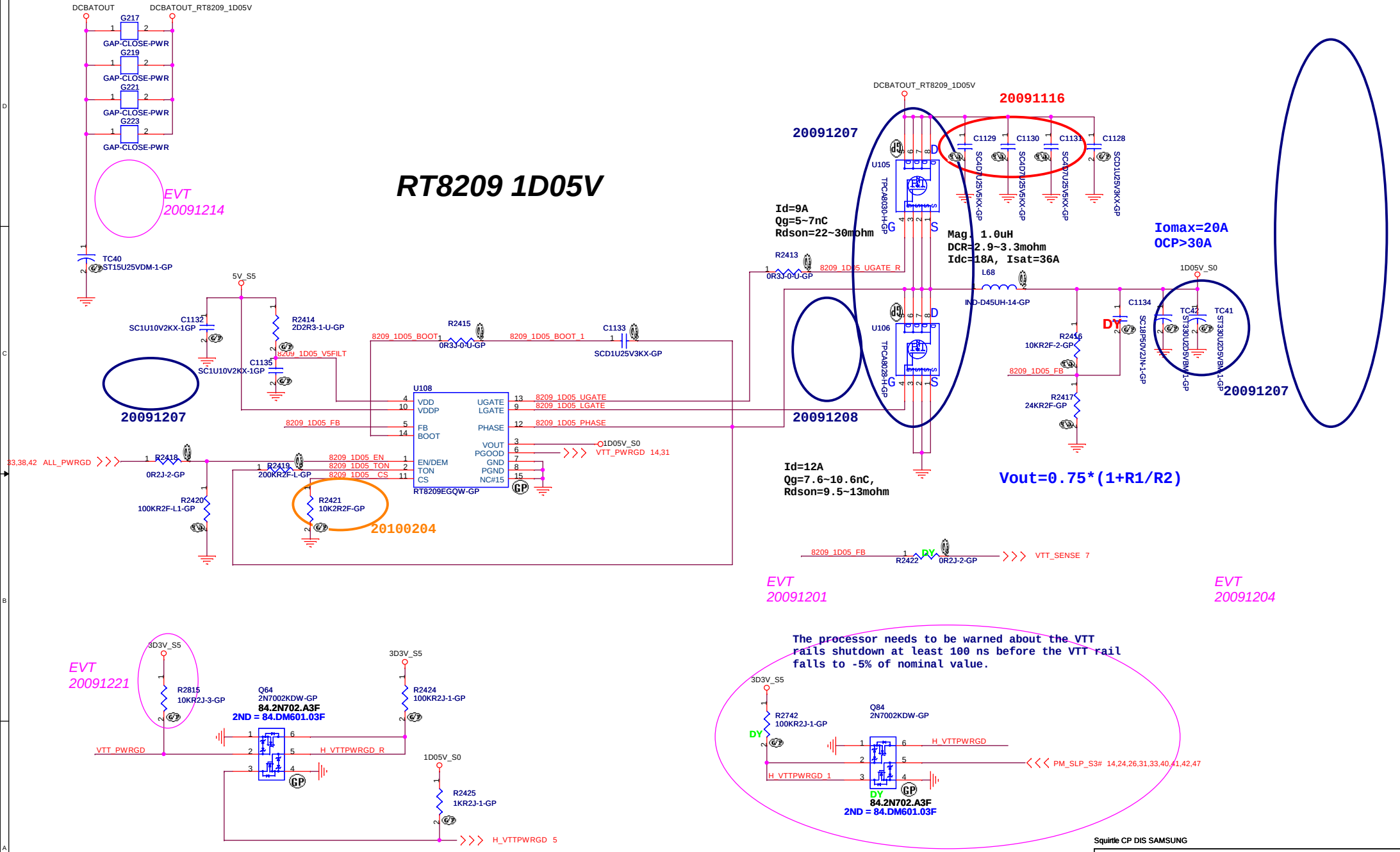
RT8209 1D05V



Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	RT8209_1D05V	
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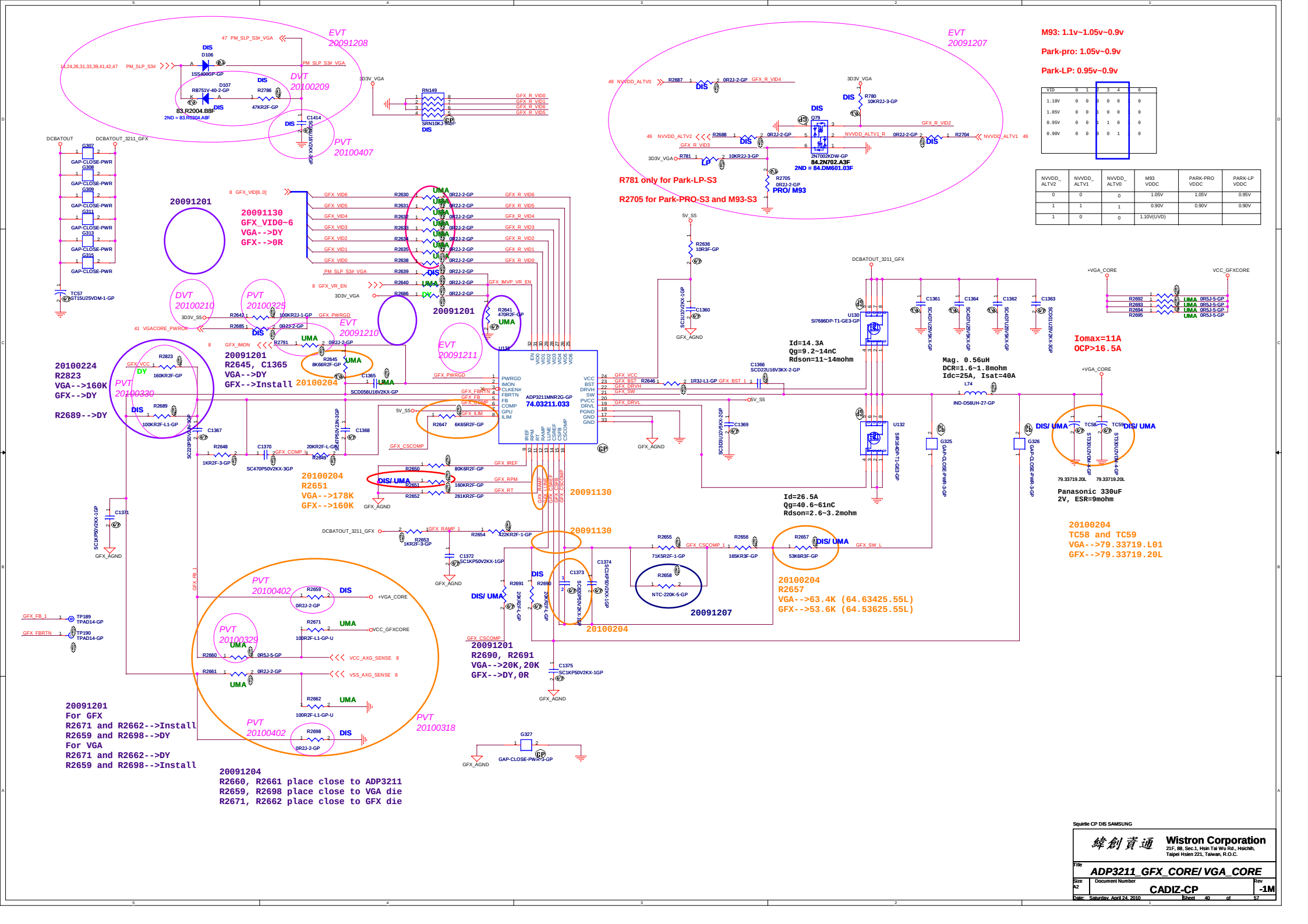
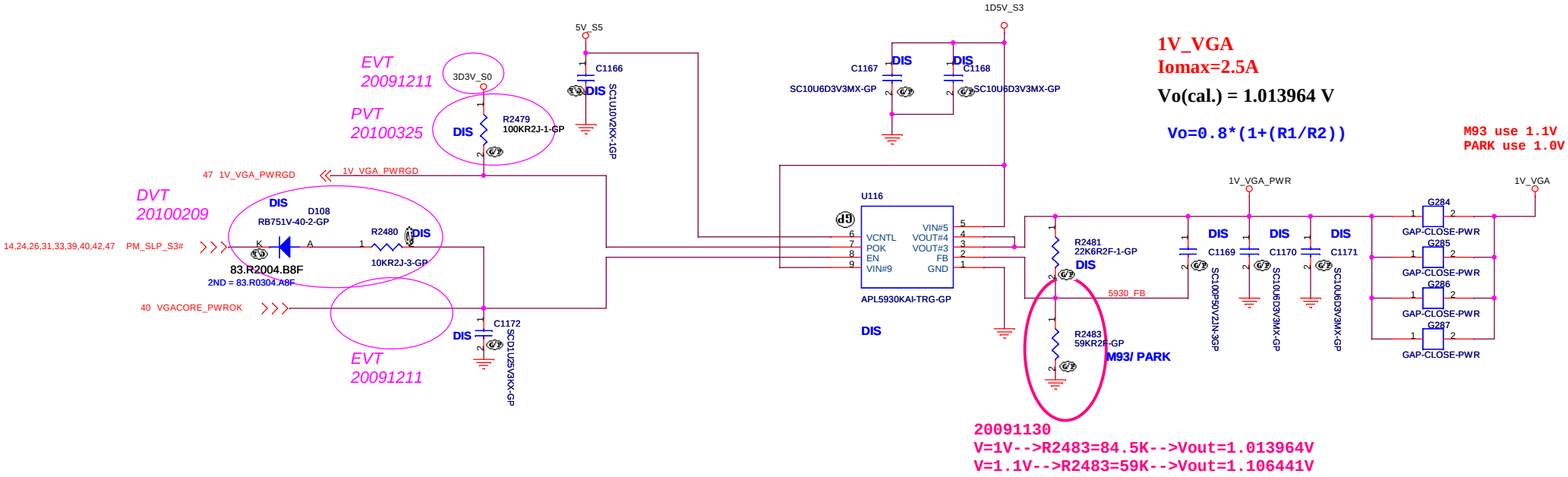


VID	0	1	2	3	4	5	6
1.10V	0	0	0	0	0	0	0
1.05V	0	0	1	0	0	0	0
0.95V	0	0	1	1	0	0	0
0.90V	0	0	0	0	1	0	0

NVVDD_ ALTV2	NVVDD_ ALTV1	NVVDD_ ALTV0	M93 VDDC	PARK-PRO VDDC	PARK-LP VDDC
0	0	0	1.05V	1.05V	0.95V
1	1	1	0.90V	0.90V	0.90V
1	0	0	1.10V(UVD)		

APL5930 for 1V_VGA



Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *ISL62881_+VCC_GFXCORE*		
Size: A3	Document Number: CADIZ-CP	Rev: -1M
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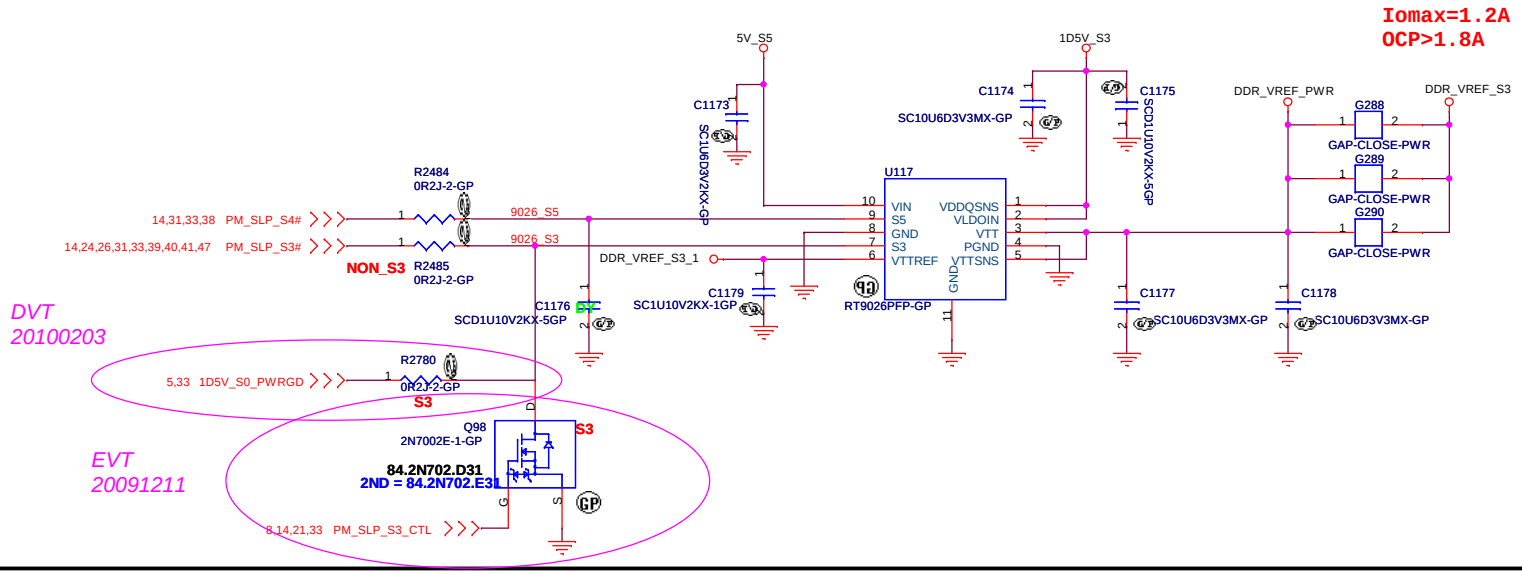
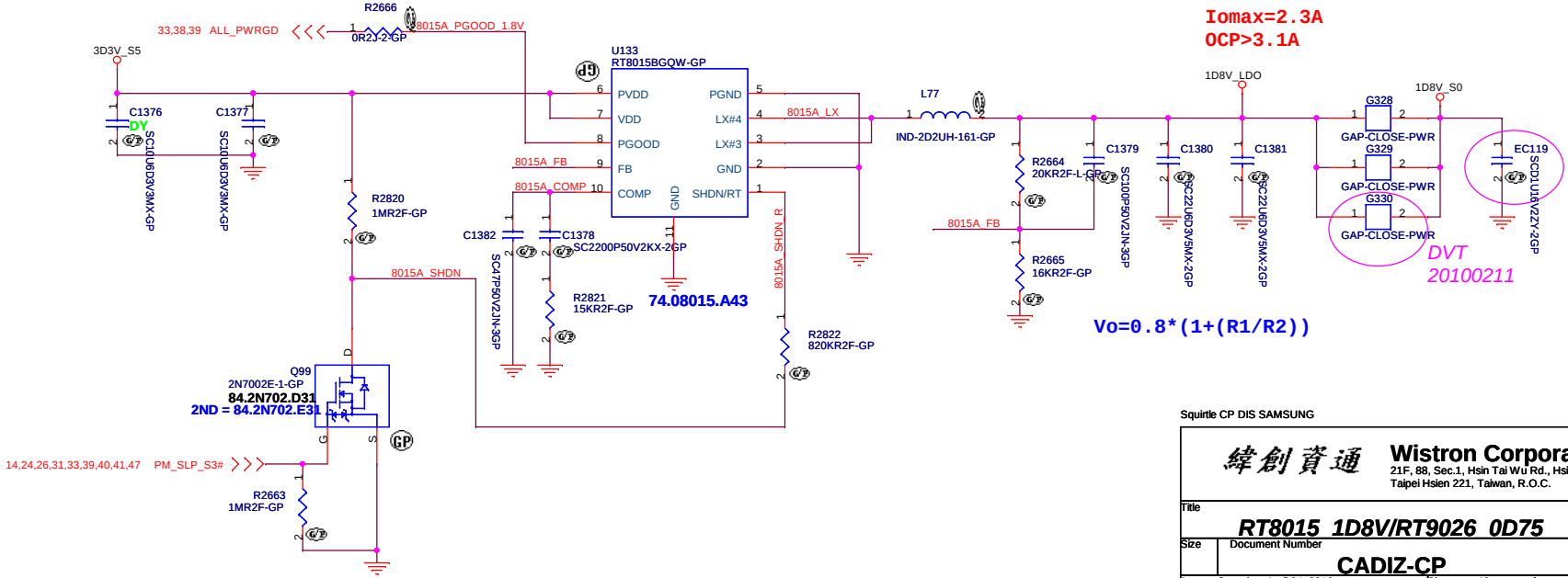
RT9026 for 0D75V_S3



20100209

RT8015 for 1D8V_S0



Squirtle CP DIS SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***RT8015_1D8V/RT9026_0D75***
Size	Document Number: **CADIZ-CP** — Rev: **-1M**
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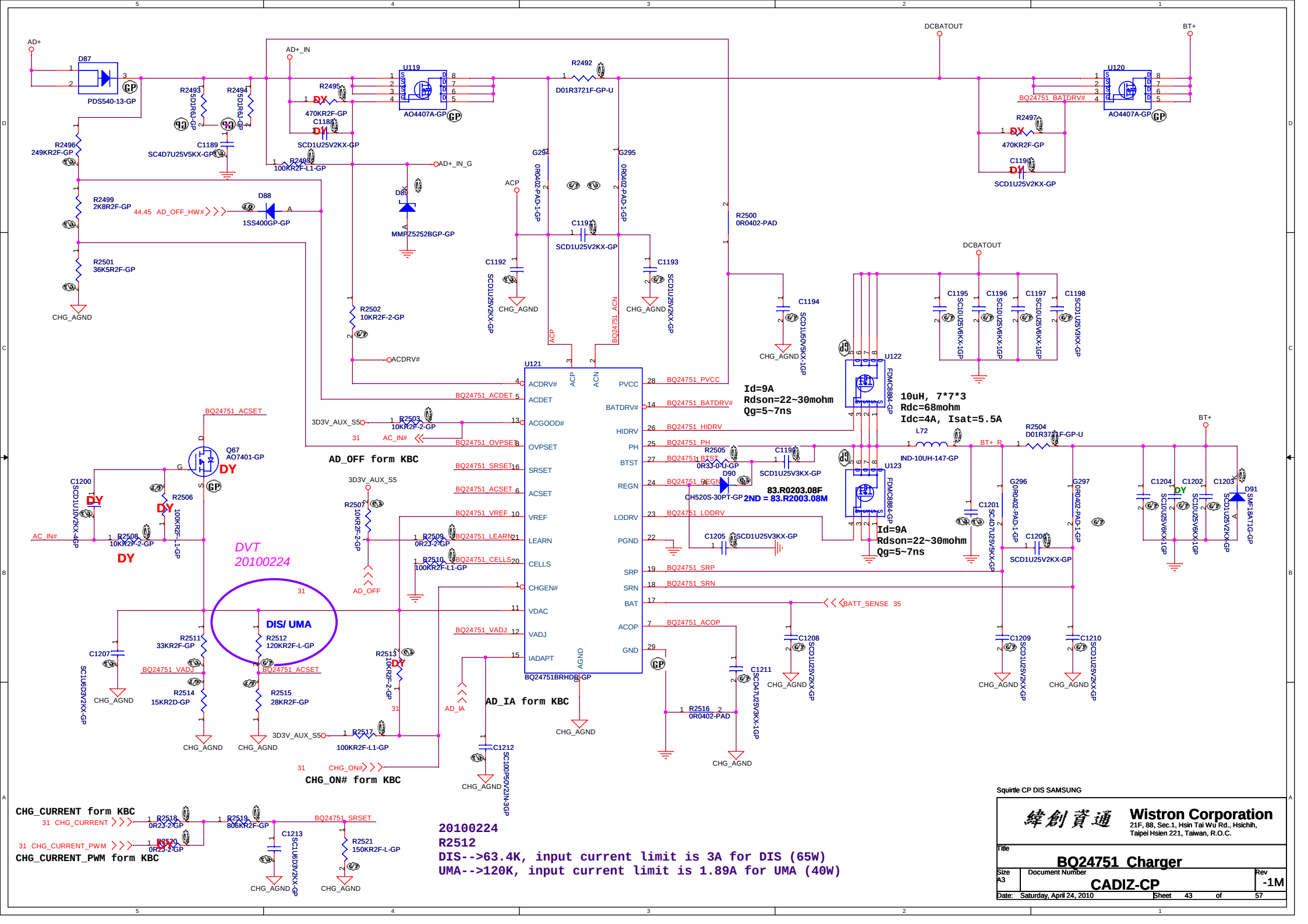
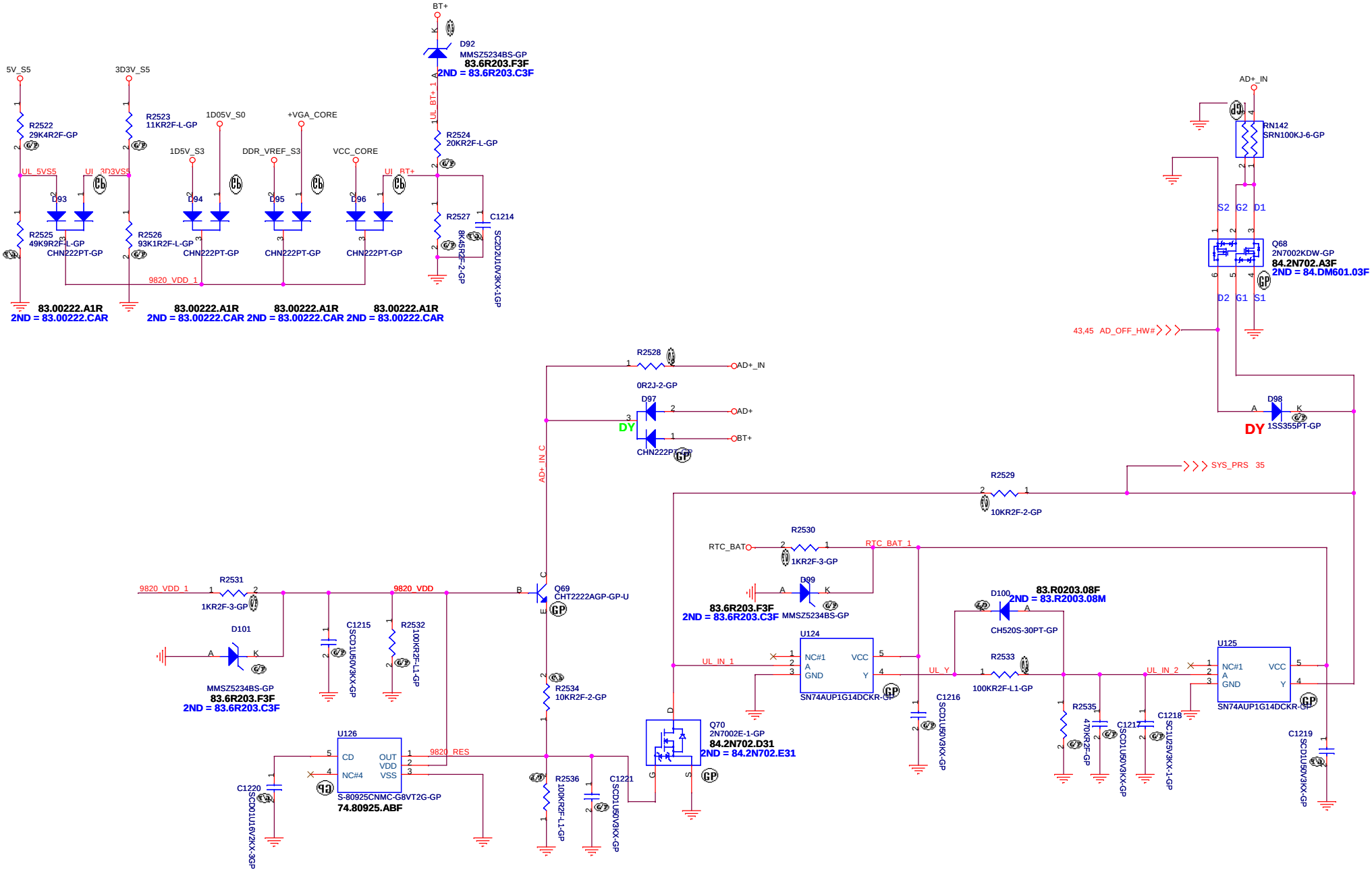
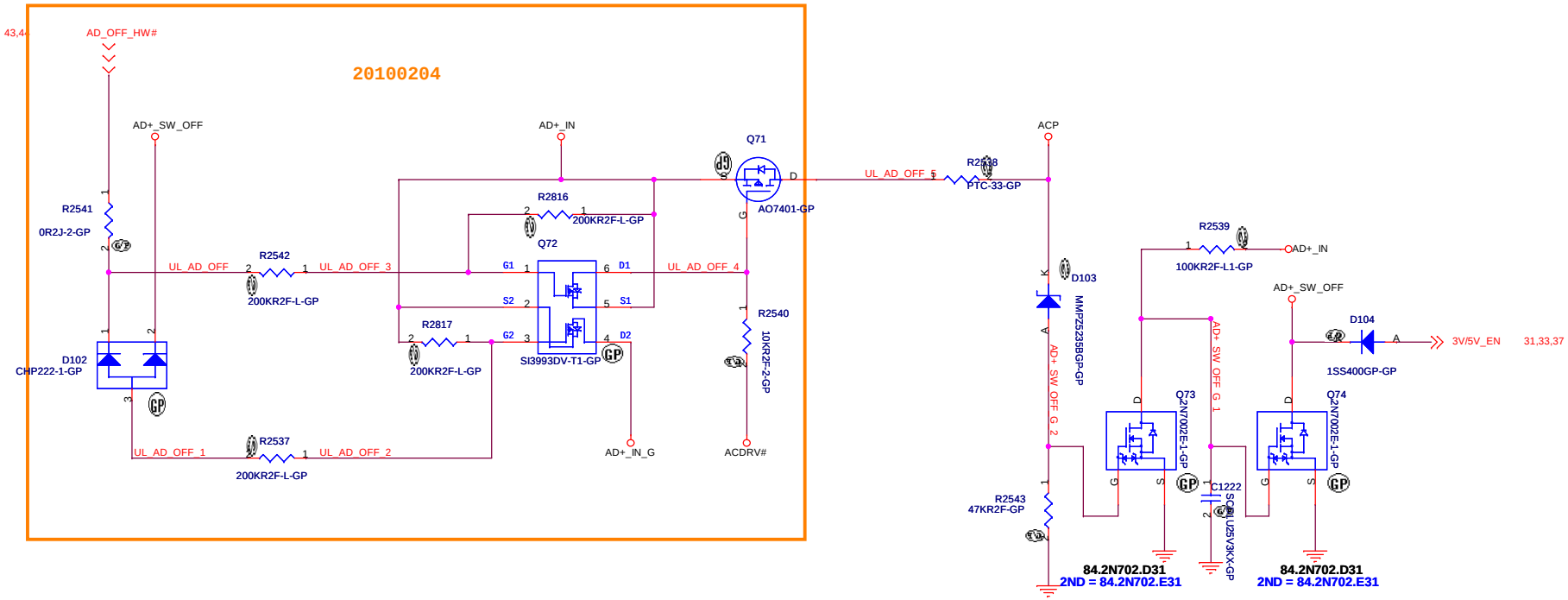

AD+
D87
PDS540-13-GP
R2493
5D1R8J-GP
R2494
5D1R8J-GP
R2496
249KR2F-GP
C1189
SC4D7U25V5KX-GP
AD+_IN
R2495
470KR2F-GP
C1188
SCD1U25V2KX-GP
R2498
100KR2F-L1-GP
AD+_IN_G
U119
AO4407A-GP
R2492
D01R3721F-GP-U
R2499
2K8R2F-GP
44,45 AD_OFF_HW#
D88
1SS400GP-GP
D89
MMPZ5252BGP-GP
R2501
36K5R2F-GP
CHG_AGND
R2502
10KR2F-2-GP
ACDRV#
ACP
G294
0R0402-PAD-1-GP
G295
0R0402-PAD-1-GP
C1191
SCD1U25V2KX-GP
C1192
SCD1U25V2KX-GP
C1193
SCD1U25V2KX-GP
BQ24751_ACN
R2500
0R0402-PAD
C1194
SCD1U50V5KX-1GP
DCBATOUT
BT+
U120
AO4407A-GP
BQ24751_BATDRV#
R2497
470KR2F-GP
C1190
SCD1U25V2KX-GP
C1195
SC10U25V6KX-1GP
C1196
SC10U25V6KX-1GP
C1197
SC10U25V6KX-1GP
C1198
SCD1U25V3KX-GP
U121
ACDRV#
ACDET
ACGOOD#
OVPSET
SRSET
ACSET
VREF
LEARN
CELLS
CHGEN#
VDAC
VADJ
IADAPT
PVCC
BATDRV#
HIDRV
PH
BTST
REGN
LODRV
PGND
SRP
SRN
BAT
ACOP
GND
BQ24751BRHDR-GP
BQ24751_PVCC
BQ24751_BATDRV#
BQ24751_HIDRV
BQ24751_PH
BQ24751_BTST
BQ24751_REGN
BQ24751_LODRV
BQ24751_SRP
BQ24751_SRN
BQ24751_ACOP
BATT_SENSE 35
U122
FDMC8884-GP
U123
FDMC8884-GP
Id=9A
Rdson=22~30mohm
Qg=5~7ns
10uH, 7*7*3
Rdc=68mohm
Idc=4A, Isat=5.5A
L72
IND-10UH-147-GP
R2504
D01R37F-GP-U
R2505
0R3J-0-U-GP
D90
CH520S-30PT-GP
C1199
SCD1U25V3KX-GP
83.R0203.08F
2ND = 83.R2003.08M
C1205
SCD1U25V3KX-GP
C1201
SC4D7U25V5KX-GP
C1200
SCD1U10V2KX-4GP
Q67
AO7401-GP
R2506
100KR2F-L1-GP
R2508
10KR2F-2-GP
AC_IN#
R2507
10KR2F-2-GP
AD_OFF
AD_OFF form KBC
R2509
0R2J-2-GP
R2510
100KR2F-L1-GP
DVT
20100224
DIS/ UMA
R2511
33KR2F-GP
R2512
120KR2F-L-GP
R2513
10KR2F-2-GP
R2514
15KR2D-GP
R2515
28KR2F-GP
C1207
SC1U6D3V2KX-GP
AD_IA
AD_IA form KBC
C1208
SCD1U25V2KX-GP
C1209
SCD1U25V2KX-GP
C1210
SCD1U25V2KX-GP
C1211
SCD47U25V9KX-1GP
R2516
0R0402-PAD
C1212
SC100P50V2JN-3GP
R2517
100KR2F-L1-GP
CHG_ON#
CHG_ON# form KBC
C1202
SC10U25V6KX-1GP
C1203
SCD1U25V2KX-GP
C1204
SC10U25V6KX-1GP
D91
SMF18ATTLG-GP
G296
0R0402-PAD-1-GP
G297
0R0402-PAD-1-GP
CHG_CURRENT form KBC
CHG_CURRENT
R2518
0R2J-2-GP
CHG_CURRENT_PWM
R2520
0R2J-2-GP
CHG_CURRENT_PWM form KBC
R2519
806KR2F-GP
C1213
SC1U6D3V2KX-GP
R2521
150KR2F-L-GP
20100224
R2512
DIS-->63.4K, input current limit is 3A for DIS (65W)
UMA-->120K, input current limit is 1.89A for UMA (40W)
Squirtle CP DIS SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24751 Charger
Size
A3
Document Number
CADIZ-CP
Rev
-1M
Date: Saturday, April 24, 2010
Sheet 43 of 57



Squirtle CP DIS SAMSUNG

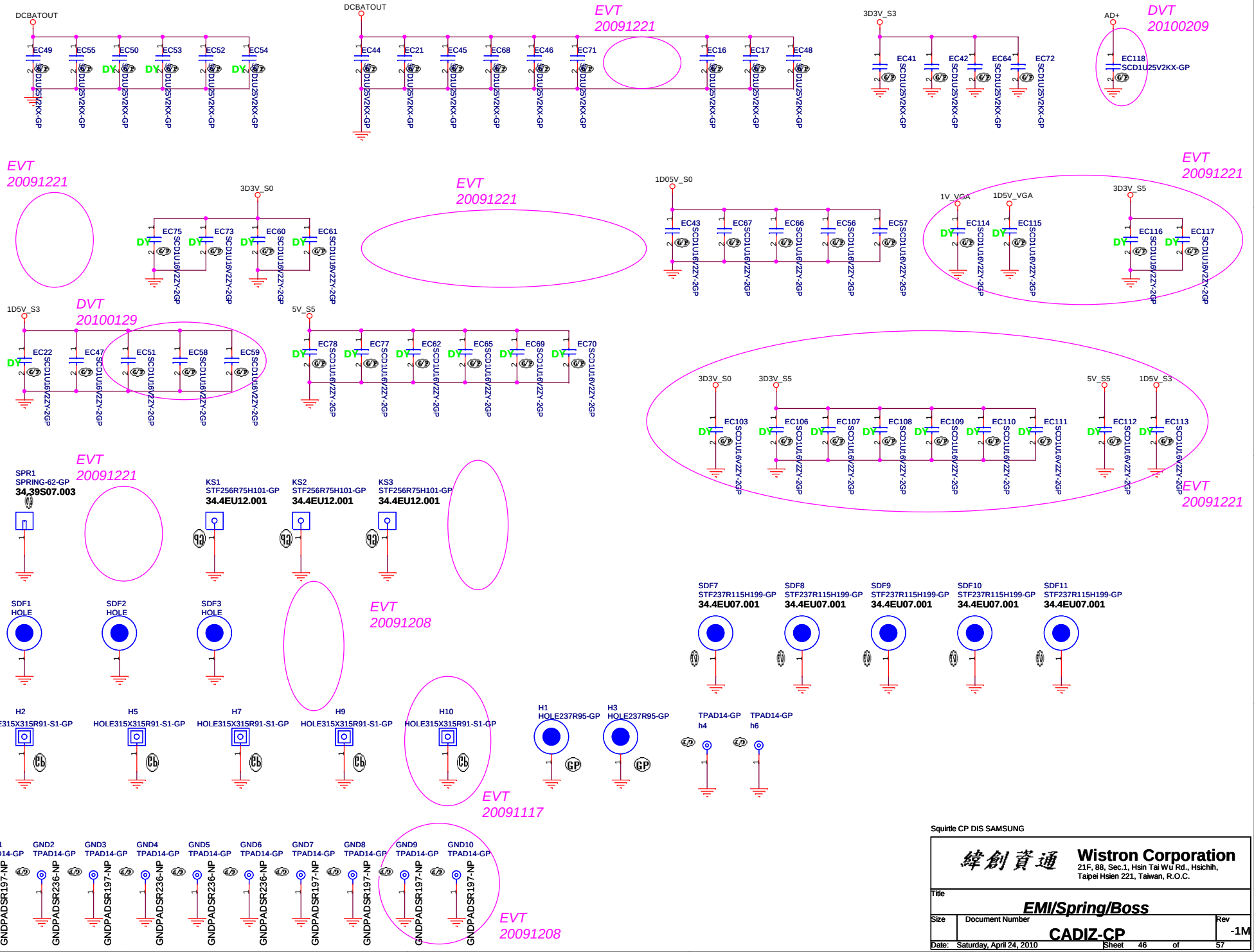
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: UL circuit		
Size: A3	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 44 of 57	



Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **UVP Protect**		
Size: A3	Document Number: **CADIZ-CP**	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 45 of 57	



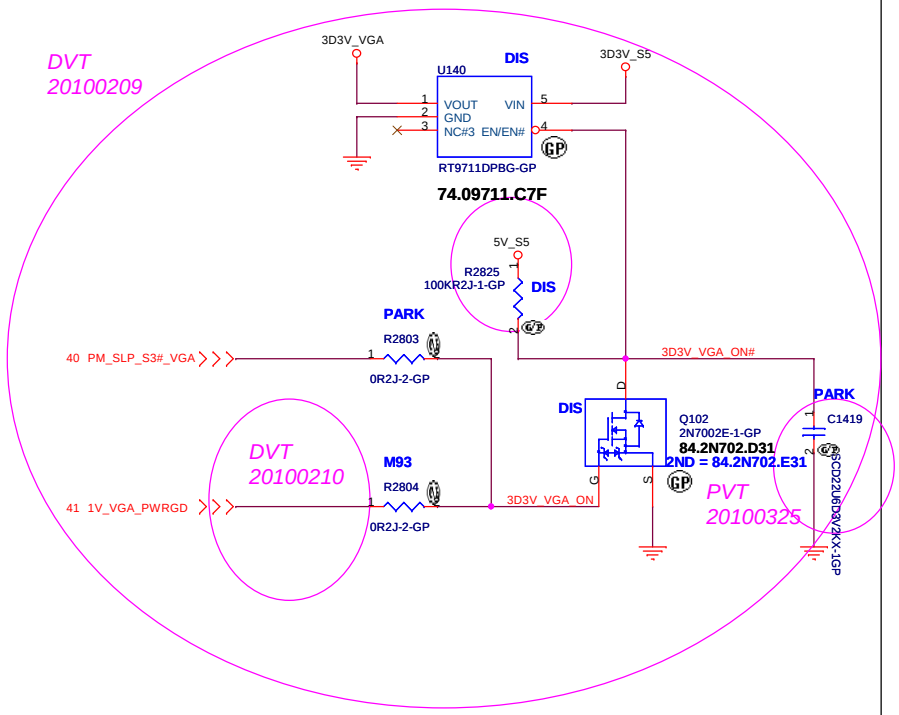
Squirtle CP DIS SAMSUNG

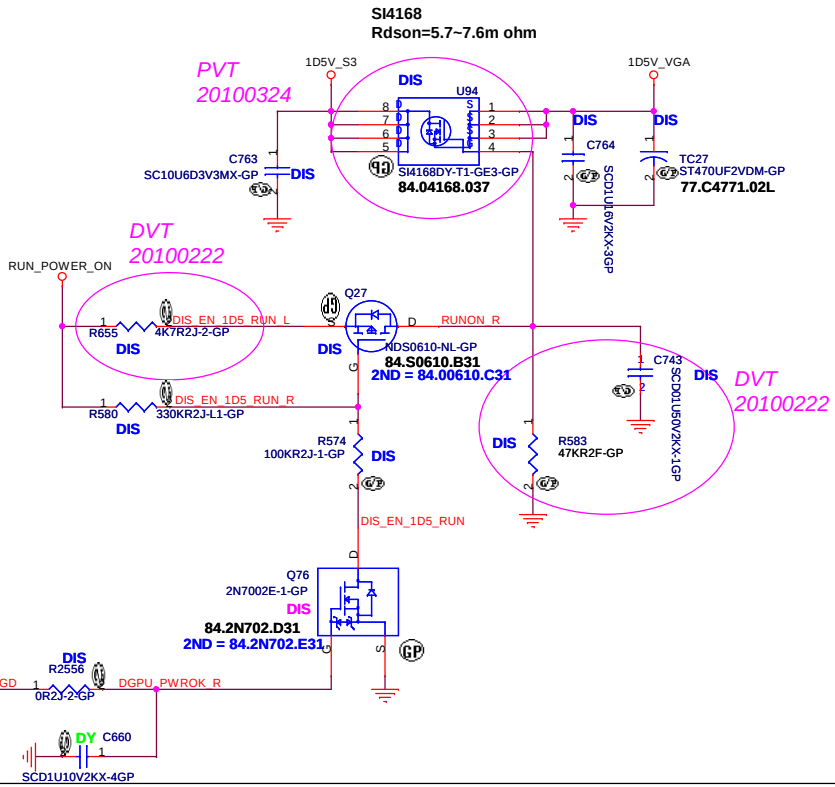
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

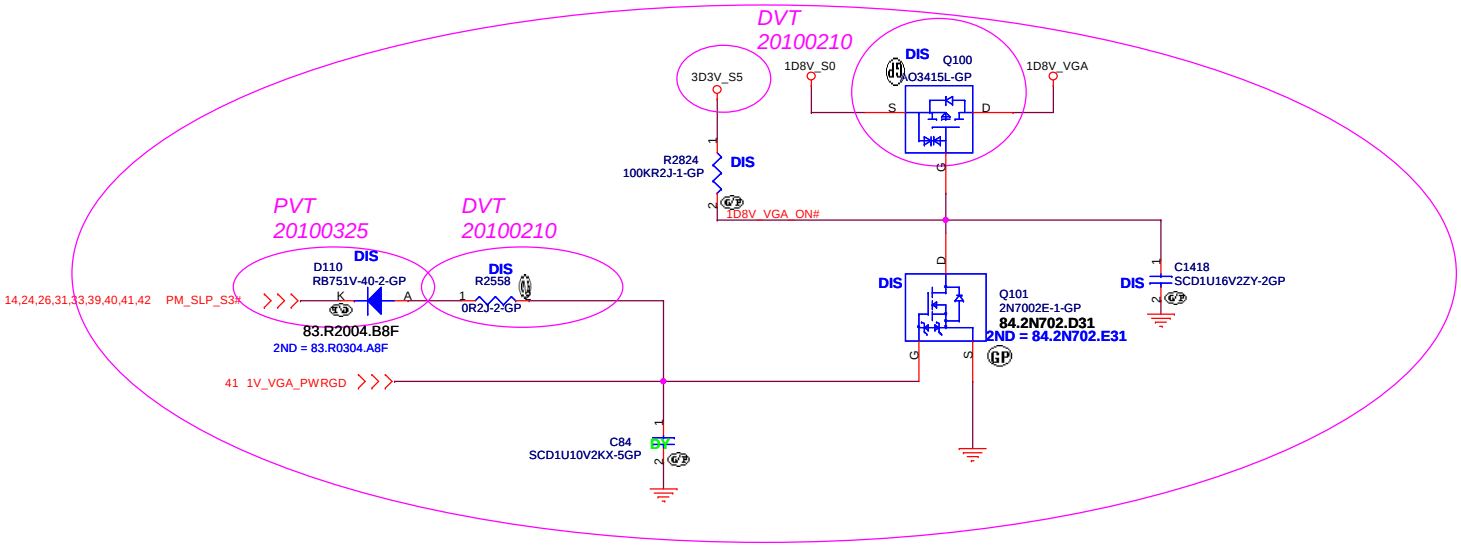
Title: ***EMI/Spring/Boss***

Size	Document Number	Rev
	CADIZ-CP	-1M

Date: Saturday, April 24, 2010 Sheet 46 of 57







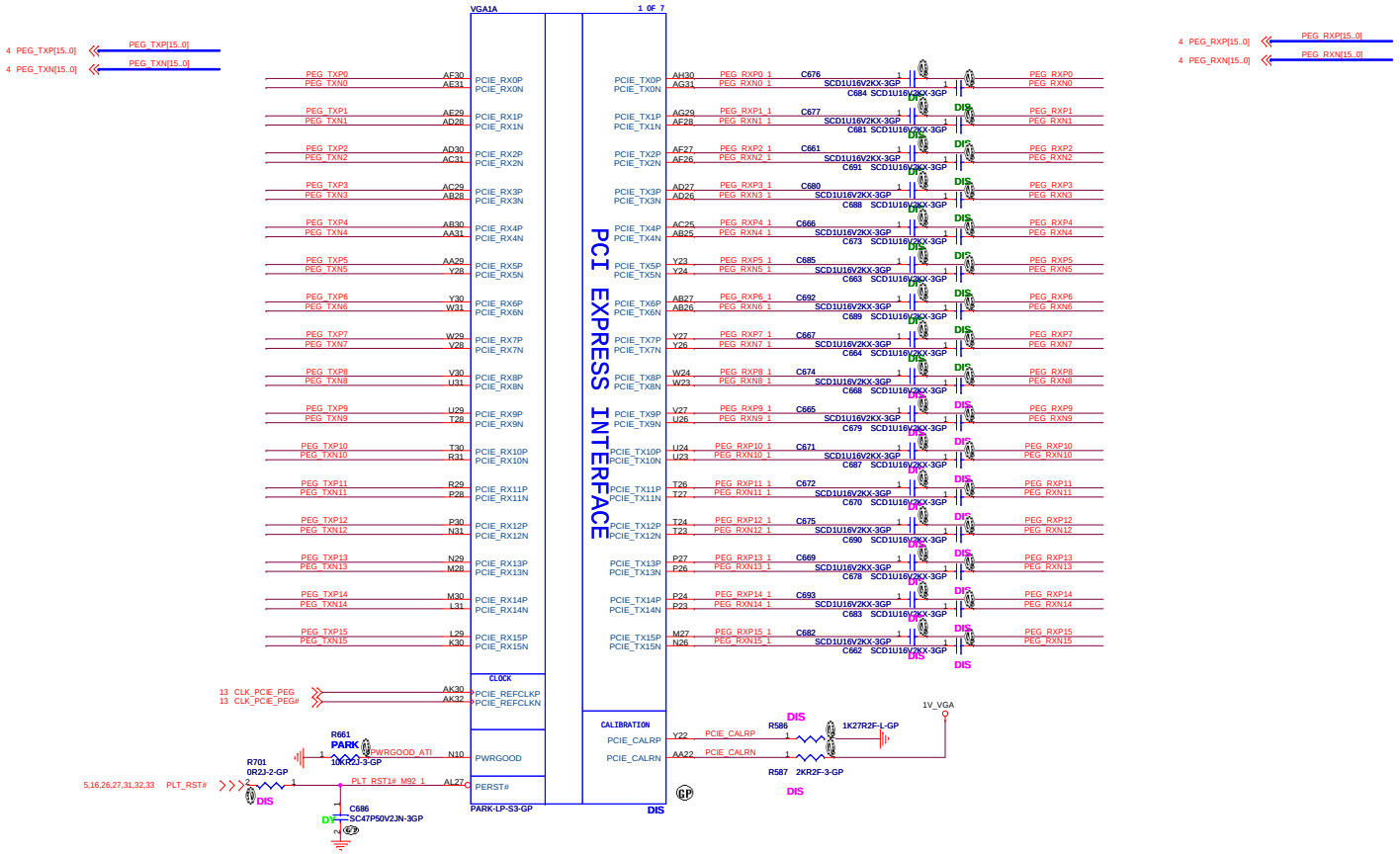
Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI POWER**

Size	Document Number	Rev
A3	CADIZ-CP	-1M

Date: Saturday, April 24, 2010 Sheet 47 of 57



EVT
20091210

49 BB_ENA

R2715
10KR2J-3-GP
DIS

BB_ENA = 0V FOR BACK BIASING DISABLED
N FET Q5 = OFF, P FET Q4 = OFF, N FET Q3 = ON
+BBP = VDD_CORE
BB_ENA = +3.3V FOR BACK BIASING ENABLED
N FET Q5 = ON, P FET Q4 = ON, N FET Q3 = OFF
+BBP = +1.8V

Squintle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Madison PCIE**

Size	Document Number	Rev
A2	CADIZ-CP	-1M

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Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

DVPDATA [3:0]
0100 512MB Hynix-H5TQ1G63BFR-12C (800MHz)
1000 512MB Samsung-K4W1G1646E-HC12 (800MHz)

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

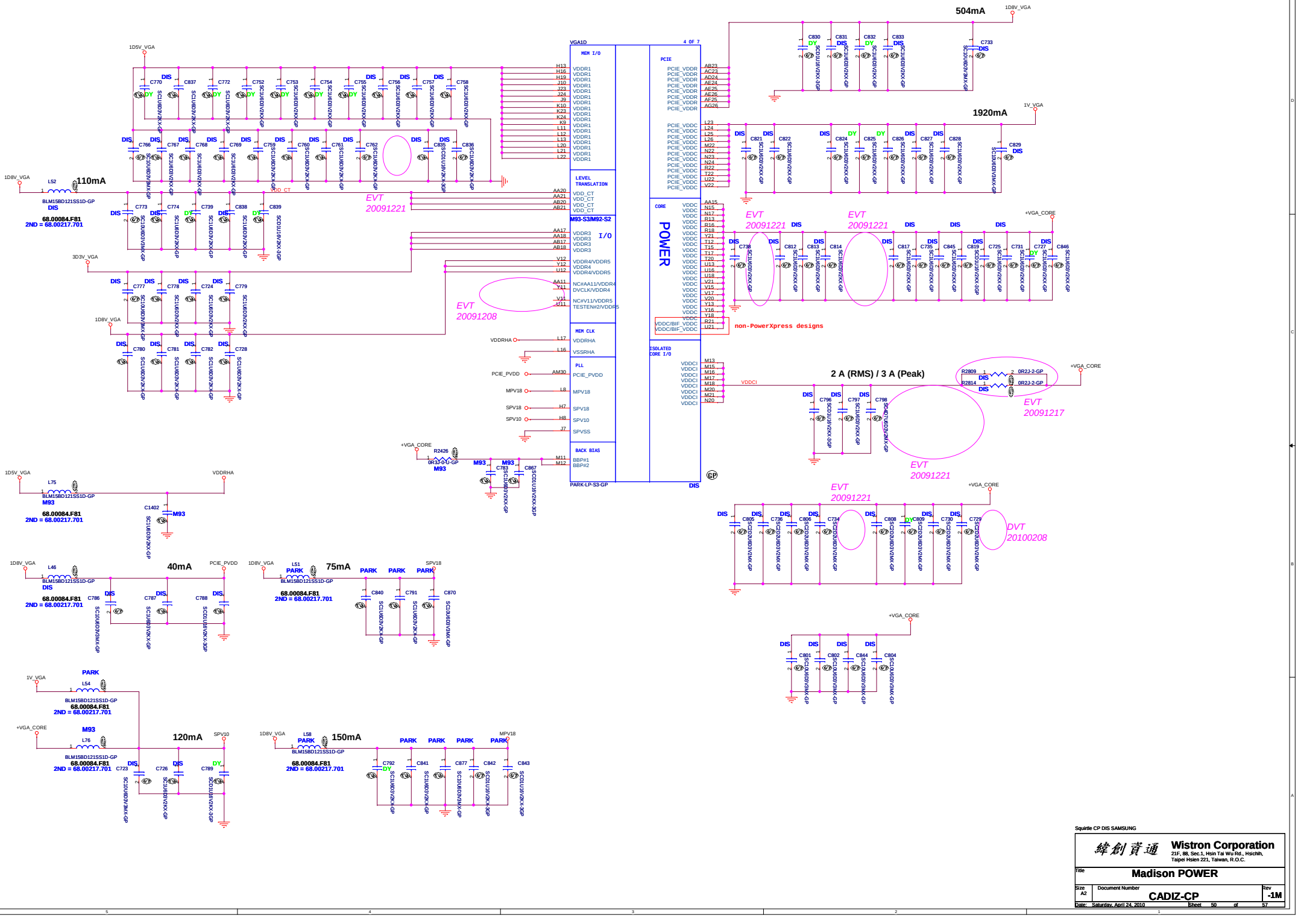
For Thermal sensor

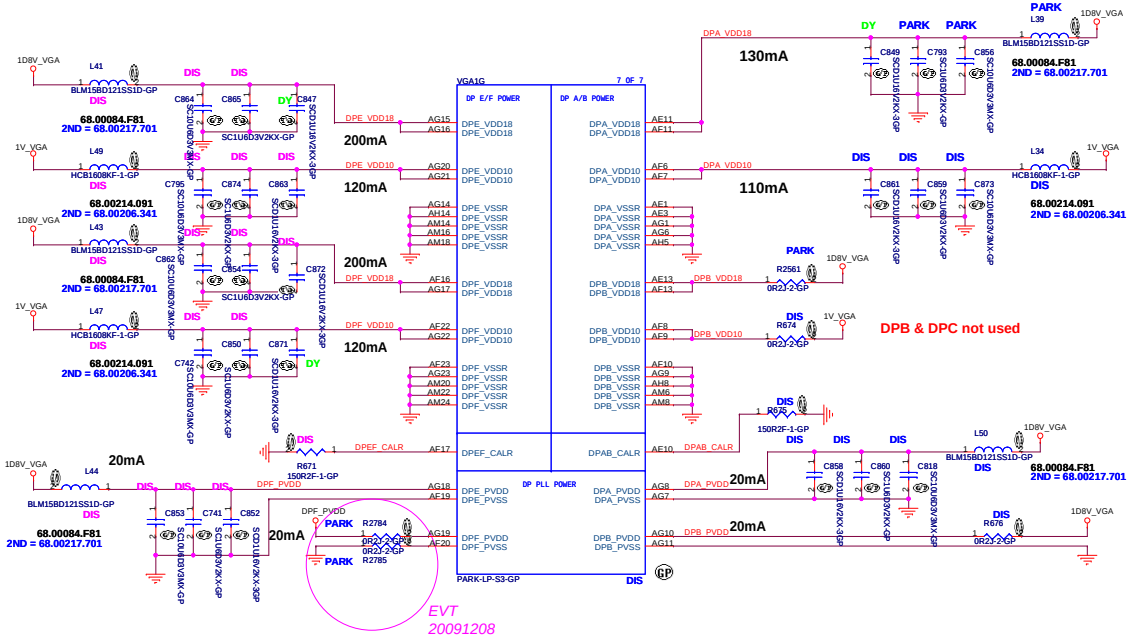
EVT 20091207
EVT 20091117
EVT 20091208
PVT 20100401

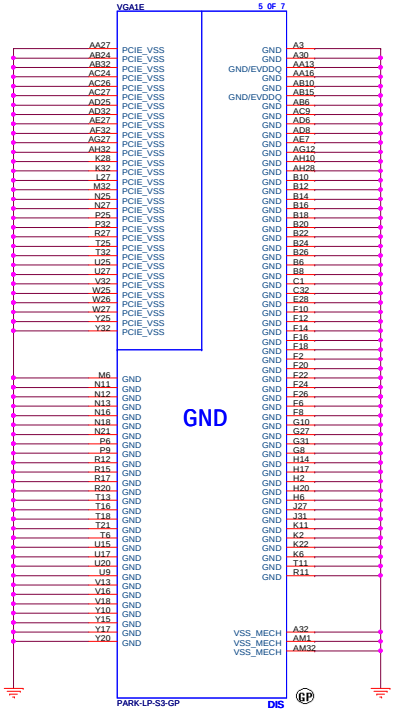
Squirtle CP DIS SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison IO
Size: Custom | Document Number: CADIZ-CP | Rev: -1M
Date: Saturday, April 24, 2010 | Sheet 49 of 57


VGA1D
4 OF 7
MEM I/O
LEVEL TRANSLATION
M93-S3/M92-S2
I/O
MEM CLK
PLL
BACK BIAS
PARK-LP-S3-GP
PCIE
CORE
POWER
ISOLATED CORE I/O
504mA
1920mA
110mA
40mA
75mA
120mA
150mA
2 A (RMS) / 3 A (Peak)
EVT 20091221
EVT 20091208
EVT 20091217
DVT 20100208
non-PowerXpress designs
68.00084.F81
2ND = 68.00217.701
Squirtle CP DIS SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison POWER
CADIZ-CP
-1M
Saturday, April 24, 2010
50
57





Squirtle CP DIS SAMSUNG

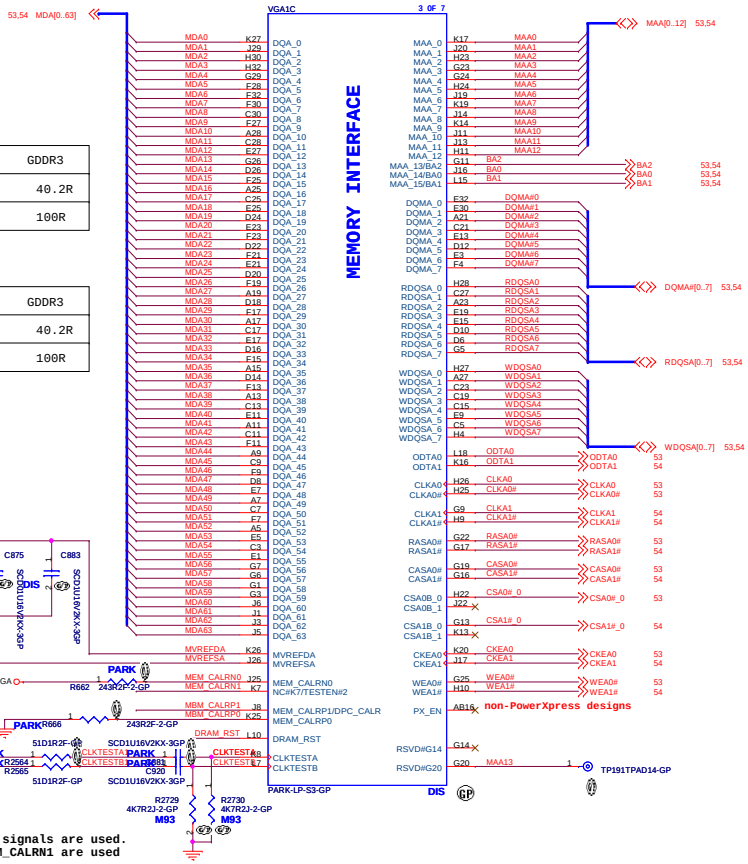
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DP POWER_GND	
Size A2	Document Number CADIZ-CP	Rev -1M
Date: Saturday, April 24, 2010	Sheet 51 of 57	

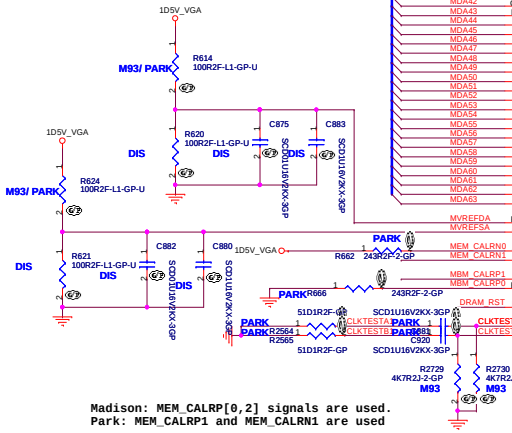
For M9X-S2/S3

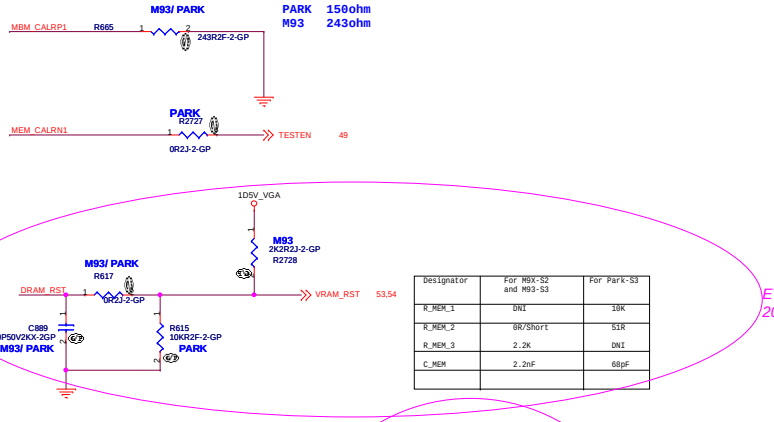
DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

For Park-S3

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

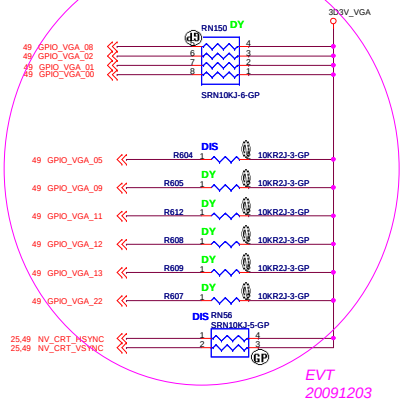






Designator	For M9X-S2 and M93-S3	For Park-S3
R_MEM_1	DNI	10K
R_MEM_2	0R/Short	51R
R_MEM_3	2.2K	DNI
C_MEM	2.2nF	68pF

EVT
20091208



EVT
20091203

Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	0
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0			If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures		GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V	128MB	x000	ST Microelectronics	M25P05A	0100
	256MB	x001		M25P10A	0101
	64MB	x010		M25P20	0101
	32MB	x		M25P40	0101
	512MB	x		M25P80	0101
	1GB	x			
	2GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
	4GB	x		Pm25LV010A	0101

Squirtle CP DIS SAMSUNG

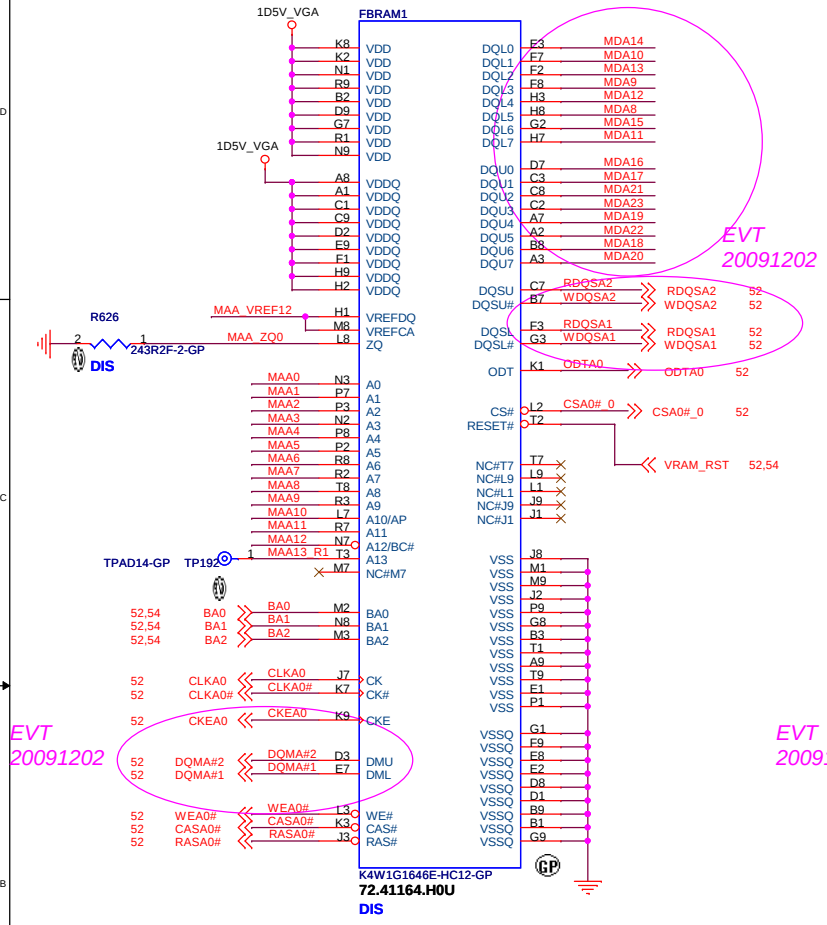
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

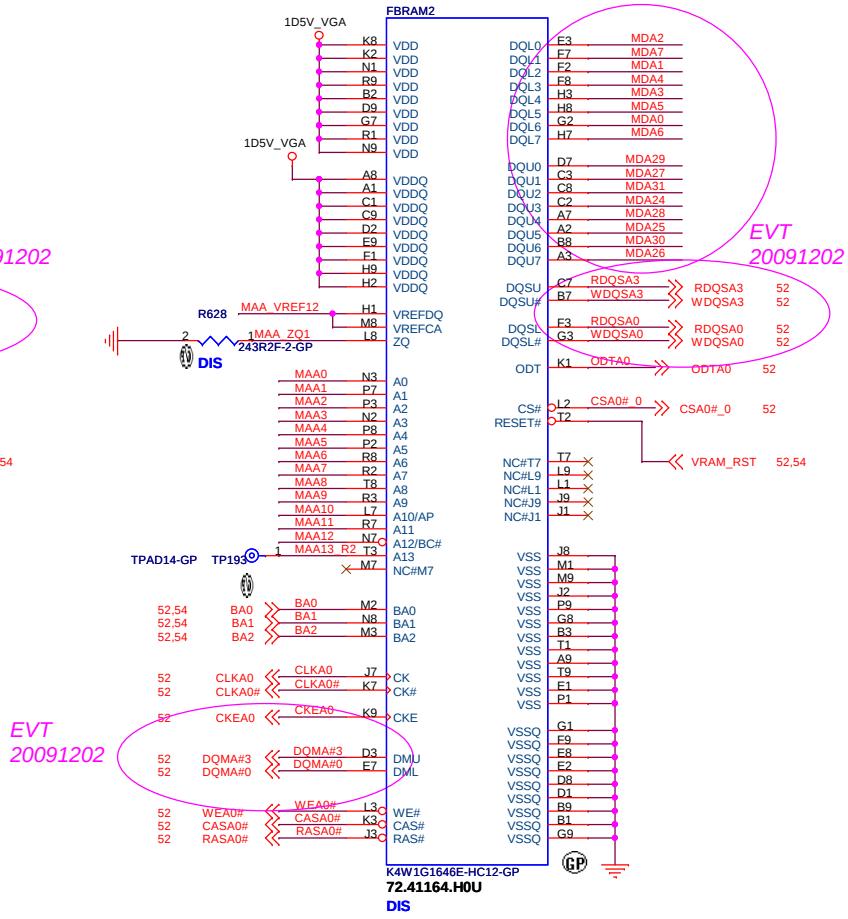
Title: **Madison Memory / Straps**

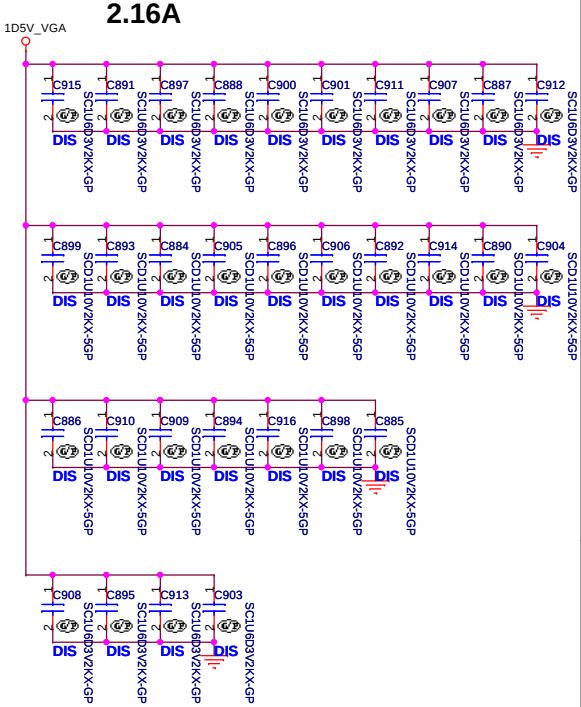
Size	Document Number	Rev
A2	CADIZ-CP	-1M

Date: Saturday, April 24, 2010 Sheet 52 of 57

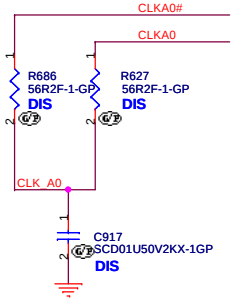
DDR3

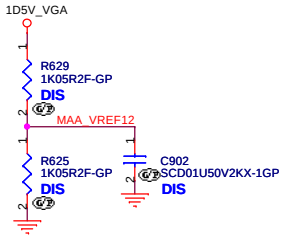


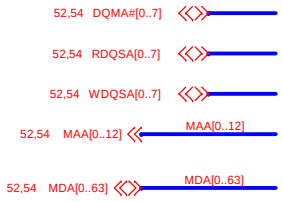




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



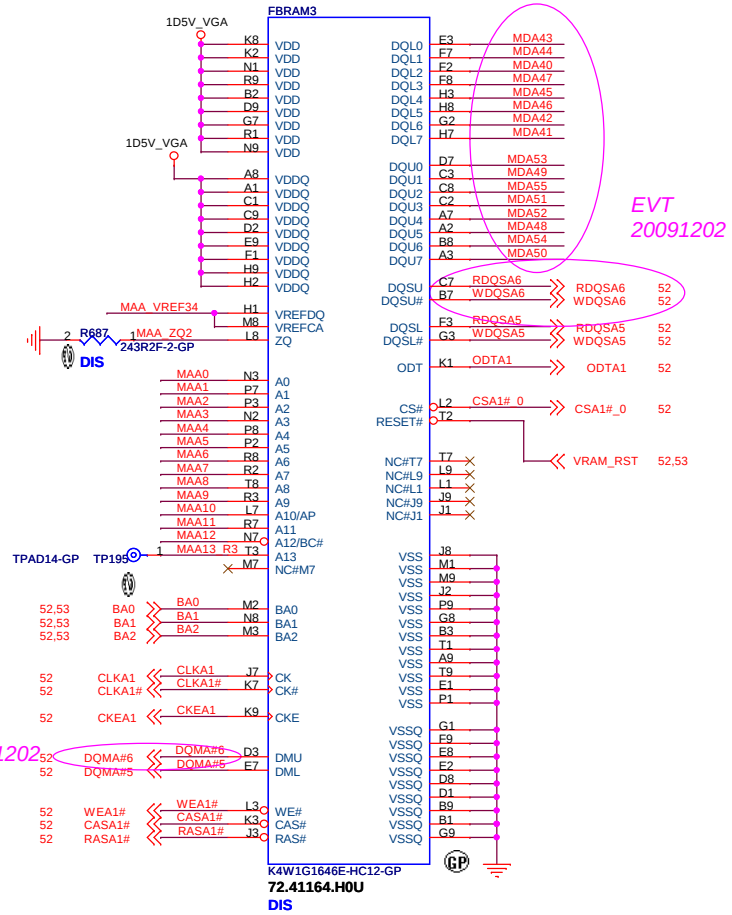


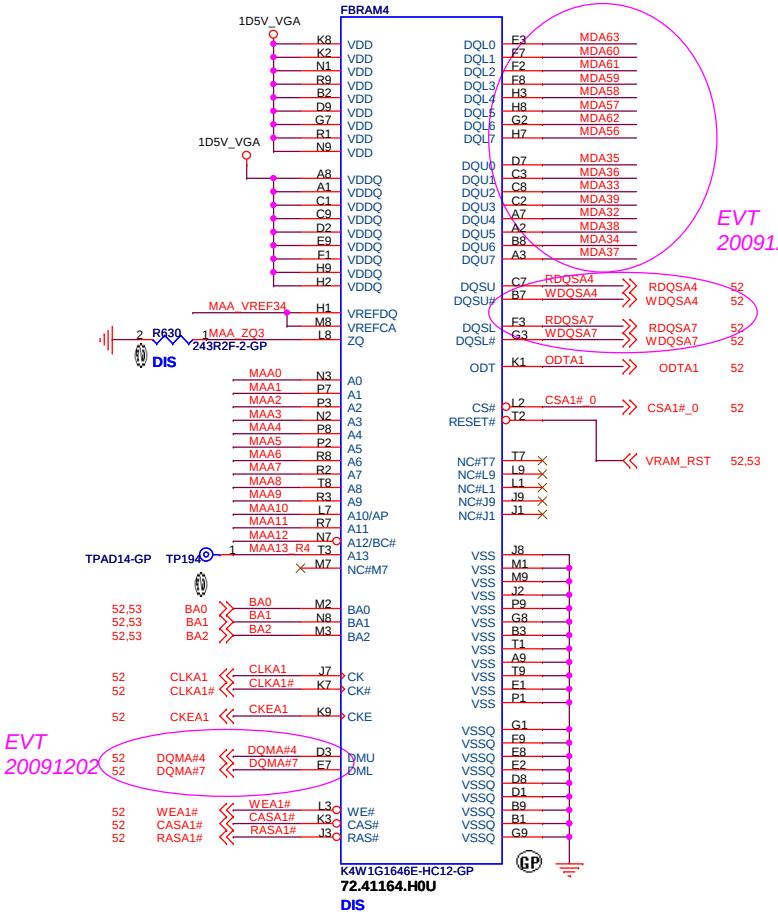


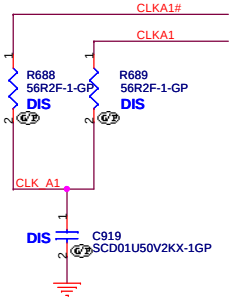
Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM(1/2)		
Size: A3	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 53 of 57	

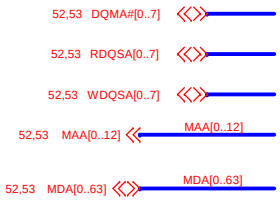
DDR3

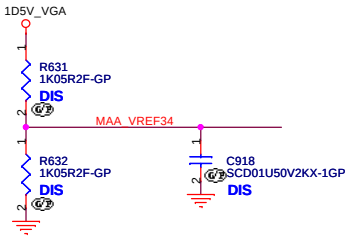






SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U





Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *VRAM(2/2)*		
Size: A3	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 54 of 57	

Reversion History

EVT

(2009/11/17)

P.8 [CPU SFF(5 of 8)-PWR/DDR/GFX]	Delete R2263 (GFX_VR_EN double pull-low)
P.15 [PCH 4 of 9(LVDS/CRT/DP]	Delete RN22 (CLK_DDC_EDID, DAT_DDC_EDID double pull-high)
P.15 [PCH 4 of 9(LVDS/CRT/DP]	Modify RN112 and add RN147
P.15 [PCH 4 of 9(LVDS/CRT/DP]	Change RN113 to three single resisters for PCH RGB signal.
P.23 [LCD CONN]	Add R2621, R2625 100Kohm pull-low for BLON_IN and BLON_OUT_R
P.25 [CRT BD CONN]	Add RN146 pull-high to 3D3V_S0 for CRT_DDCCLK1 and CRT_DDCDATA1
P.47 [EMI/Spring/Boss]	ME add stand off KS1~KS4 and H10
P.50 [PARK-S3 IO]	Change RN86 to three single resisters for VGA RGB signal.

(2009/11/20)

P.13 PCH (2 of 9)-PCIE/CLK/SMB	Modify PCI express ports connection assigned table
P.16 PCH (5 of 9)-PCI/USB	Modify USB ports connection assigned table
P.27 MINI BD CONN	Add USB port for MINI1 WIMAX function

(2009/11/23)

P.25 [CRT BD CONN]	Delete RN126~RN129

(2009/11/25)

P.24 [HDD CONN & TOUCHPAD]	Add HDD protection circuit
P.27 MINI BD CONN	Modify WIMAX USB pair connection
P.25 [CRT BD CONN]	Change HDMI 0.1UF caps to BTBCRT1 side..

(2009/11/27)

P.32 [BIOS & SW/C & BAT ID & Felic]	Add 10Kohm pull low for SPI_WP#

(2009/11/30)

P.27 MINI BD CONN	Modify 5V_MINI_S5, 3d3v_s3 and USB8 net arrangement
P.3 Clock Generator	Add damping resistor for the 14MHz crystal
P.12 PCH (1 of 9)-SATA/RTC/HDA	Add damping resistor for the 32KHz crystal

(2009/12/01)

P.13 PCH (2 of 9)-PCIE/CLK/SMB	Modify PCI express clock connection assigned table
P.40 ADP3211_GFX_CORE/ VGA_CORE	Modify VGA/ GFX co-lay power circuit
P.30 Thermal/Fan Controllor	Modify thermal contral circuit.
P.32 [BIOS & SW/C & BAT ID & Felic]	Modify net name SPI_MOSO_R to SPI_MISO_R
P.32 [BIOS & SW/C & BAT ID & Felic]	Add 100K ohms pull-down resistors on each SPI0_CLK, SPI0_MOSI and SPI0_CS# net.
P.12 PCH (1 of 9)-SATA/RTC/HDA	Add damping resistor for LPC_LAD0~LPC_LAD3 and LPC_LFRAME#
P.7 CPU SFF(4 of 8)-POWER/VTT	Delete VCORE SENSE pin double pull high/low resistors.
P.39 RT8209_1D05V	Add sequence circuit for VTTPWRGOOD and VTT.

(2009/12/02)

P.29 AUDIO JACK	Add speaker protection circuit.
P.32 [BIOS & SW/C & BAT ID & Felic]	Add golden finger debug connector GF1 and only install it on EVT
P.37 [RT8223_5V/3D3V]	Delete 3D3V_PWR 7pcs gaps for more place.
P.12 PCH (1 of 9)-SATA/RTC/HDA	Add test point for JTAG.
P.25 [CRT BD CONN]	Change HDMI_CLK, HDMI_DATA, CRT_DDCCLK1, CRT_DDCDATA1 pull high resistors to 3.83Kohm.
P.53 [VRAM(1/2)]	Swap VRAM DQ, DQS, DM net.
P.54 [VRAM(3/4)]	Swap VRAM DQ, DQS, DM net.

(2009/12/03)

P.13 PCH (2 of 9)-PCIE/CLK/SMB	Change PCIE_CLK_RQ2# to pull low for cardreader.
P.23 [LCD CONN]	Change descrete brightness source from EC to VGA.
P.52 [M93/ PARK-S3 Memory / Straps]	Modify GPIO setting

(2009/12/04)

P.40 ADP3211_GFX_CORE/ VGA_CORE	Modify sense pin circuit.
P.28 Audio Codec ALC275	Modify speaker protection circuit.
P.29 AUDIO JACK	Modify speaker protection circuit.
P.39 RT8209_1D05V	Delete 1D05V output gaps.
P.42 G9661_1D8V/ RT9026_0D75	Add S3 Power Reduction schematics.
P.5 CPU SFF(2 of 8)-CLK/Thermal	Add S3 Power Reduction schematics.
P.17 PCH (6 of 9)-GPIO/RSVD	Add S3 Power Reduction schematics.
P.33 RUN POWER	Add S3 Power Reduction schematics.
P.8 CPU SFF(5 of 8)-PWR/DDR/GFX	Add S3 Power Reduction schematics.
P.21 DDR3-SOCKET_1	Add S3 Power Reduction schematics.
P.14 PCH (3 of 9)-DMI/FDI	Add S3 Power Reduction schematics.

(2009/12/07)

P.31 KBC_NPCE781L / KB	Modify W_Disable# direction to output from EC
P.27 MINI BD CONN	Modify W_Disable# direction to output from EC
P.13 PCH (2 of 9)-PCIE/CLK/SMB	Delete RN102 and omit the routing prom PCH to CPU
P.5 CPU SFF(2 of 8)-CLK/Thermal	alway install RN89 for UMA and DIS.
P.27 MINI BD CONN	Modify power source 6 pins of 3D3V_S3 to 3D3V_S5 for WWAN power off sequence by software request.
P.36 ADP3211_CPU CORE	Power team update circuit and add EL CAP at DCBATOUT for acoustic noise.
P.38 RT8209_1D5V	Power team modify circuit.
P.39 RT8209_1D05V	Power team modify circuit
P.40 ADP3211_GFX_CORE/ VGA_CORE	Power team modify circuit and VID GPIO setting.
P.49 M93/ PARK-S3 IO	Delete VGA_XIN1 net from VGA to CLKGEN and add TP for VGA_JTAG pins and modify PEX_CLKREQ pull high to 3D3V_S5
P.3 Clock Generator	Delete the net "VGA_XIN1" net from VGA to CLKGEN routing.

(2009/12/08)

VEDS & VEDG Status

P.46 EMI/Spring/Boss	Delete SDF4, KS4 and add GND9, GND10 for ME request.
P.50 M93/ PARK-S3 POWER	Pins A11, Y11, V11, U11 can left unconnected at M93-S3 and PARK-S3.
P.51 M93/ PARK-S3 DP POWER_GND	DPF_PVDD, DPF_PVSS add damping resistor for PARK-S3.
P.49 M93/ PARK-S3 IO	Change A2VSSQ connection to clean ground.
P.52 M93/ PARK-S3 Memory / Straps	Modify "DRAM_RST" output circuit.
P.39 RT8209_1D05V	Power team modify circuit (delete U107)
P.40 ADP3211_GFX_CORE/ VGA_CORE	Modify VGA power sequence
P.41 APL5930_1V	Modify VGA power sequence
P.48 M93/ PARK-S3 PCIE	Modify VGA power sequence

(2009/12/09)

P.33 RUN POWER	Delete R344 and C28.
P.3 Clock Generator	Modify symbol to 9LVS3197BKLFT that only one CLKGEN source we will use. Delete pin16 CPU_STOP# to NC for 9LVS3197BKLFT.
P.31 KBC_NPCE781L / KB	Add 100Kohm pull up resistor for ME_UNLOCK# and combine 3pcs 100Kohm pull up to one 8P4R resistor.
P.36 ADP3211_CPU CORE	Change TC60 power plane from DCBATOUT to DCBATOUT_3211_CPU and add TC61 for DCBATOUT
P.9 CPU SFF(6 of 8)-CPUCORE	Delete C978, C979, C982, C983 for placement.
P.17 PCH (6 of 9)-GPIO/RSVD	Change PCH_GPIO57 DIS/UMA selection to KBC.

(2009/12/10)

P.36 ADP3211_CPU CORE	Change net 3211_PWRGD pull high 1Kohm to 3D3V_S0
P.12 PCH (1 of 9)-SATA/RTC/HDA	Change 4pcs TP to two dummy 0402 resistor for layout space.
P.33 RUN POWER	Delete R2720 and R513.
P.14 PCH (3 of 9)-DMI/FDI	Delete R464 and PM_PWROK connection to PCH.B17(PWROK).
P.48 M93/ PARK-S3 PCIE	Delete M93 +BBP circuit.
P.27 MINI BD CONN	Add one more power pin on BTBMINI1 for 3D3V_S3.
P.36 ADP3211_CPU CORE	Modify VID[5:3] setting for 27A CPU core power rating.
P.26 CARDREADER BD CONN	Modify WLAN_BT_DATA direction
P.27 MINI BD CONN	Modify WLAN_BT_DATA direction
P.40 ADP3211_GFX_CORE/ VGA_CORE	Add R2791 0ohm resistor installed on UMA SKU to separate the connection between VGA power circuit and CPU
P.12 PCH (1 of 9)-SATA/RTC/HDA	Add R2793 pull low resistor on la
P.39 RT8209_1D05V	Add sequence circuit for VTTPWRGOOD and VTT when system suddenly moves to G3 by removing both AC and battery at the same time.
P.14 PCH (3 of 9)-DMI/FDI	Add sequence circuit for SYS_PWROK , PWROK, MEPWROK when system suddenly moves to G3 by removing both AC and battery at the same time.

(2009/12/11)

P.5 CPU SFF(2 of 8)-CLK/Thermal	Modify RN93 resistor to two single resistors.
P.40 ADP3211_GFX_CORE/ VGA_CORE	Delete R2644 and change R2642 to 10Kohm.
P.41 APL5930_1V	Delete R2482.
P.47 ATI POWER	Modify R2330 pull-up from 3D3V_S3 to 3D3V_S0.
P.41 APL5930_1V	Modify R2479 pull-up from 3D3V_S3 to 3D3V_S0.
P.47 ATI POWER	Modify 3D3V_VGA sequence circuit.
P.27 MINI BD CONN	Modify to 8pin 3D3V_S3.
P.33 RUN POWER	Change U138 to AO4406AL.

(2009/12/12)

P.27 MINI BD CONN	Modify BTBMINI1 to 3pins of 3D3V_S3 and 6pins of 3D3V_S5.

(2009/12/14)

P.36 ADP3211_CPU CORE	Change R2573 from 1.91Kohm to 10Kohm.
P.26 CARDREADER BD CONN	Modify 5V_S0 power to 1D5V_S0 because 5V_S0 has not used on cardreader board.
P.16 PCH (5 of 9)-PCI/USB	Modify USB_OC#3~USB_OC#7 to single pull-up.
P.39 RT8209_1D05V	Delete G227, G225.
P.8 CPU SFF(5 of 8)-PWR/DDR/GFX	Change R669,R668,R685,R695 to 0402 resistors.
P.9 CPU SFF(6 of 8)-CPUCORE	Delete C1313, C1314.
P.14 PCH (3 of 9)-DMI/FDI	Add D112 to match the sequence IMVP_VR_EN and SYS_PWROK/PCH_PWROK.

(2009/12/14)

P.50 M93/ PARK-S3 POWER	Add 0ohm 0805 resistor for VDDCI.

(2009/12/15)

P.14 PCH (3 of 9)-DMI/FDI	Modify reset circuit for POWEROK and VTTPWRGOOD sequence when system suddenly moves to G3.
P.13 PCH (2 of 9)-PCIE/CLK/SMB	Add 0ohm resistor for XTAL25_OUT.

(2009/12/16)

P.14 PCH (3 of 9)-DMI/FDI	Modify reset circuit for POWEROK,PM_RSMRST# and VTTPWRGOOD sequence when system suddenly moves to G3.
P.40 ADP3211_GFX_CORE/ VGA_CORE	Modify VCC_AXG_SENSE,VSS_AXG_SENSE connection.
P.17 PCH (6 of 9)-GPIO/RSVD	[Bom change] change RN119 from 10Kohm to 33Kohm.
P.36 ADP3211_CPU CORE	[Bom change] change R2580 from 1Kohm to 3.3Kohm.
P.39 RT8209_1D05V	[Bom change] delete Q84, R2742.

(2009/12/17)

P.14 PCH (3 of 9)-DMI/FDI	Change D112 direction.
P.50 M93/ PARK-S3 POWER	Change one 0805 resistor to two 0402 resistors for layout placement space.
P.40 ADP3211_GFX_CORE/ VGA_CORE	Change R2660 size from 0402 to 0805 for VCC_AXG_SENSE/ VSS_AXG_SENSE routing.

(2009/12/21)

P.46 EMI/Spring/Boss	EMC add EC103, EC106~EC117 for 3D3V_S0, 3D3V_S5, 5V_S5, 1D5V_S3, 1V_VGA, 1D5V_VGA.
P.8 CPU SFF(5 of 8)-PWR/DDR/GFX	Delete C1282, C1281 and change C1264, C1265 to 4.7uF for layout placement space.
P.50 M93/ PARK-S3 POWER	Delete C834, C807, C800, C811, C816, C815, C737, C799 and change C789 to 4.7uF for layout placement space.
P.46 EMI/Spring/Boss	Delete EC80, EC79, EC82, EC59, EC58, EC51, EC12, SPR2 for layout placement space.
P.31 KBC_NPCE781L / KB	Change PCB version setting for power saving in S5.
P.39 RT8209_1D05V	Add VTT_PWRGD pull-up resistor.
P.37 [RT8223_5V/3D3V]	Because the shortage of FDMC8296, change U100, U101 to FDMC7692.

(2010/01/09)

P.17 PCH (6 of 9)-GPIO/RSVD	[BOM Change] change Q92 from transistor to MOS 2N7002 and change C1411 from 0.047uF to 0.1uF.
P.33 RUN POWER	[BOM Change] change Q94, Q95 from transistor to MOS 2N7002.

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(2010/01/21)

P.38 [RT8209_1D5V]	[BOM change] R2409 change from 30Kohm to 31.6Kohm.
P.37 [RT8223_5V/3D3V]	[BOM change] R2393 change from 30Kohm to 31.6Kohm.

(2010/01/25)

P.13 [PCH (2 of 9)-PCIE/CLK/SMB]	[BOM change] C1023, C1024 change from 18pF to 15pF.
P.49 [M93/ PARK-S3 IO]	[BOM change] C719, C721 change from 10pF to 12pF.
P.32 [BIOS & SW/C & BAT ID & Felic]	[BOM change] Add EC83, EC84 to 330pF for EMC request.

(2010/01/29)

P.23 [LCD CONN]	[BOM change] Change DIS brightness source to EC control.
P.46 [EMI/Spring/Boss]	Add EC51, 58,59 to 0.1uF for EMC request.

(2010/02/03)

P.24 [HDD CONN & TOUCHPAD]	Change R2701 to 91Kohm and add C1417 to 2,2uF for HDD protection.
P.33 [RUN POWER]	[BOM change] change R2779 to 100Kohm for 1D5V_S0_PWRGD.
P.42 [G9661_1D8V/ RT9026_0D75]	[BOM change] change R2780 to 0ohm for 1D5V_S0_PWRGD.

(2010/02/04)

P.36 [ADP3211_CPU CORE]	Change TC60 from EL CAP to POSCAP and change R2593 to 91Kohm.
P.37 [RT8223_5V/3D3V]	Change R2384 to 75Kohm and change R2385 to 97.6Kohm.
P.39 [RT8209_1D05V]	Change R2421 to 10.2Kohm.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Modify +VGA_CORE feedback trace connection and change C1373 to 820pF
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Change R2645 to 8.66Kohm for GFX.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Change R2657 to 63.4Kohm and cahnge R2647 to 6.65Kohm for VGA.
P.45 [UVP Protect]	Change Q72 to P-MOSFET and add R2816, R2817 to 200Kohm.
P.36 [ADP3211_CPU CORE]	Dummy R2613.
	Close all open power gaps.

(2010/02/05)

P.31 [KBC_NPCE781L / KB]	Change R2714 to 20Kohm for PCB version.
P.33 [RUN POWER]	Add a dummy resistor R2818 to 100Kohm.
	Close all open power gaps.

(2010/02/08)

P.14 [PCH (3 of 9)-DMI/FDI]	Change R2812 to 165Kohm.
P.49 [M93/ PARK-S3 IO]	Change R2562, R2563 options to PARK.
P.50 [M93/ PARK-S3 POWER]	Change L75, R2426, C783, C867 options to M93.
P.50 [M93/ PARK-S3 POWER]	Change L58, C841, C877, C842, C843 options to PARK.
P.52 [M93/ PARK-S3 Memory / Straps]	Change R665 to 243ohm, R617 to 0ohm, C889 to 2.2nF for M93.
P.41 [APL5930_1V]	Change R2483 to 59Kohm for M93.
P.50 [M93/ PARK-S3 POWER]	Delete C810 for placement space.
P.33 [RUN POWER]	Cahnge Q94 to transister, C1412 to 1uF, R2818 to 330Kohm and stuff it.
P.31 [KBC_NPCE781L / KB]	Add R2819 pull-up to 3D3V_AUX_S5 and change C364 to 1uF for vender request.
P.24 [HDD CONN & TOUCHPAD]	Modify R2701pull-up to 5V_AUX_S5 and dummy D105.
P.47 [ATI POWER]	Change 3D3V_VGA solution from MOS to switch.

(2010/02/09)

P.42 [RT8015_1D8V/ RT9026_0D75]	Change 1D8V_S0 power solution to RT8015.
P.46 [EMI/Spring/Boss]	Add EC118 to 0.1uF at AD+ for EMC request.
P.47 [ATI POWER]	Change 1D8V_VGA power solution and R2558 to 1Kohm.
P.7 [CPU SFF(4 of 8)-POWER/VTT]	Delete C1238 for placement space.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Add R2823 to 267Kohm and dummy R2689.
P.14 [PCH (3 of 9)-DMI/FDI]	Change U139 VCC to 3D3V_AUX_S5.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Change D107 to 83.R2004.B8F and R2786 to 47Kohm.
P.41 [APL5930_1V]	Change D108 to 83.R2004.B8F and R2480 to 10Kohm.
P.12 [PCH (1 of 9)-SATA/RTC/HDA]	Change R2733~R2737 to 56ohm.
P.47 [ATI POWER]	Modify 3D3V_VGA solution.

(2010/02/10)

P.47 [ATI POWER]	Change R2824 pull up to 3D3V_S5.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Change R2642 pull up to 3D3V_S5.
P.47 [ATI POWER]	Change R2558 to 0ohm, delete D109, R2788, C1415.
P.12 [PCH (1 of 9)-SATA/RTC/HDA]	Change C1008, C1009 to 5pF.
P.13 [PCH (2 of 9)-PCIE/CLK/SMB]	Delete EC91 for placement space.
P.16 [PCH (5 of 9)-PCI/USB]	Delete EC93 for placement space.
P.31 [KBC_NPCE781L / KB]	Delete C363 for placement space.
P.50 [M93/ PARK-S3 POWER]	Stuff C821 to 1uF.
P.47 [ATI POWER]	Change Q100 to AO3415.
P.24 [HDD CONN & TOUCHPAD]	Change Q77 to AO3419.
P.17 [PCH (6 of 9)-GPIO/RSVD]	Stuff R2298 to 54.9ohm and dummy RN120 for THERMTRIP#.
P.33 [RUN POWER]	Stuff R167 to 56ohm for THERMTRIP#.
P.5 [CPU SFF(2 of 8)-CLK/Thermal]	Stuff R2305 to 0ohm for PROCHOT#.

(2010/02/11)

P.42 [RT8015_1D8V/ RT9026_0D75]	Add more one gap G330 for 1D8V_S0.
P.42 [RT8015_1D8V/ RT9026_0D75]	Add EC119 to 0.1uF for EMC request.

(2010/02/22)

P.41 [APL5930_1V]	Change R2479 to 10Kohm for vga sequence.
P.47 [ATI POWER]	Change C743 to 0.01uF, R583 to 47Kohm and R655 to 4.7Kohm for vga sequence.
P.33 [RUN POWER]	Dummy R2818.

(2010/02/23)

P.17 [PCH (6 of 9)-GPIO/RSVD]	Dummy R2298 and stuff RN120 for THERMTRIP#.
P.33 [RUN POWER]	Dummy R167 for THERMTRIP#.
P.47 [ATI POWER]	Change U94 to AO4430 Rds=5.5~7.5mohm
P.31 [KBC_NPCE781L / KB]	Change U135 to G691L293T73UF.

(2010/02/24)

P.38 [RT8209_1D5V]	[BOM change] R2409 change from 31.6Kohm to 30Kohm.
P.43 [BQ24751_Charger]	[BOM change] R2512 change from 120Kohm to 63.4Kohm for DIS.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] R2823 change from 267Kohm to 160Kohm for DIS.

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(2010/03/18)

P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Modify +VGA_CORE feedback trace connection.
P.14 [PCH (3 of 9)-DMI/FDI]	Change U139 VCC from 3D3V_AUX_S5 to 5V_AUX_S5.

(2010/03/22)

P.31 [KBC_NPCE781L / KB]	[BOM change] Dummy R142 double pull low.

(2010/03/24)

P.47 [ATI POWER]	[BOM change] Change U94 toSI4168 Rds=5.7~7.6mohm.
P.33 [RUN POWER]	Delete R2818 and change Q10 pin5 connection to PM_SLP_S3_CTL.

(2010/03/25)

P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Change R2642 to 100Kohm for VGA sequence.
P.41 [APL5930_1V]	[BOM change] Change R2479 to 100Kohm for VGA sequence.
P.47 [ATI POWER]	[BOM change] Change D110 to RB751V for VGA sequence.
P.47 [ATI POWER]	[BOM change] C1419 to 0.22uF for VGA sequence PARK only.

(2010/03/29)

P.24 [HDD CONN & TOUCHPAD]	[BOM change] Change R2701 to 133Kohm and change R2702 to 3.3Kohm for HDD protection sequence.
P.24 [HDD CONN & TOUCHPAD]	Add C1379 to 0.1uF for HDD protection sequence.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Change R2660 0ohm resistor to 0805 size.

(2010/03/30)

P.36 [ADP3211_CPU CORE]	Change U127 to TPCA8030 and change U128, U129 to TPCA8028 for VCC_CORE quality.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Dummy R2823 and add R2689 to 100Kohm for VGACORE level.

(2010/03/31)

P.31 [KBC_NPCE781L / KB]	Add CP and CP2 option circuit.
Change 0ohm resistors to 0ohm pads	0402-pad: R2547, R2732, R2566, R2553, R2568, R2567, R2574, R2552, R2554, R2572, R2550, R2570, R2549, R2731, R2569, R2551, R2578, R2548 0603-pad: R2669, R2246, R2247

(2010/04/01)

P.38 [RT8209_1D5V]	[BOM change] Change R2411 to 10Kohm and change R2409 to 10.2Kohm to rise 1% of 1D5V_S3 level.
P.49 [M93/ PARK-S3 IO]	[BOM change] C719, C721 change to 6.8pF.
P.13 [PCH (2 of 9)-PCIE/CLK/SMB]	[BOM change] C1023, C1024 change to 12pF.

(2010/04/02)

P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Change R2659, R2698 to 0ohm resistor for VGA_CORE transition overshoot.

(2010/04/07)

P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Change C1414 0.1UF capacitor from Y5V to X7R.

(2010/04/12)

P.49 [M93/ PARK-S3 IO]	[BOM change] Add 2nd source for X7.

MP

(2010/04/21)

P.19 [PCH (8 of 9)-PWR\SATA\USB]	Change VCCSUSHDA power plane to 1.5V_S5.

(2010/04/24)

P.19 [PCH (8 of 9)-PWR\SATA\USB]	Add R2826 dummy pull low resistor for enable pin.

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