

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

Diagram illustrating the system architecture, including components like AMD K8 Rev.G S1g1 Socket, ATI RS690M, ATI SB600, G792, CLK GEN., DDR2 SODIMM, Power Switch, New card, Mini Card, LAN, RJ45, TXFM, INT. MIC Array, Codec ALC268, AMP G1432Q, INT. SPKR, AMP G1410Q, Line Out (No-SPDIF), MODEM MDC Card, RJ11, HDD, CDRM, USB 4 Port, MINI USB BlueTooth, Finger print, CCD .3M/1.3M, KBC Winbond WPC8768L, BIOS W25X80-VSS, LPC DEBUG CONN., Touch Pad, INT. KB, and FIR. The diagram shows connections between these components and various buses (HyperTransport, PCI-E, PCI BUS, LPC BUS, AZALIA).

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

Diagram illustrating the system architecture, including components like AMD K8 Rev.G S1g1 Socket, ATI RS690M, ATI SB600, G792, CLK GEN., DDR2 SODIMM, Power Switch, New card, Mini Card, LAN, RJ45, TXFM, INT. MIC Array, Codec ALC268, AMP G1432Q, INT. SPKR, AMP G1410Q, Line Out (No-SPDIF), MODEM MDC Card, RJ11, HDD, CDRM, USB 4 Port, MINI USB BlueTooth, Finger print, CCD .3M/1.3M, KBC Winbond WPC8768L, BIOS W25X80-VSS, LPC DEBUG CONN., Touch Pad, INT. KB, and FIR. The diagram shows connections between these components and various buses (HyperTransport, PCI-E, PCI BUS, LPC BUS, AZALIA).

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

Diagram illustrating the system architecture, including components like AMD K8 Rev.G S1g1 Socket, ATI RS690M, ATI SB600, G792, CLK GEN., DDR2 SODIMM, Power Switch, New card, Mini Card, LAN, RJ45, TXFM, INT. MIC Array, Codec ALC268, AMP G1432Q, INT. SPKR, AMP G1410Q, Line Out (No-SPDIF), MODEM MDC Card, RJ11, HDD, CDRM, USB 4 Port, MINI USB BlueTooth, Finger print, CCD .3M/1.3M, KBC Winbond WPC8768L, BIOS W25X80-VSS, LPC DEBUG CONN., Touch Pad, INT. KB, and FIR. The diagram shows connections between these components and various buses (HyperTransport, PCI-E, PCI BUS, LPC BUS, AZALIA).

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

Diagram illustrating the system architecture, including components like AMD K8 Rev.G S1g1 Socket, ATI RS690M, ATI SB600, G792, CLK GEN., DDR2 SODIMM, Power Switch, New card, Mini Card, LAN, RJ45, TXFM, INT. MIC Array, Codec ALC268, AMP G1432Q, INT. SPKR, AMP G1410Q, Line Out (No-SPDIF), MODEM MDC Card, RJ11, HDD, CDRM, USB 4 Port, MINI USB BlueTooth, Finger print, CCD .3M/1.3M, KBC Winbond WPC8768L, BIOS W25X80-VSS, LPC DEBUG CONN., Touch Pad, INT. KB, and FIR. The diagram shows connections between these components and various buses (HyperTransport, PCI-E, PCI BUS, LPC BUS, AZALIA).

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

Diagram illustrating the system architecture and components, including:

- Processor:** AMD K8 Rev.G S1g1 Socket (4,5,6,7)
- Chipset:** ATI RS690M (10,11,12,13) and ATI SB600 (16,17,18,19,20)
- Memory:** DDR2 SODIMM DIMM1 (8,9) and DIMM2 (8,9)
- Storage:** HDD (21), CDRM (21), and various USB ports (22)
- Peripherals:** G792 (36), CLK GEN. (3), S-Vedio (13), CRT (13), LCD (14), LAN (23), RJ45 (24), TXFM (24), INT. MIC Array, Codec ALC268 (29), AMP G1432Q (30), INT. SPKR, AMP G1410Q (30), Line Out (No-SPDIF), MODEM MDC Card (22), RJ11 (22), Finger print (22), CCD .3M/1.3M (14), KBC Winbond WPC8768L (31), BIOS W25X80-VSS (33), LPC DEBUG CONN. (33), Touch Pad (32), INT. KB (32), and FIR (31).
- Buses:** HyperTransport, PCI-E x 1, PCI-E x 4, PCI BUS, LPC BUS, and AZALIA.
- Power Management:** Power Switch P2231NFC1 (28), PWR SW CP2211F (25), and 1394 CONN (27).
- Connectivity:** Mini Card (802.11a/b/g/n), LAN (10/100/1000 BCM5787M), and various USB ports.

Legend:

- 5: DIMM1
- 4: DIMM2
- 3: CLK GEN.
- 2: G792
- 1: AMD K8 Rev.G S1g1 Socket

Variant Name: Orta

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Block Diagram

Size: A3
Date: Tuesday, December 12, 2006
Sheet: 1 of 46

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

Diagram illustrating the system architecture, including components like AMD K8 Rev.G S1g1 Socket, ATI RS690M, ATI SB600, G792, CLK GEN., DDR2 SODIMM, Power Switch, New card, Mini Card, LAN, RJ45, TXFM, INT. MIC Array, Codec ALC268, AMP G1432Q, INT. SPKR, AMP G1410Q, Line Out (No-SPDIF), MODEM MDC Card, RJ11, HDD, CDRM, USB 4 Port, MINI USB BlueTooth, Finger print, CCD .3M/1.3M, KBC Winbond WPC8768L, BIOS W25X80-VSS, LPC DEBUG CONN., Touch Pad, INT. KB, and FIR. The diagram shows connections between these components and various buses (HyperTransport, PCI-E, PCI BUS, LPC BUS, AZALIA).

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

Diagram illustrating the system architecture, including components like AMD K8 Rev.G S1g1 Socket, ATI RS690M, ATI SB600, G792, CLK GEN., DDR2 SODIMM, Power Switch, New card, Mini Card, LAN, RJ45, TXFM, INT. MIC Array, Codec ALC268, AMP G1432Q, INT. SPKR, AMP G1410Q, Line Out (No-SPDIF), MODEM MDC Card, RJ11, HDD, CDRM, USB 4 Port, MINI USB BlueTooth, Finger print, CCD .3M/1.3M, KBC Winbond WPC8768L, BIOS W25X80-VSS, LPC DEBUG CONN., Touch Pad, INT. KB, and FIR. The diagram shows connections between these components and various buses (HyperTransport, PCI-E, PCI BUS, LPC BUS, AZALIA).

[illegible][illegible]

Orta Block Diagram

The main block diagram illustrates the system architecture centered around the AMD K8 Rev.G S1g1 Socket. Key components include:

- Memory:** Two DDR2 SODIMM modules (DIMM1, DIMM2) connected via DDR II 533/667/800.
- GPU:** G792 graphics card connected to the socket.
- Clock:** CLK GEN. ICS 9LPRS502 (RTM875T-605) providing a 14.318MHz signal.
- Chipsets:** ATI RS690M (Northbridge) and ATI SB600 (Southbridge) connected via HyperTransport and PCI-E x4.
- Peripherals:** Various interfaces including PCI-E x1 (New card, Mini Card), LAN (BCM5787M), INT. MIC Array, Codec ALC268, AMP G1432Q/G1410Q, MODEM MDC Card, HDD, CDROM, USB x4, MINI USB Bluetooth, Finger print, CCD .3M/1.3M, Touch Pad, INT. KB, FIR, and LPC DEBUG CONN.

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

~Variant Name~

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsiehshih, Taipei

Title BLOCK DIAGRAM		
Size A3	Document Number Orta	Rev SA
Date Tuesday, December 12, 2006	Sheet 1	of 46

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

The main block diagram illustrates the system architecture centered around the AMD K8 Rev.G S1g1 Socket. Key components include:

- Memory:** Two DDR2 SODIMM modules (DIMM1, DIMM2) connected via DDR II 533/667/800.
- GPU:** G792 graphics card connected to the socket.
- Clock:** CLK GEN. ICS 9LPRS502 (RTM875T-605) providing a 14.318MHz signal.
- Chipsets:** ATI RS690M (Northbridge) and ATI SB600 (Southbridge) connected via HyperTransport and PCI-E x4.
- Peripherals:** Various interfaces including PCI-E x1 cards (New card, Mini Card, LAN BCM5787M), USB ports, SATA drives (HDD, CDROM), audio (Codec ALC268, AMPs), modem, and fingerprint sensor.

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

hexainf@hotmail.com
GRATIS - FOR FREE

Orta Block Diagram

The main block diagram illustrates the system architecture centered around the AMD K8 Rev.G S1g1 Socket. Key components include:

- Memory:** Two DDR2 SODIMM modules (DIMM1, DIMM2) connected via DDR II 533/667/800.
- GPU:** G792 graphics card connected to the socket.
- Clock:** CLK GEN. ICS 9LPRS502 (RTM875T-605) providing a 14.318MHz signal.
- Chipsets:** ATI RS690M (Northbridge) and ATI SB600 (Southbridge) connected via HyperTransport and PCI-E x4.
- Peripherals:** Various interfaces including PCI-E x1 slots for New card, Mini Card, and LAN (BCM5787M); USB ports; SATA drives (HDD, CDROM); Audio (Codec ALC268, AMP G1432Q, AMP G1410Q); Modem MDC Card; and Finger print sensor.

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

~Variant Name~

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsiehih, Taipei	
Title	BLOCK DIAGRAM		
Size	A3	Document Number	Orta
Date:	Tuesday, December 12, 2006	Sheet	1 of 46

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

hexainf@hotmail.com
GRATIS - FOR FREE

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

The main block diagram illustrates the internal architecture of the Orta laptop. At the top center is the **AMD K8 Rev.G S1g1 Socket**, which connects to two **DDR2 SODIMM** modules (DIMM1 and DIMM2) via **DDR II 533/667/800** memory buses. To the right of the socket is the **G792** graphics processor. Below the socket is the **ATI RS690M** northbridge, which interfaces with the **ATI SB600** southbridge via a **PCI-E x 4** bus. The northbridge also manages the **HyperTransport** link to the CPU and controls the **CLK GEN.** (ICS 9LPRS502) providing a **14.318MHz** clock. Various expansion cards are connected to the northbridge through **PCI-E x 1** slots, including a **New card**, **Mini Card**, and **LAN** (BCM5787M). The southbridge handles multiple **USB** ports (including a 4-port hub), **MINI USB Bluetooth**, **Finger print**, **CDDROM**, **SATA**, and **PATA** interfaces. It also manages the **Codec ALC268** for audio and the **MODEM MDC Card**. Other components include a **Power Switch**, **RJ45** port, **TXFM**, **HDD**, and various connectors for external devices like **S-Vedio**, **CRT**, and **LCD**.

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

hexainf@hotmail.com

GRATIS - FOR FREE

Size A3 Title BLOCK DIAGRAM Document Number Orta Date Tuesday, December 12, 2006 Sheet 1 of 46 Rev SA

<Variant Name>

wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsiehih, Taipei

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

[illegible]

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

Diagram illustrating the system architecture and components, including:

- Processor:** AMD K8 Rev.G S1g1 Socket (4,5,6,7)
- Chipset:** ATI RS690M (10,11,12,13) and ATI SB600 (16,17,18,19,20)
- Memory:** DDR2 SODIMM DIMM1 (8,9) and DIMM2 (8,9)
- Storage:** HDD (21), CDROM (21), and various USB ports (22)
- Peripherals:** G792 (36), CLK GEN. (3), S-Vedio (13), CRT (13), LCD (14), LAN (23), RJ45 (24), TXFM (24), INT. MIC Array, Codec ALC268 (29), AMP G1432Q (30), AMP G1410Q (30), INT. SPKR, Line Out (No-SPDIF), MODEM MDC Card (22), RJ11 (22), Finger print (22), CCD .3M/1.3M (14), KBC Winbond WPC8768L (31), BIOS W25X80-VSS (33), LPC DEBUG CONN. (33), Touch Pad (32), INT. KB (32), and FIR (31)
- Buses:** HyperTransport, PCI-E x 1, PCI-E x 4, PCI BUS, LPC BUS, and AZALIA
- Power Management:** Power Switch P2231NFC1 (28), PWR SW CP2211F (25), and 1394 CONN (27)
- Connectivity:** Mini Card (802.11a/b/g/n), LAN (10/100/1000 BCM5787M), and various USB ports

Variant Name: **Orta**

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Block Diagram
Document Number: Orta
Date: Tuesday, December 12, 2006
Sheet: 1 of 46

Orta Block Diagram

The main block diagram illustrates the internal architecture of the Orta system. At the top center is the **AMD K8 Rev.G S1g1 Socket**, which connects to two **DDR2 SODIMM** modules (DIMM1 and DIMM2) via **DDR II 533/667/800**. Below the socket is the **ATI RS690M** graphics chip, connected to the AMD socket via **HyperTransport** (16x16). The ATI RS690M also interfaces with a **CLK GEN.** (ICS 9LPRS502) providing a **14.318MHz** clock. To the left of the ATI RS690M are several expansion slots: **New card**, **Mini Card**, and **LAN BCM5787M**, all connected via **PCI-E x 1**. A **Power Switch P2231NFC1** is also shown. Below the LAN module is an **INT. MIC Array** connected to a **Codec ALC268** and an **AMP G1432Q**. The **ATI SB600** southbridge is connected to the ATI RS690M via **PCI-E x 4**. It manages multiple **USB** ports (4 Port, Mini USB Bluetooth), a **Finger print** sensor, a **CDDROM**, and a **PATA** interface. The southbridge also handles audio through **AZALIA** and **CODEC** components, including **AMP G1410Q** and **MODEM MDC Card**. On the right side, the southbridge connects to a **KBC Winbond WPC8768L** (BIOS), which in turn controls a **LPC DEBUG CONN.** and interfaces with a **Touch Pad**, **INT. KB**, and **FIR**. Other components include a **G792** GPU, a **S-Vedio** output, **CRT**, and **LCD** displays. Various other connectors like **RJ45**, **TxFM**, **RJ11**, and **HDD** are also depicted.

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

~Variant Name~

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsiehshih, Taipei

BLOCK DIAGRAM		
Title		
Size	Document Number	Rev
A3	Orta	SA
Date:	Tuesday, December 12, 2006	Sheet 1 of 46

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

AMD K8 Rev.G S1g1 Socket (4,5,6,7) connected to **DDR2 SODIMM** (DIMM1, DIMM2) via **DDR II 533/667/800**. The socket is connected to **ATI RS690M** (10,11,12,13) via **HyperTransport** (16x16) and **PCI-E x 4**. The **ATI RS690M** is connected to **ATI SB600** (16,17,18,19,20) via **PCI-E x 4**. The **ATI SB600** is connected to **02 0Z711** (25,26) via **PCI BUS** (24.576MHz, 25MHz, 32.768KHz) and **LPC BUS**. The **02 0Z711** is connected to **PCMCIA I/F** (27) and **1394 Cardbus Cardreader** (25,26). The **PCMCIA I/F** is connected to **PCMCIA SLOT Support TypeII** (27). The **1394 Cardbus Cardreader** is connected to **MS/MS Pro/xD/MMC/SD/SDIO** (6 in 1, 27). The **MS/MS Pro/xD/MMC/SD/SDIO** is connected to **KBC Winbond WPC8768L** (31) via **LPC BUS**. The **KBC Winbond WPC8768L** is connected to **BIOS W25X80-VSS** (33) via **SPI I/F** and **LPC DEBUG CONN.** (33). The **KBC Winbond WPC8768L** is connected to **Touch Pad** (32), **INT. KB** (32), and **FIR** (31). The **ATI SB600** is connected to **CODEC ALC268** (29) via **AZALIA**. The **CODEC ALC268** is connected to **AMP G1432Q** (30) and **AMP G1410Q** (30). The **AMP G1432Q** is connected to **INT. SPKR** (30). The **AMP G1410Q** is connected to **Line Out (No-SPDIF)** (30). The **CODEC ALC268** is connected to **MODEM MDC Card** (22) via **RJ11** (22). The **MODEM MDC Card** is connected to **HDD** (21) via **SATA** and **CDROM** (21) via **PATA**. The **ATI SB600** is connected to **USB x 4** (22), **MINI USB Bluetooth** (22), and **Finger print** (22). The **ATI SB600** is connected to **CCD .3M/1.3M** (14) via **USB**. The **ATI SB600** is connected to **CLK GEN.** (3) via **14.318MHz**. The **CLK GEN.** is connected to **G792** (36). The **ATI SB600** is connected to **Power Switch P2231NFC1** (28) via **New card** (28) and **Mini Card** (802.11a/b/g/n, 28) via **PCI-E x 1**. The **ATI SB600** is connected to **LAN** (10/100/1000, BCM5787M, 23) via **PCI-E x 1**. The **LAN** is connected to **RJ45** (24) via **TXFM** (24). The **LAN** is connected to **INT. MIC Array** (25MHz). The **ATI SB600** is connected to **PCB P/N** (48.4U101.0SA) via **REVISION** (06245-SA).

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Orta Block Diagram

Diagram illustrating the system architecture and components, including:

- Processor:** AMD K8 Rev.G S1g1 Socket (4,5,6,7)
- Chipset:** ATI RS690M (10,11,12,13) and ATI SB600 (16,17,18,19,20)
- Memory:** DDR2 SODIMM DIMM1 (8,9) and DIMM2 (8,9)
- Storage:** HDD (21), CDROM (21), and various USB ports (22)
- Peripherals:** G792 (36), CLK GEN. (3), S-Vedio (13), CRT (13), LCD (14), LAN (23), RJ45 (24), TXFM (24), INT. MIC Array, Codec ALC268 (29), AMP G1432Q (30), AMP G1410Q (30), INT. SPKR, Line Out (No-SPDIF), MODEM MDC Card (22), RJ11 (22), Finger print (22), CCD .3M/1.3M (14), KBC Winbond WPC8768L (31), BIOS W25X80-VSS (33), LPC DEBUG CONN. (33), Touch Pad (32), INT. KB (32), and FIR (31)
- Buses:** HyperTransport, PCI-E x 1, PCI-E x 4, PCI BUS, LPC BUS, and AZALIA
- Power Management:** Power Switch P2231NFC1 (28), PWR SW CP2211F (25), and 1394 CONN (27)
- Connectivity:** Mini Card (802.11a/b/g/n), LAN (10/100/1000 BCM5787M), and various USB ports

Variant Name: **Orta**

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Block Diagram
Document Number: Orta
Date: Tuesday, December 12, 2006
Sheet: 1 of 46

Orta Block Diagram

The main block diagram illustrates the internal architecture of the Orta system. At the top center is the **AMD K8 Rev.G S1g1 Socket**, which connects to two **DDR2 SODIMM** modules (DIMM1 and DIMM2) via **DDR II 533/667/800**. Below the socket is the **ATI RS690M** graphics chip, connected to the AMD socket via **HyperTransport** (16x16). The ATI RS690M also connects to the **ATI SB600** southbridge via **PCI-E x 4**. The ATI SB600 manages various interfaces: **USB** (4 ports), **MINI USB Bluetooth**, **Finger print**, **CDDROM** (PATA), **HDD** (SATA), **MODEM MDC Card** (RJ11), **Line Out (No-SPDIF)**, **AMP G1410Q**, **INT. SPKR**, **AMP G1432Q**, **MIC In**, **Codec ALC268**, **LAN BCM5787M** (RJ45/TXFM), **Mini Card** (802.11a/b/g/n), **New card** (PCI-E x 1), **Power Switch P2231NFC1**, and **CLK GEN.** (ICS 9LPRS502, RTM875T-605) providing **14.318MHz**. The ATI SB600 also connects to the **02 0Z711** 1394 Cardbus Cardreader via **PCI BUS** (24.576MHz, 25MHz, 32.768KHz) and to the **KBC Winbond WPC8768L** via **LPC BUS**. The KBC connects to **BIOS W25X80-VSS** and **LPC DEBUG CONN.**. Other components include **G792**, **S-Vedio**, **CRT**, **LCD**, **PCMCIA I/F**, **PCMCIA SLOT Support TypeII**, **PWR SW CP2211F**, **1394 CONN**, **MS/MS Pro/xD/MMC/SD/SDIO** (6 in 1), **CCD .3M/1.3M**, **Touch Pad**, **INT. KB**, and **FIR**.

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

hexainf@hotmail.com
GRATIS - FOR FREE

Orta Block Diagram

The main block diagram illustrates the system architecture centered around the AMD K8 Rev.G S1g1 Socket. Key components include:

- Memory:** Two DDR2 SODIMM modules (DIMM1, DIMM2) connected via DDR II 533/667/800.
- GPU:** G792 graphics card connected to the socket.
- Clock:** CLK GEN. ICS 9LPRS502 (RTM875T-605) providing a 14.318MHz signal.
- Chipsets:** ATI RS690M (Northbridge) and ATI SB600 (Southbridge).
- Storage & Expansion:** New card, Mini Card, LAN BCM5787M, HDD, CDROM, and various USB ports.
- Audio & Video:** Codec ALC268, AMP G1432Q/G1410Q, INT. MIC Array, INT. SPKR, S-Vedio, CRT, LCD.
- Connectivity:** RJ45, TXFM, RJ11, MODEM MDC Card, Finger print, MINI USB Bluetooth.

PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

14.318MHz

25MHz

24.576MHz

25MHz

32.768KHz

32.768KHz

<Variant Name>

wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsieh, Taipei

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 1 of 46

Orta Block Diagram

The main block diagram illustrates the internal architecture of the Orta system. At the top center is the **AMD K8 Rev.G S1g1 Socket**, which connects to two **DDR2 SODIMM** modules (DIMM1 and DIMM2) via **DDR II 533/667/800**. Below the socket is the **ATI RS690M** graphics chip, connected to the **ATI SB600** southbridge via **HyperTransport** (16x16). The **ATI SB600** manages multiple interfaces: it connects to a **LAN BCM5787M** via **PCI-E x 1**; handles audio through an **Codec ALC268** and **AMP G1432Q/G1410Q** via **AZALIA**; controls storage devices (**HDD**, **CDFROM**) via **SATA**; and manages USB ports (**USB 4 Port**, **MINI USB Bluetooth**, **Finger print**) via **USB**. It also interfaces with a **KBC Winbond WPC8768L** via **LPC BUS**, which includes a **BIOS W25X80-VSS** and an **LPC DEBUG CONN.**

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

G792 36

CLK GEN. ICS 9LPRS502 (RTM875T-605) 3 → 14.318MHz

PCB Layer Stackup

L1: Signal 1	
L2: VCC	
L3: Inner Signal 2	
L4: Inner Signal 3	
L5: GND	
L6: Signal 4	

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

hexainf@hotmail.com
GRATIS - FOR FREE

Orta Block Diagram

Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SA: 07/31/06 Start

- SB change
power team
- 1.change L7, L9 to 68.1R510.10D
 - 2.change U12 to 84.04706.037
 - 3.change R66 to 10K ohm

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

CHANGE HISTORY

Size

A3

Document Number

Orta

Date:

Tuesday, December 12, 2006

Sheet

2

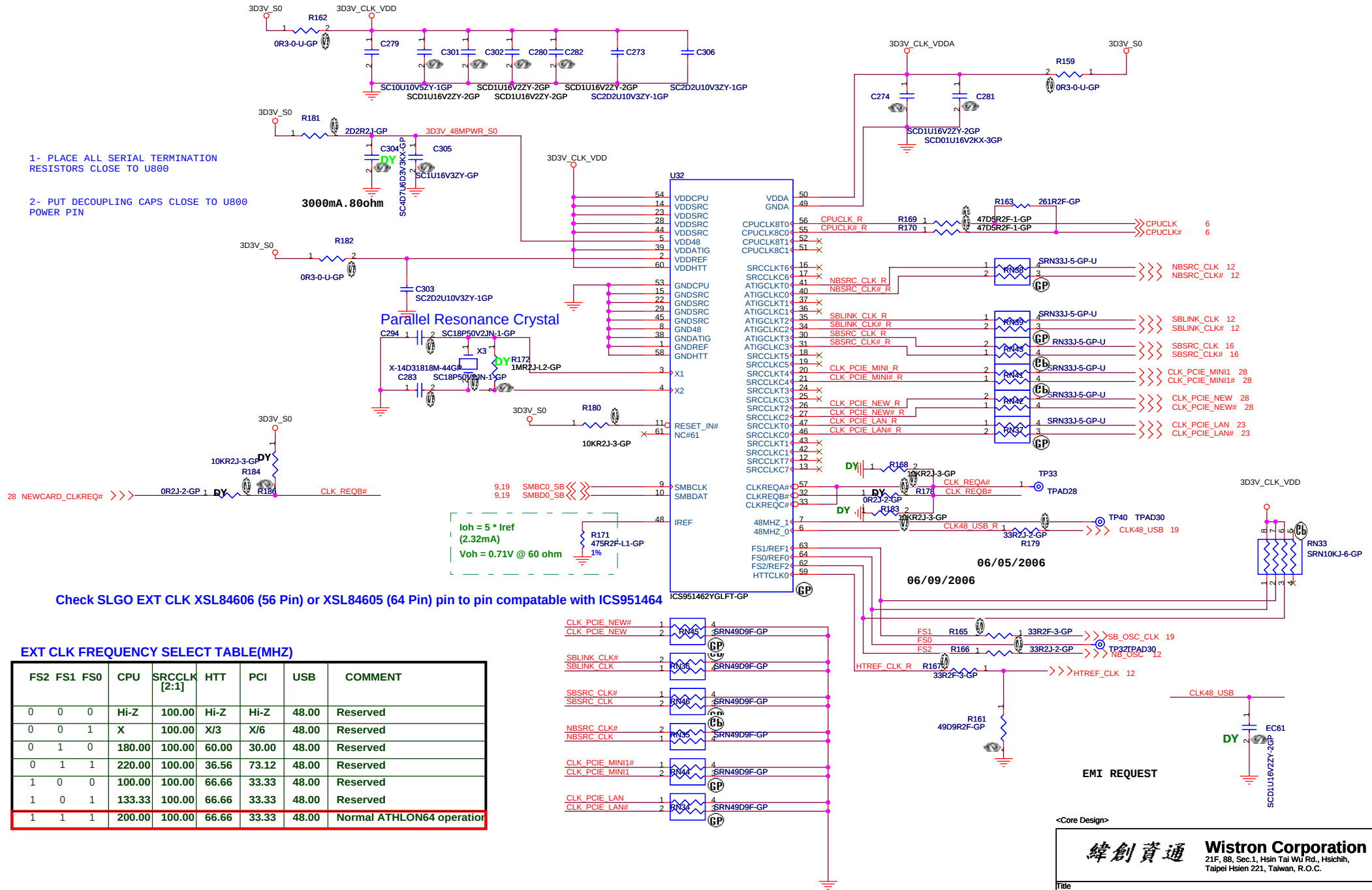
of

46

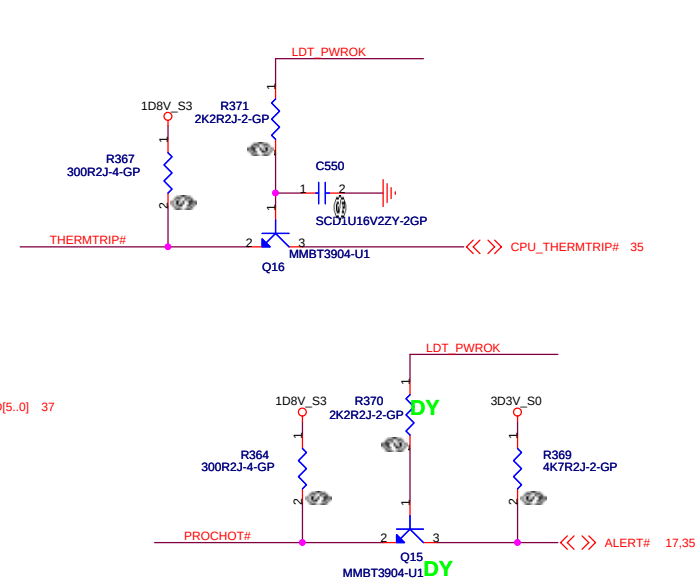
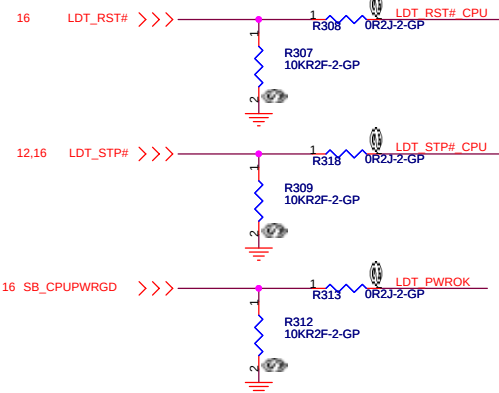
Rev

SA

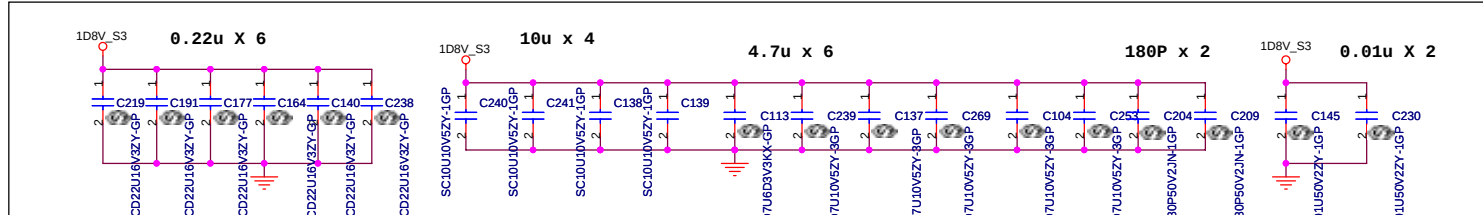
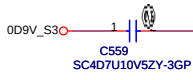
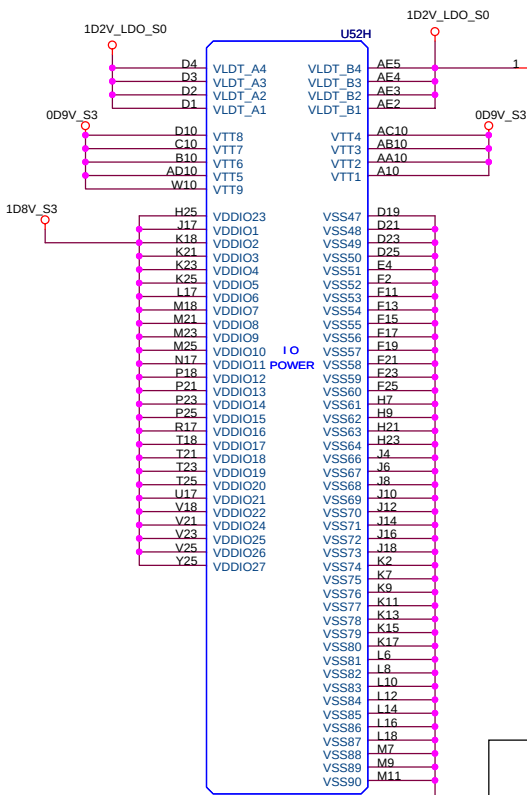
- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN





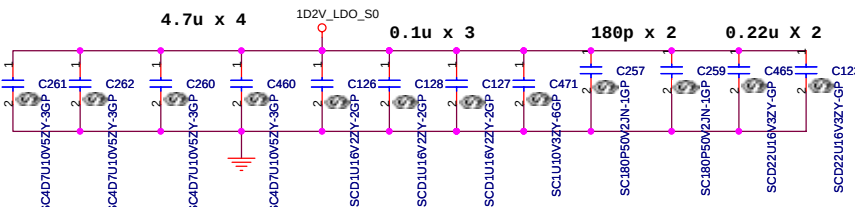
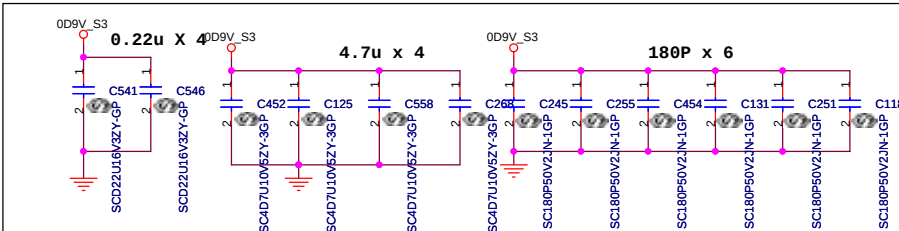
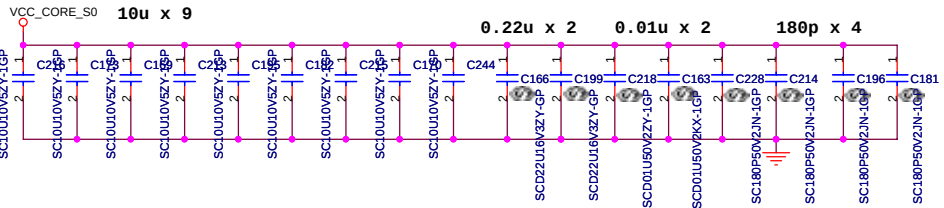
[illegible]

HDT Connectors



Place near to CPU

LAYOUT: Place on backside of processor.

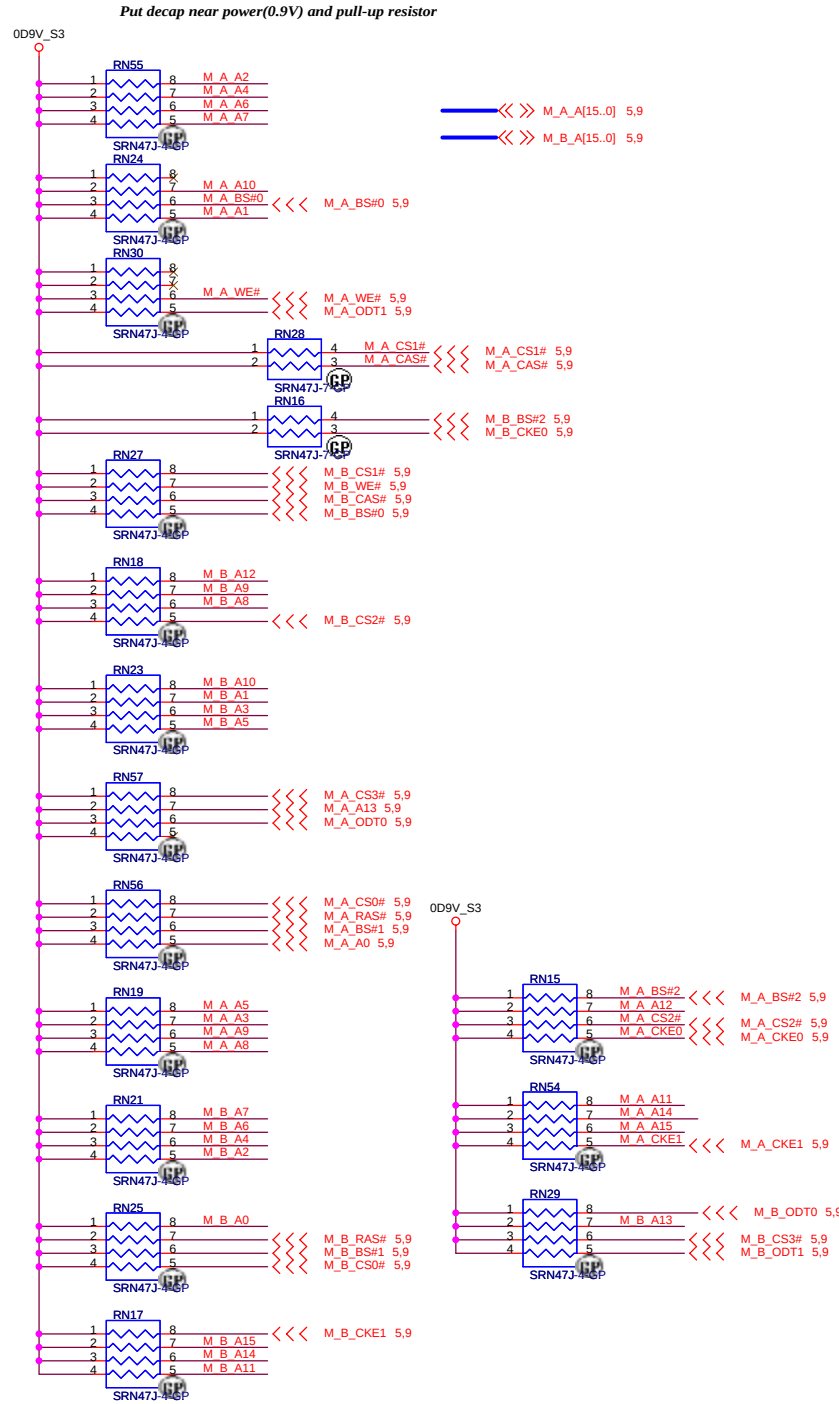


<Core Design>

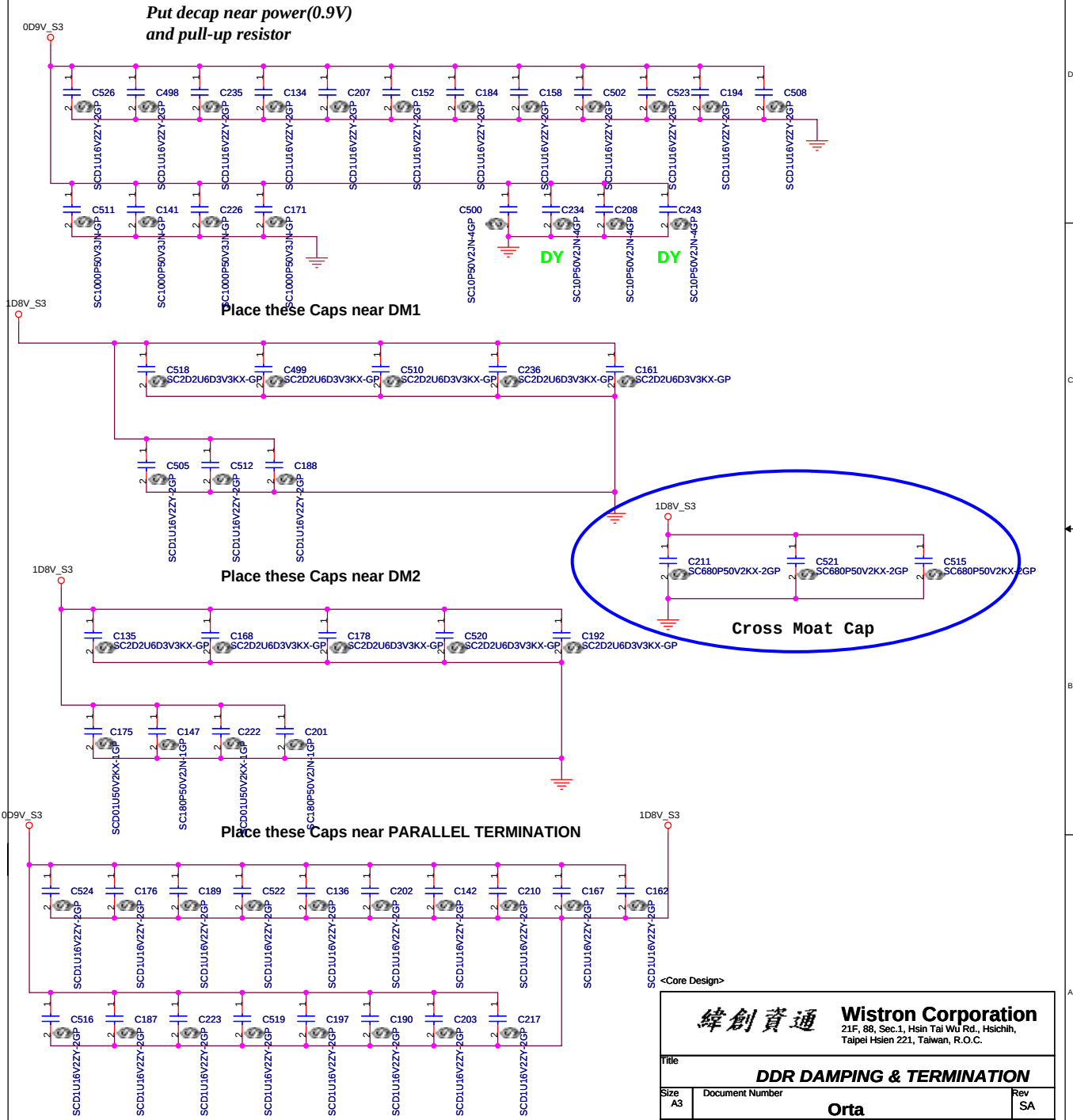
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

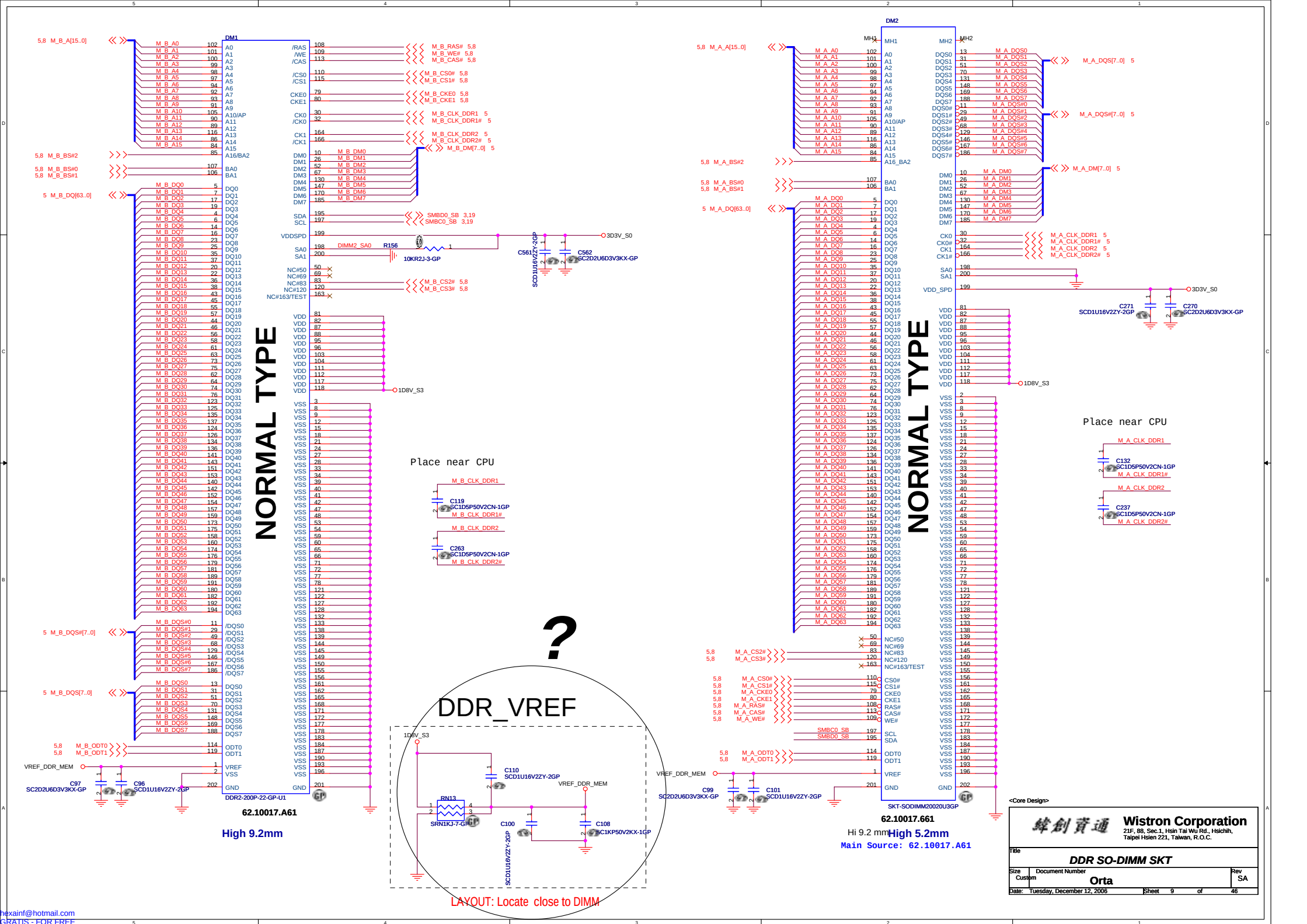
Title		CPU(4/4) Power	
Size A3	Document Number	Rev SA	
Date: Tuesday, December 12, 2006		Sheet 7	of 46

PARALLEL TERMINATION



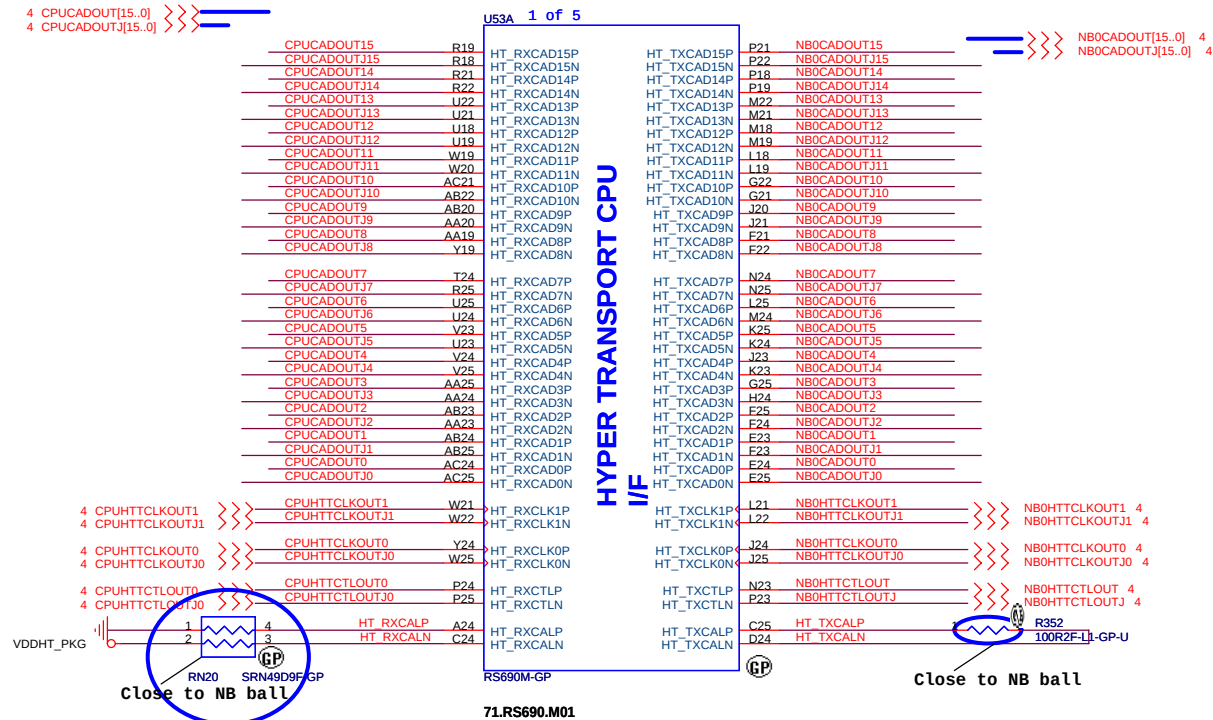
Decoupling Capacitor





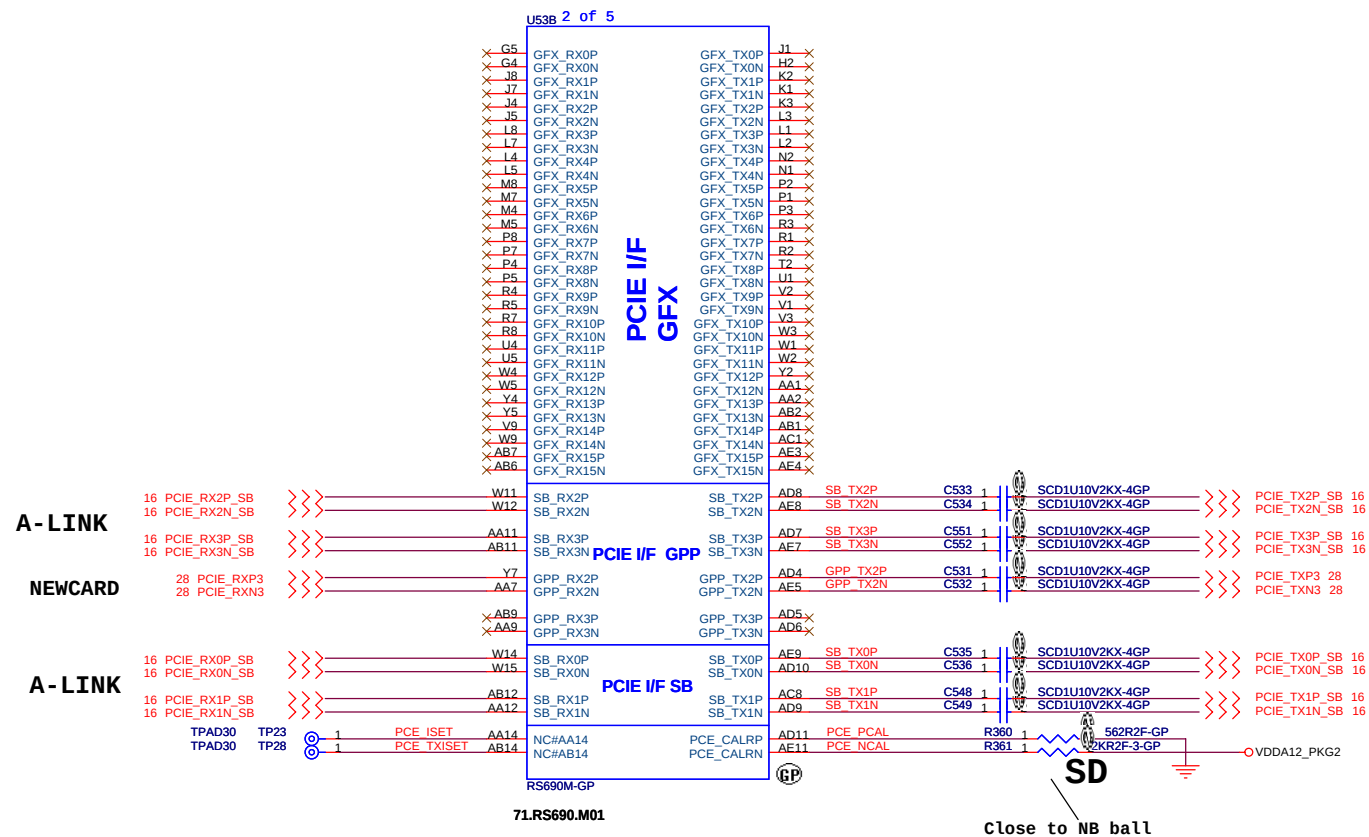
CLAW HAMMER TO NB

NB TO CLAW HAMMER



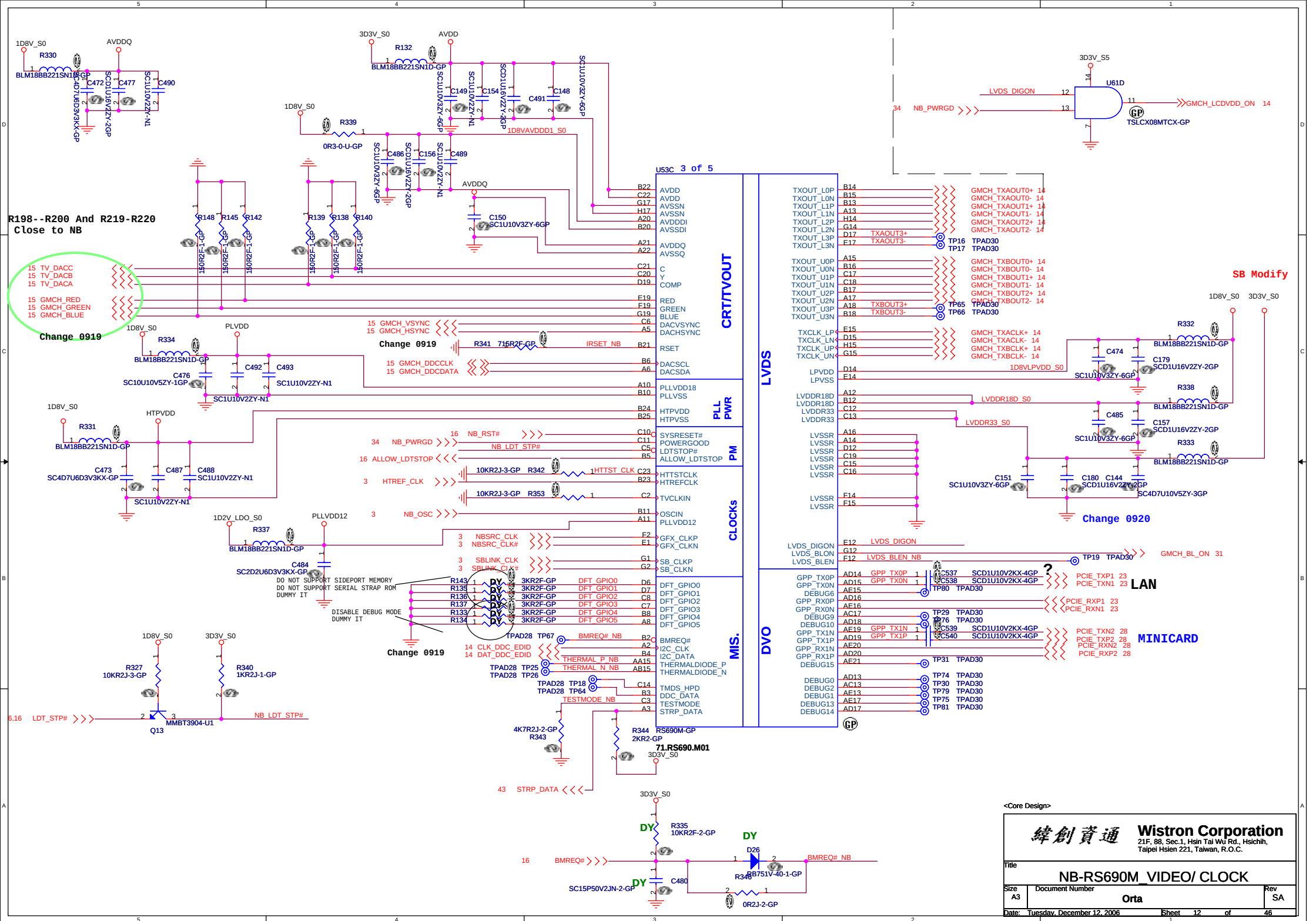
<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NB-RS690M HT			
Size	Document Number	Rev	
A3	Orta	SA	
Date:	Tuesday, December 12, 2006	Sheet	10 of 46

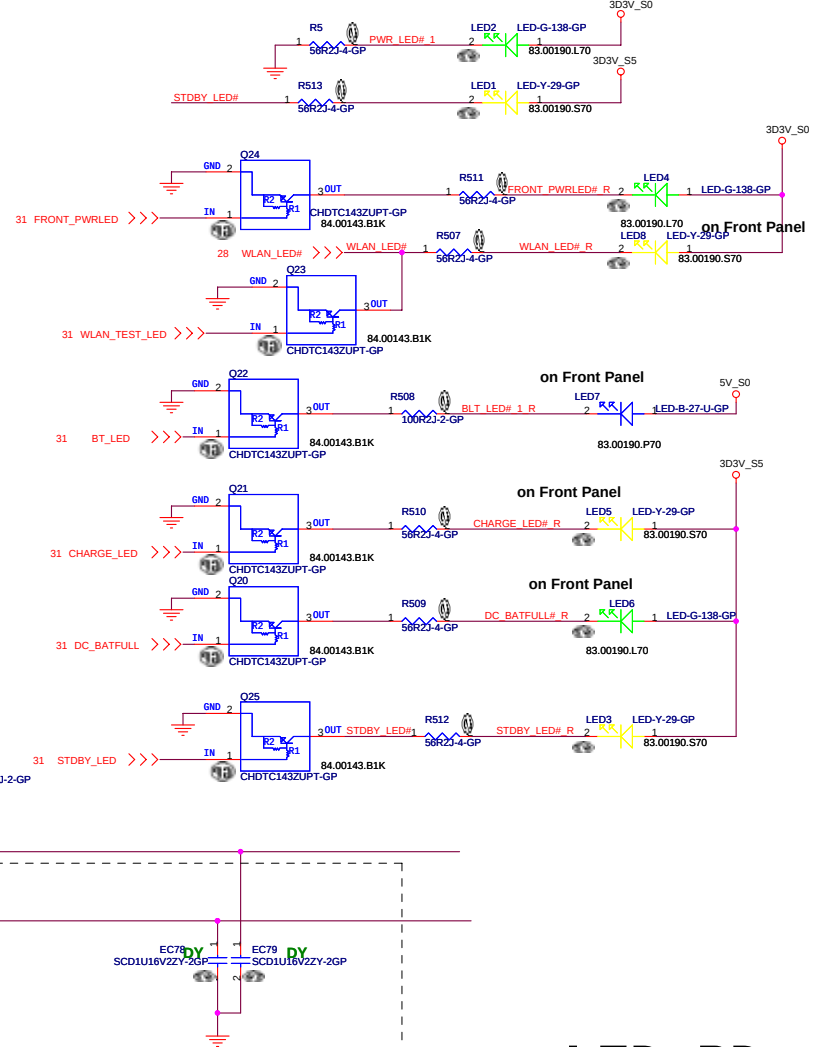
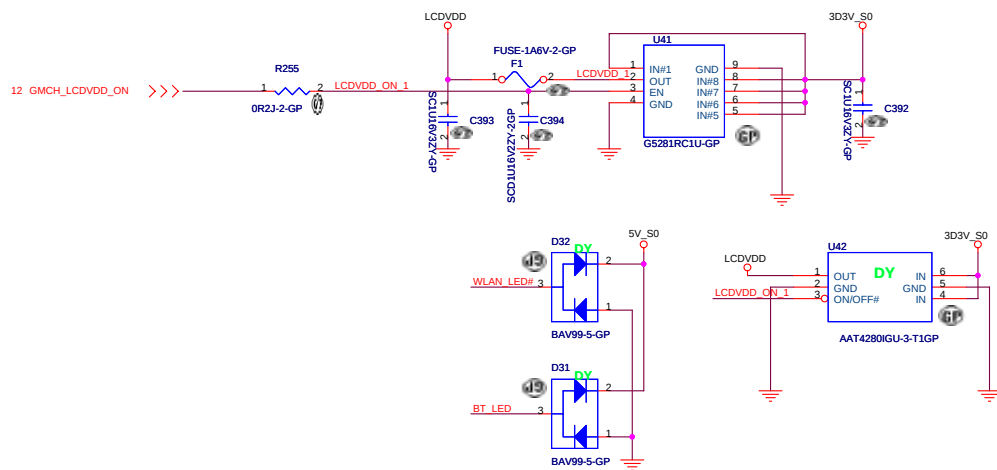


<Core Design>

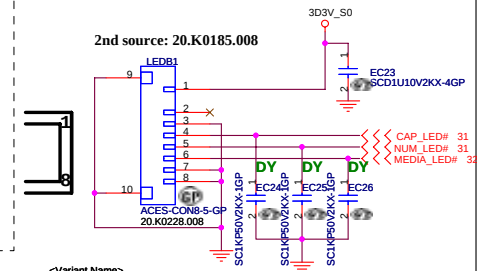
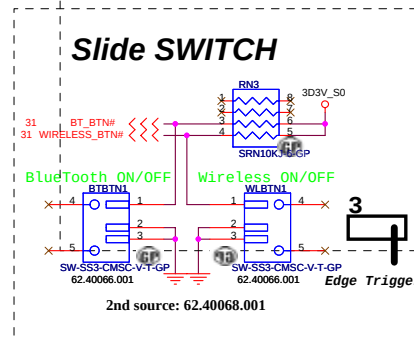
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
NB-RS690M MEM/PCIE LINK I/F			
Size	Document Number	Orta	Rev
A3			SA
Date:	Tuesday, December 12, 2006	Sheet	11 of 46



LCD/INVERTER CONN



LED BD

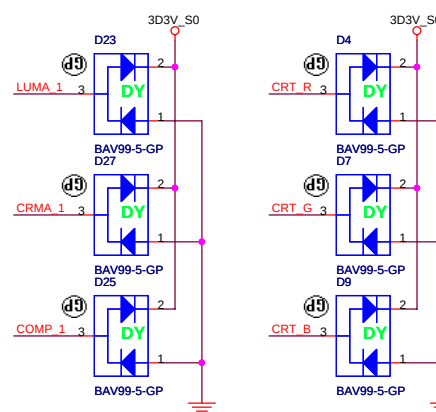
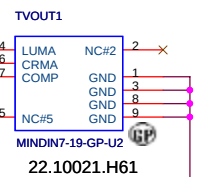
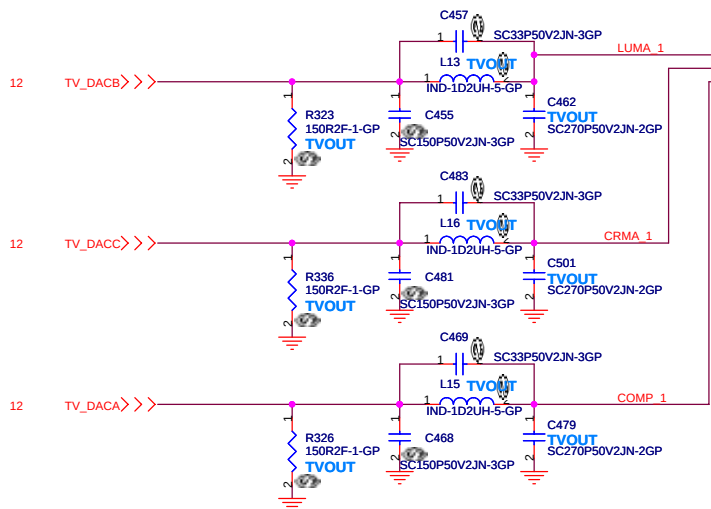
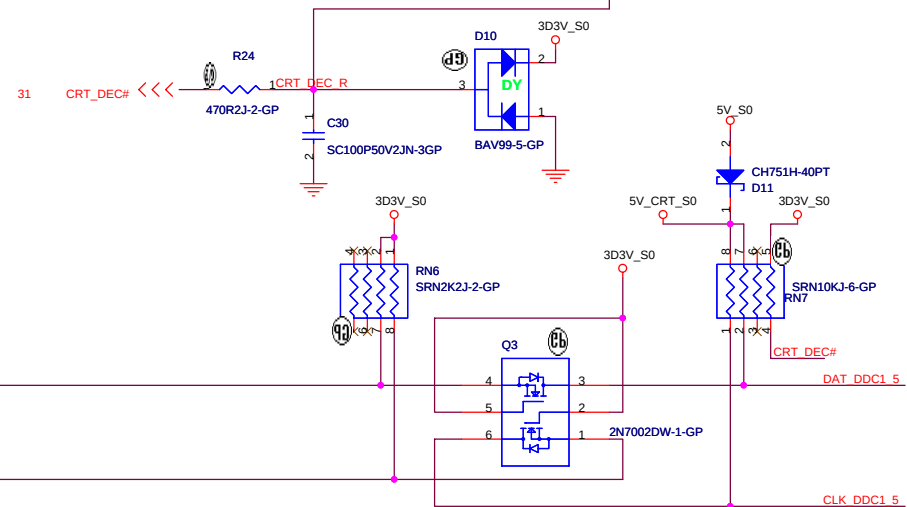
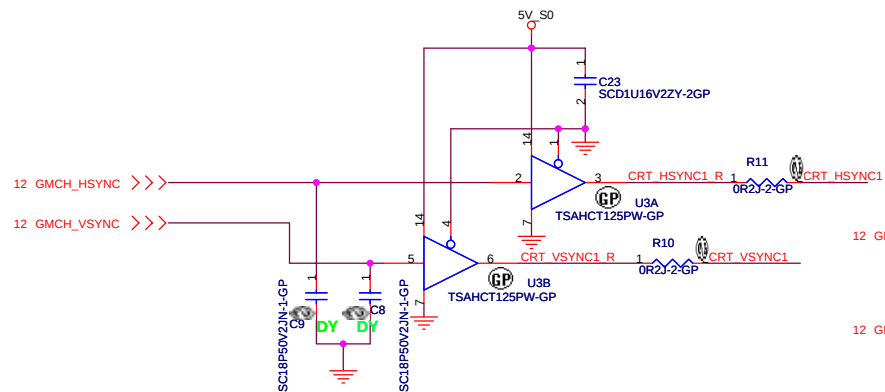
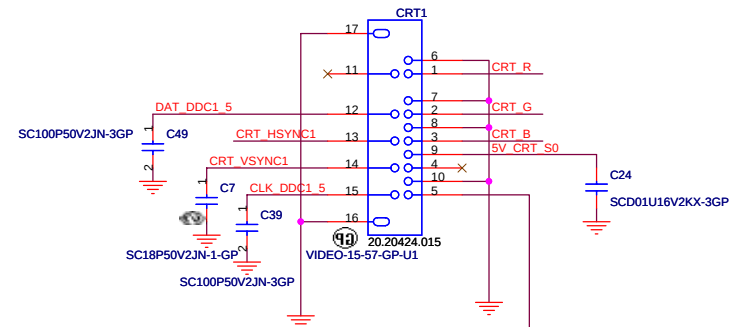
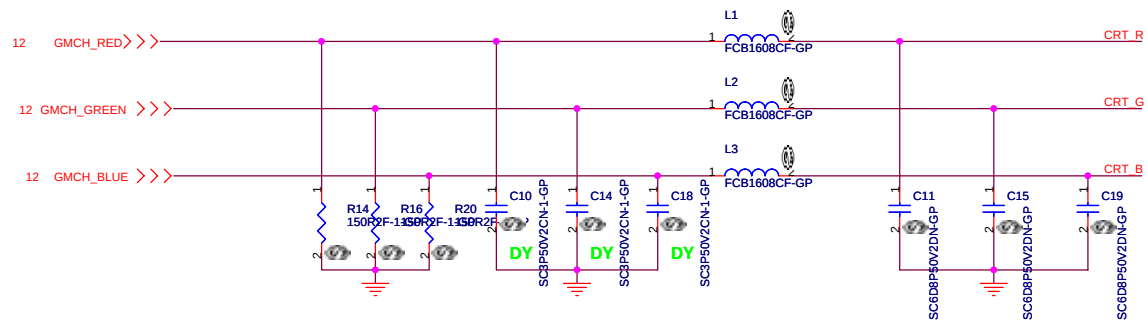


<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

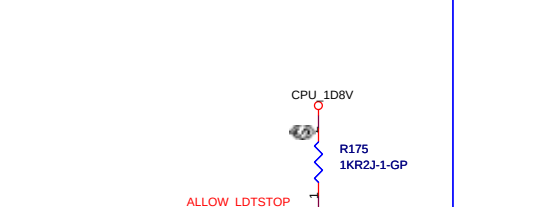
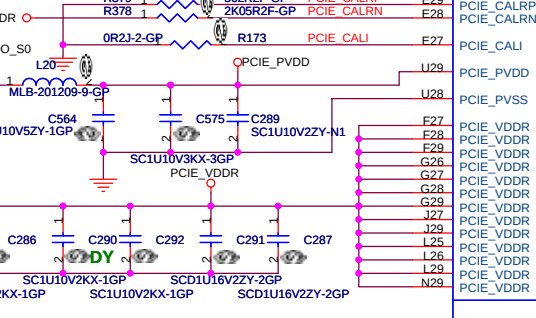
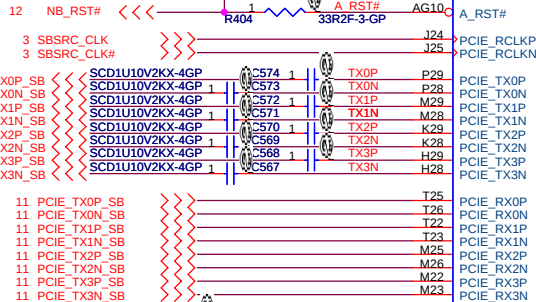
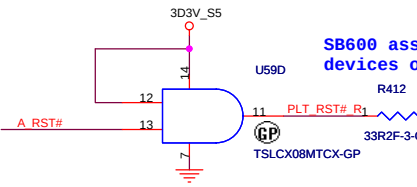
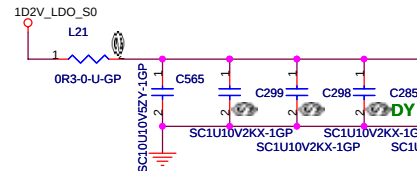
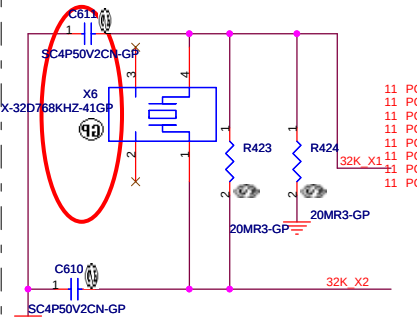
Title		LCD CONN & LED	
Size	Document Number	Orta	Rev SA
Date:	Tuesday, December 12, 2006	Sheet 14	of 46



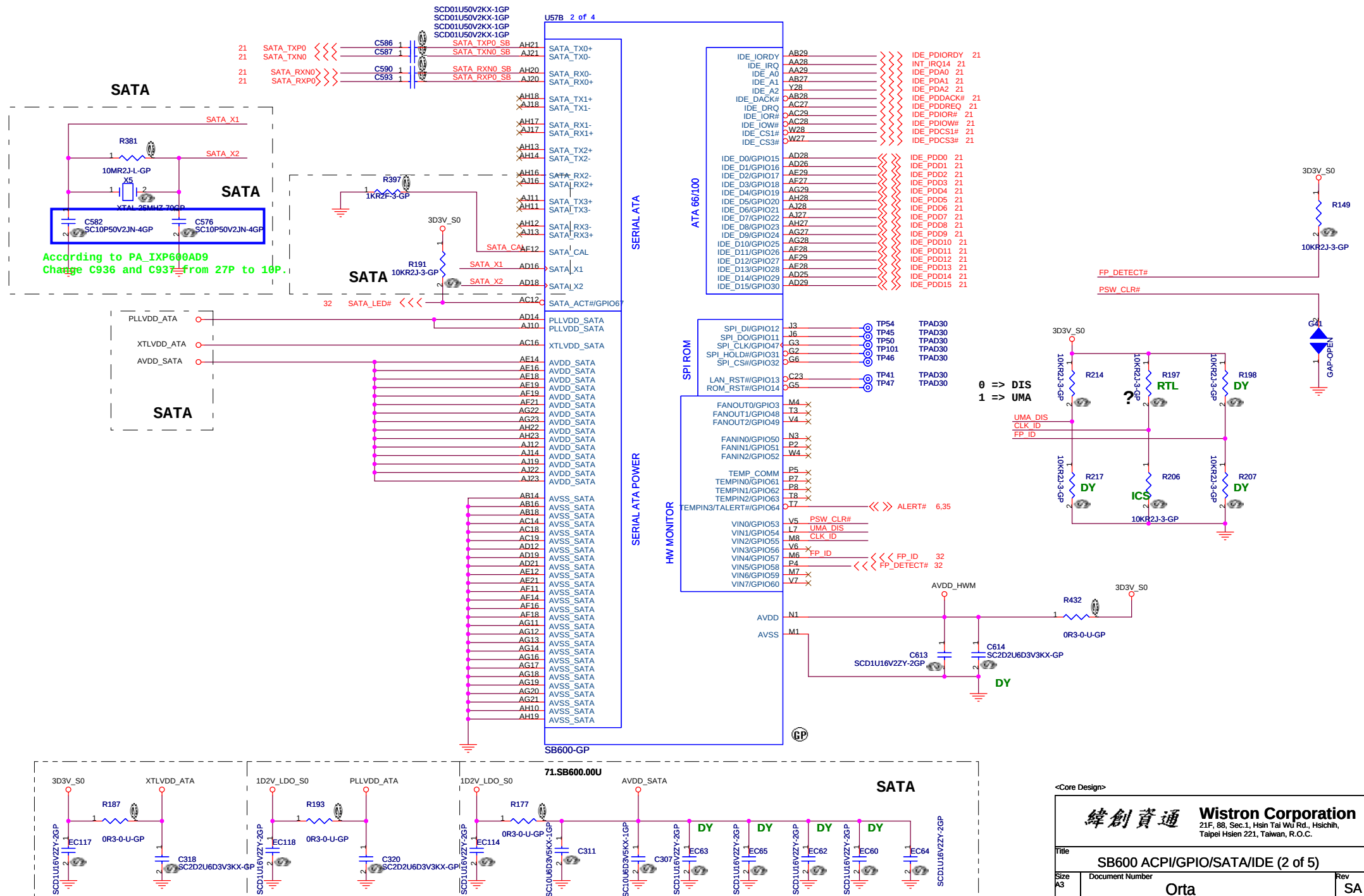
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

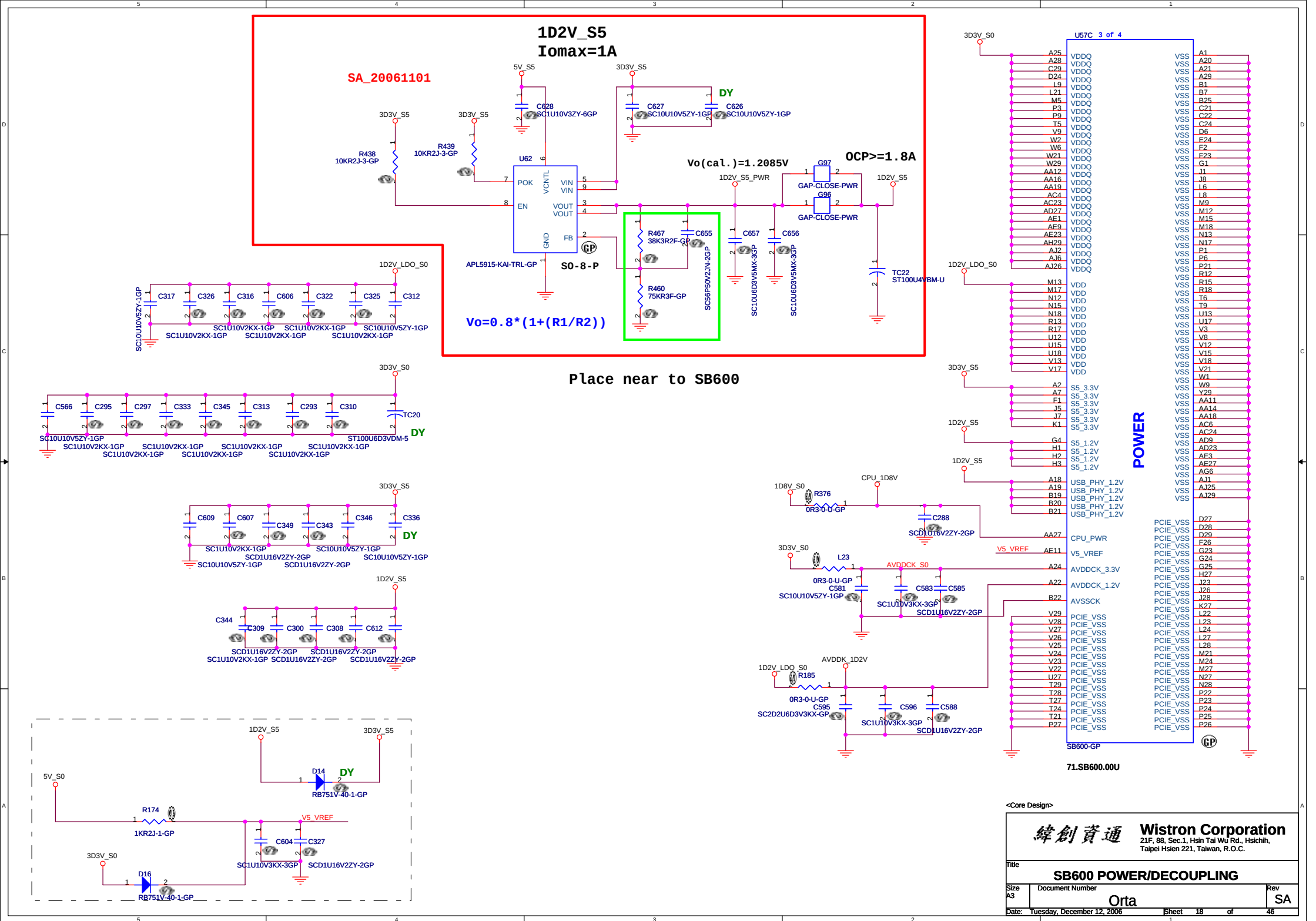
Title		CRT/TV Connector	
Size	Document Number	Rev	SA
Date: Tuesday, December 12, 2006		Sheet 15	of 46

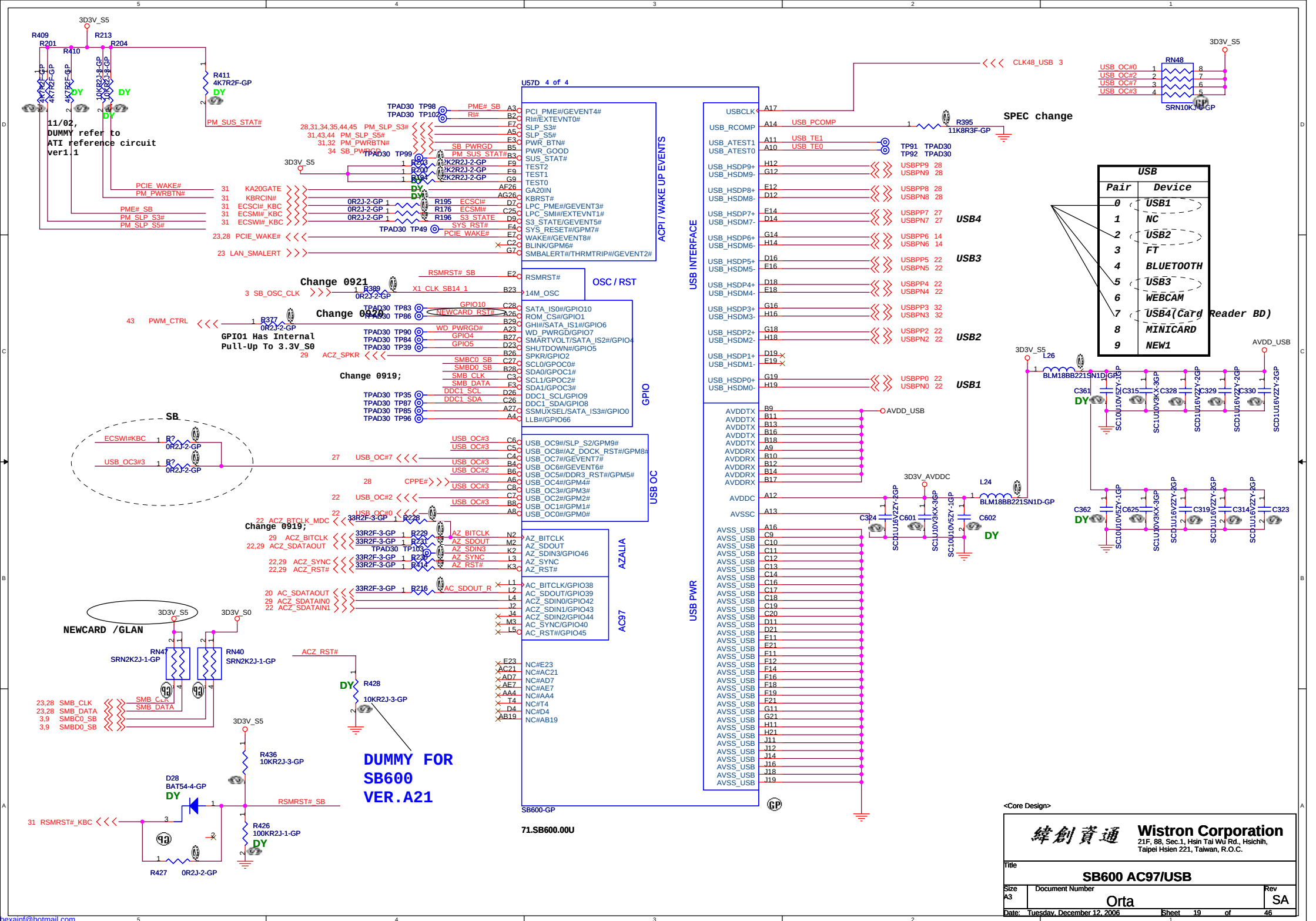
Place these components close to U13 and use ground guard for 32K_X1 and 32K_X2.



PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB460

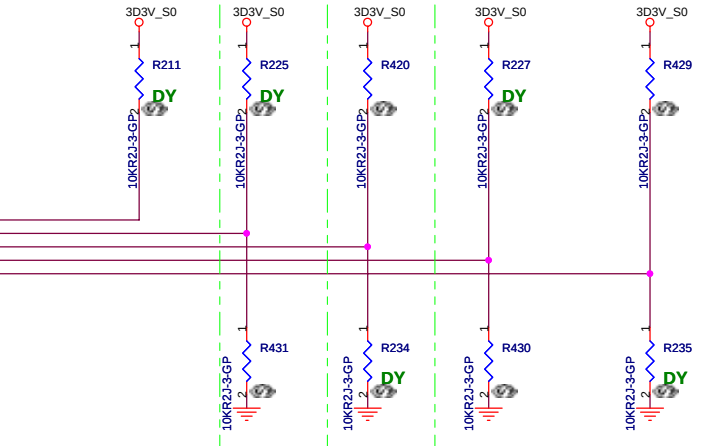






PCI_CLK4
PCI_CLK6
PCI_CLK0
PCI_CLK1

19 AC_SDATAOUT
16,31 PCLK_KBC
15 CLK33_LPCROM
16 PCI_CLK0
16,25 PCLK_PCM

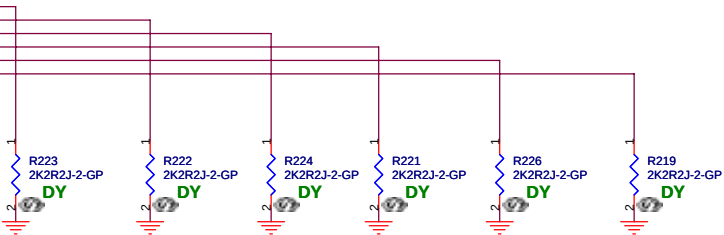


REQUIRED SYSTEM STRAPS

		SB600				
		AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM		
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

16,25 PCI_AD28
16,25 PCI_AD27
16,25 PCI_AD26
16,25 PCI_AD25
16,25 PCI_AD24
16,25 PCI_AD23



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

SB600 STRAPPING PIN

Size A3

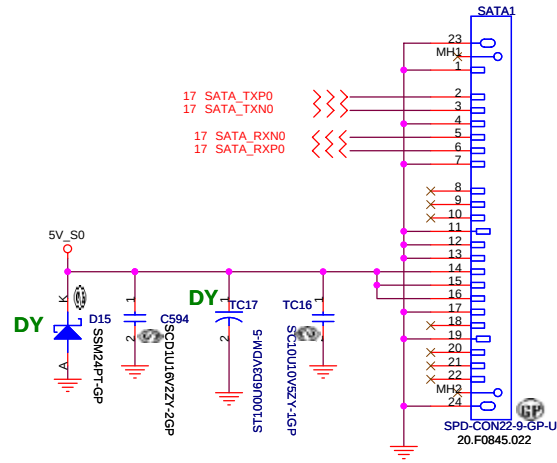
Document Number

Rev SA

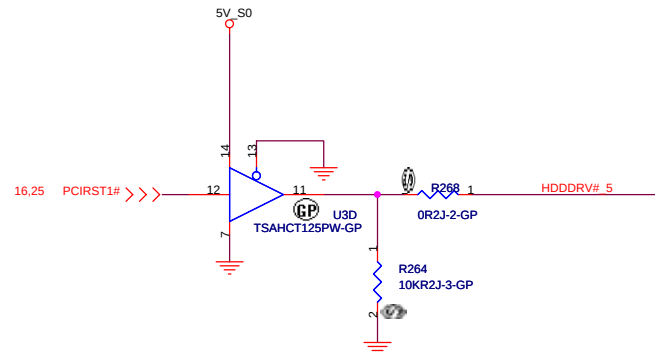
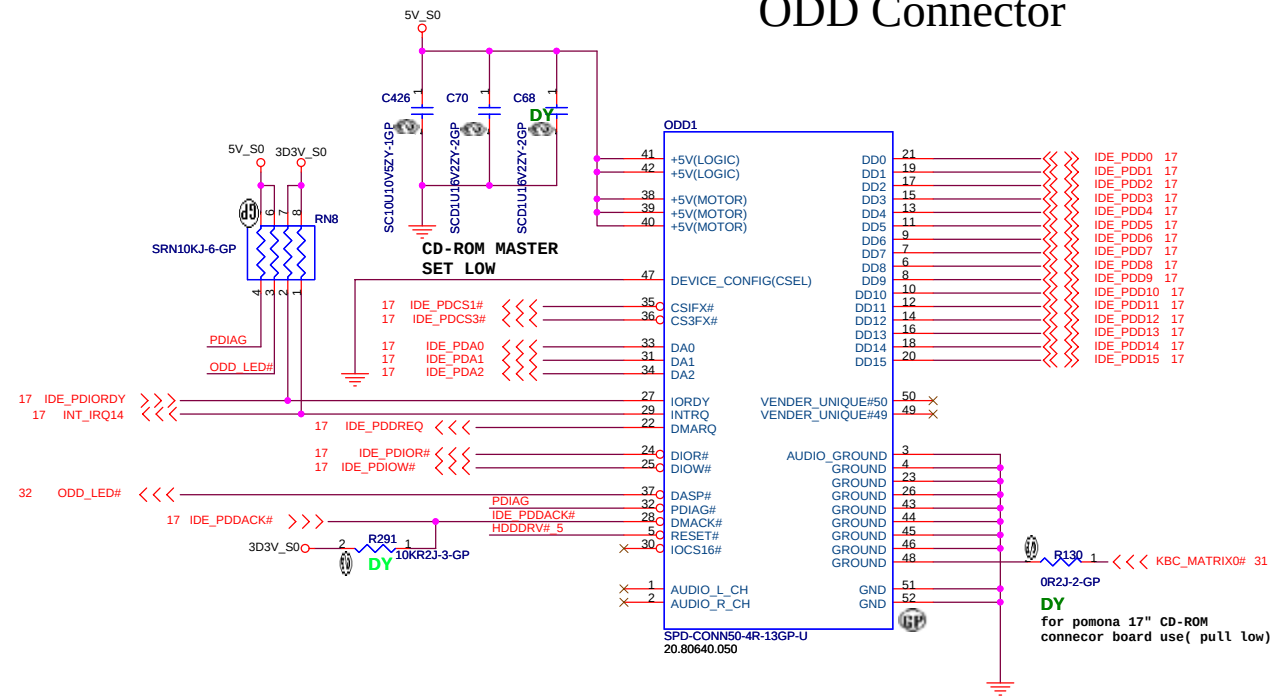
Date: Tuesday, December 12, 2006

Sheet 20 of 46

SATA HD Connector



ODD Connector



bom1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

	Title
--	-------

HDD and CDROM

Size

Document Number

Orta

Rev

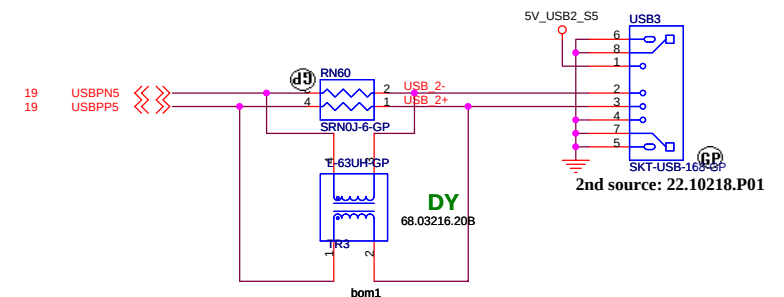
SA

Date: Tuesday, December 12, 2006

Sheet	21
-------	----

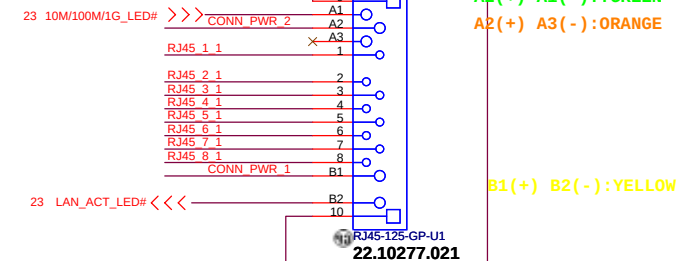
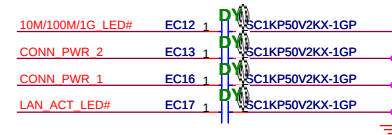
of

46

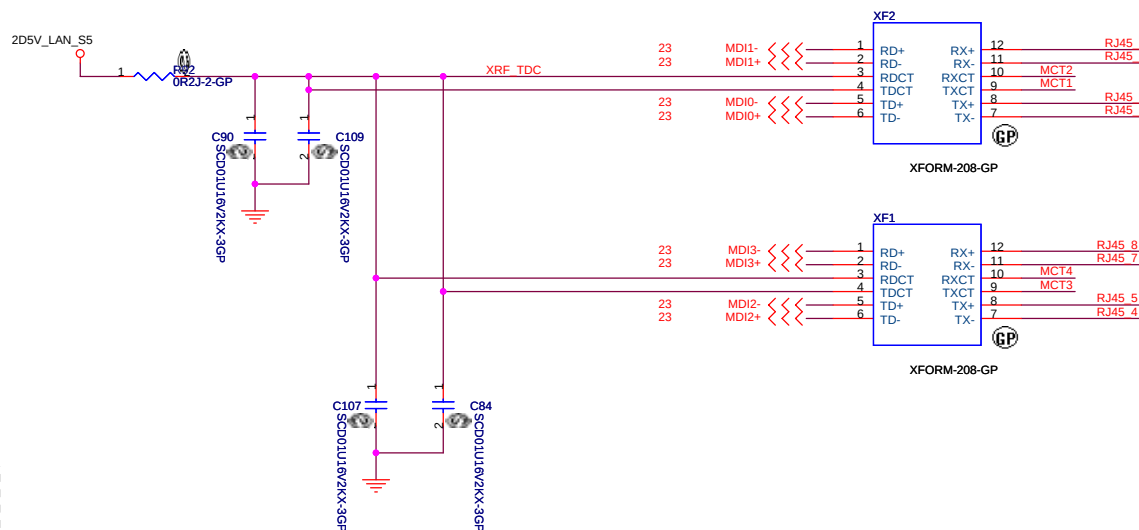


Title			
USB / MDC / BLUETOOTH			
Size	Document Number		Rev
	Orta		SA
Date:	Tuesday, December 12, 2006	Sheet 22 of	46

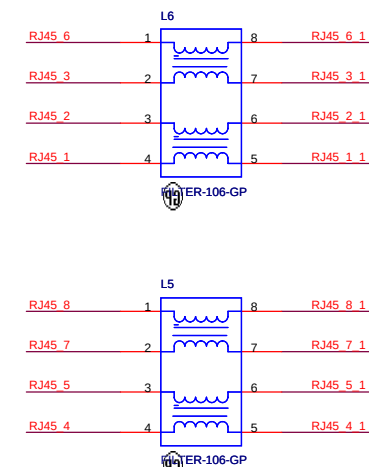
LAN Connector



GIGA Lan Transformer



For EMI request

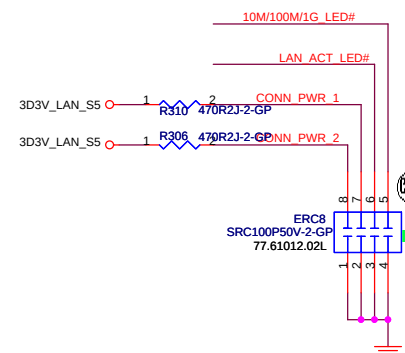
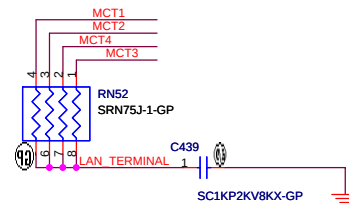


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

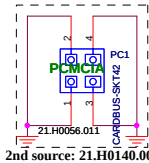
Title	LAN Connector	
Size	Document Number	Rev
A3	Orta	SA
Date: Tuesday, December 12, 2006	Sheet 24 of 46	

PCMCIA Socket

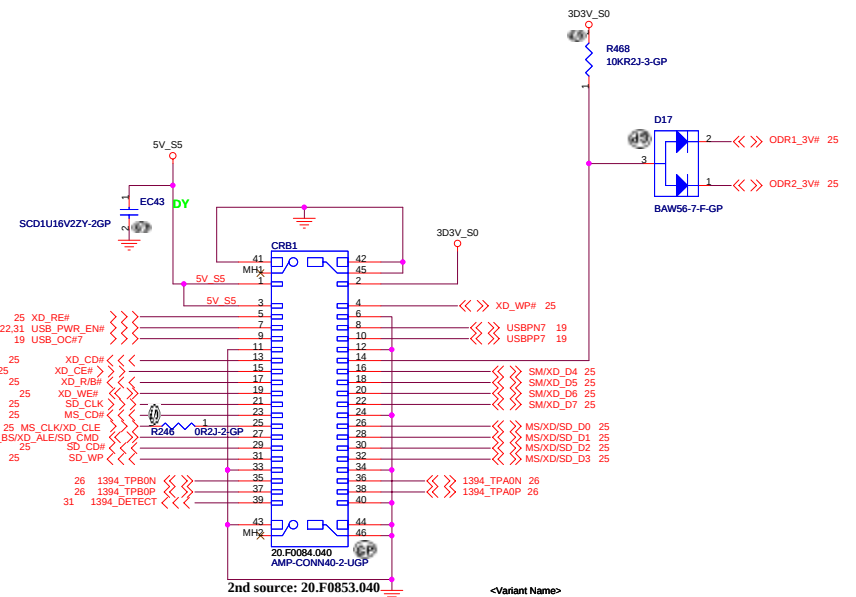
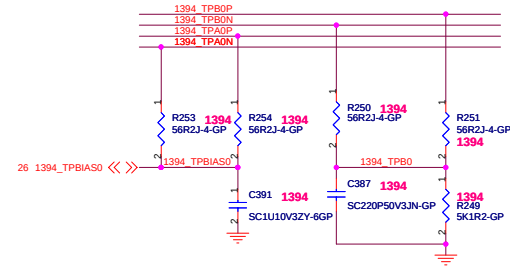
Cardbus I/F

CBB_D[15..0] << CBB_D[15..0] 25
CBB_A[25..0] << CBB_A[25..0] 25

CBB_IORD# 25
CBB_IOWR# 25
CBB_CE# 25
CBB_WE# 25
CBB_REG# 25
CBB_CE1# 25
CBB_CE2# 25
CBB_BVD1# 25
CBB_BVD2# 25
CBB_CD1# 25
CBB_CD2# 25
CBB_VS1# 25
CBB_VS2# 25



CLOSE TO CHIP



XD
MS / MS PRO
SD / SD IO / MMC

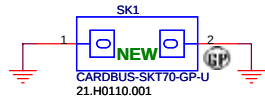
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

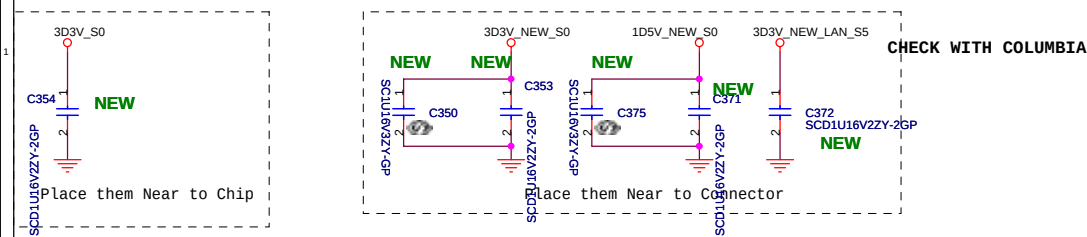
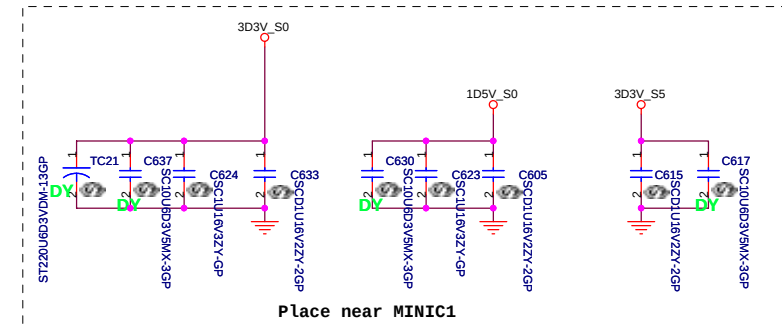
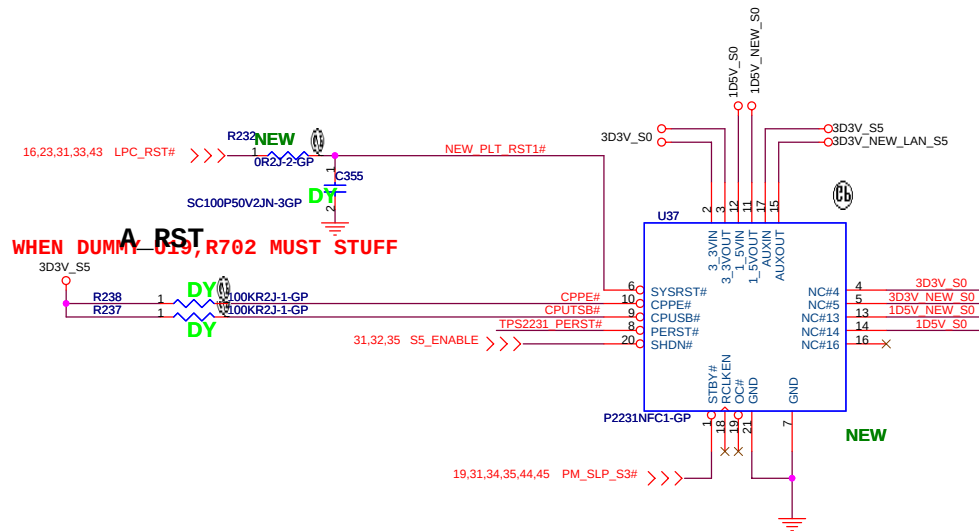
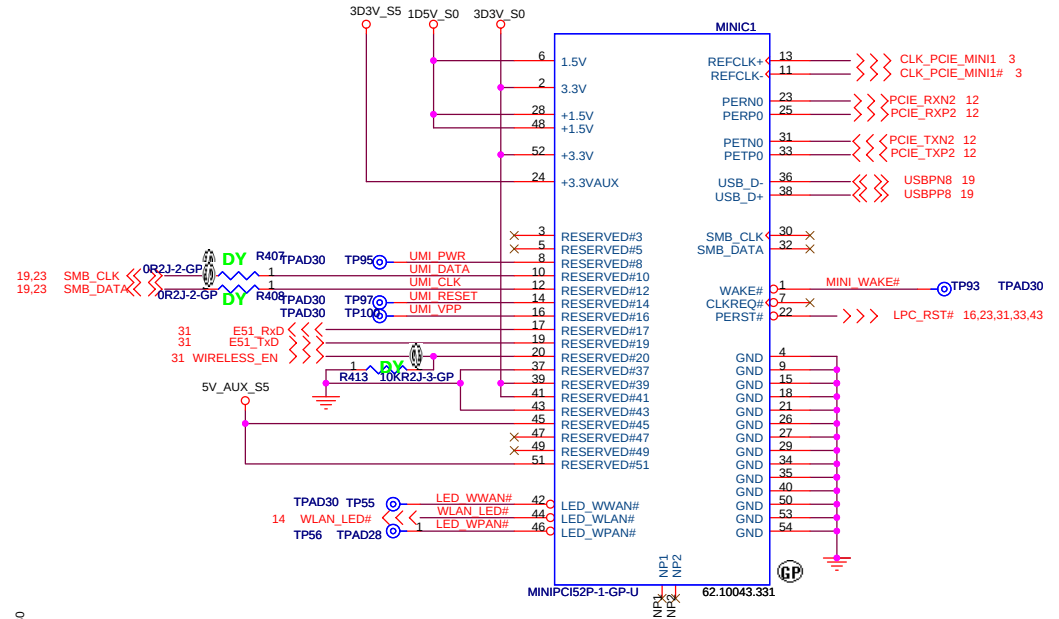
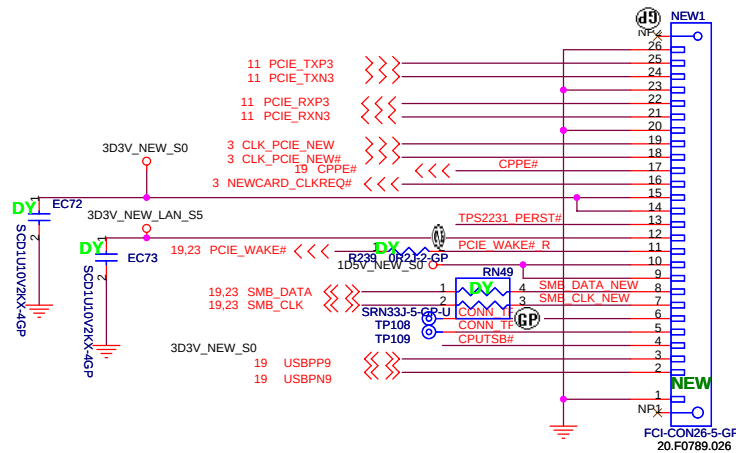
Title		PCMCIA / 1394 / CARD READER	
Size	Document Number	Rev	SA
Date: Tuesday, December 12, 2006		Sheet 27 of 46	

Mini Card Connector

NEWCARD Connector



Reserve the symbol
for bottom side
connector



bom1

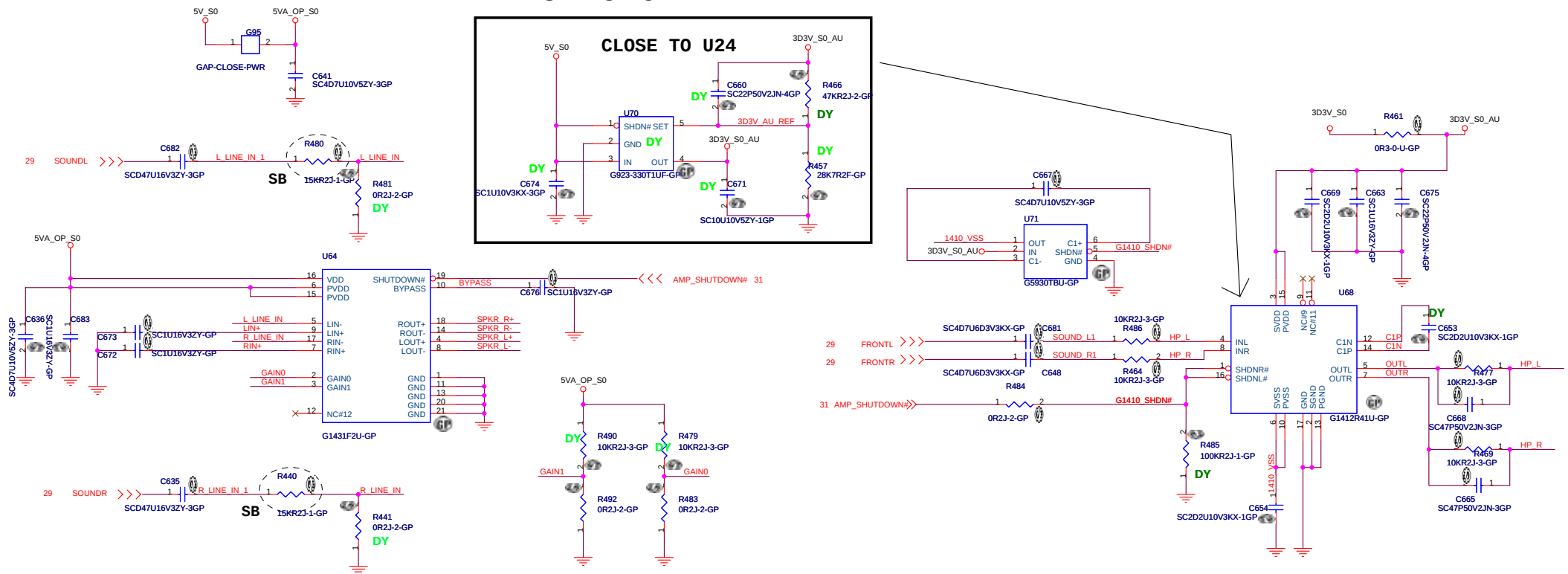
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

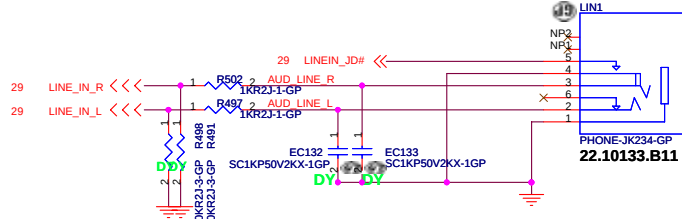
Title			
MINI CARD / NEW CARD			
Size	Document Number		Rev
	Orta		SA
Date:	Tuesday, December 12, 2006	Sheet 28 of 46	

AUDIO OP AMPLIFIER

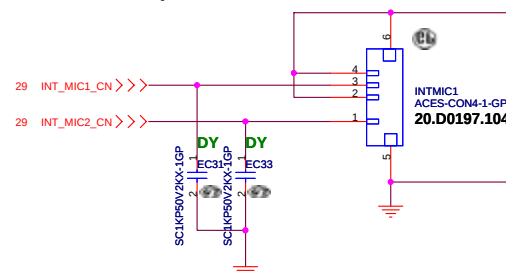
KBC_MUTE_GPIO8



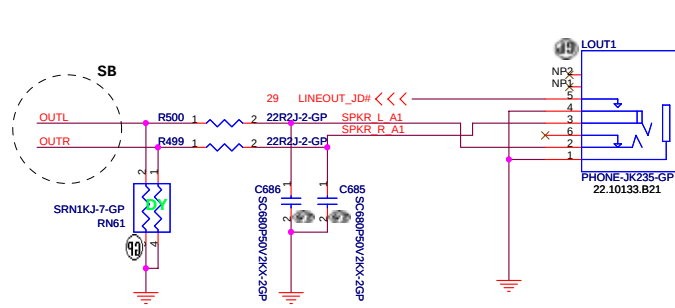
LINE IN



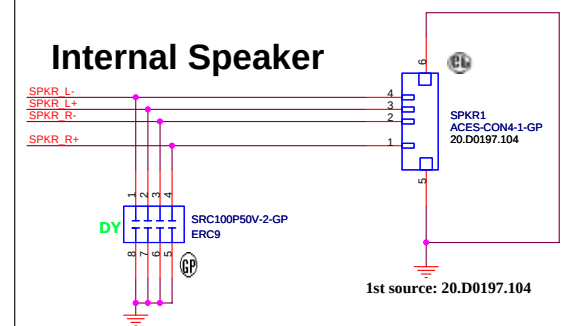
Internal Microphone



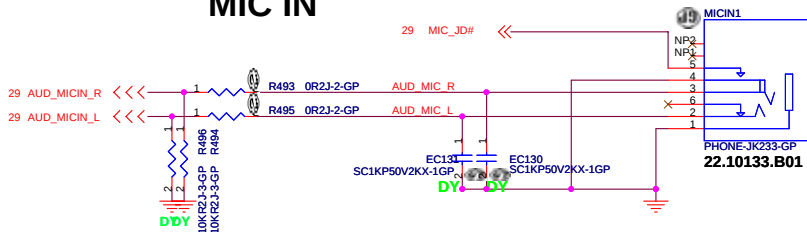
LINE OUT



Internal Speaker



MIC IN



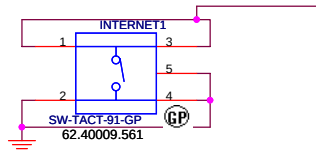
<Variant Name>

緯創資通

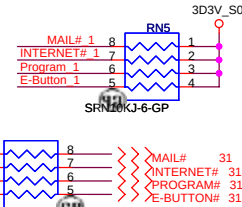
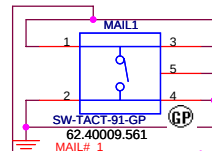
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
AUDIO AMP AND JACK		
Size	Document Number	Rev
	Orta	SA
Date: Tuesday, December 12, 2006	Sheet 30	of 46

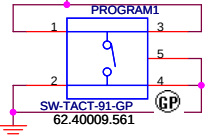
Internet Button



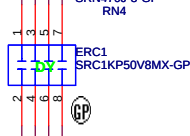
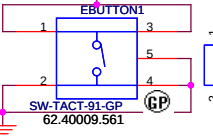
Mail Button



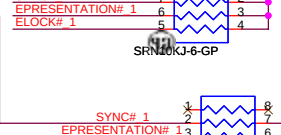
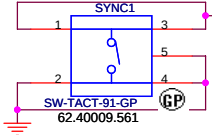
Program Button



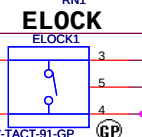
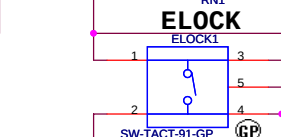
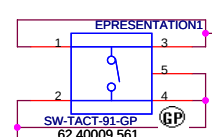
E-Button



SYNC

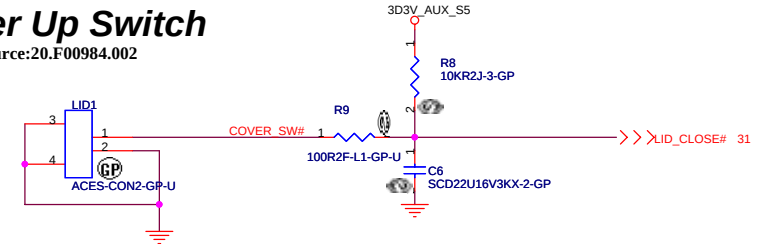


EPRESENTATION

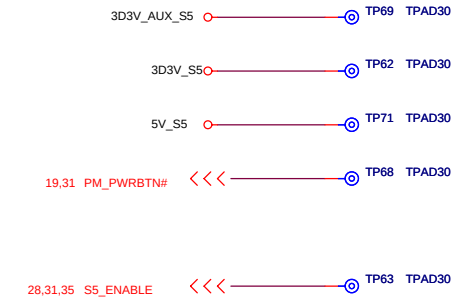


Cover Up Switch

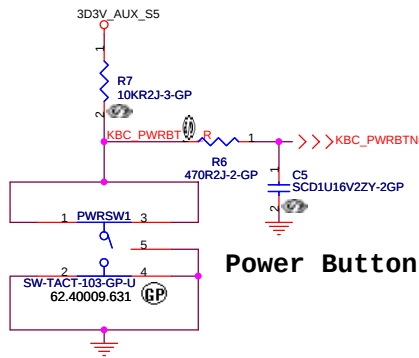
2nd source:20.F00984.002



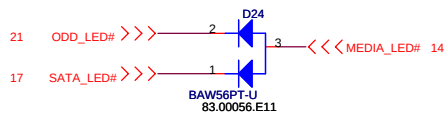
Check test point



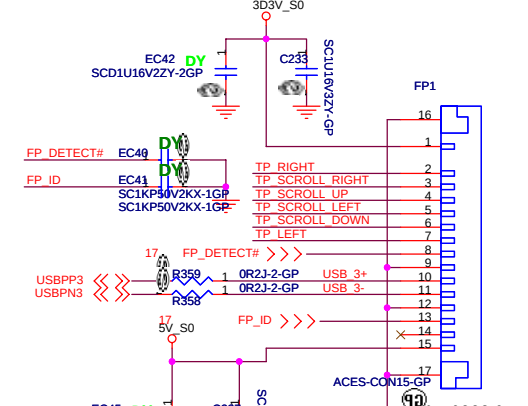
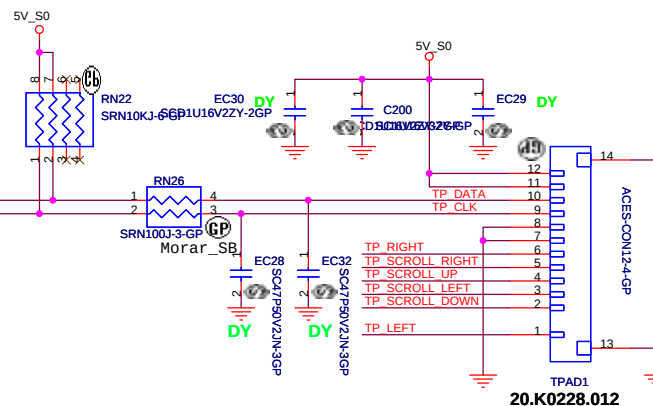
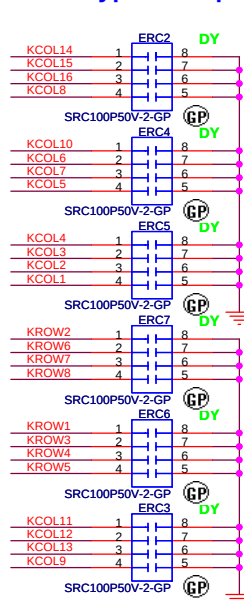
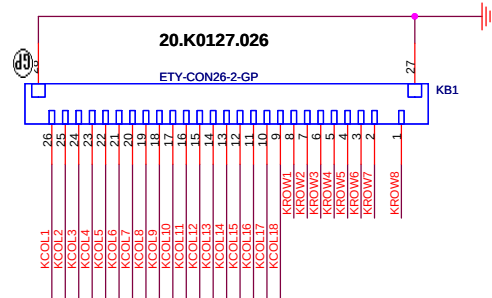
Test Point 放在 Dimm Door 打開可量測處



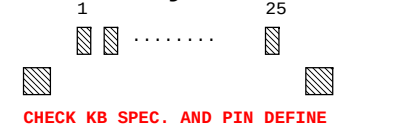
Power Button



EMI Bypass cap.



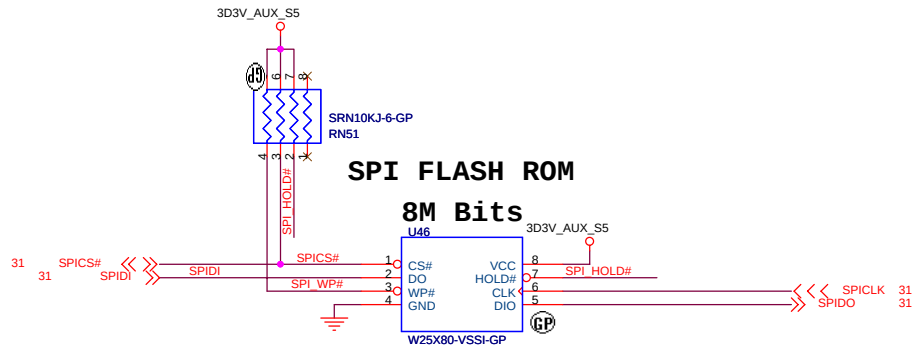
Internal KeyBoard CONN



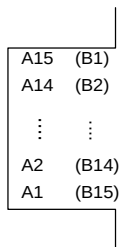
CHECK KB SPEC. AND PIN DEFINE

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BUTTONS / KB / TOUCHPAD		
Size	Document Number	Rev
	Orta	SA
Date: Tuesday, December 12, 2006	Sheet 32	of 46

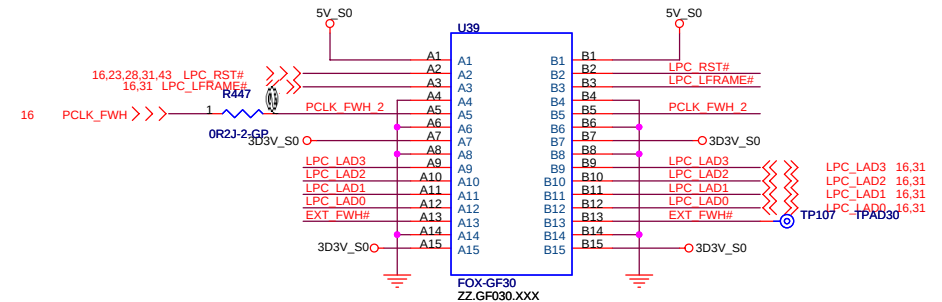


TOP VIEW

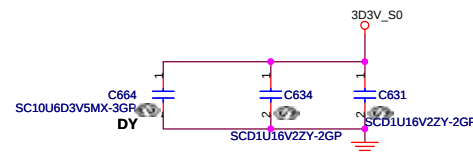


(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD

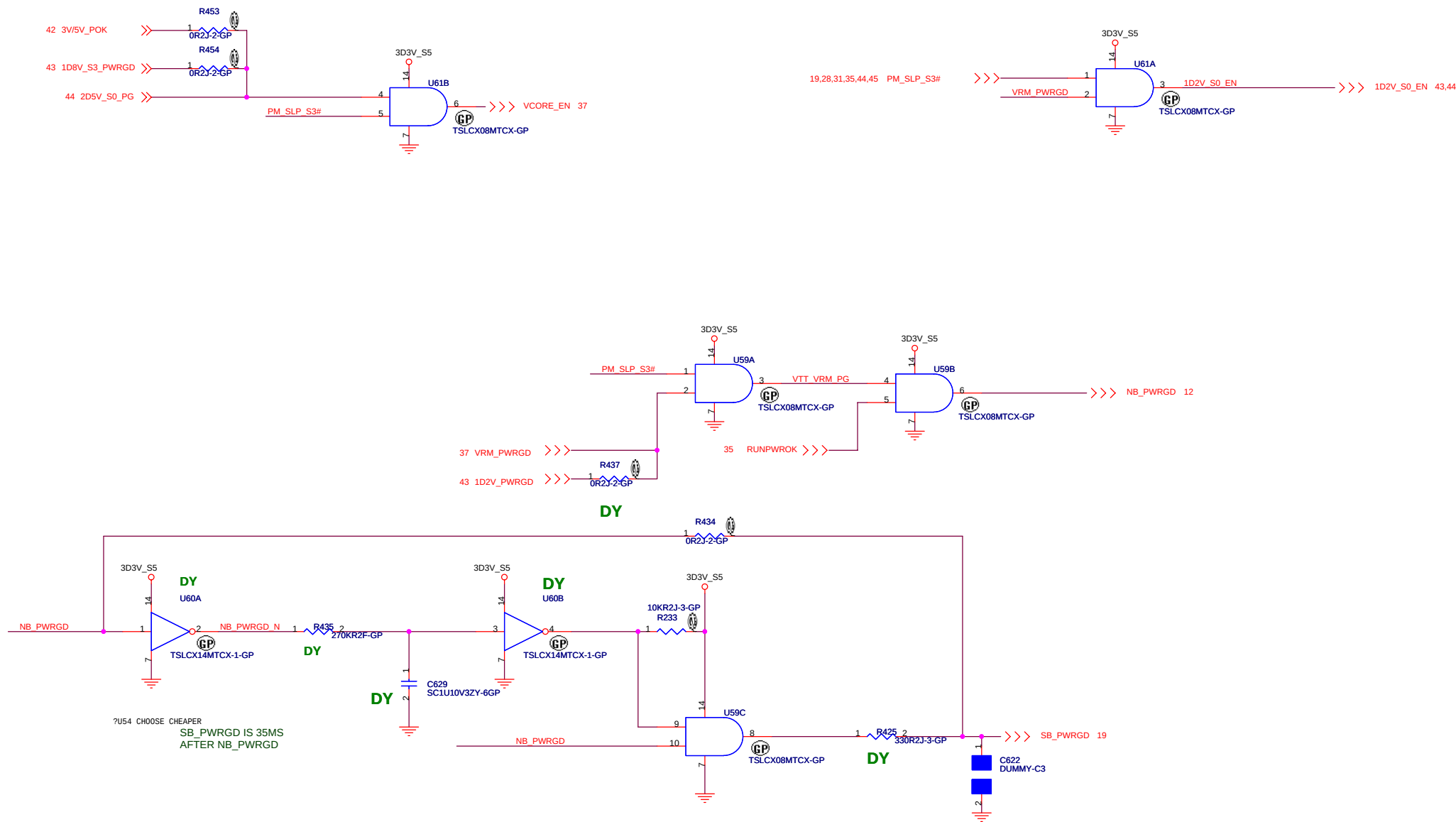


Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



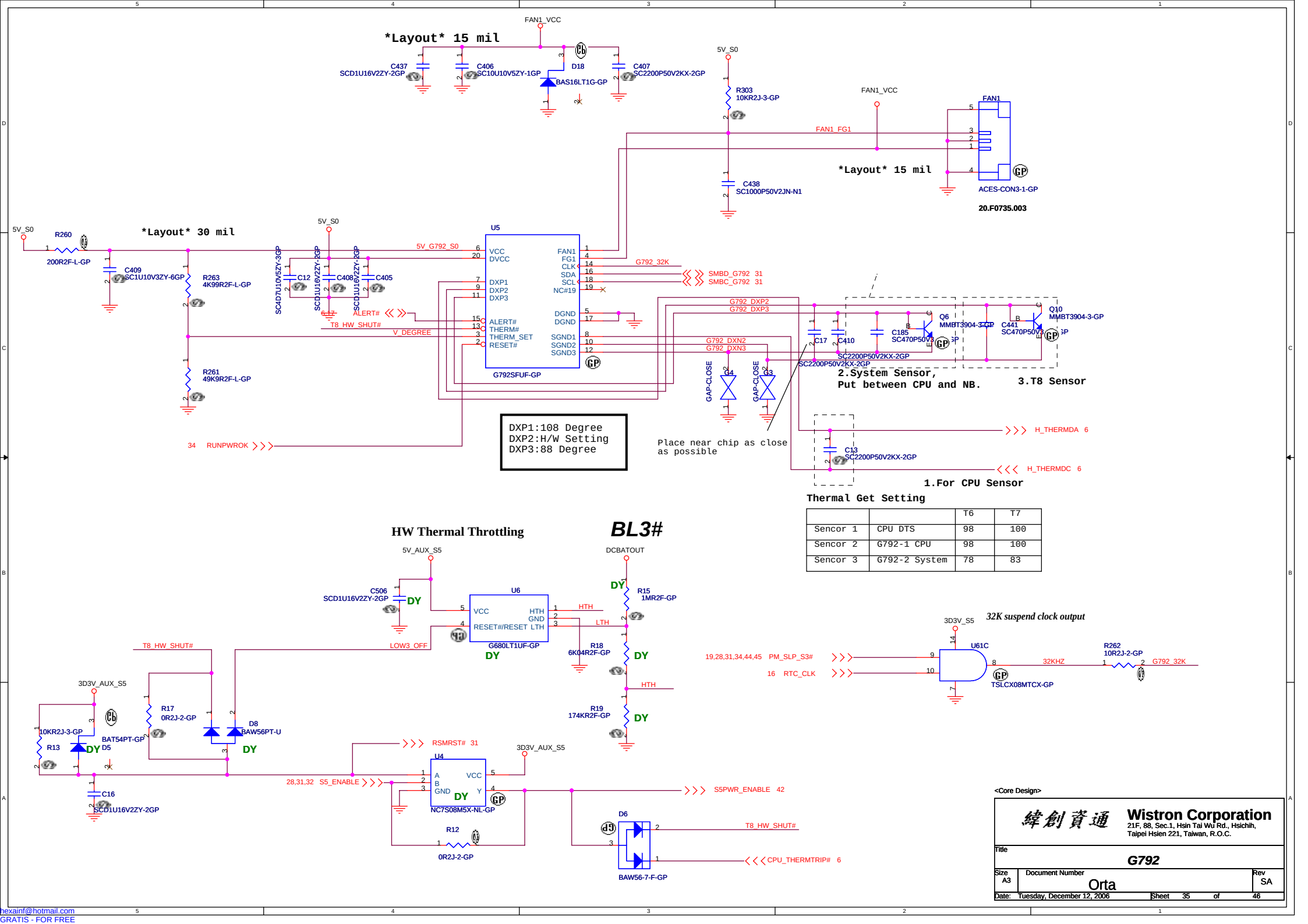
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
BIOS		
Size A3	Document Number Orta	Rev SA
Date: Tuesday, December 12, 2006	Sheet 33 of 46	

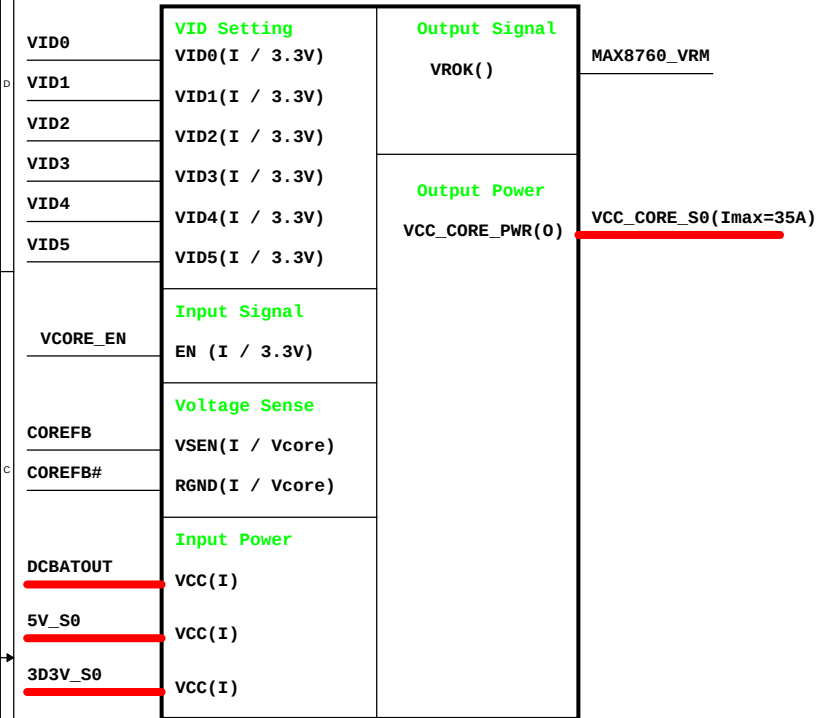


<Core Design>

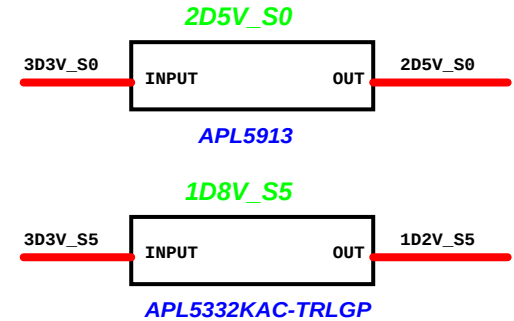
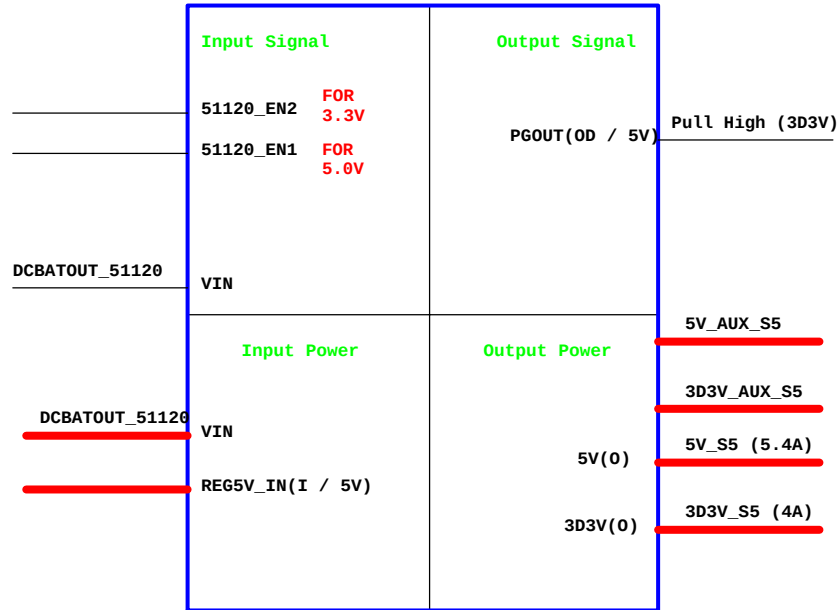
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
POWERGOOD&ENABLES(1/2)			
Size A3	Document Number Orta		Rev SA
Date: Tuesday, December 12, 2006		Sheet 34 of 46	



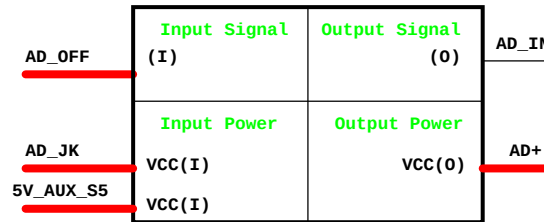
CPU_CORE
ISL6264CRZ



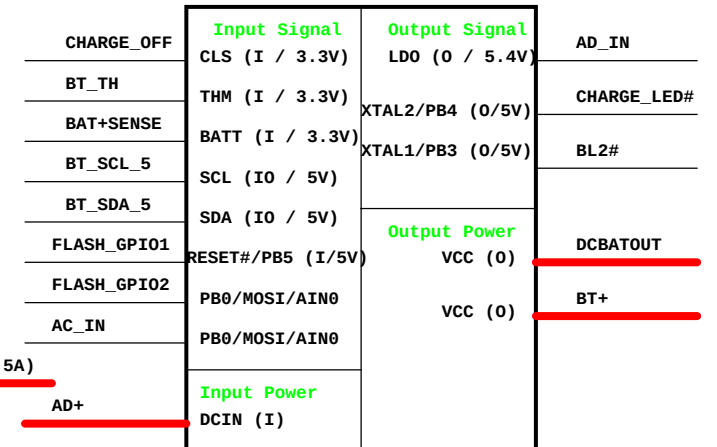
TI TPS51120
3D3V/5V



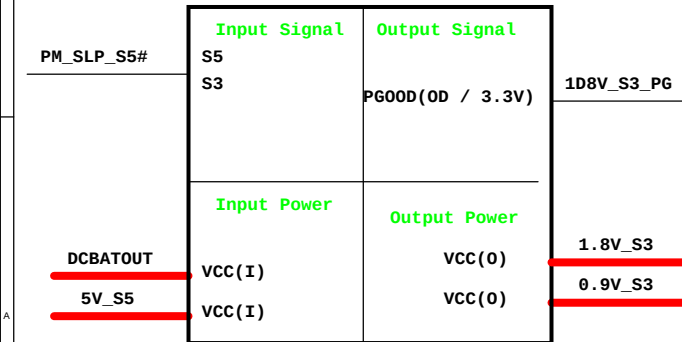
Adapter



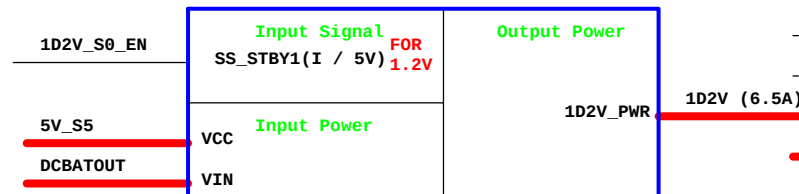
Charger_ISL6255



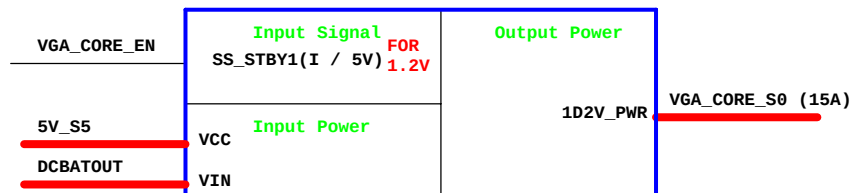
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V



ISL6268_VGA_CORE

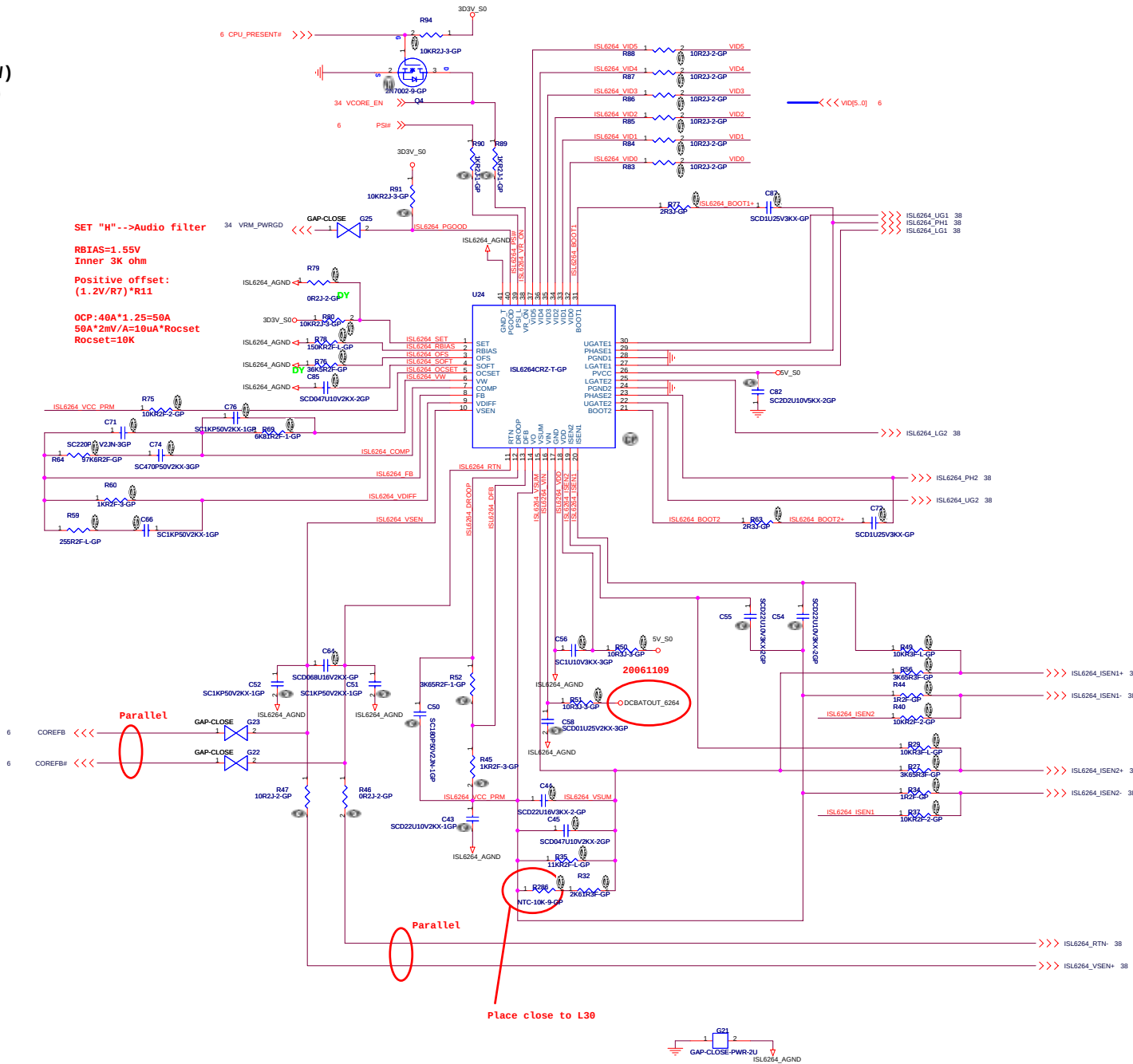


<Core Design>

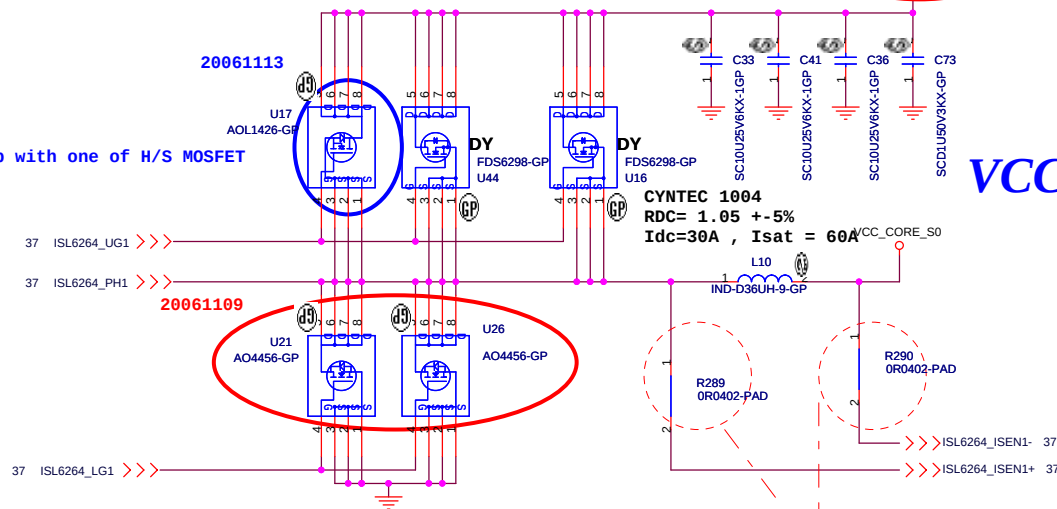
CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7525
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375

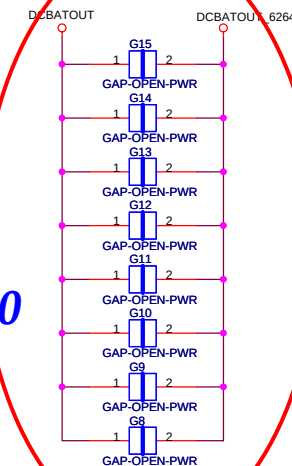


Overlap with one of H/S MOSFET



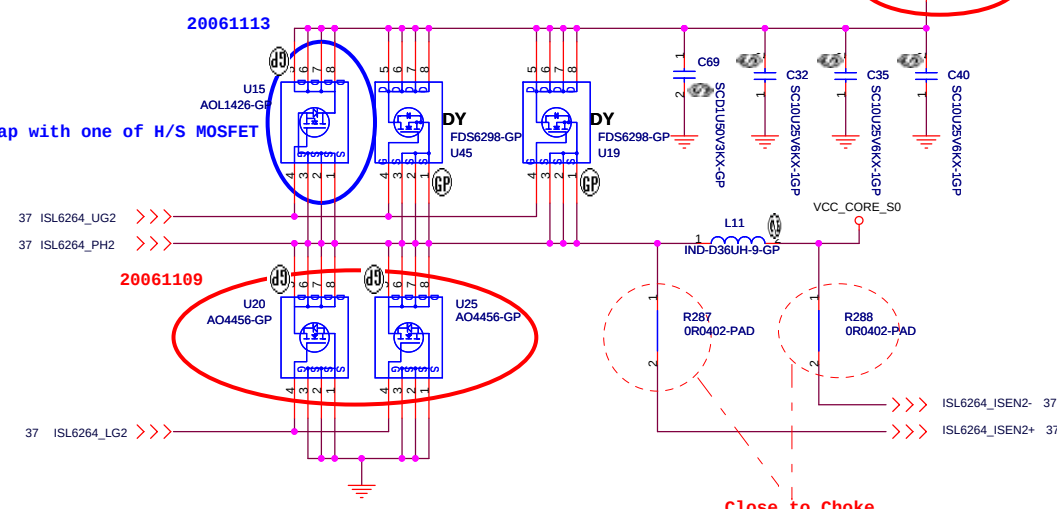
VCC_CORE_S0

20061109

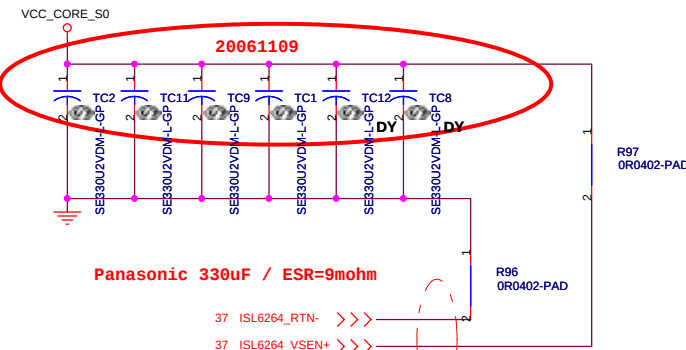


Close to Choke

20061109



Close to Choke



Panasonic 330uF / ESR=9mohm

Parallel

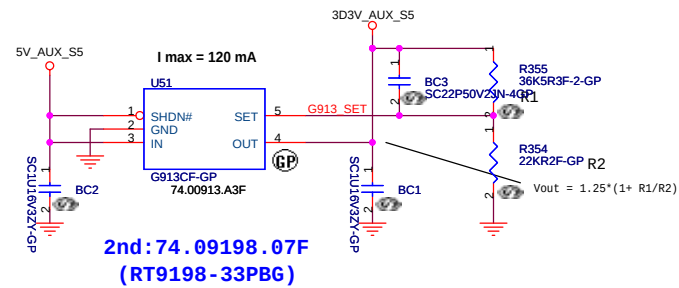
<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU Vcore Power_2			
Size	Document Number		Rev
A3	Orta		SA
Date:	Tuesday, December 12, 2006	Sheet 38 of 46	

Aux Power
3D3V_AUX_S5



<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
3D3V AUX			
Size	Document Number		Rev
A3	Orta		SA
Date:	Tuesday, December 12, 2006	Sheet 39 of 46	

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

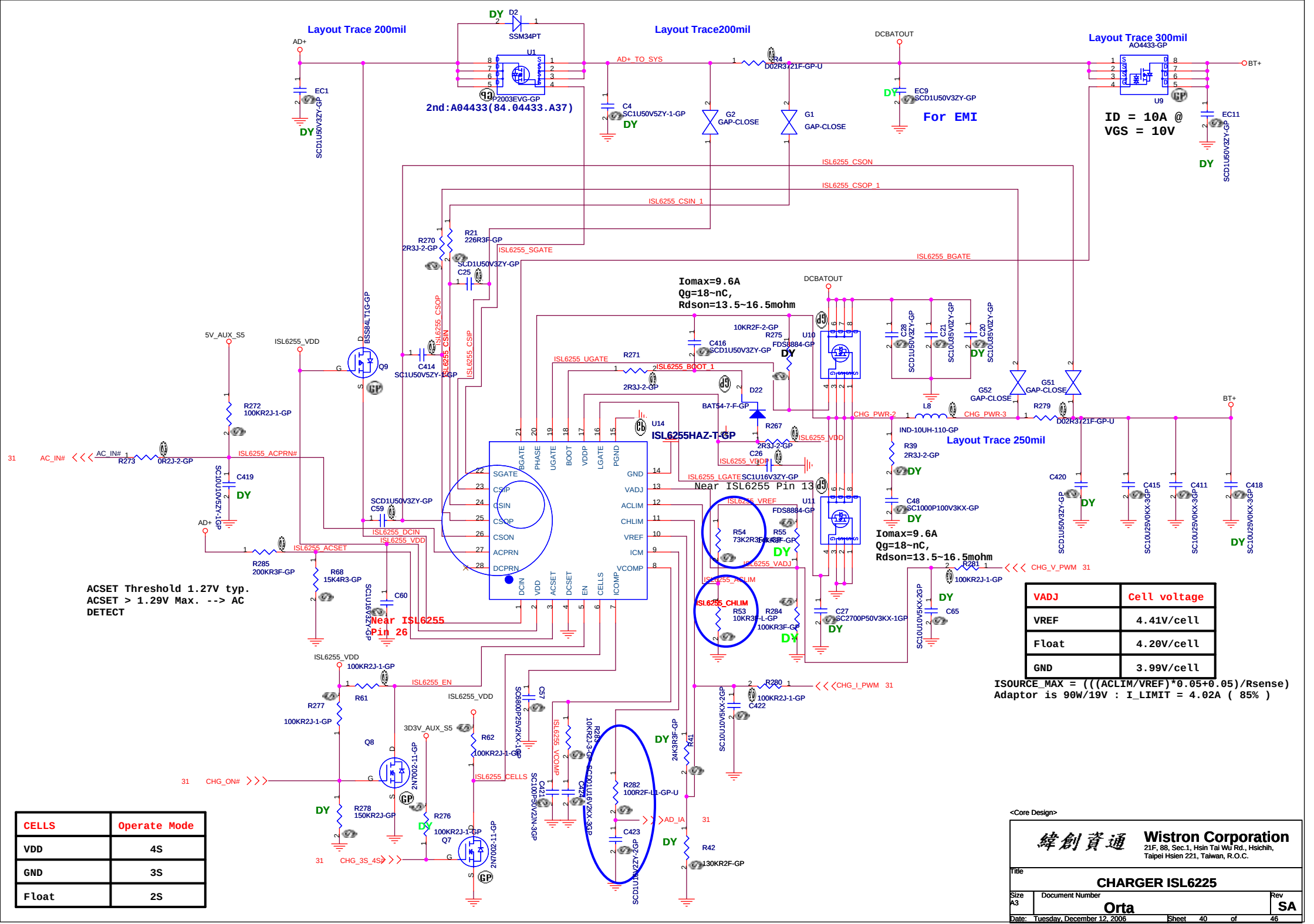
ACSET Threshold 1.27V typ.
ACSET > 1.29V Max. --> AC
DETECT

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 90W/19V : I_LIMIT = 4.02A (85%)

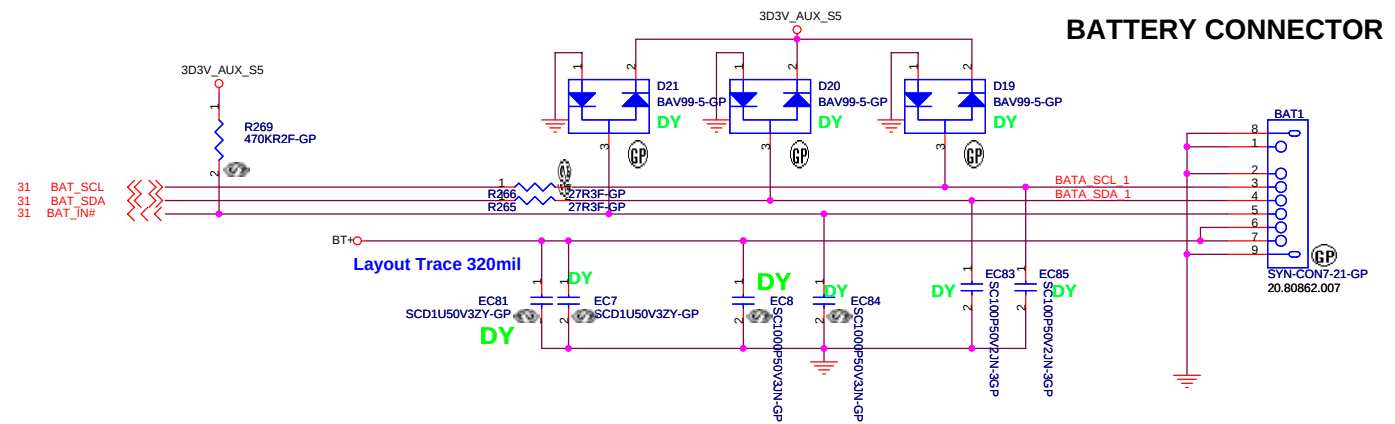
VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

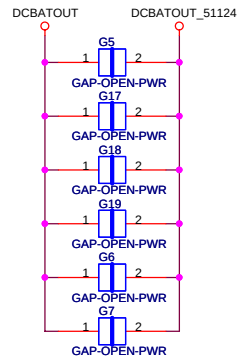
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
CHARGER ISL6225		
Size	Document Number	Rev
A3	Orta	SA
Date: Tuesday, December 12, 2006	Sheet 40 of 46	



<Variant Name>			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AD/BATT CONN			
Size A3	Document Number	Orta	Rev SA
Date: Tuesday, December 12, 2006	Sheet	41	of 46





Id=9.6A
Qg=18-nC,
Rdson=13.5~16.5mohm

Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm

Tai-Tech
DCR=3.5m ohm
Irms=20A, Isat=28A

1D8V Iomax=8A
OCP>16A

Voutsetting=1.8046V

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=15mohm

Kemet
220uF/ 4V
ESR=15mohm

$$V_{out} = 0.758V * (R1 + R2) / R2$$

19,31.44 PM_SLP_S5#
34,44 1D2V_S0_EN

20061113

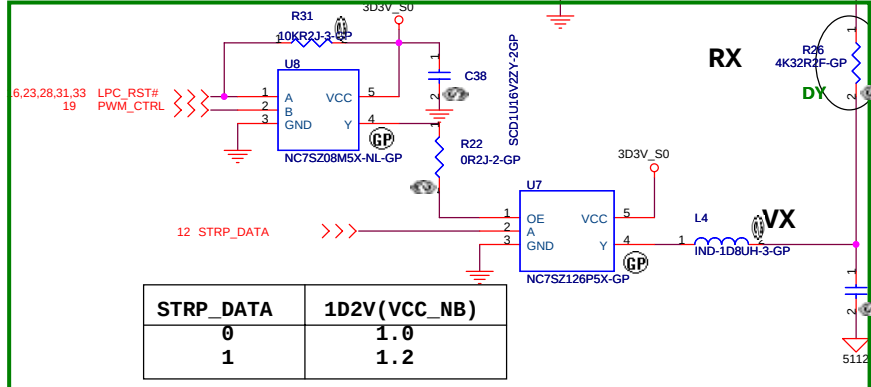
OCP

20061109

$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip} / R_{dson}) + ((1 / (2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in}))$$

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2



STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

1D2V Iomax=8A
OCP>16A

Voutsetting=1.2047V

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=15mohm

Kemet
220uF/ 4V
ESR=15mohm

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

TPS51124 1D8V 1D2V

Orta

SA

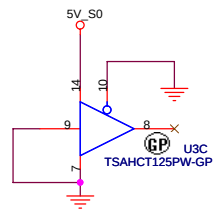
Title

Size A3

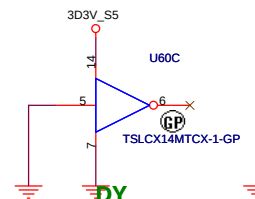
Date: Tuesday, December 12, 2006

Document Number

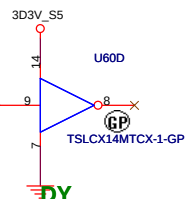
Sheet 43 of 46



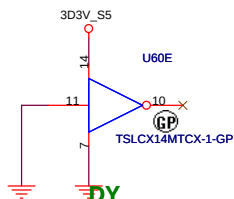
DUMMY in SA



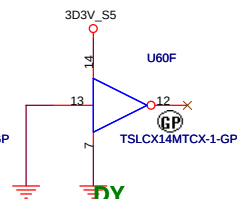
34.42Y01.001



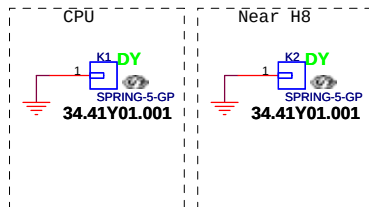
34.42Y01.001



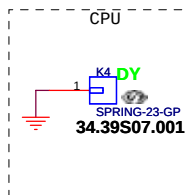
34.4G502.001



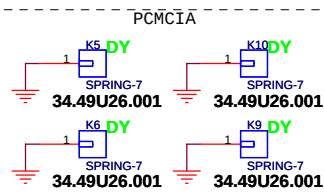
DY



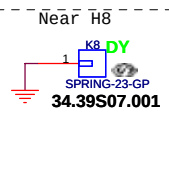
34.42Y01.001
34.42Y01.001



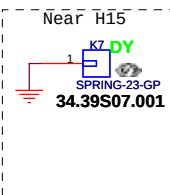
34.39S07.001



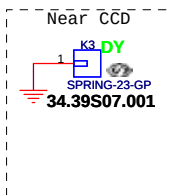
34.49U26.001
34.49U26.001



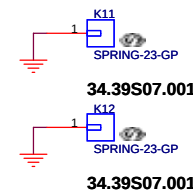
34.39S07.001



34.39S07.001



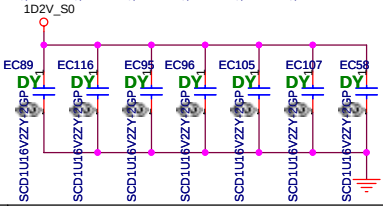
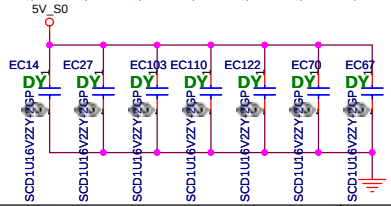
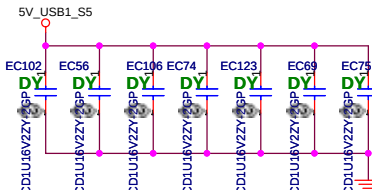
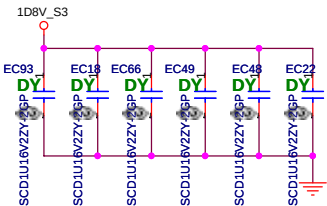
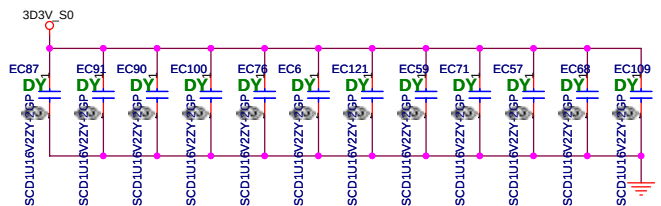
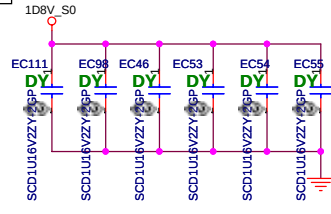
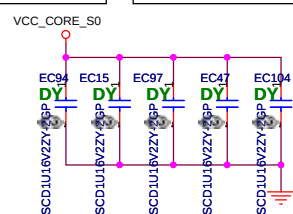
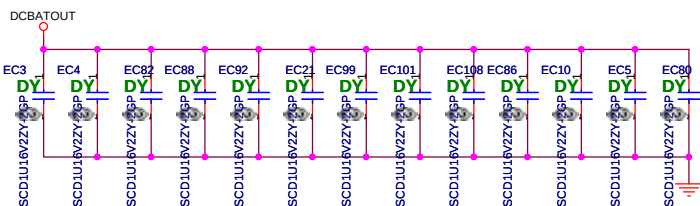
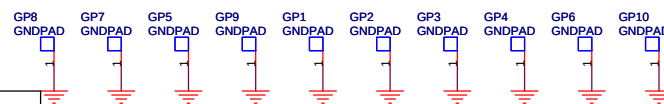
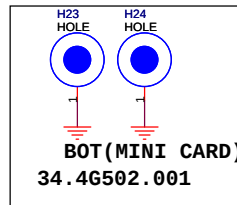
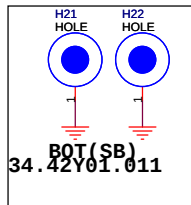
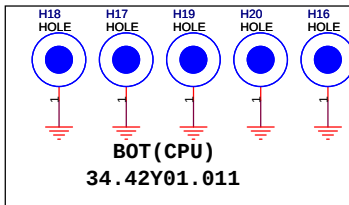
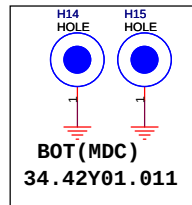
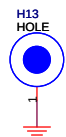
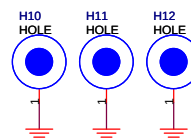
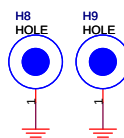
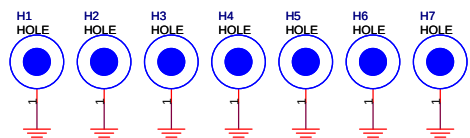
34.39S07.001



34.39S07.001

34.39S07.001

TOP(CARD READER BD)
34.42Y01.011



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		EMI/Spring/Boss	
Size	Document Number	Rev	SA
Date: Tuesday, December 12, 2006		Sheet 46	of 46