HSF Property: ROHS

ACER_BAP31U

MAIN BOARD

2009.05.13

Wednesday, May 20, 2009		A01
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

INVENTEC

TITLE ACER_BAP31U

SIZE	CODE	DOC.NUMBER	REV
C	AX1	D-CS-1310A2264501-ALG	A01

SHEET 1 of 35

1. Schematic Page Description :

Montevina Schematic Ver : A02

1. Title
2. Schematic Page DESCR
3. Block Diagram
4. Annotations
5. Schematic Modify
6. Timing Diagram
7. Power Block Diagram
8. Adaptor in/Charge
9. 5VLA/5VA/3VA
10. 3VS/5VS/1.5V (DDR3)
11. 1.05VS/1.5S/1.8V/1.5VA
12. Power Latch/1.5VS/SCREW HOLE
13. CPU Core Power
14. GPU Core Power
15. Penryn Processor(1/2)
16. Penryn Processor(2/2)
17. CPU Thermal
18. Cantiga Host(1/6)
19. Cantiga DMI/Graph(2/6)
20. Cantiga DDRII(3/6)
21. Cantiga Power(4/6)
22. Cantiga Power(5/6)
23. Cantiga Ground(6/6)
24. Clock Generator
25. DDR3 SDRAM SO-DIMM0
26. DDR3 SDRAM SO-DIMM1
27. ICH9M CPU/IDE/SATA(1/4)
28. ICH9M PCI/PCIE/DMI/USB(2/4)
29. ICH9M GPIO(3/4)
30. ICH9M Power/GND(4/4)
31. LCD CNN/SATA/3G/WLAN
32. KBC ITE8512F
33. IO CN
34. IO CN
35. AUDIO CODEC

INVENTEC

TITLE: BAP31U

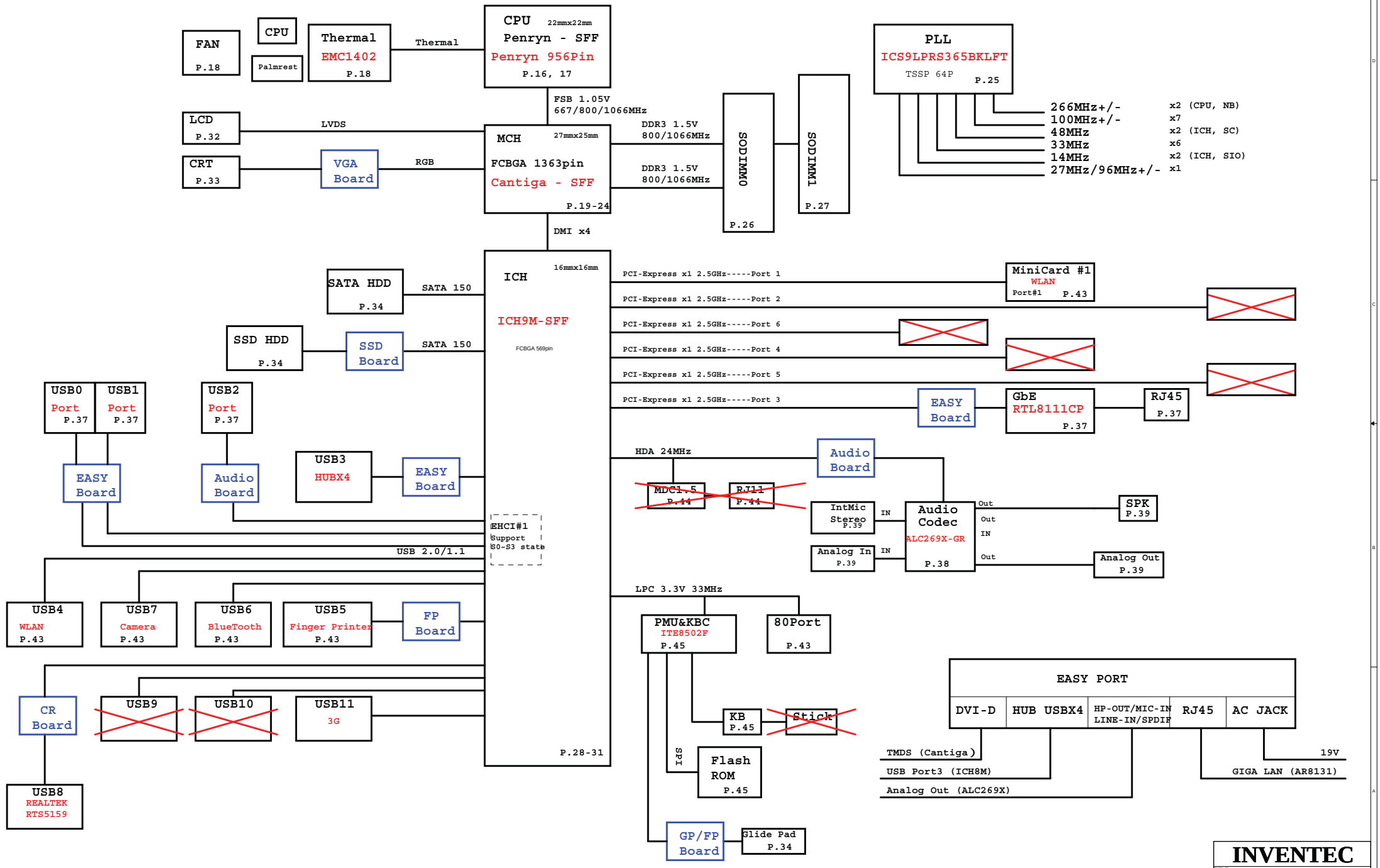
Schematic Page

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 2 of 35

CHANGE by Harry Chen DATE Wednesday, May 20, 2009

3. Block Diagram :



INVENTEC

TITLE: BAP31U

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 3 of 35

CHANGE by Harry Chen DATE Wednesday, May 20, 2009

4. Net name Description

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM:	1.3319V~1.4375V~1.4591V	18A
	LFM:	0.9221V~0.9625V~0.9739V	
1.05VS	Penryn SFF : AGTL+ termination	1V~1.05V~1.10V	4.5A
	Cantiga GS: Core	0.997V~1.05V~1.102V	8.7A
	Cantiga GS: PCIE	0.9975V~1.05V~1.1025V	1.78A
	Cantiga GS:Core+IMEL+HSIO	0.9975V~1.05V~1.1025V	2.898A
	Cantiga GS:VCC_GMCH	0.997V~1.05V~1.102V	10.154A
	Cantiga GS:VCCA_SM_CK and NCTF	0.997V~1.05V~1.102V	37.95mA
	Cantiga GS:VCC_DMI	0.997V~1.05V~1.102V	456mA
	Cantiga GS:VCCA_SM	0.997V~1.05V~1.102V	747.5mA
	Cantiga GS:VTT	0.997V~1.05V~1.102V	852mA
	ICH9M:VCC1_05	0.997V~1.05V~1.102V	1.634A
	ICH9M:DMI	0.997V~1.05V~1.102V	48mA
	ICH9M:CPU_IO	0.997V~1.05V~1.102V	2mA
1.5VS	Penryn SFF PLL	1.425V~1.5V~1.575V	130mA
	Cantiga GS: QDAC	1.425V~1.5V~1.575V	0.5mA
	Cantiga GS: LVDS	1.71V~1.8V~1.89V	60.31mA
	Cantiga GS: TVDAC	1.425V~1.5V~1.575V	35mA
	Cantiga GS: Various PLLS analog supply	1.425V~1.5V~1.575V	485mA
	Cantiga GS: VCC_SM_CK	1.425V~1.5V~1.575V	149.5mA
	Cantiga GS: VCC_SM	1.425V~1.5V~1.575V	3.1625A
	ICH9M:PCIE_ICH	1.425V~1.5V~1.575V	646mA
	ICH9M:SATA_ICH	1.425V~1.5V~1.575V	1.342A
	ICH9M:VCC_GLAN	1.425V~1.5V~1.575V	80mA
	Mini Card:		
	Express Card:	1.425V~1.5V~1.575V	650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GS: HV CMOS	3.135V~3.3V~3.465V	105.3mA
	Cantiga GS: VCCS_TVDAC	3.135V~3.3V~3.465V	78mA
	ICH9M:VCC3_3	3.135V~3.3V~3.465V	308mA
	ICH9M:VCCGLAN3_3	3.135V~3.3V~3.465V	1mA
	Thermal Sensor:	3.0V~3.3V~3.6V	5mA
	Mini Card: UMTS		
	Express Card:	3.135V~3.3V~3.465V	1.3A
	CLK Generator: ICS9LPRS365BKLFT	3.135V~3.3V~3.465V	500mA
	Mini Card: WirelessLan		
	Bluetooth:	3.0V~3.3V~3.6V	
	Super I/O: IT8305E		
	Azalia Codec: ALC262		
	Azalia MDC:		
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC	2V~3.3V~3.465V	6uA
	ICH9M:VCCSUS3_3	3.135V~3.3V~3.465V	212mA
	ICH9M:VCCCL3_3	3.135V~3.3V~3.465V	73mA
	ICH9M:VCCLAN3_3	3.135V~3.3V~3.465V	78mA
	LCD:	3.0V~3.3V~3.6V	2A
	Lan:AR8131	3.0V~3.3V~3.6V	1A
	Azalia MDC:		
	Flash ROM: BIOS	3.0V~3.3V~3.6V	
5VS	Cardreader: RTS5159	3.0V~3.3V~3.6V	
	Azalia Codec: ALC269	3.0V~3.3V~3.6V	
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA
	~~ODD: SATA~~	~~4.75V~5.0V~5.25V~~	~~Max: 1.5A ; R/W: 900mA ; STDBY: 45mA~~
	~~Audio AMP: G1432~~		
	Inverter:		
	WebCam	4.75V~5.0V~5.25V	1A
5VA	USB: x 2 ports	5VA	2A
	USB	5VA	1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE BAP31U

ANNOTATIONS

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 4 of 35

6.Schematic modify Item and History:

CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE **BAP31U**

Schematic Modify

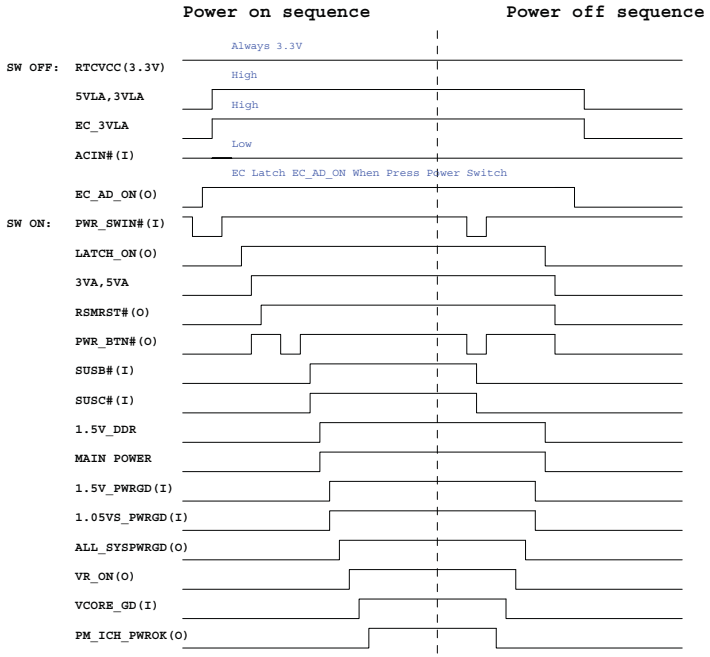
SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 5 of 35

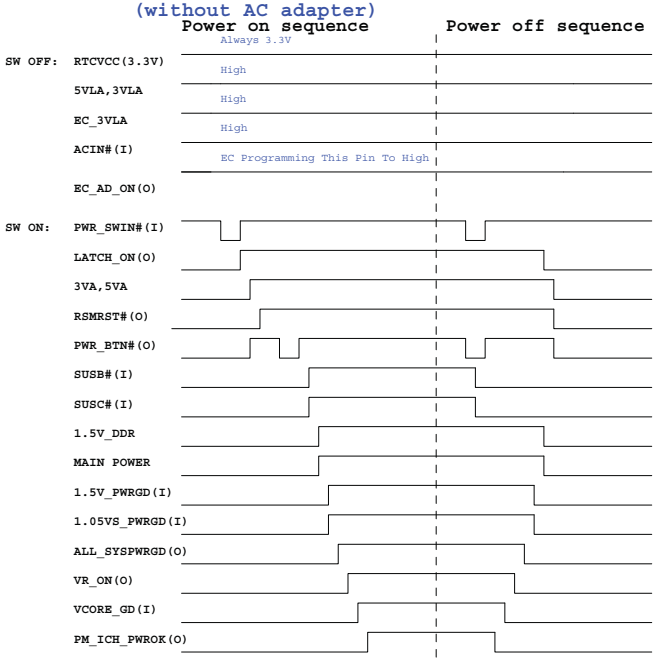
SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

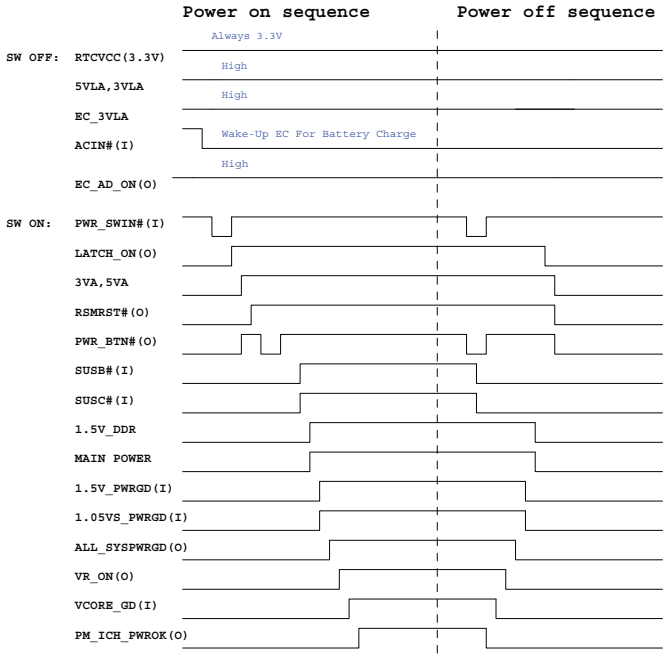
Power on/off sequence AC insert (without Battery Pack)



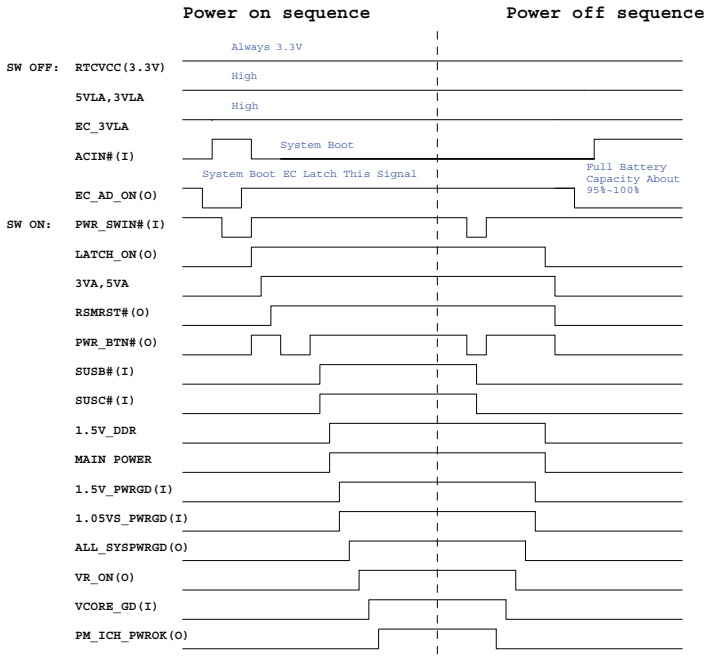
Power on/off sequence Battery insert (without AC adapter)



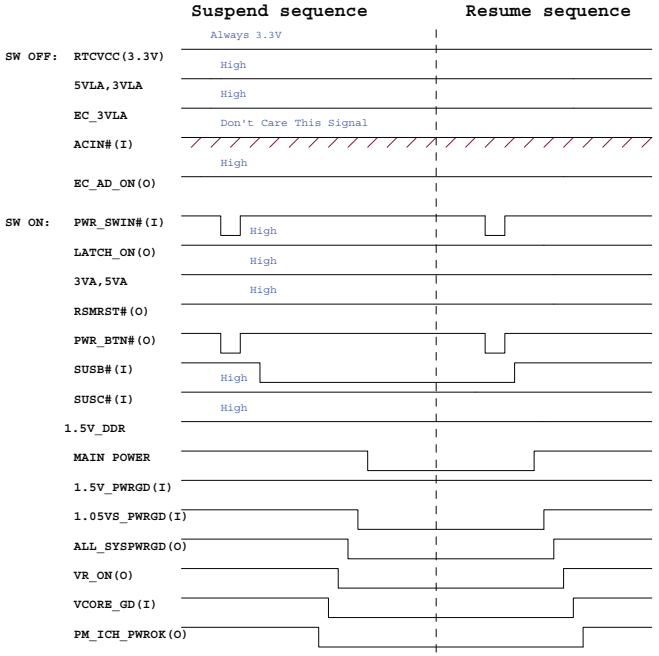
Power on/off sequence AC insert(with charge over 95%)



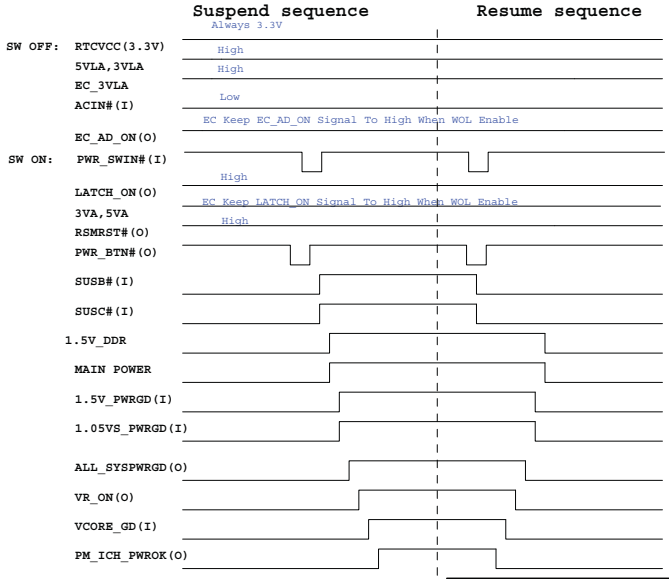
Power on/off sequence AC insert(without charge over 95%)



Suspend And Resume Sequence (S3)



Power on/off sequence after windows shoutdown (WOL enable)



INVENTEC

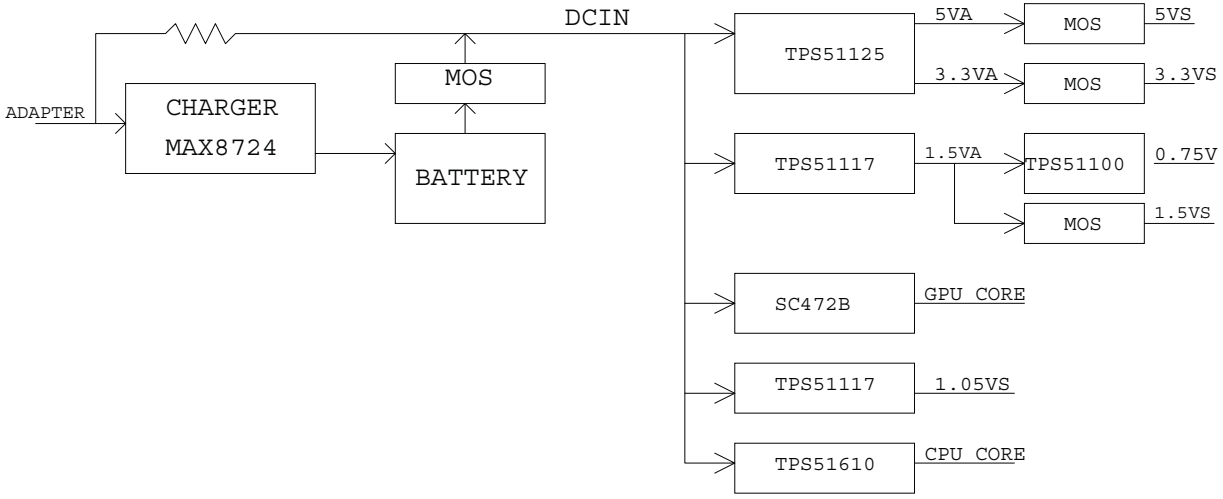
TITLE
BAP31U
Time Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 6 of 35

CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

Power Block Diagram :



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

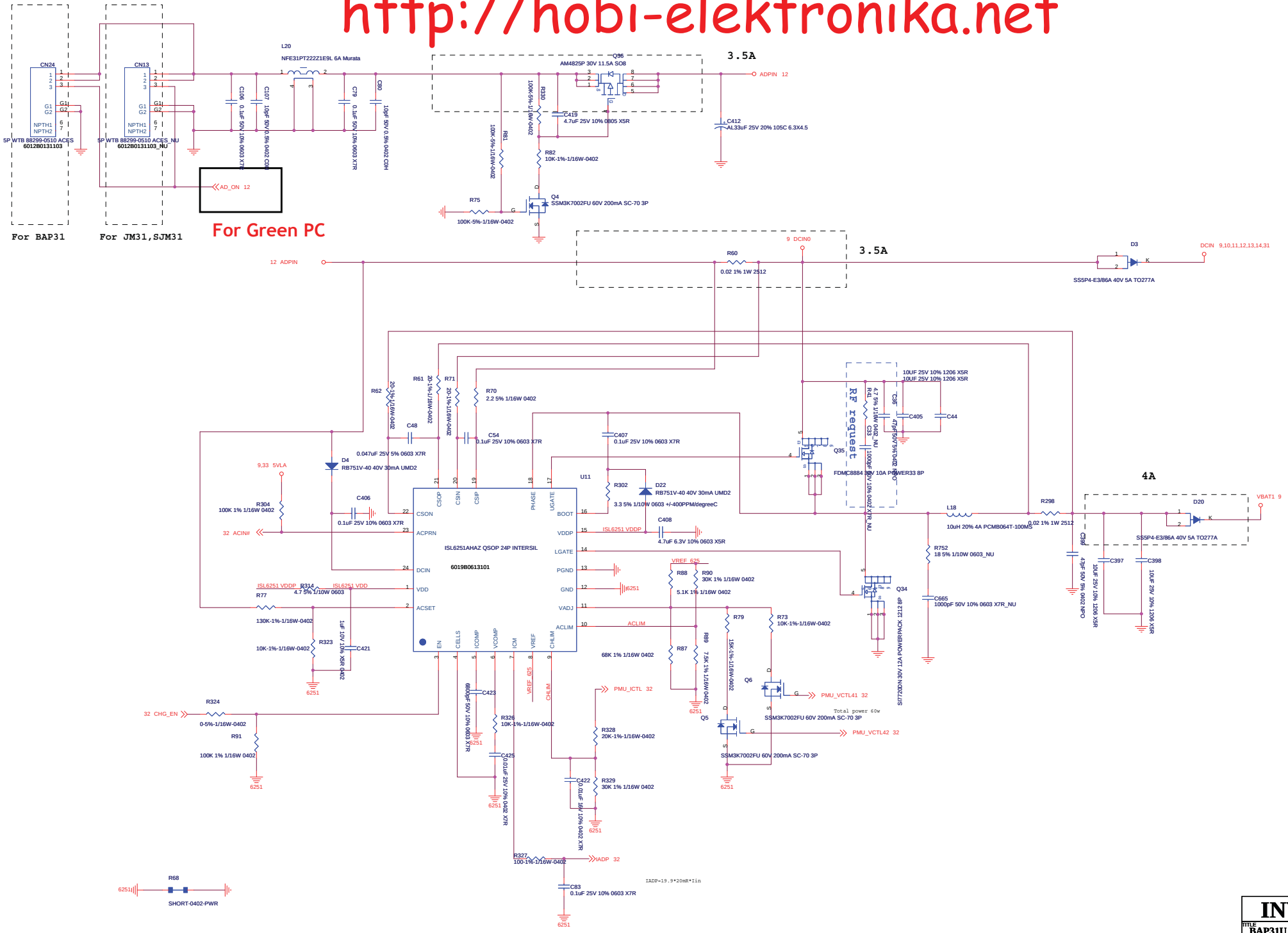
INVENTEC

TITLE BAP31U

Power Block Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 7 of 35



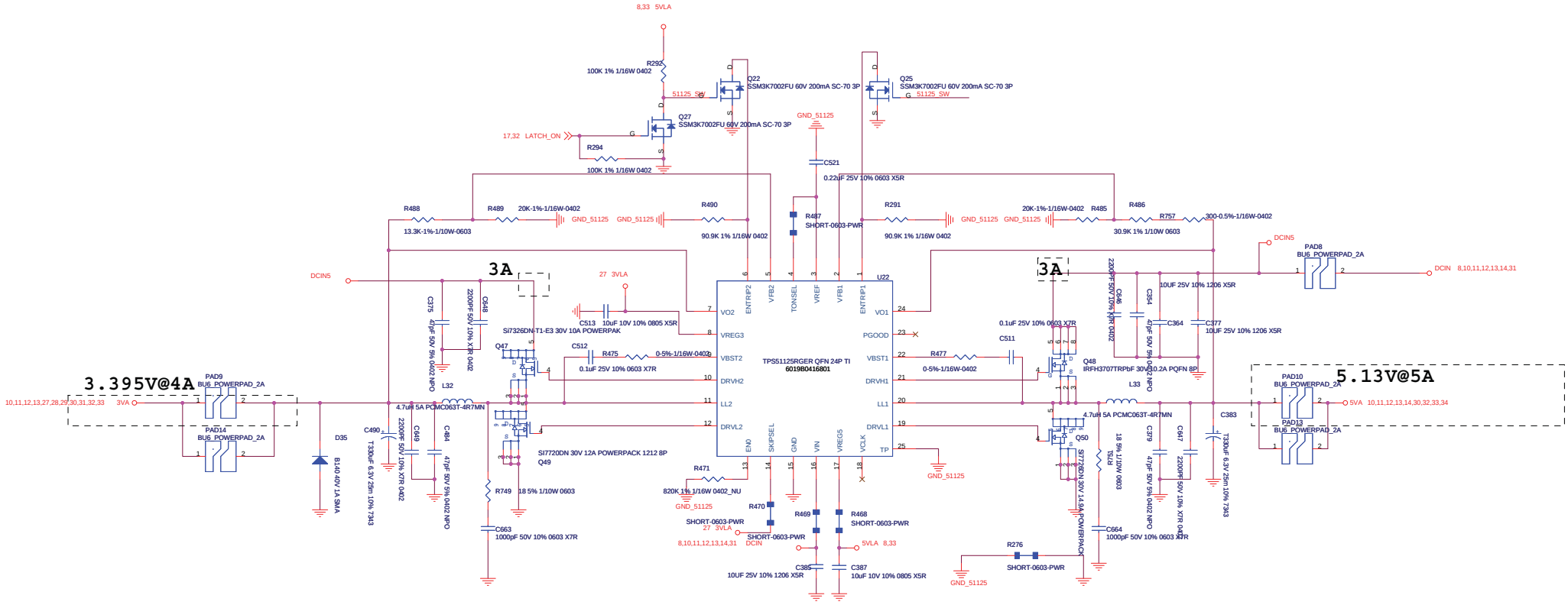
CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

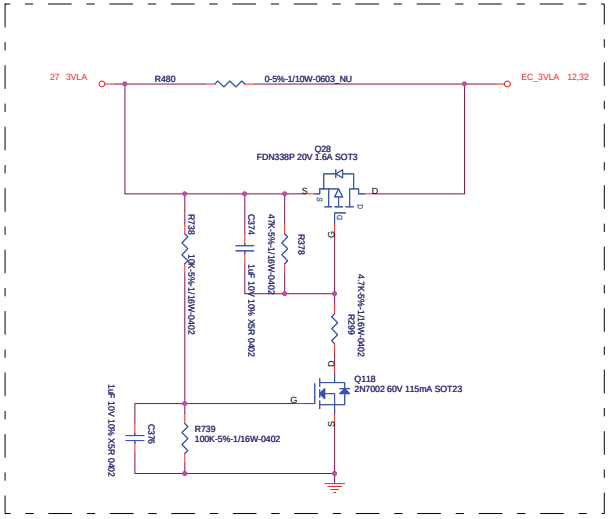
TITLE: **BAP31U** — Adaptor in / Charge

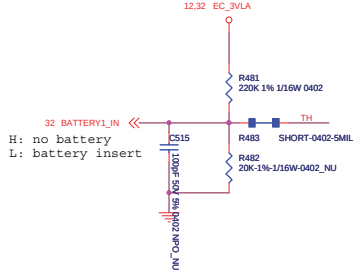
SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

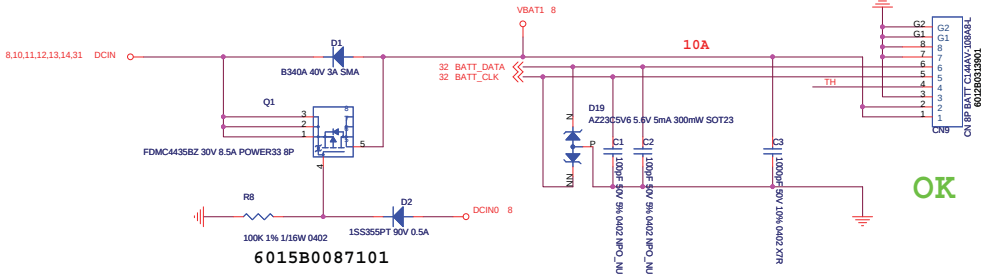
SHEET 8 of 35



For Green PC







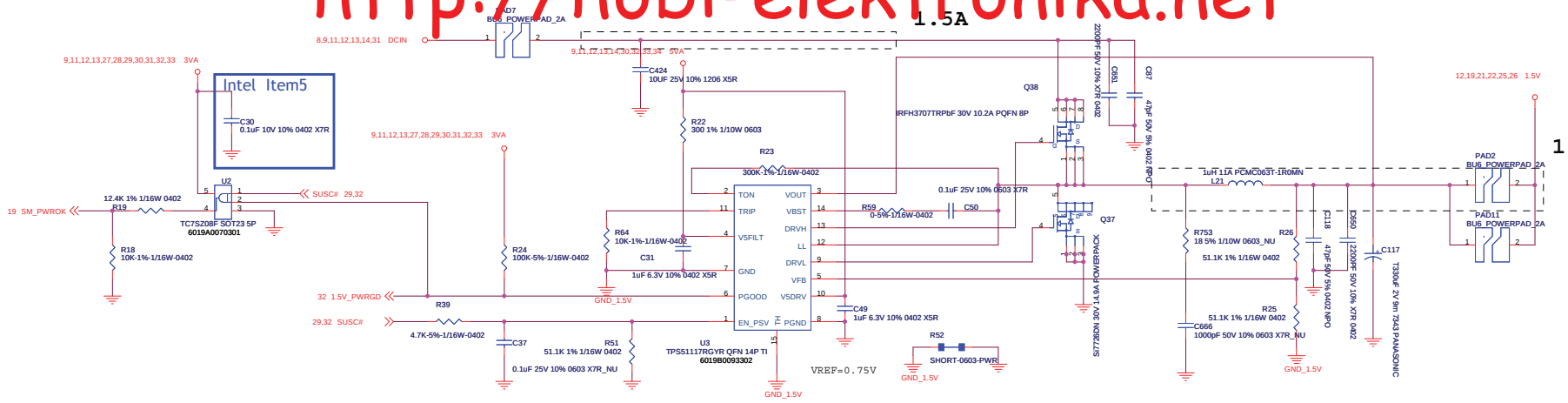
CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009	SHEET	9 of 35

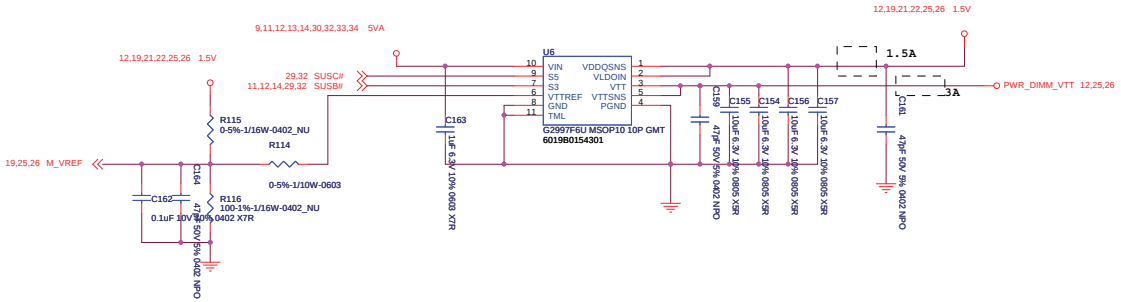
INVENTEC

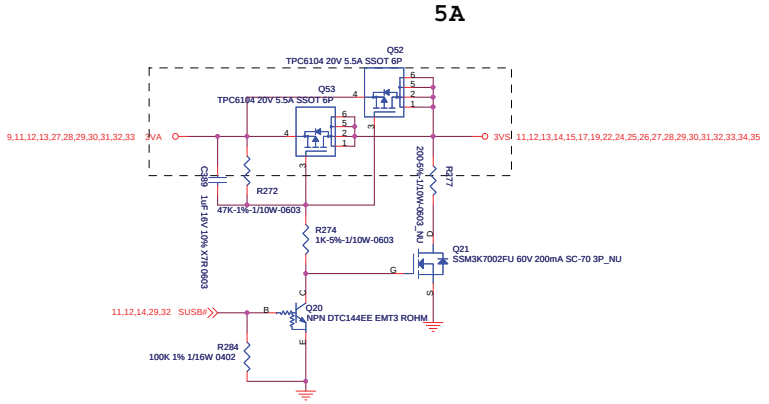
TITLE **BAP31U**

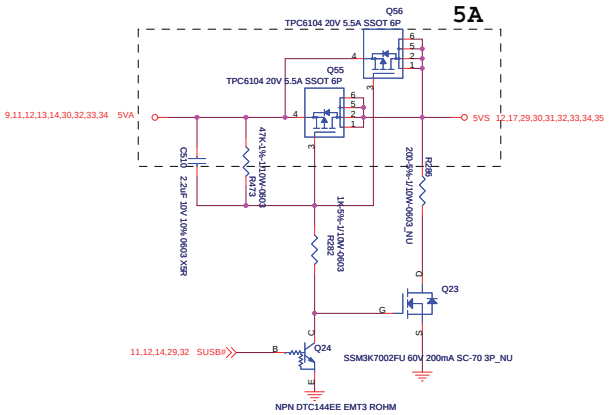
5VLA/5VA/3VLA/3VA

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

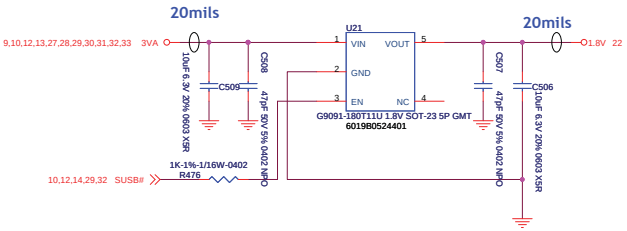


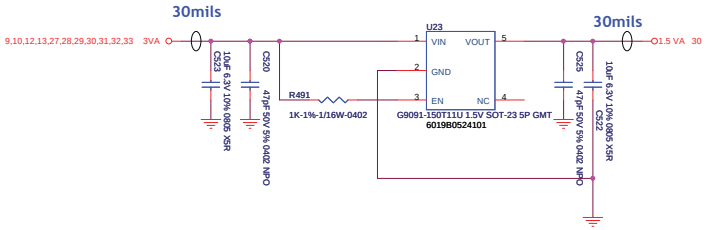


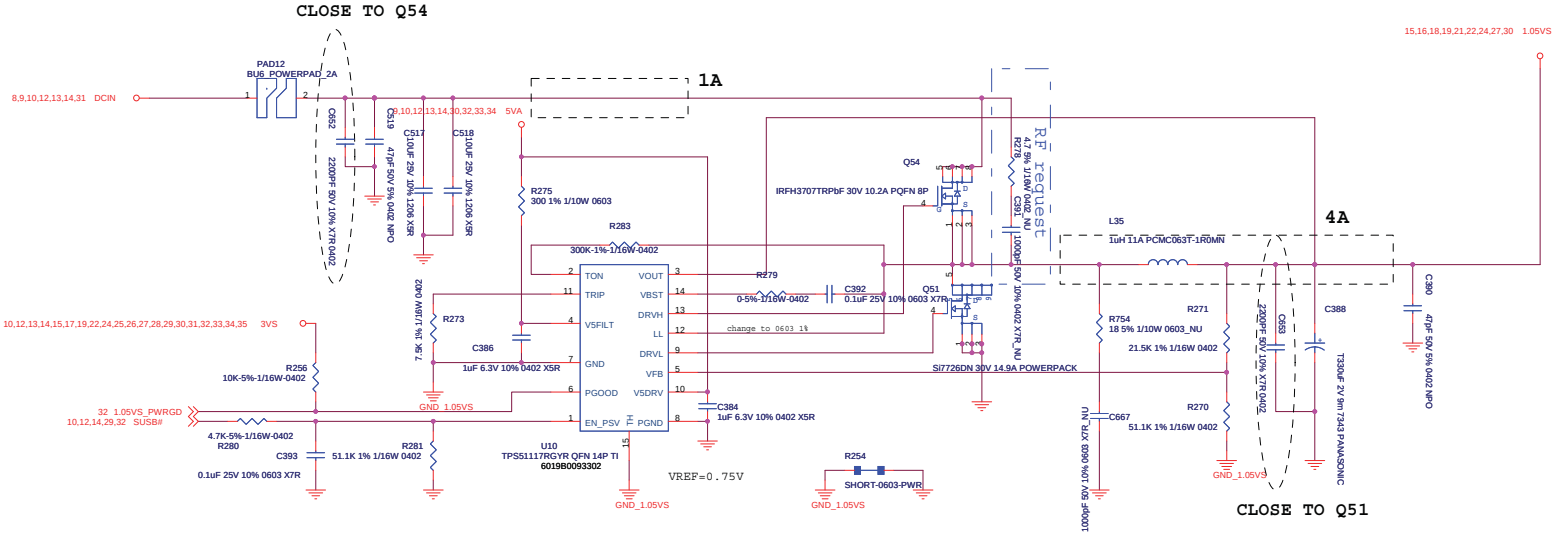




INVENTEC			
TITLE: BAP31U			
3VS/5VS/1.5V (DDR3)			
SIZE: Custom	CODE: AX1	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: A01
		SHEET: 10 of 35	
CHANGE by: Harry Chen	DATE: Wednesday, May 20, 2009		







CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

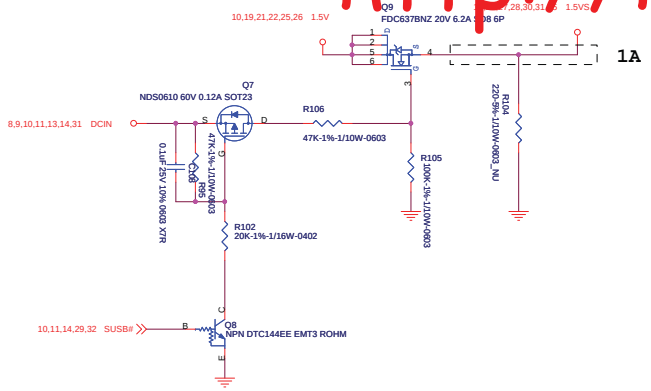
TITLE: **BAP31U**

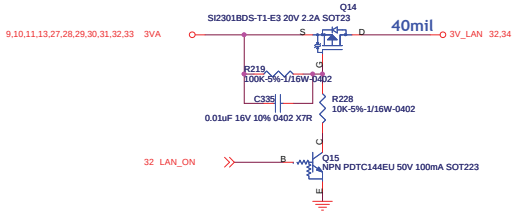
1.05VS/1.5S/1.8V/1.5VA

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

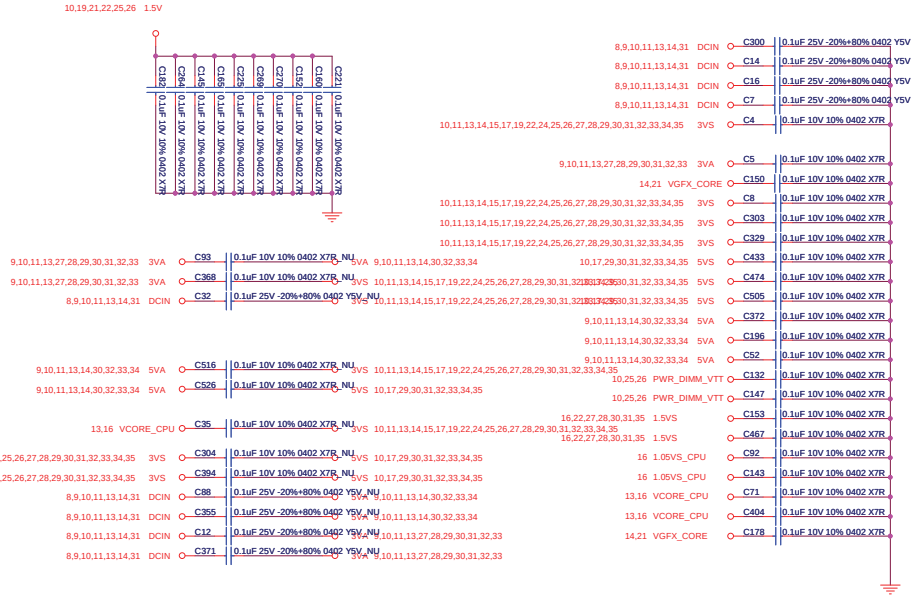
SHEET 11 of 35

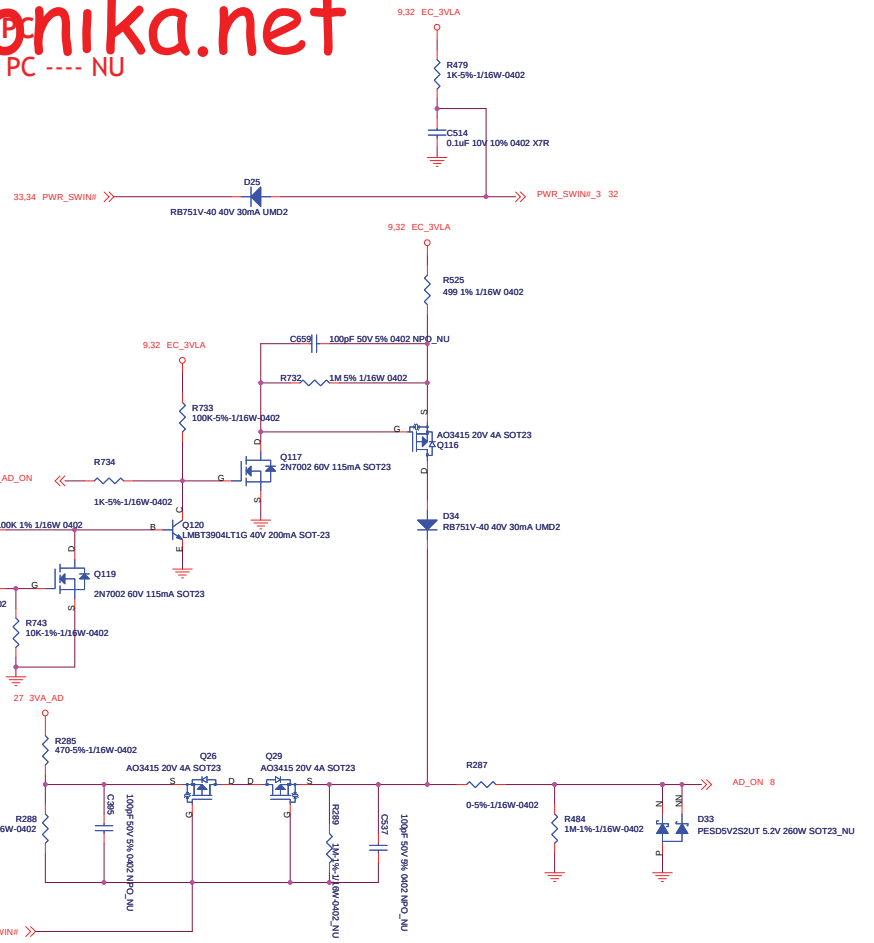
1.5VS

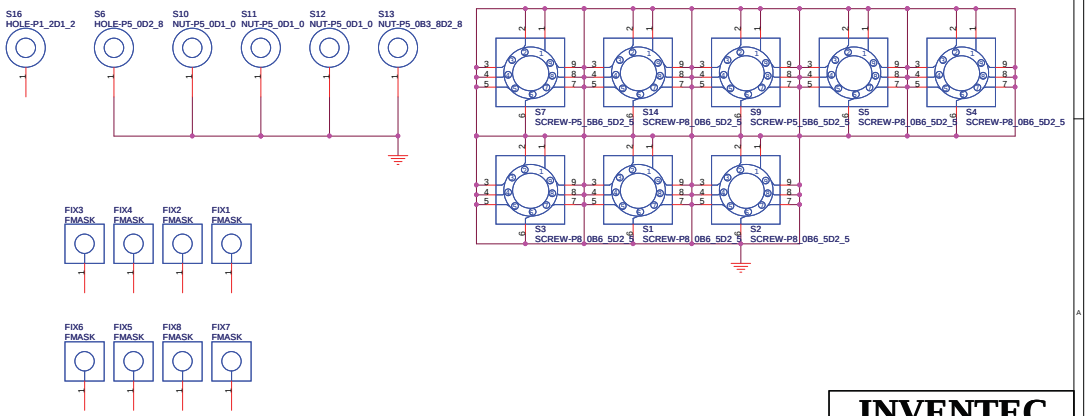




EMI Cap







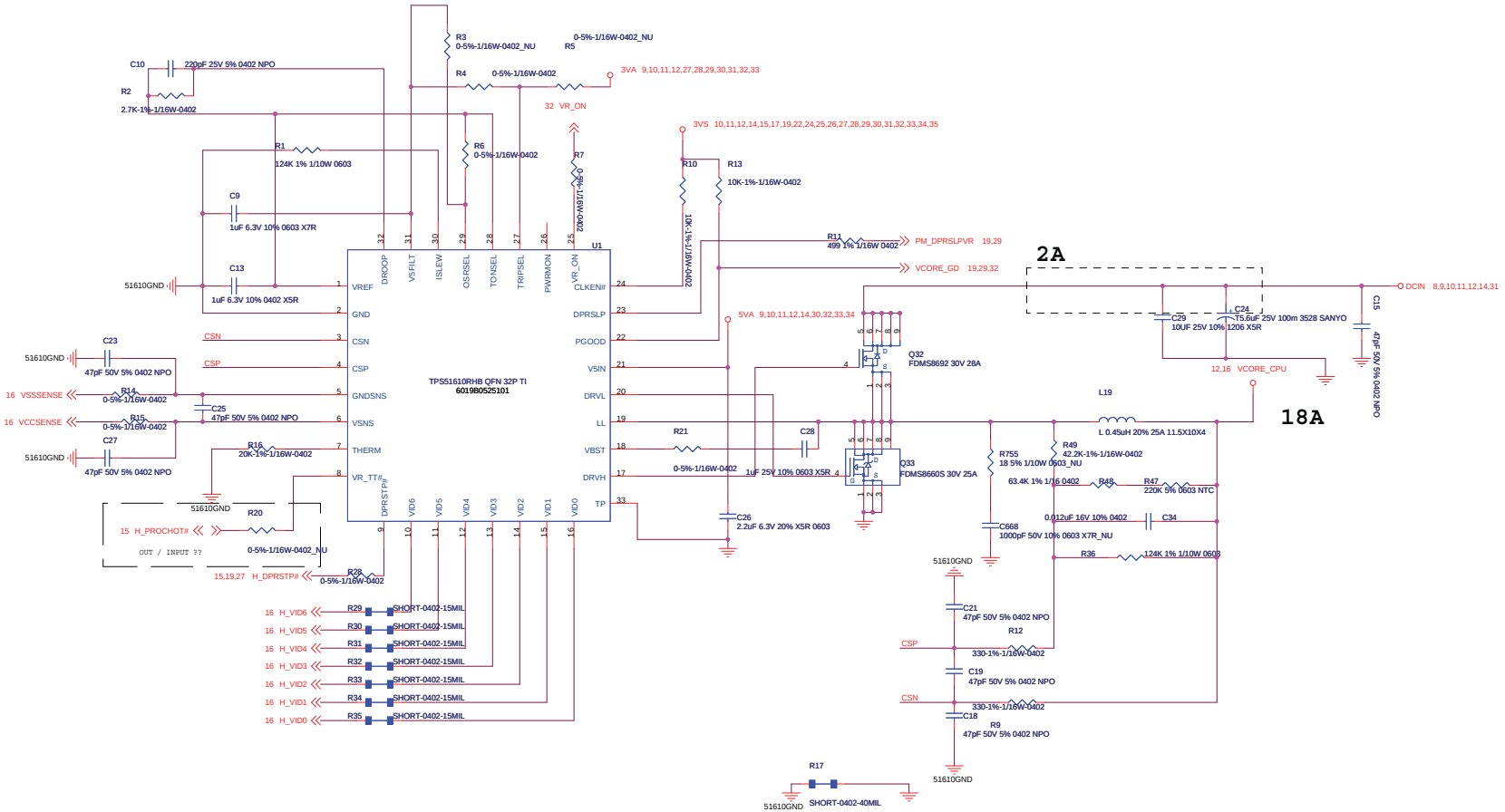
INVENTEC

TITLE: BAP31U

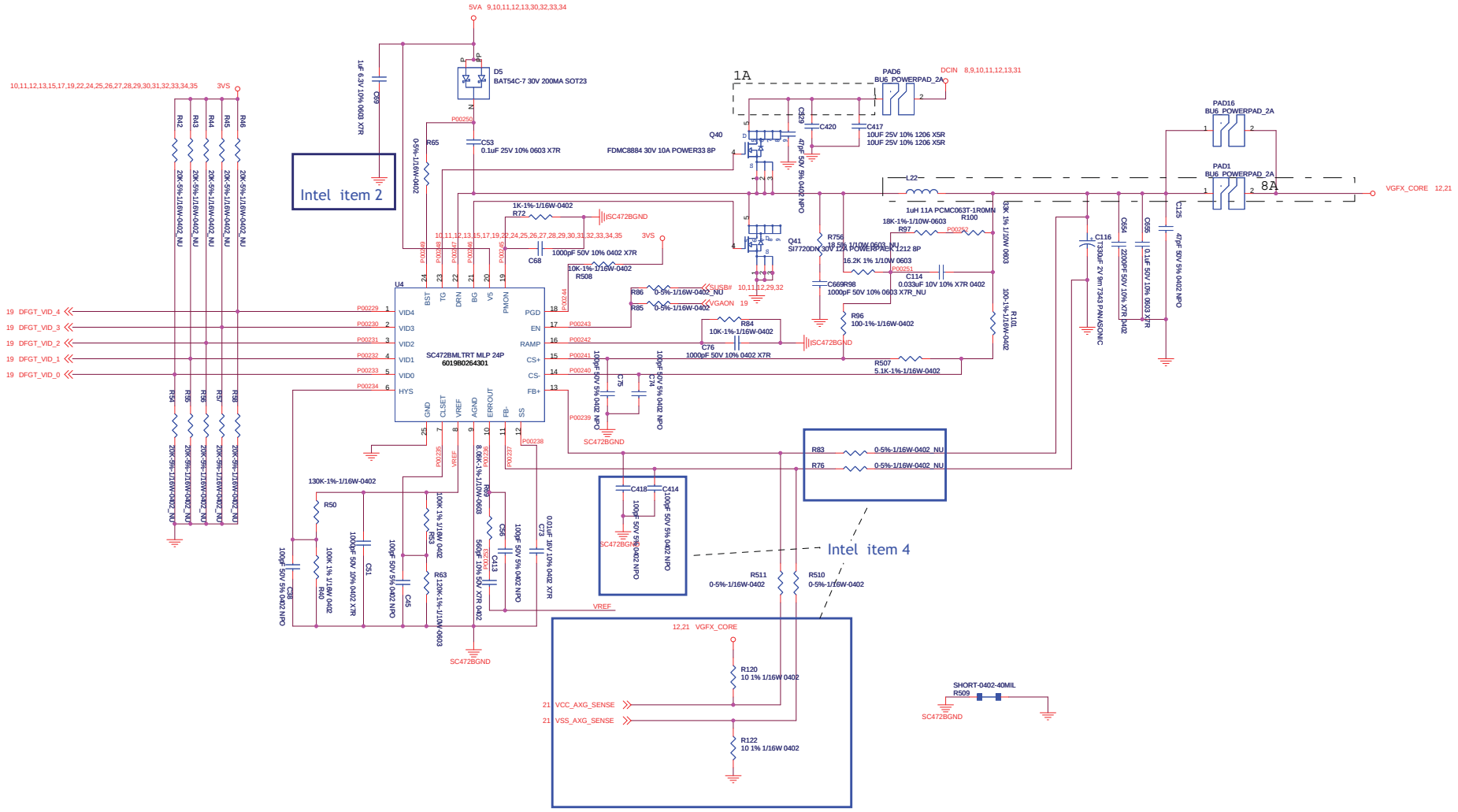
Power on latch

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

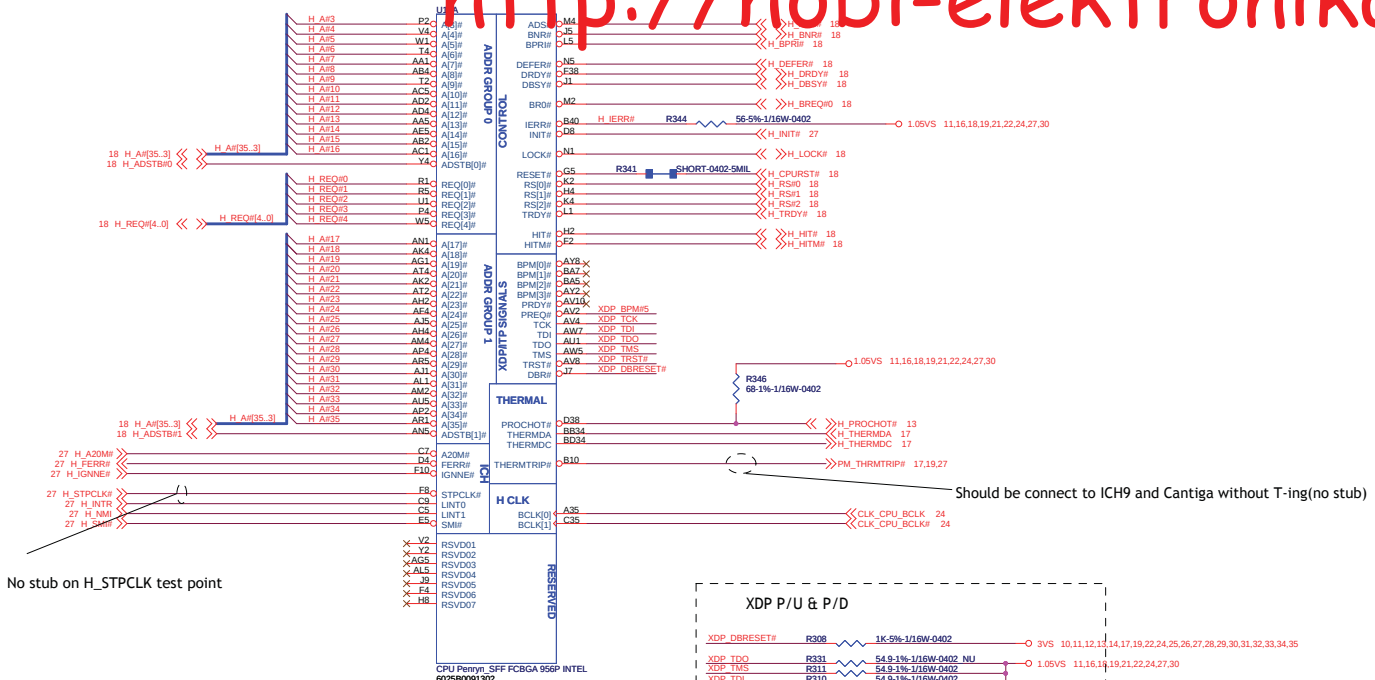
CHANGE by: Harry Chen | DATE: Wednesday, May 20, 2009 | SHEET 12 of 35



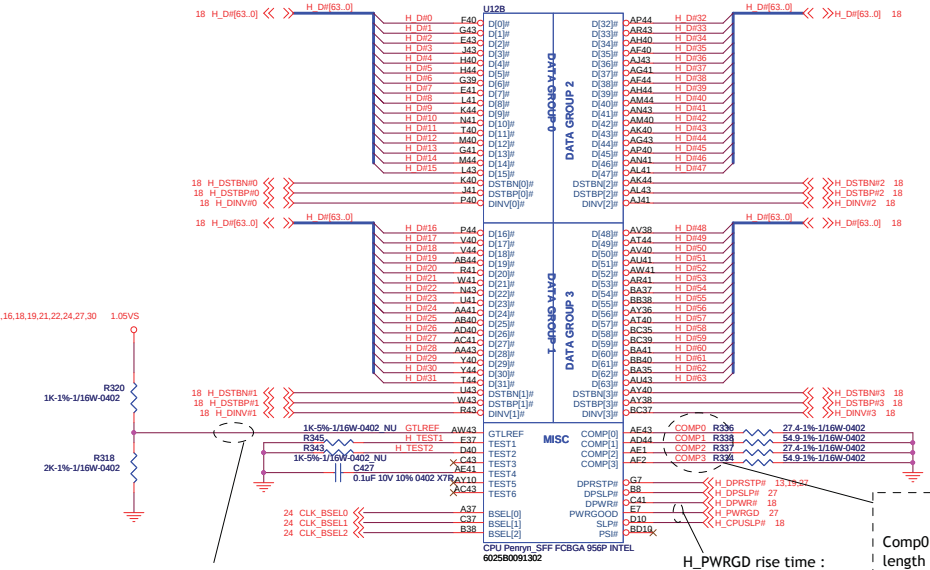
INVENTEC			
TITLE: BAP31U			
CPU Core Power			
SIZE: Custom	CODE: AX1	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: A01
		SHEET: 13 of 35	
CHANGE by: Harry Chen	DATE: Wednesday, May 20, 2009		

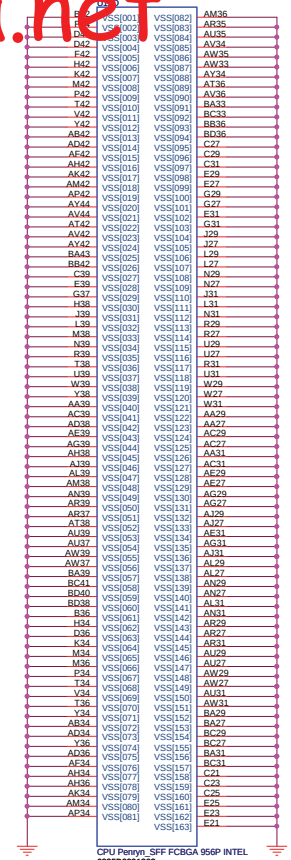


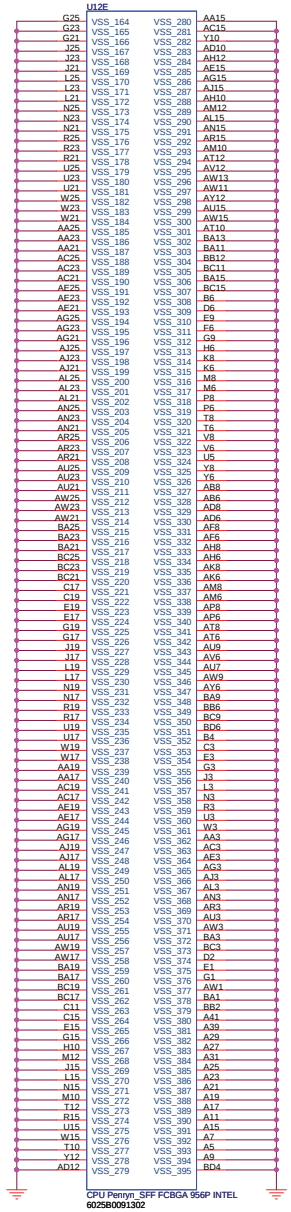
INVENTEC			
TITLE: BAP31U			
GPU CORE			
SIZE: Custom	CODE: AX1	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: A01
		SHEET: 14 of 35	
CHANGE by: Harry Chen	DATE: Wednesday, May 20, 2009		



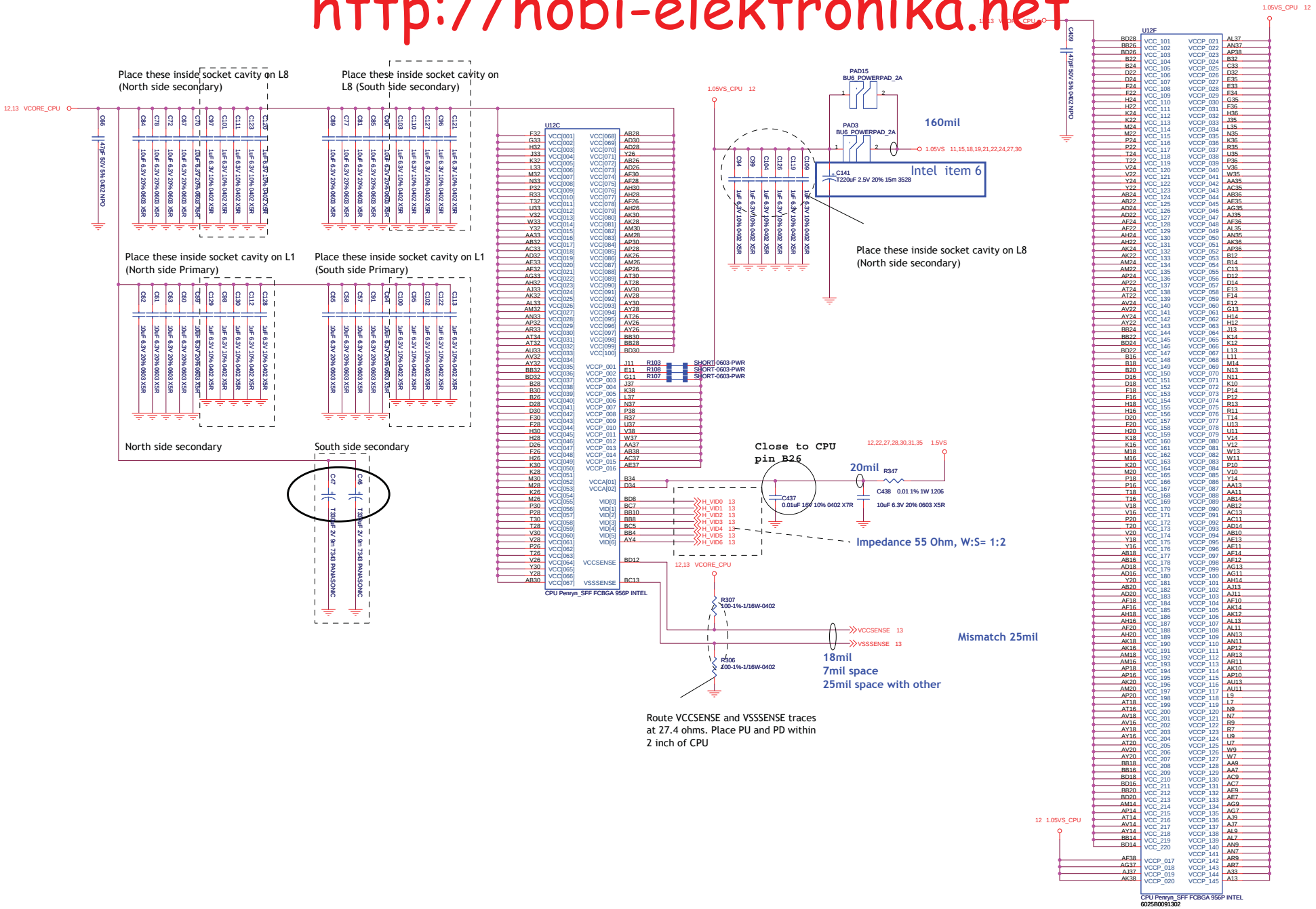
A#[32-39], APM#[0-1]:Leave escape routing on for future functionality







INVENTEC			
TITLE: BAP31U			
Penryn Processor(1/2)			
SIZE: Custom	CODE: AX1	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: A01
CHANGE by: Harry Chen	DATE: Wednesday, May 20, 2009	SHEET: 15 of 35	



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

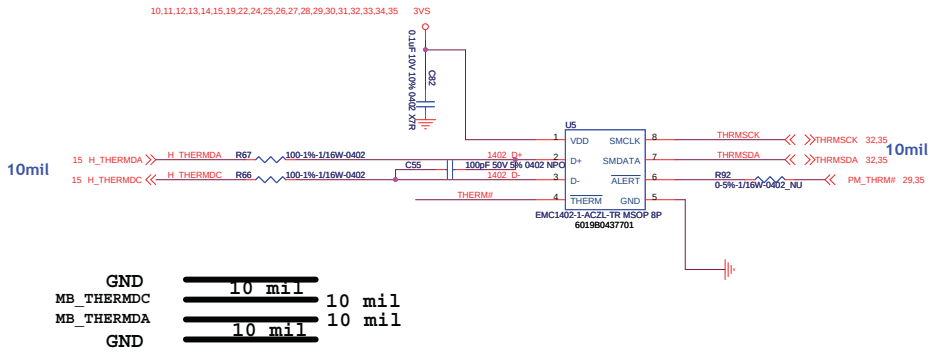
INVENTEC

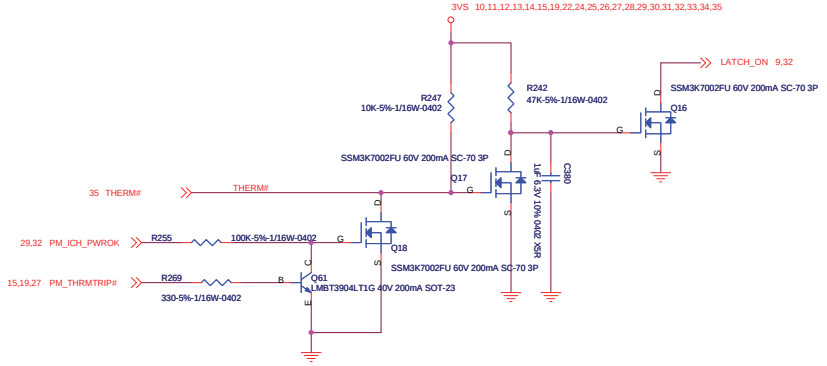
TITLE: **BAP31U**
Penryn Processor(2/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

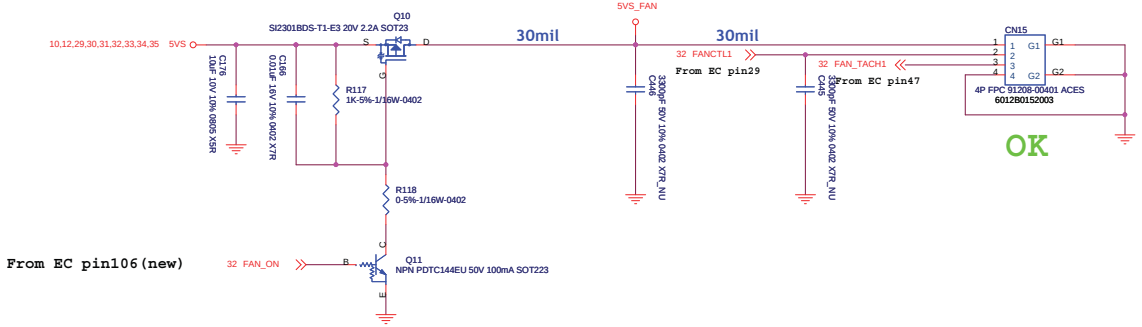
SHEET 16 of 35

THERMAL SENSOR





Fan control



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

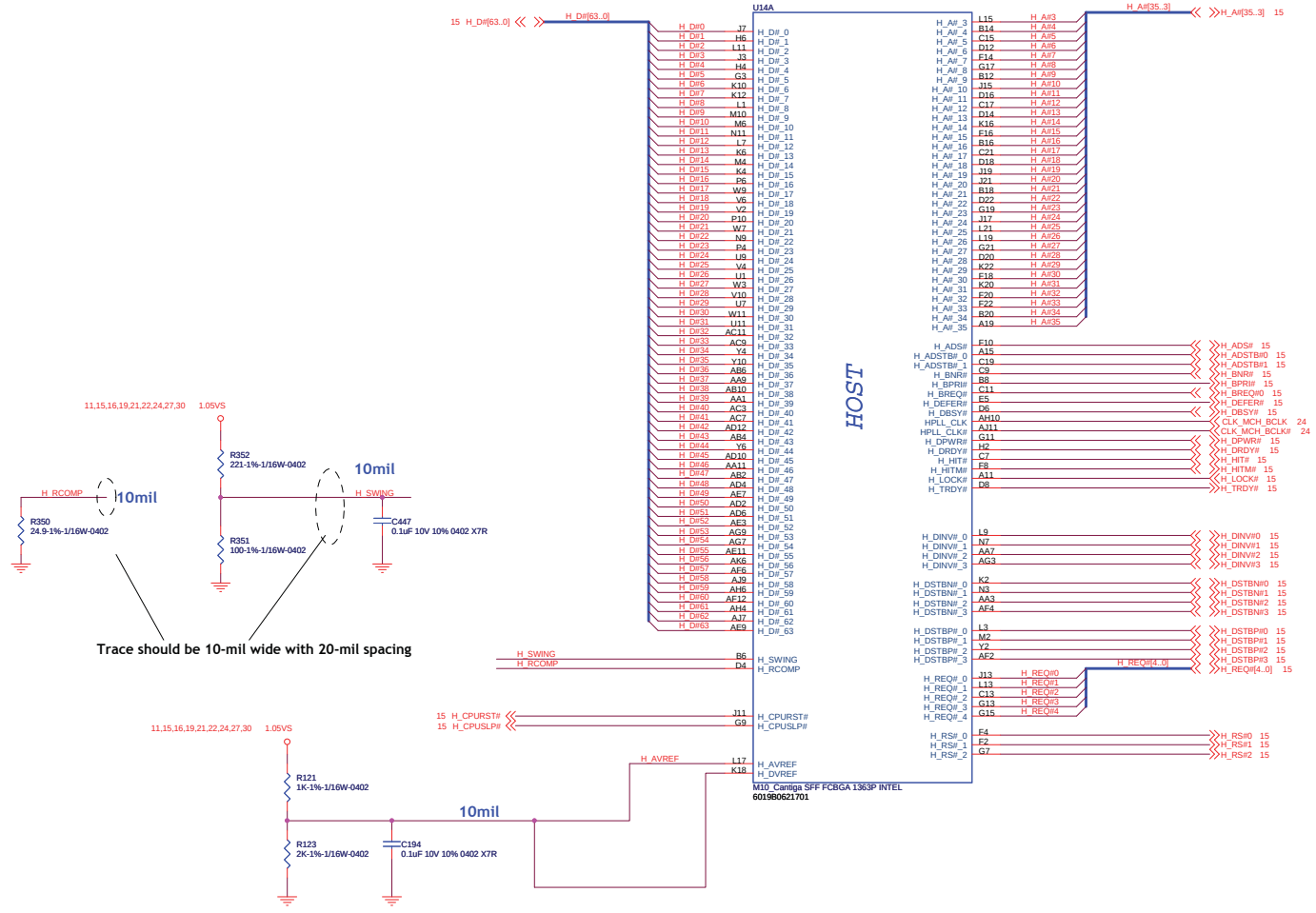
INVENTEC

TITLE: **BAP31U**

CPU Thermal

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 17 of 35



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE: **BAP31U**

Cantiga Host(1/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 18 of 35

Route M_OCDCMOP 0&1 as short as possible

Place 150ohm termination resistor close to GMCH

As close as possible to GMCH and Minimum spacing of 20 mils away from any toggle signals

When the display is completely white , the RGB voltage is between 665mV to 770mV by VESA Spec

If meet , CRT_IREF resistor value is optimal

INTEL SPEC : 75nF ~ 200nF

Cantiga Strapping:

	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG6(iTPM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIE Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIE loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIE x1 is operation	Only SDVO or PCIE x1 with PEG port

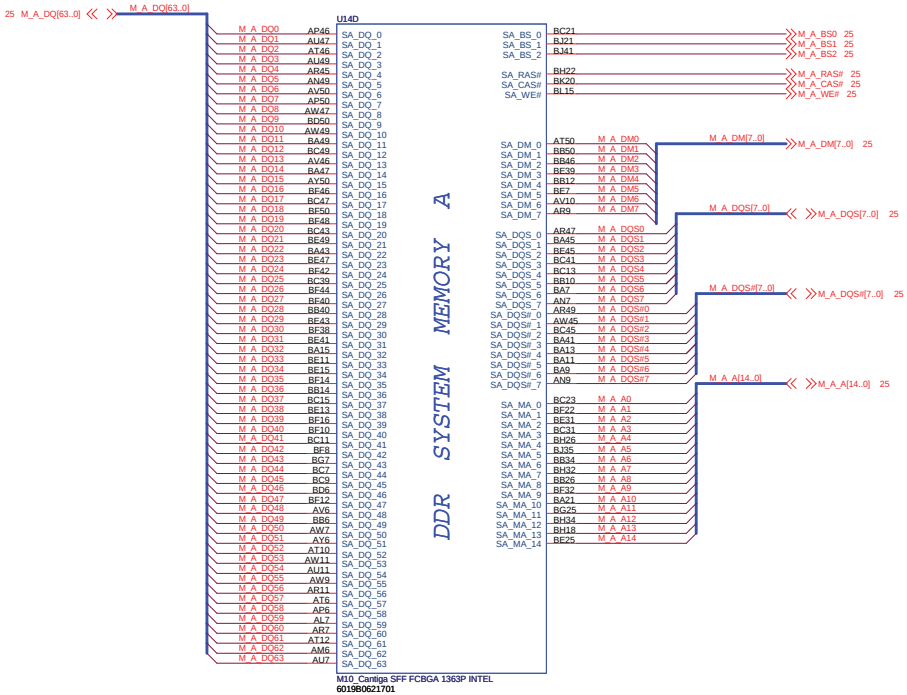
INVENTEC

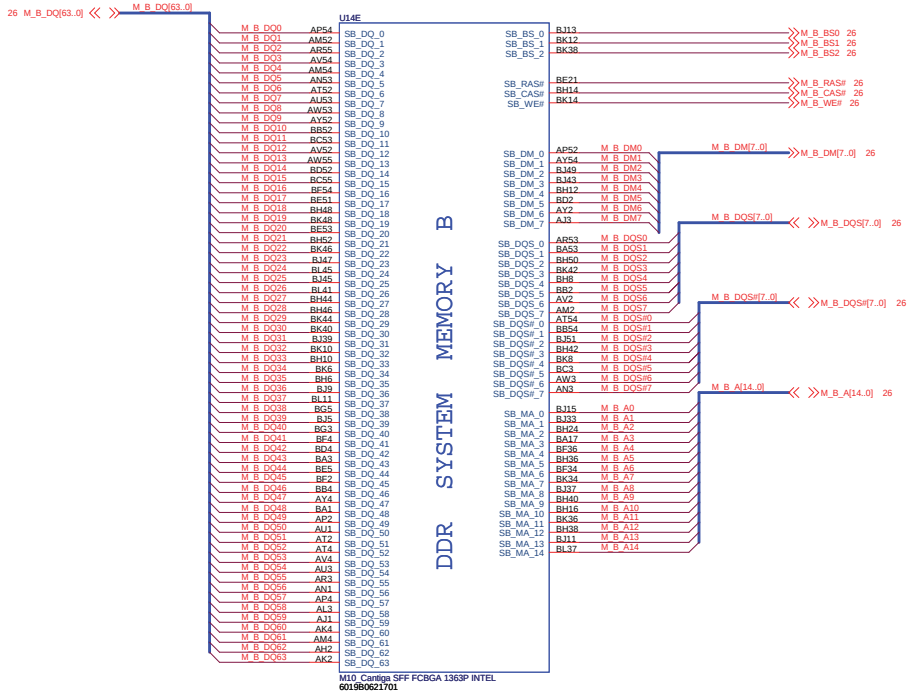
TITLE: BAP31U

Cantiga DMI/Graph2/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

CHANGE by: Harry Chen | DATE: Wednesday, May 20, 2009 | SHEET 19 of 35





CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

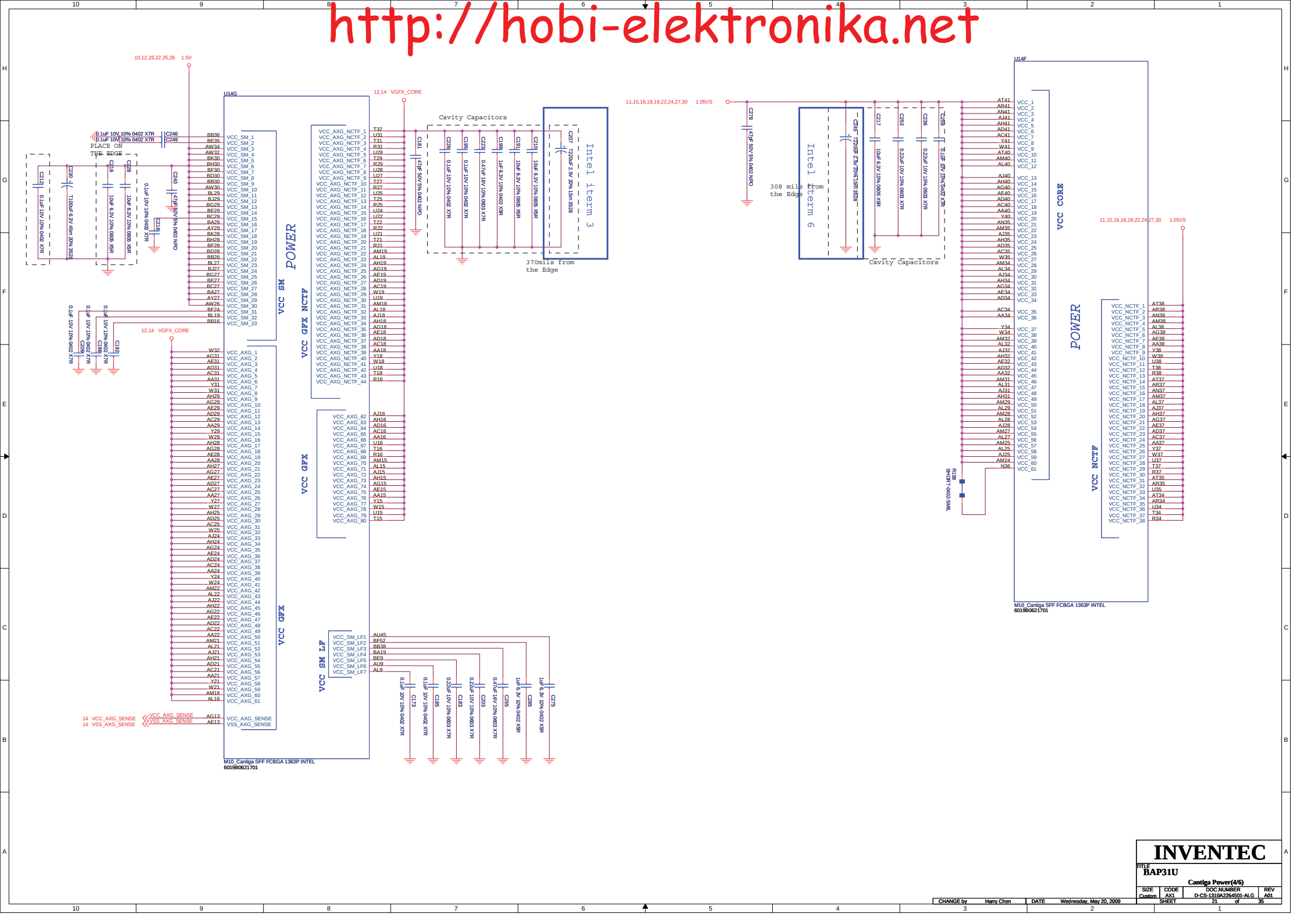
INVENTEC

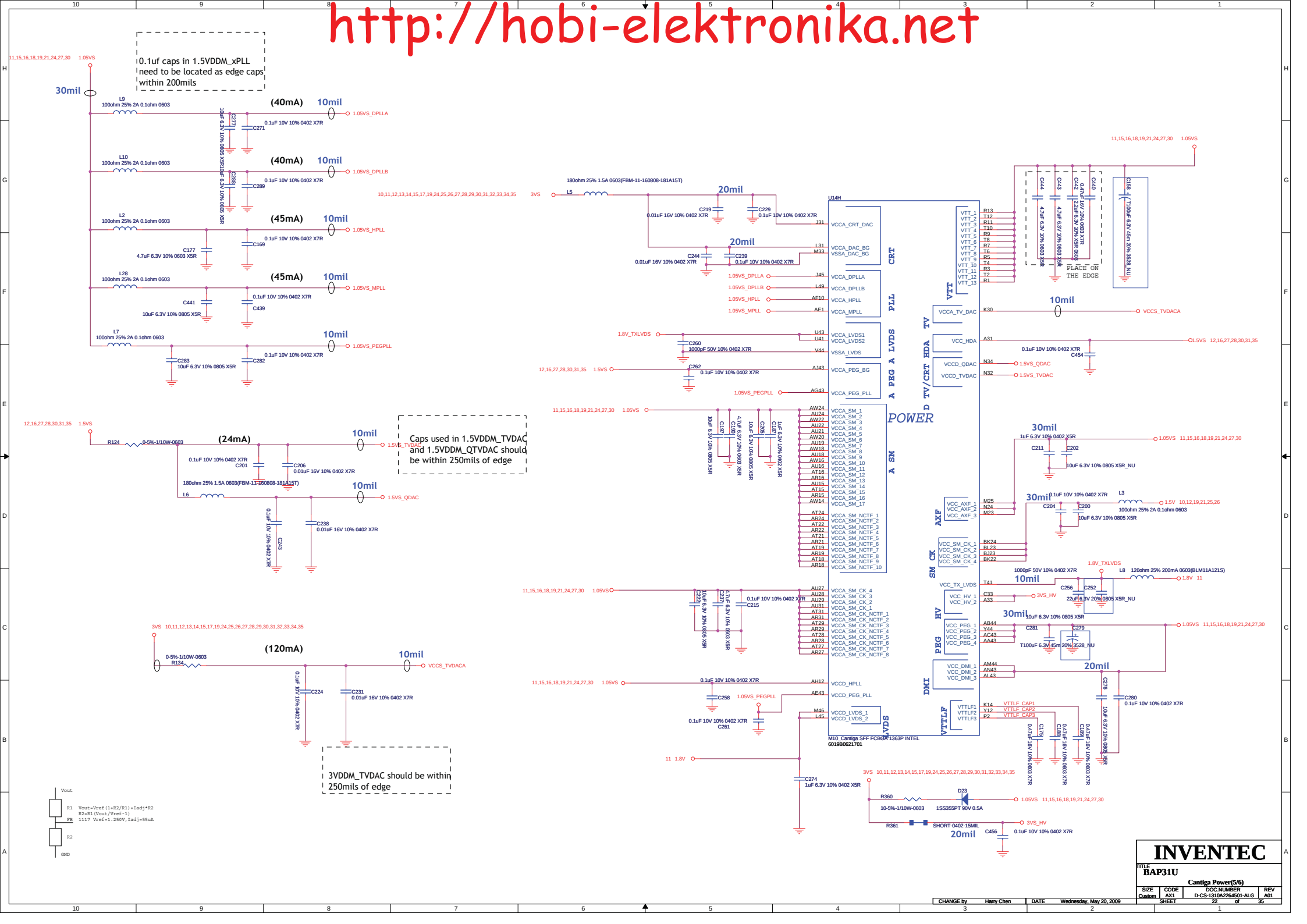
TITLE: BAP31U

Cantiga DDR3(3/6)

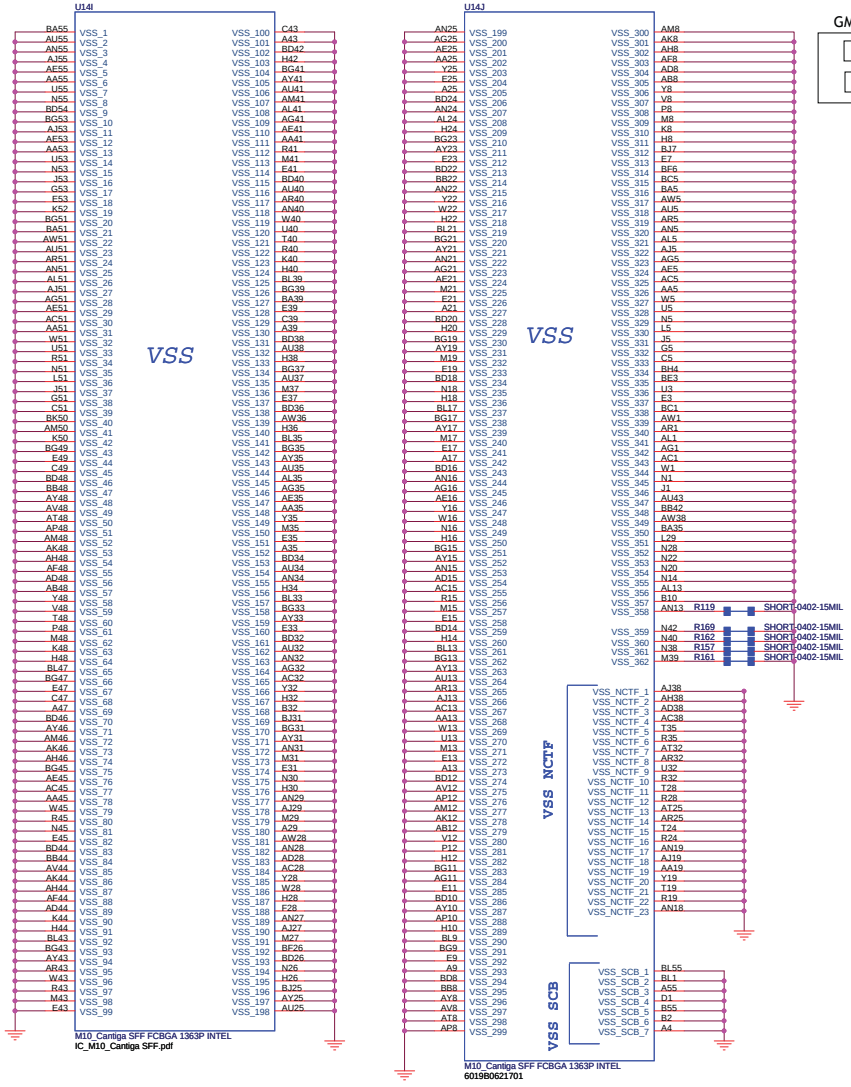
SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 20 of 35

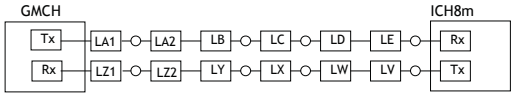




INVENTEC			
TITLE: BAP31U			
Cantiga Power(5/6)			
SIZE: Custom	CODE: AX1	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: A01
CHANGE by: Harry Chen	DATE: Wednesday, May 20, 2009	SHEET: 22 of 35	



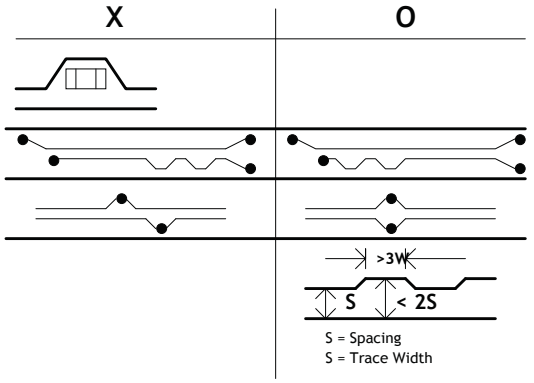
DMI Routing Guideline



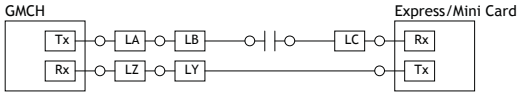
Breakout/in LA/LZ	Main Route LB/LY		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



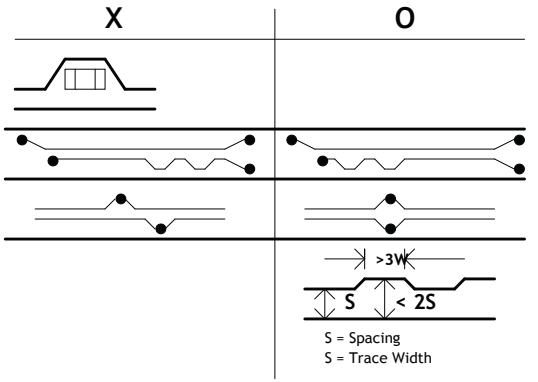
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



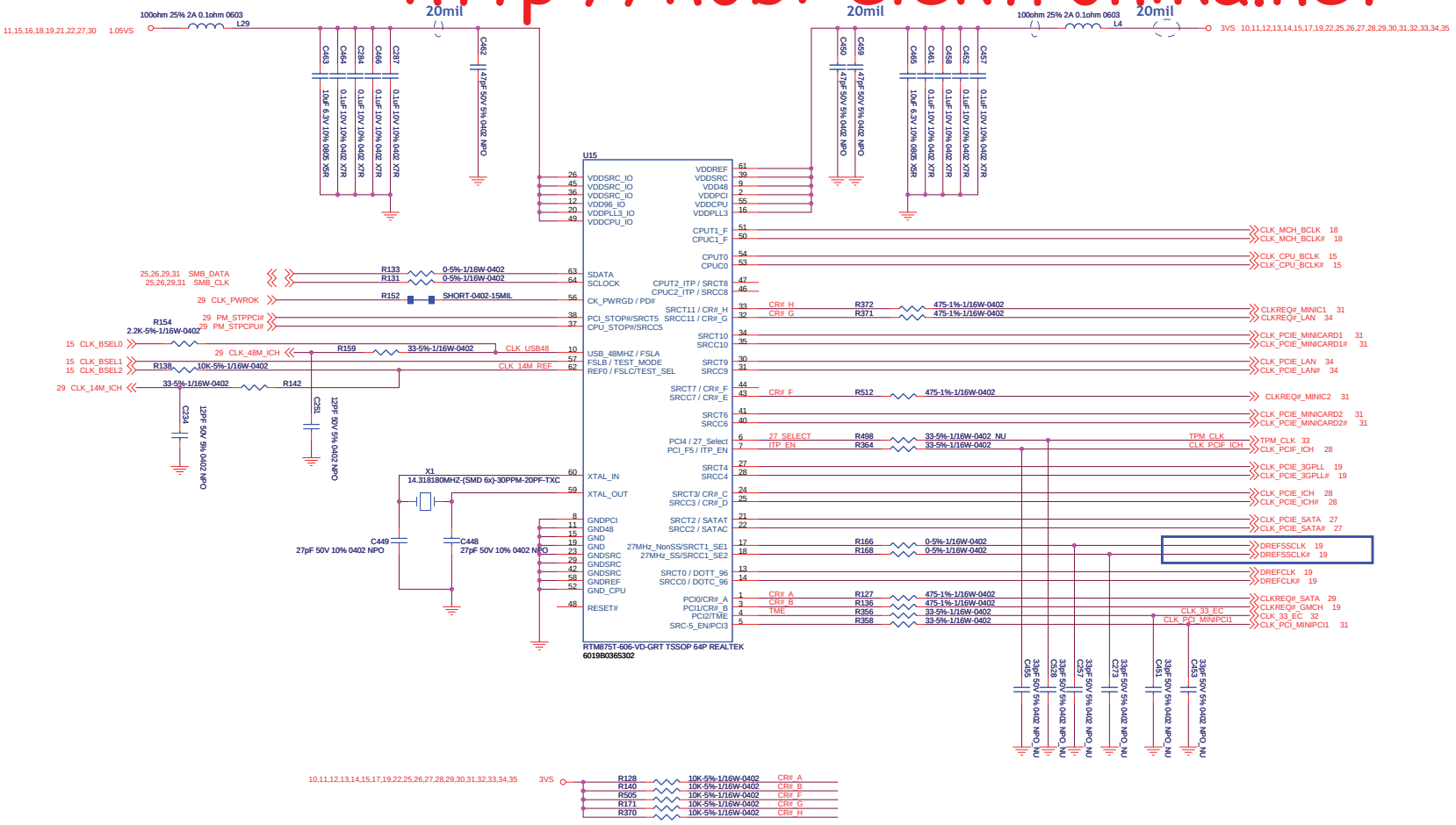
INVENTEC

TITLE BAP31U
Cantiga Ground(6/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 23 of 35

CHANGE by Harry Chen | DATE Wednesday, May 20, 2009



CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266 *

By Tony

CHANGE by	Harry Chen
DATE	Wednesday, May 20, 2009

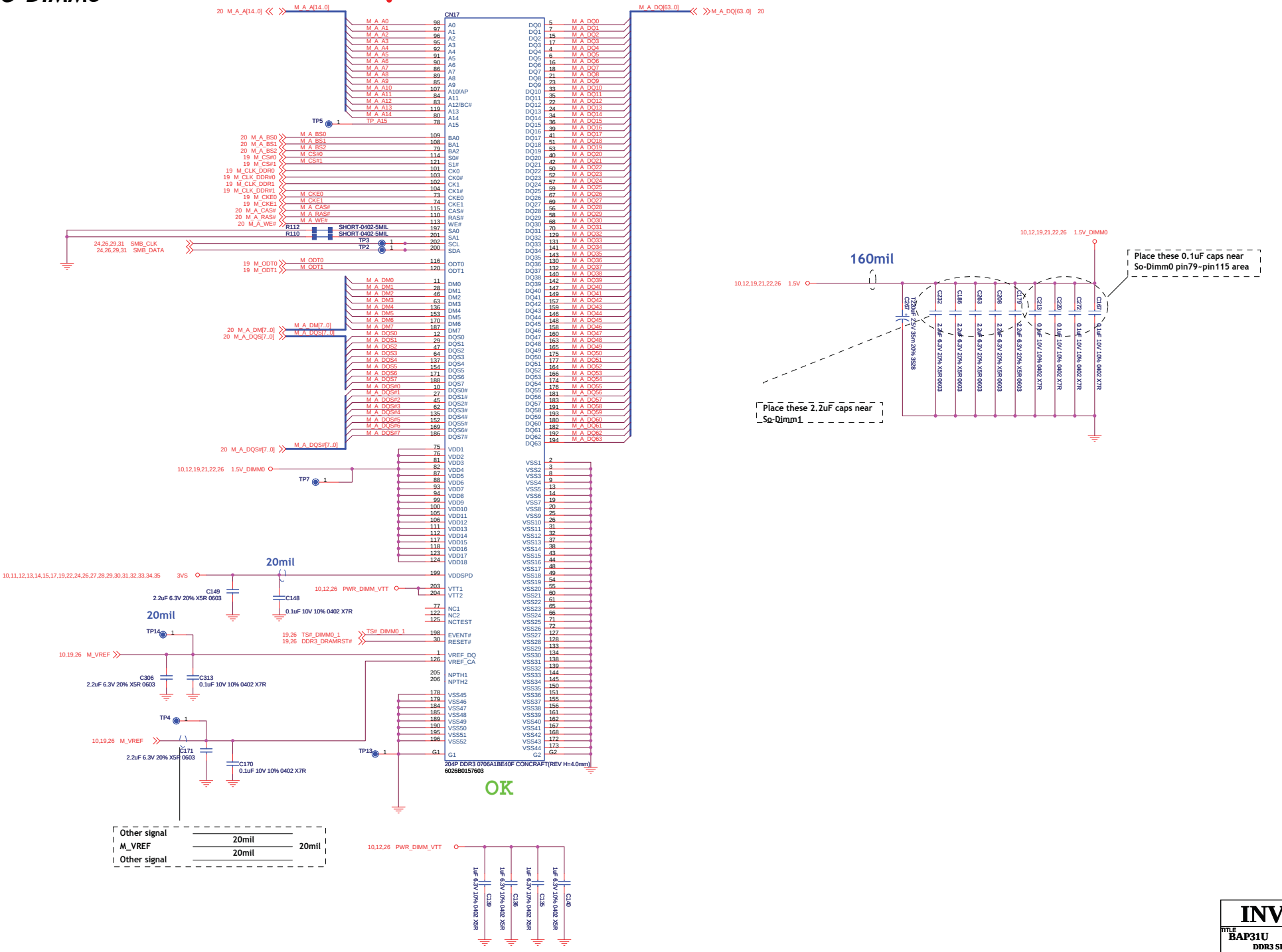
INVENTEC

TITLE: BAP31U
Clock Generator

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 24 of 35

SO-DIMM0



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

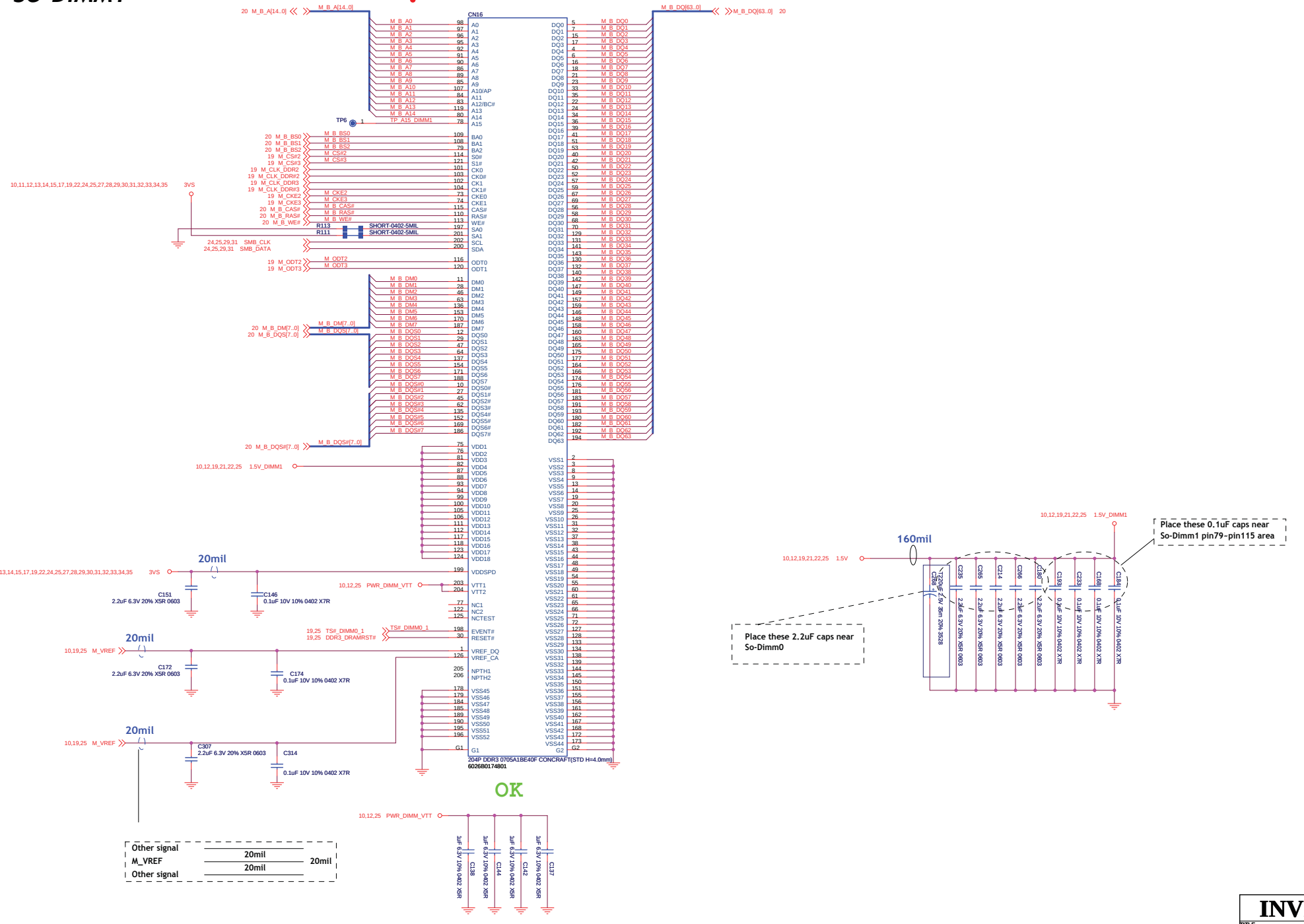
INVENTEC

TITLE
BAP31U
DDR3 SDRAM SO-DIMM0

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 25 of 35

SO-DIMM1



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

INVENTEC

TITLE
BAP31U
DDR3 SDRAM SO-DIMM1

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01
	SHEET	26 of 35	

RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

For JM31,SJM31 For BAP31

For Green PC

BATT1

123

CABLE,ROUND,3POS,75mm,I,RTC_NU

6027B0066801

Place all series resistors 0.6 to 2.6 inches from the ICH9

Needs to be placed within 2" of ICH9m

Must be placed within 2" of 24.9 ohm w/o stub

Distance between the ICH9-M and cap on the "P" signal should be identical distance between the ICH9-M and cap on the "N" signal for same pair.

Placed within 500mils of ICH9m ball

ICH8m internal VR enable strap

	Enable	Disable
INTVRMEN	1(Default)	0

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05

Short pins AG1 and AG2 at the package

ACZ_SDATAOUT strap functionality base on RSVD9 strap

XOR chain entrance (RSVD9 pulled low)

PCIE port config bit 1(RSVD9 not pulled low)

Stuff for XOR chain testing

XOR Chain Entrance Strap - to be updated		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

By Tony

INVENTEC

TITLE: BAP31U

ICH9M CPU/IDE/SATA(1/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 27 of 35

CHANGE by: Harry Chen | DATE: Wednesday, May 20, 2009

PCIE AC coupling caps need to be within 250mils of the driver

WLAN

3G

LAN

U18D

PCI-Express Direct Media Interface

SPI

USB

M10_ICH9M_SFF FCBGA 569P INTEL
6019B06218D1

STUFF for iTPM enable

R194 1K-5%-1/16W-0402_NU

R206 24.9-1%-1/16W-0402

10mil

Place within 500mils of ICH

USB P0--------> USB port
USB P1--------> USB port
USB P2 --------> USB port
USB P3 --------> EASY PORT
USB P4 --------> WLAN
USB P5 --------> Finger printer
USB P6 --------> Bluetooth
USB P7 --------> Camera
USB P8 --------> Card Reader
USB P6 --------> 3G

R442 22.6-1%-1/16W-0402

Place within 500mils of ICH
5/5 mils spacing on microstrip

U16 W25X32VSSIG SOIC 8P Winbon_NU
6019B0499501_NU

By Tony

U18B

PCI

Interrupt I/F

M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801

PCI Pull up

Buffer to reduce loading on PLT_RST#

U17 TC7SZ08F SOT23 5P
6019A0070301

PCI_GNT#3	No stuff : by default Stuff : For A16 swap override

PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI

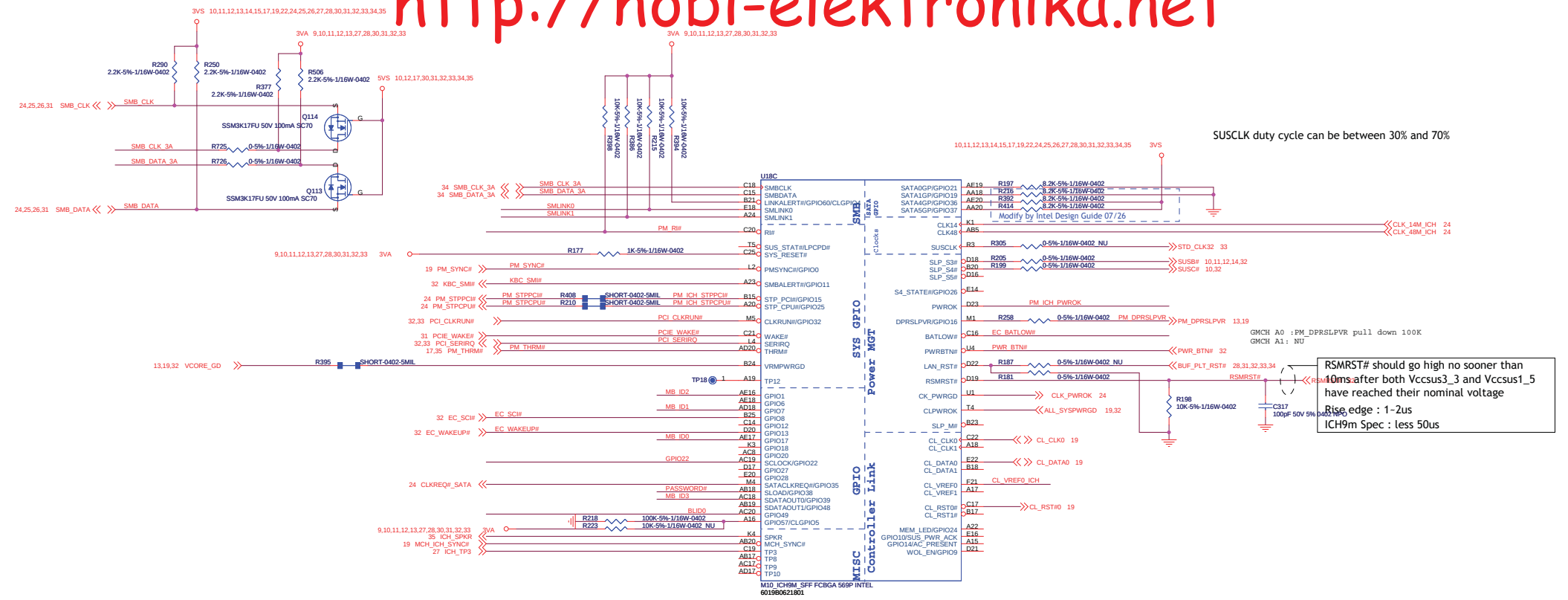
Check BIOS type

INVENTEC

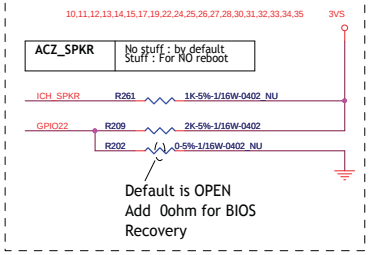
TITLE
BAP31U
ICH9M PCI/PCIE/DMI/USB(2/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

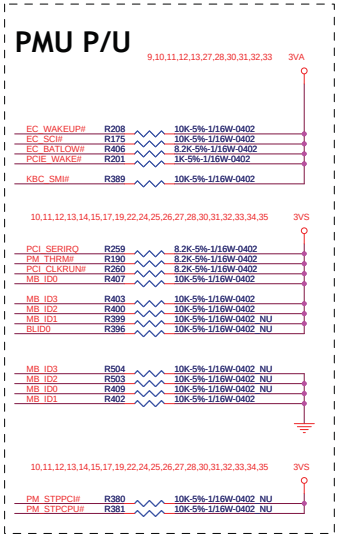
CHANGE by Harry Chen | DATE Wednesday, May 20, 2009 | SHEET 28 of 35



ICH9m strap

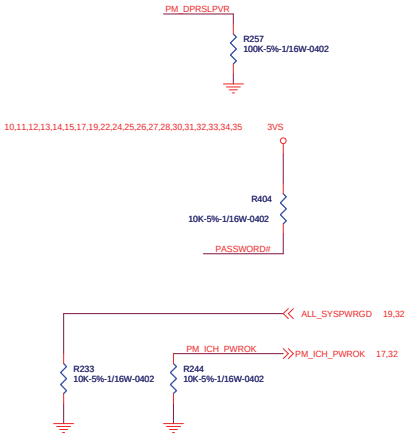


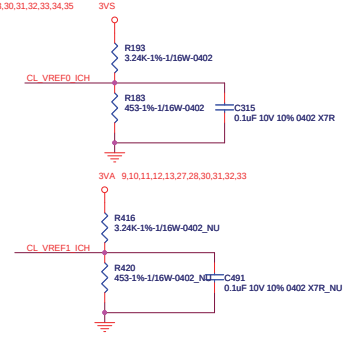
PMU P/U



BIOS ID setting

Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
	1	1	0	0
	1	0	1	1
	1	0	1	0
	1	0	0	1
	1	0	0	0
	0	1	1	1
	0	1	1	0
	0	1	0	1
	0	1	0	0
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0





CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

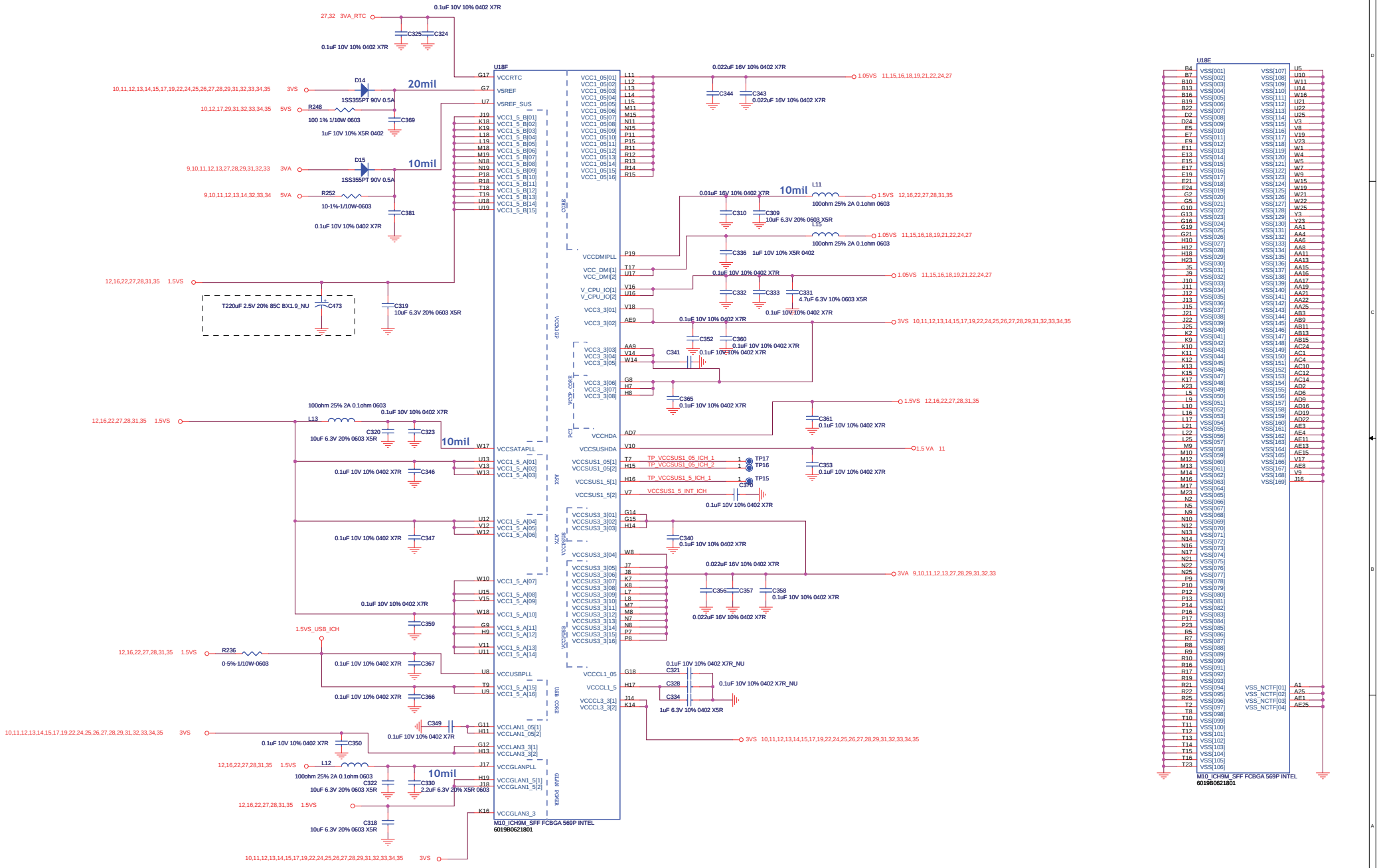
INVENTEC

TITLE: **BAP31U**

ICH9M GPIO(3/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 29 of 35



CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009

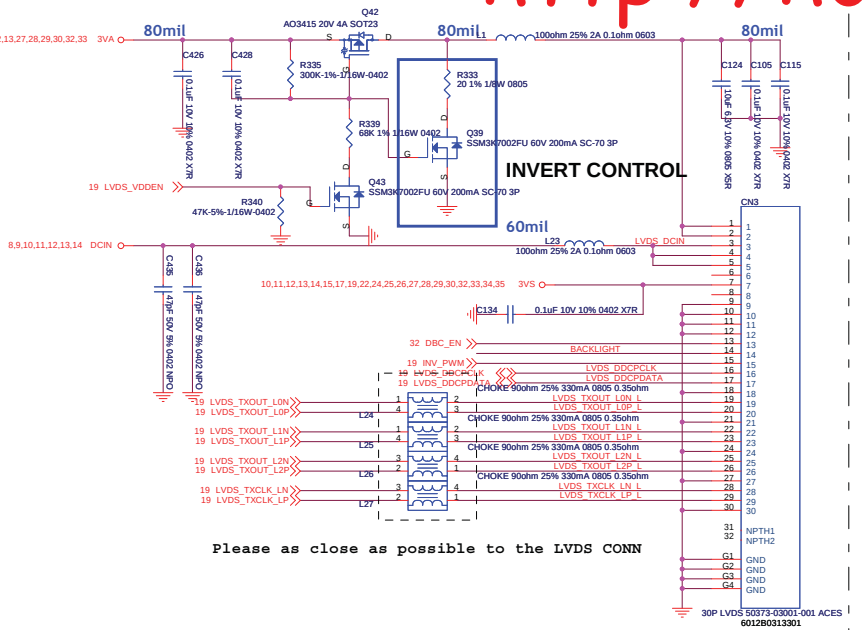
INVENTEC

TITLE
BAP31U
ICH9M Power/GND(4/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

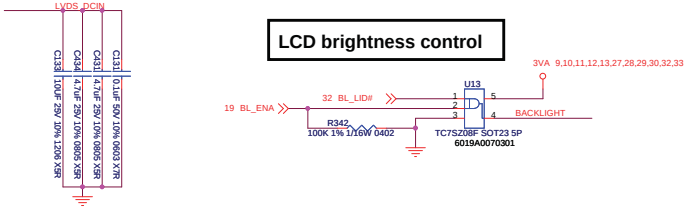
SHEET 30 of 35

LVDS Interface

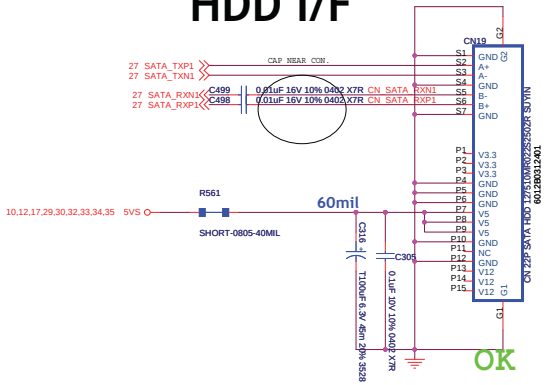


OK

LCD brightness control

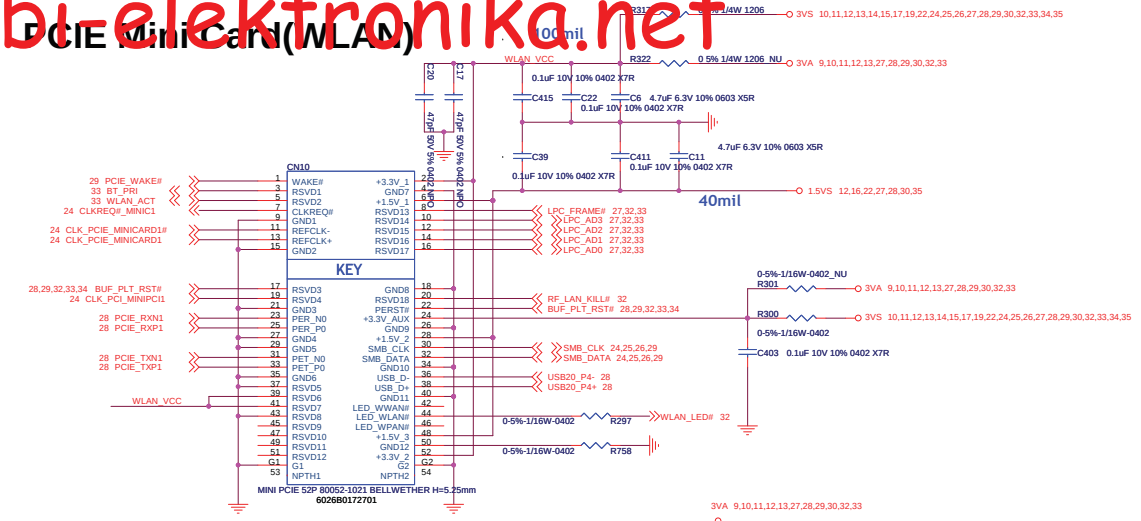


HDD I/F



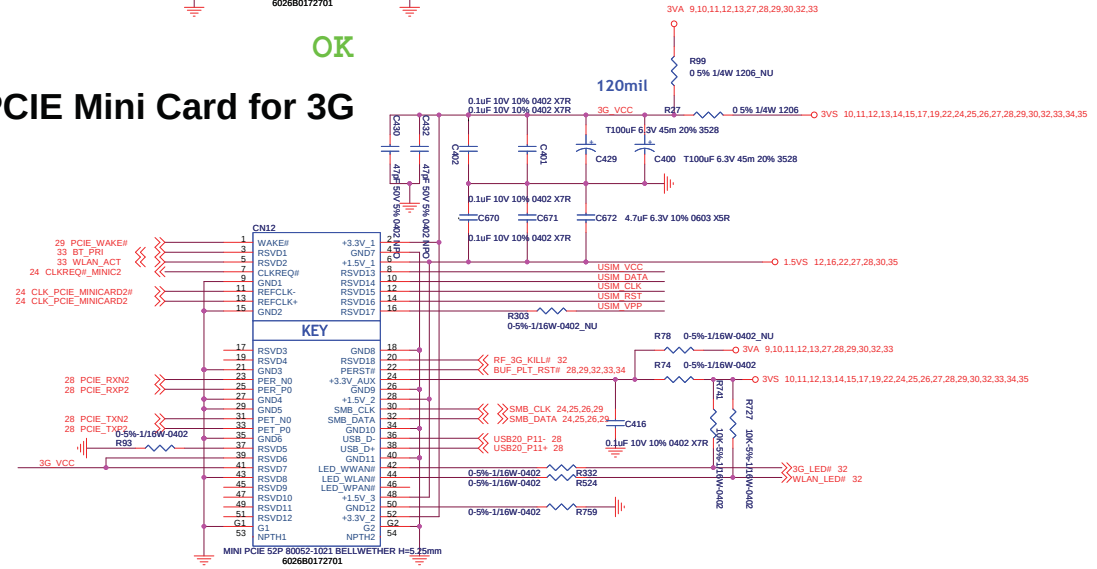
OK

PCIE Mini Card(WLAN)



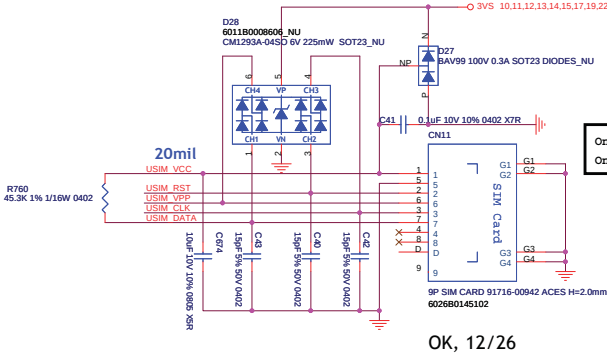
OK

PCIE Mini Card for 3G



SIM CARD slot

OK



On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.

OK, 12/26

INVENTEC			
TITLE: BAP31U			
LCD CNN & WLAN & 3G			
SIZE: Custom	CODE: AX1	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: A01
CHANGE by: Harry Chen	DATE: Wednesday, May 20, 2009	SHEET: 31 of 35	

For Green PC

IT8502E-L

SPI FLASH

To K/B(For JM31,BAP31)

SW Sensor BOARD(For JM31,SJM31)

SW (FOR JM31,BAP31) OK

SW (FOR SJM31) OK

OK

Don't place any pull-up resistor on GPG0 and GPG6

Pull down is for SPI flash

GPIO groud I are only input mode
Group I and J are not 5V tolerant
GPIO groud J are only output mode

	R239	C363
For IT8502IX	0 Ohm	NU
For IT8502JX	NU	0.1uF

CHANGE by	Harry Chen
DATE	Wednesday, May 20, 2009

INVENTEC

TITLE: BAP31U

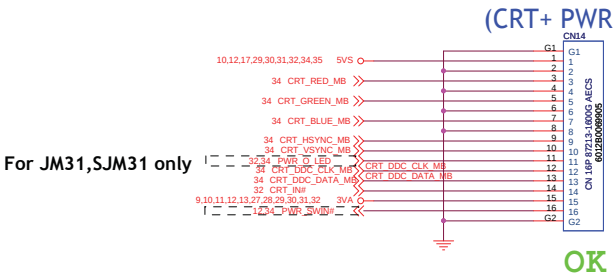
KBC ITE8512F/IO

SIZE	CODE	DOC.NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01

SHEET 32 of 35

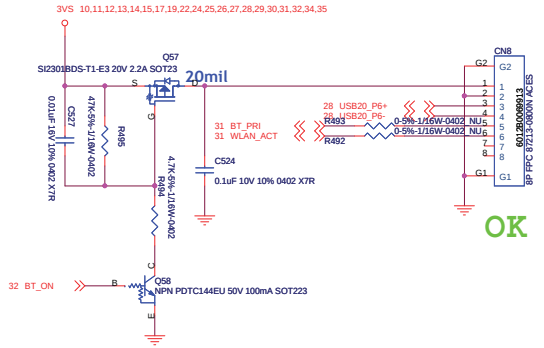
VGA Board CN

(CRT+ PWR SW)



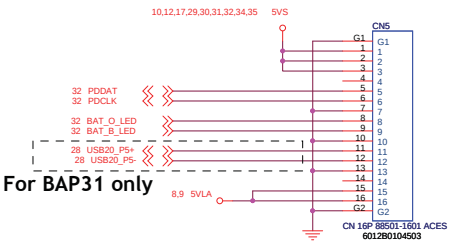
OK

Bluetooth CON.

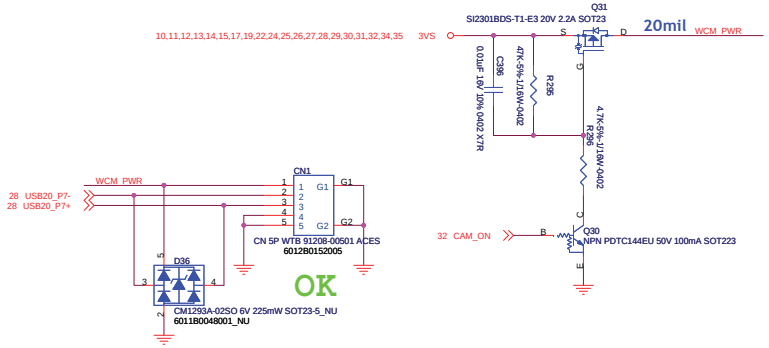


OK

MB(GP) TO GP/B

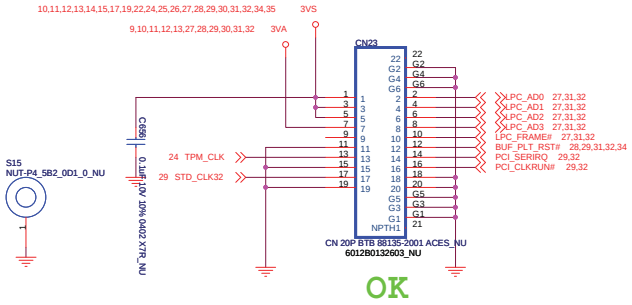


WEB Cam.



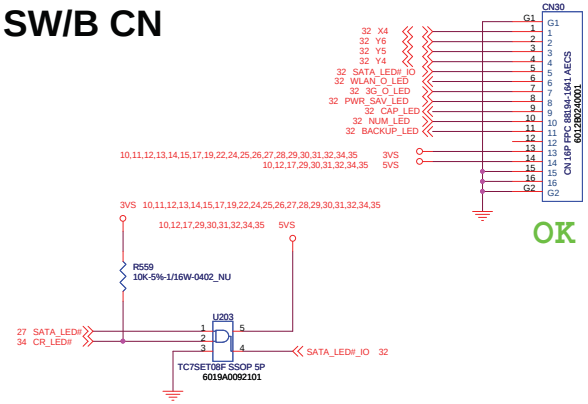
OK

TPM CN



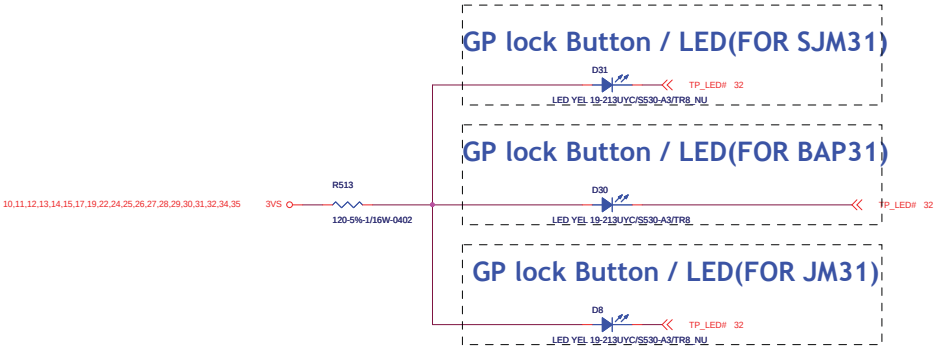
OK

SW/B CN



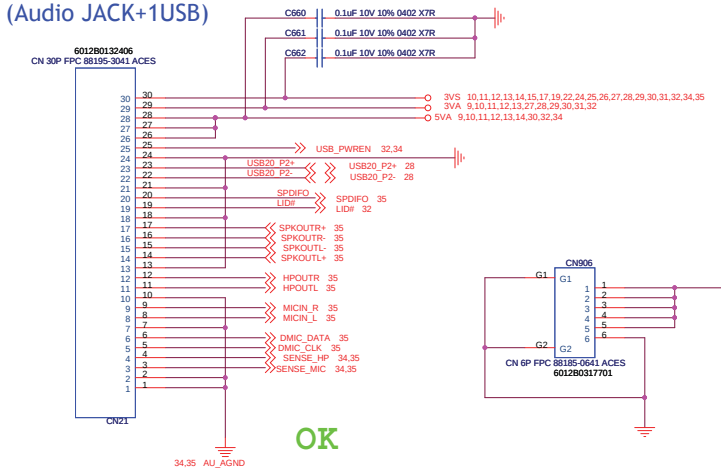
OK

GP lock Button / LED(FOR SJM31)



AUDIO Board CN

(Audio JACK+1USB)

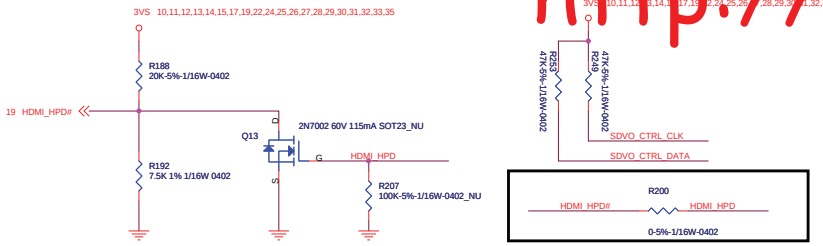


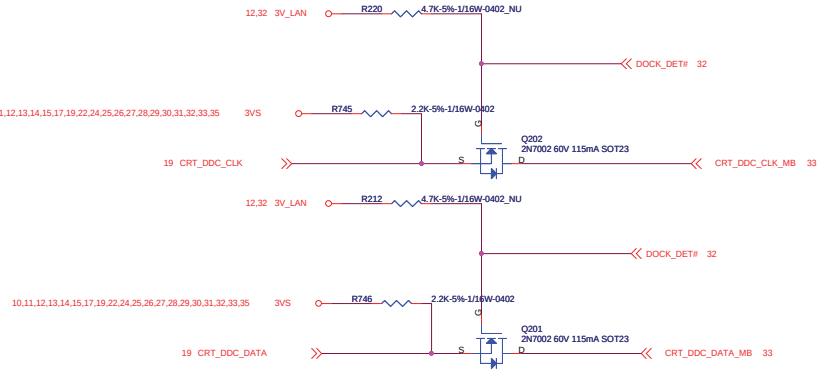
OK

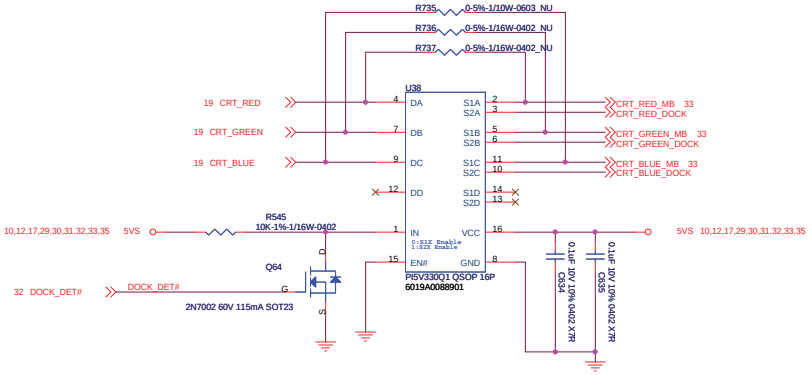
INVENTEC

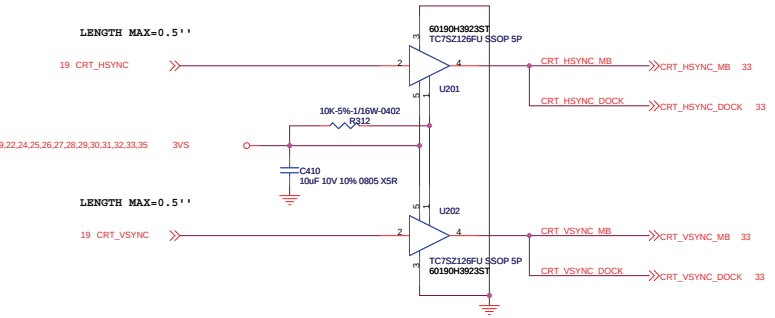
TITLE	BAP31U IO(1/2)		
SIZE	CODE	DOC NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01
CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009
		SHEET	33 of 35

For BAP31 IO/B

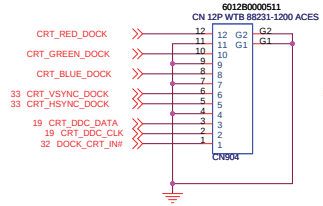




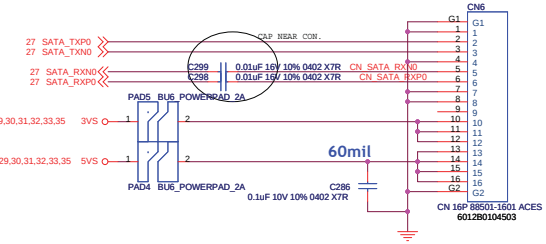




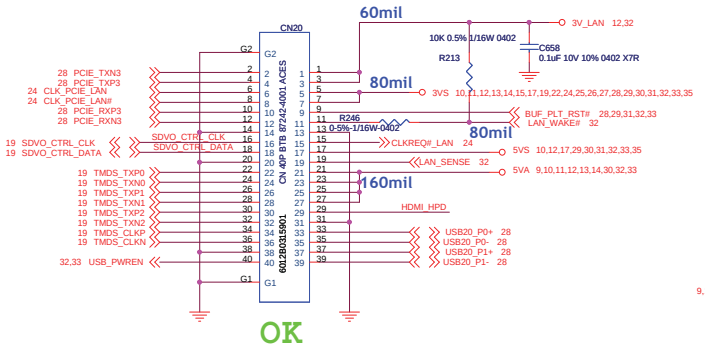
MB(RGB) TO IO/B



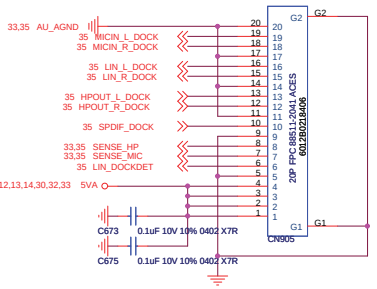
MB(SSD) TO IO/B



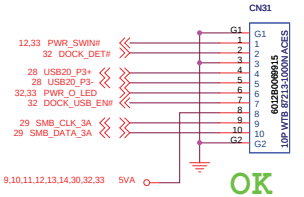
MB(LAN+HDMI+2USB) TO IO/B



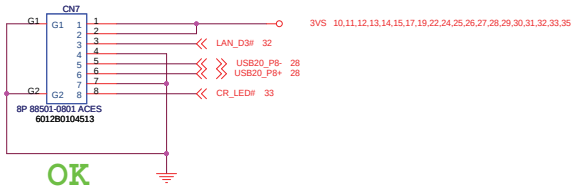
MB(AUDIO) TO IO/B



MB(USB) TO IO/B



MB(CardReader) TO IO/B

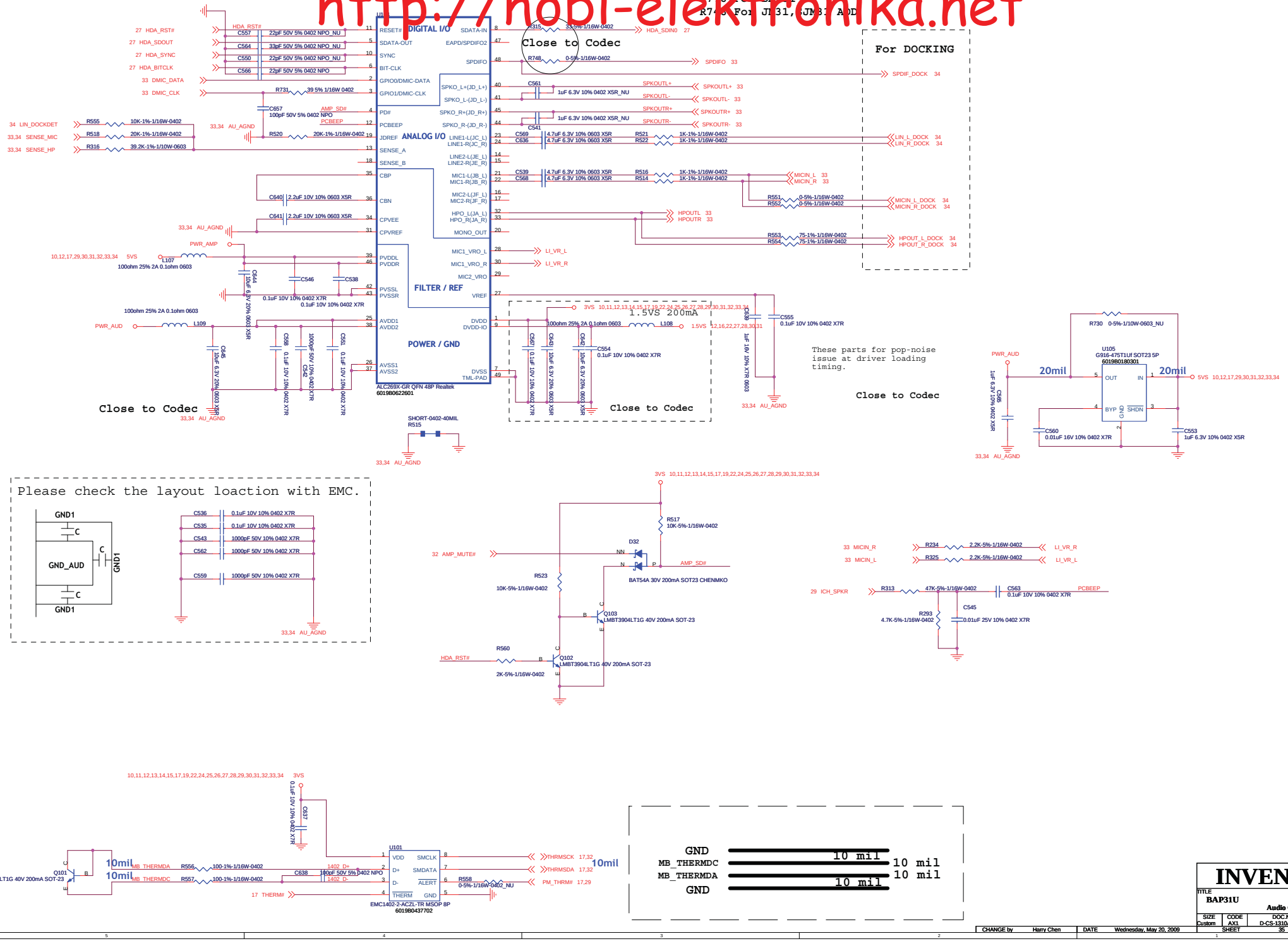


CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009		

INVENTEC

TITLE: BAP31U
IO(2/2)

SIZE	CODE	DOC NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01
		SHEET 34 of 35	



INVENTEC

TITLE	BAP31U		
	Audio Codec		
SIZE	CODE	DOC NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01
CHANGE by	Harry Chen	DATE	Wednesday, May 20, 2009
SHEET	35	of	35