HSF Property:ROHS

ACER

JM31/SJM31/BAP31 Discrete MAIN BOARD

2009.05.26

Tuesday, May 26, 2009		A03
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

INVENTEC

TITLE: BAP31G SFF

SIZE	CODE	DOC.NUMBER	REV
C	CS	D-CS-1310A2264501-ALG	A03

SHEET 1 of 47

1. Schematic Page Description :

Montevina Schematic Ver : A03

INVENTEC

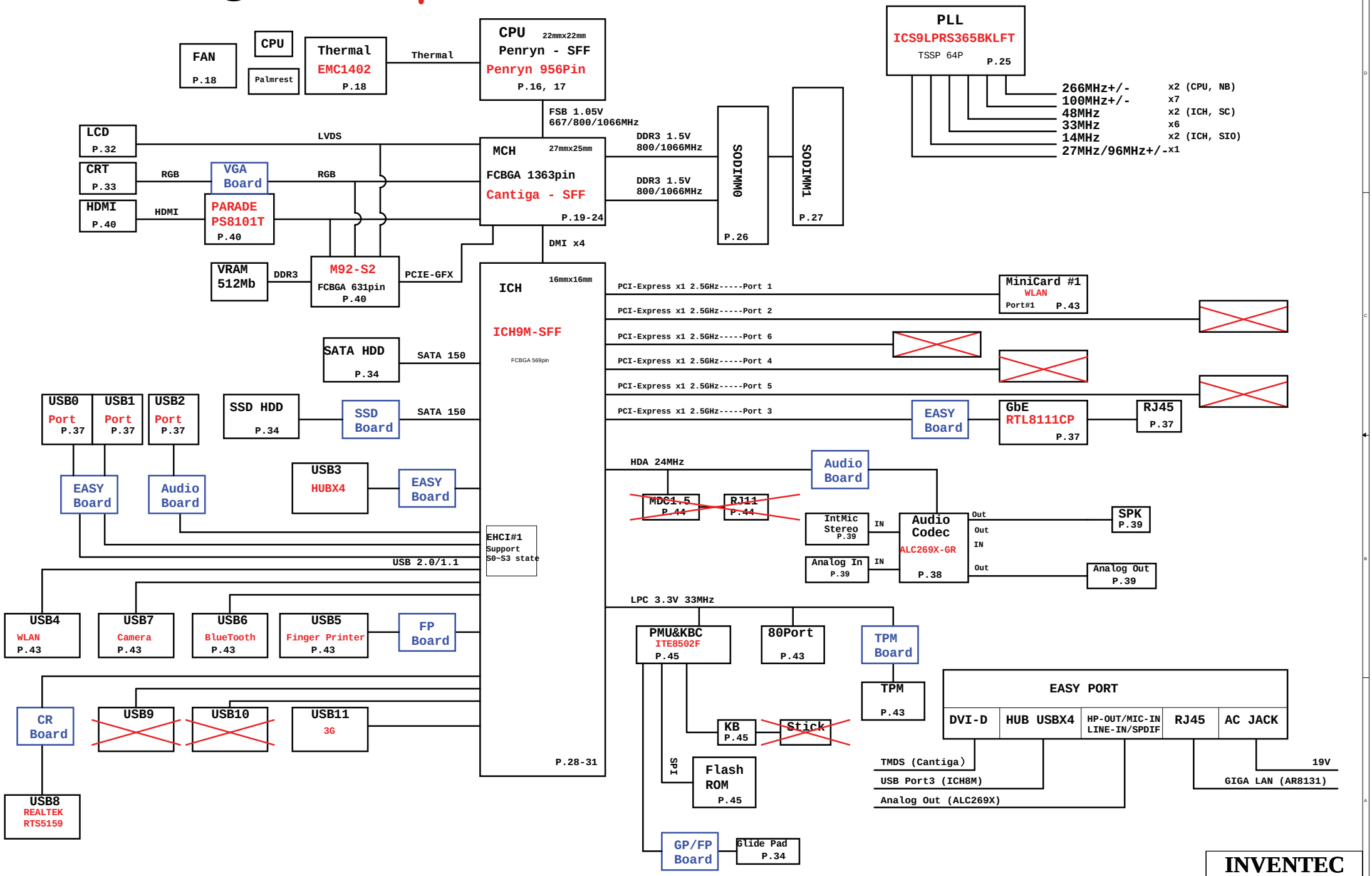
TITLE: BAP31G SFF
Schematic Page

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

SHEET 2 of 47

CHANGE by S-H Chung DATE Tuesday, May 26, 2009

3. Block Diagram :



INVENTEC

TITLE: BAP31G SFF Block Diagram			
SIZE: Custom	CODE: CS	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: A03
SHEET 3 of 47			

CHANGE by S-H Chung DATE Tuesday, May 26, 2009

4. Net name Description

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current	
VCC_CORE	Penryn SFF:	1.3319V~1.4375V~1.4591V	18A	
	LFM:	0.9221V~0.9625V~0.9739V		
1.05VS	Penryn SFF : AGTL+ termination	1V~1.05V~1.10V	4.5A	
	Cantiga GS: Core	0.997V~1.05V~1.102V	8.7A	
	Cantiga GS: PCIE	0.9975V~1.05V~1.1025V	1.78A	
	Cantiga GS:Core+IMEL+HSIO	0.9975V~1.05V~1.1025V	2.898A	
	Cantiga GS:VCC_GMCH	0.997V~1.05V~1.102V	10.154A	
	Cantiga GS:VCCA_SM_CK and NCTF	0.997V~1.05V~1.102V	37.95mA	
	Cantiga GS:VCC_DMI	0.997V~1.05V~1.102V	456mA	
	Cantiga GS:VCCA_SM	0.997V~1.05V~1.102V	747.5mA	
	Cantiga GS:VTT	0.997V~1.05V~1.102V	852mA	
	ICH9M:VCC1_05	0.997V~1.05V~1.102V	1.634A	
	ICH9M:DMI	0.997V~1.05V~1.102V	48mA	
	ICH9M:CPU_IO	0.997V~1.05V~1.102V	2mA	
1.5VS	Penryn SFF PLL	1.425V~1.5V~1.575V	130mA	
	Cantiga GS: QDAC	1.425V~1.5V~1.575V	0.5mA	
	Cantiga GS: LVDS	1.71V~1.8V~1.89V	60.31mA	
	Cantiga GS: TVDAC	1.425V~1.5V~1.575V	35mA	
	Cantiga GS: Various PLLS analog supply	1.425V~1.5V~1.575V	485mA	
	Cantiga GS: VCC_SM_CK	1.425V~1.5V~1.575V	149.5mA	
	Cantiga GS: VCC_SM	1.425V~1.5V~1.575V	3.1625A	
	ICH9M:PCIE_ICH	1.425V~1.5V~1.575V	646mA	
	ICH9M:SATA_ICH	1.425V~1.5V~1.575V	1.342A	
	ICH9M:VCC_GLAN	1.425V~1.5V~1.575V	80mA	
	Mini Card:			
	Express Card:	1.425V~1.5V~1.575V	650mA	
1.5V	Cantiga GS: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)	
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A	
3VS	Cantiga GS: HV CMOS	3.135V~3.3V~3.465V	105.3mA	
	Cantiga GS: VCCS_TVDAC	3.135V~3.3V~3.465V	78mA	
	ICH9M:VCC3_3	3.135V~3.3V~3.465V	308mA	
	ICH9M:VCCGLAN3_3	3.135V~3.3V~3.465V	1mA	
	Thermal Sensor:	3.0V~3.3V~3.6V	5mA	
	Mini Card: UMTS			
	Express Card:	3.135V~3.3V~3.465V	1.3A	
	CLK Generator: ICS9LPRS365BKLFT	3.135V~3.3V~3.465V	500mA	
	Mini Card: WirelessLan			
	Bluetooth:	3.0V~3.3V~3.6V		
	Super I/O: IT8305E			
	Azalia Codec: ALC262			
	Azalia MDC:			
1.8VS	DVI	3.0V~3.3V~3.6V	120mA	
3VA	ICH9M: RTC	2V~3.3V~3.465V	6uA	
	ICH9M:VCCSUS3_3	3.135V~3.3V~3.465V	212mA	
	ICH9M:VCCCL3_3	3.135V~3.3V~3.465V	73mA	
	ICH9M:VCCLAN3_3	3.135V~3.3V~3.465V	78mA	
	LCD:	3.0V~3.3V~3.6V	2A	
	Lan:AR8131	3.0V~3.3V~3.6V	1A	
	Azalia MDC:			
	Flash ROM: BIOS	3.0V~3.3V~3.6V		
5VS	Cardreader: RTS5159	3.0V~3.3V~3.6V		
	Azalia Codec: ALC269	3.0V~3.3V~3.6V		
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA	
	~~ODD: SATA~~	~~4.75V~5.0V~5.25V~~	~~Max: 1.5A ; R/W: 900mA ; STDBY: 45mA~~	
	~~Audio AMP: G1432~~			
	Inverter:			
	WebCam	4.75V~5.0V~5.25V	1A	
5VA	USB: x 2 ports	5VA	2A	
	USB	5VA	1.5A	
5VLA	Control Power			
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA	

INVENTEC

TITLE: BAP31G SFF

ANNOTATIONS

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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CHANGE by S-H Chung DATE Tuesday, May 26, 2009

6.Schematic modify Item and History

2009.0108

1. ADD USB P3 for Docking, USB P5 for Finger printer,
   Modify CN5 -----P28
2. Modify CN20 to 50pin-------P33
3. Move PWR_SWIN# from CN14 to CN20
4. ADD TPM module------P34

2009.0109

1. ADD DOCK_USB_EN, DOCK_CRT_IN#-----P32,33

2009.0112

1. Change power item: R490,R291,BAT CNN TH PIN

INVENTEC

TITLE: BAP31G SFF

Schematic Modify

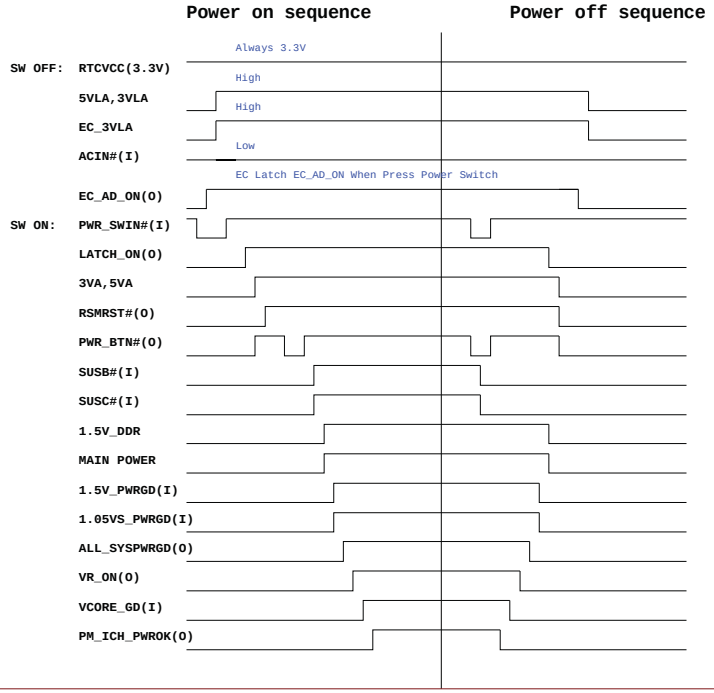
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

CHANGE by S-H Chung | DATE Tuesday, May 26, 2009 | SHEET 5 of 47

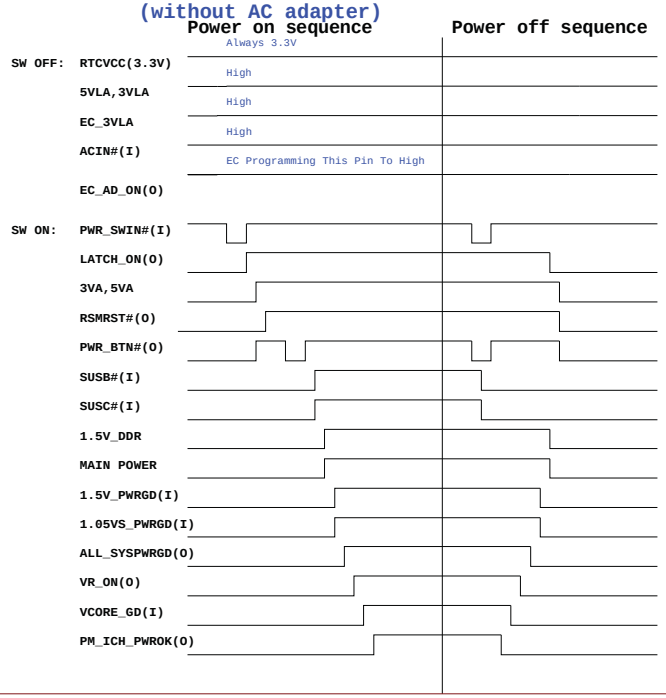
SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

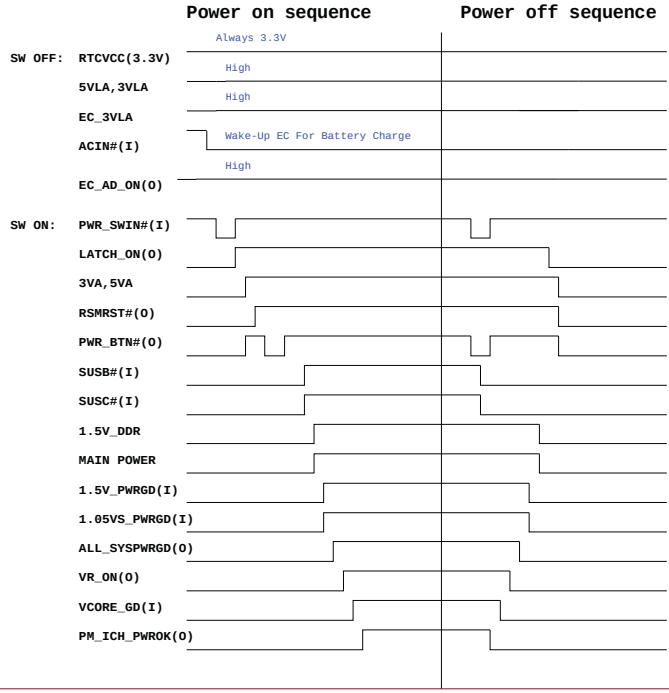
Power on/off sequence AC insert (without Battery Pack)



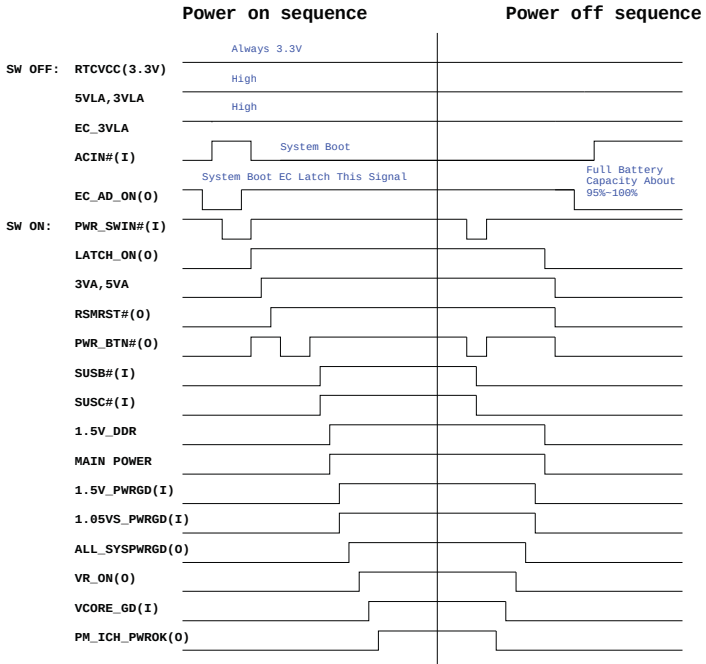
Power on/off sequence Battery insert (without AC adapter)



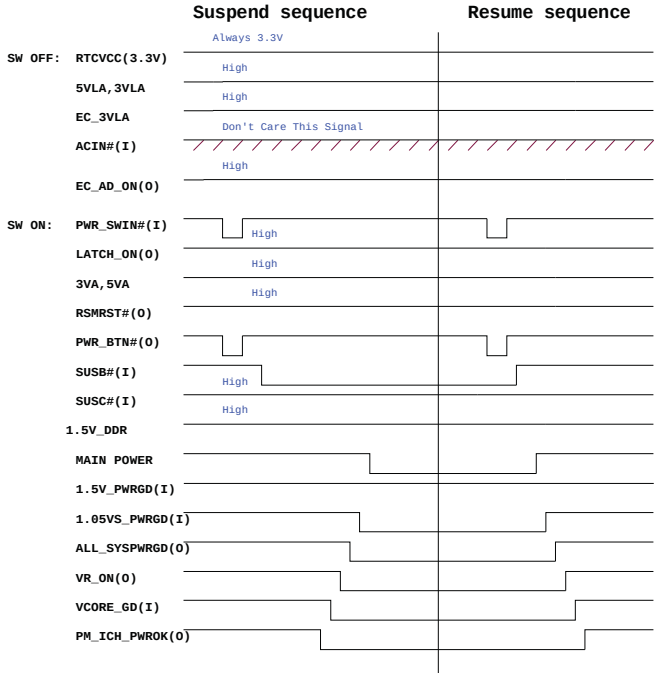
Power on/off sequence AC insert(with charge over 95%)



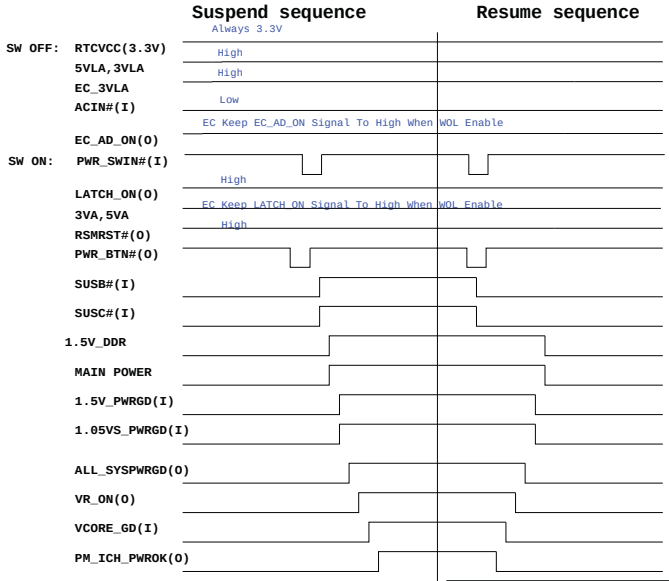
Power on/off sequence AC insert(without charge over 95%)



Suspend And Resume Sequence (S3)



Power on/off sequence after windows shoutdown (WOL enable)



INVENTEC

TITLE: BAP31G SFF
Time Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2284501-ALG	A03

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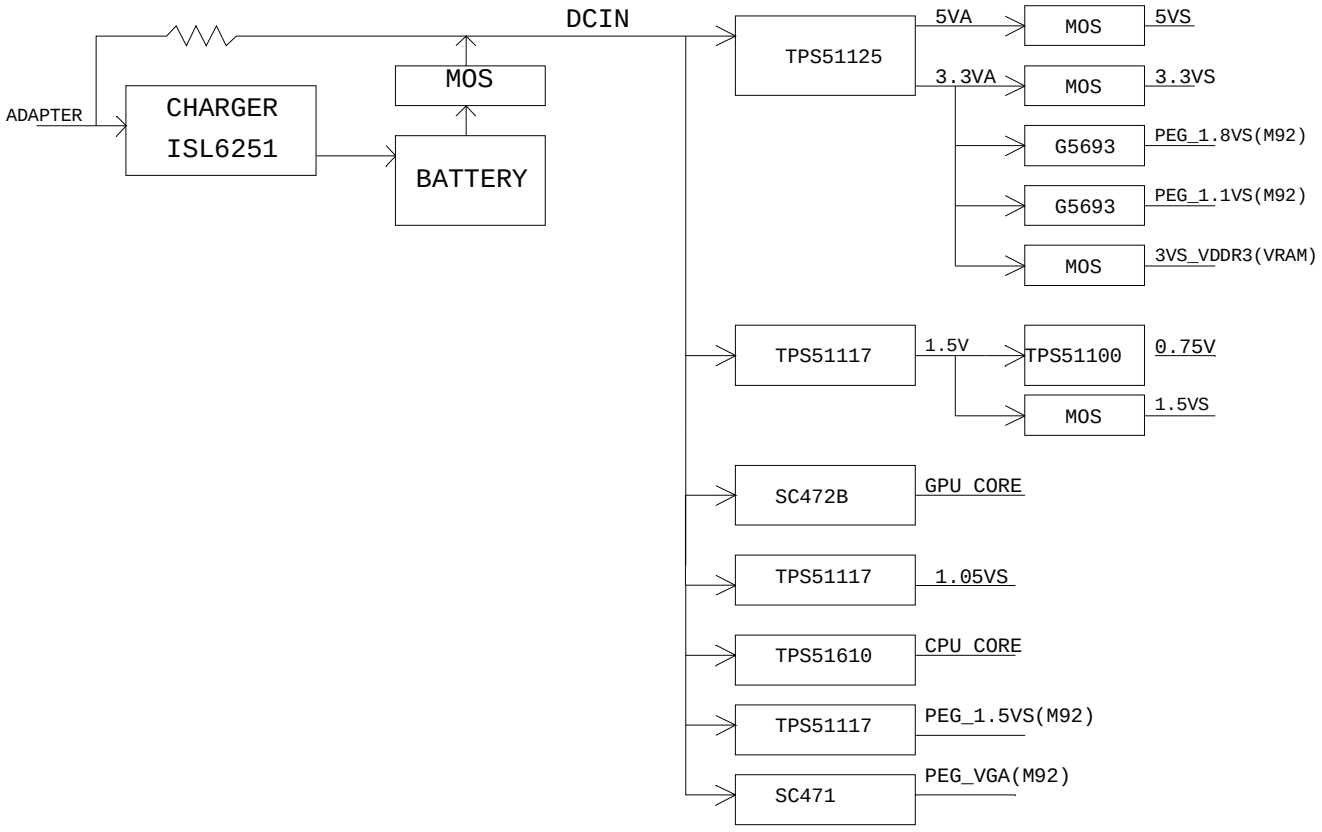
CHANGE by S-H Chung | DATE Tuesday, May 26, 2009

Power Block Diagram



CHANGE by	S-H Chung	DATE	Thursday, June 04, 2009

INVENTEC

TITLE: BAP31G SFF
Power Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	CS	D-CS-1310A2264501-ALG	A03

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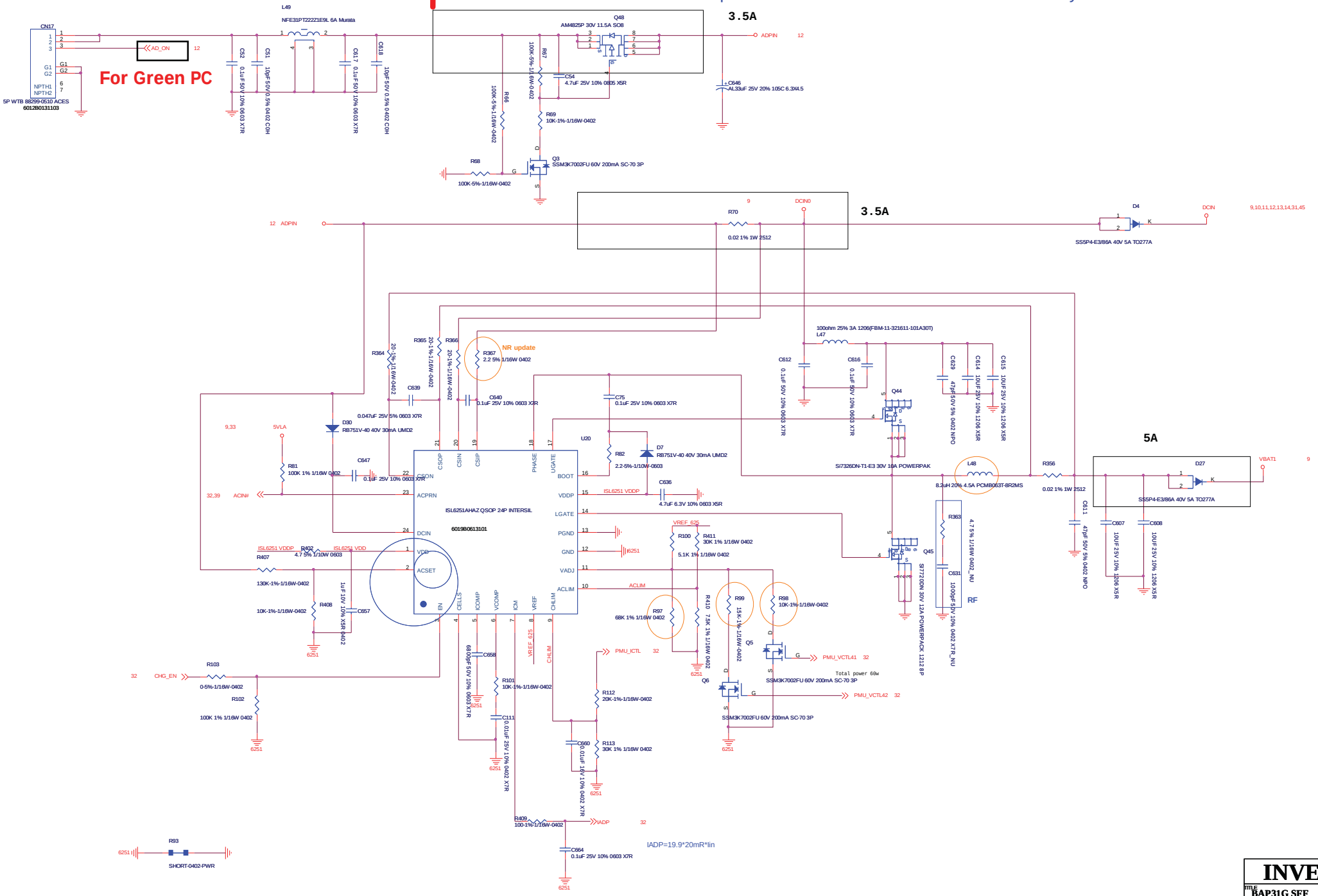
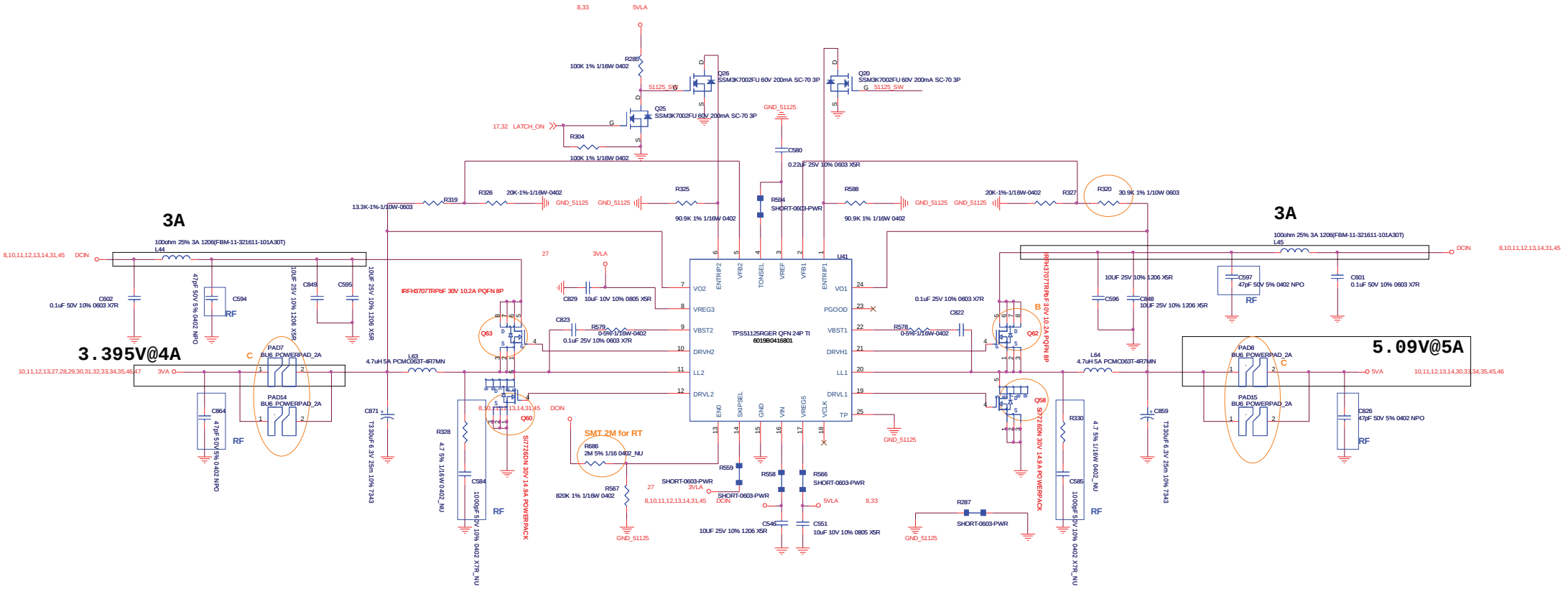
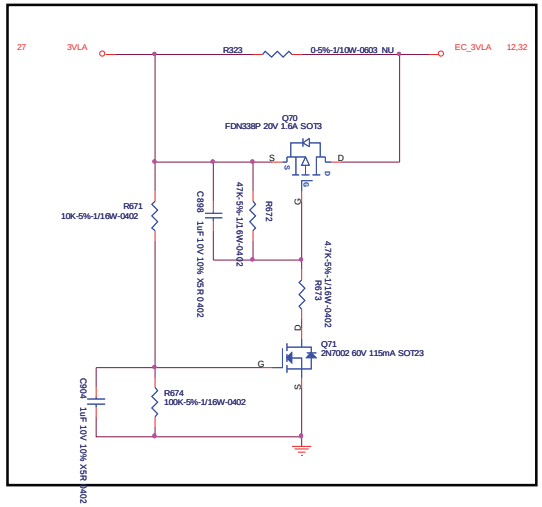
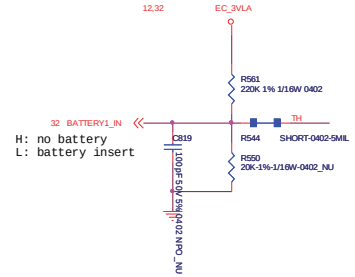


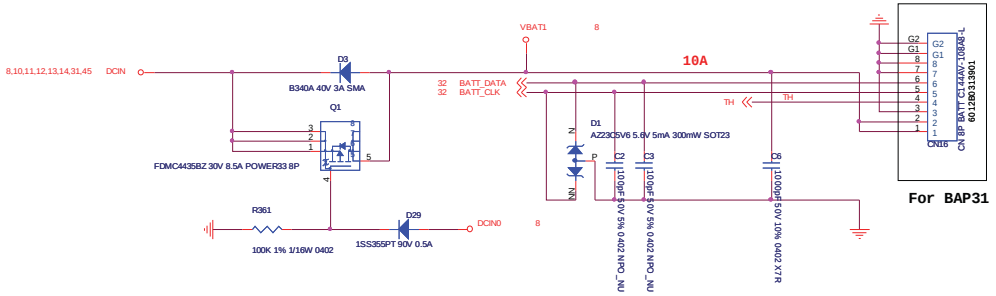


For Green PC





JM31, SJM31 USE 6012B0311301 H=4.7
BAP31 USE 6012B0313901 H=5.25



INVENTEC			
TITLE: BAP31G SFF			
5VLA/5VA/3VLA/3VA			
SIZE: Custom	CODE: CS	DOC.NUMBER: D-CS-1310A2284501-ALG	REV: A03
CHANGE by: S-H Chung	DATE: Tuesday, May 26, 2009	SHEET: 9 of 47	

2A

1.5V@8A

If voltage divide circuit OK,
U2, C30, R724 can remove
02/17

Intel Item5

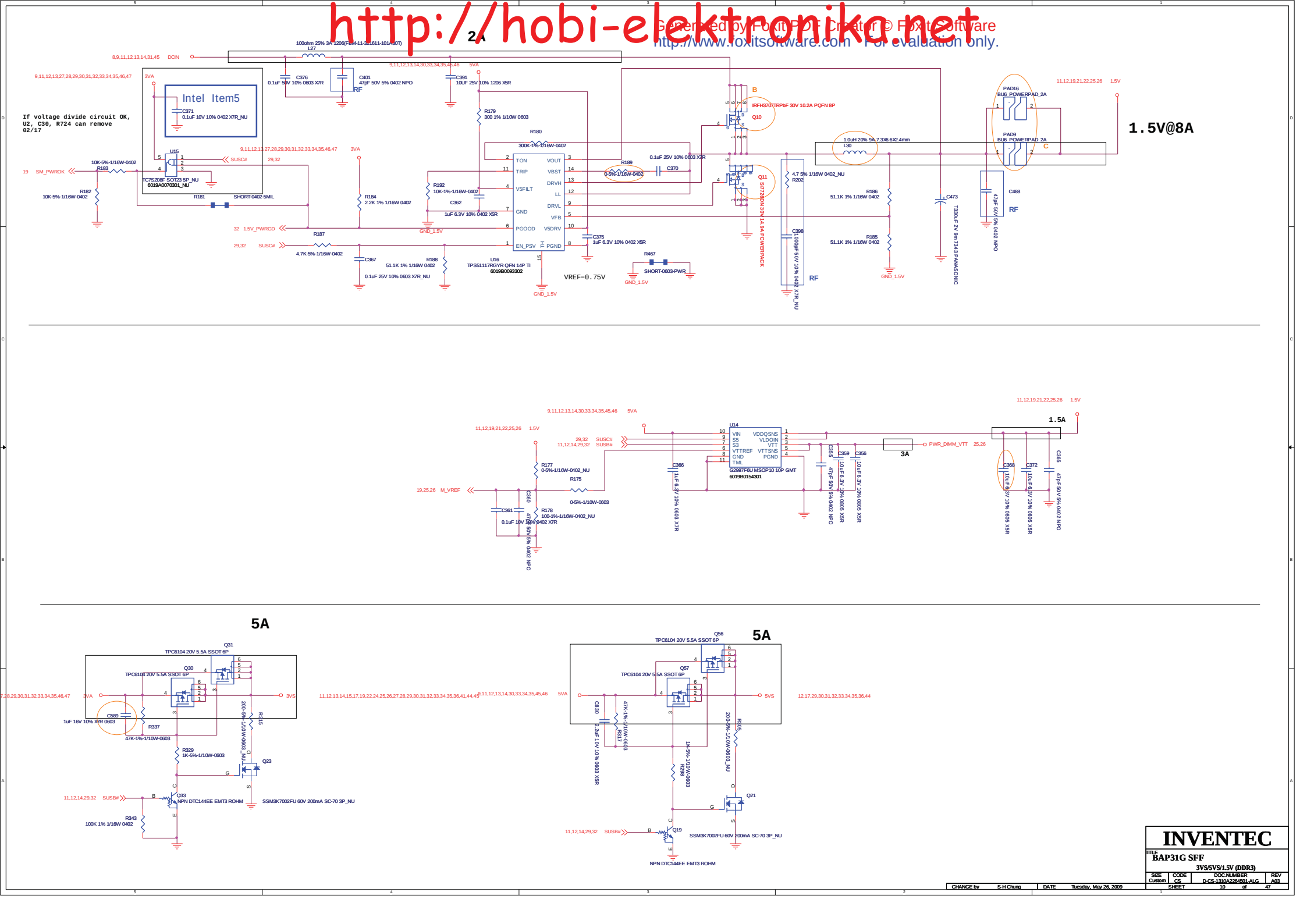
VREF=0.75V

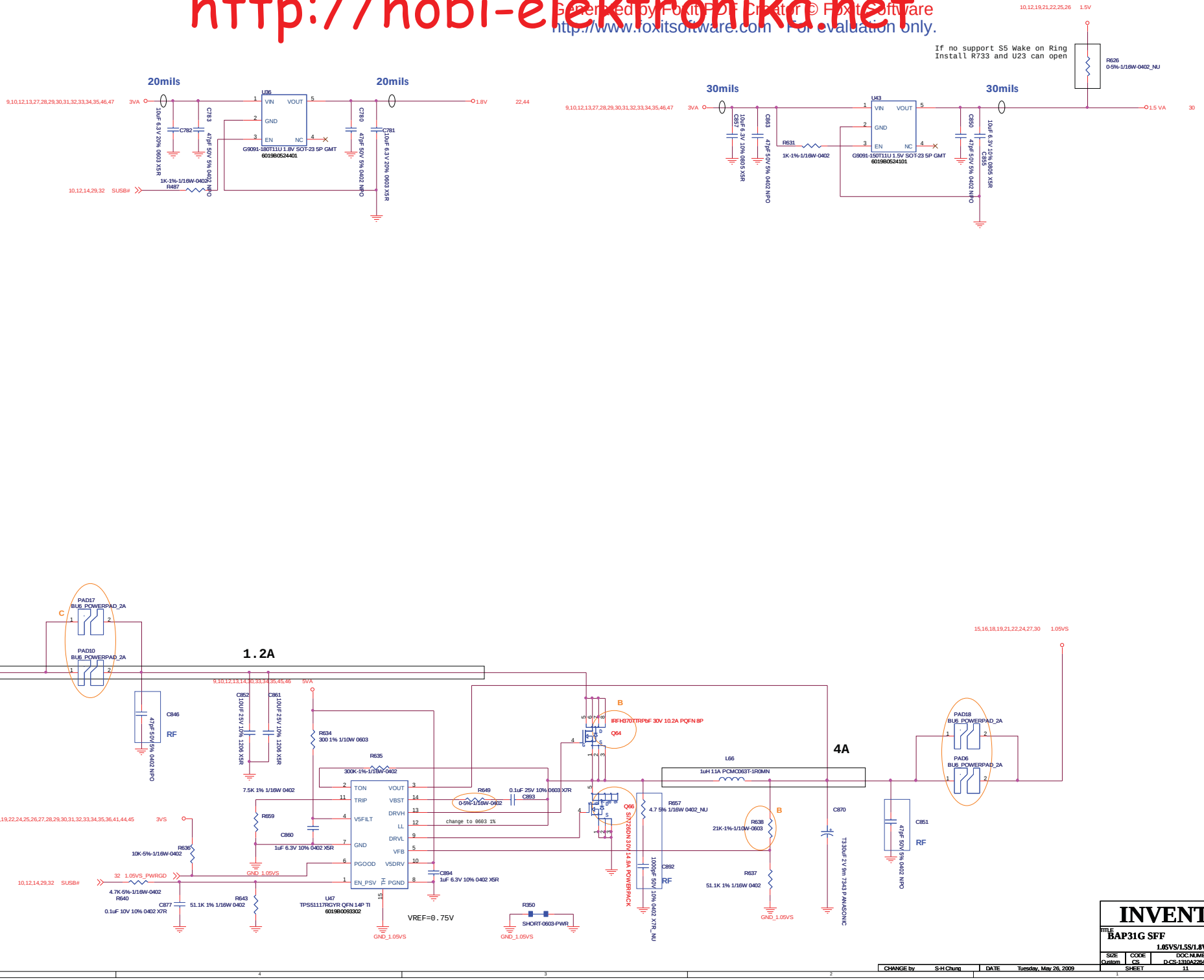
1.5A

3A

5A

5A





CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009

INVENTEC

TITLE: **BAP31G SFF**

1.05VS/1.5S/1.8V/1.5VA

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A284501-ALG	A03

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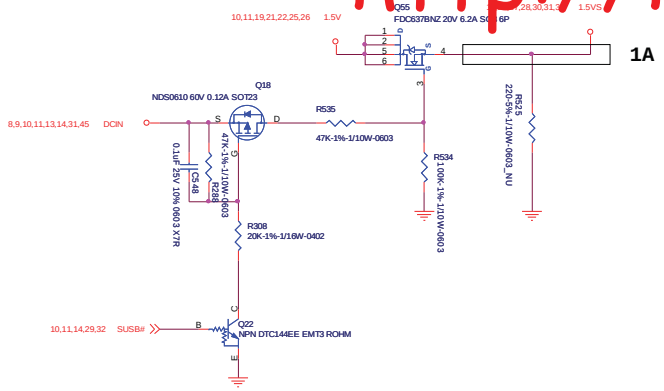
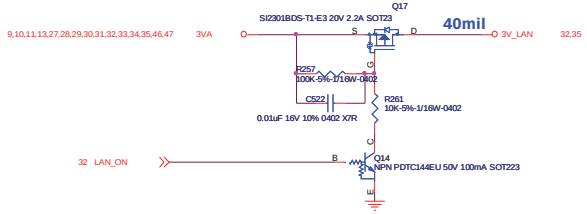
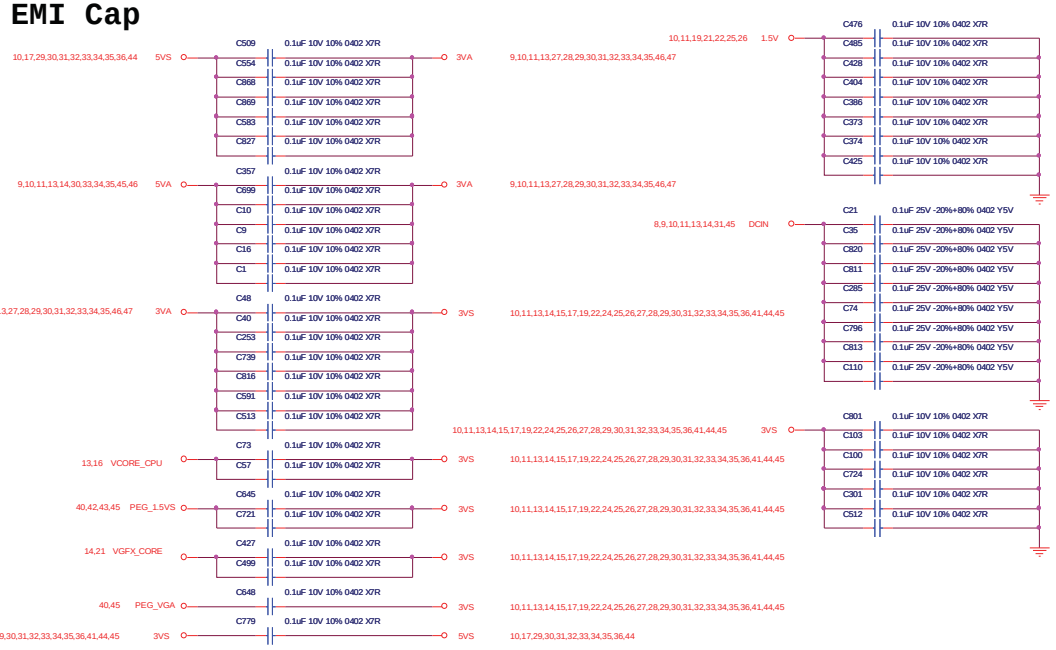
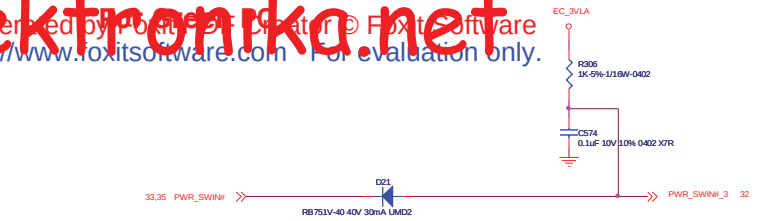
1.5VS

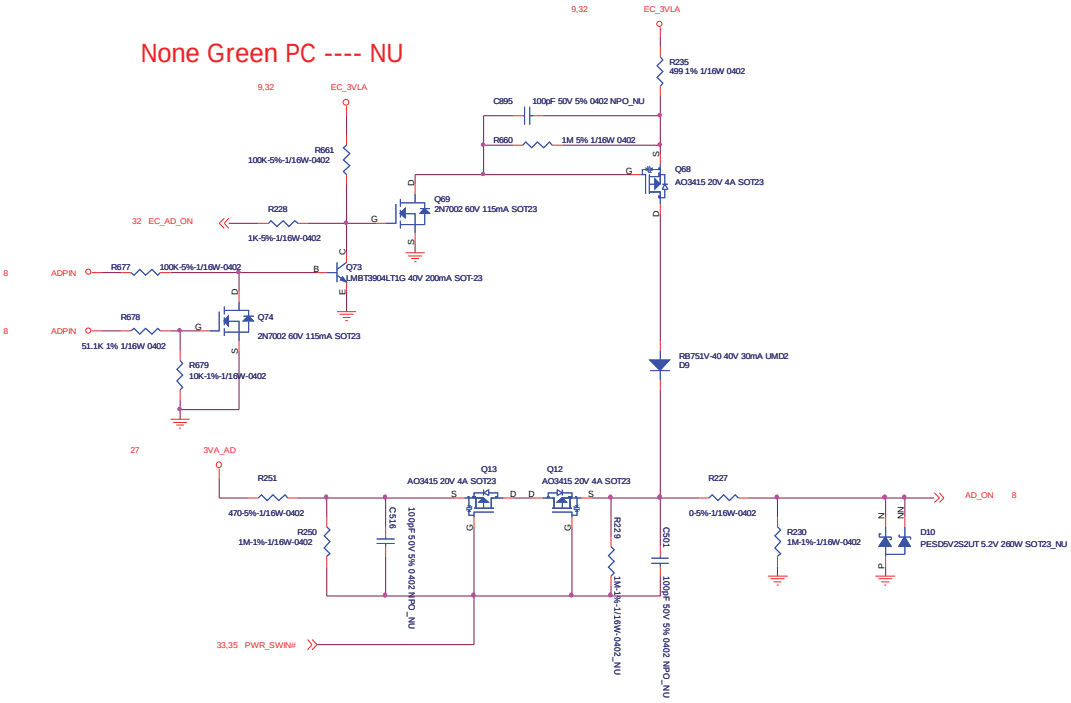


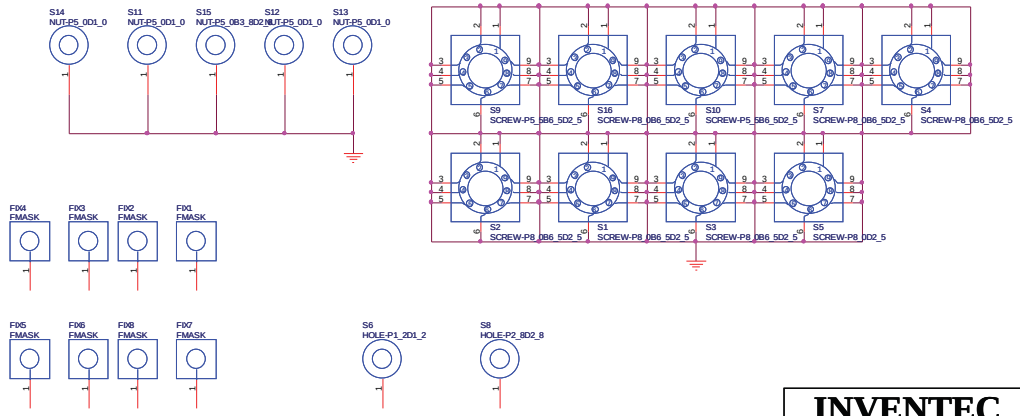


EMI Cap







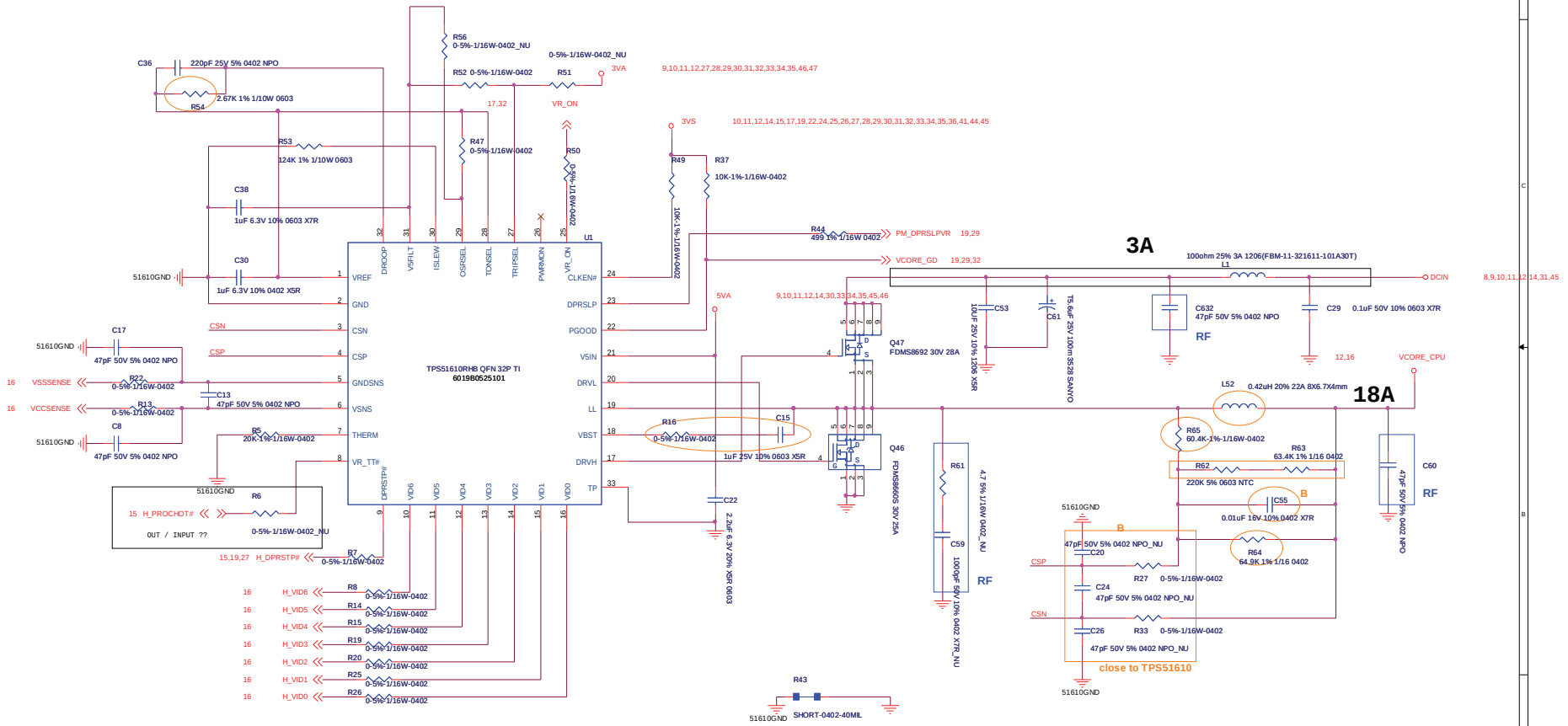


INVENTEC

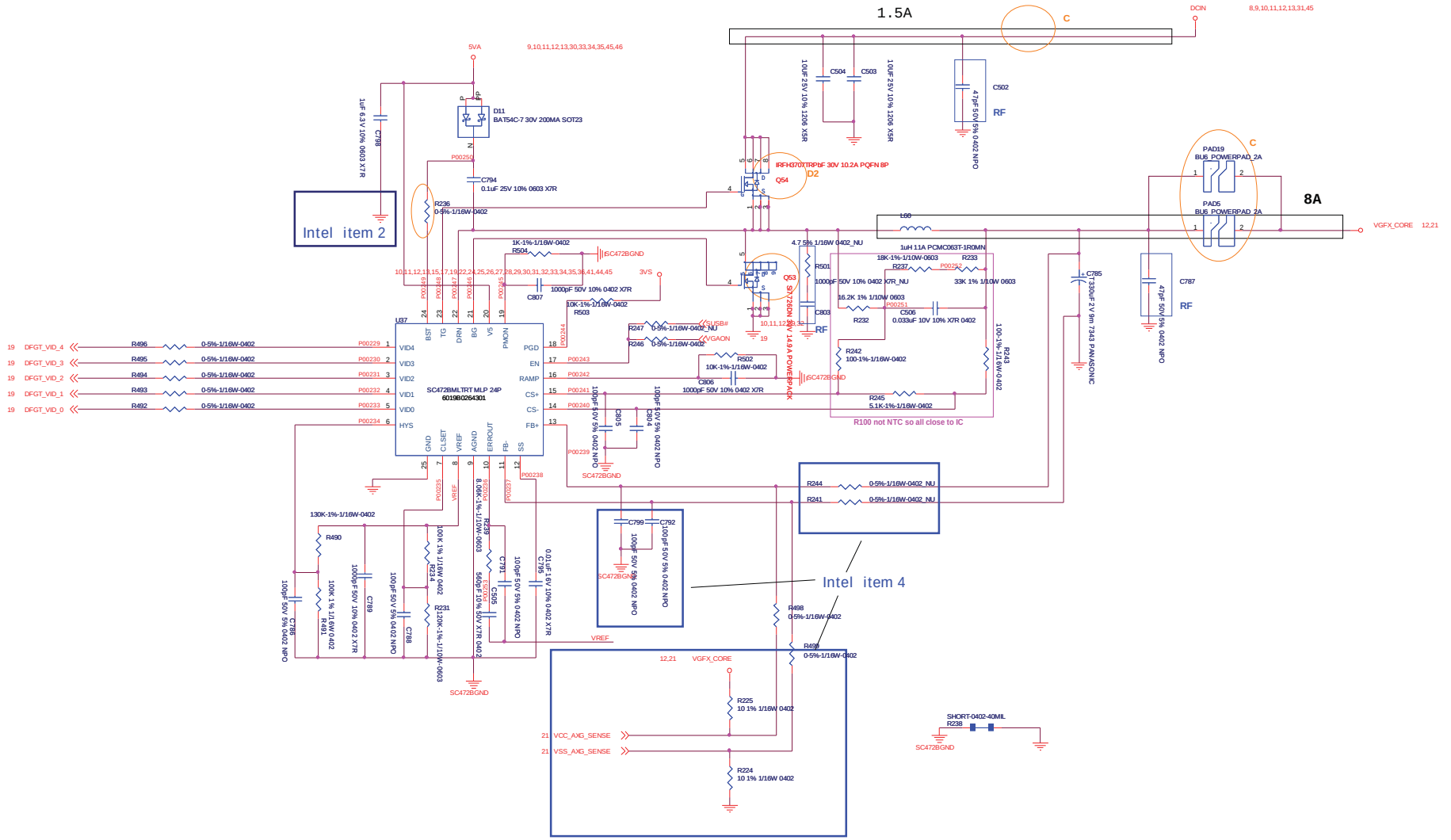
TITLE: BAP31G SFF
Power on latch

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A284501-ALG	A03

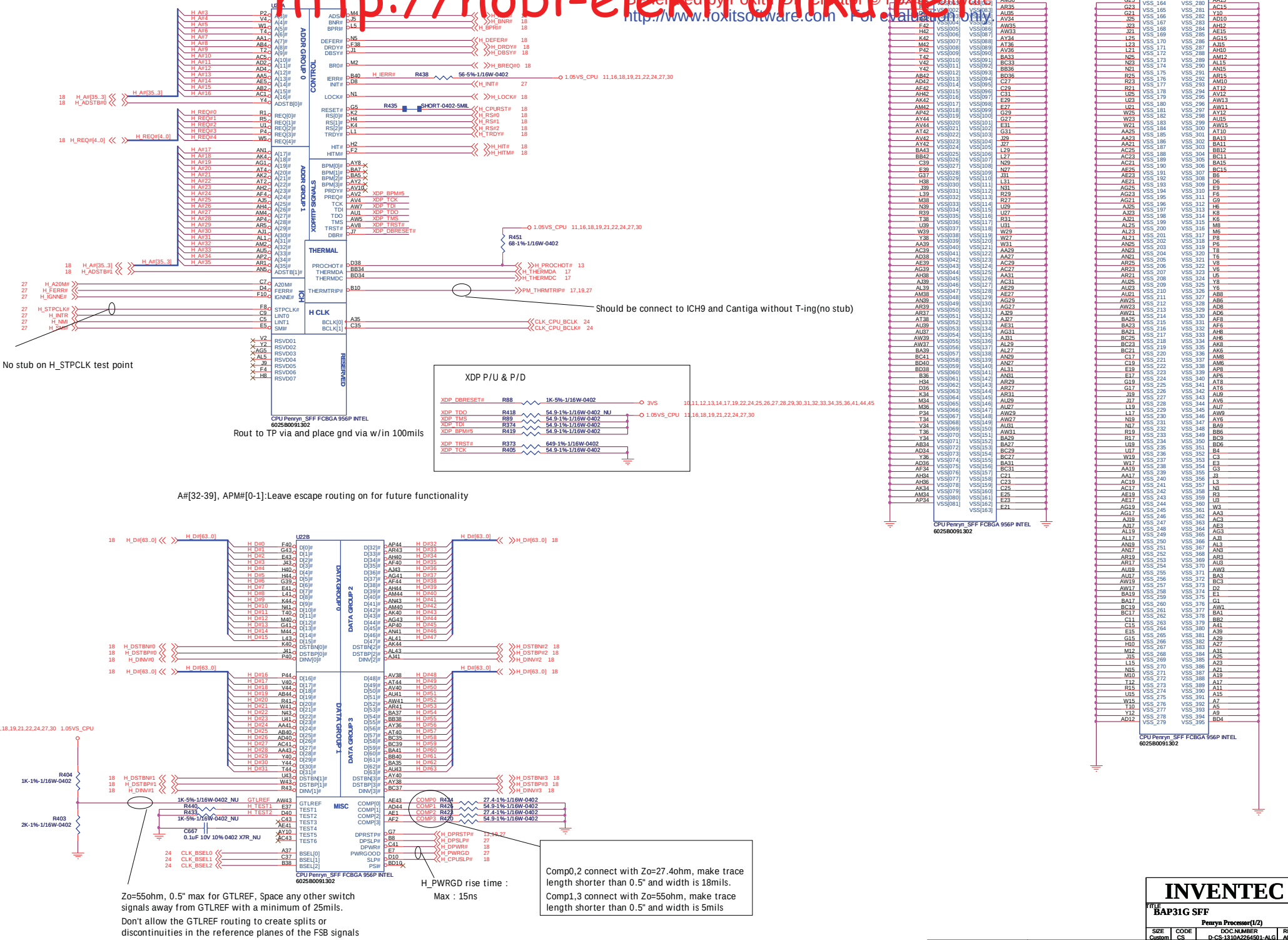
CHANGE by S-H Chung | DATE Tuesday, May 26, 2009 | SHEET 12 of 47



INVENTEC			
TITLE: BAP31G SFF CPU Core Power			
SIZE: C	CODE: CS	DOC NUMBER: D-CS-1310A2264501-ALG	REV: A03
CHANGE by: S-H Chung	DATE: Tuesday, May 26, 2009	SHEET: 13 of 47	



INVENTEC			
TITLE: BAP31G SFF			
GPU CORE			
SIZE: Custom	CODE: CS	DOC NUMBER: D-CS-1310A284501-ALG	REV: A03
CHANGE by: S-H Chung	DATE: Tuesday, May 26, 2009	SHEET: 14 of 47	



CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009

INVENTEC

TITLE: **BAP31G SFF**

Penryn Processor(1/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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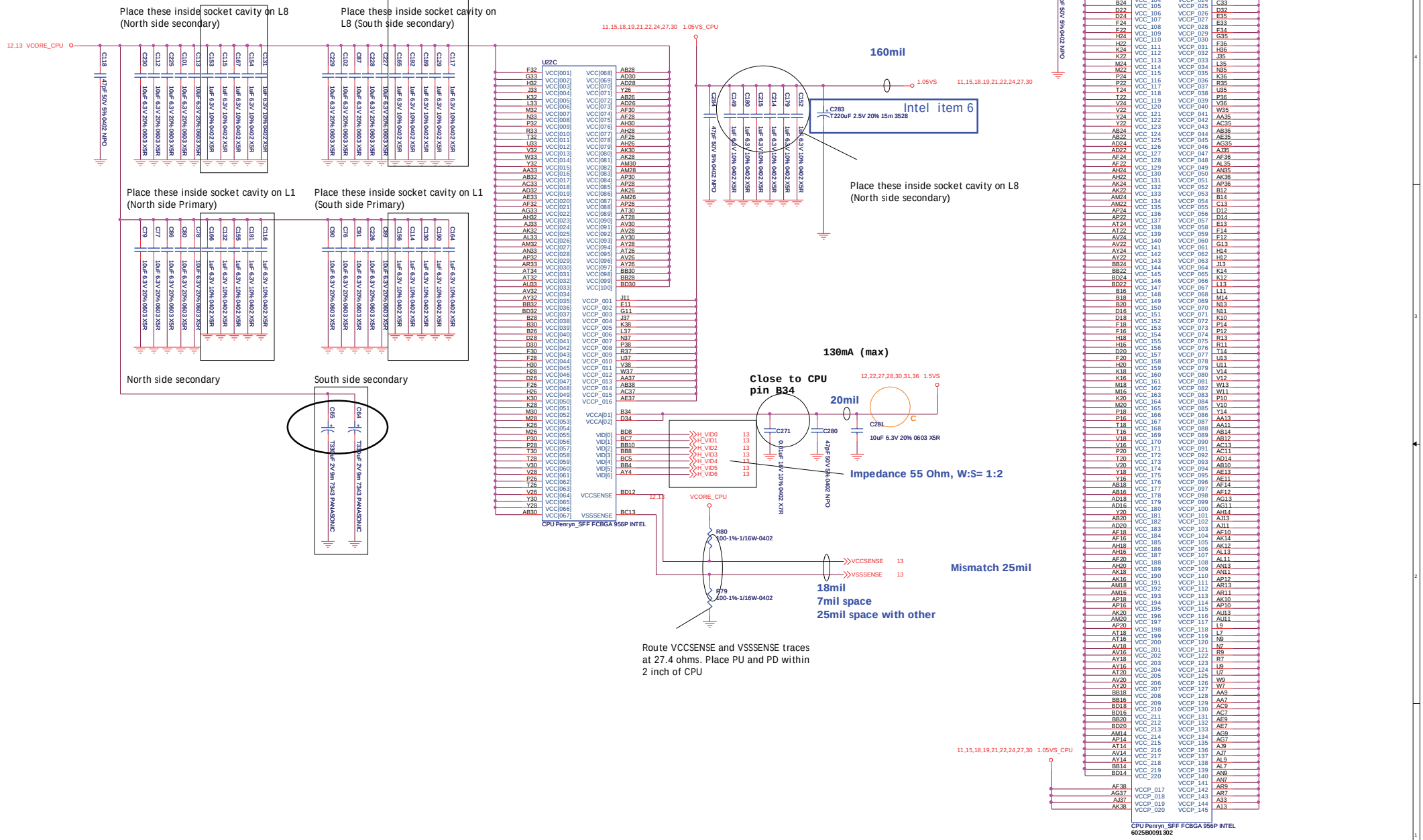
ULV Dual-Core : 18A(max)
ULV Single-Core : 9A(max)

Power-up peak current : 5A (max)
Steady-state current : 2.5A (max)



CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009

INVENTEC

TITLE: BAP31G SFF
Penryn Processor(2/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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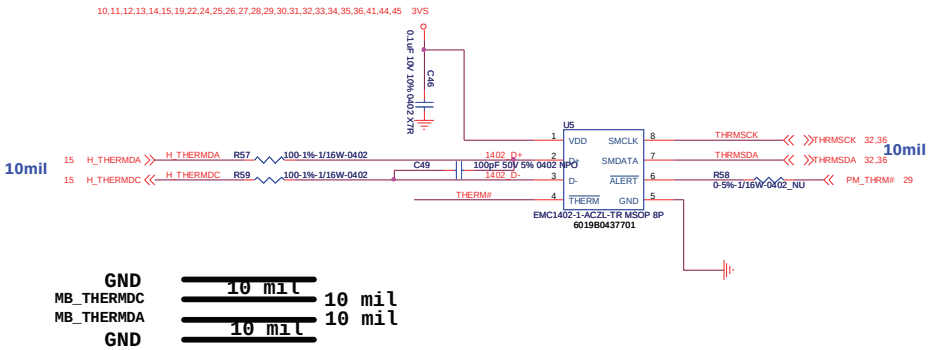
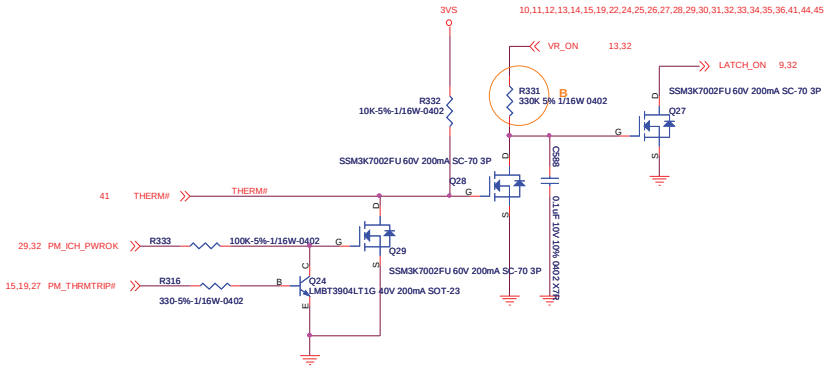
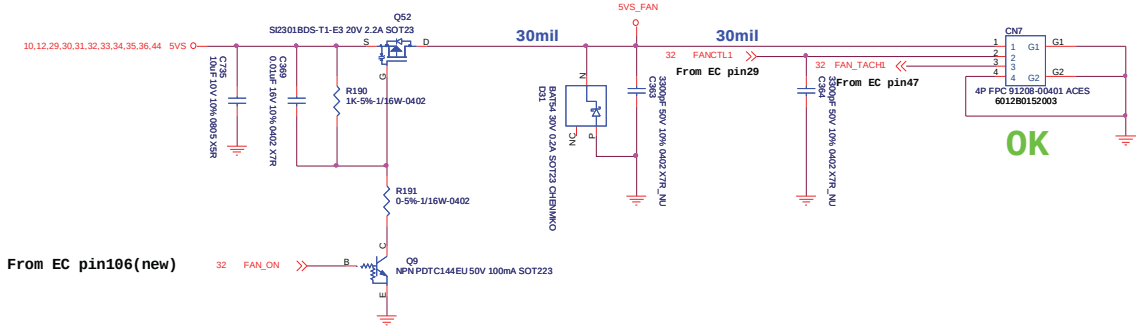
THERMAL SENSOR





Fan control



CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009

INVENTEC

TITLE: BAP31G SFF
CPU Thermal

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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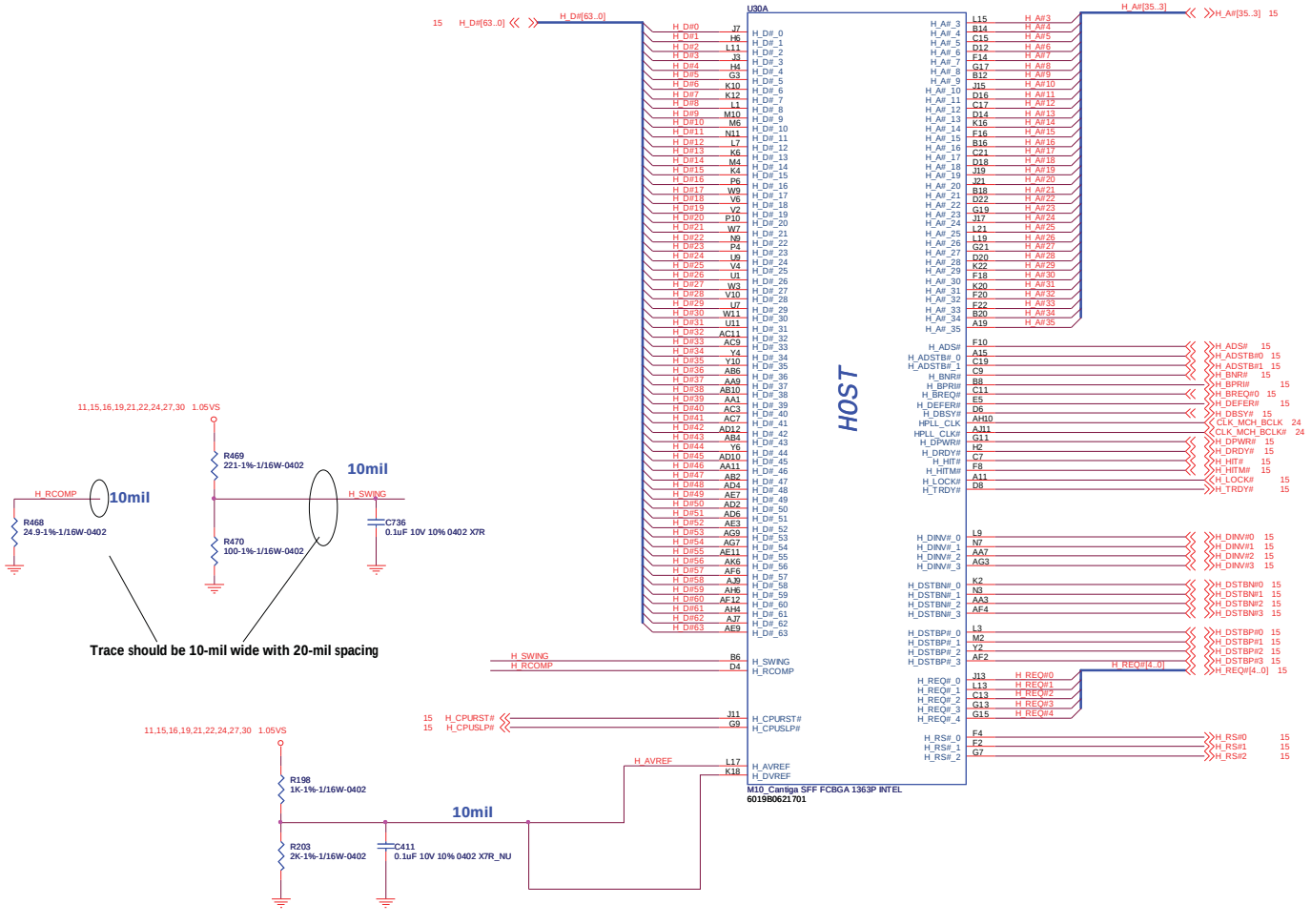
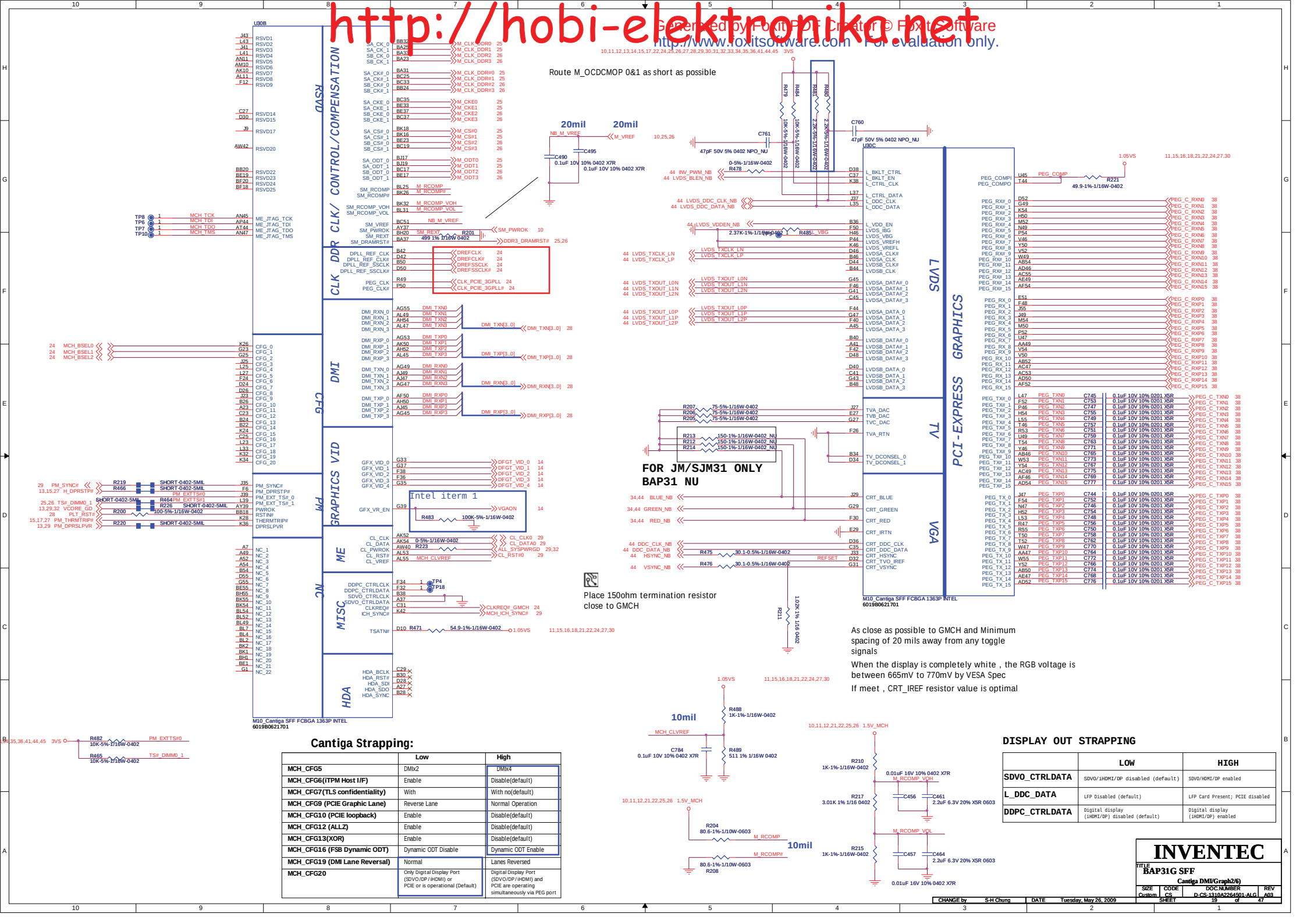


CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009		

INVENTEC

TITLE: BAP31G SFF
Cantiga Host(1/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03
SHEET	18	of	47



Cantiga Strapping:

	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG6(iTPM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIE Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIE loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only Digital Display Port (SDVO/DP /HDMI) or PCIE or is operational (Default)	Digital Display Port (SDVO/DP /HDMI) and PCIE are operating simultaneously via PEG port

DISPLAY OUT STRAPPING

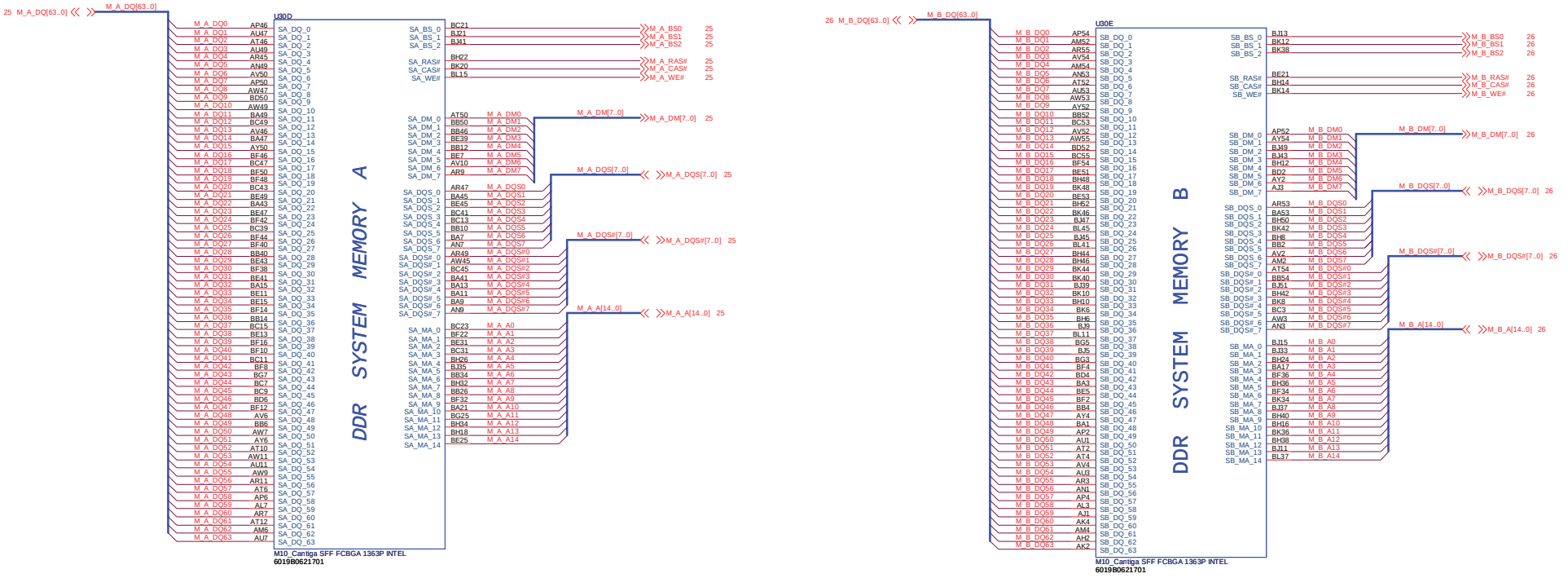
	LOW	HIGH
SDVO_CTRLDATA	SDVO/iHDMI/DP disabled (default)	SDVO/HDMI/DP enabled
L_DDC_DATA	LFP Disabled (default)	LFP Card Present; PCIE disabled
DDPC_CTRLDATA	Digital display (iHDMI/DP) disabled (default)	Digital display (iHDMI/DP) enabled

INVENTEC

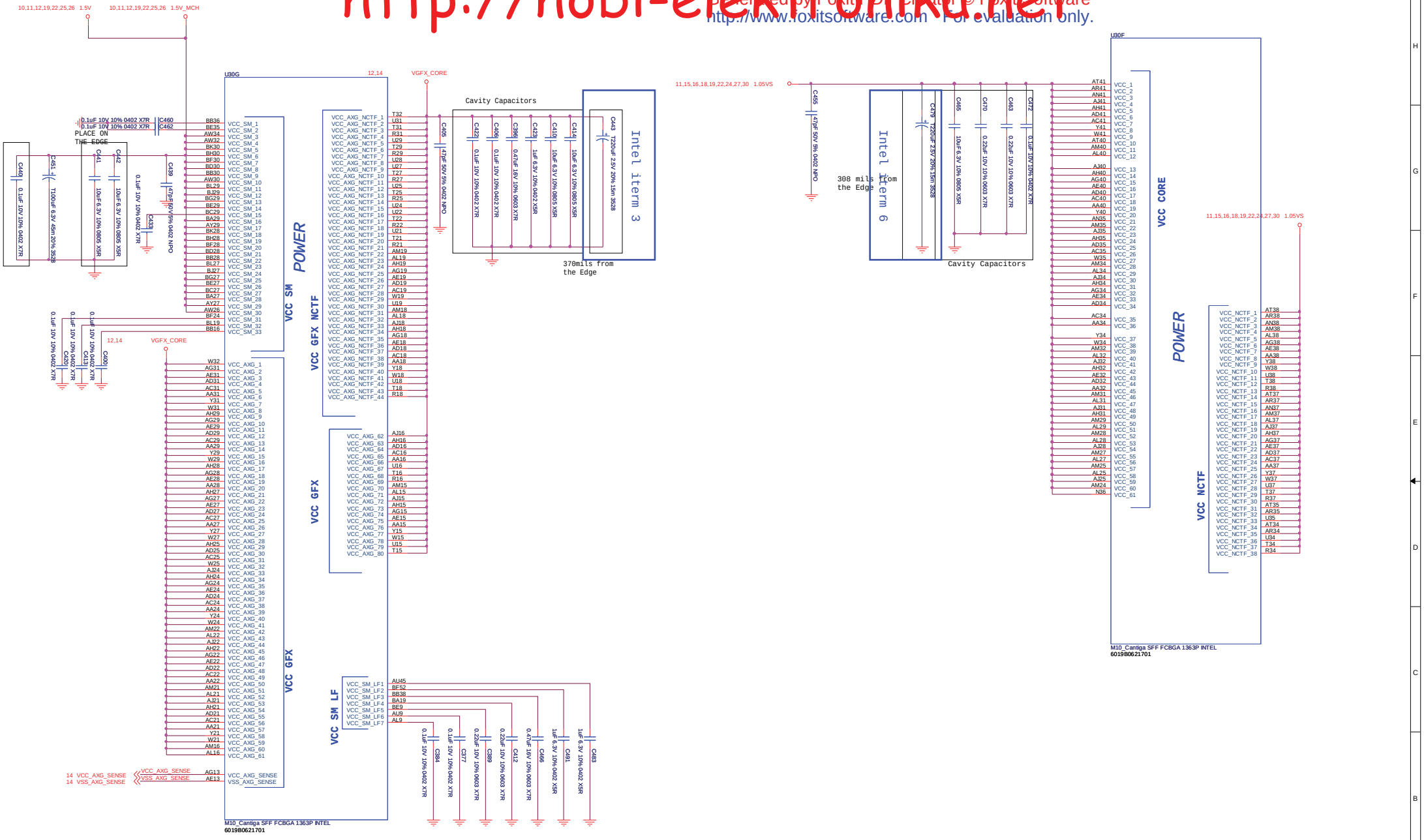
TITLE: BAP31G SFF
Cantiga DMI/Graph2/6)

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

CHANGE by S-H Chung | DATE Tuesday, May 26, 2009 | SHEET 19 of 47



INVENTEC			
TITLE: BAP31G SFF			
Cantiga DDR3(3/6)			
SIZE: Custom	CODE: CS	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: A03
CHANGE by: S-H Chung	DATE: Tuesday, May 26, 2009	SHEET: 20 of 47	



CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009	

INVENTEC

TITLE: **BAP31G SFF**

Cantiga Power(4/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils

11,15,16,18,19,21,24,27,30 1.05VS

30mil

L33 100ohm 25% 2A 0.1ohm 0603 — (64.8mA) 10mil — 1.05VS_DPLLA
C484 10uF 6.3V 10% 0805 X5R; C481 0.1uF 10V 10% 0402 X7R

L35 100ohm 25% 2A 0.1ohm 0603 — (64.8mA) 10mil — 1.05VS_DPLLB
C497 10uF 6.3V 10% 0805 X5R; C494 0.1uF 10V 10% 0402 X7R

L26 100ohm 25% 2A 0.1ohm 0603 — (24mA) 10mil — 1.05VS_HPLL
C383 4.7uF 6.3V 10% 0603 X5R; C385 0.1uF 10V 10% 0402 X7R

L58 100ohm 25% 2A 0.1ohm 0603 — (139.2mA) 10mil — 1.05VS_MPLL
C728 10uF 6.3V 10% 0805 X5R; C732 0.1uF 10V 10% 0402 X7R

L34 100ohm 25% 2A 0.1ohm 0603 — 10mil — 1.05VS_PEGPLL
C489 10uF 6.3V 10% 0805 X5R; C478 0.1uF 10V 10% 0402 X7R

12,16,27,28,30,31,36 1.5VS

0-5%-1/10W-0603 R209 — (35mA) 10mil — 1.5VS_TVDAC
C435 0.1uF 10V 10% 0402 X7R; C444 0.01uF 16V 10% 0402 X7R

L29 180ohm 25% 1.5A 0603(FBM-11-160808-181A15T) — (0.5mA) 10mil — 1.5VS_QDAC
C458 0.1uF 10V 10% 0402 X7R; C448 0.01uF 16V 10% 0402 X7R

Caps used in 1.5VDDM_TVDAC and 1.5VDDM_QTVDAC should be within 250mils of edge

3VS 10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35,36,41,44,45

0-5%-1/10W-0603 R218 — (120mA) 10mil — VCCS_TVDACA
C459 0.1uF 10V 10% 0402 X7R; C454 0.01uF 16V 10% 0402 X7R

3VDDM_TVDAC should be within 250mils of edge

Vout
R1 Vout=Vref(1+R2/R1)+Iadj*R2
R2=R1(Vout/Vref-1)
FB 1117 Vref=1.250V,Iadj=55uA
R2
GND

180ohm 25% 1.5A 0603(FBM-11-160808-181A15T) L31
10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35,36,41,44,45 3VS

(73mA) 20mil — C437 0.01uF 16V 10% 0402 X7R; C453 0.1uF 10V 10% 0402 X7R — J31 VCCA_CRT_DAC
(5mA) 20mil — C452 0.01uF 16V 10% 0402 X7R; C436 0.1uF 10V 10% 0402 X7R — L31 M33 VCCA_DAC_BG VSSA_DAC_BG

CRT

1.05VS_DPLLA J45 VCCA_DPLLA
1.05VS_DPLLB L49 VCCA_DPLLB
1.05VS_HPLL AF10 VCCA_HPLL
1.05VS_MPLL AE1 VCCA_MPLL

PLL

(10mA) — 1.8V_TXLVDS — C468 1000pF 50V 10% 0402 X7R — U43 U41 VCCA_LVDS1 VCCA_LVDS2; V44 VSSA_LVDS

A LVDS

(0.414mA) — 12,16,27,28,30,31,36 1.5VS — C475 0.1uF 10V 10% 0402 X7R — AJ43 VCCA_PEG_BG
(50mA) — 1.05VS_PEGPLL — AG43 VCCA_PEG_PLL

A PEG

(747.5mA) — 11,15,16,18,19,21,24,27,30 1.05VS
C392 10uF 6.3V 10% 0805 X5R; C394 4.7uF 6.3V 10% 0603 X5R; C418 10uF 6.3V 10% 0805 X5R; C401 1uF 6.3V 10% 0402 X5R
AW24 AU24 AW22 AU22 AU21 AW20 AU19 AW18 AU18 AW16 AU16 AT16 AR16 AU15 AT15 AR15 AW14 — VCCA_SM_1 … VCCA_SM_17

POWER

A SM

AT24 AR24 AT22 AR22 AT21 AR21 AT19 AR19 AT18 AR18 — VCCA_SM_NCTF_1 … VCCA_SM_NCTF_10

(37.95mA) — 11,15,16,18,19,21,24,27,30 1.05VS
C447 10uF 6.3V 10% 0805 X5R; C429 4.7uF 6.3V 10% 0603 X5R; C432 0.1uF 10V 10% 0402 X7R
AU27 AU28 AU29 AU31 AT31 AR31 AT29 AR29 AT28 AR28 AT27 AR27 — VCCA_SM_CK_4 … VCCA_SM_CK_NCTF_8

SM CK

(157.2mA) — 11,15,16,18,19,21,24,27,30 1.05VS — C393 0.1uF 10V 10% 0402 X7R — AH12 VCCD_HPLL
(50mA) — 1.05VS_PEGPLL — C474 0.1uF 10V 10% 0402 X7R — AE43 VCCD_PEG_PLL; M46 L45 VCCD_LVDS_1 VCCD_LVDS_2

VCCD

(30mA) — 11,44 1.8V — C480 1uF 6.3V 10% 0402 X5R

M10_Cantiga SFF FCBGA 1363P INTEL
6019B0621701

(852mA) — 11,15,16,18,19,21,24,27,30 1.05VS
C726 4.7uF 6.3V 10% 0603 X5R; C727 4.7uF 6.3V 10% 0603 X5R; C731 2.2uF 6.3V 20% X5R 0603; C733; C730 T100uF 6.3V 45m 20% 3528 -NU
PLACE ON THE EDGE

VTT

R13 T12 R11 T10 R9 T8 R7 T6 R5 T4 R3 T2 R1 — VTT_1 … VTT_13

(79mA) 10mil — K30 VCCA_TV_DAC — VCCS_TVDACA

TV

(50mA) — A31 VCC_HDA

HDA

IF use iHDMI, VCC_HDA need connnect to 1.5VS

N34 VCCD_QDAC — 1.5VS_QDAC
N32 VCCD_TVDAC — 1.5VS_TVDAC

TV/CRT

30mil (440mA) — 1uF 6.3V 10% 0402 X5R — 1.05VS — 11,15,16,18,19,21,24,27,30
C419 C424 10uF 6.3V 10% 0805 X5R_NU

30mil (149.5mA) — 0.1uF 10V 10% 0402 X7R — L28 100ohm 25% 2A 0.1ohm 0603 — 1.5V_MCH — 10,11,12,19,21,25,26
C421 C417 10uF 6.3V 10% 0805 X5R

M25 N24 M23 — VCC_AXF_1 … VCC_AXF_3

AXF

BK24 BL23 BJ23 BK22 — VCC_SM_CK_1 … VCC_SM_CK_4

(80mA) — 1.8V_TXLVDS — 10mil — 1000pF 50V 10% 0402 X7R — L32 — 1.8V — 11,44
C469 C471 120ohm 25% 200mA 0603(BLM11A121S); 22uF 6.3V 20% 0805 X5R_NU

T41 — VCC_TX_LVDS
C33 A33 — VCC_HV_1 VCC_HV_2 — 3VS_HV

HV

(1782mA) — 10uF 6.3V 10% 0805 X5R — 1.05VS — 11,15,16,18,19,21,24,27,30
C482 C492 T100uF 6.3V 45m 20% 3528

AB44 Y44 AC43 AA43 — VCC_PEG_1 … VCC_PEG_4

PEG

(456mA) 20mil — GM OPEN

AM44 AN43 AL43 — VCC_DMI_1 … VCC_DMI_3

DMI

C493 C477 0.1uF 10V 10% 0402 X7R

K14 Y12 P2 — VTTLF1 VTTLF2 VTTLF3 — VTTLF_CAP1 VTTLF_CAP2 VTTLF_CAP3

VTTLF

C734 0.47uF 16V 10% 0603 X7R; C395 0.47uF 16V 10% 0603 X7R; C409 0.47uF 16V 10% 0603 X7R; 10uF 6.3V 10% 0805 X5R

3VS 10,11,12,13,14,15,17,19,24,25,26,27,28,29,30,31,32,33,34,35,36,41,44,45

R216 10-5%-1/10W-0603 — D8 1SS355PT 90V 0.5A — 1.05VS — 11,15,16,18,19,21,24,27,30

20mil (105.3mA) — R477 SHORT-0402-15MIL — 3VS_HV — C742 0.1uF 10V 10% 0402 X7R

INVENTEC

TITLE BAP31G SFF
Cantiga Power(5/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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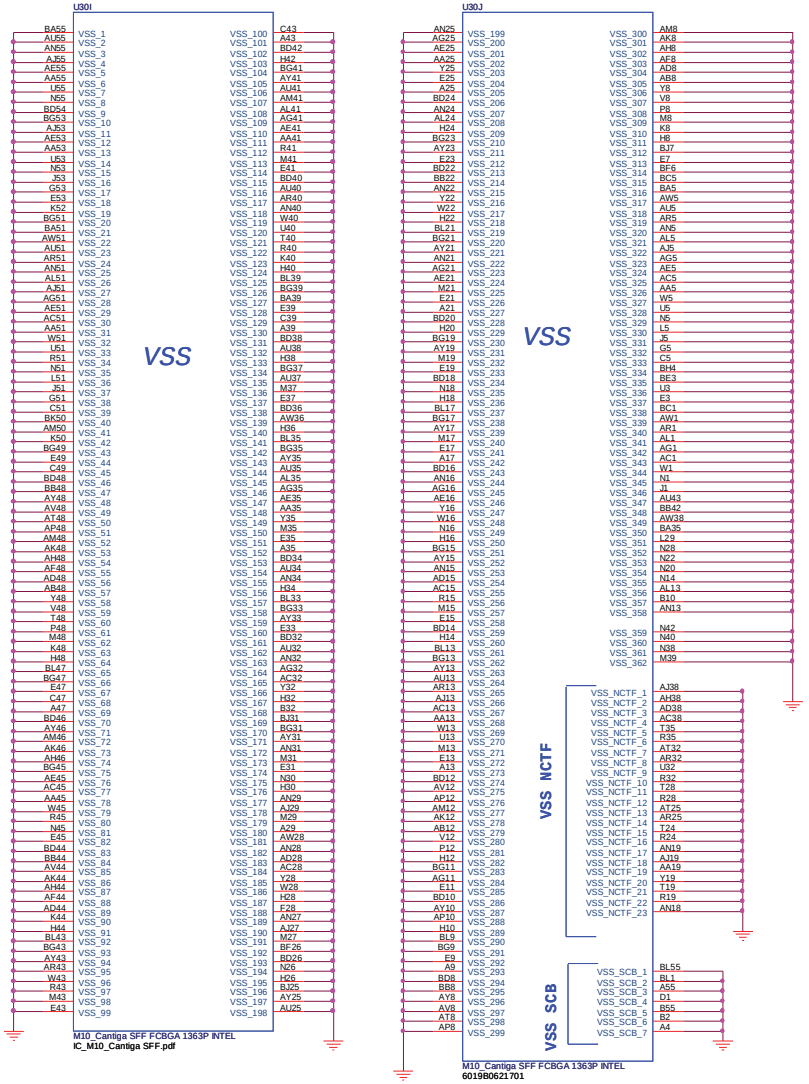
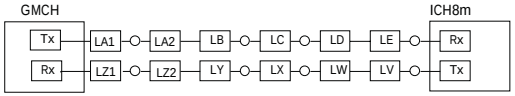
CHANGE by S-H Chung DATE Tuesday, May 26, 2009



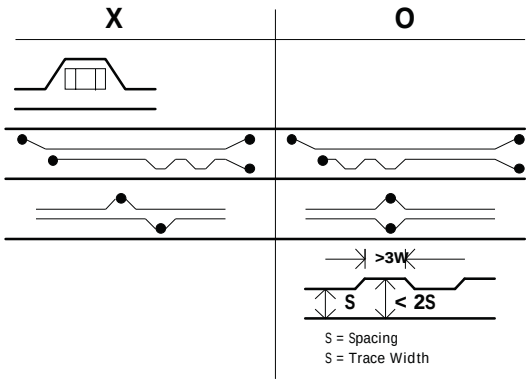
DMI Routing Guideline



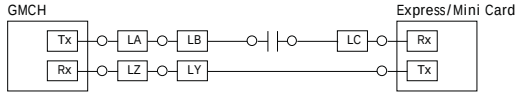
Breakout/in LA/LZ	Main Route LB/LY		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



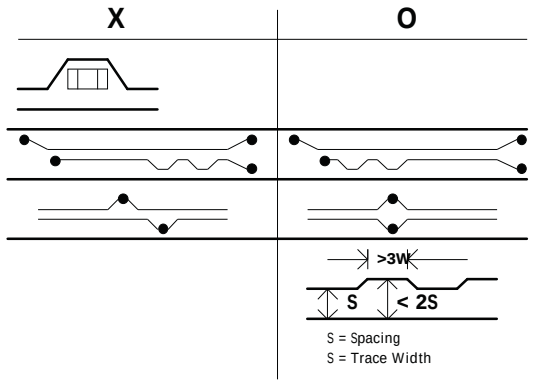
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils

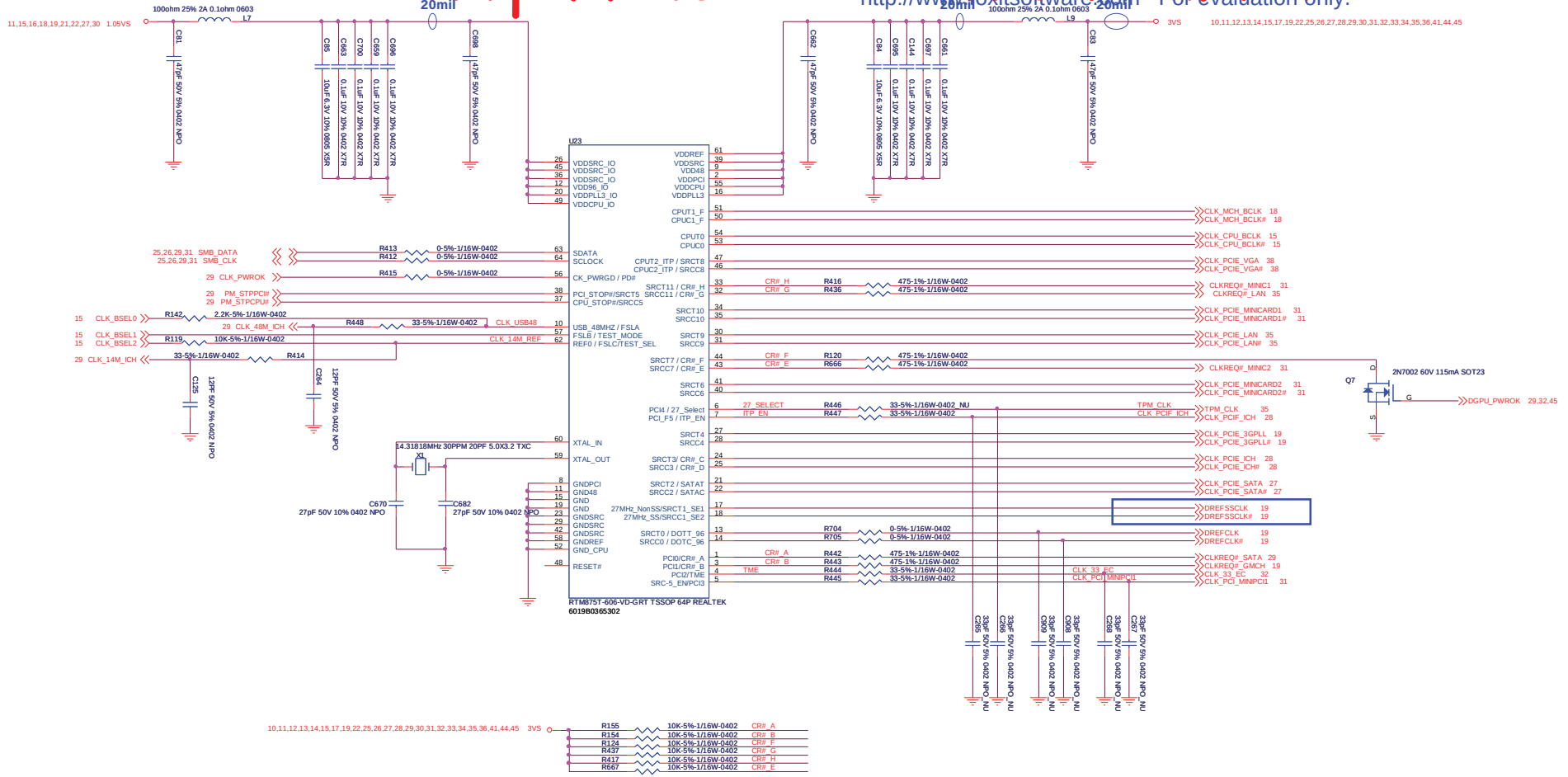


INVENTEC

TITLE: BAP31G SFF
Cantiga Ground(6/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

CHANGE by S-H Chung | DATE Tuesday, May 26, 2009 | SHEET 23 of 47



CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY	
1	1	0	667	166	
0	1	0	800	200	
0	0	0	1067	266	*

ITP_EN =0
SRC8/SRC8#
ITP_EN =1
ITP/ITP#

27_SELECT =0
Dot96/ LCD_SS /SE
27_SELECT =1
SRC8/ 27MHz

By Tony

INVENTEC	
TITLE	BAP31G SFF
	Clock Generator
SIZE: Custom	CODE: CS
DOC.NUMBER	D-CS-1310A2264501-ALG
REV	A03
CHANGE by	S-H Chung
DATE	Tuesday, May 26, 2009
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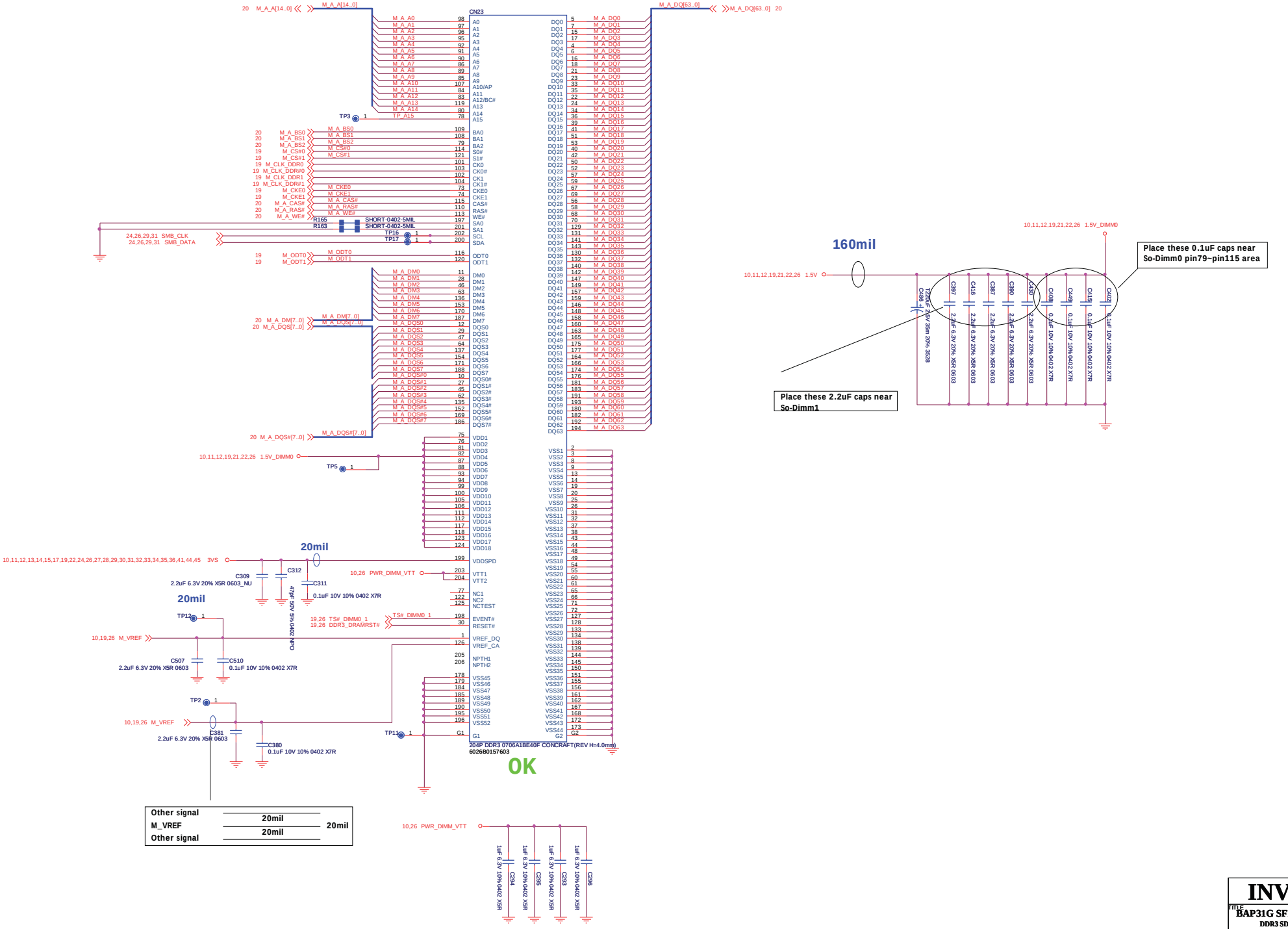
SO-DIMM0



CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009

INVENTEC

TITLE
BAP31G SFF
DDR3 SDRAM SO-DIMM0

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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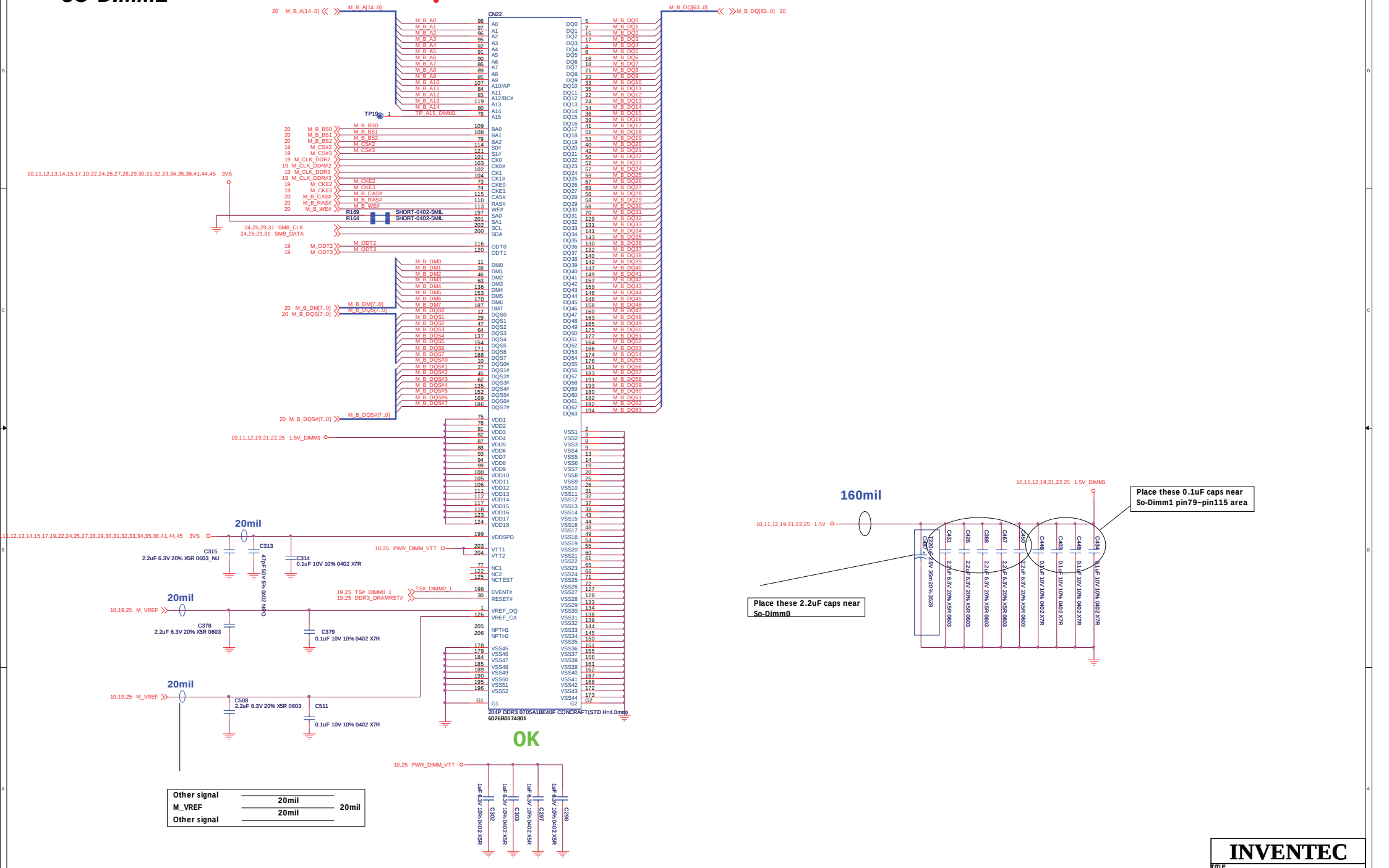
SO-DIMM1



Other signal	20mil	20mil
M_VREF	20mil	
Other signal		

INVENTEC

TITLE: BAP31G SFF
DDR3 SDRAM SO-DIMM1

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

CHANGE by S-H Chung | DATE Tuesday, May 26, 2009 | SHEET 26 of 47

RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICHm requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

For JM31,SJM31 For BAP31

For Green PC

BATT1

123

CABLE,ROUND,3POS,75mm,I,RTC_NU

6027B0066801

RTC Battery Life :

220mAh(220000uAh) / 6uA = 4.2 year

Place all series resistors 0.6 to 2.6 inches from the ICH9

Needs to be placed within 2" of ICH9m

Must be placed within 2" of 24.9 ohm w/o stub

Distance between the ICH9-M and cap on the "P" signal should be identical distance between the ICH9-M and cap on the "N" signal for same pair.

Placed within 500mils of ICH9m ball

ICH8m internal VR enable strap

	Enable	Disable
INTVRMEN	1(Default)	0

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05

Short pins AG1 and AG2 at the package

ACZ_SDATAOUT strap functionality base on RSVD9 strap

XOR chain entrance (RSVD9 pulled low)

PCIE port config bit 1(RSVD9 not pulled low)

Stuff for XOR chain testing

XOR Chain Entrance Strap - to be updated		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

By Tony

INVENTEC

TITLE: BAP31G SFF

ICH9M CPU/IDE/SATA(1/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

CHANGE by S-H Chung DATE Tuesday, May 26, 2009 SHEET 27 of 47

PCIE AC coupling caps need to be within 250mils of the driver

WLAN
3G
LAN

C518 C519 C896 C897 C515 C514 0.1uF 10V 10% 0402 X7R

PCIE_RXN1 PCIE_RXP1 PCIE_TXN1 PCIE_TXP1
PCIE_RXN2 PCIE_RXP2 PCIE_TXN2 PCIE_TXP2
PCIE_RXN3 PCIE_RXP3 PCIE_TXN3 PCIE_TXP3

U40D

PCI-Express

Direct Media Interface

DMI0RXN DMI0RXP DMI0TXN DMI0TXP
DMI1RXN DMI1RXP DMI1TXN DMI1TXP
DMI2RXN DMI2RXP DMI2TXN DMI2TXP
DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_CLKN DMI_CLKP
DMI_ZCOMP DMI_IRCOMP

DMI_RXN0 DMI_RXP0 DMI_TXN0 DMI_TXP0
DMI_RXN1 DMI_RXP1 DMI_TXN1 DMI_TXP1
DMI_RXN2 DMI_RXP2 DMI_TXN2 DMI_TXP2
DMI_RXN3 DMI_RXP3 DMI_TXN3 DMI_TXP3
CLK_PCIE_ICH# CLK_PCIE_ICH

DMI_IRCOMP_R

12,16,22,27,30,31,36 1.5VS
R263 24.9-1%-1/16W-0402
10mil

Place within 500mils of ICH

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP

SPI_CLK SPI_CS0# SPI_CS1#/GPIO58/CLGPIO6 SPI_MOSI SPI_MISO

SPI

USB

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P

USB_RBIAS_PN
USBRBIAS USBRBIAS#
R591 22.6-1%-1/16W-0402

9,10,11,12,13,27,29,30,31,32,33,34,35,46,47 3VA
R619 10K-5%-1/16W-0402

OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8#/GPIO44 OC9#/GPIO45 OC10#/GPIO46 OC11#/GPIO47

USB port
USB port
USB port
EASY PORT
WLAN
Finger printer
Bluetooth
Camera
Card Reader
3G

M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801

Place within 500mils of ICH
5/5 mils spacing on microstrip

U40B

PCI

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

REQ0# GNT0# REQ1#/GPIO50 GNT1#/GPIO51 REQ2#/GPIO52 GNT2#/GPIO53 REQ3#/GPIO54 GNT3#/GPIO55

C/BE0# C/BE1# C/BE2# C/BE3#

IRDY# PAR PCIRST# DEVSEL# PERR# PLOCK# SERR# STOP# TRDY# FRAME#

PLTRST# PCICLK PME#

PCI_REQ#0 PCI_GNT#0 PCI_REQ#1 DGPU_SELECT# 34,44 PCI_GNT#2 PCI_REQ#3 PCI_GNT#3 PCI_IRDY# PCI_DEVSEL# PCI_PERR# PCI_LOCK# PCI_SERR# PCI_STOP# PCI_TRDY# PCI_FRAME# PLT_RST# CLK_PCIF_ICH

Interrupt I/F

PIRQA# PIRQB# PIRQC# PIRQD#
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5

PCI_IRQA# PCI_IRQB# PCI_IRQC# PCI_IRQD#
PCI_IRQE# PCI_IRQF# PCI_IRQG# PCI_IRQH#

M10_ICH9M_SFF FCBGA 569P INTEL
6019B0621801

PCI Pull up

10,11,12,13,14,15,17,19,22,24,25,26,27,29,30,31,32,33,34,35,36,41,44,45 3VS

PCI_DEVSEL#	R582	8.2K-5%-1/16W-0402
PCI_SERR#	R318	8.2K-5%-1/16W-0402
PCI_PERR#	R590	8.2K-5%-1/16W-0402
PCI_IRDY#	R599	8.2K-5%-1/16W-0402
PCI_LOCK#	R589	8.2K-5%-1/16W-0402
PCI_FRAME#	R576	8.2K-5%-1/16W-0402
PCI_STOP#	R586	8.2K-5%-1/16W-0402
PCI_TRDY#	R598	8.2K-5%-1/16W-0402
PCI_REQ#0	R602	8.2K-5%-1/16W-0402
PCI_REQ#1	R574	8.2K-5%-1/16W-0402
DGPU_SELECT#	R569	8.2K-5%-1/16W-0402
PCI_REQ#3	R583	8.2K-5%-1/16W-0402
PCI_IRQA#	R609	8.2K-5%-1/16W-0402
PCI_IRQB#	R601	8.2K-5%-1/16W-0402
PCI_IRQC#	R608	8.2K-5%-1/16W-0402
PCI_IRQD#	R577	8.2K-5%-1/16W-0402
PCI_IRQE#	R610	8.2K-5%-1/16W-0402
PCI_IRQF#	R611	8.2K-5%-1/16W-0402
PCI_IRQG#	R603	8.2K-5%-1/16W-0402
PCI_IRQH#	R322	8.2K-5%-1/16W-0402

9,10,11,12,13,27,29,30,31,32,33,34,35,46,47 3VA
C812 0.1uF 10V 10% 0402 X7R
U38
PLT_RST#
TC7SZ08F SOT23 5P
6019A0070301
TP20
BUF_PLT_RST# 29,31,32,35,38
Buffer to reduce loading on PLT_RST#
R518 100K-5%-1/16W-0402
R514 0-5%-1/16W-0402_NU

PCI_GNT#2 R573 1K-5%-1/16W-0402_NU
PCI_GNT#3 R587 1K-5%-1/16W-0402_NU
PCI_GNT#0 R604 1K-5%-1/16W-0402_NU

PCI_GNT#3	No stuff : by default Stuff : For A16 swap override

PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI

Check BIOS type

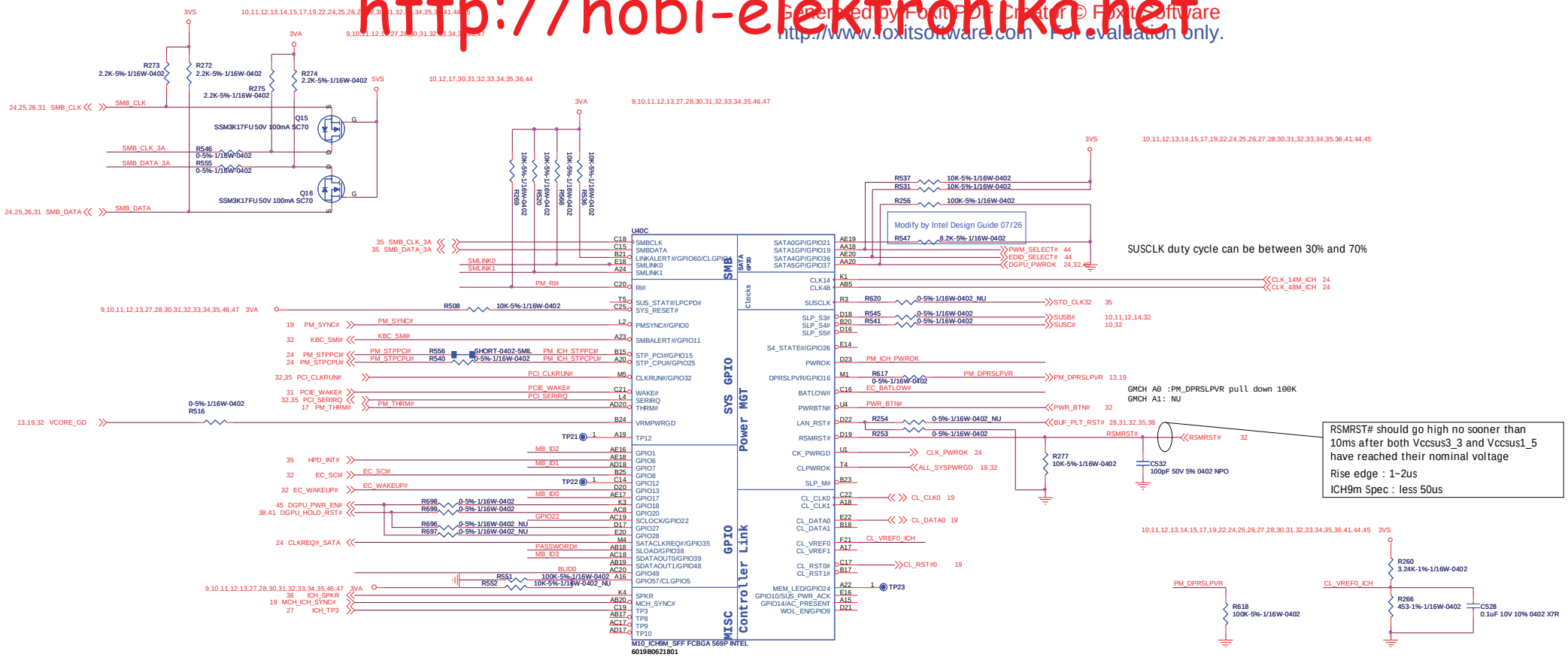
INVENTEC

TITLE: BAP31G SFF
ICH9M PCI/PCIE/DMI/USB(2/4)

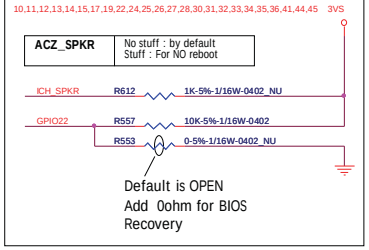
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

SHEET 28 of 47

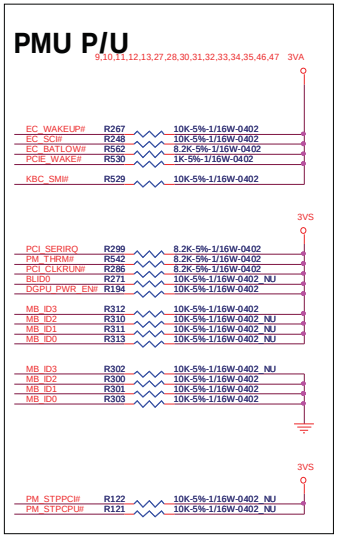
CHANGE by S-H Chung DATE Tuesday, May 26, 2009



ICH9m strap



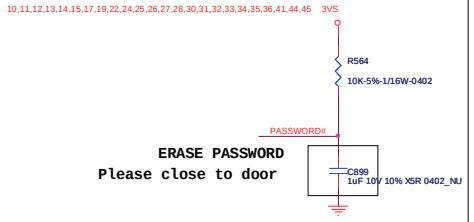
PMU P/U

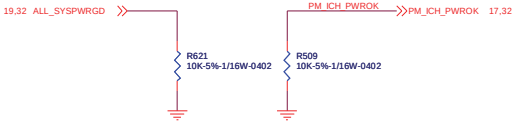


BIOS ID setting

Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
BAP41 (UMA)	1	1	0	0
BAP51 (UMA)	1	0	1	1
JM31 (dGPU)	1	0	1	0
SJM31 (dGPU)	1	0	0	1
BAP31 (dGPU)	1	0	0	0
BAP41 (dGPU)	0	1	1	1
BAP51 (dGPU)	0	1	1	0
	0	1	0	1
	0	1	0	0
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0

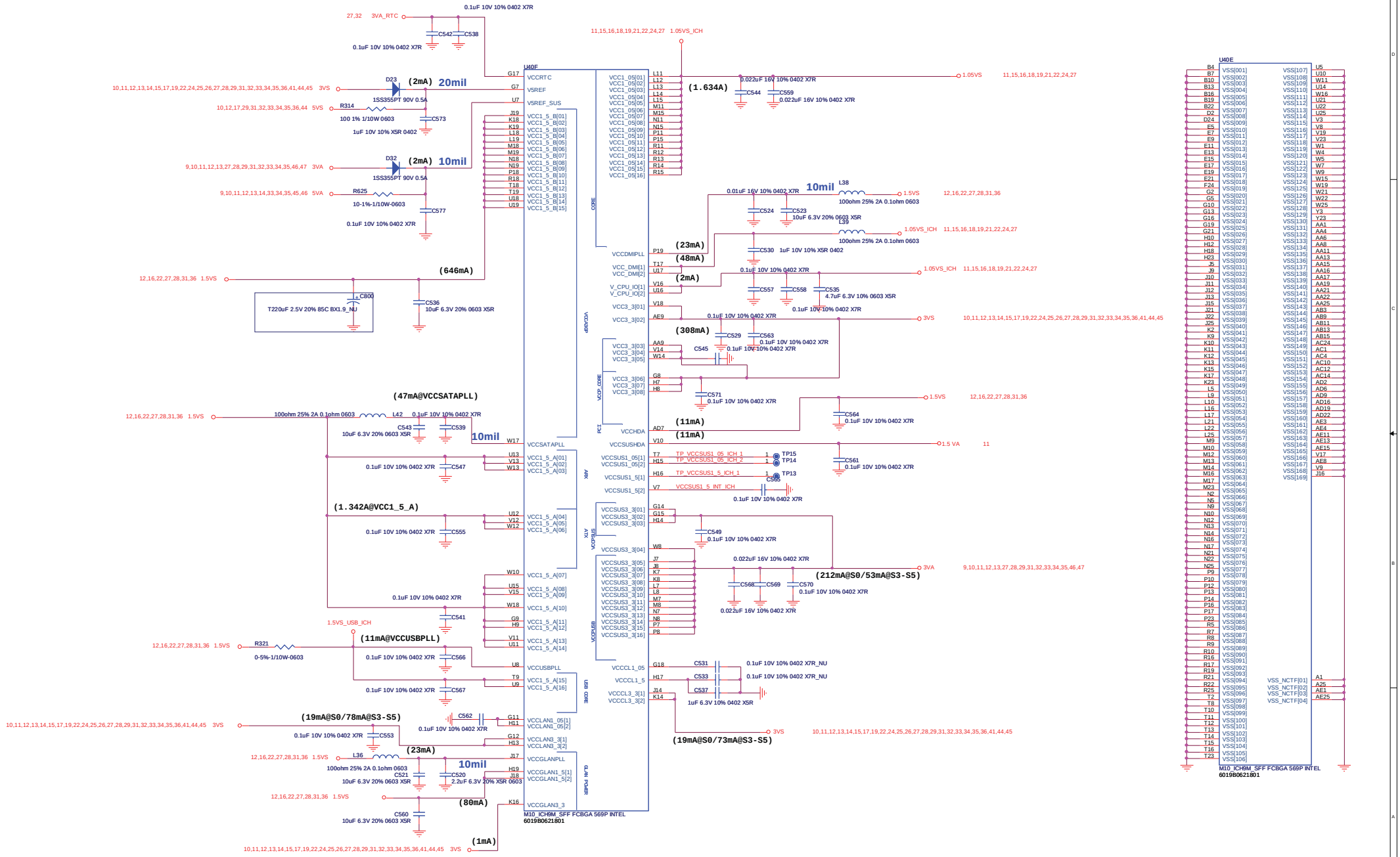
PASSWORD CLEAR





CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009	
SIZE	CODE	DOC.NUMBER		REV
Custom	CS	D-CS-1310A2264501-ALG		A03
		SHEET	29 of 47	

INVENTEC
TITLE
BAP31G SFF
ICH9M GPIO(3/4)



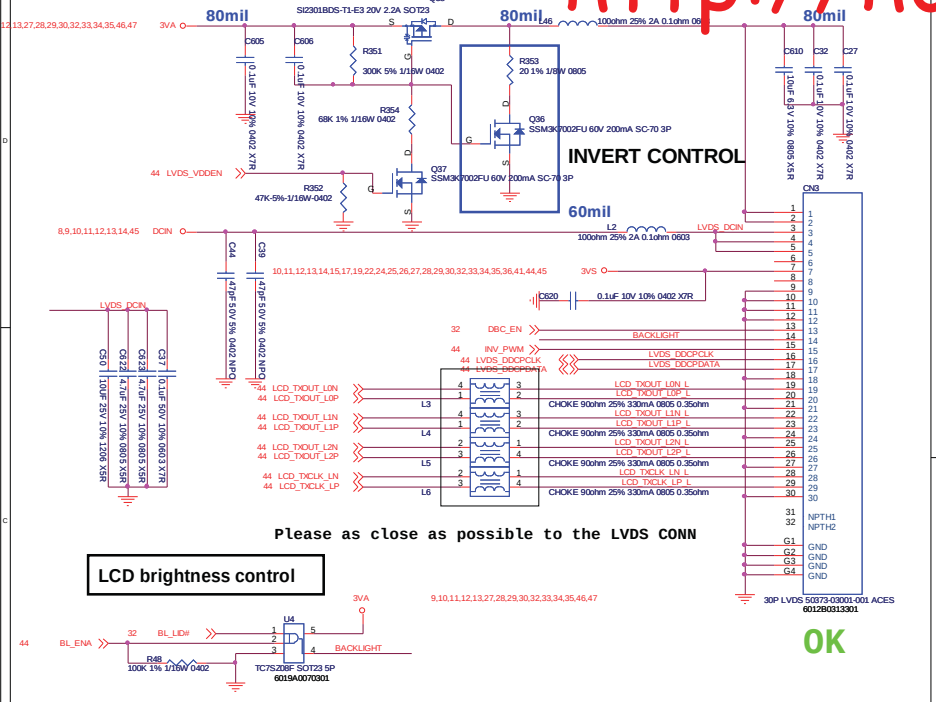
CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009	

INVENTEC

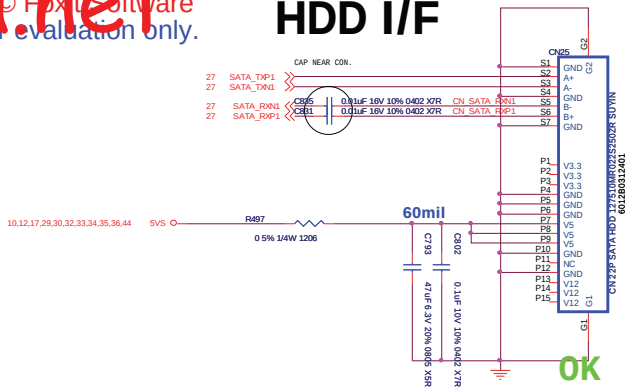
TITLE
BAP31G SFF
ICH9M Power/GND(4/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03
	SHEET	30 of 47	

LVDS Interface

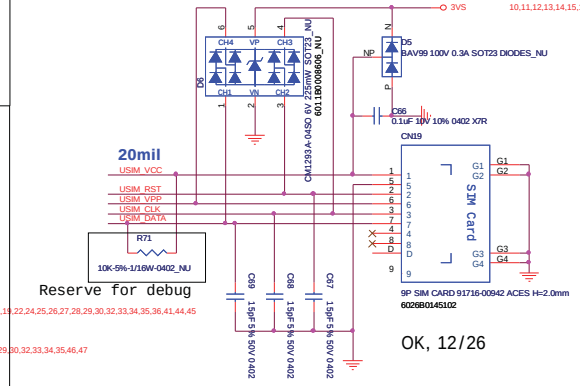


HDD I/F

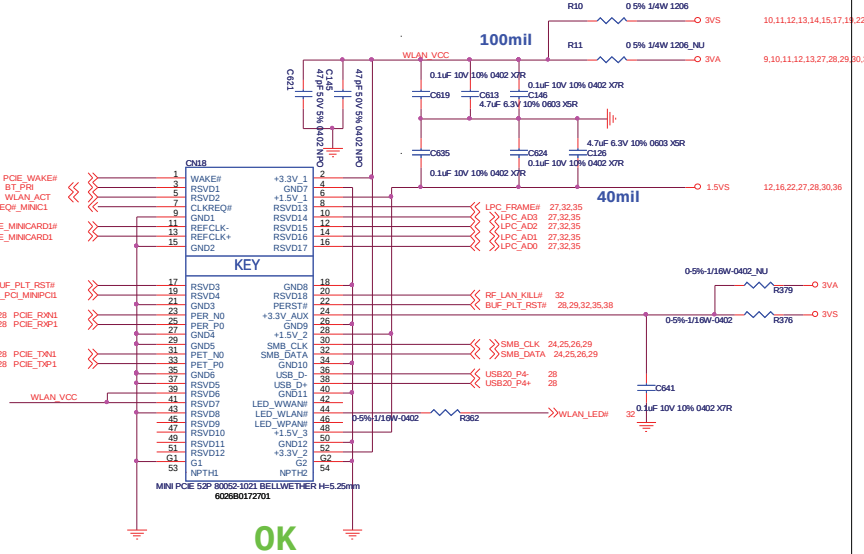


SIM CARD slot

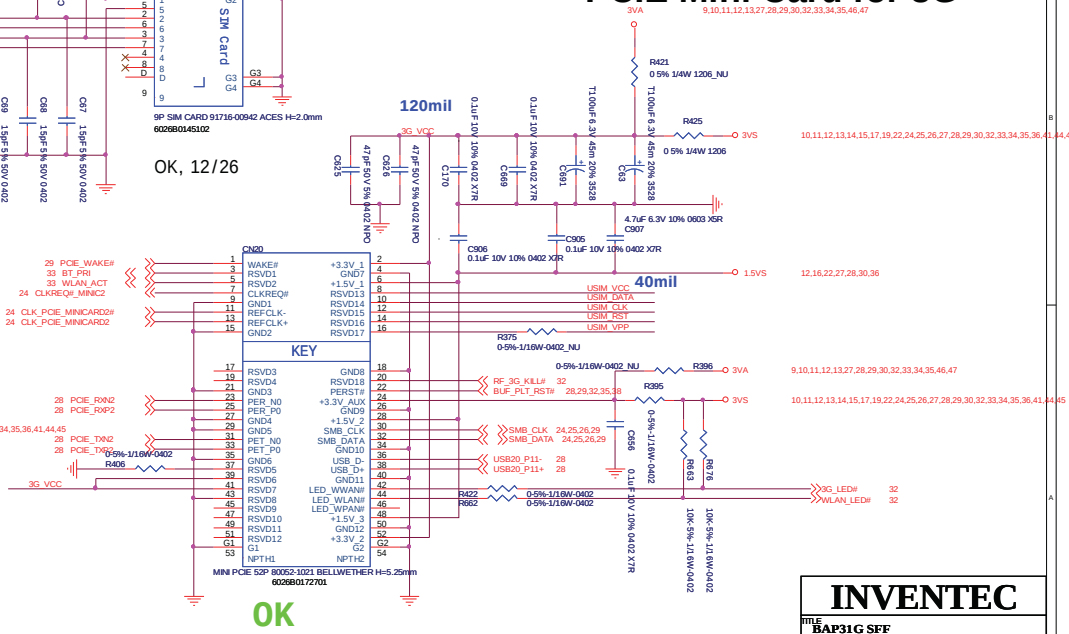
On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.



PCIE Mini Card(WLAN)



PCIE Mini Card for 3G



INVENTEC

TITLE: BAP31G SFF
LCD CNN & WLAN & 3G

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A284501-ALG	A03

CHANGE by: S-H Chung | DATE: Tuesday, May 26, 2009 | SHEET 31 of 47

IT8502E-L

IT8502E-L LQFP 128P ITE
6019B0617001

SPI FLASH

W25X16AVSSIG 1.8M SOIC 8P
6019B0307303

Don't place any pull-up resistor on GPG0 and GPG6

Pull down is for SPI flash

GPIO groud I are only input mode
Group I and J are not 5V tolerant
GPIO groud J are only output mode

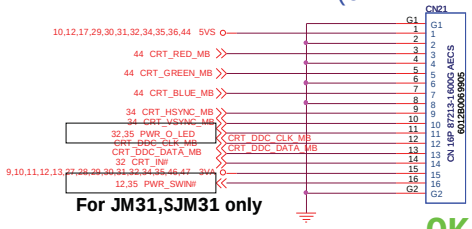
	R549	C818
For IT8502IX	0 Ohm	NU
For IT8502JX	NU	0.1uF

TITLE	INVENTEC BAP31G SFF KBC ITE8512F
SIZE / CODE / DOC.NUMBER / REV	Custom / CS / D-CS-1310A284501-ALG / A03
CHANGE by	S-H Chung
DATE	Tuesday, May 26, 2009
SHEET	32 of 47

For All Model

VGA Board CN

(CRT+ PWR SW)

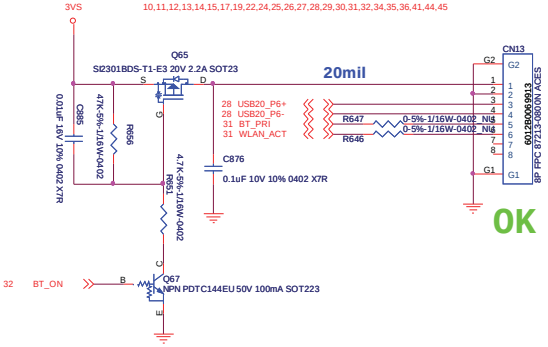


For JM31,SJM31 only

OK

For All Model

Bluetooth CON.

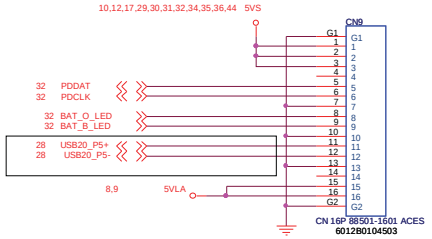


OK

For All Model

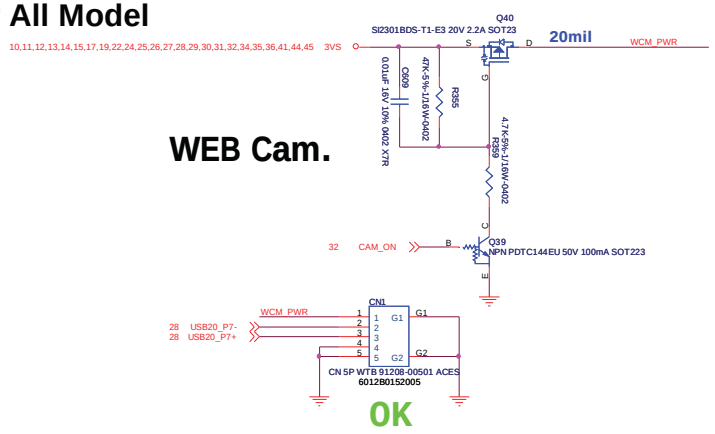
GLIDE PAD Board

For BAP31 only



For All Model

WEB Cam.



OK

For All Model

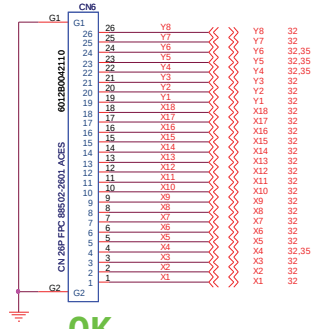
AUDIO Board CN

(Audio JACK+1USB)

OK

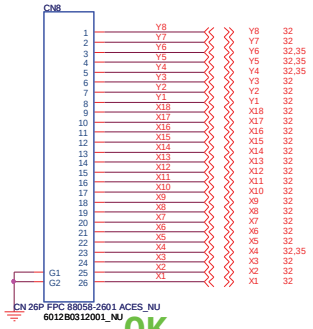
INVENTEC			
TITLE: BAP31G SFF Daughter Connector			
SIZE: Custom	CODE: CS_E	DOC NUMBER: D-CS-1310A2264501-ALG	REV: A03
CHANGE by: S-H Chung	DATE: Tuesday, May 26, 2009	SHEET: 33 of 47	

To K/B(For All Model)

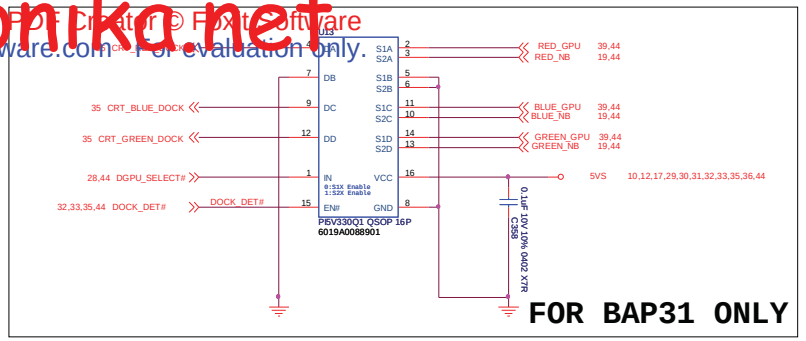


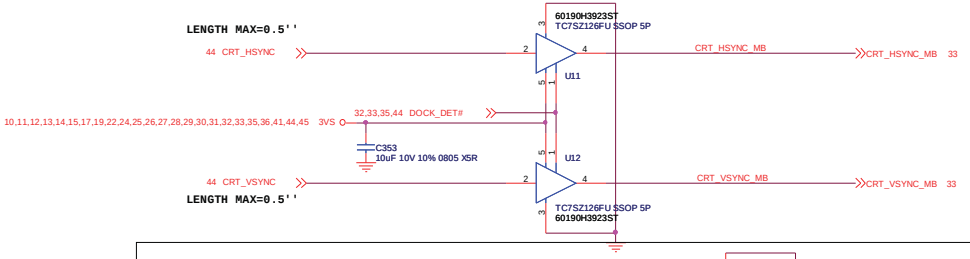
OK

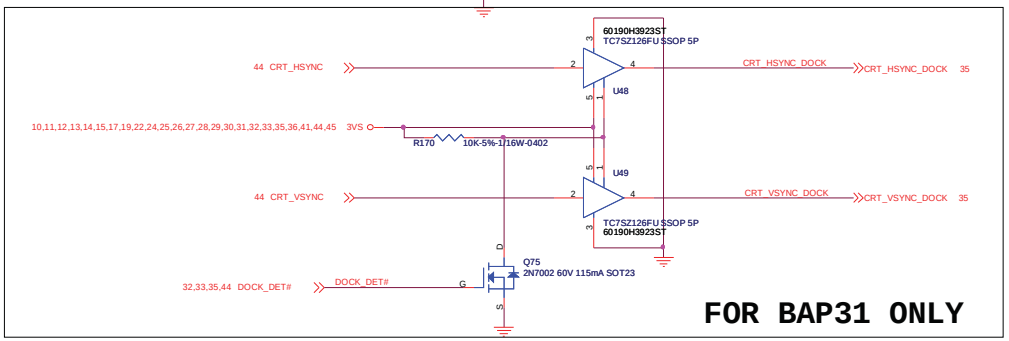
To K/B(No Use)



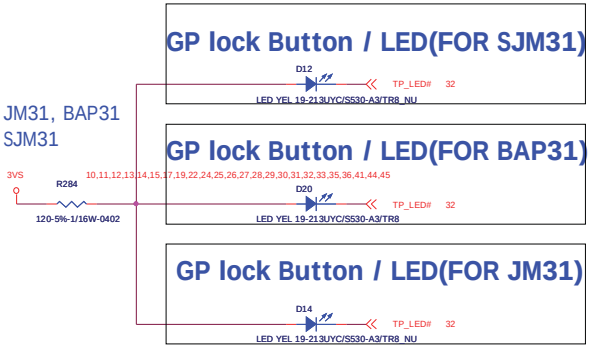
OK



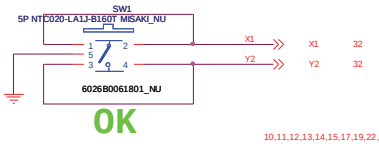




R284
120 ohm for JM31, BAP31
470 ohm for SJM31

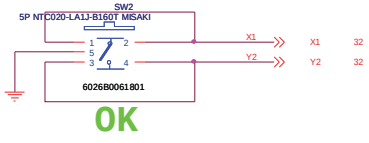


SW (No Use)



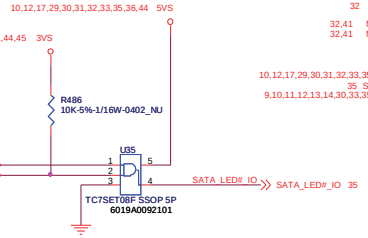
OK

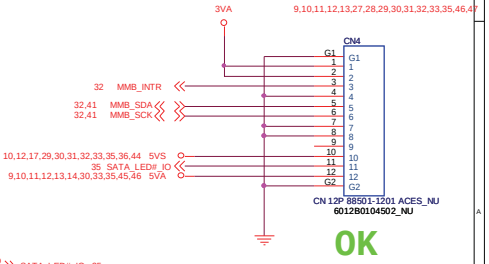
SW (FOR All Model)



OK

SW Sensor BOARD(For JM31,SJM31)



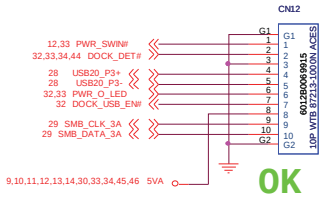


OK

CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009		
INVENTEC					
TITLE	BAP31G SFF				
	BDP				
SIZE	CODE	DOC NUMBER		REV	
Custom	CS	D-CS-1310A2264501-ALG		A03	
		SHEET	34 of 47		

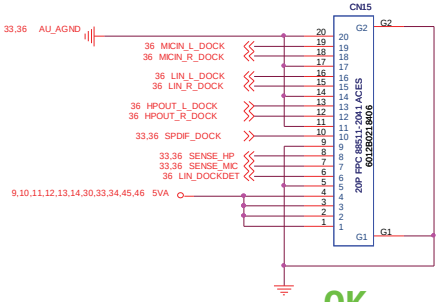
For BAP31(EASY/B)

MB(USB) TO EASY/B
For BAP31



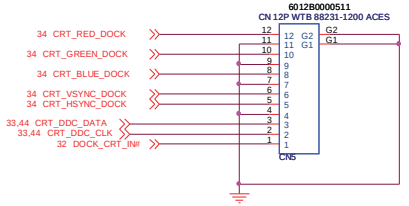
OK

MB(AUDIO) TO EASY/B
For BAP31

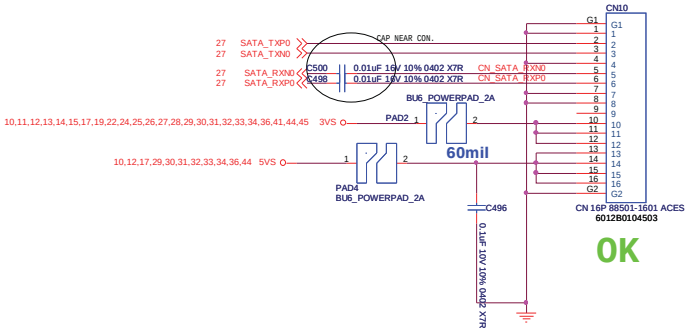


OK

MB(RGB) TO EASY/B
For BAP31

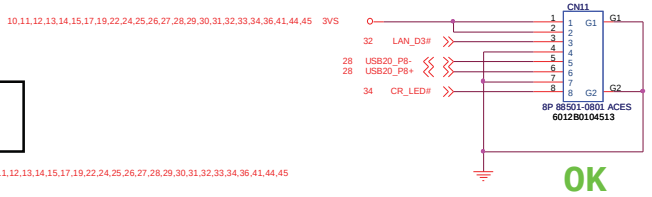


SSD I/F
For All Model



OK

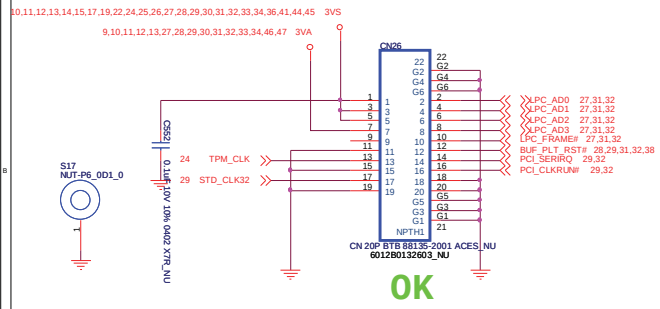
Card Reader BOARD CN
For All Model



OK

NO NEED

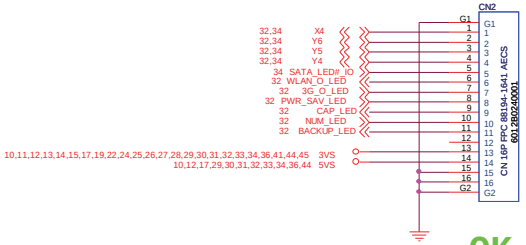
TPM CN



OK

For BAP31

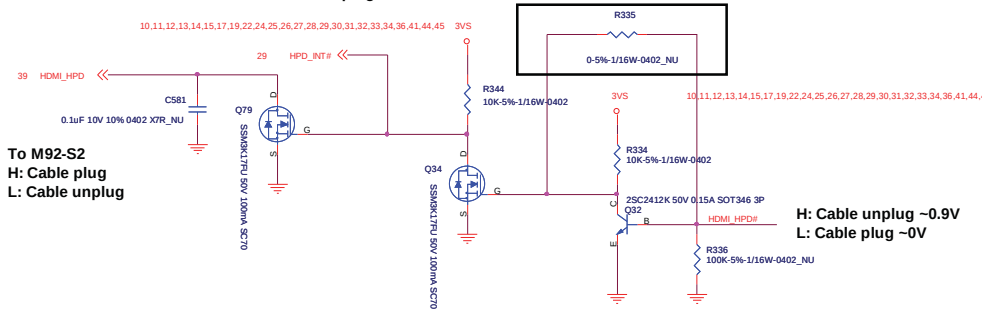
SW/B CN



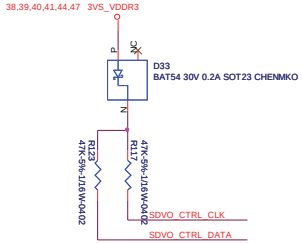
OK

To ICH-9M
H: Cable unplug
L: Cable plug

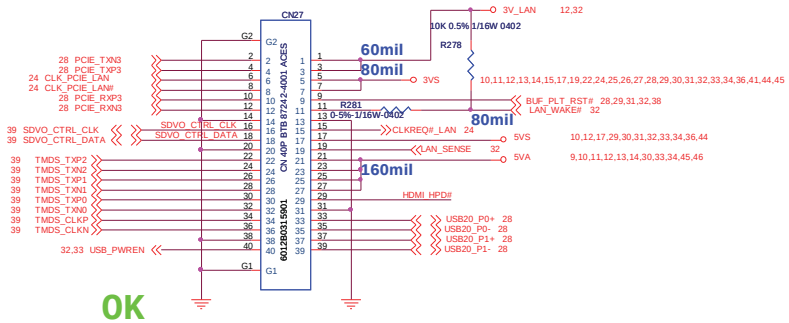
To M92-S2
H: Cable plug
L: Cable unplug



H: Cable unplug ~0.9V
L: Cable plug ~0V



USB Board CN (LAN+HDMI+2USB)
For All Model



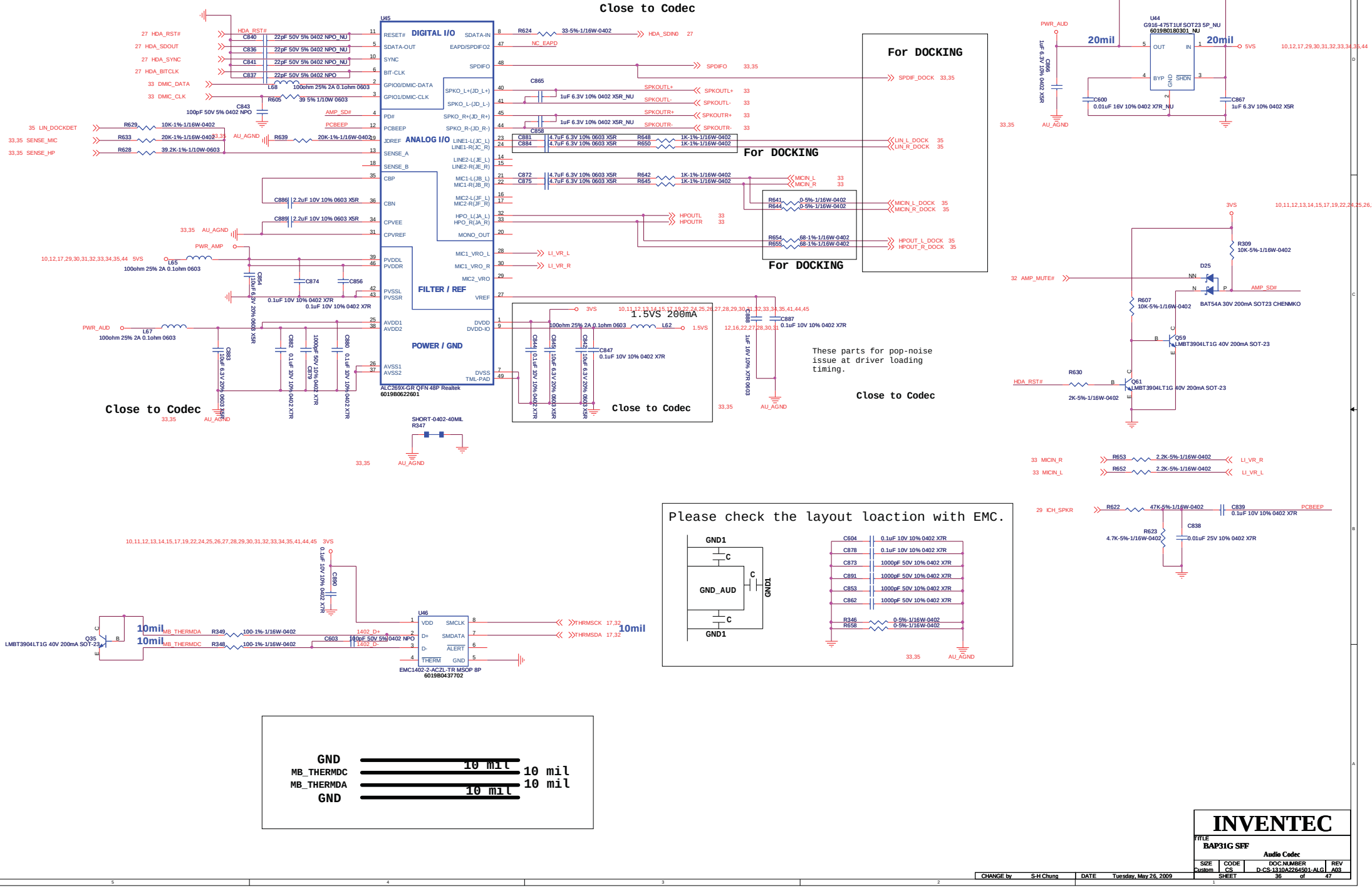
OK

INVENTEC

TITLE: BAP31G SFF
BDP

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

CHANGE by S-H Chung | DATE Tuesday, May 26, 2009 | SHEET 35 of 47



BLANK

CHANGE by	S-H Chung		
DATE	Tuesday, May 26, 2009		

INVENTEC

TITLE
BAP31G SFF
BLANK

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A284501-ALG	A03

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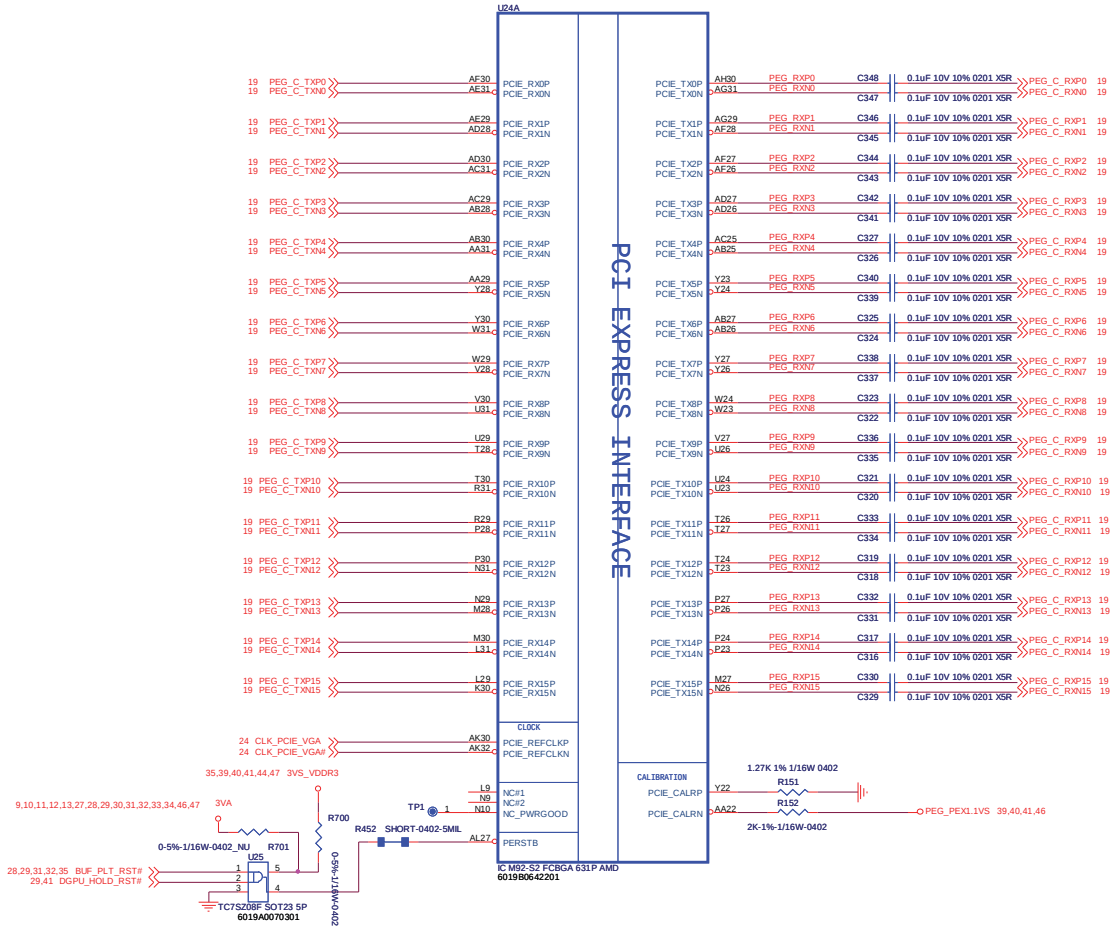

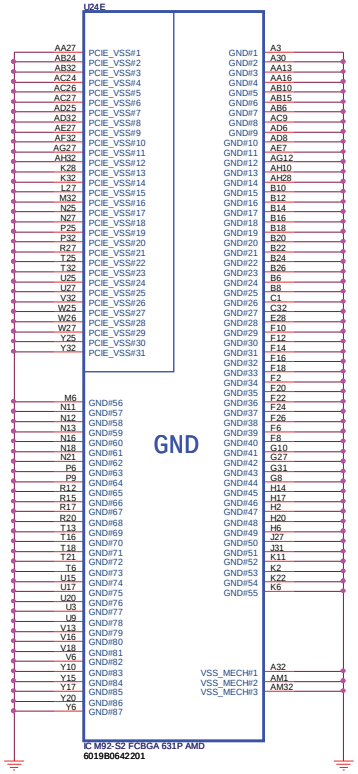

CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009

INVENTEC

TITLE: BAP31G SFF
M92 [1/5]

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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GPIO_13	GPIO_12	GPIO_11	For DDR3
0	0	0	128M
0	0	1	256M(Default)
1	1	0	Reserved

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	VENDOR
0	0	0	0	Hynix 64Mx16
1	0	0	0	Samsung 64Mx16

PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

FOR JM/SJM31 ONLY
BAP31 NU

H: Cable plug
L: Cable unplug

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

(1.8V@120mA DPLL_PVDD)

(1.1V@300mA DPLL_VDDC)

(1.8V@20mA TSVDD)

(1.8V@70mA AVDD)

(1.8V@45mA VDD1DI)

(1.8V@2mA AVDDQ)

(1.8V@40mA VDD2DI)

(3.3V@65mA A2VDD)

RESERVE SERIAL EEPROM 512K/1M

IC M92-S2 FCBGA 631P AMD
6019B0642201

CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009

INVENTEC

TITLE: BAP31G SFF
M92 [2/5]

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03
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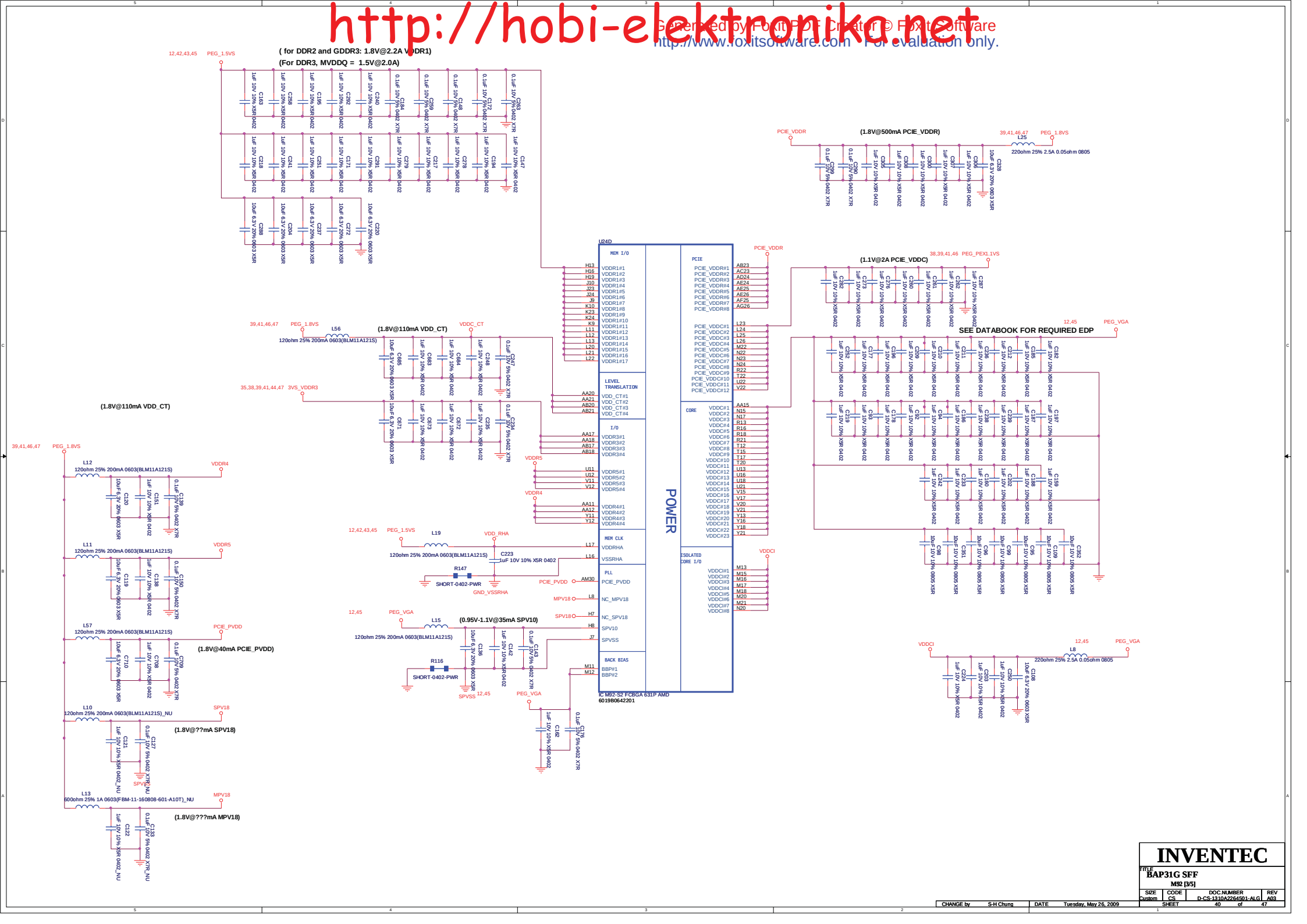
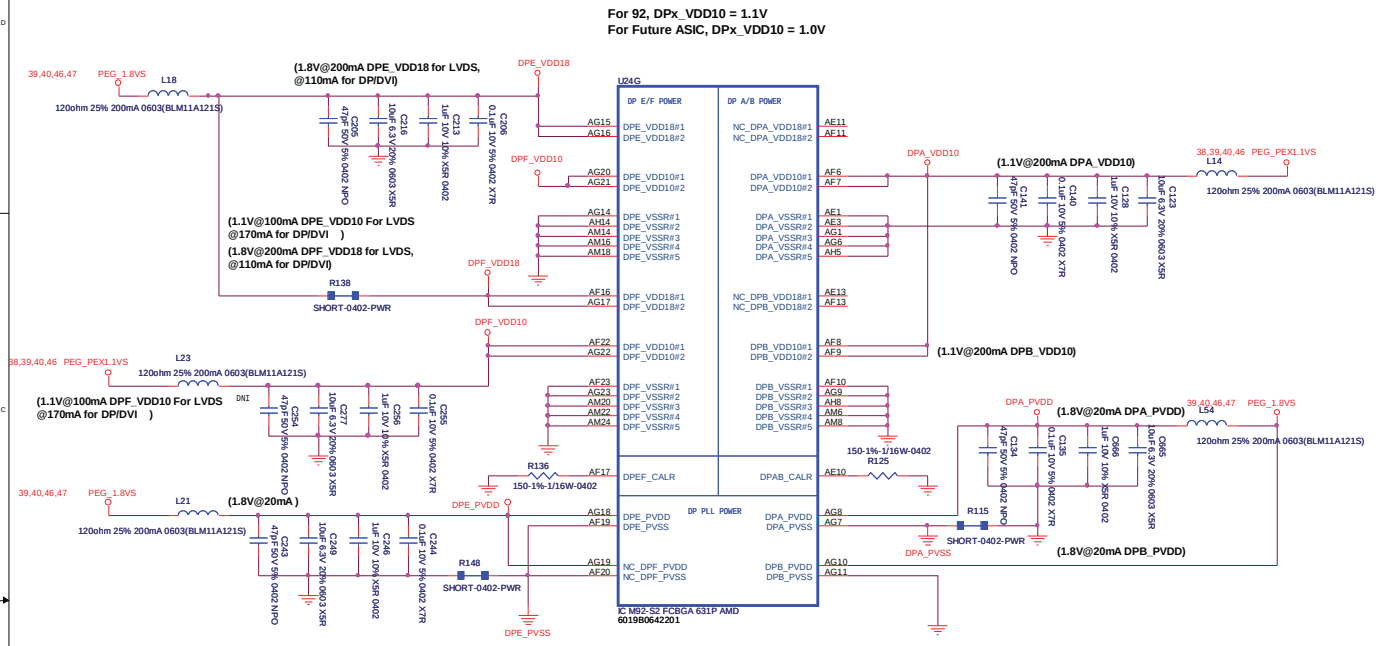


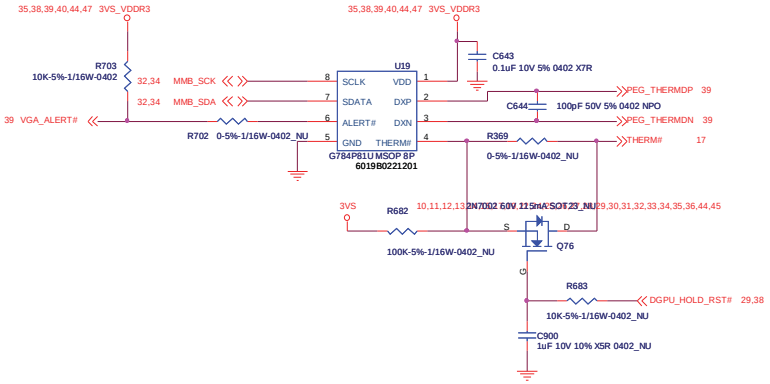
CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009		

INVENTEC

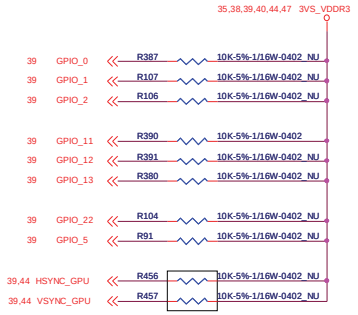
TITLE
BAP31G SFF
M92 [3/5]

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03
	SHEET	40 of 47	





PIN STRAPS



BAP31 R721, R722 OPEN
DVI no need Audio fuction
JM31/SJM31 R721, R722 install
HDMI need Audio function

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSYNC	0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

INVENTEC

TITLE: BAP31G SFF
M92 [4/5]

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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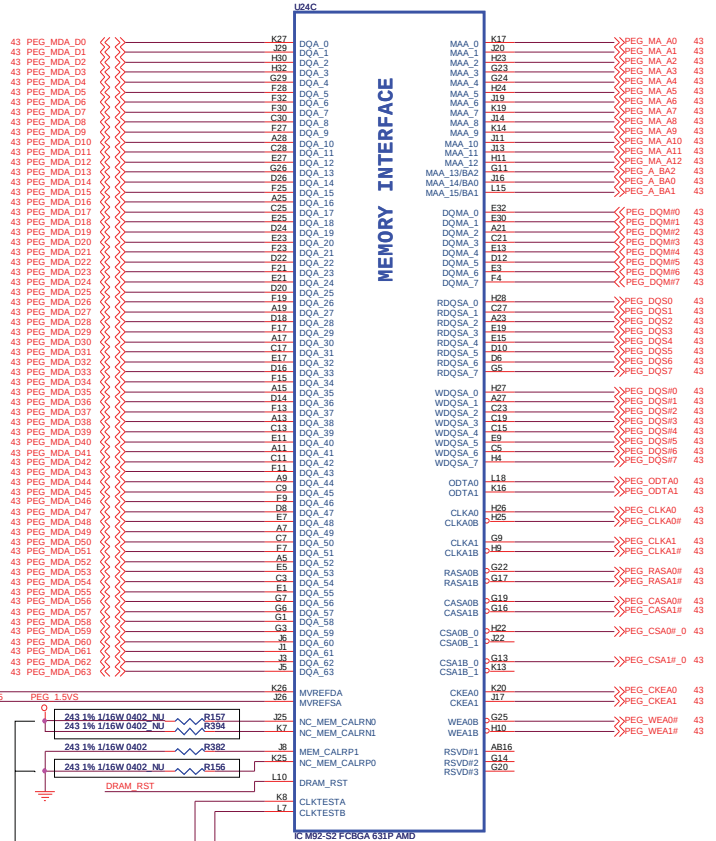
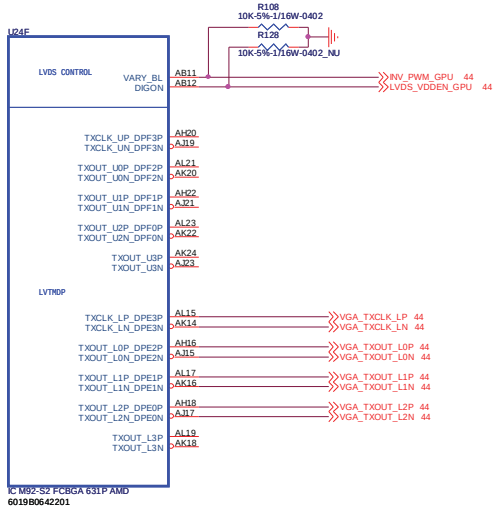
DDR3 Memory Interface



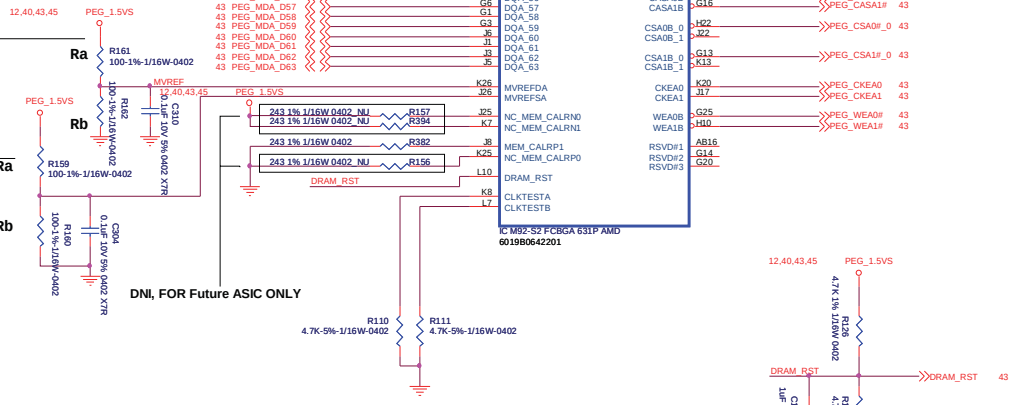
LVDS Interface



MVDDQ = 1.5V FOR DDR3 Memory

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R



CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009	

INVENTEC

TITLE: BAP31G SFF
M92 [5/5]

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03
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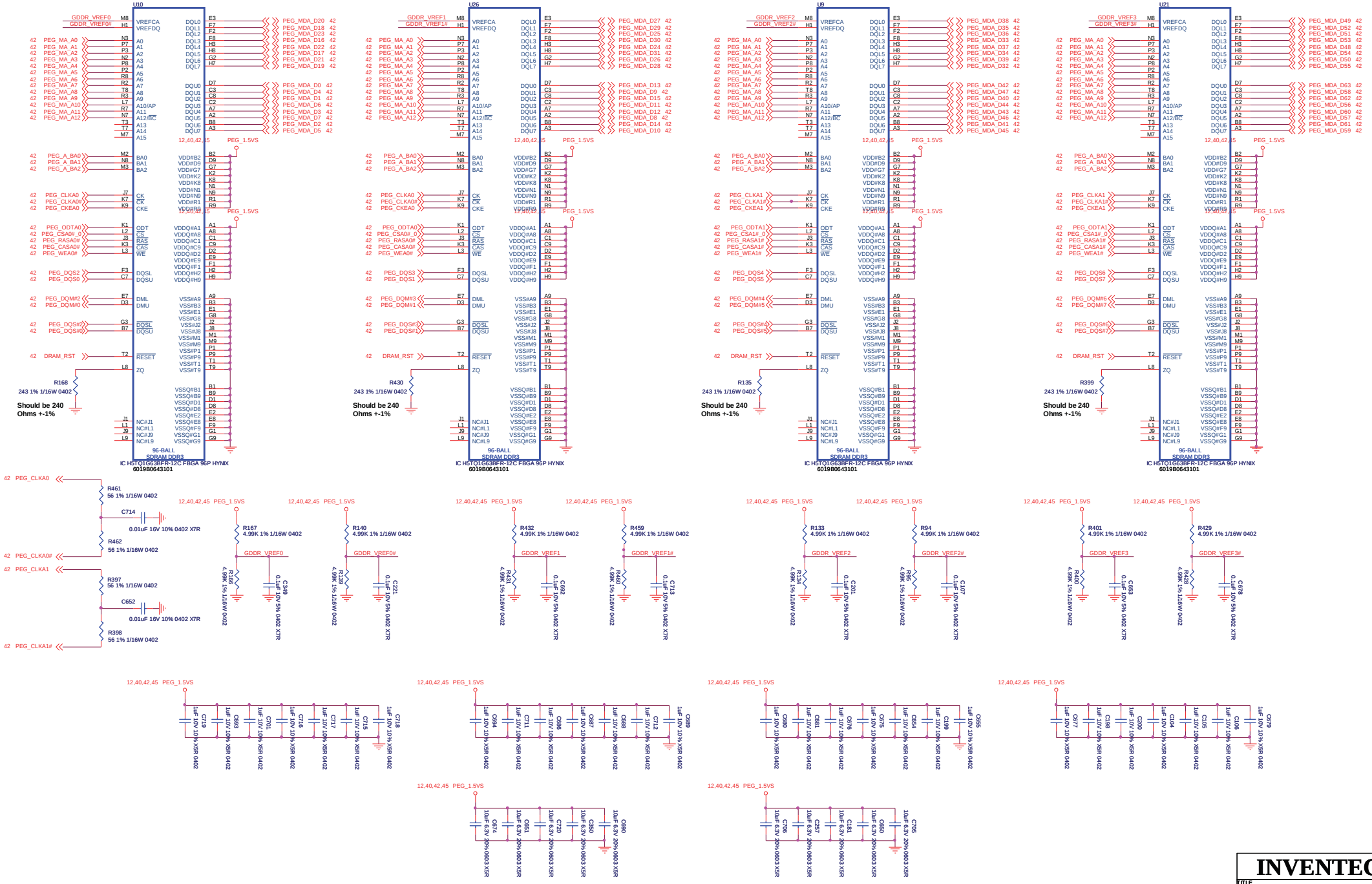

CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009

INVENTEC

TITLE: **BAP31G SFF**
VRAM

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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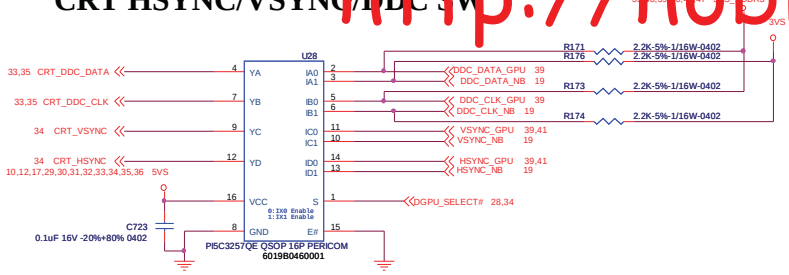
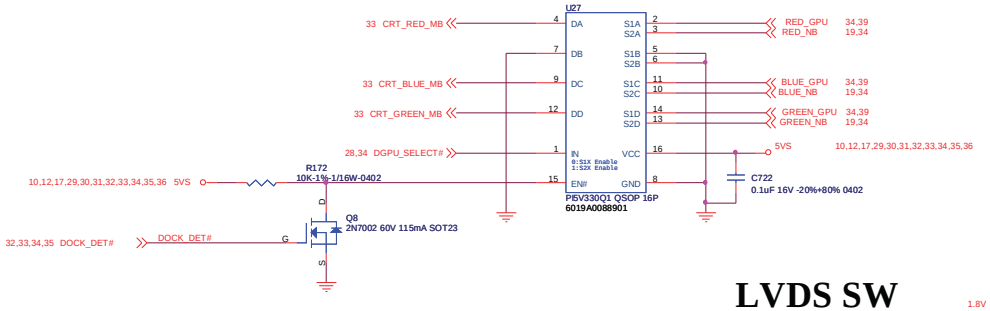
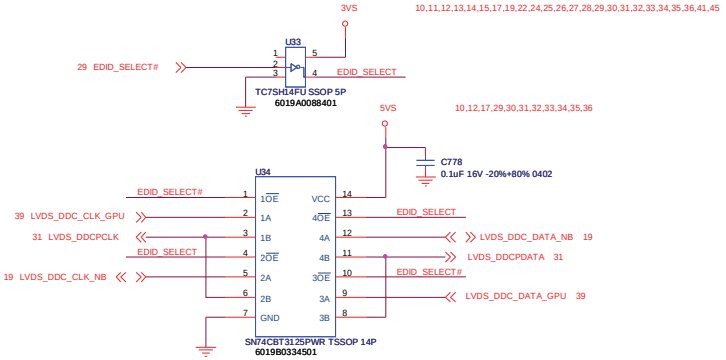
CRT HSYNC/VSYNC/DDC SW



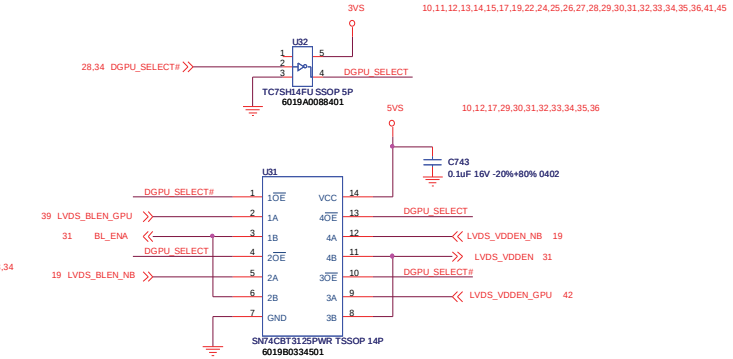
CRT R/G/B SW



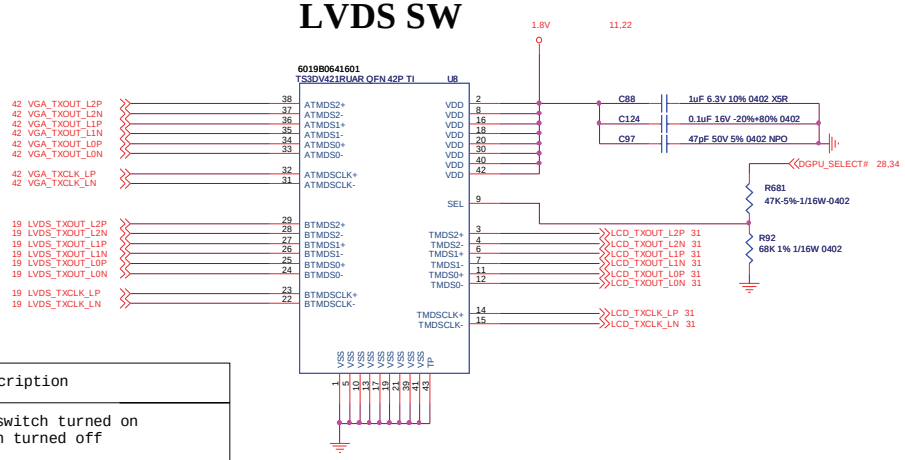
LCD DDC SW



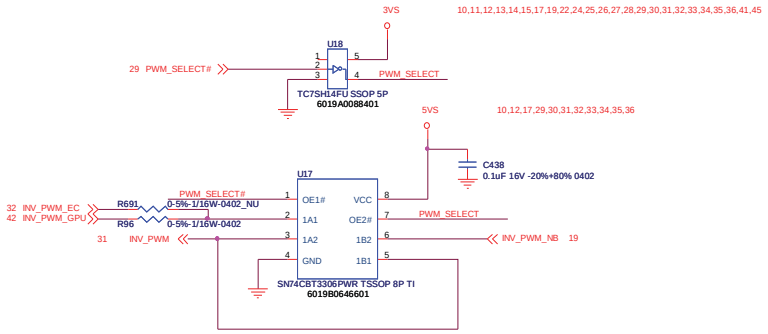
LVDS BKL and Vcc Enable SW



LVDS SW



LCD PWM SW



Signal	During Reset	After Reset	Description
DGPU_PWR_EN#	High	High	0 : dGPU power switch turned on 1 : power switch turned off
DGPU_PWROK			0 : dGPU power is not stable 1 : dGPU power is stable
DGPU_HOLD_RST#	Low	Low	0 : Keep dGPU in reset 1 : Reset is released
DGPU_SELECT#	High	High	0 : Display switch enabled for dGPU 1 : Display switch enabled for iGPU
HPD_INT#			0 : DVI insertion 1 : No DVI insertion
PWM_SELECT#		High	0 : PWM switch enabled for dGPU 1 : PWM switch enabled for iGPU
EDID_SELECT#		High	0 : EDID/DDC switch enabled for dGPU 1 : EDID/DDC switch enabled for iGPU

INVENTEC

TITLE: BAP31G SFF
Hybird Switch

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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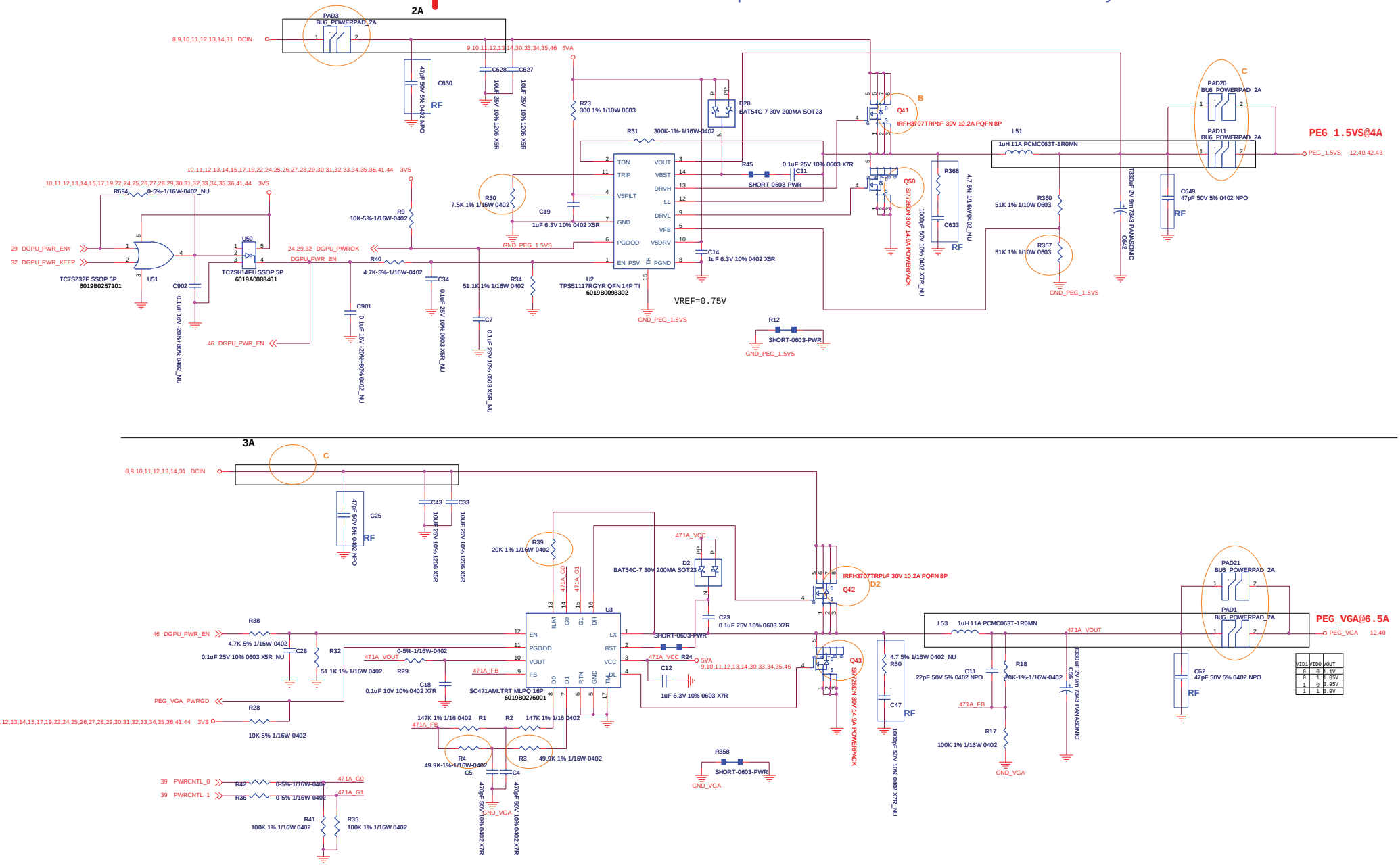

PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

INVENTEC

TITLE: BAP31G SFF
VGA Power[1/3]

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

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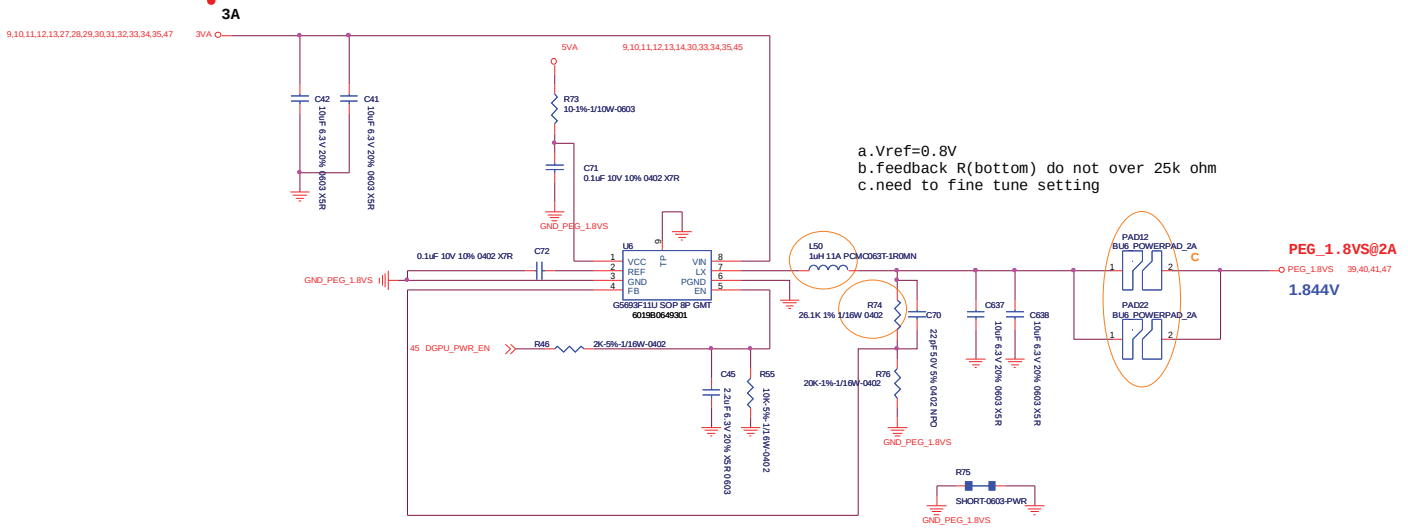
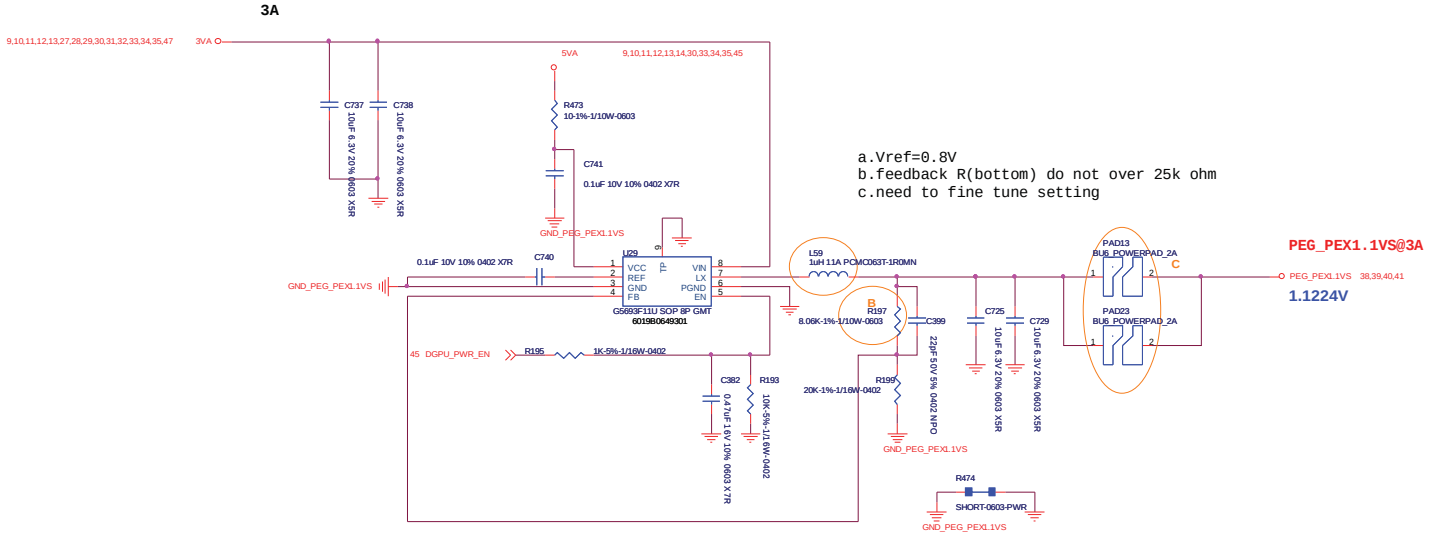


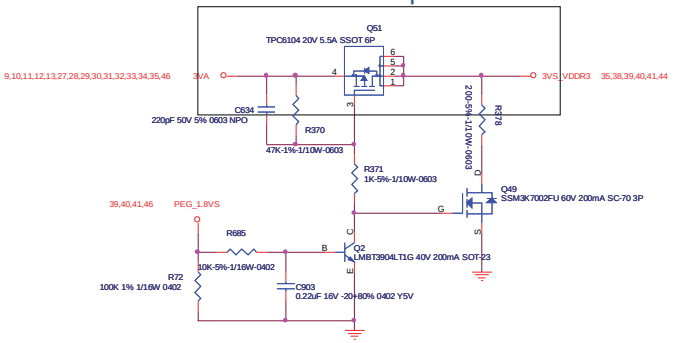


INVENTEC

TITLE: BAP31G SFF
VGA Power[2/3]

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A284501-ALG	A03

CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009	SHEET	46 of 47



CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009

INVENTEC

TITLE
BAP31G SFF
VGA Power[3/3]

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	D-CS-1310A284501-ALG	A03

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