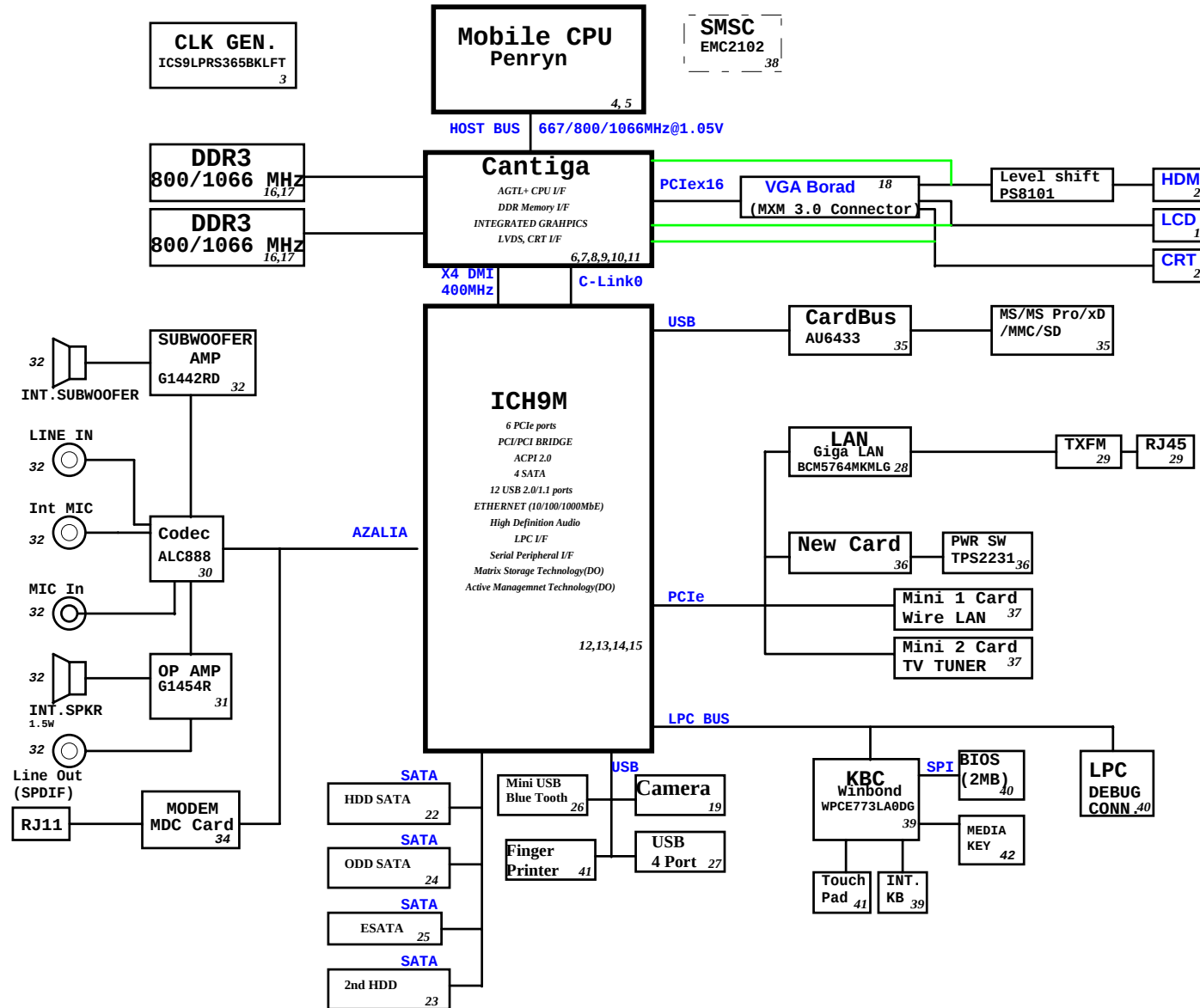


JM70 -MV Block Diagram

Project code: 91.4AN01.001
PCB P/N : 48.4AN01.0SA
REVISION : SB 08246



SYSTEM DC/DC ISL62392 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5
SYSTEM DC/DC TP551124 46	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A) 1D5V_S3(10A)
RT9026 49	
1.5V_S3	DDR_VREF_S3 (1.2A)
G9198-15 14	
3D3V_S5	1D5V_S5 (300mA)
CHARGER ISL88731A 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC ADP3208C 51	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0-1.3V 38A
GFX DC/DC ISL6263 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0-1.3V 6.5A

PCB STACKUP

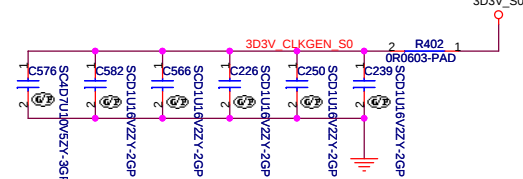
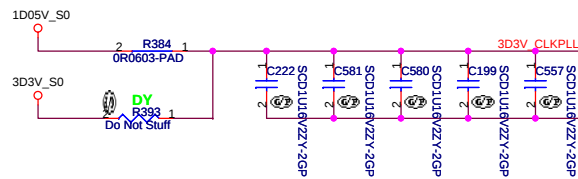
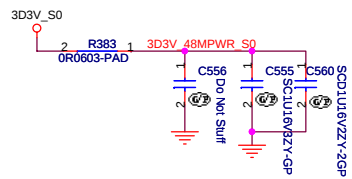
TOP _____
GND _____
S _____
S _____
GND _____
BOTTOM _____

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default). 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

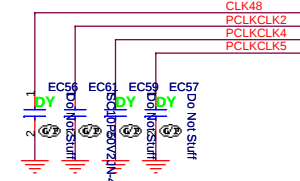
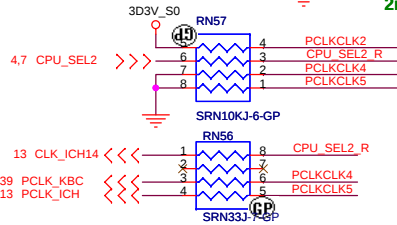
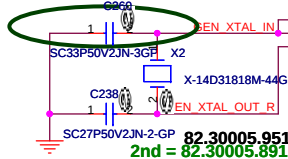
NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.



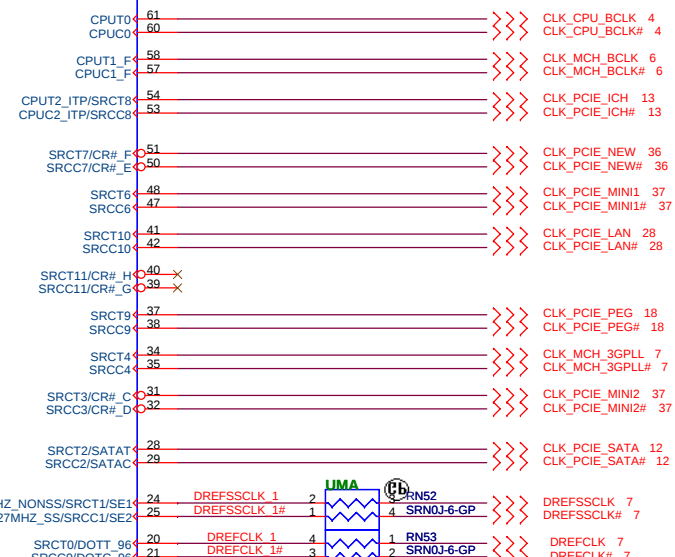
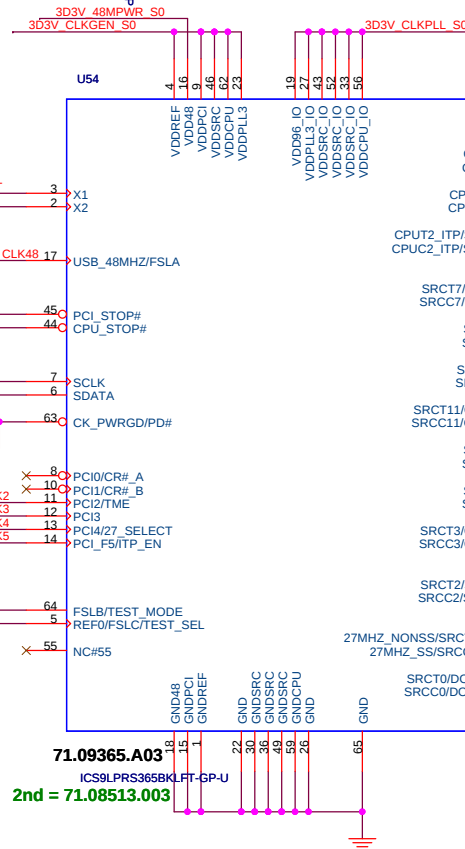
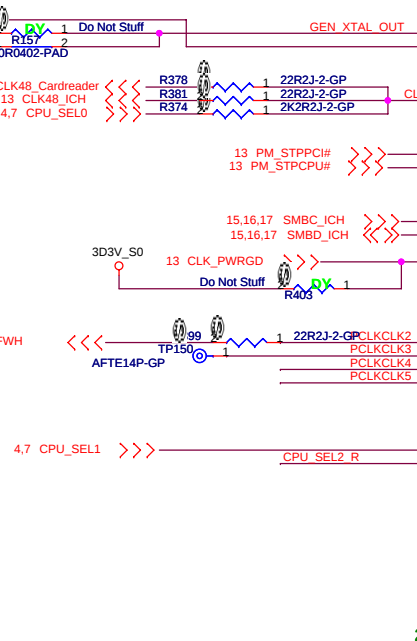
DY

2008.12.08 SB

CL=20pF±0.2pF



EMI capacitor



ICS9LPRS365YGLFT setting table

PIN	NAME	DESCRIPTION
PCI0/CR#_A		Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR# A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR# A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B		Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR# B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR# B controls SRC1 pair (default) 1 = CR# B controls SRC4 pair
PCI2/TME		0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3		
PCI4/27M_SEL		0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN		0 = SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C		Byte 5, bit 3 0 = SRC3 enabled (default) 1 = CR# C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR# C controls SRC0 pair (default), 1 = CR#_C controls SRC2 pair

PIN	NAME	DESCRIPTION
SRCC3/CR#_D		Byte 5, Bit 1 0 = SRC3 enabled (default) 1 = CR# D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1 = CR#_D controls SRC4 pair
SRCC7/CR#_E		Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_F controls SRC6
SRCT7/CR#_F		Byte 6, bit 6 0 = SRC7 enabled (default) 1 = CR#_F controls SRC8
SRCC11/CR#_G		Byte 6, bit 5 0 = SRC11# enabled (default) 1 = CR#_6 controls SRC9
SRCT11/CR#_H		Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

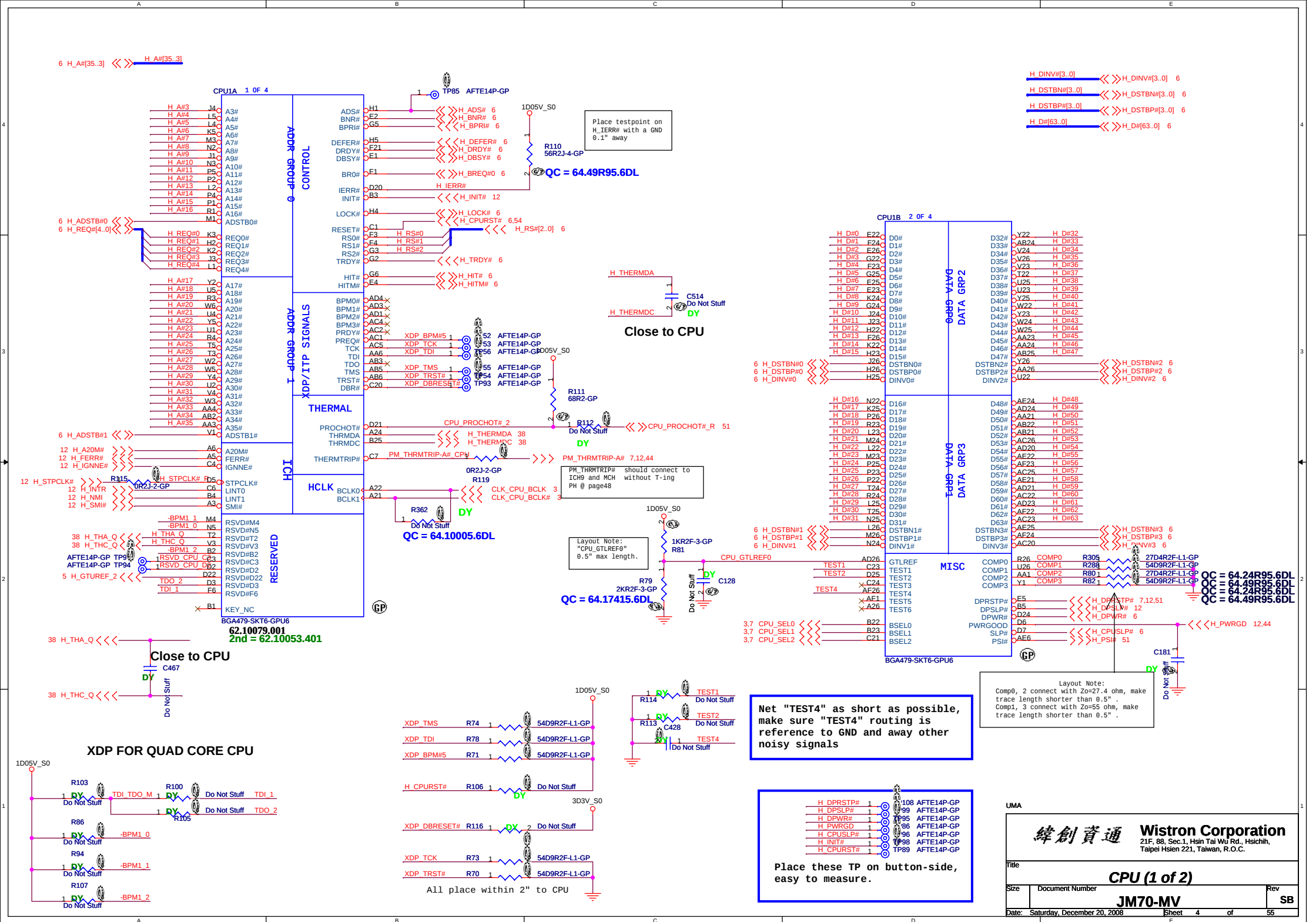
UMA

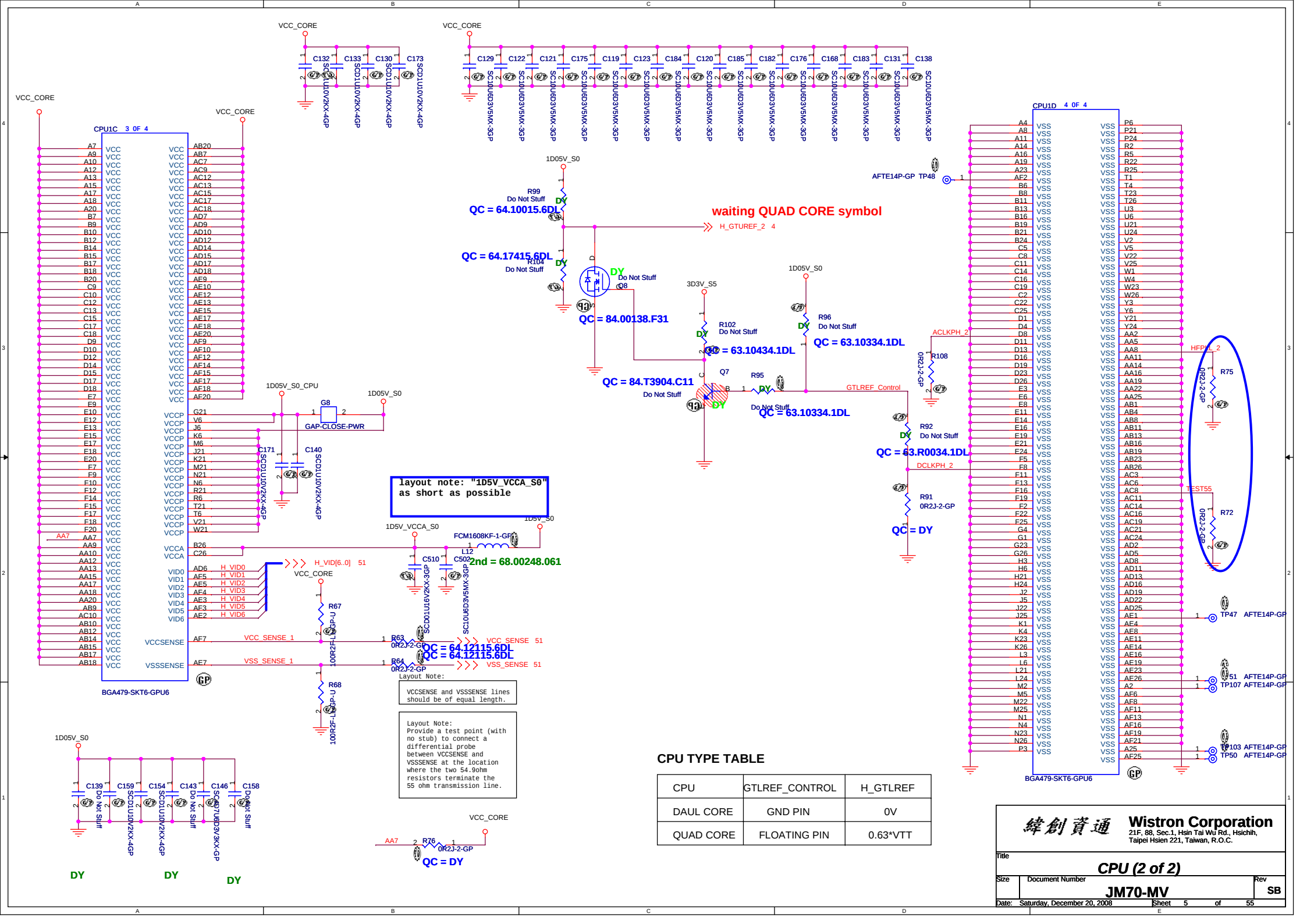
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator**

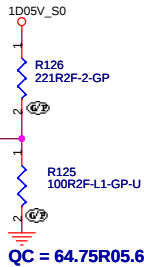
Size: Document Number **JM70-MV** Rev **SB**

Date: Saturday, December 20, 2008 Sheet 3 of 55



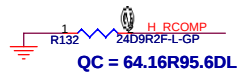


H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)

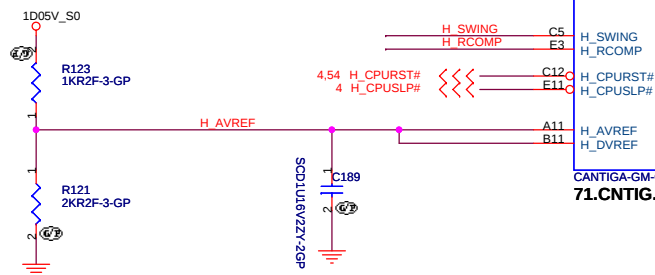


4 H_D#[63..0] << >> H_D#[63..0]





Place them near to the chip (< 0.5")



NB1A 1 OF 10

H_A# 3	A14	H_A#3
H_A# 4	C15	H_A#4
H_A# 5	F16	H_A#5
H_A# 6	H13	H_A#6
H_A# 7	C18	H_A#7
H_A# 8	M16	H_A#8
H_A# 9	J13	H_A#9
H_A# 10	P16	H_A#10
H_A# 11	P17	H_A#11
H_A# 12	M13	H_A#12
H_A# 13	E17	H_A#13
H_A# 14	P17	H_A#14
H_A# 15	P17	H_A#15
H_A# 16	E17	H_A#16
H_A# 17	G20	H_A#17
H_A# 18	B19	H_A#18
H_A# 19	H16	H_A#19
H_A# 20	E20	H_A#20
H_A# 21	H16	H_A#21
H_A# 22	J20	H_A#22
H_A# 23	L17	H_A#23
H_A# 24	H17	H_A#24
H_A# 25	B17	H_A#25
H_A# 26	L16	H_A#26
H_A# 27	C21	H_A#27
H_A# 28	J19	H_A#28
H_A# 29	H20	H_A#29
H_A# 30	A17	H_A#30
H_A# 31	L17	H_A#31
H_A# 32	B20	H_A#32
H_A# 33	F21	H_A#33
H_A# 34	K21	H_A#34
H_A# 35	L20	H_A#35

H_ADST#	H12	H_ADST# 4
H_ADSTB#0	R16	H_ADSTB#0 4
H_ADSTB#1	G17	H_ADSTB#1 4
H_BNR#	A9	H_BNR# 4
H_BPRI#	G12	H_BPRI# 4
H_BREQ#	E9	H_BREQ# 4
H_DEFER#	B10	H_DEFER# 4
H_DBSY#	AH7	H_DBSY# 4
HPLL_CLK	AH6	CLK_MCH_BCLK 3
HPLL_CLK#	J11	CLK_MCH_BCLK# 3
H_DPWR#	H9	H_DPWR# 4
H_DRDY#	E12	H_DRDY# 4
H_HIT#	H11	H_HIT# 4
H_HITM#	C9	H_HITM# 4
H_LOCK#	H11	H_LOCK# 4
H_TRDY#	H11	H_TRDY# 4

Figure 10: Pin connections for the HPS.

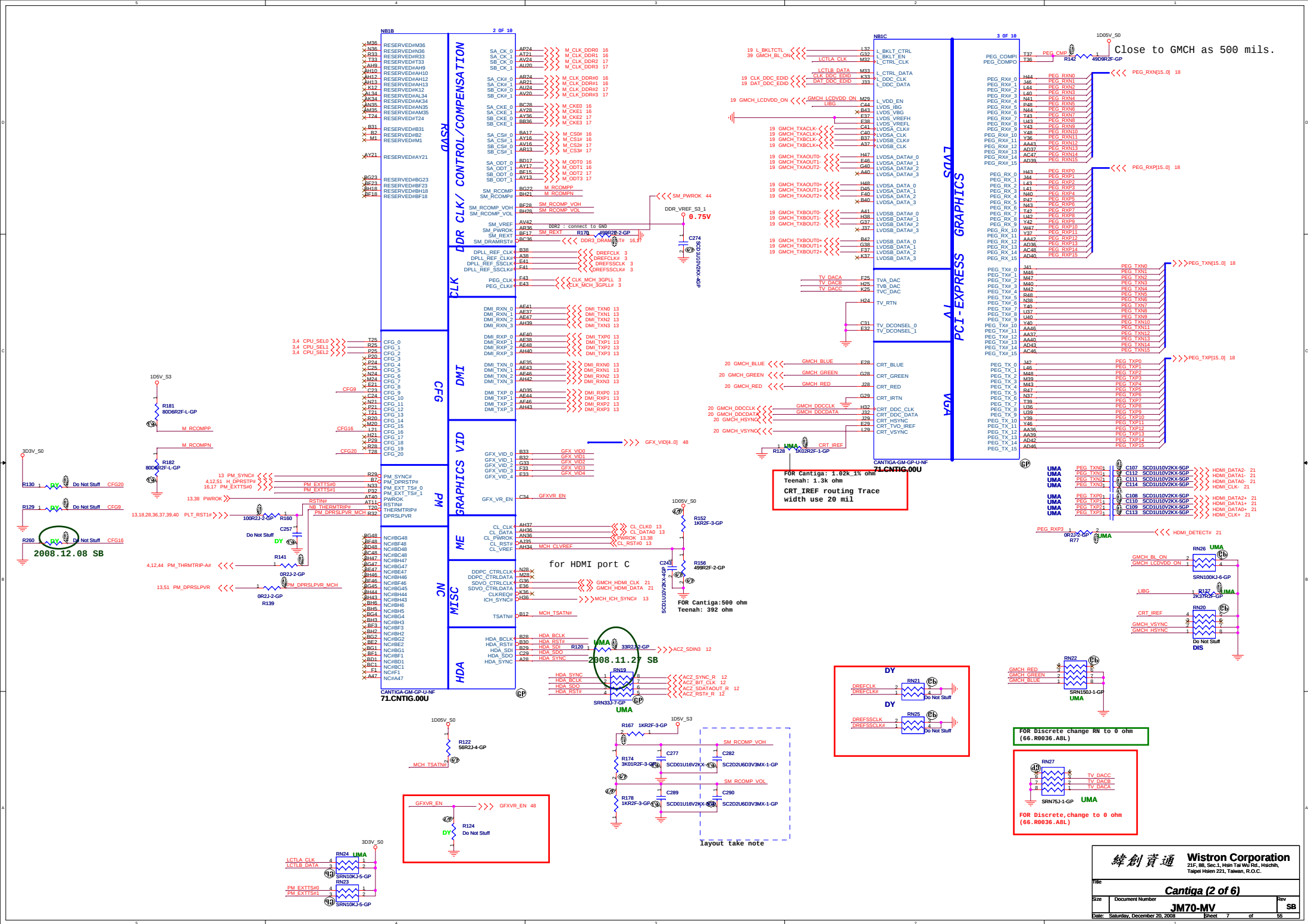
Pin	Function
H_DINV#_0	H_DINV#0
H_DINV#_1	H_DINV#1
H_DINV#_2	H_DINV#2
H_DINV#_3	H_DINV#3
H_DSTBN#_0	H_DSTBN#0
H_DSTBN#_1	H_DSTBN#1
H_DSTBN#_2	H_DSTBN#2
H_DSTBN#_3	H_DSTBN#3
H_DSTBP#_0	H_DSTBP#0
H_DSTBP#_1	H_DSTBP#1
H_DSTBP#_2	H_DSTBP#2
H_DSTBP#_3	H_DSTBP#3
H_REQ#_0	H_REQ#0, H_REQ#1, H_REQ#2, H_REQ#3, H_REQ#4
H_REQ#_1	
H_REQ#_2	
H_REQ#_3	
H_REQ#_4	
H_RS#_0	H_RS#0, H_RS#1, H_RS#2
H_RS#_1	
H_RS#_2	

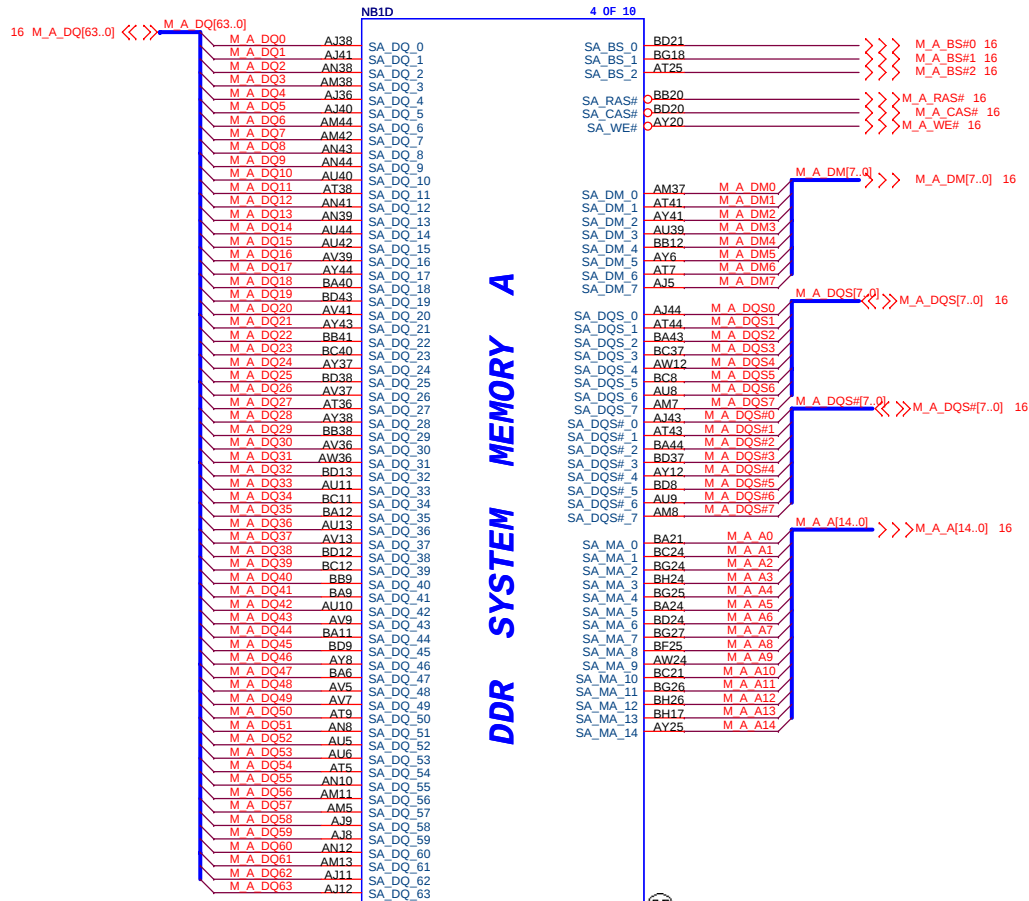
CANTIGA-GM-GP-U-NF
71.CNTIG.00U

UMA

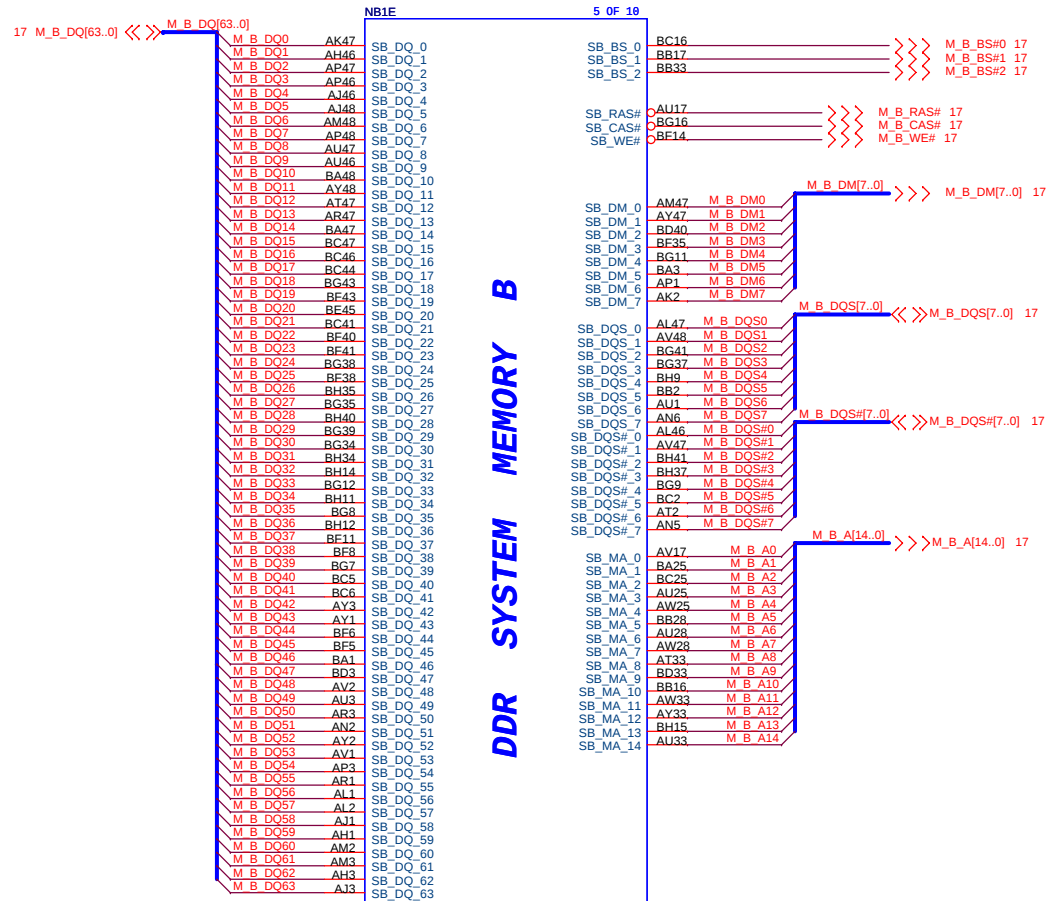
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Title			
<i>Cantiga (1 of 6)</i>			
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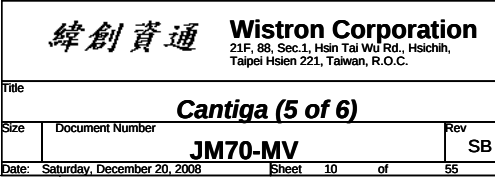


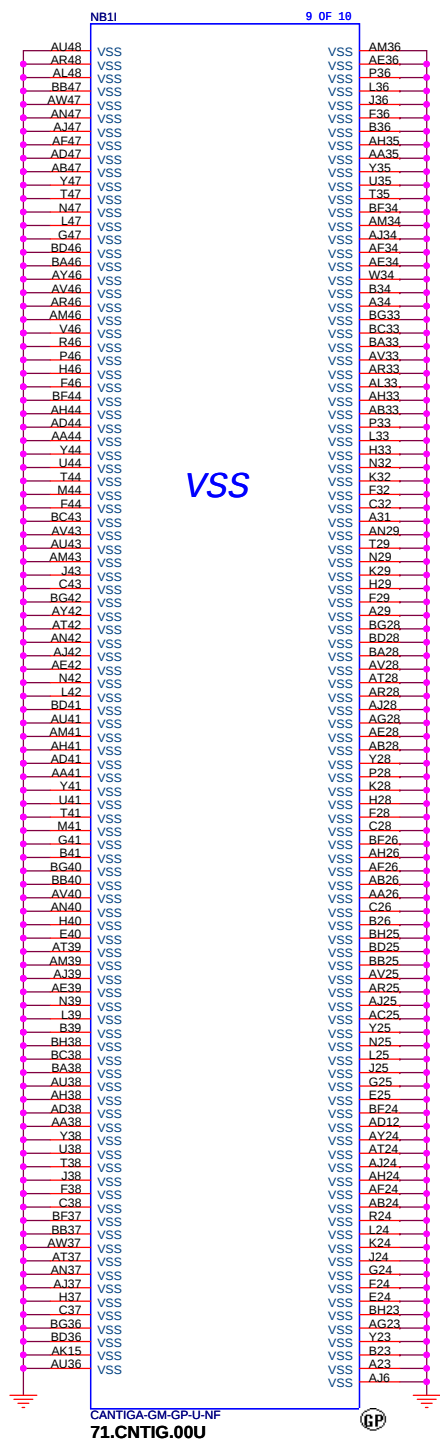
CANTIGA-GM-GP-U-NF
71.CNTIG.00U



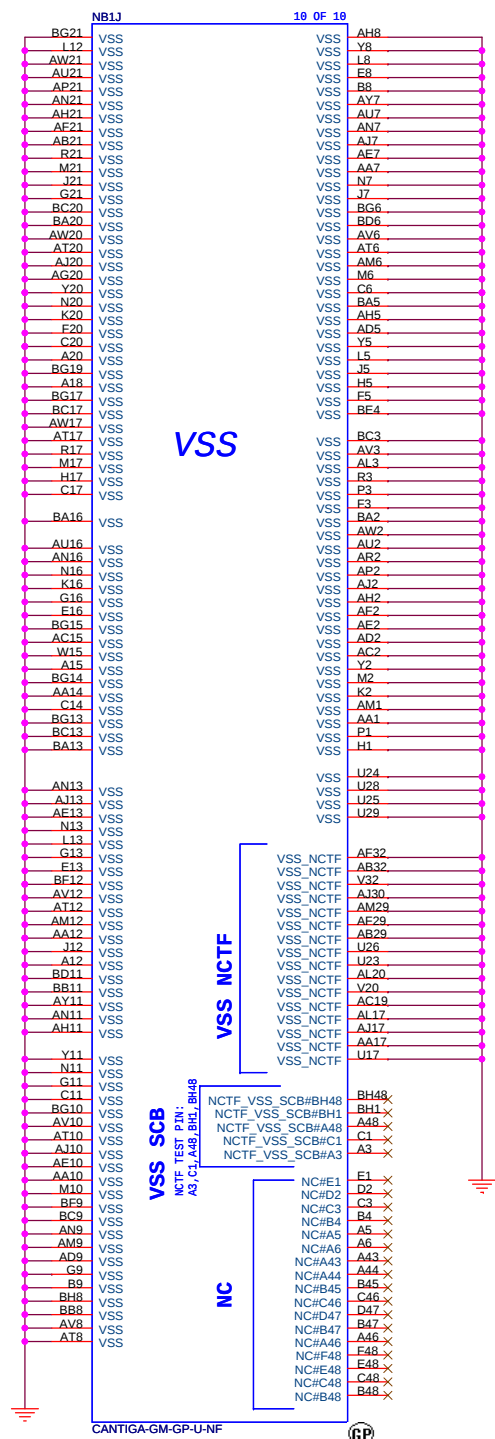
CANTIGA-GM-GP-U-NF
71.CNTIG.00U

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CANTIGA-GM-GP-U-NF
71.CNTIG.00U



CANTIGA-GM-GP-U-NF
71.CNTIG.00U



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Title

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Size

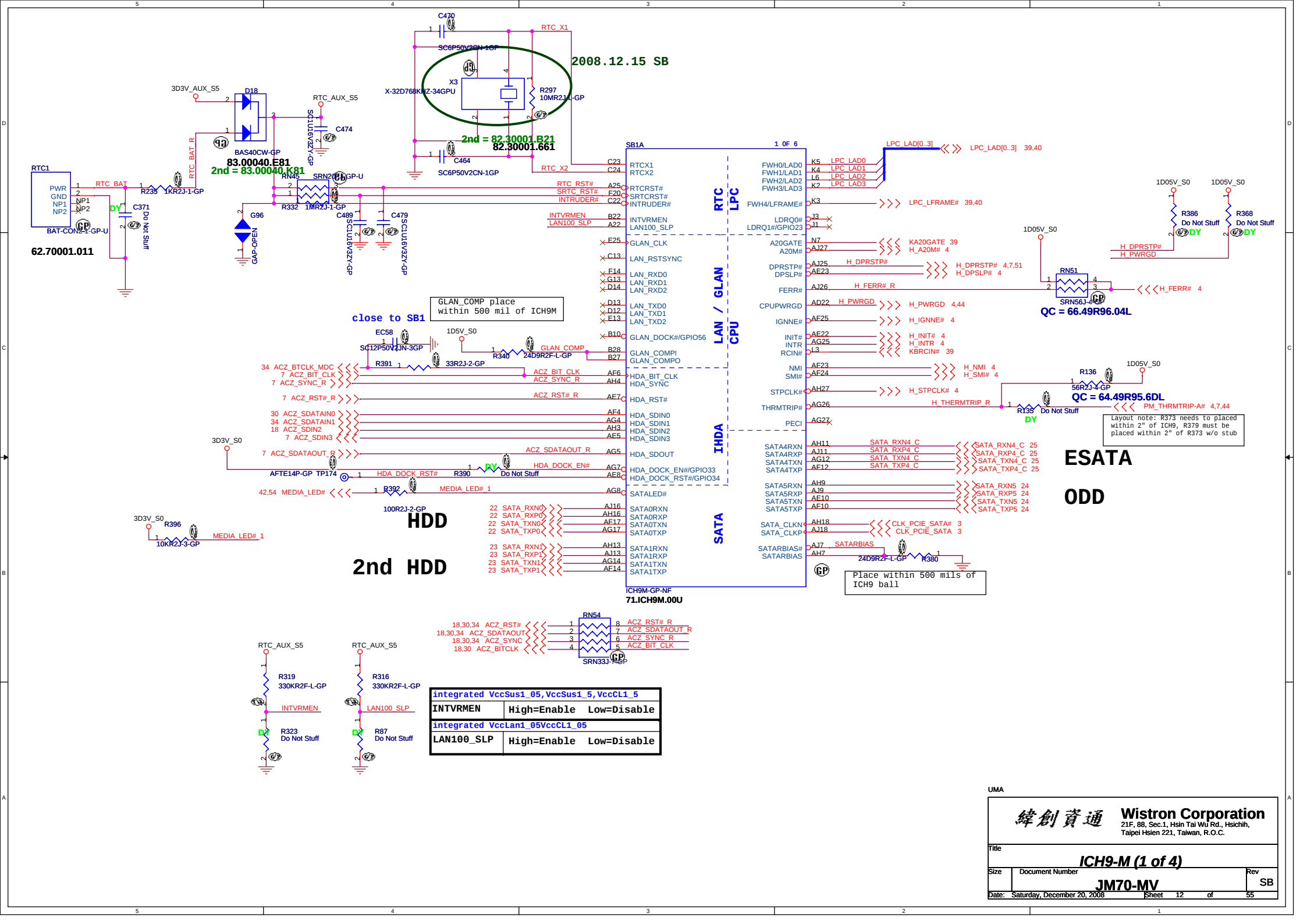
Document Number

Rev

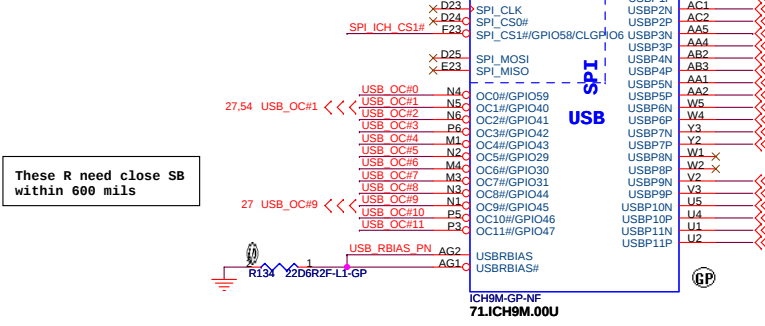
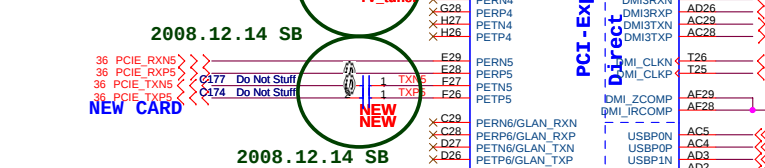
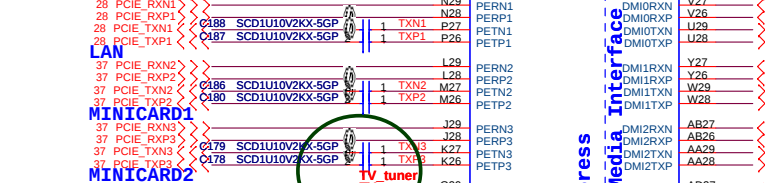
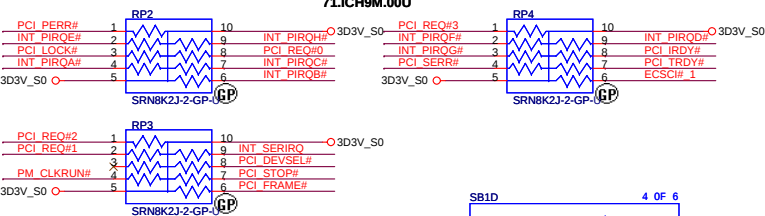
SB

Date: Saturday, December 20, 2008

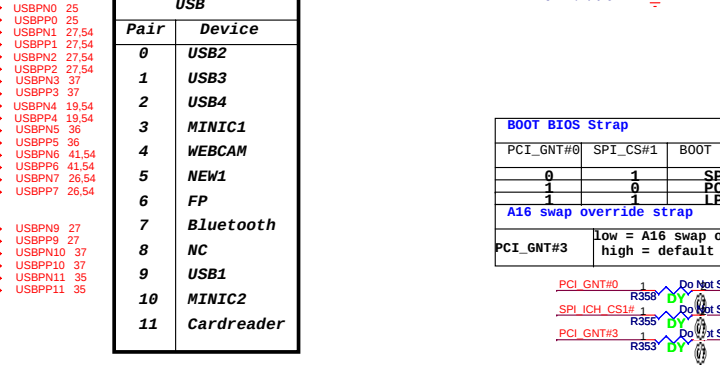
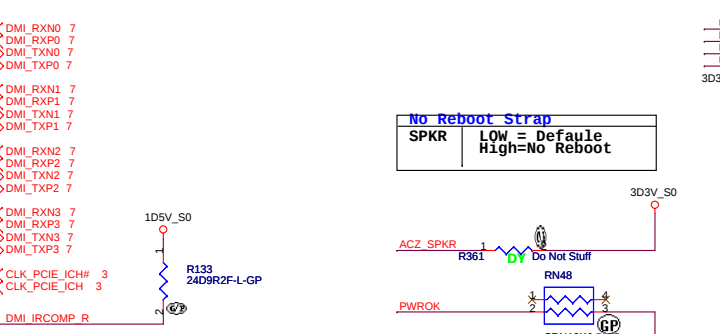
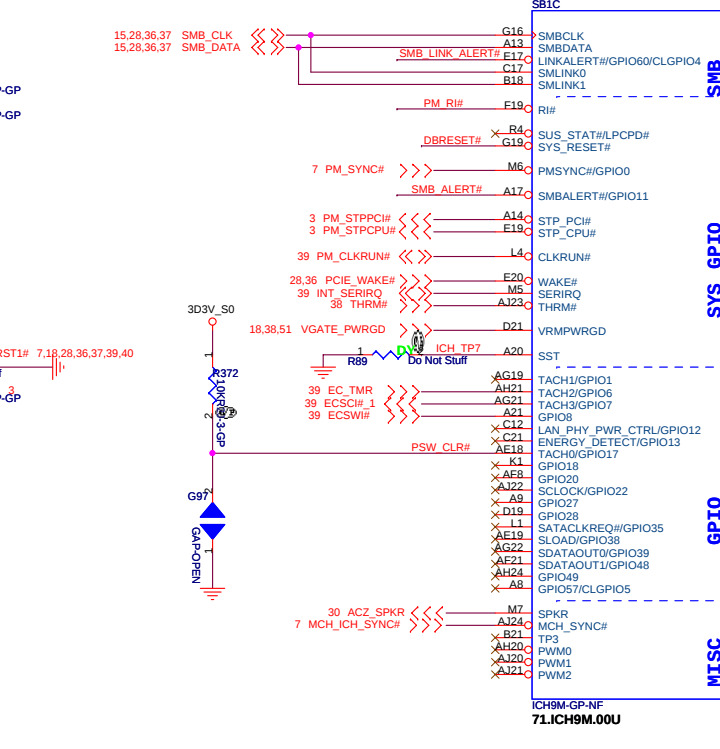
Sheet 11 of 55



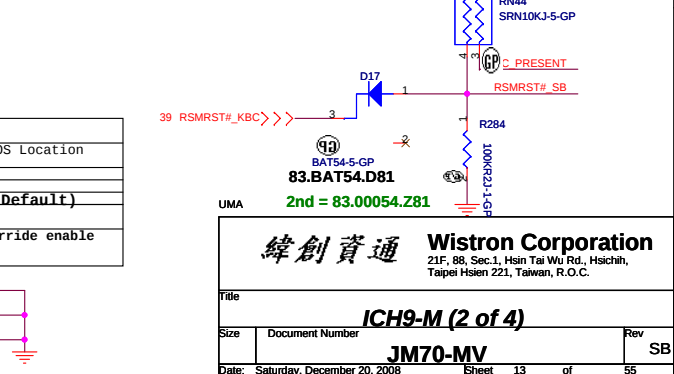
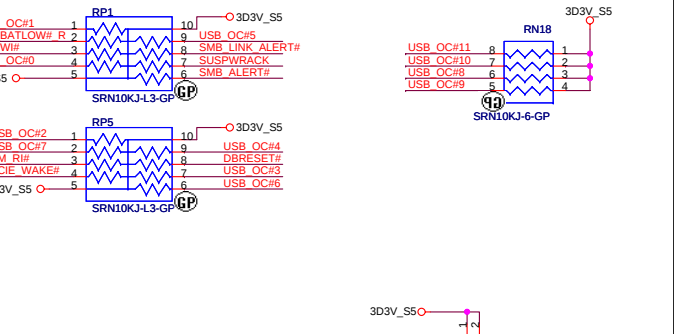
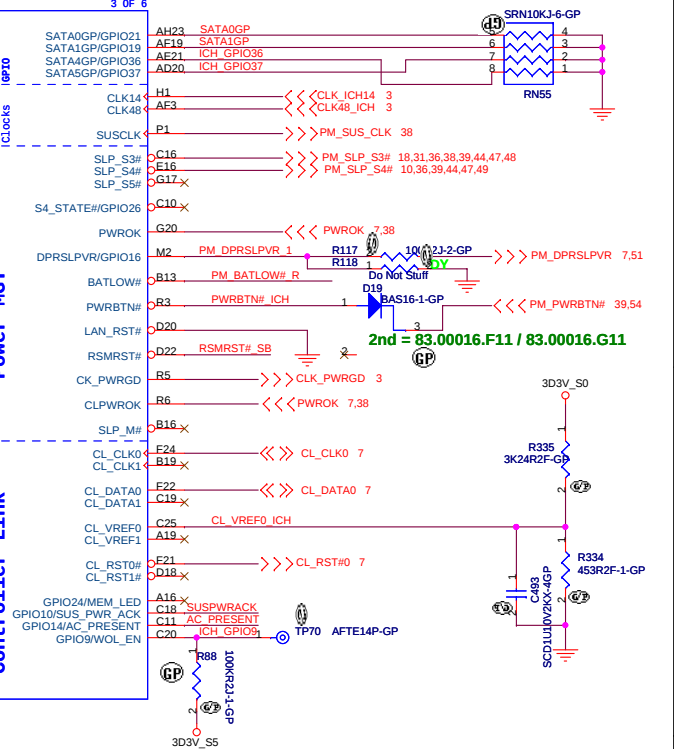
PCI_GNT#0 and SPI_CS1#
have weak internal Pull up



These R need close SB
within 600 mils



USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINIC1
4	WEBCAM
5	NEW1
6	FP
7	Bluetooth
8	NC
9	USB1
10	MINIC2
11	Cardreader



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	Low = A16 swap override enable high = default
-----------	--

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ICH9-M (2 of 4)
JM70-MV

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*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

2mA

2mA

47mA

1.64A

USBPLL=11mA

23mA

80mA

1mA

646mA

1.16A

41mA

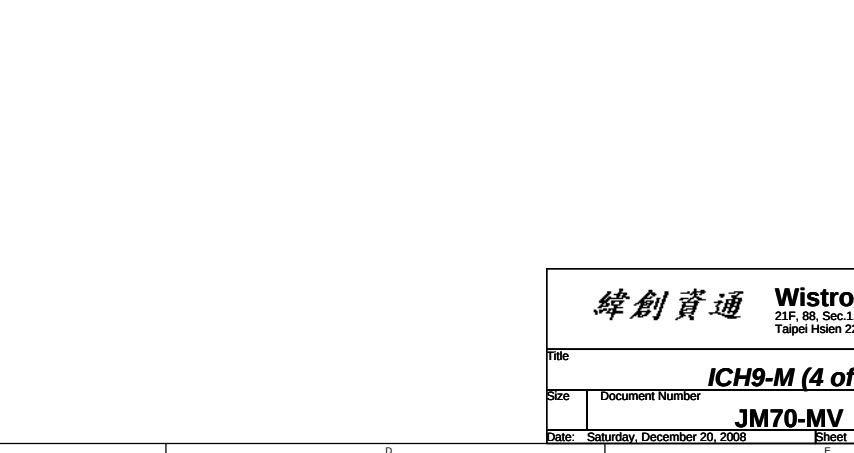
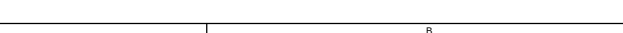
VCC3_3=308mA

32mA

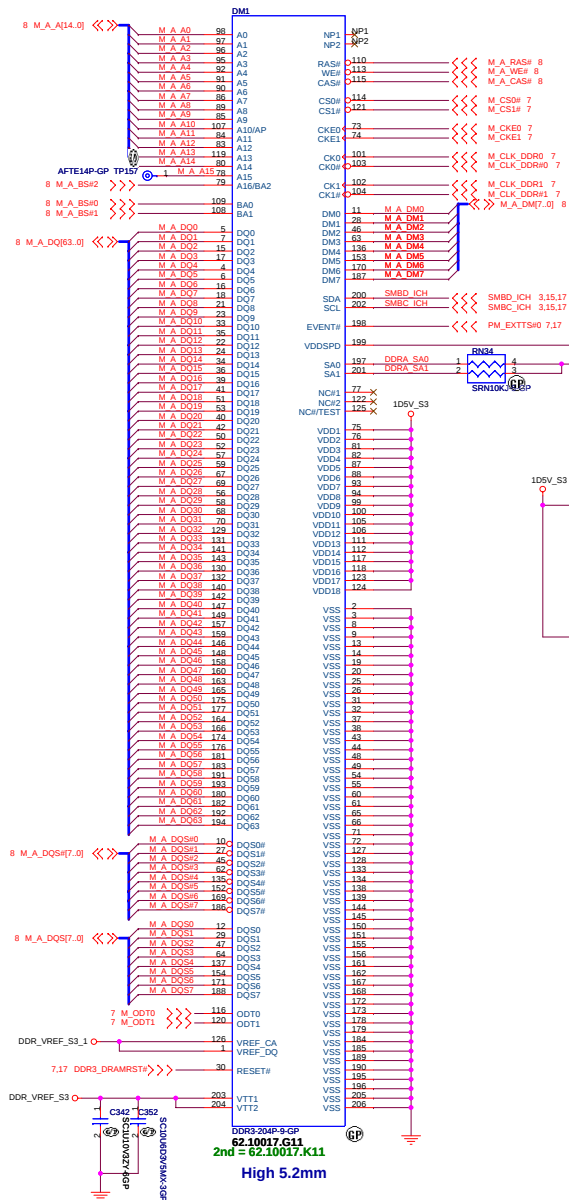
32mA

212mA

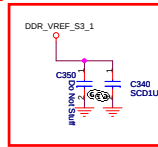
19mA



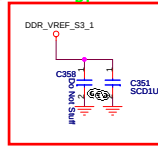
DDR3 SOCKET_1



Layout Note : Near Pin 126



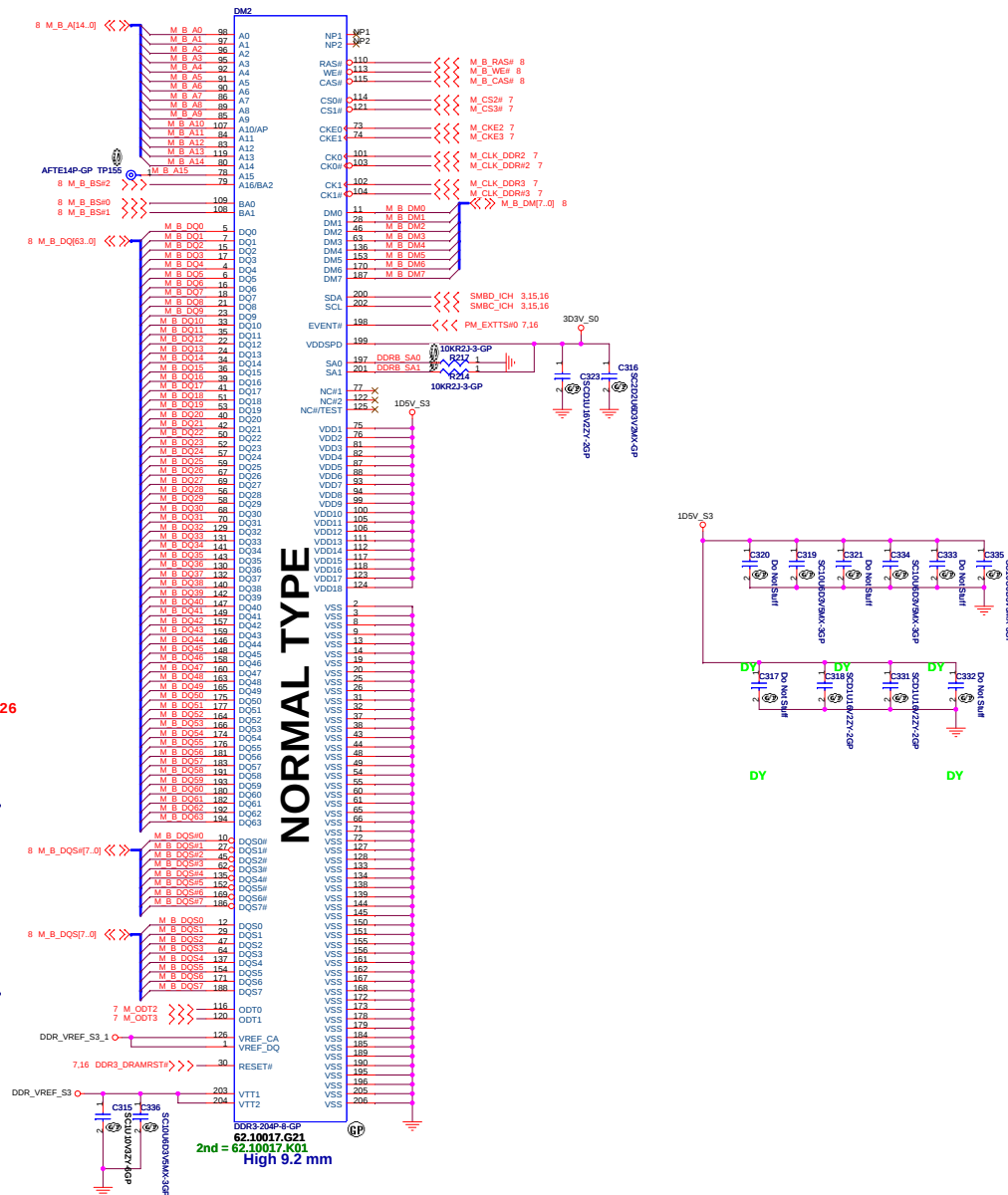
Layout Note : Near Pin 1



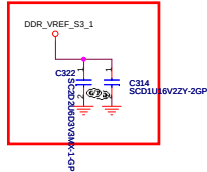
DY

 緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wai Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Size		Rev	
Document Number		DDR3 Socket	
		JM70-MV	
Date: Saturday, December 20, 2008		Sheet 16 of 55	

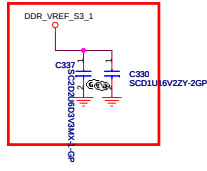
DDR3 SOCKET_2



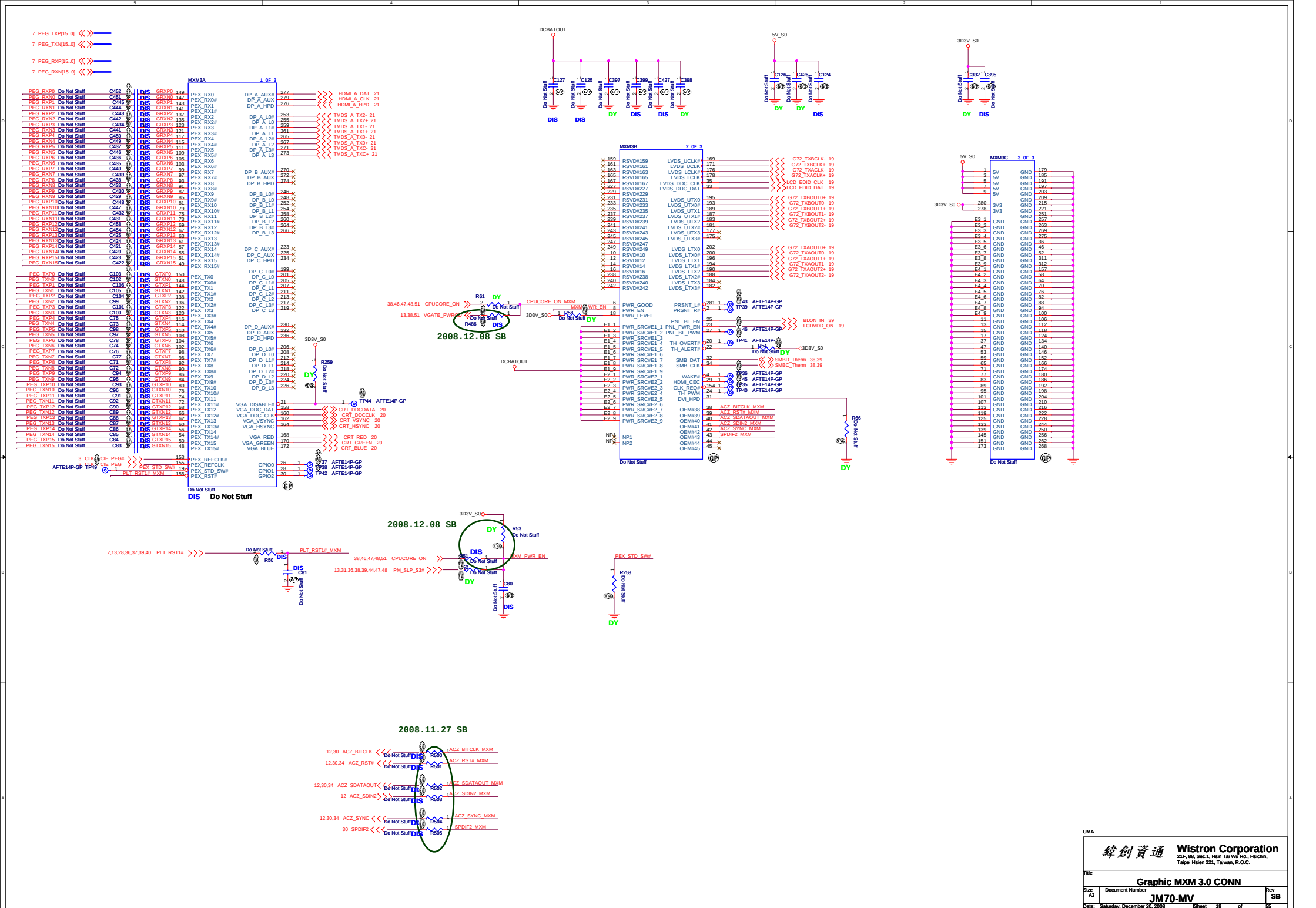
Layout Note : Near Pin 126



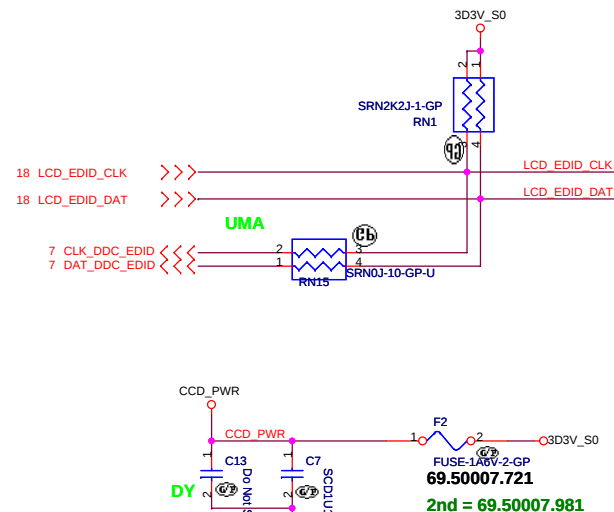
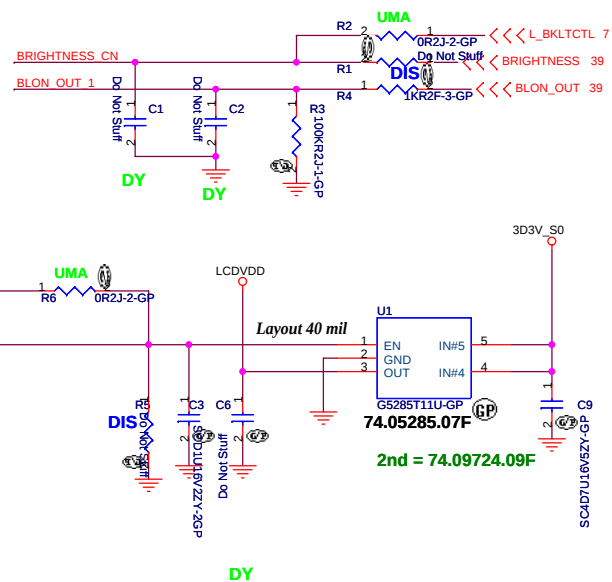
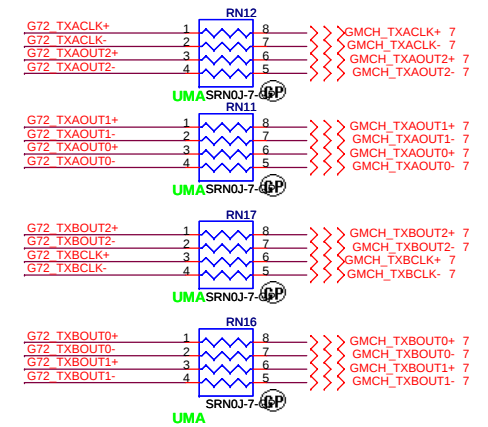
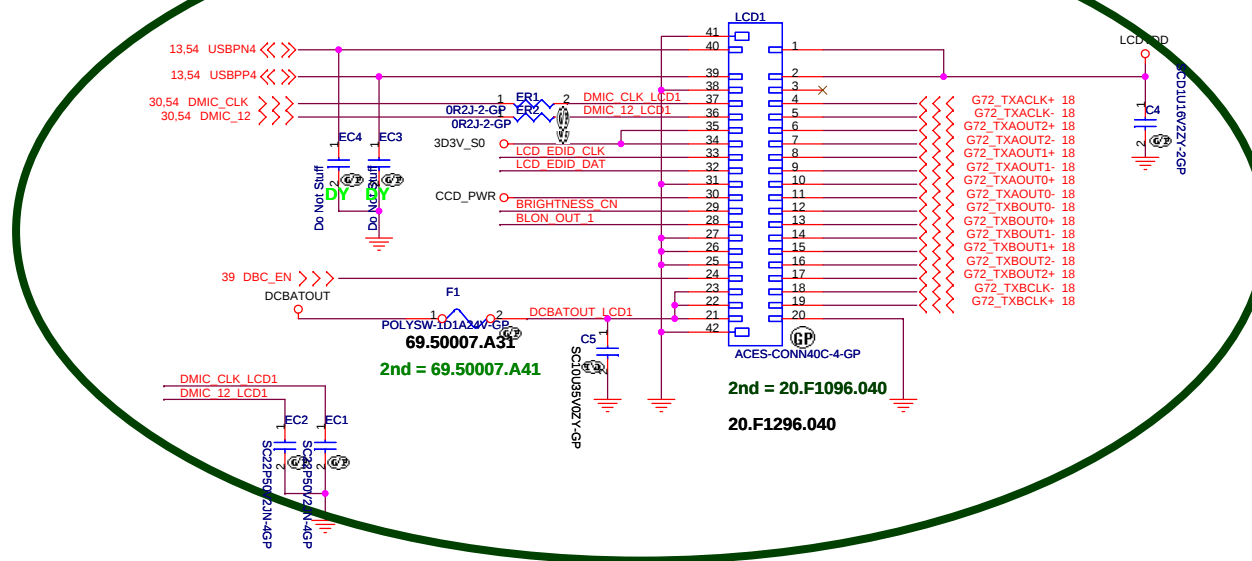
Layout Note : Near Pin 1



NORMAL TYPE



2008.12.16 SB

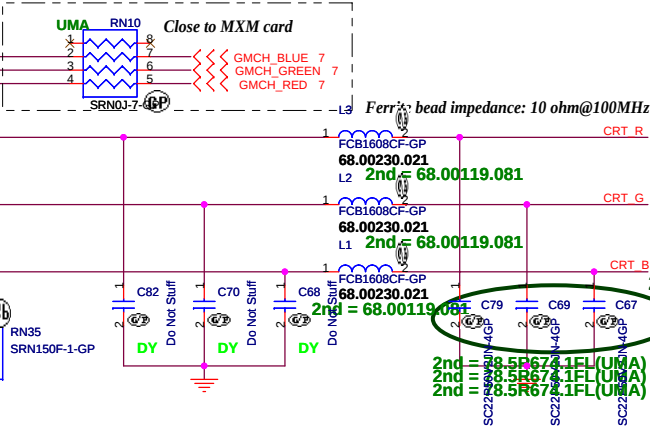


UMA

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

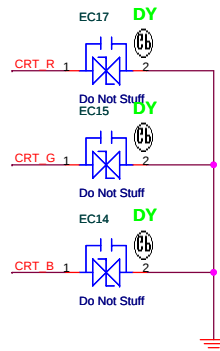
LCD CONN			
Size	Document Number	Rev	
		JM70-MV	
Date: Saturday, December 20, 2008	Sheet	19	of 55

Layout Note:
Place these resistors
close to the CRT-out
connector

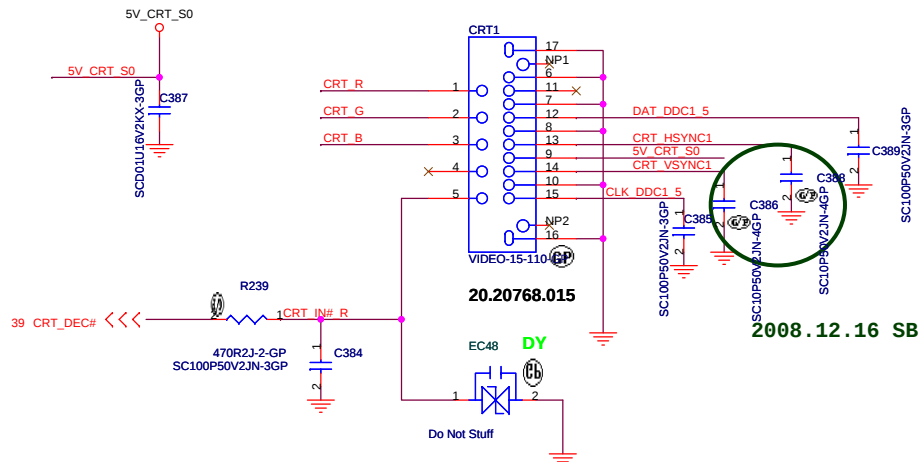


Layout Note:

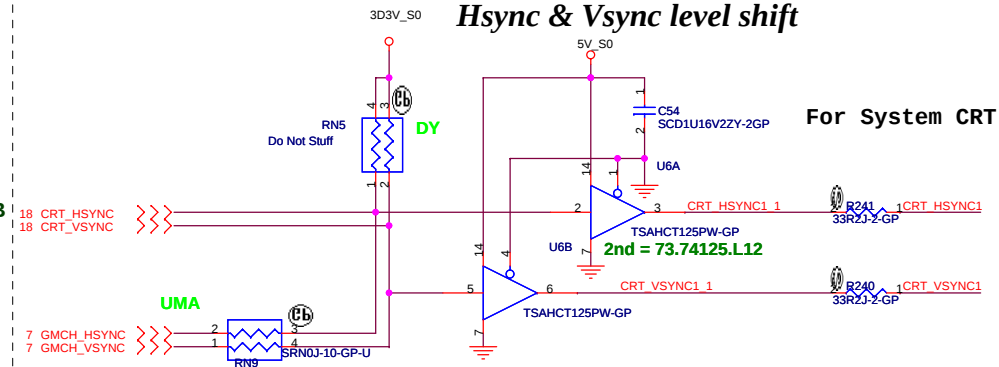
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



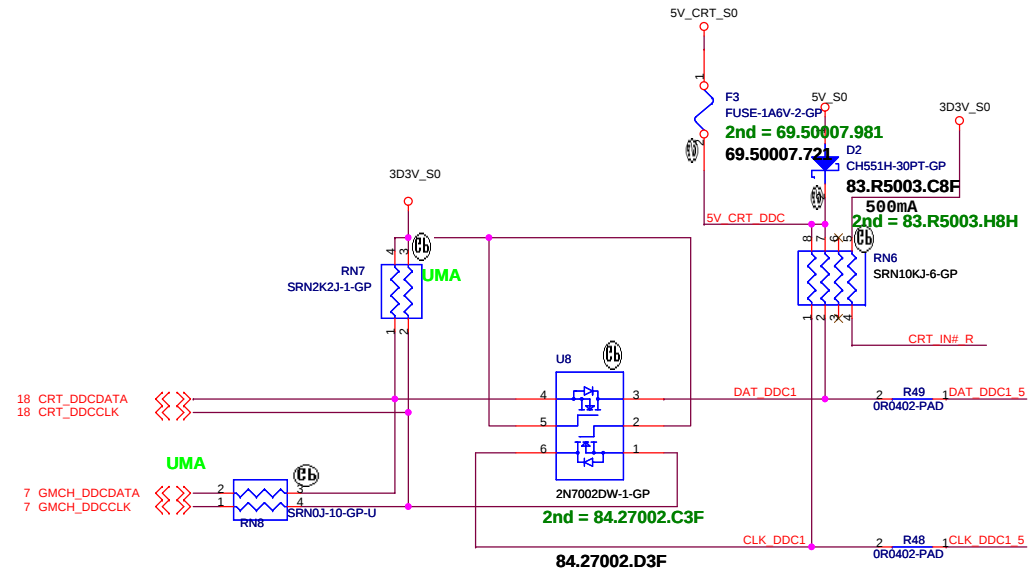
CRT I/F & CONNECTOR



Hsync & Vsync level shift



DDC_CLK & DATA level shift

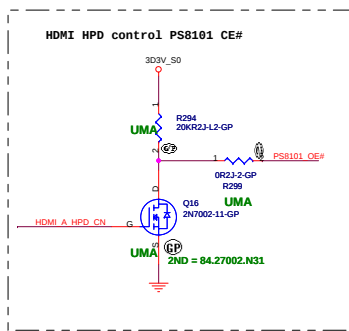
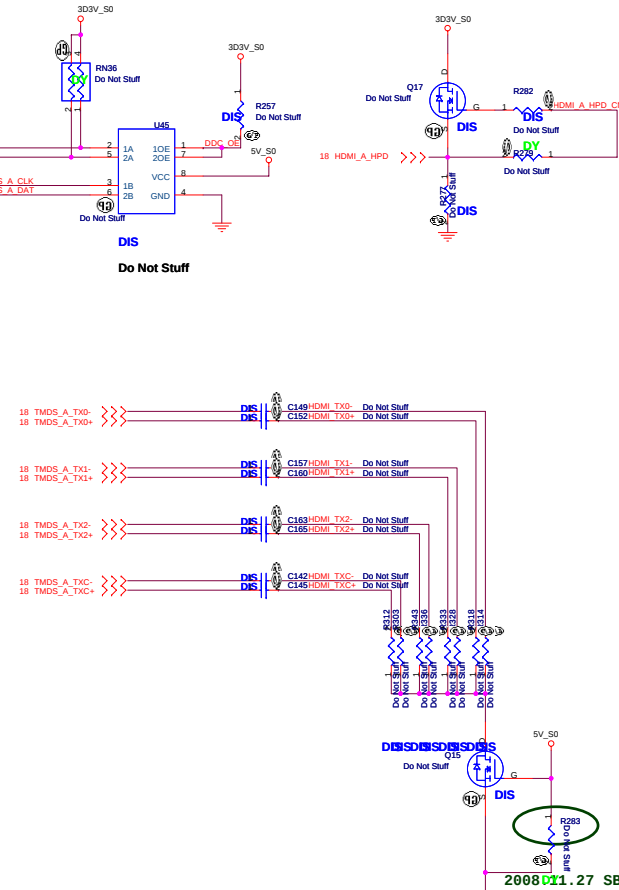
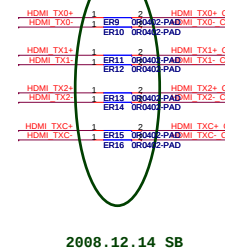
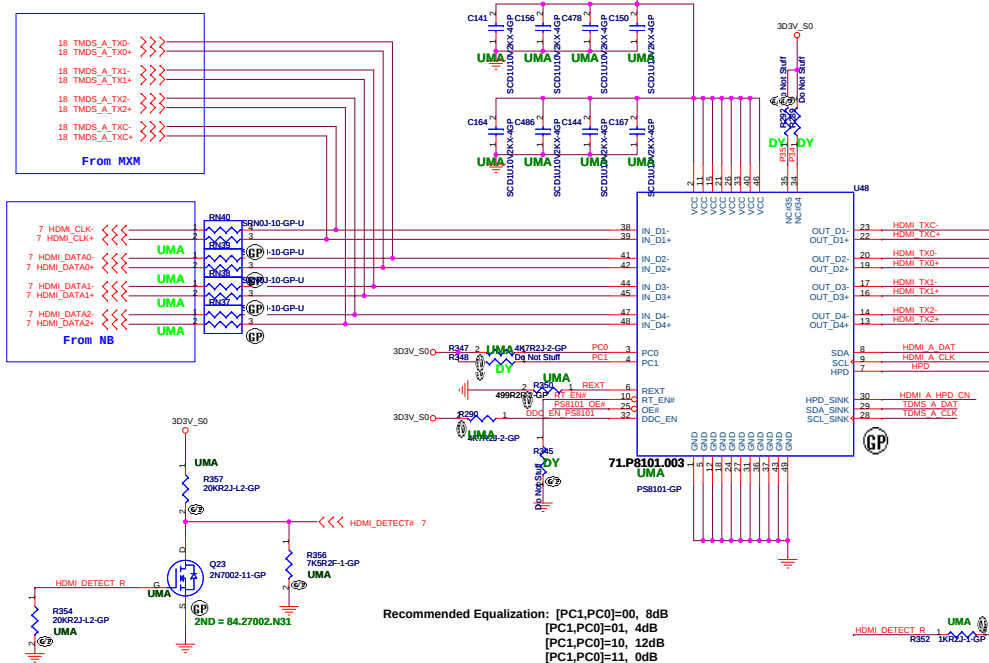
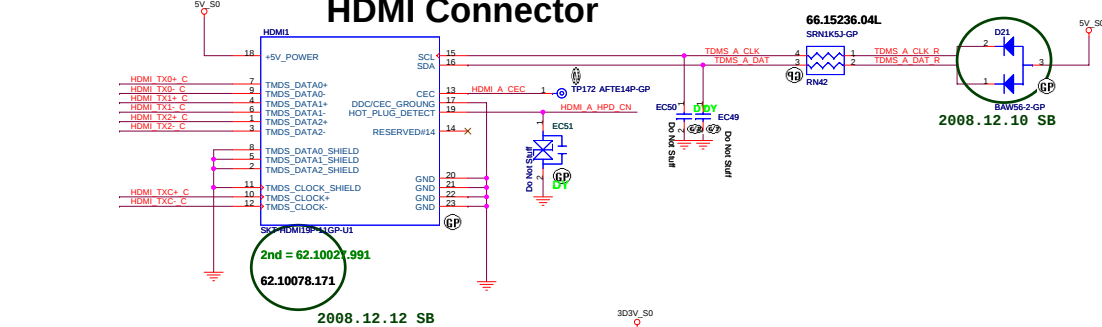


UMA

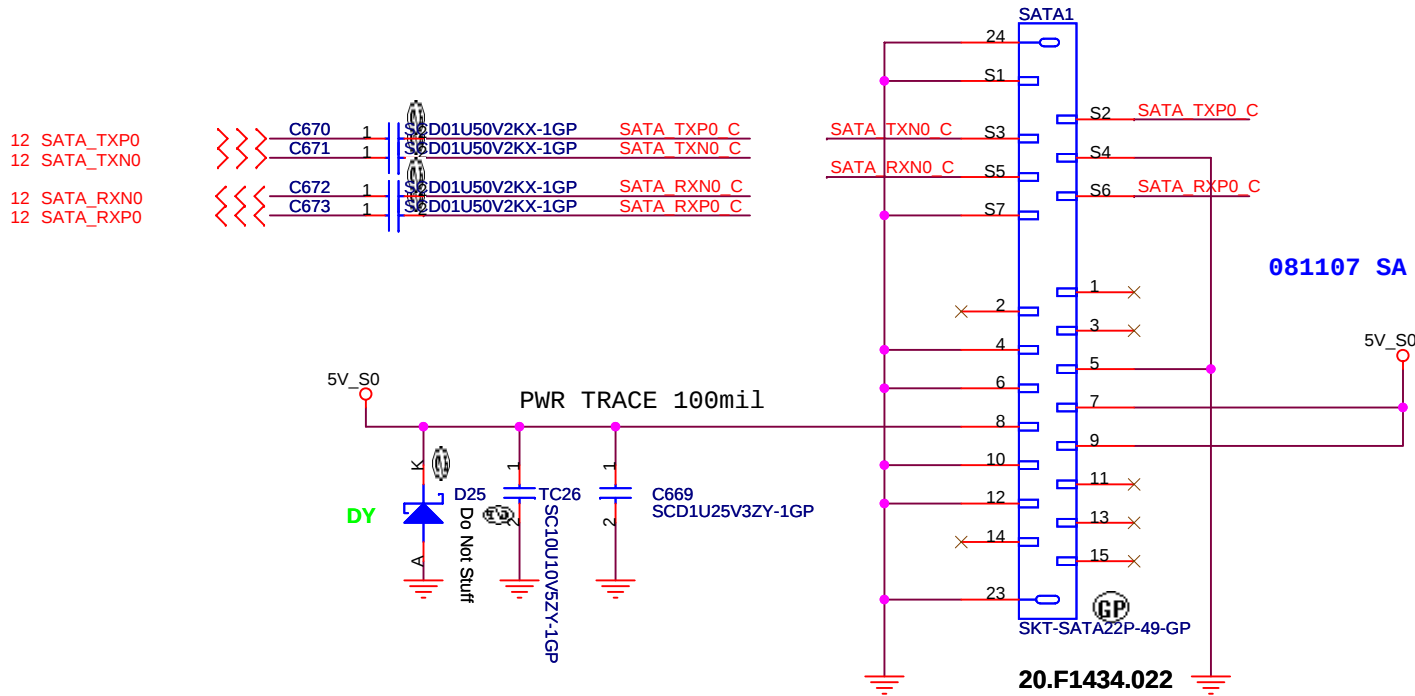
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CRT CONN			
Size	Document Number		Rev
	JM70-MV		SE
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HDMI Connector



SATA Connector

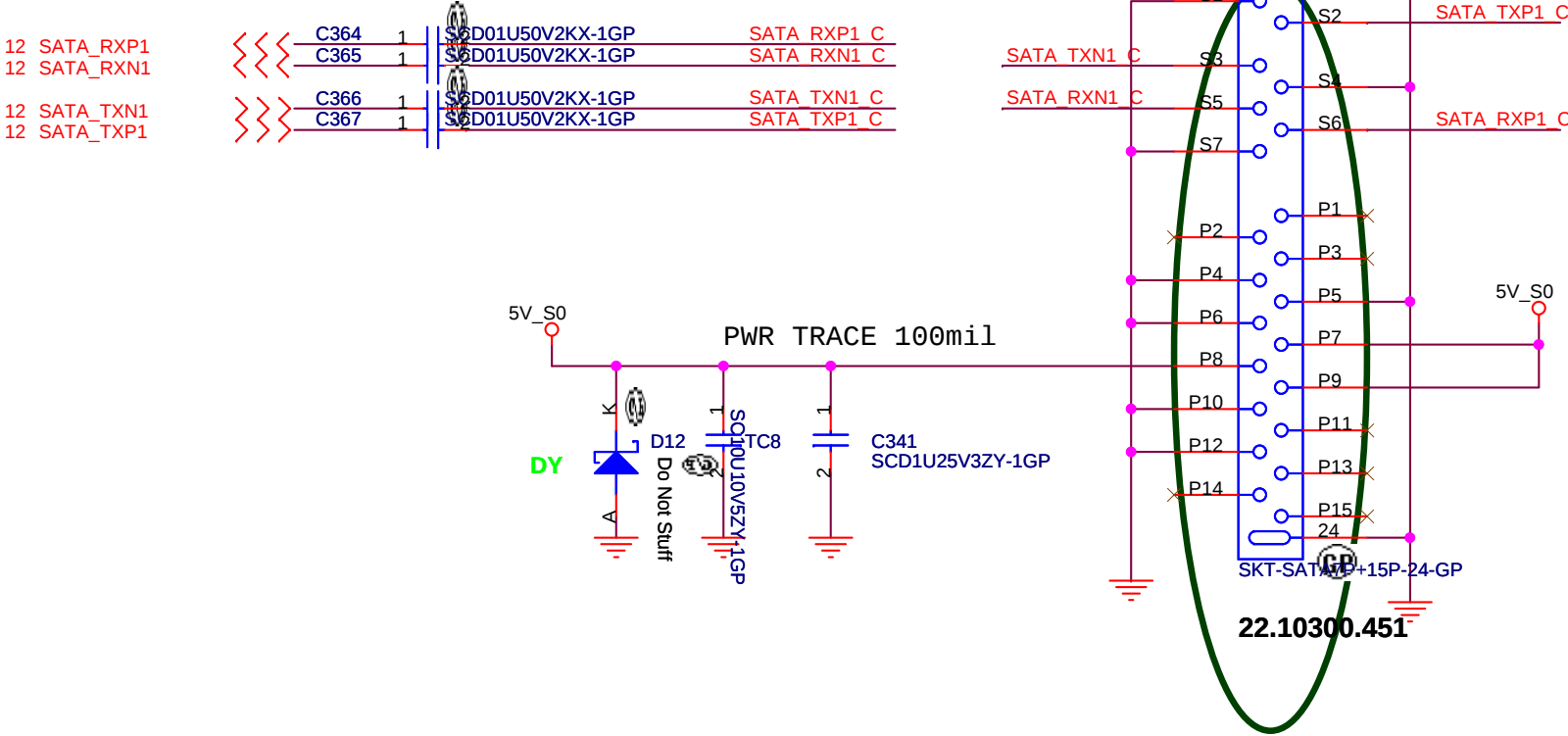


UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
HDD CONN			
Size	Document Number		Rev
	JM70-MV		SB
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2nd HDD SATA Connector

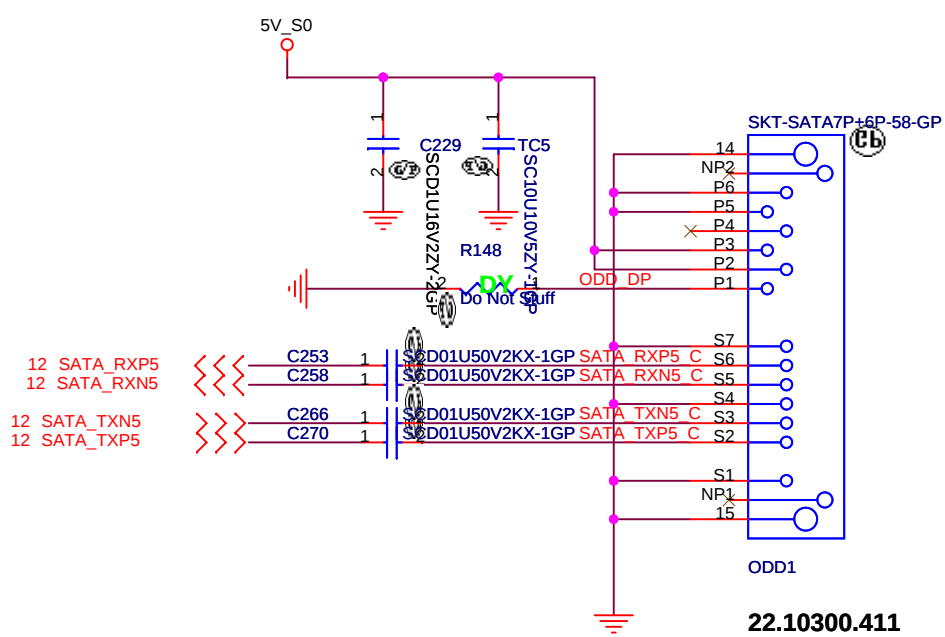
2008.12.12 SB



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緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
2nd HDD			
Size	Document Number		Rev
	JM70-MV		SB
Date:	Saturday, December 20, 2008	Sheet	23 of 55

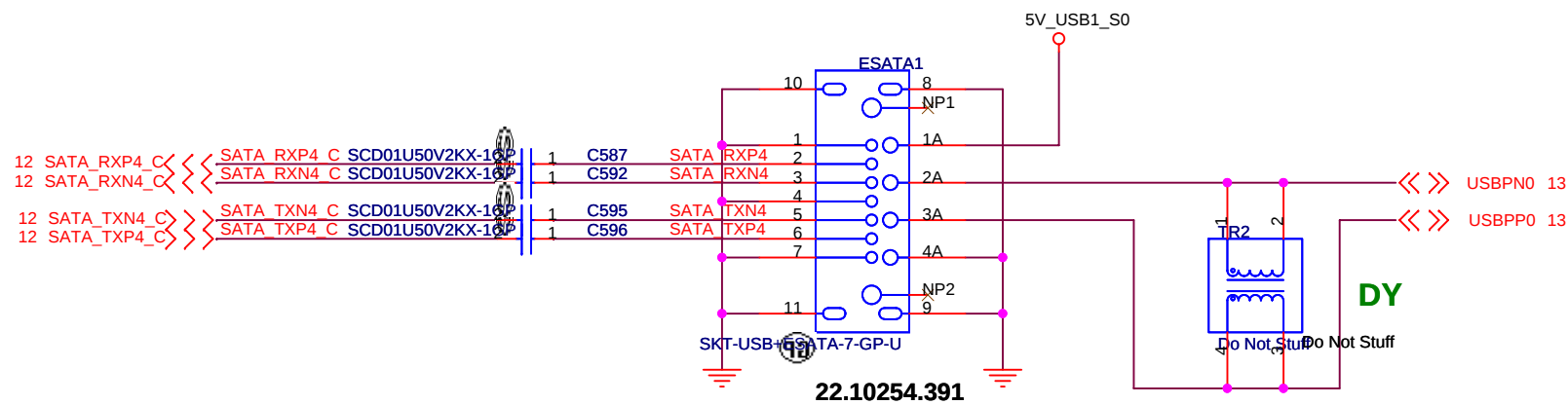
ODD Connector



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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ODD			
Size	Document Number		Rev
	JM70-MV		SB
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ESATA Connector



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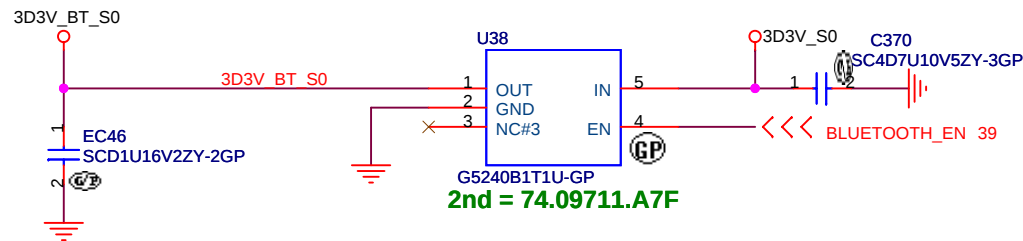
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ESATA
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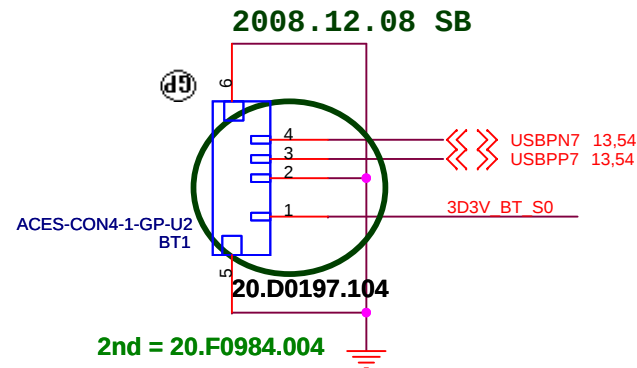
Size A4	Document Number JM70-MV	Rev SB
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BLUETOOTH MODULE



EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



UMA

緯創資通

Wistron Corporation

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Title

BLUETOOTH

Size

Document Number

JM70-MV

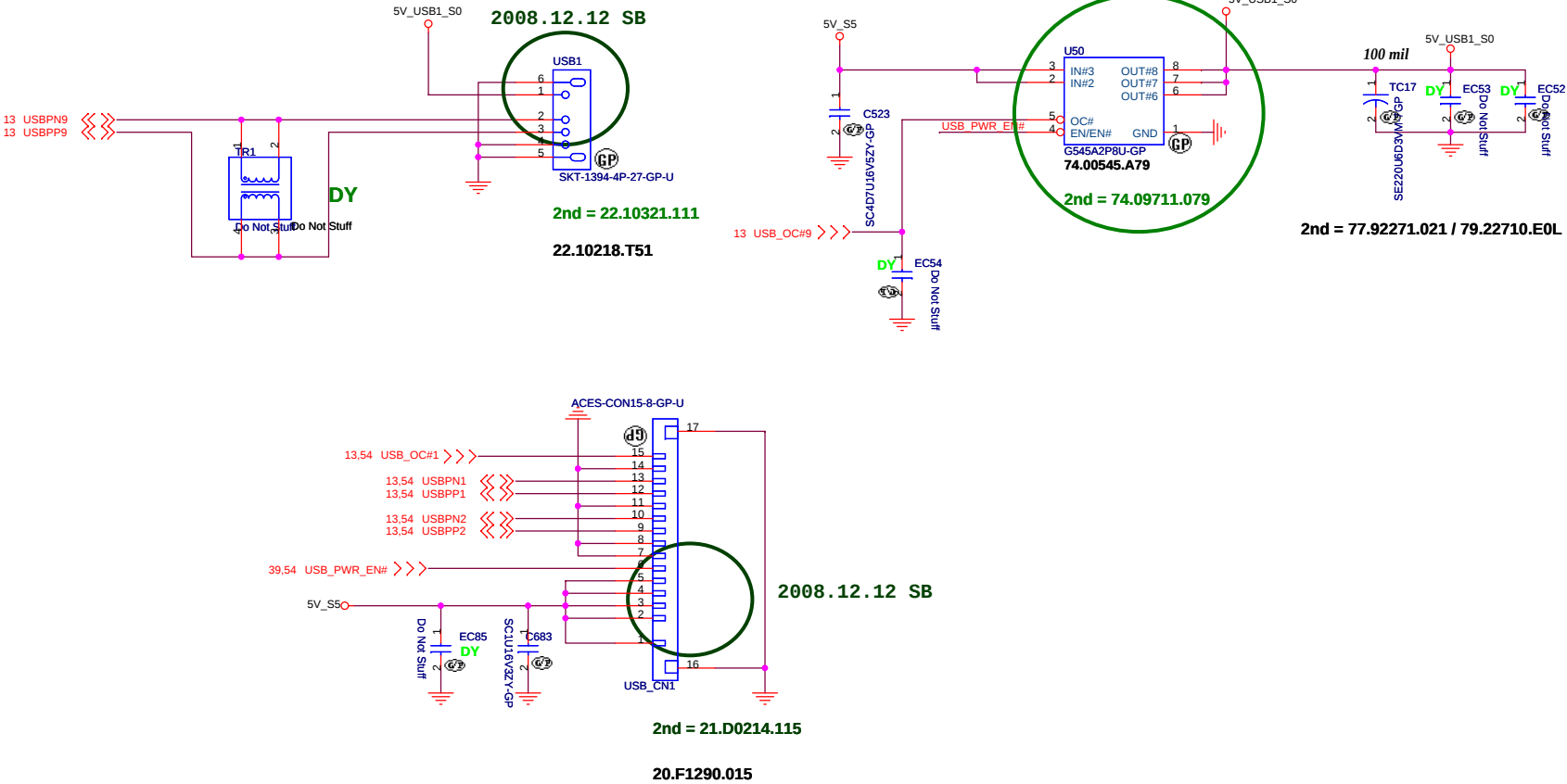
Rev

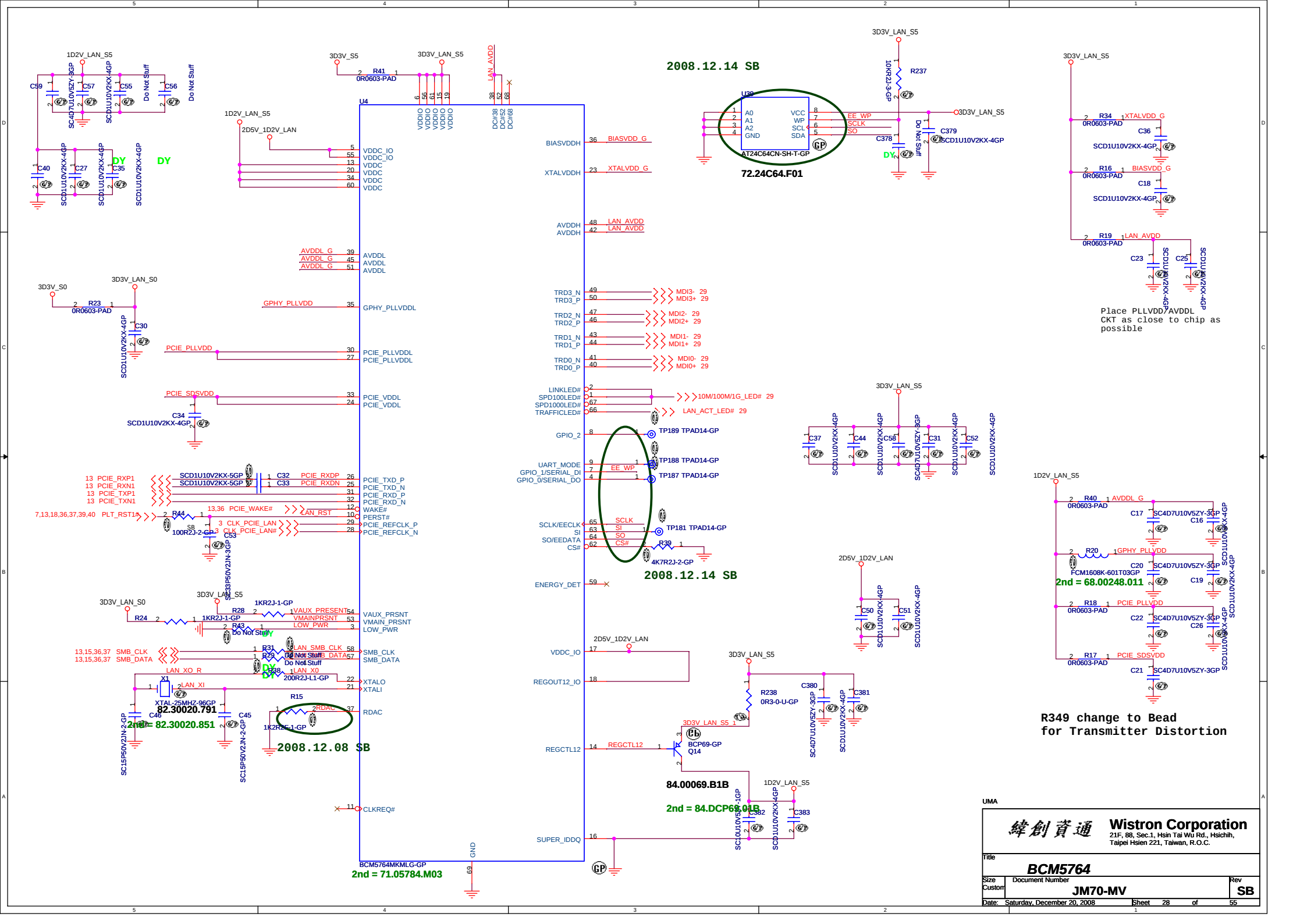
SB

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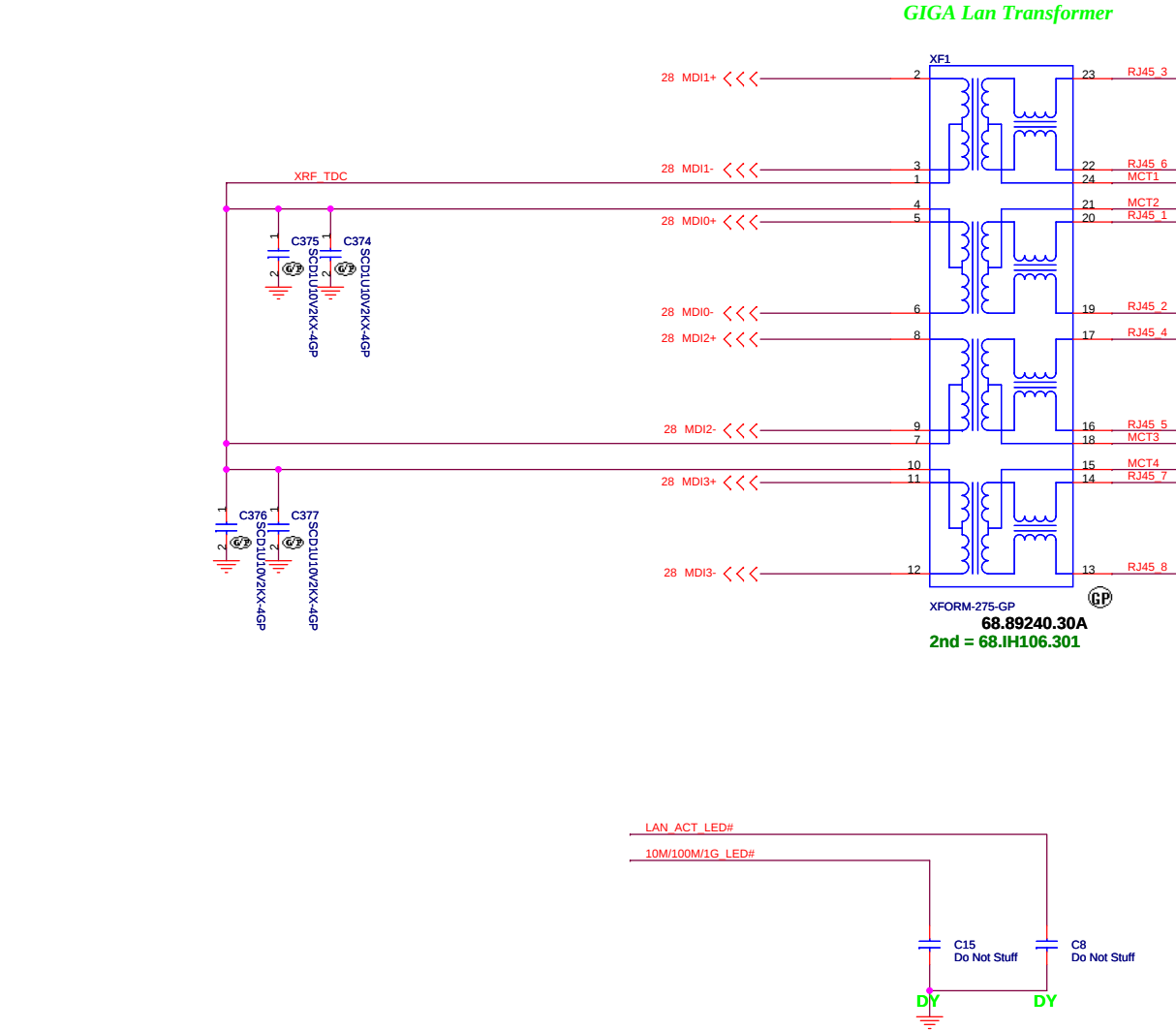
USB1 Connector



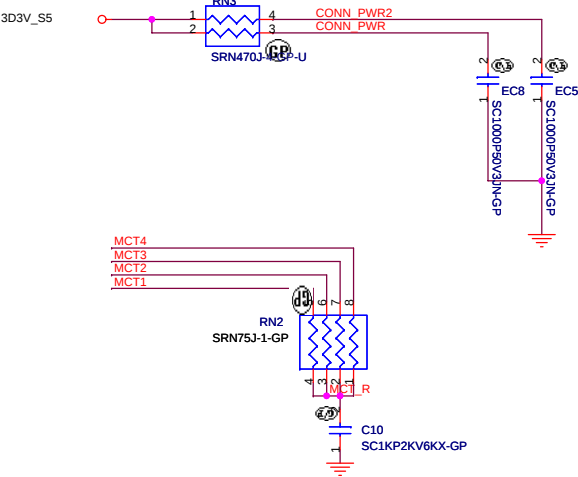
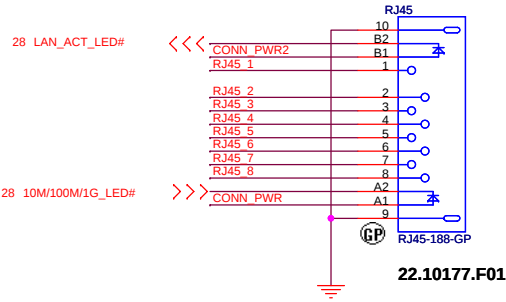


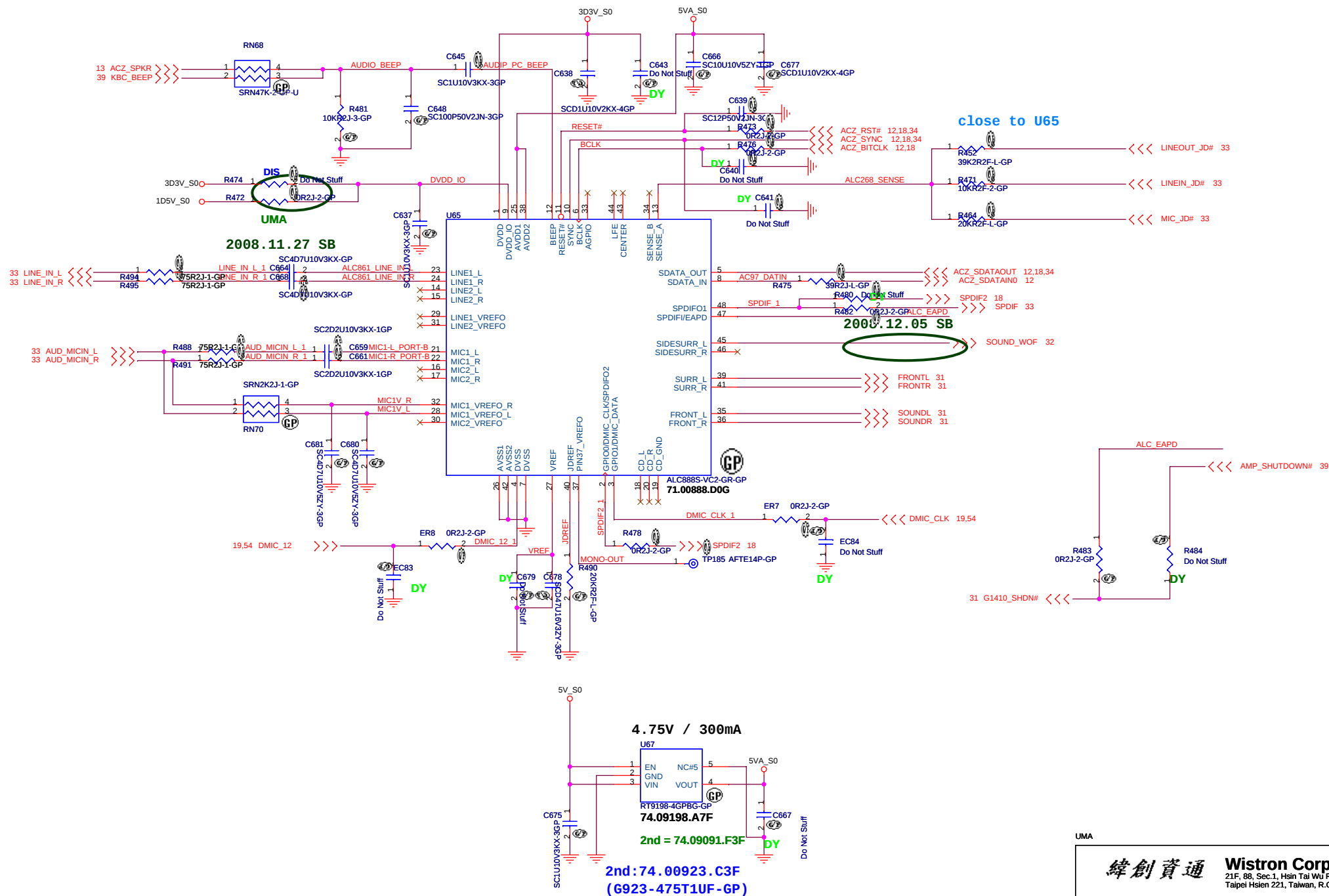
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector



LAN Connector





UMA

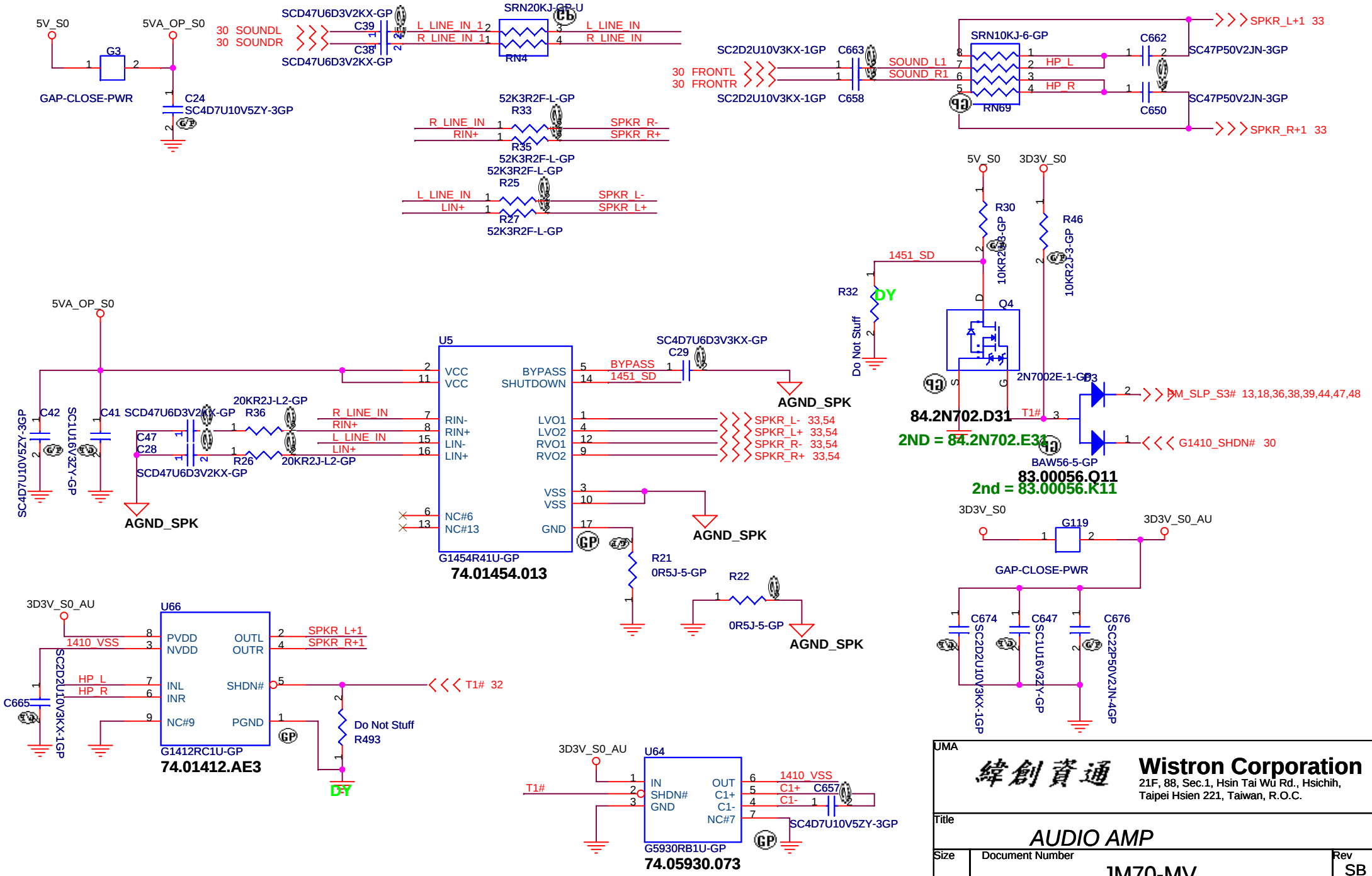
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Azalia codec ALC888**

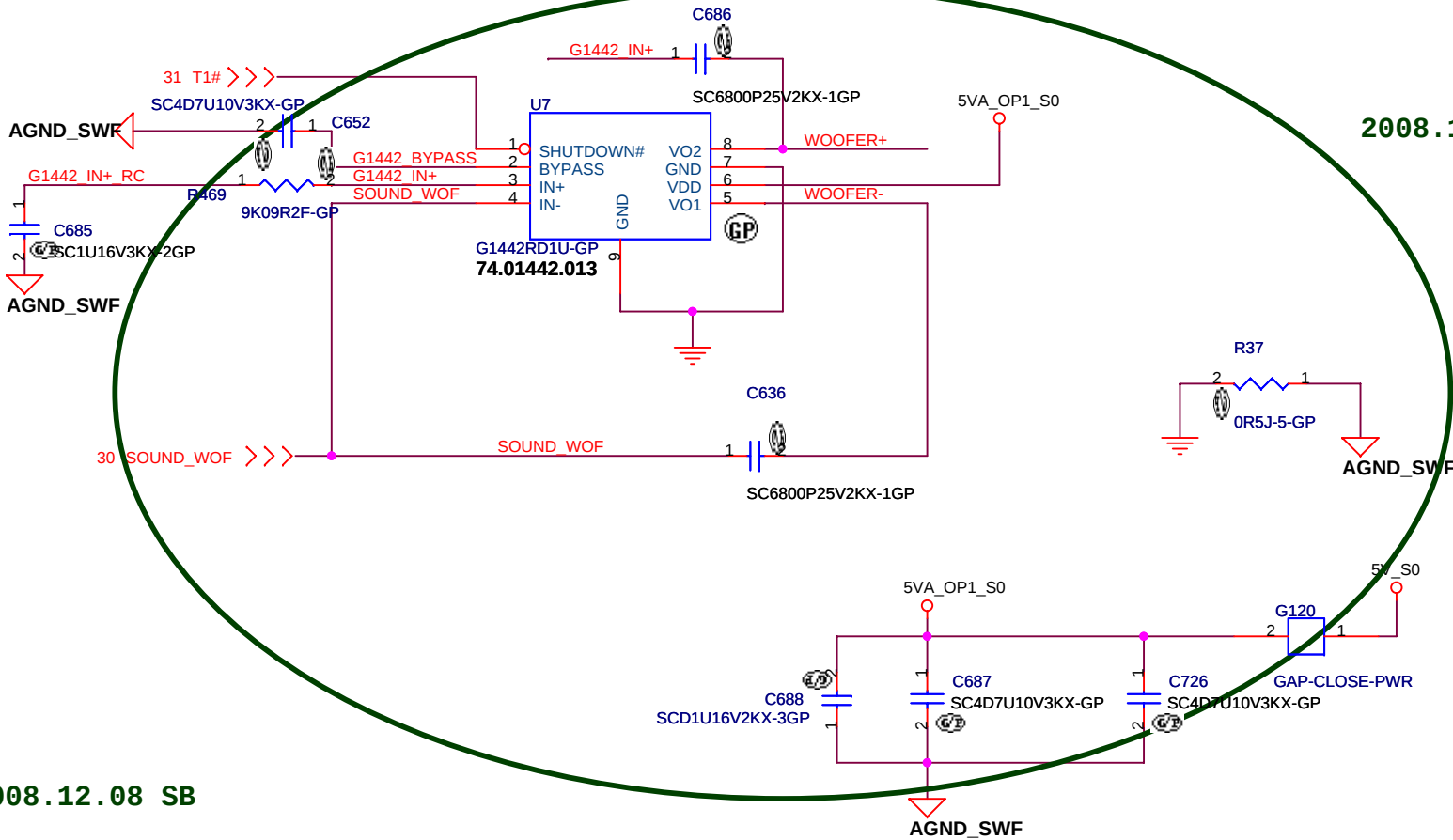
Size A3	Document Number JM70-MV	Rev SB
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AUDIO OP AMPLIFIER

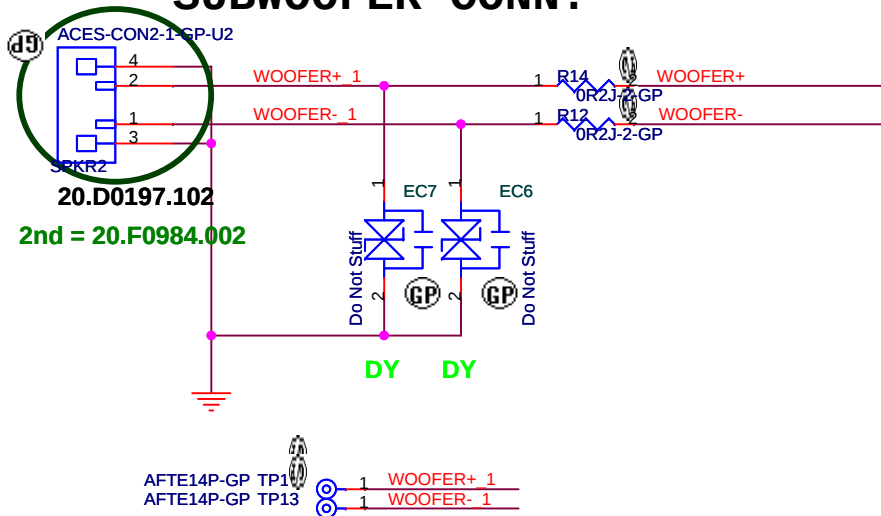


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title AUDIO AMP	
Size Document Number	Rev SB
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2008.12.08 SB

SUBWOOFER CONN.

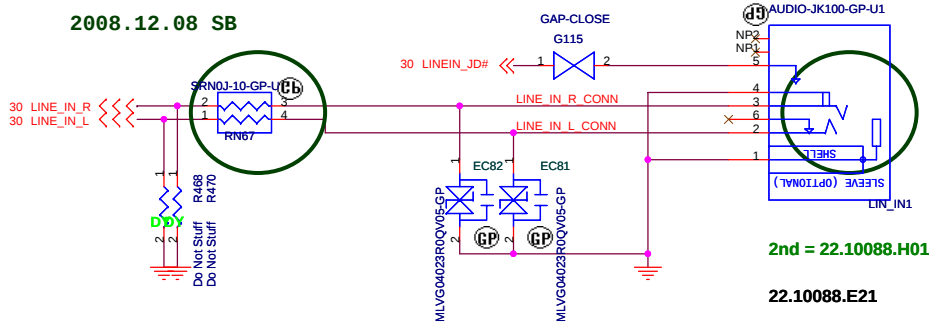


UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
SUBWOOFER CONN.	
Size	Document Number
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	Rev SB

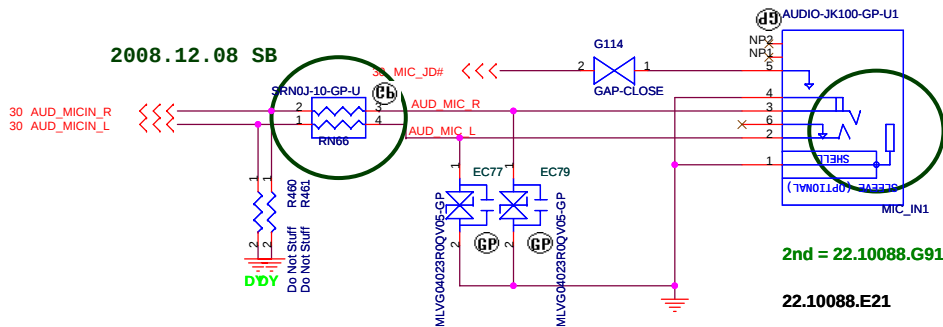
LINE IN

2008.12.08 SB



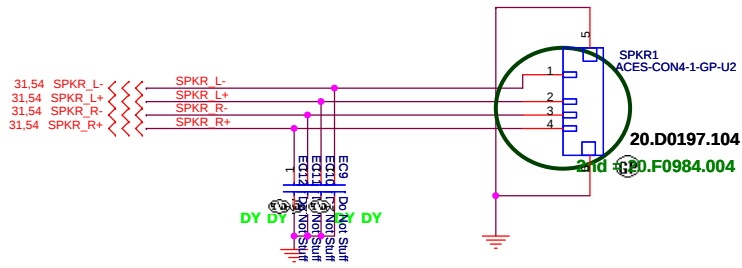
MIC IN

2008.12.08 SB



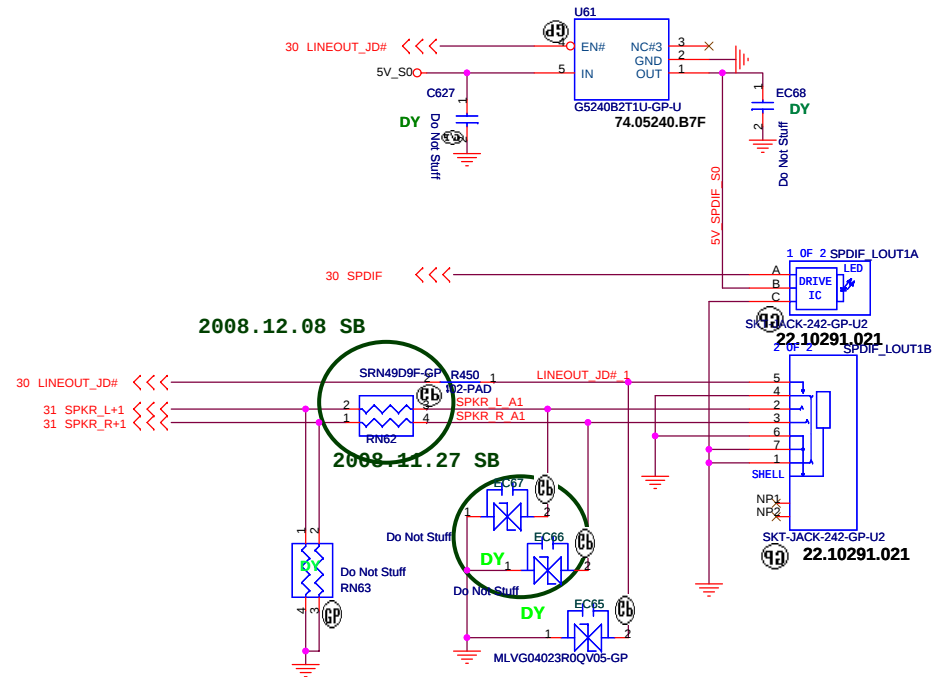
Internal Speaker

2008.12.08 SB



LINE OUT / SPDIF

2008.12.08 SB

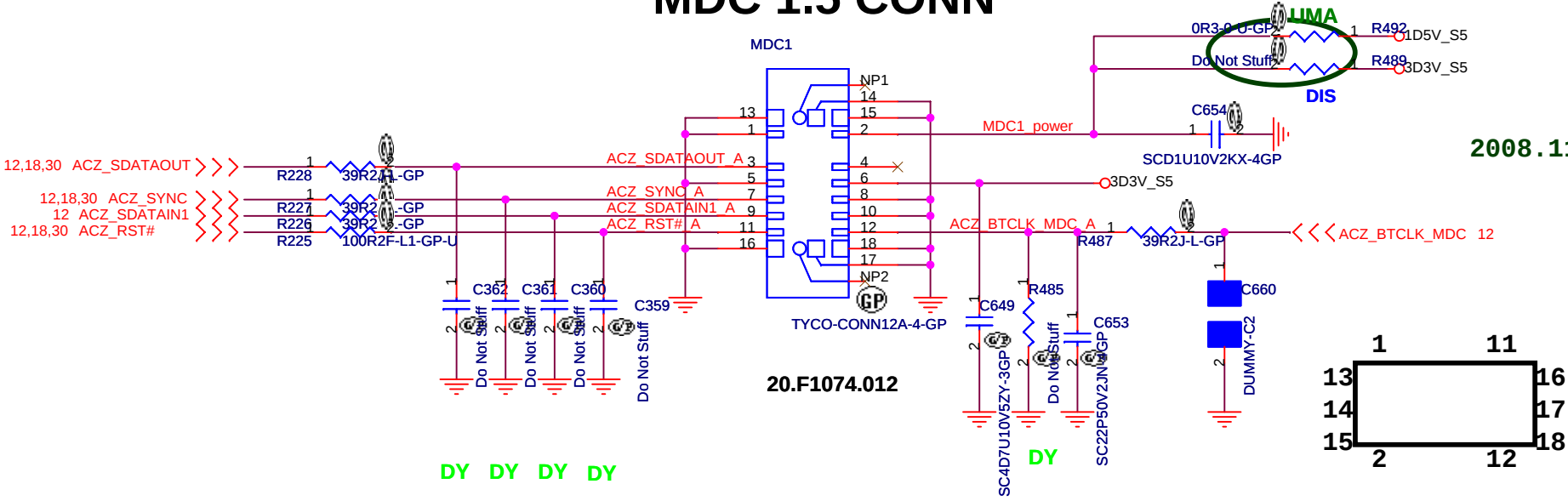


2008.11.27 SB

UMA

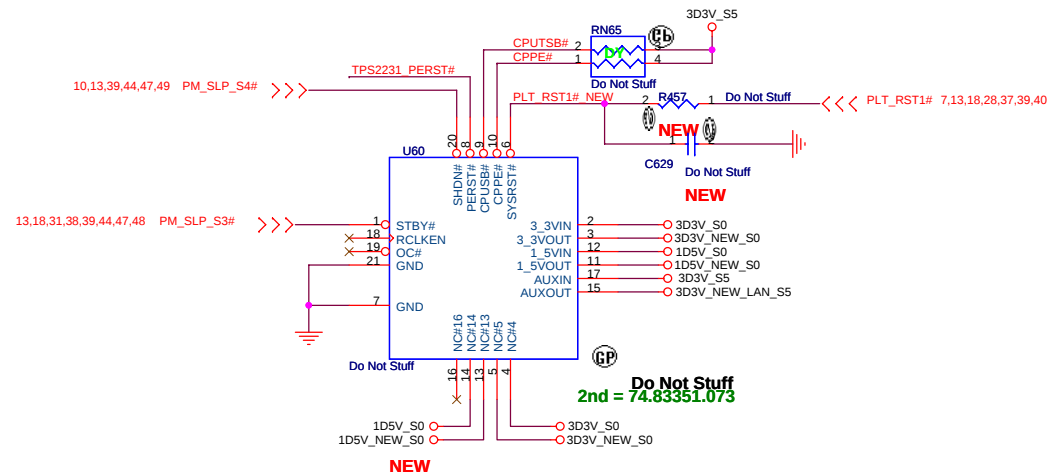
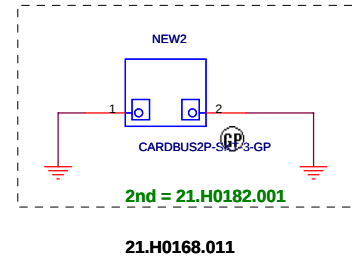
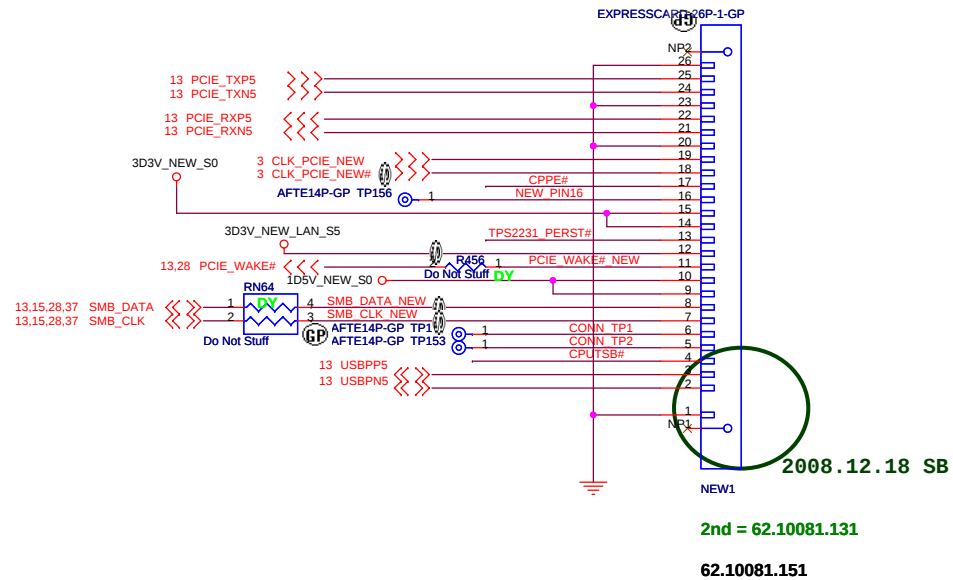
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AUDIO jack			
Size	Document Number		Rev
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MDC 1.5 CONN

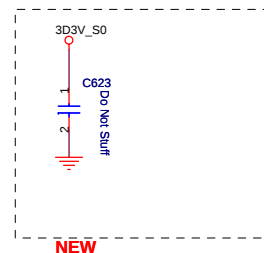


2008.11.27 SB

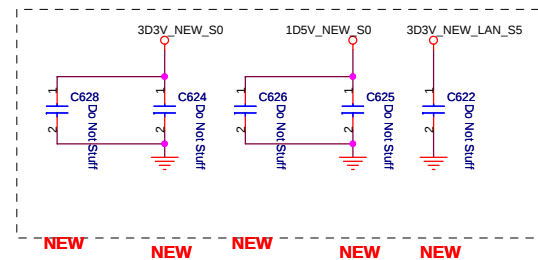
UMA



Place them Near to Chip



Place them Near to Connector

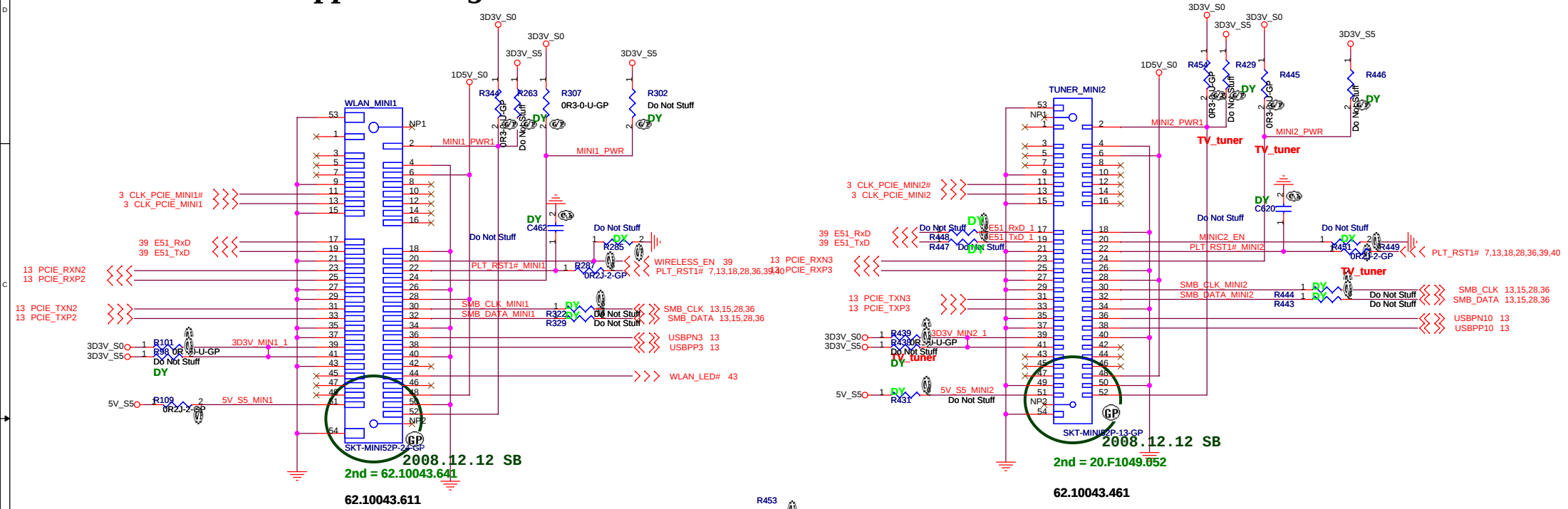


UMA

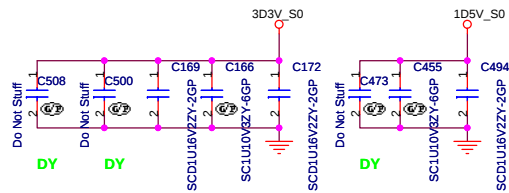
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
NEW CARD		Size	
Document Number		Rev	
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Mini1 Card Connector(WLAN) Support debug-card

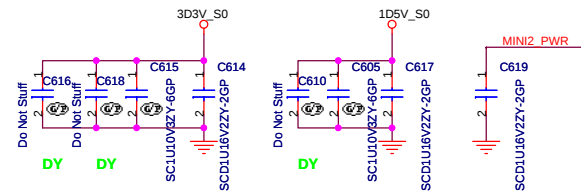
Mini2 Card Connector(TV tuner)



Place near MINI1

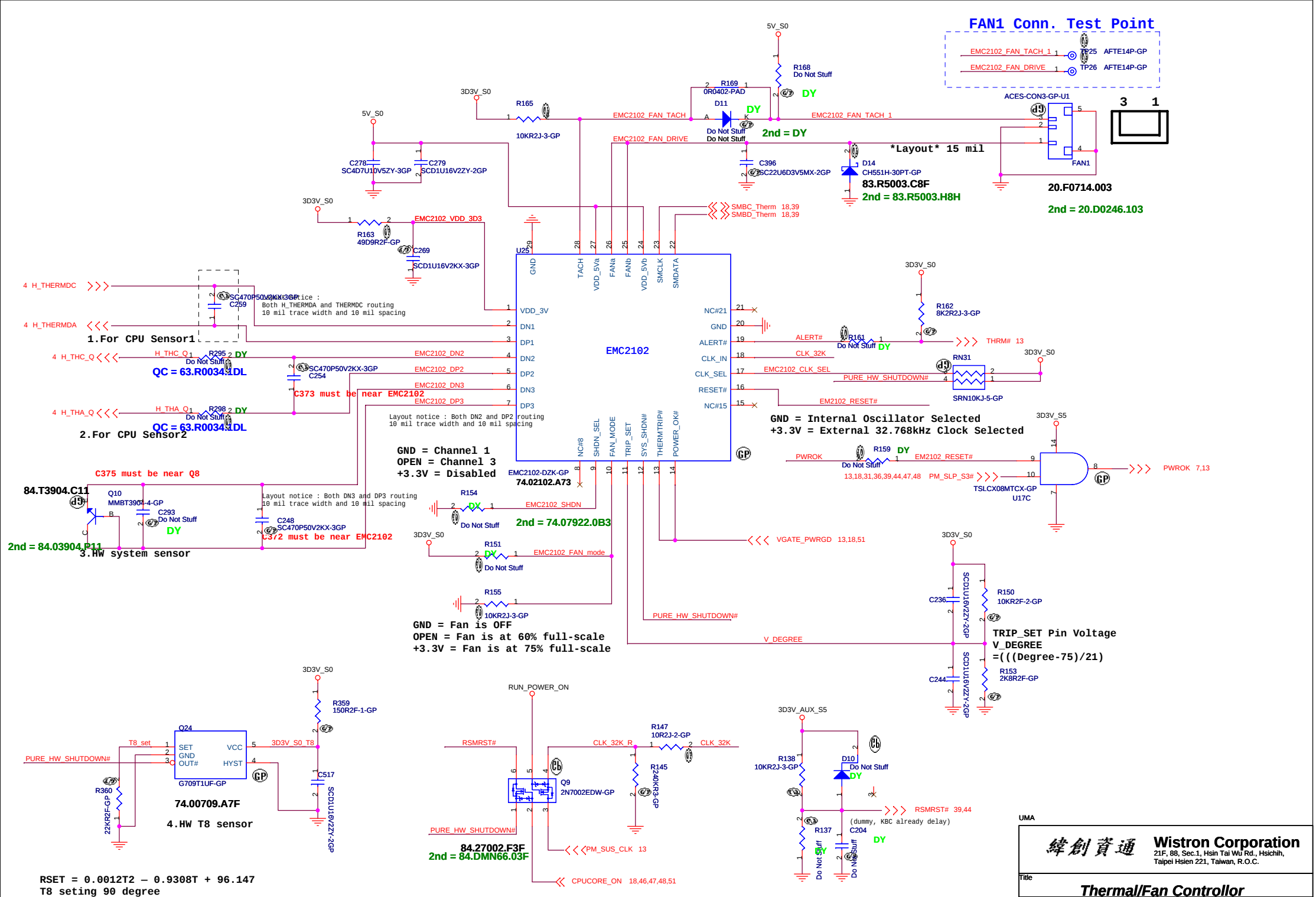


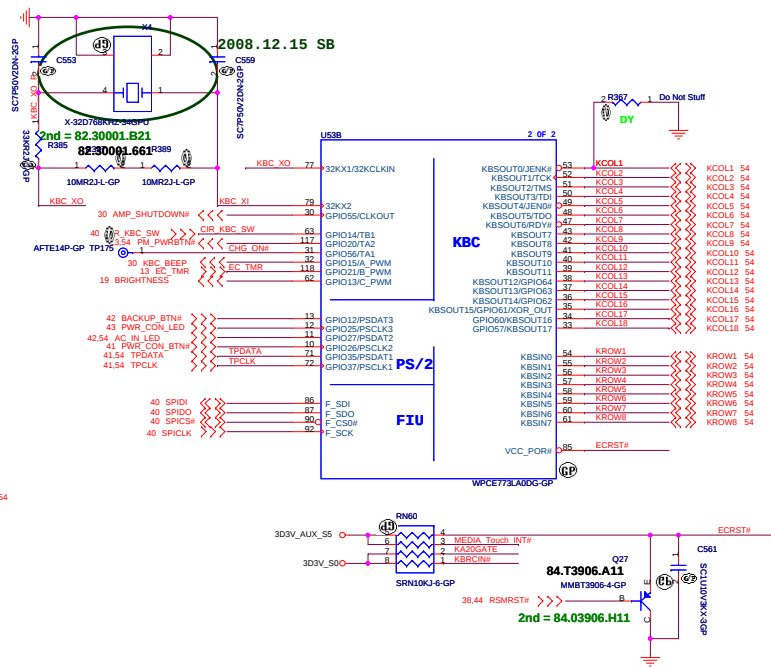
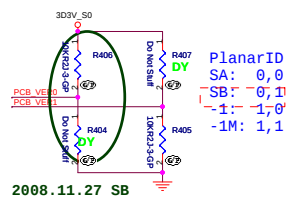
Place near MINIC2



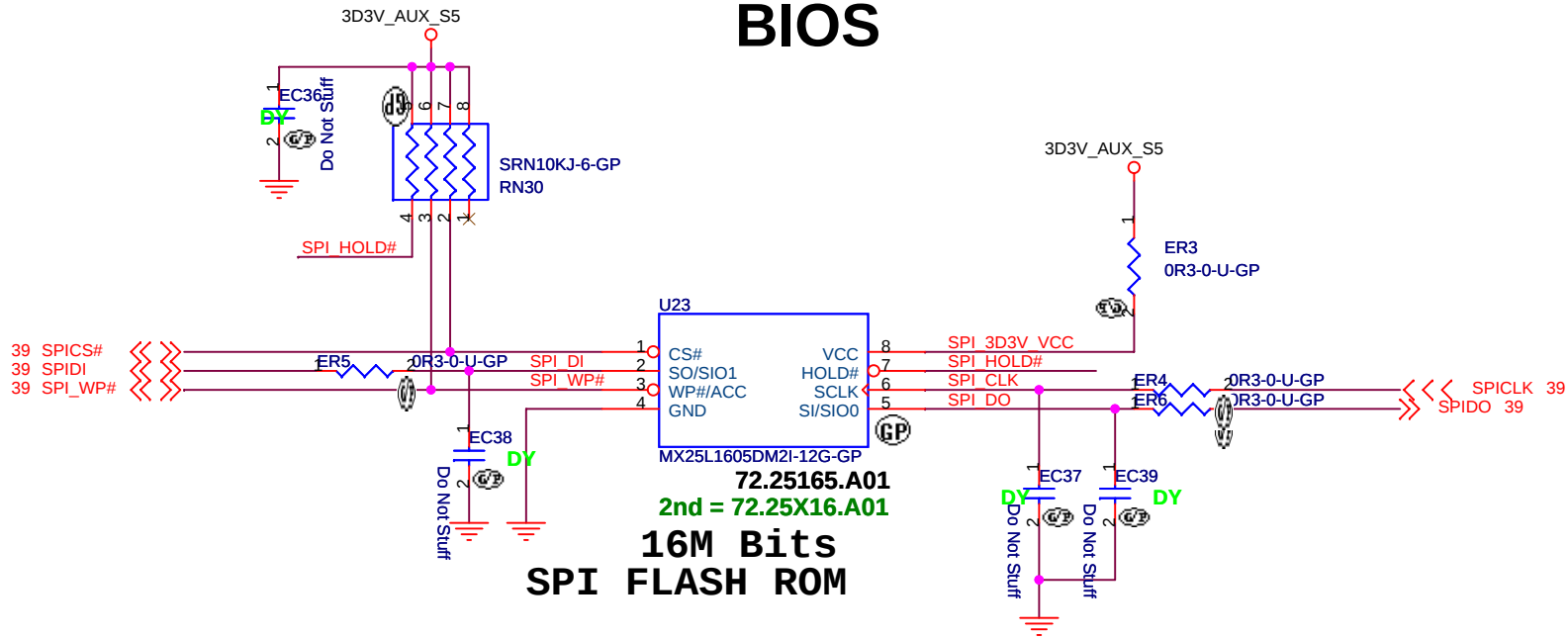
UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
MINI CARD		
Size	Document Number	Rev
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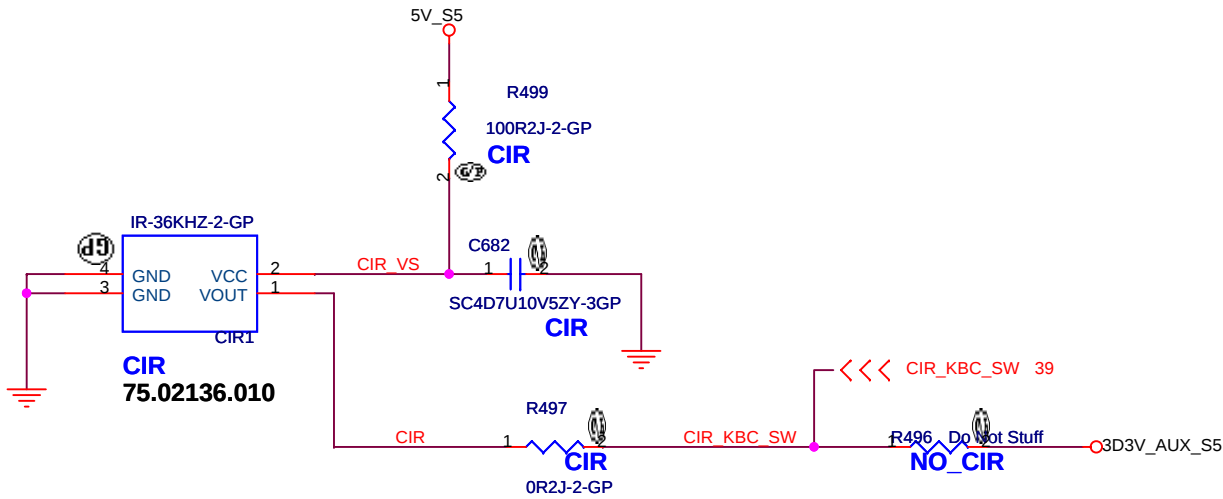


[illegible][illegible]

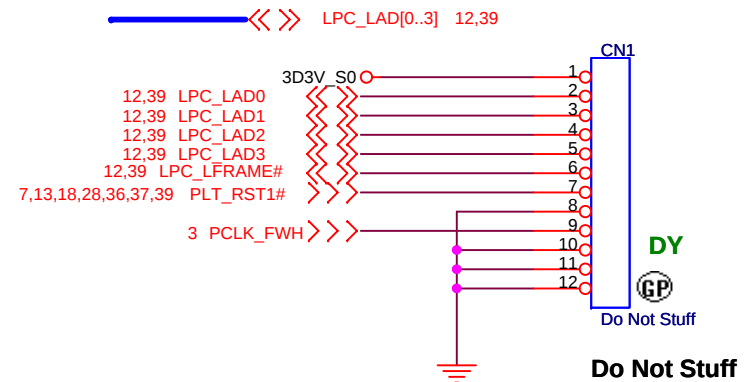
BIOS



VISHAY CIR Module



GOLDEN FINGER FOR DEBUG BOARD



UMA

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

BIOS

Size

Document Number

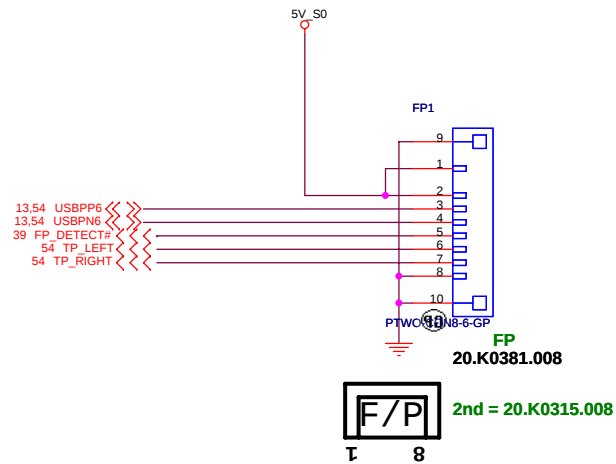
ev

JM70-MV

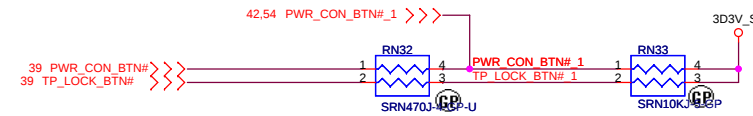
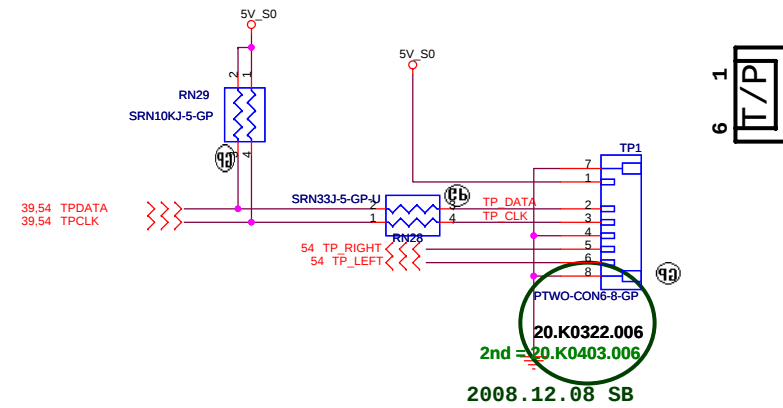
Date: Saturday, December 20, 2008

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Finger printer

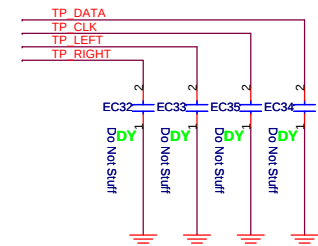
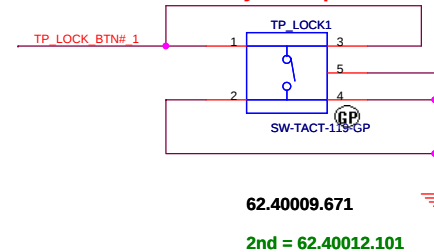


Touch Pad



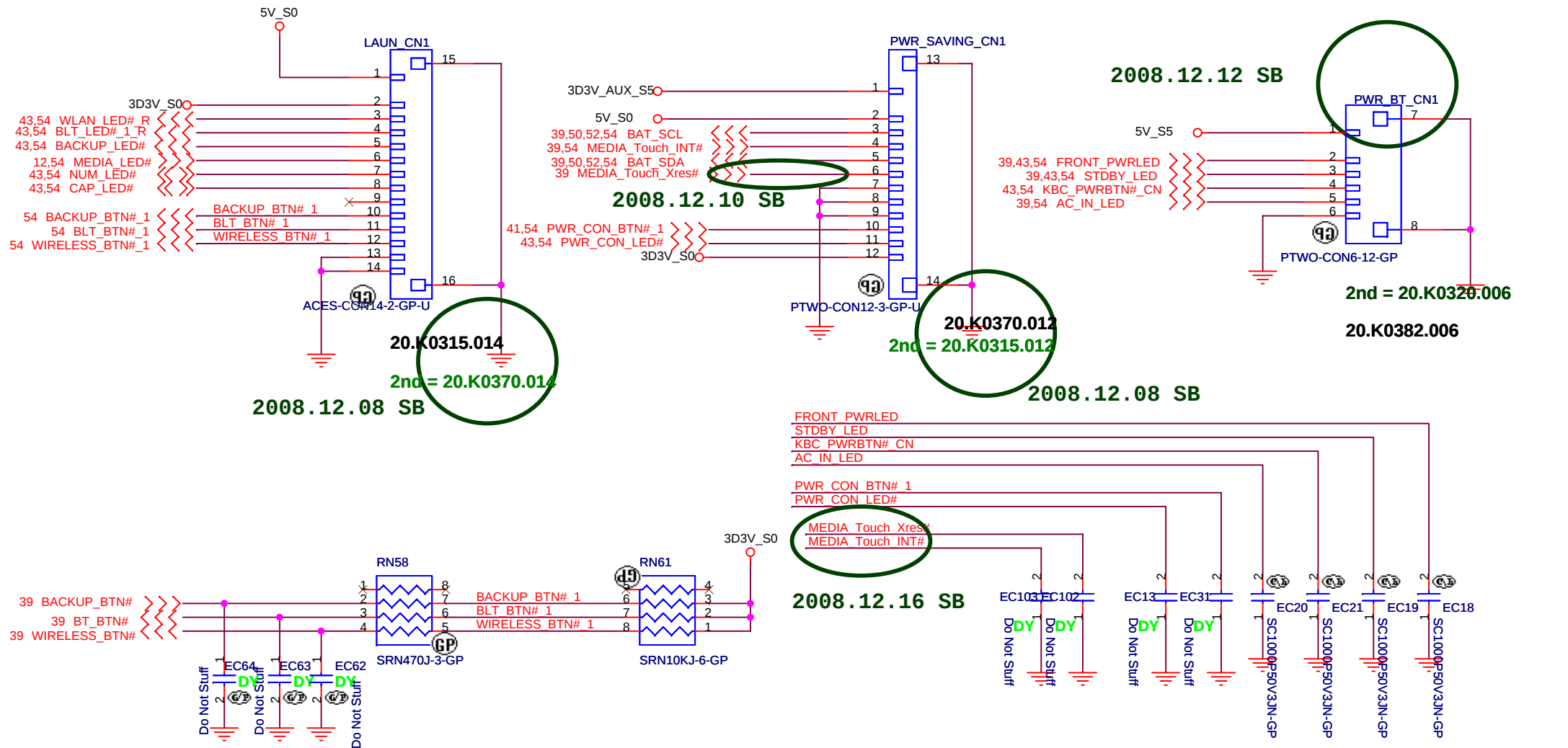
TP_LOCK key

Note. main with 2nd symbol pin define different

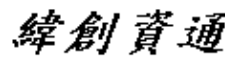


UMA

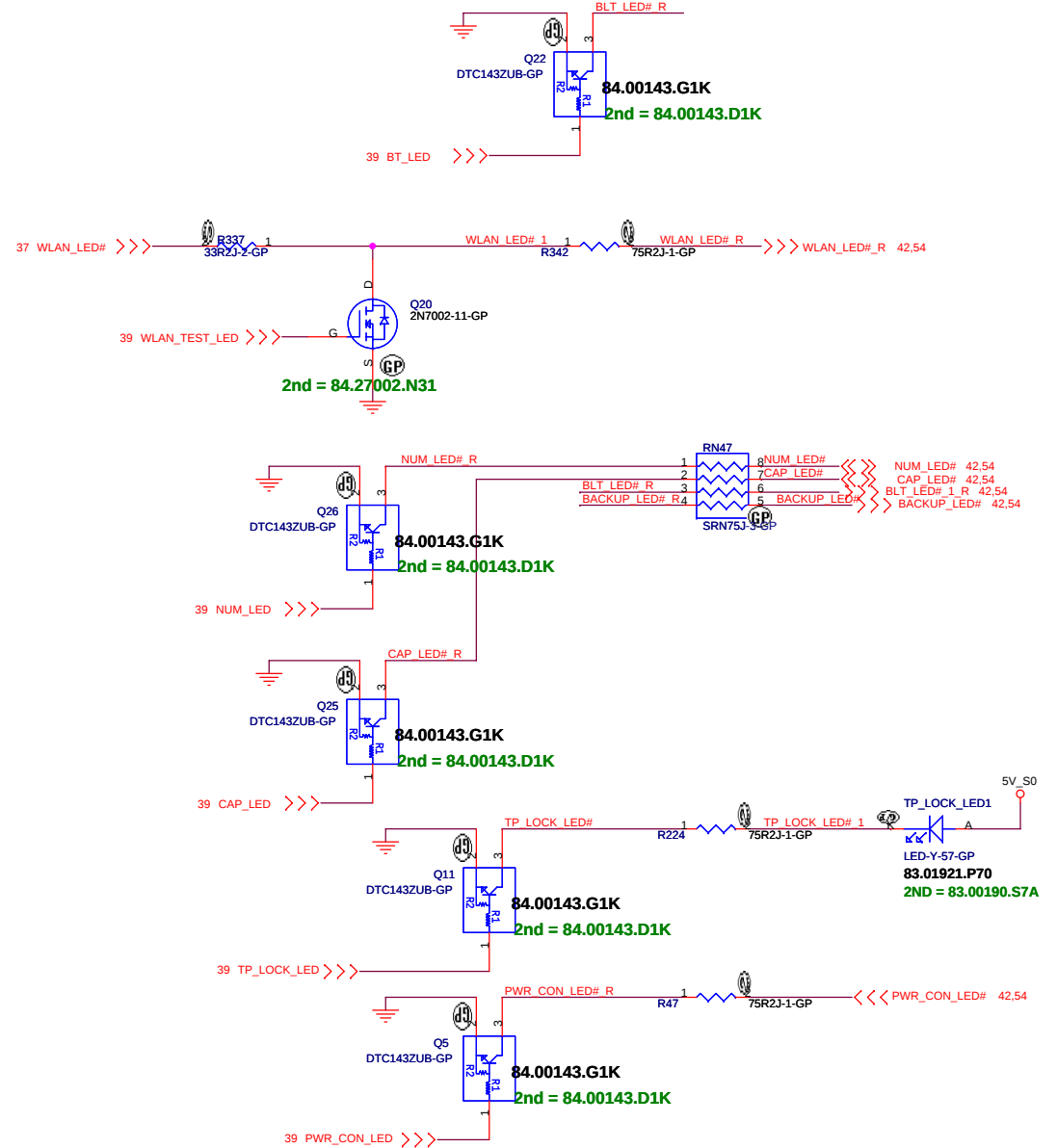
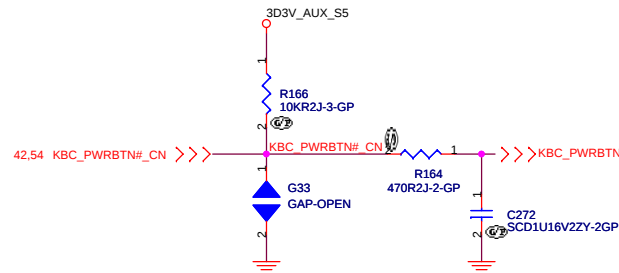
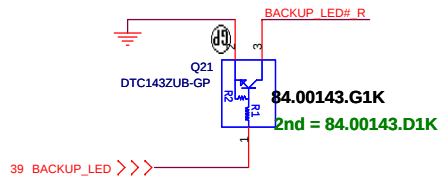
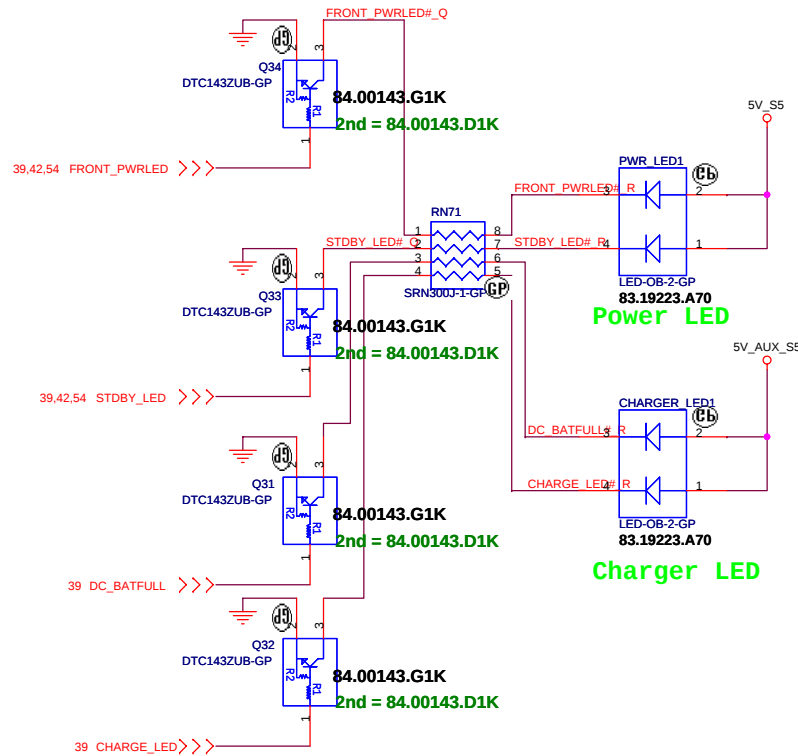
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Touch PAD and FP			
Size	Document Number		Rev
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UMA

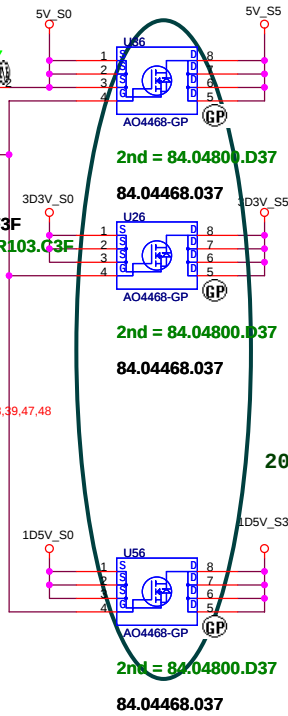
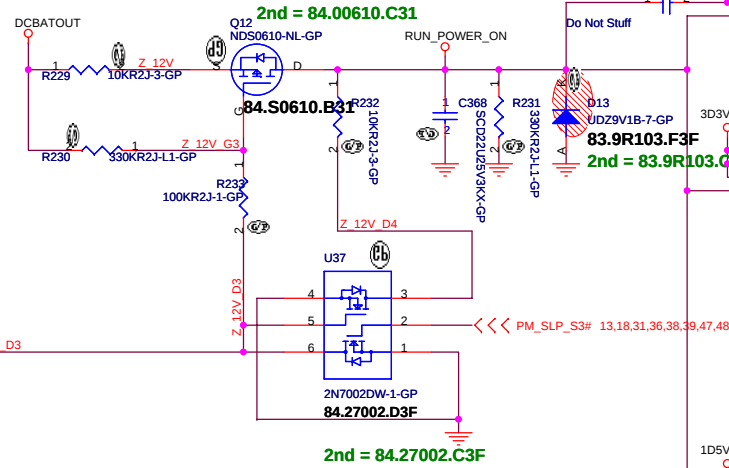
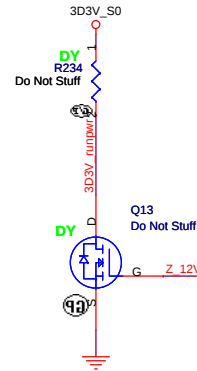
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Launch CN	
Size A4	Document Number JM70-MV
Date: Saturday, December 20, 2008	
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LED

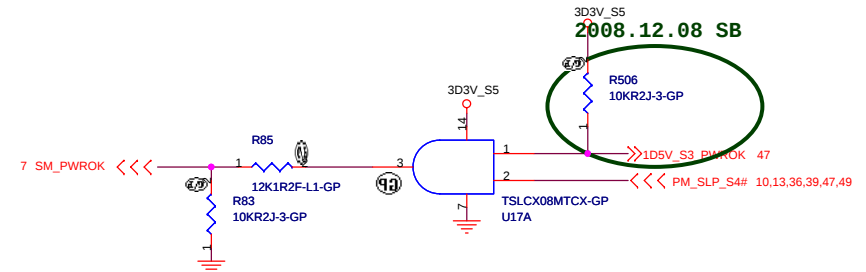


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3D3V_AUX_S5



2008.12.08 SB



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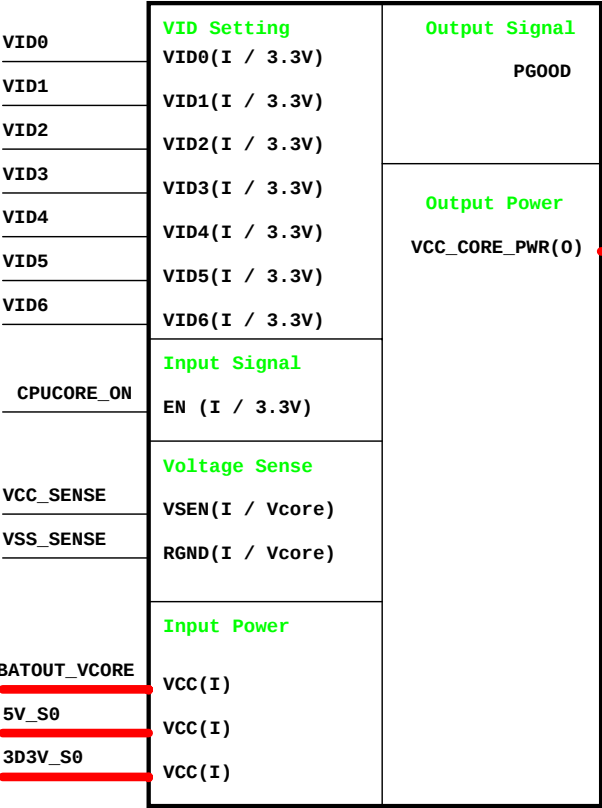
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Taipei Hsien 221, Taiwan, R.O.C.

Title	<i>RUN POWER and 3D3V_AUX_S5</i>
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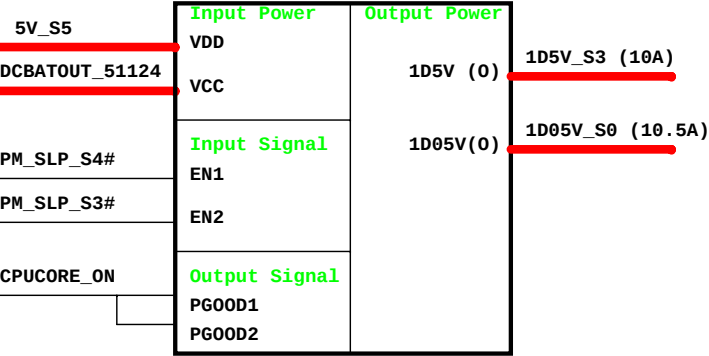
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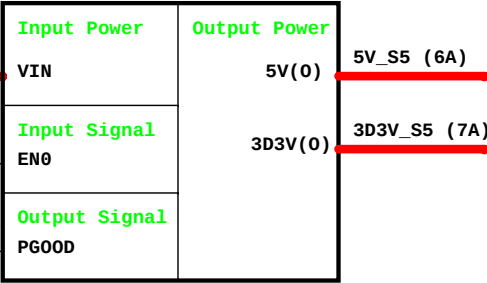
CPU_CORE
ADP3208C



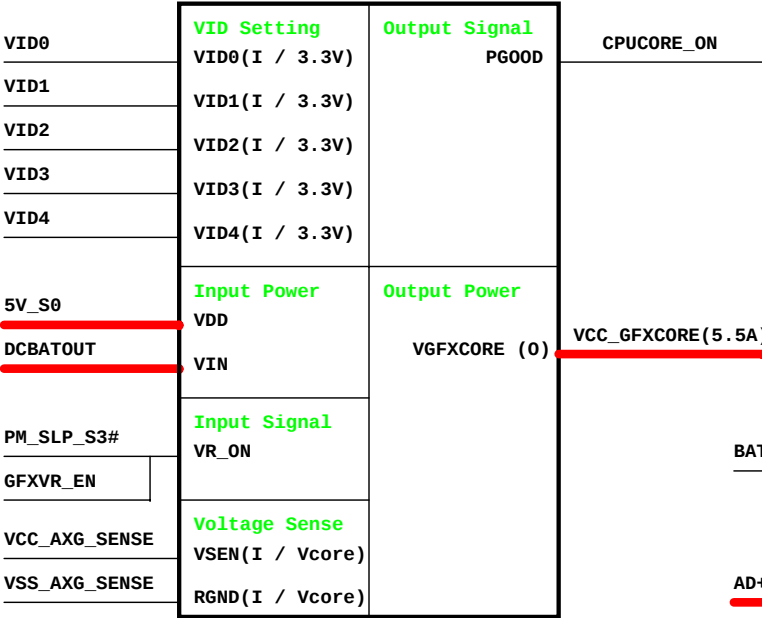
TPS51124
1D5V/1D05V



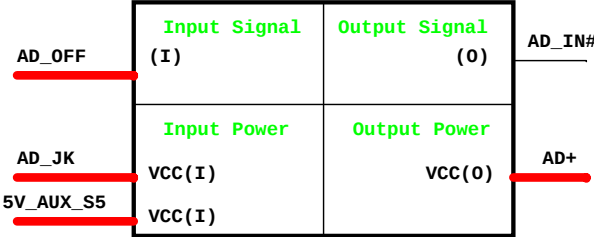
ISL62392
5V/3D3V



GFX_CORE
ISL6263A

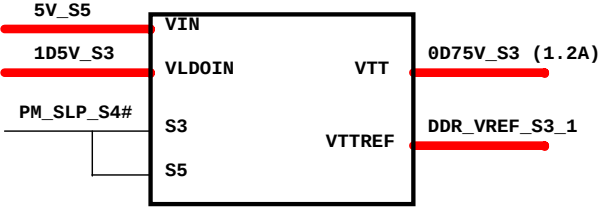


Adapter

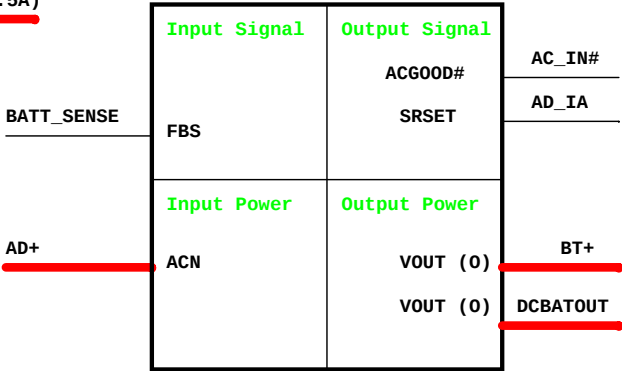


DDR 3.0

RT9026 0D75V_S0



Charger ISL88731A



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Title

Power Block Diagram

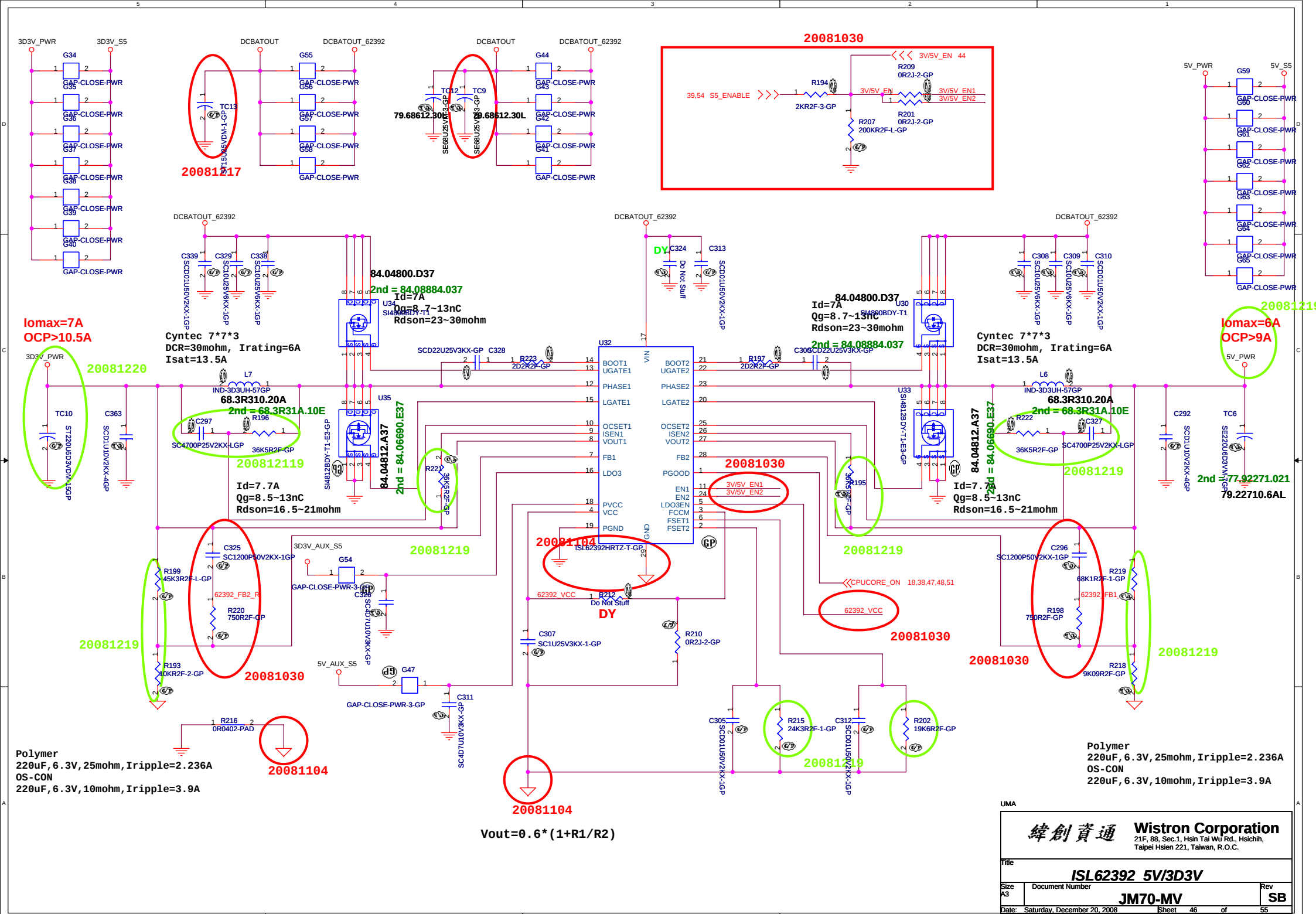
Size B

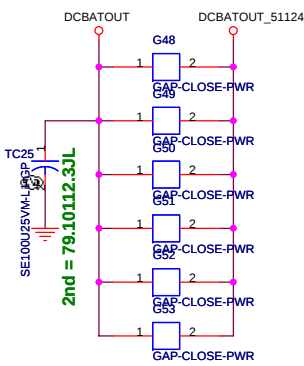
Document Number

Rev SB

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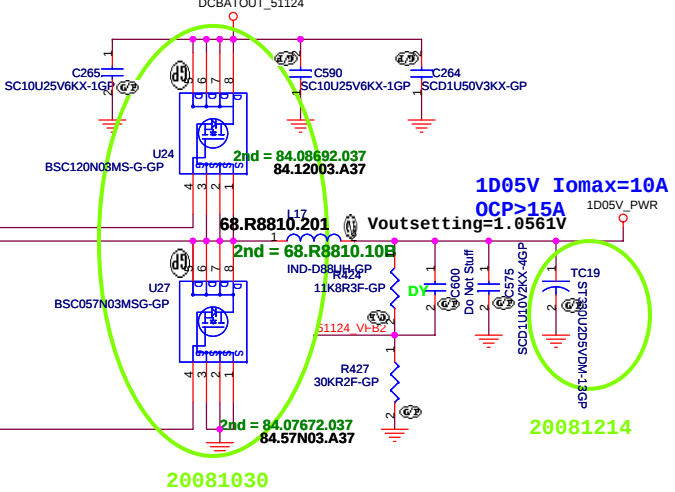
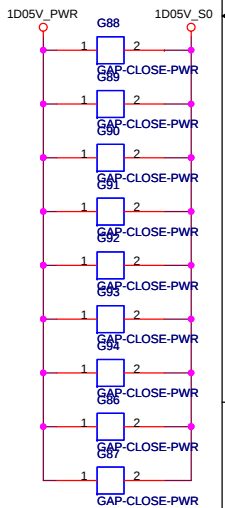
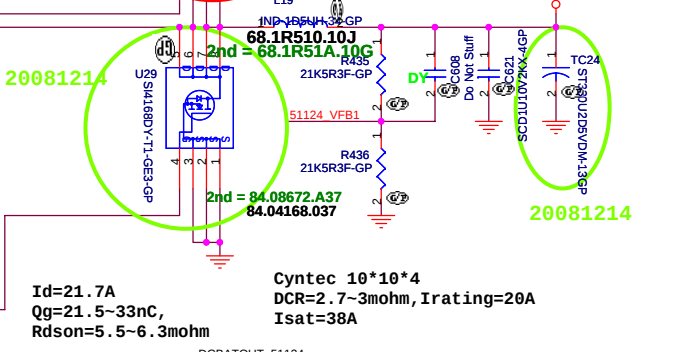
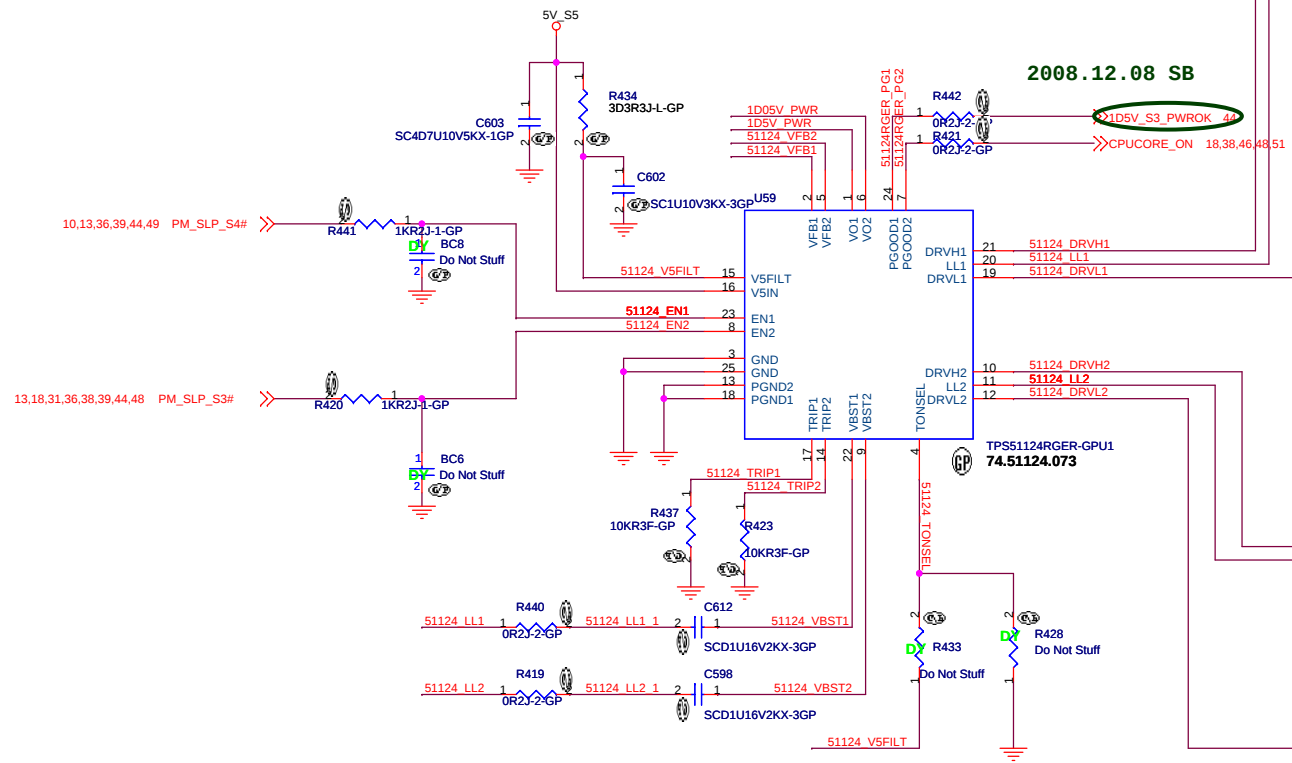
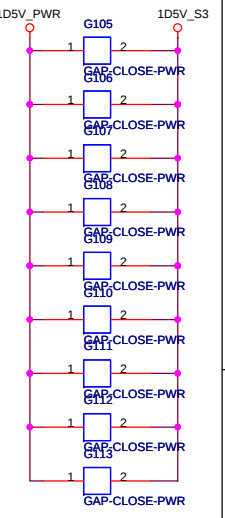
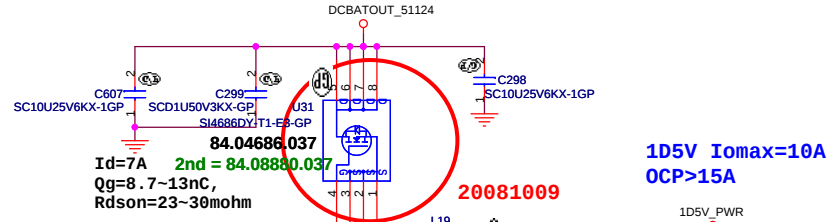
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$$V_{trip}(mV) = R_{trip}(Kohm) * I_0(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out})/V_{in}))$$

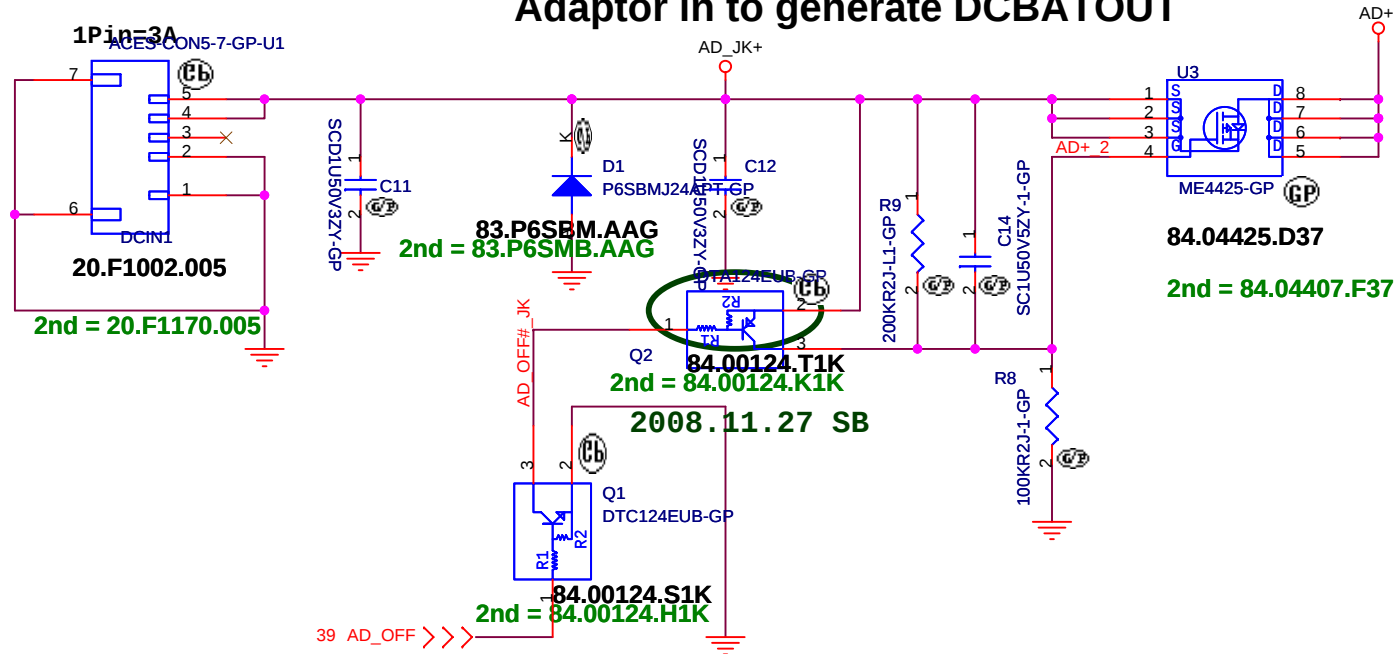


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

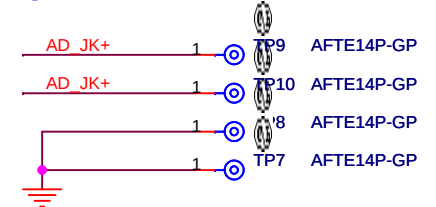
$V_{out} = 0.758V * (R1+R2)/R2$ --> PWM mode

$V_{out} = 0.764V * (R1+R2)/R2$ --> Skip Mode

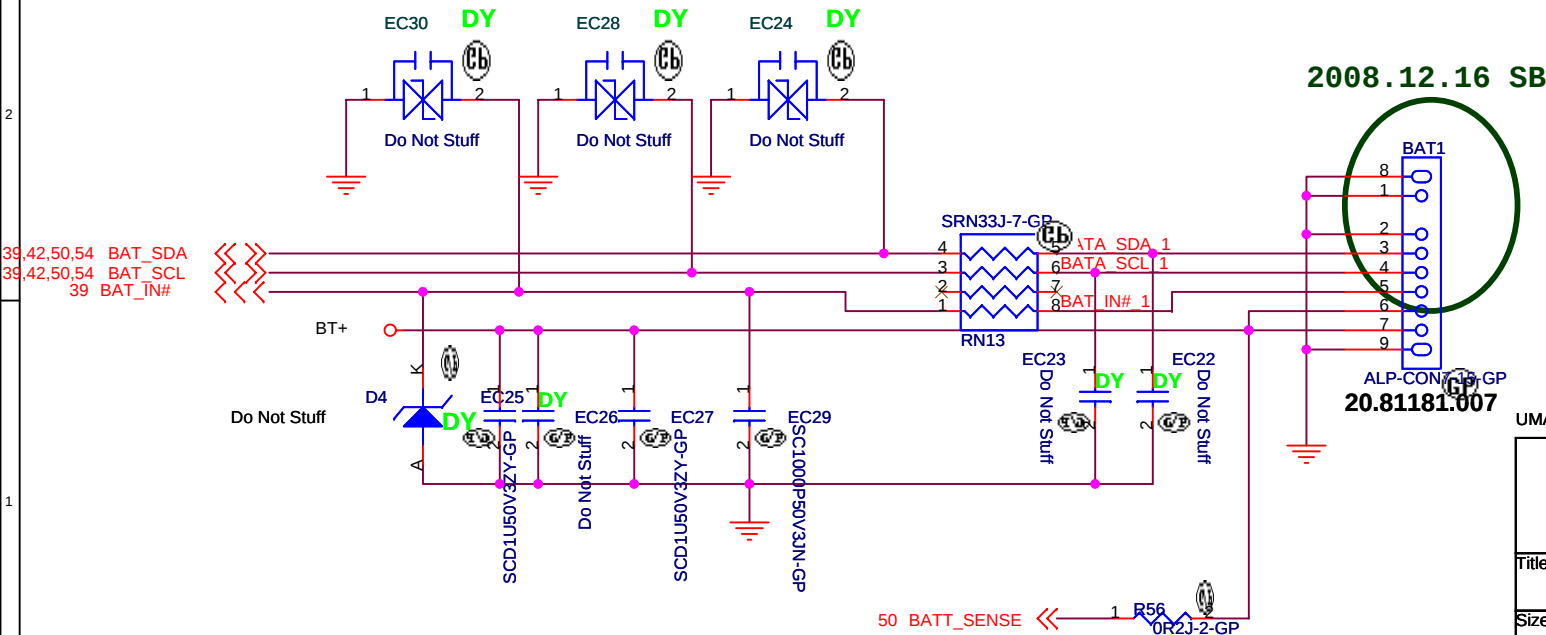
Adaptor in to generate DCBATOUT



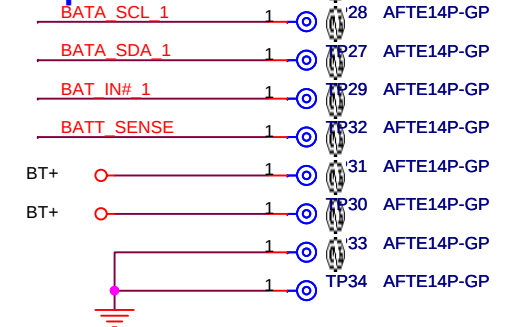
KB Conn. Test Point
keep on connector side



MAIN BATTERY CONNECTOR



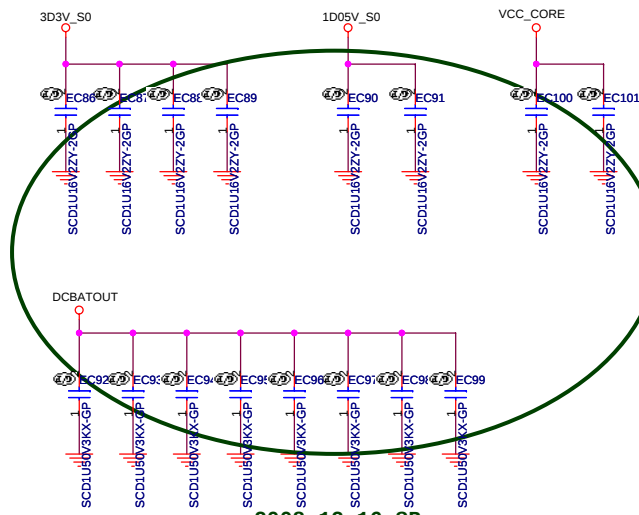
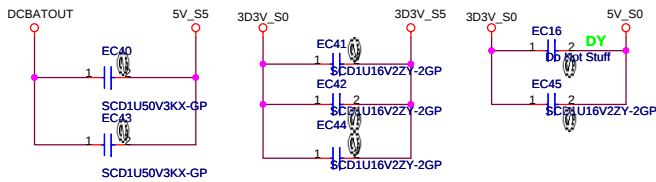
BAT1 Conn. Test Point
keep on connector side



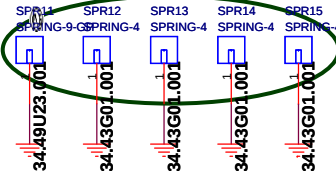
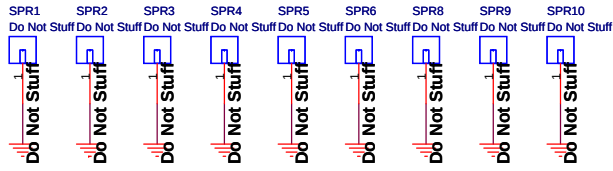
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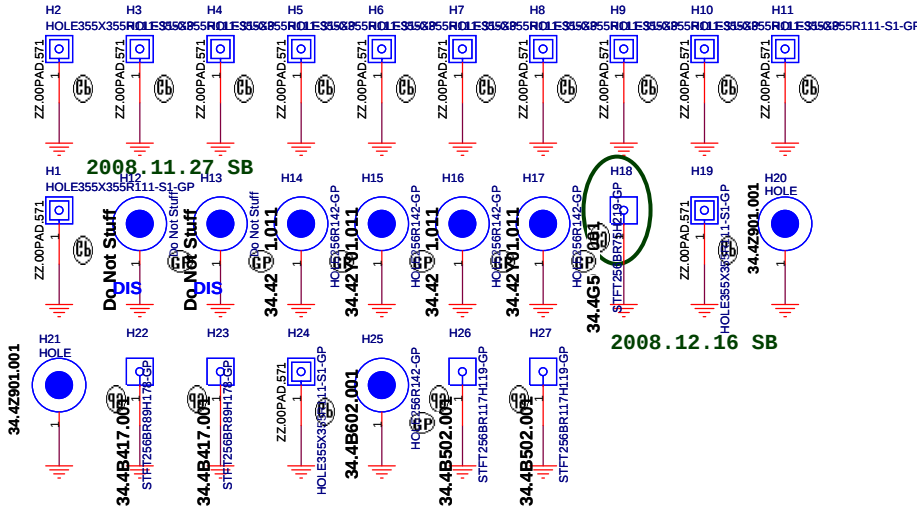


2008.12.16 SB

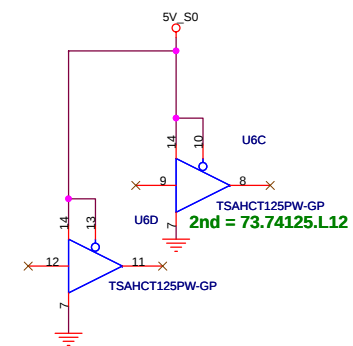
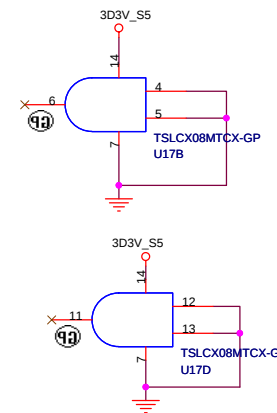


2008.12.16 SB

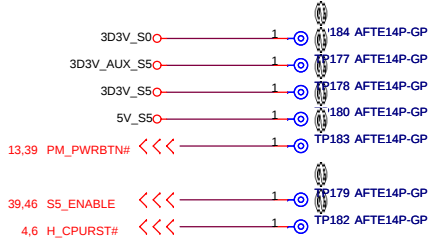
DY DY DY DY DY DY DY DY DY



2008.12.16 SB

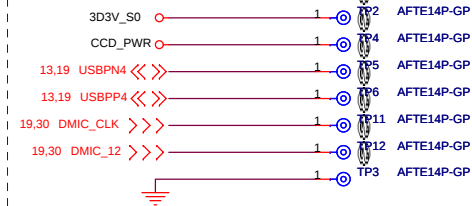


Check test point

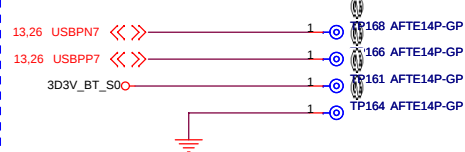


Test Point放在Dimm Door打開可量測處

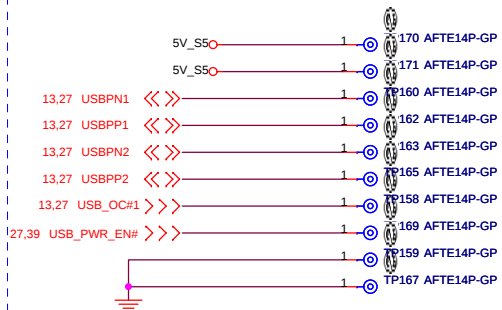
CCD_DMIC_CN1 Conn. Test Point keep on connector side



BT Conn. Test Point keep on connector side



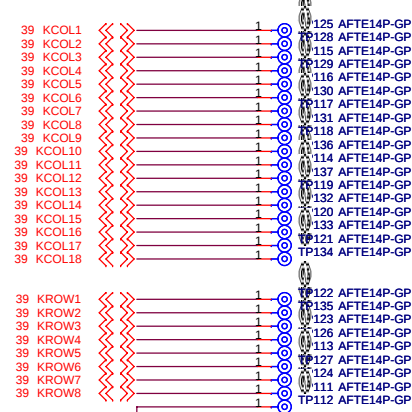
USB_CN1 Conn. Test Point keep on connector side



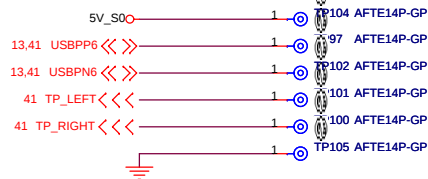
SPKR1 Conn. Test Point keep on connector side



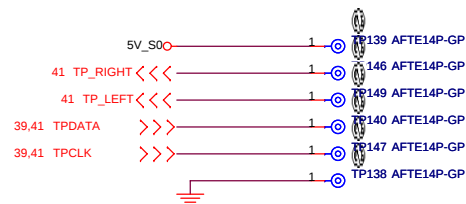
KB1 Conn. Test Point keep on connector side



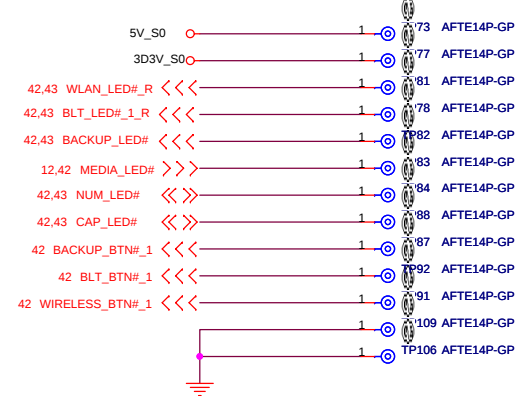
FP test Point keep on connector side



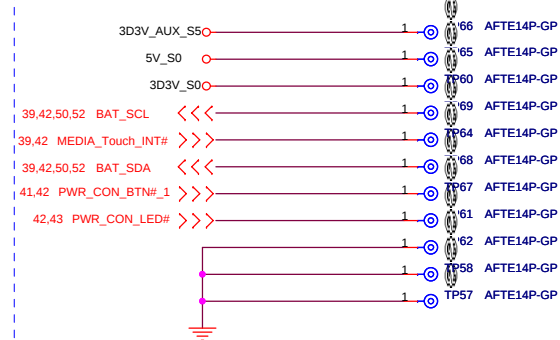
TOUCH PAD Conn. Test Point keep on connector side



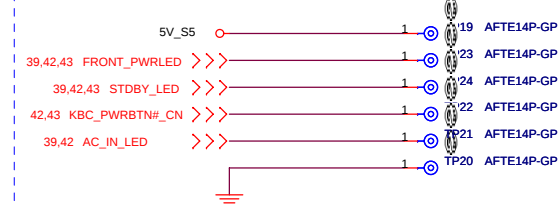
LAUN_CN1 Conn. Test Point keep on connector side



PWR_SAVING_CN1 Conn. Test Point keep on connector side



PWR_BT_CN1 Conn. Test Point keep on connector side



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