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16	PCH (POWER) 1/2	SA		58	FAN	SA			
17	PCH (POWER) 2/2	SA		59	Thermal Sensor	SA			
18	PCH (VSS)	SA		60	Touch Pad	SA			
19	CLOCK GEN	SA		61	Function DB Conn.	SA			
20	DDRIII(SO-DIMM_0) 1/3	SA		62	Audio/USB DB Conn.	SA			
21	DDRIII(SO-DIMM_1) 2/3	SA		63	Function DB(SPEAKER)	SA			
22	VGA (PCI-E) 1/9	SA		64	Function DB (Botton & LED)	SA			
23	VGA (PCIE-BUS/Strap) 2/9	SA		65	Audio (CODEC)	SA			
24	VGA (DDR3) 3/9	SA		66	Audio (MUTE)	SA			
25	VGA (DDR3) 4/9	SA		67	Audio (Power)	SA			
26	VGA (CRT) 5/9	SA		68	Audio (Audio & USB Conn.)	SA			
27	VGA (LVDS/HDMI) 6/9	SA		69	Audio (Head Phone Jack)	SA			
28	VGA (GPIO) 7/9	SA		70	Audio (Ext MIC Jack)	SA			
29	VGA (XTAL) 8/9	SA		71	Audio (USB Portx2)	SA			
30	VGA (Power/GND) 9/9	SA		72	Power Design Diagram	SA			
31	VRAM(DDR3)# 1/4	SA		73	DCIN&Charger	SA			
32	VRAM(DDR3)# 2/4	SA		74	SYS Power (+3_3V/+5V)	SA			
33	VRAM(DDR3)# 3/4	SA		75	VTT&PCH Power(+1_05V)	SA			
34	VRAM(DDR3)# 4/4	SA		76	DDR3 Power(+1_5V/+0_75V)	SA			
35	VRAM(BYPASS) 1/2	SA		77	SYS Power(+1_8V)	SA			
36	VRAM(BYPASS) 2/2	SA		78	CPU Power_VHCORE	SA			
37	MUX LVDS	SA		79	CPU Power_VID	SA			
38	MUX CRT	SA		80	VGA GFX Power-VGFX CORE	SA			
39	CRT	SA		81	VGA Power(NV_VDD)	SA			
40	Optimux	SA		82	Others power plane	SA			
41	LVDS	SA		83	OVP protection	SA			
42	HDMI Optimux	SA		84	Discharger Circuit	SA			

BOM Control Table

Project Code & Schematics Subject: **W930 H1&H2**

PCB P/N:

P. Leader	Check by	Design by

FOXCONN — HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: *Index Page*

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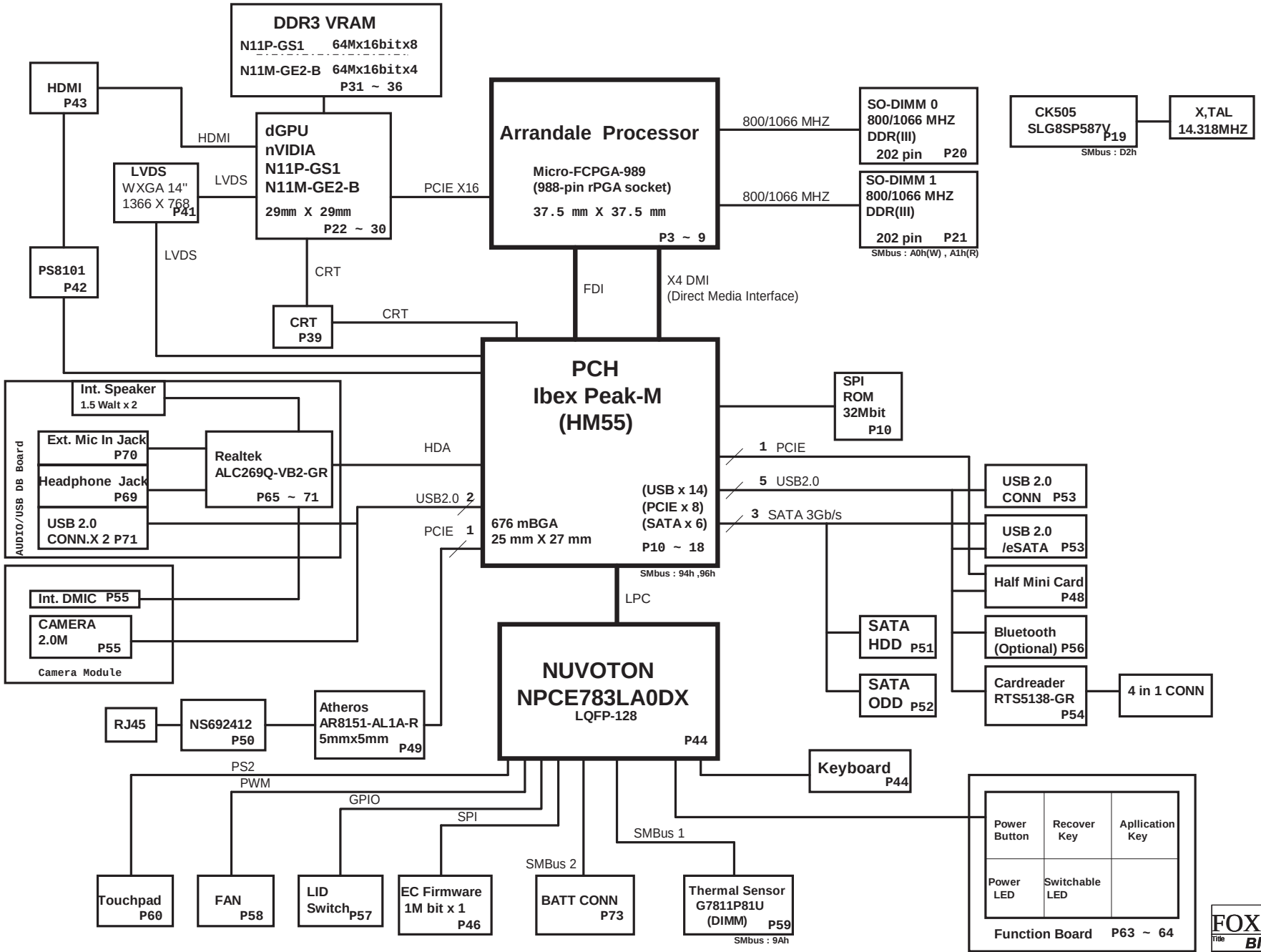
W930 Block

H1 Discrete (NV_)
H2 Switchable(nVIDIA Optimus) (SG_)
Both



TI CHARGER BQ24753 P.73

	OUTPUTS
DC_IN	BT+ DCBATOUT

SYSTEM DC/DC TI SN0608098RHBR P.74

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +12V

SYSTEM DC/DC FP6339WQGTR P.75

INPUTS	OUTPUTS
DCBATOUT	+1_05V_VTT

SYSTEM DC/DC FP6339WQGTR GMT G2998F11U P.76

INPUTS	OUTPUTS
DCBATOUT	+1_5VSUS
+1_5VSUS	+0_75VRUN

CPU DC/DC FP6149SPGTR P.77

INPUTS	OUTPUTS
+3VRUN	+1_8VRUN

CPU DC/DC MAX17030GTL+ P.78

INPUTS	OUTPUTS
DCBATOUT	VHCORE

SYSTEM DC/DC ADP3211MNR2G P.80

INPUTS	OUTPUTS
DCBATOUT	GFXCORE

SYSTEM DC/DC TI TPS51217DSCR FP6149SPGTR P.81

INPUTS	OUTPUTS
DCBATOUT	NV_VDD
+1_5VRUN	PEX_VDD

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Title: **Block Diagram**

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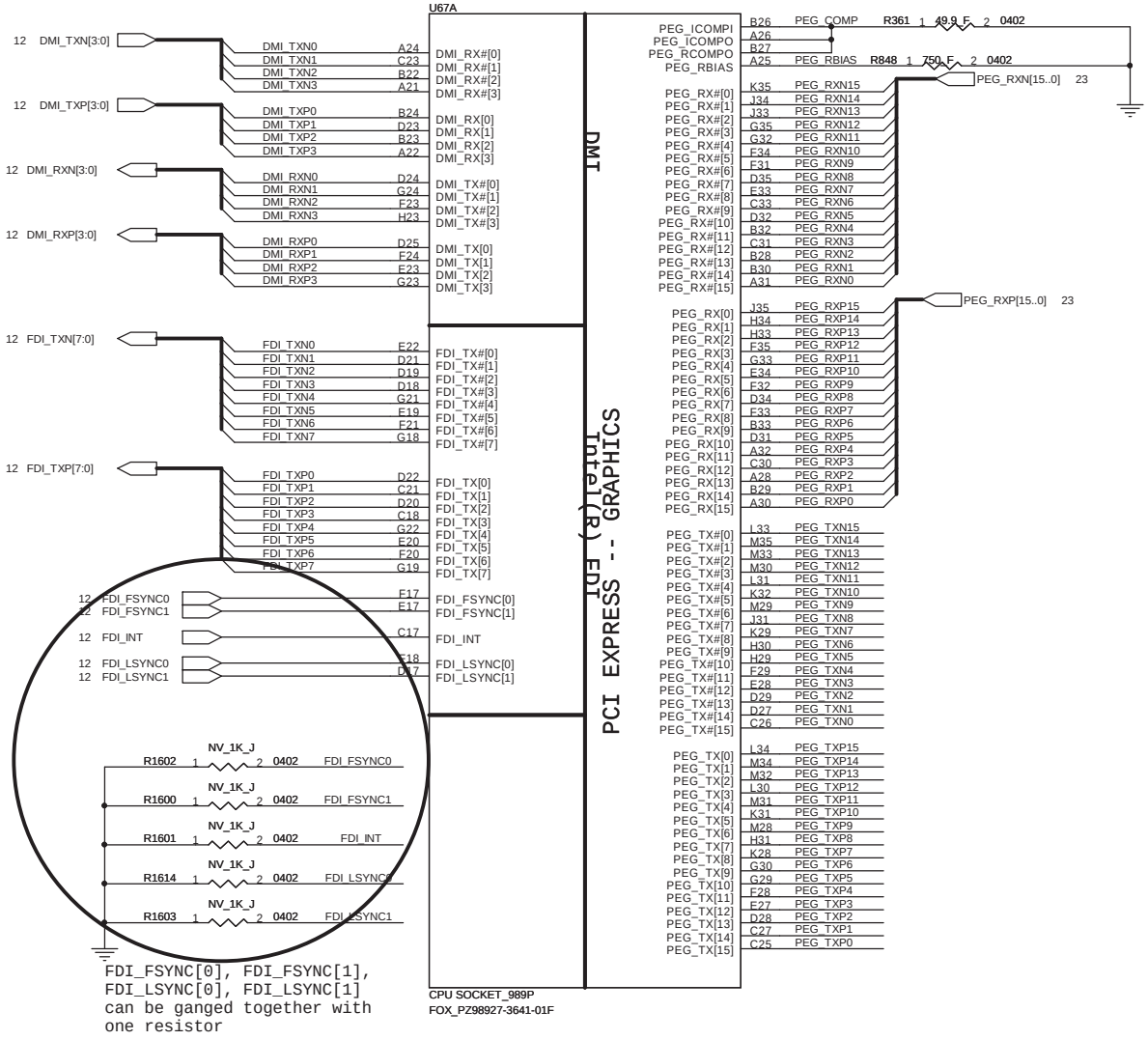
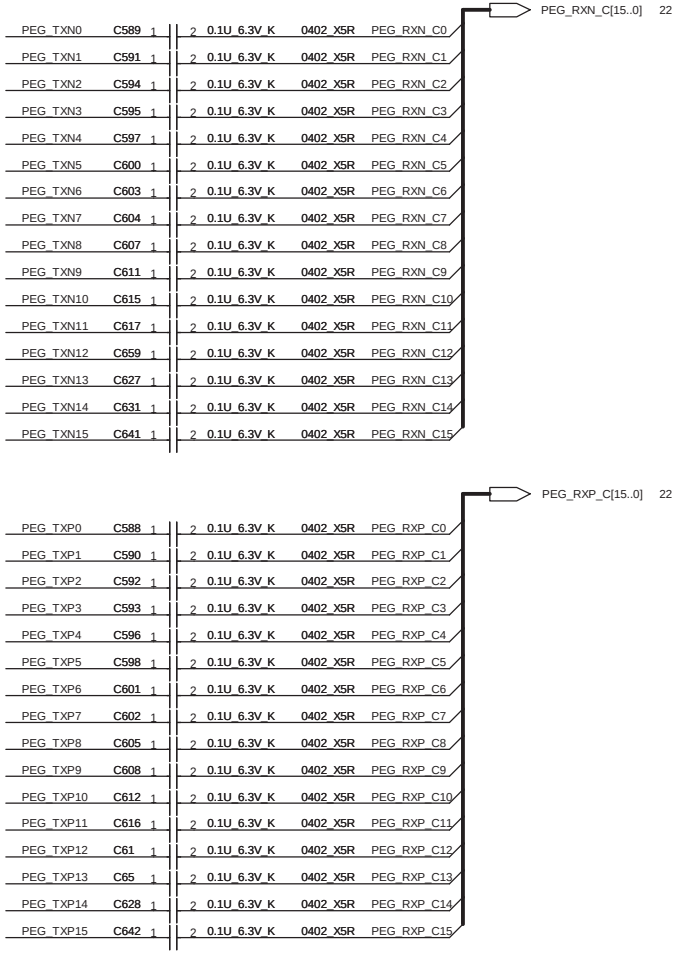


FDI_FSYNC[0], FDI_FSYNC[1],
FDI_LSYNC[0], FDI_LSYNC[1]
can be ganged together with
one resistor

If PCIe Graphics is not implemented,
the TX/RX pairs can be left as No Connect.



For Disable Arrandale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH. FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors). FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be ganged together with one resistor.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	ARD (DMI,PEG,FDI)		
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Layout Note:
Comp0,1 connect with Zo=49.9 ohm,
Comp2,3 connect with Zo=20 ohm,
In order to minimize resistance,
use thick traces to route all
COMP signals, use 10-mils
(0.254-mm) wide trace for
routing less than 500 mils (12.7
mm), or 20-mils (0.508-mm)
wide trace for routing between
500 mils (12.7 mm) and
1000 mils (25.4 mm). Keep 20-mils
(0.508-mm) spacing to
any other signals in order to
minimize crosstalk.

U67B

MISC
THERMAL
CLOCKS
DDR3 MISC
JTAG & BPM
PWR MANAGEMENT

COMP3 AT23 — R849 1 20_F 2 0402 COMP3
COMP2 AT24 — R850 1 20_F 2 0402 COMP2
COMP1 G16 — R851 1 49.9_F 2 0402 COMP1
COMP0 AT26 — R852 1 49.9_F 2 0402 COMP0
SKTOCC# AH24 — 20MIL TP60 1 SKTOCC#
CATERR# AK14 — H_CATERR#
PECI AT15 — 15 H_PECI — H_PECI
PROCHOT# AN26 — 78 PROCHOT# — PROCHOT#
THERMTRIP# AK15 — 15,28,44 PM_THRMTRIP# — R939 1 0_J 2 0402 PM_THRMTRIP# 1
RESET_OBS# AP26 — H_CPURST# R
PM_SYNC AL15 — 12 H_PM_SYNC — H_PM_SYNC
VCCPWRGOOD_1 AN14 — R937 1 0_J 2 0402 SYS_AGENT_PWROK
VCCPWRGOOD_0 AN27 — 15 H_CPUPWRGD — R930 1 0_J 2 0402 CPUPWRGD_R
SM_DRAMPWROK AK13 — 12 PM_DRAM_PWRGD — PM_DRAM_PWRGD
VTTPWRGOOD AM15 — VTTPWRGOOD
TAPPWRGOOD AM26 — 20MIL TP94 1 TAPPWRGOOD
RSTIN# AL14 — 14,44,47 BUF_PLT_RST# — R925 1 2 BUF_PLT_RST# R — 1.5K_F 0402 — R926 750_F 0402

CPU SOCKET_989P
FOX_PZ98927-3641-01F

BCLK A16 ARD_BCLK — R1450 1 0_J 2 0402 — CLK_PCH_CPU_CLK 15
BCLK# B16 ARD_BCLK# — R1451 1 NC_0_J 2 0402 — CLK_CPU_BCLK 19
BCLK_ITP AR30 BCLK_ITP 1 — R1452 1 NC_0_J 2 0402 — CLK_CPU_BCLK# 19
BCLK_ITP# AT30 BCLK_ITP# 1 — R1453 1 0_J 2 0402 — CLK_PCH_CPU_CLK# 15
TP61 20MIL
TP63 20MIL
PEG_CLK E16 CLK_EXP_P_R — 1 4 — CLK_EXP_P 11
PEG_CLK# D16 CLK_EXP_N_R — 2 3 — CLK_EXP_N 11
RP80 0 0404_4P2R
DPLL_REF_SSCLK A18 CLK_DP_P_R
DPLL_REF_SSCLK# A17 CLK_DP_N_R

SM_DRAMRST# F6 DDR3_DRAMRST# Q
SM_RCOMP[0] AL1 SM_RCOMP0 R854 1 100_F 2 0402
SM_RCOMP[1] AM1 SM_RCOMP1 R853 1 24.9_F 2 0402
SM_RCOMP[2] AN1 SM_RCOMP2 R855 1 130_F 2 0402
PM_EXT_TS#[0] AN15 PM_EXTTS#0
PM_EXT_TS#[1] AP15 PM_EXTTS#1

PRDY# AT28 XDP_PRDY# 1 — TP75 20MIL
PREQ# AP27 XDP_PREQ#
TCK AN28 XDP_TCLK
TMS AP28 XDP_TMS
TRST# AT27 XDP_TRST#
TDI AT29 XDP_TDI_R
TDO AR27 XDP_TDO_R
TDI_M AR29 XDP_TDI_M
TDO_M AP29 XDP_TDO_M
DBR# AN25 XDP_DBRESET#
+3VRUN — R1292 NC_51_J 0402
BPM#[0] AJ22 BPM#0 1 — TP64 20MIL
BPM#[1] AK22 BPM#1 1 — TP65 20MIL
BPM#[2] AK24 BPM#2 1 — TP66 20MIL
BPM#[3] AJ24 BPM#3 1 — TP67 20MIL
BPM#[4] AJ25 BPM#4 1 — TP68 20MIL
BPM#[5] AH22 BPM#5 1 — TP69 20MIL
BPM#[6] AK23 BPM#6 1 — TP70 20MIL
BPM#[7] AH23 BPM#7 1 — TP71 20MIL

+1_05V_VTT — R932 10K_J 0402 — R933 10K_J 0402
PM_EXTTS#0 20
PM_EXTTS#1 20,21
R1231 NC_12.4K_F 0402

+3VRUN — R262 4.7K_J 0402 — A0205 — PROCHOT# — Q14A 2N7002DW null
Q14B 2N7002DW null
44 OVT_EC#

CLK_DP_P_R — R1607 0_J 0402
CLK_DP_N_R — R1608 0_J 0402

For Disable Arrandale Graphic
DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Arrandale directly if motherboard only supports discrete graphics.

XDP_TDO_R 51_J — R1290
XDP_TMS NC_51_J — R1258
XDP_TDI_R NC_51_J — R1259
XDP_PREQ# NC_51_J — R1260
XDP_TCLK NC_51_J — R1261
XDP_TRST# 51_J — R1262
+1_05V_VTT
XDP_TDO_M — R969 0_J 0402 — XDP_TDI_M

JTAG Mapping -Scan Chain (Default)

For Intel S3 Power Reduction issue

+3VRUN — R14 10K_J 0402 — C13 0.1U_6.3V_K 0402_X5R
U2 74AHC1G08GW
RUN_PWRGD
4VTTPW_R R1572 1 2K_F 2 0402 VTTPWRGOOD
R1573 1K_F 0402
R970 1 NC_0_J 2 0402

For Intel S3 Power Reduction issue

+3VSUS
+1_5VSUS_CPU
R5950 NC_1.1K_F 0402
PM_DRAM_PWRGD
0402 750_F R5927
C6316 0.1U_6.3V_K 0402_X5R
R5926 1 4 0402 1.5K_F
U217 74AHC1G08GW
R5951 10K_J 0402
RUN_PWRGD 12,44,76,76,81

+1_05V_VTT — R861 49.9_F 0402 — R936 NC_68_J 0402
H_CATERR#
H_CPURST# R

For Intel S3 Power Reduction issue

R5948 1 NC_0_J 2 0402
Q72 2N7002W null
+1_5VSUS
0402 1K_J R5925
DDR3_DRAMRST# Q
DDR3_DRAMRST#
DDR3_DRAMRST# 20,21
R5949 100K_J 0402
C6317 0.047U_16V_K 0402_X7R
15 RST_GATE

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (CLK,MISC,JTAG)	
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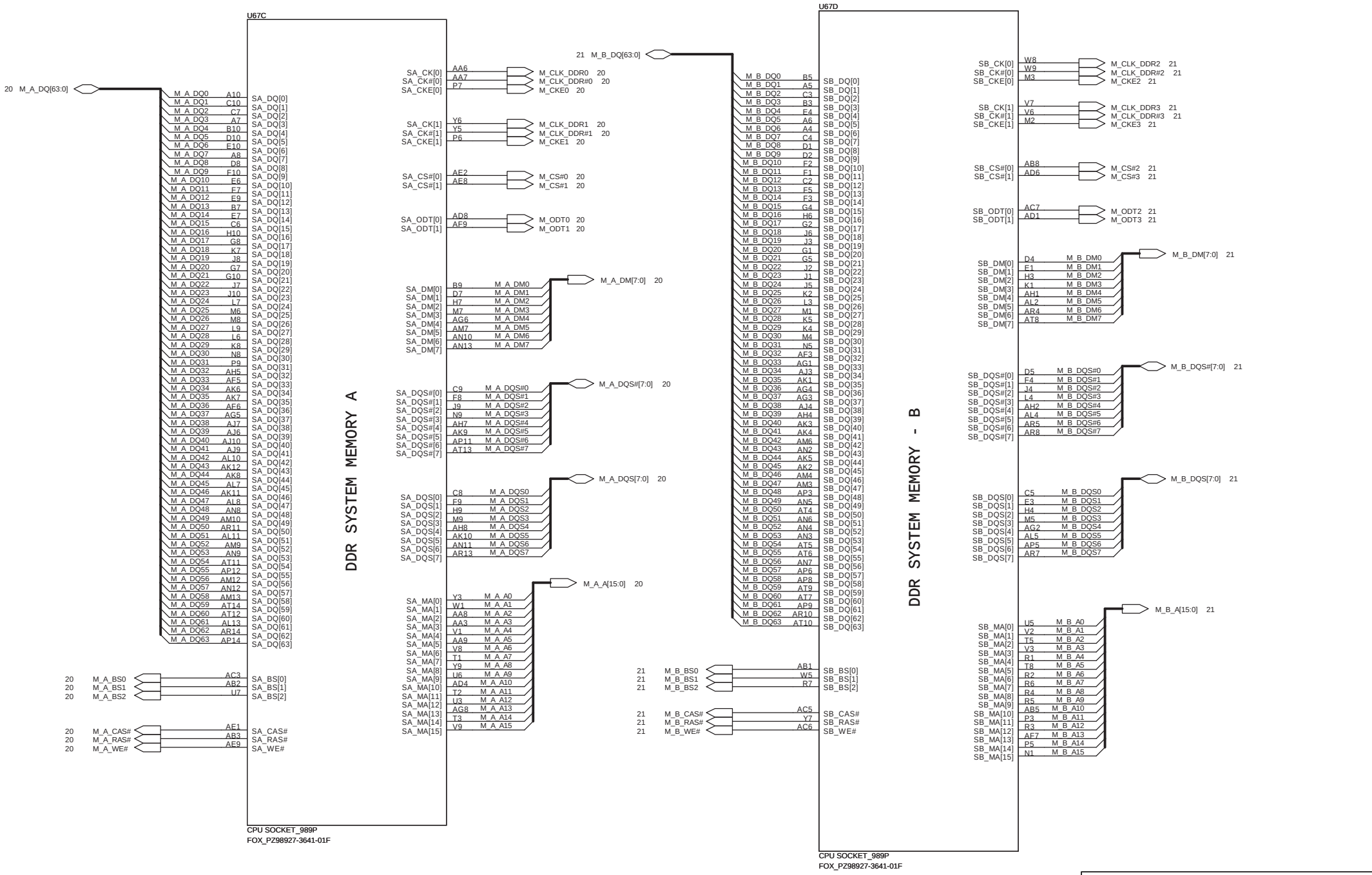

FOXCONN	HON HAI Precision Ind. Co., Ltd.	
	CCPBG - R&D Division	
Title	ARD (DDR3)	
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48A (SV)

VHCORE

C509 22U_6.3V_M 0805_X5R
C491 22U_6.3V_M 0805_X5R
C510 22U_6.3V_M 0805_X5R
C496 22U_6.3V_M 0805_X5R
C502 NC_22U_6.3V_M 0805_X5R

VHCORE

C490 22U_6.3V_M 0805_X5R
C48 22U_6.3V_M 0805_X5R
C492 22U_6.3V_M 0805_X5R
C504 22U_6.3V_M 0805_X5R
C507 22U_6.3V_M 0805_X5R

VHCORE

C495 22U_6.3V_M 0805_X5R
C497 22U_6.3V_M 0805_X5R
C499 NC_22U_6.3V_M 0805_X5R
C503 22U_6.3V_M 0805_X5R
C505 NC_22U_6.3V_M 0805_X5R

VHCORE

C508 NC_22U_6.3V_M 0805_X5R
C921 10U_6.3V_M 0805_X5R
C922 10U_6.3V_M 0805_X5R
C923 10U_6.3V_M 0805_X5R
C924 10U_6.3V_M 0805_X5R

VHCORE

C925 10U_6.3V_M 0805_X5R
C926 10U_6.3V_M 0805_X5R
C927 10U_6.3V_M 0805_X5R
C928 10U_6.3V_M 0805_X5R
C929 10U_6.3V_M 0805_X5R

VHCORE

C930 10U_6.3V_M 0805_X5R
C931 10U_6.3V_M 0805_X5R
C932 10U_6.3V_M 0805_X5R
C933 10U_6.3V_M 0805_X5R
C934 10U_6.3V_M 0805_X5R

VHCORE

C935 10U_6.3V_M 0805_X5R
C936 10U_6.3V_M 0805_X5R
C5244 22P_50V_J 0402_NPO
C5245 22P_50V_J 0402_NPO

For RF Noise

U67F

VHCORE

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

CPU SOCKET_989P
FOX_PZ98927-3641-01F

CPU CORE SUPPLY

1.1V RAIL POWER

VTT0_1 AH14
VTT0_2 AH12
VTT0_3 AH11
VTT0_4 AH10
VTT0_5 J14
VTT0_6 J13
VTT0_7 H14
VTT0_8 H12
VTT0_9 G14
VTT0_10 G13
VTT0_11 G12
VTT0_12 G11
VTT0_13 F14
VTT0_14 F13
VTT0_15 F12
VTT0_16 F11
VTT0_17 E14
VTT0_18 E12
VTT0_19 D14
VTT0_20 D13
VTT0_21 D12
VTT0_22 D11
VTT0_23 C14
VTT0_24 C13
VTT0_25 C12
VTT0_26 C11
VTT0_27 B14
VTT0_28 B12
VTT0_29 A14
VTT0_30 A13
VTT0_31 A12
VTT0_32 A11

18A (SV) (VTT)

+1_05V_VTT

C911 10U_6.3V_M 0805_X5R
C912 10U_6.3V_M 0805_X5R
C913 10U_6.3V_M 0805_X5R
C914 10U_6.3V_M 0805_X5R
C915 10U_6.3V_M 0805_X5R

+1_05V_VTT

C738 22U_6.3V_M 0805_X5R
C640 22U_6.3V_M 0805_X5R
C629 22U_6.3V_M 0805_X5R

C916 10U_6.3V_M 0805_X5R
C917 10U_6.3V_M 0805_X5R
C918 NC_10U_6.3V_M 0805_X5R
C919 NC_10U_6.3V_M 0805_X5R

18A (SV) (VTT)

VTT0_33 AF10
VTT0_34 AE10
VTT0_35 AC10
VTT0_36 AB10
VTT0_37 Y10
VTT0_38 W10
VTT0_39 U10
VTT0_40 T10
VTT0_41 J12
VTT0_42 J11
VTT0_43 J16
VTT0_44 J15

+1_05V_VTT

C893 22U_6.3V_M 0805_X5R
C506 22U_6.3V_M 0805_X5R

+1_05V_VTT

+1_05V_VTT_43 R858 0 J 0603
+1_05V_VTT_44 R859 0 J 0603

POWER

CPU VIDS

PSI# AN33 → PSI# 78,79

VID[0] AK35 → VID0 78,79
VID[1] AK33 → VID1 78,79
VID[2] AK34 → VID2 78,79
VID[3] AL35 → VID3 78,79
VID[4] AL33 → VID4 78,79
VID[5] AM33 → VID5 78,79
VID[6] AM35 → VID6 78,79

PROC_DPRSLPVR AM34 PROC_DPRSLPVR R860 0 J 0402 → PM_DPRSLPVR 78,79

VTT_SELECT G15 VTT_SELECT 1 TP1114 20MIL

SENSE LINES

ISENSE AN35 → IMVP_IMON 78

VCC_SENSE AJ34 VCCSENSE → VCCSENSE 78
VSS_SENSE AJ35 VSSSENSE → VSSSENSE 78

VTT_SENSE B15 → VTT_SENSE 75
VSS_SENSE_VTT A15 VSS_SENSE_VTT 1 TP178 20MIL

VHCORE

R27 100_F 0402
R19 100_F 0402

Analog Signal

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: ARD (POWER)
Size: Custom
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For Disable Arrandale Graphic
VAXG should be connected to GND when disable iGPU.

For Disable Arrandale Graphic
VAXG_SENSE and VSSAXG_SENSE on Arrandale can be left as no connect.

For Disable Arrandale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH. FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

GFXCORE

22A (ARD iGPU)

C587 SG_22U_6.3V_M 0805_X5R
C576 SG_22U_6.3V_M 0805_X5R
C938 SG_10U_6.3V_M 0805_X5R
C937 SG_10U_6.3V_M 0805_X5R

CAP18 NC_100U_6.3V_M 3528
CAP19 NC_100U_6.3V_M 3528
CAP20 NC_100U_6.3V_M 3528
R938 NV_0_J 0402

U67G

GRAPHICS POWER

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

SENSE LINES
VAXG_SENSE AR22
VSSAXG_SENSE AT22
GFX_VCC_SENSE 80
GFX_VSS_SENSE 80

GRAPHICS VIDs
GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24
GFX_VID0 80
GFX_VID1 80
GFX_VID2 80
GFX_VID3 80
GFX_VID4 80
GFX_VID5 80
GFX_VID6 80

R401 NC_10K_J 0402

GFX_VR_EN AR25
GFX_DPRSLPVR AT25
GFX_IMON AM24
GFX_VR_EN 80
GFX_IMON 80

R1604 NV_1K_J 0402

+1_5VSUS_CPU

3A (VDDQ)

DDR3 - 1.5V RAILS
VDDQ1 AJ1
VDDQ2 AF1
VDDQ3 AE7
VDDQ4 AE4
VDDQ5 AC1
VDDQ6 AB7
VDDQ7 AB4
VDDQ8 Y1
VDDQ9 W7
VDDQ10 W4
VDDQ11 U1
VDDQ12 T7
VDDQ13 T4
VDDQ14 P1
VDDQ15 N7
VDDQ16 N4
VDDQ17 L1
VDDQ18 H1

C1146 1U_10V_K 0603_X5R
C1147 1U_10V_K 0603_X5R
C1148 1U_10V_K 0603_X5R
C1149 1U_10V_K 0603_X5R
C1150 1U_10V_K 0603_X5R
C832 22U_6.3V_M 0805_X5R
C833 22U_6.3V_M 0805_X5R
CAP23 NC_100U_6.3V_M 3528

+1_05V_VTT
R864 0_J 0603
+V1_05S_VTT_FDI
C824 22U_6.3V_M 0805_X5R
C819 22U_6.3V_M 0805_X5R

18A (SV) (VTT)

FDI
VTT1_45
VTT1_46
VTT1_47

+1_05V_VTT
R866 0_J 1206
+V1_05S_VTT_PEG_DMI
C828 22U_6.3V_M 0805_X5R
C827 22U_6.3V_M 0805_X5R
C826 22U_6.3V_M 0805_X5R
C825 22U_6.3V_M 0805_X5R

PEG & DMI
K26 VTT1_48
J27 VTT1_49
J26 VTT1_50
J25 VTT1_51
H27 VTT1_52
G28 VTT1_53
G27 VTT1_54
G26 VTT1_55
F26 VTT1_56
E26 VTT1_57
E25 VTT1_58

1.1V
VTT0_59 P10
VTT0_60 N10
VTT0_61 L10
VTT0_62 K10
+V1_05S_VCCTTA_DDR
C940 10U_6.3V_M 0805_X5R
C939 10U_6.3V_M 0805_X5R
R868 0_J 0603
+1_05V_VTT

18A (SV) (VTT)

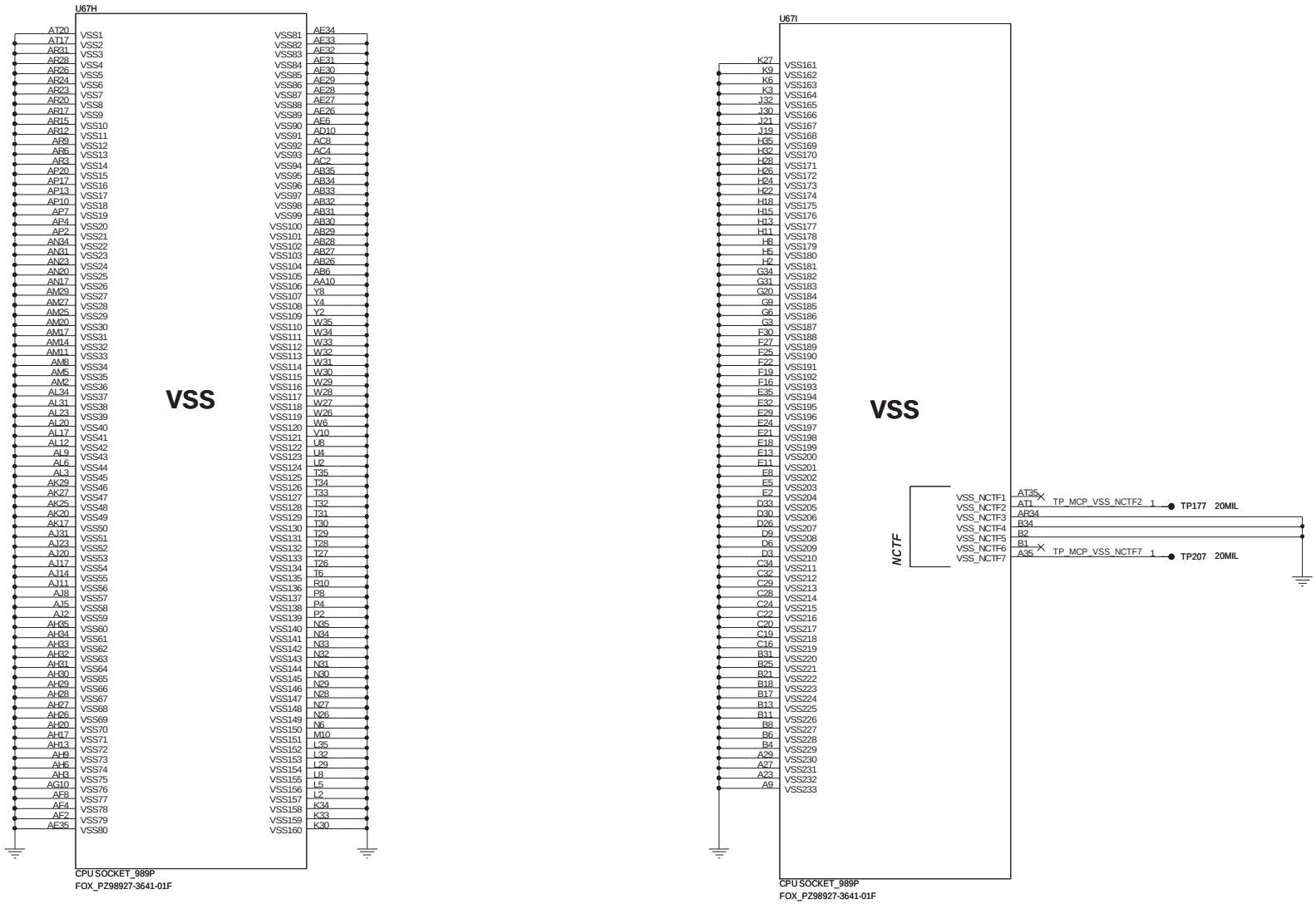
VTT1_63 J22
VTT1_64 J20
VTT1_65 J18
VTT1_66 H21
VTT1_67 H20
VTT1_68 H19
+V1_05S_VCC_SA
C830 22U_6.3V_M 0805_X5R
C829 22U_6.3V_M 0805_X5R
R869 0_J 0603
+1_05V_VTT

1.8V
VCCPLL1 L26
VCCPLL2 L27
VCCPLL3 M26
VCCPLL_1.8V
C941 1U_10V_K 0603_X5R
C942 1U_10V_K 0603_X5R
C943 2.2U_10V_M 0603_X5R
C944 4.7U_10V_K 0805_X5R
C831 22U_6.3V_M 0805_X5R
R870 0_J 0805
+1_8VRUN

1.35A (VCCPLL)

CPU SOCKET_989P
FOX_PZ98927-3641-01F

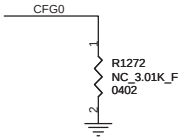
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (GRAPHICS POWER)	
Size: Custom	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 7 of 86	



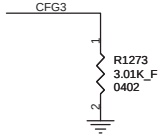
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: ARD (GND)		
Size: Custom	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 8 of 86	

PCI Express Configuration Select
CFG0 1 : Single PEG
0 : Bifurcation enable

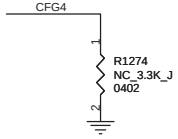
3393727 The VIL Voltage DC Specification for CFG[0] Pin is in Violation of the EDS Value by a Large Amount
The Clarksfield EDS Vol1 documents the CFG[1:0] pins for PCI Express Port Bifurcation, the straps may not work correctly when using a pull down resistor of value other than 250 Ohms to drive a value of zero on the CFG[0] pin. When left floating a value of one is sensed and there is no impact in this case.

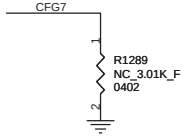


CFG3 PCI Express Static Lane Reversal
CFG3 1 : Normal Operation
0 : Lane Numbers Reversed
15 ->0 , 14-> 1 , ...



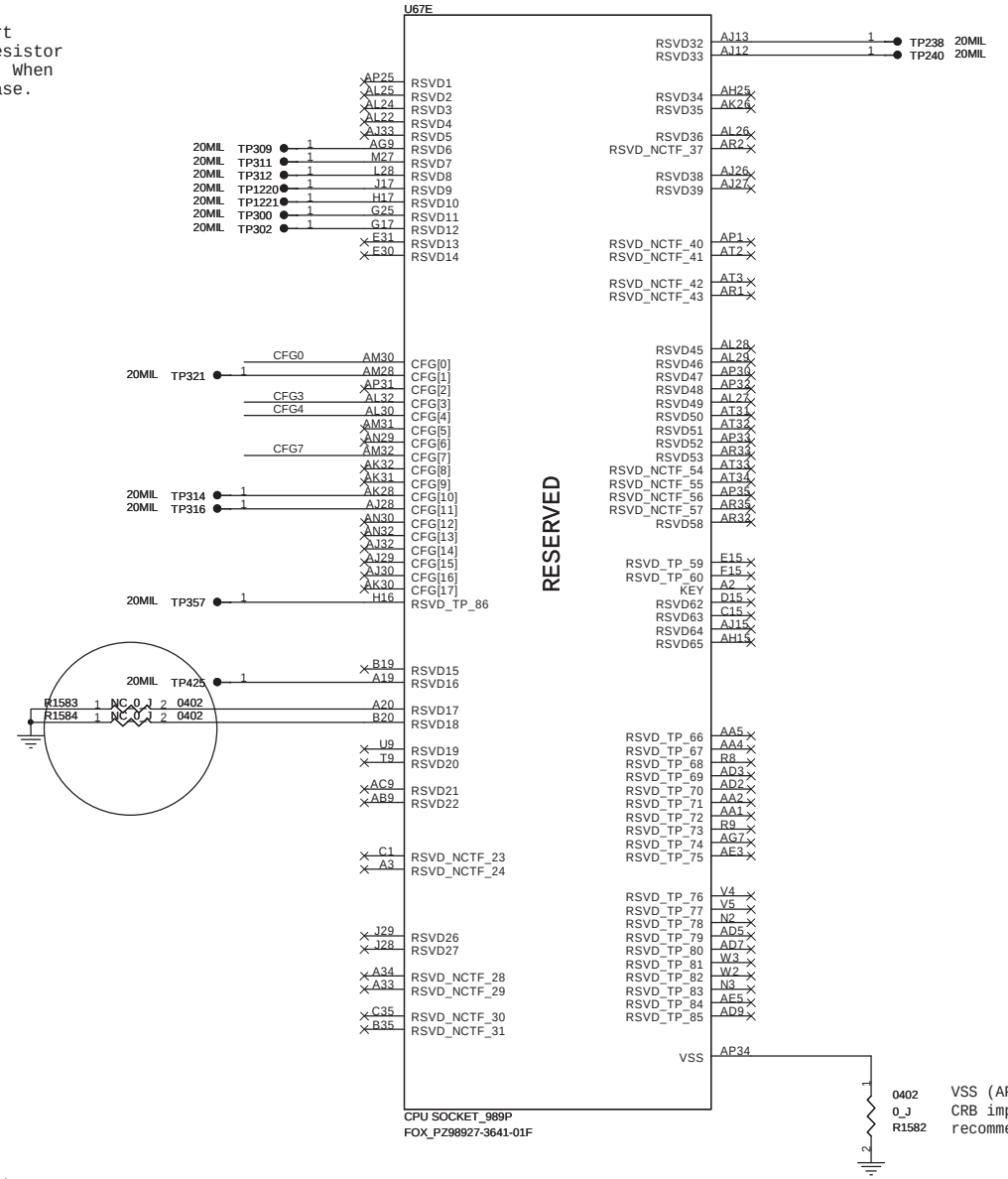
CFG4 Display Port Presence
CFG4 1 : Disabled ; No Physical Display Port attached to Embedded Display Port
0 : Enable ; An external Display Port device is connected to the Embedded Display Port





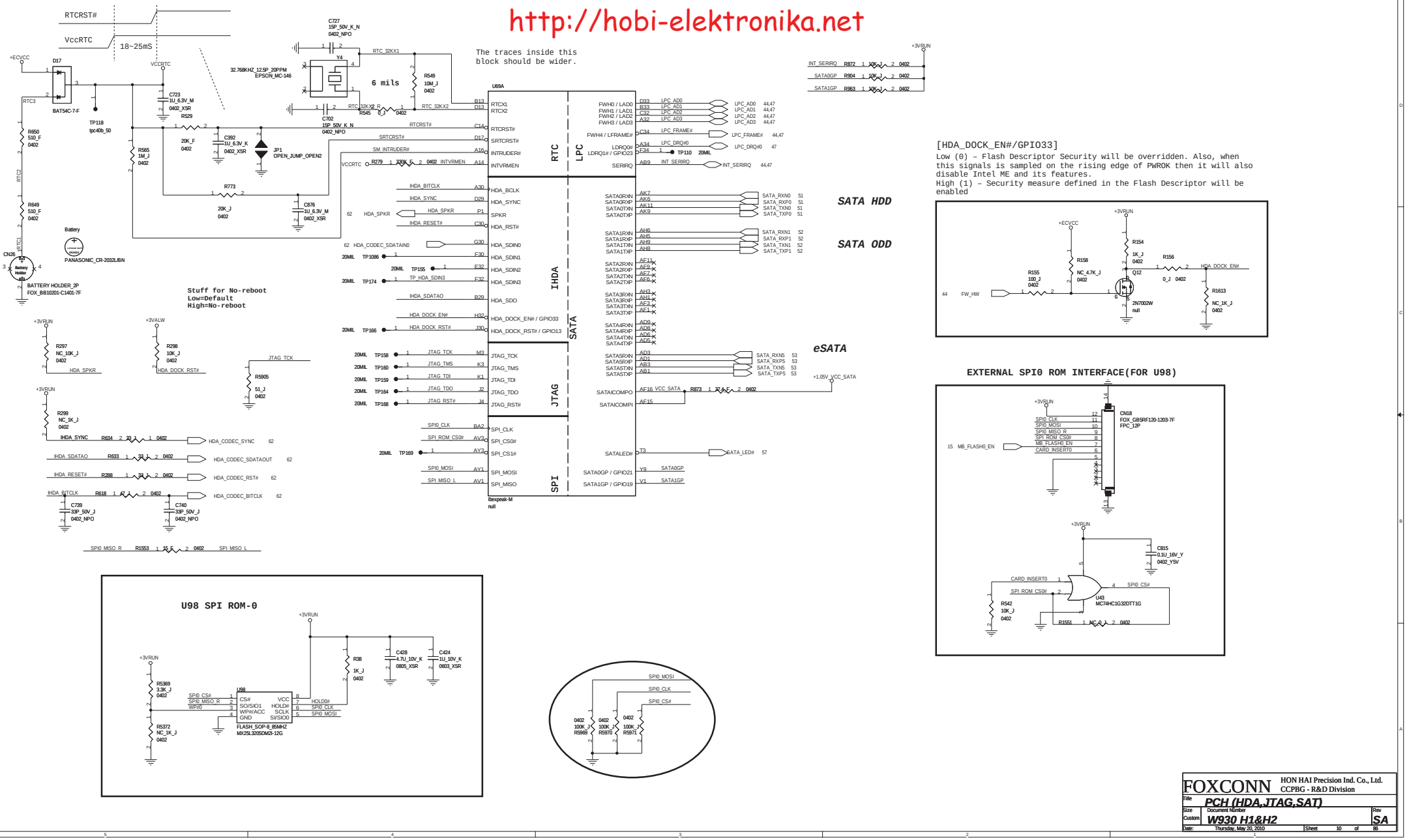
2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down).
Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: ARD (RESERVED)		
Size: A3	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 9 of 86	

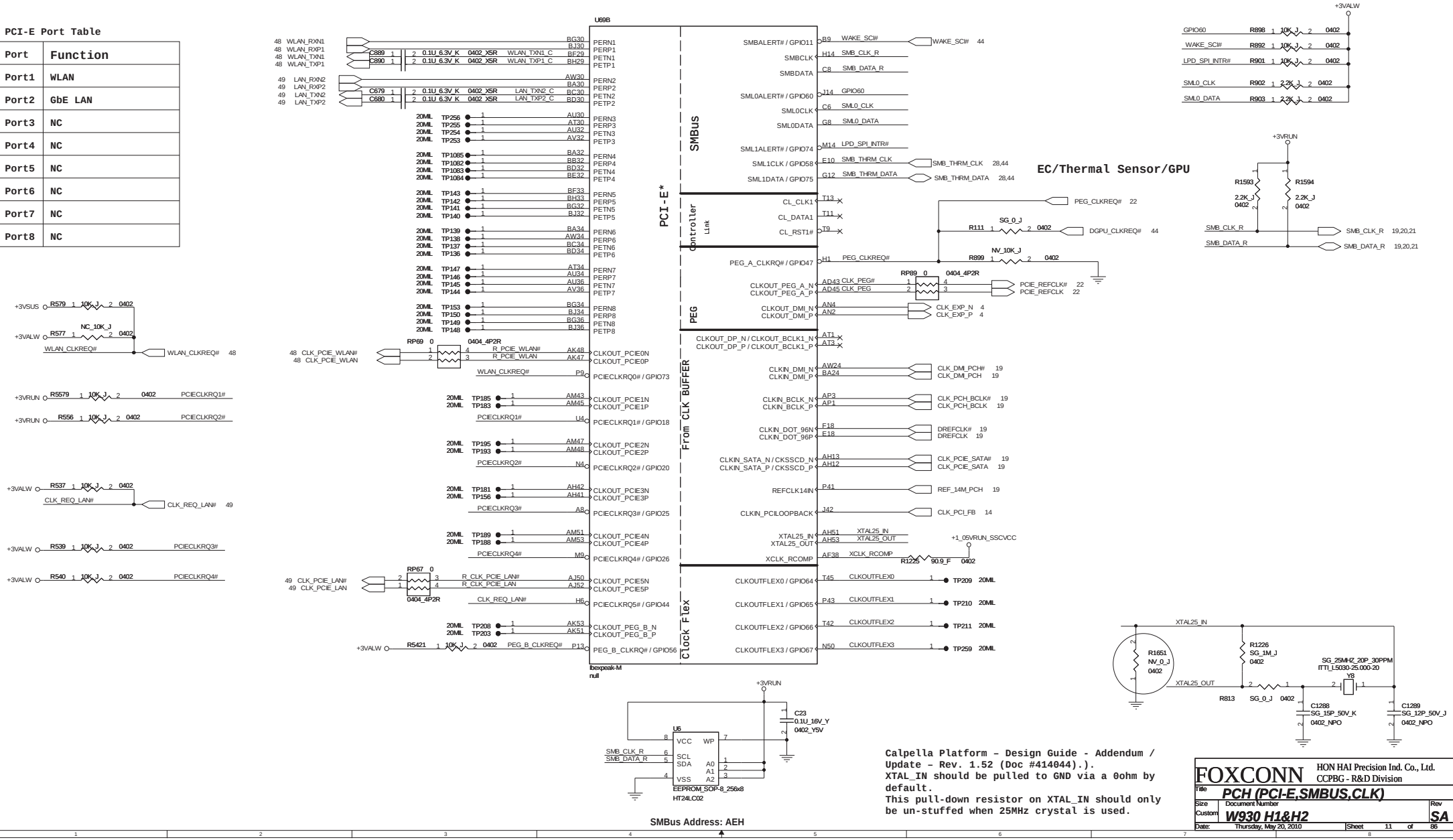


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (HDA,JTAG,SAT)		
Size: Custom	Document Number: W930 H1&H2		Rev: SA
Date: Thursday, May 20, 2010		Sheet 10 of 86	

PCH EEPROM/CKG/DIMM

PCI-E Port Table

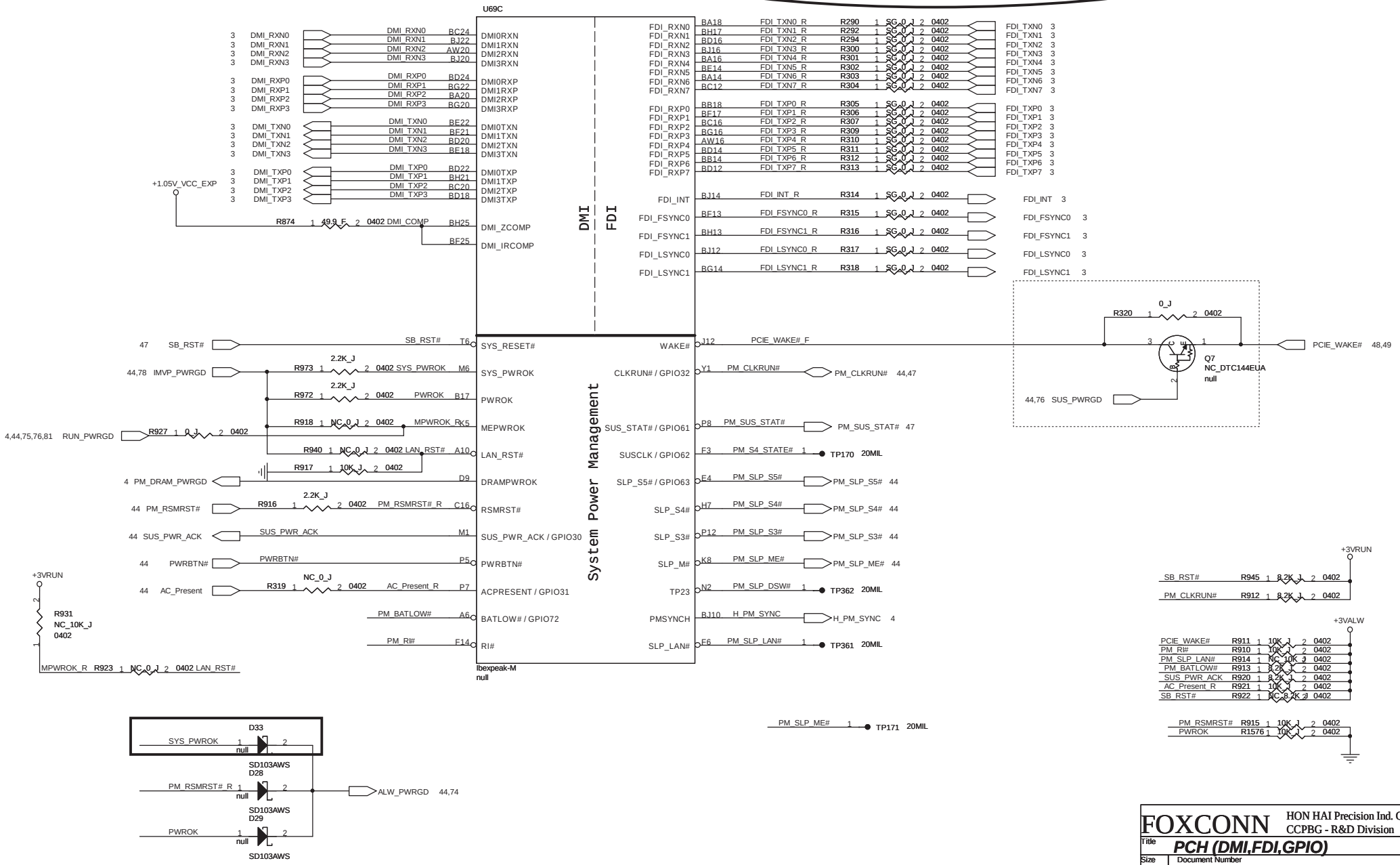
Port	Function
Port1	WLAN
Port2	GbE LAN
Port3	NC
Port4	NC
Port5	NC
Port6	NC
Port7	NC
Port8	NC



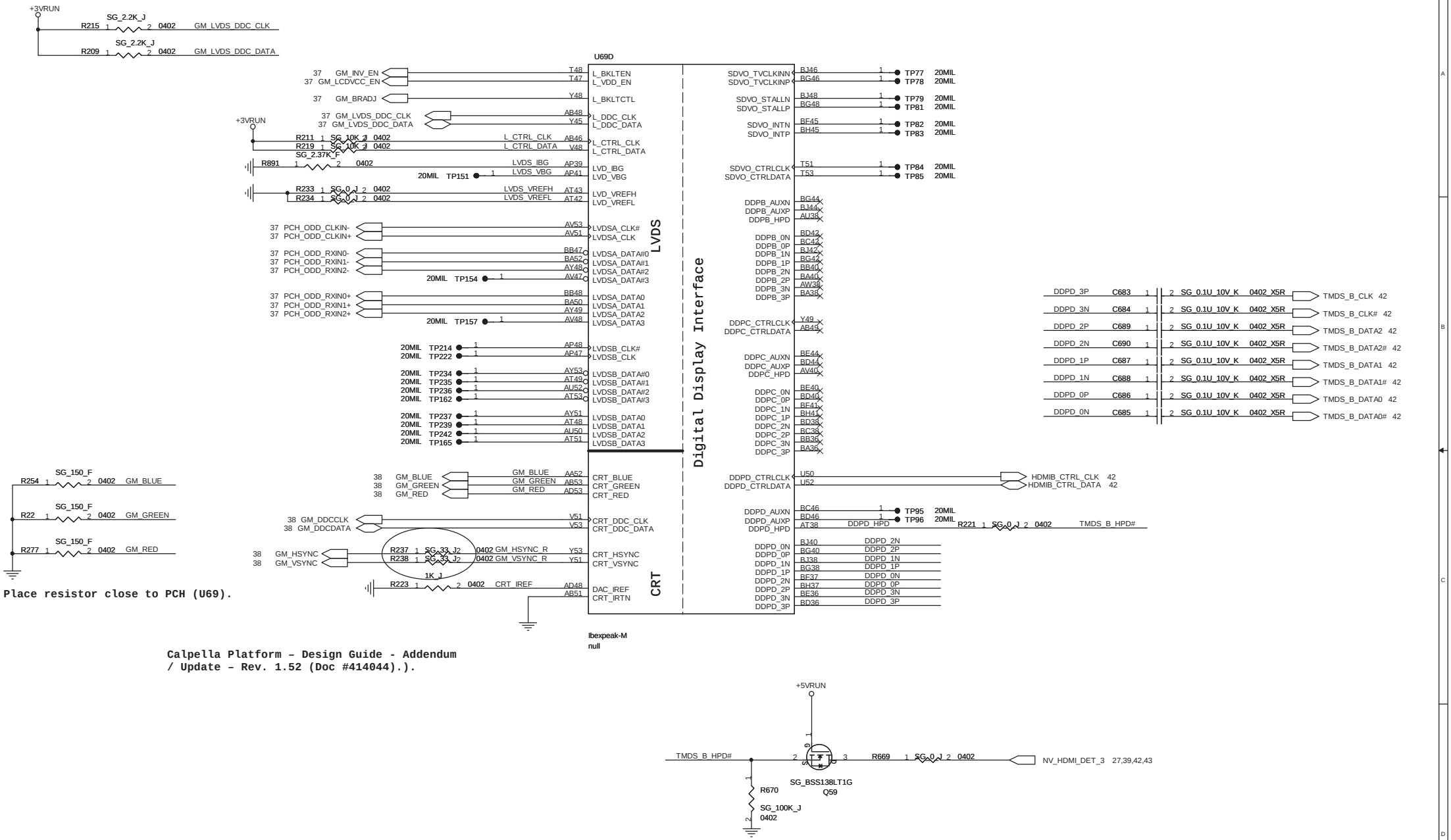
Calpella Platform – Design Guide - Addendum / Update – Rev. 1.52 (Doc #414044).).
XTAL_IN should be pulled to GND via a 0ohm by default.
This pull-down resistor on XTAL_IN should only be un-stuffed when 25MHz crystal is used.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (PCI-E,SMBUS,CLK)	
Size: Custom	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 11 of 86	

For Disable Arrandale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH. FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (DMI,FDI,GPIO)		
Size A3	Document Number W930 H1&H2		Rev SA
Date: Thursday, May 20, 2010		Sheet 12 of 86	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (LVDS,DDI)	
Size: Custom	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 13 of 86	

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Danbury Technology
Disabled when Low
Enabled when High

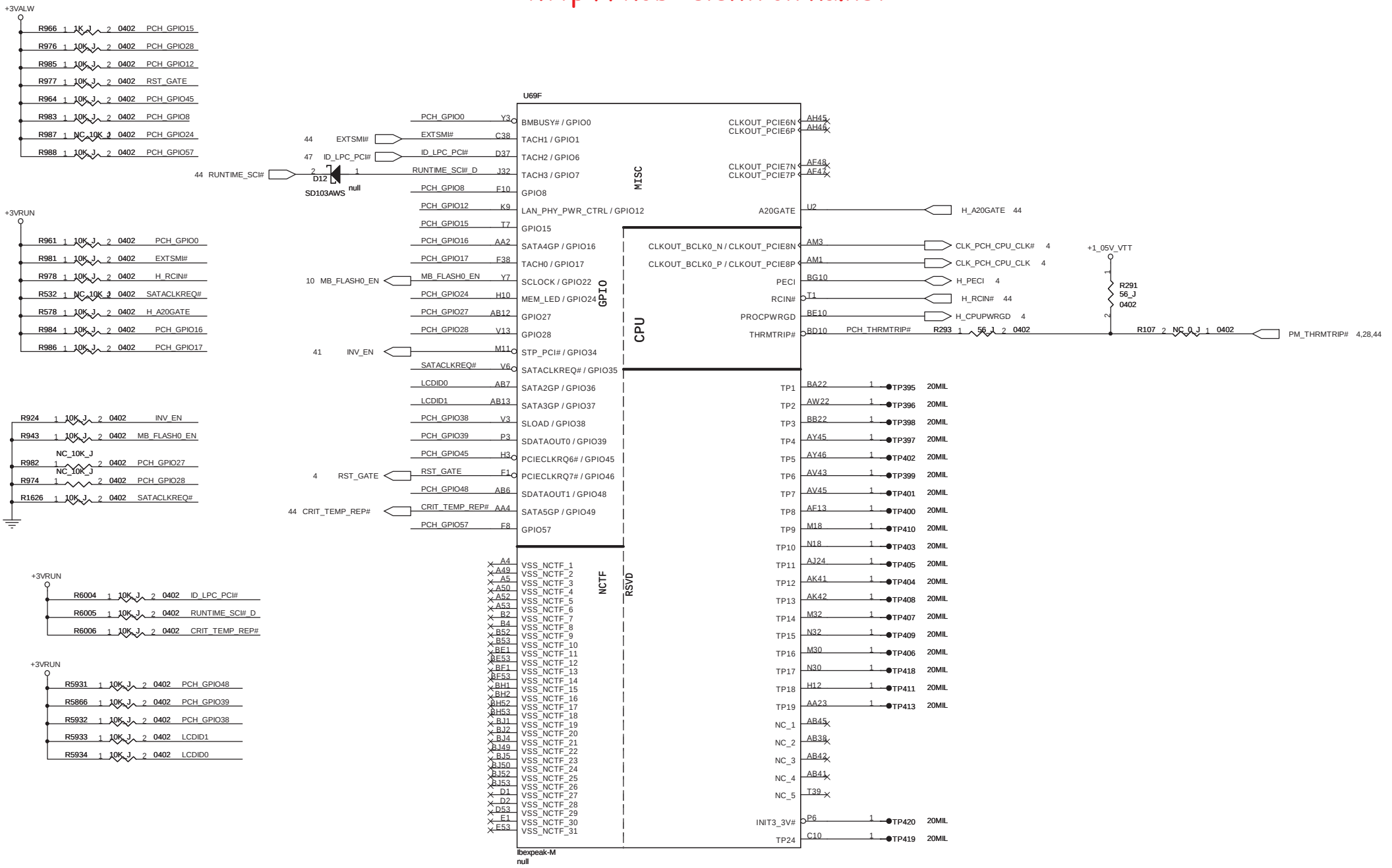
USB PORT	Function
PORT-0	eSATA
PORT-1	External Port-1
PORT-2	External Port-2
PORT-3	Bluetooth
PORT-4	NC
PORT-5	Camera
PORT-6	NC
PORT-7	NC
PORT-8	Cardreader
PORT-9	WLAN
PORT-10	External Port-3
PORT-11	NC
PORT-12	NC
PORT-13	NC

Reserve for BIOS Reset
Place close to DIMM door

Buffer to reduce loading on PLT_RST#.

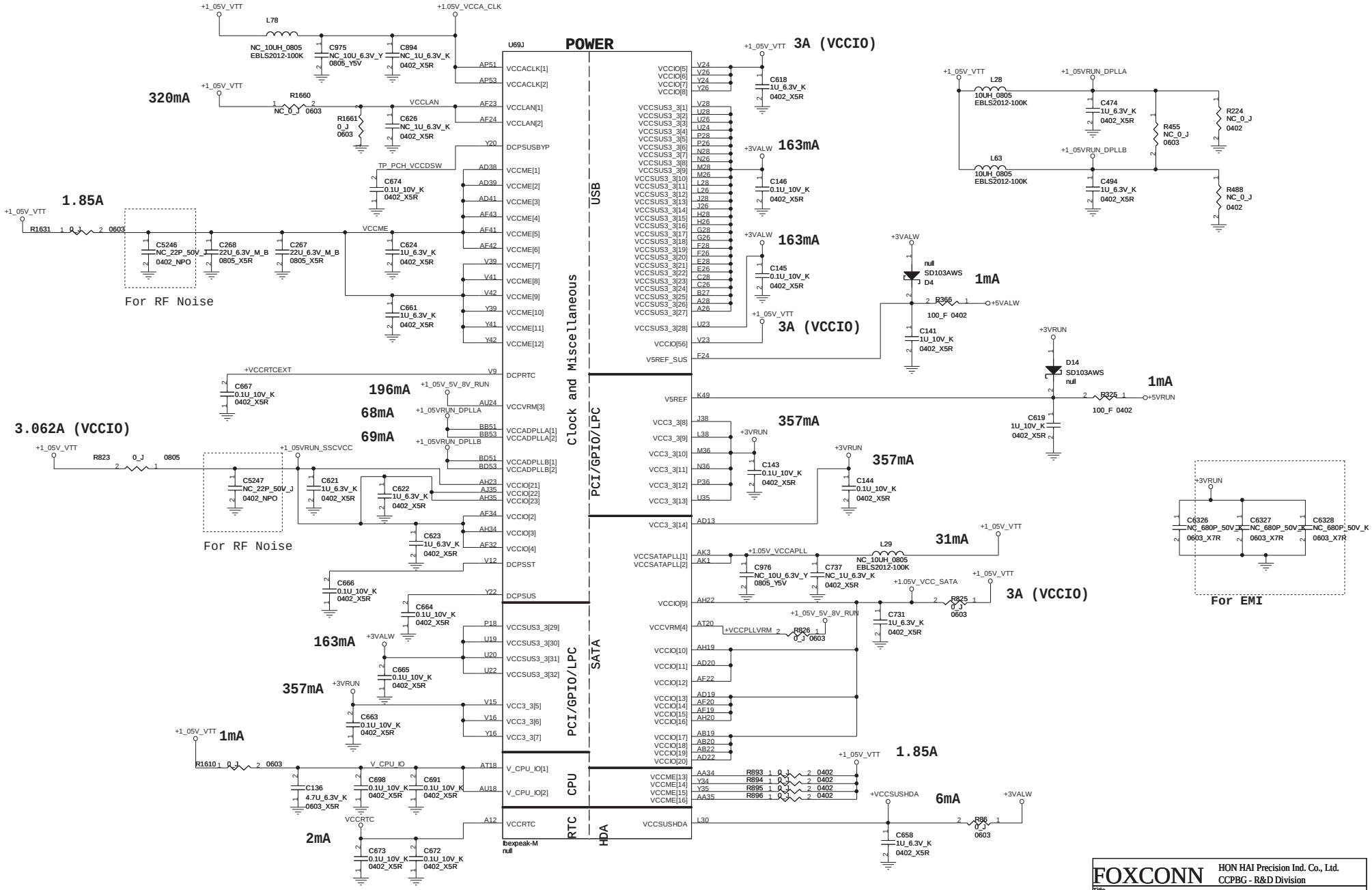
In case of BIOS flash failed, the system may not boot OS.
Our BIOS will implement a feature, when short the pad,
BIOS will perform crisis recovery.
If possible, please put the pad near the DIMM door,
then end-user will be easily to recover their BIOS.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (PCI,USB,NVRAM)		
Size A3	Document Number W930 H1&H2		Rev SA
Date: Thursday, May 20, 2010	Sheet 14 of 86		

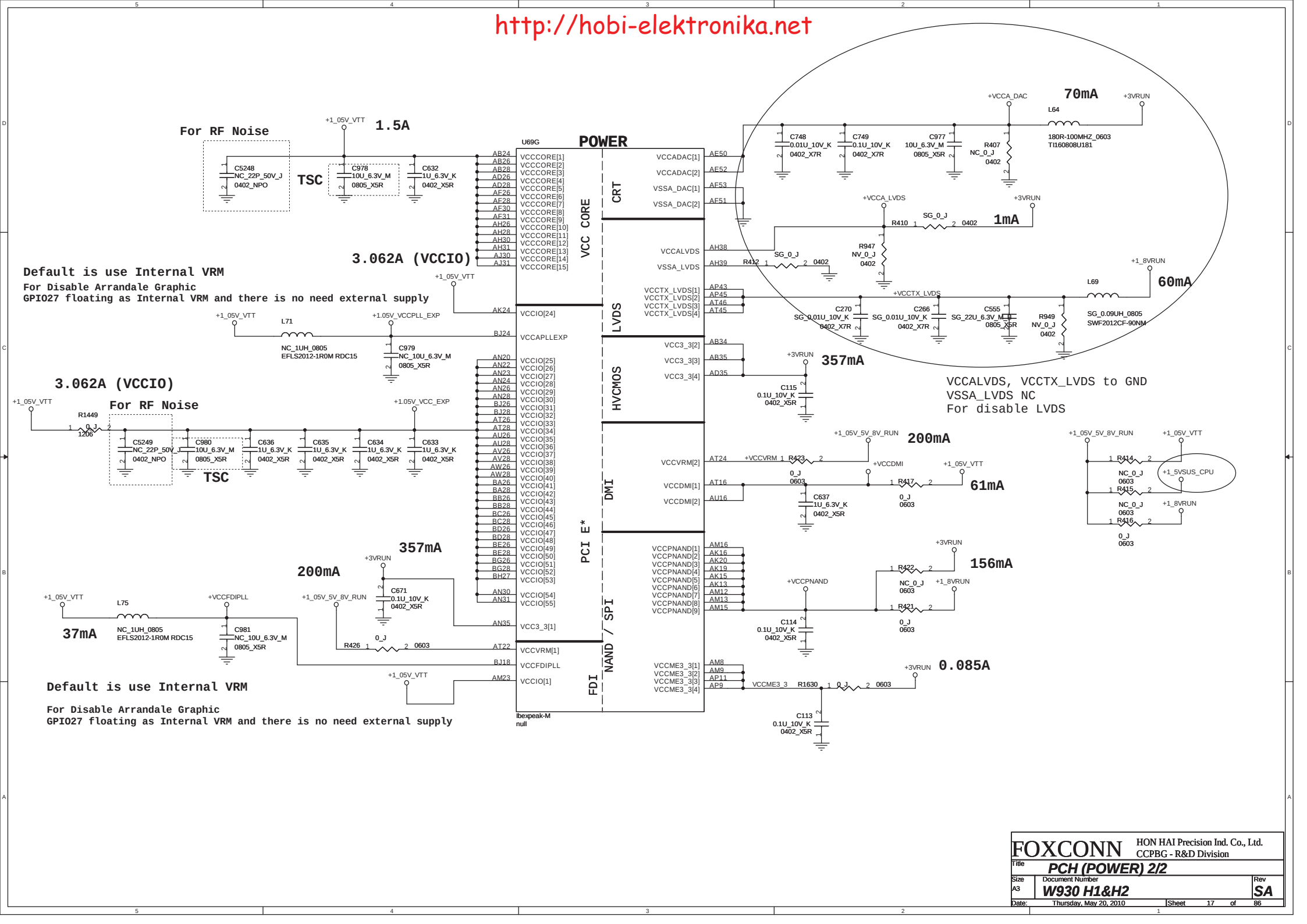


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (GPIO,VSS_NCTF,RSVD)	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 15 of 86	

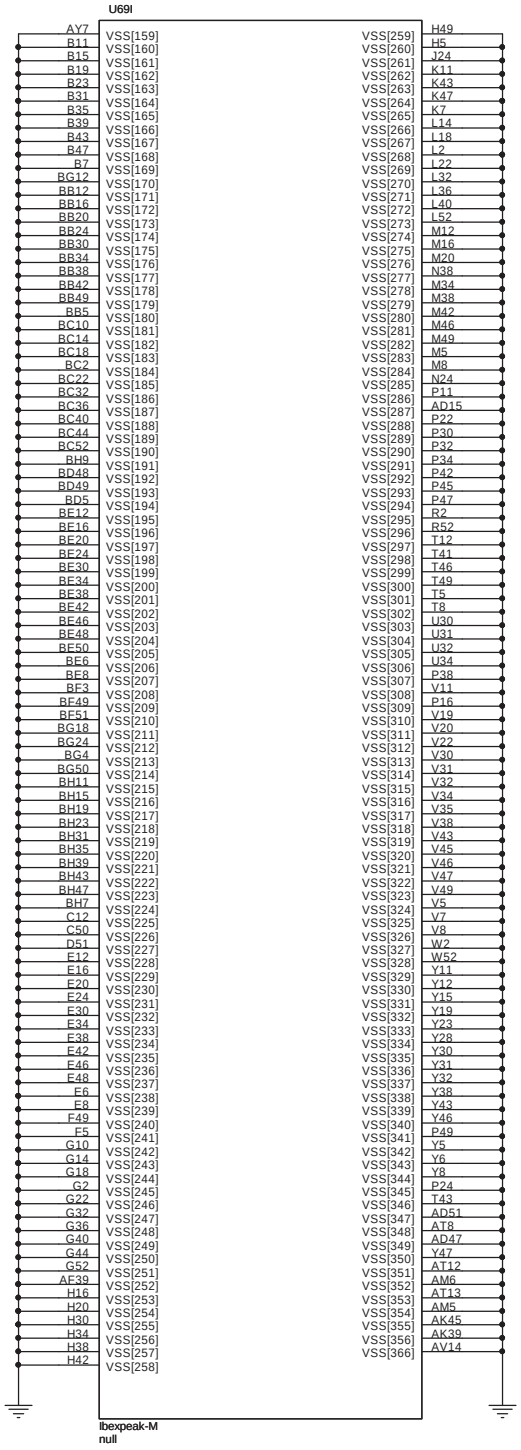
Default is use Internal VRM
For Disable Arrandale Graphic
GPIO27 floating as Internal VRM and there is no need external supply

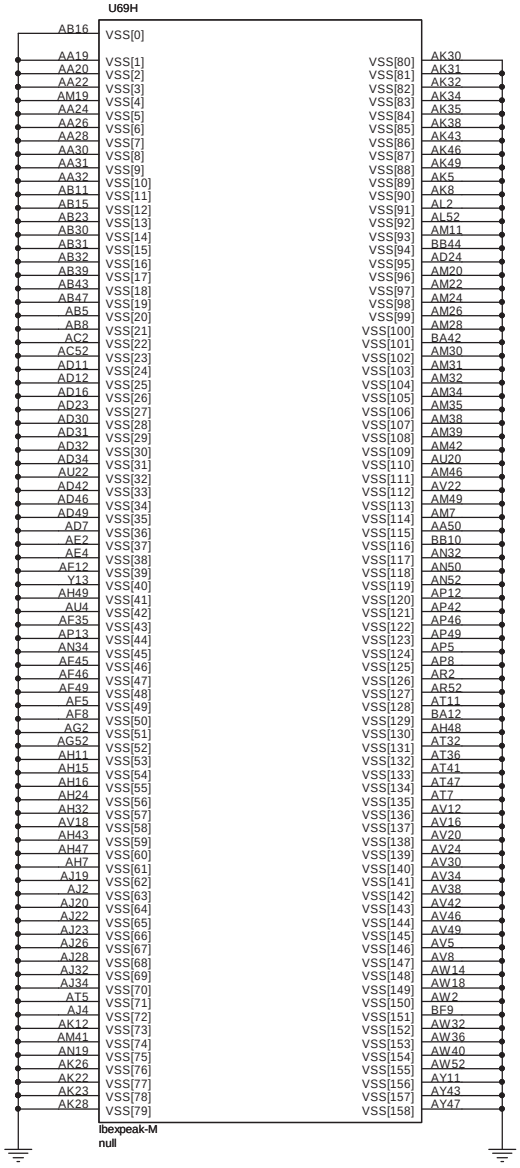


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (POWER) 1/2		
Size: Custom	Document Number: W930 H1&H2		Rev: SA
Date: Thursday, May 20, 2010	Sheet 16 of 86		

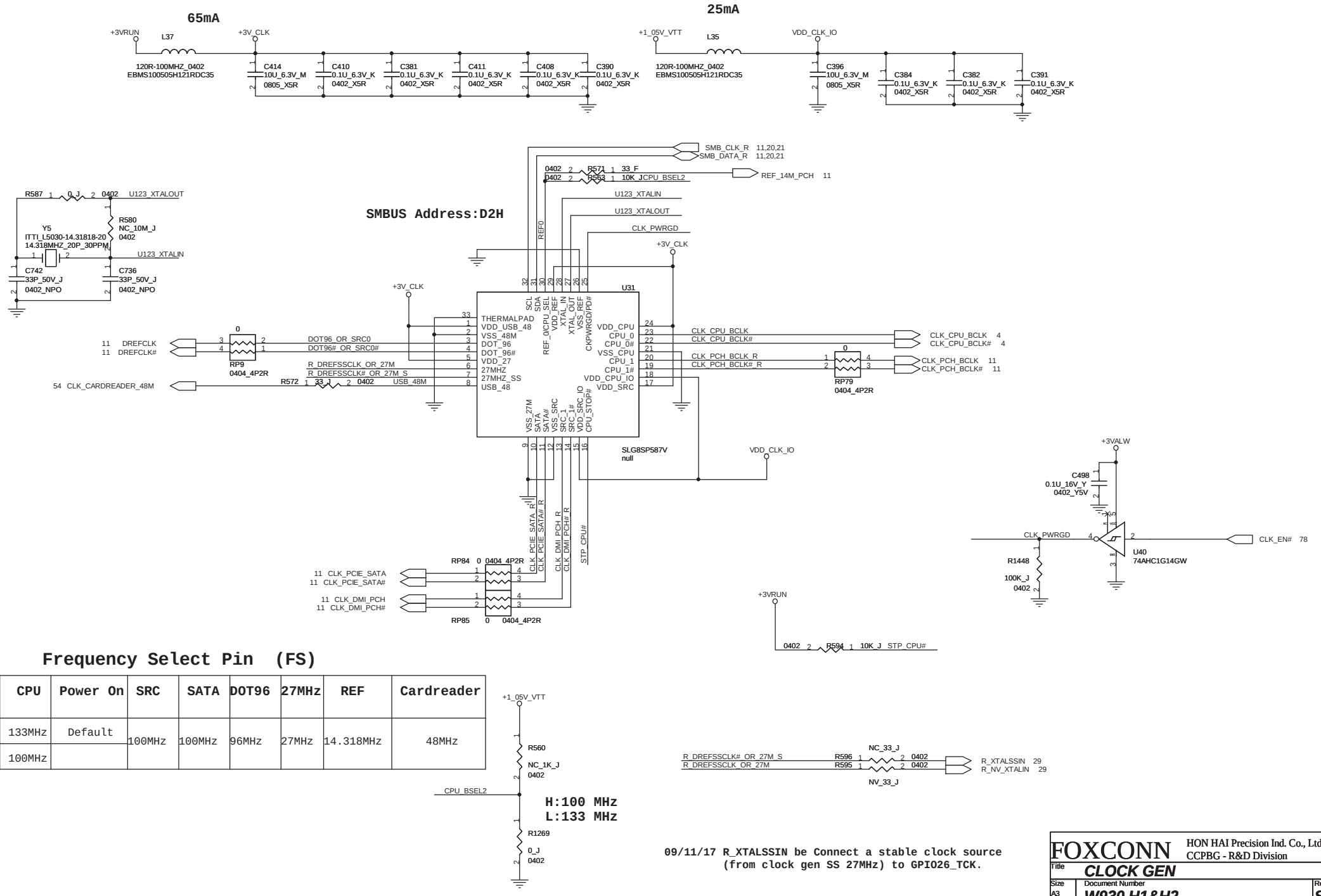


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (POWER) 2/2	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 17 of 86	





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (VSS)	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 18 of 86	

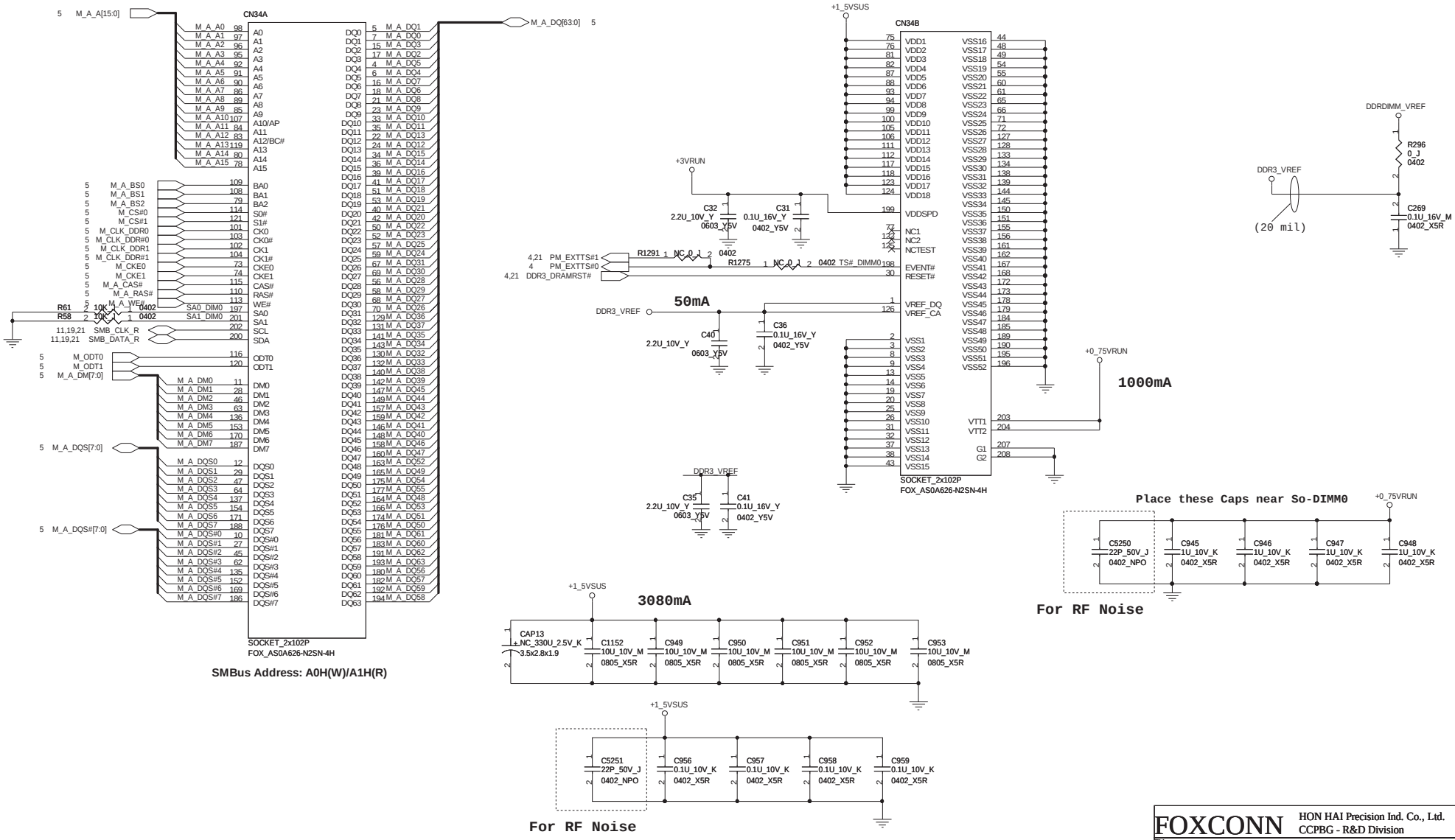


Frequency Select Pin (FS)

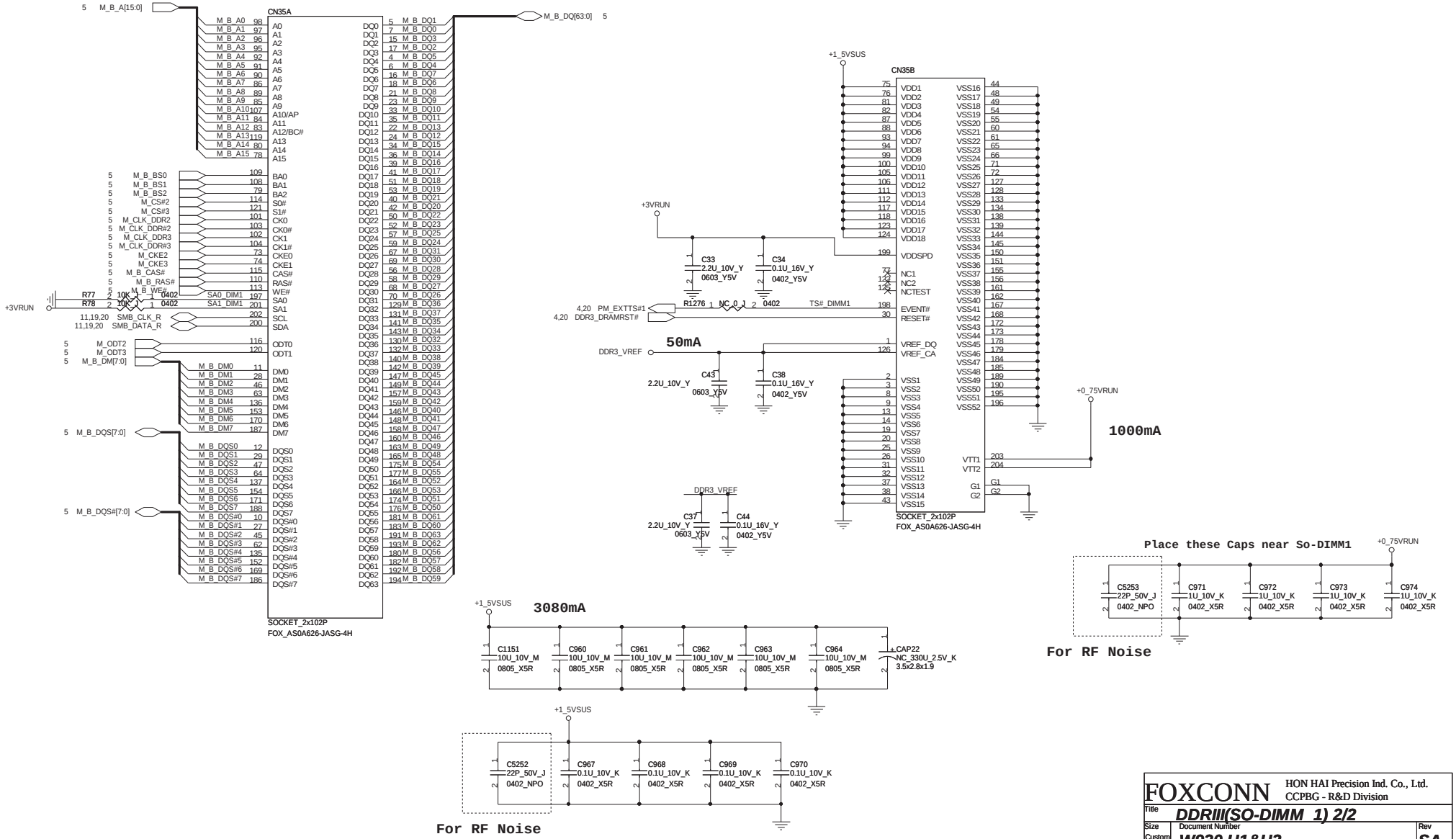
FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF	Cardreader
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz	48MHz
1	100MHz							

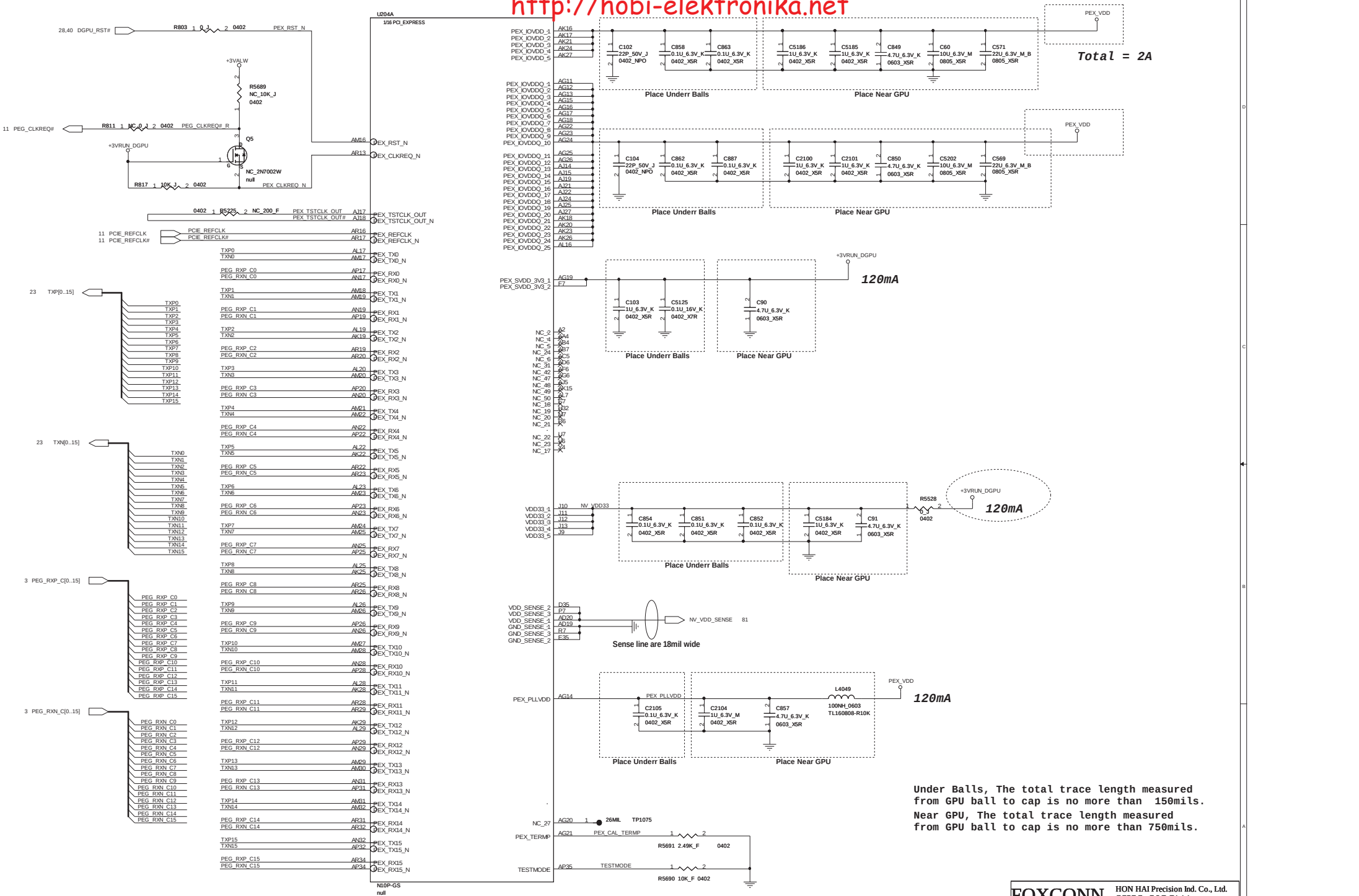
H:100 MHz
L:133 MHz

09/11/17 R_XTALSSIN be Connect a stable clock source (from clock gen SS 27MHz) to GPIO26_TCK.

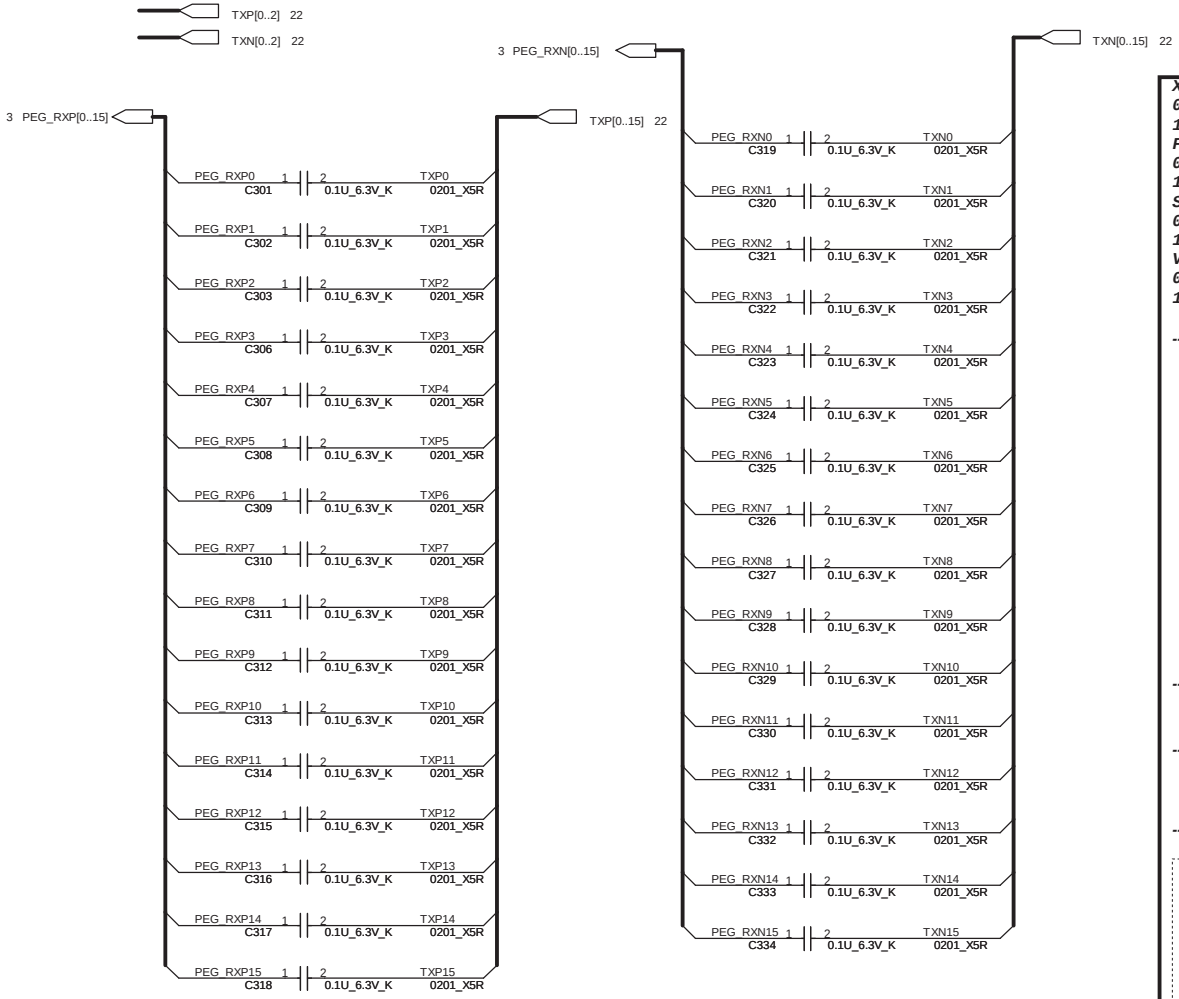


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDRIII(SO-DIMM_0) 1/2	
Size: Custom	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 20 of 86	

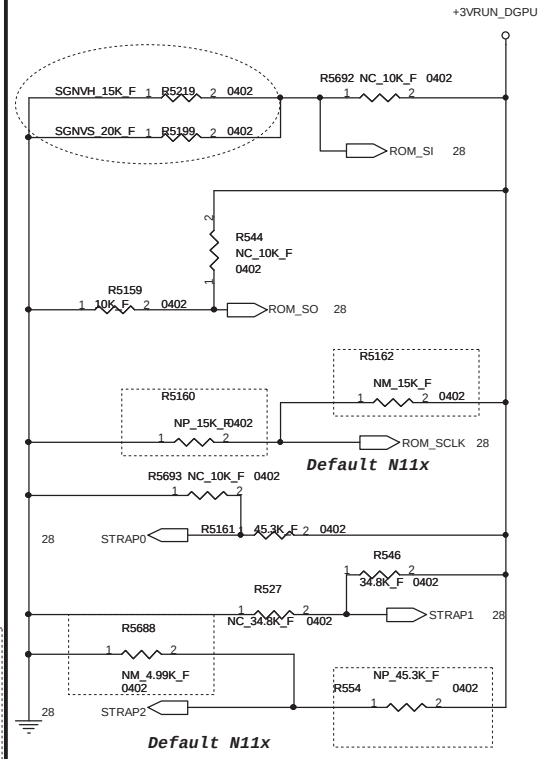




FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VGA (PCI-E) 1/9	
Size: Custom	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 22 of 86	



XCLK_417 0 (277M Hz) 1 (Reserved) FB_0_BAR_SIZE 0 256MB 1 (Reserved) SMB_ALT_ADDR 0 0x9E 1 0x9C(multi-GPU usage) VGA_DEVICE 0 3D device(class code 302h) 1 VGA device(class code 300h)	ROM_SO 0001
PCIE DEVID[4] 0 (N11P-GS1) 1 (N11M-GE2-B) SUB_VENDOR 0 (No vedio BIOS ROM) 1 (BIOS ROM is present) SLOT_CLK_CFG 0 (GPU and MCH not share a common reference clk) 1 (GPU and MCH share a common reference clk) PEX_PLL_EN_TERM 0 (Disable) 1 (Enable)	ROM_SCLK N11P-GS1 0010 N11M-GE2-B 1010
USER[3:0] 1111 EDID Enable	STRAP0 (1111)
N10x/N11x 3GIO_PADCFG[3:0] 0110 Notebook	STRAP1 (1110)
N11X PCI_DEVID[3:0] N11P-GS1 1111b N11M-GE2-B 0000b PCI DEVICE IDs N11P-GS1 (0x0CAF) N11M-GE2-B (0x0A70)	Strap2 N11P-GS1 1111 N11M-GE2-B 0000



ROM_SI

0000 64-bit Reserved
0010 64Mx16 DDR3 - 96 ball 128-bit Hynix(13-H5T01G6-3000) 15K Pull Low.
0011 64Mx16 DDR3 - 96 ball 128-bit Samsung(13-K4W1G16-3000) 20K pull Low

Logical Strap bit Mapping

Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	BGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

Refer to <GB1 Family Design Guide DG-04202-001_v02_secured>

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (PCI-E BUS)Strap 2/9

Size: Custom | Document Number: W930 H1&H2 | Rev: SA

Date: Thursday, May 20, 2010 | Sheet 23 of 86

5.85A (N11P-GS1)

3.98A (N11M-GE2)

For RF Noise

Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

	FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA(DDR)# 3/9		
Size: Custom	Document Number: W930 H1&H2		Rev: SA
Date: Thursday, May 20, 2010		Sheet 24 of 86	

5.42A (N11P-GS1)
3.98A (N11M-GE2)

+1_5VRUN_DGPU

C5208 10P_50V_J 0402_NPO
C883 0.1U_6.3V_K 0402_X5R
C882 0.1U_6.3V_K 0402_X5R
C879 NP_0.1U_6.3V_K 0402_X5R
C888 0.047U_16V_K 0402_X7R
C884 0.047U_16V_K 0402_X7R
C5209 NP_0.047U_16V_K 0402_X7R

Place Under Balls

C2108 4.7U_6.3V_K 0603_X5R
C867 NP_4.7U_6.3V_K 0603_X5R
C6019 0.01U_10V_K 0402_X7R
C6020 0.01U_10V_K 0402_X7R
C6021 NP_0.01U_10V_K 0402_X7R
C6018 NP_0.01U_10V_K 0402_X7R
C5256 22P_50V_J 0402_NPO

Place Near GPU
Place Under Balls
Place Near GPU

For RF Noise

Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

U204C
3/16 FBC
N10P-GS
null

33,34 FBCD[0:63]
33,34 FBCDQM[7..0]
33,34 FBCWDQS[7..0]
33,34 FBCRDQS[7..0]

FBVDDQ_26 FBVDDQ_29 FBVDDQ_30 FBVDDQ_31 FBVDDQ_32 FBVDDQ_33 FBVDDQ_34 FBVDDQ_35 FBVDDQ_36 FBVDDQ_37 FBVDDQ_38

FBC_CMD0 FBC_CMD1 FBC_CMD2 FBC_CMD3 FBC_CMD4 FBC_CMD5 FBC_CMD6 FBC_CMD7 FBC_CMD8 FBC_CMD9 FBC_CMD10 FBC_CMD11 FBC_CMD12 FBC_CMD13 FBC_CMD14 FBC_CMD15 FBC_CMD16 FBC_CMD17 FBC_CMD18 FBC_CMD19 FBC_CMD20 FBC_CMD21 FBC_CMD22 FBC_CMD23 FBC_CMD24 FBC_CMD25 FBC_CMD26 FBC_CMD27 FBC_CMD28 FBC_CMD29 FBC_CMD30

FBC_RAS# 33,34
FBC_BA1 33,34
FBD_CKE 34
FBD_CS0# 34
FBC_CAS# 33,34
FBC_WE# 33,34
FBC_BA0 33,34
FBC_RESET 33,34
FBC_CKE 33
FBC_BA2 33,34
FBD_ODT 34
FBC_CS0# 33
FBC_ODT 33

FBC_A[0..13] 33,34
FBD_A[2..5] 34

	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

FBC_CLK0 FBC_CLK0# FBC_CLK1 FBC_CLK1#
FBC_CLK0 33
FBC_CLK0# 33
FBC_CLK1 34
FBC_CLK1# 34

+1_5VRUN_DGPU
R5560 NC_60.4_F 0402
FBC_DEBUG

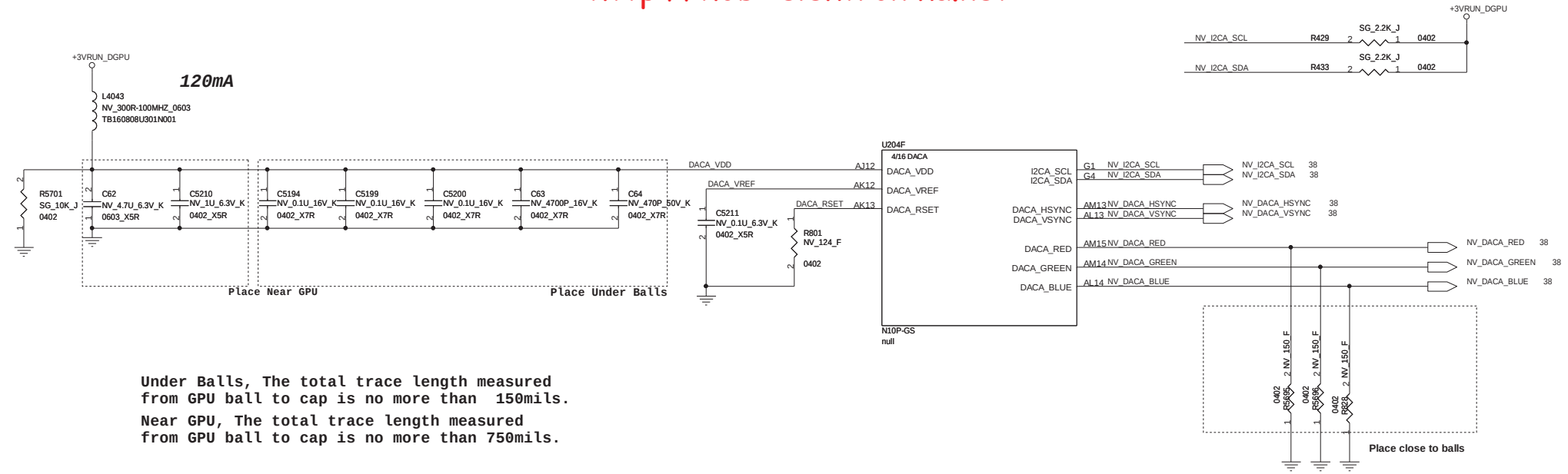
NC_34 NC_35 NC_32 NC_33 NC_38 NC_39 NC_36 NC_37

NC_16 NC_15
26MIL TP131
26MIL TP1077

+1_5VRUN_DGPU
FB_CAL_PD_VDDQ R5529 40.2_F 0402
FB_CAL_PU_GND R5163 40.2_F 0402 NP_40.2_F
FB_CAL_TERM_GND R812 NM_60.4_F 0402
R5562 0402

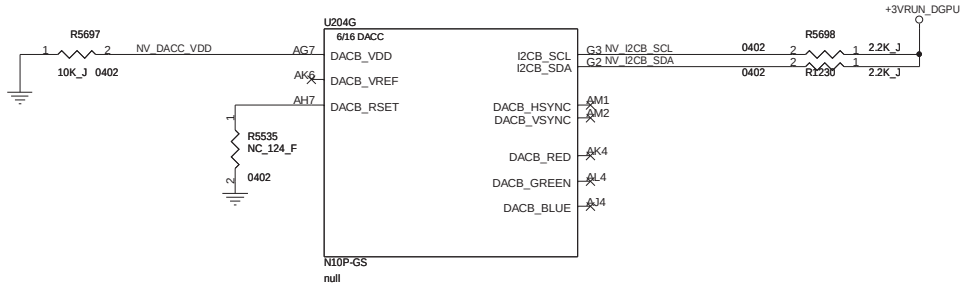
PLACE CLOSE TO BALLS

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	VGA(DDR)# 4/9		
Size Custom	Document Number W930 H1&H2		Rev SA
Date: Thursday, May 20, 2010		Sheet 25 of 86	

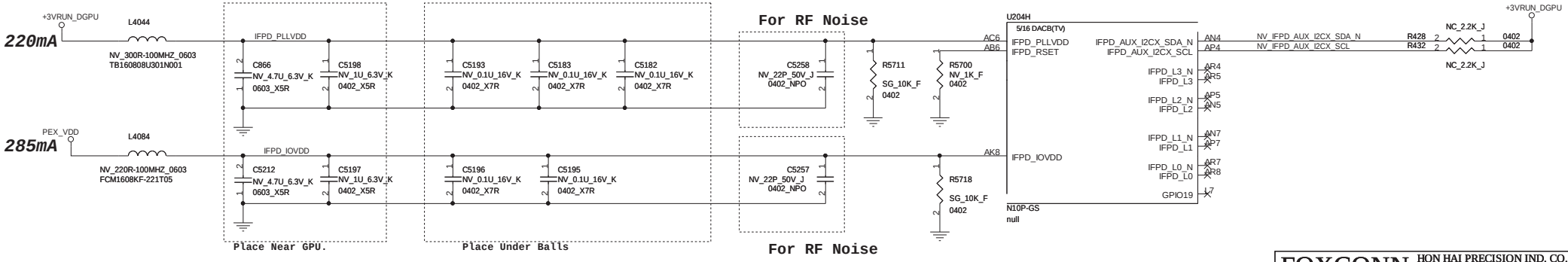


Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

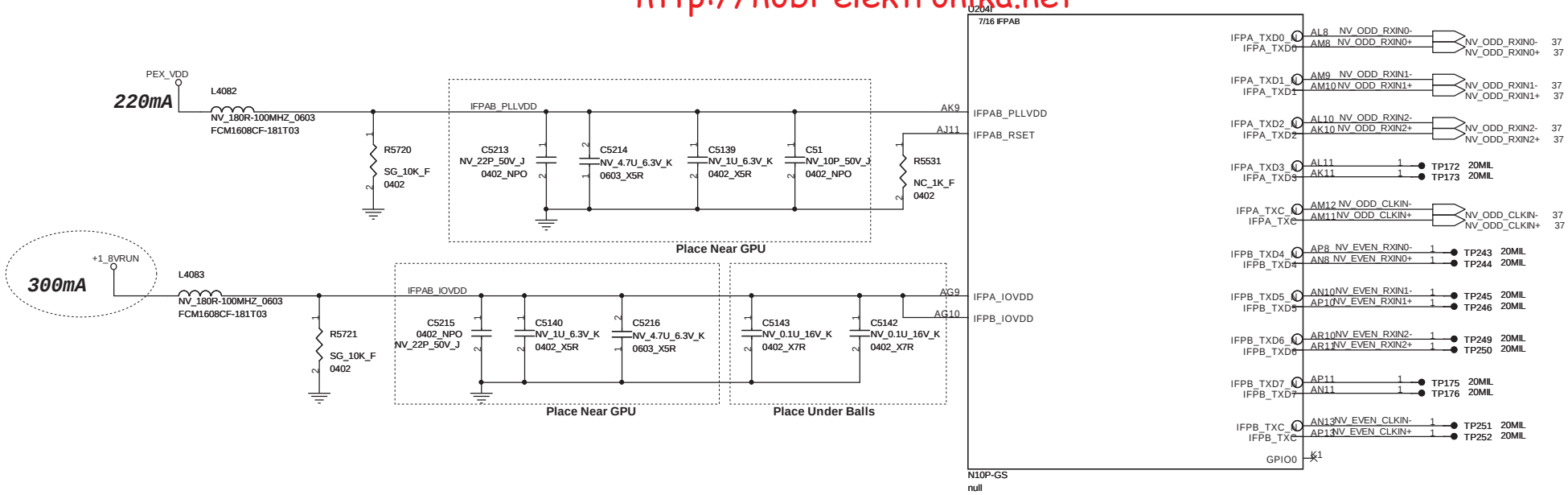
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

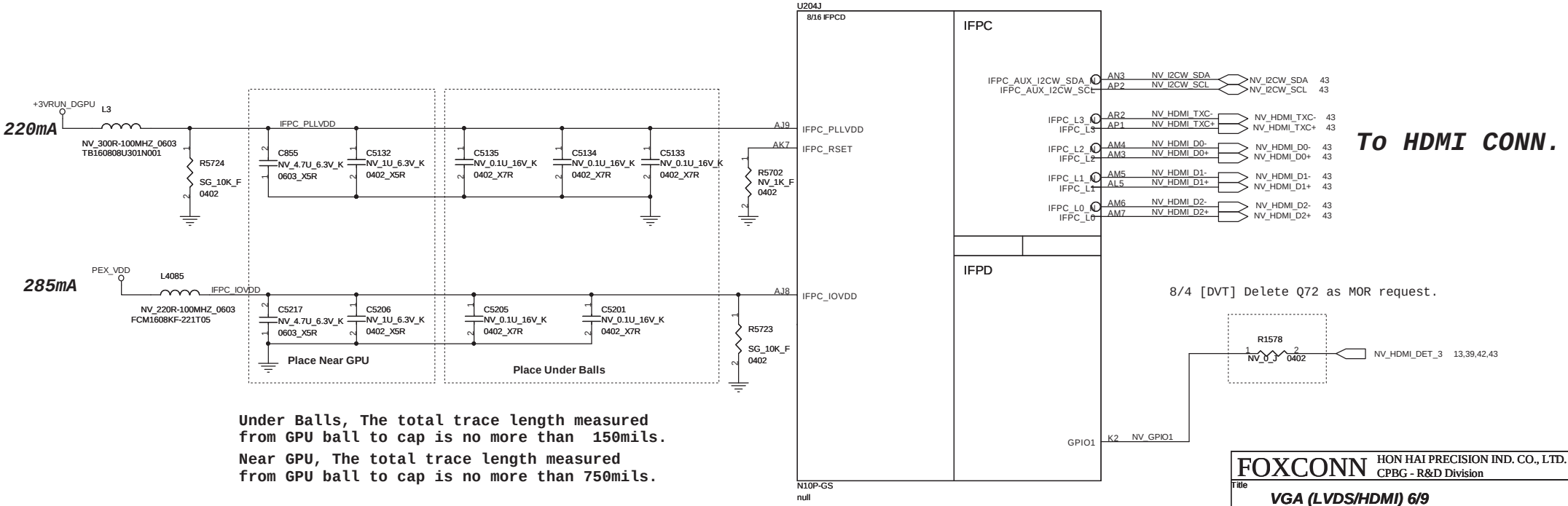


DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDATA	SDA



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	VGA(CRT/eDP) 5/9		
Size: Custom	Document Number: W930 H1&H2		Rev: SA
Date: Thursday, May 20, 2010	Sheet 26 of 86		





To HDMI CONN.

8/4 [DVT] Delete Q72 as MOR request.

Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

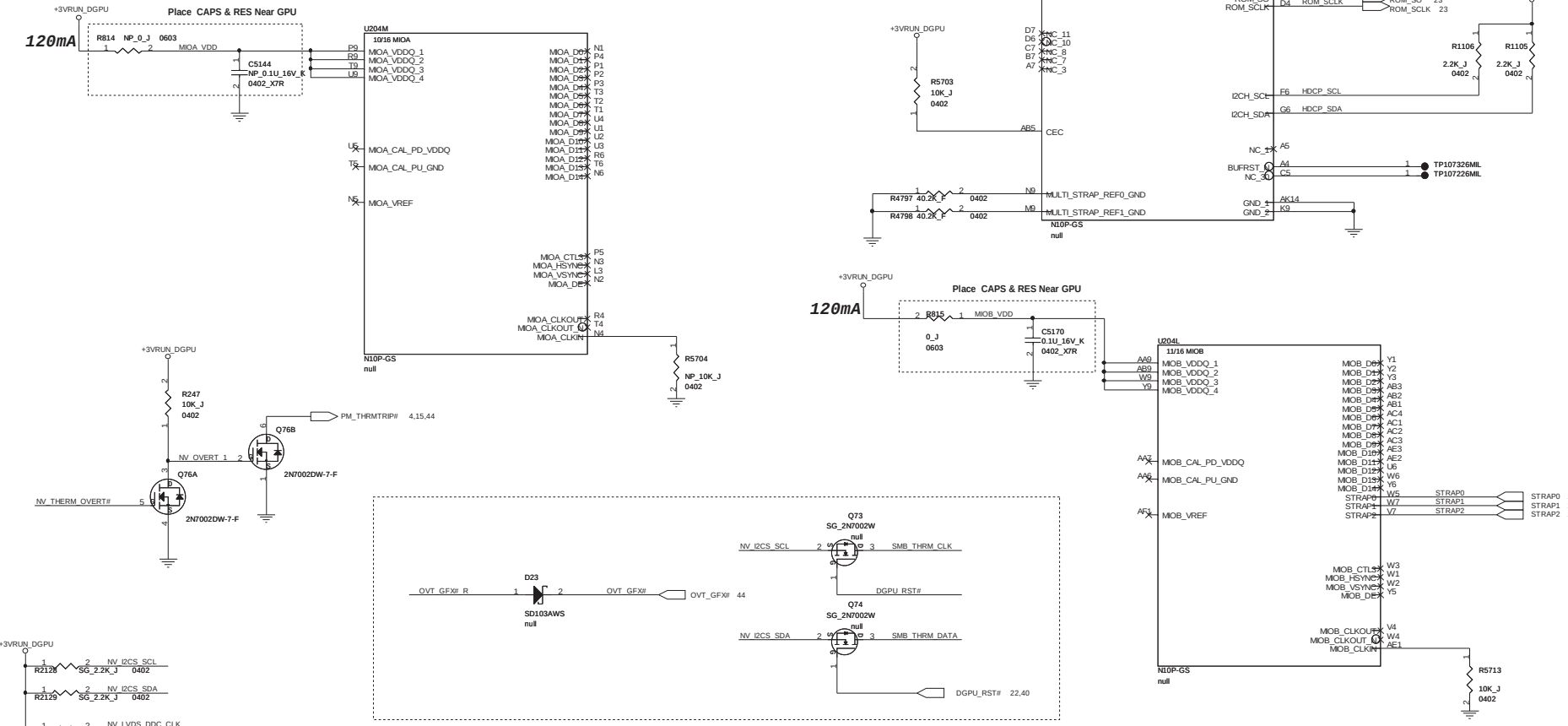
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (LVDS/HDMI) 6/9

Size: A3 | Document Number: W930 H1&H2 | Rev: SA

Date: Thursday, May 20, 2010 | Sheet 27 of 86



GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	YES		
GPIO1	I	Yes	HDMI Hot Plug Detect 0(HPD0)	**Active High**
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	**Active High**
GPIO3	O	No	Panel Power(LCD0_VDD)	**Active High**
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN)	**Active High**
GPIO5	O	Yes	FOR Power Control NVDD	**Active High or Low**
GPIO6	O	No	FOR Power Control NVDD	**Active High or Low**
GPIO8	O	No	For GPU Thermaltrip	**Active Low**
GPIO9	I	No	System Power Limit Alert Input	**Active Low**

SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	For Panel EDID
I2CS_SCL I2CS_SDA	I/O	For VGA thermial I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor
I2CH_SCL I2CH_SDA	I/O	NC(for HDCP I2C_Compatibal Bus Signals)

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (XTAL/GPIO) 7/9

Size: Custom | Document Number: W930 H1&H2 | Rev: SA

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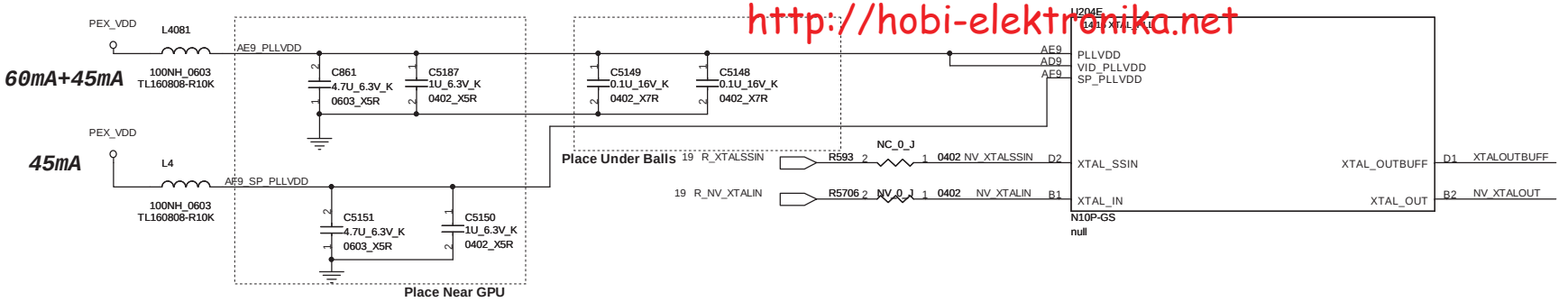

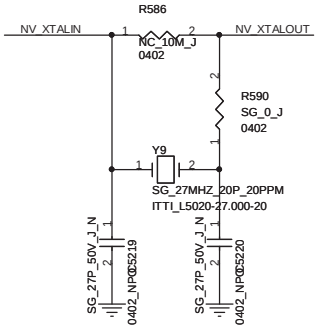

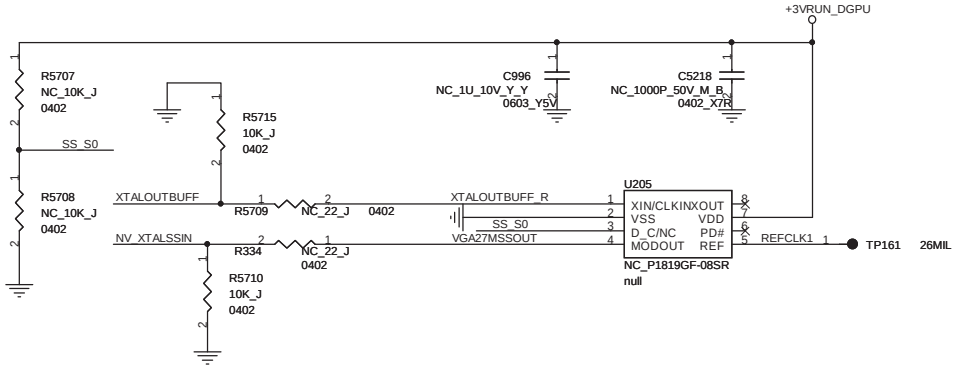

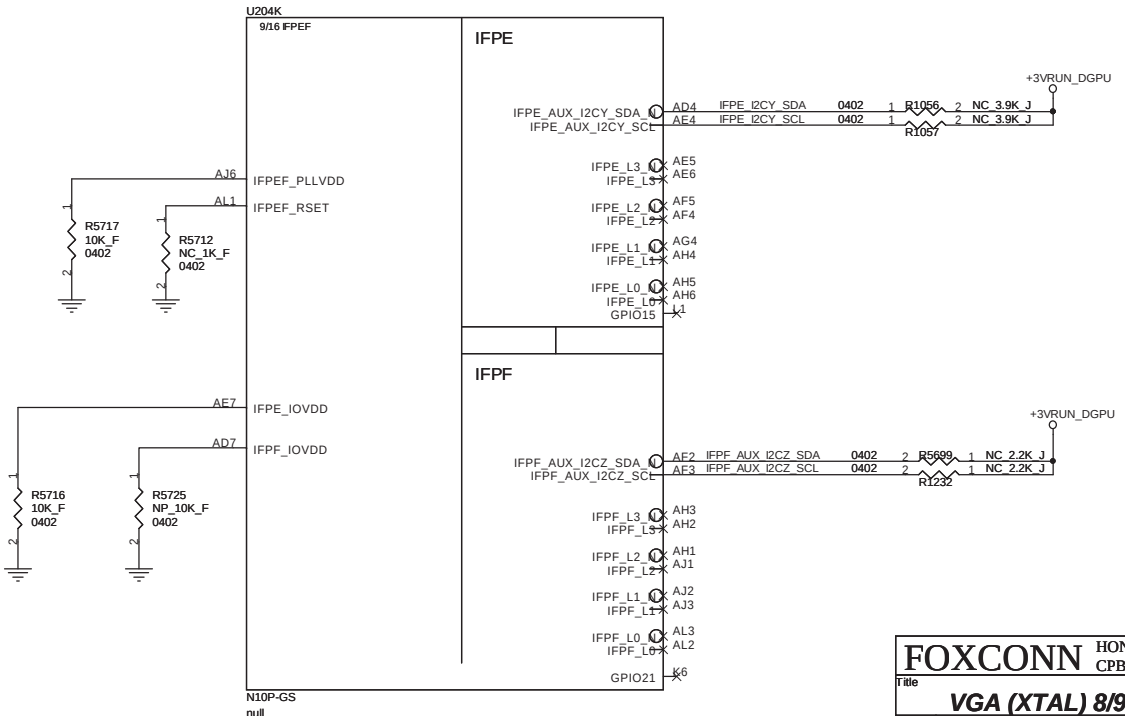

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA (XTAL) 8/9	
Size A3	Document Number W930 H1&H2	Rev SA
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28.85A (N11P-GS1)
16.09A (N11M-GE2)

NV_VDD

U204O
16/16 NVVDD

AB11	VDD_001	VDD_057 P21
AB13	VDD_002	VDD_058 P23
AB15	VDD_003	VDD_059 P25
AB17	VDD_004	VDD_060 R11
AB19	VDD_005	VDD_061 R12
AB21	VDD_006	VDD_062 R13
AB23	VDD_007	VDD_063 R14
AB25	VDD_008	VDD_064 R15
AC11	VDD_009	VDD_065 R16
AC12	VDD_010	VDD_066 R17
AC13	VDD_011	VDD_067 R18
AC14	VDD_012	VDD_068 R19
AC15	VDD_013	VDD_069 R20
AC16	VDD_014	VDD_070 R21
AC17	VDD_015	VDD_071 R22
AC18	VDD_016	VDD_072 R23
AC19	VDD_017	VDD_073 R24
AC20	VDD_018	VDD_074 R25
AC21	VDD_019	VDD_075 T12
AC22	VDD_020	VDD_076 T14
AC23	VDD_021	VDD_077 T16
AC24	VDD_022	VDD_078 T18
AC25	VDD_023	VDD_079 T20
AD12	VDD_024	VDD_080 T22
AD14	VDD_025	VDD_081 T24
AD16	VDD_026	VDD_082 V11
AD18	VDD_027	VDD_083 V13
AD22	VDD_028	VDD_084 V15
AD24	VDD_029	VDD_085 V17
L11	VDD_030	VDD_086 V19
L12	VDD_031	VDD_087 V21
L13	VDD_032	VDD_088 V23
L14	VDD_033	VDD_089 V25
L15	VDD_034	VDD_090 W11
L16	VDD_035	VDD_091 W12
L17	VDD_036	VDD_092 W13
L18	VDD_037	VDD_093 W14
L19	VDD_038	VDD_094 W15
L20	VDD_039	VDD_095 W16
L21	VDD_040	VDD_096 W17
L22	VDD_041	VDD_097 W18
L23	VDD_042	VDD_098 W19
L24	VDD_043	VDD_099 W20
L25	VDD_044	VDD_100 W21
M12	VDD_045	VDD_101 W22
M14	VDD_046	VDD_102 W23
M16	VDD_047	VDD_103 W24
M18	VDD_048	VDD_104 W25
M20	VDD_049	VDD_105 Y12
M22	VDD_050	VDD_106 Y14
M24	VDD_051	VDD_107 Y16
P11	VDD_052	VDD_108 Y18
P13	VDD_053	VDD_109 Y20
P15	VDD_054	VDD_110 Y22
P17	VDD_055	VDD_111 Y24
P19	VDD_056	

N10P-GS
null

NV_VDD

C5152 0.01U_16V_K 0402_X7R
C5153 0.01U_16V_K 0402_X7R
C5154 0.01U_16V_K 0402_X7R
C5155 0.01U_16V_K 0402_X7R
C5156 0.01U_16V_K 0402_X7R
C5157 0.01U_16V_K 0402_X7R

C5158 0.022U_16V_K 0402_X7R
C5159 0.022U_16V_K 0402_X7R
C5160 0.022U_16V_K 0402_X7R
C5161 0.022U_16V_K 0402_X7R

C5166 0.047U_16V_K 0402_X7R
C5167 0.047U_16V_K 0402_X7R
C5169 0.047U_16V_K 0402_X7R

C5179 1U_10V_K 0603_X5R
C1581 4700P_25V_K 0402_X7R
C1582 4700P_25V_K 0402_X7R

C6040 0.22U_6.3V_K 0402_X5R
C6041 0.22U_6.3V_K 0402_X5R

Place Underr Balls

C5176 10U_6.3V_M 0603_X5R
C5177 10U_6.3V_M 0603_X5R
C5175 4.7U_6.3V_K 0603_X5R
C5259 22P_50V_J 0402_NPO

Place Near GPU

For RF Noise

Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

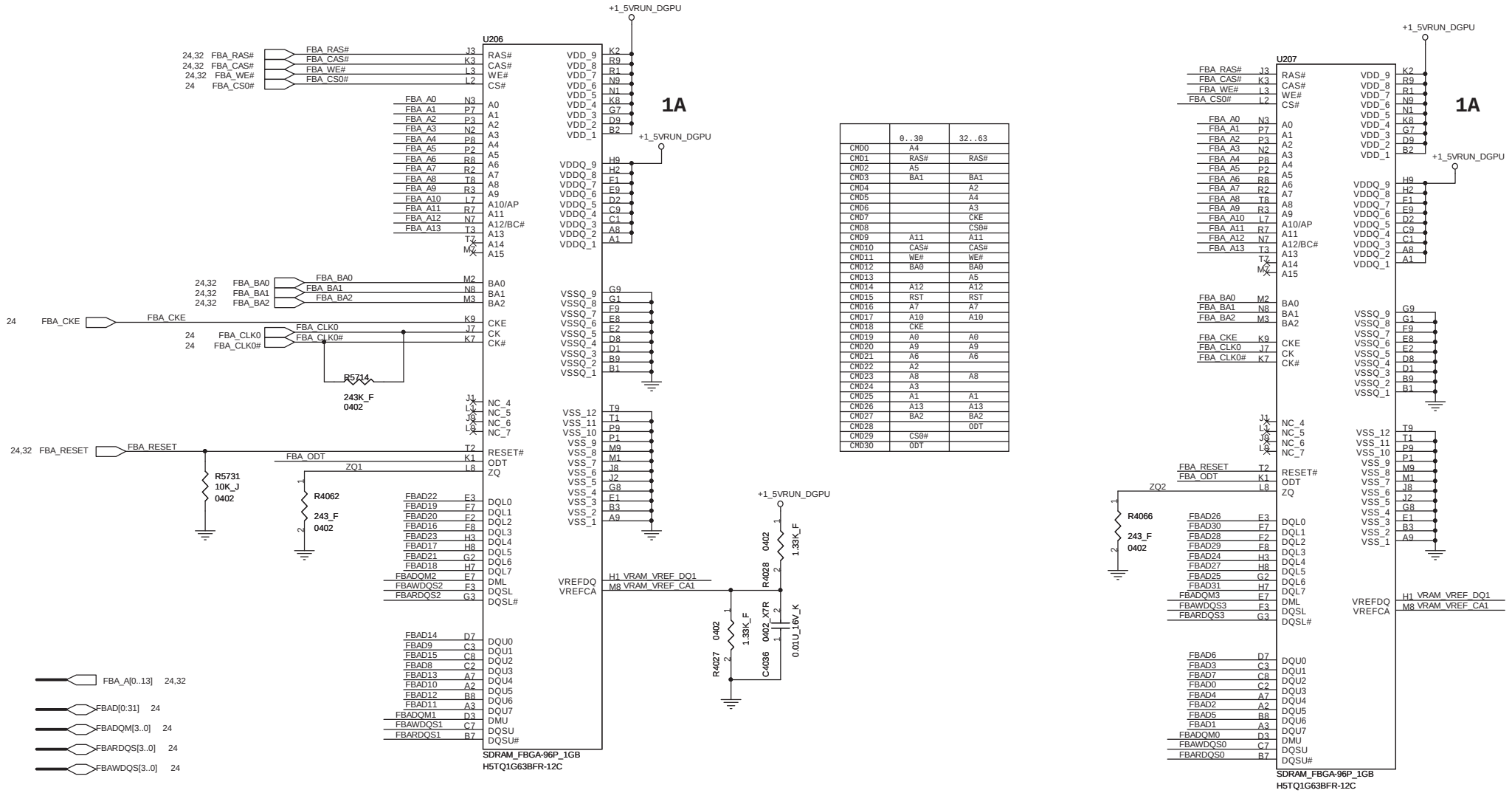
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

U204P
15/16 GND

AA11	GND_22	GND_18 E15
AA12	GND_125	GND_19 E18
AA13	GND_136	GND_20 E24
AA14	GND_147	GND_21 E27
AA15	GND_158	GND_24 E30
AA16	GND_169	GND_25 E6
AA17	GND_180	GND_26 E9
AA18	GND_191	GND_27 F2
AA19	GND_193	GND_28 F31
AA2	GND_23	GND_29 F34
AA20	GND_34	GND_30 F5
AA21	GND_45	GND_31 J2
AA22	GND_56	GND_32 J31
AA23	GND_67	GND_33 J34
AA24	GND_78	GND_35 J5
AA25	GND_89	GND_36 L9
AA34	GND_100	GND_37 M11
AA5	GND_111	GND_38 M13
AB12	GND_122	GND_39 M15
AB14	GND_126	GND_40 M17
AB16	GND_127	GND_41 M19
AB18	GND_128	GND_42 M2
AB20	GND_129	GND_43 M21
AB22	GND_130	GND_44 M23
AB24	GND_131	GND_46 M25
AC9	GND_132	GND_47 M31
AD11	GND_133	GND_48 M34
AD13	GND_134	GND_49 M5
AD15	GND_135	GND_50 N11
AD17	GND_137	GND_51 N12
AD2	GND_138	GND_52 N13
AD21	GND_139	GND_53 N14
AD23	GND_140	GND_54 N15
AD25	GND_141	GND_55 N16
AD31	GND_142	GND_57 N17
AD34	GND_143	GND_58 N18
AD5	GND_144	GND_59 N19
AE11	GND_145	GND_60 N20
AE12	GND_146	GND_61 N21
AE13	GND_148	GND_62 N22
AE14	GND_149	GND_63 N23
AE15	GND_150	GND_64 N24
AE16	GND_151	GND_65 N25
AE17	GND_152	GND_66 P12
AE18	GND_153	GND_68 P14
AE19	GND_154	GND_69 P16
AE20	GND_155	GND_70 P18
AE21	GND_156	GND_71 P20
AE22	GND_157	GND_72 P22
AE23	GND_159	GND_73 P24
AE24	GND_160	GND_74 R2
AE25	GND_161	GND_75 R31
AG2	GND_162	GND_76 R34
AG31	GND_163	GND_77 R5
AG34	GND_164	GND_79 T11
AG5	GND_165	GND_80 T13
AK2	GND_166	GND_81 T15
AK31	GND_167	GND_82 T17
AK34	GND_168	GND_83 T19
AK5	GND_170	GND_84 T21
AL12	GND_171	GND_85 T23
AL15	GND_172	GND_86 T25
AL18	GND_173	GND_87 U11
AL21	GND_174	GND_88 U12
AL24	GND_175	GND_90 U13
AL27	GND_176	GND_91 U14
AL30	GND_177	GND_92 U15
AL6	GND_178	GND_93 U16
AL9	GND_179	GND_94 U17
AN2	GND_181	GND_95 U18
AN34	GND_182	GND_96 U19
AP12	GND_183	GND_97 U20
AP15	GND_184	GND_98 U21
AP18	GND_185	GND_99 U22
AP21	GND_186	GND_101 U23
AP24	GND_187	GND_102 U24
AP27	GND_188	GND_103 U25
AP3	GND_189	GND_104 V12
AP30	GND_190	GND_105 V14
AP33	GND_192	GND_106 V16
AP6	GND_3	GND_107 V18
AP9	GND_4	GND_108 V2
B12	GND_5	GND_109 V20
B15	GND_6	GND_110 V22
B21	GND_7	GND_112 V24
B24	GND_8	GND_113 V31
B27	GND_9	GND_114 V5
B3	GND_10	GND_115 V9
B30	GND_11	GND_116 Y11
B33	GND_12	GND_117 Y13
B6	GND_13	GND_118 Y15
B9	GND_14	GND_119 Y17
C2	GND_15	GND_120 Y19
C34	GND_16	GND_121 Y21
E12	GND_17	GND_123 Y23
		GND_124 Y25

N10P-GS
null

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA(POWER/GROUND) 9/9	
Size Custom	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 30 of 86	



	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VRAM(DDR)# 1/4
Size A3	Document Number W930 H1&H2
Rev	SA
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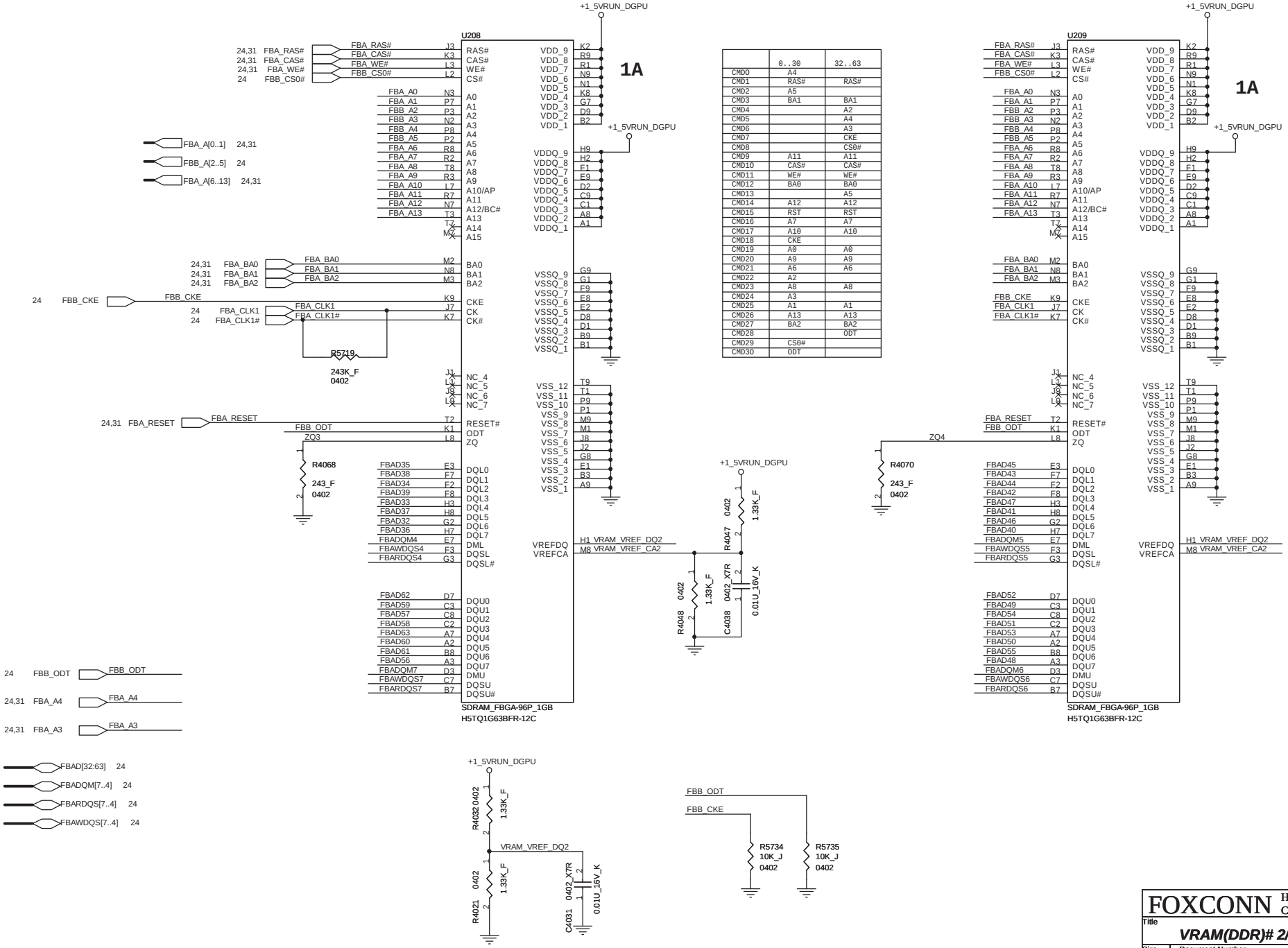

	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM(DDR)# 2/4	
Size A3	Document Number W930 H1&H2	Rev SA
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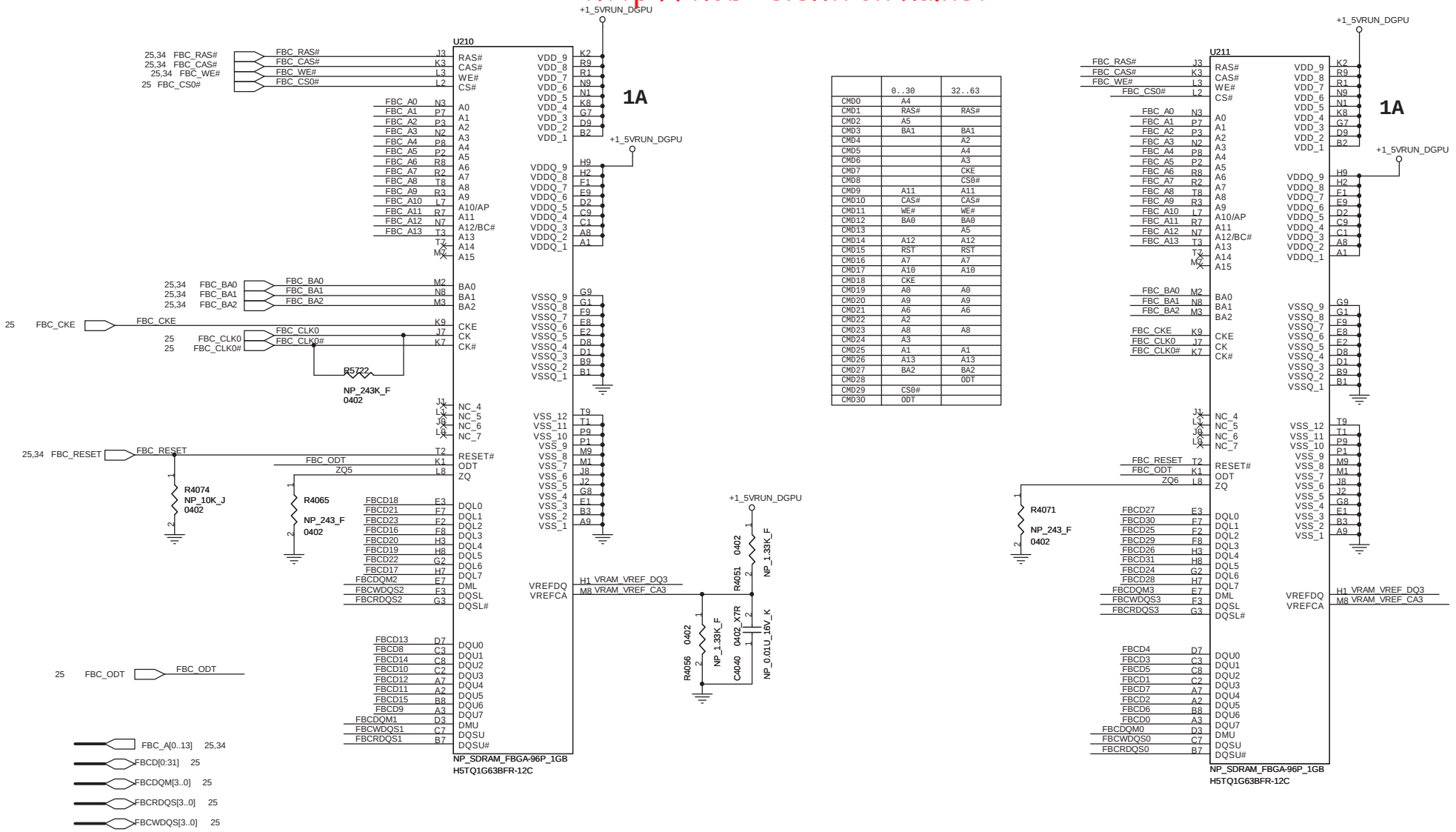
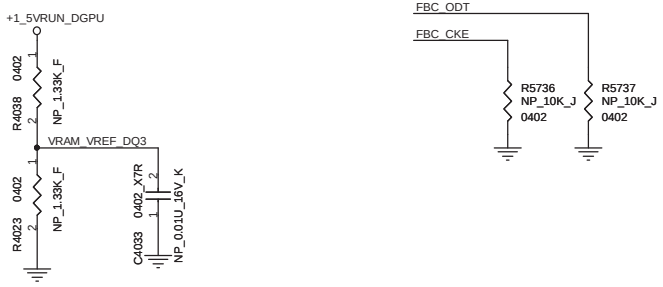
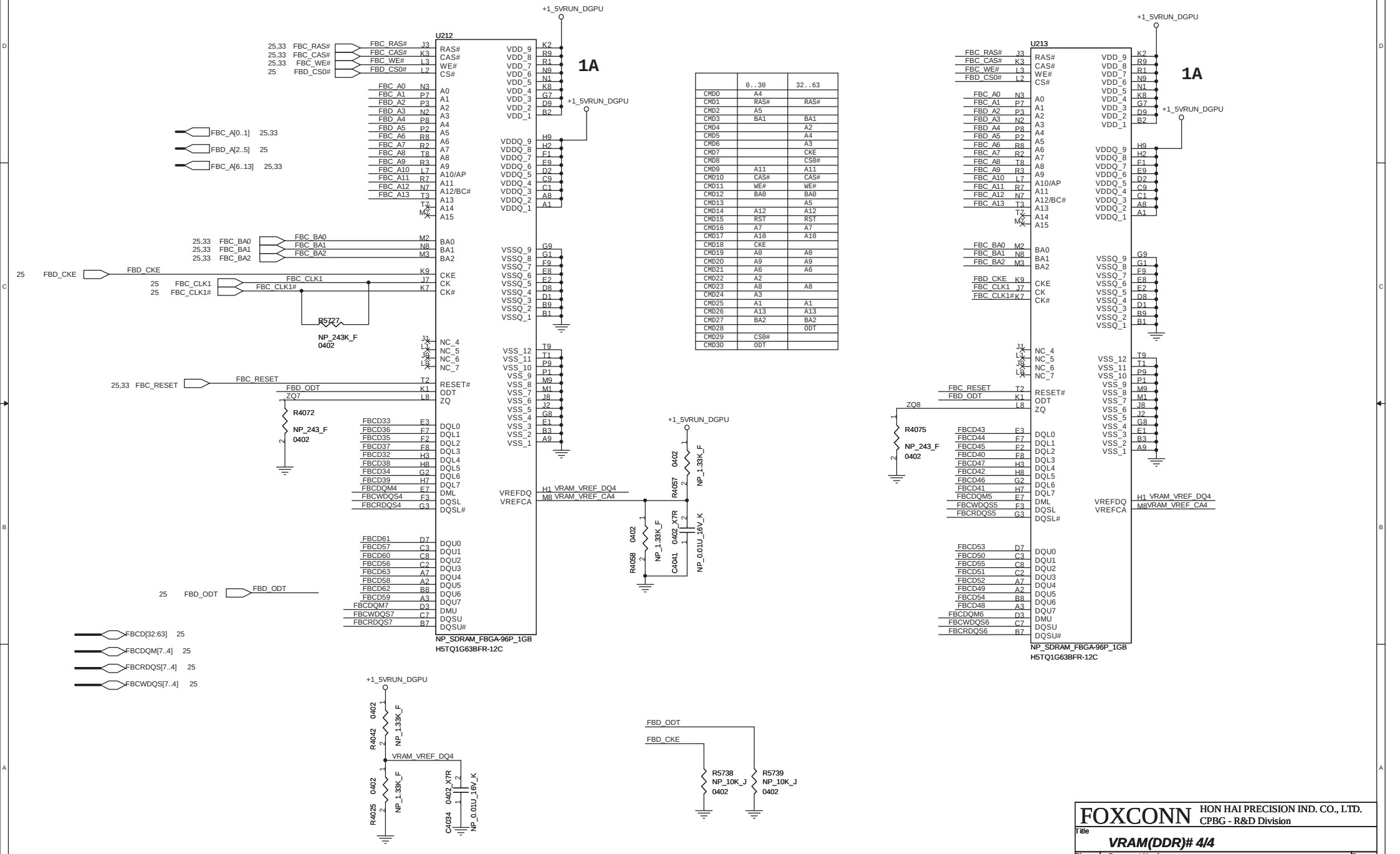


	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	



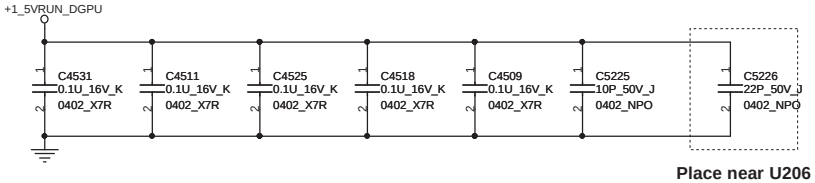
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM(DDR)# 3/4	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 33 of 86	



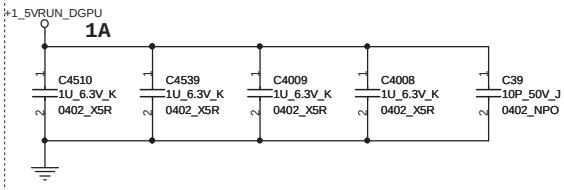
	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM(DDR)# 4/4	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 34 of 86	

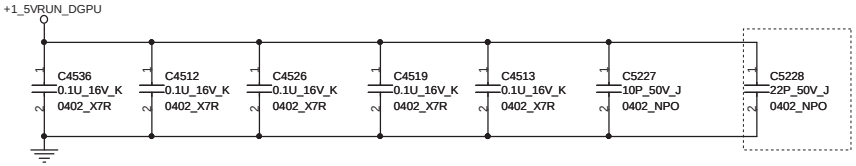
Place around the VRAM U206



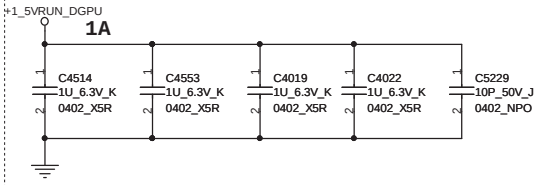
Place near U206



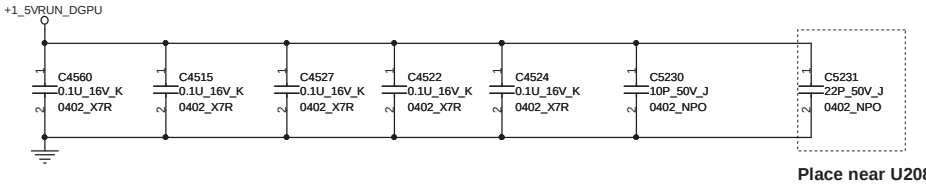
Place around the VRAM U207



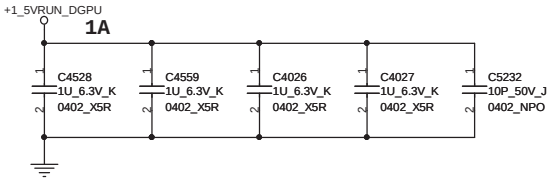
Place near U207



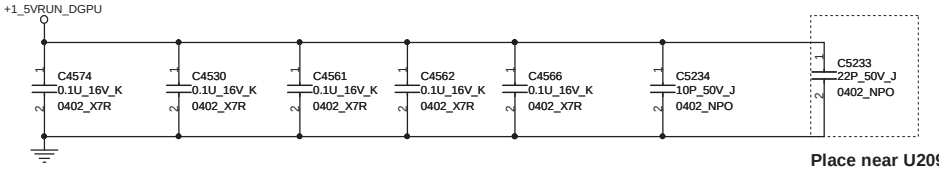
Place around the VRAM U208



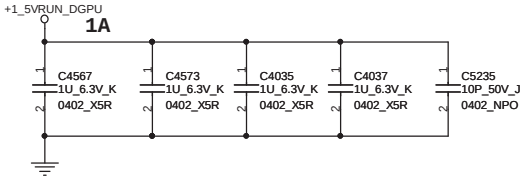
Place near U208



Place around the VRAM U209



Place near U209



PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*VRAM(BYPASS) 1/2*	
Size A3	Document Number *W930 H1&H2*	Rev *SA*
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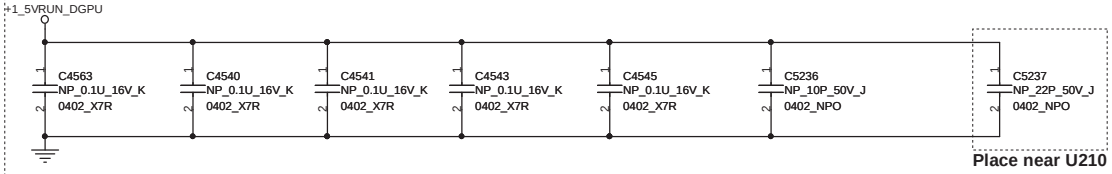
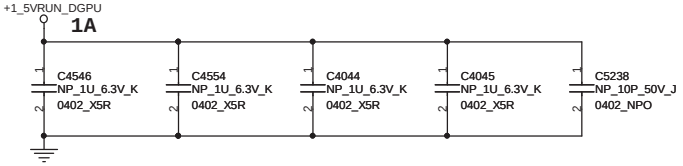
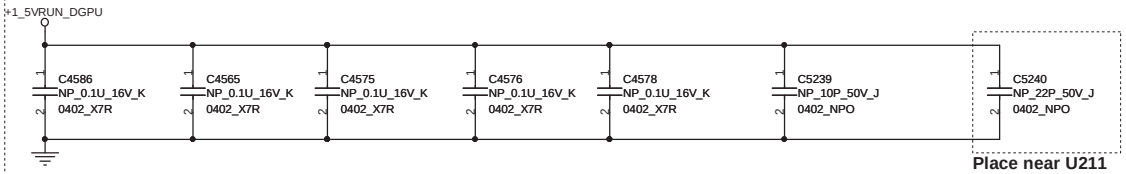
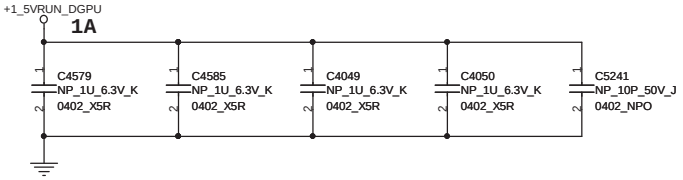
Place around the VRAM U210



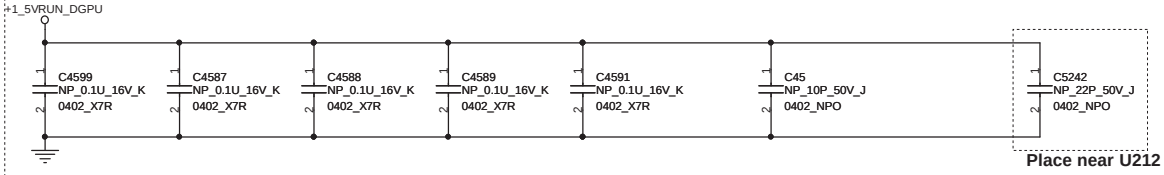


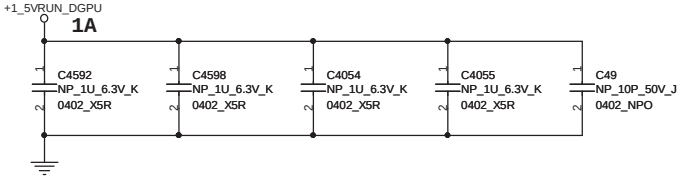
Place around the VRAM U211



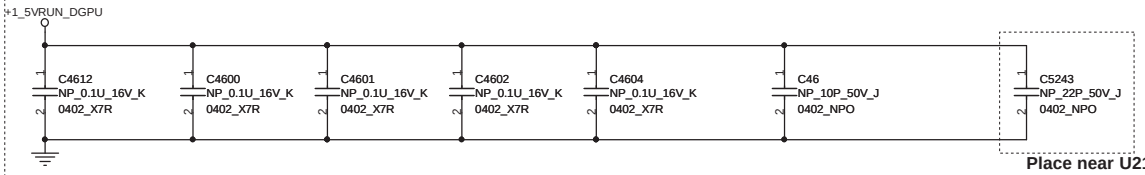


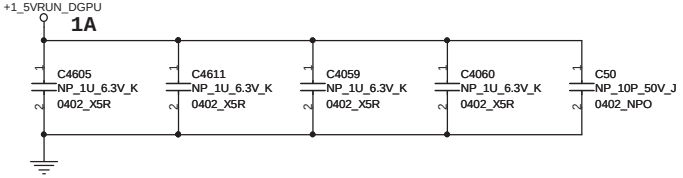
Place around the VRAM U212





Place around the VRAM U213

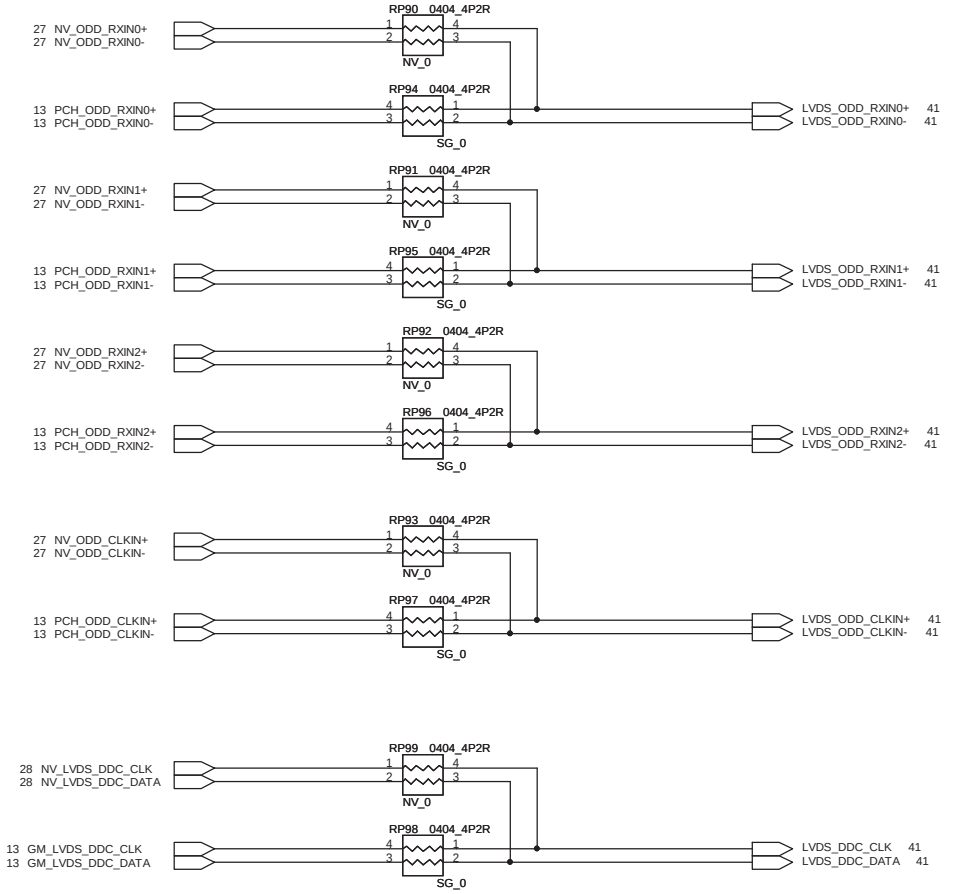


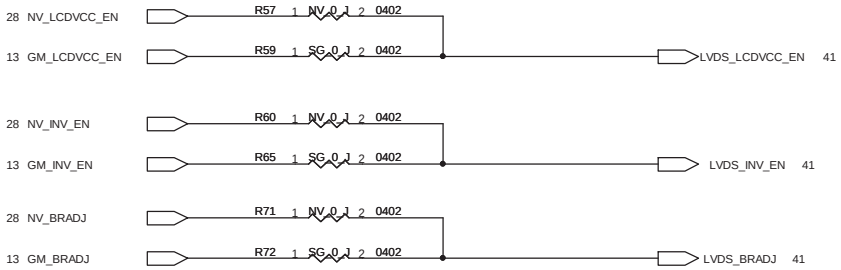


PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

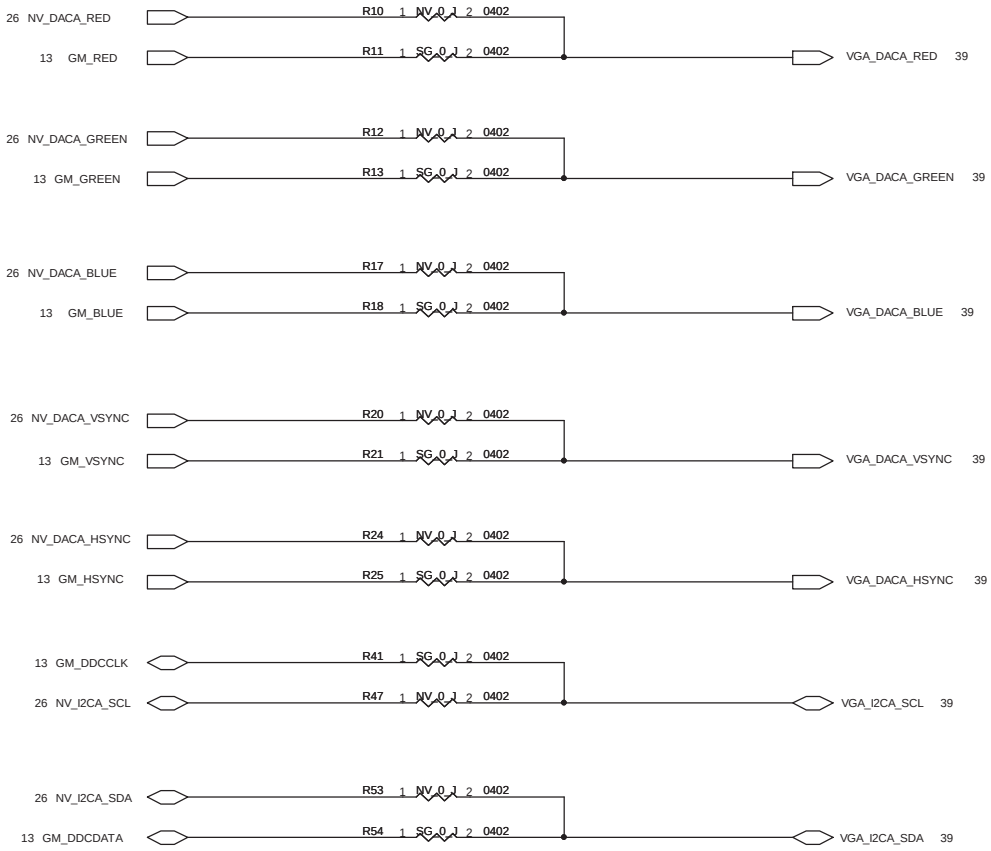
PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*VRAM(BYPASS) 2/2*	
Size A3	Document Number *W930 H1&H2*	Rev *SA*
Date: Thursday, May 20, 2010	Sheet 36 of 86	

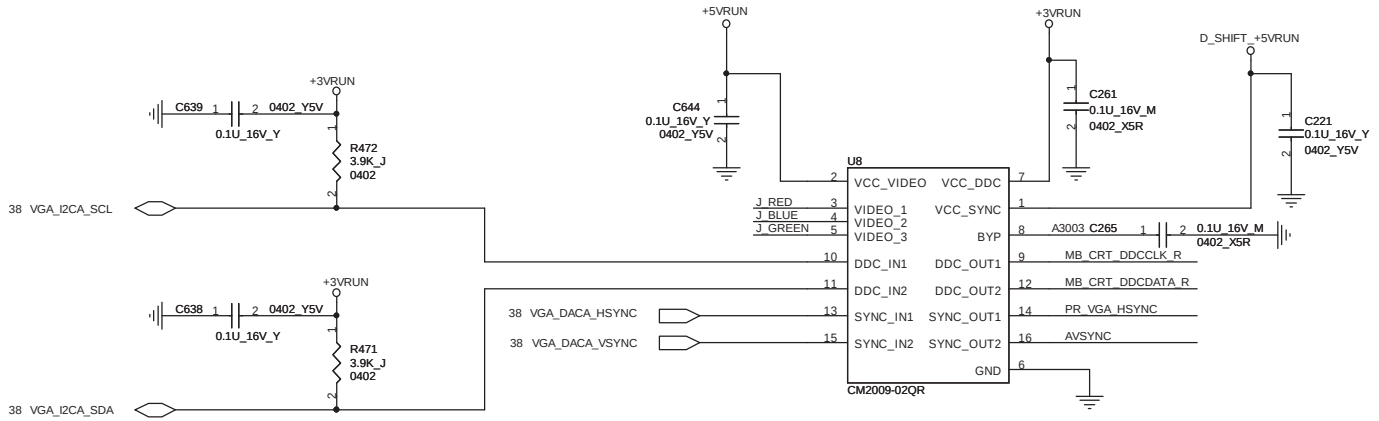




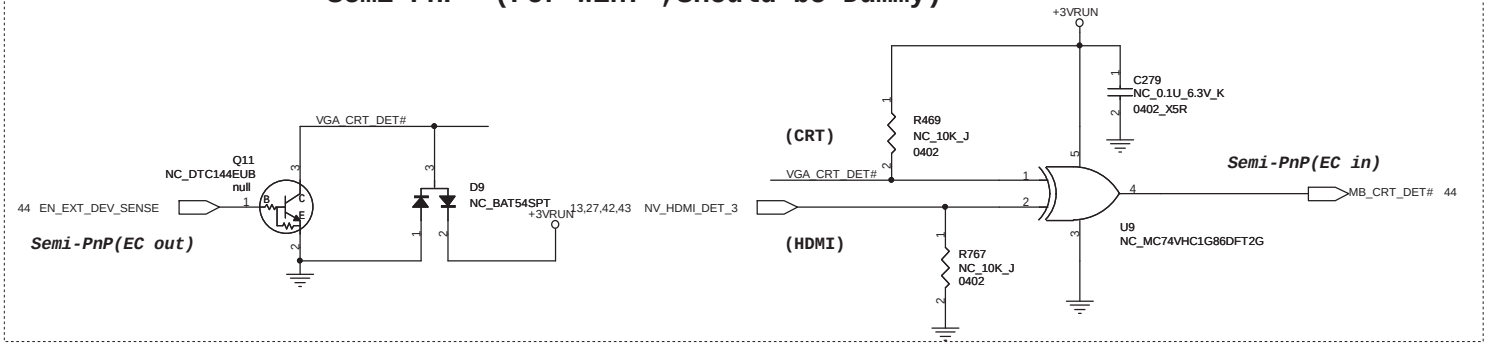
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	MUX LVDS	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 37 of 86	

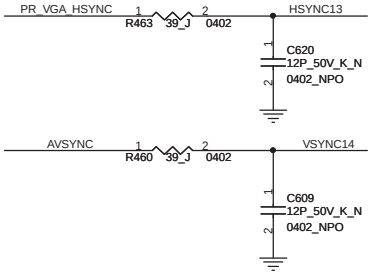


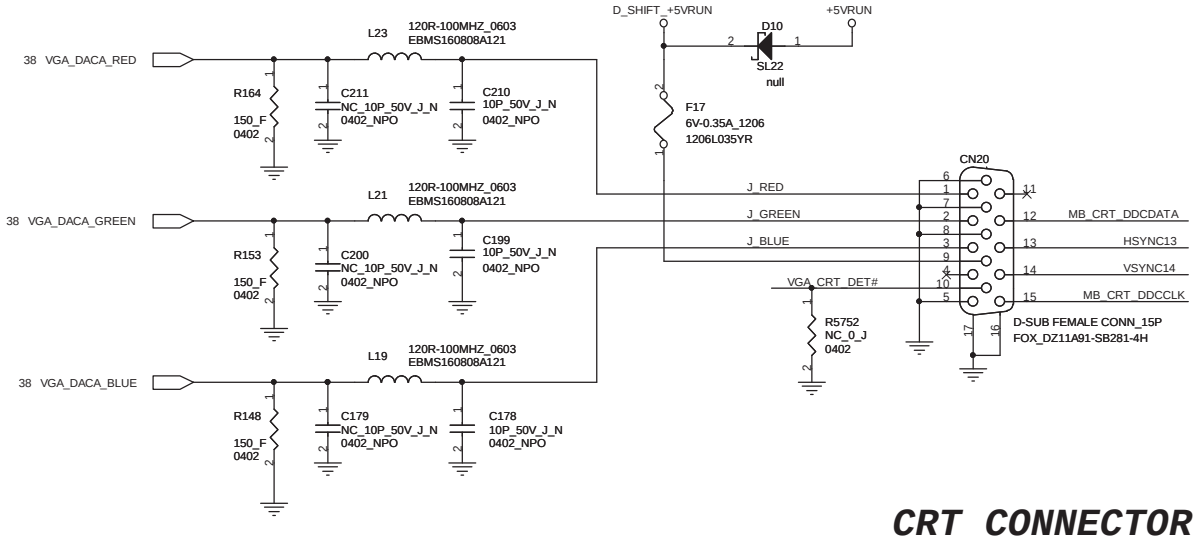
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	MUX CRT	
Size: A3	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 38 of 86	

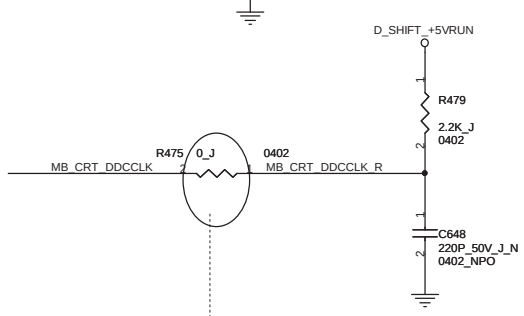


Semi-PnP (For Win7 ,Should be Dummy)

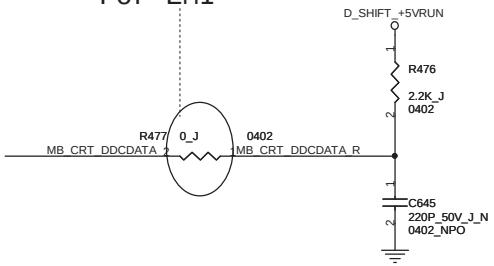


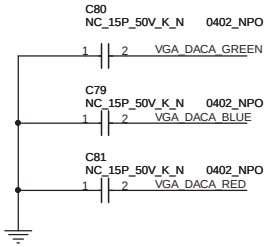






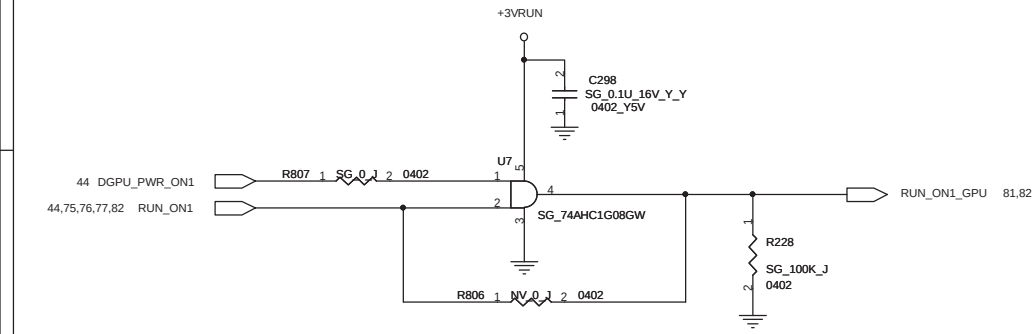
For EMI

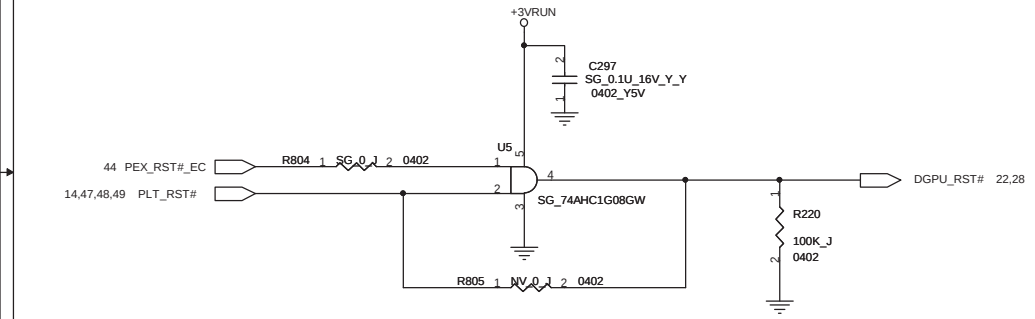


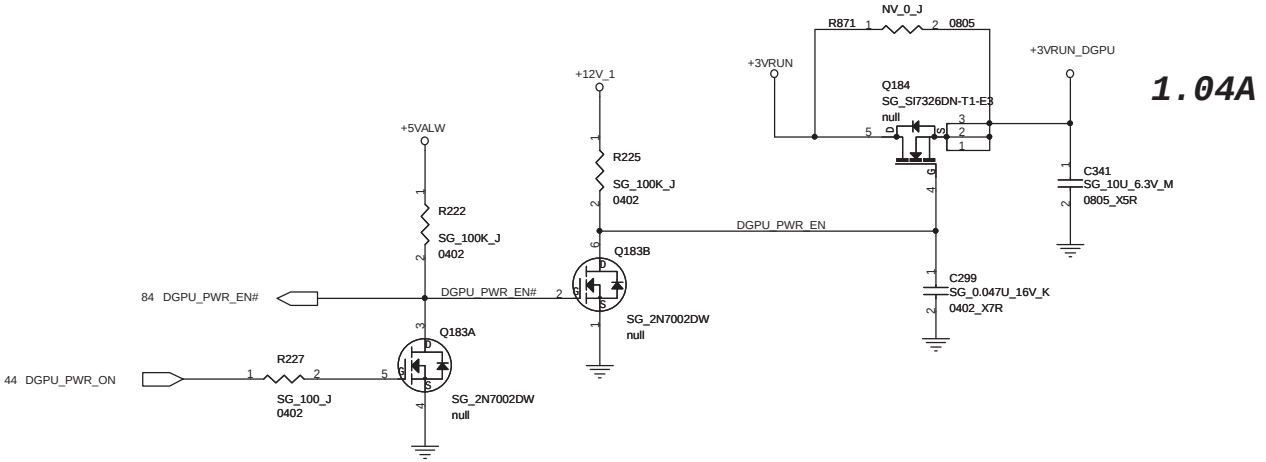


CRT CONNECTOR

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CRT	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 39 of 86	

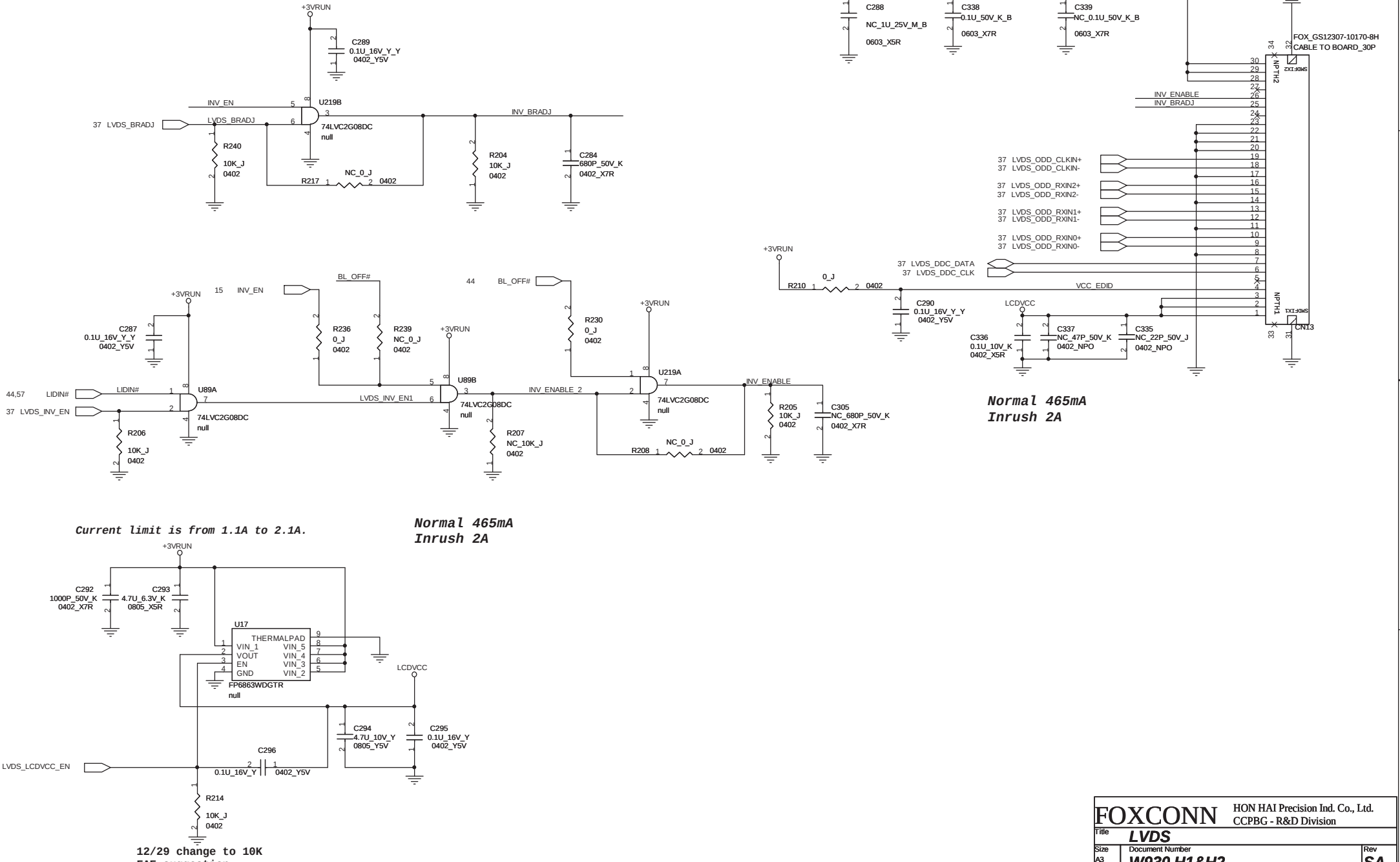




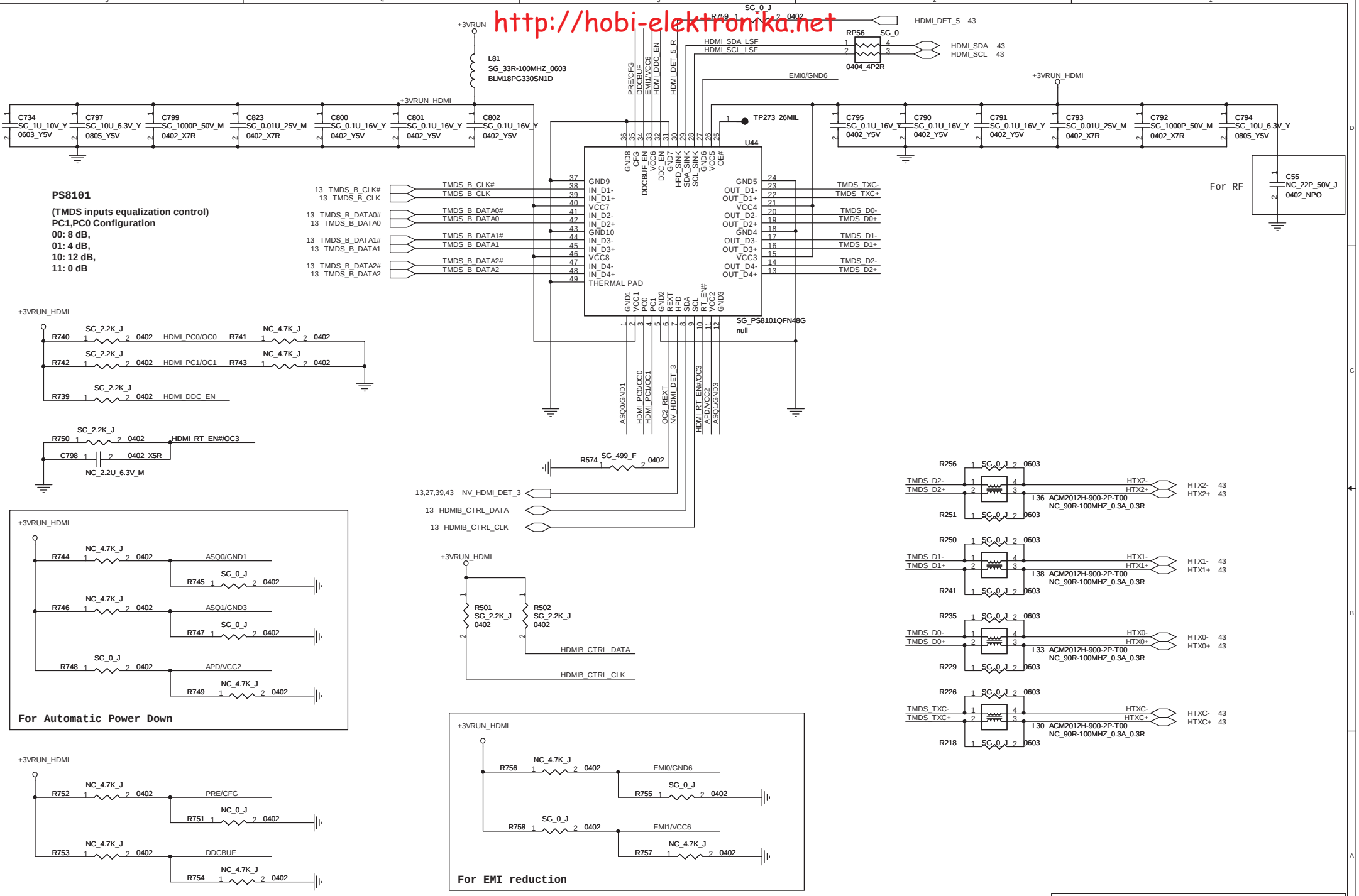


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Optimux	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 40 of 86	

LVDS CONNECTOR



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LVDS	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 41 of 86	



Company	FOXCONN — HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	HDMI Optimux
Size	A3
Document Number	W930 H1&H2
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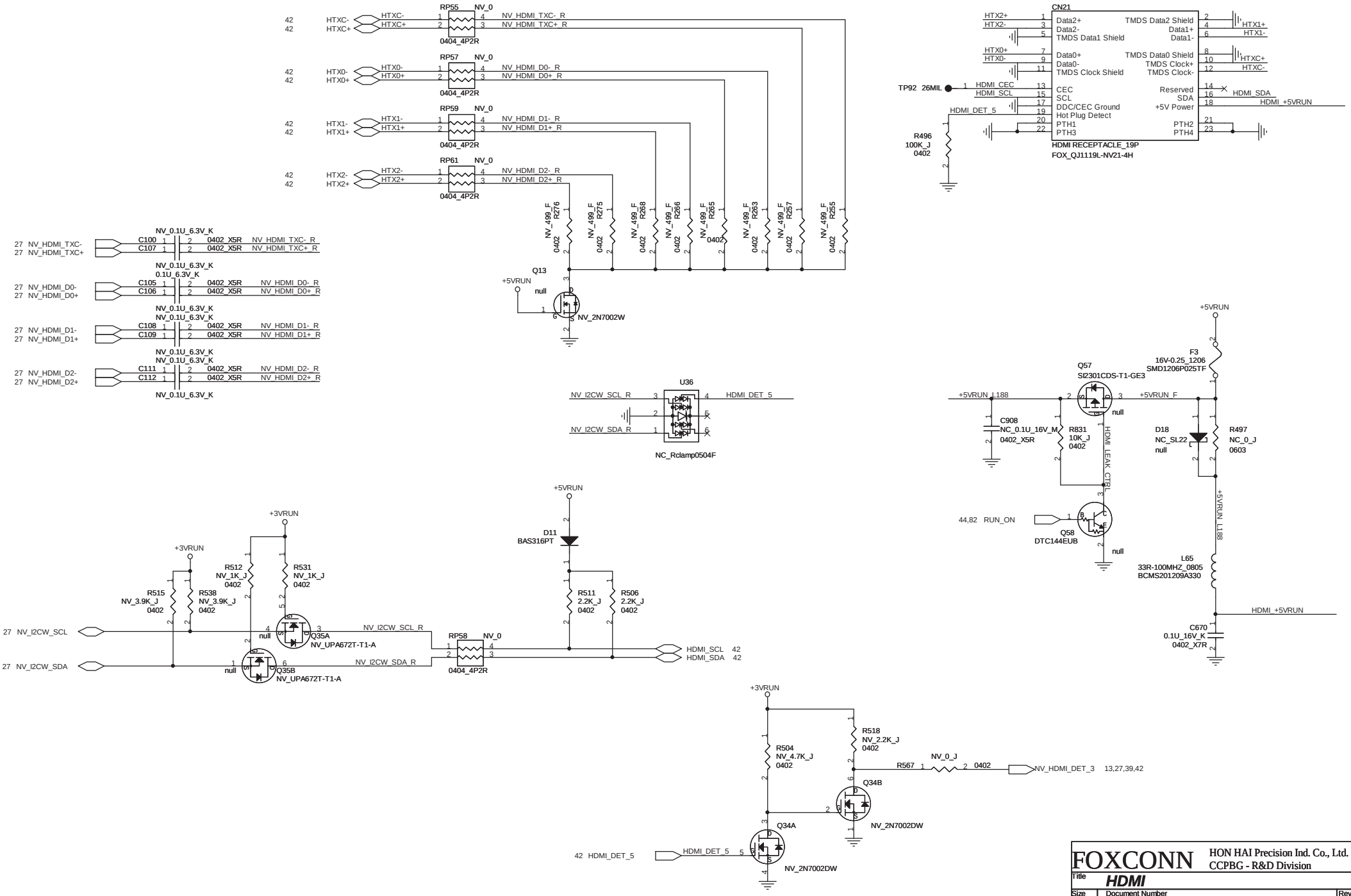
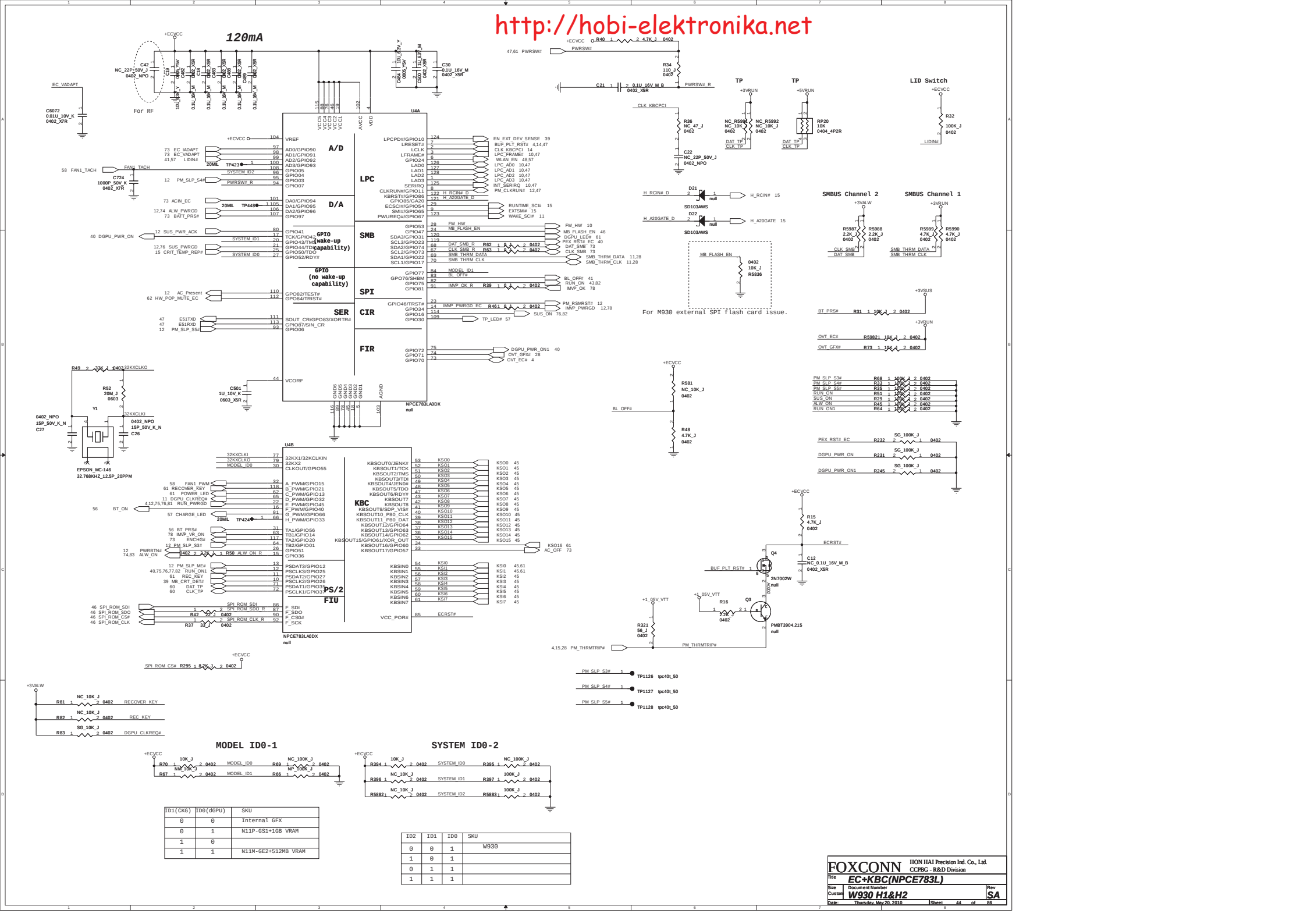
Data line capacitance to GND need less than 10pF,
so those parts need close to HDMI connector



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HDMI	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 43 of 86	



ID1(CKG)	ID0(dGPU)	SKU
0	0	Internal GFX
0	1	N11P-GS1+1GB VRAM
1	0	
1	1	N11M-GE2+512MB VRAM

ID2	ID1	ID0	SKU
0	0	1	W930
1	0	1	
0	1	1	
1	1	1	

FOXCONN — HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: EC+KBC(NPCE783L)

Size: Custom | Document Number: W930 H1&H2 | Rev: SA

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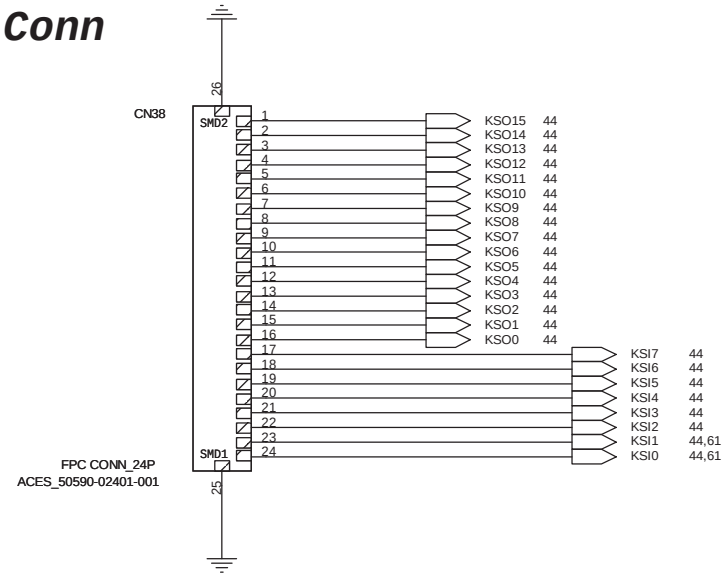
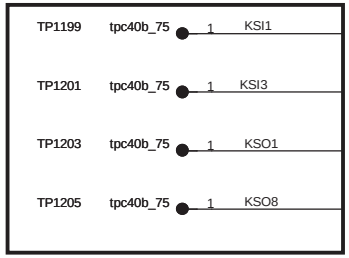
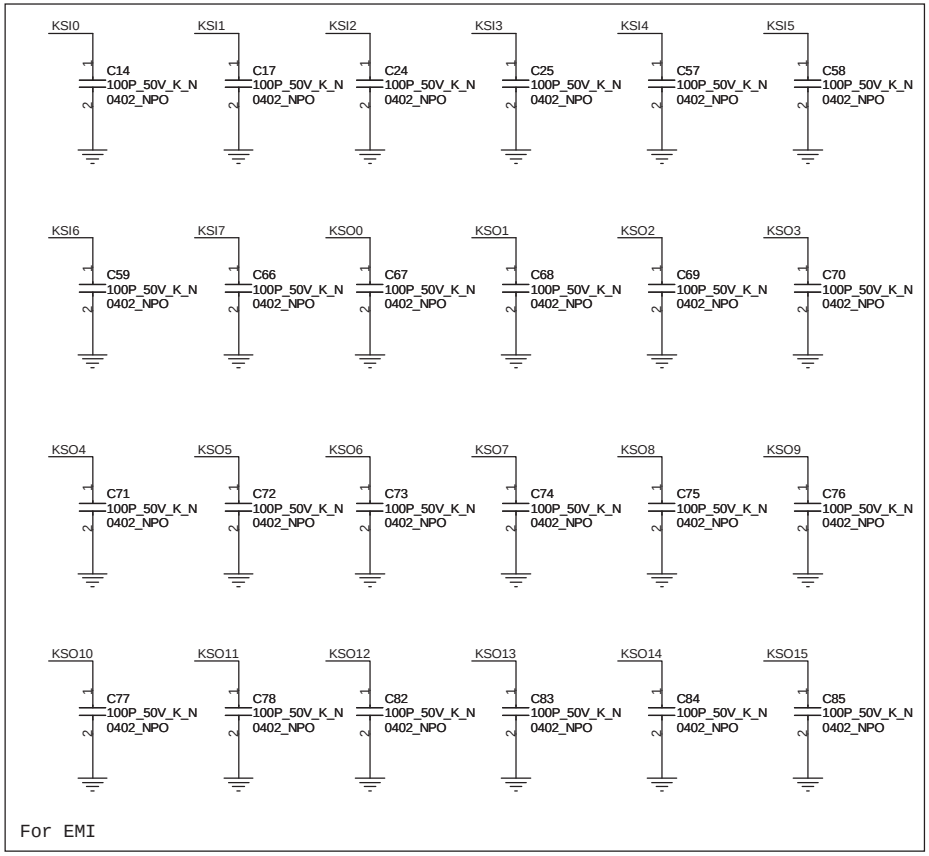
KBC Conn

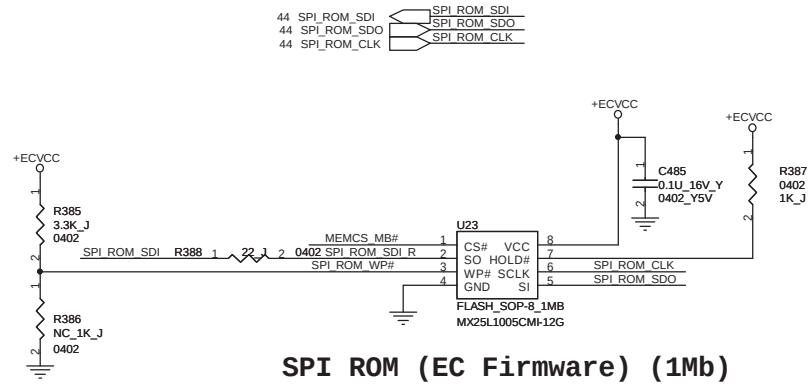


BFT Test Pad(Bottom)

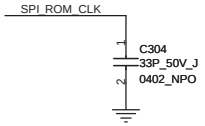


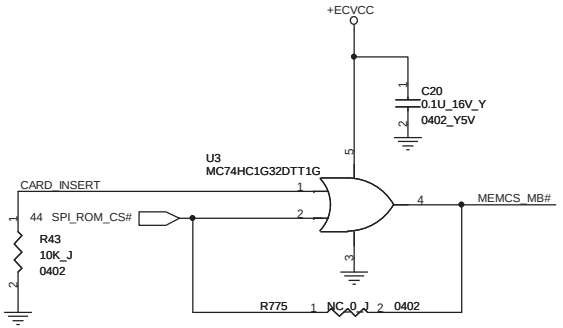


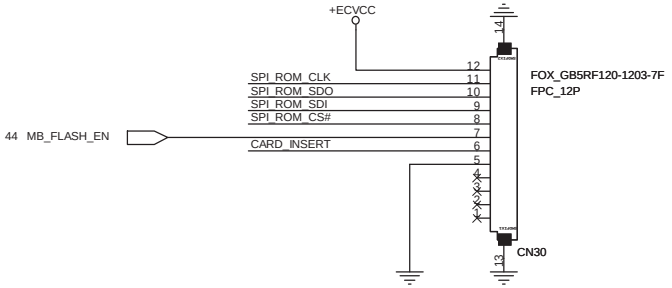
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: ***KB Connector***		
Size: B	Document Number: ***W930 H1&H2***	Rev: ***SA***
Date: Thursday, May 20, 2010	Sheet 45 of 86	



SPI ROM (EC Firmware) (1Mb)

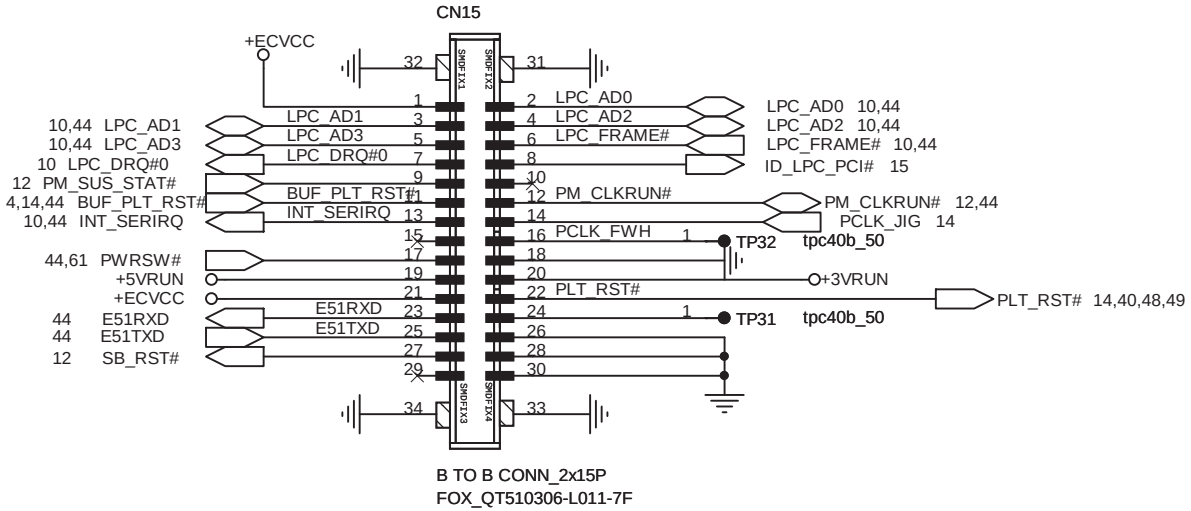






EXTERNAL SPI ROM INTERFACE (EC)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SPI Flash ROM	
Size: A3	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 46 of 86	



JIG-120

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: ***Debug Port***		
Size: A4	Document Number: ***W930 H1&H2***	Rev: ***SA***
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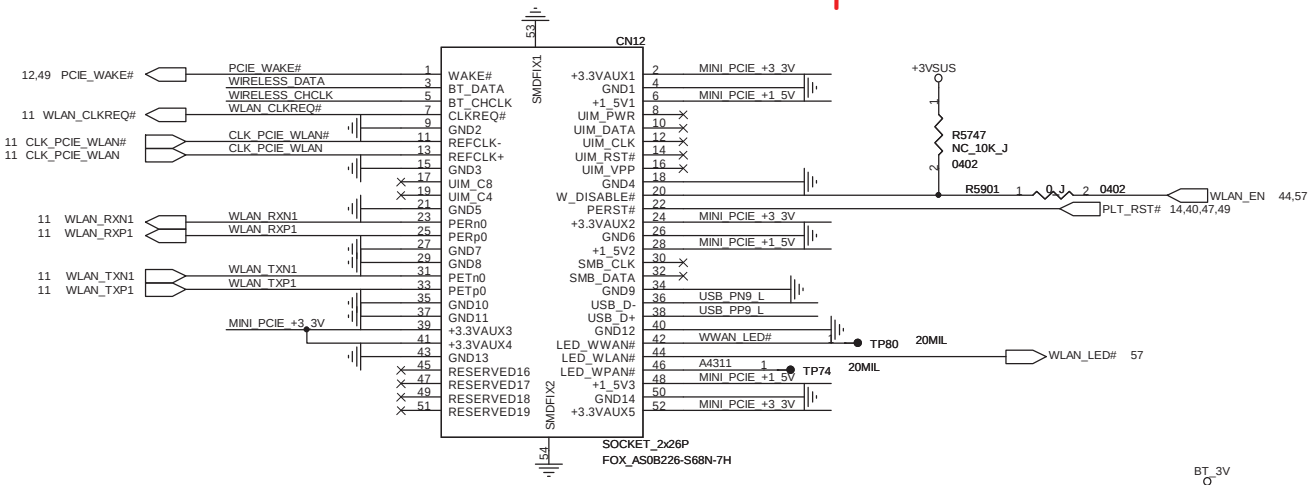
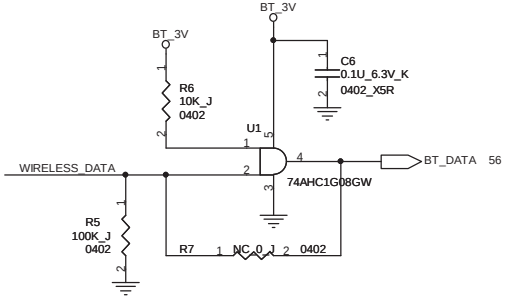
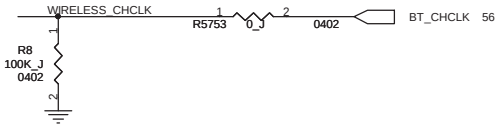
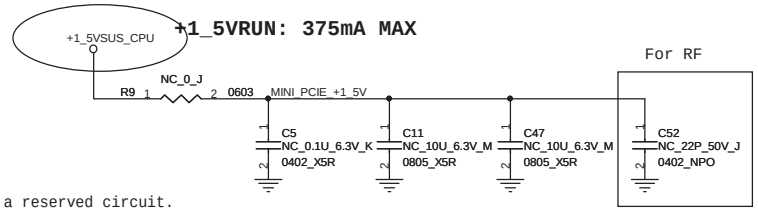
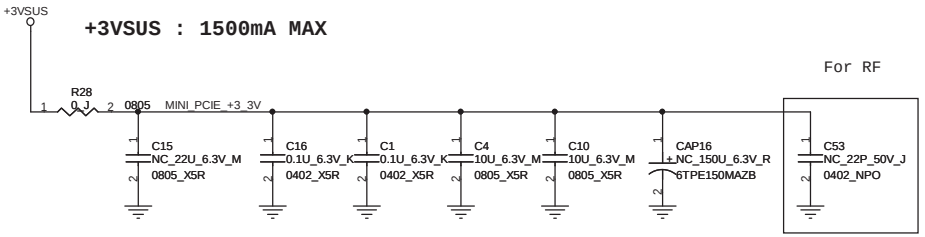


Half Size Mini Card

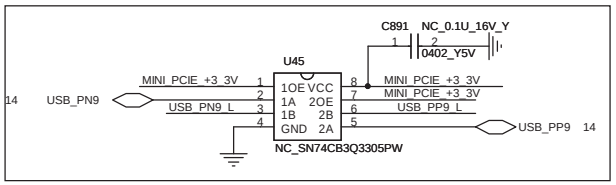




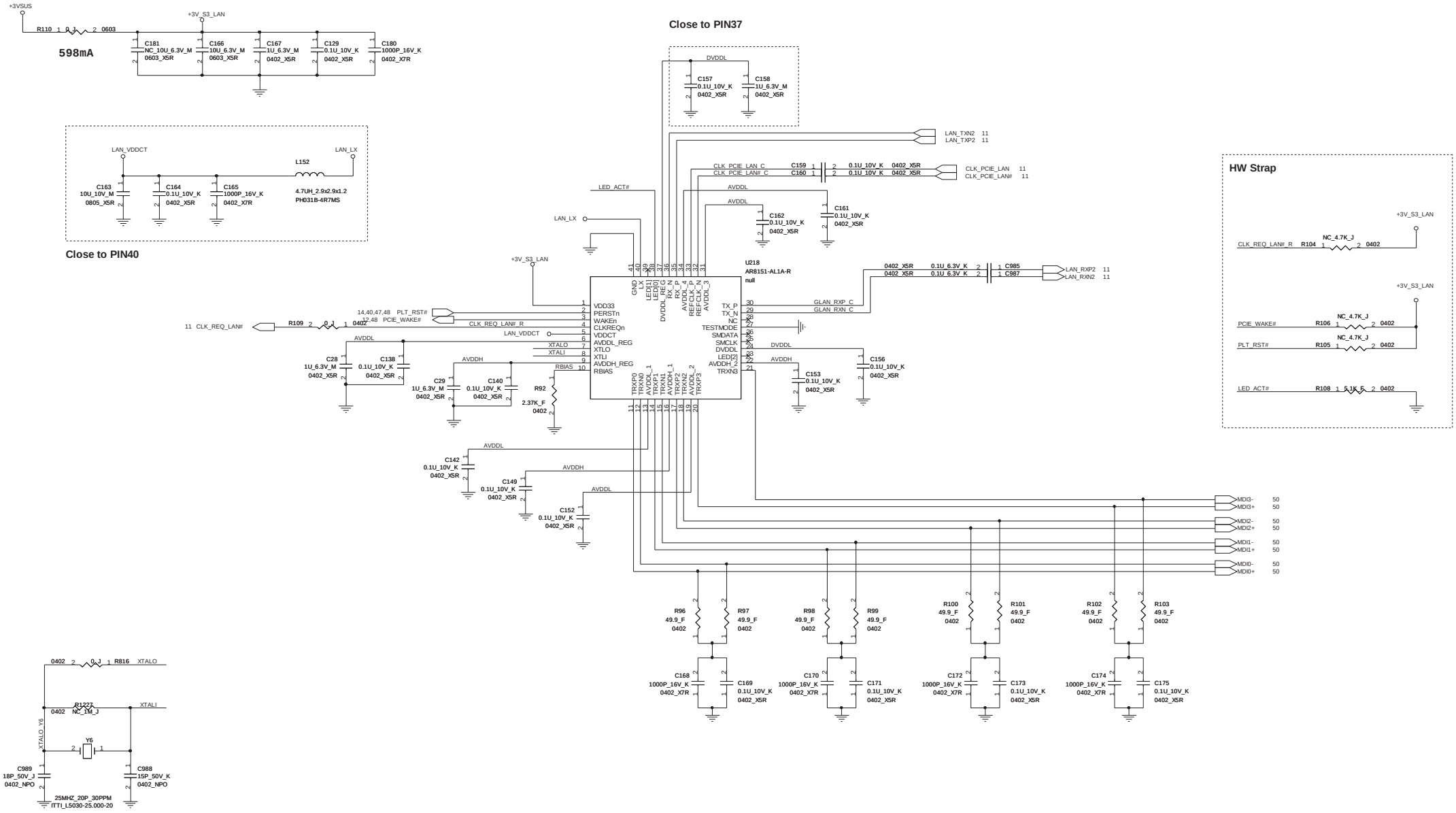




This is a reserved circuit.
According to RF comment,
this circuit could be deleted
if Layout space is not enough.

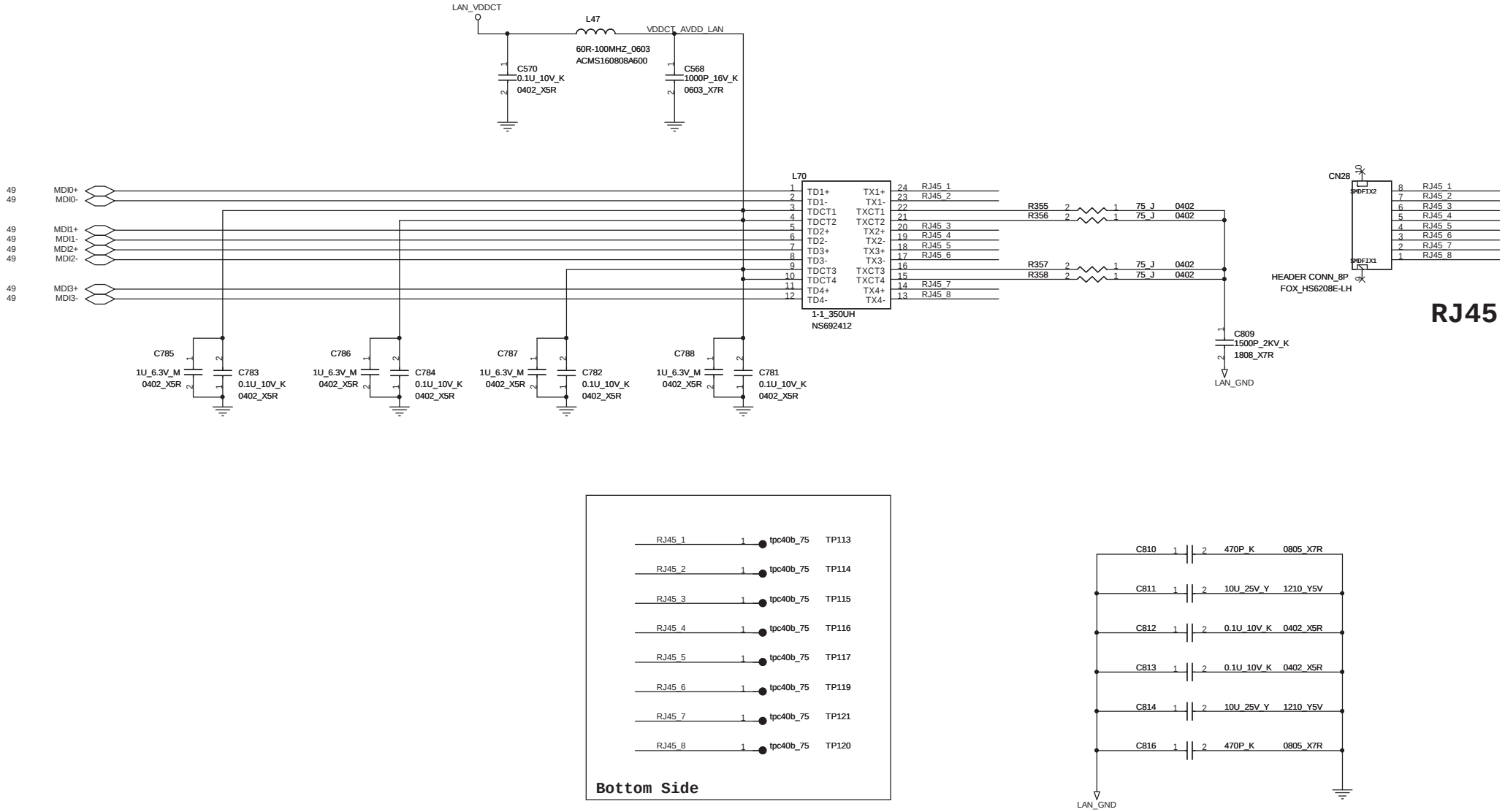


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Mini-PCIE Card (WLAN)	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 48 of 86	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	LAN (AR8151) 1/2		
Size: Custom	Document Number: W930 H1&H2		Rev: SA
Date: Thursday, May 20, 2010		Sheet 49 of 86	

For EMI



RJ45

Bottom Side

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LAN (Transfomer)(2/2)	
Size A3	Document Number W930 H1&H2	Rev SA
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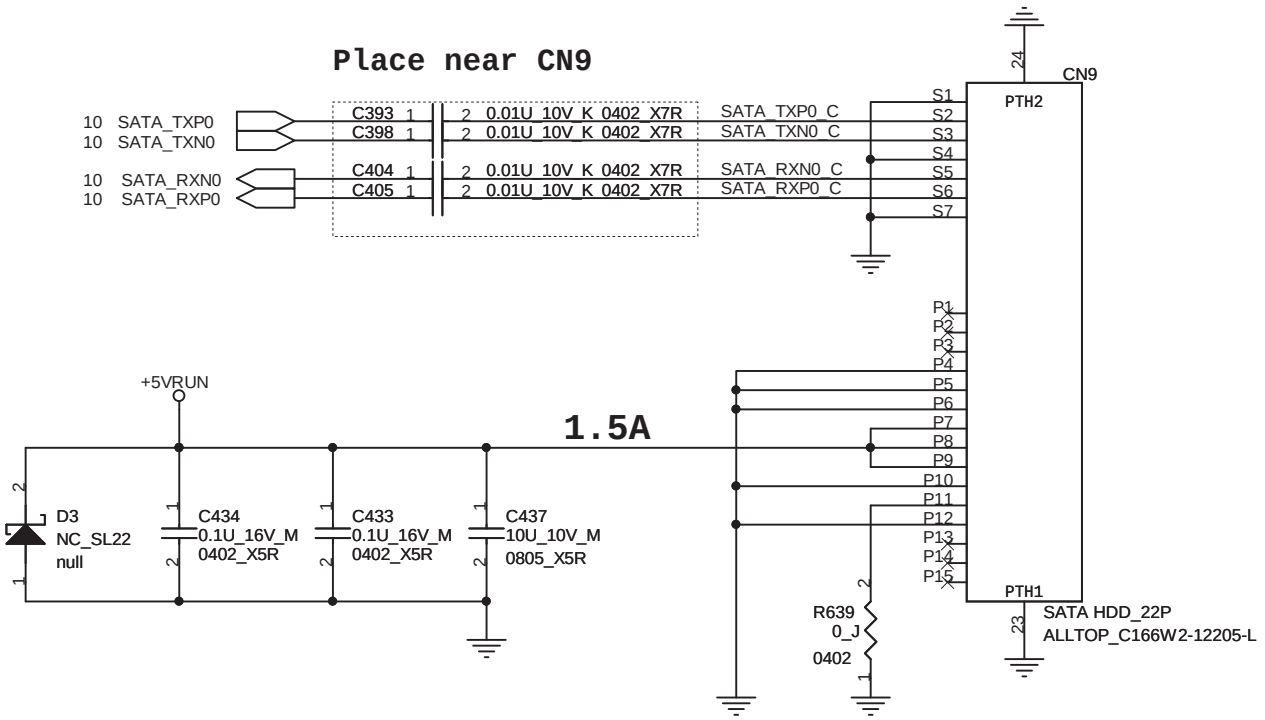

SATA HDD CONN

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: SATA HDD		
Size: A4	Document Number: W930 H1&H2	Rev: SA
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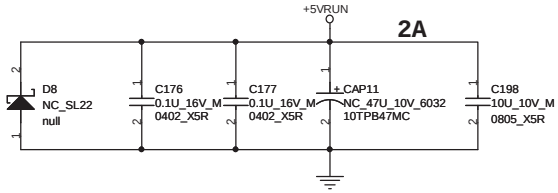
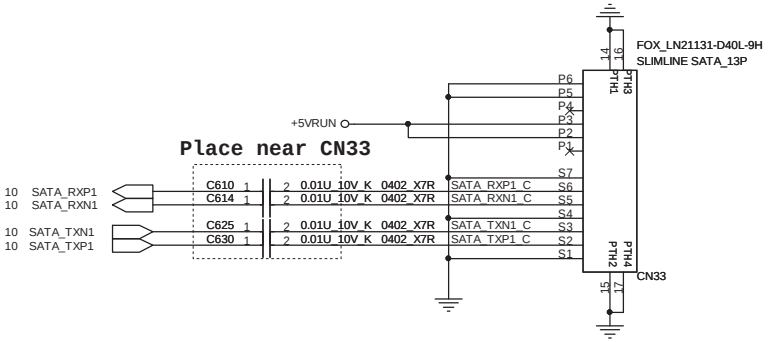
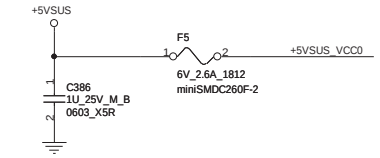
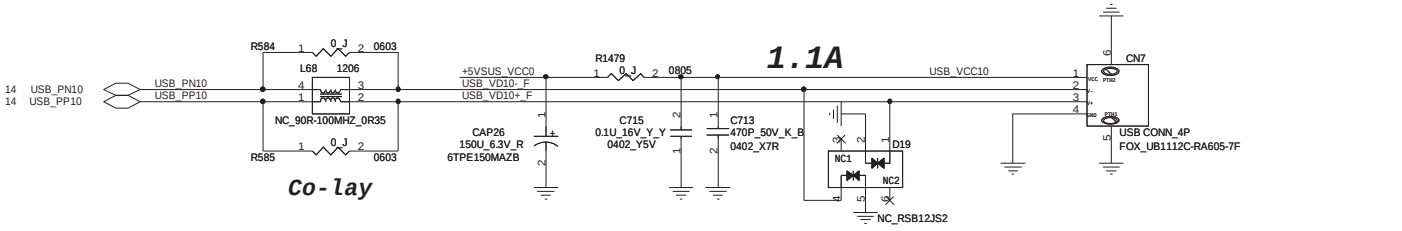


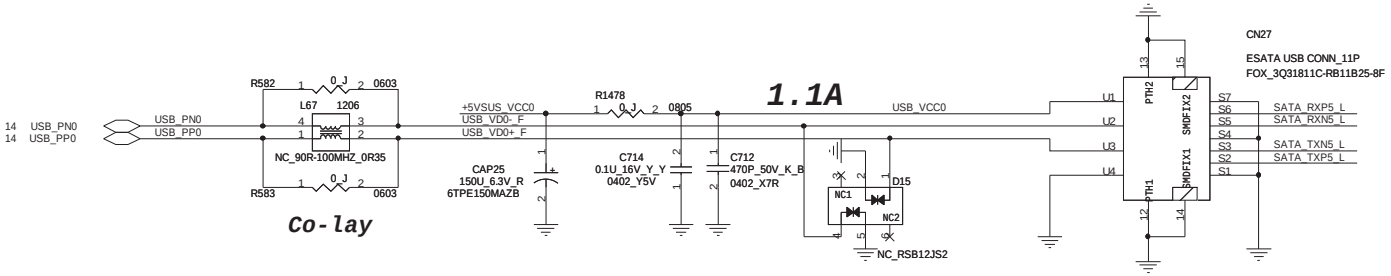


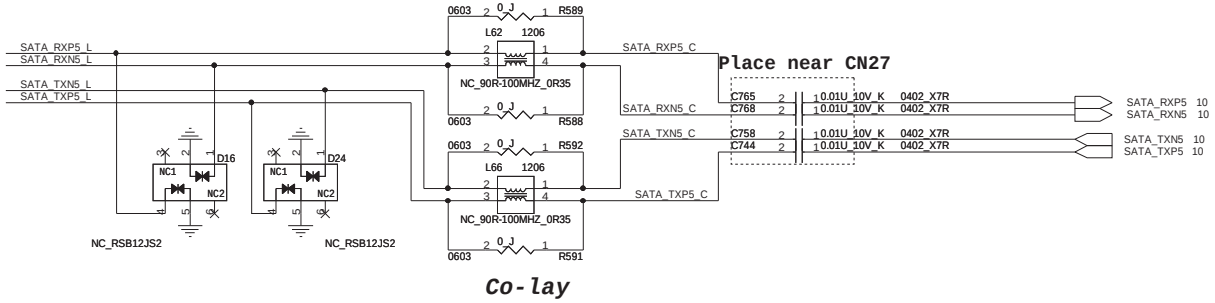
SATA ODD CONN

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SATA ODD	
Size: A3	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 52 of 86	



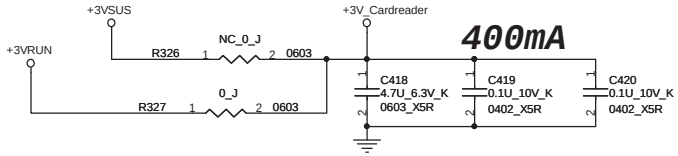


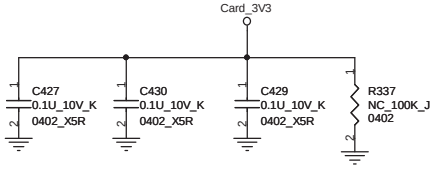


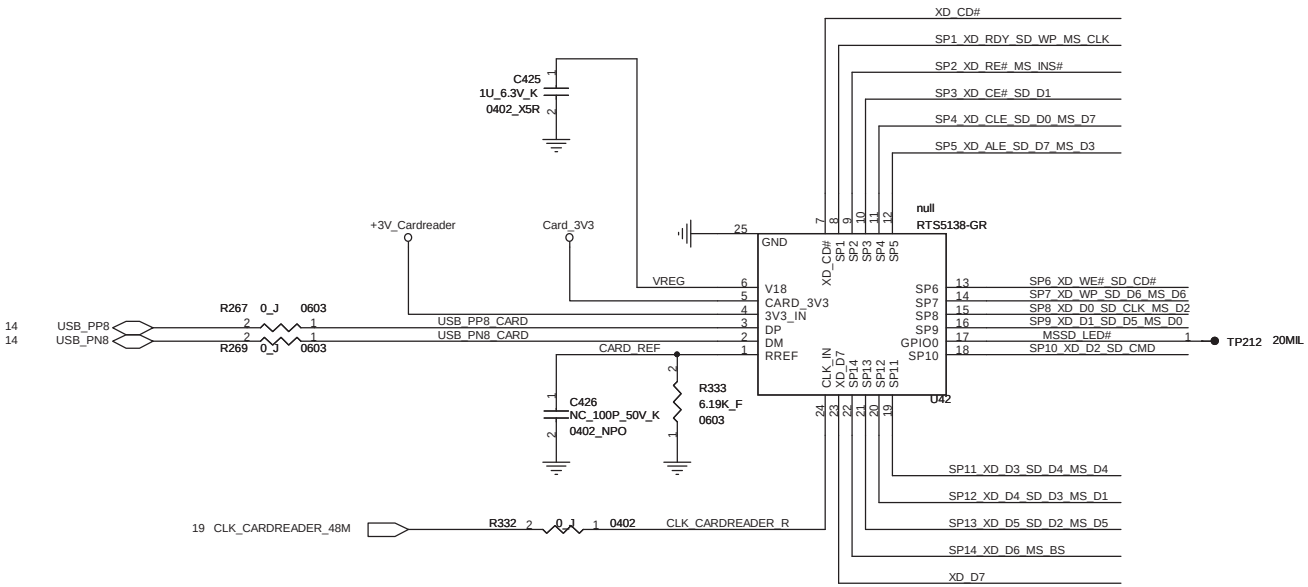


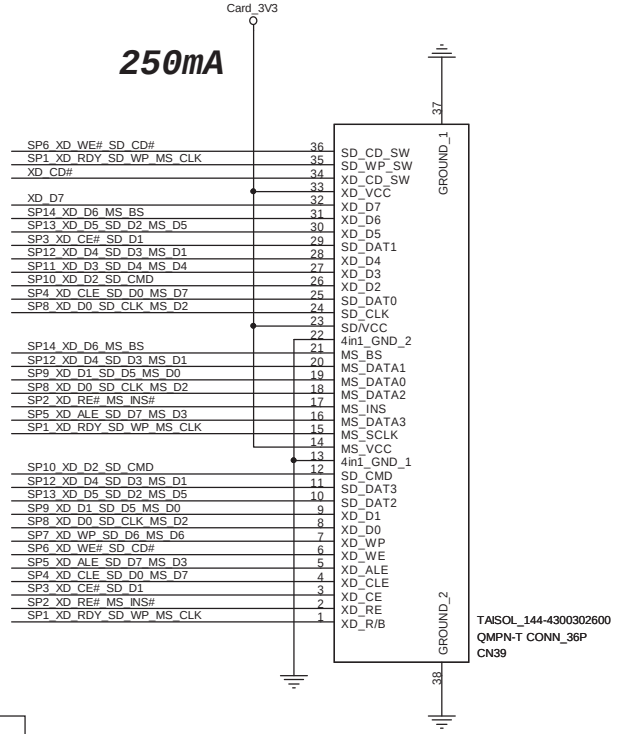
USB + eSATA on MB

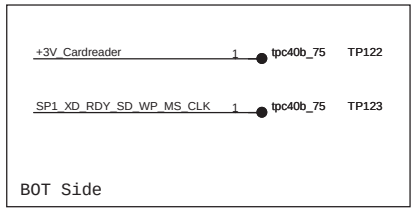
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	eSATA Combo		
Size: Custom	Document Number: W930 H1&H2		Rev: SA
Date: Thursday, May 20, 2010	Sheet 53 of 86		











FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Cardreader(USB)	
Size A3	Document Number W930 H1&H2	Rev SA
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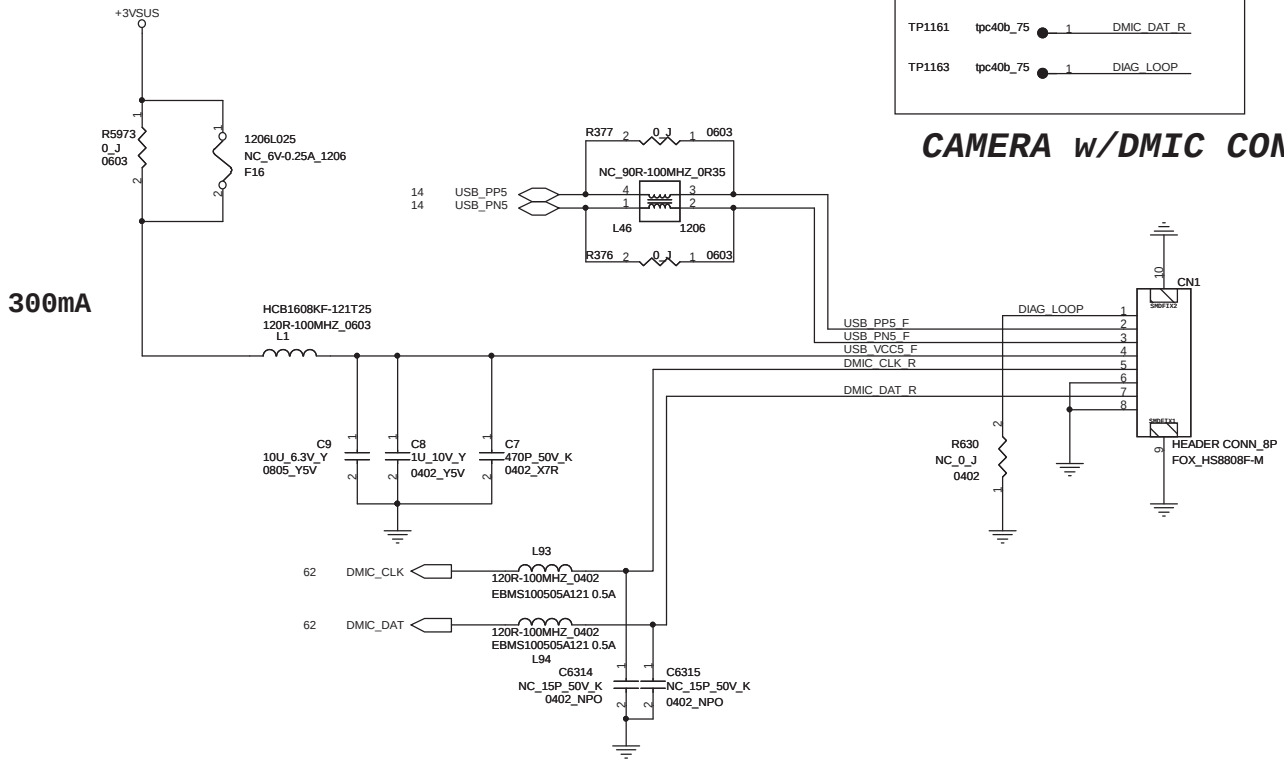
BFT Test Point(Bottom)

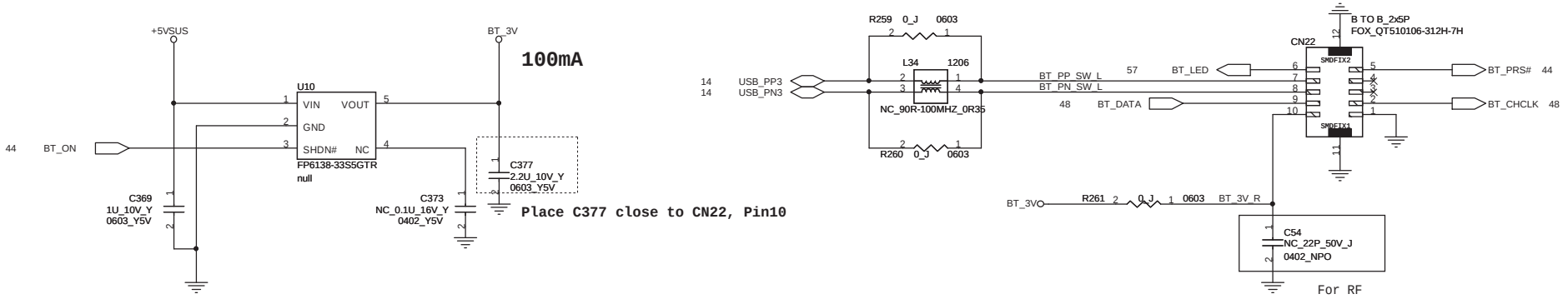
TP1156	tpc40b_75	1	USB_VCC5_F
TP1157	tpc40b_75	1	USB_PN5_F
TP1158	tpc40b_75	1	USB_PP5_F
TP1159	tpc40b_75	1	
TP1160	tpc40b_75	1	DMIC_CLK_R
TP1161	tpc40b_75	1	DMIC_DAT_R
TP1163	tpc40b_75	1	DIAG_LOOP

CAMERA w/DMIC CONN.



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Camera w/DMIC Connector	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 55 of 86	

Bluetooth CONN.



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Bluetooth Connector		
Size: Custom	Document Number: W930 H1&H2	Rev: SA
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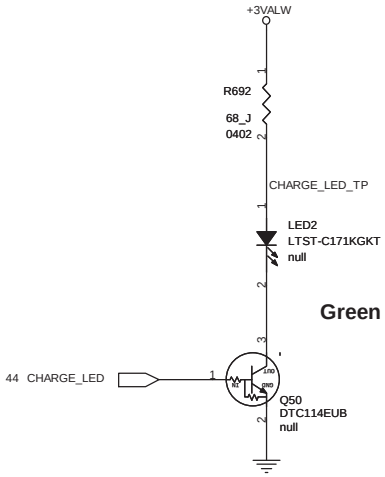
Power Test Test Point (Top)

TP1224 tpc60t_100 — 1 CHARGE_LED
TP1228 tpc60t_100 — 1 CHARGE_LED_TP

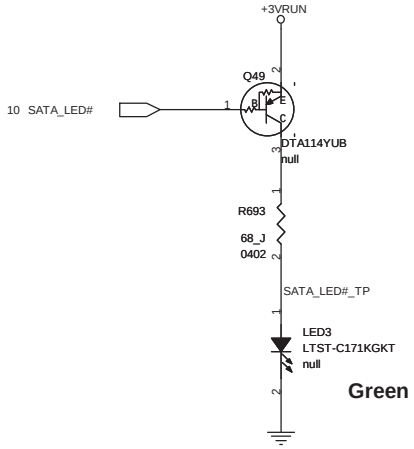
Power Test Test Point (Top)

TP1225 tpc60t_100 — 1 SATA_LED#
TP1229 tpc60t_100 — 1 SATA_LED#_TP

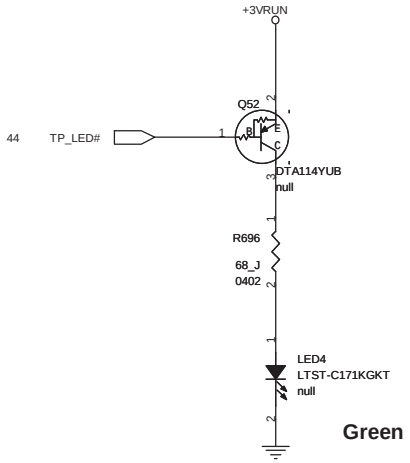
Charger LED



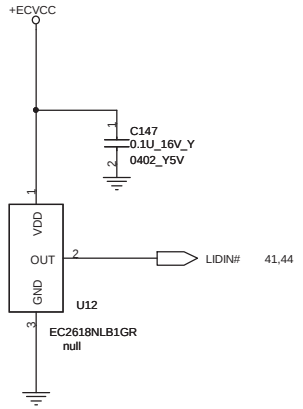
HDD LED



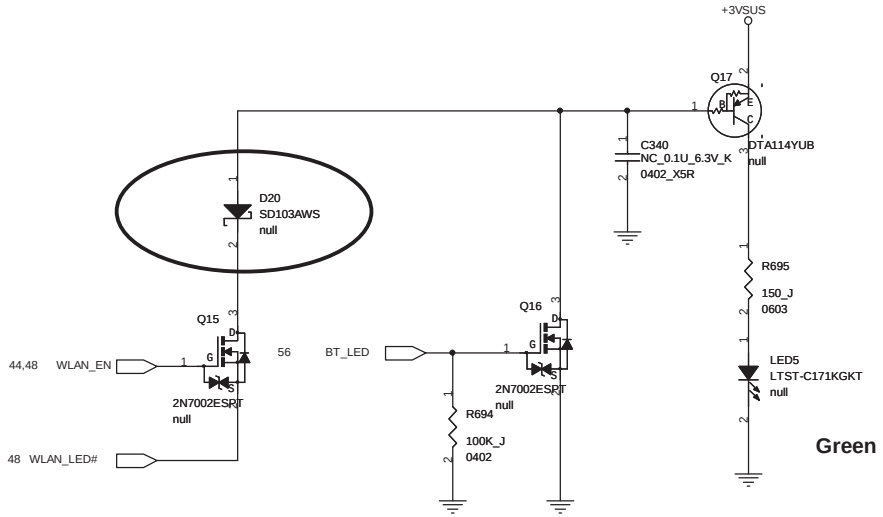
T/P LED



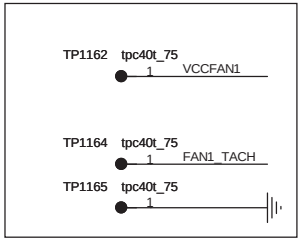
LID Switch



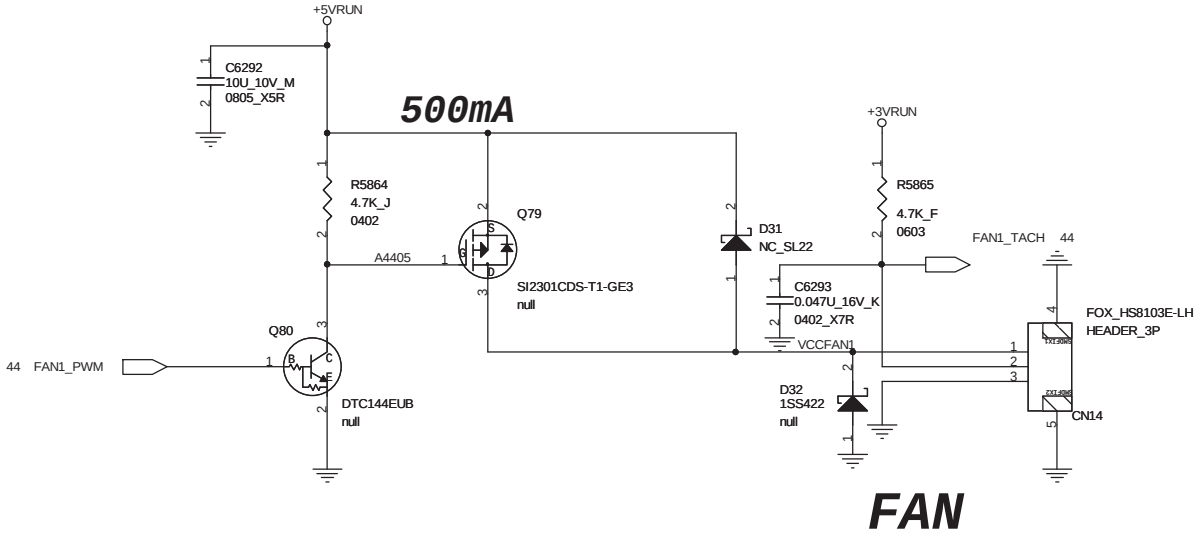
WLAN LED



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Status LED&LID	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 57 of 86	



BFT Test Point(BOT)



FAN

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: **FAN**		
Size: B	Document Number: **W930 H1&H2**	Rev: **SA**
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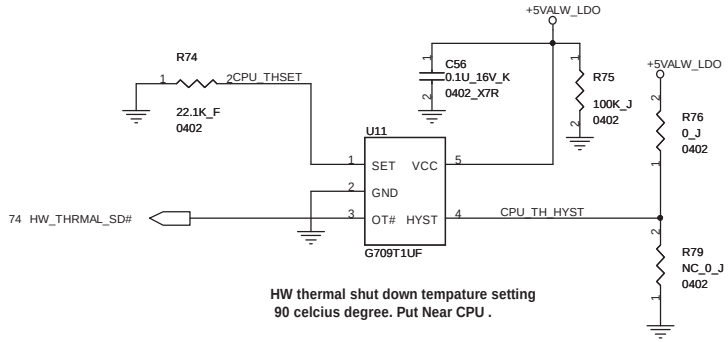
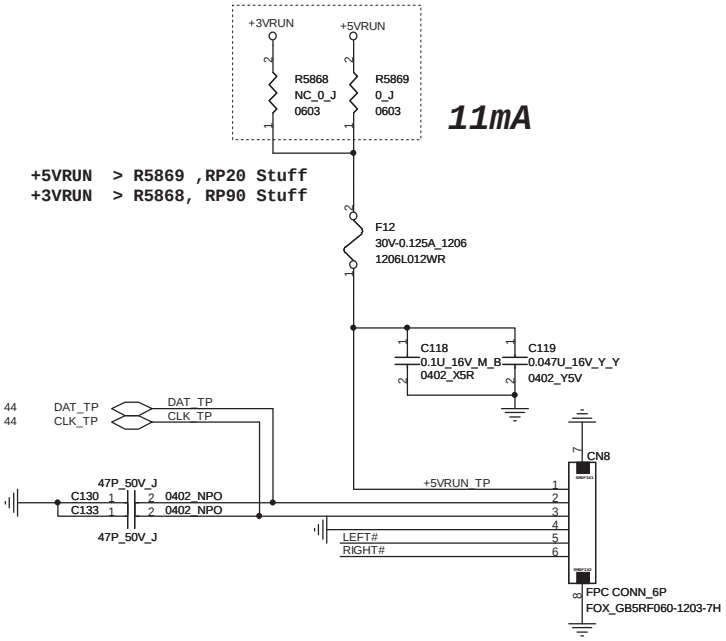
HW THERMAL PROTECTION

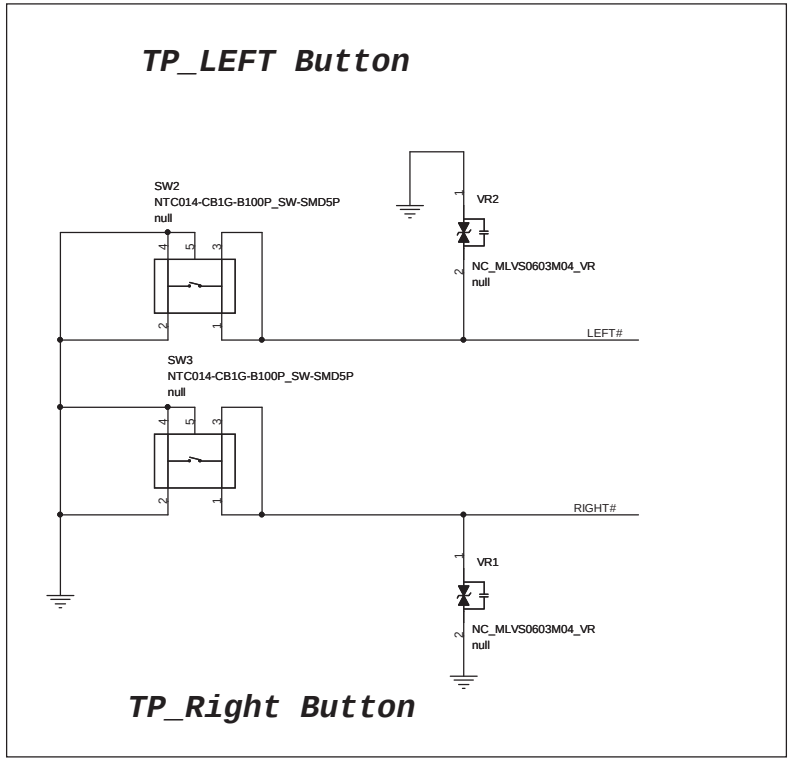


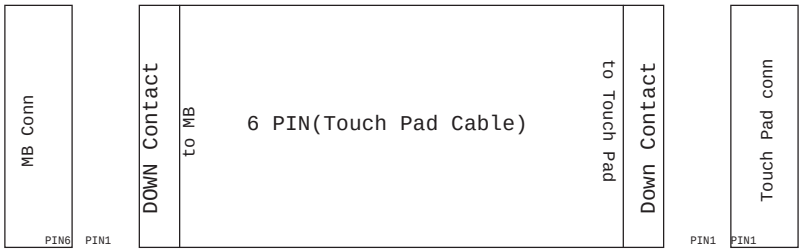
HW thermal shut down tempature setting
90 celcius degree. Put Near CPU .

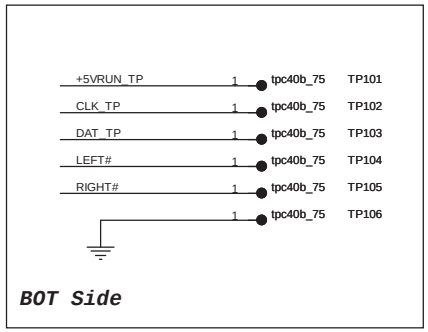
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	***Thermal Sensor***	
Size A3	Document Number ***W930 H1&H2***	Rev ***SA***
Date: Thursday, May 20, 2010	Sheet 59 of 86	



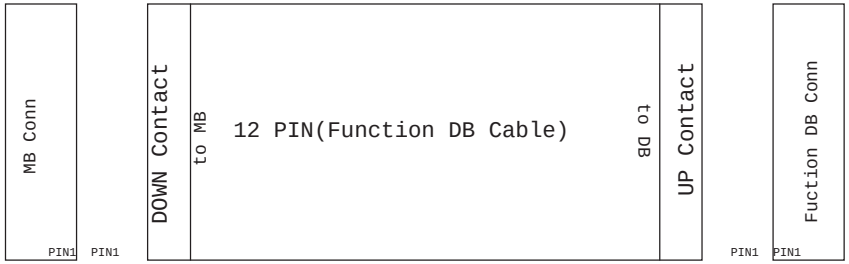
Touch Pad Conn

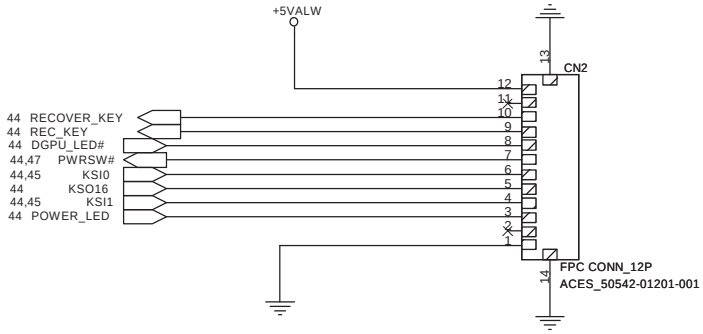




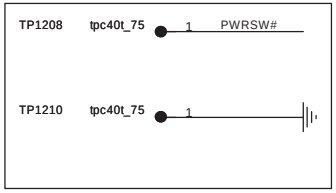


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Touch Pad		
Size: A3	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 60 of 86	

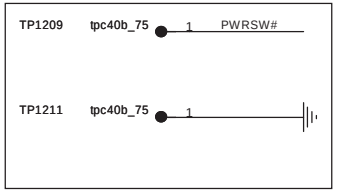




BFT Test Pad(Top)



BFT Test Pad(Bottom)



Function DB Conn.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SWITCH DB Connector	
Size: Custom	Document Number: W930 H1&H2	Rev: SA
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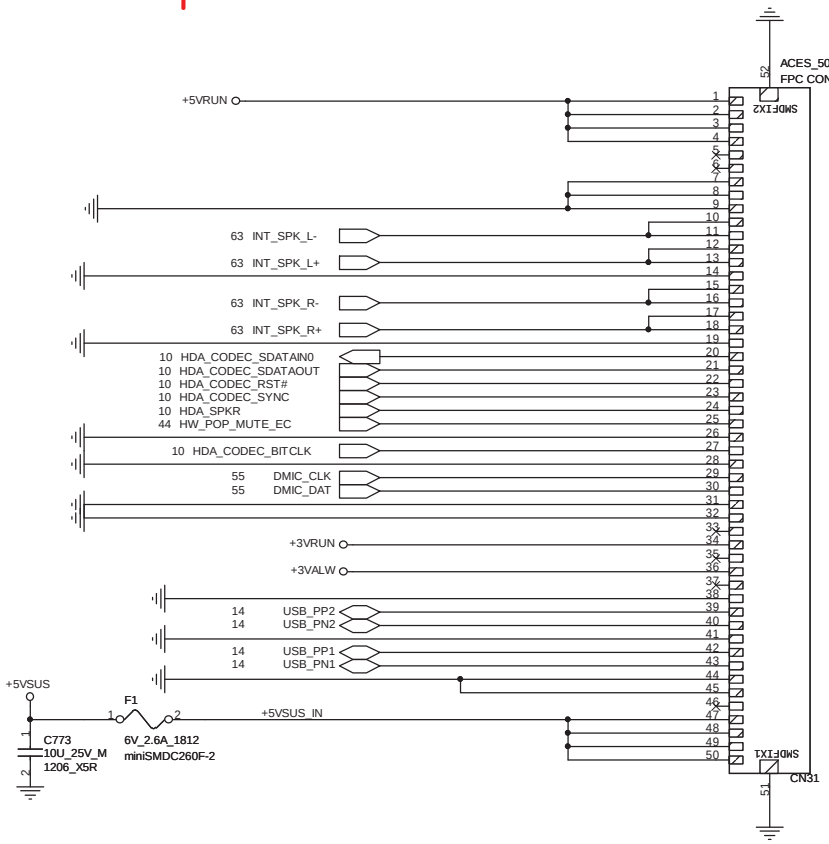

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO/USB DB Conn.	
Size A3	Document Number W930 H1&H2	Rev SA
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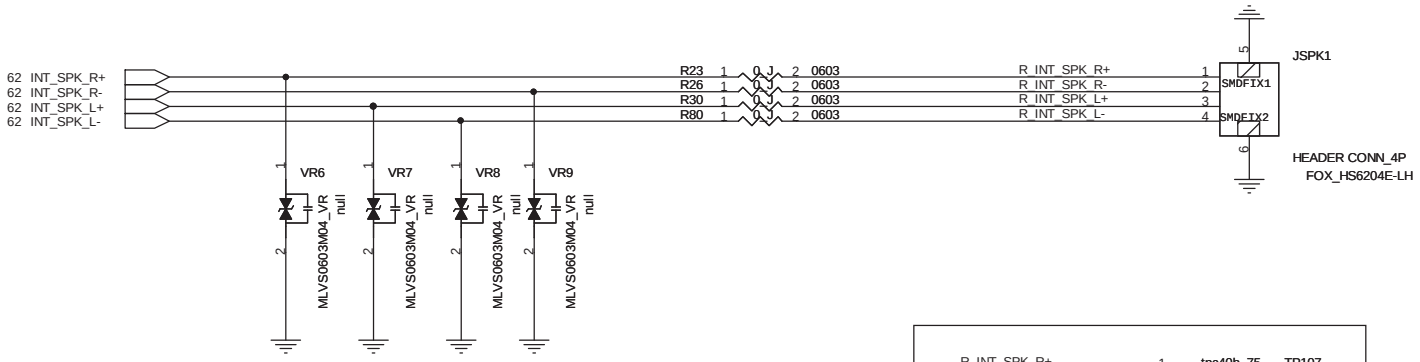
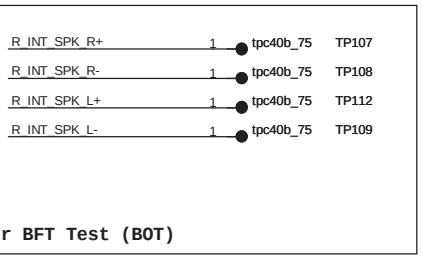
Internal Speaker





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**AUDIO SPEAKER CONNECTOR**	
Size: B	Document Number: **W930 H1&H2**	Rev: **SA**
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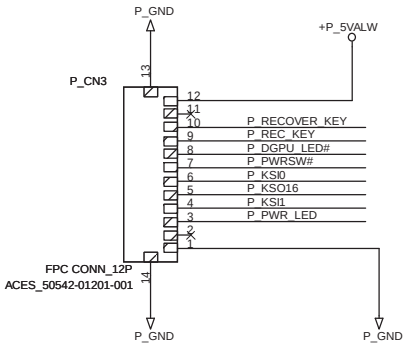
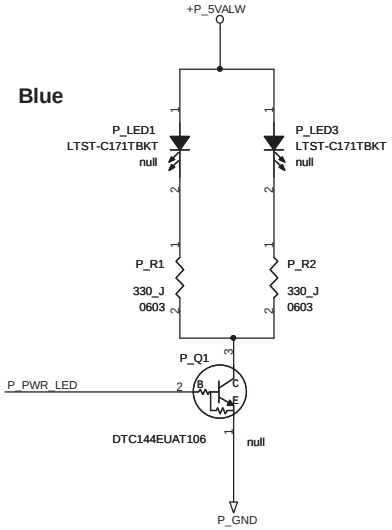


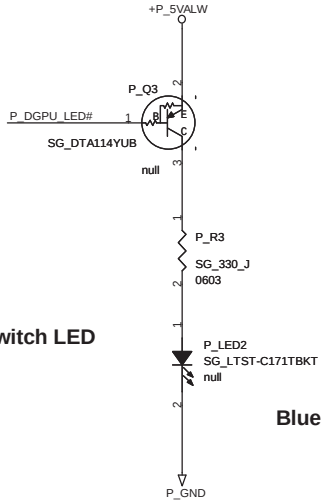
Power LED

Blue

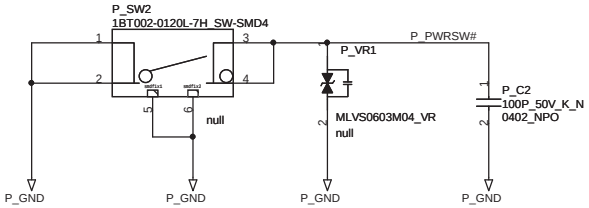


Switch LED

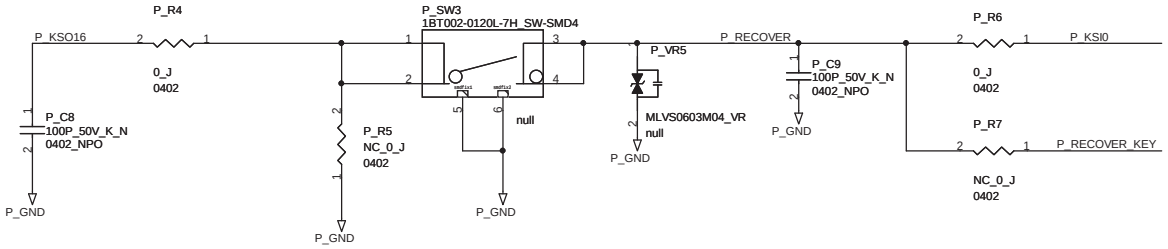
Blue



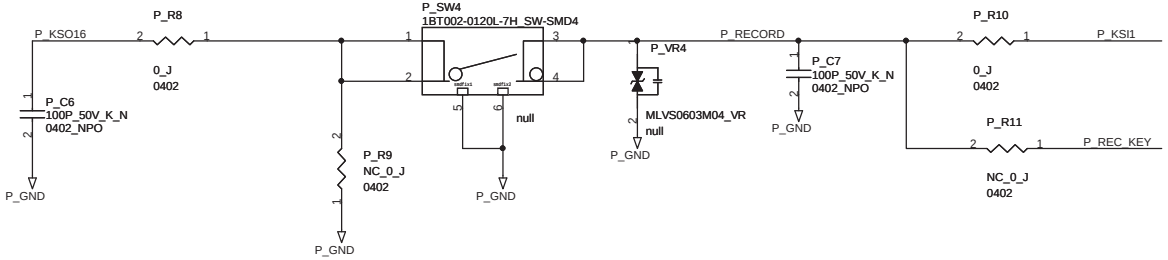
Power Button



One Key Recover Button



Record Button



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Function Board(Botton&LED)	
Size A3	Document Number W930 H1&H2	Rev SA
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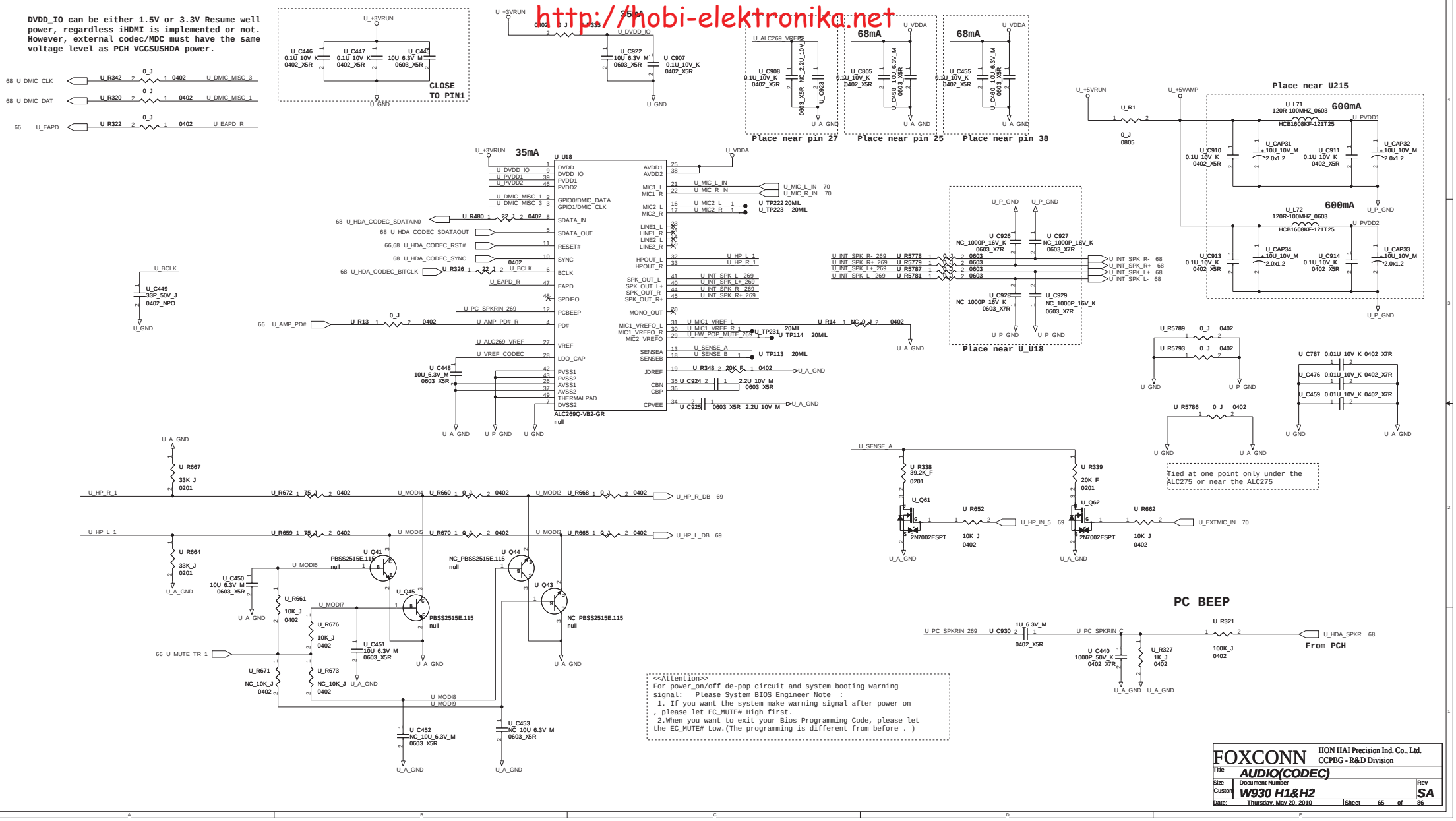
DVDD_IO can be either 1.5V or 3.3V Resume well power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUSHDA power.



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	AUDIO(CODEC)		
Size: Custom	Document Number: W930 H1&H2		Rev: SA
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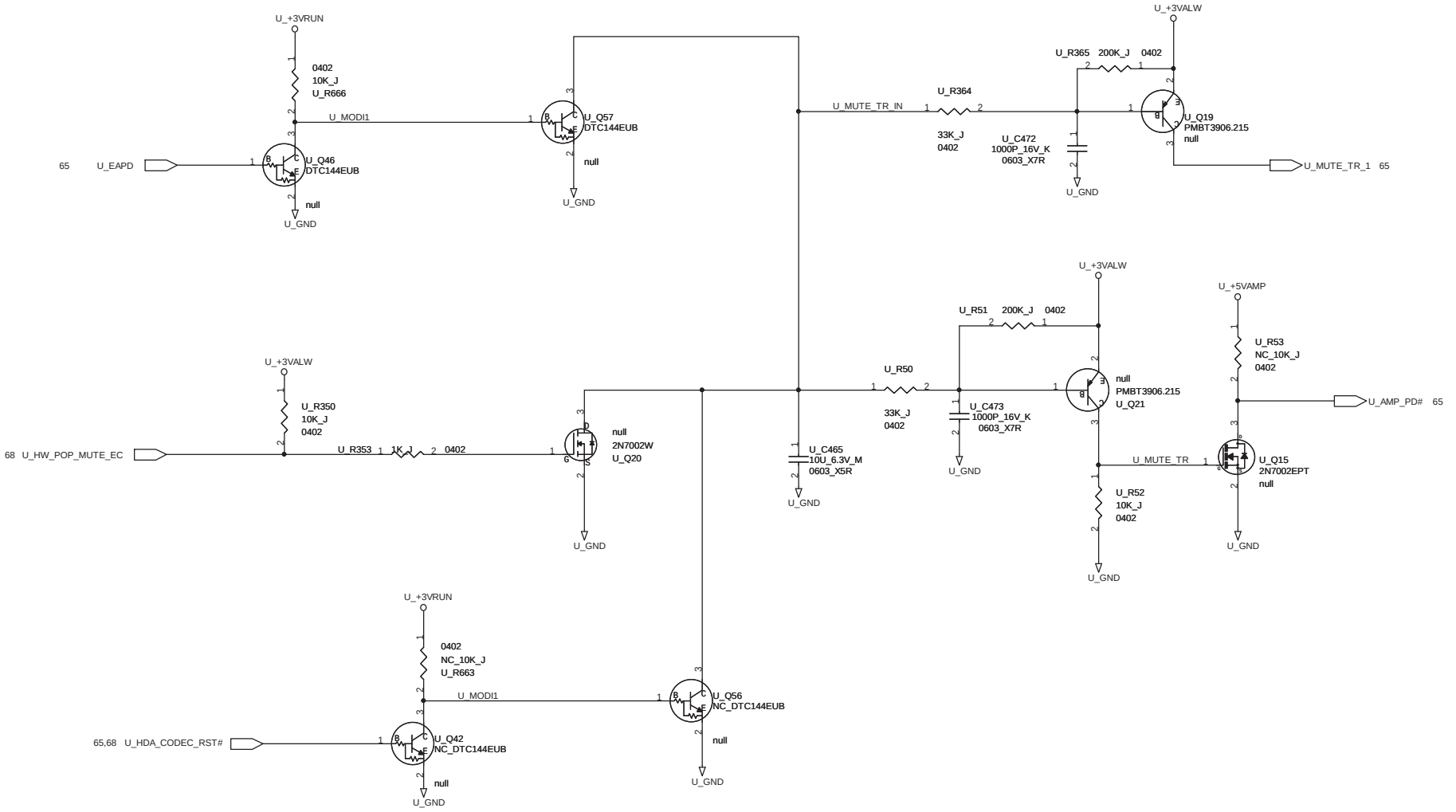

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO (MUTE)	
Size A3	Document Number W930 H1&H2	Rev SA
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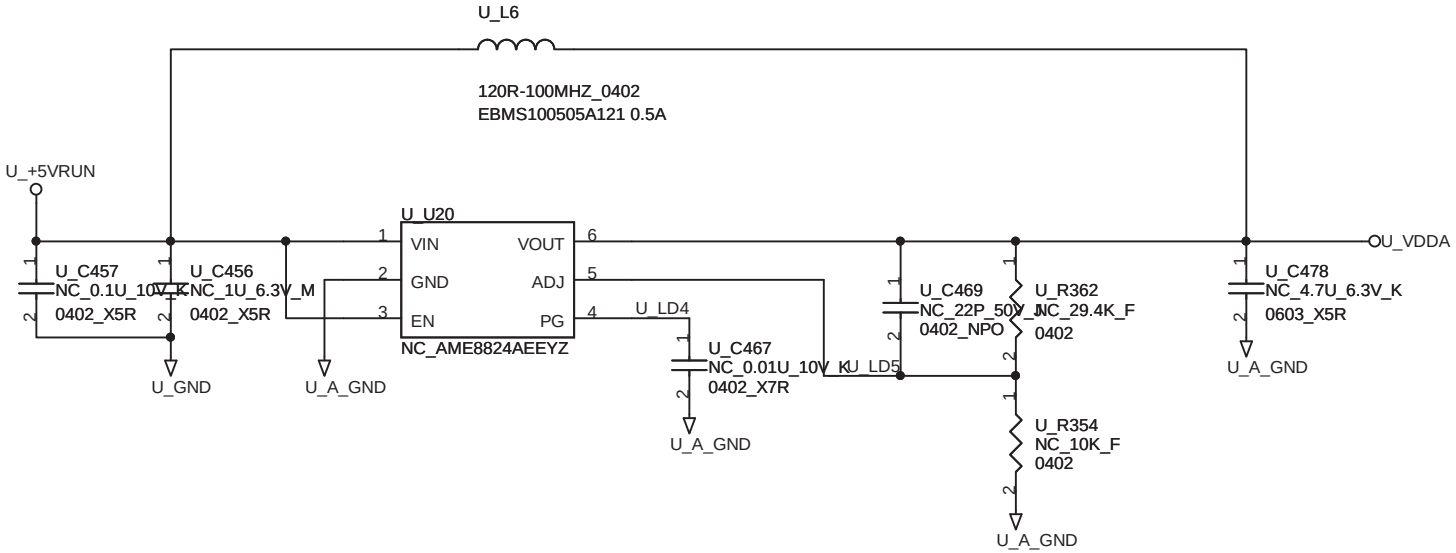
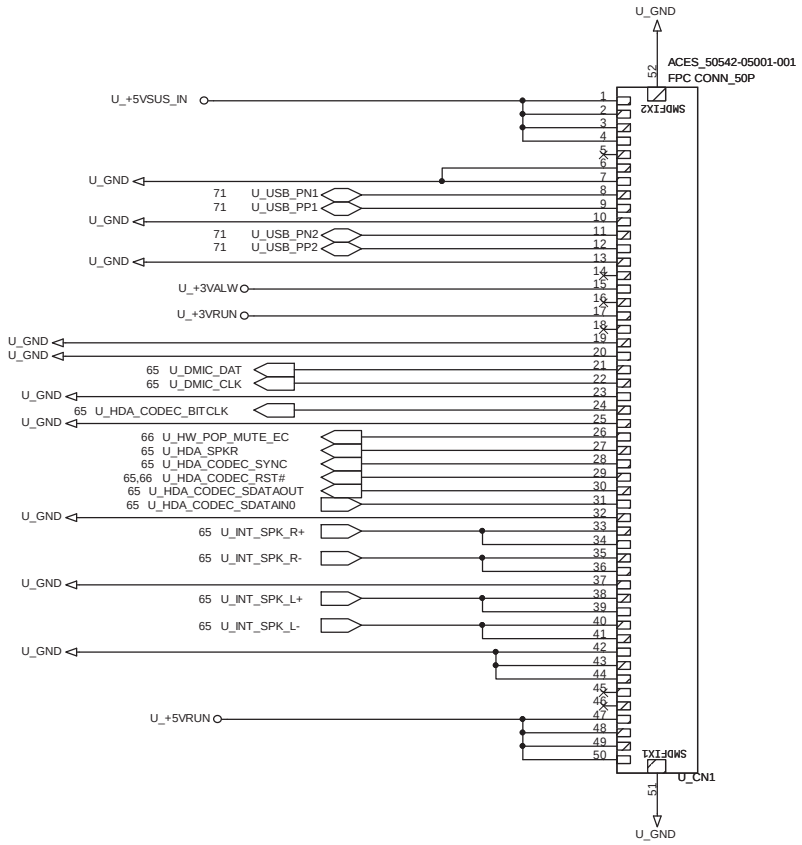
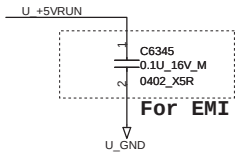


AUDIO POWER(4.75V/200mA)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: AUDIO POWER		
Size: A4	Document Number: W930 H1&H2	Rev: SA
Date: Thursday, May 20, 2010	Sheet 67 of 86	





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO & USB CONN	
Size A3	Document Number W930 H1&H2	Rev SA
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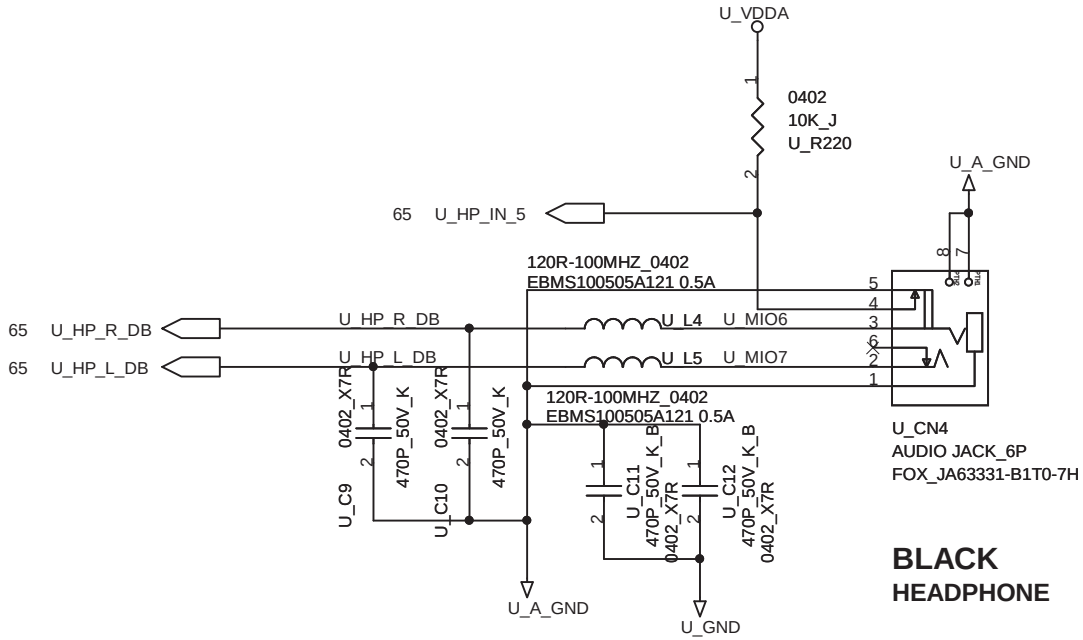
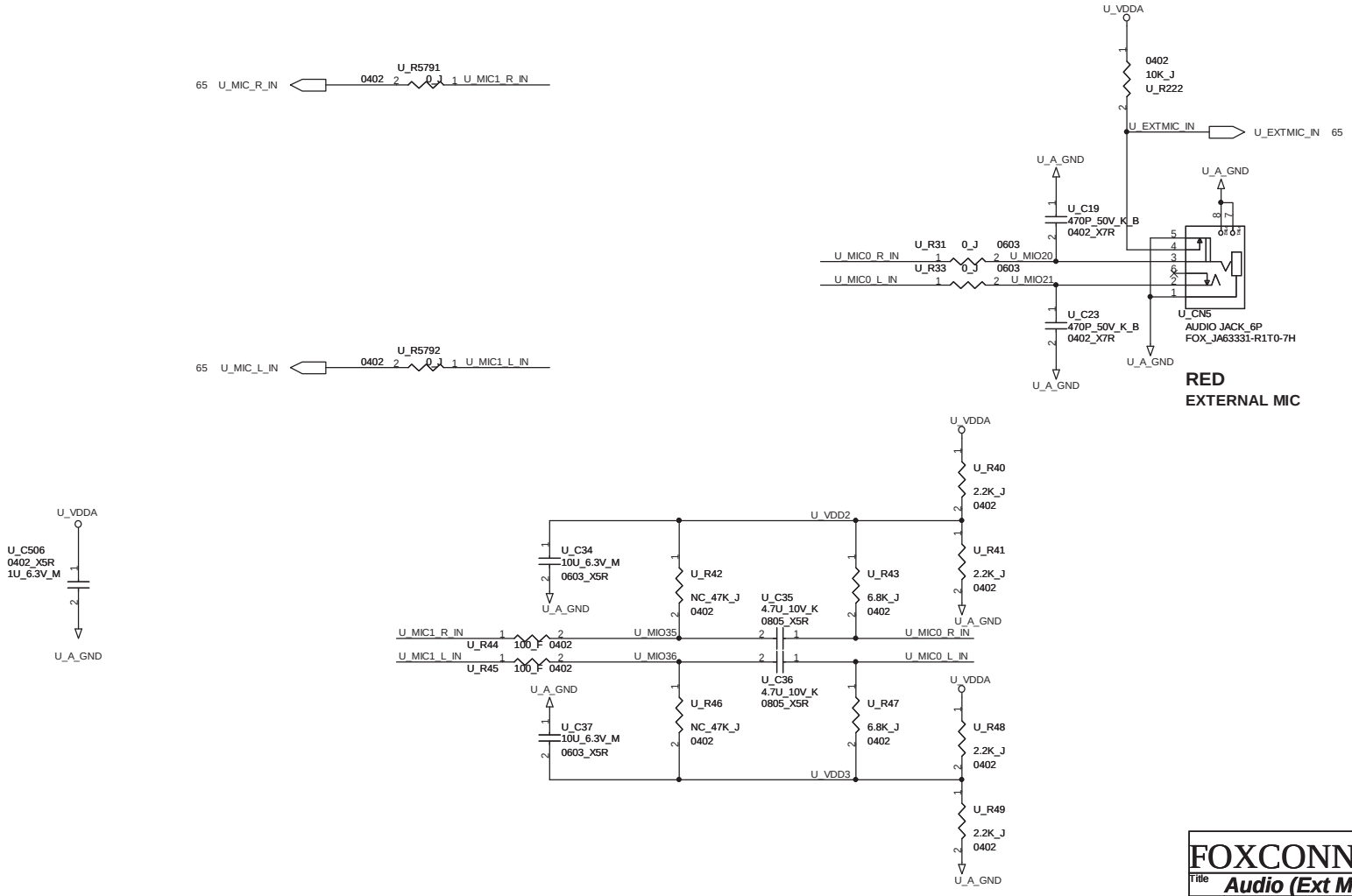


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***Audio (Head Phone Jack)***	
Size A4	Document Number ***W930 H1&H2***	Rev ***SA***
Date: Thursday, May 20, 2010	Sheet 69 of 86	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Audio (Ext MIC Jack)	
Size A3	Document Number W930 H1&H2	Rev SA
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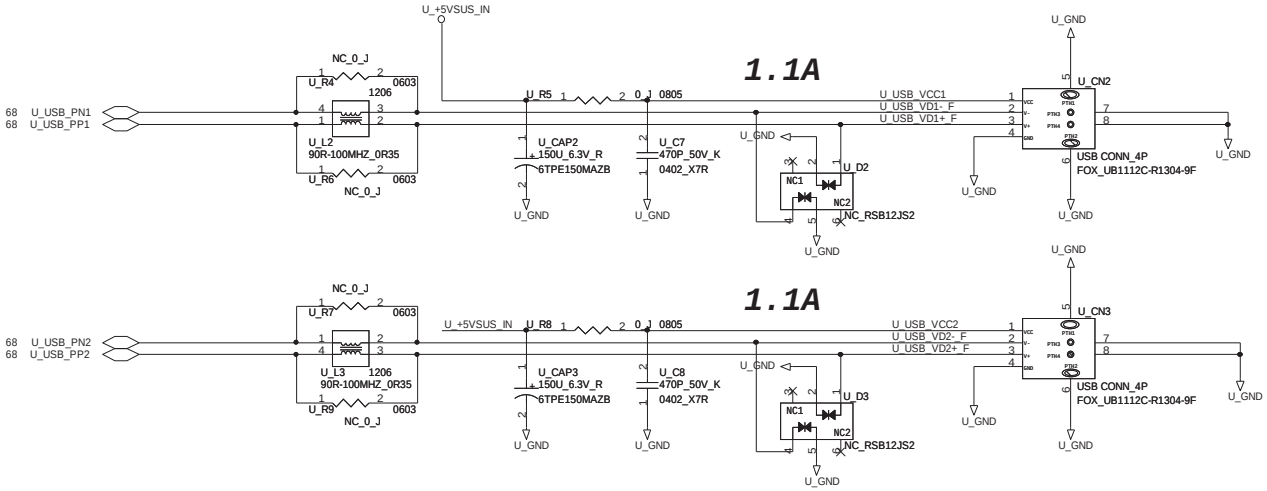
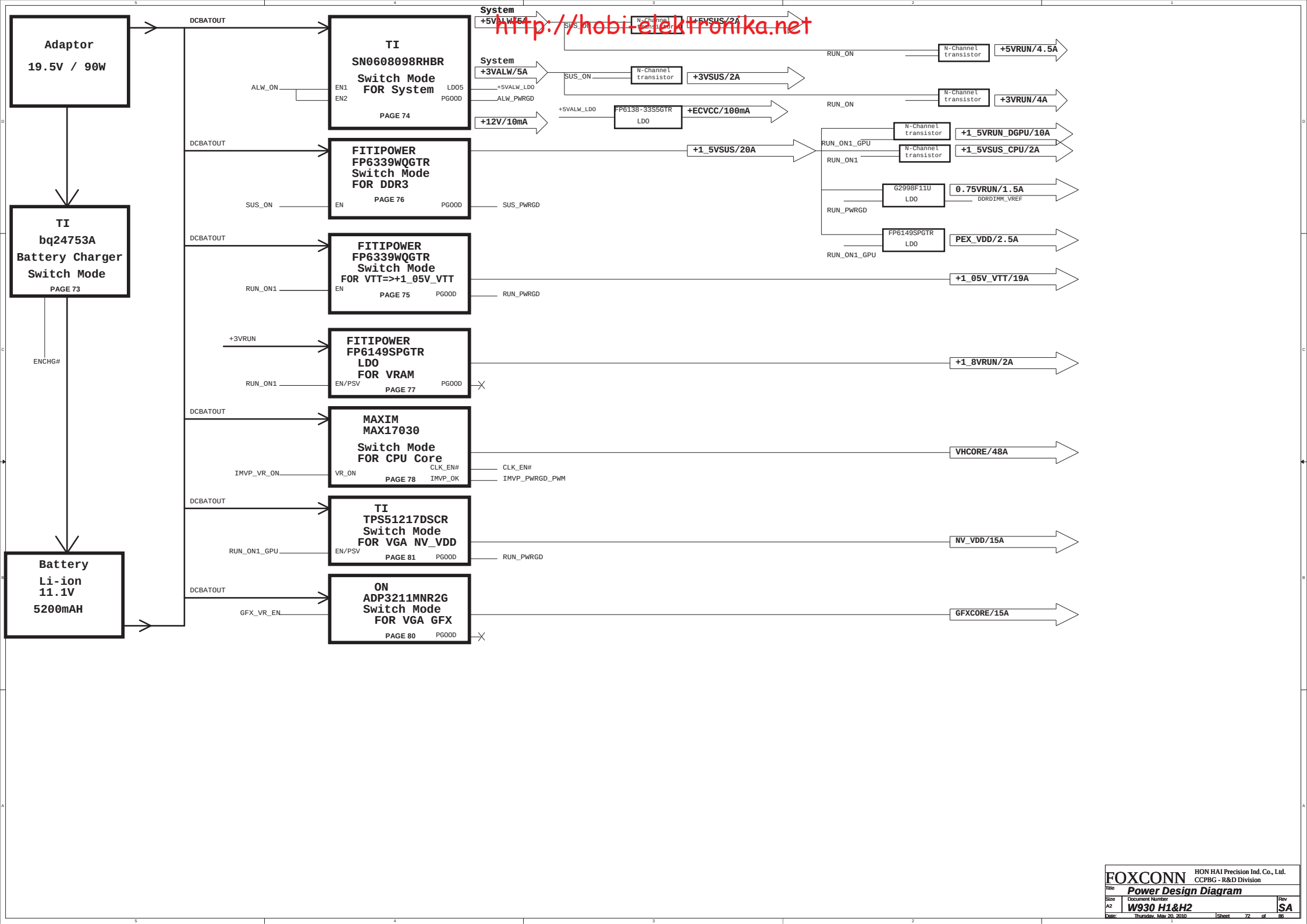


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	***Audio (USB Port)***	
Size: Custom	Document Number: ***W930 H1&H2***	Rev: ***SA***
Date: Thursday, May 20, 2010	Sheet 71 of 86	



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: Power Design Diagram

Size: A2 | Document Number: W930 H1&H2 | Rev: SA

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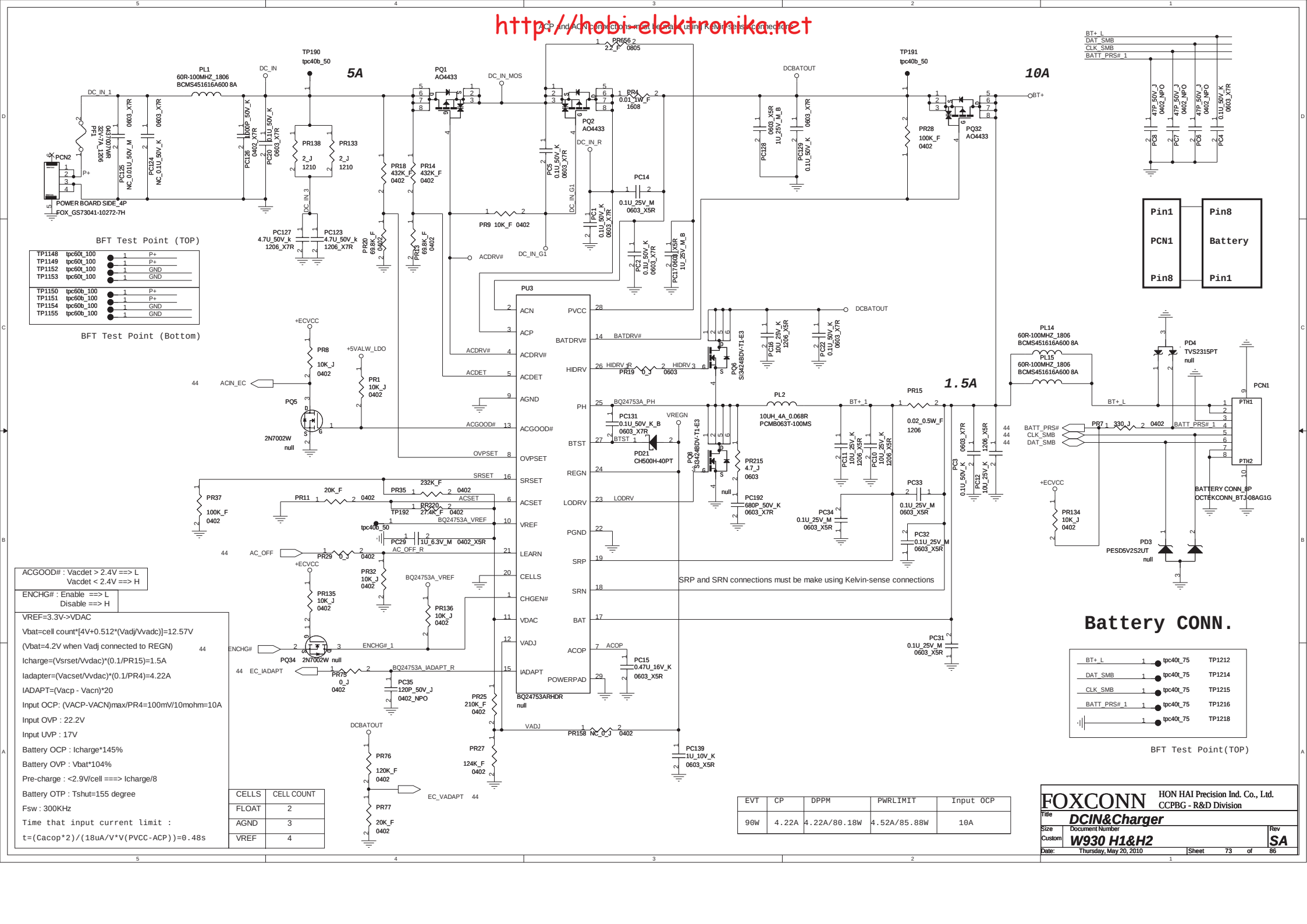

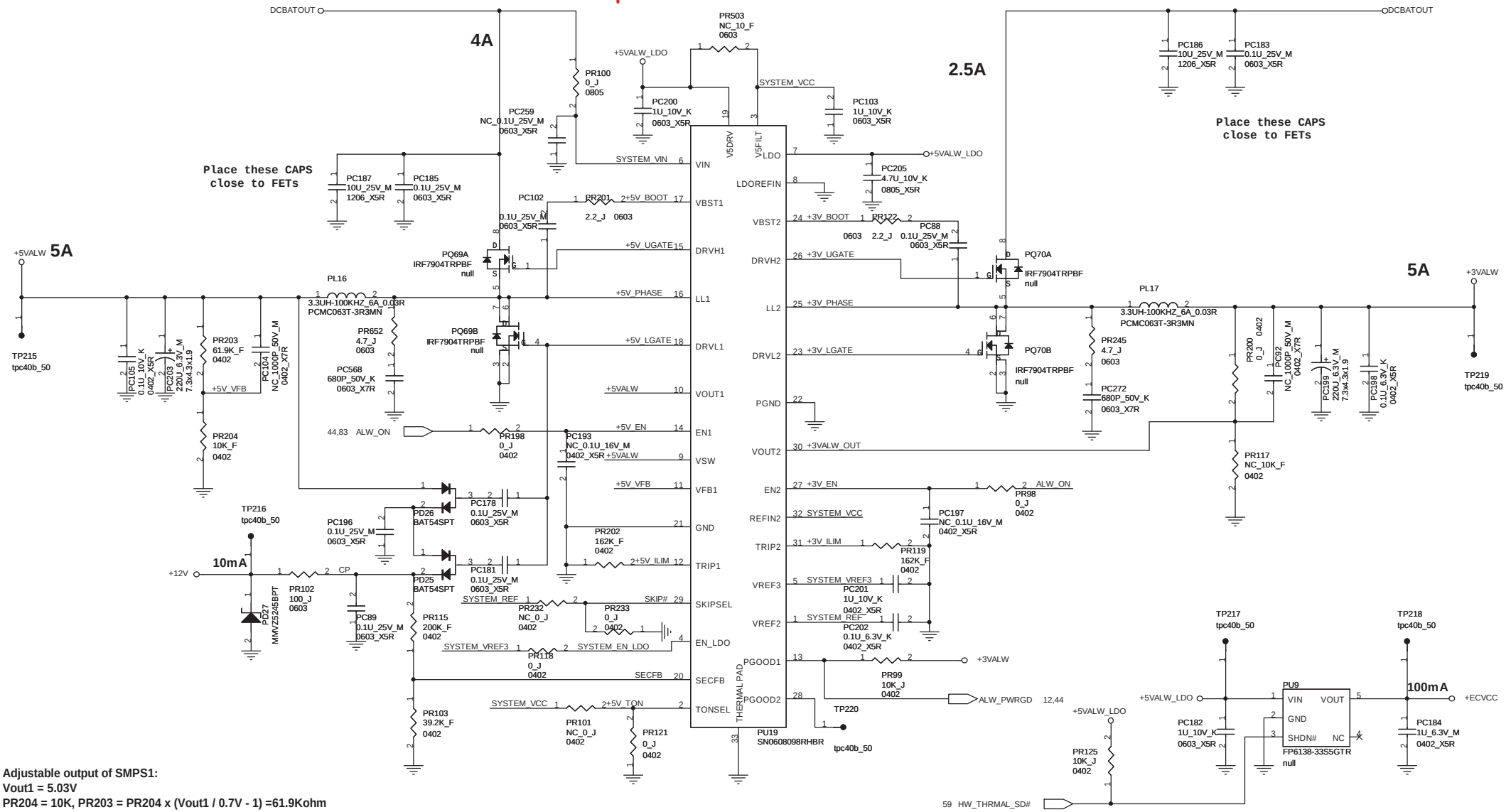

Adjustable output of SMPS1:
Vout1 = 5.03V
PR204 = 10K, PR203 = PR204 x (Vout1 / 0.7V - 1) =61.9Kohm

Second Feedback :
Vout_sec = 12.2V, PR103 = 39.2Kohm
PR115 = PR103 x (Vout_sec / 2V - 1) =200Kohm

TON	Operating Frequence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
Rocp=(Iocp-Iripple/2)*(10*Rds(on))/5uA
+5VALW=((PR203/PR204)+1)*VFB1

Current limit resistor for SMPS1 :
OCP=7.64A
Ivalley_5 = 6.23A, Rcs_5 = Rds1 = 13mohm
PR202 = (10 x Ivalley_5 x Rcs_5) / 5uA = 162K

Current limit resistor for SMPS2 :
OCP=7.06A
Ivalley_3 = 6.23A, Rcs_3 = Rds2 = 13mohm
PR119 = (10 x Ivalley_3 x Rcs_3) / 5uA = 162K

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **SYS Power (+3_3V/+5V)**
Size: A3
Document Number: **W930 H1&H2**
Rev: **SA**
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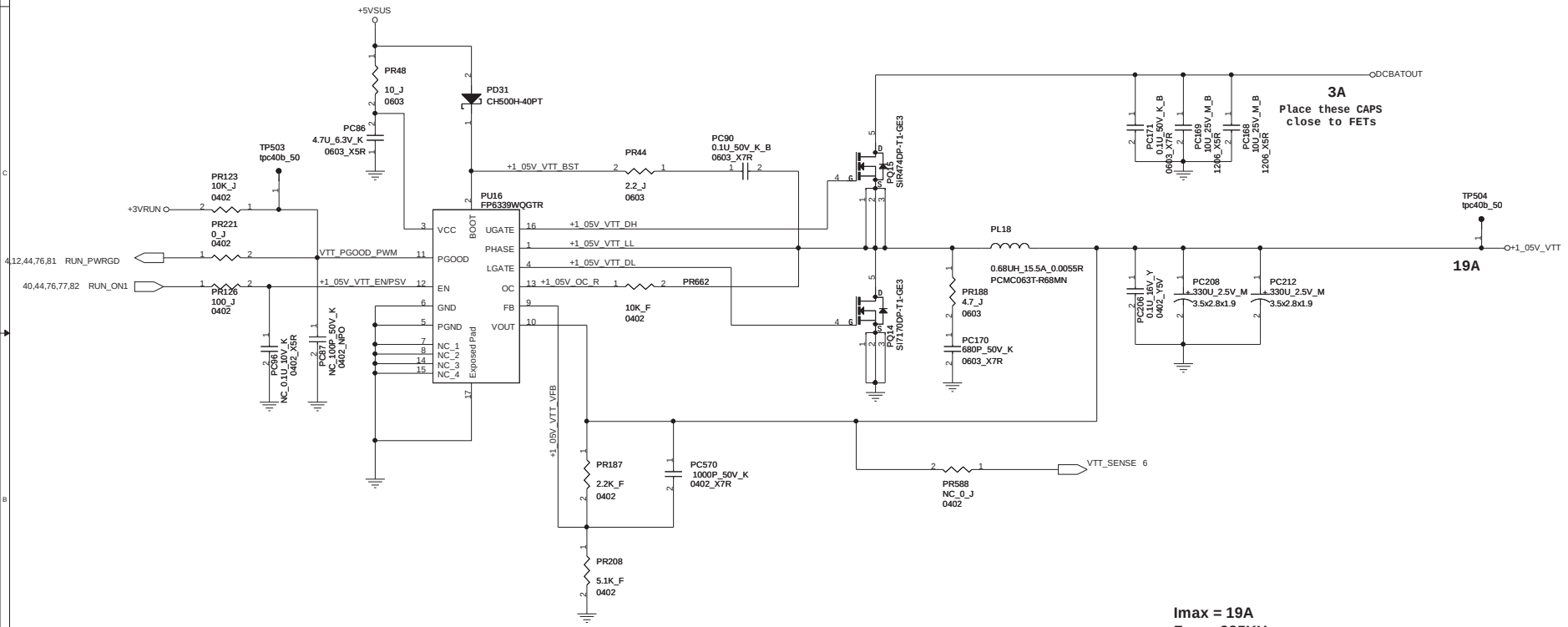
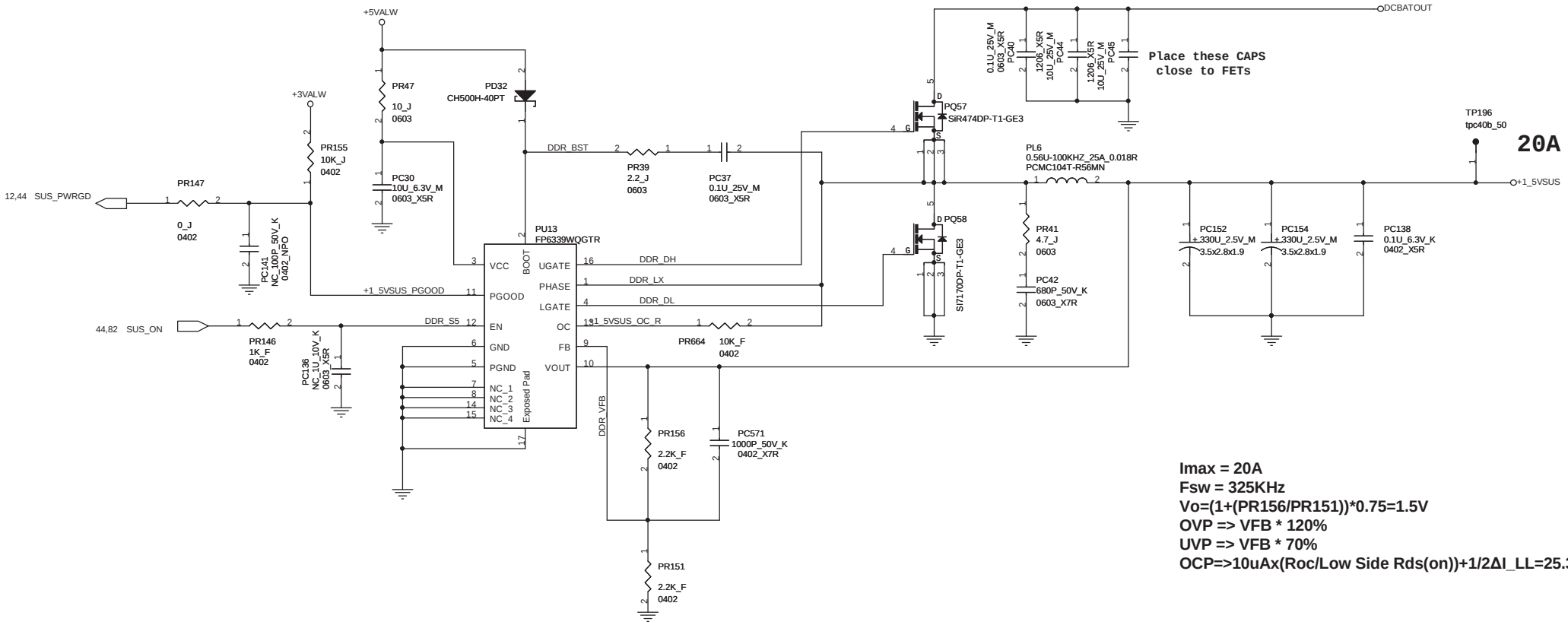


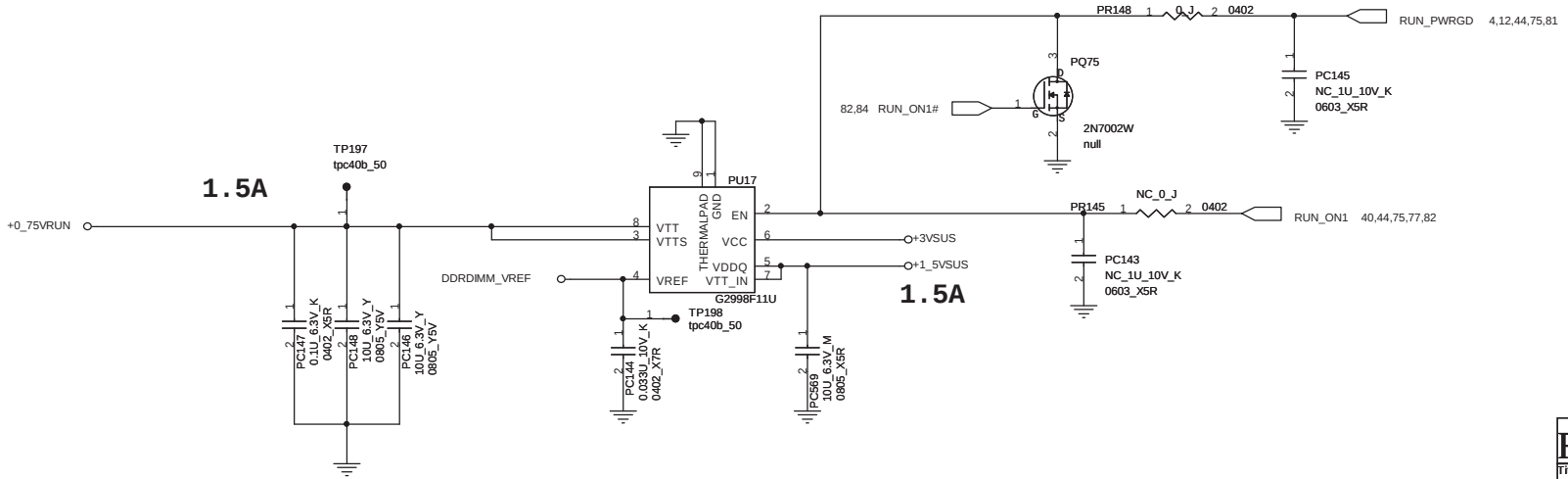
Imax = 19A
Fsw = 325KHz
Vo=(1+(PR187/PR208))*0.75=1.05V
OVP => VFB * 120%
UVP => VFB * 70%
OCP=>10uAx(Roc/Low Side Rds(on))+1/2ΔI_LL=25.57A

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	*SYS Power(+1_05V_VTT)*	
Size: Custom	Document Number: *W930 H1&H2*	Rev: *SA*
Date: Thursday, May 20, 2010	Sheet 75 of 86	

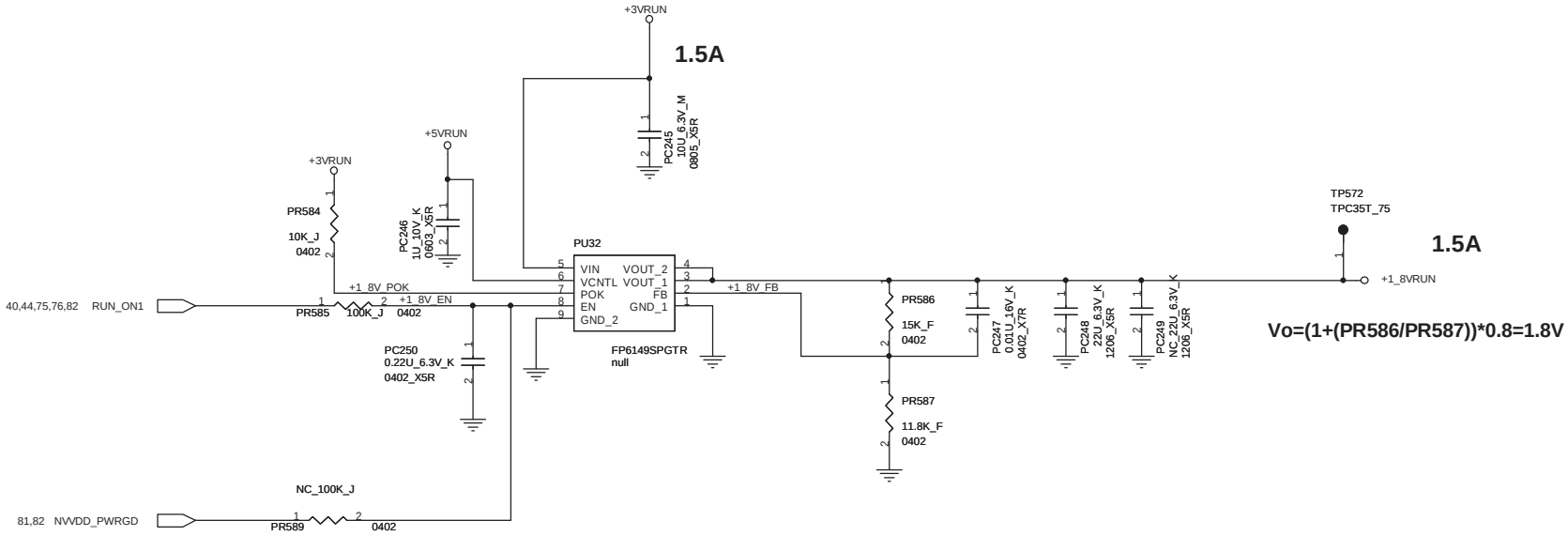
4A



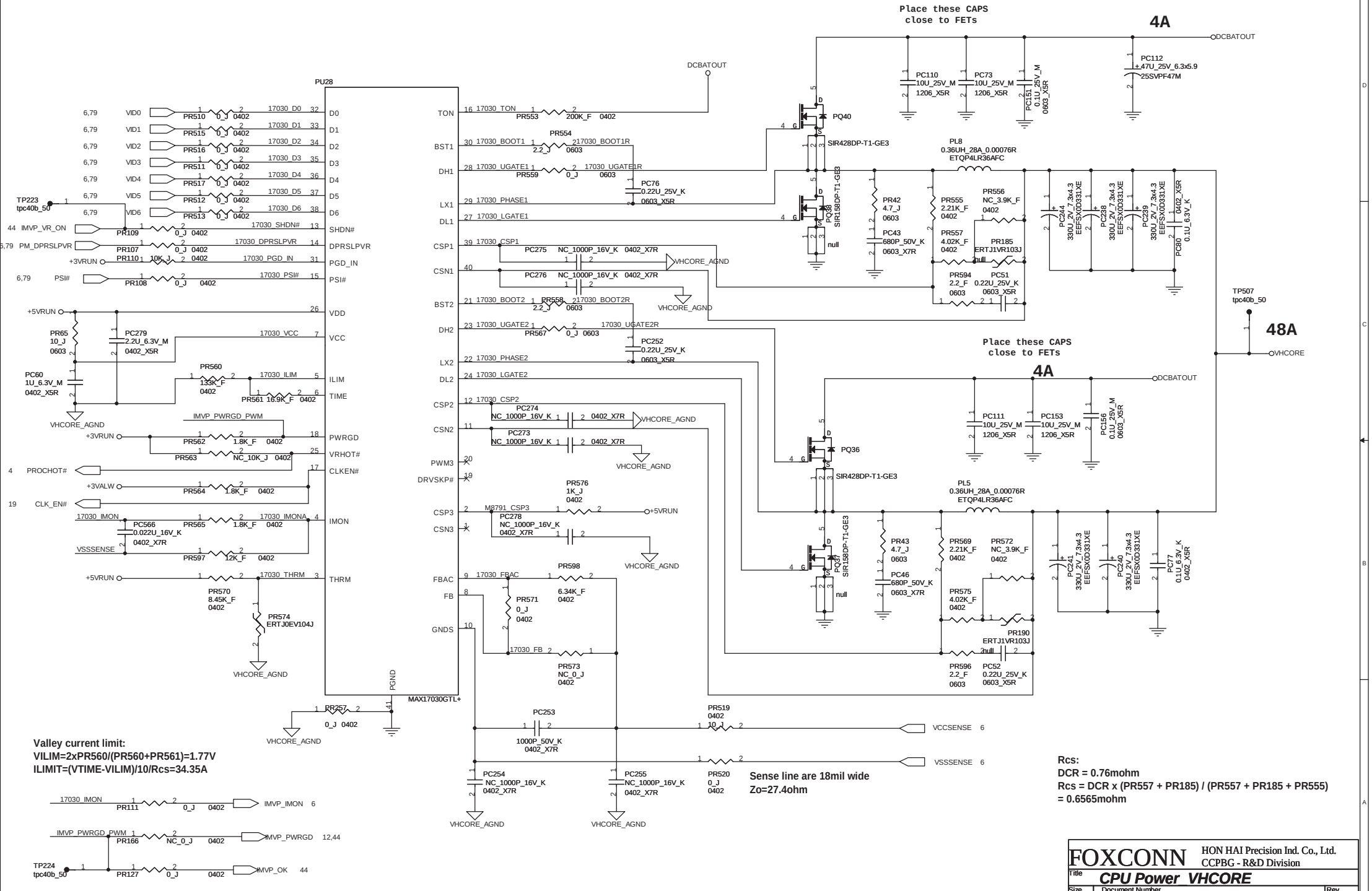
Imax = 20A
Fsw = 325KHz
Vo=(1+(PR156/PR151))*0.75=1.5V
OVP => VFB * 120%
UVP => VFB * 70%
OCP=>10uAx(Roc/Low Side Rds(on))+1/2ΔI_LL=25.32A



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR3 Power(+1_5V/+0_75V)	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 76 of 86	



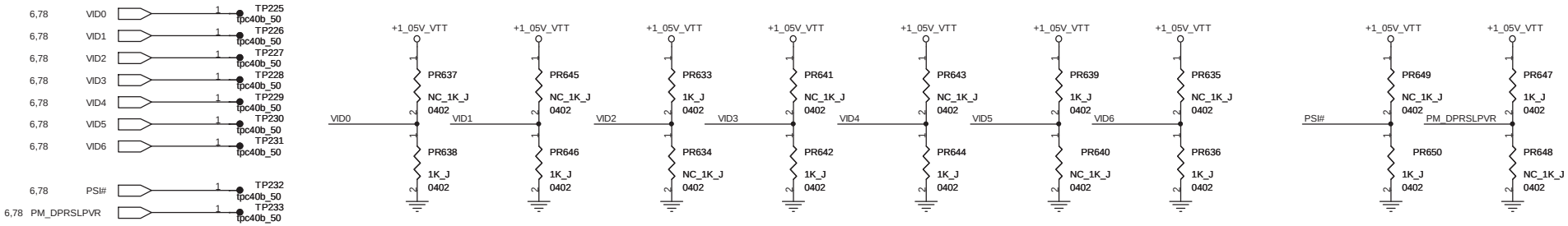
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power(+1_8V)	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 77 of 86	



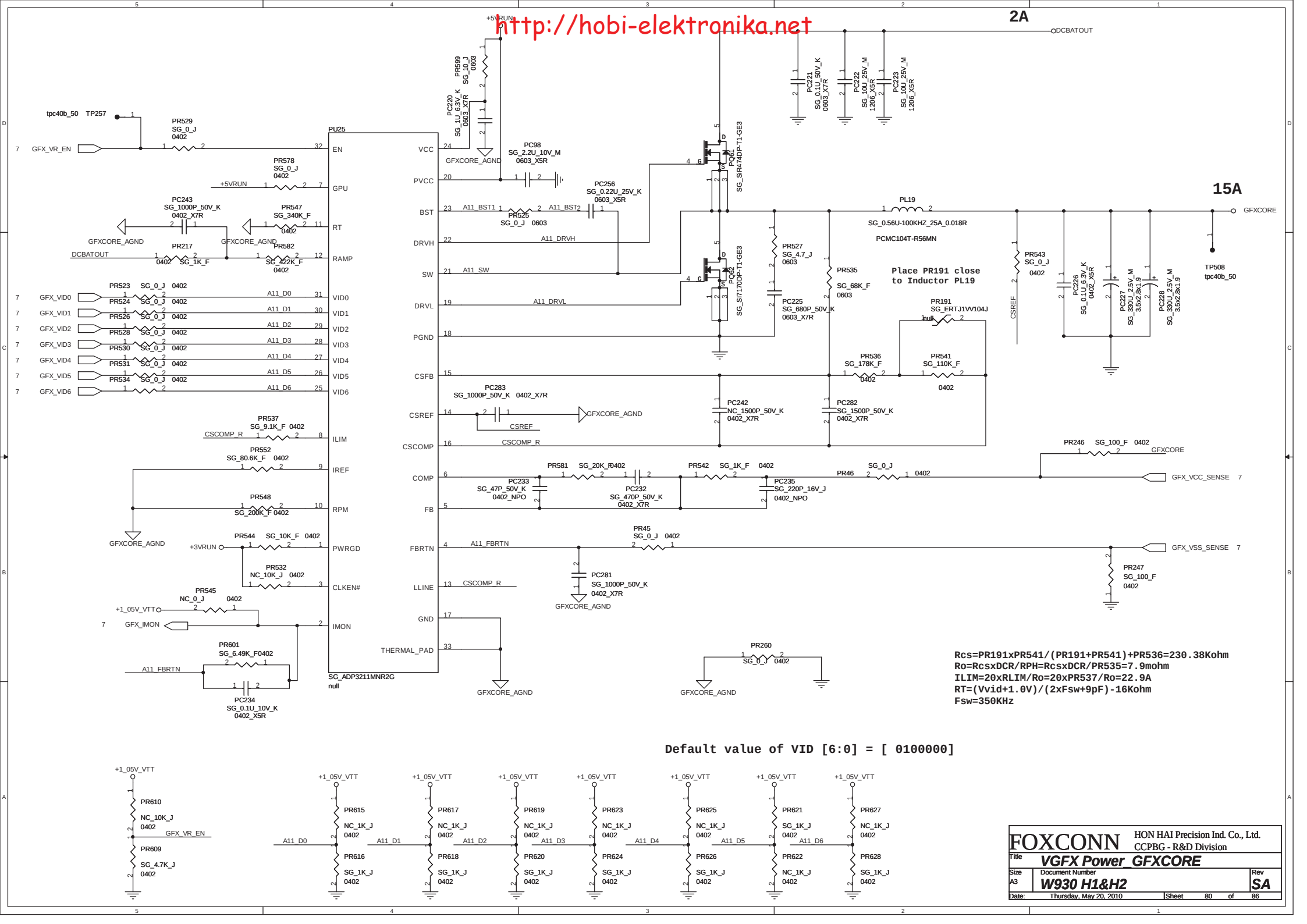
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CPU Power VHCORE	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 78 of 86	

Default value of VID [6:0] = [0100100] , PSI = 0 , PROC_DPRSLPVR = 1

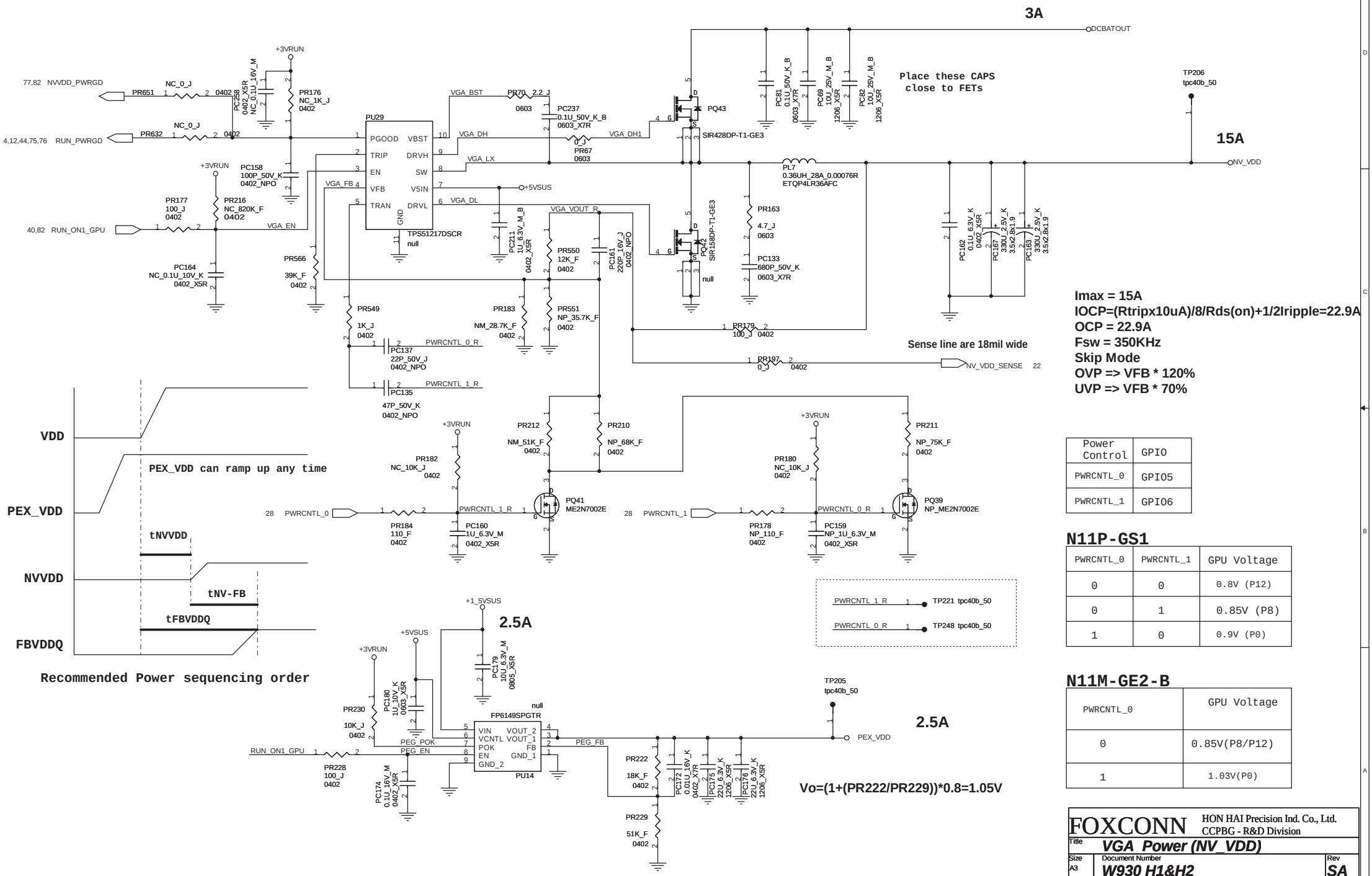
VHCORE=1.05V



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	CPU Power_VID		
Size A3	Document Number W930 H1&H2		Rev SA
Date: Thursday, May 20, 2010	Sheet 79 of 86		



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	VGFX Power_GFXCORE		
Size A3	Document Number W930 H1&H2		Rev SA
Date: Thursday, May 20, 2010	Sheet 80 of 86		



Power Control	GPIO
PWRCNTL_0	GPIO5
PWRCNTL_1	GPIO6

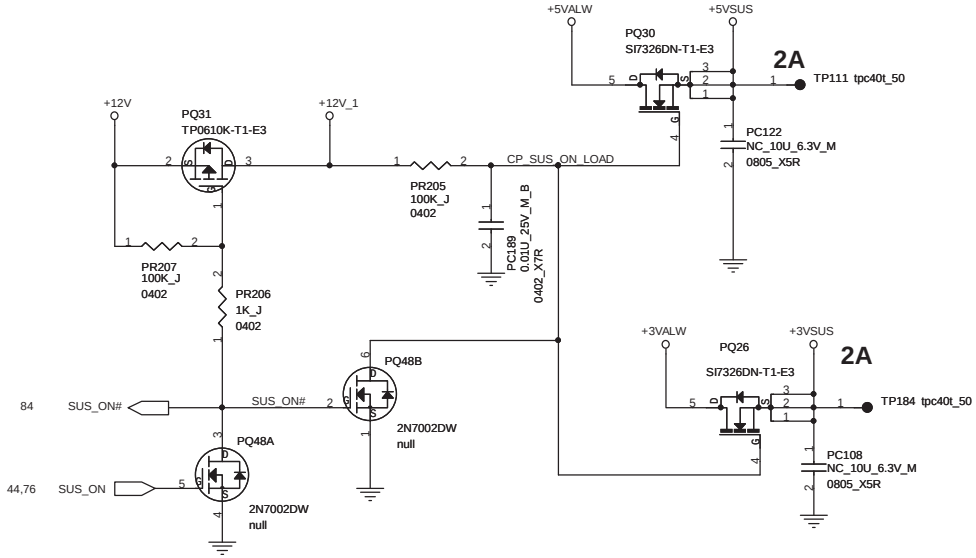
N11P-GS1

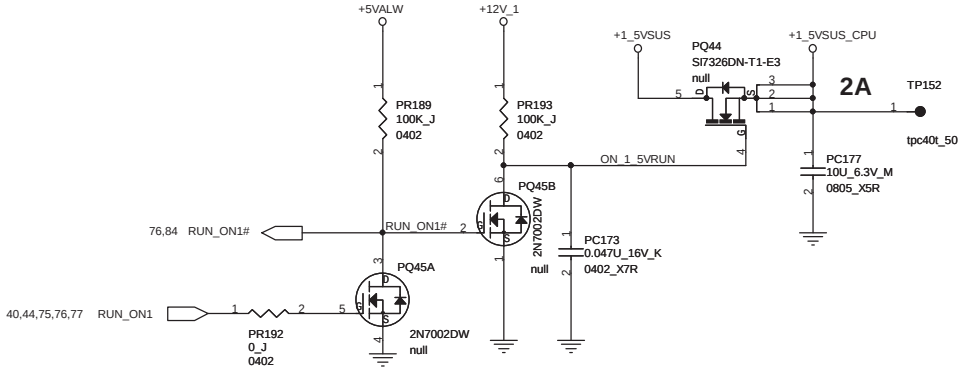
PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	0	0.8V (P12)
0	1	0.85V (P8)
1	0	0.9V (P0)

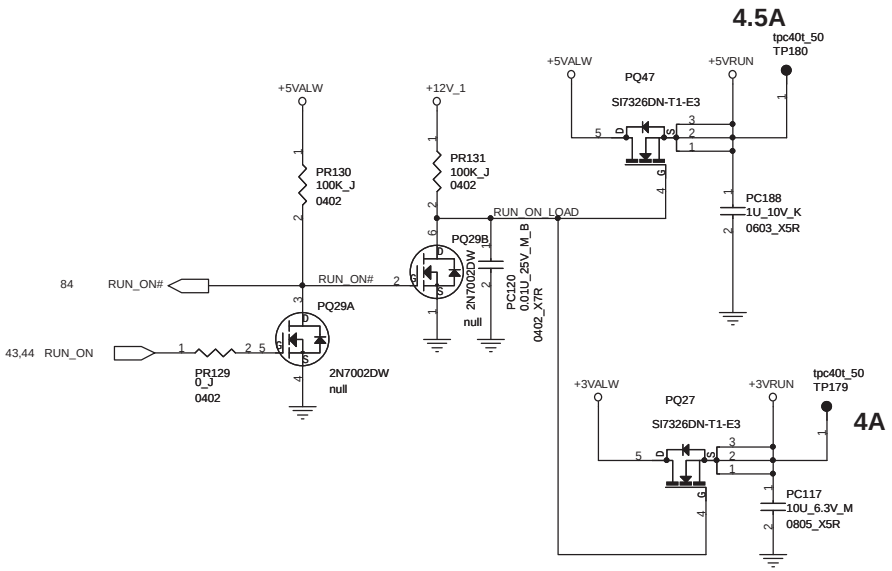
N11M-GE2-B

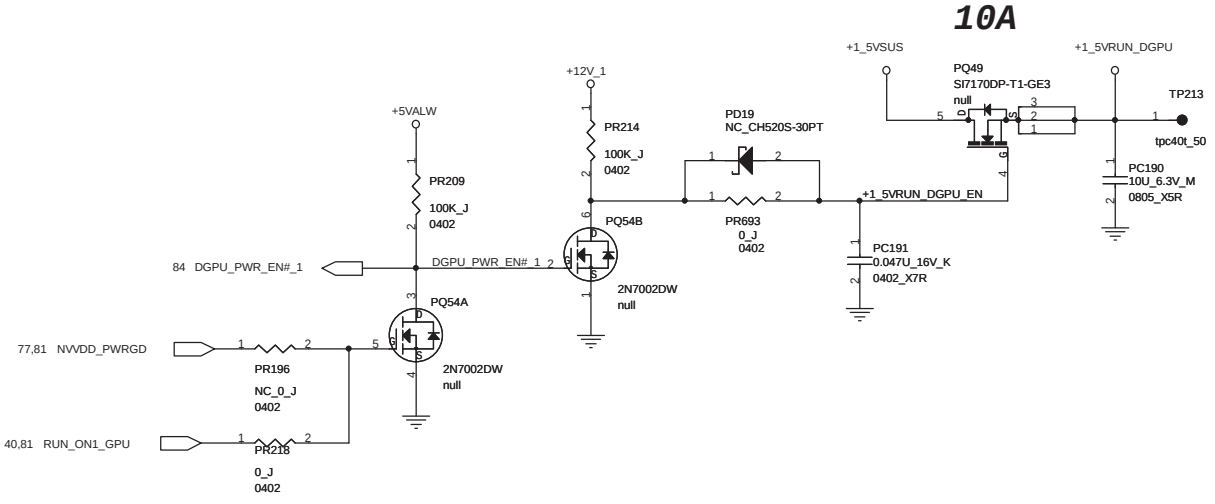
PWRCNTL_0	GPU Voltage
0	0.85V(P8/P12)
1	1.03V(P0)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VGA_Power (NV_VDD)	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 81 of 86	









FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Others power plan	
Size A3	Document Number W930 H1&H2	Rev SA
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Wireless card

null
BOSS_4x4.5
BOSS1

null
BOSS_4x4.5
BOSS2

Blue Tooth

null
BOSS_4x4.2
BOSS3

Thermal

null
BOSS_4.45x5
BOSS4

null
BOSS_4.45x5
BOSS5

LABLE1
NC_AMI-APTIO

AMI Label (For MP Only)

CPU

H1
hole_c158d158n

H2
hole_c158d158n

H3
hole_c158d158n

H4
hole_c158d158n

Type A

H5
hole_tbs315x315d91

H6
hole_tbs315x315d91

H7
hole_tbrsh276x217d91

H8
hole_tr315x315br299x315d91

H9
hole_tbs315x315d91

H10
hole_tbs315x315d91

H11
hole_tbs315x315d91

H18
hole_tbs315x315d91

Type D

PAD1
pad_smd315x197

PAD2
pad_smd315x197

PAD4
pad_smd315x197

Type E

H12
hole_tbsh472x315d91do154x75n

Type F

PAD3
pad_smd236x197

Type N

H15
hole_tbsh492x315d91d79n

Audio&USB

U_H1
hole_tbsh661x315d91d91d83n
U_GND

U_H2
hole_tbrsh256x315d91do83x95n
U_GND

U_H3
hole_tbrsh315x315d91
U_GND

Function DB

P_H1
hole_tsh220x354bc220d91d79n
P_GND

P_H2
hole_tsh354x209bshd91d79n
P_GND

Type H

H13
hole_tbsh276x298d91_a60

Type B

H16
hole_odo315x126n

Type K

H14
hole_tc217bc158d91

Type O

H17
hole_tbr236x236d83

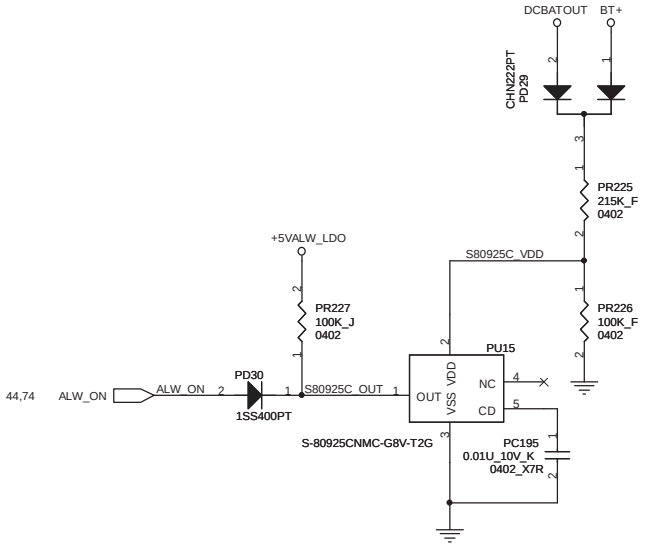
Type P

H19
hole_tsh187x236bc97d87d43n

Type Q

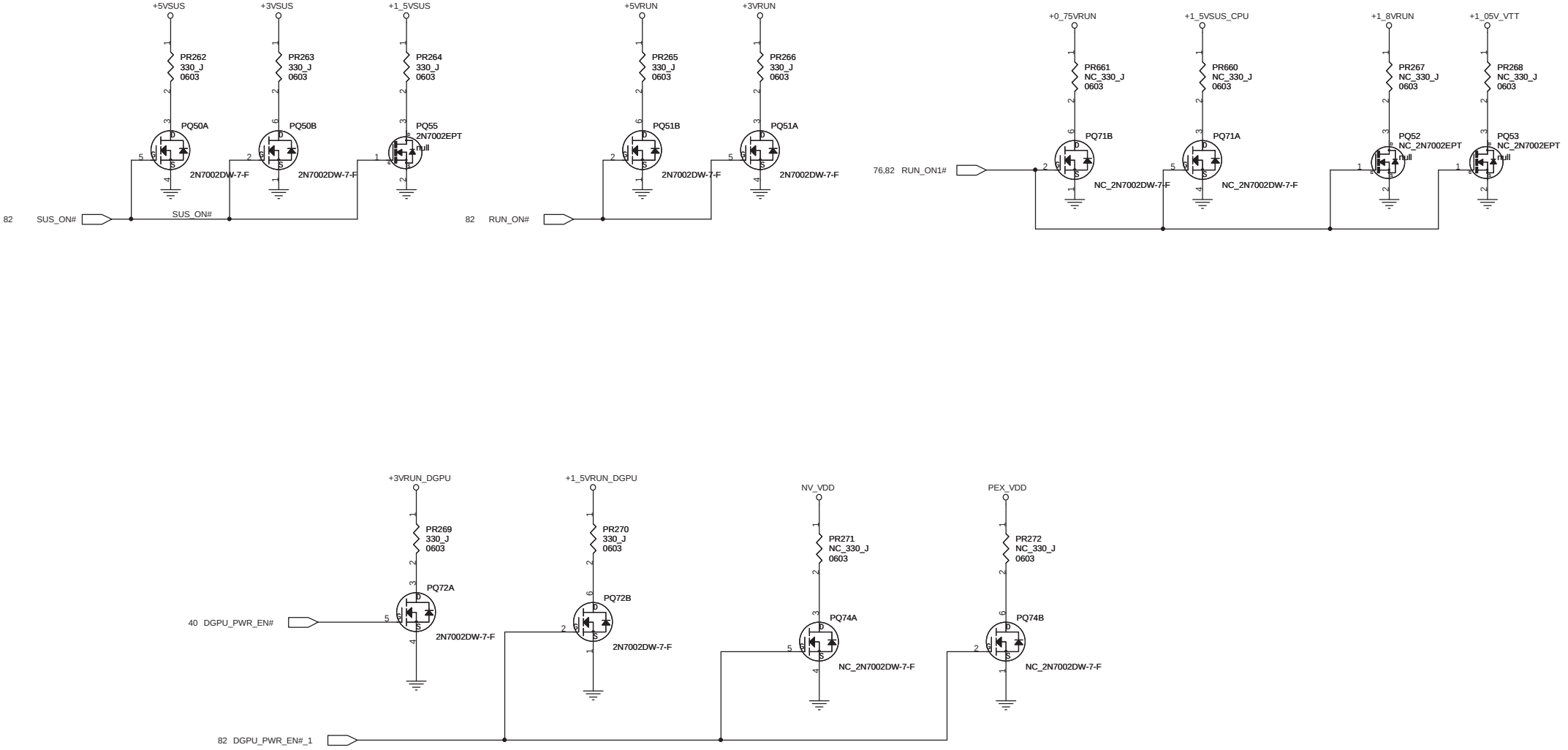
H20
hole_tsh187x236bc97d87d43n_u

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HOLE	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 83 of 86	



Battery UVP Protect(8.475V)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	OVP protection	
Size A3	Document Number W930 H1&H2	Rev SA
Date: Thursday, May 20, 2010	Sheet 83 of 86	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DISCHARGE CIRCUIT	
Size: A3	Document Number: W930 H1&H2	Rev: SA
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2010/05/11

P64:Add P_LED3,P_R2 for Power LED base on ME request.

2010/05/12

P61:Change CN2 from 1N-0012000-F000 to 1N-0012000-FKG0.

P64:Change P_CN3 from 1N-0012000-F000 to 1N-0012000-FKG0.

P74:Del PJ2,PJ17.Change +5VALW_PWM to +5VALW,Del +3VALW_PWM.

P75:Del PJ39,+1_05V_VTT_PWM.

P76:Del PJ44,PJ11;Del +1_5VSUS_PWM,+0_75VRUN_VTT.

P77:Del PJ15,+1_8VRUN_VOUT.

P80:Del PJ33,Change GFXCORE-A to GFXCORE.

P81:Del PJ36,PJ12,NV_VDD_VGA,PEX_VDD_LDO.

P85:Change H14 from 1X-HOLE000-1407 to 1X-HOLE000-1357.
Change H12 from 1X-HOLE000-1400 to 1X-HOLE000-1486.
Add HOLE H19,H20.

2010/05/13

P85:Change H14 from 1X-HOLE000-1357 to 1X-HOLE000-1492.
Change H8 from 1X-HOLE000-1399 to 1X-HOLE000-1493.

P08:Del TP204,TP124.

P09:Del TP343,TP350,TP349,TP348,TP341,TP342,TP337,TP333,TP338,TP339,TP346,
TP336,TP332,TP331,TP335,TP334,TP344,TP340,TP345,TP347,TP261,TP304,TP303
TP310,TP308,TP307,TP258,TP305.

2010/05/14

P81:Change PR566 from 75K_F to 39K_F.

P76:Change PR156,PR151 from 10K_F to 2.2K_F.

P75:Change PR187 from 4.42K_F to 2.2K_F;
Change PR208 from 10K_F to 5.1K_F.

P22:Change Q5,R5689,R811 from stuff to NC.

P11:Change R111 from NC_ to stuff.

P44:Change R83 from NC to stuff.

P09:Del TP354,TP356,TP355,TP320,TP325,TP317,TP315,TP323,TP353,TP313,TP318.

2010/05/17

P64:Change P_R1,P_R2,P_R3 from 68_J to 330_J.

P59:Change R74 from 1R-0000183-F200 to 1R-0002212-F200 for thermal request.

2010/05/19

P80:Change PR615,PR617,PR619,PR623,PR625,PR621,PR627 from 10K_J to 1K_J;
Change PR616,PR618,PR620,PR624,PR626,PR622,PR628 from 0_J to 1K_J.

P39:Change F17 from 1M-F006A35-F000 to 1M-F6V0A35-F000(Halogen Free) for PUR.

P60:Change F12 from 1M-F10V0A1-F000 to 1M-F30VA12-F000(Halogen Free) for PUR.

P43:Change Q57 from 17-S12301B-DS00 to 17-S12301C-DS00 for PUR.

P58:Change Q79 from 17-S12301B-DS00 to 17-S12301C-DS00 for PUR.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: History		
Size: A2	Document Number: W930 H1&H2	Rev: SA
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