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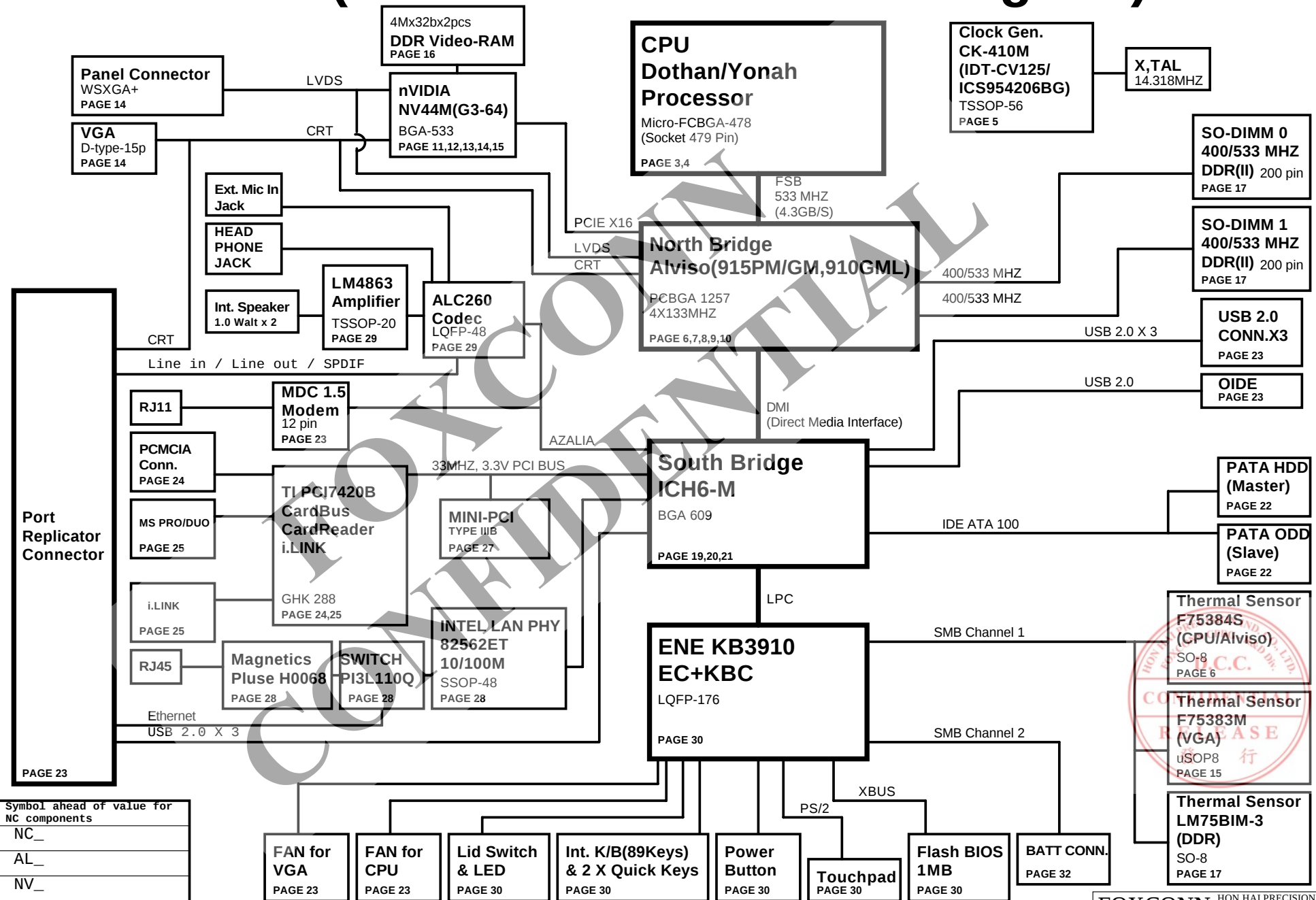


P. Leader	Appr. by	Check by	Design by
			Alex

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Title MS03 DVT_M/B			
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Project Code & Schematics Subject:	MS03 M/B-FUBAI	PCB P/N:	1P-0055100-80SB
Project Code & Schematics Subject:	MS03 M/B-HANNSTAR	PCB P/N:	1P-0055500-80SB
Project Code & Schematics Subject:	MS03 M/B-NAN YA	PCB P/N:	1P-0055200-80SB

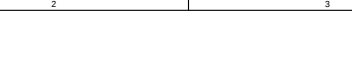
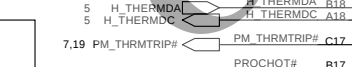
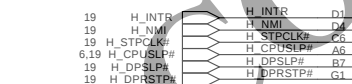
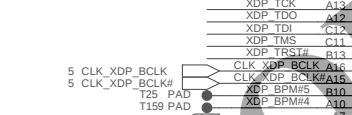
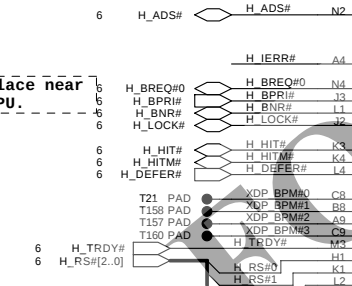
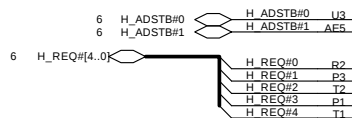
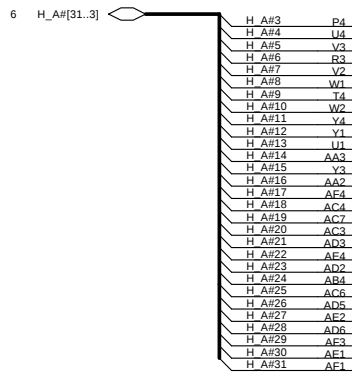
MS03(915PM/GM+Gfx Block Diagram)



BOM configuration

Dothan 1 OF 3

U30A



REQUEST
PHASE
SIGNALS

DATA
PHASE
SIGNALS

ERROR
SIGNALS

ARBITRATION
PHASE
SIGNALS

SNOOP PHASE
SIGNALS

RESPONSE
PHASE
SIGNALS

PC COMPATIBILITY
SIGNALS

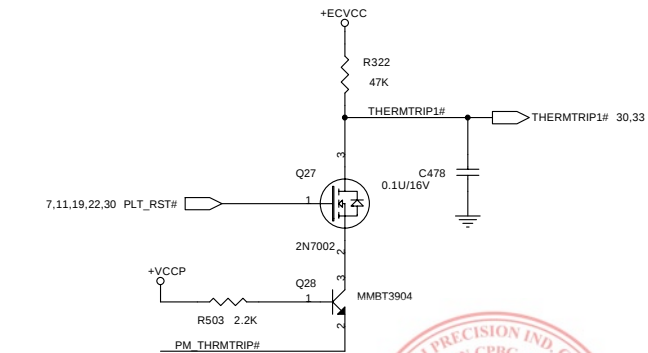
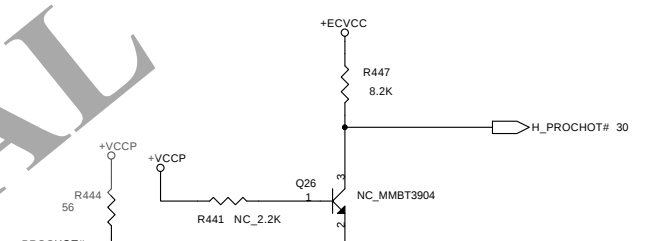
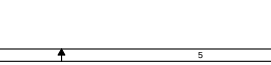
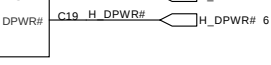
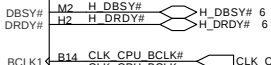
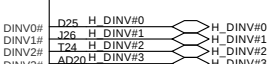
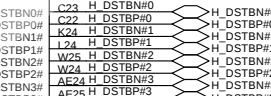
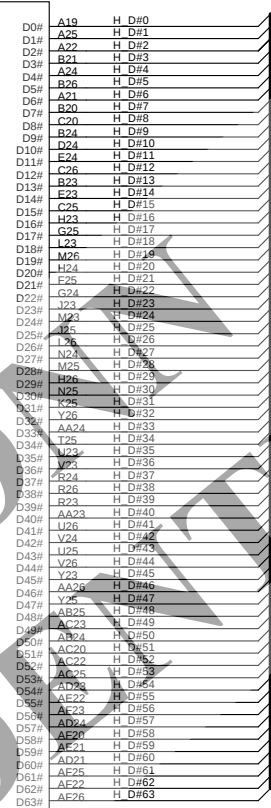
DIAGNOSTIC
& TEST
SIGNALS

EXECUTION
CONTROL
SIGNALS

THERMTRIP#

PROCHOT#

Dothan Processor



PM_THRMTRIP#
should connect to
ICH6-M and ALVISO
without T-ing (No
stub)



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FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Placed within
500mils of Y1

Length as short
as possible.

IDTCV125 / ICS954206BG
SM bus Address :
1101001 (ICH6)
For c/clock generator

SM bus Address :
1001101 (EC)
For F75384S

Place Thermal-Sensor
near CPU & GMCH.

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Alviso Chip
HOST

CPU

Alviso Chip

ICH6
DMI

Graphic
NV44M

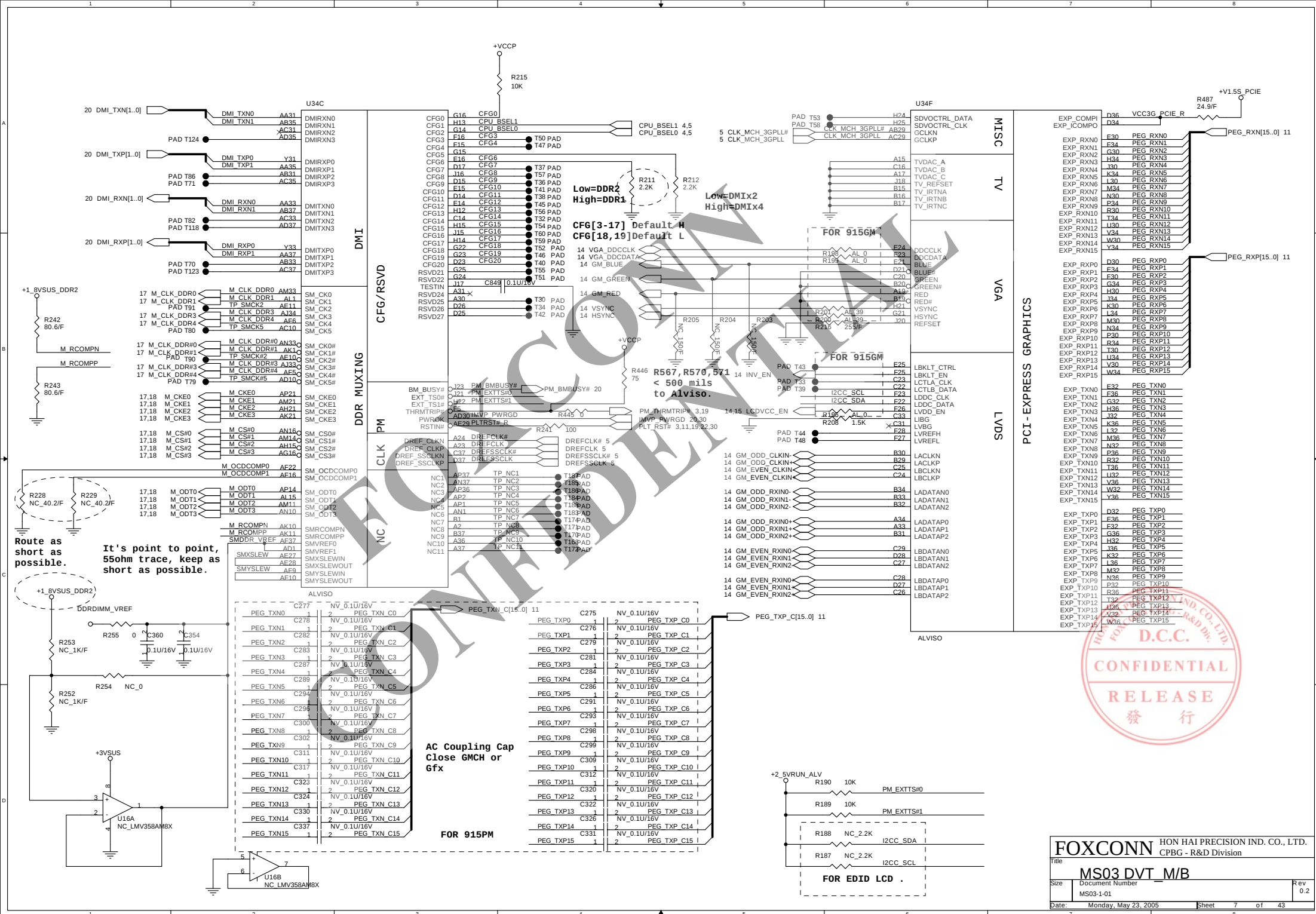
ALVISO SSCK

CLK_XDP_BCLK# R460 NC 49.9/F
CLK_XDP_BCLK# R458 NC 49.9/F
CLK_MCH_BCLK# R465 49.9/F
CLK_MCH_BCLK# R463 49.9/F
CLK_CPU_BCLK# R471 49.9/F
CLK_CPU_BCLK# R469 49.9/F
CLK_MCH_3GPLL R457 49.9/F
CLK_MCH_3GPLL# R455 49.9/F

CLK_PCIE_ICH# R459 49.9/F
CLK_PCIE_ICH# R456 49.9/F

CLK_PCIE_PEG# R462 NV 49.9/F
CLK_PCIE_PEG# R461 NV 49.9/F
DREFCLK# R470 AL 49.9/F
DREFSSCLK# R466 NV 0
DREFSSCLK# R185 AL 49.9/F
DREFSSCLK# R183 NV 0
DREFCLK# R631 AL 49.9/F
DREFSSCLK# R632 AL 49.9/F

For NV44M & Alviso option
R_CLK_KBCPCI R626 NC 10K
R_PCLK_MINI R627 NC 10K



17 M_A_DQ[63..0]

M A DQ0 AG35
M A DQ1 AH35
M A DQ2 AL35
M A DQ3 AL37
M A DQ4 AH36
M A DQ5 AJ35
M A DQ6 AK37
M A DQ7 AL34
M A DQ8 AM36
M A DQ9 AN35
M A DQ10 AP32
M A DQ11 AM31
M A DQ12 AL34
M A DQ13 AM35
M A DQ14 AL32
M A DQ15 AM32
M A DQ16 AN31
M A DQ17 AP31
M A DQ18 AN28
M A DQ19 AP28
M A DQ20 AL30
M A DQ21 AM31
M A DQ22 AM28
M A DQ23 AL28
M A DQ24 AP27
M A DQ25 AM27
M A DQ26 AM23
M A DQ27 AM22
M A DQ28 AL23
M A DQ29 AM24
M A DQ30 AM22
M A DQ31 AP22
M A DQ32 AM9
M A DQ33 AL9
M A DQ34 AL6
M A DQ35 AP7
M A DQ36 AP11
M A DQ37 AP10
M A DQ38 AL7
M A DQ39 AM7
M A DQ40 AN5
M A DQ41 AN6
M A DQ42 AN3
M A DQ43 AP3
M A DQ44 AP6
M A DQ45 AM6
M A DQ46 AL4
M A DQ47 AM3
M A DQ48 AK2
M A DQ49 AK3
M A DQ50 AG2
M A DQ51 AG1
M A DQ52 AL3
M A DQ53 AM2
M A DQ54 AH3
M A DQ55 AG3
M A DQ56 AE3
M A DQ57 AE8
M A DQ58 AD6
M A DQ59 AC4
M A DQ60 AF2
M A DQ61 AE1
M A DQ62 AD4
M A DQ63 AD5

U34B

DDR SYSTEM MEMORY A

SA_BS0# AK15 M A BS#0
SA_BS1# AK16 M A BS#1
SA_BS2# AL21
SA_DM0 AJ37 M A DM0
SA_DM1 AP35 M A DM1
SA_DM2 AL29 M A DM2
SA_DM3 AP24 M A DM3
SA_DM4 AP9 M A DM4
SA_DM5 AP4 M A DM5
SA_DM6 AJ2 M A DM6
SA_DM7 AD3 M A DM7
SA_DQS0 AK36 M A DQS0
SA_DQS1 AP33 M A DQS1
SA_DQS2 AN29 M A DQS2
SA_DQS3 AP23 M A DQS3
SA_DQS4 AM9 M A DQS4
SA_DQS5 AM4 M A DQS5
SA_DQS6 AJ1 M A DQS6
SA_DQS7 AE5 M A DQS7
SA_DQS0# AK35 M A DQS#0
SA_DQS1# AP34 M A DQS#1
SA_DQS2# AN30 M A DQS#2
SA_DQS3# AN23 M A DQS#3
SA_DQS4# AN8 M A DQS#4
SA_DQS5# AM5 M A DQS#5
SA_DQS6# AH1 M A DQS#6
SA_DQS7# AE4 M A DQS#7
SA_MA0 AL17 M A A0
SA_MA1 AP17 M A A1
SA_MA2 AP18 M A A2
SA_MA3 AM17 M A A3
SA_MA4 AN18 M A A4
SA_MA5 AM18 M A A5
SA_MA6 AL19 M A A6
SA_MA7 AP20 M A A7
SA_MA8 AM19 M A A8
SA_MA9 AL20 M A A9
SA_MA10 AM16 M A A10
SA_MA11 AN20 M A A11
SA_MA12 AM20 M A A12
SA_MA13 AM15 M A A13
SA_CAS# AN15 M A CAS#
SA_RAS# AP16 M A RAS#
SA_RCVENIN# AE29
SA_RCVENOUT# AE28
SA_WE# AP15 M A WE#

M A BS#0 17,18
M A BS#1 17,18
M A BS#2-17,18
M A BS#7-0 17

M_A_DQS[7..0] 17

M_A_DQS#7[7..0] 17

M_A_A[13..0] 17,18

M_A_CAS# 17,18

M_A_RAS# 17,18

PAD

M_A_WE# 17,18

17 M_B_DQ[63..0]

M B DQ0 AE31
M B DQ1 AE32
M B DQ2 AG32
M B DQ3 AG36
M B DQ4 AE34
M B DQ5 AE33
M B DQ6 AE31
M B DQ7 AE30
M B DQ8 AH33
M B DQ9 AH32
M B DQ10 AK31
M B DQ11 AG30
M B DQ12 AG34
M B DQ13 AG33
M B DQ14 AH31
M B DQ15 AJ31
M B DQ16 AK30
M B DQ17 AJ30
M B DQ18 AH29
M B DQ19 AH28
M B DQ20 AK29
M B DQ21 AH27
M B DQ22 AG28
M B DQ23 AG28
M B DQ24 AE24
M B DQ25 AG23
M B DQ26 AJ22
M B DQ27 AK22
M B DQ28 AH24
M B DQ29 AH23
M B DQ30 AG22
M B DQ31 AJ21
M B DQ32 AG10
M B DQ33 AG9
M B DQ34 AG8
M B DQ35 AH8
M B DQ36 AH11
M B DQ37 AH10
M B DQ38 AJ9
M B DQ39 AK9
M B DQ40 AJ7
M B DQ41 AK6
M B DQ42 AJ4
M B DQ43 AH5
M B DQ44 AK8
M B DQ45 AJ8
M B DQ46 AJ5
M B DQ47 AK4
M B DQ48 AC5
M B DQ49 AG4
M B DQ50 AD8
M B DQ51 AD9
M B DQ52 AH4
M B DQ53 AG6
M B DQ54 AE8
M B DQ55 AD7
M B DQ56 AC5
M B DQ57 AE8
M B DQ58 AE6
M B DQ59 AA8
M B DQ60 ACR
M B DQ61 AC7
M B DQ62 AA4
M B DQ63 AA5

U34G

DDR SYSTEM MEMORY B

SB_BS0# AJ15 M B BS#0
SB_BS1# AG17 M B BS#1
SB_BS2# AG21
SB_DM0 AF32 M B DM0
SB_DM1 AK34 M B DM1
SB_DM2 AK27 M B DM2
SB_DM3 AJ10 M B DM3
SB_DM4 AK5 M B DM5
SB_DM5 AE7 M B DM6
SB_DM6 AB7 M B DM7
SB_DM7
SB_DQS0 AF34 M B DQS0
SB_DQS1 AK32 M B DQS1
SB_DQS2 AJ28 M B DQS2
SB_DQS3 AK23 M B DQS3
SB_DQS4 AM10 M B DQS4
SB_DQS5 AH6 M B DQS5
SB_DQS6 AF8 M B DQS6
SB_DQS7 AB4 M B DQS7
SB_DQS0# AF35 M B DQS#0
SB_DQS1# AK33 M B DQS#1
SB_DQS2# AK28 M B DQS#2
SB_DQS3# AJ23 M B DQS#3
SB_DQS4# AJ10 M B DQS#4
SB_DQS5# AH7 M B DQS#5
SB_DQS6# AE7 M B DQS#6
SB_DQS7# AB5 M B DQS#7
SB_MA0 AH17 M B A0
SB_MA1 AK17 M B A1
SB_MA2 AH18 M B A2
SB_MA3 AJ18 M B A3
SB_MA4 AK18 M B A4
SB_MA5 AJ19 M B A5
SB_MA6 AK19 M B A6
SB_MA7 AH19 M B A7
SB_MA8 AJ20 M B A8
SB_MA9 AH20 M B A9
SB_MA10 AJ16 M B A10
SB_MA11 AG18 M B A11
SB_MA12 AG20 M B A12
SB_MA13 AG15 M B A13
SB_CAS# AH14 M B CAS#
SB_RAS# AK14 M B RAS#
SB_RCVENIN# AE15
SB_RCVENOUT# AE14
SB_WE# AH16 M B WE#

M B BS#0 17,18
M B BS#1 17,18
M B BS#2-17,18
M B BS#7-0 17

M_B_DQS[7..0] 17

M_B_DQS#7[7..0] 17

M_B_A[13..0] 17,18

M_B_CAS# 17,18

M_B_RAS# 17,18

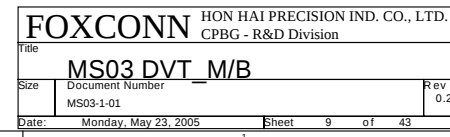
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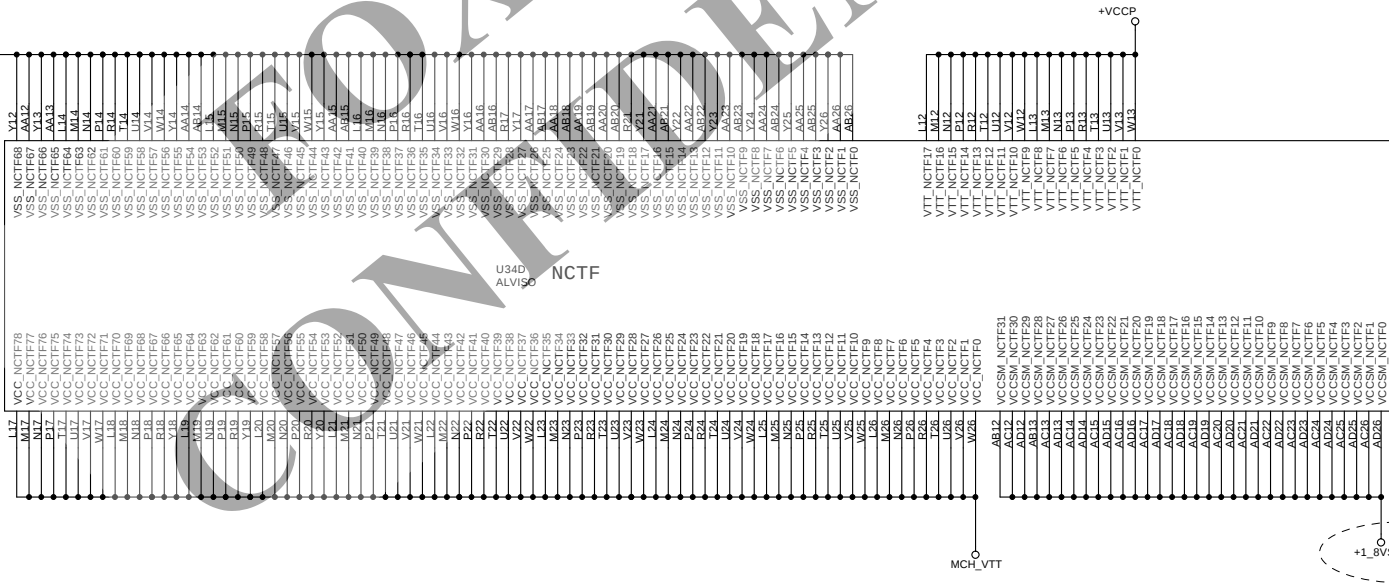
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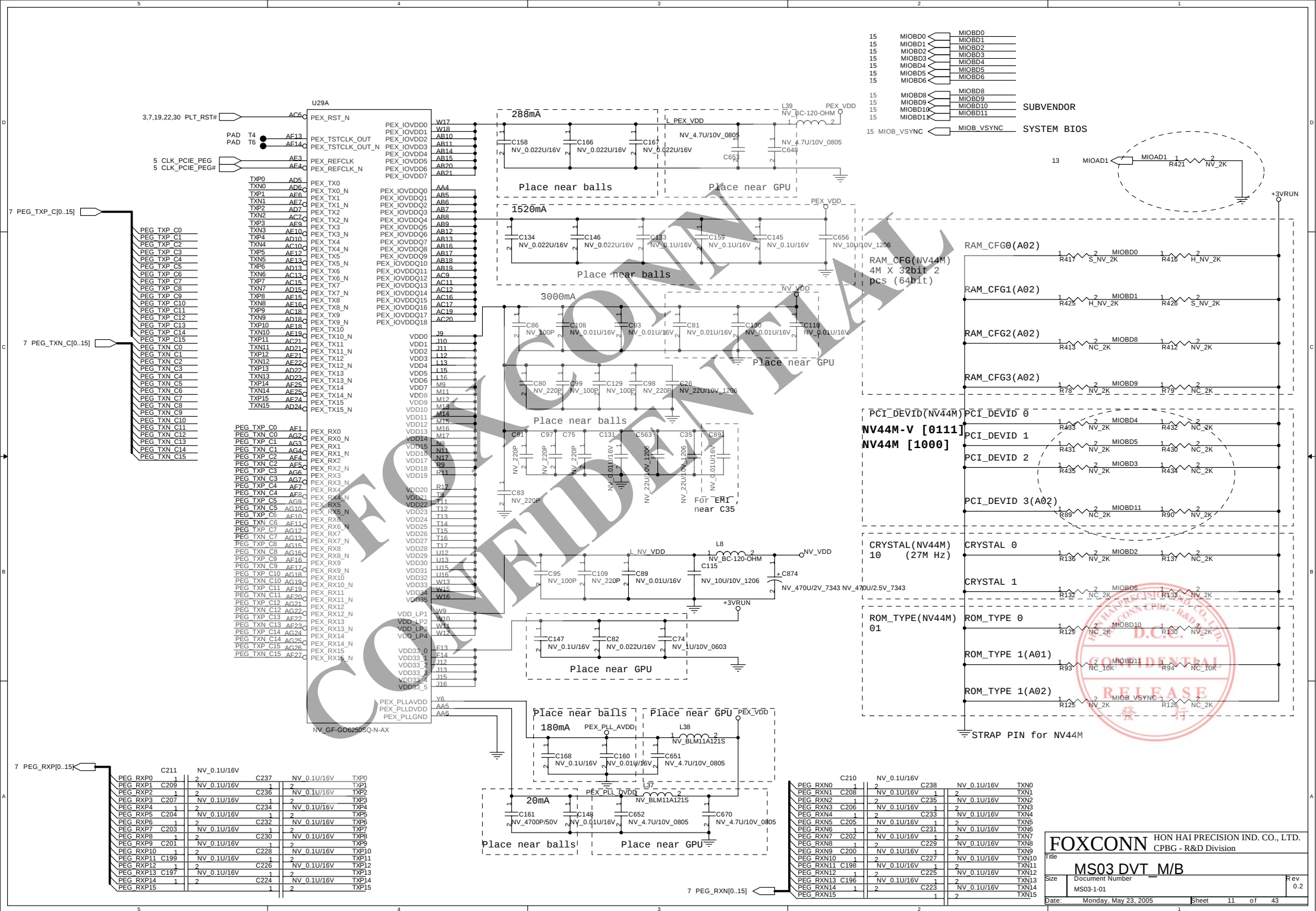


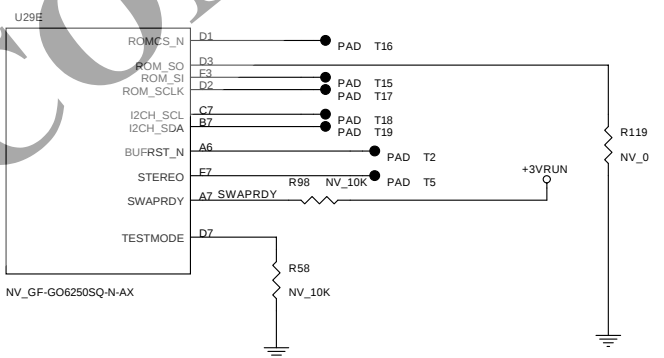
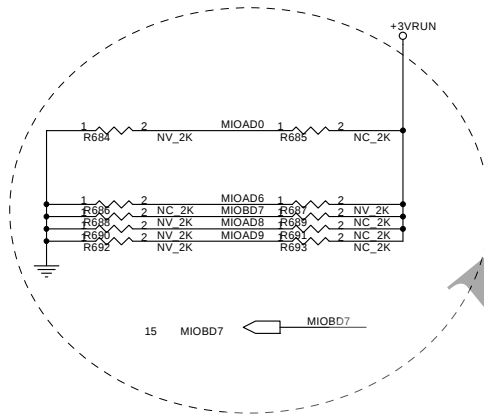
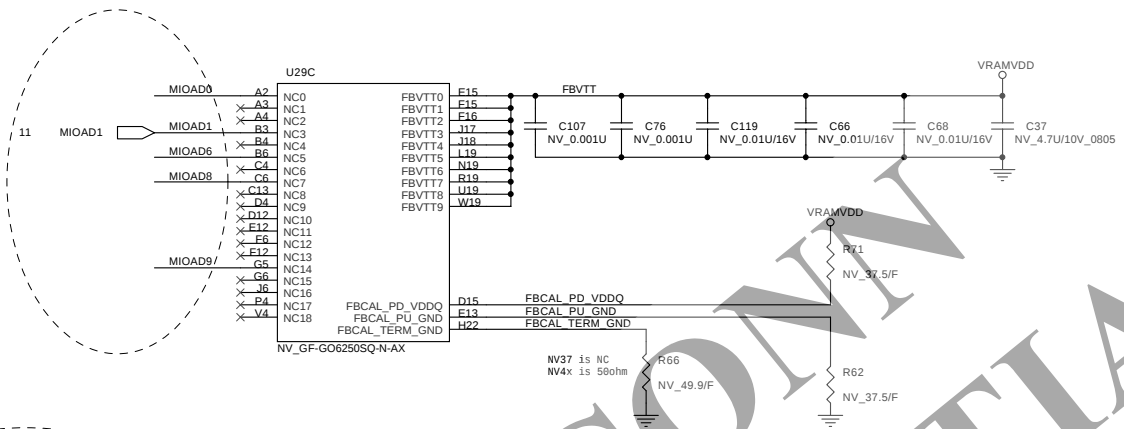


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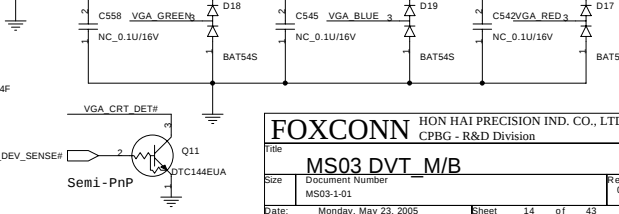
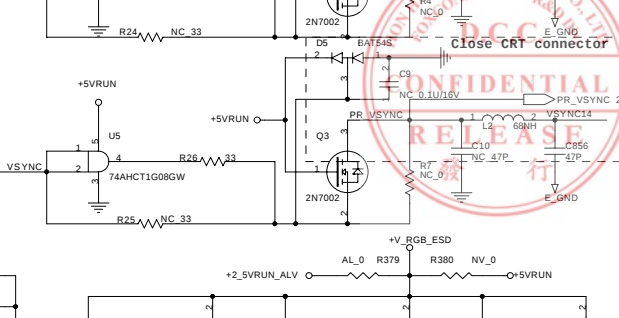
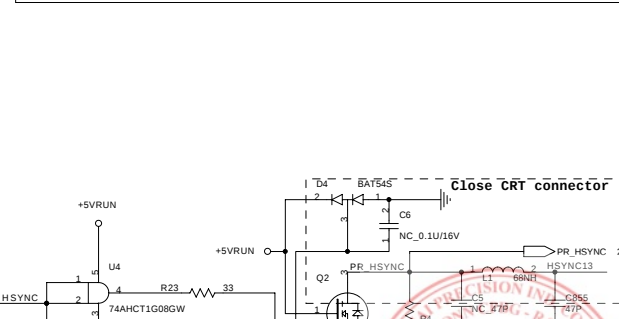
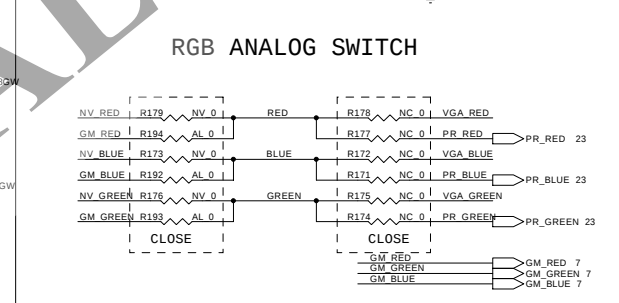
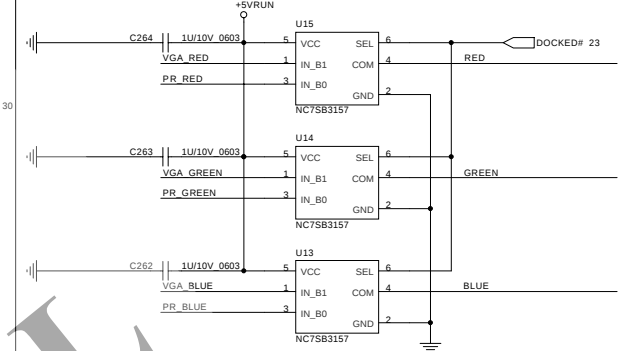
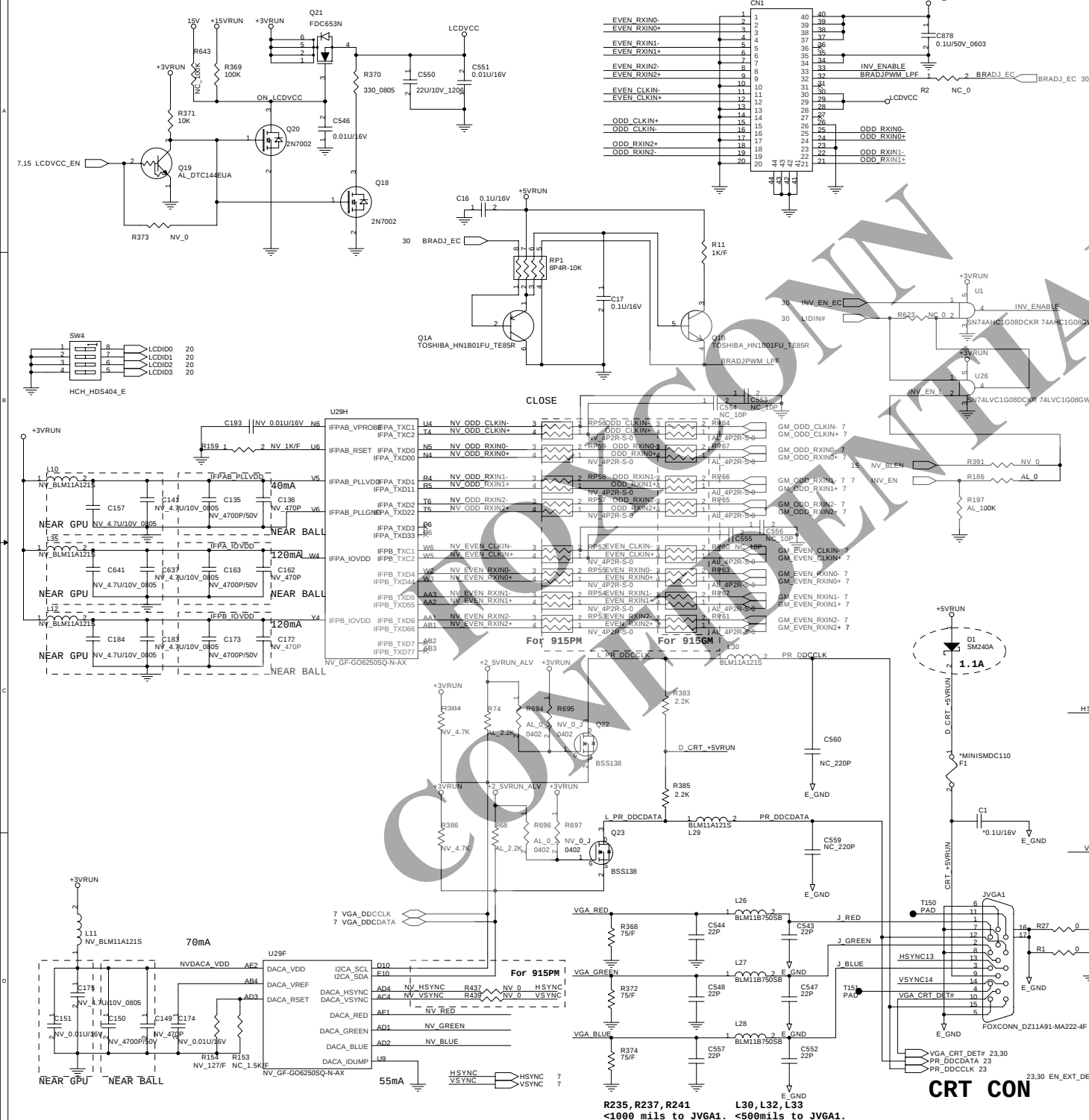




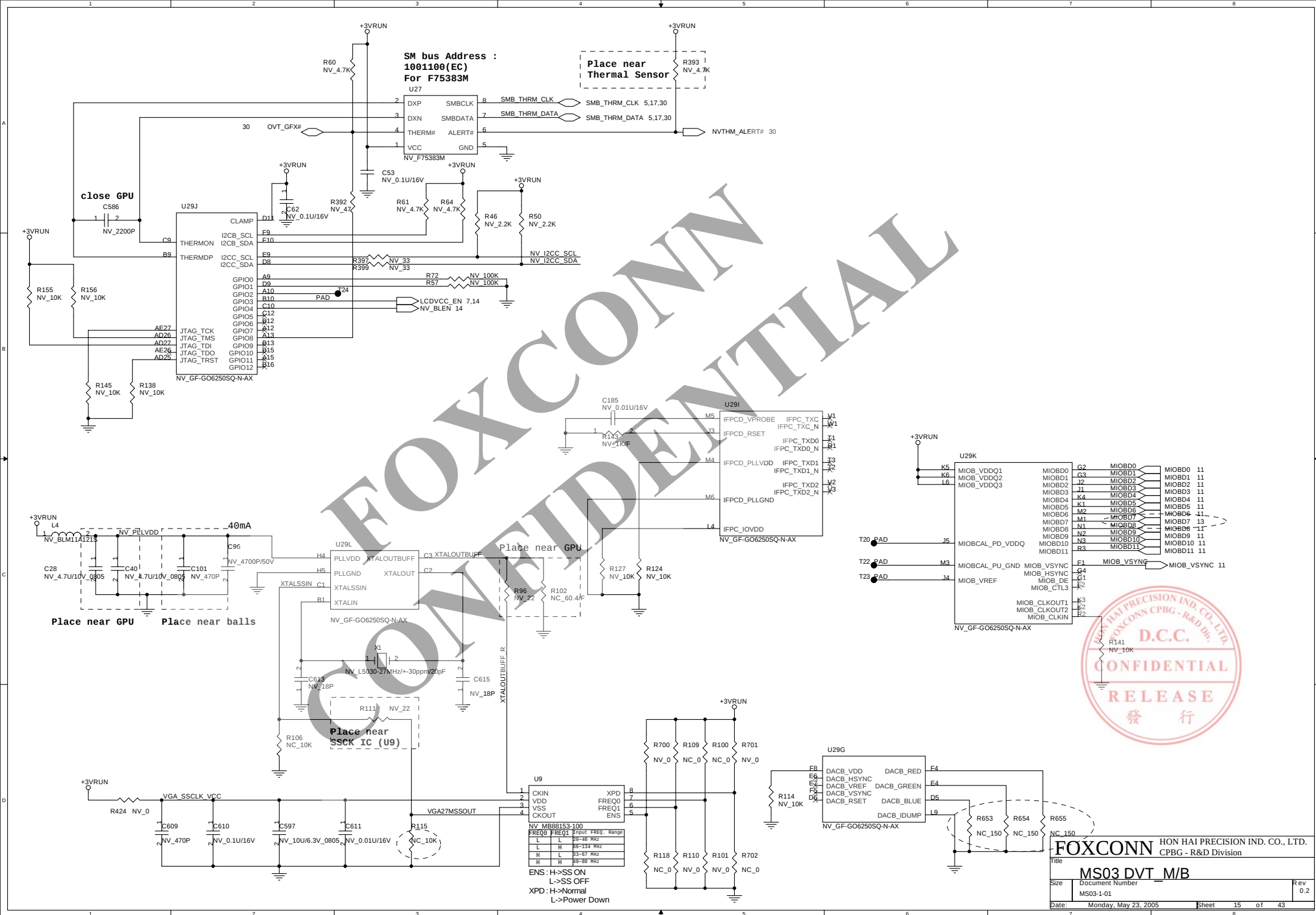
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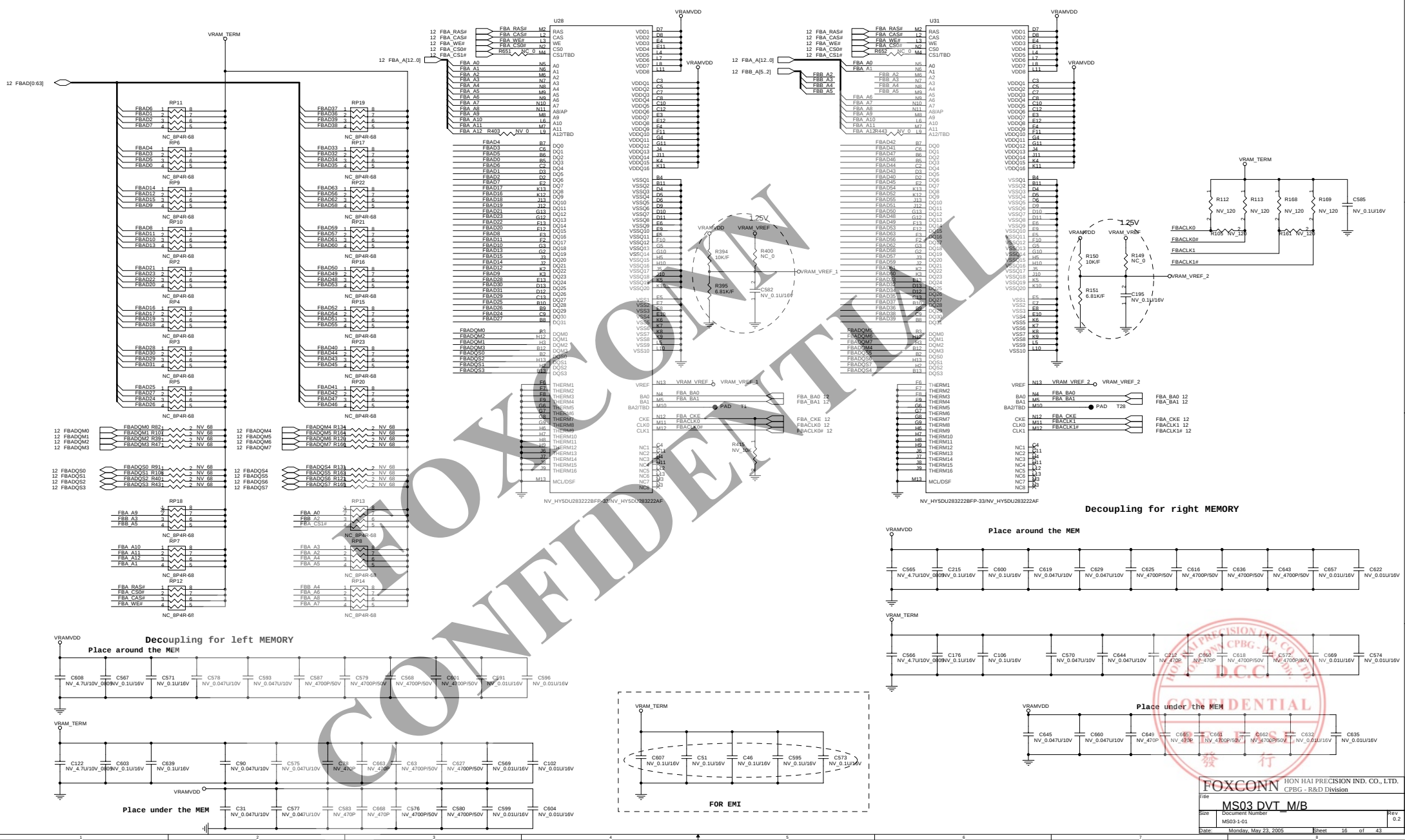
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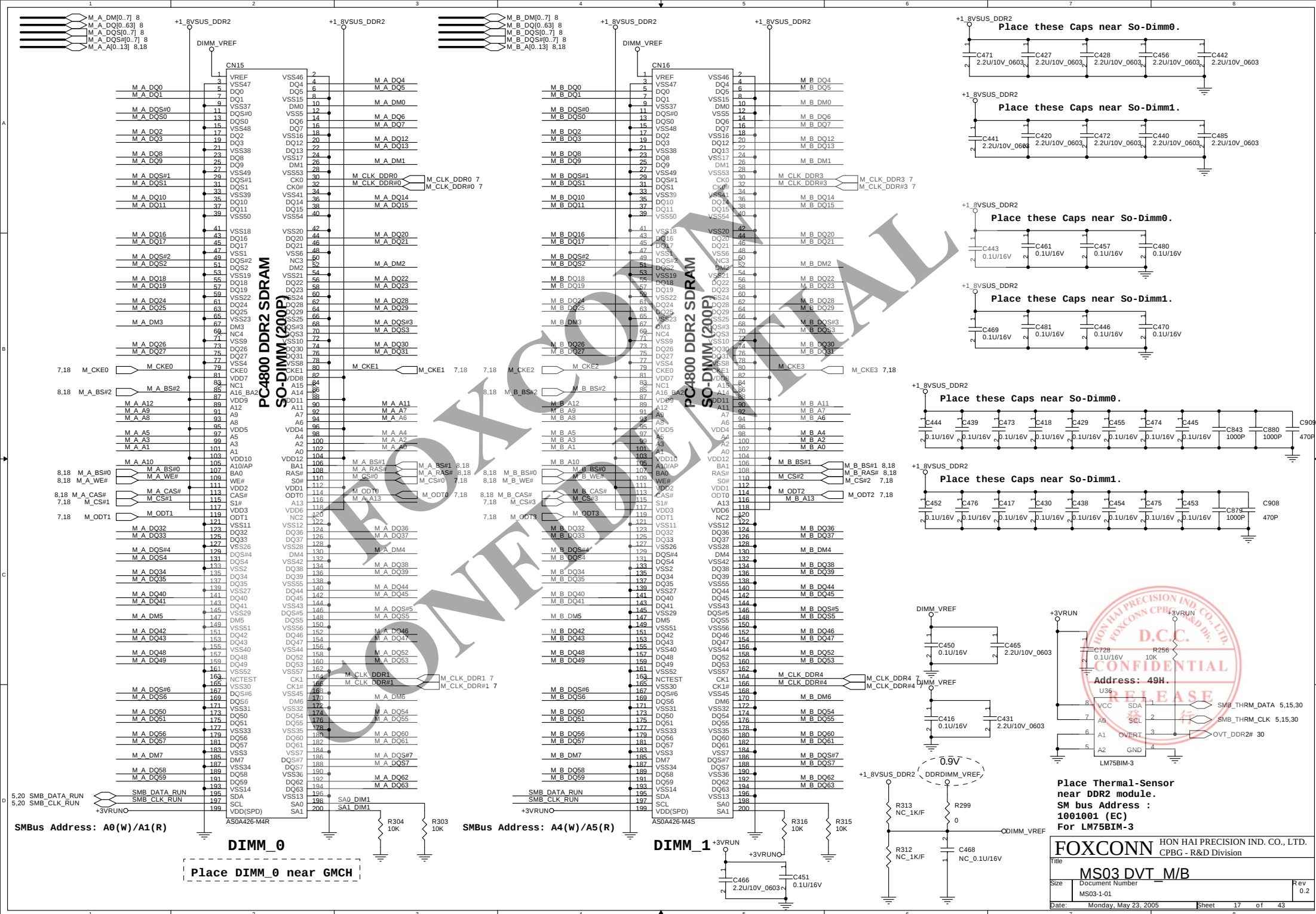
H : NOTEBOOK
L : PORT REPLICATOR

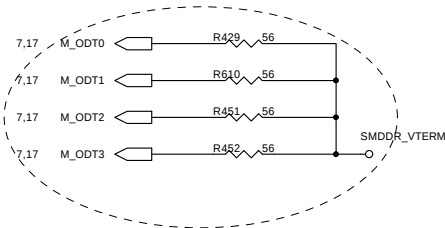
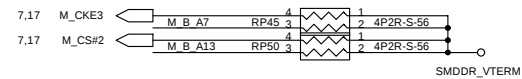
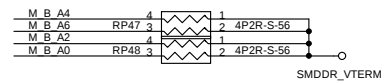
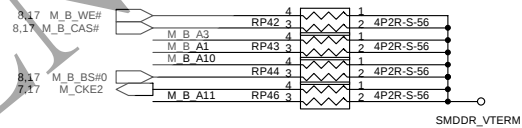
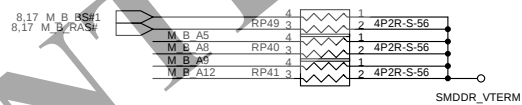
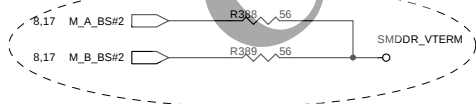
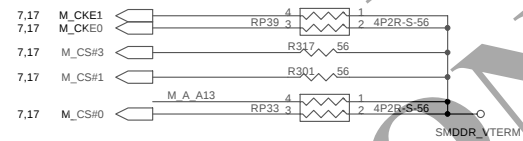
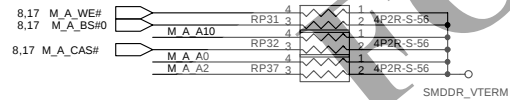
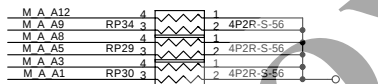
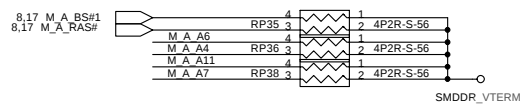
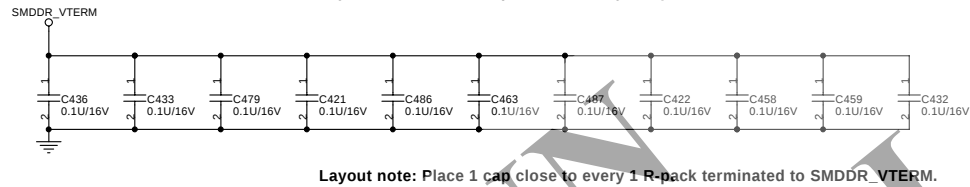
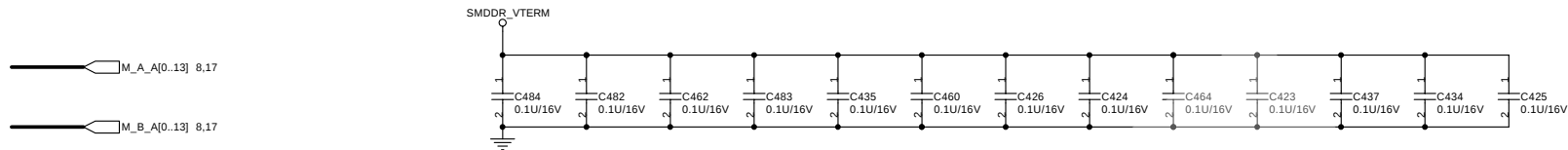


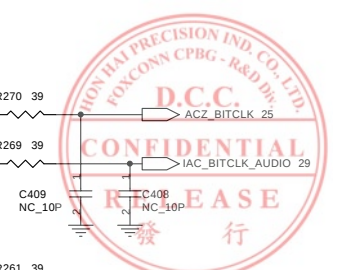
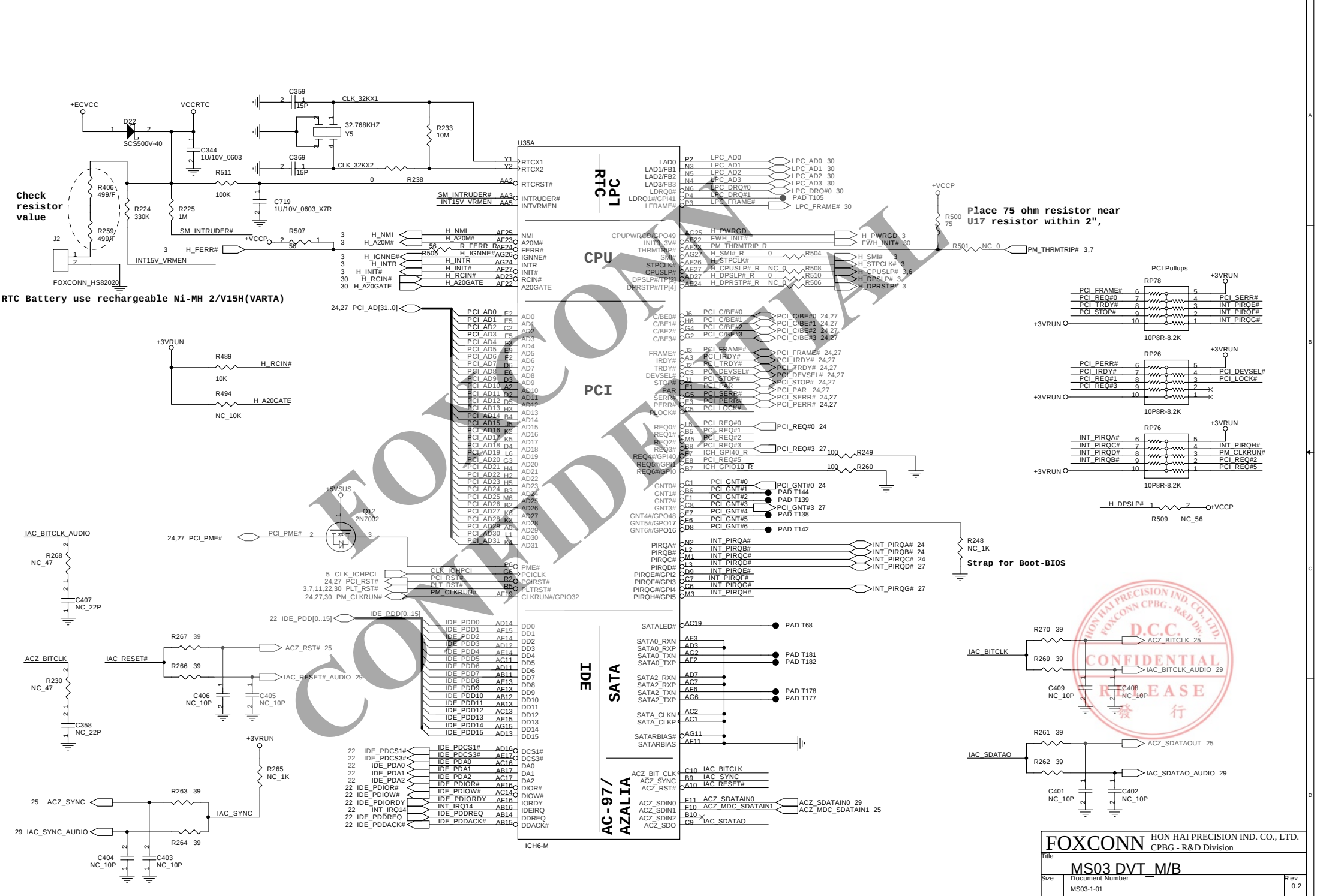
R235, R237, R241 L30, L32, L33
1000 mils to JVG1. 500mils to JVG1.

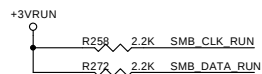






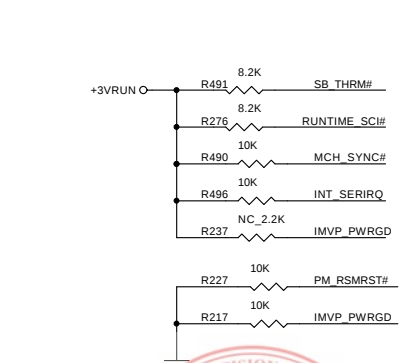
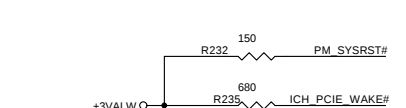
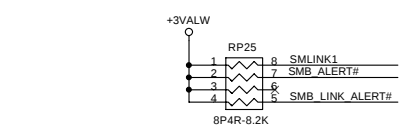
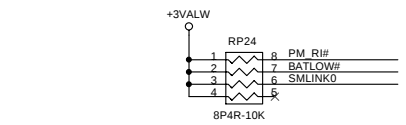
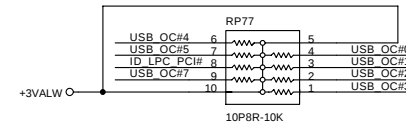
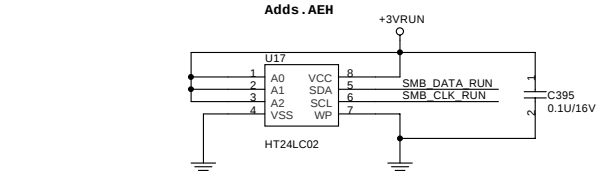
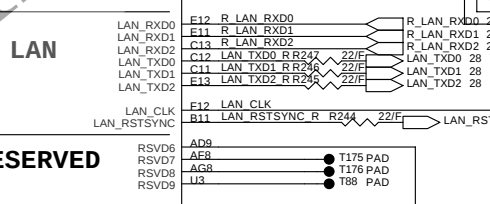
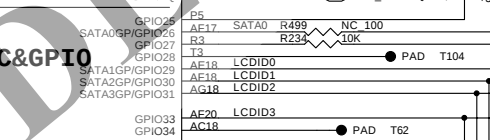
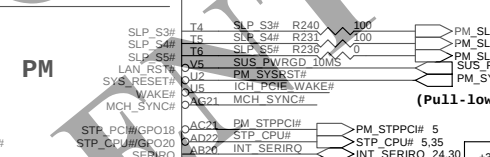
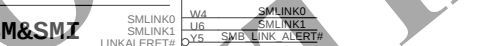
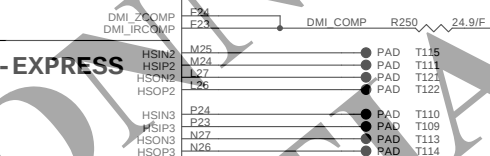
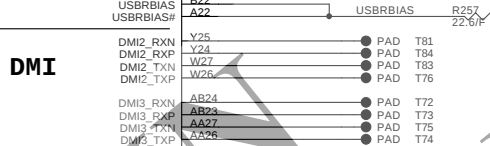
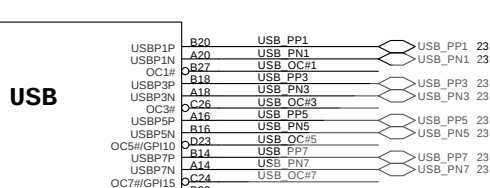
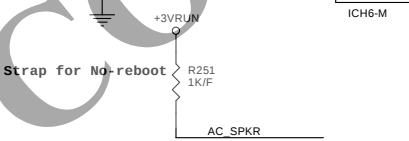
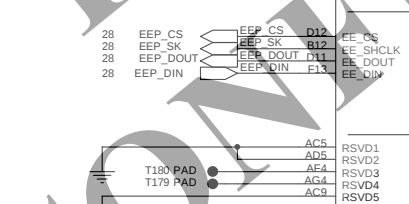
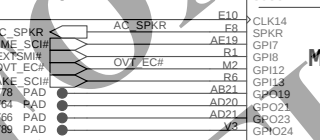
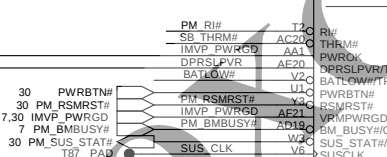
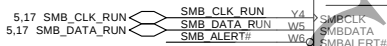
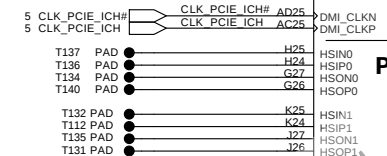
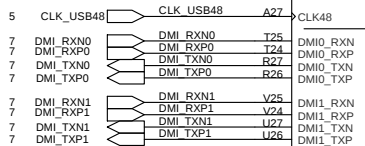
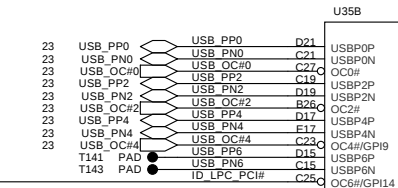
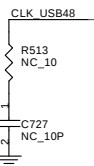
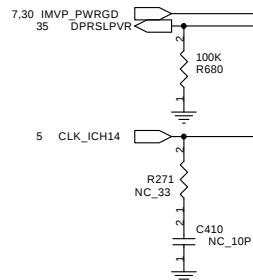


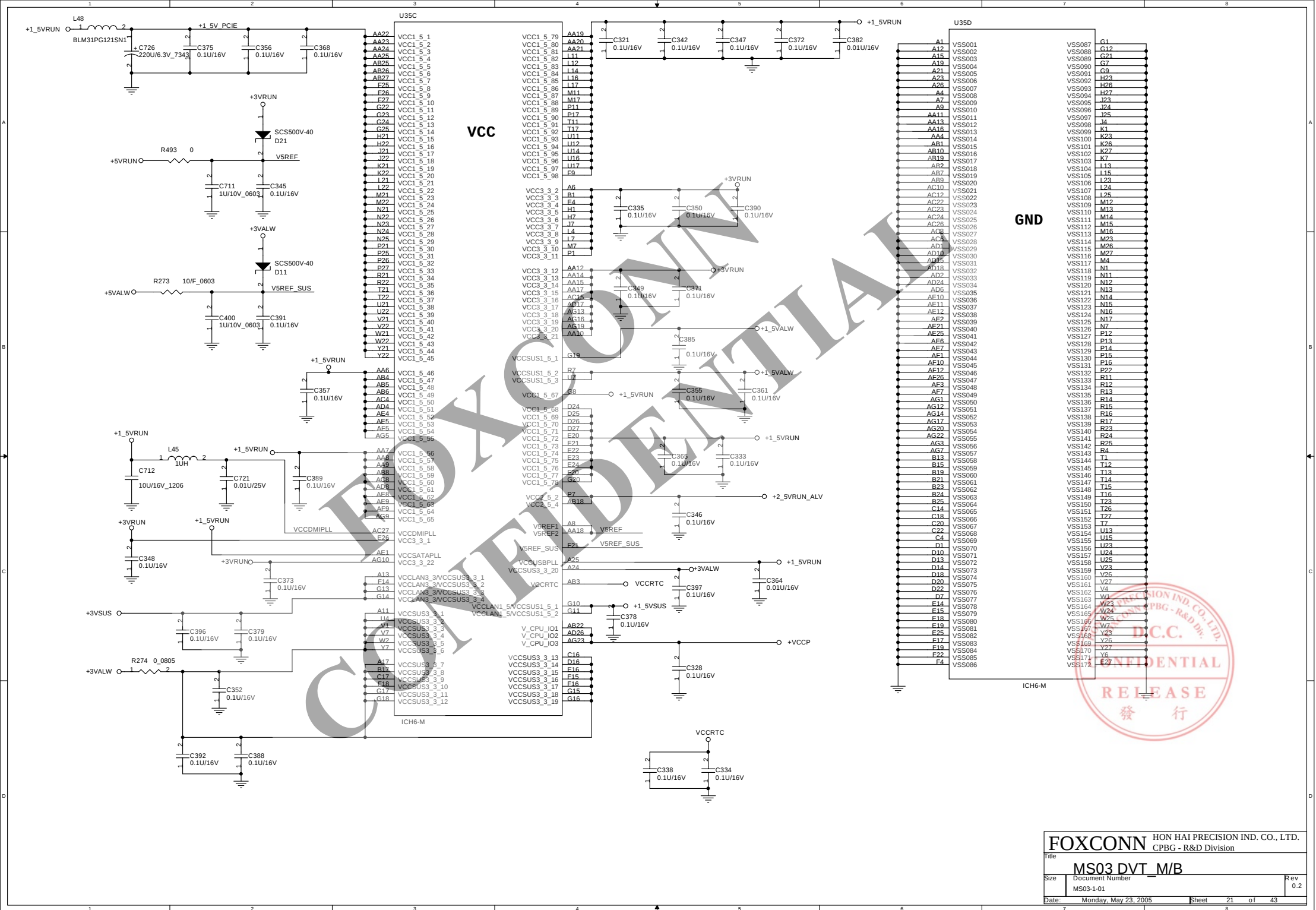


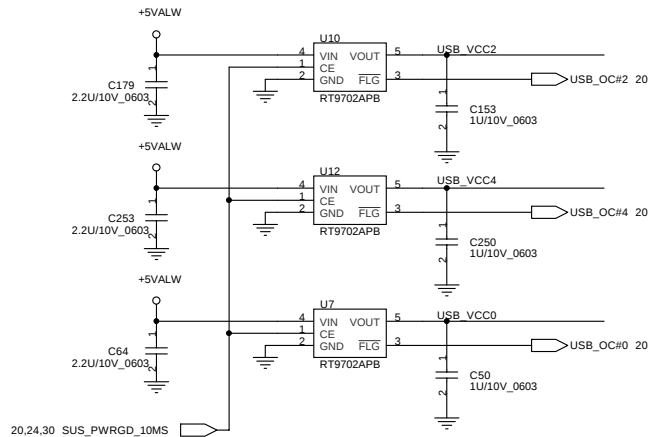


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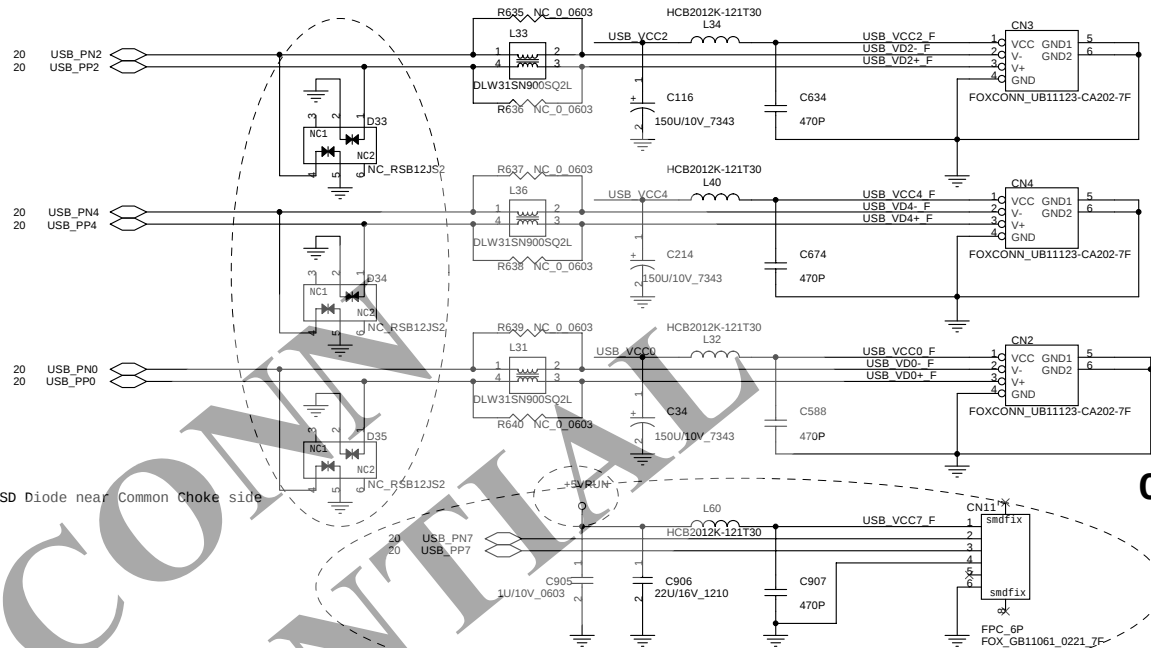
80 Port I/F:
H: LCP bus
L: PCI bus





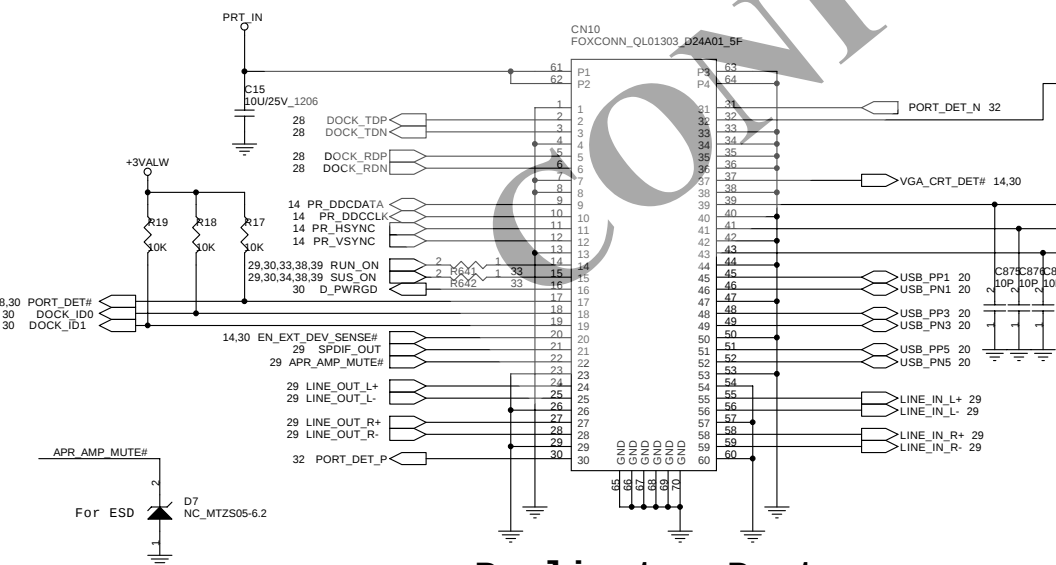
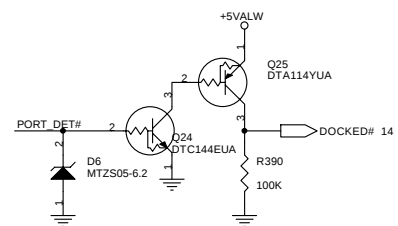


Place ESD Diode near Common Choke side

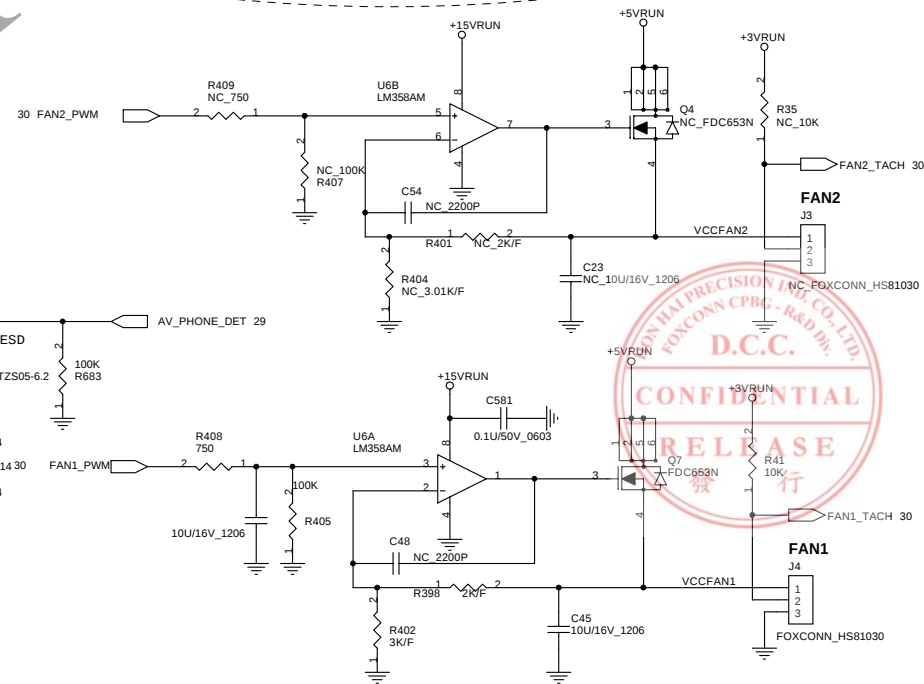


USB2.0 X 3

OIDE

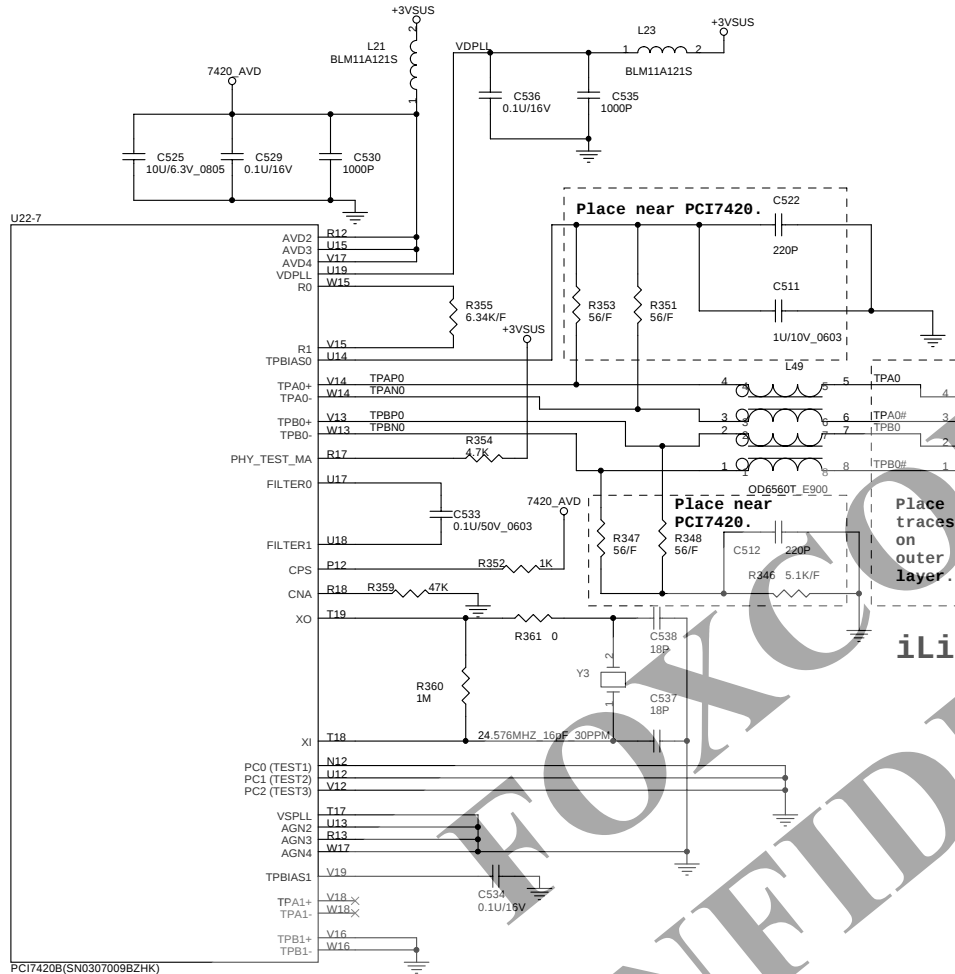


Replicator Port



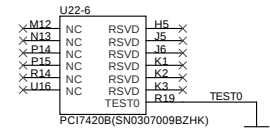
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CPBG - R&D Division	
Title MS03 DVT_M/B	
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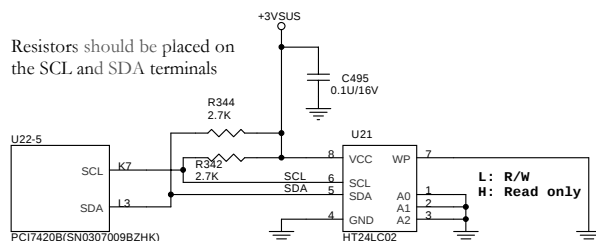


PCI7420B(SN0307009BZHK)

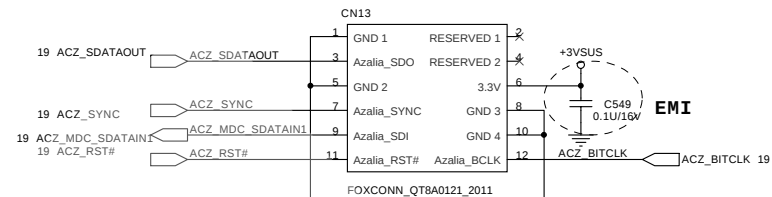
PCI7420 UNUSED TERMINALS



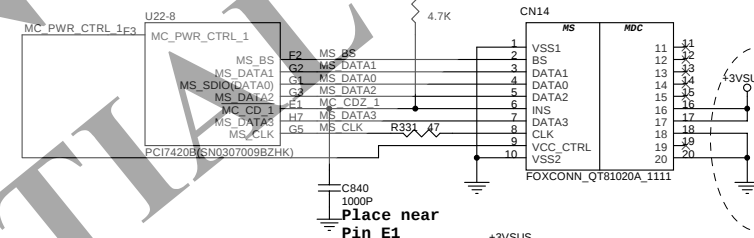
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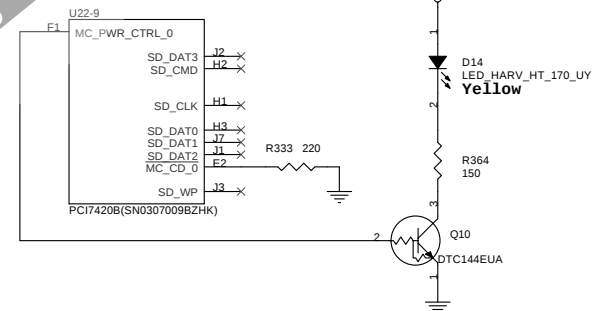
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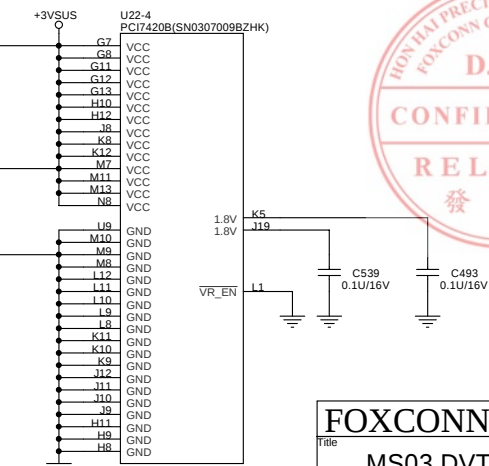
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iLink CONN.

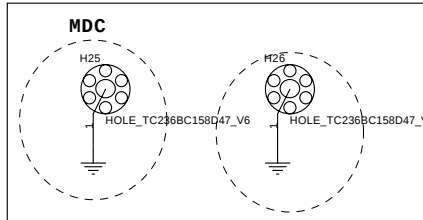
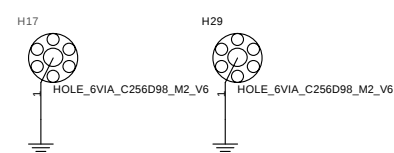
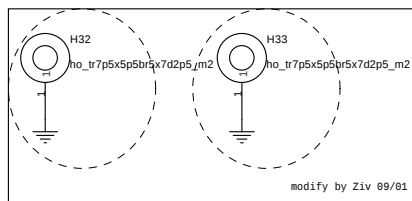
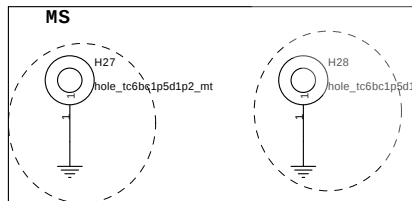
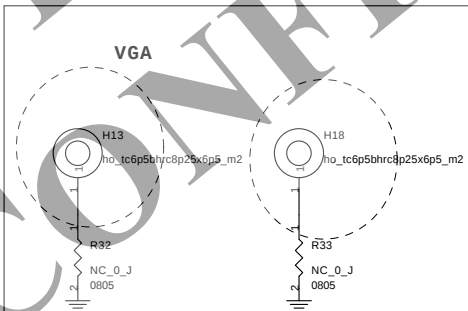
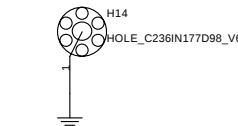
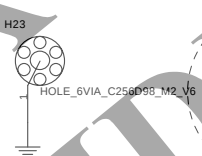
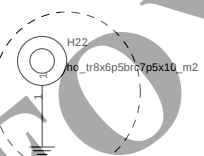
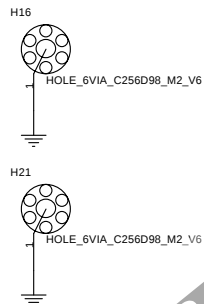
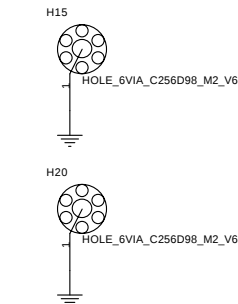
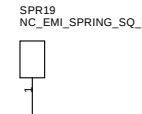
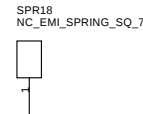
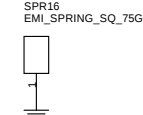
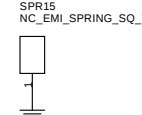
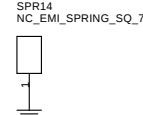
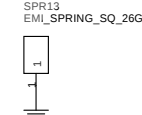
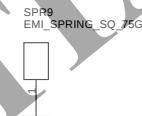
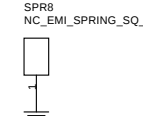
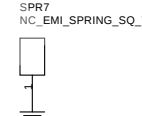
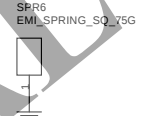
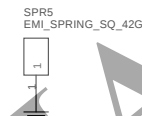
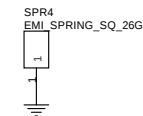
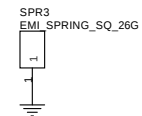
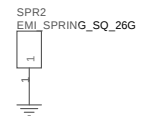
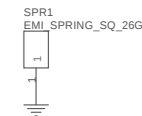
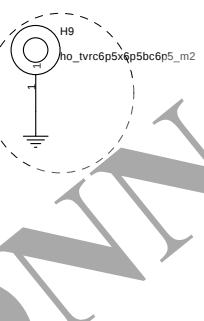
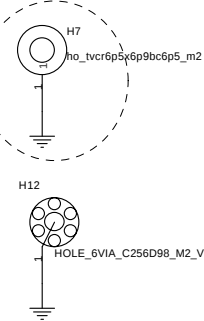
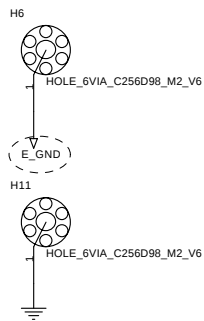
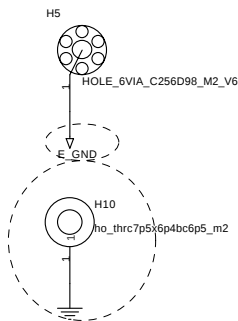
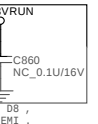
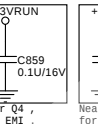
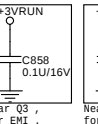
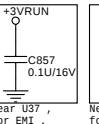
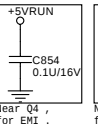
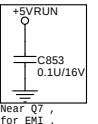
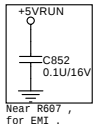
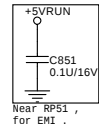
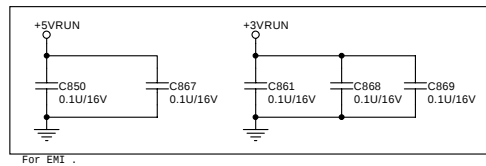


PCI7420 Power Terminals



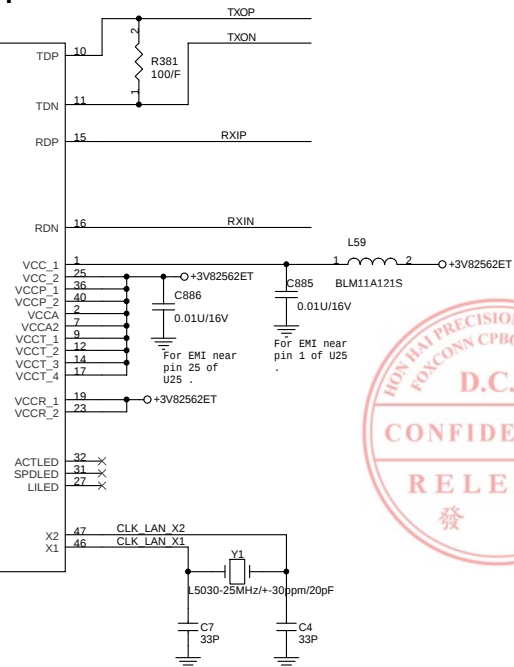
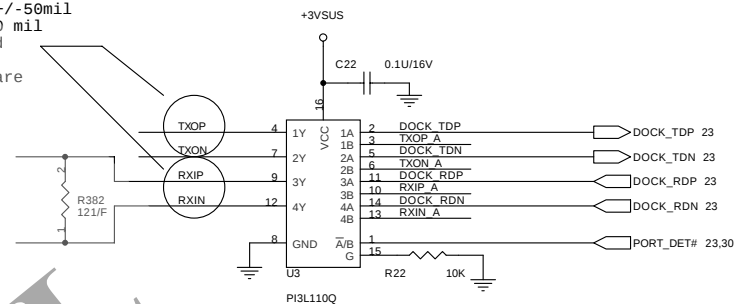
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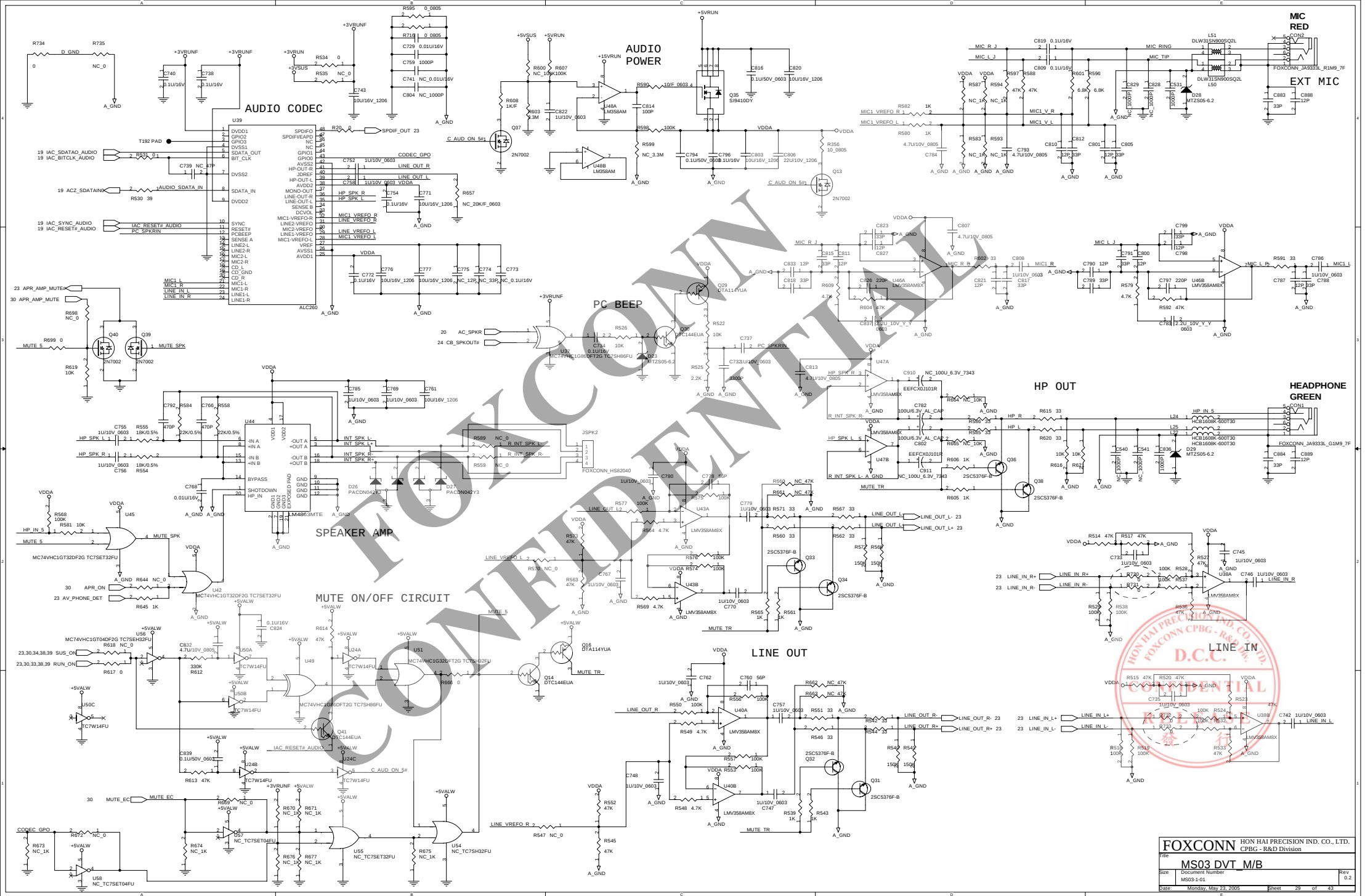
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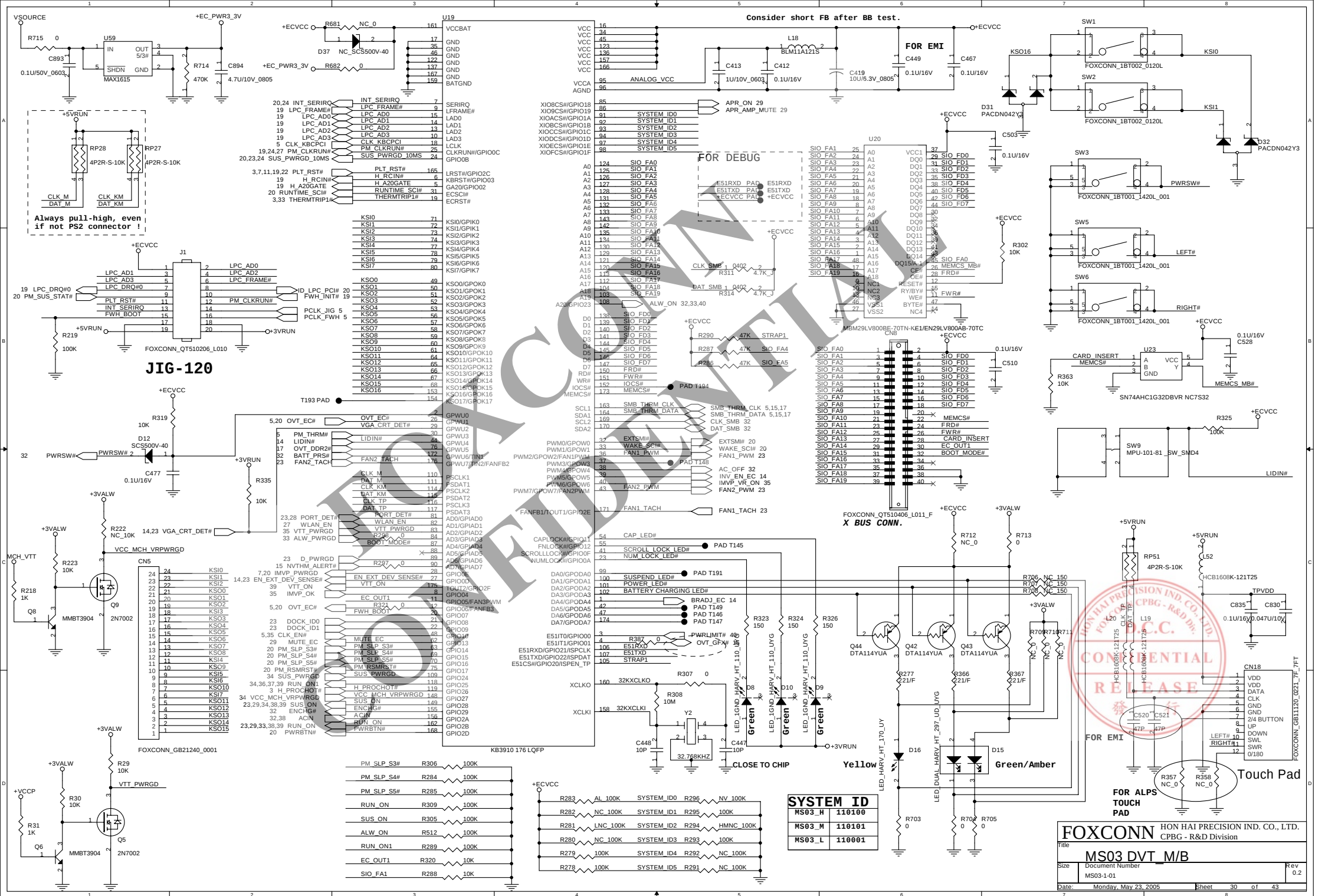


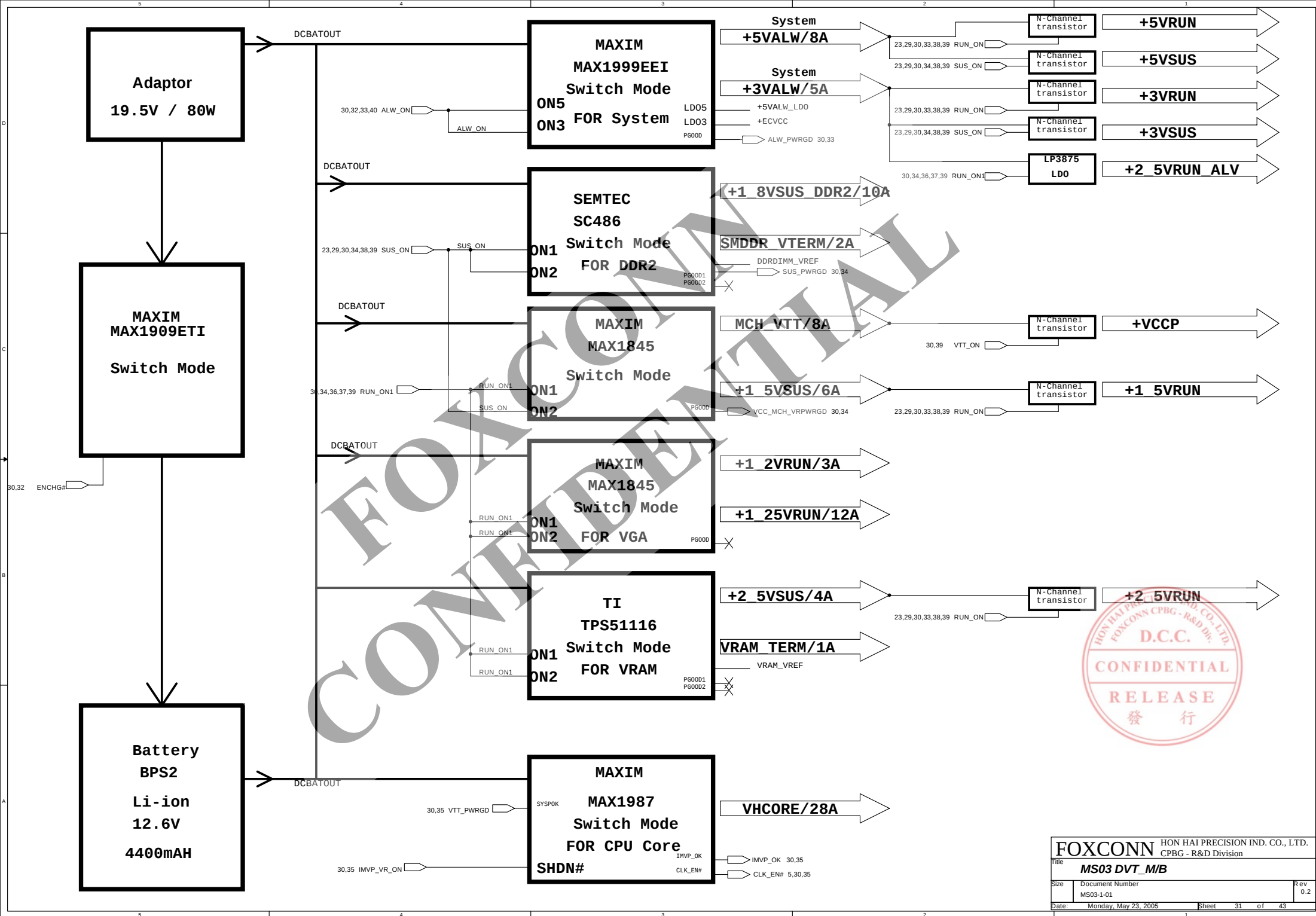
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LAYOUT NOTES:
Match total length of chip side Rx and Tx pair traces +/-50mil
Match length of cable side Rx and Tx pair traces +/- 50 mil
Total line TX+ to TX- and RX- and RX+ should be matched within 50 mils.
Keep 50mil space between pairs and other traces.Pairs are 100ohm differential,









DC_IN from port replicator

AC_IN Threshold 2.089V Max.
AC_IN > 2.089V -> AC DETECT

BT+ 4
DAT SMB 1
CLK SMB 1
BATT_PRS 1
SYS_PRS 1

SM bus Address :
0001011 (EC)
For Smart Battery .

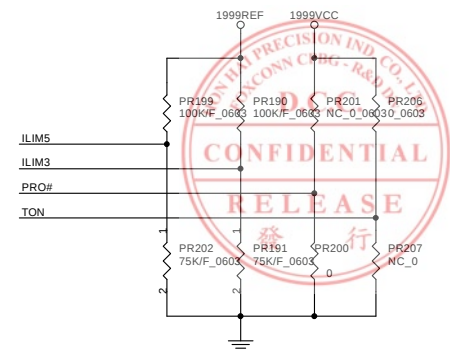
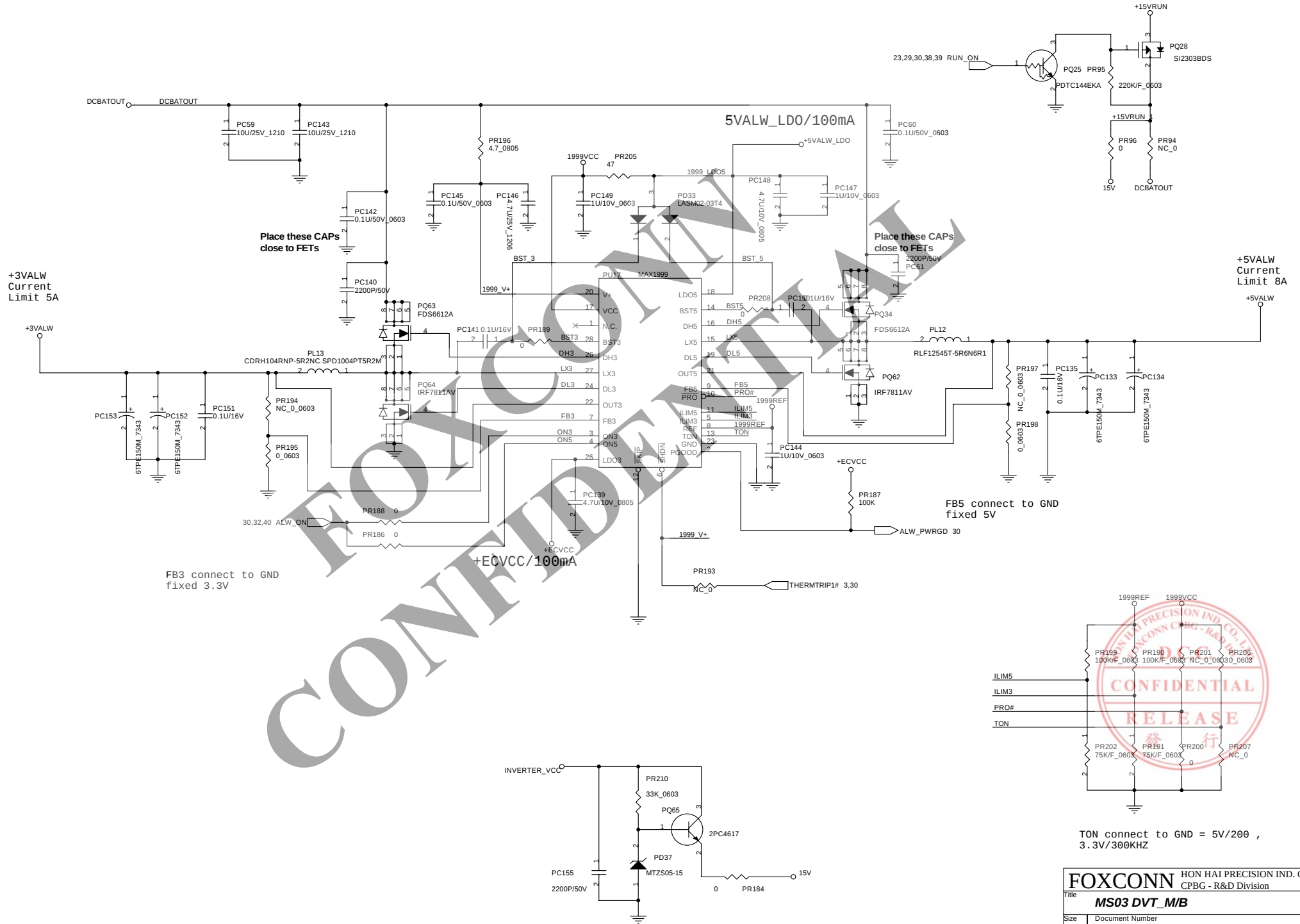
When Battery only and not power off, disconnect KBC power

When battery in BATT_PRES# pull low

V_REF : 4.2235V (<500uA)
ISOURCE_MAX Current = 4A
So, Constant Power=19.5 *4=78W

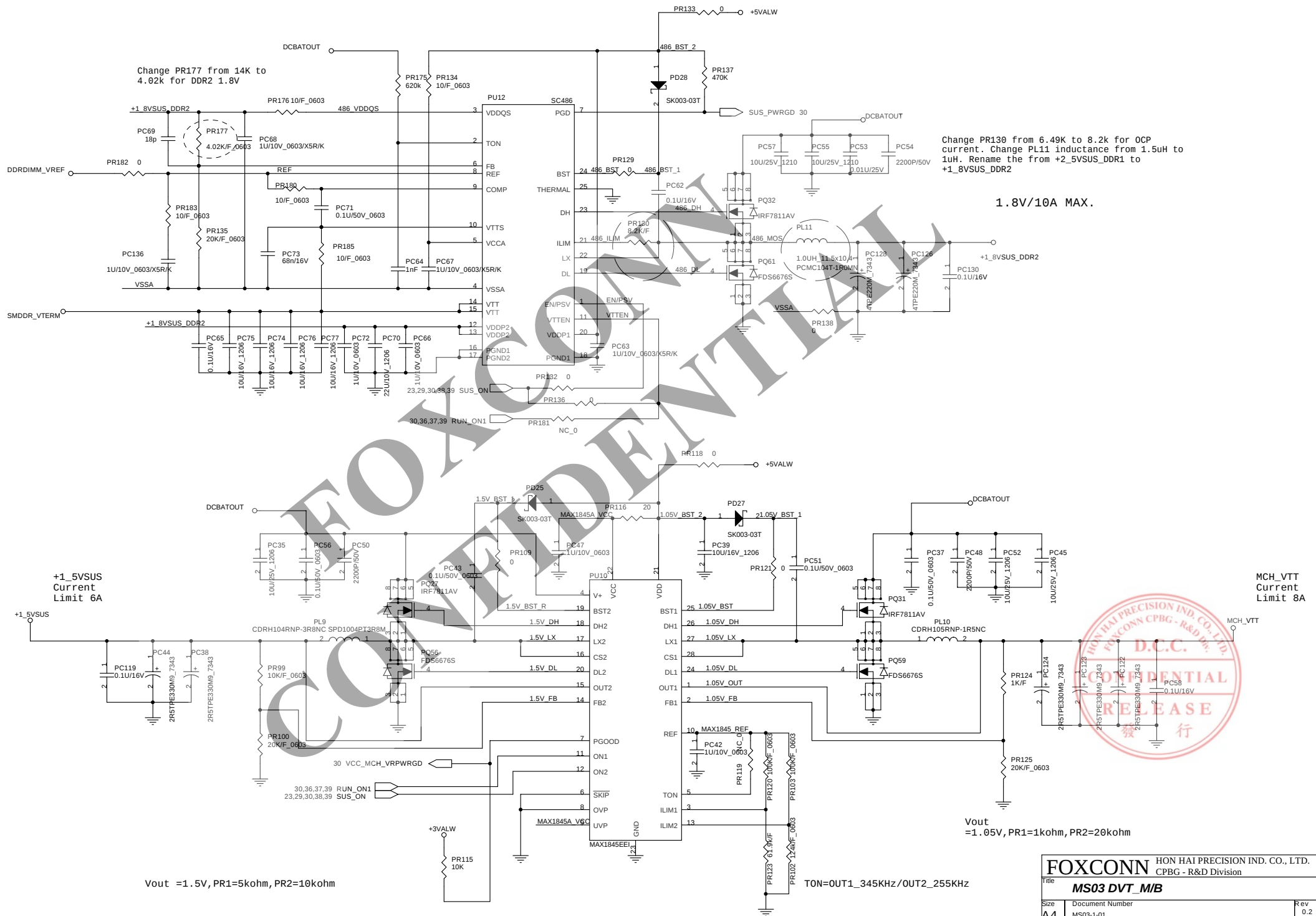
Low voltage protect set in 8.1v

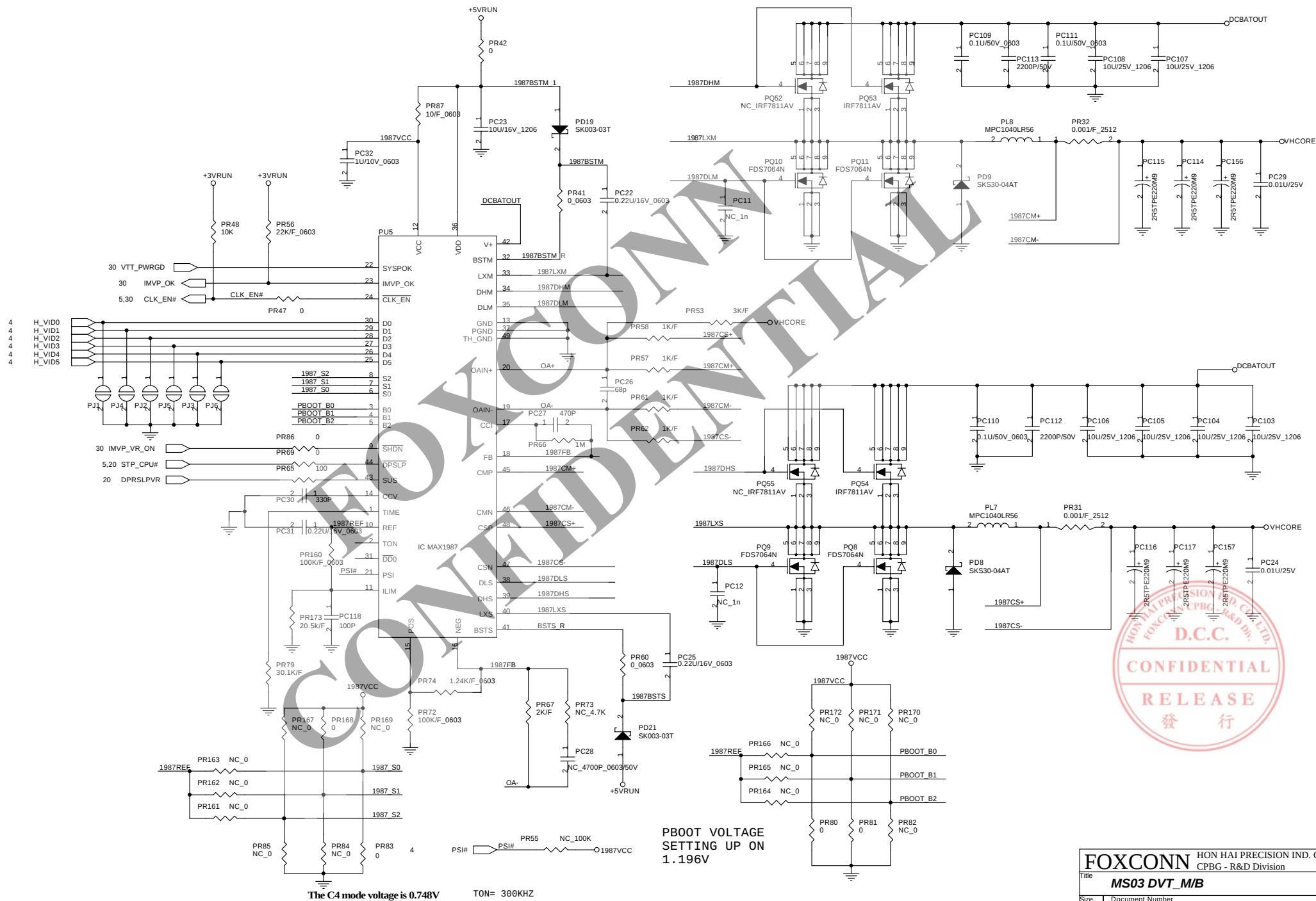
Port Replicator connection



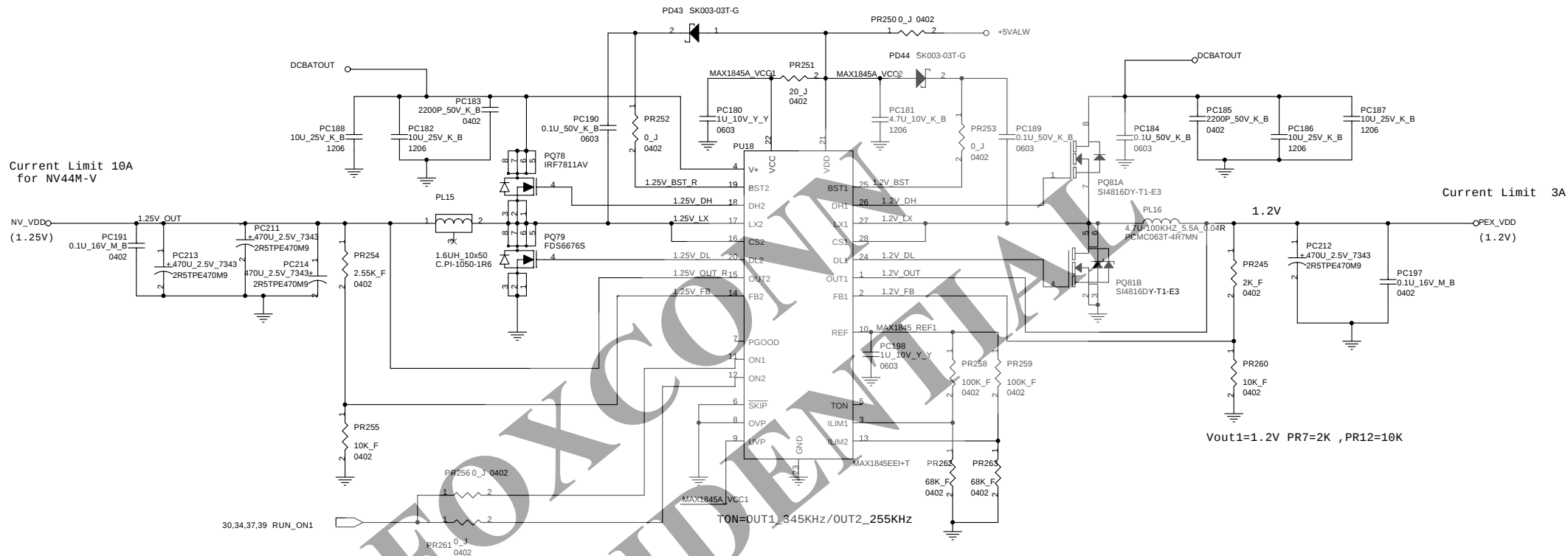
TON connect to GND = $5V/200$, $3.3V/300KHZ$

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Current Limit 10A
for NV44M-V

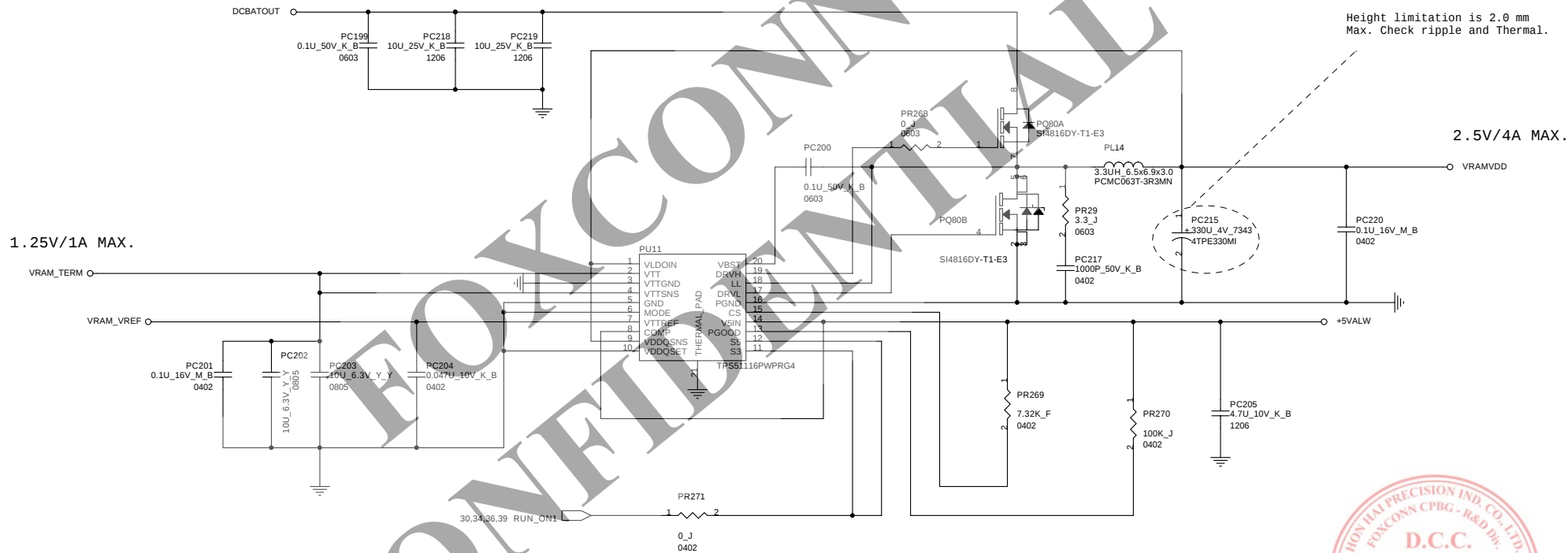


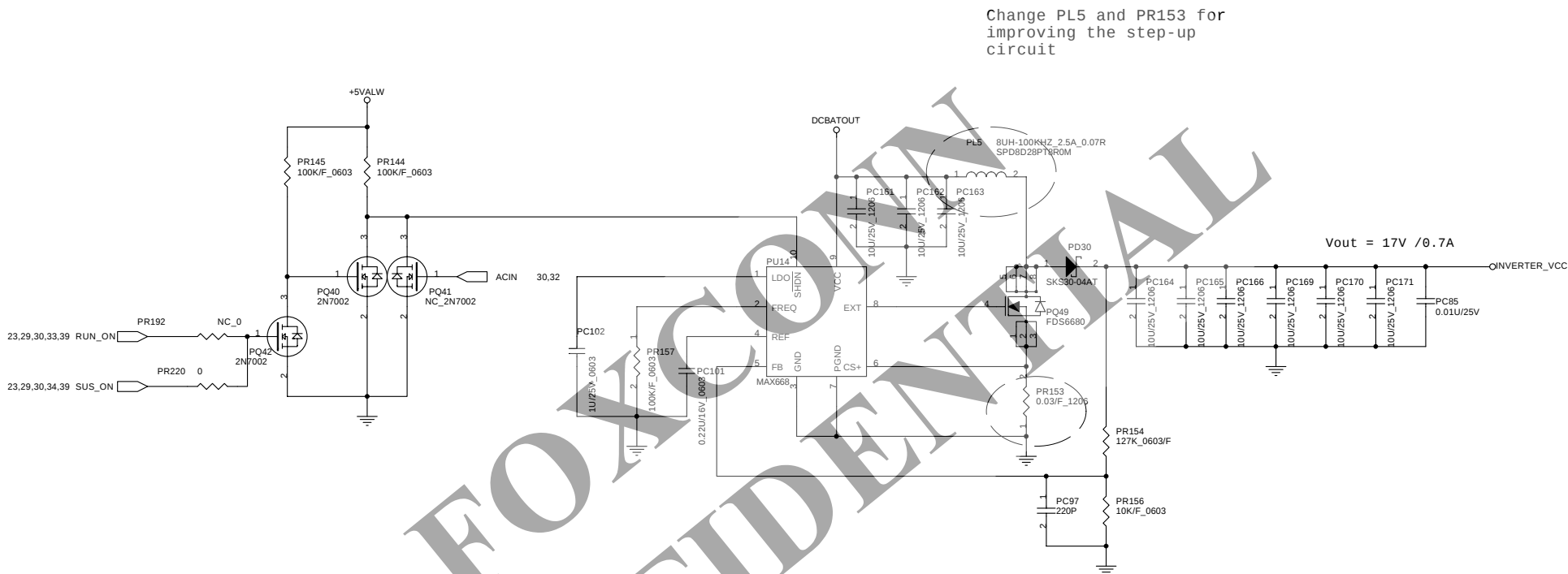
Vout1=1.2V PR7=2K ,PR12=10K

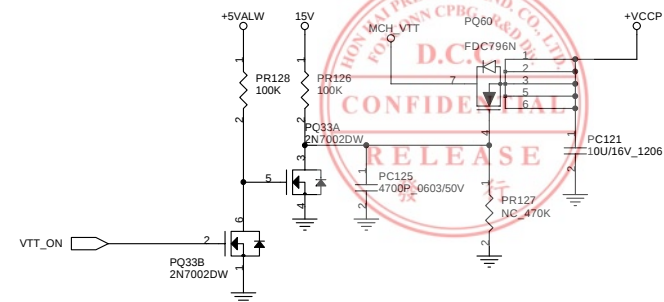
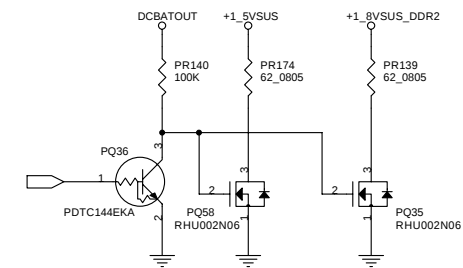
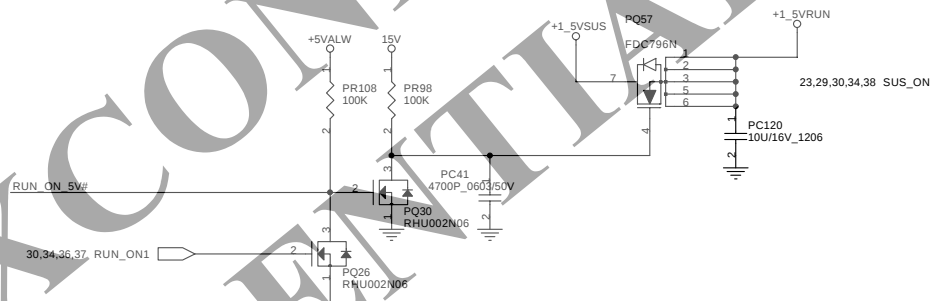
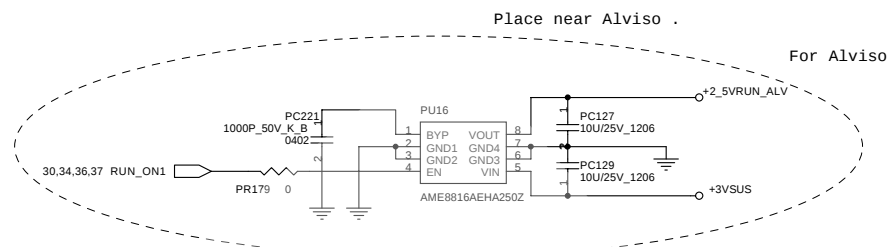
Power daughter board for VGA



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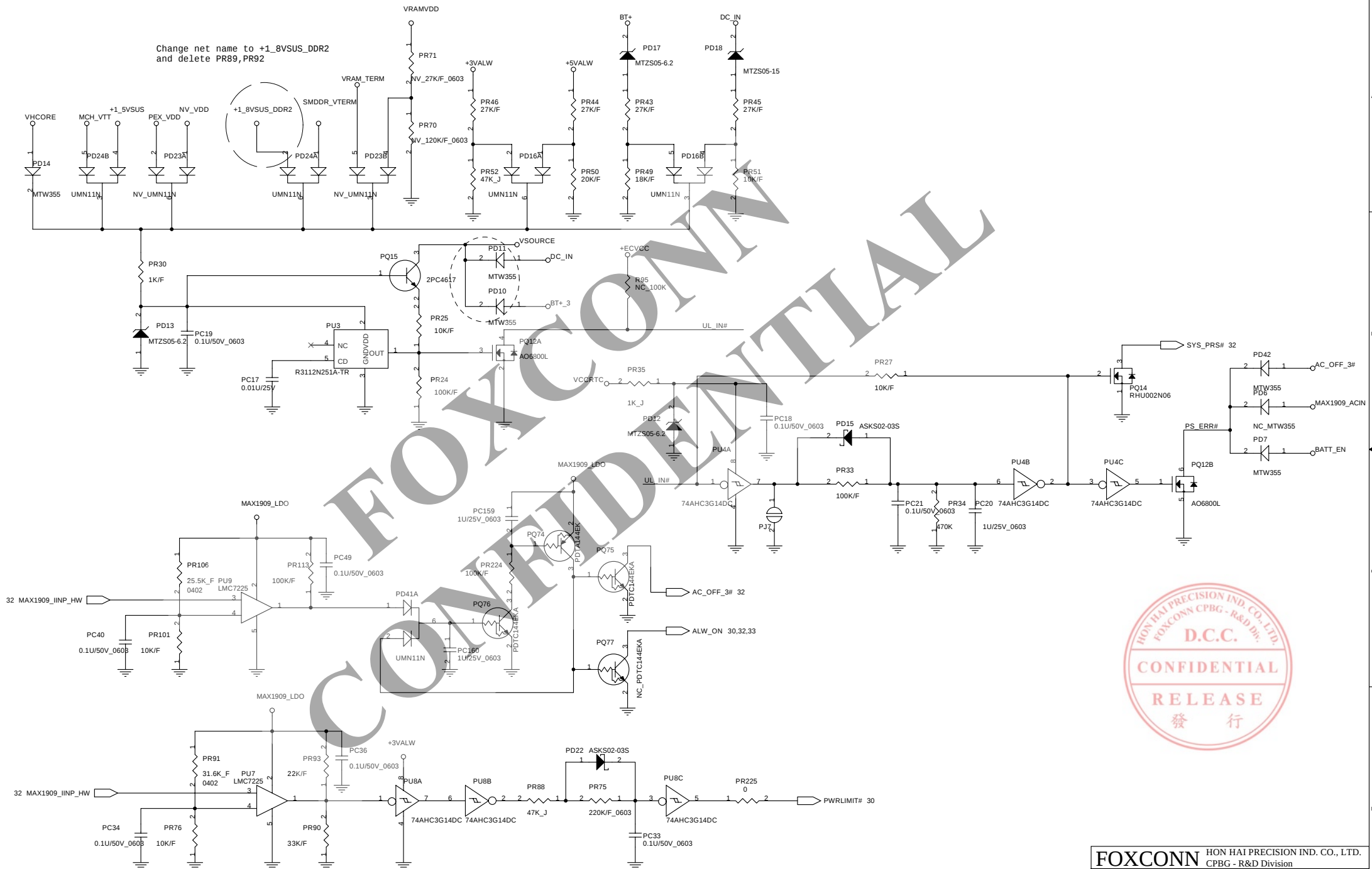






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Change net name to +1_8VSUS_DDR2
and delete PR89,PR92



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HISTORY
EVT board start .

(2005/03/31)
P14: Change D1 from NC to mount.
P15: Change R115 from mount to NC.

(2005/04/01)
P40: Rotate PD10, PD11.

(2005/04/12)
P14: Correct LVDS Bus relative of connection (swap Data+/Data-, CLK+/CLK-).
P25: Change CN14 pin16, pin17 from NC to +3VSUS, change CN14 pin18, pin20 from NC to GND.
P30: Delete SW7, Q46, R396, R721.

(2005/04/25)
P12: Add T195 for measure VRAM Timing.

(2005/04/26)
P14: Delete the right side dot of L1.

(2005/04/29)
P14: Change Q22, Q23 from 2N7002 to BSS138.

(2005/05/04)
P14: Change R694, R695, R696, R697 from 2.2K to 0 ohm.

(2005/05/09)
P26: Change H14 part from HOLE_6VIA_C256IN177D98_M2_V6(6.5mm) to HOLE_C236IN177D98_V6(6.0mm).
P15: Change R701 from NC to mount, change R702 from mount to NC.

(2005/05/10)
P32: Change PD3 from P4SSMJ24APT to MM3Z22VT1G.
P32: Change PQ5 from PDMC144EKA to 2PC4617.
P32: Change PR5 from 75K/F_0603 to 10K/F_0402.
P32: Change PR6 from 120K_0603 to 10K/F_0402.
P32: Add PU19 AME, AME431BBJETB25Z.
P32: Add PR272 100K/F_0402.
P32: Add PR273 1K/F_0402.
P36: Change PR262 from 15.8K/F_0402 to 68K/F_0402.
P36: Change PR263 from 40.2K/F_0402 to 68K/F_0402.
P36: Change PL15 footprint from CHOKE_3P_348_409X409_2 to CHOKE_3P_315_394X394_2.
P36: Delete PJ11, PJ12.
P37: Delete PJ13, PJ14.
P39: Delete PJ8, PR178.
P39: Add PC221 1000P_50V_0402.
P39: Change PU16 from LP3875 to AME8816AEHA250Z.
P05: Change R478, R481 from 33ohm to 56ohm for rising edge rate and falling edge rate.
P05: Change C696, C698, C700, C701, C702, C706 from NC to 18pF (EMI solution).
P22: Add C730, C731 (EMI solution).
P22: Connect CN17.20, CN17.32, CN17.44 to GND.
P26: Change SPR7, SPR15 from mount to NC (EMI solution).

(2005/05/11)
P23: Add D33,D34 and D35 for ESD(Not mount).
P36: Change PL15 footprint from CHOKE_3P_348_409X409_2 to L_3P_315_394X394.

(2005/05/13)
P26: Change H25, H26 footprint from ho_tc236bc158d47_v6 to ho_tc236bc158d47_mt.
P26: Change H27, H28 footprint from ho_tc1p5bc6d1p2_m2 to ho_tc1p5bc6d1p2_mb.

(2005/05/16)
P02: Update symbol ahead table, add LNC_ and HMNC_.
P30: Change R280 from mount to NC.
P30: Change R281 from AL_100K to LNC_100K.
P30: Change R293 from NC to mount.
P30: Change R294 from NV_100K to HMNC_100K.

(2005/05/17)
P26: Add R32, R33 NC_0_J (EMI solution).



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HISTORY
(2005/05/18)

P29: Change C783, C837 from 1U/10V_0603 to 2.2U_10V_Y_Y.
P26: Change H27, H28 from ho_tc1p5bc6d1p2_m2(ho_tc1p5bc6d1p2_mb) to hole_tc6bc1p5d1p2_mt(ho_tc6bc1p5d1p2_mt).
P40: Change PR91 from 31.6K to 25.5K, change PR109 from 49.9K to 31.6K.
P29: Delete R611, R622, R628, R629, R647, R648, R649, R650, JSPK1.
P29: Add C910, C911 NC_100U_6.3V_7343.

(2005/05/19)

P29: Add R734,R735 for anti-digital noise interference.

(2005/05/20)

P30: Change R311, R314 from 10K to 4.7K_J.
P29: Change R735 from mount to NC.
P05: Change R481 from 56ohm to 47ohm.
P05: Change R478 from 56ohm to 47ohm.

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