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21	VGA(LVDS/VDAC)	1.0	07'10/19	56	SYS Power(+1_5V/+1_05V)	1.0	07'10/19
22	VRAM(GDDR)	1.0	07'10/19	57	DDR2 Power(+1_8V/+0_9V)	1.0	07'10/19
23	VGA(POWER) 1/3	1.0	07'10/19	58	CPU Power_VHCORE	1.0	07'10/19
24	VGA(POWER) 2/3	1.0	07'10/19	59	VGA Power(+1_2V/+1_2V)	1.0	07'10/19
25	VGA(POWER) 3/3	1.0	07'10/19	60	Others power plane	1.0	07'10/19
26	VRAM(BYPASS)	1.0	07'10/19	61	OVP protection	1.0	07'10/19
27	CRT	1.0	07'10/19	62	HOLE	1.0	07'10/19
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M730 Main Board

M/B P/N:	**1P-0079100-8010(FUBAI)** **1P-0079500-8010(HANSTAR)** **1P-0079G00-8010(TRIPOD)**
P/B P/N:	**1P-1079100-8010(FUBAI)** **1P-1079500-8010(HANSTAR)** **1P-1079G00-8010(TRIPOD)**
U/B P/N:	**1P-1079101-8010(FUBAI)** **1P-1079501-8010 (HANSTAR)** **1P-1079G01-8010(TRIPOD)**

P. Leader	Check by	Design by

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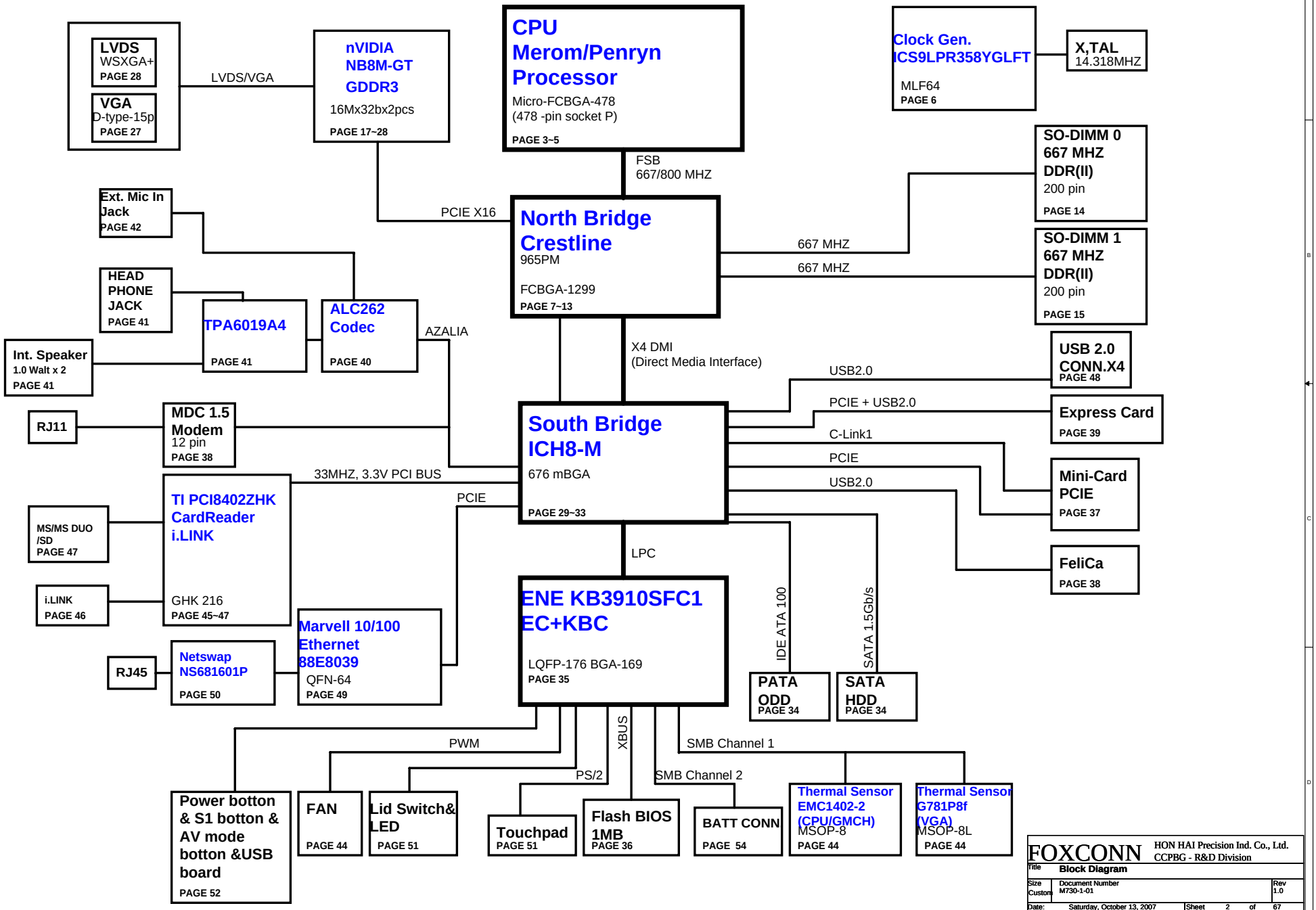
M730 (Crestline PM+Gfx Block Diagram)



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Title	Block Diagram	
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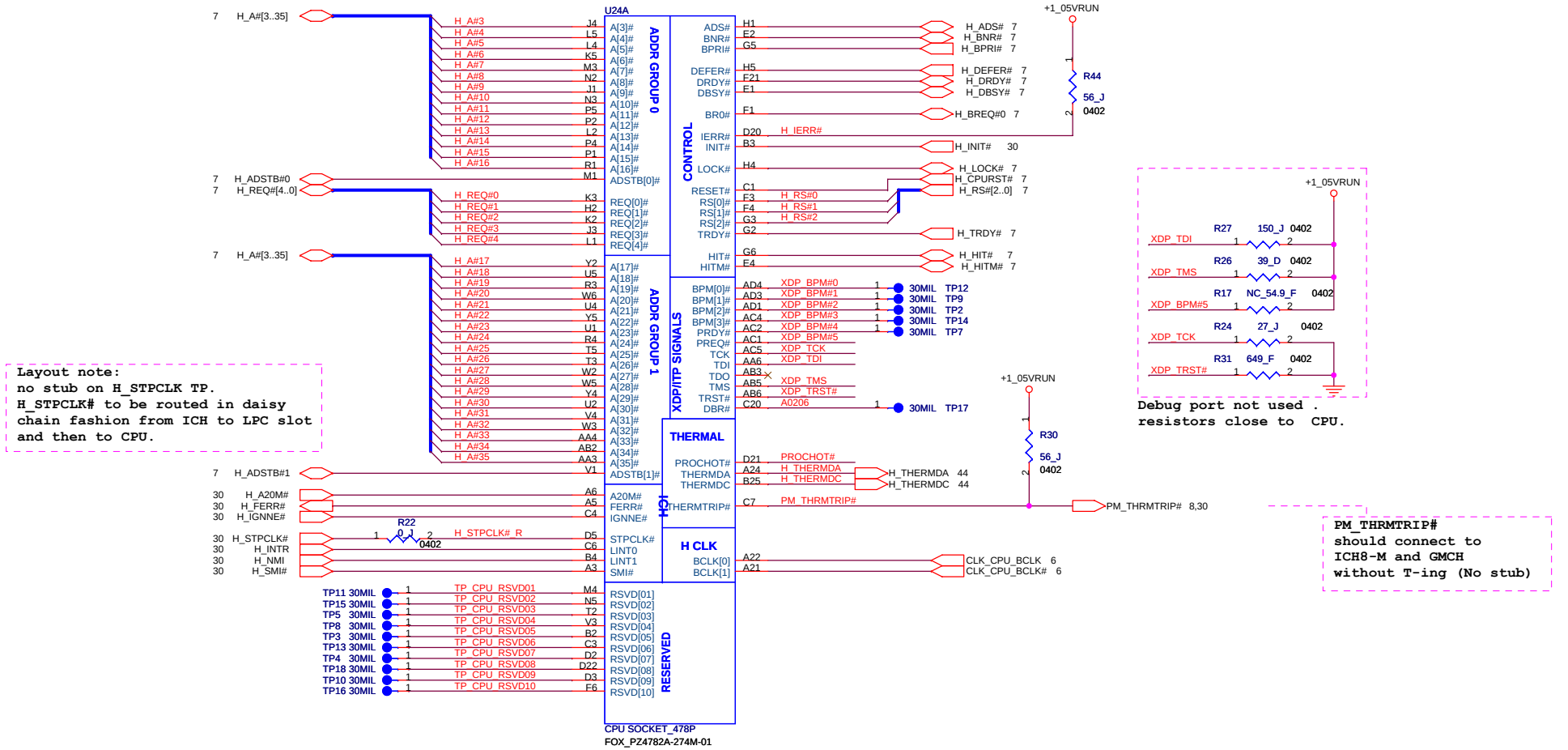

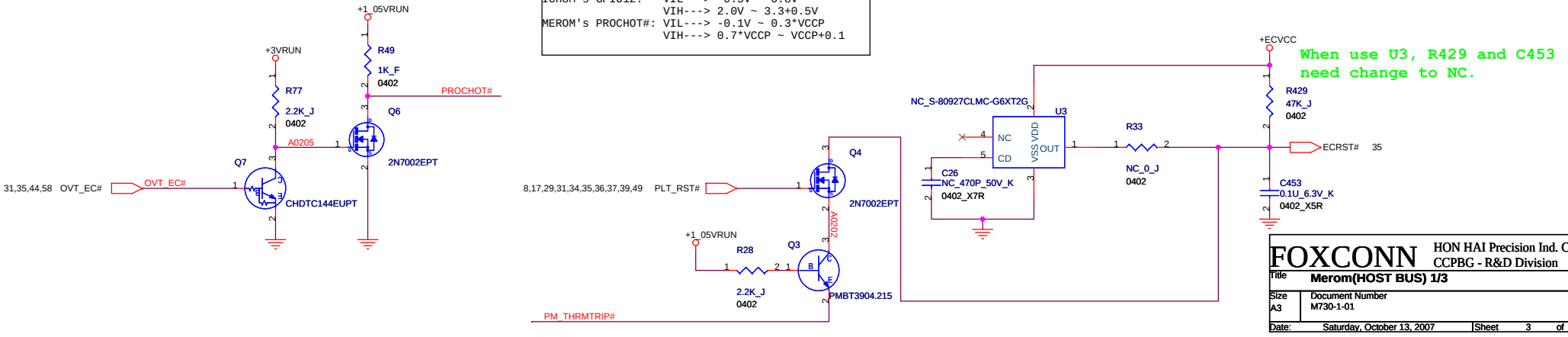

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Title	Merom(HOST BUS) 1/3		
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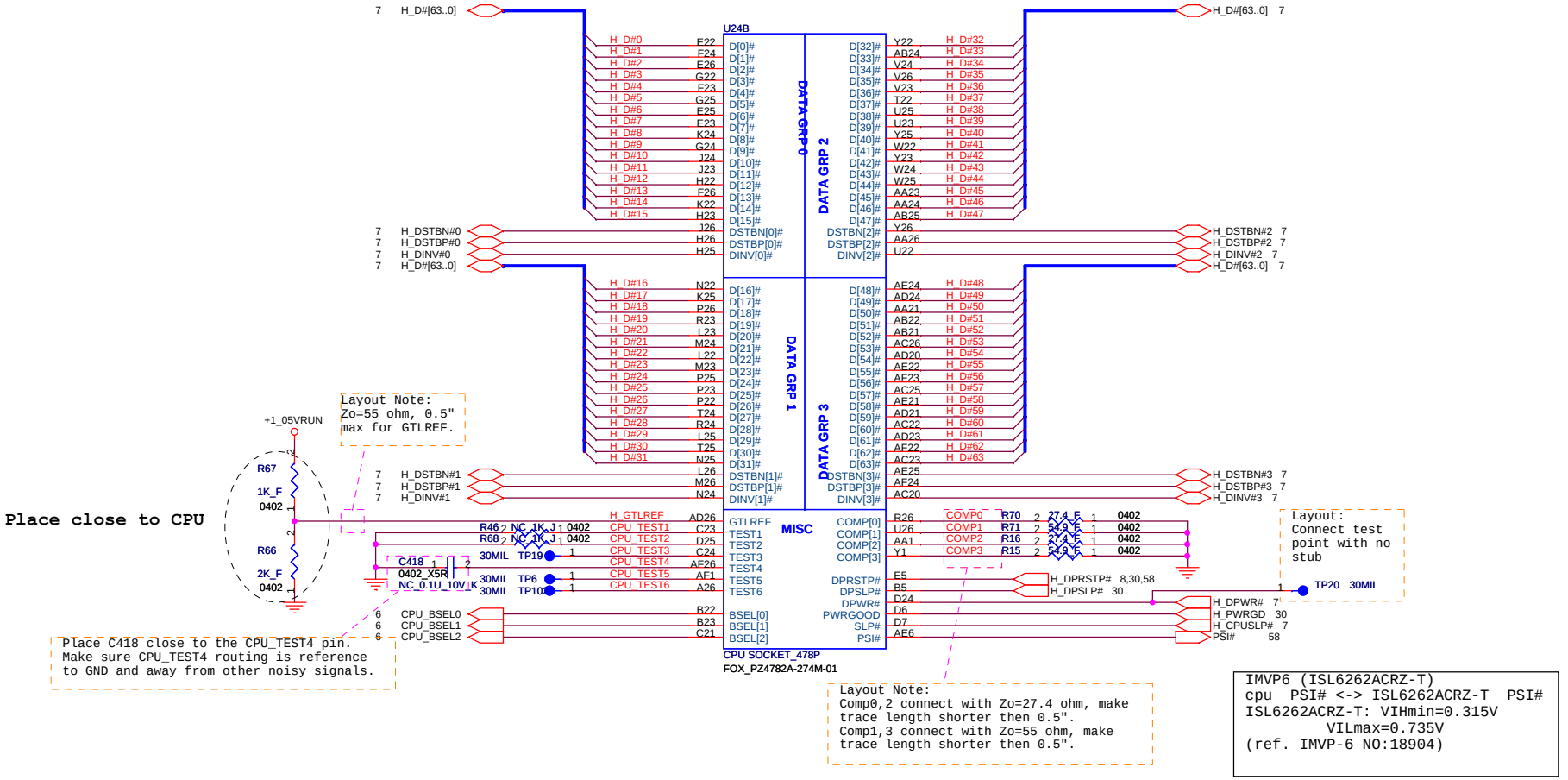

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Merom (HOST BUS) 2/3		
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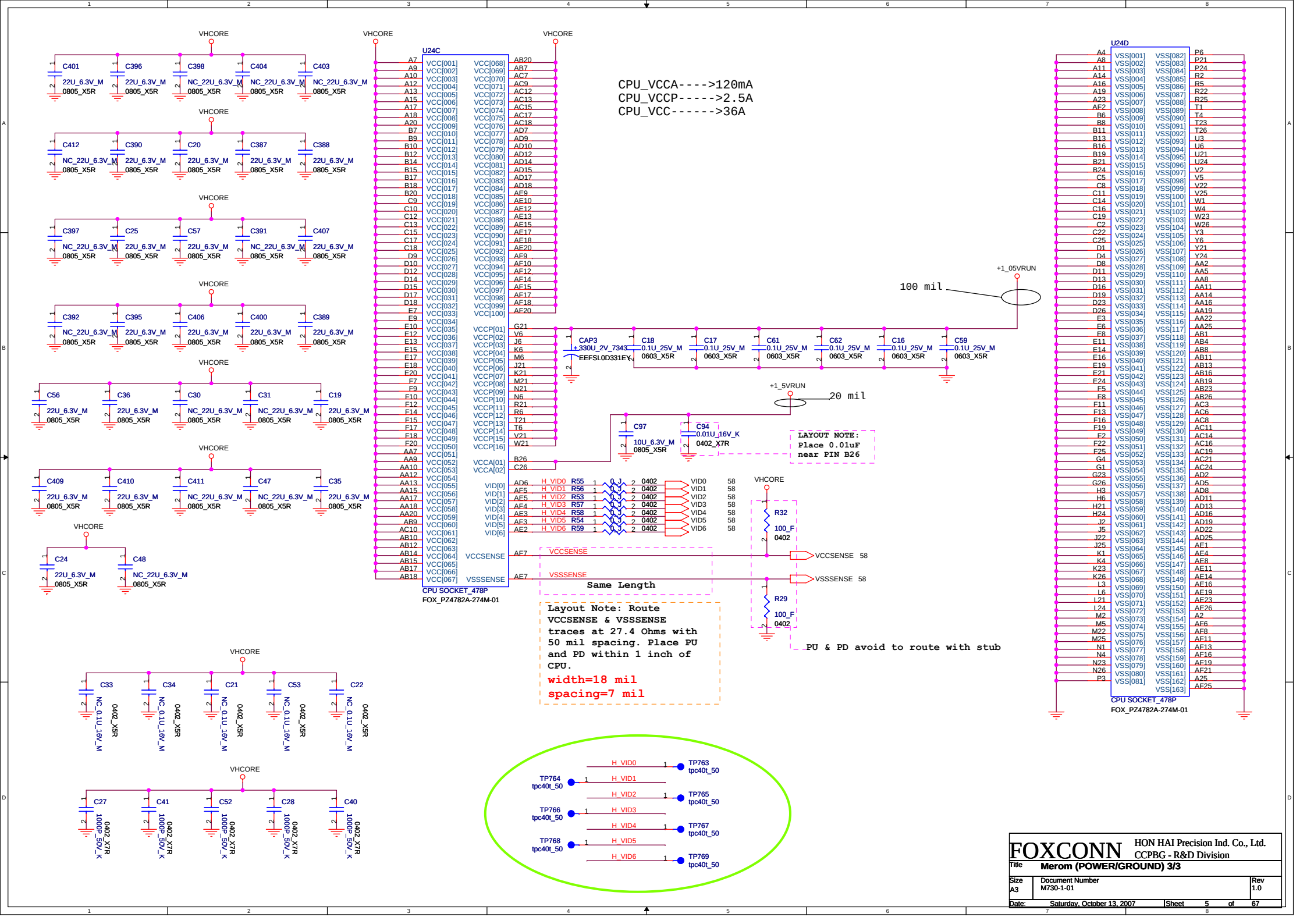
CPU_VCCA----->120mA
CPU_VCCP----->2.5A
CPU_VCC------>36A
U24C
CPU SOCKET_478P
FOX_PZ4782A-274M-01
U24D
CPU SOCKET_478P
FOX_PZ4782A-274M-01
100 mil
20 mil
+1_05VRUN
+1_5VRUN
VHCORE
LAYOUT NOTE:
Place 0.01uF
near PIN B26
Same Length
Layout Note: Route
VCCSENSE & VSSSENSE
traces at 27.4 Ohms with
50 mil spacing. Place PU
and PD within 1 inch of
CPU.
width=18 mil
spacing=7 mil
PU & PD avoid to route with stub
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Merom (POWER/GROUND) 3/3
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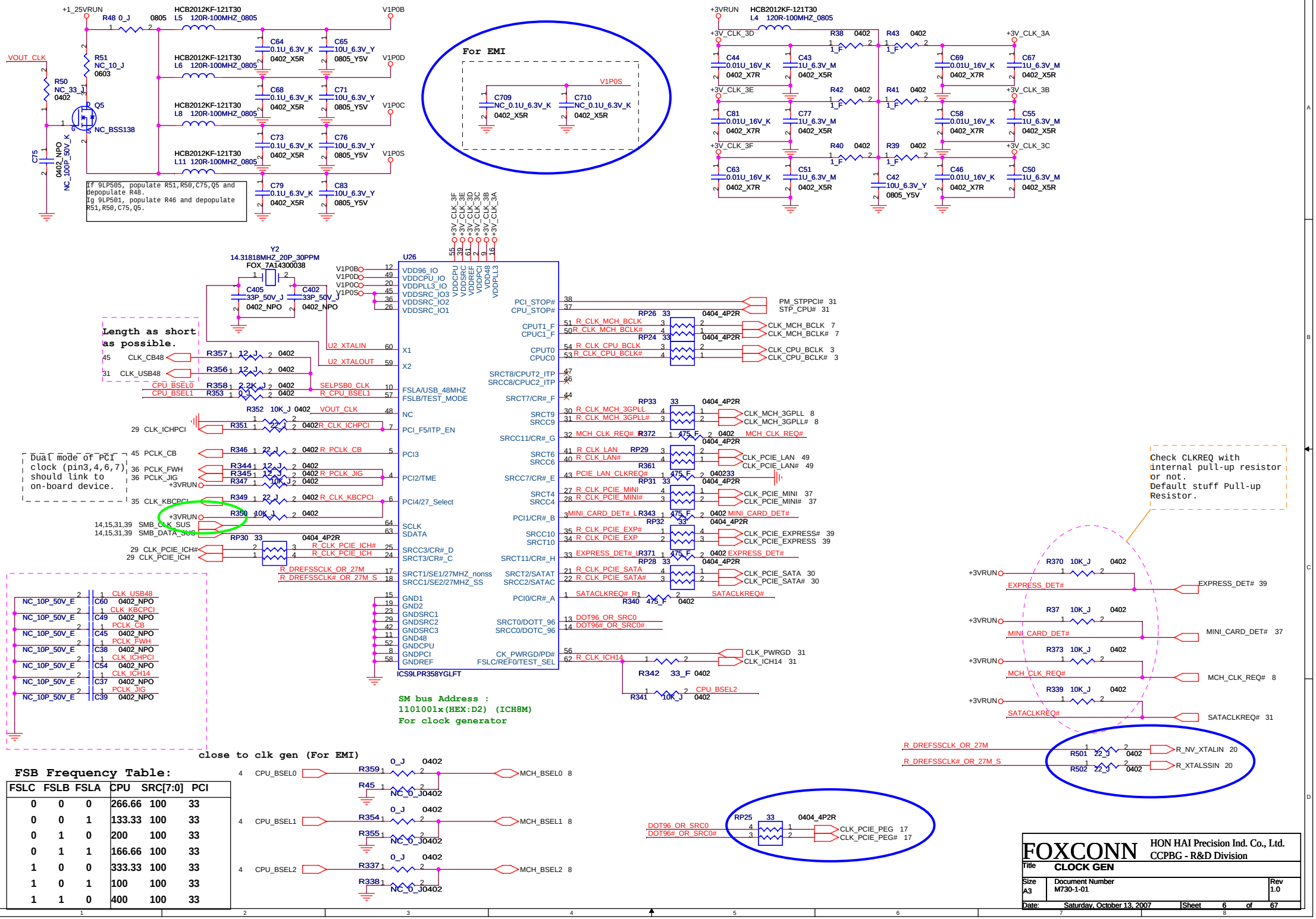
+1_25VRUN
R48 0_J 0805
HCB2012KF-121T30 L5 120R-100MHZ_0805
V1P0B
VOUT_CLK
R51 NC_10_J 0603
R50 NC_33_J 0402
Q5 NC_BSS138
C75 0402_NPO NC_100P_50V_K
HCB2012KF-121T30 L6 120R-100MHZ_0805
V1P0D
HCB2012KF-121T30 L8 120R-100MHZ_0805
V1P0C
HCB2012KF-121T30 L11 120R-100MHZ_0805
V1P0S
C64 0.1U_6.3V_K 0402_X5R
C65 10U_6.3V_Y 0805_Y5V
C68 0.1U_6.3V_K 0402_X5R
C71 10U_6.3V_Y 0805_Y5V
C73 0.1U_6.3V_K 0402_X5R
C76 10U_6.3V_Y 0805_Y5V
C79 0.1U_6.3V_K 0402_X5R
C83 10U_6.3V_Y 0805_Y5V
If 9LP505, populate R51,R50,C75,Q5 and depopulate R48.
Ig 9LP501, populate R46 and depopulate R51,R50,C75,Q5.
For EMI
C709 NC_0.1U_6.3V_K 0402_X5R
C710 NC_0.1U_6.3V_K 0402_X5R
V1P0S
+3VRUN
HCB2012KF-121T30 L4 120R-100MHZ_0805
+3V_CLK_3D
R38 0402
R43 0402
+3V_CLK_3A
C44 0.01U_16V_K 0402_X7R
C43 1U_6.3V_M 0402_X5R
C69 0.01U_16V_K 0402_X7R
C67 1U_6.3V_M 0402_X5R
+3V_CLK_3E
R42 0402
R41 0402
+3V_CLK_3B
C81 0.01U_16V_K 0402_X7R
C77 1U_6.3V_M 0402_X5R
C58 0.01U_16V_K 0402_X7R
C55 1U_6.3V_M 0402_X5R
+3V_CLK_3F
R40 0402
R39 0402
+3V_CLK_3C
C63 0.01U_16V_K 0402_X7R
C51 1U_6.3V_M 0402_X5R
C42 10U_6.3V_Y 0805_Y5V
C46 0.01U_16V_K 0402_X7R
C50 1U_6.3V_M 0402_X5R
Y2 14.31818MHZ_20P_30PPM FOX_7A14300038
C405 33P_50V_J 0402_NPO
C402 33P_50V_J 0402_NPO
U26
ICS9LPR358YGLFT
VDD96_IO
VDDCPU_IO
VDDPLL3_IO
VDDSRC_IO3
VDDSRC_IO2
VDDSRC_IO1
X1
X2
FSLA/USB_48MHZ
FSLB/TEST_MODE
NC
PCI_F5/ITP_EN
PCI3
PCI2/TME
PCI4/27_Select
SCLK
SDATA
SRCC3/CR#_D
SRCT3/CR#_C
SRCT1/SE1/27MHZ_nonss
SRCC1/SE2/27MHZ_SS
GND1
GND2
GNDSRC1
GNDSRC2
GNDSRC3
GND48
GNDCPU
GNDPCI
GNDREF
PCI_STOP#
CPU_STOP#
CPUT1_F
CPUC1_F
CPUT0
CPUC0
SRCT8/CPUT2_ITP
SRCC8/CPUC2_ITP
SRCT7/CR#_F
SRCT9
SRCC9
SRCC11/CR#_G
SRCT6
SRCC6
SRCC7/CR#_E
SRCT4
SRCC4
PCI1/CR#_B
SRCC10
SRCT10
SRCT11/CR#_H
SRCT2/SATAT
SRCC2/SATAC
PCI0/CR#_A
SRCT0/DOTT_96
SRCC0/DOTC_96
CK_PWRGD/PD#
FSLC/REF0/TEST_SEL
Length as short as possible.
CLK_CB48
CLK_USB48
R357 12_J 0402
R356 12_J 0402
U2_XTALIN
U2_XTALOUT
CPU_BSEL0
CPU_BSEL1
R358 2.2K_J 0402
R353 0_J 0402
SELPSB0_CLK
R_CPU_BSEL1
R352 10K_J 0402
VOUT_CLK
CLK_ICHPCI
R351 22_J 0402
R_CLK_ICHPCI
Dual mode of PCI clock (pin3,4,6,7) should link to on-board device.
PCLK_CB
PCLK_FWH
PCLK_JIG
R346 22_J 0402
R_PCLK_CB
R344 12_J 0402
R345 12_J 0402
R_PCLK_JIG
R347 10K_J 0402
+3VRUN
CLK_KBCPCI
R349 22_J 0402
R_CLK_KBCPCI
R359 10K_J 0402
SMB_CLK_SUS
SMB_DATA_SUS
RP30 33 0404_4P2R
R_CLK_PCIE_ICH#
R_CLK_PCIE_ICH
CLK_PCIE_ICH#
CLK_PCIE_ICH
R_DREFSSCLK_OR_27M
R_DREFSSCLK#_OR_27M_S
NC_10P_50V_E C60 0402_NPO CLK_USB48
NC_10P_50V_E C49 0402_NPO CLK_KBCPCI
NC_10P_50V_E C45 0402_NPO PCLK_CB
NC_10P_50V_E C38 0402_NPO PCLK_FWH
NC_10P_50V_E C54 0402_NPO CLK_ICHPCI
NC_10P_50V_E C37 0402_NPO CLK_ICH14
NC_10P_50V_E C39 0402_NPO PCLK_JIG
SM bus Address :
1101001x(HEX:D2) (ICH8M)
For clock generator
close to clk gen (For EMI)
CPU_BSEL0 R359 0_J 0402 MCH_BSEL0
R45 NC_0_J0402
CPU_BSEL1 R354 0_J 0402 MCH_BSEL1
R355 NC_0_J0402
CPU_BSEL2 R337 0_J 0402 MCH_BSEL2
R338 NC_0_J0402
FSB Frequency Table:
FSLC FSLB FSLA CPU SRC[7:0] PCI
0 0 0 266.66 100 33
0 0 1 133.33 100 33
0 1 0 200 100 33
0 1 1 166.66 100 33
1 0 0 333.33 100 33
1 0 1 100 100 33
1 1 0 400 100 33
+3V_CLK_3F +3V_CLK_3E +3V_CLK_3D +3V_CLK_3C +3V_CLK_3B +3V_CLK_3A
55 39 61 2 9 16
V1P0B V1P0D V1P0C V1P0S
VDDCPU VDDSRC VDDREF VDDPCI VDD48 VDDPLL3
RP26 33 0404_4P2R
R_CLK_MCH_BCLK
R_CLK_MCH_BCLK#
CLK_MCH_BCLK
CLK_MCH_BCLK#
RP24 33 0404_4P2R
R_CLK_CPU_BCLK
R_CLK_CPU_BCLK#
CLK_CPU_BCLK
CLK_CPU_BCLK#
PM_STPPCI# STP_CPU#
RP33 33 0404_4P2R
R_CLK_MCH_3GPLL
R_CLK_MCH_3GPLL#
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
R372 475_F 0402
MCH_CLK_REQ#
RP29 33 0404_4P2R
R_CLK_LAN
R_CLK_LAN#
CLK_PCIE_LAN
CLK_PCIE_LAN#
R361 475_F 0402
PCIE_LAN_CLKREQ#
040233
RP31 33 0404_4P2R
R_CLK_PCIE_MINI
R_CLK_PCIE_MINI#
CLK_PCIE_MINI
CLK_PCIE_MINI#
R343 475_F 0402
MINI_CARD_DET#
RP32 33 0404_4P2R
R_CLK_PCIE_EXP#
R_CLK_PCIE_EXP
CLK_PCIE_EXPRESS#
CLK_PCIE_EXPRESS
R371 475_F 0402
EXPRESS_DET#
RP28 33 0404_4P2R
R_CLK_PCIE_SATA
R_CLK_PCIE_SATA#
CLK_PCIE_SATA
CLK_PCIE_SATA#
R340 475_F 0402
SATACLKREQ#
DOT96_OR_SRC0
DOT96#_OR_SRC0#
R_CLK_ICH14
CLK_PWRGD
CLK_ICH14
R342 33_F 0402
CPU_BSEL2
R341 10K_J 0402
Check CLKREQ with internal pull-up resistor or not.
Default stuff Pull-up Resistor.
R370 10K_J 0402
+3VRUN
EXPRESS_DET#
EXPRESS_DET# 39
R37 10K_J 0402
MINI_CARD_DET#
MINI_CARD_DET# 37
R373 10K_J 0402
MCH_CLK_REQ#
MCH_CLK_REQ# 8
R339 10K_J 0402
SATACLKREQ#
SATACLKREQ# 31
R_DREFSSCLK_OR_27M
R_DREFSSCLK#_OR_27M_S
R501 22_J 0402
R502 22_J 0402
R_NV_XTALIN 20
R_XTALSSIN 20
RP25 33 0404_4P2R
DOT96_OR_SRC0
DOT96#_OR_SRC0#
CLK_PCIE_PEG 17
CLK_PCIE_PEG# 17
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
CLOCK GEN
Size A3
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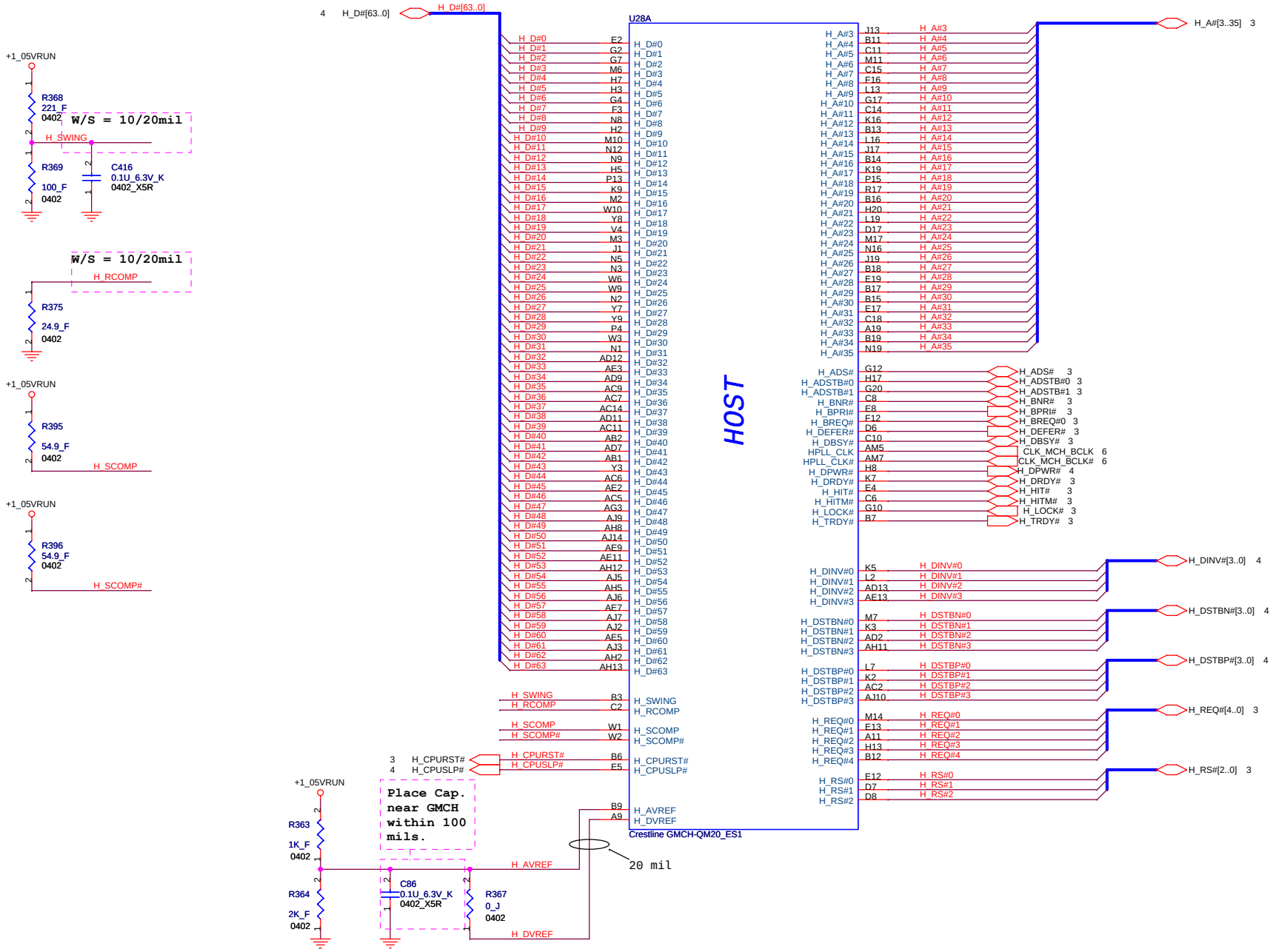

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Crestline (HOST) 1/7	
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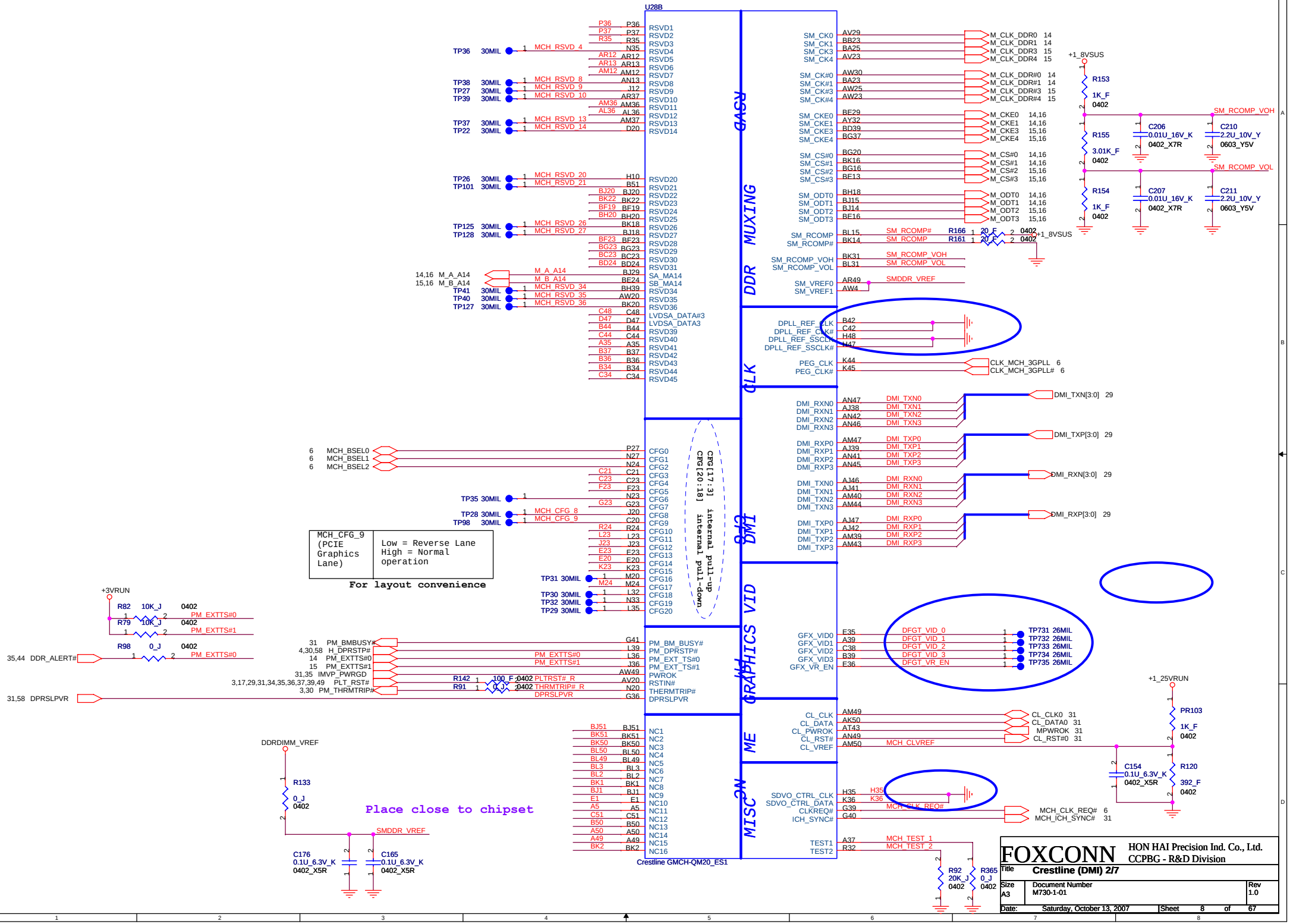
U28B
GMCH
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
SA_MA14
SB_MA14
RSVD34
RSVD35
RSVD36
LVDSA_DATA#3
LVDSA_DATA3
RSVD39
RSVD40
RSVD41
RSVD42
RSVD43
RSVD44
RSVD45
MCH_RSVD_4
MCH_RSVD_8
MCH_RSVD_9
MCH_RSVD_10
MCH_RSVD_13
MCH_RSVD_14
MCH_RSVD_20
MCH_RSVD_21
MCH_RSVD_26
MCH_RSVD_27
MCH_RSVD_34
MCH_RSVD_35
MCH_RSVD_36
M_A_A14
M_B_A14
TP36 30MIL
TP38 30MIL
TP27 30MIL
TP39 30MIL
TP37 30MIL
TP22 30MIL
TP26 30MIL
TP101 30MIL
TP125 30MIL
TP128 30MIL
TP41 30MIL
TP40 30MIL
TP127 30MIL
SM_CK0
SM_CK1
SM_CK3
SM_CK4
SM_CK#0
SM_CK#1
SM_CK#3
SM_CK#4
SM_CKE0
SM_CKE1
SM_CKE3
SM_CKE4
SM_CS#0
SM_CS#1
SM_CS#2
SM_CS#3
SM_ODT0
SM_ODT1
SM_ODT2
SM_ODT3
SM_RCOMP
SM_RCOMP#
SM_RCOMP_VOH
SM_RCOMP_VOL
SM_VREF0
SM_VREF1
M_CLK_DDR0 14
M_CLK_DDR1 14
M_CLK_DDR3 15
M_CLK_DDR4 15
M_CLK_DDR#0 14
M_CLK_DDR#1 14
M_CLK_DDR#3 15
M_CLK_DDR#4 15
M_CKE0 14,16
M_CKE1 14,16
M_CKE3 15,16
M_CKE4 15,16
M_CS#0 14,16
M_CS#1 14,16
M_CS#2 15,16
M_CS#3 15,16
M_ODT0 14,16
M_ODT1 14,16
M_ODT2 15,16
M_ODT3 15,16
SM_RCOMP# R166 1 20_F 2 0402
SM_RCOMP R161 1 20_F 2 0402
+1_8VSUS
SMDDR_VREF
DDR MUXING
DPLL_REF_CLK
DPLL_REF_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
PEG_CLK
PEG_CLK#
CLK_MCH_3GPLL 6
CLK_MCH_3GPLL# 6
CLK
DMI_RXN0
DMI_RXN1
DMI_RXN2
DMI_RXN3
DMI_TXN0
DMI_TXN1
DMI_TXN2
DMI_TXN3
DMI_TXN[3:0] 29
DMI_TXP[3:0] 29
DMI_RXN[3:0] 29
DMI_RXP[3:0] 29
DMI
CFG[20:18] internal pull-up
CFG[17:3] internal pull-down
MCH_BSEL0 6
MCH_BSEL1 6
MCH_BSEL2 6
MCH_CFG_8
MCH_CFG_9
TP35 30MIL
TP28 30MIL
TP98 30MIL
TP31 30MIL
TP30 30MIL
TP32 30MIL
TP29 30MIL
MCH_CFG_9 (PCIE Graphics Lane)
Low = Reverse Lane
High = Normal operation
For layout convenience
CFG
GFX_VID0
GFX_VID1
GFX_VID2
GFX_VID3
GFX_VR_EN
DFGT_VID_0
DFGT_VID_1
DFGT_VID_2
DFGT_VID_3
DFGT_VR_EN
TP731 26MIL
TP732 26MIL
TP733 26MIL
TP734 26MIL
TP735 26MIL
VID
GRAPHICS
PM_BMBUSY#
PM_DPRSTP#
PM_EXT_TS#0
PM_EXT_TS#1
PWROK
RSTIN#
THERMTRIP#
DPRSLPVR
PM_EXTTS#0
PM_EXTTS#1
IMVP_PWRGD
PLT_RST#
PLTRST#_R
THRMTRIP#_R
R142 100_F 0402
R91 0_J 0402
31,58 DPRSLPVR
35,44 DDR_ALERT#
+3VRUN
R82 10K_J 0402 PM_EXTTS#0
R79 10K_J 0402 PM_EXTTS#1
R98 0_J 0402
GMCH
CL_CLK
CL_DATA
CL_PWROK
CL_RST#
CL_VREF
CL_CLK0 31
CL_DATA0 31
MPWROK 31
CL_RST#0 31
MCH_CLVREF
ME
SDVO_CTRL_CLK
SDVO_CTRL_DATA
CLKREQ#
ICH_SYNC#
MCH_CLK_REQ# 6
MCH_ICH_SYNC# 31
MISC
TEST1
TEST2
MCH_TEST_1
MCH_TEST_2
R92 20K_J 0402
R365 0_J 0402
+1_25VRUN
PR103 1K_F 0402
C154 0.1U_6.3V_K 0402_X5R
R120 392_F 0402
DDRDIMM_VREF
R133 0_J 0402
SMDDR_VREF
C176 0.1U_6.3V_K 0402_X5R
C165 0.1U_6.3V_K 0402_X5R
Place close to chipset
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
NC13
NC14
NC15
NC16
Crestline GMCH-QM20_ES1
+1_8VSUS
R153 1K_F 0402
R155 3.01K_F 0402
R154 1K_F 0402
C206 0.01U_16V_K 0402_X7R
C207 0.01U_16V_K 0402_X7R
C210 2.2U_10V_Y 0603_Y5V
C211 2.2U_10V_Y 0603_Y5V
SM_RCOMP_VOH
SM_RCOMP_VOL
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title Crestline (DMI) 2/7
Size A3
Document Number M730-1-01
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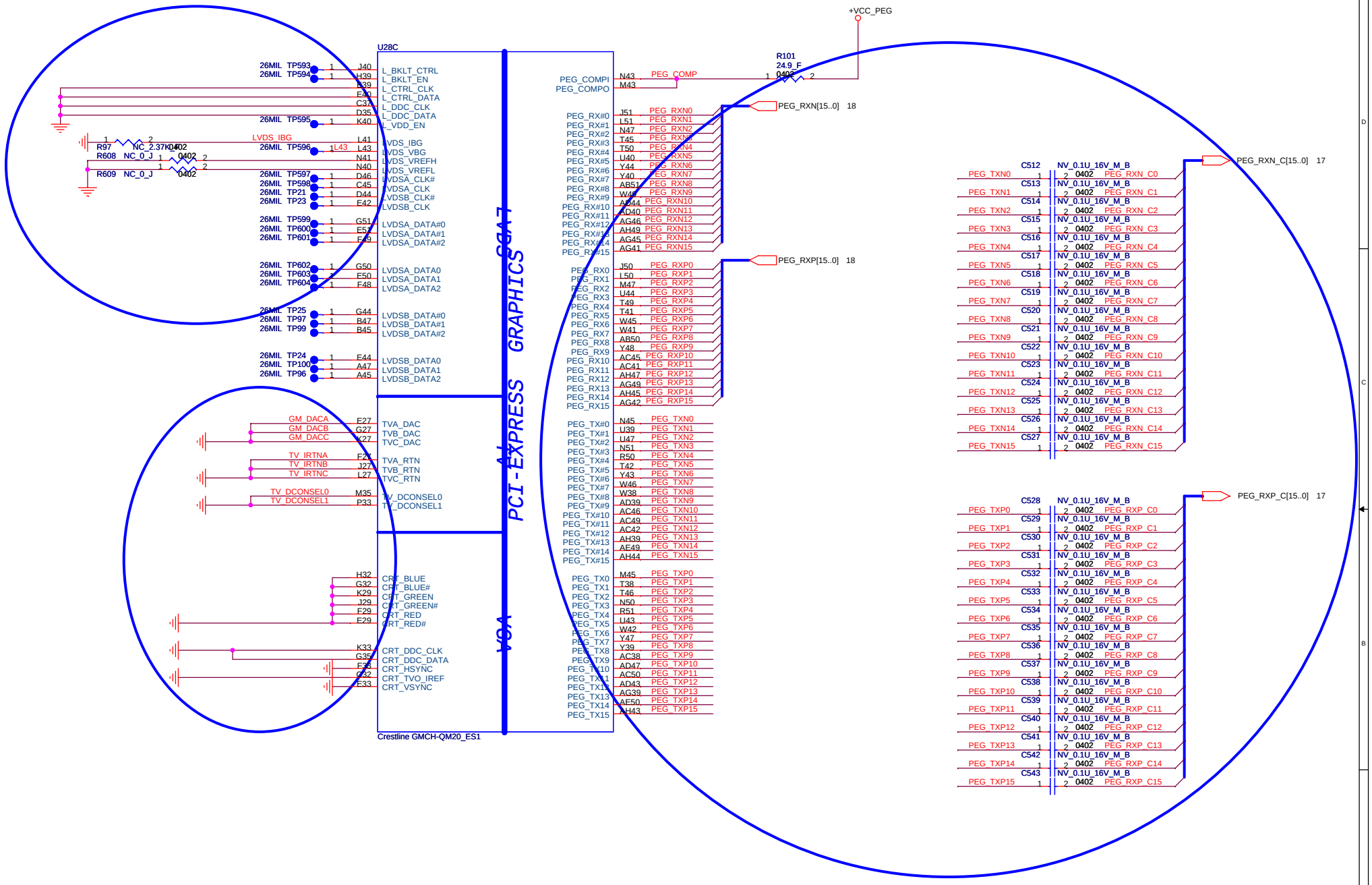
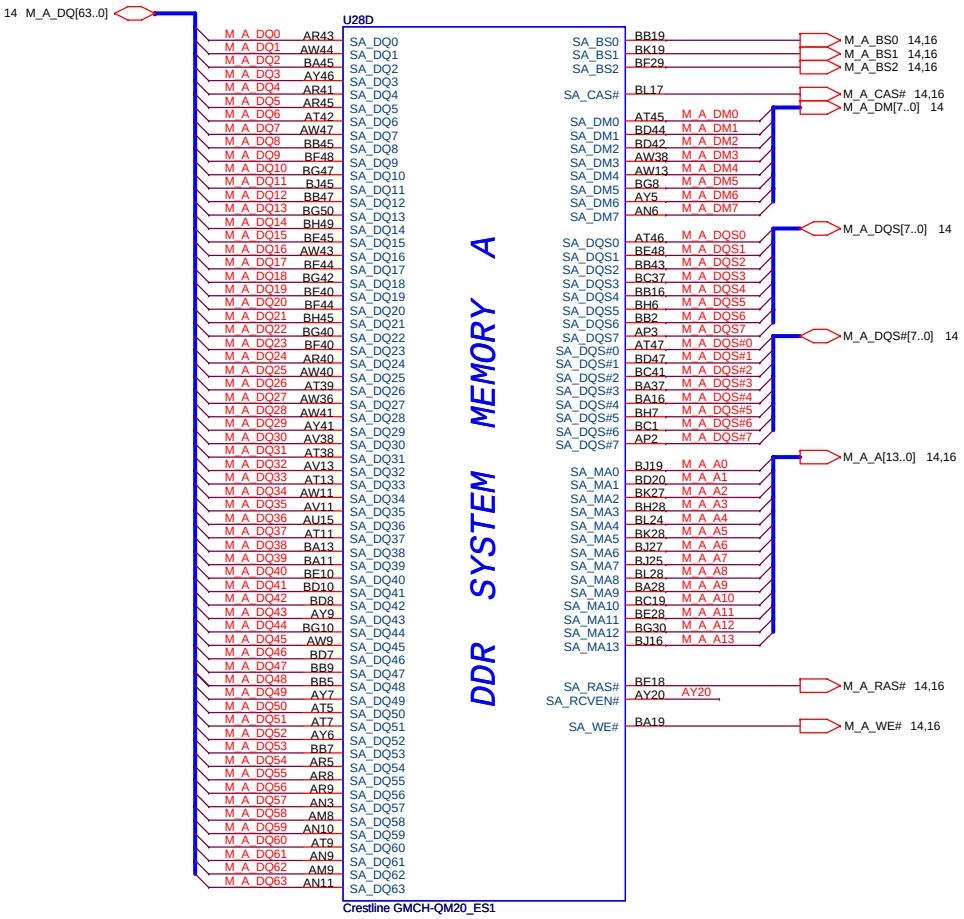
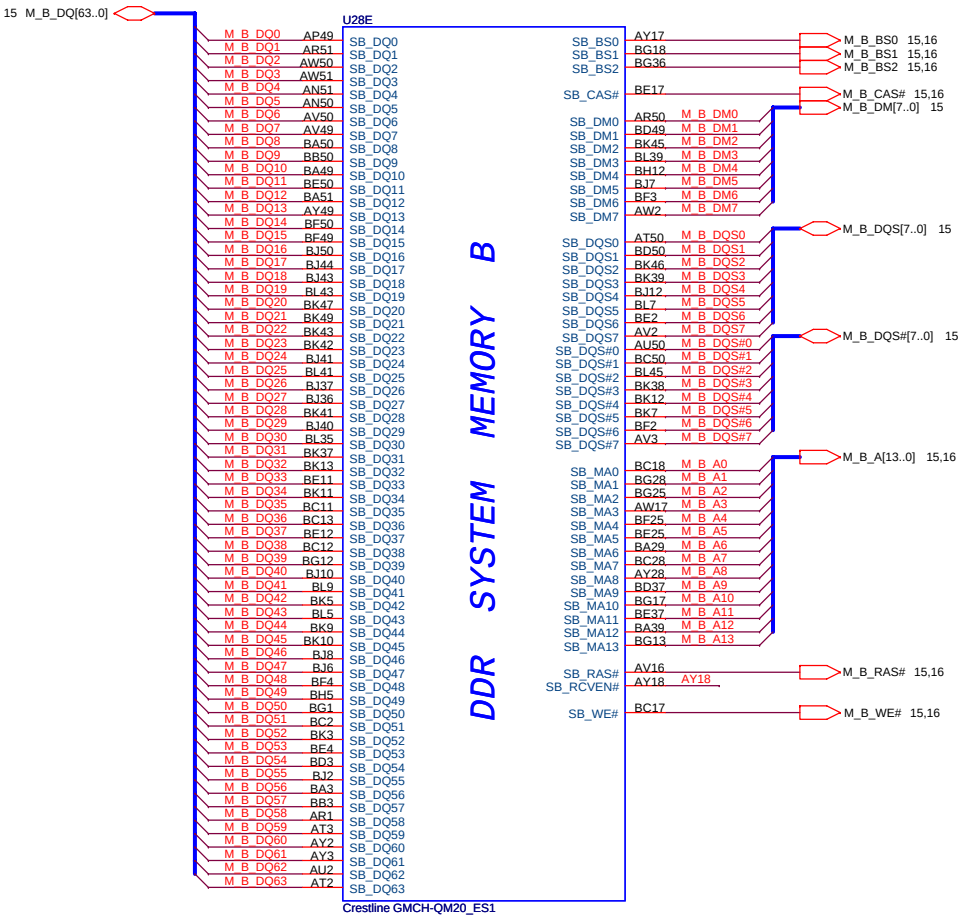
Date: Saturday, October 13, 2007
Sheet 8 of 67



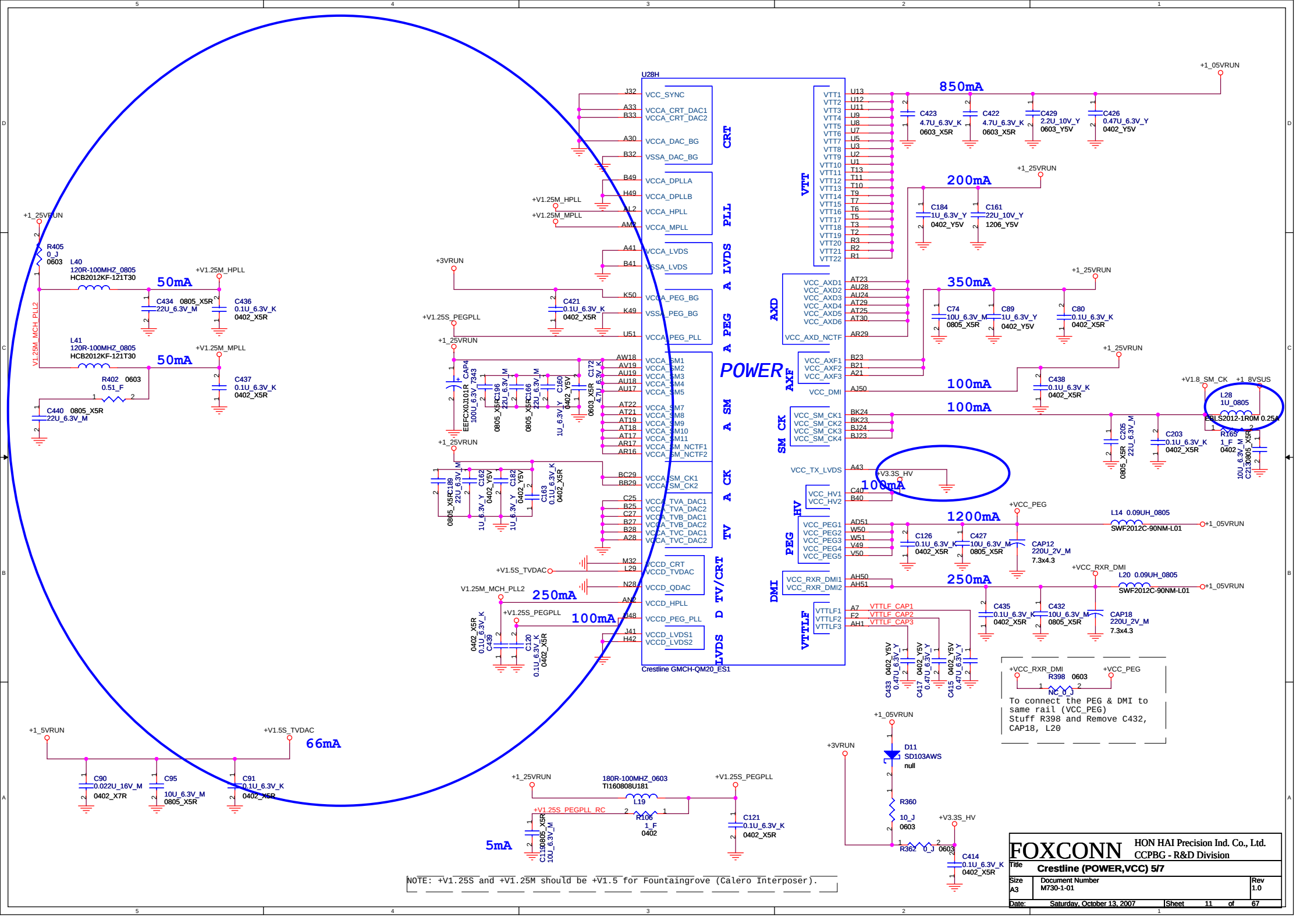
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Crestline (GRAPHIC) 3/7		
Size A3	Document Number M730-1-01		Rev 1.0
Date: Saturday, October 13, 2007		Sheet 9 of 67	





FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Crestline (DDRII) 4/7	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 10 of 67	


POWER
U28H
Crestline GMCH-QM20_ES1
CRT
PLL
LVDS
PEG
SM
CK
TV
TV/CRT
LVDS
VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
850mA
200mA
350mA
100mA
100mA
100mA
1200mA
250mA
250mA
50mA
50mA
66mA
5mA
+1_05VRUN
+1_25VRUN
+3VRUN
+1.8_SM_CK
+1_8VSUS
+V3.3S_HV
+VCC_PEG
+VCC_RXR_DMI
+V1.5S_TVDAC
+V1.25S_PEGPLL
+V1.25M_HPLL
+V1.25M_MPLL
V1.25M_MCH_PLL2
To connect the PEG & DMI to same rail (VCC_PEG)
Stuff R398 and Remove C432, CAP18, L20
NOTE: +V1.25S and +V1.25M should be +V1.5 for Fountaingrove (Calero Interposer).
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Crestline (POWER,VCC) 5/7
Size A3
Document Number M730-1-01
Rev 1.0
Date: Saturday, October 13, 2007
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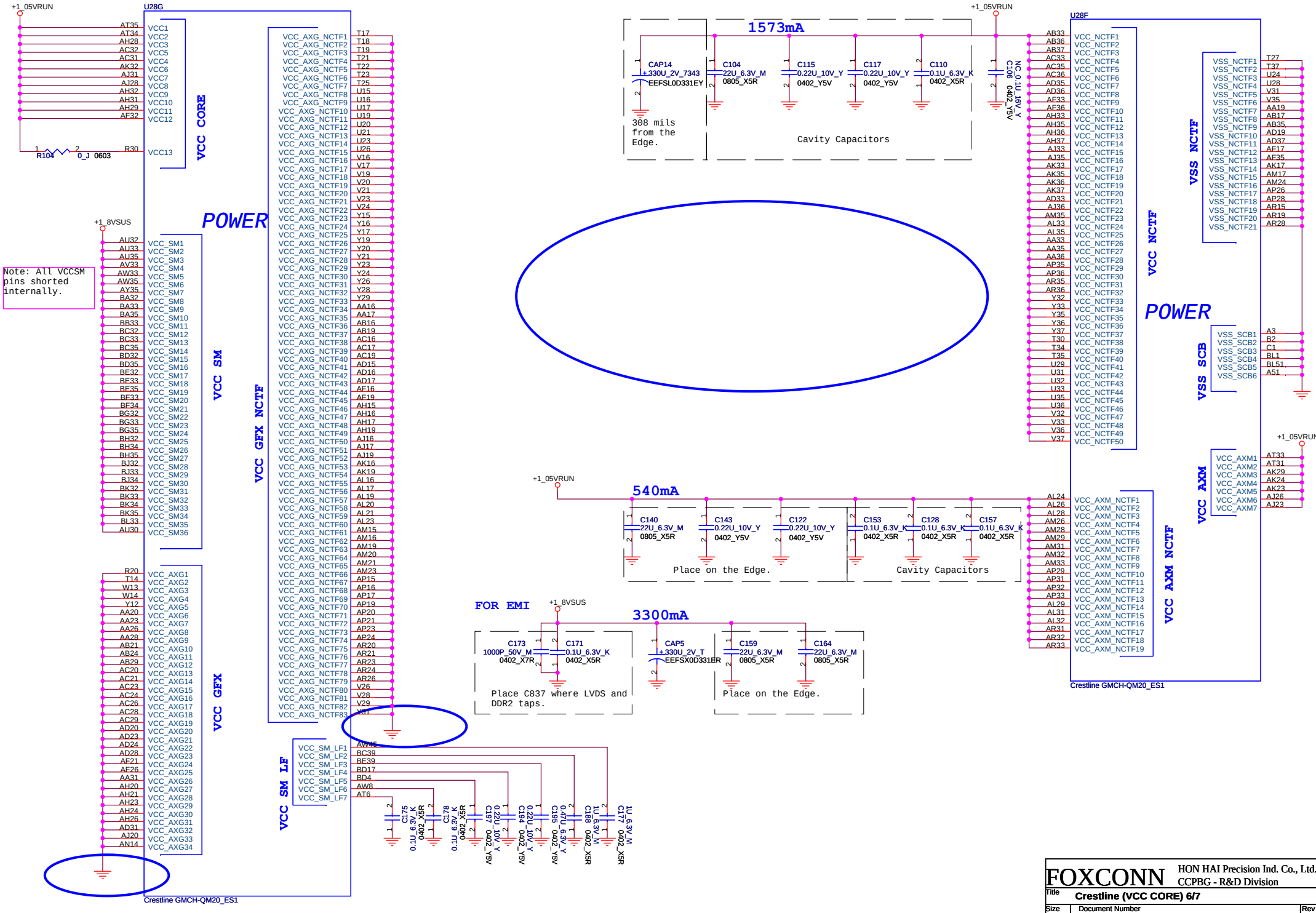
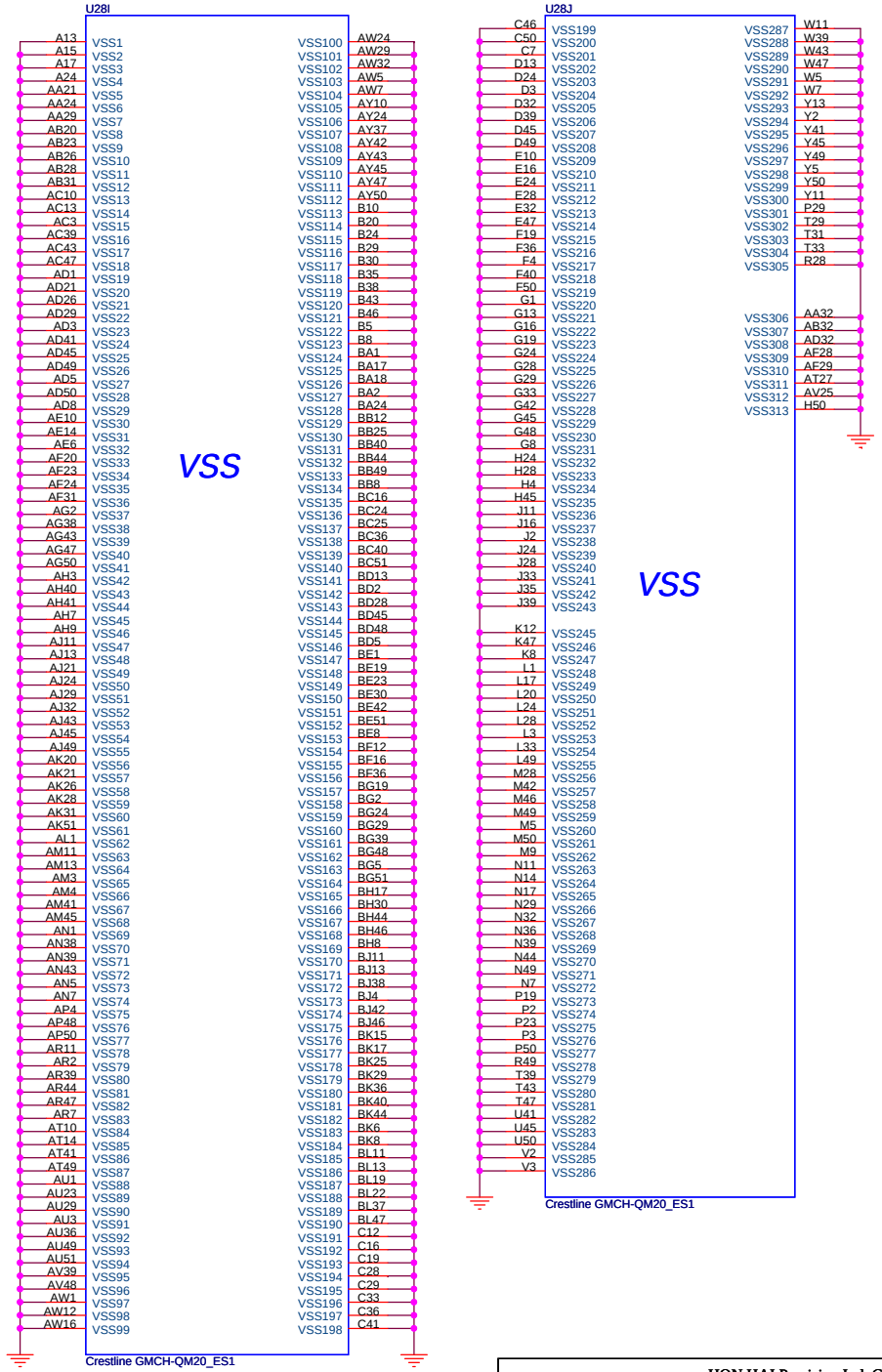
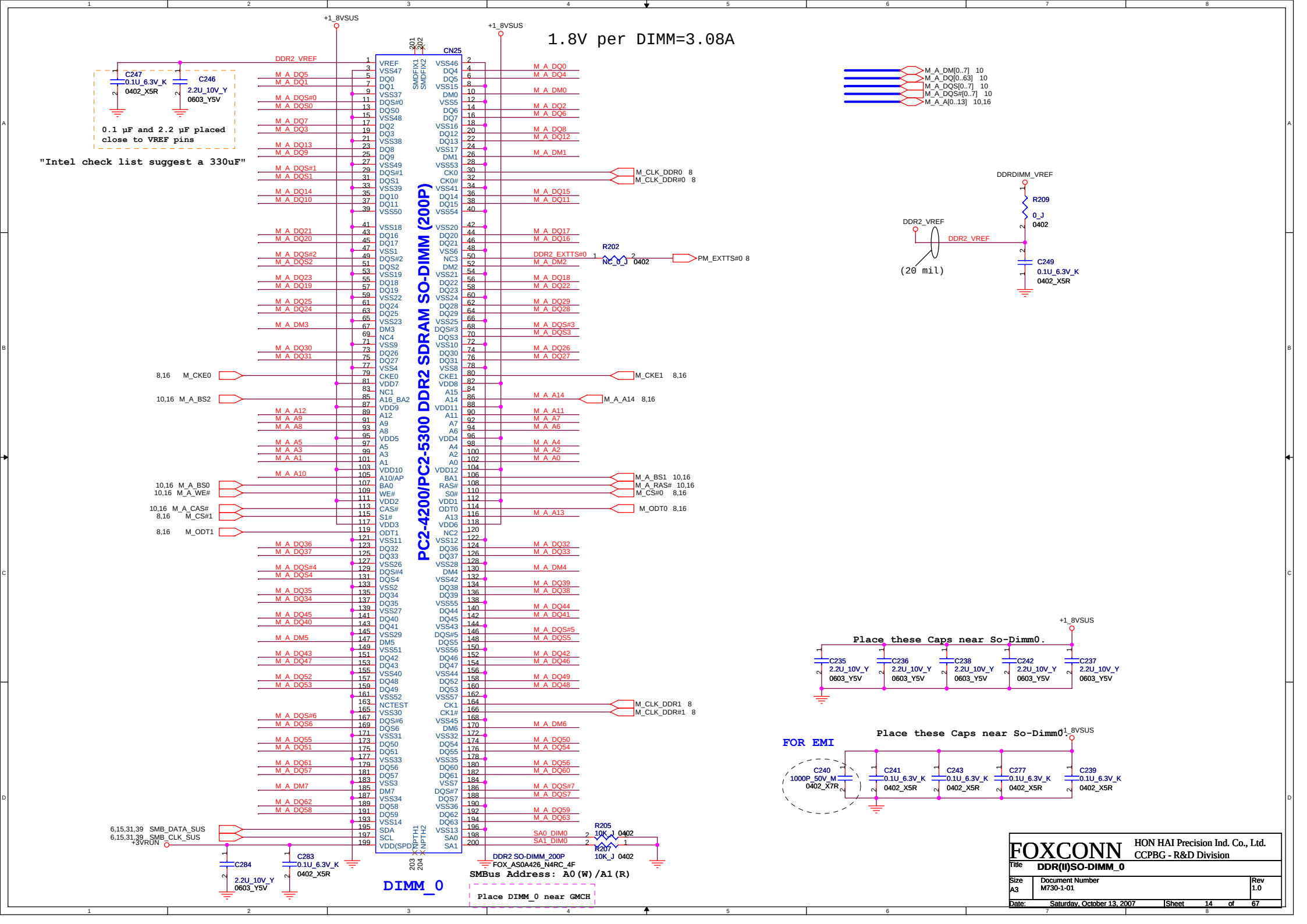


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Crestline (VCC CORE) 6/7	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 12 of 67	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Crestline (VSS) 7/7	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 13 of 67	


1.8V per DIMM=3.08A
+1_8VSUS
CN25
PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)
DDR2 SO-DIMM_200P
FOX_AS0A426_N4RC_4F
DIMM_0
SMBus Address: A0(W)/A1(R)
Place DIMM_0 near GMCH
"Intel check list suggest a 330uF"
0.1 µF and 2.2 µF placed close to VREF pins
C247 0.1U_6.3V_K 0402_X5R
C246 2.2U_10V_Y 0603_Y5V
DDR2_VREF
M_A_DM[0..7] 10
M_A_DQ[0..63] 10
M_A_DQS[0..7] 10
M_A_DQS#[0..7] 10
M_A_A[0..13] 10,16
DDRDIMM_VREF
R209 0_J 0402
C249 0.1U_6.3V_K 0402_X5R
(20 mil)
R202 NC_0_J 0402
DDR2_EXTTS#0
PM_EXTTS#0 8
M_CLK_DDR0 8
M_CLK_DDR#0 8
M_CLK_DDR1 8
M_CLK_DDR#1 8
M_CKE0 8,16
M_CKE1 8,16
M_A_BS2 10,16
M_A_A14 8,16
M_A_BS0 10,16
M_A_WE# 10,16
M_A_BS1 10,16
M_A_RAS# 10,16
M_CS#0 8,16
M_A_CAS# 10,16
M_CS#1 8,16
M_ODT0 8,16
M_ODT1 8,16
SMB_DATA_SUS 6,15,31,39
SMB_CLK_SUS 6,15,31,39
+3VRUN
SA0_DIM0
SA1_DIM0
R205 10K_J 0402
R207 10K_J 0402
C284 2.2U_10V_Y 0603_Y5V
C283 0.1U_6.3V_K 0402_X5R
Place these Caps near So-Dimm0.
C235 2.2U_10V_Y 0603_Y5V
C236 2.2U_10V_Y 0603_Y5V
C238 2.2U_10V_Y 0603_Y5V
C242 2.2U_10V_Y 0603_Y5V
C237 2.2U_10V_Y 0603_Y5V
FOR EMI
Place these Caps near So-Dimm0.
C240 1000P_50V_M 0402_X7R
C241 0.1U_6.3V_K 0402_X5R
C243 0.1U_6.3V_K 0402_X5R
C277 0.1U_6.3V_K 0402_X5R
C239 0.1U_6.3V_K 0402_X5R
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title DDR(II)SO-DIMM_0
Size A3
Document Number M730-1-01
Rev 1.0
Date: Saturday, October 13, 2007
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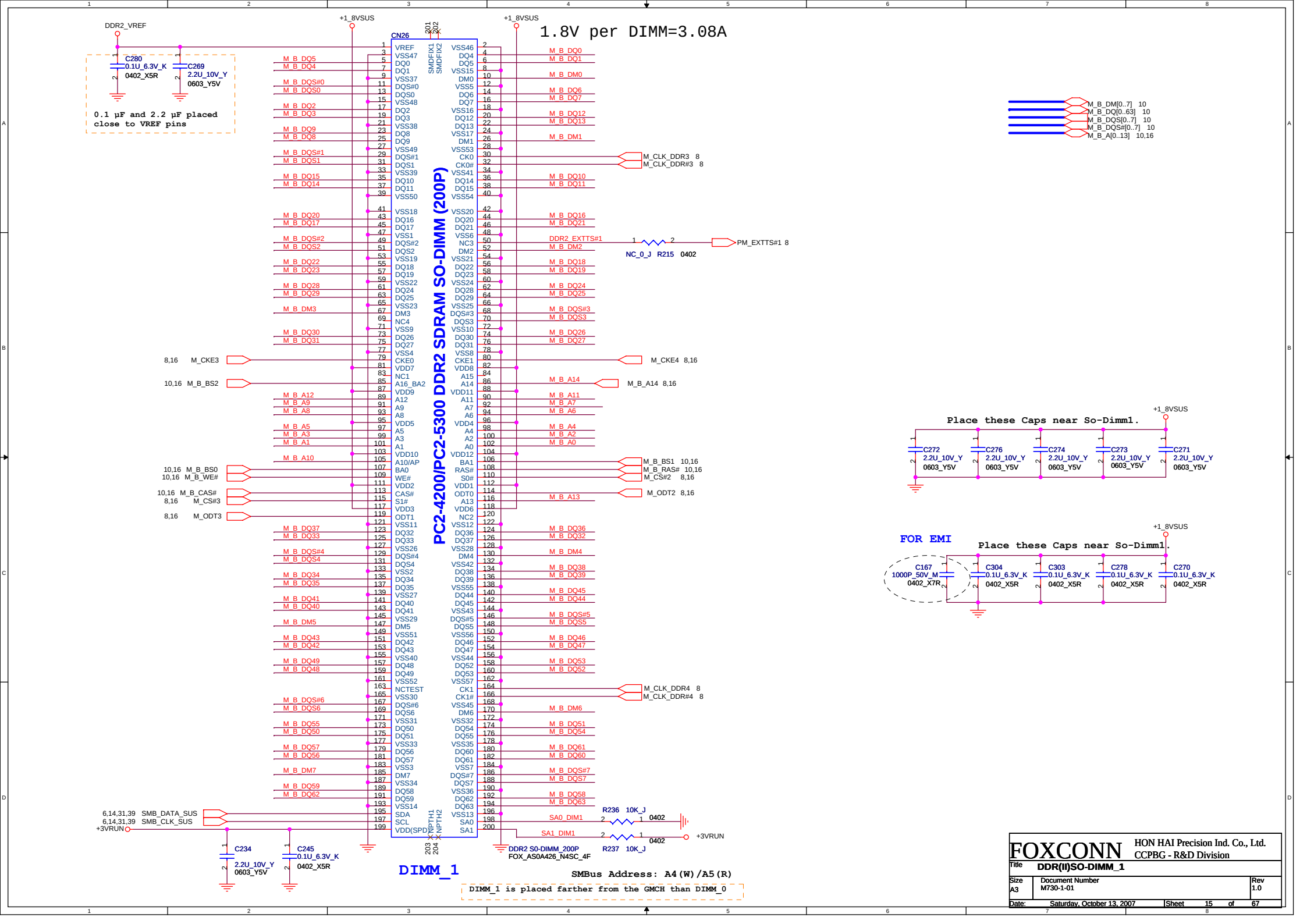
1.8V per DIMM=3.08A
DDR2_VREF
+1_8VSUS
C280 0.1U_6.3V_K 0402_X5R
C269 2.2U_10V_Y 0603_Y5V
0.1 µF and 2.2 µF placed close to VREF pins
CN26
PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)
DDR2 S0-DIMM_200P FOX_AS0A426_N4SC_4F
DIMM_1
SMBus Address: A4(W)/A5(R)
DIMM_1 is placed farther from the GMCH than DIMM_0
M_B_DM[0..7] 10
M_B_DQ[0..63] 10
M_B_DQS[0..7] 10
M_B_DQS#[0..7] 10
M_B_A[0..13] 10,16
Place these Caps near So-Dimm1.
FOR EMI
Place these Caps near So-Dimm1.
C272 2.2U_10V_Y 0603_Y5V
C276 2.2U_10V_Y 0603_Y5V
C274 2.2U_10V_Y 0603_Y5V
C273 2.2U_10V_Y 0603_Y5V
C271 2.2U_10V_Y 0603_Y5V
C167 1000P_50V_M 0402_X7R
C304 0.1U_6.3V_K 0402_X5R
C303 0.1U_6.3V_K 0402_X5R
C278 0.1U_6.3V_K 0402_X5R
C270 0.1U_6.3V_K 0402_X5R
C234 2.2U_10V_Y 0603_Y5V
C245 0.1U_6.3V_K 0402_X5R
R236 10K_J 0402
R237 10K_J 0402
NC_0_J R215 0402
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title DDR(II)SO-DIMM_1
Size A3
Document Number M730-1-01
Rev 1.0
Date: Saturday, October 13, 2007
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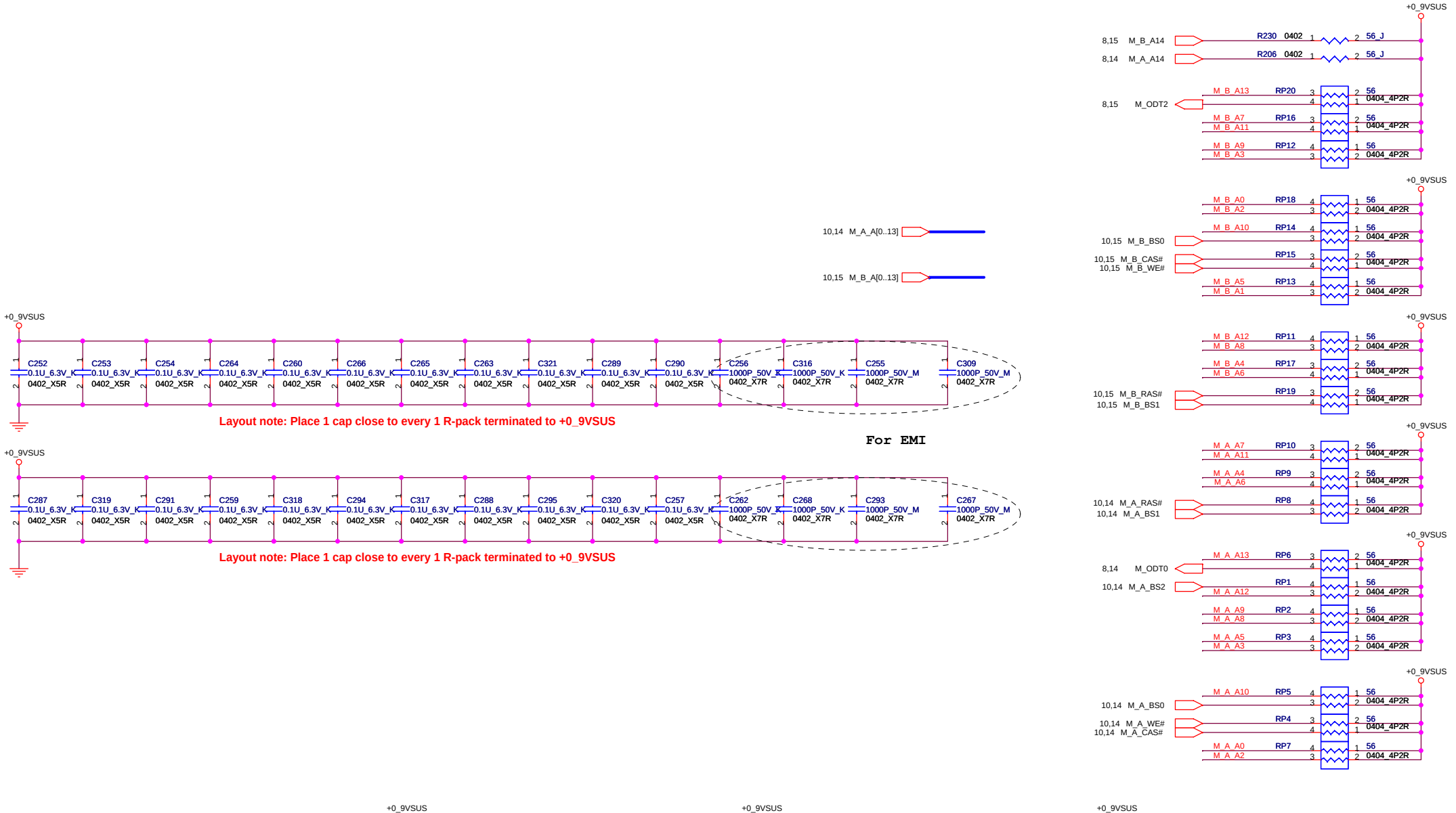
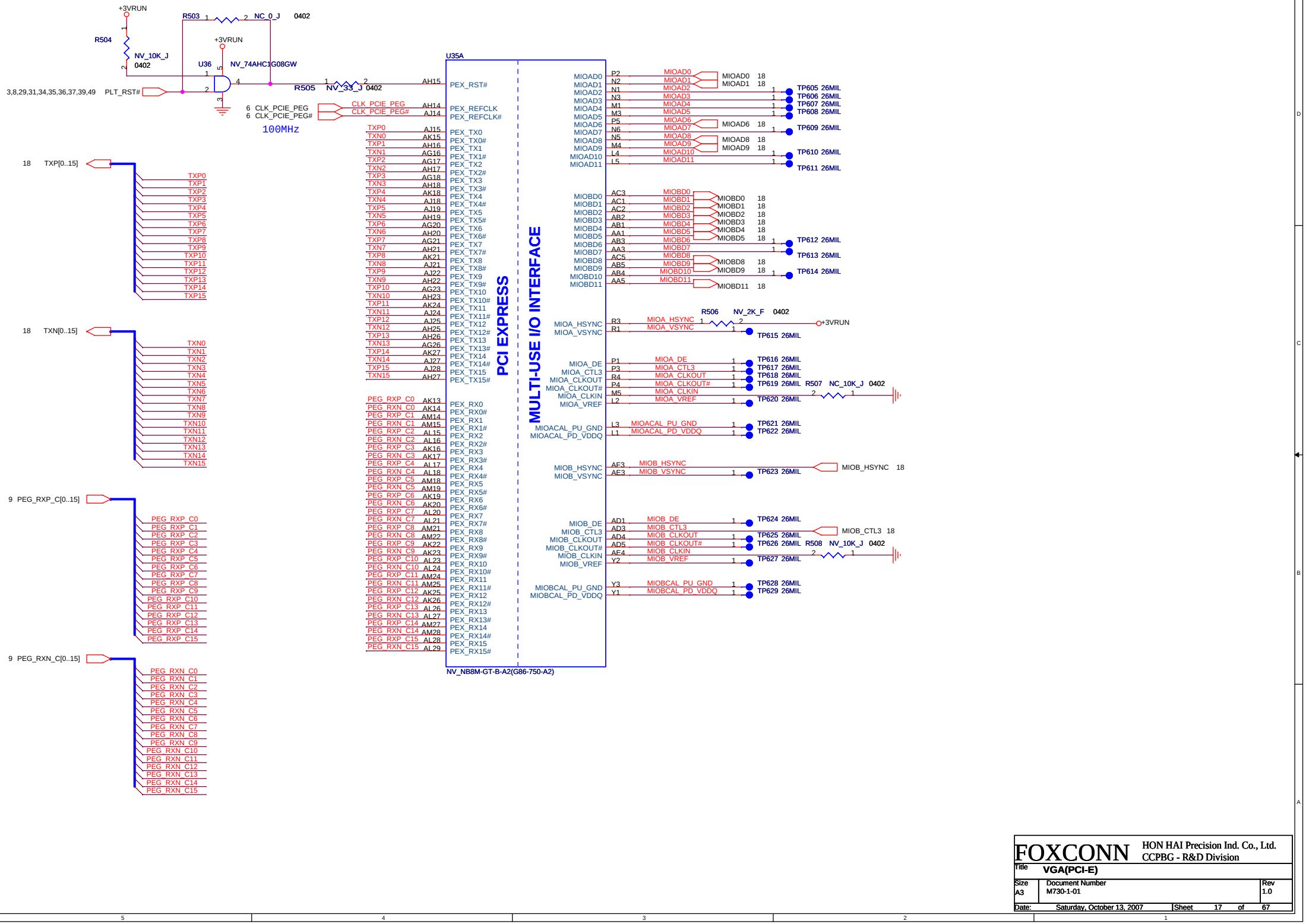


FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	DDR(II)Termination	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 16 of 67	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	VGA(PCI-E)		
Size A3	Document Number M730-1-01		Rev 1.0
Date: Saturday, October 13, 2007		Sheet 17 of 67	

SKU			
Vender	Qimonda(Infineon)	HYNIX	Samsung
Vendor PN	HYB18H512321BF-14	HY5RS123235BFP-14	K4J52324QE-BC14
H.H PN	13-HYB18H5-3003	13-HY5RS12-3001	13-K4J5232-3001
Configuration	NB8M-GT with 2pcs (16Mx32) GDDR3		
lOCATION	Stuff R511,R510 No Stuff R512,R509	Stuff R512,R509 No Stuff R511,R510	Stuff R512,R510 No Stuff R511,R509

FAE: TV Mode Strap no use, remove.
(MIOAD7, MIOAD10, MIOBD6)

+3VRUN

9 PEG_RXP[0..15]

PEG_RXP0 C544 NV_0.1U_16V_M_B 0402 TXP0
PEG_RXP1 C546 NV_0.1U_16V_M_B 0402 TXP1
PEG_RXP2 C548 NV_0.1U_16V_M_B 0402 TXP2
PEG_RXP3 C550 NV_0.1U_16V_M_B 0402 TXP3
PEG_RXP4 C552 NV_0.1U_16V_M_B 0402 TXP4
PEG_RXP5 C554 NV_0.1U_16V_M_B 0402 TXP5
PEG_RXP6 C556 NV_0.1U_16V_M_B 0402 TXP6
PEG_RXP7 C558 NV_0.1U_16V_M_B 0402 TXP7
PEG_RXP8 C560 NV_0.1U_16V_M_B 0402 TXP8
PEG_RXP9 C562 NV_0.1U_16V_M_B 0402 TXP9
PEG_RXP10 C564 NV_0.1U_16V_M_B 0402 TXP10
PEG_RXP11 C566 NV_0.1U_16V_M_B 0402 TXP11
PEG_RXP12 C568 NV_0.1U_16V_M_B 0402 TXP12
PEG_RXP13 C570 NV_0.1U_16V_M_B 0402 TXP13
PEG_RXP14 C572 NV_0.1U_16V_M_B 0402 TXP14
PEG_RXP15 C574 NV_0.1U_16V_M_B 0402 TXP15

TXP[0..15] 17

9 PEG_RXN[0..15]

PEG_RXN0 C545 NV_0.1U_16V_M_B 0402 TXN0
PEG_RXN1 C547 NV_0.1U_16V_M_B 0402 TXN1
PEG_RXN2 C549 NV_0.1U_16V_M_B 0402 TXN2
PEG_RXN3 C551 NV_0.1U_16V_M_B 0402 TXN3
PEG_RXN4 C553 NV_0.1U_16V_M_B 0402 TXN4
PEG_RXN5 C555 NV_0.1U_16V_M_B 0402 TXN5
PEG_RXN6 C557 NV_0.1U_16V_M_B 0402 TXN6
PEG_RXN7 C559 NV_0.1U_16V_M_B 0402 TXN7
PEG_RXN8 C561 NV_0.1U_16V_M_B 0402 TXN8
PEG_RXN9 C563 NV_0.1U_16V_M_B 0402 TXN9
PEG_RXN10 C565 NV_0.1U_16V_M_B 0402 TXN10
PEG_RXN11 C567 NV_0.1U_16V_M_B 0402 TXN11
PEG_RXN12 C569 NV_0.1U_16V_M_B 0402 TXN12
PEG_RXN13 C571 NV_0.1U_16V_M_B 0402 TXN13
PEG_RXN14 C573 NV_0.1U_16V_M_B 0402 TXN14
PEG_RXN15 C575 NV_0.1U_16V_M_B 0402 TXN15

TXN[0..15] 17

Strap for GDDR3-136ball
1001 16Mx32 (64-bits) Qimonda
1010 16Mx32 (64-bits) Hynix
1011 16Mx32 (64-bits) Samsung_E-die

SUBVENDOR
0 (USE SYSTEM BIOS)
1 (USE EXTERNAL ROM)

MIOAD0 is used to set the PCI Express PLL termination enable.
DEFAULT "0"

3GIO_PADCFG[3:0]
-> 0001 for Mobile

NB8M-GT
PCI_DEVID[4:0]= "00110" -> 6
NB8M-GS
PCI_DEVID[4:0]= "00111" -> 7
NB8M-SE
PCI_DEVID[4:0]= "01000" -> 8

RAM_CFG0 R509 NC_2K_J 0402 MIOBD0 R510 NV_2K_J 0402
RAM_CFG1 R511 NV_2K_J 0402 MIOBD1 R512 NC_2K_J 0402
RAM_CFG2 R513 NV_2K_J 0402 MIOBD8 R514 NC_2K_J 0402
RAM_CFG3 R515 NC_2K_J 0402 MIOBD9 R516 NV_2K_J 0402

SUBVENDOR R517 NV_2K_J 0402 MIOAD1 MIOAD1 17

PEX_PLL_EN_TERM R518 NV_2K_J 0402 MIOAD0 MIOAD0 17

3GIO_PADCFG0 R519 NC_2K_J 0402 MIOAD6 R520 NV_2K_J 0402
3GIO_PADCFG1 R521 NV_2K_J 0402 MIOAD8 R522 NC_2K_J 0402
3GIO_PADCFG2 R523 NV_2K_J 0402 MIOAD9 R524 NC_2K_J 0402
3GIO_PADCFG3 R525 NV_2K_J 0402 MIOB_HSYNC R526 NC_2K_J 0402

PCI_DEVID_0 R527 NV_2K_J 0402 MIOBD4 R528 NC_2K_J 0402
PCI_DEVID_1 R529 NC_2K_J 0402 MIOBD5 R530 NV_2K_J 0402
PCI_DEVID_2 R531 NC_2K_J 0402 MIOBD3 R532 NV_2K_J 0402
PCI_DEVID_3 R533 NV_2K_J 0402 MIOBD11 R534 NC_2K_J 0402
PCI_DEVID_4 R535 NV_2K_J 0402 MIOB_CTL3 R536 NC_2K_J 0402

CRYSTAL R537 NV_2K_J 0402 MIOBD2 MIOBD2 17

MIOBD2	Crystal
0	27MHz (Default)
1	Reserved

MIOAD6 MIOAD6 17
MIOAD8 MIOAD8 17
MIOAD9 MIOAD9 17

MIOBD0 MIOBD0 17
MIOBD1 MIOBD1 17
MIOBD3 MIOBD3 17
MIOBD4 MIOBD4 17
MIOBD5 MIOBD5 17
MIOBD8 MIOBD8 17
MIOBD9 MIOBD9 17
MIOBD11 MIOBD11 17

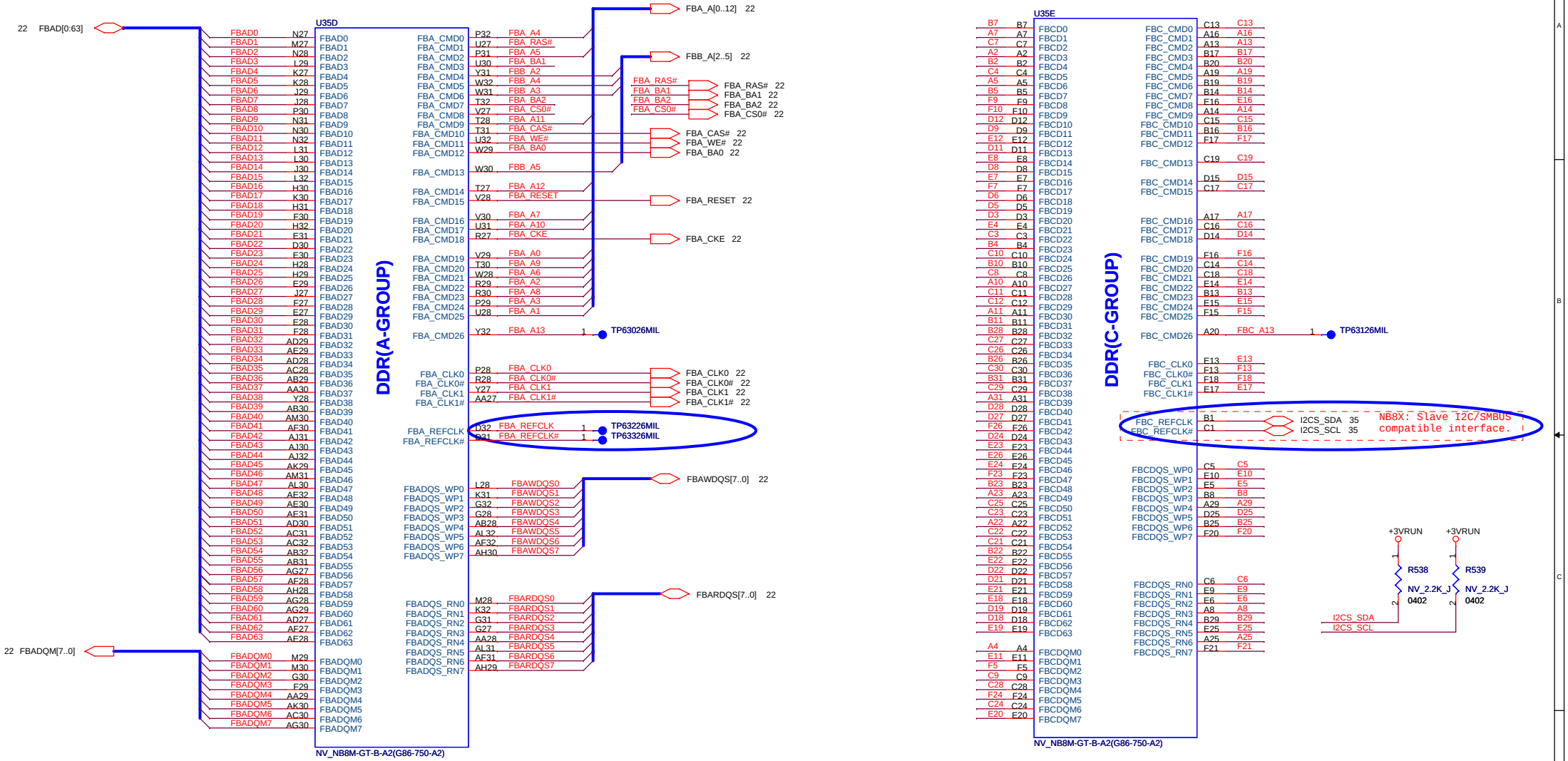
MIOB_CTL3 MIOB_CTL3 17
MIOB_HSYNC MIOB_HSYNC 17

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

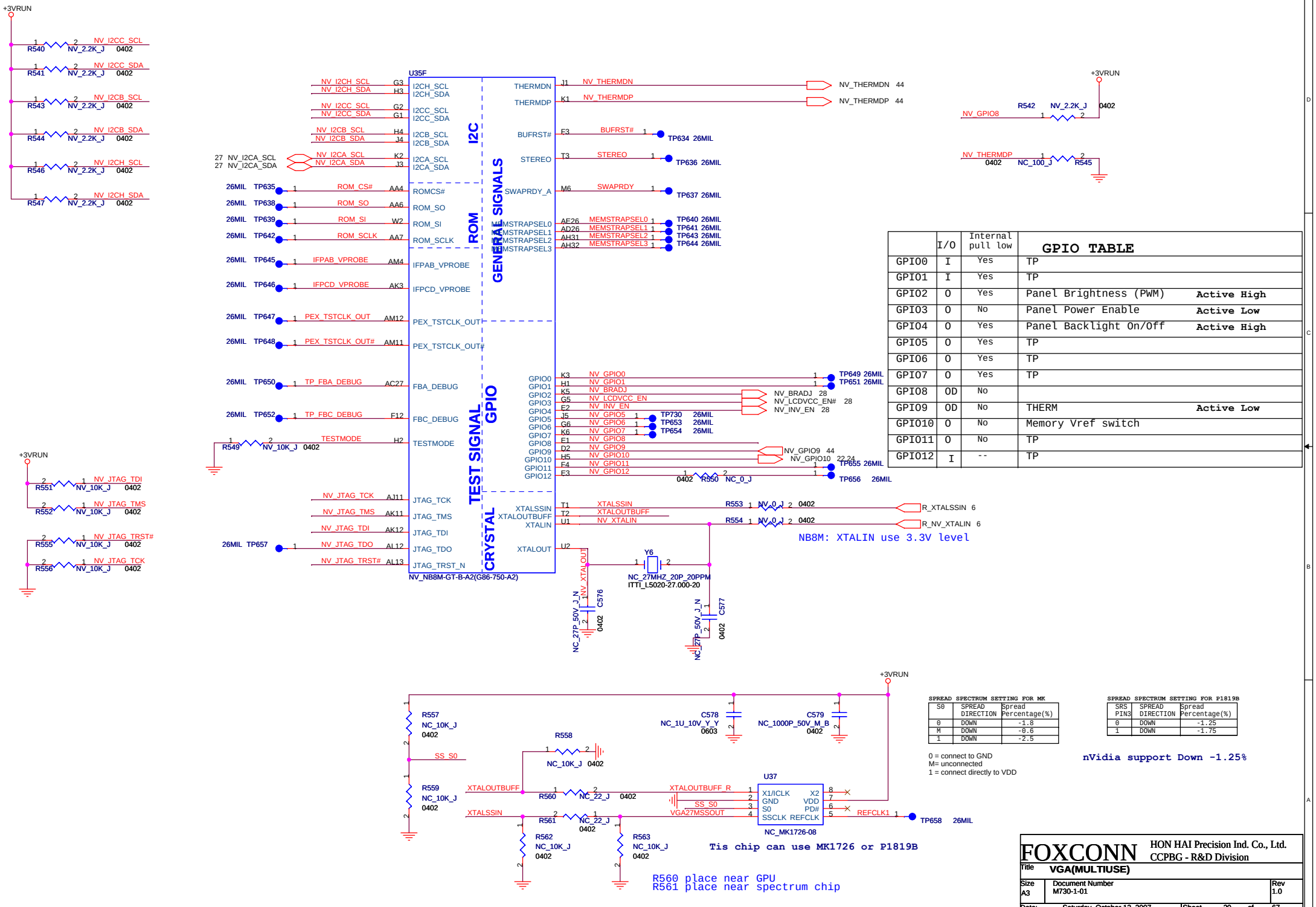
Title VGA(STRAP)

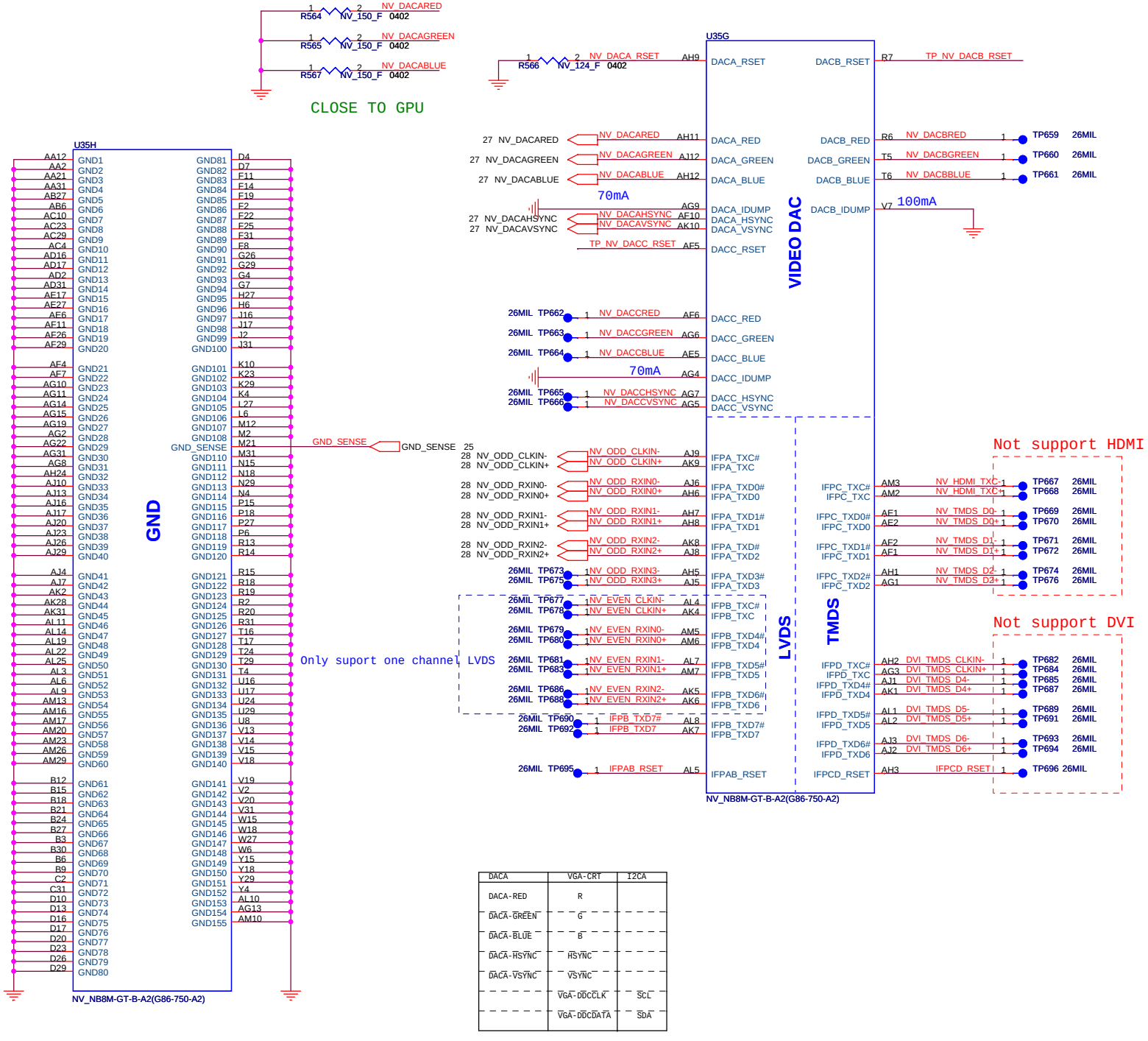
Size A3 | Document Number M730-1-01 | Rev 1.0

Date: Saturday, October 13, 2007 | Sheet 18 of 67



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VGA(GDDR)#	
Size A3	Document Number M730-1-011	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 19 of 67	


+3VRUN
R540 NV_2.2K_J 0402 NV_I2CC_SCL
R541 NV_2.2K_J 0402 NV_I2CC_SDA
R543 NV_2.2K_J 0402 NV_I2CB_SCL
R544 NV_2.2K_J 0402 NV_I2CB_SDA
R546 NV_2.2K_J 0402 NV_I2CH_SCL
R547 NV_2.2K_J 0402 NV_I2CH_SDA
U35F
I2C
ROM
GENERAL SIGNALS
GPIO
TEST SIGNAL
CRYSTAL
NV_I2CH_SCL G3
NV_I2CH_SDA H3
NV_I2CC_SCL G2
NV_I2CC_SDA G1
NV_I2CB_SCL H4
NV_I2CB_SDA J4
NV_I2CA_SCL K2
NV_I2CA_SDA J3
27 NV_I2CA_SCL
27 NV_I2CA_SDA
26MIL TP635 ROM_CS# AA4
26MIL TP638 ROM_SO AA6
26MIL TP639 ROM_SI W2
26MIL TP642 ROM_SCLK AA7
26MIL TP645 IFPAB_VPROBE AM4
26MIL TP646 IFPCD_VPROBE AK3
26MIL TP647 PEX_TSTCLK_OUT AM12
26MIL TP648 PEX_TSTCLK_OUT# AM11
26MIL TP650 TP_FBA_DEBUG AC27
26MIL TP652 TP_FBC_DEBUG F12
R549 NV_10K_J 0402 TESTMODE H2
NV_JTAG_TCK AJ11
NV_JTAG_TMS AK11
NV_JTAG_TDI AK12
26MIL TP657 NV_JTAG_TDO AL12
NV_JTAG_TRST# AL13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST_N
NV_NB8M-GT-B-A2(G86-750-A2)
THERMDN J1 NV_THERMDN
THERMDP K1 NV_THERMDP
NV_THERMDN 44
NV_THERMDP 44
BUFRST# F3 BUFRST# 1 TP634 26MIL
STEREO T3 STEREO 1 TP636 26MIL
SWAPRDY_A M6 SWAPRDY 1 TP637 26MIL
MEMSTRAPSEL0 AE26 MEMSTRAPSEL0 1 TP640 26MIL
MEMSTRAPSEL1 AD26 MEMSTRAPSEL1 1 TP641 26MIL
MEMSTRAPSEL2 AH31 MEMSTRAPSEL2 1 TP643 26MIL
MEMSTRAPSEL3 AH32 MEMSTRAPSEL3 1 TP644 26MIL
GPIO0 K3 NV_GPIO0 1 TP649 26MIL
GPIO1 H1 NV_GPIO1 1 TP651 26MIL
GPIO2 K5 NV_BRADJ NV_BRADJ 28
GPIO3 G5 NV_LCDVCC_EN NV_LCDVCC_EN# 28
GPIO4 E2 NV_INV_EN NV_INV_EN 28
GPIO5 J5 NV_GPIO5 1 TP730 26MIL
GPIO6 G6 NV_GPIO6 1 TP653 26MIL
GPIO7 K6 NV_GPIO7 1 TP654 26MIL
GPIO8 E1 NV_GPIO8
GPIO9 D2 NV_GPIO9 NV_GPIO9 44
GPIO10 H5 NV_GPIO10 NV_GPIO10 22,24
GPIO11 F4 NV_GPIO11 1 TP655 26MIL
GPIO12 E3 NV_GPIO12 1 TP656 26MIL
0402 R550 NC_0_J
XTALSSIN T1 XTALSSIN
XTALOUTBUFF T2 XTALOUTBUFF
XTALIN U1 NV_XTALIN
XTALOUT U2 NV_XTALOUT
R553 1 NV_0_J 2 0402 R_XTALSSIN 6
R554 1 NV_0_J 2 0402 R_NV_XTALIN 6
NB8M: XTALIN use 3.3V level
Y6
NC_27MHZ_20P_20PPM
ITTI_L5020-27.000-20
NC_27P_50V_J_N C576 0402
NC_27P_50V_J_N C577 0402
+3VRUN
R542 NV_2.2K_J 0402 NV_GPIO8
NV_THERMDP 0402 NC_100_J R545
GPIO TABLE
GPIO0 I Yes TP
GPIO1 I Yes TP
GPIO2 O Yes Panel Brightness (PWM) Active High
GPIO3 O No Panel Power Enable Active Low
GPIO4 O Yes Panel Backlight On/Off Active High
GPIO5 O Yes TP
GPIO6 O Yes TP
GPIO7 O Yes TP
GPIO8 OD No
GPIO9 OD No THERM Active Low
GPIO10 O No Memory Vref switch
GPIO11 O No TP
GPIO12 I -- TP
+3VRUN
R551 NV_10K_J 0402 NV_JTAG_TDI
R552 NV_10K_J 0402 NV_JTAG_TMS
R555 NV_10K_J 0402 NV_JTAG_TRST#
R556 NV_10K_J 0402 NV_JTAG_TCK
+3VRUN
R557 NC_10K_J 0402
SS_S0
R559 NC_10K_J 0402
R558 NC_10K_J 0402
C578 NC_1U_10V_Y_Y 0603
C579 NC_1000P_50V_M_B 0402
XTALOUTBUFF
R560 NC_22_J 0402
XTALSSIN
R561 NC_22_J 0402
R562 NC_10K_J 0402
R563 NC_10K_J 0402
U37
X1/ICLK X2
GND VDD
S0 PD#
SSCLK REFCLK
XTALOUTBUFF_R
SS_S0
VGA27MSSOUT
NC_MK1726-08
REFCLK1 TP658 26MIL
Tis chip can use MK1726 or P1819B
R560 place near GPU
R561 place near spectrum chip
SPREAD SPECTRUM SETTING FOR MK
S0 | SPREAD DIRECTION | Spread Percentage(%)
0 DOWN -1.8
M DOWN -0.6
1 DOWN -2.5
0 = connect to GND
M= unconnected
1 = connect directly to VDD
SPREAD SPECTRUM SETTING FOR P1819B
SRS PIN3 | SPREAD DIRECTION | Spread Percentage(%)
0 DOWN -1.25
1 DOWN -1.75
nVidia support Down -1.25%
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title VGA(MULTIUSE)
Size A3
Document Number M730-1-01
Rev 1.0
Date: Saturday, October 13, 2007
Sheet 20 of 67



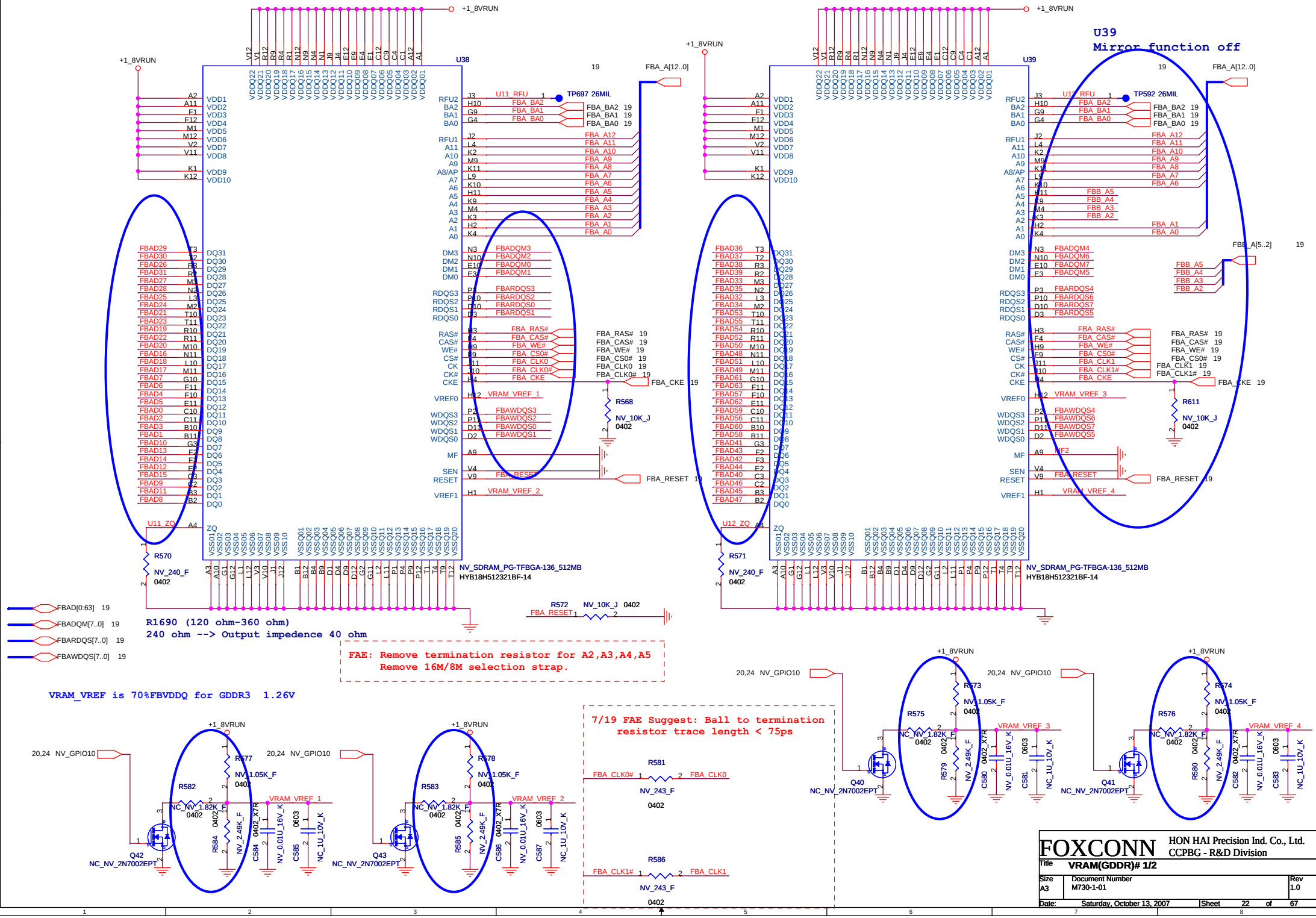
DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDATA	SDA

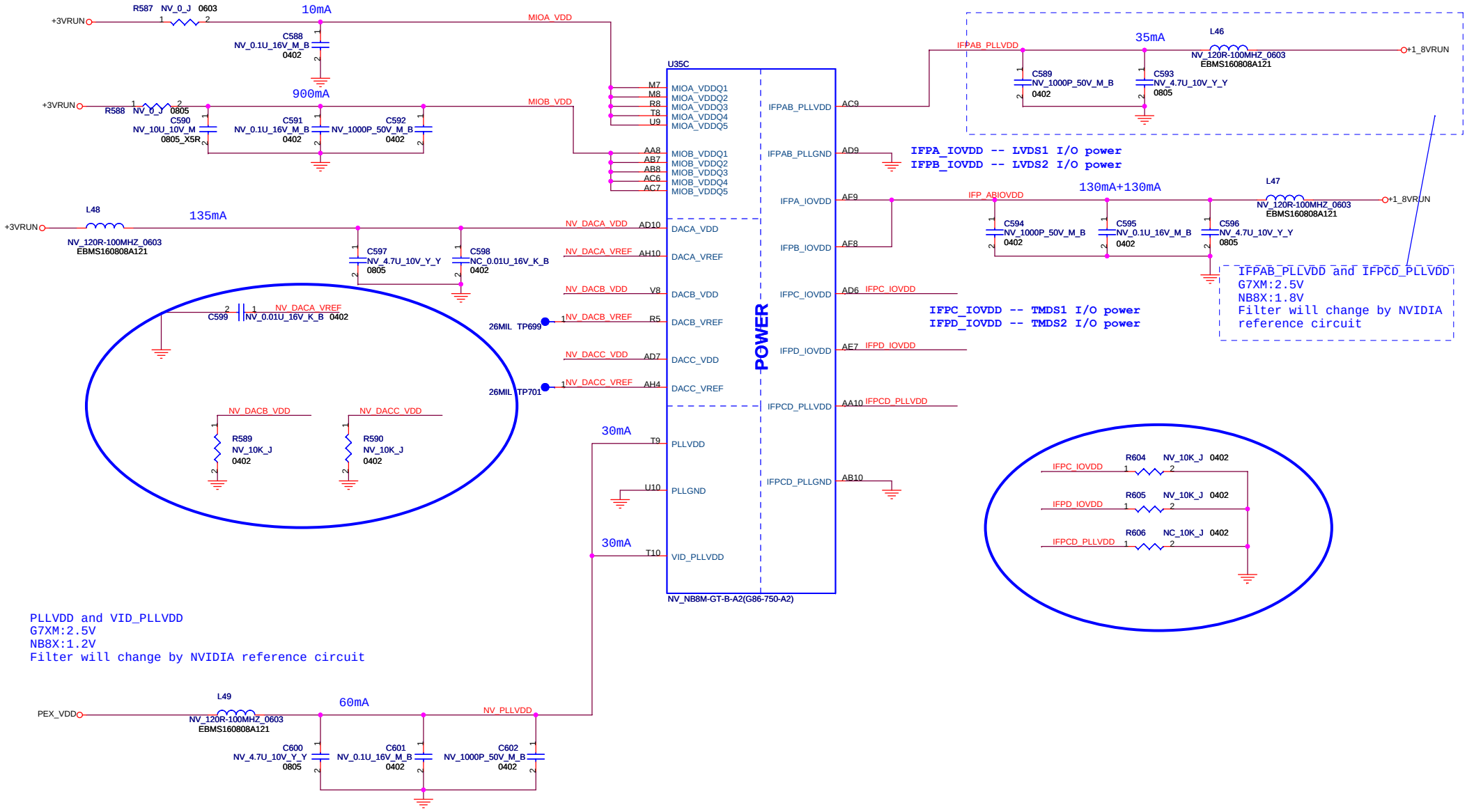
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: VGA(LVD/VDAC)

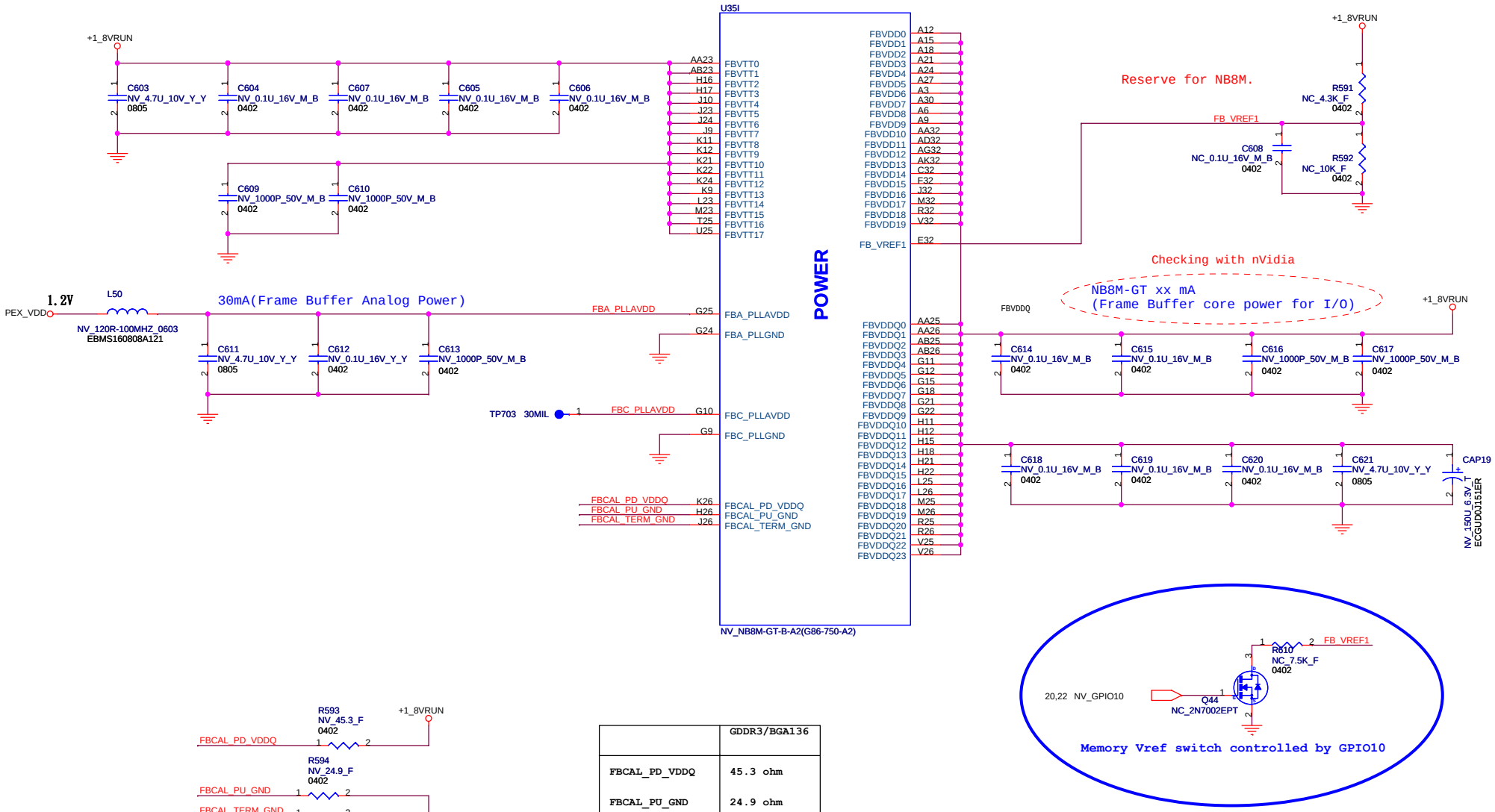
Size: A3 | Document Number: M730-1-01 | Rev: 1.0

Date: Saturday, October 13, 2007 | Sheet 21 of 67


U38
U39
Mirror function off
+1_8VRUN
NV_SDRAM_PG-TFBGA-136_512MB
HYB18H512321BF-14
R1690 (120 ohm-360 ohm)
240 ohm --> Output impedence 40 ohm
FAE: Remove termination resistor for A2,A3,A4,A5
Remove 16M/8M selection strap.
VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V
7/19 FAE Suggest: Ball to termination
resistor trace length < 75ps
TP697 26MIL
TP592 26MIL
FBAD[0:63] 19
FBADQM[7..0] 19
FBARDQS[7..0] 19
FBAWDQS[7..0] 19
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title VRAM(GDDR)# 1/2
Size A3
Document Number M730-1-01
Rev 1.0
Date: Saturday, October 13, 2007
Sheet 22 of 67



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VGA(POWER) 1/3	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 23 of 67	



	GDDR3/BGA136
FBCAL_PD_VDDQ	45.3 ohm
FBCAL_PU_GND	24.9 ohm
FBCAL_TERM_GND	40.2 ohm

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	VGA(POWER) 2/3
Size A3	Document Number M730-1-01
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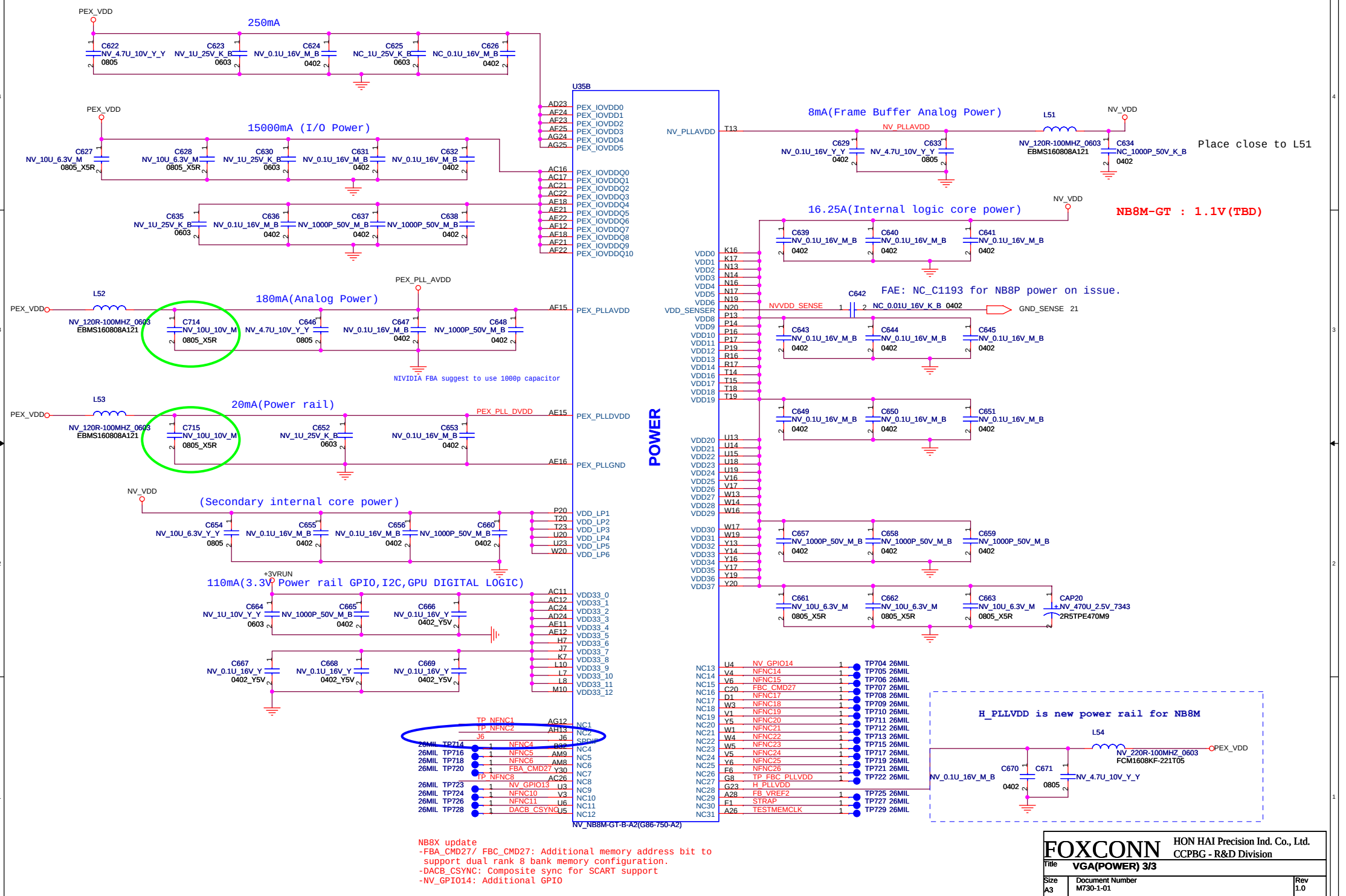
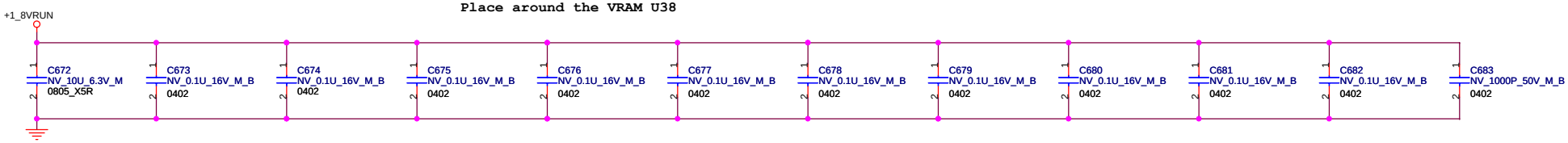
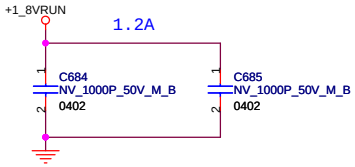
Date:	Saturday, October 13, 2007
Sheet	24 of 67

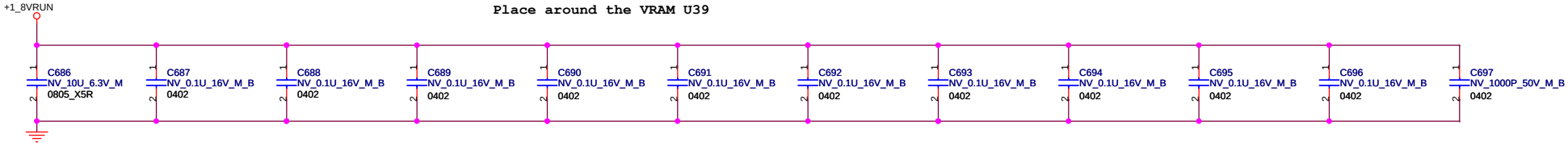

250mA
15000mA (I/O Power)
180mA(Analog Power)
20mA(Power rail)
(Secondary internal core power)
110mA(3.3V Power rail GPIO,I2C,GPU DIGITAL LOGIC)
8mA(Frame Buffer Analog Power)
16.25A(Internal logic core power)
NB8M-GT : 1.1V(TBD)
FAE: NC_C1193 for NB8P power on issue.
Place close to L51
NIVIDIA FBA suggest to use 1000p capacitor
H_PLLVDD is new power rail for NB8M
POWER
U35B
NV_NB8M-GT-B-A2(G86-750-A2)
NB8X update
-FBA_CMD27/ FBC_CMD27: Additional memory address bit to support dual rank 8 bank memory configuration.
-DACB_CSYNC: Composite sync for SCART support
-NV_GPIO14: Additional GPIO
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title VGA(POWER) 3/3
Size A3
Document Number M730-1-01
Rev 1.0
Date: Wednesday, October 17, 2007
Sheet 25 of 67

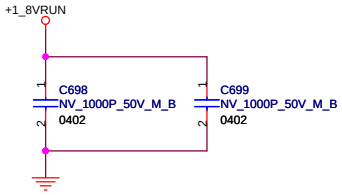
Place around the VRAM U38





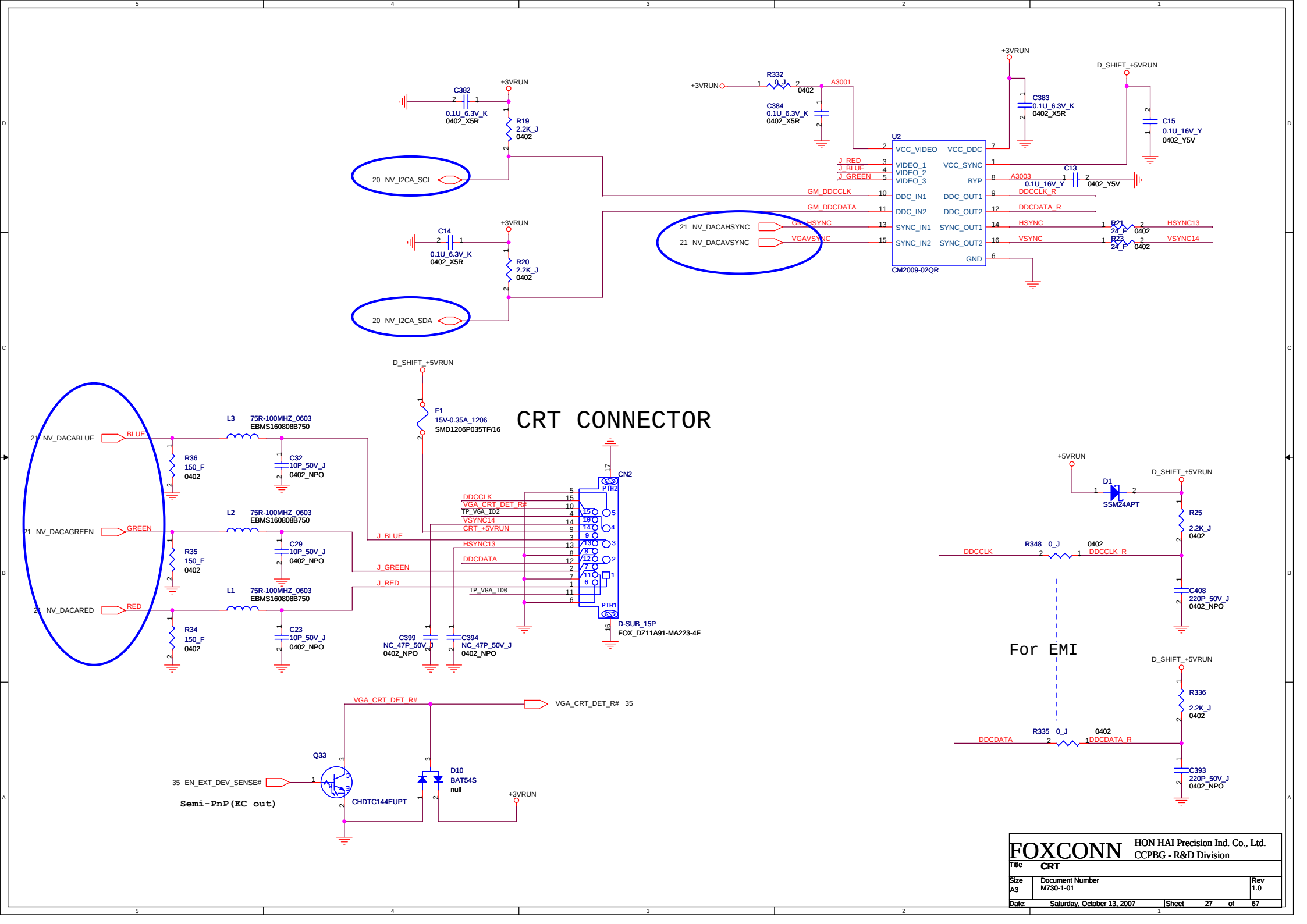
Place around the VRAM U39





FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	VRAM(BYPASS) 2/2	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 26 of 67	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: CRT		
Size: A3	Document Number: M730-1-01	Rev: 1.0
Date: Saturday, October 13, 2007	Sheet 27 of 67	

LVDS

ODD_CLKIN-
ODD_CLKIN+
NV_ODD_CLKIN- 21
NV_ODD_CLKIN+ 21

ODD_RXIN0-
ODD_RXIN0+
NV_ODD_RXIN0- 21
NV_ODD_RXIN0+ 21

ODD_RXIN1-
ODD_RXIN1+
NV_ODD_RXIN1- 21
NV_ODD_RXIN1+ 21

ODD_RXIN2-
ODD_RXIN2+
NV_ODD_RXIN2- 21
NV_ODD_RXIN2+ 21

DCBATOUT

For EMI mount.

C376 0.1U_50V_K 0603_X7R
C373 1U_25V_Y 0805_Y5V
C377 0.1U_50V_K 0603_X7R

Place C375 and C373 close to CN14.

DCBATOUT
L55 600R-100MHZ_0805 ACMS201209A601 2A

C375 0.1U_50V_K 0603_X7R
DCBATOUT_1
2A
CN14

20 NV_BRADJ
INV_ENABLE
INV_BRADJ

R3 10K_J 0402
R326 10K_J 0402

B TO B HEADER CONN_6P
FOX_HS8106E

INVERTER CONN.

CN18
LCDVCC
LCDVCC
ODD_RXIN1-
ODD_RXIN1+
ODD_RXIN0-
ODD_RXIN0+
ODD_RXIN2+
ODD_RXIN2-
ODD_CLKIN-
ODD_CLKIN+

C380 0.1U_10V_K 0402_X5R

FOX_HT1310F
HEADER CONN_20P

U1 74AHC1G08GW
+3VRUN
31 INV_EN_EC
INV_ENABLE
INV_ENABLE_1

U22 74AHC1G08GW
+3VRUN
35,51 LIDIN#
20 NV_INV_EN

R328 10K_J 0402

SW1
LCDID0 31
LCDID1 31
LCDID2 31
LCDID3 31
HDS404-E_SW-SLIDE

PANEL ID

Type	WXGA	WXGA	WXGA	WXGA
Size	15.4"W	15.4"W	15.4"W	15.4"W
Vendor	AUO	CPT	LPL	AUO
Device Name	B154EW02V7	CLAA154WB05AN	LP154WX4-TLC5	QD15TL0703
Panel ID Check[3..0]	0001	0010	0011	0100

R612 NC_0_J 0402
+3VRUN
R596 2K_J 0402
U40 74AHC1G14GW
20 NV_LCDVCC_EN#

+3VRUN
C378 4.7U_6.3V_K 0805_X5R
U23 G5281RC1U_V0.1
IN1 IN2 IN3 IN4 IN5 EN GND THERMAL PAD OUT
+3VRUN

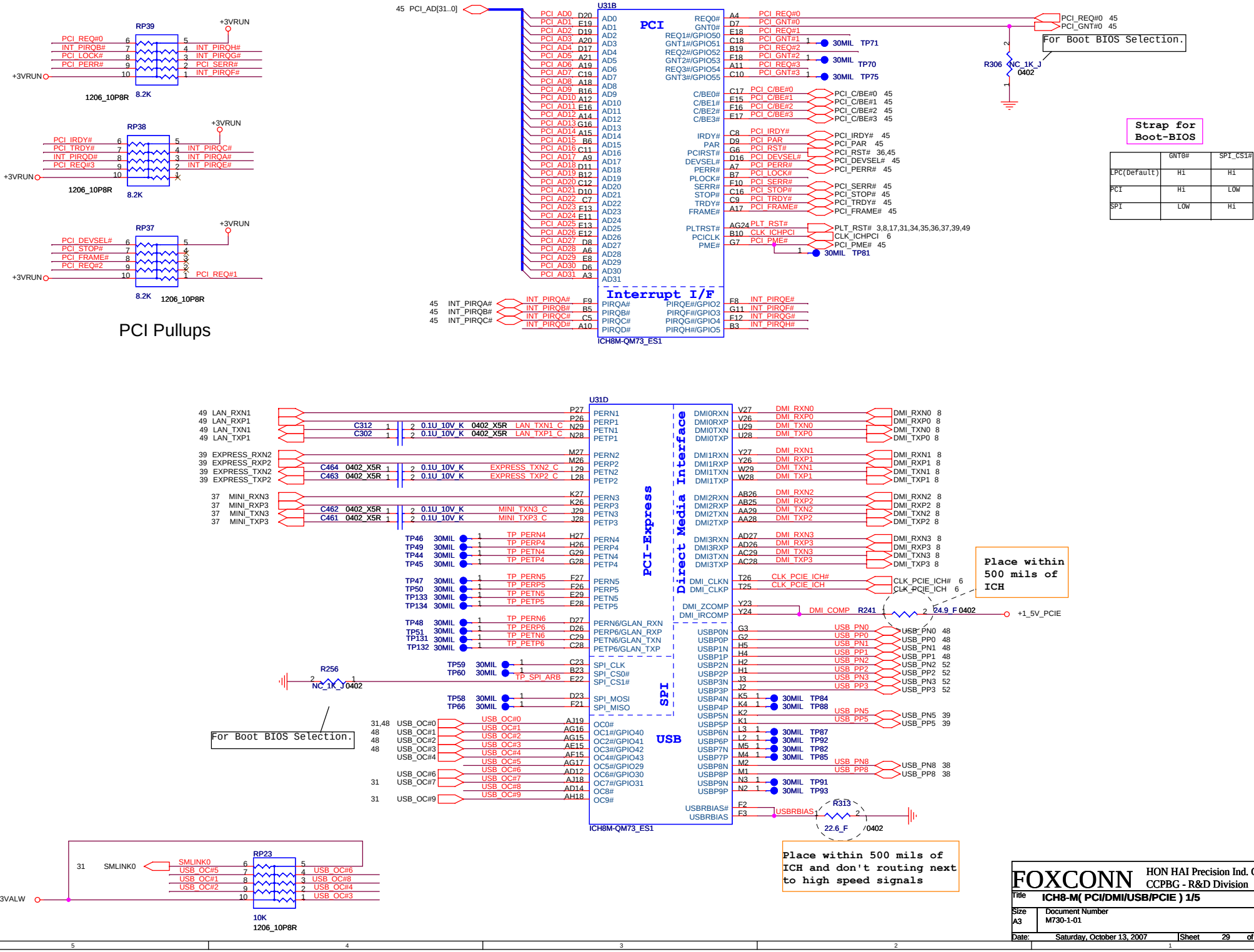
C702 0402 0.1U_16V_Y_Y
R329 100K_J 0402

LCDVCC
C381 4.7U_10V_K 0805_X5R
C379 0.1U_16V_Y 0402_Y5V
R597 200_J 0603

The R597 will consume about 0.054 Watt (3.3x3.3/200 = 0.054W). We changed resistor to 0603 size (1/8 Watt)

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	LVDS		
Size A3	Document Number M730-1-01		Rev 1.0
Date: Saturday, October 13, 2007	Sheet 28 of 67		


RP39
+3VRUN
PCI_REQ#0
INT_PIRQB#
PCI_LOCK#
PCI_PERR#
INT_PIRQH#
INT_PIRQG#
PCI_SERR#
INT_PIRQF#
1206_10P8R
8.2K
RP38
PCI_IRDY#
PCI_TRDY#
INT_PIRQD#
PCI_REQ#3
INT_PIRQC#
INT_PIRQA#
INT_PIRQE#
RP37
PCI_DEVSEL#
PCI_STOP#
PCI_FRAME#
PCI_REQ#2
PCI_REQ#1
PCI Pullups
45 PCI_AD[31..0]
U31B
PCI
Interrupt I/F
ICH8M-QM73_ES1
PCI_REQ#0 45
PCI_GNT#0 45
For Boot BIOS Selection.
R306
NC_1K_J
0402
Strap for Boot-BIOS
GNT0#
SPI_CS1#
LPC(Default)
PCI
SPI
45 INT_PIRQA#
45 INT_PIRQB#
45 INT_PIRQC#
U31D
PCI-Express
Direct Media Interface
SPI
USB
49 LAN_RXN1
49 LAN_RXP1
49 LAN_TXN1
49 LAN_TXP1
C312
C302
0.1U_10V_K
0402_X5R
LAN_TXN1_C
LAN_TXP1_C
39 EXPRESS_RXN2
39 EXPRESS_RXP2
39 EXPRESS_TXN2
39 EXPRESS_TXP2
C464
C463
EXPRESS_TXN2_C
EXPRESS_TXP2_C
37 MINI_RXN3
37 MINI_RXP3
37 MINI_TXN3
37 MINI_TXP3
C462
C461
MINI_TXN3_C
MINI_TXP3_C
TP46 TP49 TP44 TP45
TP47 TP50 TP133 TP134
TP48 TP51 TP131 TP132
TP59 TP60
TP58 TP66
TP_SPI_ARB
R256
NC_1K_J0402
For Boot BIOS Selection.
31,48 USB_OC#0
48 USB_OC#1
48 USB_OC#2
48 USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
31 USB_OC#7
USB_OC#8
31 USB_OC#9
DMI_RXN0 8
DMI_RXP0 8
DMI_TXN0 8
DMI_TXP0 8
DMI_RXN1 8
DMI_RXP1 8
DMI_TXN1 8
DMI_TXP1 8
DMI_RXN2 8
DMI_RXP2 8
DMI_TXN2 8
DMI_TXP2 8
DMI_RXN3 8
DMI_RXP3 8
DMI_TXN3 8
DMI_TXP3 8
Place within 500 mils of ICH
CLK_PCIE_ICH# 6
CLK_PCIE_ICH 6
DMI_COMP R241 24.9_F 0402
+1_5V_PCIE
USB_PN0 48
USB_PP0 48
USB_PN1 48
USB_PP1 48
USB_PN2 52
USB_PP2 52
USB_PN3 52
USB_PP3 52
USB_PN5 39
USB_PP5 39
USB_PN8 38
USB_PP8 38
R313
22.6_F /0402
Place within 500 mils of ICH and don't routing next to high speed signals
RP23
31 SMLINK0
+3VALW
10K
1206_10P8R
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
ICH8-M(PCI/DMI/USB/PCIE) 1/5
Size
A3
Document Number
M730-1-01
Rev
1.0
Date:
Saturday, October 13, 2007
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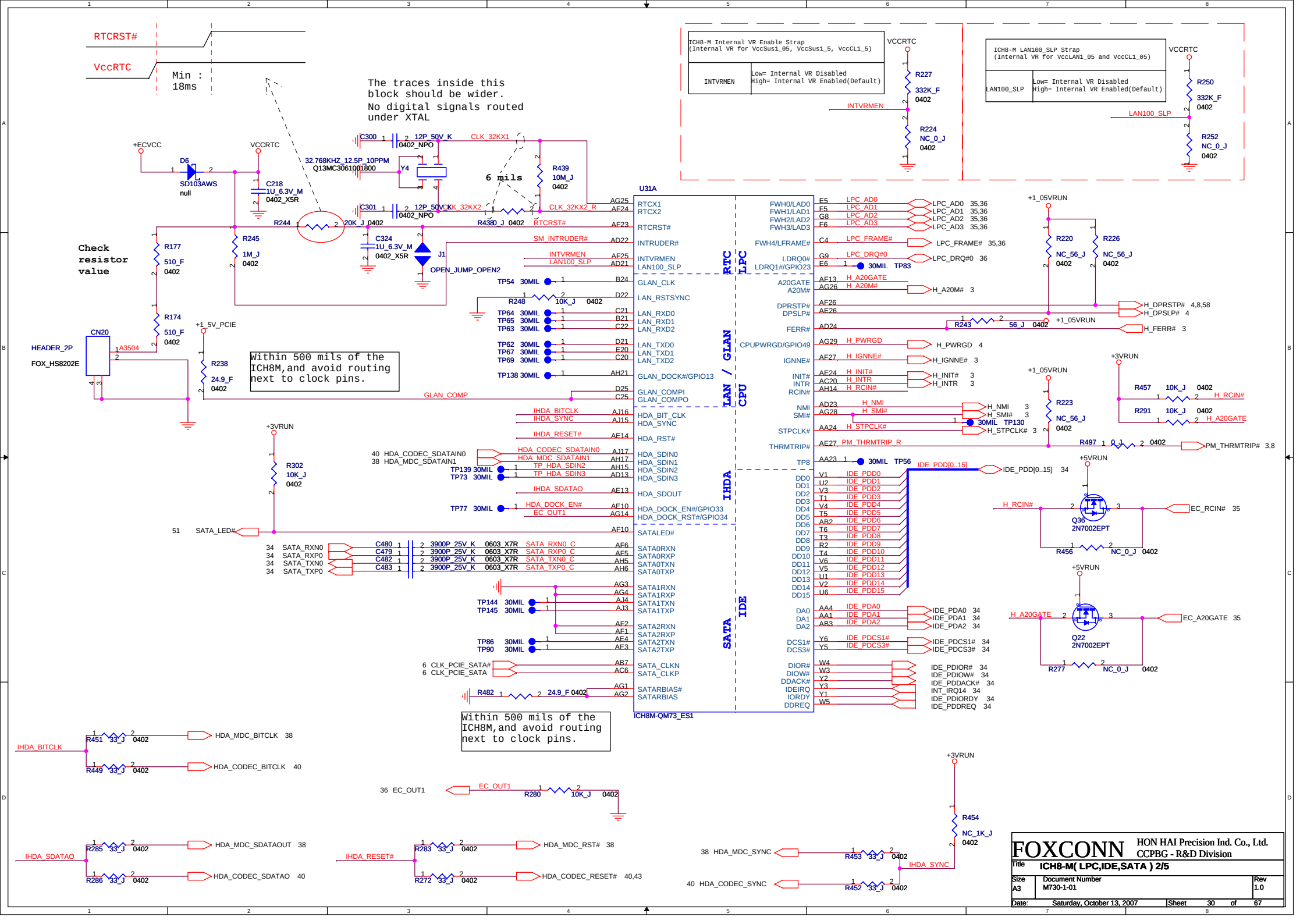
RTCRST#
VccRTC
Min : 18ms
The traces inside this block should be wider.
No digital signals routed under XTAL
ICH8-M Internal VR Enable Strap (Internal VR for VccSus1_05, VccSus1_5, VccCL1_5)
INTVRMEN
Low= Internal VR Disabled
High= Internal VR Enabled(Default)
ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1_05)
LAN100_SLP
Low= Internal VR Disabled
High= Internal VR Enabled(Default)
Check resistor value
Within 500 mils of the ICH8M,and avoid routing next to clock pins.
Within 500 mils of the ICH8M,and avoid routing next to clock pins.
U31A
ICH8M-QM73_ES1
RTC
LPC
LAN / GLAN
CPU
IHDA
IDE
SATA
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
ICH8-M(LPC,IDE,SATA) 2/5
Size
A3
Document Number
M730-1-01
Rev
1.0
Date:
Saturday, October 13, 2007
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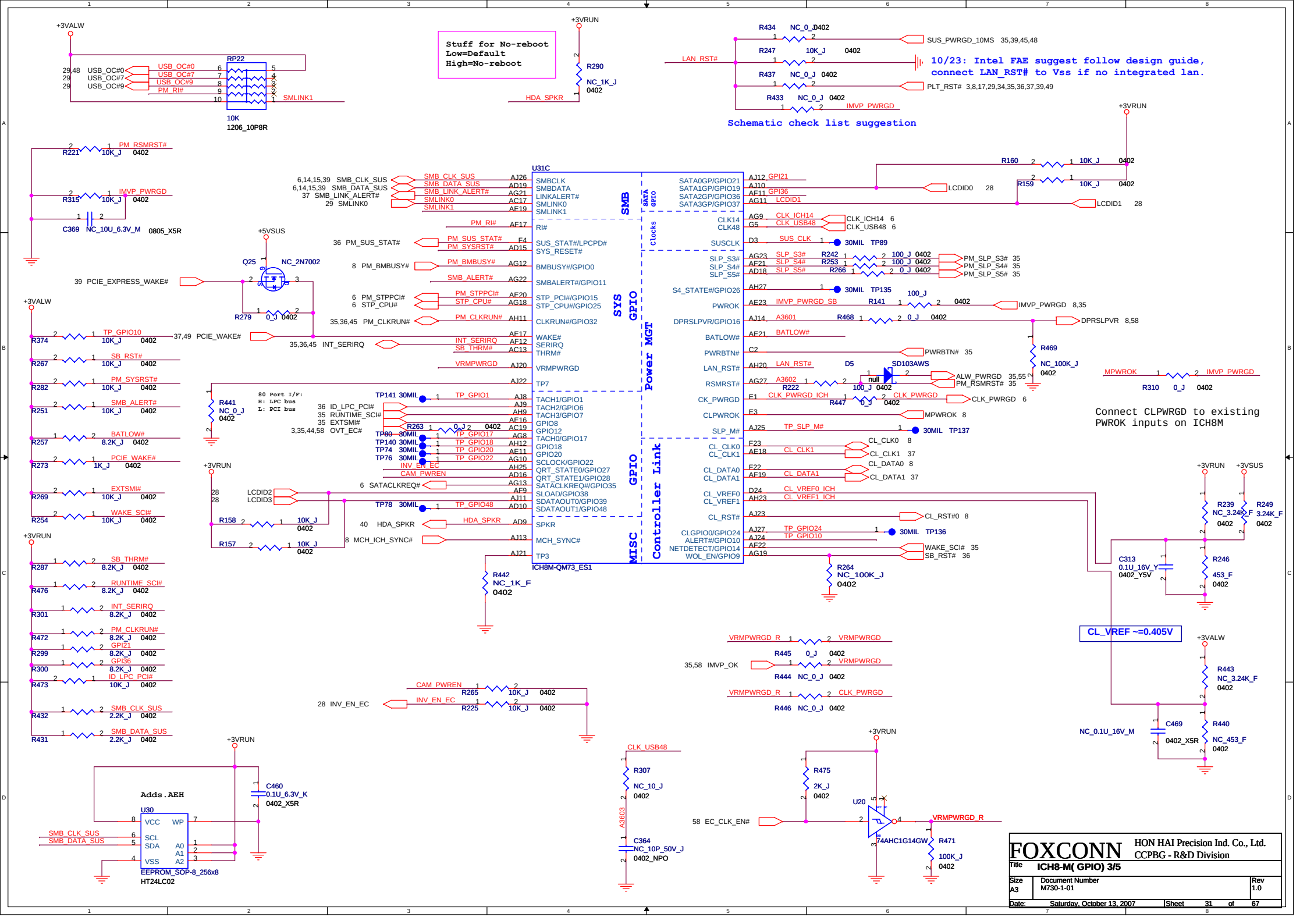
Stuff for No-reboot
Low=Default
High=No-reboot
10/23: Intel FAE suggest follow design guide, connect LAN_RST# to Vss if no integrated lan.
Schematic check list suggestion
U31C
ICH8M-QM73_ES1
SMB
GPIO
Power MGT
Controller Link
MISC
Clocks
SYS
Connect CLPWRGD to existing PWROK inputs on ICH8M
CL_VREF ~=0.405V
Adds.AEH
EEPROM_SOP-8_256x8
HT24LC02
74AHC1G14GW
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
ICH8-M(GPIO) 3/5
Size
A3
Document Number
M730-1-01
Rev
1.0
Date:
Saturday, October 13, 2007
Sheet
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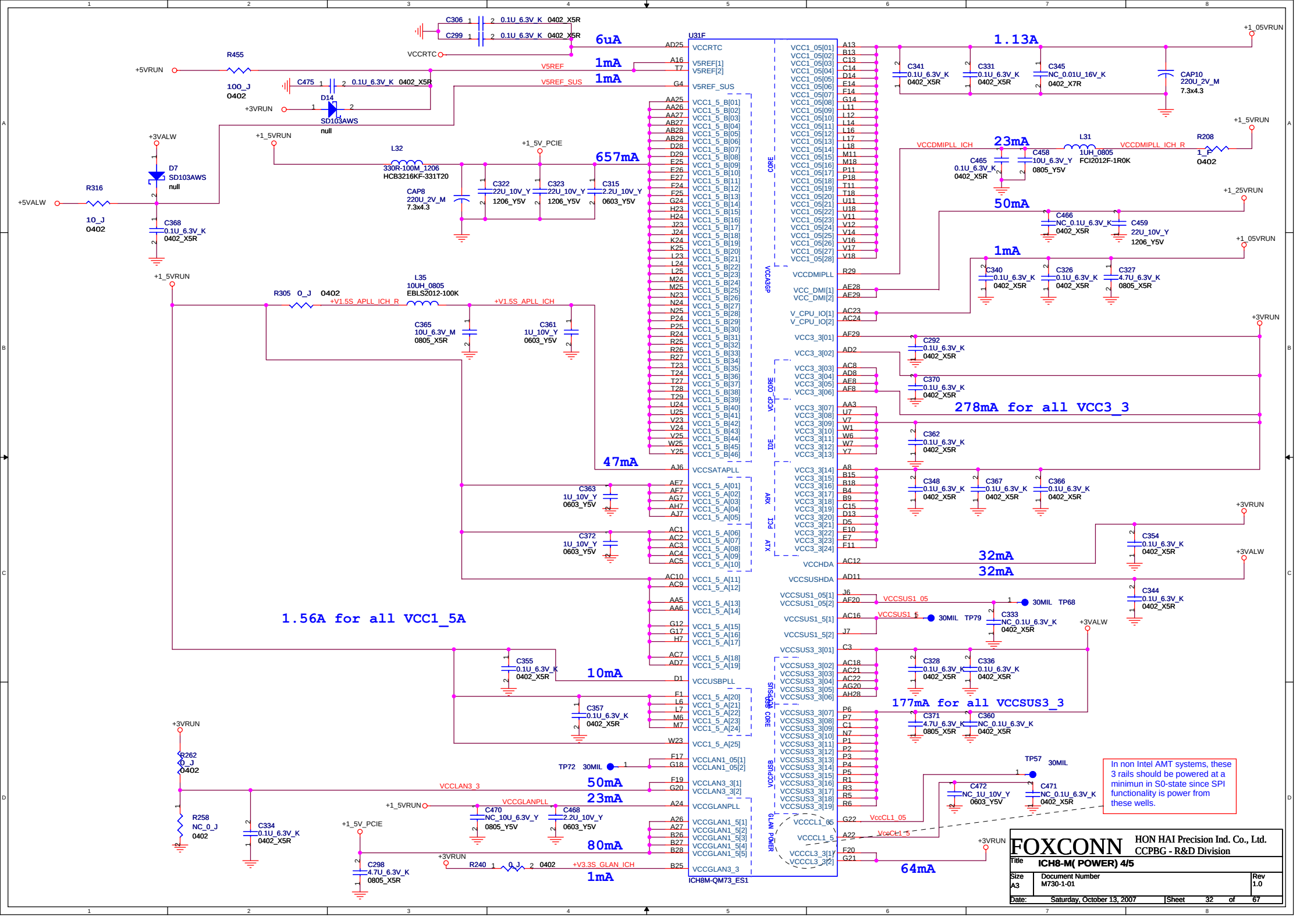
U31F
ICH8M-QM73_ES1
6uA
1mA
1mA
657mA
47mA
1.56A for all VCC1_5A
10mA
50mA
23mA
80mA
1mA
1.13A
23mA
50mA
1mA
278mA for all VCC3_3
32mA
32mA
177mA for all VCCSUS3_3
64mA
In non Intel AMT systems, these 3 rails should be powered at a minimun in S0-state since SPI functionality is power from these wells.
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title ICH8-M(POWER) 4/5
Size A3
Document Number M730-1-01
Rev 1.0
Date: Saturday, October 13, 2007
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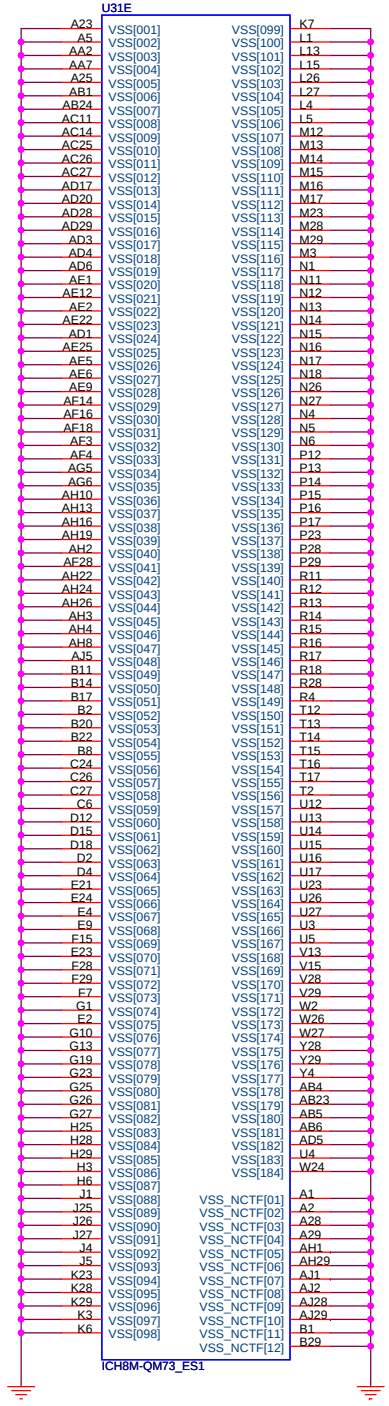
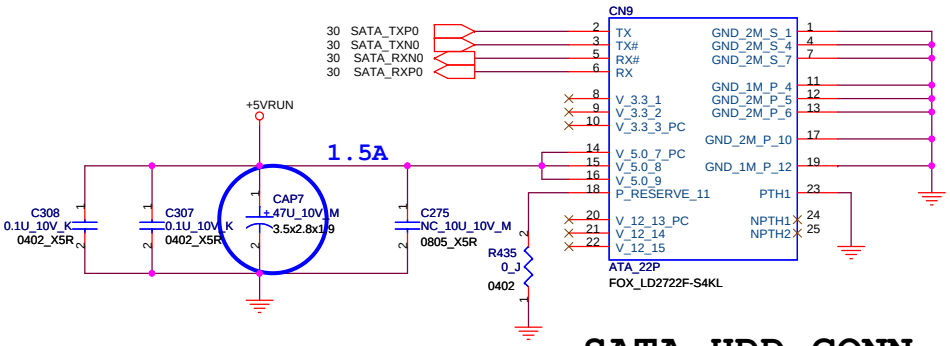
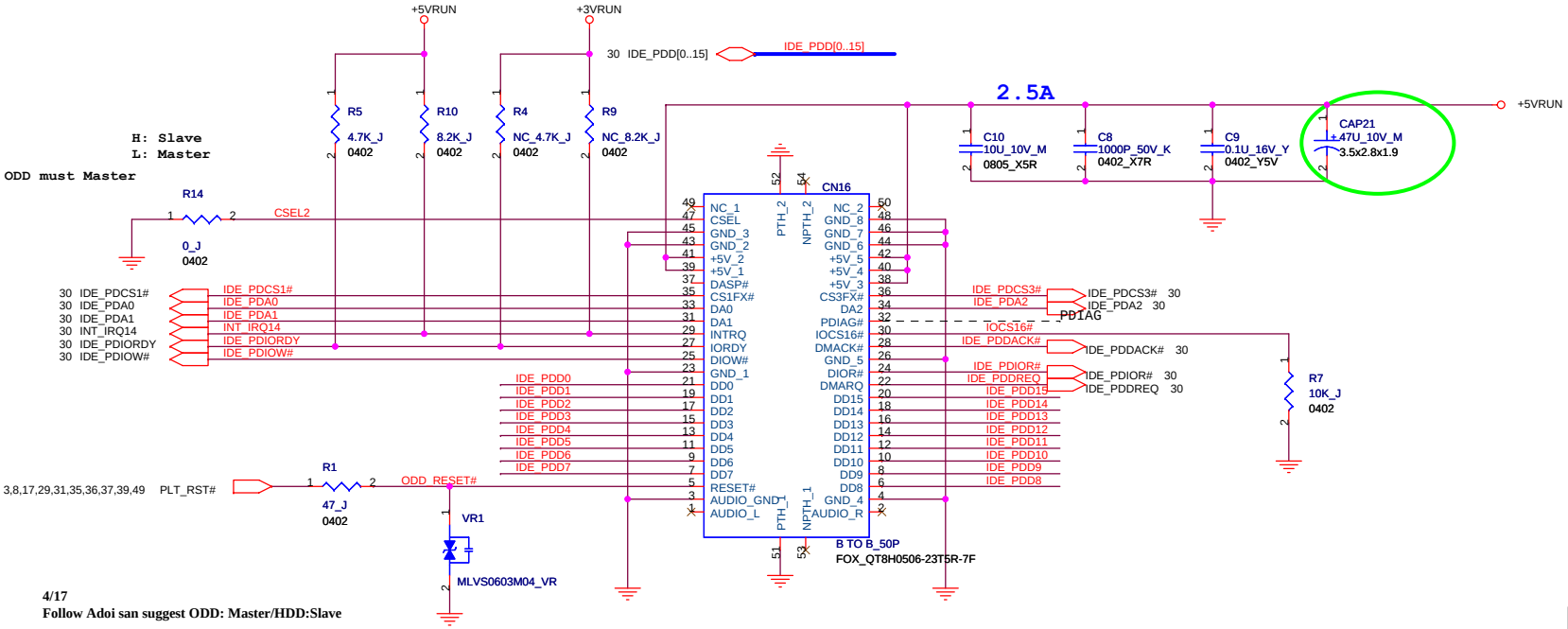


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ICH8-M(GND) 5/5	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 33 of 67	

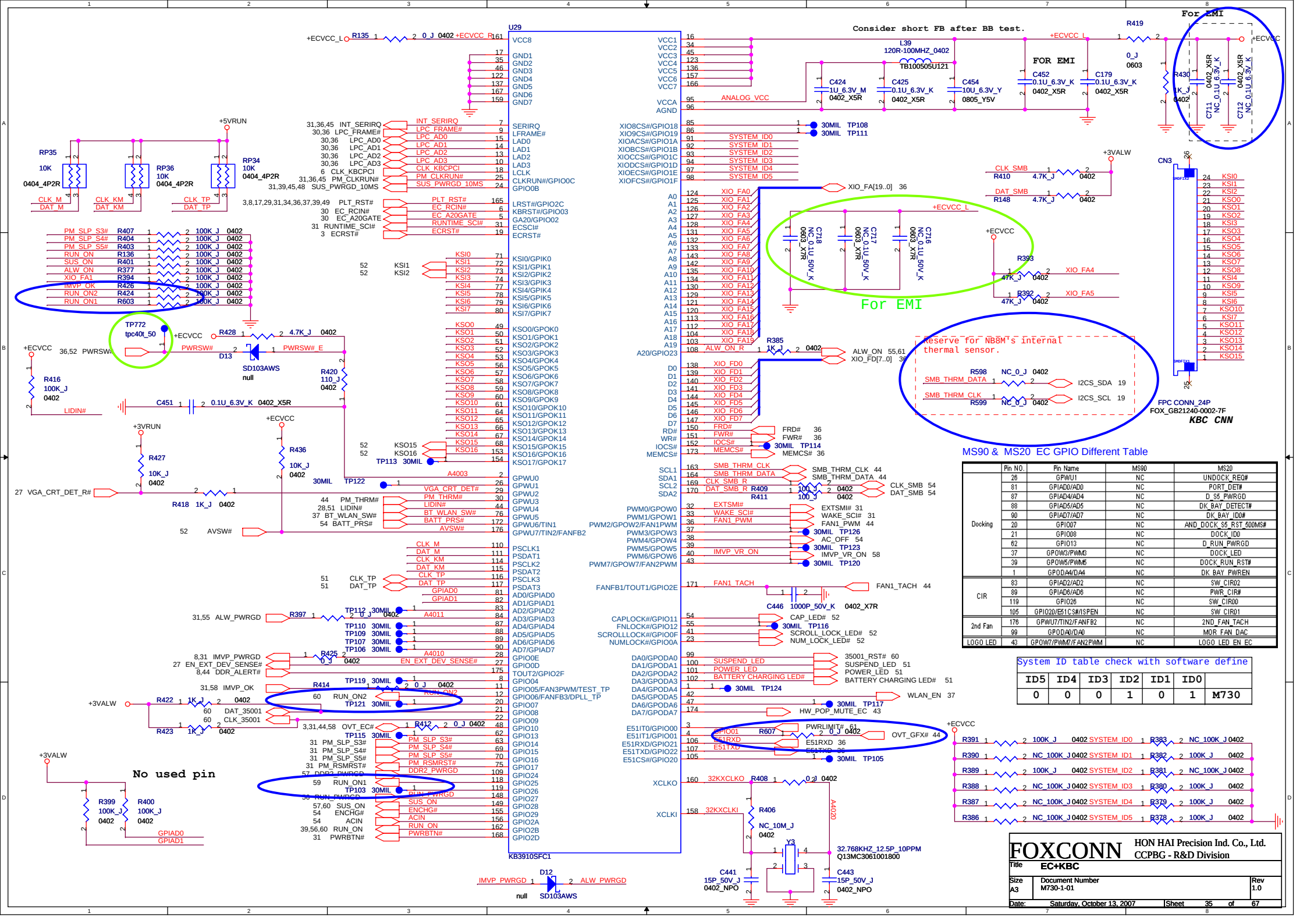


SATA HDD CONN



CD-ROM CONN

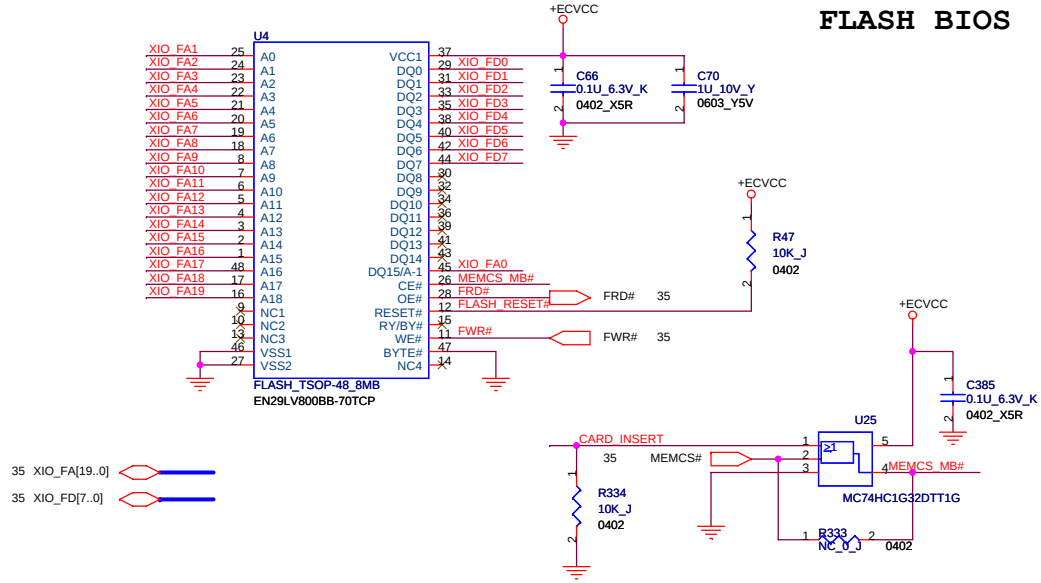
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SATA HDD/CD-ROM	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 34 of 67	



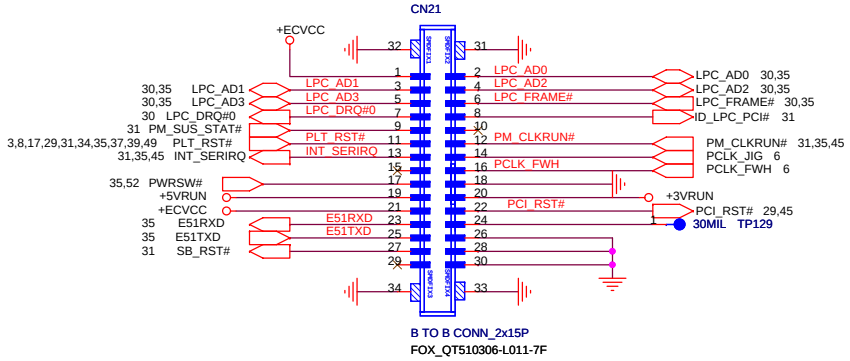
	Pin NO.	Pin Name	MS90	MS20
Docking	26	GPIW1	NC	UNDOCK_REQ#
	81	GPIAD0/AD0	NC	PORT_DET#
	87	GPIAD4/AD4	NC	D_S5_PWRGD
	88	GPIAD5/AD5	NC	DK_BAY_DETECT#
	90	GPIAD7/AD7	NC	DK_BAY_ID0#
	20	GPIO07	NC	AND_DOCK_S5_RST_50DMS#
	21	GPIO08	NC	DOCK_ID0
	62	GPIO13	NC	D_RUN_PWRGD
	37	GPOW3/PWM3	NC	DOCK_LED
	39	GPOW5/PWM5	NC	DOCK_RUN_RST#
	1	GPODA4/DA4	NC	DK_BAY_PWREN
CIR	83	GPIAD2/AD2	NC	SW_CIR02
	89	GPIAD6/AD6	NC	PWR_CIR#
	119	GPIO26	NC	SW_CIR00
	105	GPIO20/E51CS#/ISPEN	NC	SW_CIR01
2nd Fan	176	GPWU7/TIN2/FANFB2	NC	2ND_FAN_TACH
	99	GPODA0/DA0	NC	MOR_FAN_DAC
LOGO LED	43	GPOW7/PWM7/FAN2PWM	NC	LOGO_LED_EN_EC

ID5	ID4	ID3	ID2	ID1	ID0	
0	0	0	1	0	1	M730

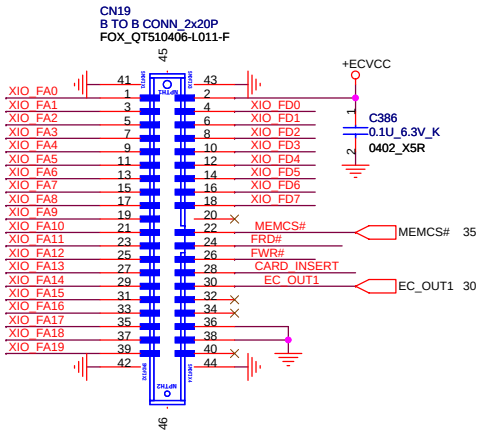
FLASH BIOS



JIG-120

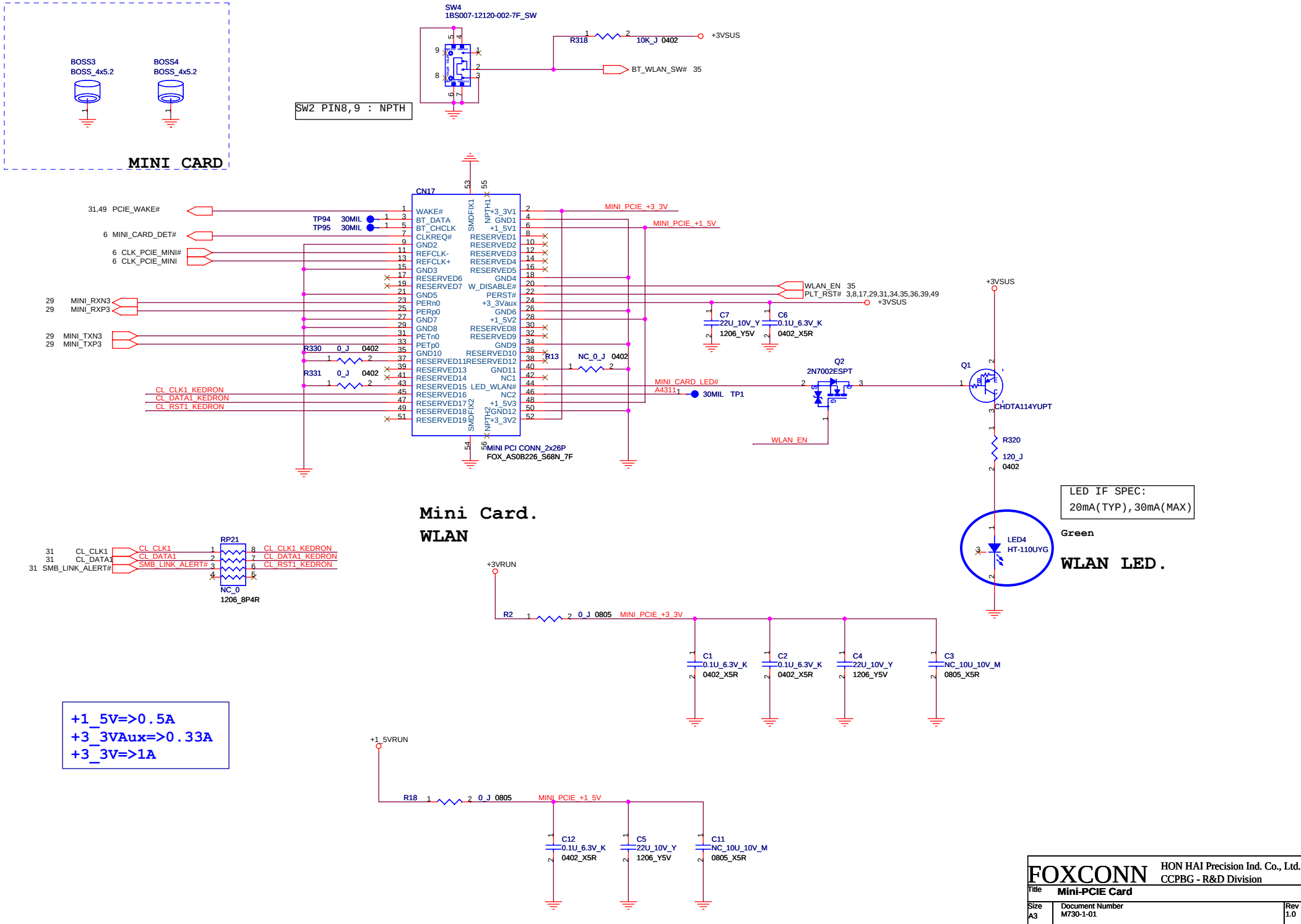


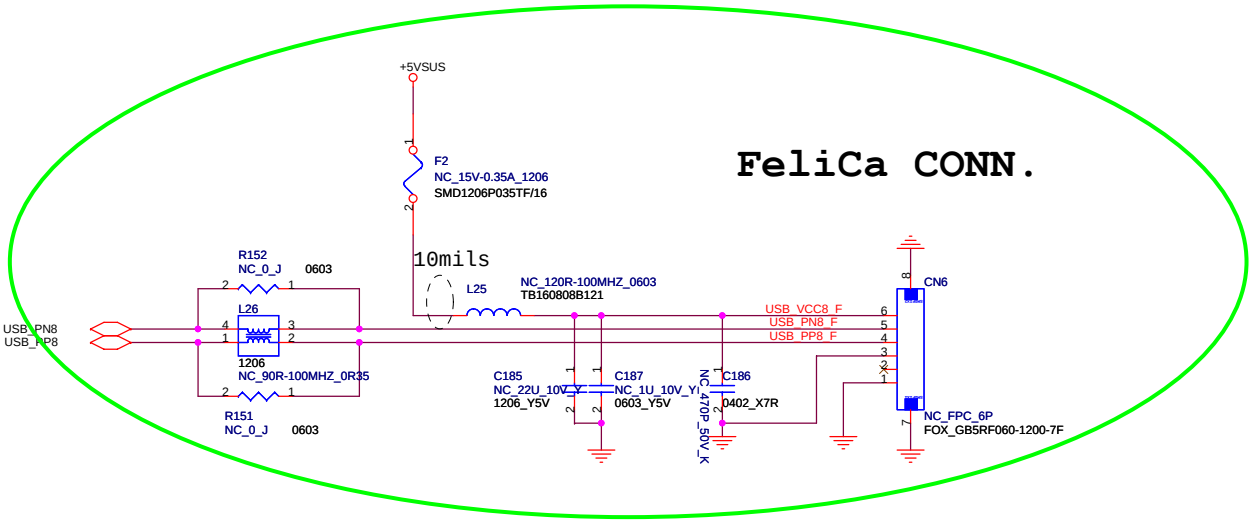
Pin 18 of JIG-120 is useless in debug board, so we let pin 18 NC.



X-BUS

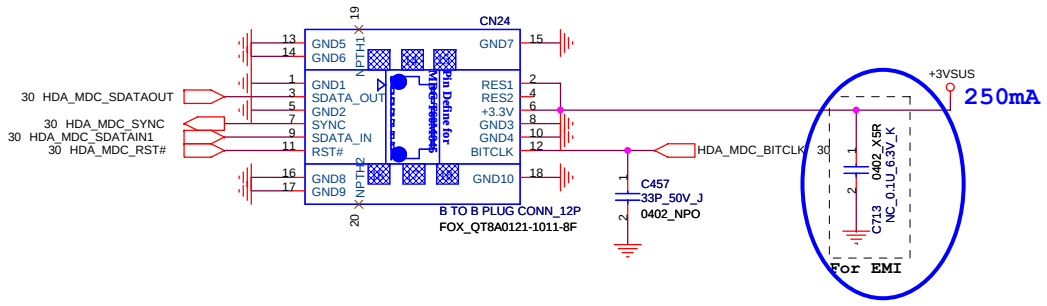
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Flash ROM/X-Bus CONN		
Size A3	Document Number M730-1-01		Rev 1.0
Date: Saturday, October 13, 2007		Sheet 36 of 67	


MINI CARD
BOSS3
BOSS_4x5.2
BOSS4
BOSS_4x5.2
SW4
1BS007-12120-002-7F_SW
SW2 PIN8,9 : NPTH
R318
10K_J 0402
+3VSUS
BT_WLAN_SW# 35
CN17
MINI PCI CONN_2x26P
FOX_AS0B226_S68N_7F
31,49 PCIE_WAKE#
6 MINI_CARD_DET#
6 CLK_PCIE_MINI#
6 CLK_PCIE_MINI
29 MINI_RXN3
29 MINI_RXP3
29 MINI_TXN3
29 MINI_TXP3
TP94 30MIL
TP95 30MIL
R330 0_J 0402
R331 0_J 0402
R13 NC_0_J 0402
CL_CLK1_KEDRON
CL_DATA1_KEDRON
CL_RST1_KEDRON
MINI_PCIE_+3_3V
MINI_PCIE_+1_5V
WLAN_EN 35
PLT_RST# 3,8,17,29,31,34,35,36,39,49
+3VSUS
C7 22U_10V_Y 1206_Y5V
C6 0.1U_6.3V_K 0402_X5R
MINI_CARD_LED#
A4311
30MIL TP1
Q2
2N7002ESPT
Q1
CHDTA114YUPT
WLAN_EN
R320
120_J
0402
LED IF SPEC:
20mA(TYP),30mA(MAX)
Green
LED4
HT-110UYG
WLAN LED.
Mini Card.
WLAN
RP21
NC_0
1206_8P4R
31 CL_CLK1
31 CL_DATA1
31 SMB_LINK_ALERT#
CL_CLK1
CL_DATA1
SMB_LINK_ALERT#
CL_CLK1_KEDRON
CL_DATA1_KEDRON
CL_RST1_KEDRON
+3VRUN
R2 0_J 0805
MINI_PCIE_+3_3V
C1 0.1U_6.3V_K 0402_X5R
C2 0.1U_6.3V_K 0402_X5R
C4 22U_10V_Y 1206_Y5V
C3 NC_10U_10V_M 0805_X5R
+1_5VRUN
R18 0_J 0805
MINI_PCIE_+1_5V
C12 0.1U_6.3V_K 0402_X5R
C5 22U_10V_Y 1206_Y5V
C11 NC_10U_10V_M 0805_X5R
+1_5V=>0.5A
+3_3VAux=>0.33A
+3_3V=>1A
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
Mini-PCIE Card
Size
A3
Document Number
M730-1-01
Rev
1.0
Date:
Saturday, October 13, 2007
Sheet
37
of
67



BOM Notice:

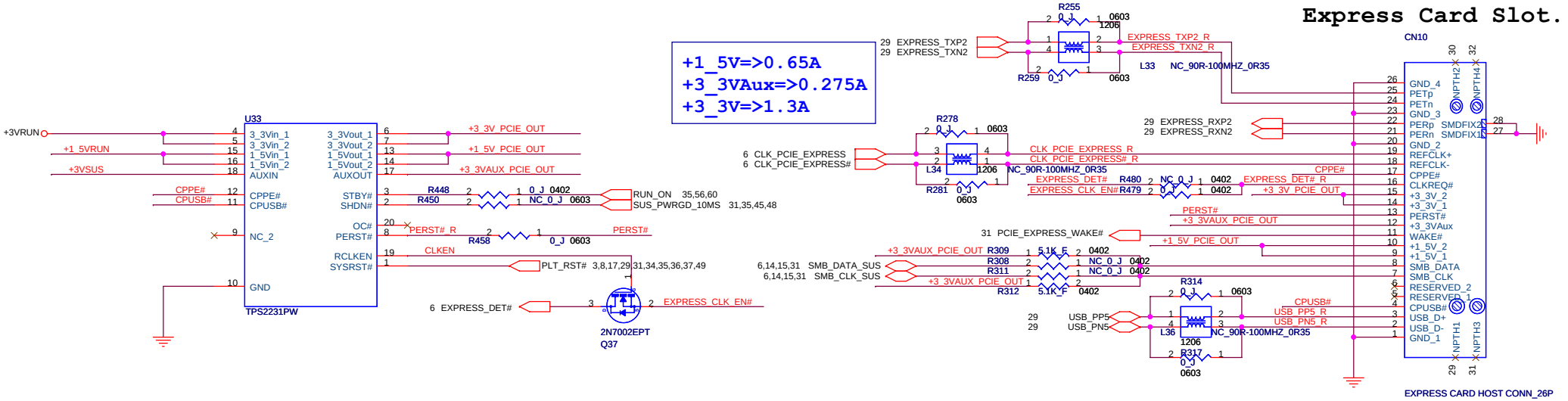
W/ FeliCa SKU	R151,R152,L25,C185,C186,F2,CN6	stuff
W/O FeliCa SKU	R151,R152,L25,C185,C186,F2,CN6	no stuff

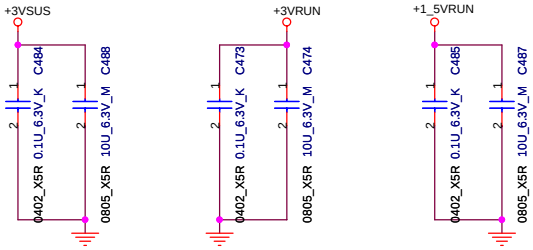


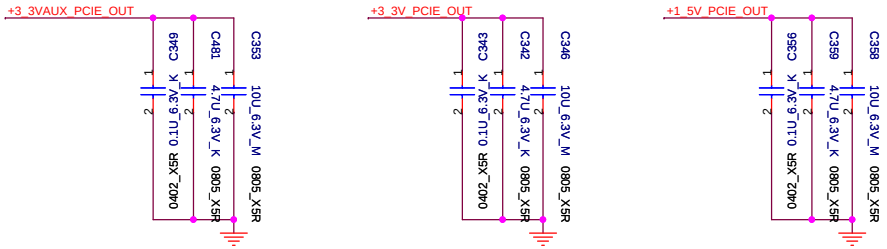
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	FeliCa/MDC		
Size A3	Document Number M730-1-01		Rev 1.0
Date: Saturday, October 13, 2007	Sheet 38 of 67		

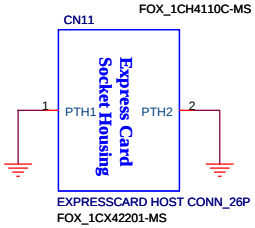
Express Card Slot.

+1_5V=>0.65A
+3_3VAux=>0.275A
+3_3V=>1.3A



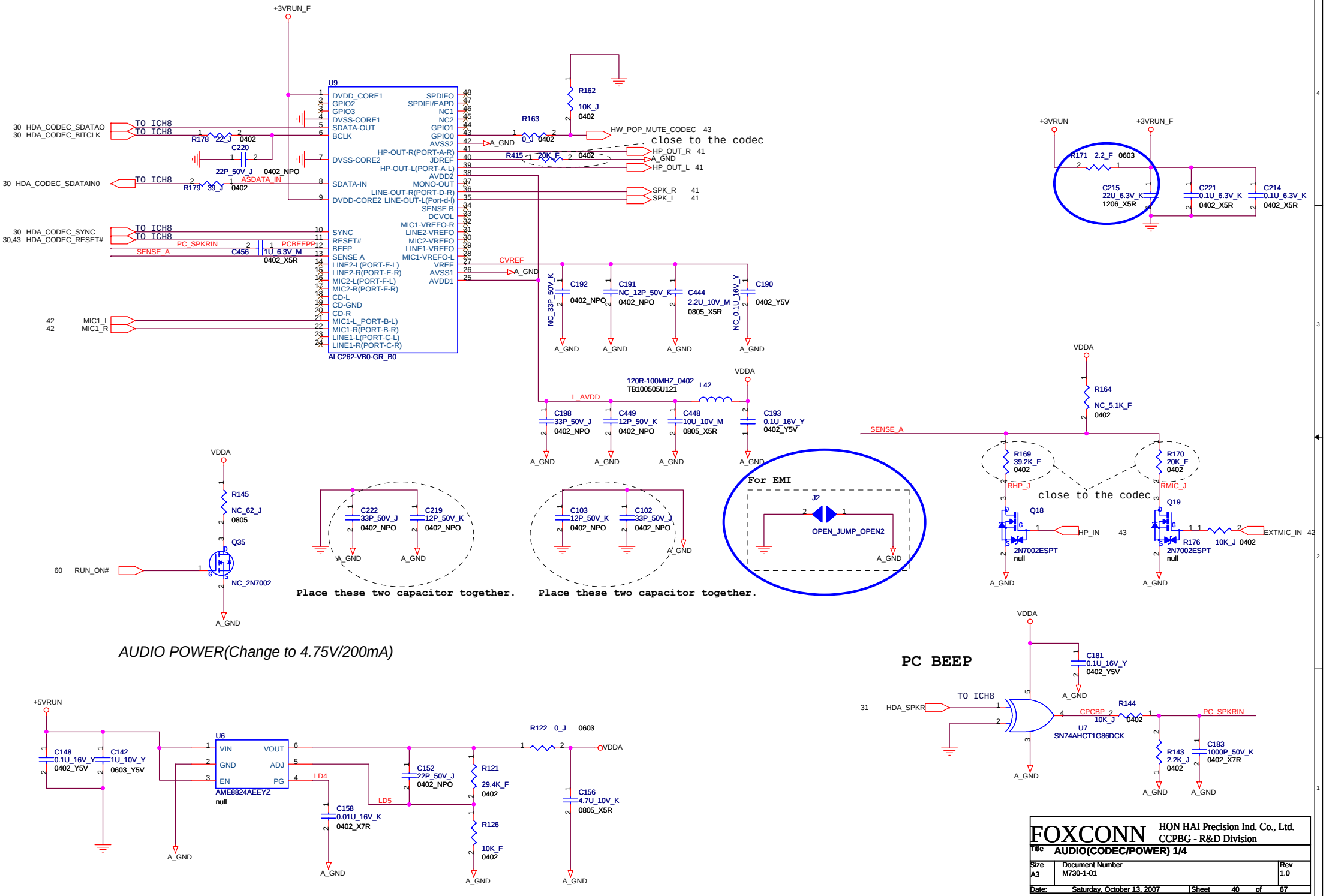




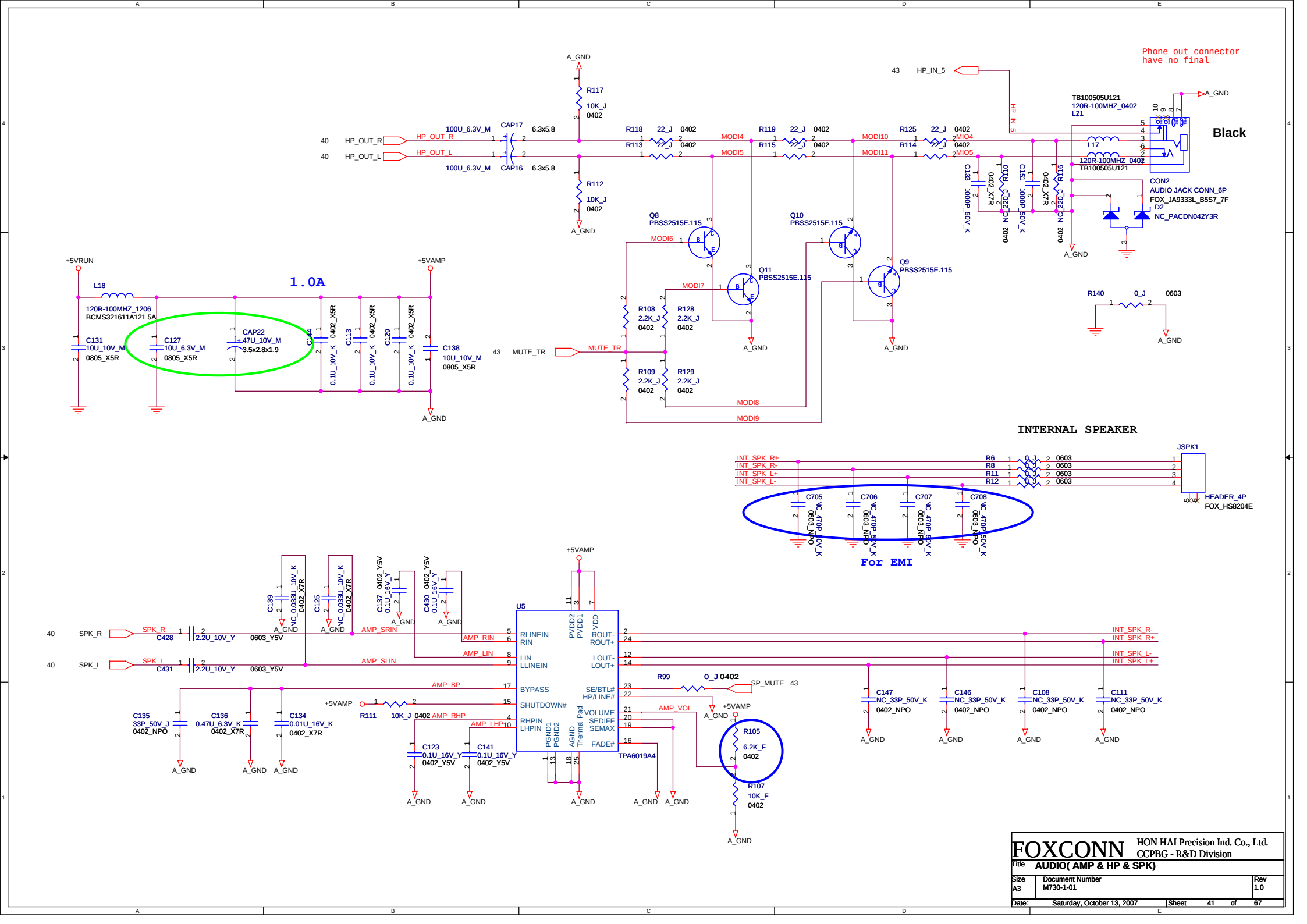


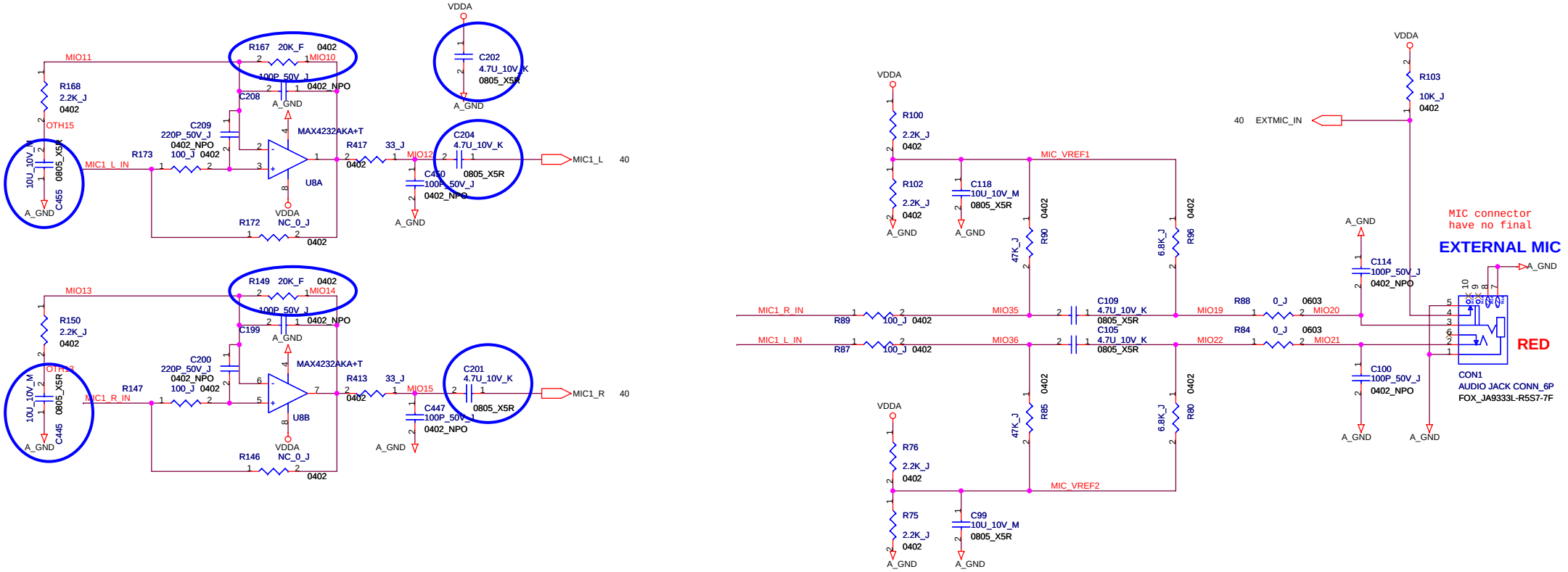
Express Card Housing.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: EXPRESS		
Size: A3	Document Number: M730-1-01	Rev: 1.0
Date: Saturday, October 13, 2007	Sheet 39 of 67	

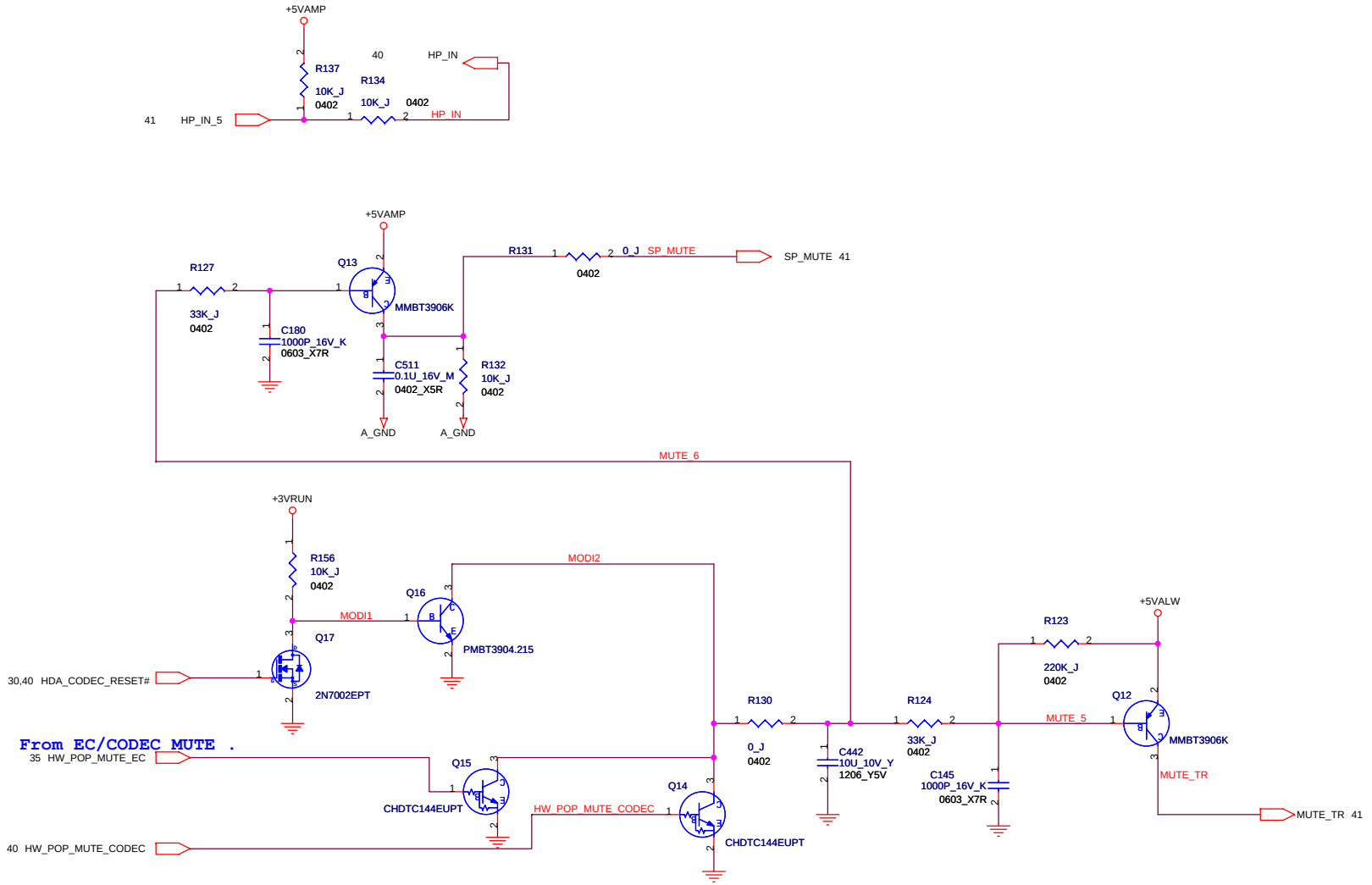


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO(CODEC/POWER) 1/4	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 40 of 67	

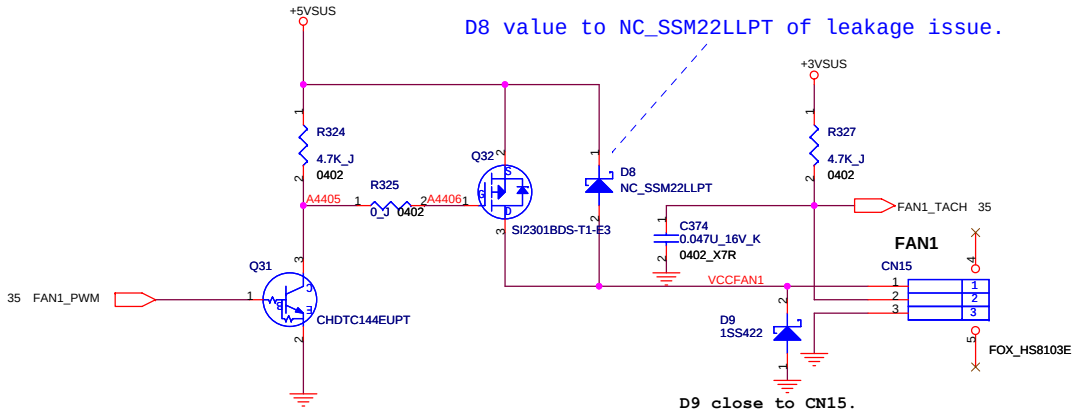

Phone out connector have no final
Black
INTERNAL SPEAKER
For EMI
1.0A
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title AUDIO(AMP & HP & SPK)
Size A3
Document Number M730-1-01
Rev 1.0
Date: Saturday, October 13, 2007
Sheet 41 of 67



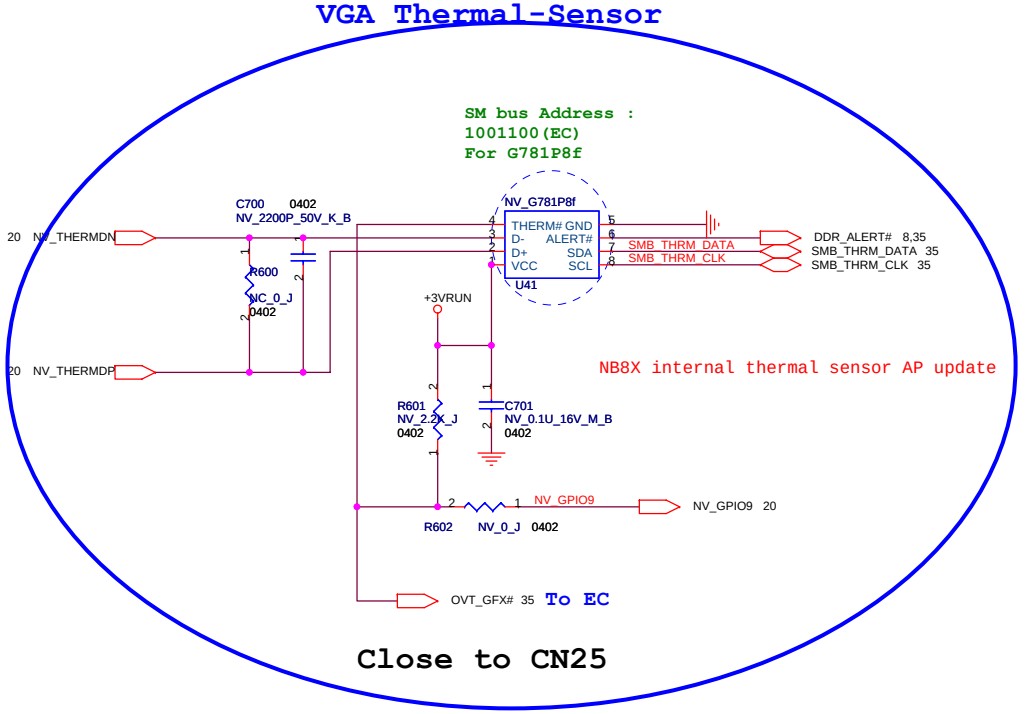
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO(EXT MIC & PHONE OUT)	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 42 of 67	

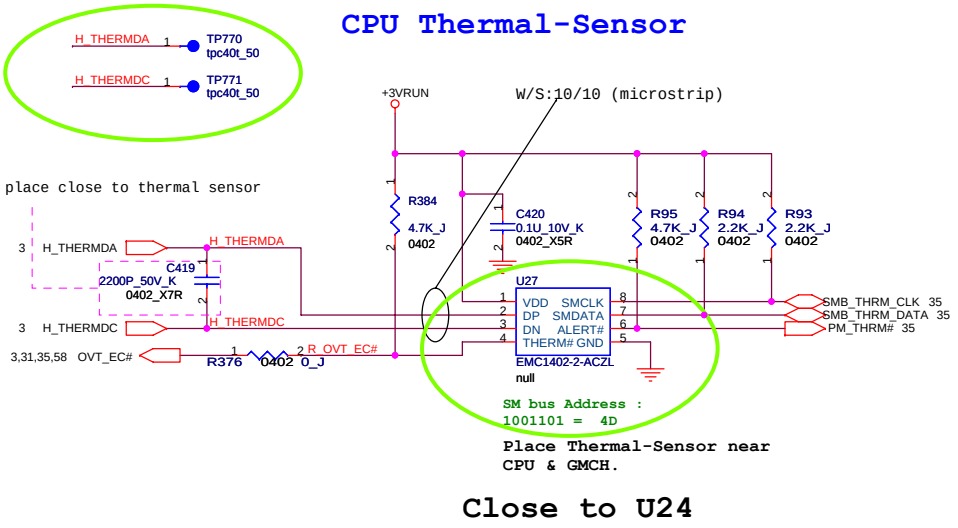


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO (MUTE & INTMIC)	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 43 of 67	

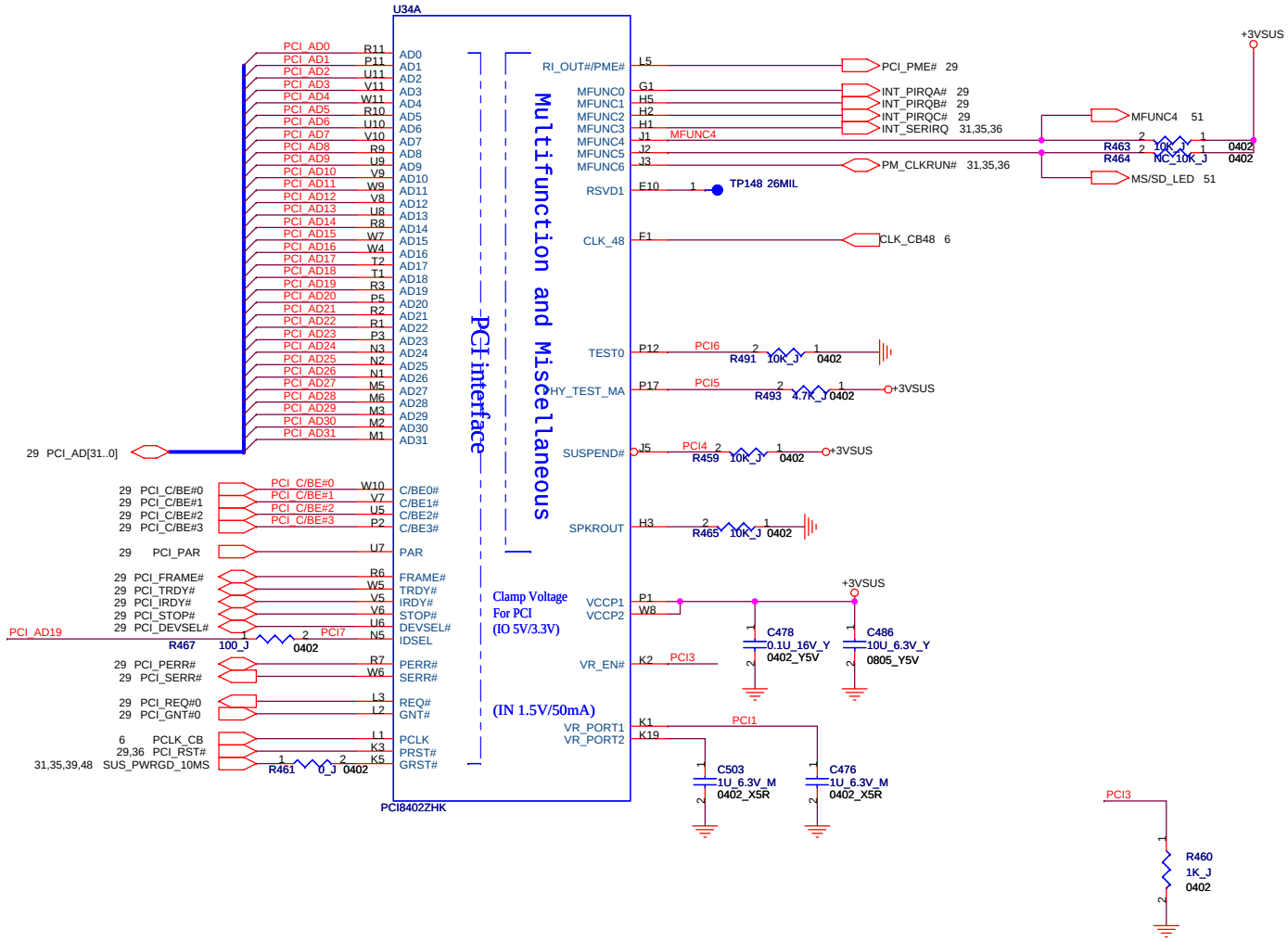


FAN

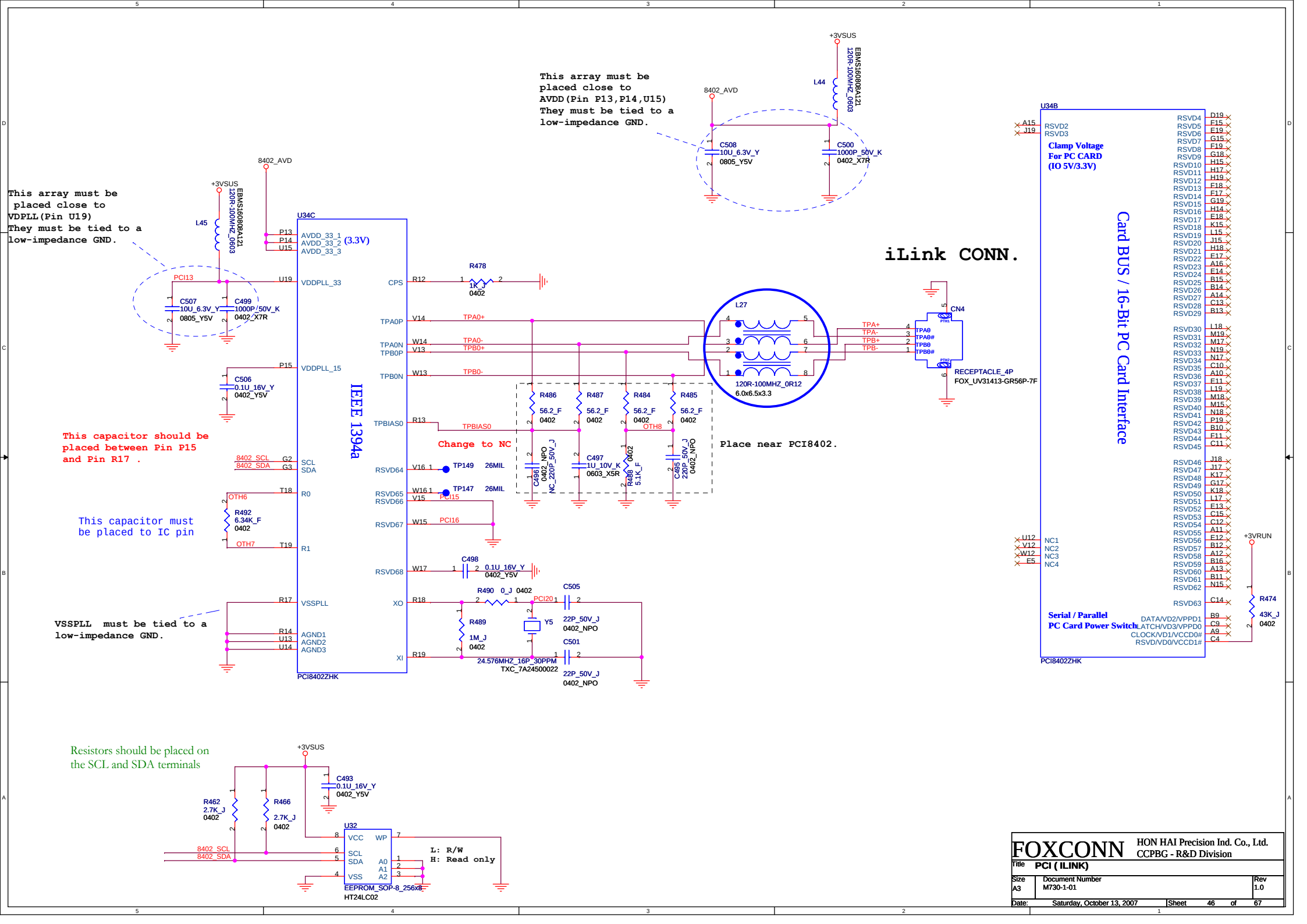




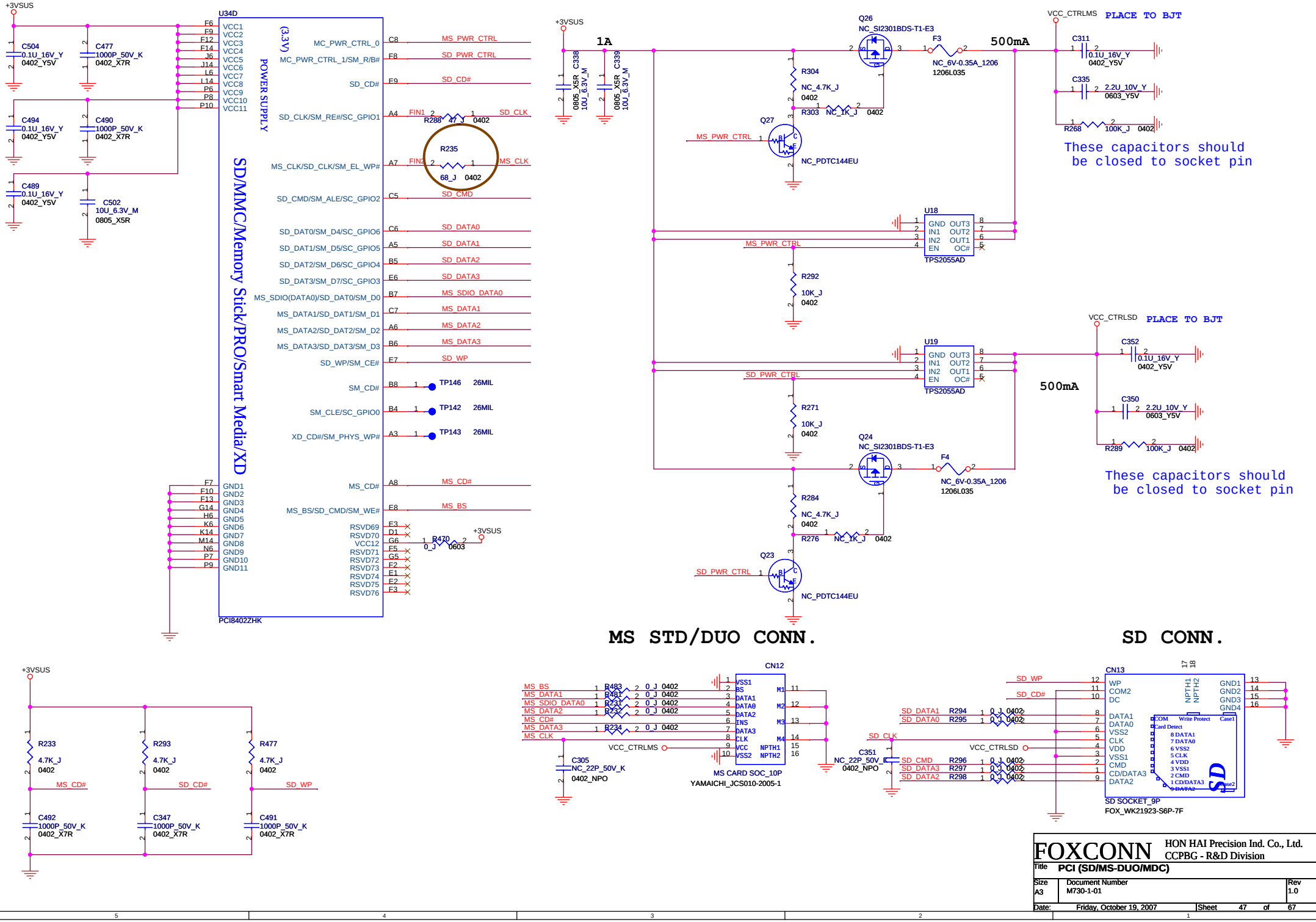
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	FAN/Thermal-Sensor	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 44 of 67	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCI (PCI BUS)	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 45 of 67	



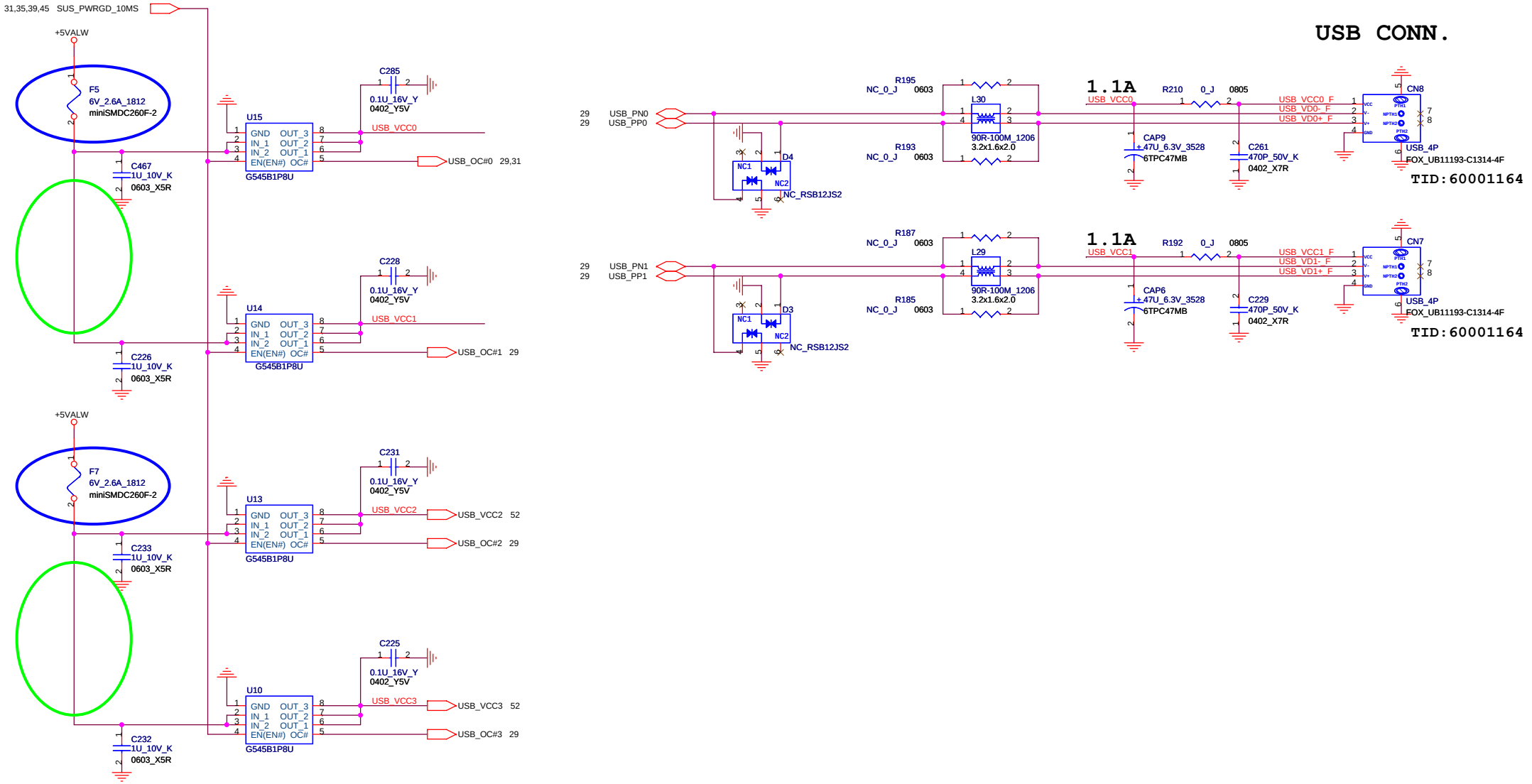
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCI (ILINK)	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 46 of 67	



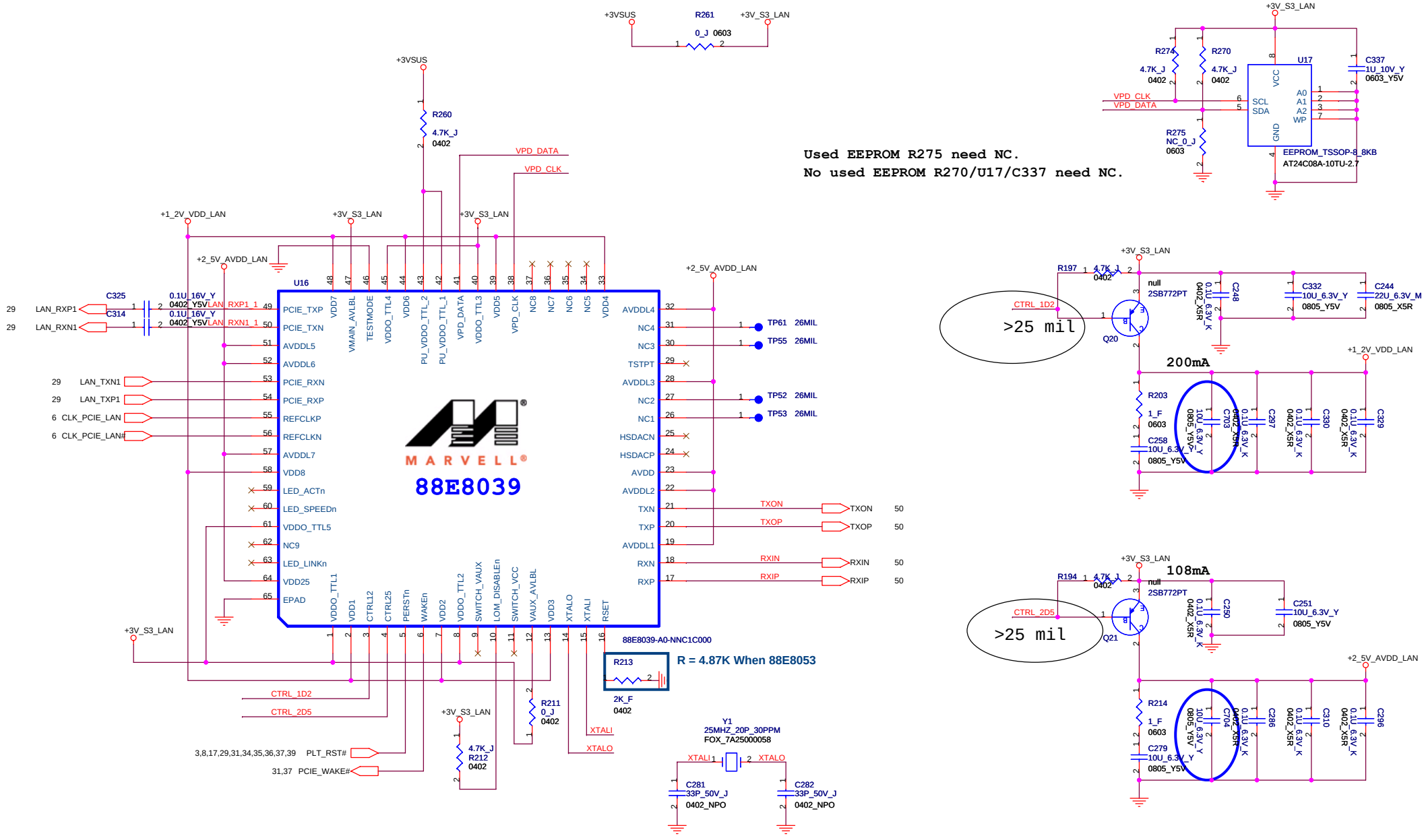
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	PCI (SD/MS-DUO/MDC)	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Friday, October 19, 2007	Sheet 47 of 67	

USB CONN.

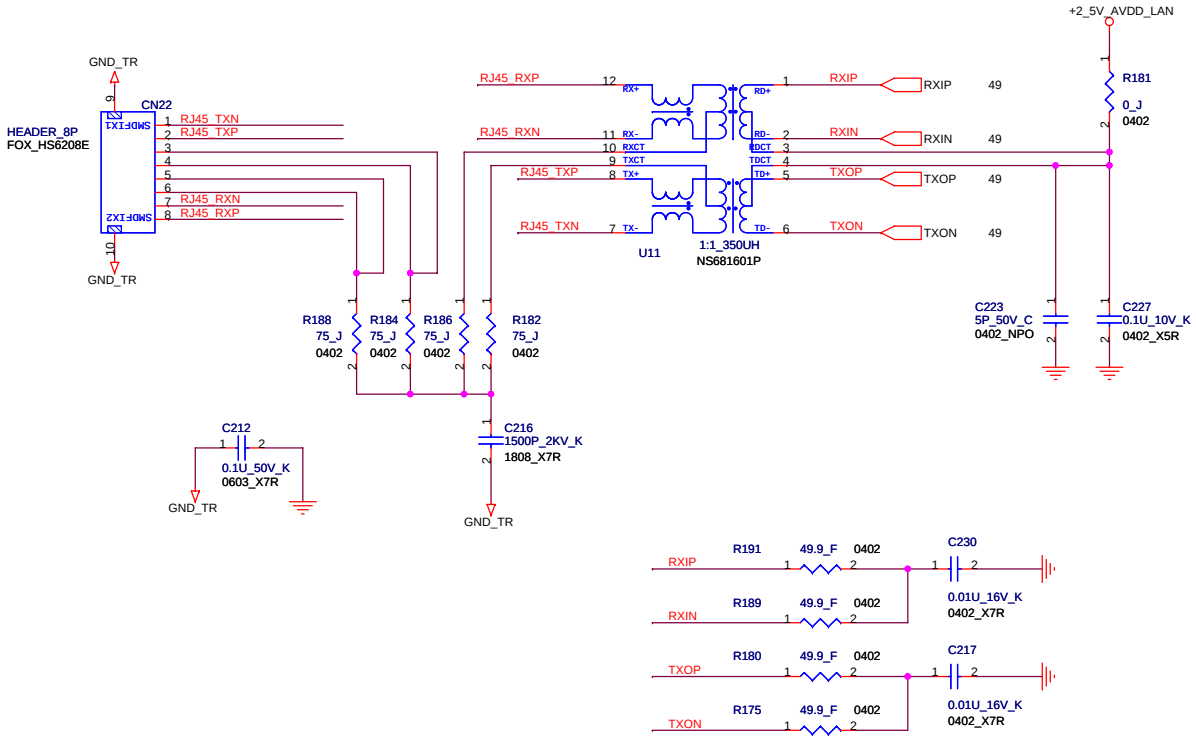


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	USB2.0	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 48 of 67	



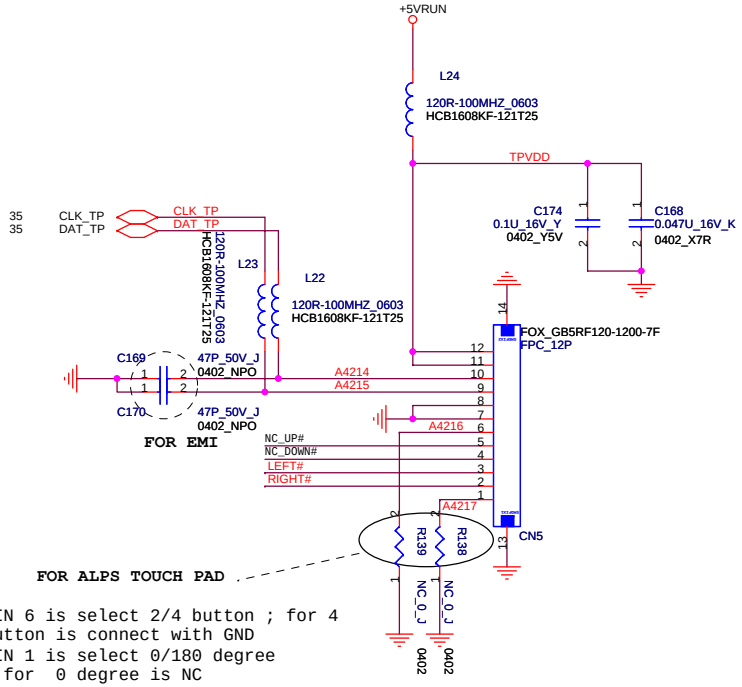
Used EEPROM R275 need NC.
No used EEPROM R270/U17/C337 need NC.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	LAN (88E8036)	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 49 of 67	



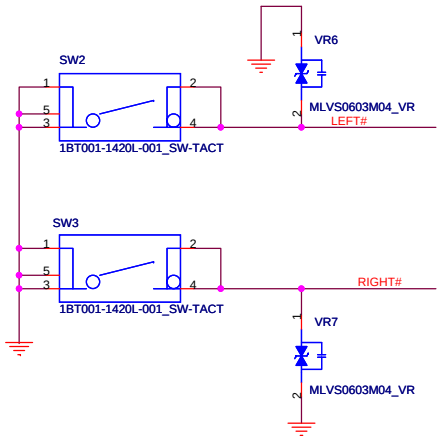
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LAN Transformer	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 50 of 67	

Touch Pad CONN.

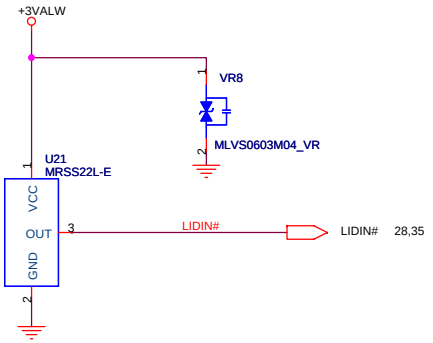


PIN 6 is select 2/4 button ; for 4 button is connect with GND
PIN 1 is select 0/180 degree ; for 0 degree is NC

TP_LEFT Button

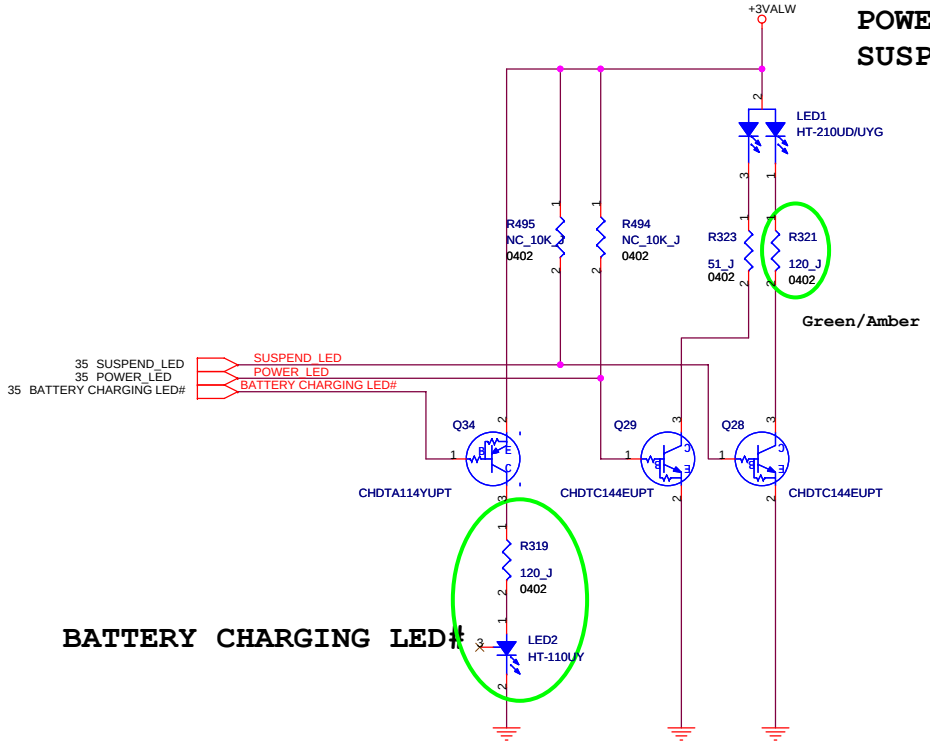


LID Switch

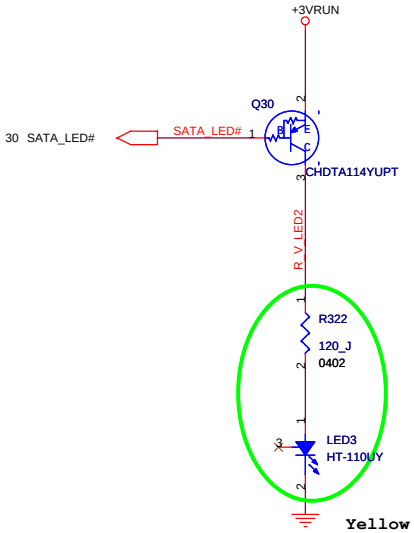


TP_Right Button

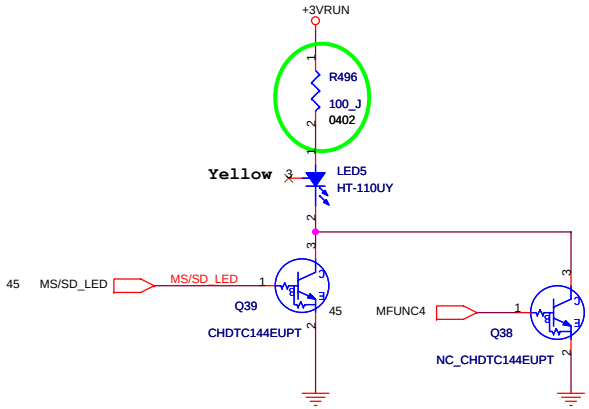
POWER_LED
SUSPEND_LED



SATA_LED#



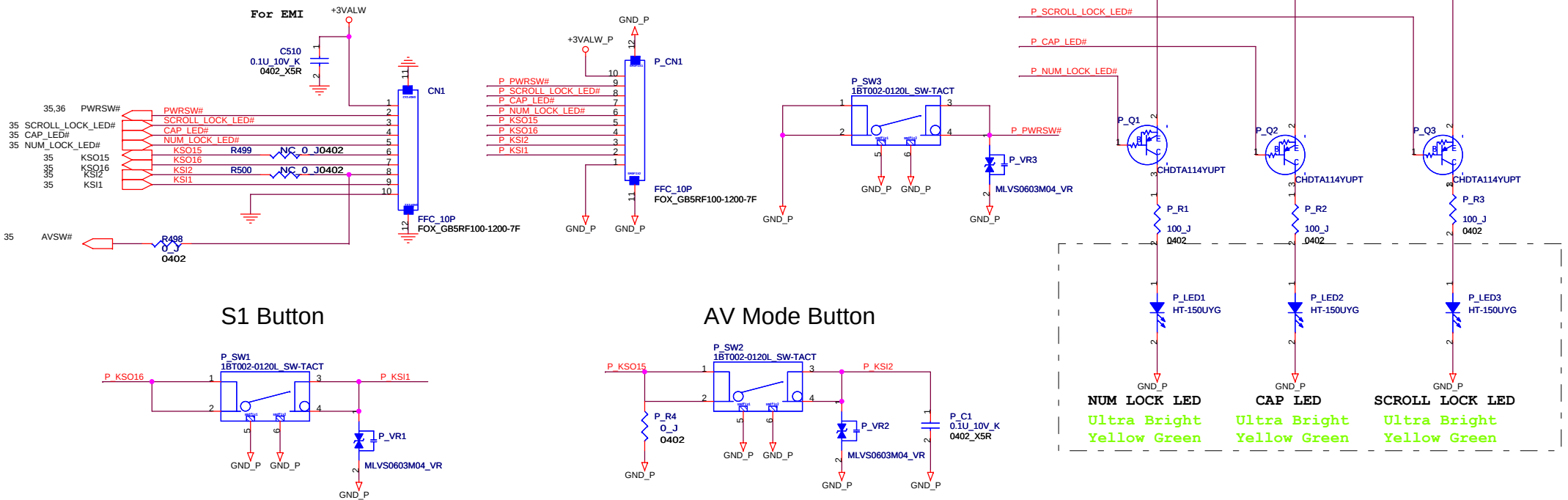
MS/SD LED



BATTERY CHARGING LED#

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	LED/Touch/Lid		
Size A3	Document Number M730-1-01		Rev 1.0
Date: Saturday, October 13, 2007	Sheet 51 of 67		

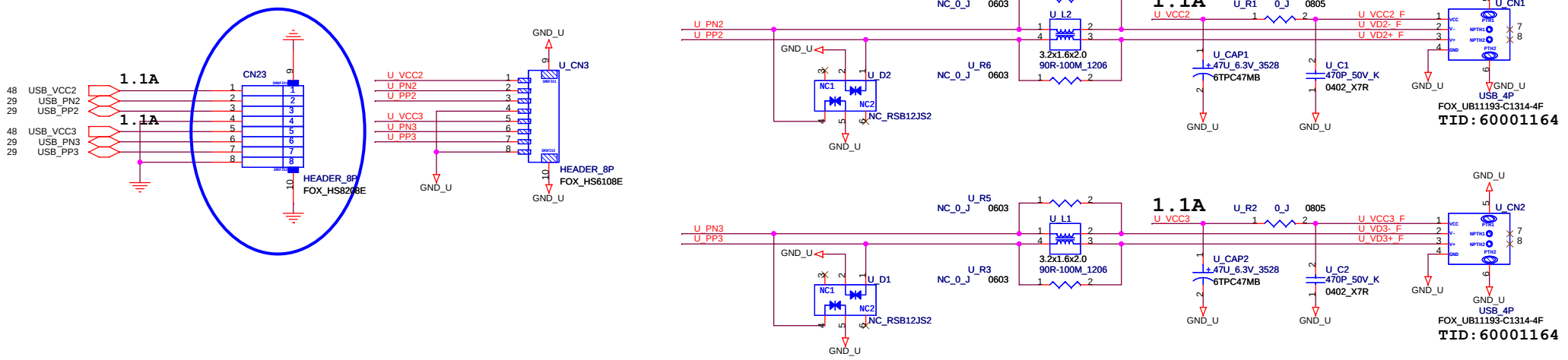
Power Button Board



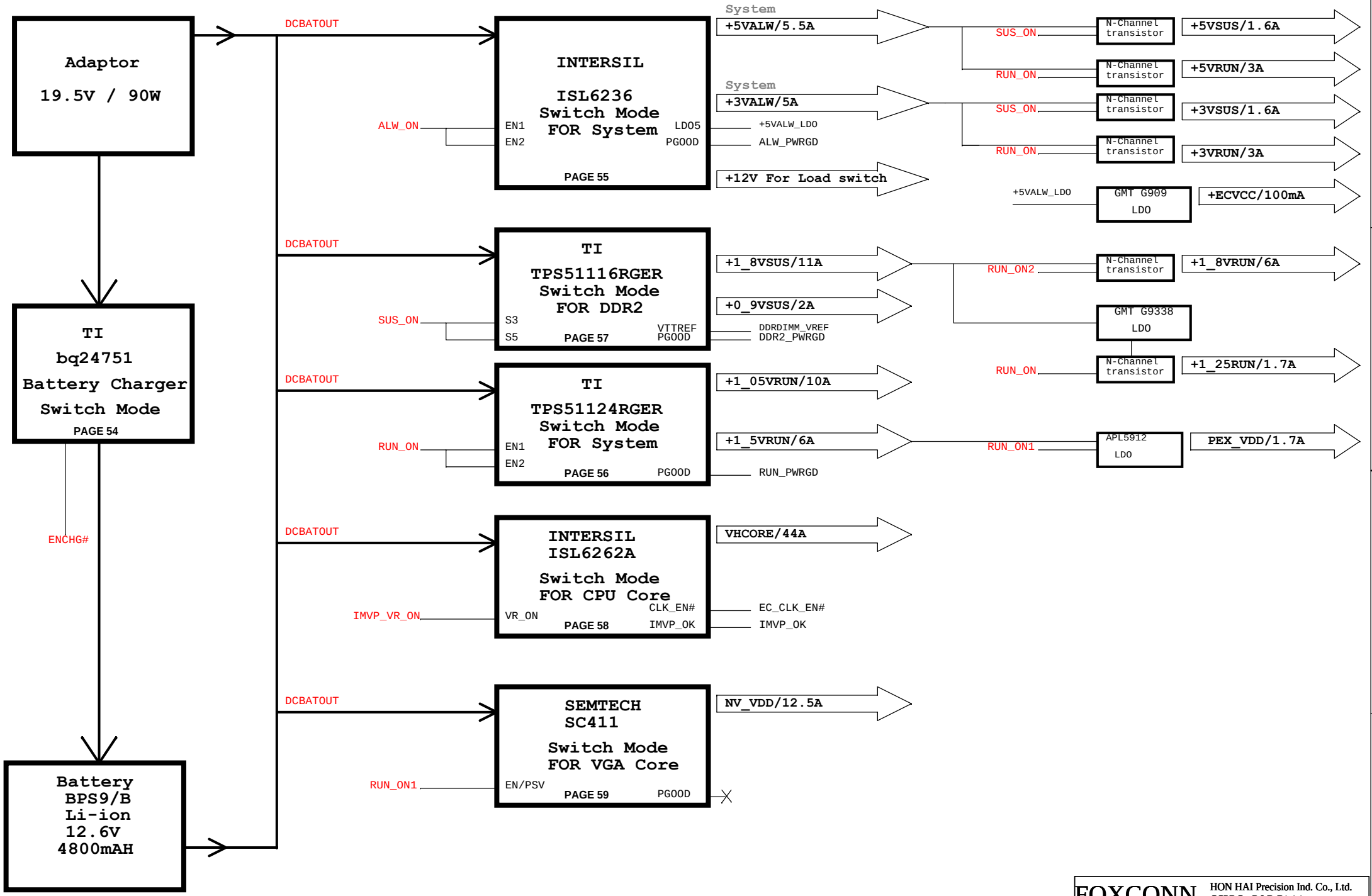
S1 Button

AV Mode Button

USB Board

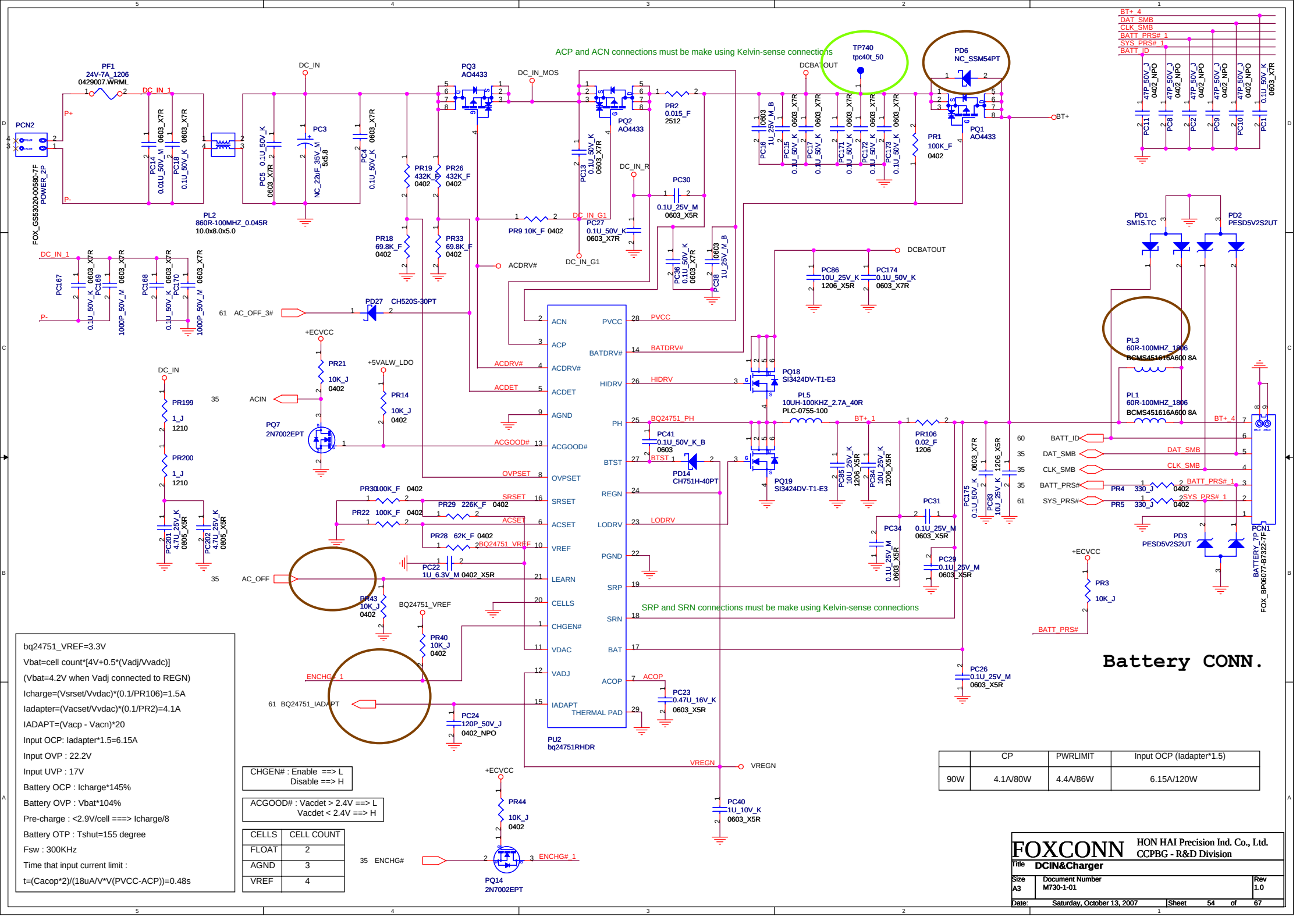


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	KEYBOARD LED & Power SW	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 52 of 67	



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Power Design Diagram	
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 53 of 67	


ACP and ACN connections must be make using Kelvin-sense connections
SRP and SRN connections must be make using Kelvin-sense connections
Battery CONN.
PU2
bq24751RHDR
PF1
24V-7A_1206
0429007.WRML
PCN2
FOX_GS53020-00580-7F
POWER_2P
PL2
860R-100MHZ_0.045R
10.0x8.0x5.0
PQ3
AO4433
PQ2
AO4433
PQ1
AO4433
PR2
0.015_F
2512
PR1
100K_F
0402
PD6
NC_SSM54PT
TP740
tpc40t_50
PD1
SM15.TC
PD2
PESD5V2S2UT
PD3
PESD5V2S2UT
PL3
60R-100MHZ_1806
BCMS451616A600 8A
PL1
60R-100MHZ_1806
BCMS451616A600 8A
PL5
10UH-100KHZ_2.7A_40R
PLC-0755-100
PQ18
SI3424DV-T1-E3
PQ19
SI3424DV-T1-E3
PD14
CH751H-40PT
PD27
CH520S-30PT
PQ7
2N7002EPT
PQ14
2N7002EPT
PCN1
BATTERY_7P
FOX_BP06077-B7322-7F
DC_IN
DC_IN_1
DC_IN_MOS
DC_IN_R
DC_IN_G1
DCBATOUT
BT+
BT+_1
BT+_4
ACDRV#
ACDET
ACGOOD#
OVPSET
SRSET
ACSET
BQ24751_VREF
LEARN
CELLS
CHGEN#
VDAC
VADJ
IADAPT
THERMAL PAD
ACN
ACP
AGND
BATDRV#
HIDRV
PH
BTST
REGN
LODRV
PGND
SRP
SRN
BAT
ACOP
PVCC
VREGN
+ECVCC
+5VALW_LDO
ACIN
AC_OFF
AC_OFF_3#
ENCHG#
ENCHG#_1
BQ24751_IADAPT
BATT_ID
DAT_SMB
CLK_SMB
BATT_PRS#
SYS_PRS#
BATT_PRS#_1
SYS_PRS#_1
PR199 1_J 1210
PR200 1_J 1210
PR201 4.7U_25V_K 0805_X5R
PR202 4.7U_25V_K 0805_X5R
PR21 10K_J 0402
PR14 10K_J 0402
PR43 10K_J 0402
PR40 10K_J 0402
PR44 10K_J 0402
PR3 10K_J
PR4 330_J 0402
PR5 330_J 0402
PR106 0.02_F 1206
PR19 432K_F 0402
PR26 432K_F 0402
PR18 69.8K_F 0402
PR33 69.8K_F 0402
PR9 10K_F 0402
PR30 100K_F 0402
PR29 226K_F 0402
PR22 100K_F 0402
PR28 62K_F 0402
PC22 1U_6.3V_M 0402_X5R
PC24 120P_50V_J 0402_NPO
PC23 0.47U_16V_K 0603_X5R
PC40 1U_10V_K 0603_X5R
PC26 0.1U_25V_M 0603_X5R
PC29 0.1U_25V_M 0603_X5R
PC31 0.1U_25V_M 0603_X5R
PC34 0.1U_25V_M 0603_X5R
PC41 0.1U_50V_K_B 0603
PC27 0.1U_50V_K 0603_X7R
PC30 0.1U_25V_M 0603_X5R
PC86 10U_25V_K 1206_X5R
PC174 0.1U_50V_K 0603_X7R
PC85 10U_25V_K 1206_X5R
PC84 10U_25V_K 1206_X5R
PC175 0.1U_50V_K 0603_X7R
PC83 10U_25V_K 1206_X5R
PC167 0.1U_50V_K 0603_X7R
PC169 1000P_50V_M 0603_X7R
PC168 0.1U_50V_K 0603_X7R
PC170 1000P_50V_M 0603_X7R
PC36 0.1U_50V_K 0603_X7R
PC38 1U_25V_M_B 0603
PC16 1U_25V_M_B 0603
PC15 0.1U_50V_K 0603_X7R
PC17 0.1U_50V_K 0603_X7R
PC171 0.1U_50V_K 0603_X7R
PC172 0.1U_50V_K 0603_X7R
PC173 0.1U_50V_K 0603_X7R
PC11 47P_50V_J 0402_NPO
PC8 47P_50V_J 0402_NPO
PC2 47P_50V_J 0402_NPO
PC9 47P_50V_J 0402_NPO
PC10 47P_50V_J 0402_NPO
PC1 0.1U_50V_K 0603_X7R
PC14 0.01U_50V_M 0603_X7R
PC18 0.1U_50V_K 0603_X7R
PC5 0.1U_50V_K 0603_X7R
PC3 NC_22uF_35V_M 5x5.8
PC4 0.1U_50V_K 0603_X7R
PC13 0.1U_50V_K 0603_X7R
CHGEN# : Enable ==> L
Disable ==> H
ACGOOD# : Vacdet > 2.4V ==> L
Vacdet < 2.4V ==> H
bq24751_VREF=3.3V
Vbat=cell count*[4V+0.5*(Vadj/Vvadc)]
(Vbat=4.2V when Vadj connected to REGN)
Icharge=(Vsrset/Vvdac)*(0.1/PR106)=1.5A
Iadapter=(Vacset/Vvdac)*(0.1/PR2)=4.1A
IADAPT=(Vacp - Vacn)*20
Input OCP: Iadapter*1.5=6.15A
Input OVP : 22.2V
Input UVP : 17V
Battery OCP : Icharge*145%
Battery OVP : Vbat*104%
Pre-charge : <2.9V/cell ===> Icharge/8
Battery OTP : Tshut=155 degree
Fsw : 300KHz
Time that input current limit :
t=(Cacop*2)/(18uA/V*V(PVCC-ACP))=0.48s
CELLS | CELL COUNT
FLOAT | 2
AGND | 3
VREF | 4
CP | PWRLIMIT | Input OCP (Iadapter*1.5)
90W | 4.1A/80W | 4.4A/86W | 6.15A/120W
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title DCIN&Charger
Size A3
Document Number M730-1-01
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Date: Saturday, October 13, 2007
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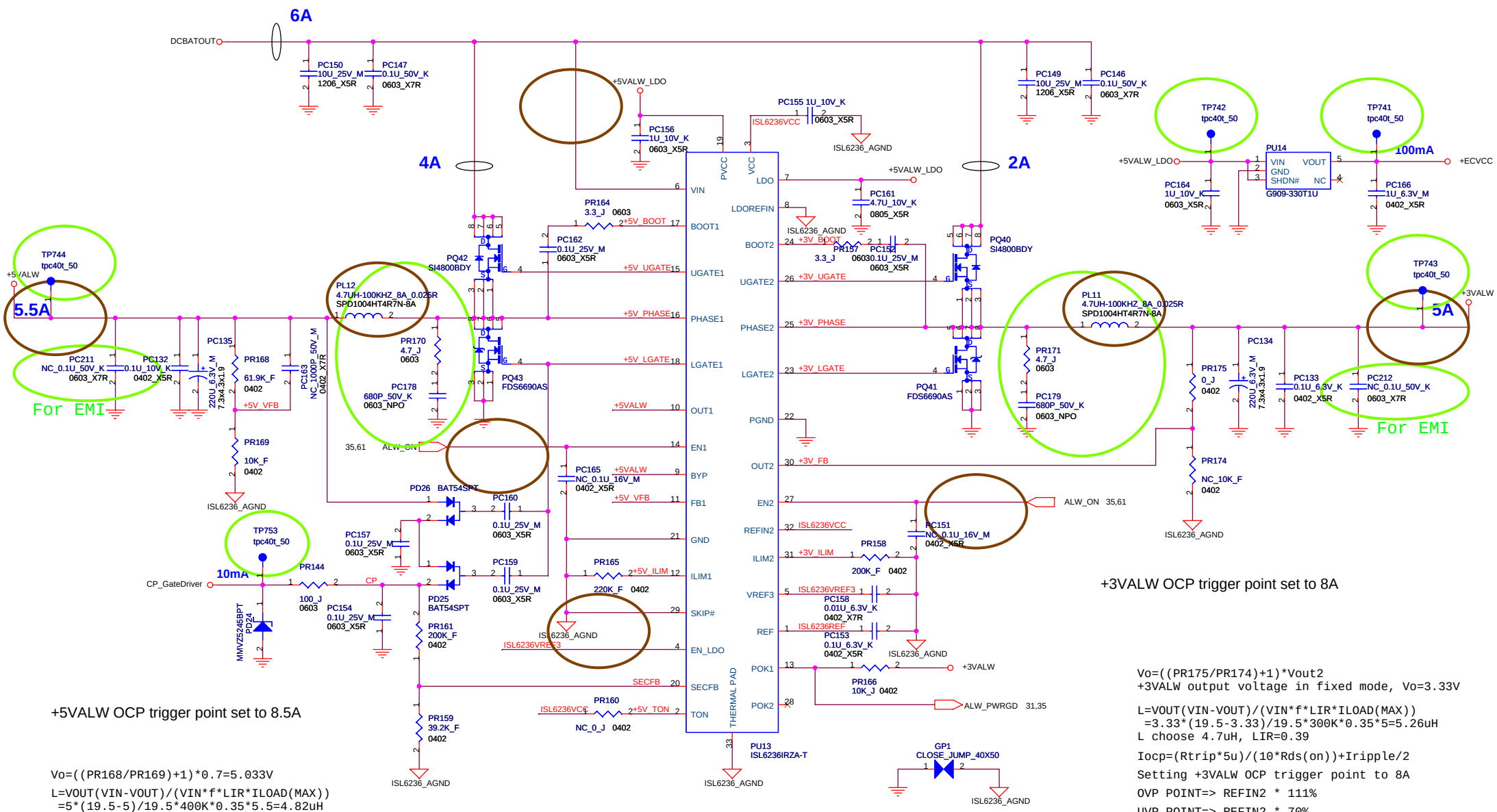

+5VALW OCP trigger point set to 8.5A

Vo=((PR168/PR169)+1)*0.7=5.033V

L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
=5*(19.5-5)/19.5*400K*0.35*5.5=4.82uH
L choose 4.7uH, LIR=0.36

Iocp=(Rtrip*5u)/(10*Rds(on))+Iripple/2

Setting +5VALW OCP trigger point to 8.5A

OVP POINT=> VFB * 111%

UVP POINT=> VFB * 70%

Switching Frequency = 400KHz

TON	Operating Frequence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

+3VALW OCP trigger point set to 8A

Vo=((PR175/PR174)+1)*Vout2
+3VALW output voltage in fixed mode, Vo=3.33V

L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
=3.33*(19.5-3.33)/19.5*300K*0.35*5=5.26uH
L choose 4.7uH, LIR=0.39

Iocp=(Rtrip*5u)/(10*Rds(on))+Iripple/2

Setting +3VALW OCP trigger point to 8A

OVP POINT=> REFIN2 * 111%

UVP POINT=> REFIN2 * 70%

Switching Frequency = 300KHz

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: SYS Power (+3_3V/+5V)

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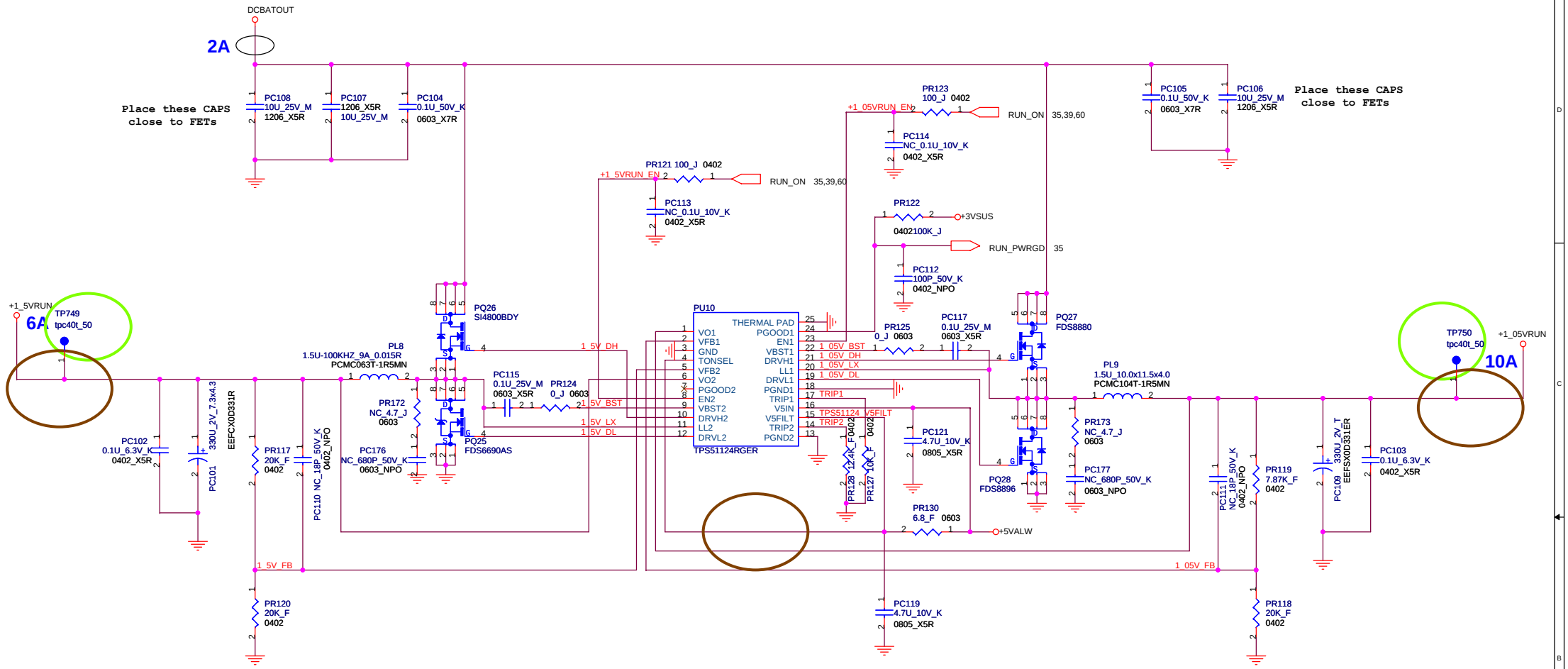

Setting +1_5VRUN OCP trigger point to 10.6A

Vo=((PR117/PR120)+1)*0.758=1.516V

L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
=1.5*(19.5-1.5)/19.5*420K*0.35*6=1.57uH
L choose 1.5uH, LIR=0.366

Iocp=(Rtrip*10u)/Rds(on)+Iripple/2

Setting +1_5VRUN OCP trigger point to 10.6A

OVP POINT=> VFB * 115%

UVP POINT=> VFB * 70%

Switching Frequency = 420KHz

Setting +1_05VRUN OCP trigger point to 14.6A

Vo=((PR119/PR118)+1)*0.758=1.056V

L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
=1.05*(19.5-1.05)/19.5*360K*0.35*10=0.79uH
L choose 1.5uH, LIR=0.18

Iocp=(Rtrip*10u)/Rds(on)+Iripple/2

Setting +1_05VRUN OCP trigger point to 14.6A

OVP POINT=> VFB * 115%

UVP POINT=> VFB * 70%

Switching Frequency = 360KHz

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	SYS Power(+1_5V/+1_05V)	
Size A3	Document Number M730-1-01	Rev 1.0
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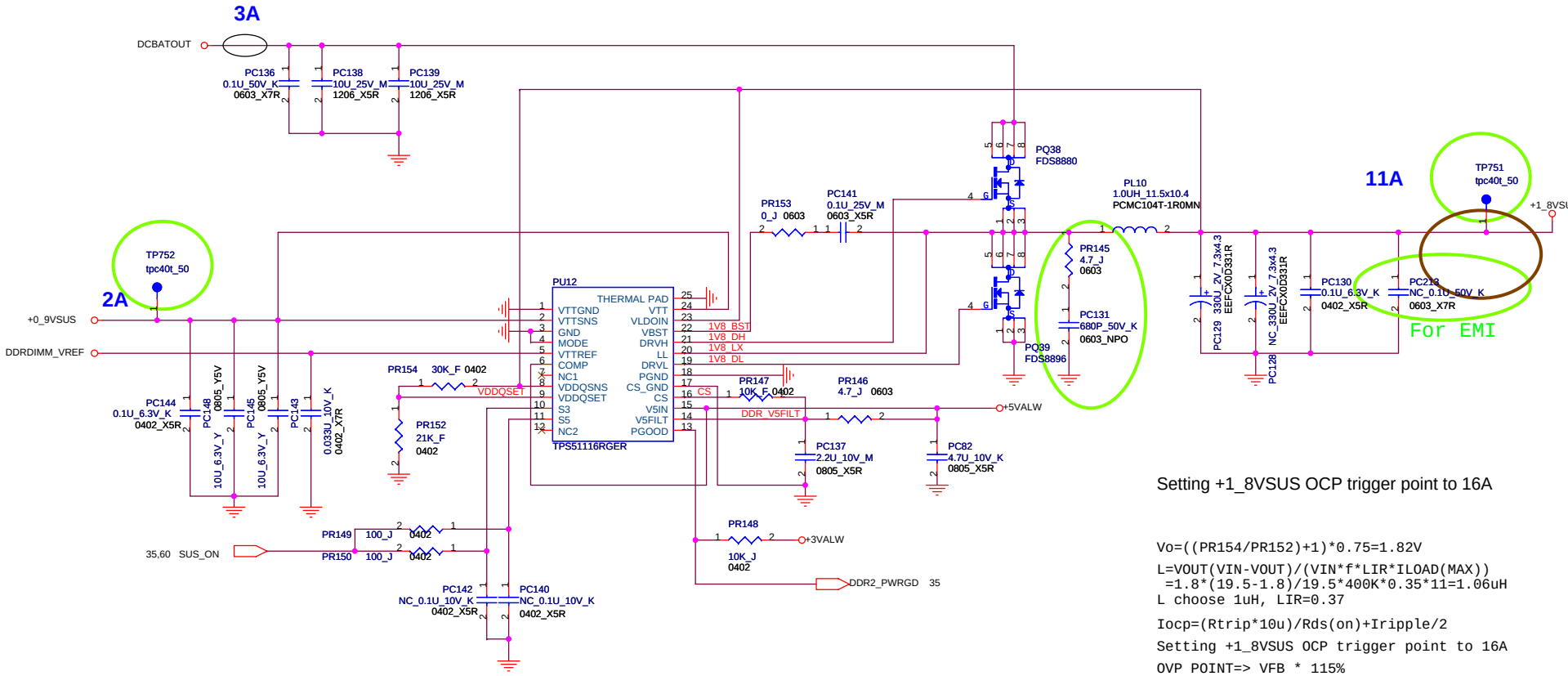


Setting +1_8VSUS OCP trigger point to 16A

Vo=((PR154/PR152)+1)*0.75=1.82V

L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
=1.8*(19.5-1.8)/19.5*400K*0.35*11=1.06uH
L choose 1uH, LIR=0.37

Iocp=(Rtrip*10u)/Rds(on)+Iripple/2

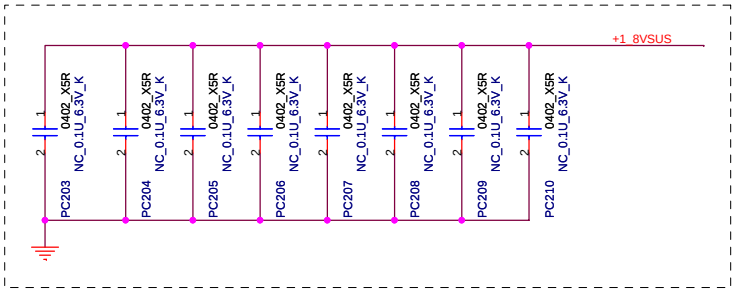
Setting +1_8VSUS OCP trigger point to 16A

OVP POINT=> VFB * 115%

UVP POINT=> VFB * 70%

Switching Frequency = 400KHz

For EMI



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR2 Power(+1_8V/+0_9V)	
Size A3	Document Number M730-1-01	Rev 1.0
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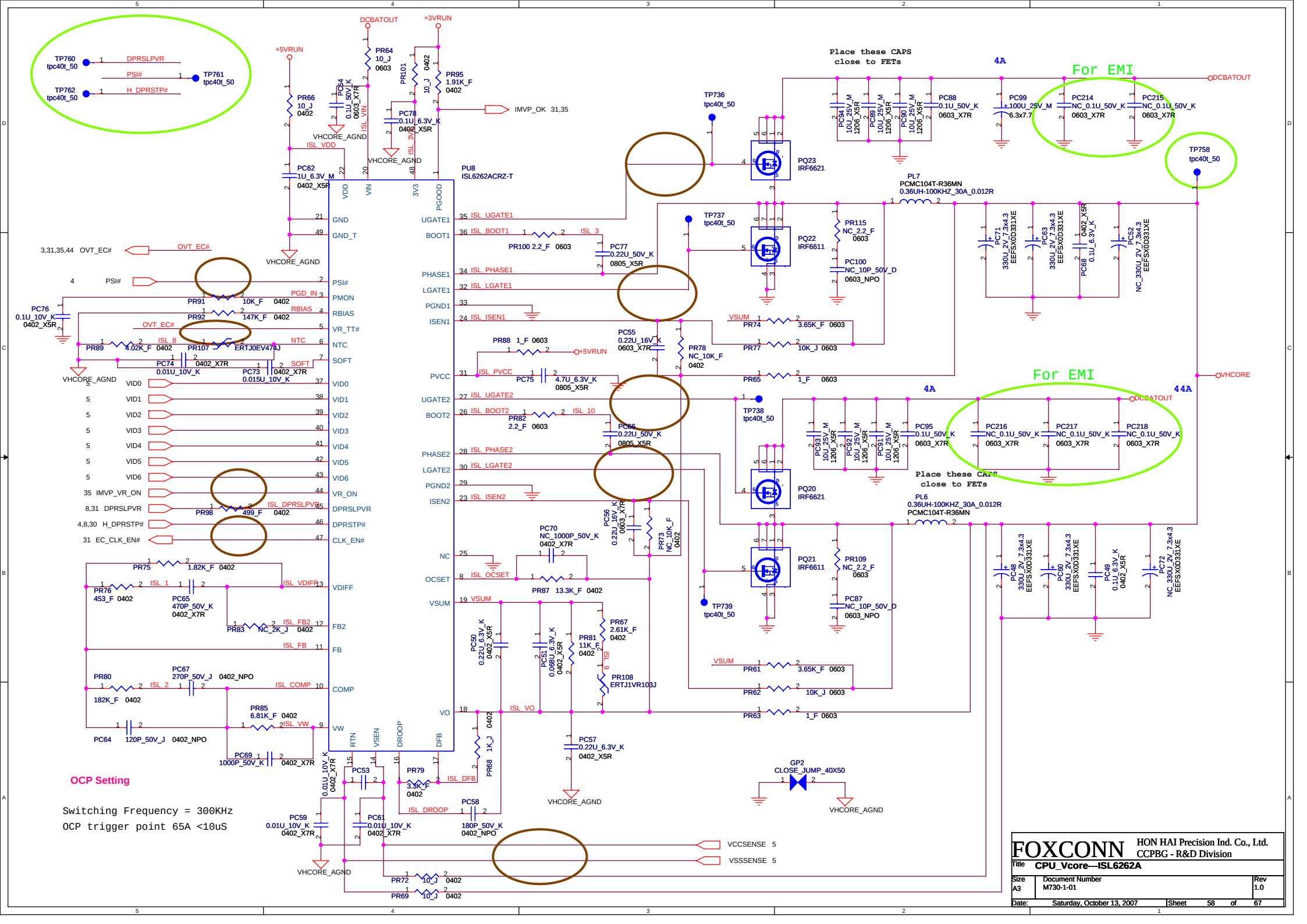

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CPU_Vcore---ISL6262A	
Size A3	Document Number M730-1-01	Rev 1.0
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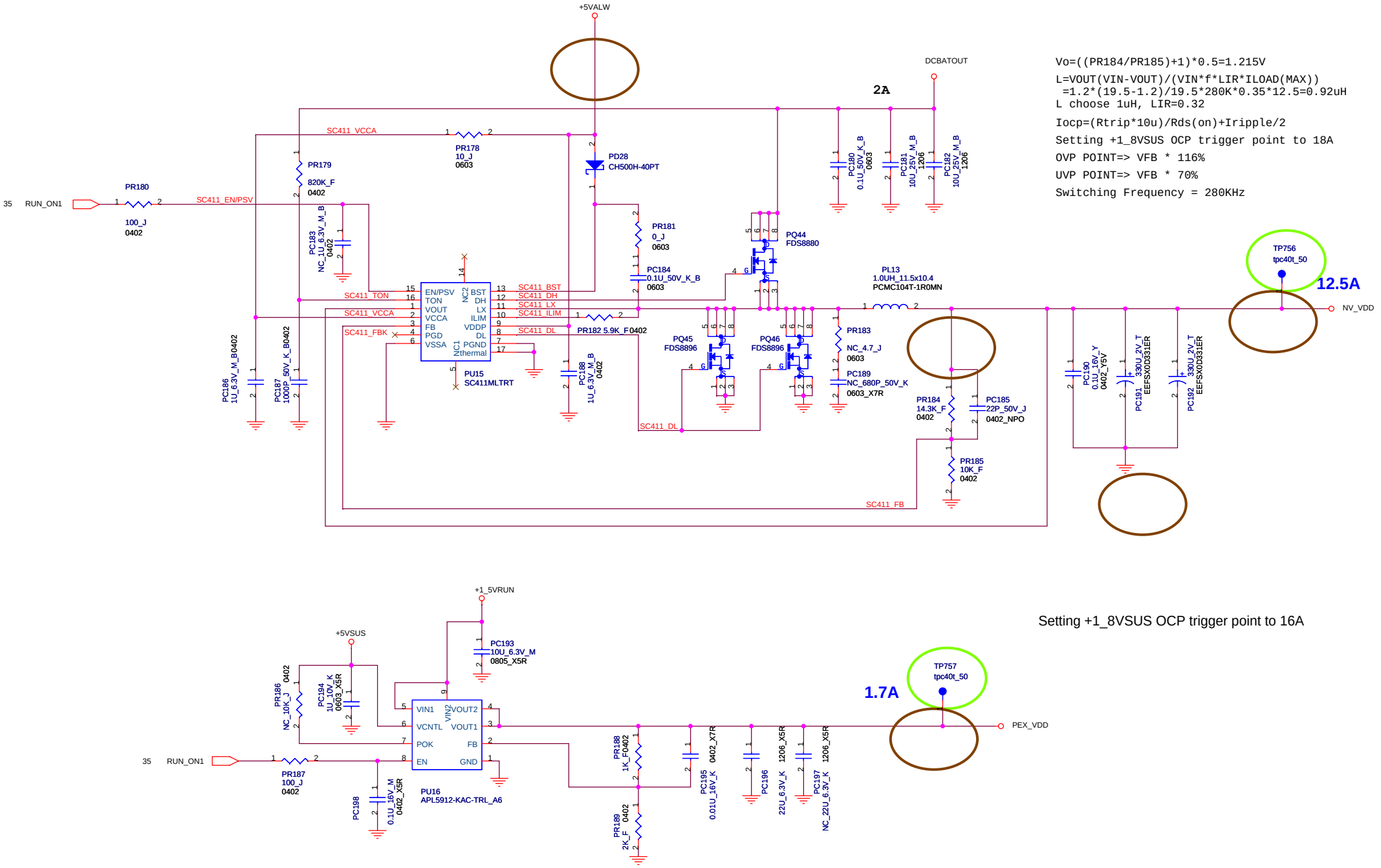

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: OVP protection

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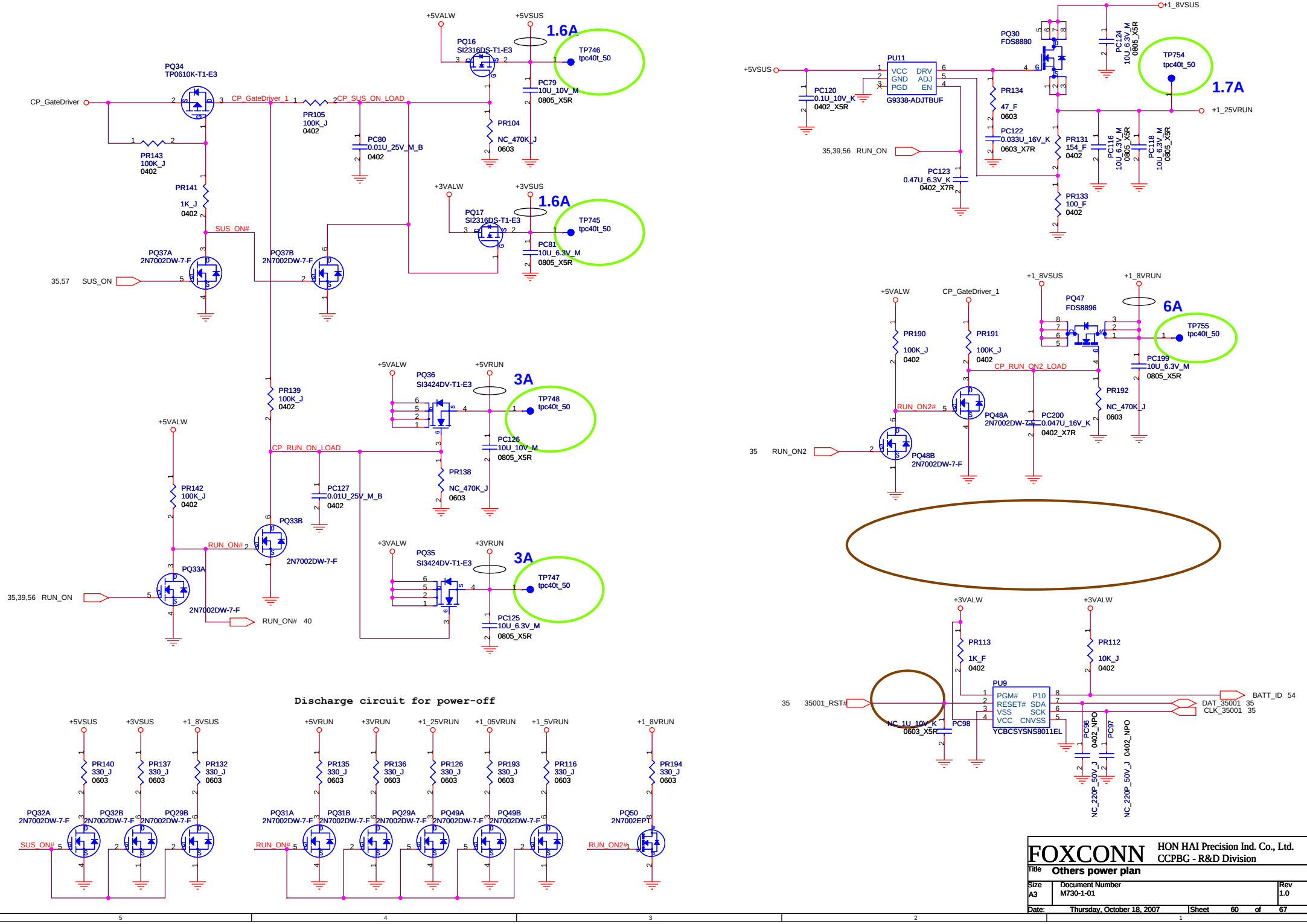
+5VALW
+5VSUS
1.6A
PQ16
SI2316DS-T1-E3
TP746
tpc40t_50
PQ34
TP0610K-T1-E3
CP_GateDriver
CP_GateDriver_1
CP_SUS_ON_LOAD
PR105
100K_J
0402
PC79
10U_10V_M
0805_X5R
PC80
0.01U_25V_M_B
0402
PR104
NC_470K_J
0603
PR143
100K_J
0402
PR141
1K_J
0402
+3VALW
+3VSUS
1.6A
PQ17
SI2316DS-T1-E3
TP745
tpc40t_50
SUS_ON#
PC81
10U_6.3V_M
0805_X5R
PQ37A
2N7002DW-7-F
PQ37B
2N7002DW-7-F
35,57 SUS_ON
+5VALW
+5VRUN
3A
PQ36
SI3424DV-T1-E3
TP748
tpc40t_50
PR139
100K_J
0402
PC126
10U_10V_M
0805_X5R
PR138
NC_470K_J
0603
CP_RUN_ON_LOAD
PC127
0.01U_25V_M_B
0402
+5VALW
PR142
100K_J
0402
PQ33B
2N7002DW-7-F
RUN_ON#
PQ33A
2N7002DW-7-F
35,39,56 RUN_ON
RUN_ON# 40
+3VALW
+3VRUN
3A
PQ35
SI3424DV-T1-E3
TP747
tpc40t_50
PC125
10U_6.3V_M
0805_X5R
+5VSUS
PU11
VCC DRV
GND ADJ
PGD EN
G9338-ADJTBUF
PC120
0.1U_10V_K
0402_X5R
PQ30
FDS8880
+1_8VSUS
PC124
10U_6.3V_M
0805_X5R
TP754
tpc40t_50
1.7A
+1_25VRUN
PR134
47_F
0603
PC122
0.033U_16V_K
0603_X7R
PR131
154_F
0402
PC116
10U_6.3V_M
0805_X5R
PC118
10U_6.3V_M
0805_X5R
35,39,56 RUN_ON
PC123
0.47U_6.3V_K
0402_X7R
PR133
100_F
0402
+1_8VSUS
+1_8VRUN
6A
PQ47
FDS8896
TP755
tpc40t_50
+5VALW
CP_GateDriver_1
PR190
100K_J
0402
PR191
100K_J
0402
PC199
10U_6.3V_M
0805_X5R
CP_RUN_ON2_LOAD
PR192
NC_470K_J
0603
RUN_ON2#
PQ48A
2N7002DW-7-F
PC200
0.047U_16V_K
0402_X7R
35 RUN_ON2
PQ48B
2N7002DW-7-F
+3VALW
+3VALW
PR113
1K_F
0402
PR112
10K_J
0402
PU9
PGM# P10
RESET# SDA
VSS SCK
VCC CNVSS
YCBCSYSNS8011EL
35 35001_RST#
NC_1U_10V_K
0603_X5R
PC98
BATT_ID 54
DAT_35001 35
CLK_35001 35
PC96
0402_NPO
PC97
0402_NPO
NC_220P_50V_J
NC_220P_50V_J
Discharge circuit for power-off
+5VSUS
+3VSUS
+1_8VSUS
PR140
330_J
0603
PR137
330_J
0603
PR132
330_J
0603
PQ32A
2N7002DW-7-F
PQ32B
2N7002DW-7-F
PQ29B
2N7002DW-7-F
SUS_ON#
+5VRUN
+3VRUN
+1_25VRUN
+1_05VRUN
+1_5VRUN
PR135
330_J
0603
PR136
330_J
0603
PR126
330_J
0603
PR193
330_J
0603
PR116
330_J
0603
PQ31A
2N7002DW-7-F
PQ31B
2N7002DW-7-F
PQ29A
2N7002DW-7-F
PQ49A
2N7002DW-7-F
PQ49B
2N7002DW-7-F
RUN_ON#
+1_8VRUN
PR194
330_J
0603
PQ50
2N7002EPT
RUN_ON2#
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
Others power plan
Size
A3
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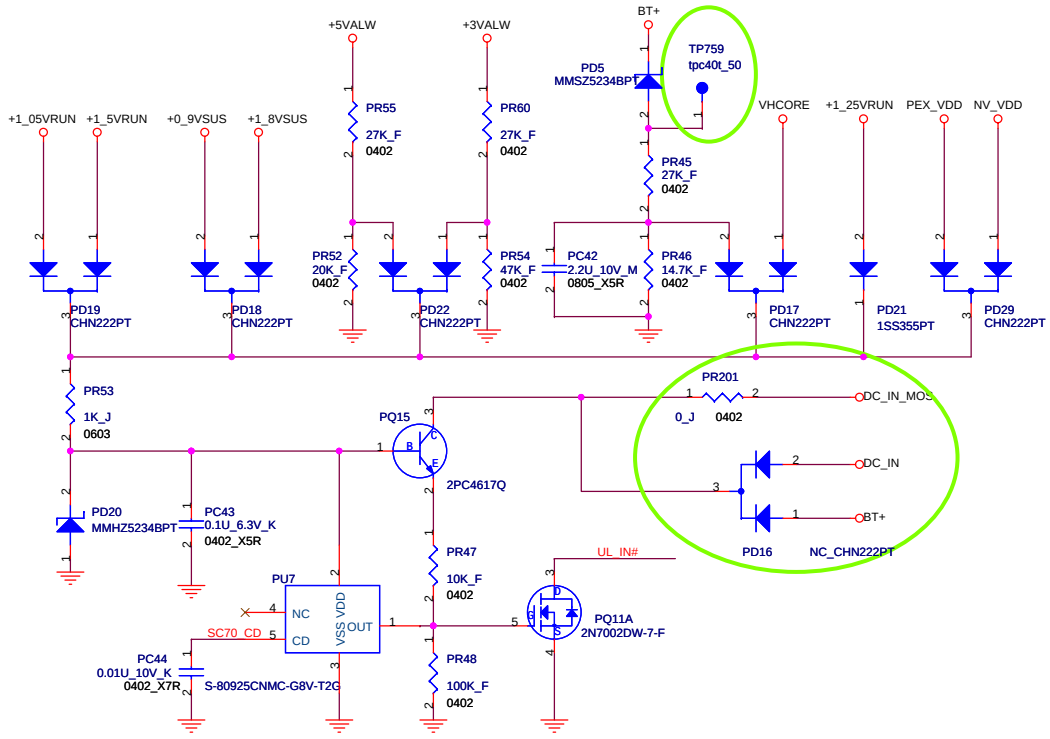
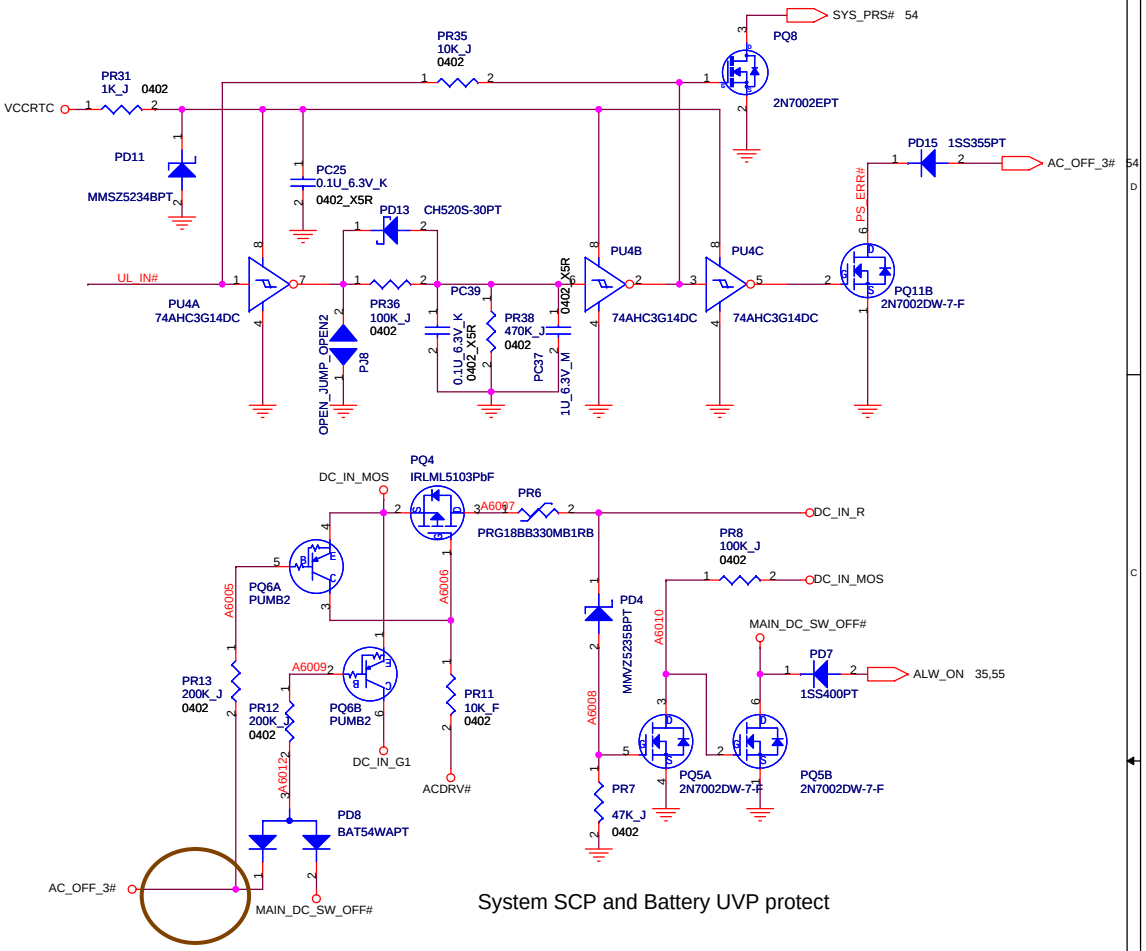
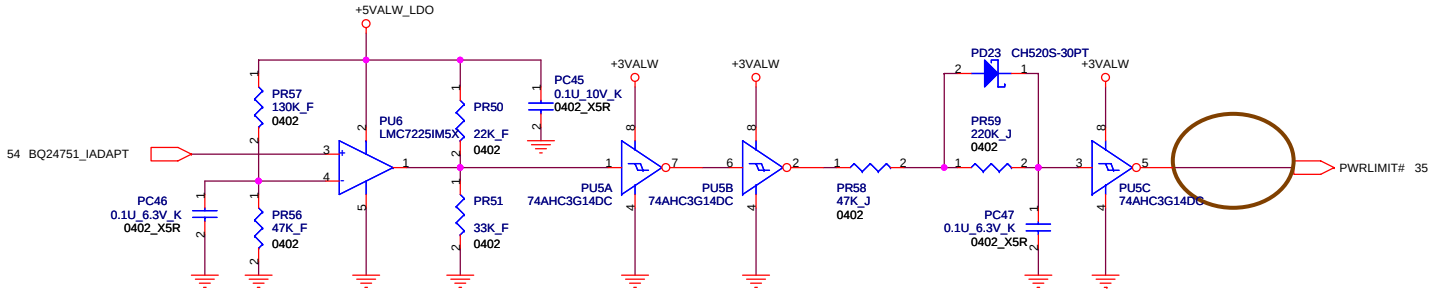




System SCP and Battery UVP protect



Setting PWRLIMIT# trigger point to 4.4A

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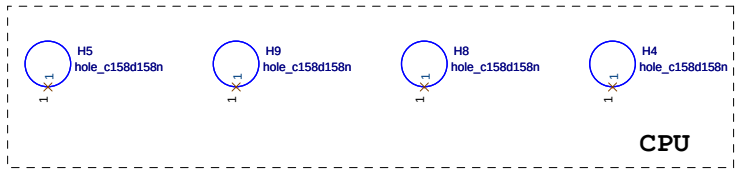

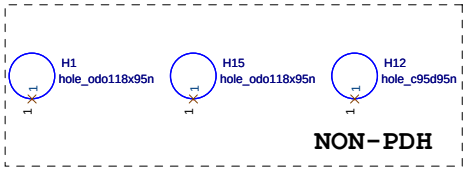

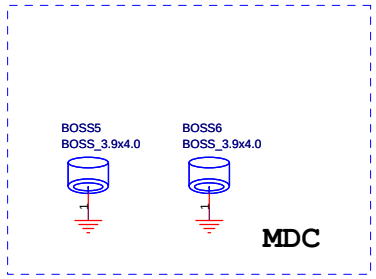

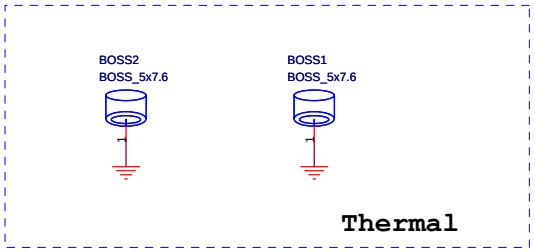

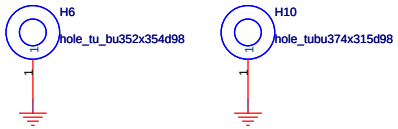

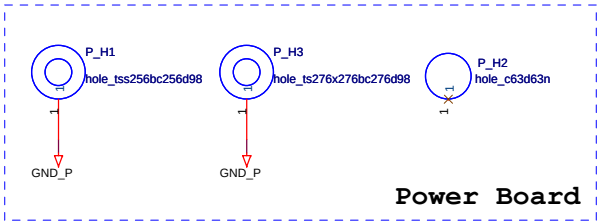

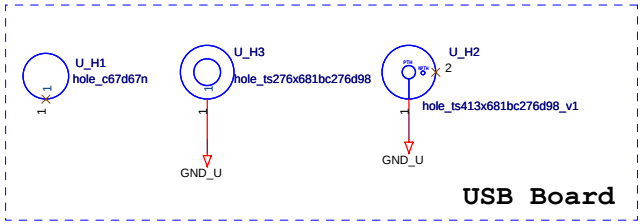

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
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M730 EVT

(2007/05/29)
Base on M720_SCHEMATIC_0528_1700.

(2007/05/30)
P.35 Add R607 for OVT_GFX#
P.23 Add R604,R605 and R606 for IFPC/D power

(2007/05/31)
P.40 Change R171 to 22ohm,C215 to 22uf.
P.42 Change C201,C202,C204 to X5R.
P.44 Delete U12,R183,R190 and C224 for remove memory thermal sensor solution.
P.9 Delete R366,R69,R74 and R81.
P.11 Delete Internal graphics power.
P.12 Delete Internal graphics power.
P.54 Change PR2 from 0.02_F 2512 to 0.015_F 2512 for 90W adapter application.
P.60 Change PQ47 from SI4800BDY to FDS8896
P.28 Add C702

(2007/06/04)
P.54 Change PR28 from 44.2K_F to 62K_F for setting constant power trigger point to 4.1A
P.57 Change PR147 from 6.8K_F to 10K_F for setting +1_8VSUS OCP trigger point to 16A
P.59 Change PR184 from 14K_F to 14.3K_F for setting NV_VDD to 1.215V
P.59 Change PR182 from 6.8K_F to 5.9K_F for setting NV_VDD OCP to 18A
P.59 Add PR197, PR198 0_J for NV_VDD feedback remote sense.
P.61 Change PR56 from 53.6K_F to 47K_F for setting PWRLIMIT trigger point to 4.4A.

(2007/06/05)
P.54 Change PQ18 and PQ19 from SI4800BDY to SI3424DV for layout space.
P.54 Change PC24 from 120pF 10% to 120pF 5% for purchase difficult.
P.60 Change PQ35 and PQ36 from SI4800BDY to SI3424DV for layout space.

(2007/06/08)
P.62 Add BOSS7 and BOSS8 for thermal request

(2007/06/14)
P.9 Change R97 to NC
P.9 Add R608/R609 and NC for LVDS_VREFH and LVDS_VREFL
P.8 Add TP731,TP732,TP733,TP734,TP735 for GFX_VID[3:0] and GFX_VR_EN

(2007/06/22)
P.19 Net I2CS_SDA & I2CS_SCL exchange with TP632 & TP633
P.22 Q40,Q41,Q42,Q43,R575,R576,R582 and R583 change from NC to mount for Nvidia save power function
P.24 Add and NC Q44,R610 for Nvidia save power function reserve
P.34 CAP7 change from 1C-41S0476-M000 to 1C-41R0476-M200 for layout convenient
P.62 Delete BOSS7,BOOS8 for ME request

(2007/06/23)
P.62 H14 change to 1X-HOLE000-0474 for ME request
P.62 H17 change to 1X-HOLE000-0473 for ME request

(2007/06/25)
P.62 Update H14 screw hole pad.
P.34 Change CAP7 to mount, and C275 to no mount for M720 HDD noise issue.
P.38 Update FeliCa pin define for M720 A'SSY issue.
P.49 Add C703,C704 for M720 LAN noise issue.

(2007/06/28)
P.57 Delete PR151 0ohm for application note.
P.58 Change PC67 from 270pF 10% to 270pF 5% for purchase difficult.
P.58 Add TP736, TP737, TP738 and TP739 test pin for application note.
P.56 PL8 change from 1L-DSPD100-4H02 to 1T-00001U5-0000 for layout convenient.

(2007/06/29)
P.22 Delete R569 and add R611 for mirror function off.
P.22 Modify address and command signals of U39 for mirror function off.

(2007/07/02)
P.22 R577,R578,R573,R574 change from 4.3k to 1.05k for nVidia's suggestion.
P.22 R582,R583,R575,R576 change from 4.02k to 1.82k for nVidia's suggestion.
P.22 R584,R585,R579,R580 change from 10k to 2.49k for nVidia's suggestion.
P.28 Add R612 and NC R596,U40 for GPIO3 of GPU is active high which is nVidia's suggestion.

(2007/07/03)
P.37 Change LED4 to HT-110YG for M720 LED issue.
P.51 Change R321,R323 to 51ohm,LED2,LED3 to HT-110Y for M720 LED issue.
P.48 Change F5~F8 to 2.6A poly-switch for M720 USB loading and noise issue.
P.52 Change CN23 to HS-8208E for M720 USB loading and noise issue.

(2007/07/05)
P.11 L28 change to 1uH/220mA for M720 component spec. issue.
P.08 Delete C509 for layout convenient.
P.46 Change L27 to SINKA OD6560T-E900T for purchase difficult.
P.28 NC R612 and mount R596,U40 for GPIO3 of GPU is set active low which is the same as MS90.
P.22 Swap data signals of VRAM for layout convenient.

(2007/07/06)
P.54 Change PC3 from mount to dummy for M720 application note.
P.54 Change PC38 from 4.7uF_25V 0805 to 1uF_25V 0603 for M720 application note.
P.54 Remove PR176 10_J for M720 application note.
P.54 Add PR199, PR200 1_J 1206 and PC201, PC202 4.7uF_25V 0805 for M720 DC_IN RC snubber circuit.
P.38 L25 change from BK1608LL121-T to TB160808B121 for purchase difficult.
P.54 PL1,PL3 change from BLM41PG600SN1L to BCMS451616A600-8A for purchase difficult.
P.05 CAP3 change from EEFSL0D331EY to 2R5TPE330M9 for purchase difficult.
P.12 CAP14 change from EEFSL0D331EY to 2R5TPE330M9 for purchase difficult.

(2007/07/09)
P.54 Change PR199, PR200 form 1206 to 1210 for M720 power rating safety.
P.05 CAP3 change back to EEFSL0D331EY for purchase difficult.
P.12 CAP14 change back to EEFSL0D331EY for purchase difficult.

(2007/07/10)
P.11 L28 change to EBLS2012-1R0M 0.25A for M720 component spec. issue.

(2007/07/11)
P.28 Add L55 for M720 EMI issue.
P.41 Delete VR2~VR5 and add C705~C708(NC) for M720 EMI issue.

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

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(2007/07/12)
P.54 Add PJ9 for application.
P.55 PR170,PR171,PC178,PC179 change to NC for application.
P.59 PR183,PC189 change to NC for application.
P.22 Change Q40~Q43 and R575,R576,R582,R583 to NC for customer request.
P.06 Add C709,C710 and reserve for EMI application.
P.57 Add PC203~PC210 and reserve for EMI application.
P.35 Add C711,C712 and reserve for EMI application.
P.38 Add C713 and reserve for EMI application.

(2007/07/13)
P.40 Add J2 for EMI application.

(2007/07/16)
P.42 Change C455,C445 to 10uF,R167,R149 to 20 Kohm for M720 MIC. THD+N issue.
P.35 Change R382 to mount and R390 to NC for system ID modification.
P.54 PR199,PR200 change to 1/3 W for PUR issue.

(2007/07/17)
P.37 Change LED4 to HT-110UYG for M720 MOR request.

(2007/07/20)
P.41 Change R105 to 6.2Kohm for M720 audio issue.

M730 DVT

(2007/07/27)
P.48 Delete F6,F8 for MOR's request.
P.61 Change PD16 from mount to NC, add PR201 0ohm for application.
P.06 Modify R350 pin1 connection from GND to +3VRUN for GPU select 27MHz issue.

(2007/08/13)
P.51 Change LED2,LED3 from HT-110Y to HT-110UY
Change R319,R322 from 47ohm to 120ohm and R321 from 51ohm to 120ohm
Change R496 from 47ohm to 100ohm for M720 LED brightness request from MOR

(2007/08/14)
Add test pin TP740~TP772 for power test jig.

(2007/08/17)
P.34 Add CAP21 for +5VRUN noise issue of ODD
P.41 Add CAP22 for +5VAMP noise issue of CODEC
C127 change from no mount to mount for +5VAMP noise issue of CODEC
P.25 Add C714/C715 for PEX_PLL_AVDD/PEX_PLL_DVDD noise issue

(2007/08/23)
P.38 NC R152,R151,F2,L25,C185,C186,CN6 for no Felica SKU
P.44 U27 change from GMT G781-1P8f to SMSC EMC1402-2-ACZL for Penryn CPU concern

(2007/08/25)
P.62 H3 change to 1X-HOLE000-0519 for ME's request

(2007/08/28)
P.55 PL11,PL12 change from SPD1004HT4R7N-8A to PCMC063T-4R7MN
for ME interference issue.
P.55 PR170,PR171,PC178,PC179 change from NC to mount for EMI issue.
P.57 PR145 change from 3.3ohm to 4.7ohm and PC131 change from 1000P to 680P
for EMI issue.

(2007/08/28)
P.35 Add and reserve C716,C717,C718 0603 cap for EMI solution.
P.55 Add and reserve PC211,PC212 0603 cap for EMI solution.
P.57 Add and reserve PC213 0603 cap for EMI solution.
P.58 Add and reserve PC214~PC218 0603 cap for EMI solution.

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(2007/09/27)
P.54 Delete PJ9 for application.
P.54 Change PD6 from mount to NC for UL_Lock issue.
P.54 Delete PR25, PR41, PR42 for application.
P.55 PL11,PL12 change from PCMC063T-4R7MN to SPD1004HT4R7N-8A
for MOR request.
P.55 Delete PJ4, PJ5 for application.
P.55 Delete PR155, PR156, PR162, PR163, PR167 for application.
P.56 Delete PJ1, PJ2 for application.
P.56 Delete PR129 for application.
P.57 Delete PJ3 for application.
P.58 Delete PR70, PR71, PR84, PR86, PR90, PR93, PR94, PR96, PR97, PR99,
PR102 for application.
P.59 Delete PJ6, PJ7 for application.
P.59 Delete PR177, PR197, PR198 for application.
P.60 Delete PR110, PR111, PR114 for application.
P.61 Delete PR20, PR49 for application.

(2007/10/17)
P.25 Add netname "J6" for U35 Pin J6 for application.

(2007/10/19)
P.47 Change R235 from 47ohm to 68ohm for MS Card Media-C
MS_CLK undershoot issue

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