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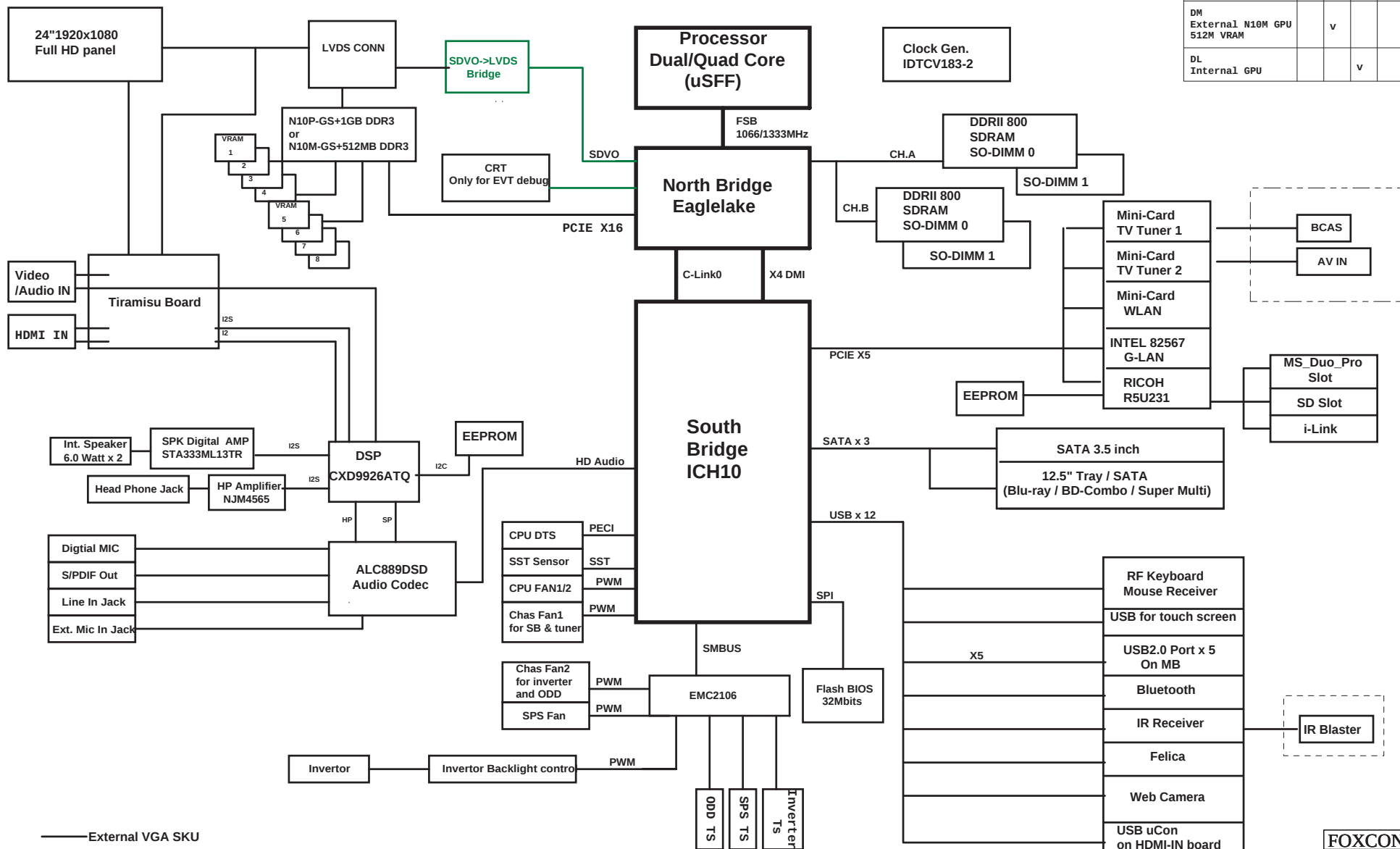
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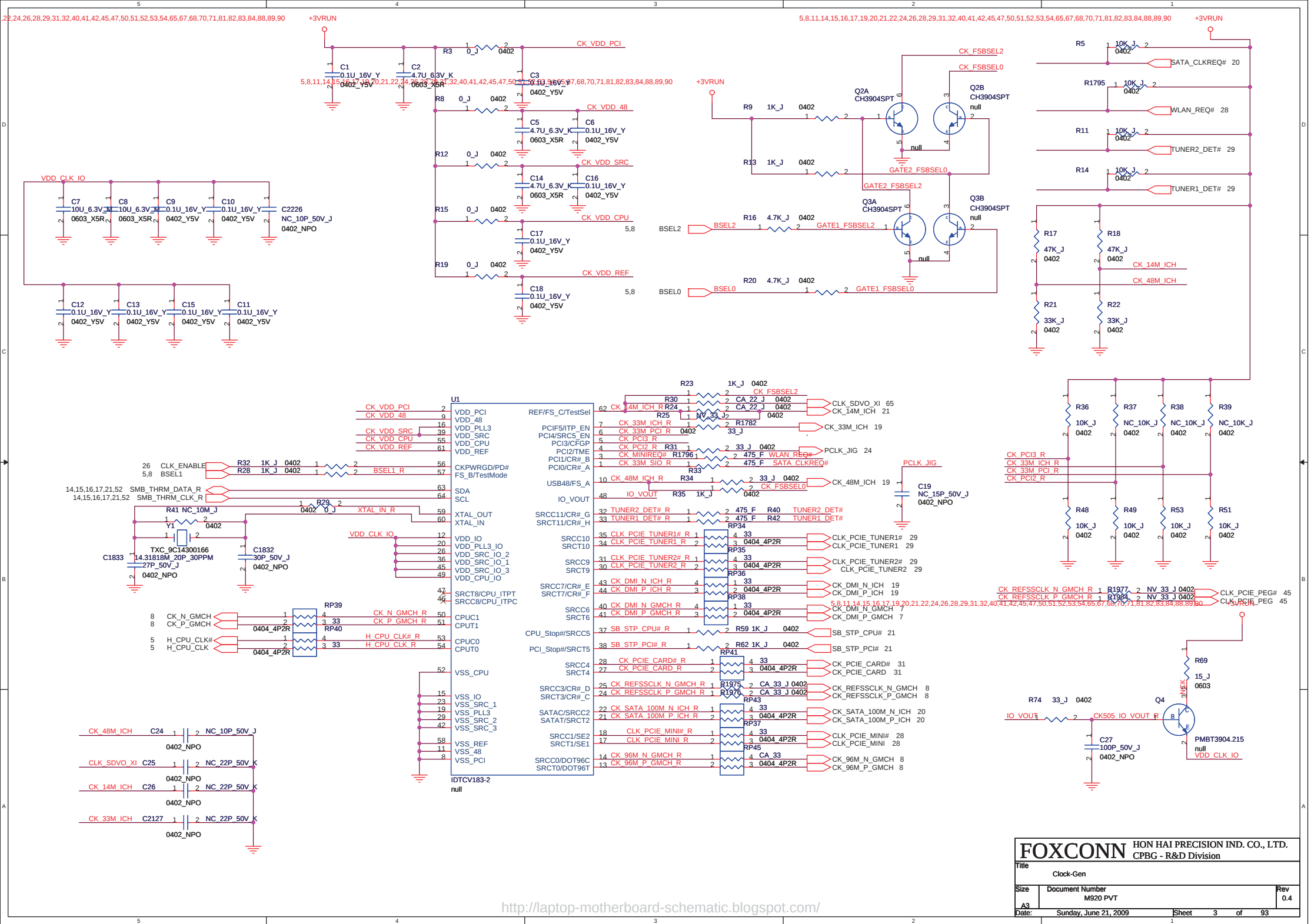
M920 Block Diagram (24" Wide Screen)

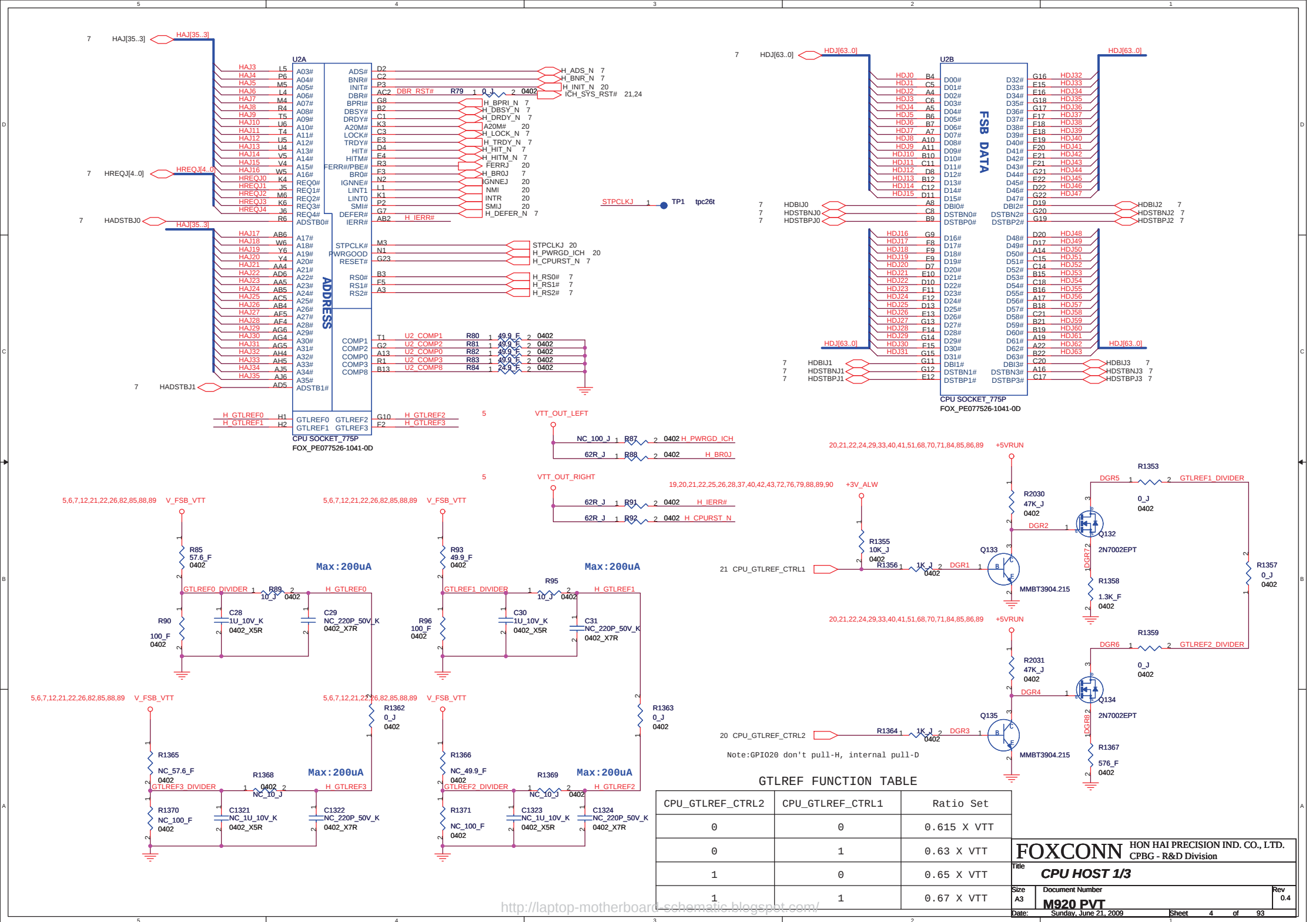
SKU	Ahead-value	NC-	NV-	CA-	NP-	NM-
DH External N10P GPU 16 VRAM			v		v	
DM External N10M GPU 512M VRAM			v			v
DL Internal GPU				v		

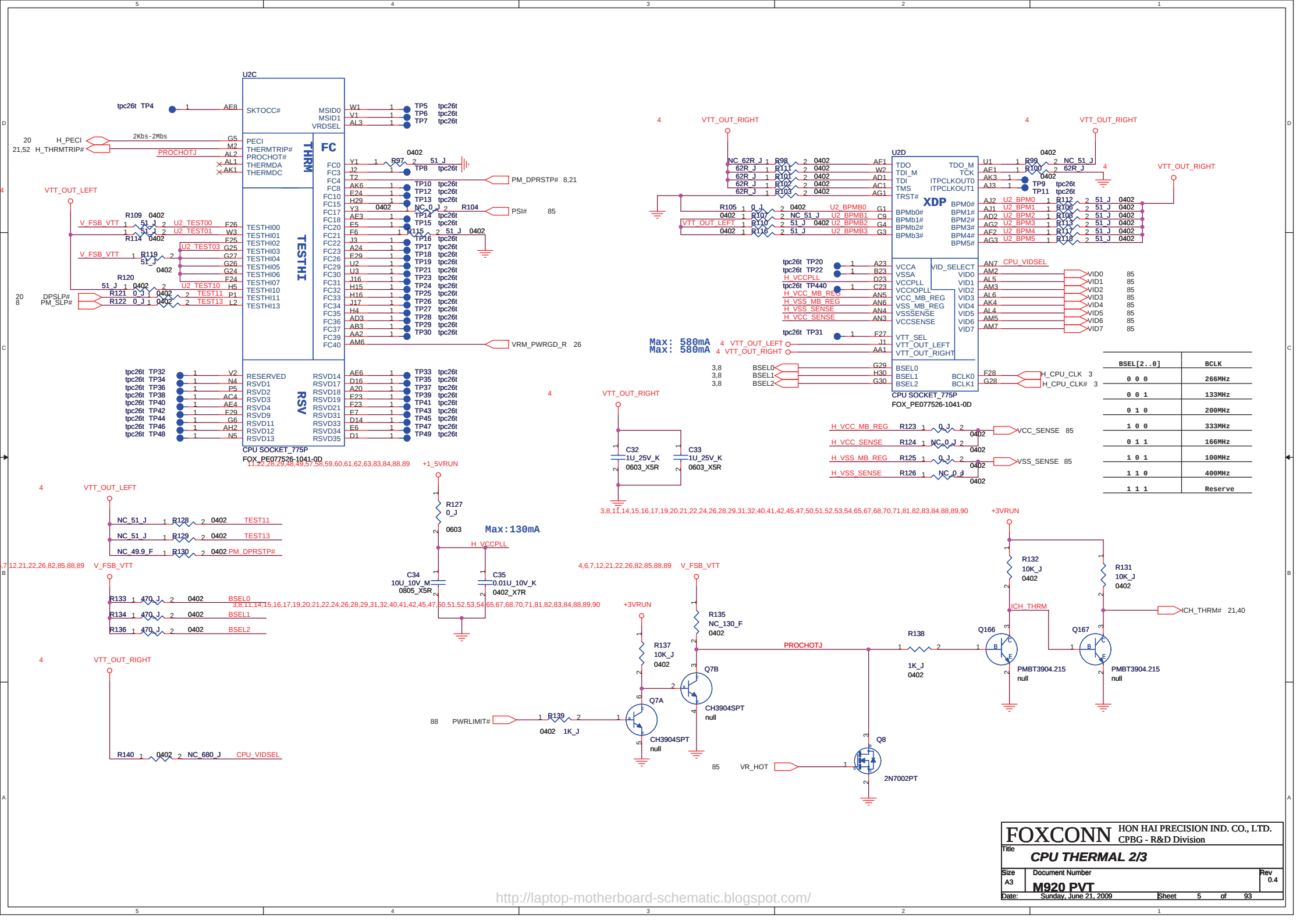


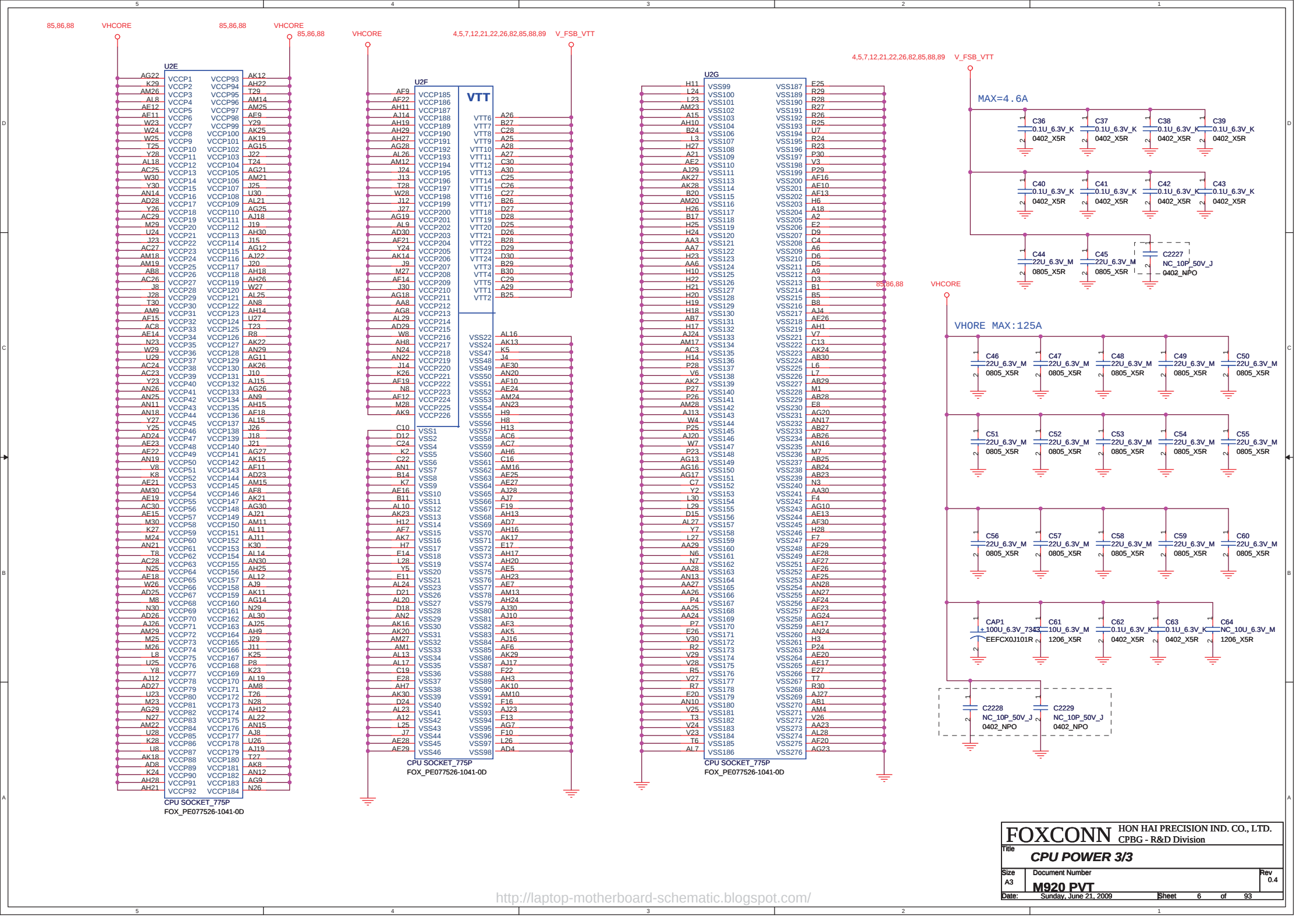
— External VGA SKU
— Internal VGA SKU

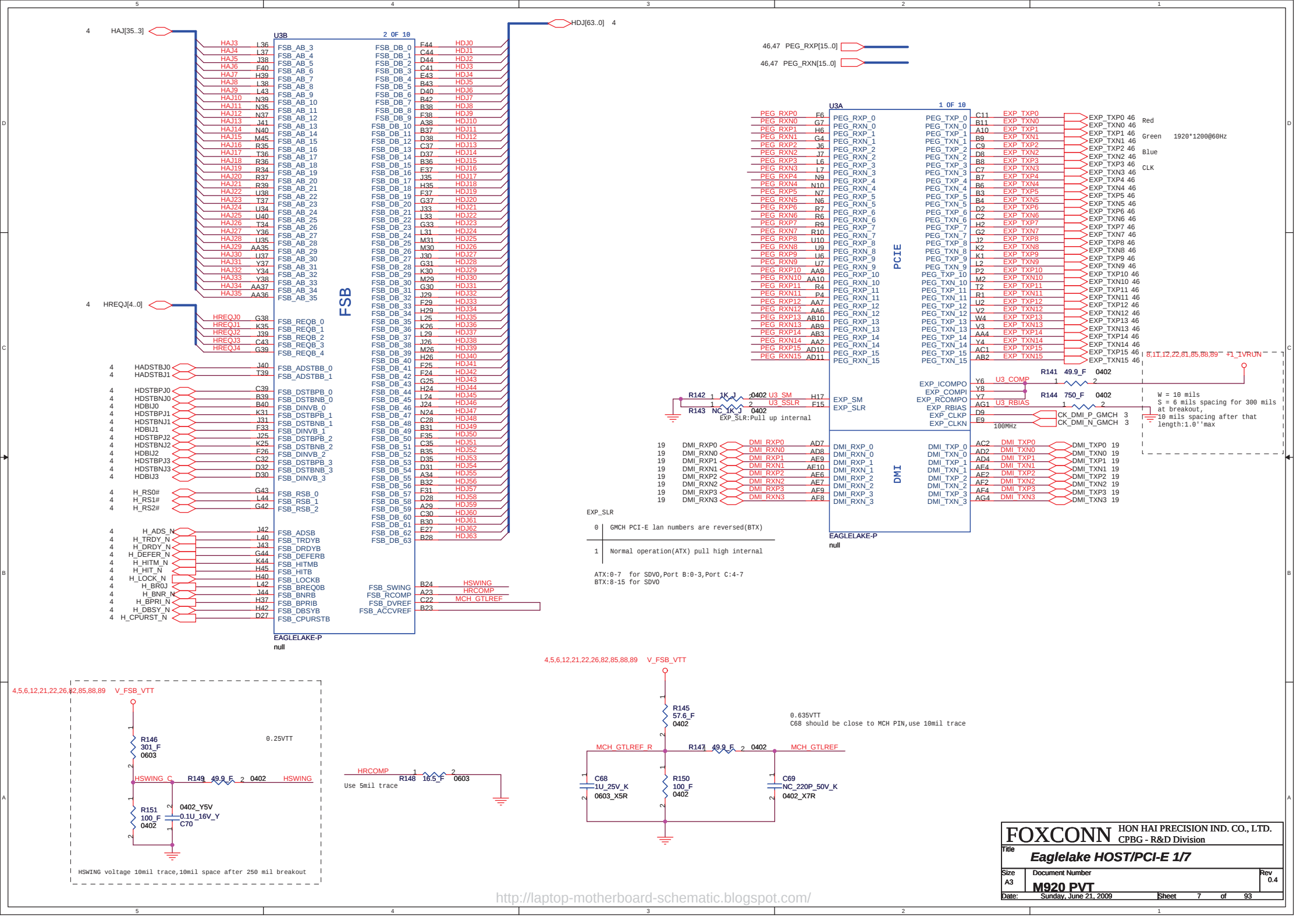
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Block Diagram		CPBG - R&D Division	
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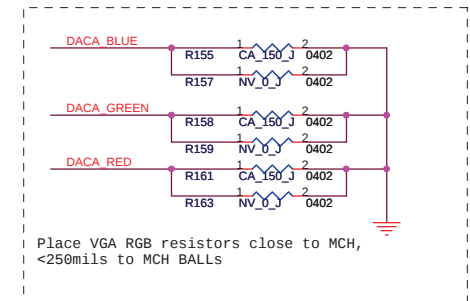
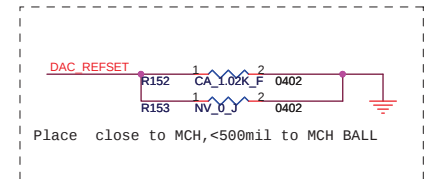
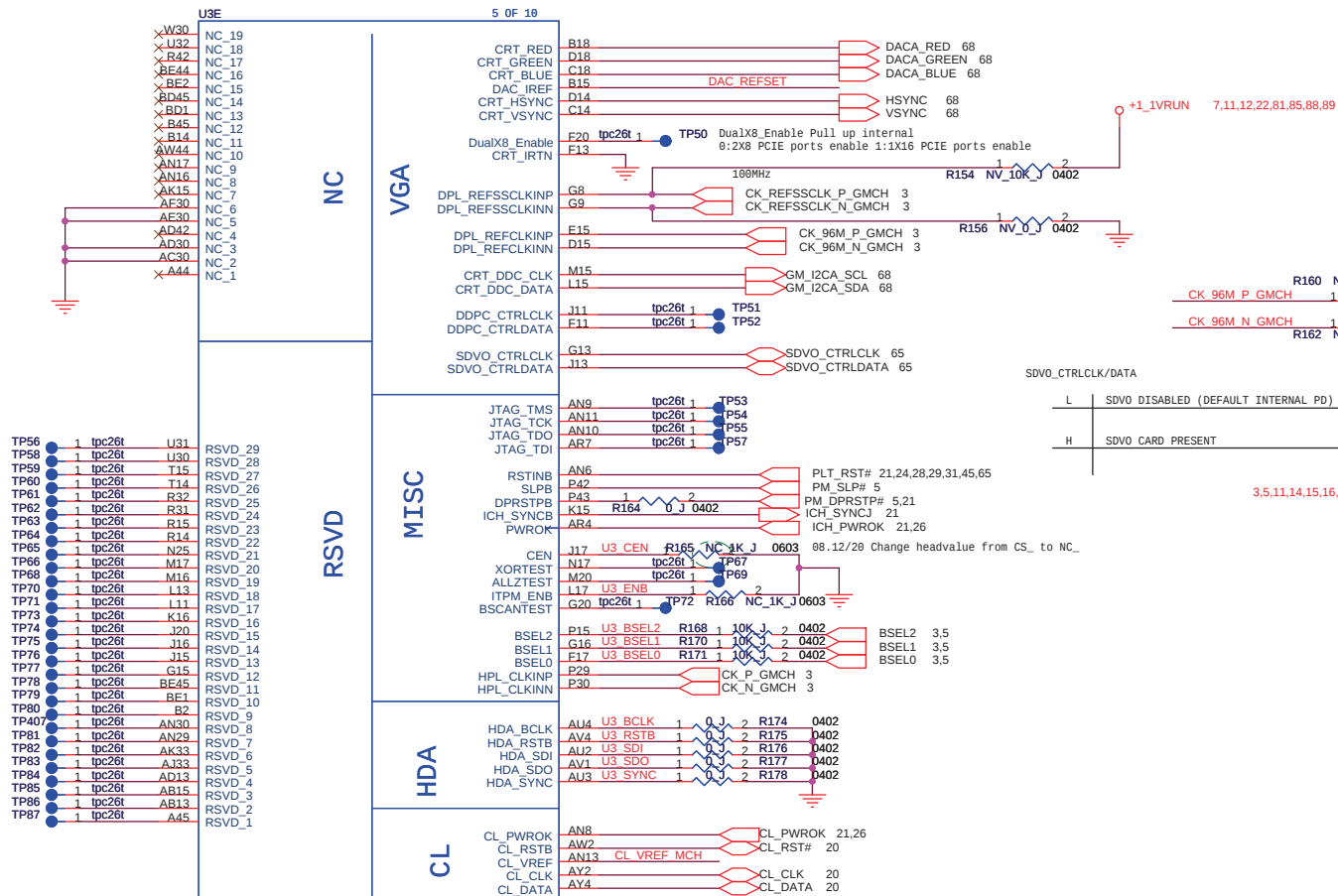




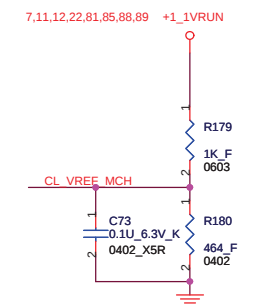
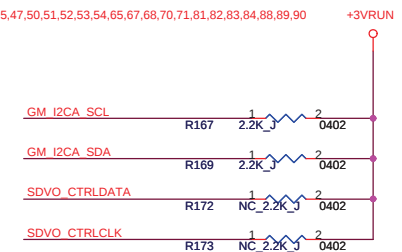


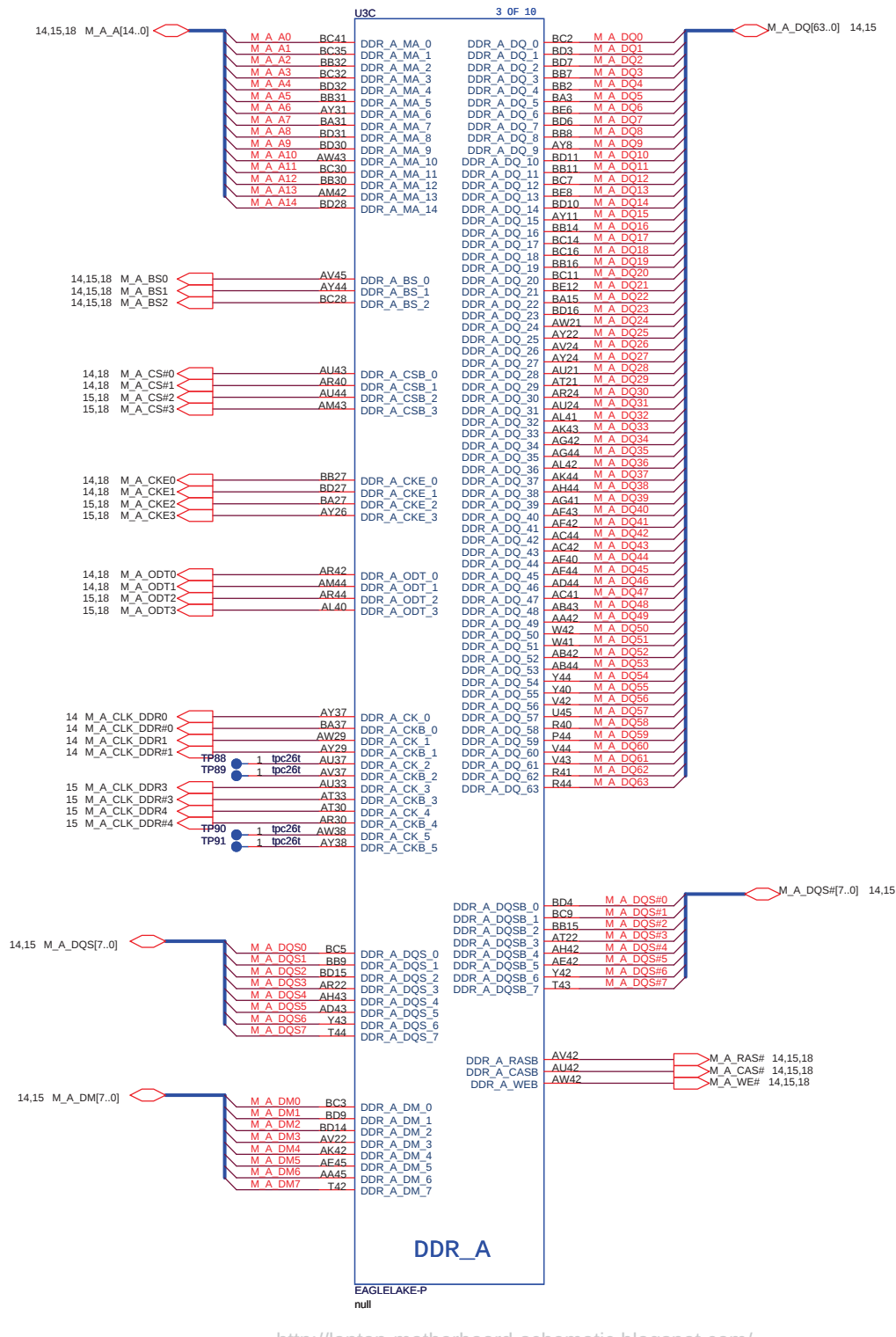


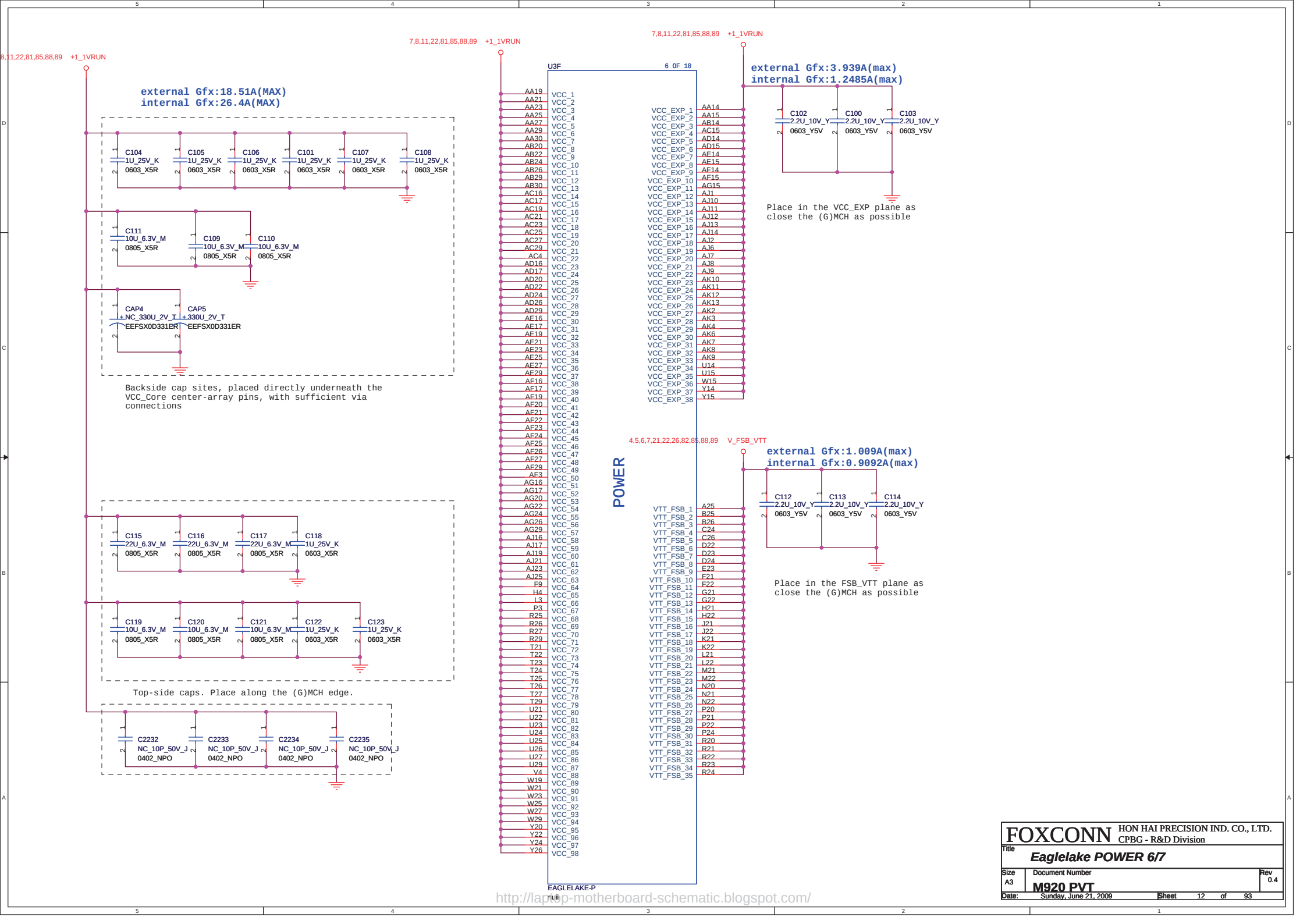




3,5,11,14,15,16,17,19,20,21,22,24,26,28,29,31,32,40,41,42,45,47,50,51,52,53,54,65,67,68,70,71,81,82,83,84,88,89,90







external Gfx:18.51A(MAX)
internal Gfx:26.4A(MAX)

external Gfx:3.939A(max)
internal Gfx:1.2485A(max)

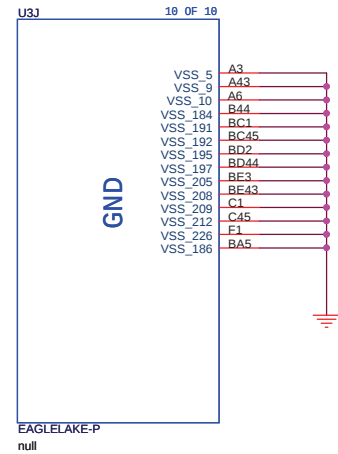
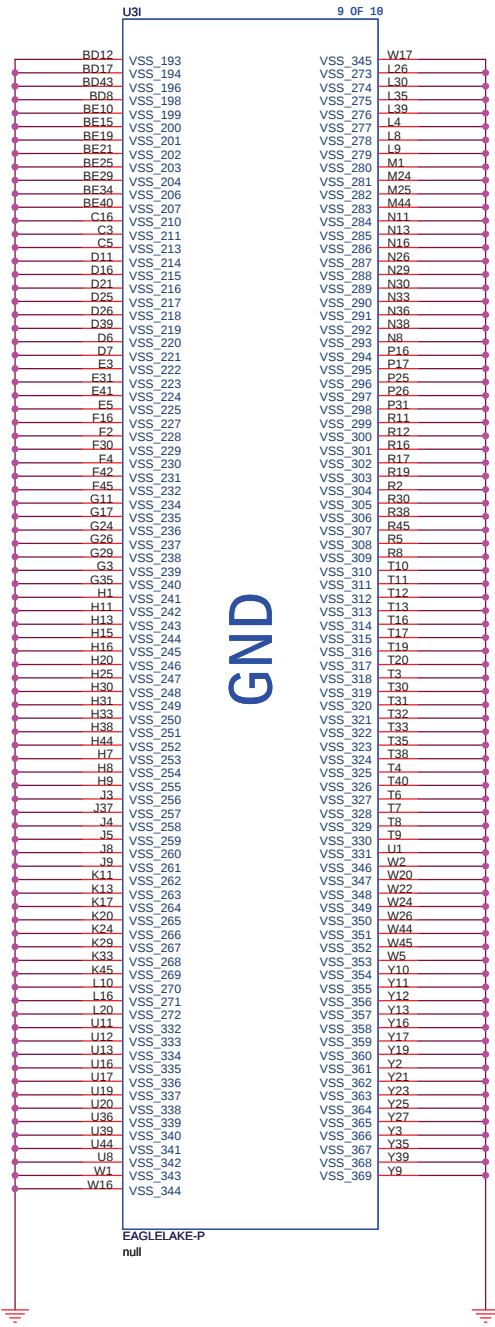
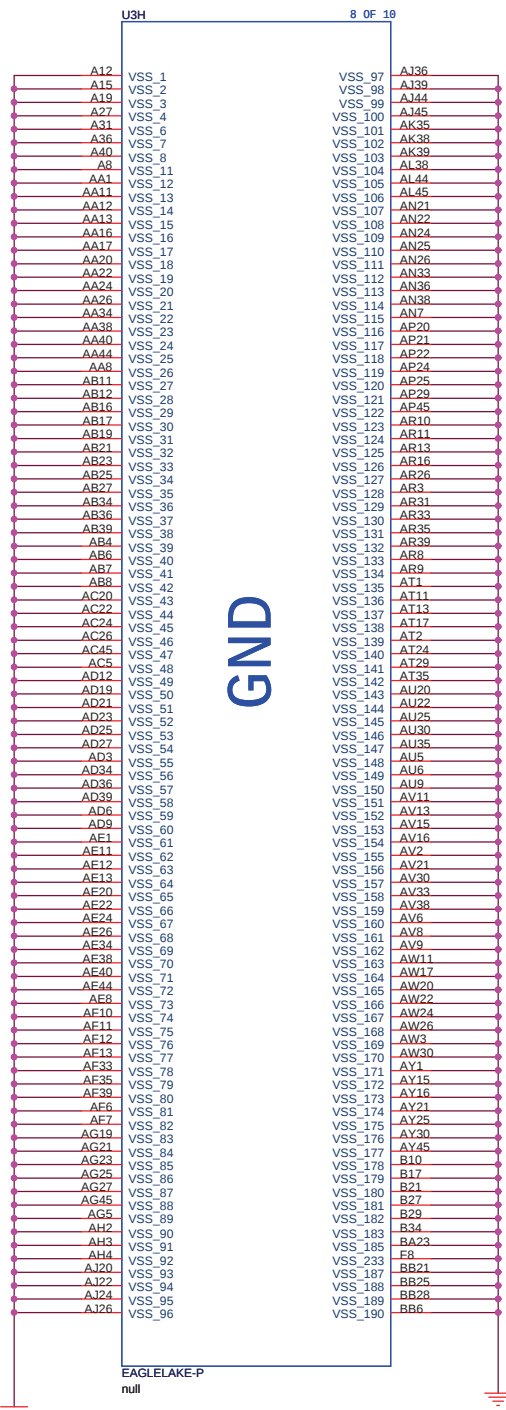
Place in the VCC_EXP plane as
close the (G)MCH as possible

Backside cap sites, placed directly underneath the
VCC_Core center-array pins, with sufficient via
connections

external Gfx:1.009A(max)
internal Gfx:0.9092A(max)

Place in the FSB_VTT plane as
close the (G)MCH as possible

Top-side caps. Place along the (G)MCH edge.



15

DDR2_VREF_A

10,11,15,16,17,51,80,88,89

+1.8V_S3_SUS

10,11,15,16,17,51,80,88,89

+1.8V_S3_SUS

1.8V per DIMM=4.06A

0.1 μ F and 2.2 μ F
placed close to VREF
pins

9,18 M_A_CKE0

9,15,18 M_A_BS2

9,15,18 M_A_BS0

9,15,18 M_A_WE#

9,15,18 M_A_CAS#

9,18 M_A_CS#1

9,18 M_A_ODT1

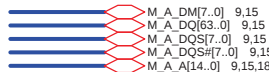
3,15,16,17,21,52 SMB_THRM_DATA R
3,15,16,17,21,52 SMB_THRM_CLK R



DIMM 0

DDR2_200P
FOX_AS0A426-N2RN-4F

SMBus Address: A0(W)/A1(R)



10,11,15,16,17,51,80,88,89

+1.8V_S3_SUS

10,16,80

DDR2_VREF

DDR2_VREF_A

0.1u_16V_M

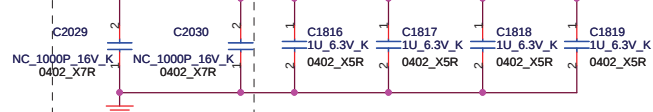
0402_X5R

Close to DIMM

10,11,15,16,17,51,80,88,89

+1.8V_S3_SUS

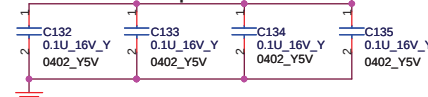
Place these Caps near So-Dimm0.



10,11,15,16,17,51,80,88,89

+1.8V_S3_SUS

Place these Caps near So-Dimm0.

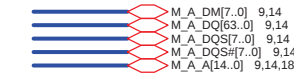
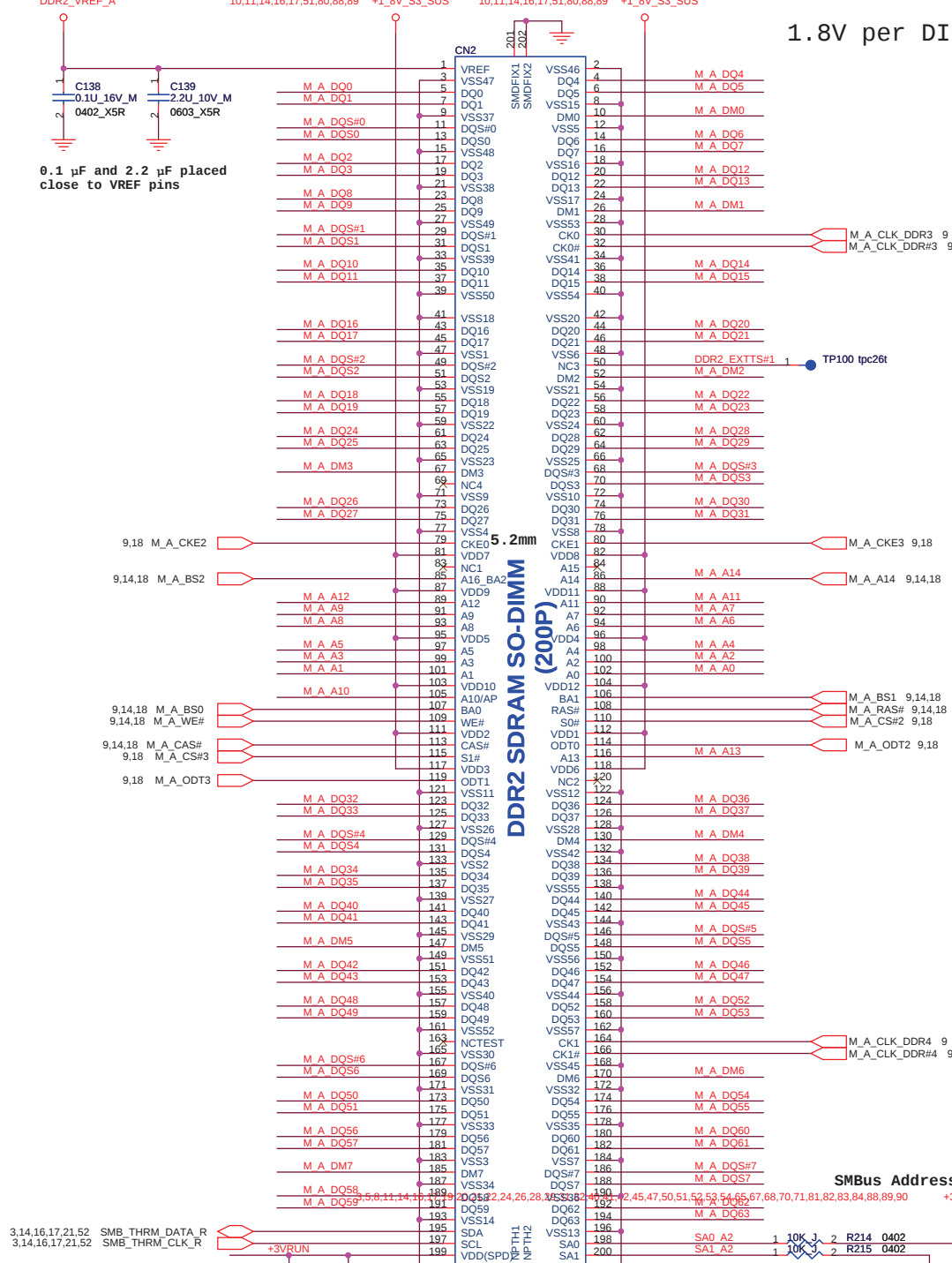


FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
File			
DDRII(CHA DIMM0) 1/4			
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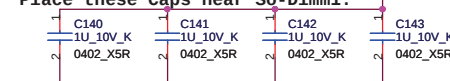
DDR2_VREF_A 10,11,14,16,17,51,80,88,89 +1.8V_S3_SUS 10,11,14,16,17,51,80,88,89 +1.8V_S3_SUS

1.8V per DIMM=4.06A

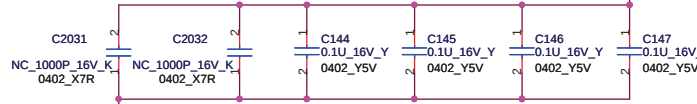
0.1 pF and 2.2 pF placed close to VREF pins



Place these Caps near So-Dimm1.



Place these Caps near So-Dimm1.



SMBus Address: A2(W)/A3(R)

DIMM_1 <http://laptop-motherboard-schematic.blogspot.com/>

FOXCONN HON HAI PRECISION IND. CO., L.TD. CPBG - R&D Division		
File: DDRII(CHA DIMM1) 2/4		
Size: A3	Document Number: M920 PVT	Rev: 0.4
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1.8V per DIMM=4.06A

0.1 μ F and 2.2 μ F
placed close to VREF
pins

Close to DIMM

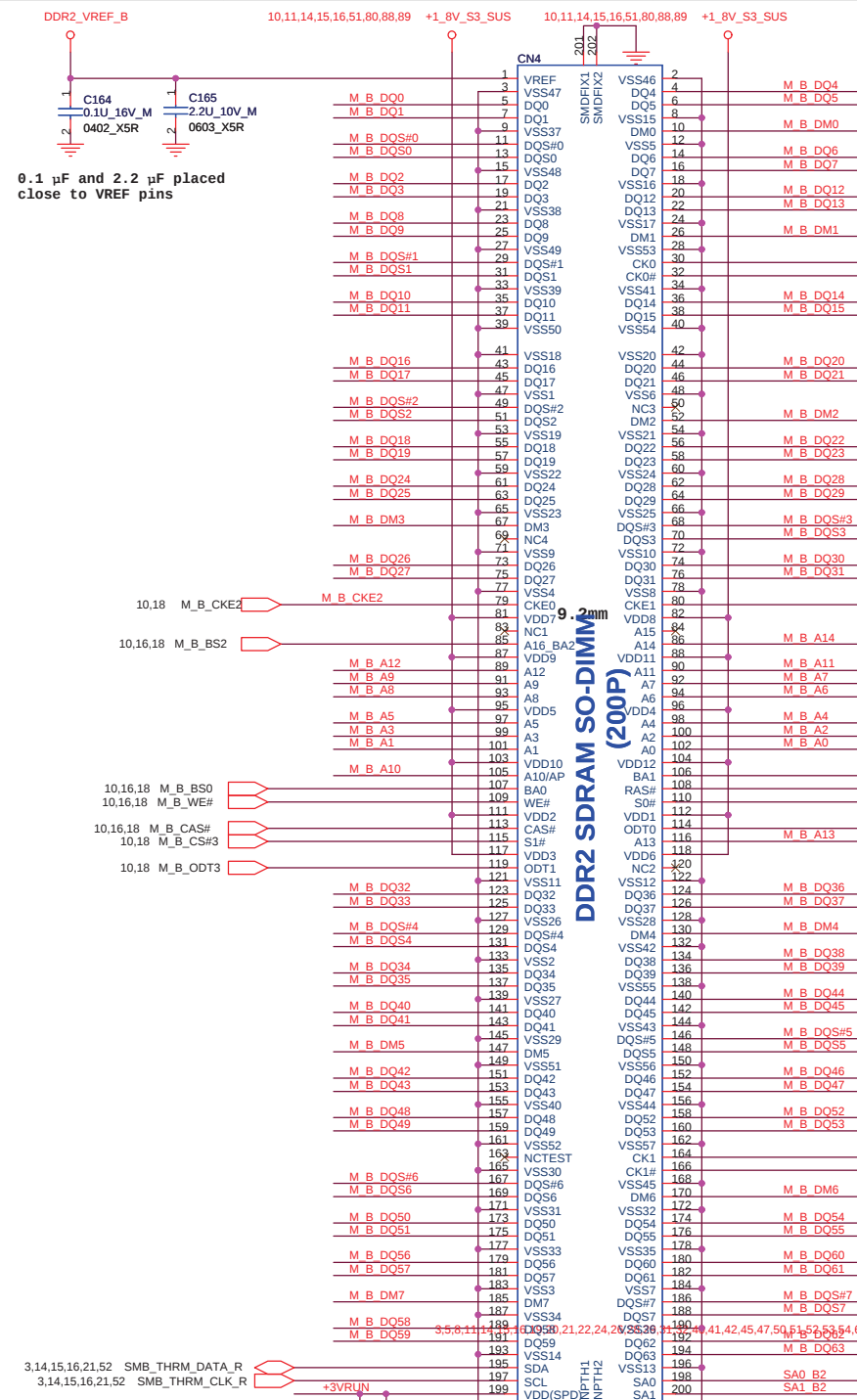
Place these Caps near So-Dimm0.

Place these Caps near So-Dimm0.

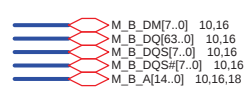
SMBus Address: A4(W)/A5(R)

DIMM_0

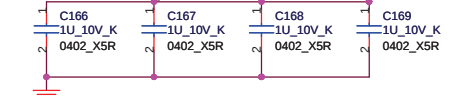
<http://laptop-motherboard-schematic.blogspot.com/>



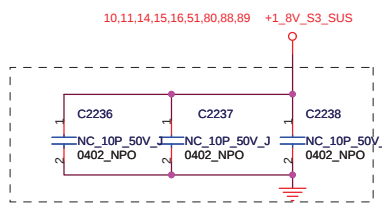
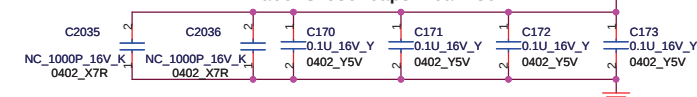
1.8V per DIMM=4.06A



Place these Caps near So-Dimm1.



Place these Caps near So-Dimm1.



SMBus Address: A6(W)/A7(R)

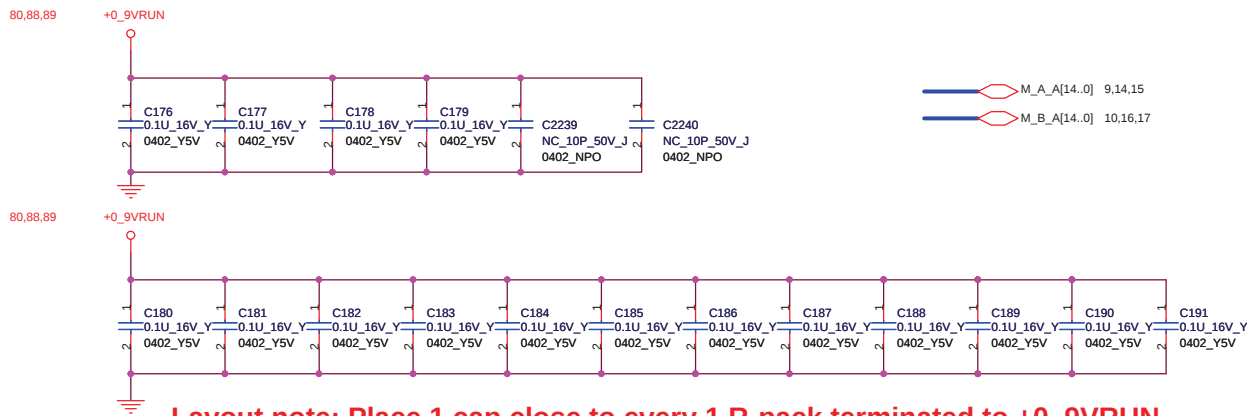
3,14,15,16,21,52 SMB_THRM_DATA_R
3,14,15,16,21,52 SMB_THRM_CLK_R



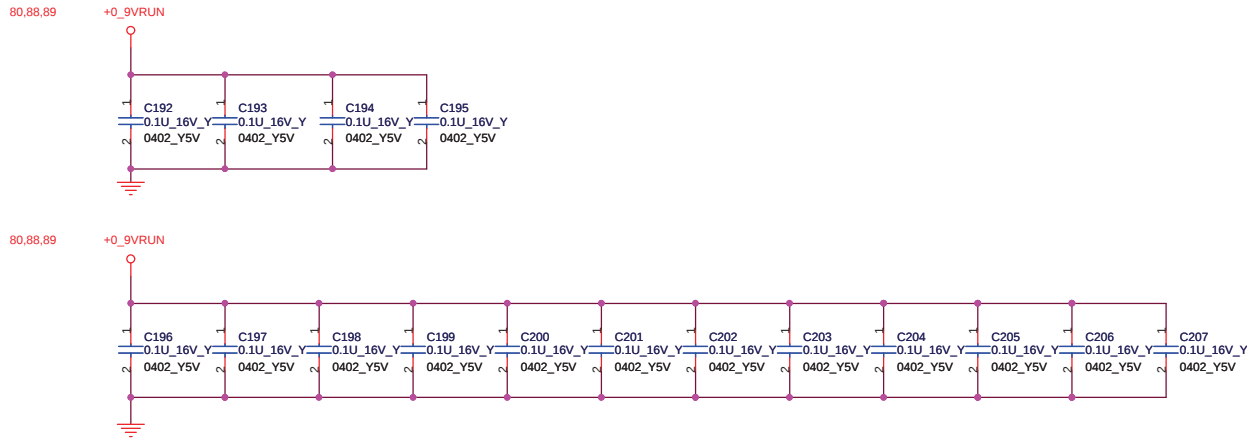
DIMM_1

<http://laptop-motherboard-schematic.blogspot.com/>

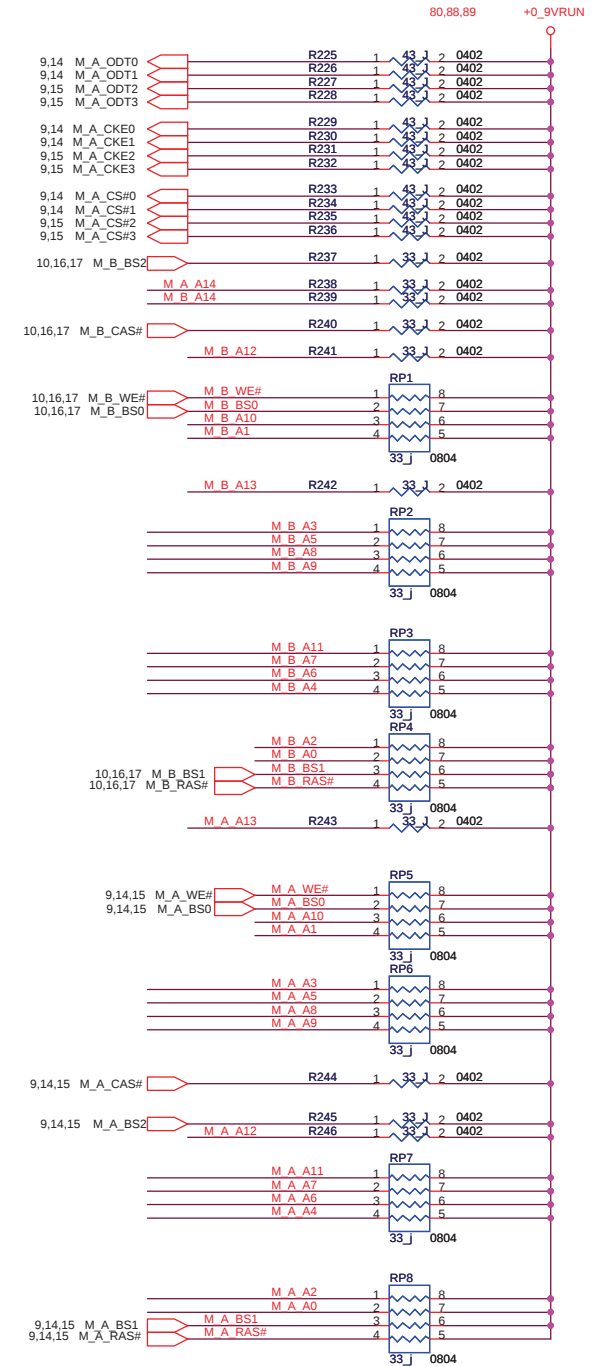
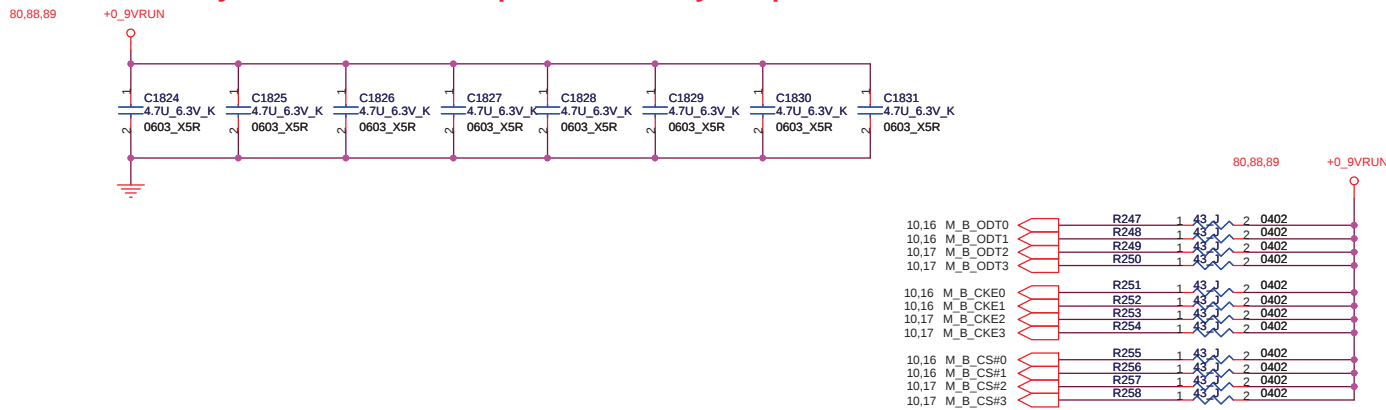
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
File: DDRII(CHB DIMM1) 4/4		
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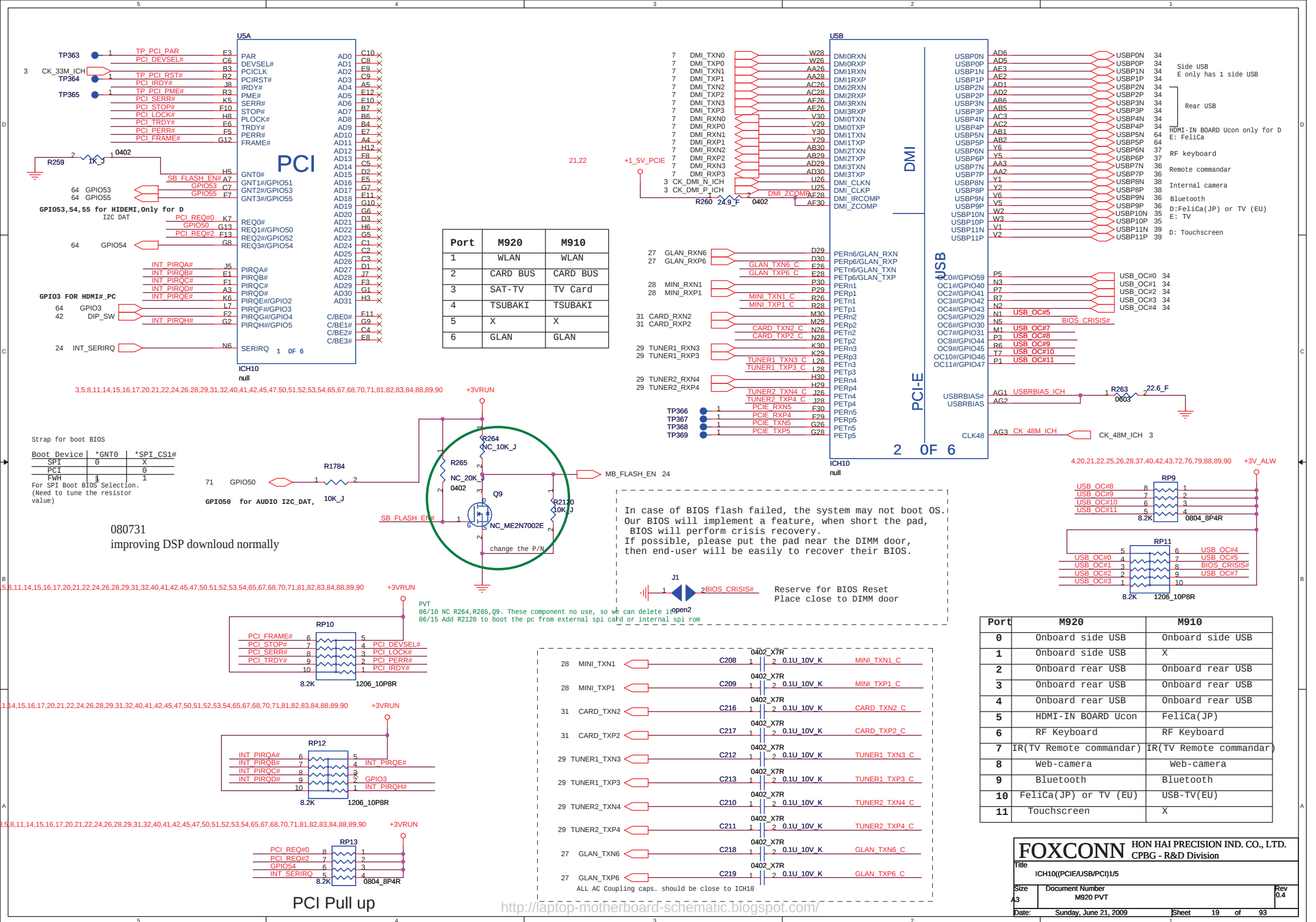


Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



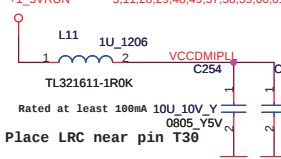
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



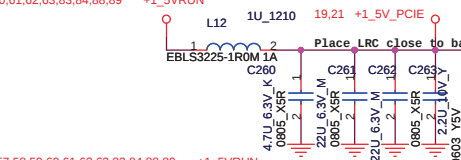


HDA Decoupling caps

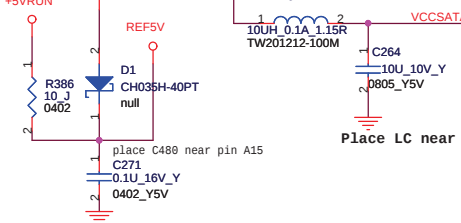
VCCDMIPLL LRC Filter



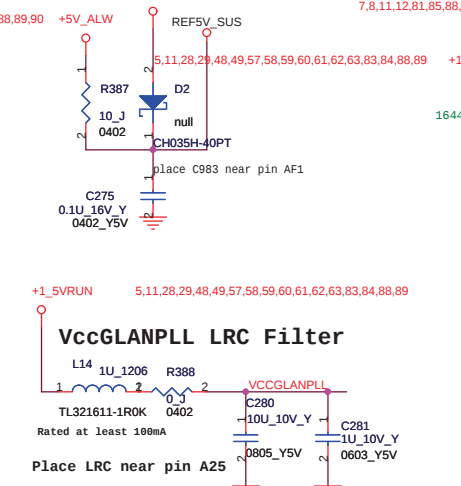
PCI-E (VCC1_5_B) Filter



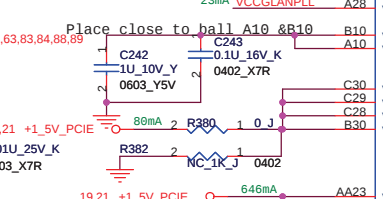
VccSATAPLL LC Filter



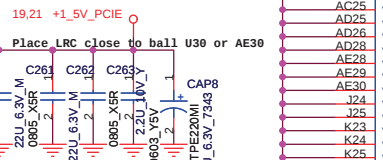
VccGLANPLL LRC Filter



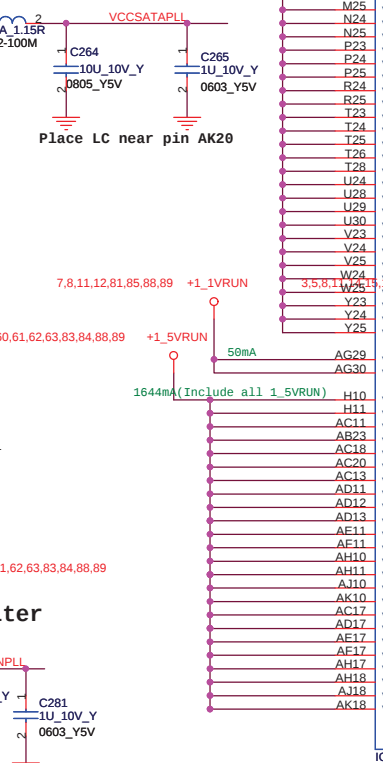
PCI-E (VCC1_5_B) Filter



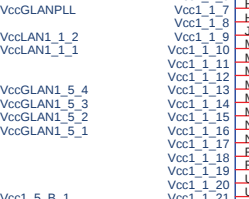
VccSATAPLL LC Filter



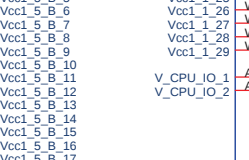
VccGLANPLL LRC Filter



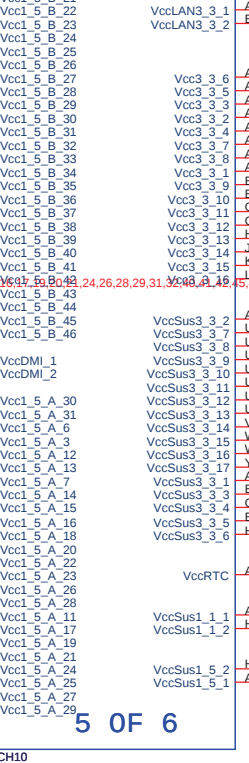
PCI-E (VCC1_5_B) Filter



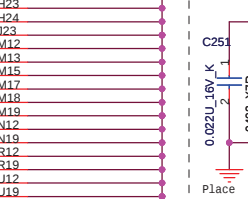
VccSATAPLL LC Filter



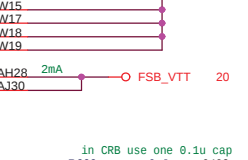
VccGLANPLL LRC Filter



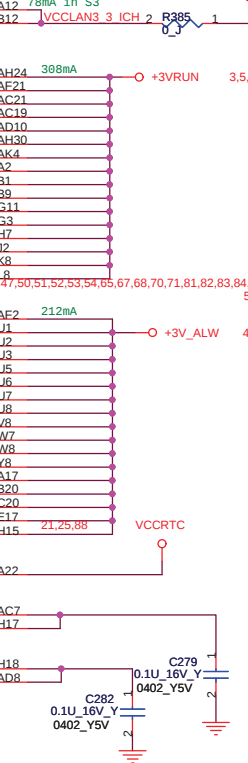
PCI-E (VCC1_5_B) Filter



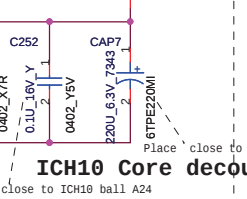
VccSATAPLL LC Filter



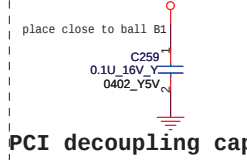
VccGLANPLL LRC Filter



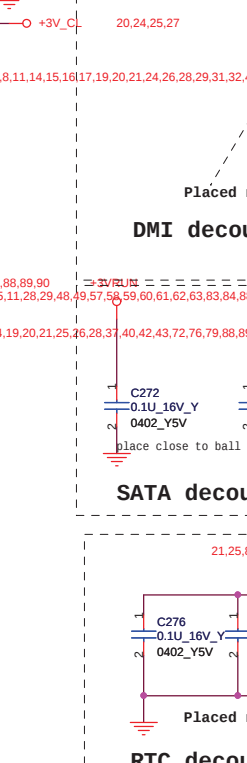
PCI-E (VCC1_5_B) Filter



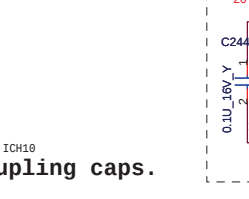
VccSATAPLL LC Filter



VccGLANPLL LRC Filter



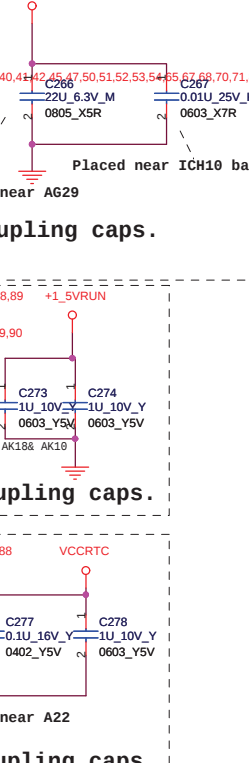
PCI-E (VCC1_5_B) Filter



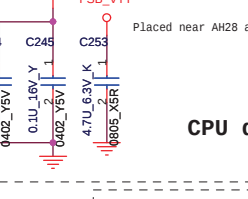
VccSATAPLL LC Filter



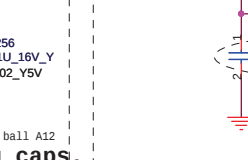
VccGLANPLL LRC Filter



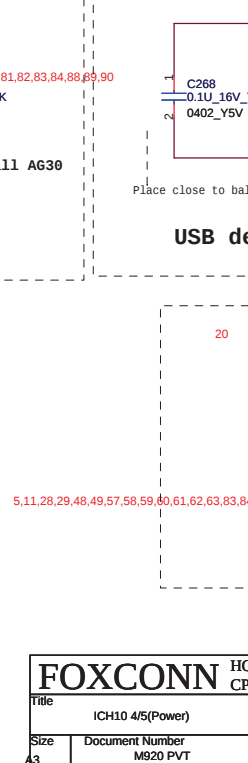
PCI-E (VCC1_5_B) Filter



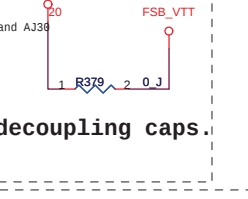
VccSATAPLL LC Filter



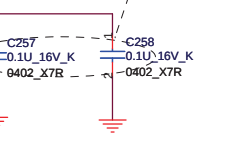
VccGLANPLL LRC Filter



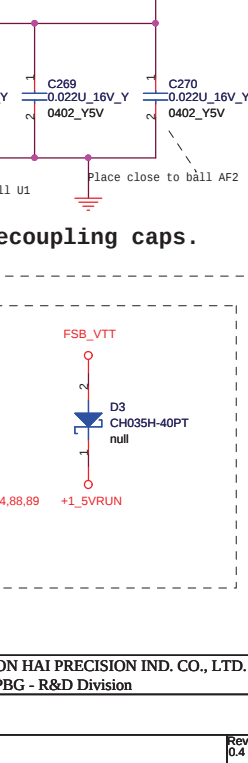
PCI-E (VCC1_5_B) Filter



VccSATAPLL LC Filter



VccGLANPLL LRC Filter



U5F

G30	Vss_104	Vss_105	H13
G29	Vss_103	Vss_106	H19
G25	Vss_102	Vss_107	H2
G16	Vss_101	Vss_108	H22
F9	Vss_100	Vss_109	H25
F6	Vss_99	Vss_110	H26
F28	Vss_98	Vss_111	H28
F26	Vss_97	Vss_112	H9
F21	Vss_96	Vss_113	J29
F12	Vss_95	Vss_114	J30
E30	Vss_94	Vss_115	J6
E29	Vss_93	Vss_116	K26
E22	Vss_92	Vss_117	K28
E2	Vss_91	Vss_118	L2
E18	Vss_90	Vss_119	L23
E15	Vss_89	Vss_120	L29
D28	Vss_88	Vss_121	L30
B8	Vss_87	Vss_122	M14
B5	Vss_86	Vss_123	M16
B28	Vss_85	Vss_124	M26
B25	Vss_83	Vss_125	M28
B22	Vss_82	Vss_126	M6
B2	Vss_81	Vss_127	M8
B19	Vss_80	Vss_128	N13
B17	Vss_79	Vss_129	N14
B14	Vss_78	Vss_130	N15
B11	Vss_77	Vss_131	N16
AK8	Vss_76	Vss_132	N17
AK30	Vss_75	Vss_133	N18
AK29	Vss_74	Vss_134	N23
AK2	Vss_72	Vss_135	N29
AK16	Vss_71	Vss_136	N30
AK14	Vss_70	Vss_137	P12
AK12	Vss_69	Vss_138	P13
AJ8	Vss_68	Vss_139	P14
AJ5	Vss_67	Vss_140	P15
AJ26	Vss_65	Vss_141	P16
AJ23	Vss_64	Vss_142	P17
AJ20	Vss_63	Vss_143	P18
AJ16	Vss_62	Vss_144	P19
AJ14	Vss_61	Vss_145	P2
AJ12	Vss_60	Vss_146	P26
AH8	Vss_59	Vss_147	P28
AH6	Vss_58	Vss_148	P6
AH20	Vss_56	Vss_149	R13
AH2	Vss_55	Vss_150	R14
AH19	Vss_54	Vss_151	R15
AH15	Vss_53	Vss_152	R16
AH13	Vss_52	Vss_153	R17
AG28	Vss_51	Vss_154	R18
AF9	Vss_50	Vss_155	R23
AF7	Vss_49	Vss_156	R29
AF29	Vss_47	Vss_157	R30
AF25	Vss_46	Vss_158	R8
AF23	Vss_45	Vss_159	T12
AF20	Vss_44	Vss_160	T13
AF15	Vss_43	Vss_161	T14
AF13	Vss_42	Vss_162	T15
AE9	Vss_41	Vss_163	T16
AE8	Vss_40	Vss_164	T17
AE6	Vss_39	Vss_165	T18
AE5	Vss_38	Vss_166	T19
AE25	Vss_37	Vss_167	T2
AE19	Vss_36	Vss_168	T29
AE18	Vss_35	Vss_169	T5
AE16	Vss_34	Vss_170	U13
AE15	Vss_33	Vss_171	U14
AE14	Vss_32	Vss_172	U15
AE13	Vss_31	Vss_173	U16
AE12	Vss_30	Vss_174	U17
AE10	Vss_29	Vss_175	U18
AE1	Vss_28	Vss_176	U23
AD9	Vss_27	Vss_177	V13
AD7	Vss_26	Vss_178	V14
AD3	Vss_25	Vss_179	V15
AD22	Vss_24	Vss_180	V16
AD19	Vss_23	Vss_181	V17
AD18	Vss_22	Vss_182	V18
AD16	Vss_21	Vss_183	V26
AD15	Vss_20	Vss_184	V28
AD14	Vss_19	Vss_185	V3
AC8	Vss_18	Vss_186	V7
AC6	Vss_17	Vss_187	W1
AC5	Vss_16	Vss_188	W14
AC30	Vss_15	Vss_189	W16
AC29	Vss_14	Vss_190	W23
AC24	Vss_13	Vss_191	W29
AC12	Vss_12	Vss_192	W30
AC1	Vss_11	Vss_193	W5
AB3	Vss_10	Vss_194	W6
AB28	Vss_9	Vss_195	Y26
AB26	Vss_8	Vss_196	Y28
AA6	Vss_7	Vss_197	Y3
AA5	Vss_6	Vss_198	Y7
AK27	Vss_73	Vss_5	AA30
AH29	Vss_57	Vss_4	AA29
AJ4	Vss_66	Vss_3	AA1
AE3	Vss_48	Vss_2	A30
B27	Vss_84	Vss_1	A1

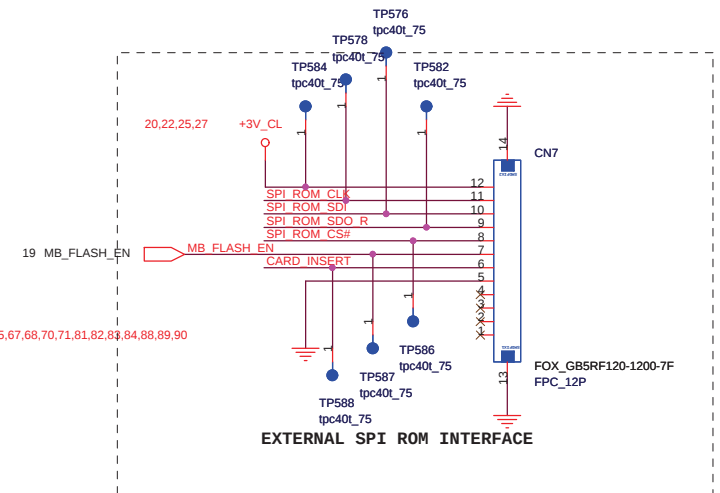
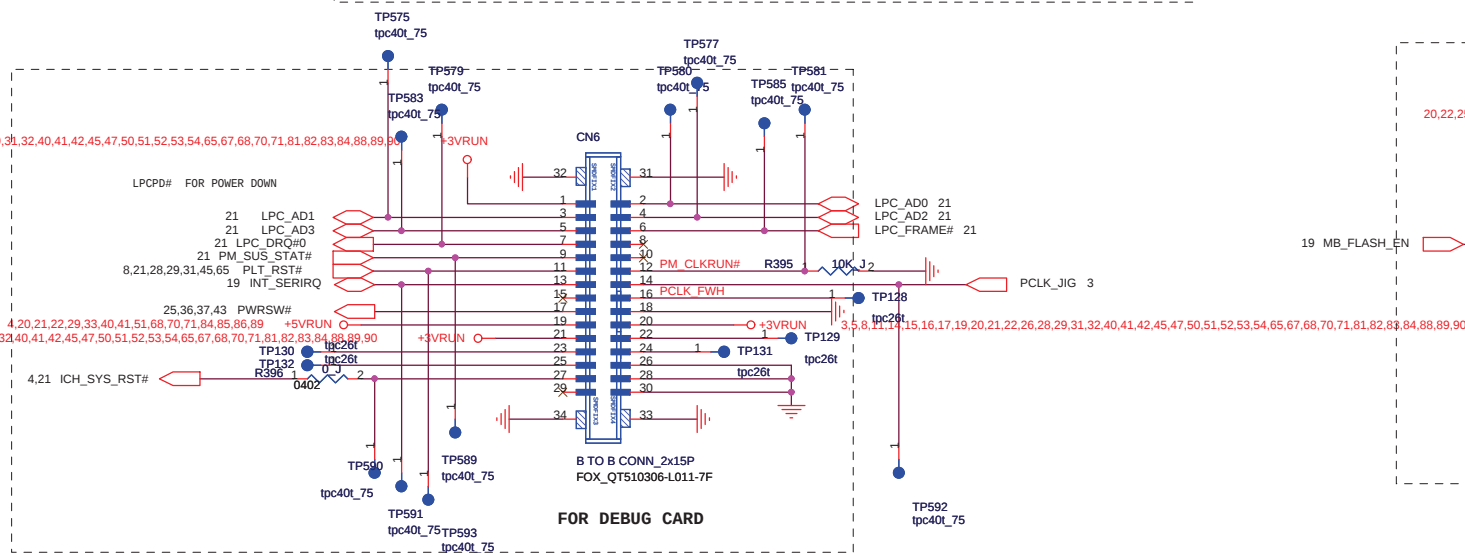
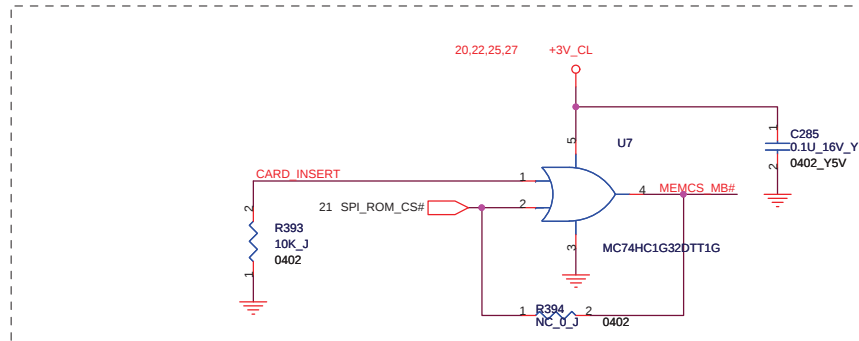
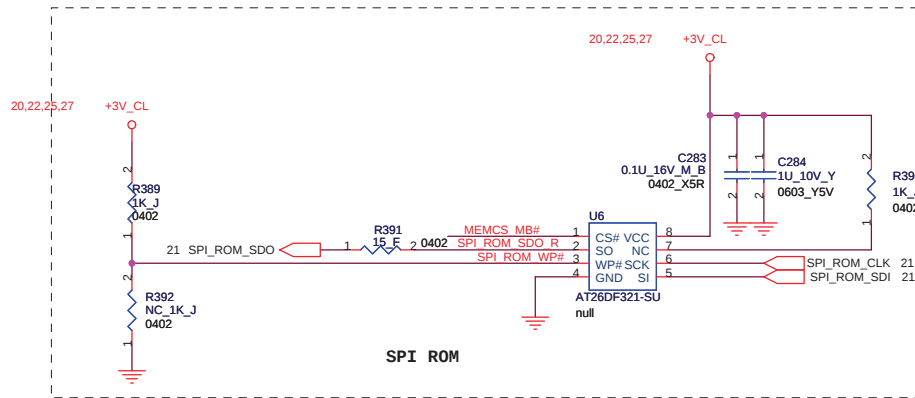
6 OF 6

ICH10

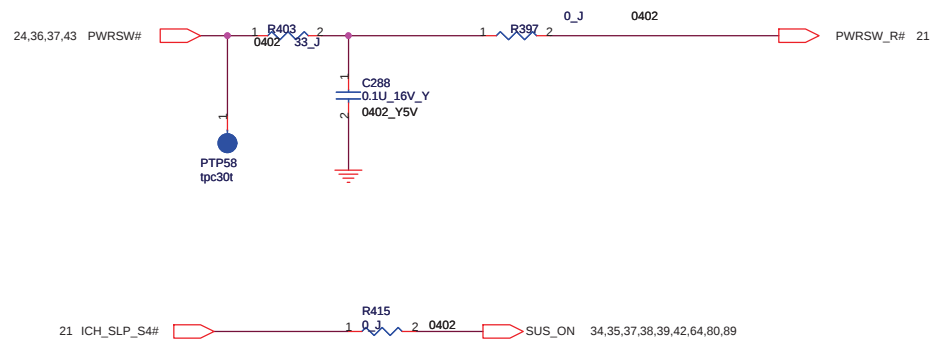
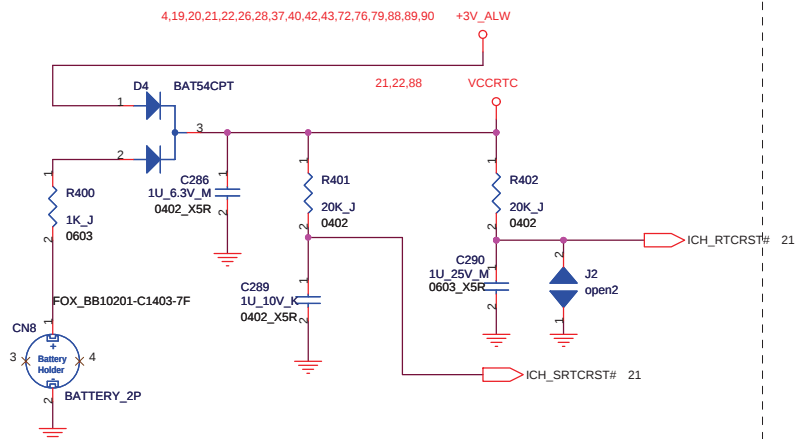
null

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Delay time from VCCRTC high to RTCRST# inactive 18~25mS

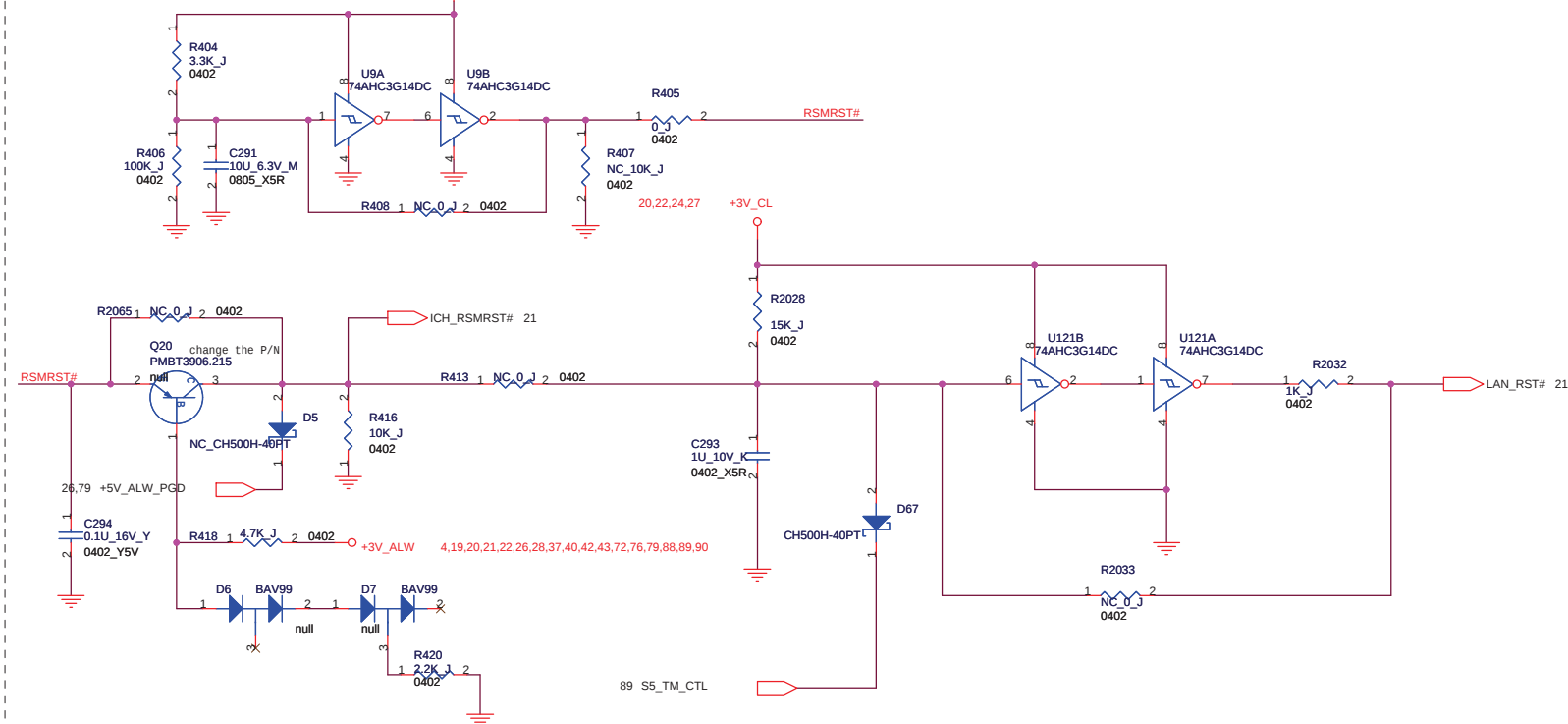


Delay time from +3v_alw high to RSMRST# inactive

Minimum 10 mS DELAY ---26mS

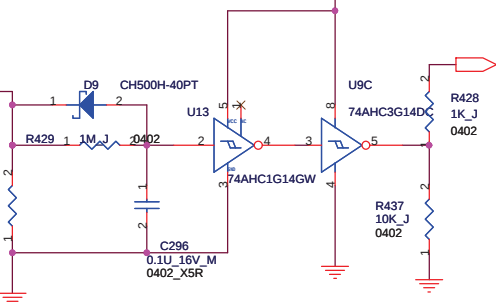
4,19,20,21,22,26,28,37,40,42,43,72,76,79,88,89,90 +3V_ALW

0189 change R484 from 3.24K_F to 3.3K_J for MOR suggestion



ICH_SLP_S3# inactive to RUN_ON active(3/5VRUN) delay
Minimum 20mS -- 80mS

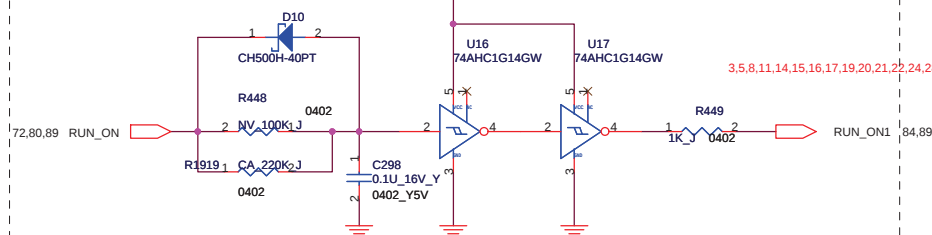
4,19,20,21,22,25,28,37,40,42,43,72,76,79,88,89,90 +3V_ALW



NV_VDD POWER LOGIC

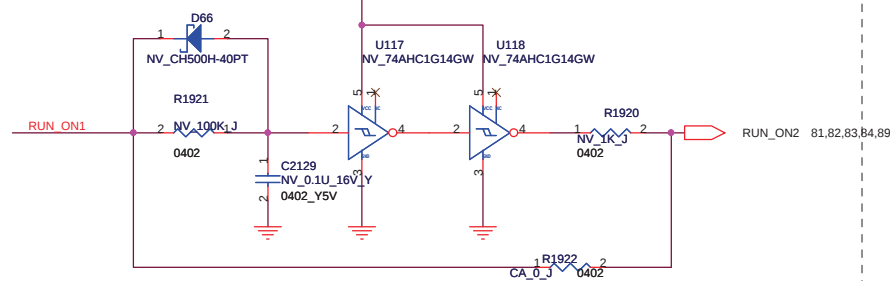
Minimum 5mS DELAY -- 10mS

4,19,20,21,22,25,28,37,40,42,43,72,76,79,88,89,90 +3V_ALW



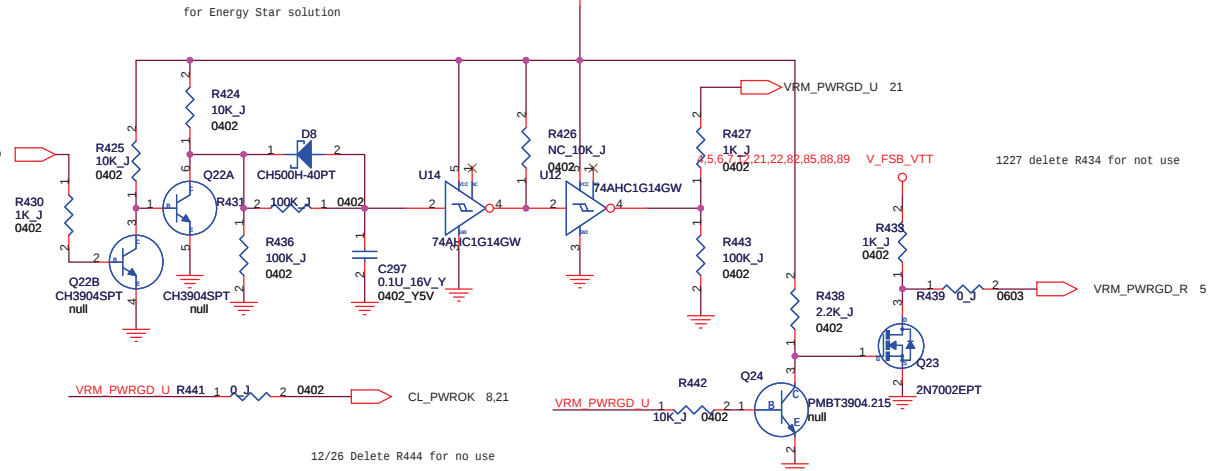
+1_5VRUN/+1_1VRUN/V_FSB_VTT/PEX_VDD
Minimum 5mS DELAY -- 10mS

4,19,20,21,22,25,28,37,40,42,43,72,76,79,88,89,90 +3V_ALW



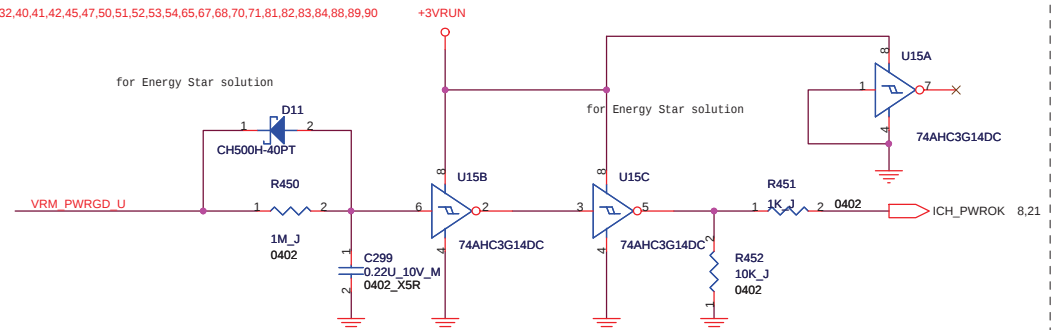
VRM_PWRGD Delay time and level shift

3,5,8,11,14,15,16,17,19,20,21,22,24,28,29,31,32,40,41,42,45,47,50,51,52,53,54,65,67,68,70,71,81,82,83,84,88,89,90



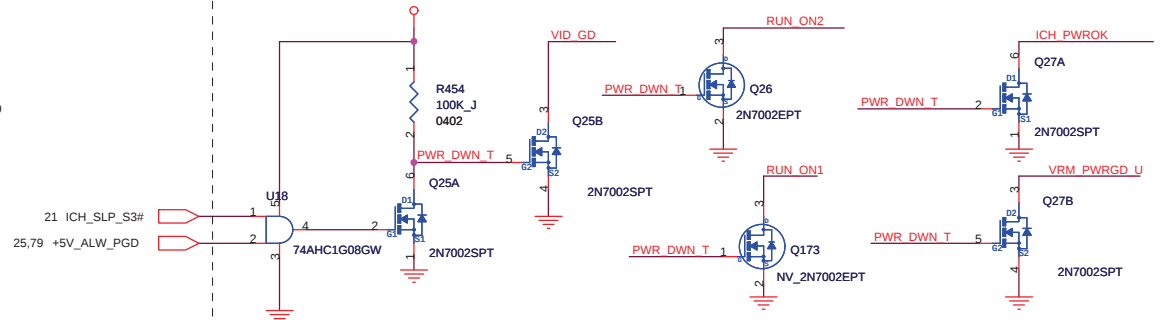
ICH_VRM_PWRGD DELAY 99ms to ICH_PWROK Minimum 99mS DELAY

3,5,8,11,14,15,16,17,19,20,21,22,24,28,29,31,32,40,41,42,45,47,50,51,52,53,54,65,67,68,70,71,81,82,83,84,88,89,90



POWER DOWN TIMING

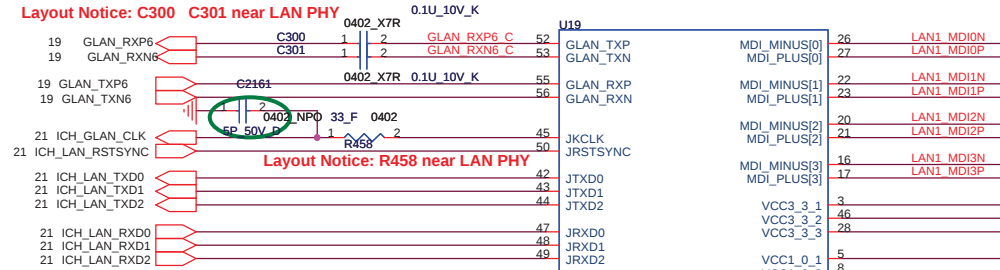
4,19,20,21,22,25,28,37,40,42,43,72,76,79,88,89,90 +3V_ALW



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In 1000 Mb/s mode, JKCLK frequency is 62.5 MHz.
In 100 Mb/s mode, JKCLK frequency is 50 MHz.
In 10 Mb/s mode, JKCLK frequency is 5 MHz.
In power down mode, JKCLK frequency is 0 MHz.

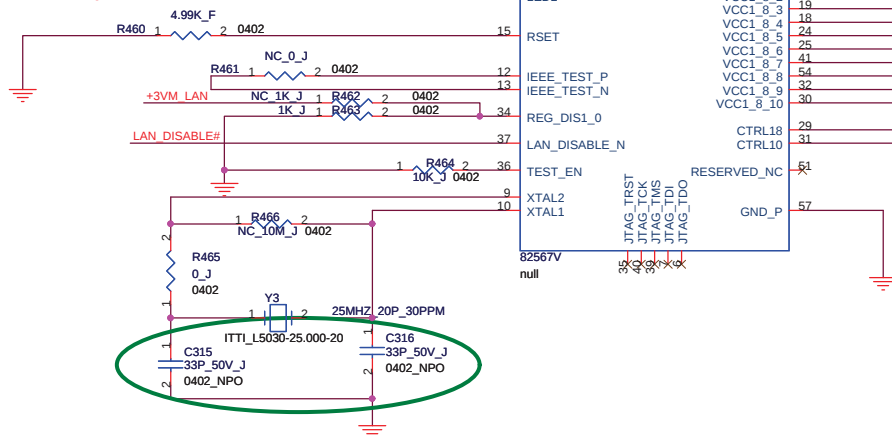
Layout Notice: C300 C301 near LAN PHY



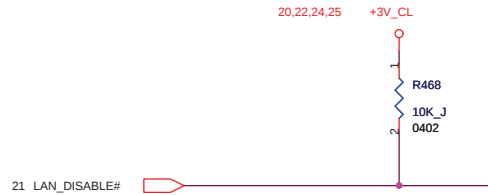
Layout Notice: R458 near LAN PHY

06/15 PVT Change C2161 From 1C-2B20104-K000 1C-2N20050-D000 for EMI Request

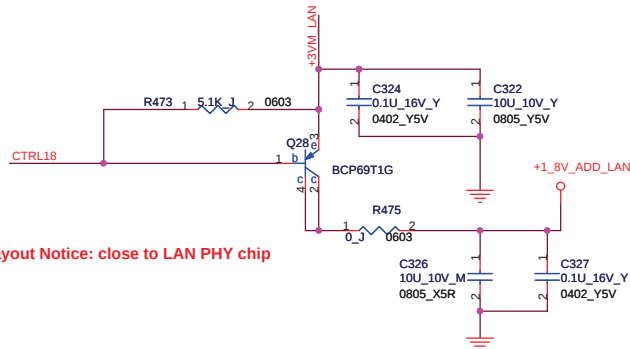
Layout Notice: R460 near LAN PHY



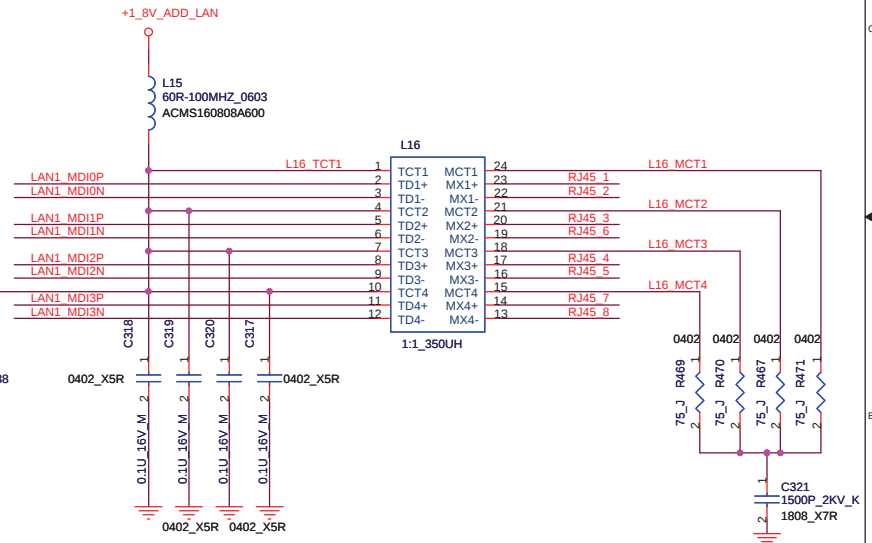
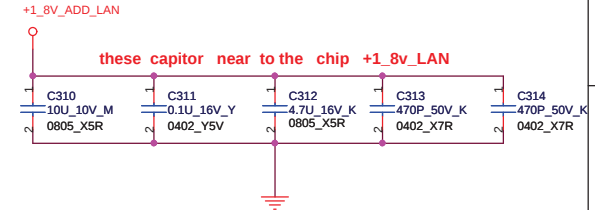
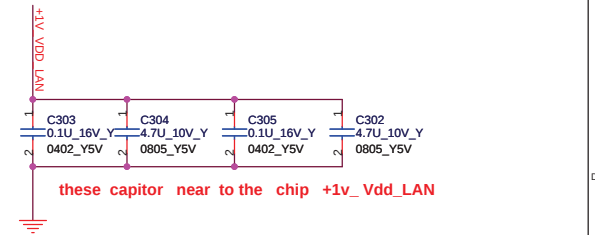
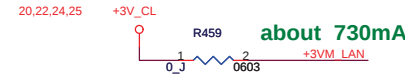
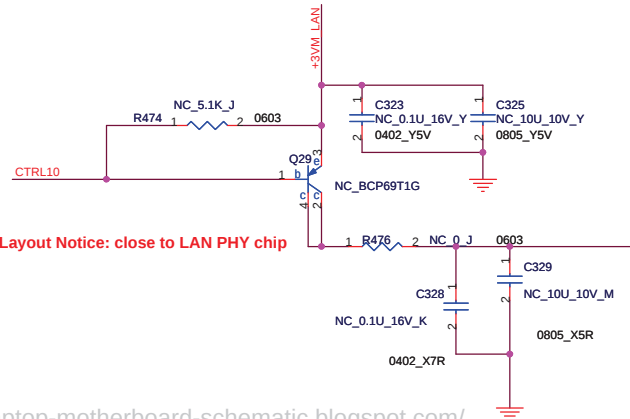
0619 Change C315 and C316 from 1C-2N20150-J000 to 1C-2N20330-J000 for crystal test result



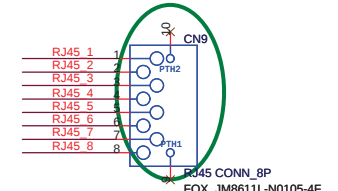
Layout Notice: close to LAN PHY chip



Layout Notice: close to LAN PHY chip

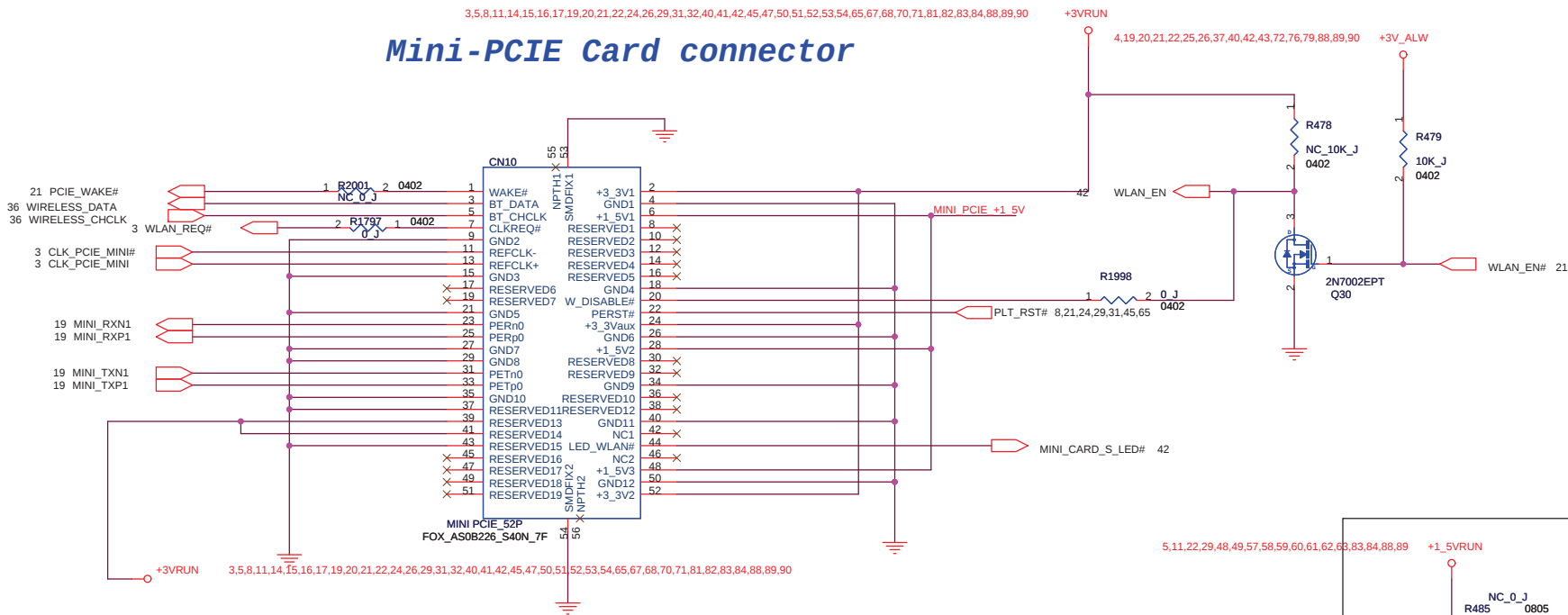


PVT 0610 Change CN9 from 2N-000800F-FKN0 to 2N-0008001-FKN0 for packaging changed



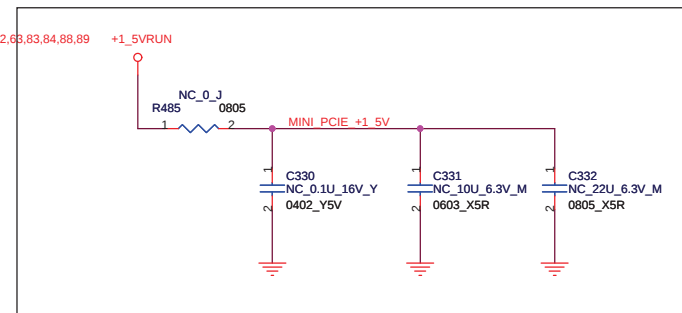
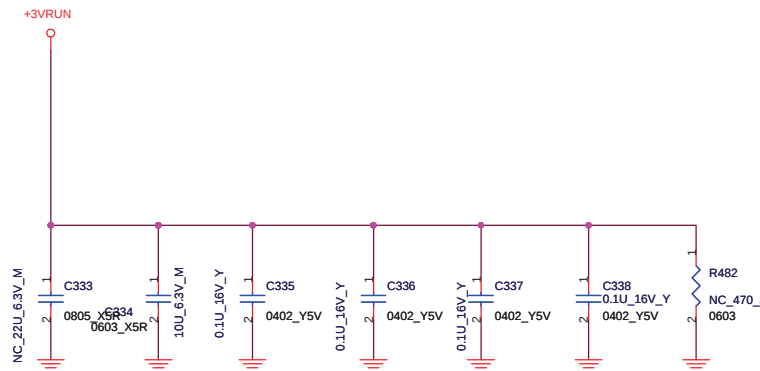
FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
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Size	Document Number	Rev	
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Mini-PCIE Card connector

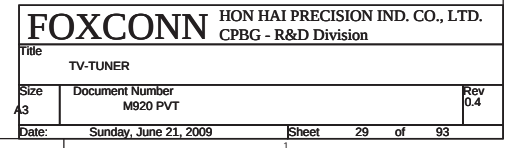


PCIE 3.3V spec.(Normal 750mA)(MAX 1100mA)

3,5,8,11,14,15,16,17,19,20,21,22,24,26,29,31,32,40,41,42,45,47,50,51,52,53,54,65,67,68,70,71,81,82,83,84,88,89,90



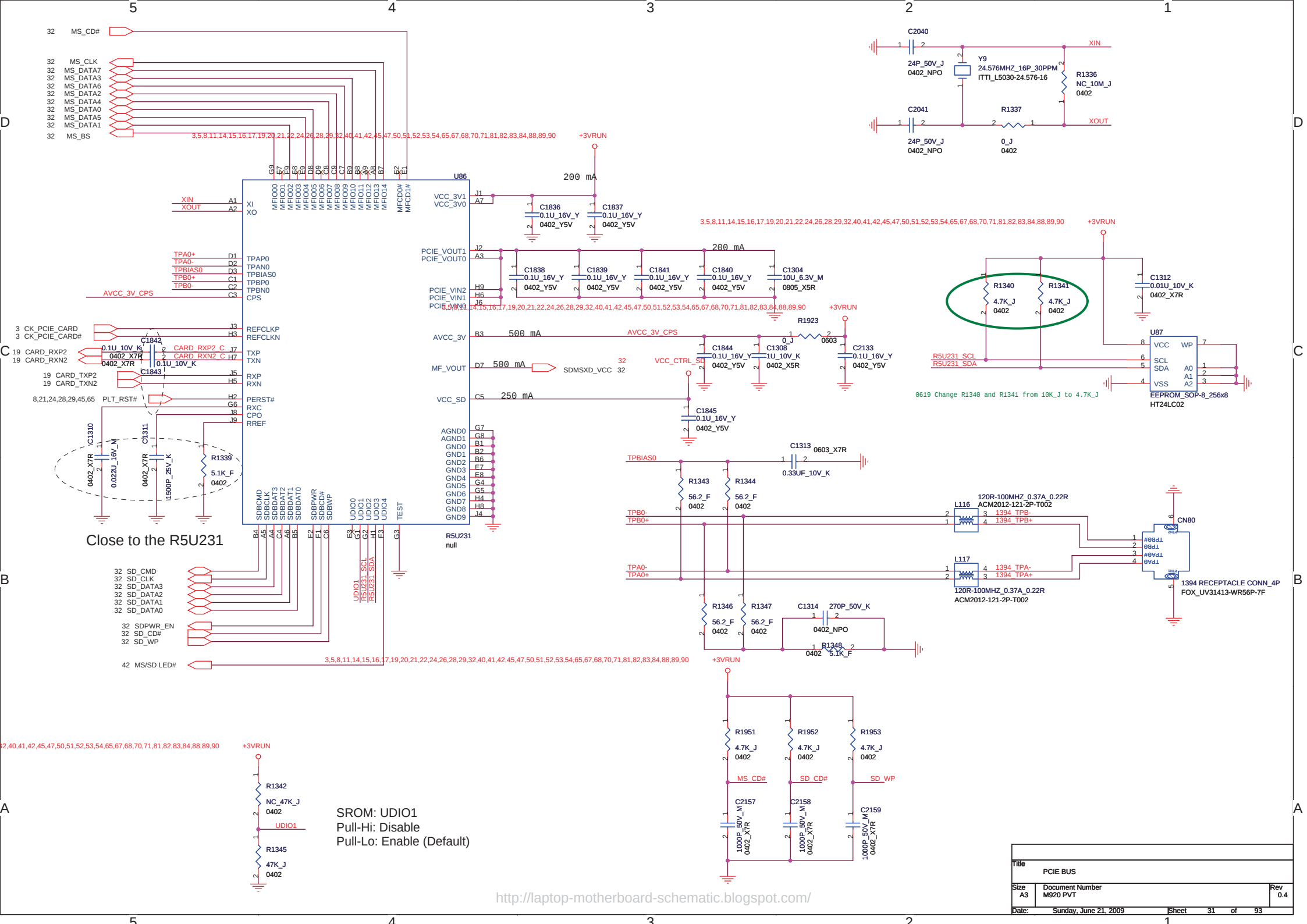
24,26,28,31,32,40,41,42,45,47,50,51,52,53,54,65,67,68,70,71,81,82,83,84,88,89,90 +3VRUN 2500mA

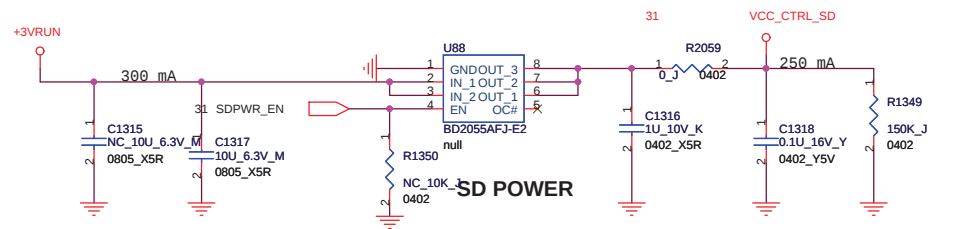


Blank

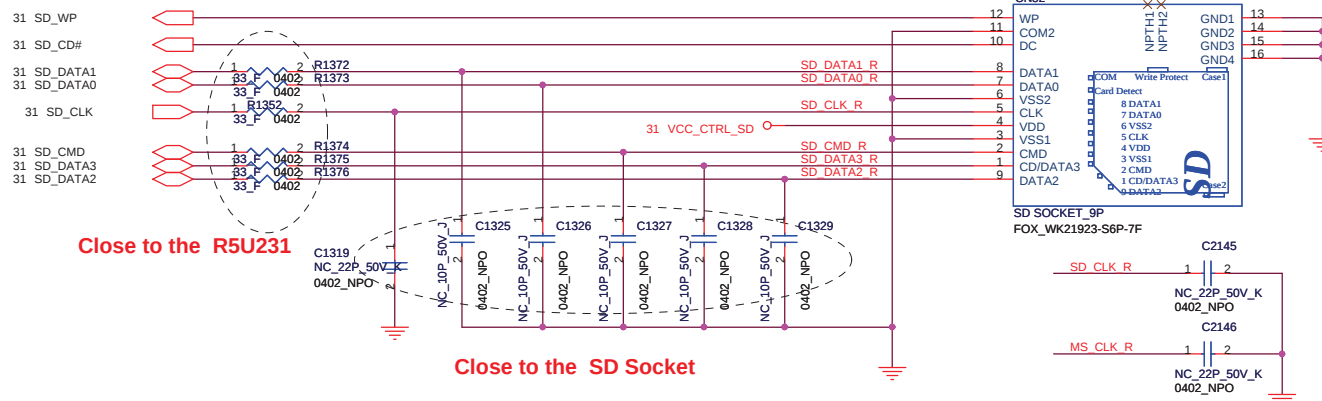
DVT
04/14 Delete all AV_IN function for MOR request
(Delete CN14, C368, C2131, C2132, C2138, C2839, TP486, TP485, TP484, TP487, TP489, TP491, TP487, TP490 and TP488)

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Title			
AV/IR DB CONN			
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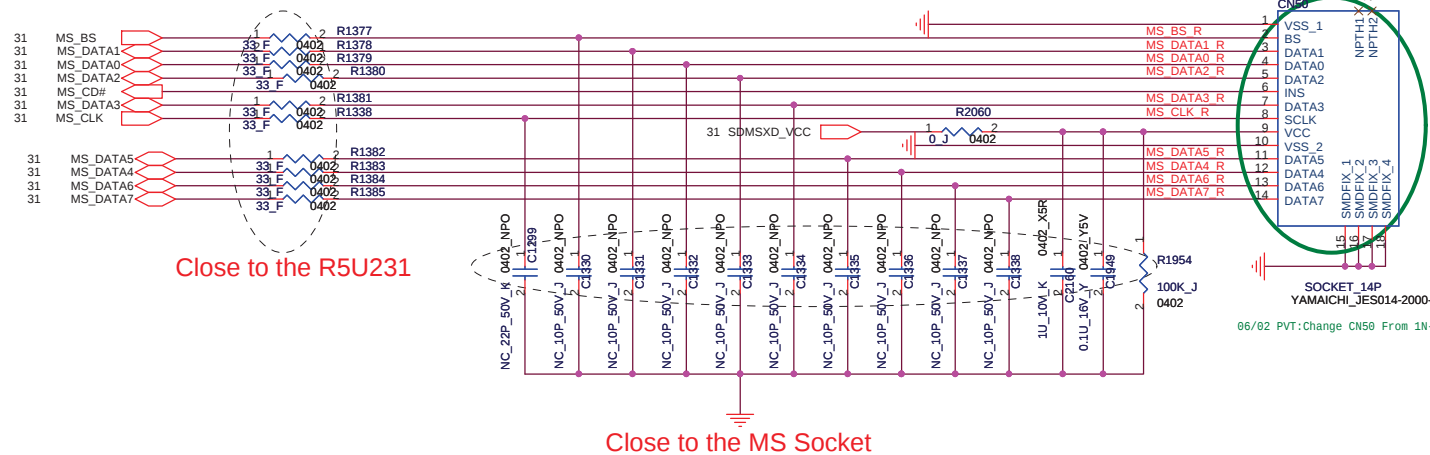




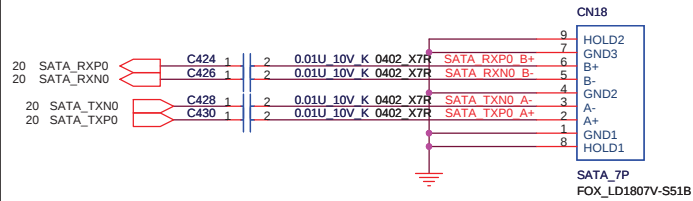
SD CONN.



MS PRO-HG DUO/MS DUO CONN.

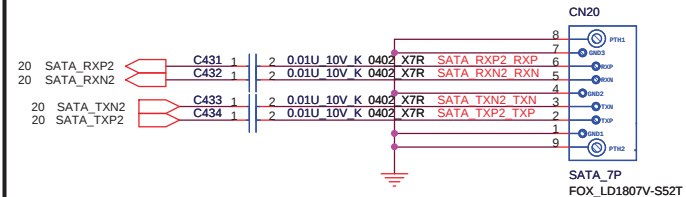


SATA HDD



PLACE SHESE CAPS CLOSE TO CN18

SATA ODD

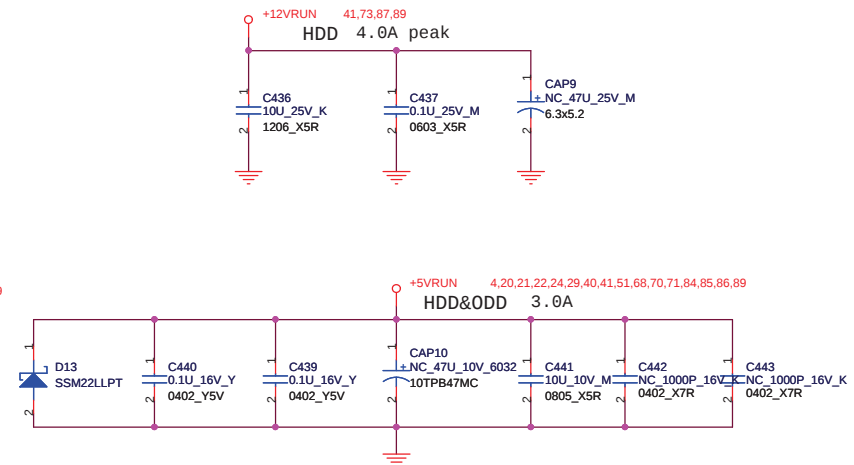
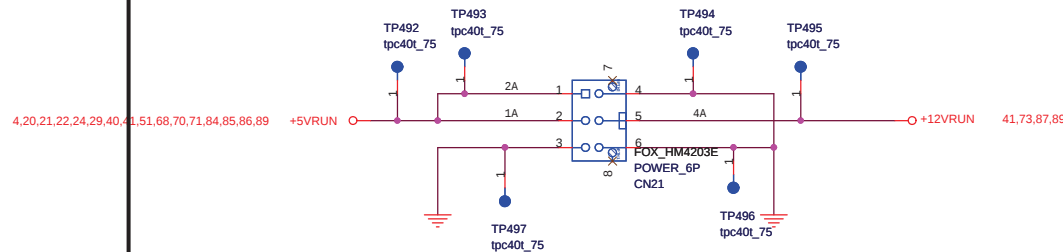


PLACE SHESE CAPS CLOSE TO CN20

HDD&ODD POWER

5V: 3A (HDD 0.8A+ODD 2A)

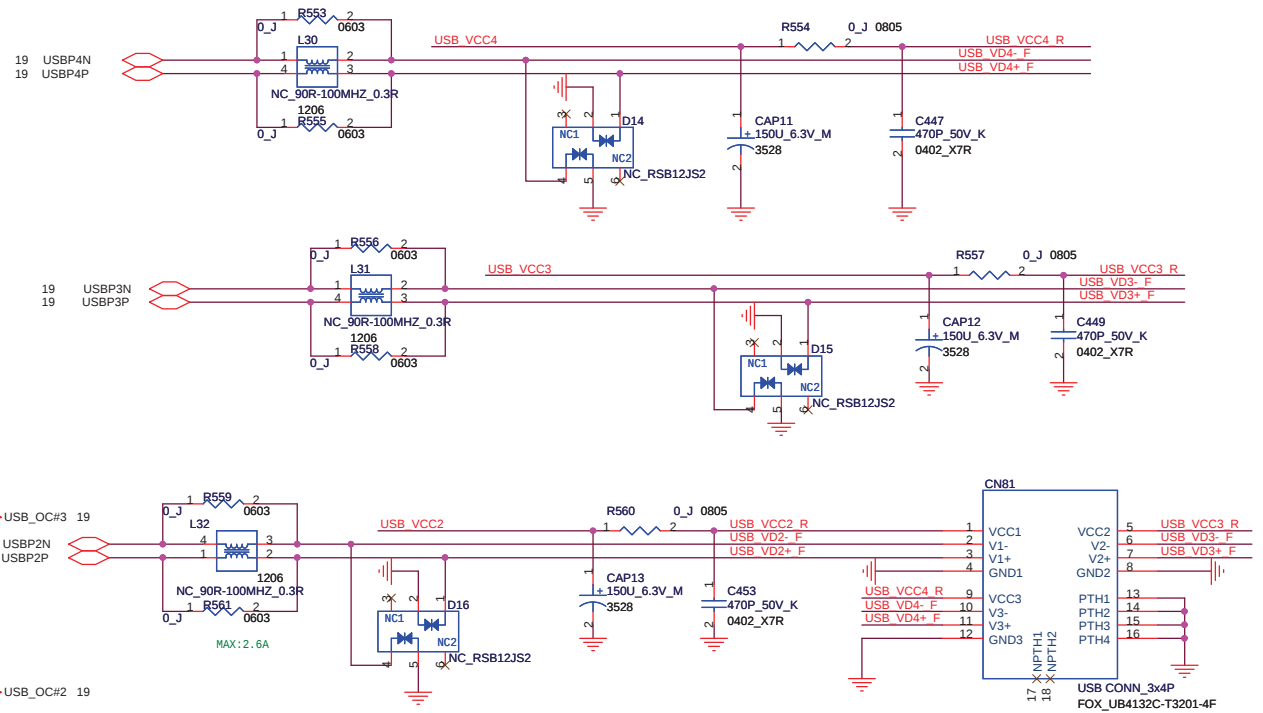
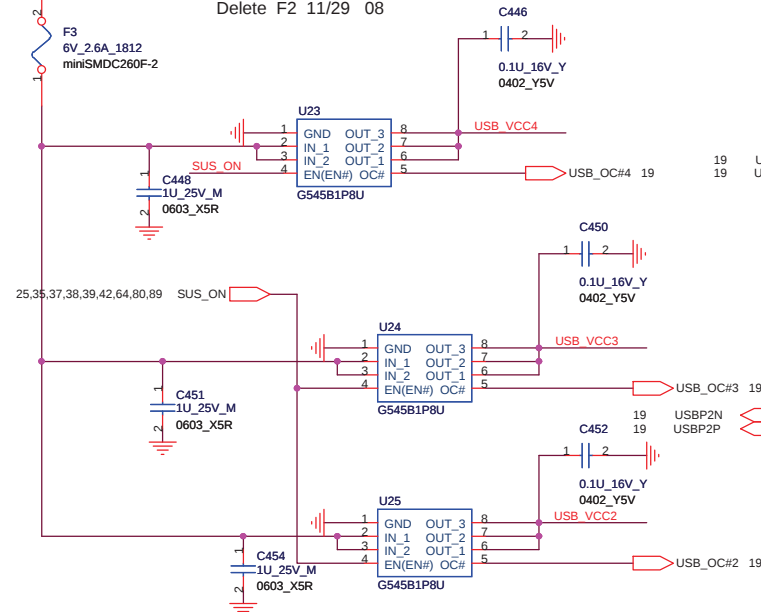
12V: 4A peak, 4 seconds(HDD 4A)



22,36,42,64,66,79,88,89,90 +5V_ALW

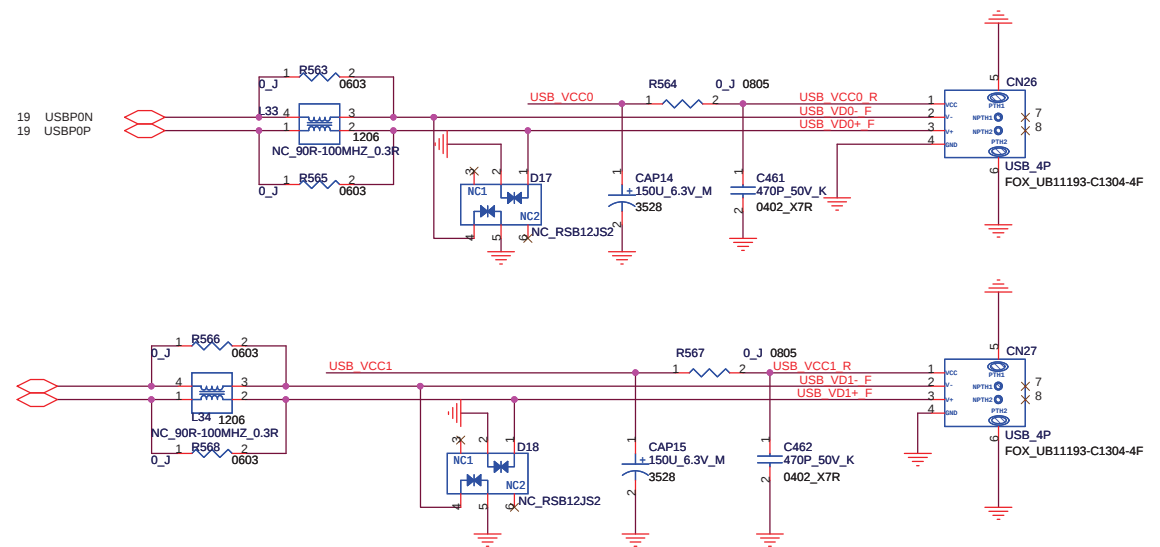
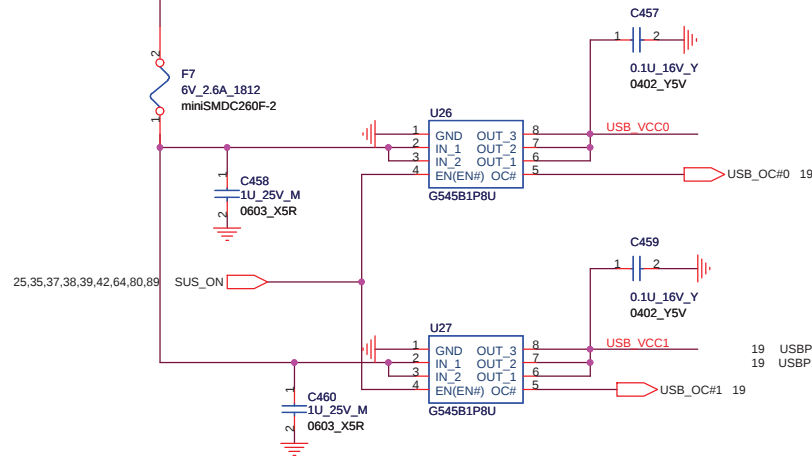
rear USB

Delete F2 11/29 08



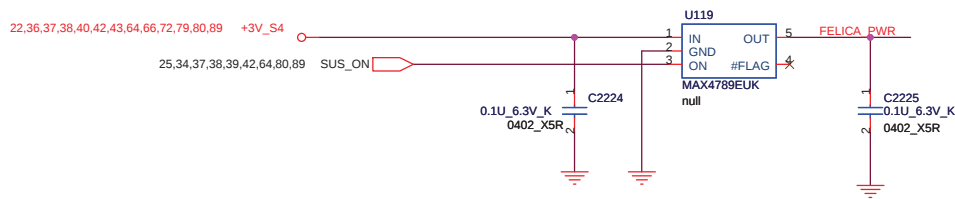
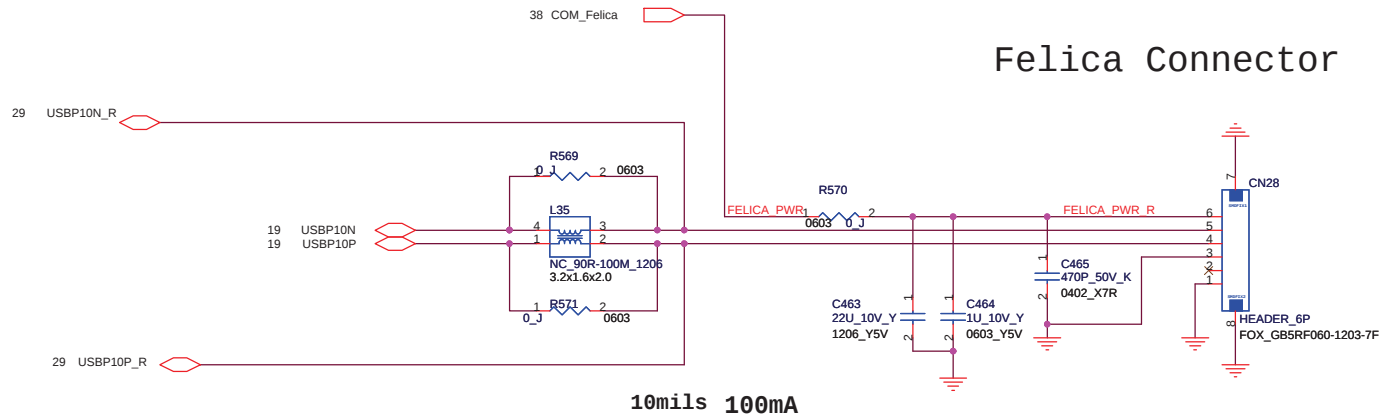
22,36,42,64,66,79,88,89,90 +5V_ALW

SIDE USB

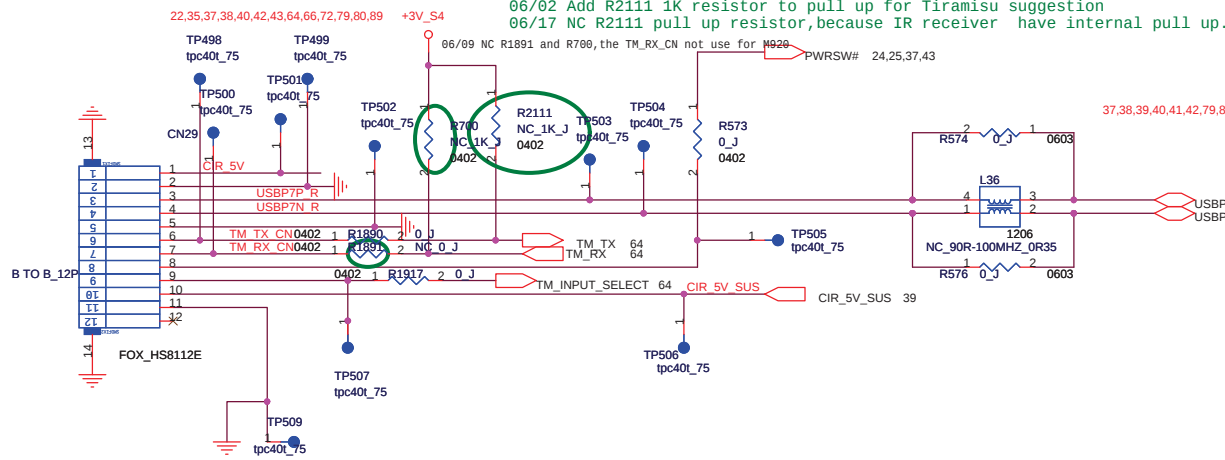


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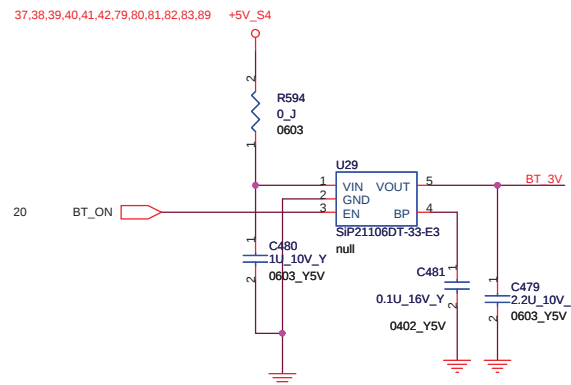
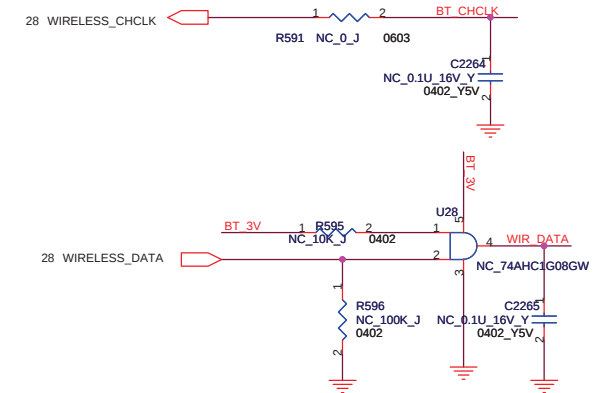
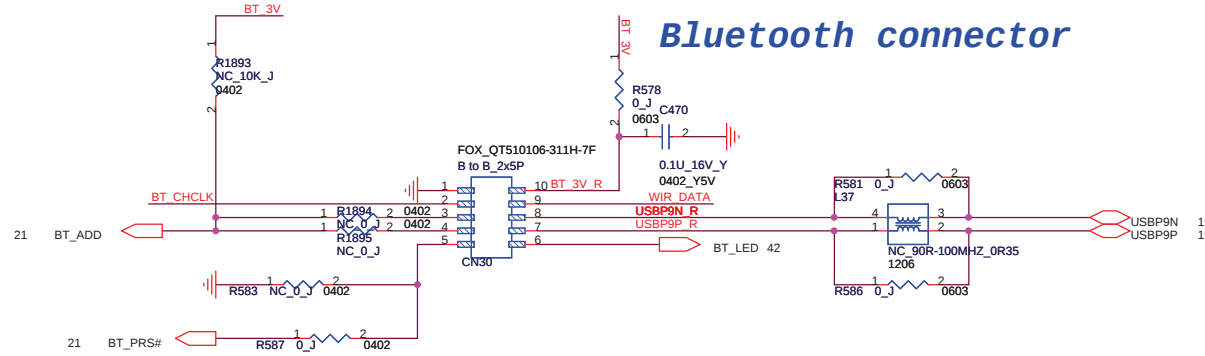
File	USB PORT		
Size	Document Number		
A3	M920 PVT		
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Rev	0.4		



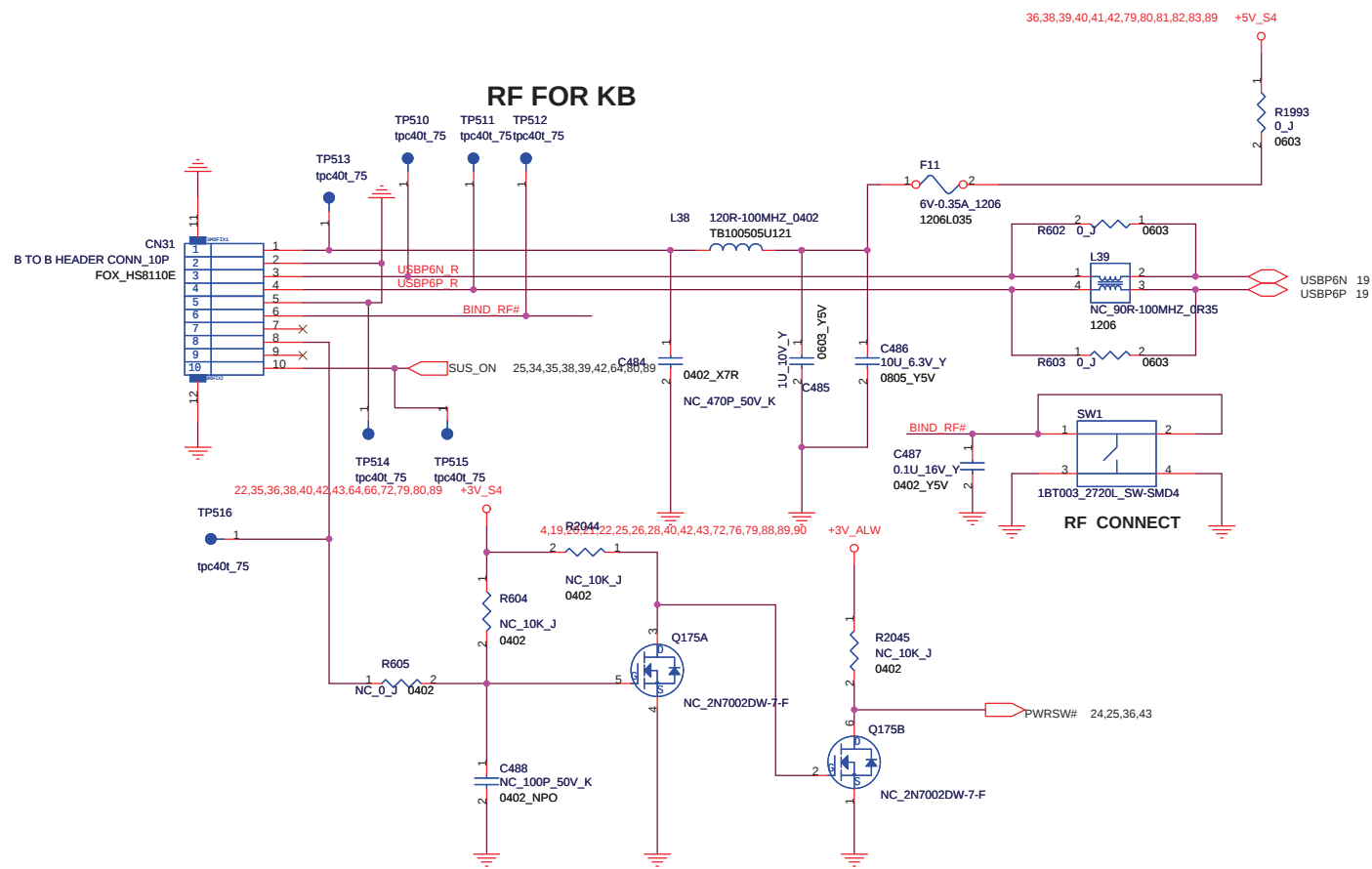
FOR TV Remote commandar

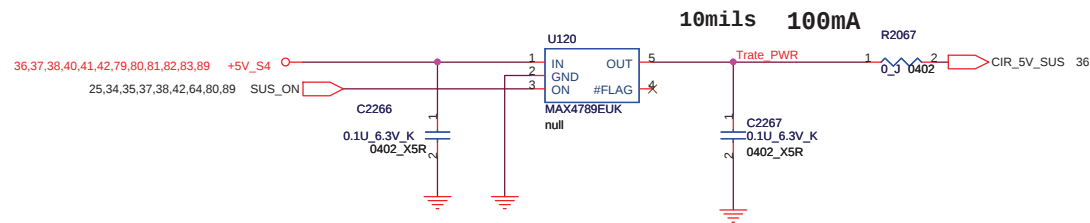
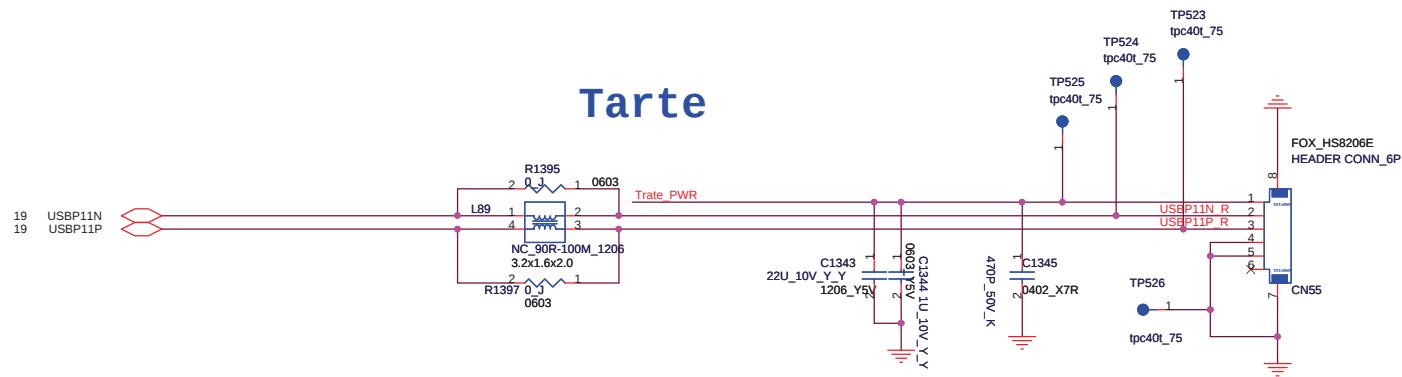


Bluetooth connector



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Title CIR&BT			
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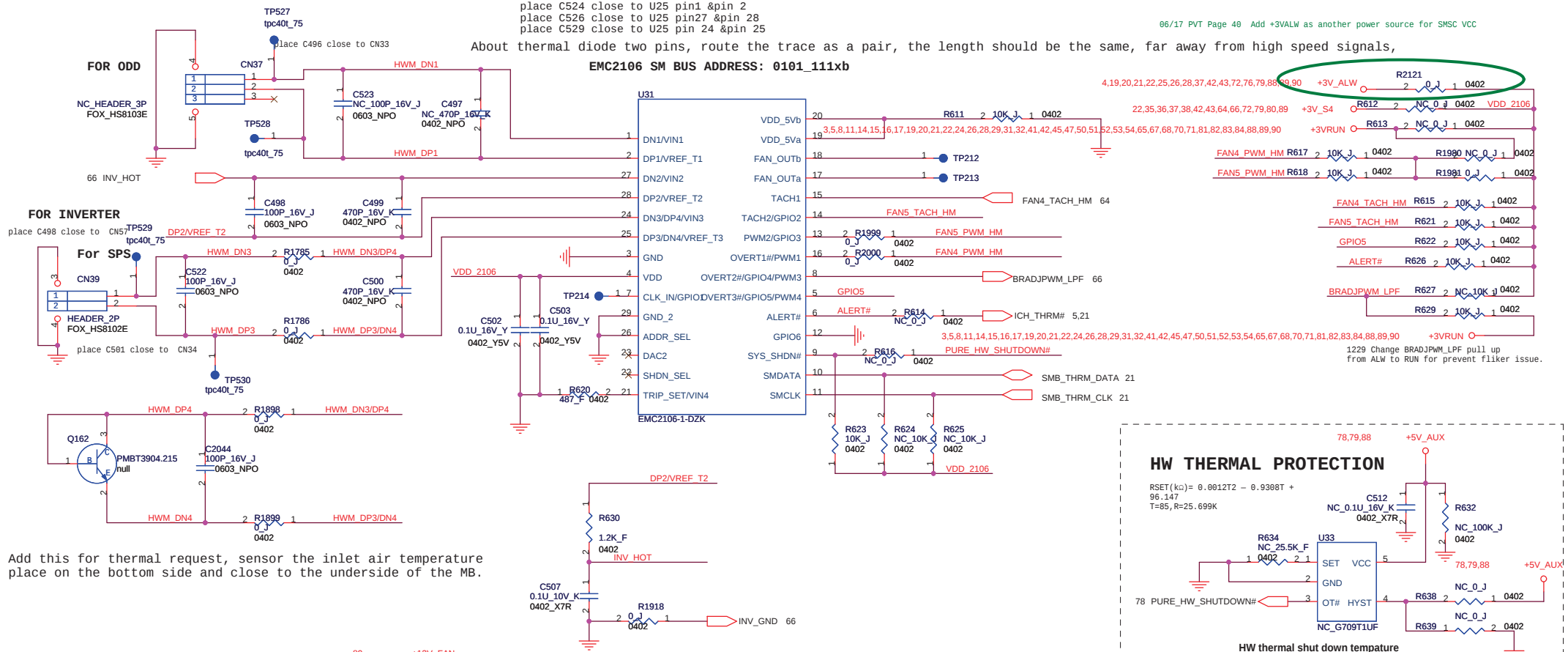




place C524 close to U25 pin1 & pin 2
place C526 close to U25 pin27 & pin 28
place C529 close to U25 pin 24 & pin 25

About thermal diode two pins, route the trace as a pair, the length should be the same, far away from high speed signals,

EMC2106 SM BUS ADDRESS: 0101_111xb

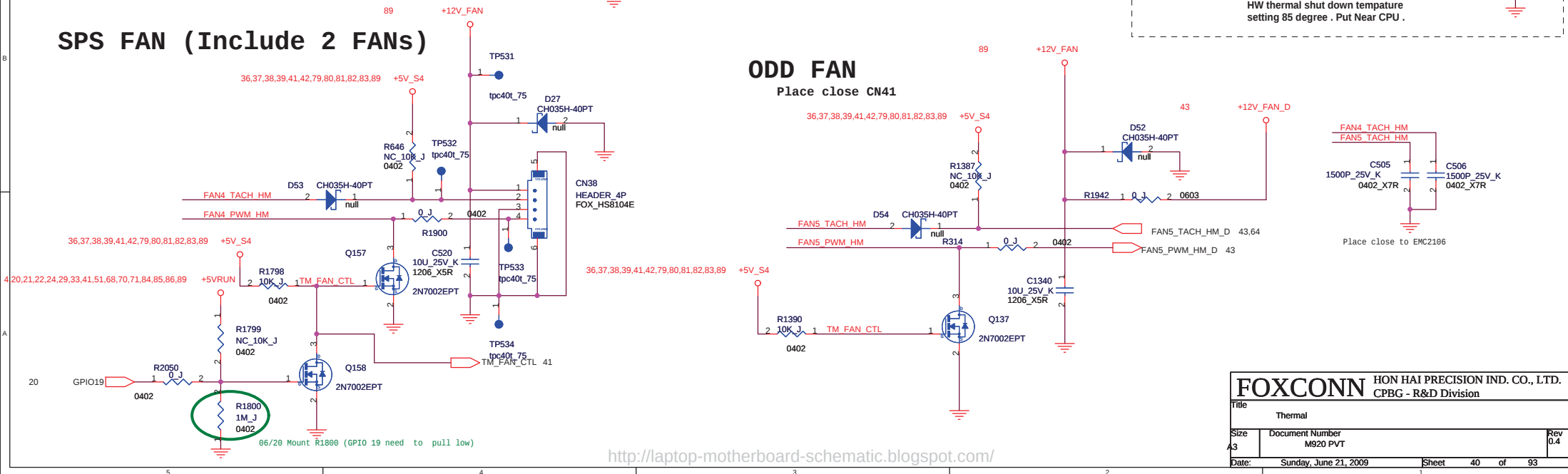


Add this for thermal request, sensor the inlet air temperature place on the bottom side and close to the underside of the MB.

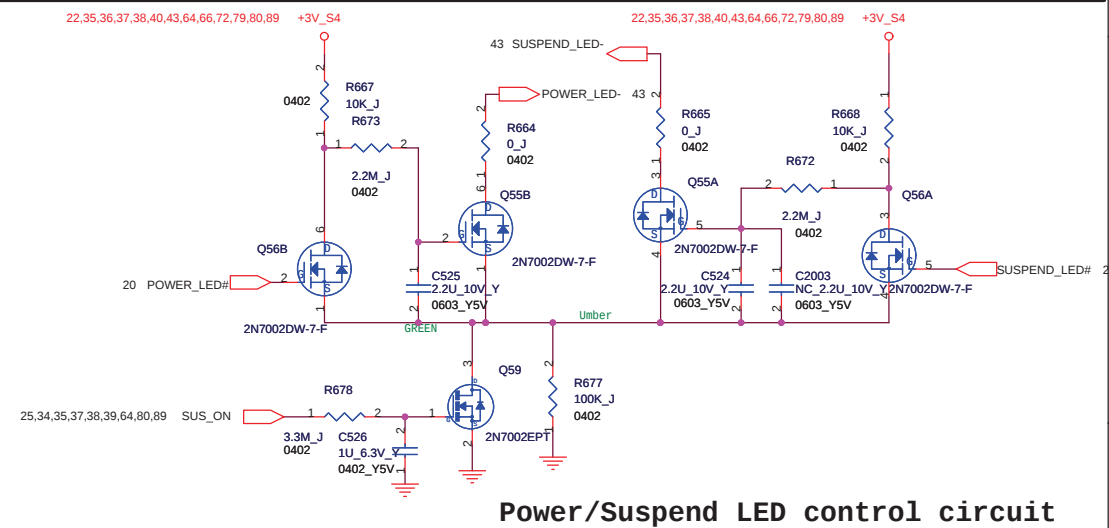
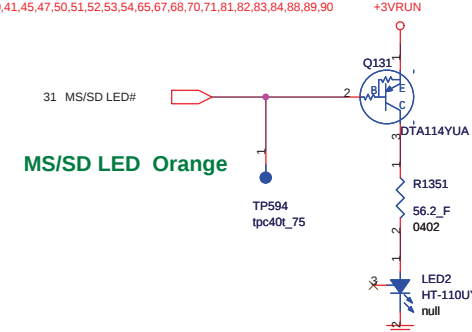
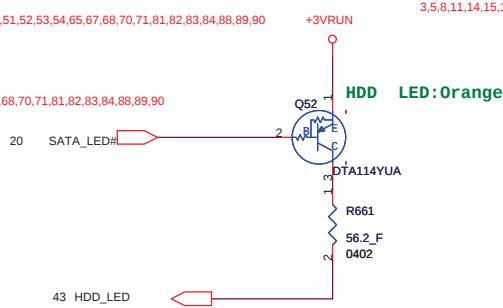
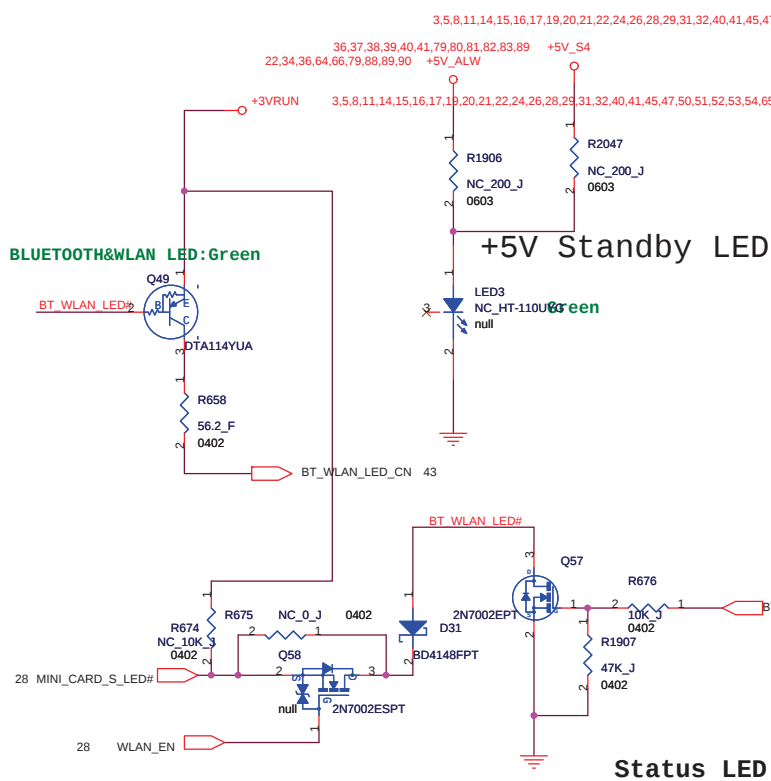
SPS FAN (Include 2 FANS)

ODD FAN

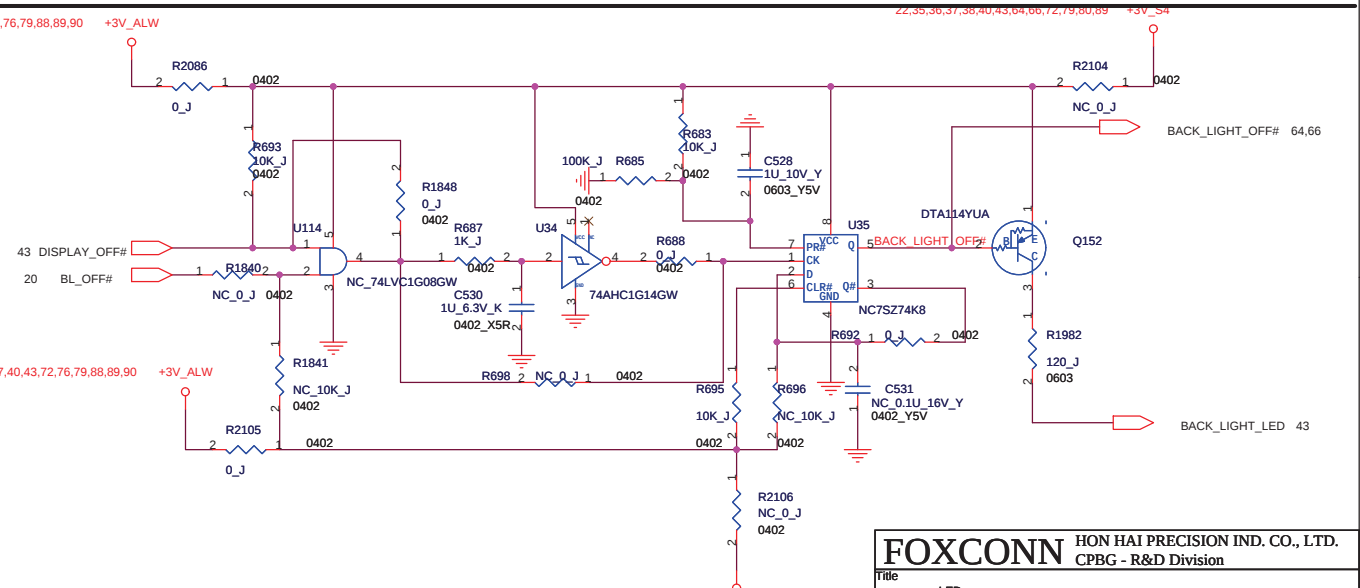
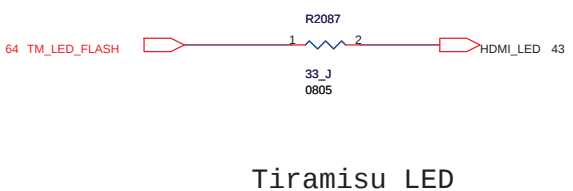
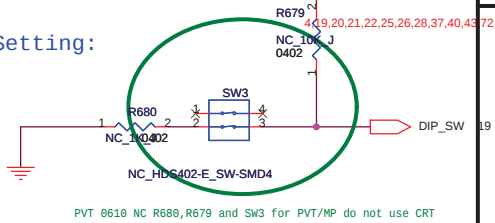
Place close CN41



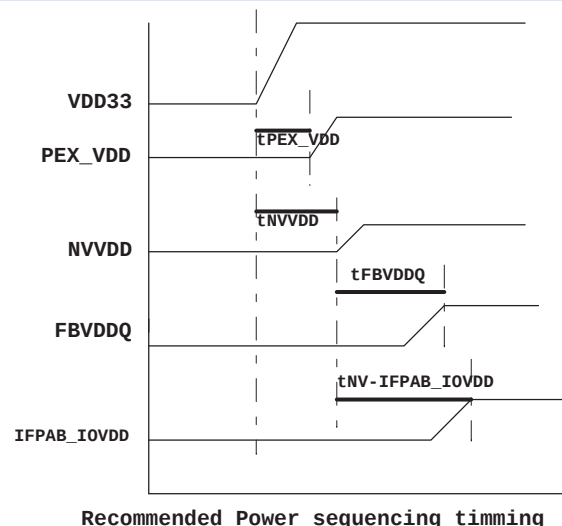
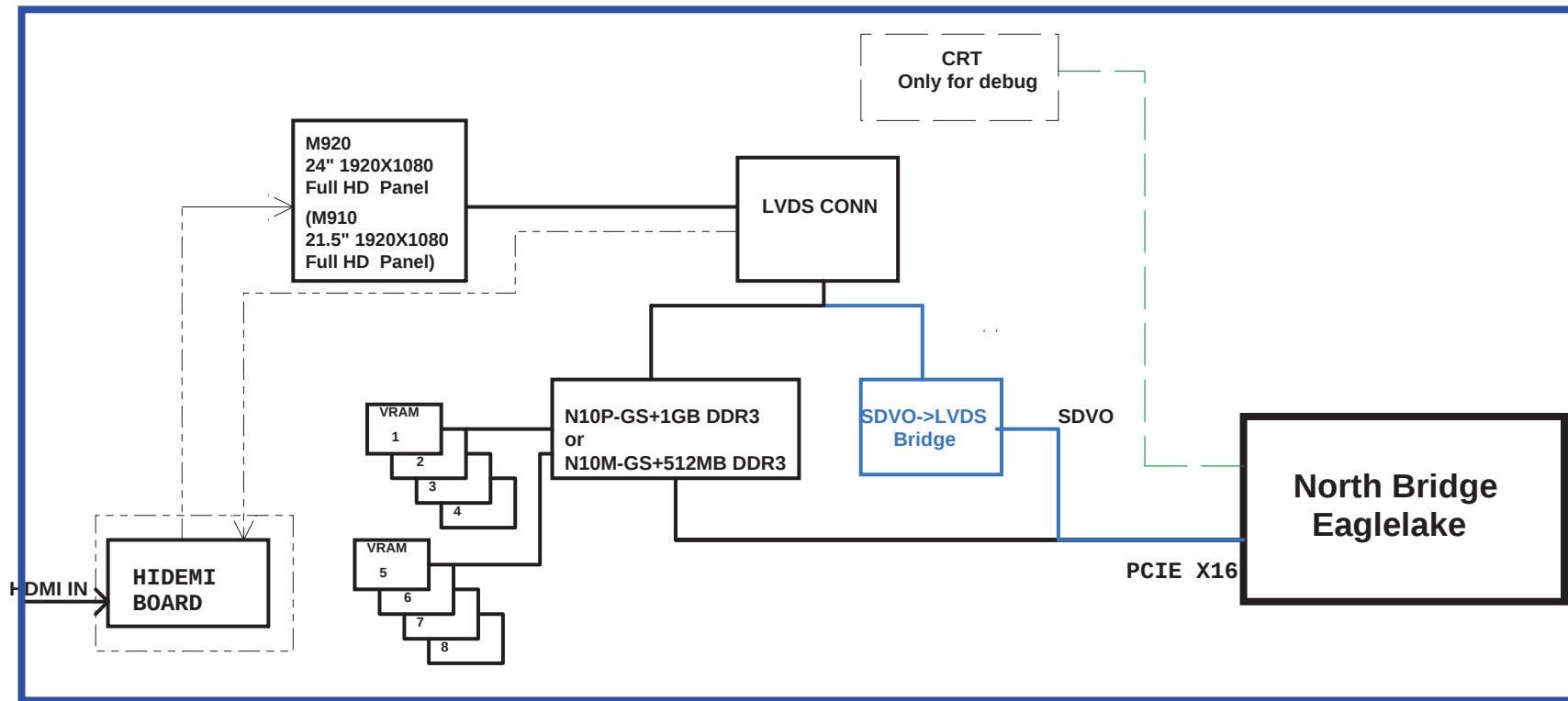
FOXCONN HON HAI PRECISION IND. CO., LTD.			
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DIP Switch Setting:
ON = CRT
Off = LCD



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note:
 $VDD33 = +3VRUN$
 $NVVDD = NV_VDD$
 $FBVDDQ = FBVDD = +1_5VRUN$

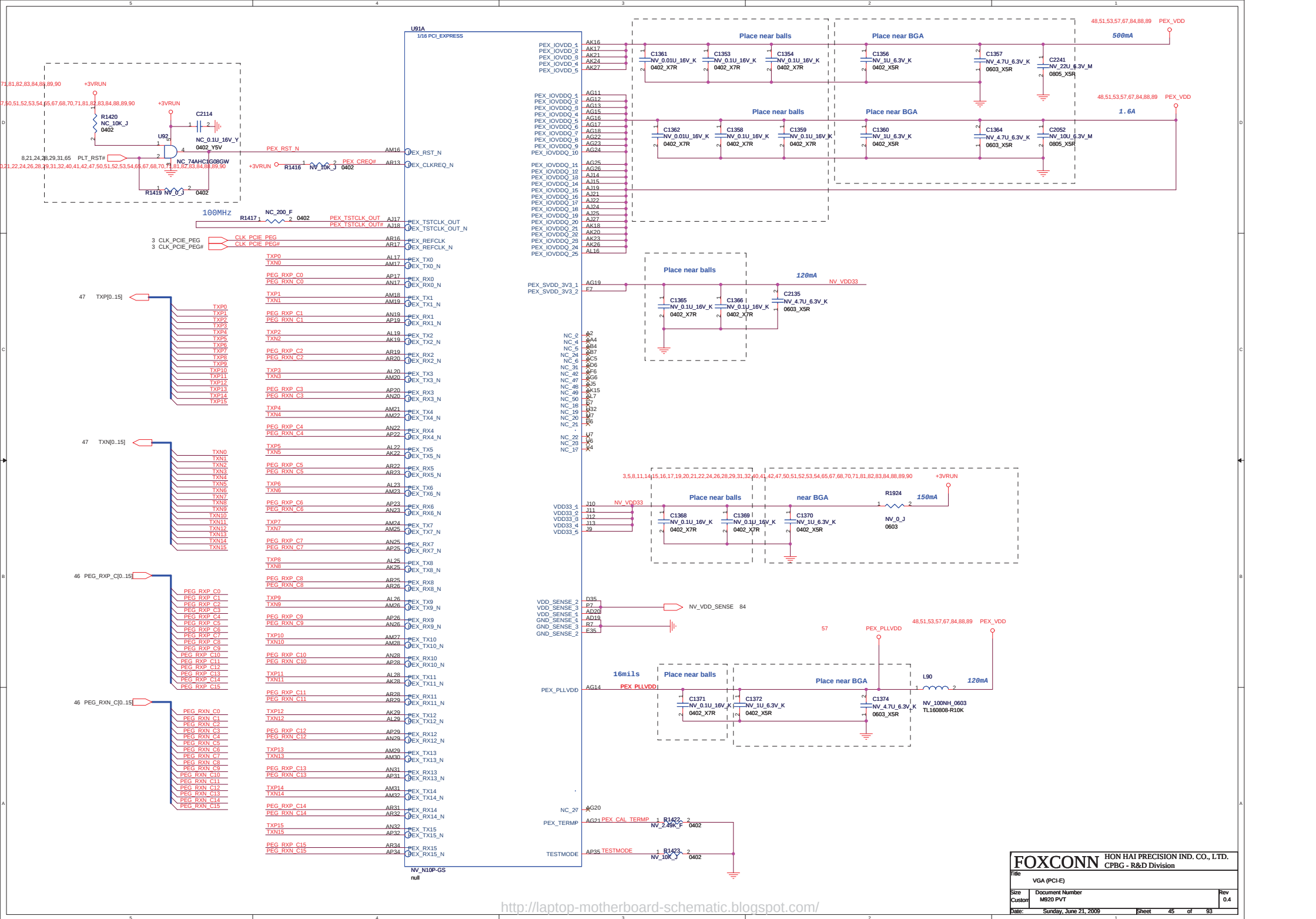
$t_{NVVDD} \geq 0$
 $t_{FBVDDQ} \geq 0$
 $t_{NV-IFPAB_IOVDD} > 0$
 $t_{PEX_VDD} > 0$ NV suggestion

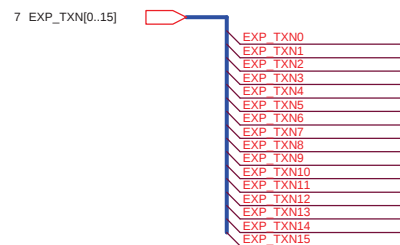
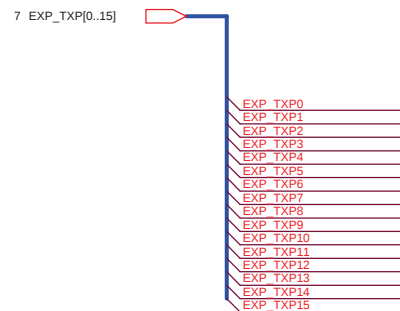
The ramp time for any rail must be more than 40 us

At any time
 $NVVDD \leq VDD33 + 0.5V$
 $FBVDDQ \leq VDD33 + 0.5V$

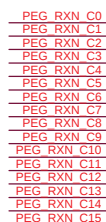
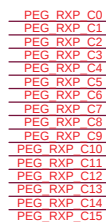
NOTE:

Head value table		
M920 H	NV_	NP_
M920 M	NV_	
M920 L	CA_	
M920 MST	NV_	NP_ TM_





EXP_TXP0	C1420	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C0
EXP_TXN0	C1421	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C0
EXP_TXP1	C1422	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C1
EXP_TXN1	C1423	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C1
EXP_TXP2	C1424	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C2
EXP_TXN2	C1425	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C2
EXP_TXP3	C1426	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C3
EXP_TXN3	C1427	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C3
EXP_TXP4	C1428	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C4
EXP_TXN4	C1429	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C4
EXP_TXP5	C1430	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C5
EXP_TXN5	C1431	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C5
EXP_TXP6	C1432	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C6
EXP_TXN6	C1433	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C6
EXP_TXP7	C1434	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C7
EXP_TXN7	C1435	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C7
EXP_TXP8	C1436	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C8
EXP_TXN8	C1437	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C8
EXP_TXP9	C1438	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C9
EXP_TXN9	C1439	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C9
EXP_TXP10	C1440	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C10
EXP_TXN10	C1441	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C10
EXP_TXP11	C1442	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C11
EXP_TXN11	C1443	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C11
EXP_TXP12	C1444	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C12
EXP_TXN12	C1445	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C12
EXP_TXP13	C1446	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C13
EXP_TXN13	C1447	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C13
EXP_TXP14	C1448	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C14
EXP_TXN14	C1449	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C14
EXP_TXP15	C1450	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C15
EXP_TXN15	C1451	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C15



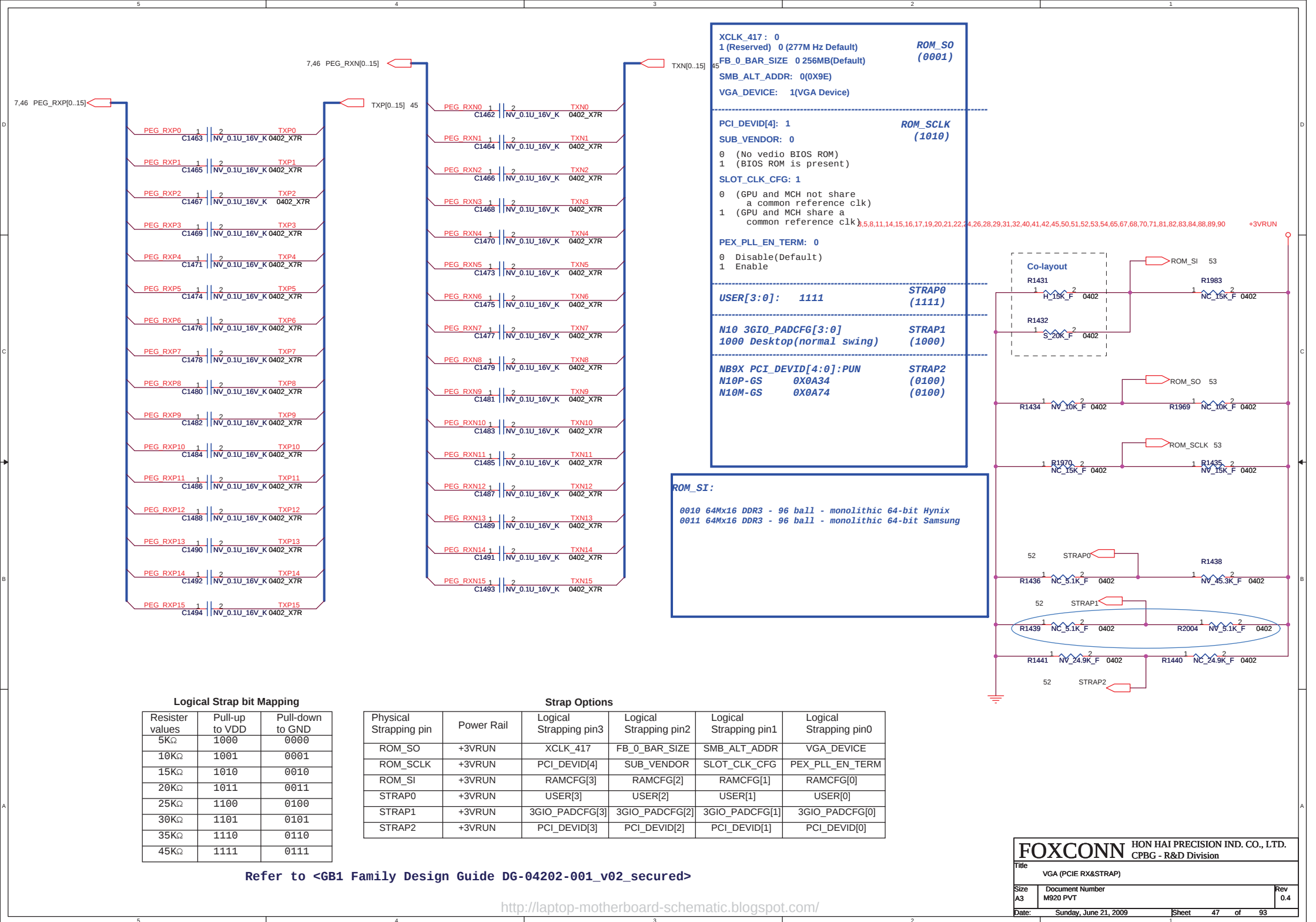
close to NB

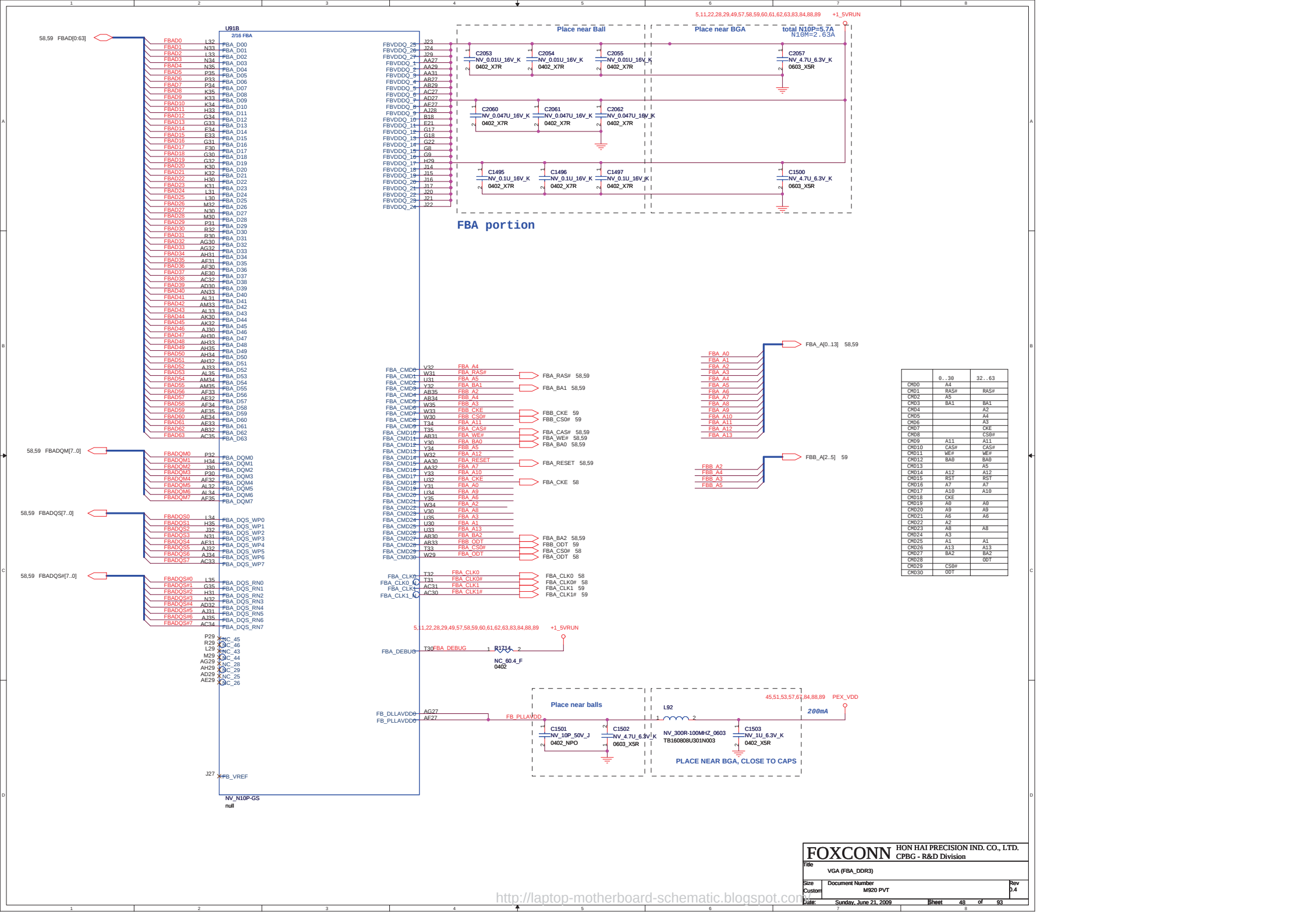
EXP_TXP0	0402_X7R	2	1	CA 0.1U_16V_K	C1452	SDVOB_RED+	SDVOB_RED+	65
EXP_TXN0	0402_X7R	2	1	CA 0.1U_16V_K	C1453	SDVOB_RED-	SDVOB_RED-	65
EXP_TXP1	0402_X7R	2	1	CA 0.1U_16V_K	C1454	SDVOB_GREEN+	SDVOB_GREEN+	65
EXP_TXN1	0402_X7R	2	1	CA 0.1U_16V_K	C1455	SDVOB_GREEN-	SDVOB_GREEN-	65
EXP_TXP2	0402_X7R	2	1	CA 0.1U_16V_K	C1456	SDVOB_BLUE+	SDVOB_BLUE+	65
EXP_TXN2	0402_X7R	2	1	CA 0.1U_16V_K	C1457	SDVOB_BLUE-	SDVOB_BLUE-	65
EXP_TXP3	0402_X7R	2	1	CA 0.1U_16V_K	C1458	SDVOB_CLK+	SDVOB_CLK+	65
EXP_TXN3	0402_X7R	2	1	CA 0.1U_16V_K	C1459	SDVOB_CLK-	SDVOB_CLK-	65

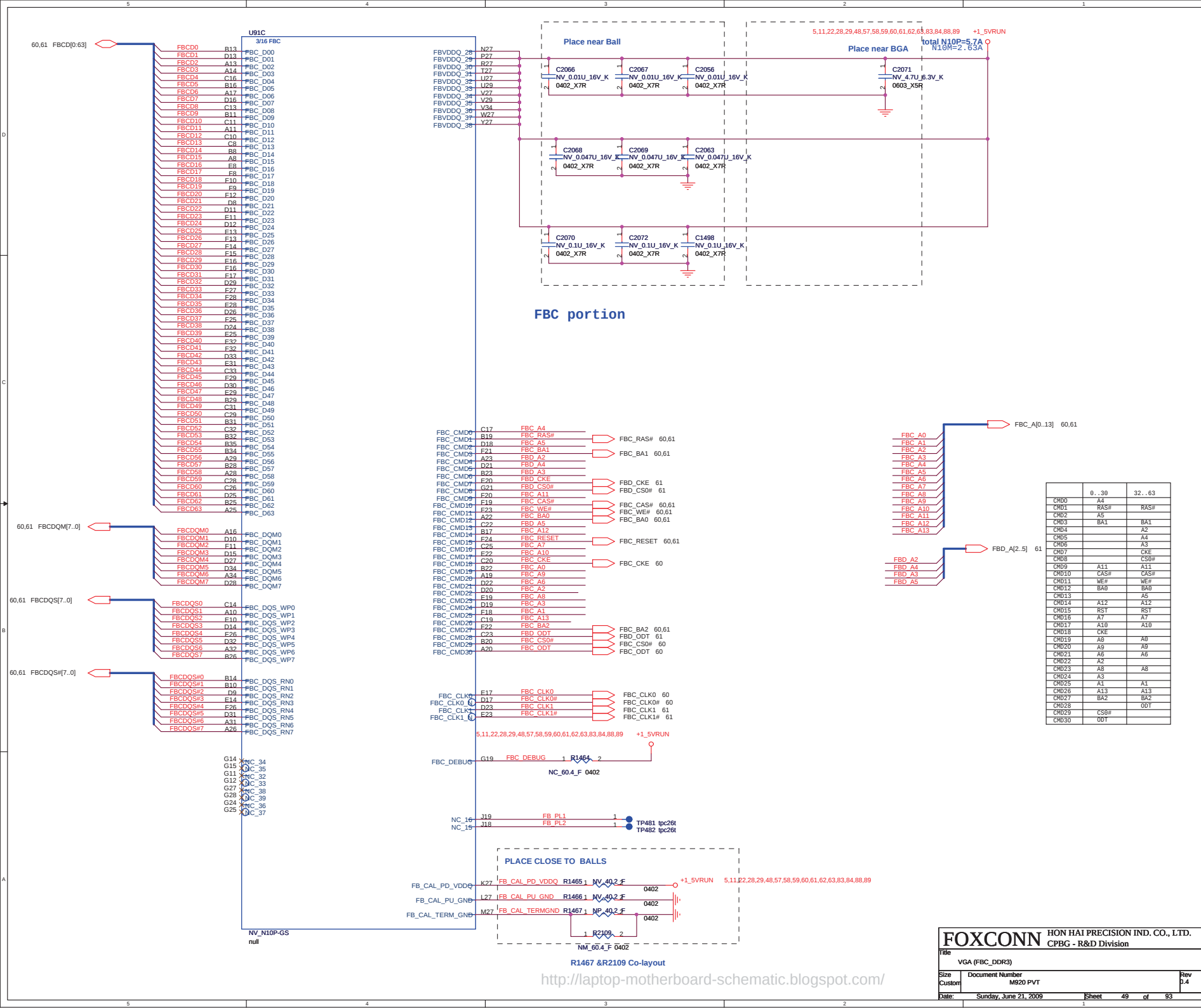
close to NB

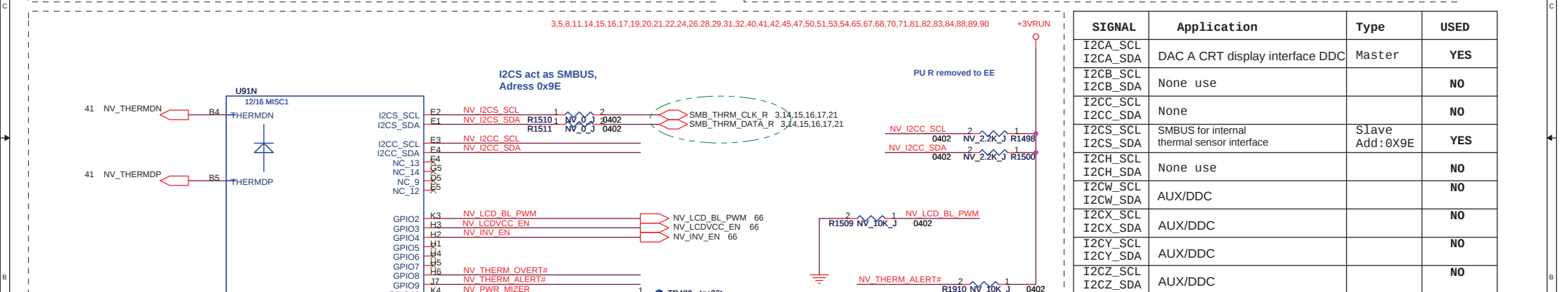
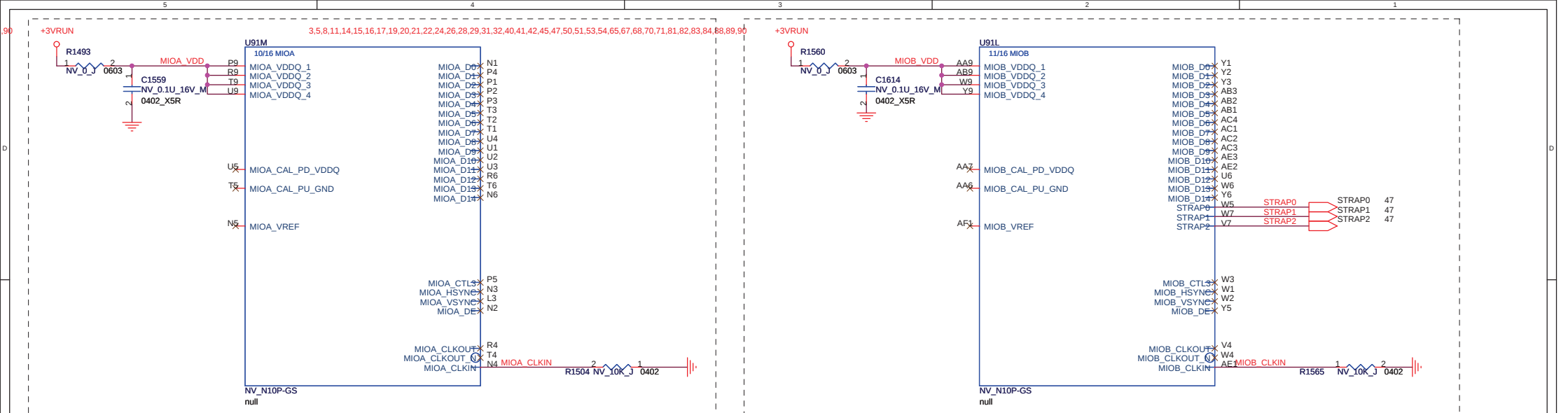
7.47	PEG_RXN2	0402_X7R	2	1	CA 0.1U_16V_K	C1460	STALL-	STALL-	65
7.47	PEG_RXP2	0402_X7R	2	1	CA 0.1U_16V_K	C1461	STALL+	STALL+	65

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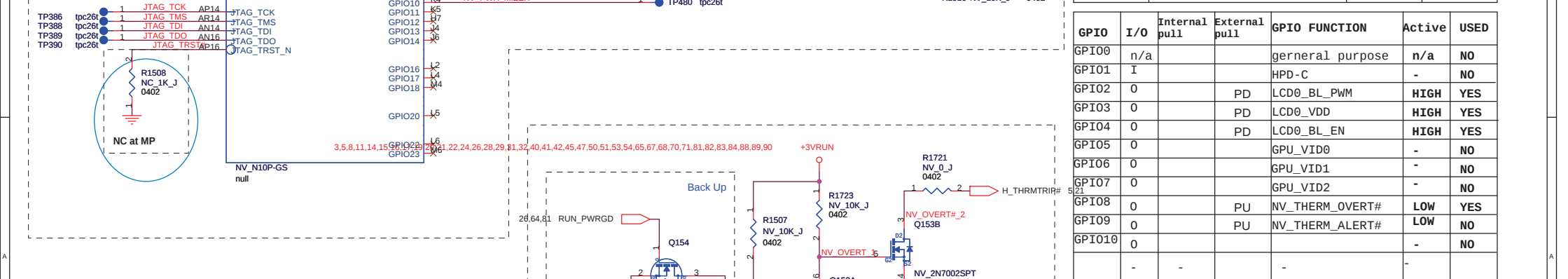








SIGNAL	Application	Type	USED
I2CA_SCL	DAC A CRT display interface DDC	Master	YES
I2CA_SDA			
I2CB_SCL	None use		NO
I2CB_SDA			
I2CC_SCL	None		NO
I2CC_SDA			
I2CS_SCL	SMBUS for internal thermal sensor interface	Slave	YES
I2CS_SDA		Add:0X9E	
I2CH_SCL	None use		NO
I2CH_SDA			
I2CW_SCL	AUX/DDC		NO
I2CW_SDA			
I2CX_SCL	AUX/DDC		NO
I2CX_SDA			
I2CY_SCL	AUX/DDC		NO
I2CY_SDA			
I2CZ_SCL	AUX/DDC		NO
I2CZ_SDA			

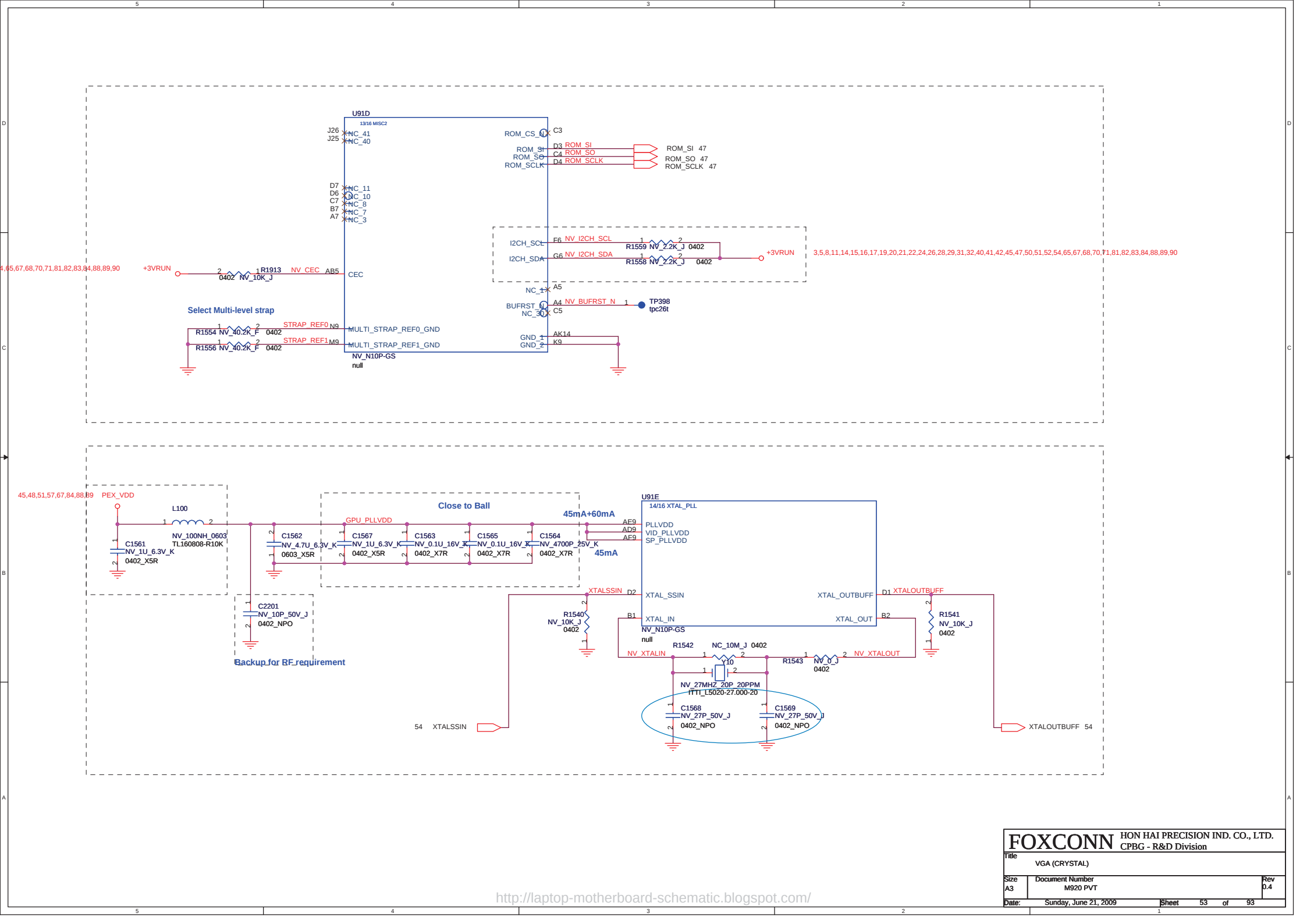


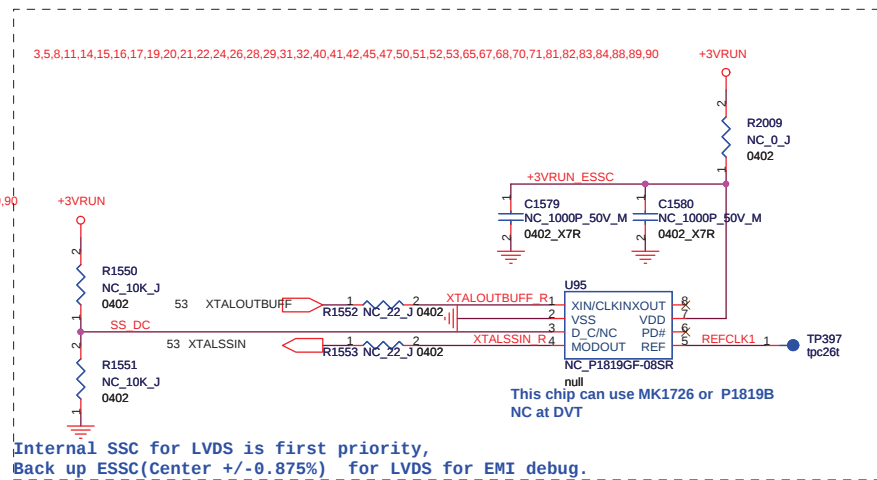
GPIO	I/O	Internal pull	External pull	GPIO FUNCTION	Active	USED
GPIO0	n/a			general purpose	n/a	NO
GPIO1	I			HPD-C	-	NO
GPIO2	0		PD	LCD0_BL_PWM	HIGH	YES
GPIO3	0		PD	LCD0_VDD	HIGH	YES
GPIO4	0		PD	LCD0_BL_EN	HIGH	YES
GPIO5	0			GPU_VID0	-	NO
GPIO6	0			GPU_VID1	-	NO
GPIO7	0			GPU_VID2	-	NO
GPIO8	0		PU	NV_THERM_OVERT#	LOW	YES
GPIO9	0		PU	NV_THERM_ALERT#	LOW	NO
GPIO10	0				-	NO

External pull-ups and pull-downs, when needed, must be 5-10Kohm

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Title	VGA (GPIO)
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M920 Change History

11/18 Initial release with NB9X v01

12/03 Rough for RFQ V02

12/04 Rough for RFQ V03

12/09 Rough for netin v04

12/15 Rough for netin v05

- 12/30
- 1.cancel PCIE lane reverse
 - 2.NC R1417 for PEX_CLK test
 - 3.NC AND gate U92 which for PEX_RST
 - 4.Correct GPU_VDD_SENSE reverse
 - 5.Change ROM_SO PD 10K
 - 6.Change ROM_SCLK 5K PU
 - 7.Del FB_CKE &CS0#&ODT 0ohm
 - 8.Del FB_CKE&ODT PD 10K
 - 9.Del GPU_Vref mizer funtion to fix Vref =0.5X
 - 10.Change FB_CAL_TERM_GND PD 40.2ohm to TP
 - "11.Share none use IFPC_PLLVDD&IFPD_PLLVDD, IFPC_IOVDD&IFPD_IOVDD,IFPE_IOVDD&IFPF_IOVDD with a common resistor 10K PD"
 - 12.PU GPIO_NV_THERM_ALERT# 10K
 - 13.camcel GPIO10 to TP
 - 14.Stuff R1508 JTAG_TRST_N
 - 15.PU I2CH 10K
 - 16.PU CEC 10K
 - 17.NC ESS

- 18.Change VRAM_CLK term R to 73.2ohm_F
- 19.Del VRAM_Vref_Mizer
- 20.Add 0.1u cap for Term resistor array
- 21.update VRAM symbol
- 22.Update Headvalue to NPd
- 23.Change TIRAMISU_CONN to 50 PIN
- 24.Change U106 from G546A to G546B
- 25.Change INVERTOR_CONNECTOR to 8PIN
- 26.Change SW_U105 &U101 Sel signal TIRAMISU_EXIST_SEL
- 27.Camcel BL_OFF# function on VGA page
- 28 add a cap for U102
- 29.Change LVDS connector to 1N-0040000-FWG0
- 30.I2C add 10pF
- 31.GPU Power add 22pF
- 32.FB_DATA_SWAP
- 33.FBVDDQ =+1_5VRAN
- 34.Change Power decoupling follow DG
- 35 Change L94 Form 240R to 220R follow DG

- 01/03
- 1.Add a 0.1uF cap for u92 NC.
 - 2.Change R1417 200_Ω to 200_Ω_F consist with M910
 - 3.Add a 4.7uF cap for PEX_SVDD
 - 4.Add a 0ohm Resistor for VDD33 backup for debug
 - 5.Revise PCIE_TX Off-Page name .
 - 6.Revise SDVO_AC coupling capacitance headvalue
 - 7.Revise DACA decoupling cap.
 - 8.Revise IFPAB_IOCDD latch.
 - 9.Del GPU_GPIO3&4 duplicate PD 10K
 - 10.Revise PLLVDD_SP_PLLVDD decoupling capacitance.
 - 11.Del TM_Exist_SEL duplicate PU.

- 01/07
- 1.reassign the TIRAMISU_50Pin connector pin assignent.
 - 2.Mirror LVDS_RP horizontally for layout requirement.
 - 3.Change GPU strap Pin,re define VRAM head value as Q_H_S_.
 - 4.Change LVDS connectoer pin assignment.

- 01/08
- 1.Change FBA_CMD term R assignment fro layout requirement.
 - 2.chang I2CH PD 10K to 2.2K.
 - 3.Change CN57 inverter connector to 10pin 1N-0010000-M1T0.
 - 4.Change CN57 Pin assignment.
 - 5.Change R1416 from 0 to 10K for PEX_CLKREQ#
 - 6,add NC_PU resistor for GPU strap.
 - 7,PD_FB_CAL_TERM_GND_NC_40.2ohm
 - 8,Delete C1786&L105 for CH7308B_LVDD,change L106 to 0603 size.

- 01/09
- 1.Del Ch7308 none use NC part R1662,R1651&R1652&R1658,
 - 2.Add c71 c72 for SDVO_Ctrl BUS
 - 4,Revise FB_CAL_TERM_GND PD 40.2ohm from NV to NC_
 - 5.TIRAMISU_Vedio_IN change to A_GND_T

- 01/13
- Add two cap for PEX_VDD
 - change L97 from 30R to 22R
 - change PEX_SVDD

- 01/14
- Change GPU strap pin
 - Change Rom_SCLK from 15K PD to 15K PU
 - Change strap 2 from 10K PU to 25K PD
 - Add a 0ohm NC resistor for ESSC_VCC

- 01/14
- Change INV_CONN pin assignment
 - Backup 3v3Run for IFPAB_IOVDD

- 01/19
- Back roll from 01/17 to 01/14
 - Change Q147 part
 - Add ICH_GPIO8 connect to TM_EXIST_SEL_NC back up

- 01/21
- 1.Change R1721 to NC.
 - 2.Change FBCAL_PU_GND R1466 40.2 -> 40.2ohm FBCAL_PD_VDDQ R1465 60.4 -> 40.2ohm FBCAL_TERM_GND R1465 NC -> 40.2ohm FBCLK Termination = R1568,R1581 73.2 -> 242ohm
 - 3.Change ODT Term &CKE term

EVT2

- 02/23
- 1.del VRAM Termination resistor.
 - 2.del excrement capacitance based on layout to cost down.
 - 3.NC CH7308B reserve pin and Bscan pin

- 02/25
- 1.Change +3V_ALW power to +3V_S4 for Tiramisu portion circuit.
 - 2.Add TM_HWS#

- 02/25
- 1.add a RC for LCDVCC_EN

- 03/02
- 1.Change Headvalue_NPD_ to NP_;
 - 2.Stuff R1721 for NV thermal alert.

- 03/03
- 1.Modified by Chen QianKun,add TMDS output solution.

- 03/09
- 1.update the power filter Cap&Bead&inductor based on DG v04.
 - NV_VDD two caps 0.01u change to 4700p
 - PEX_VDD two 0.1u chage to 0.01u
 - L90 change from 10nH to 100nH
 - L100 change from 120R/100MHz to 100nH
 - L92 change from 220R/100MHz to 300R/100MHz
 - L94 change from 220R/100MHz to 300R/100MHz
 - L96 change from 120R to 180R
 - L97 change from 220R to 180R

- 2.Rivise TMDS output circuit I2CW for DCC
- 3.del unused NC part R1574,R2015,R1588,R2088,R1602,R2019,R1616 and R2021
- 4.Del extra caps for VRAM bypass to cost down.

- 03/12
- 1.change TMDS DDC resistor to RP
 - 2.change net name HDMI_IN_DETECT to TM_SOURCE_IN_DETECT
 - 3,change net name HDMI_PC#_SELECT to TM_PC#_SELECT
 - 5.change Q154 latch signal from +3VRUN to RUN_PWRGD
 - 4,Add 0.1u between GND and A_GND

- 03/16
- 1. change tiramisu conn pin define
 - 2. change C2108 from 0.1uf to 0.01uf
 - 3. change D68? from 16-RSB12JS-2000 to 16-PESD5V2-S200

- 03/16_2
- 1. Change TM_SUS_ON# circuit
 - 2. NC CAP33 and change C1793 from 4.7u to 10u.
 - 3. Change r2025 from 0ohm to 10Kohm
 - 4. NC RF solution caps
 - 5. NC ESSC

- 03/16_2
- 1. PD_IFPCD power
 - 2. PD_IFPCD RSET

DVT

- 04/08
- 1. P49, Change FB_CAL_TERM_GND resistor for 10M_SKU
 - 2. P53, Change the CRYSTAL caps C1568,C1569 from 1C-2N20270-J000 to 1C-2N20200-J600

- 04/14
- 1.P51/P67, NC tiramisu MST solution parts : R2057,R2058,R2108,R2034,L118,L119, C2276,C2277,C2278,C2282,C2283,C2284,RP95,RP96,RP97,RP98,RP99,D68,D70, R2038,C2269,C2270,C2271,C2272,C2273,C2274,C2279
 - 2.P66, Del C1795,R2025 change to 1K, CAP33 change to 330uF , add discharge circuit
 - 3.P47, Del Qimonda strap resistor R1433
 - 4.P51, Del IFPAB-IOVDD backup +3VRUN circuit R2011

- 04/15
- 1.P48/P49/P58/P59/P60/P61,change net name FBA(C)WDQS[7..0] to FBA(C)DQS[7..0], change FBA(C)RDQS[7..0] to FBA(C)DQS#[7..0].
 - 2,P67,Change RP95,RP96,RP97,RP98,RP99 from 1R-1010000-JP00 to 1R-1010000-JX00.

- 04/17
- 1.P64, Change CN56 PIN 1 to +5V_ALW PIN 5 to DC_OUT,Change F18 from 1M-F6V0A25-F000 to 1M-F6V0A75-0000.
 - 2.P66,Change C1793 from 1C-2B70106-M100 to 1C-33R0157-M101. Change R1669 from 1R-0000471-J300 to 1R-0000101-J300 and stuff it.
 - 3.P51, Change IFPAB-IOVDD from +1_8V_S3_SUS to +3VRUN

- 04/18
- 1.P64, Change C2120,C2122 from 1C-2B20471-K000 to 1C-2N20221-K000 and stuff it as audio request.
 - 2.P66, Change R1669 from 1R-0000101-J300 to 1R-0000101-J600 .

- 04/20
- 1.P66, Add a 10uF cap C ? .

PVT

- 06/02
- 1.Page 51 Change IFPAB_ABIOVDD power latch circuit (Q141).
 - 2.Page 47 Change strap 1 from PD 5K to PU 5K according to Nvidia N10x GPU qualification.
 - 3.Nc CRT function for H&M_SKU.
 - 4,NC R1508

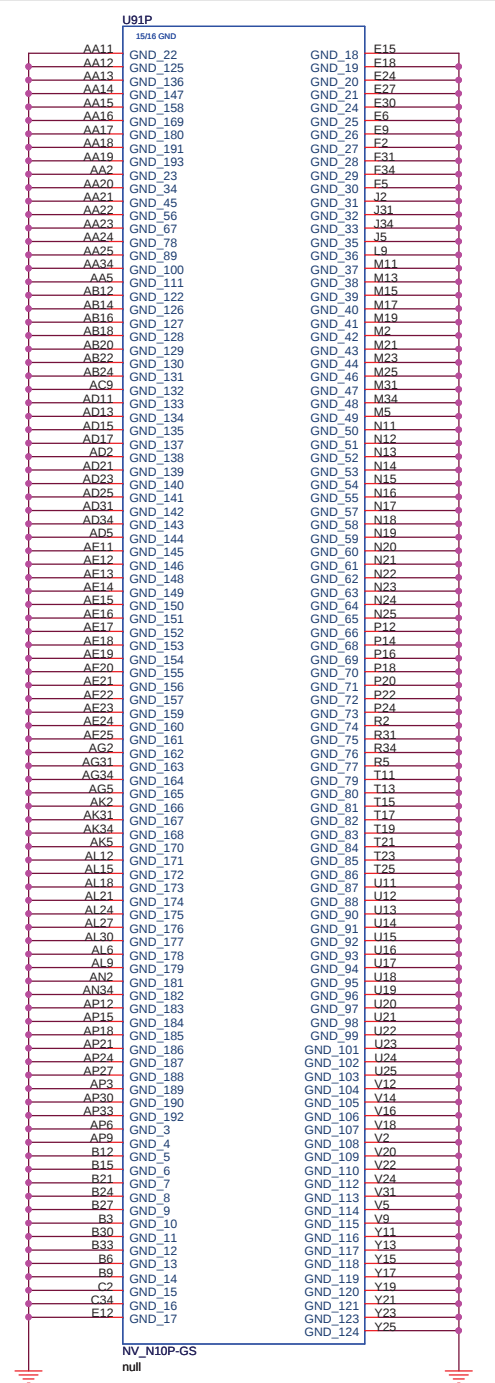
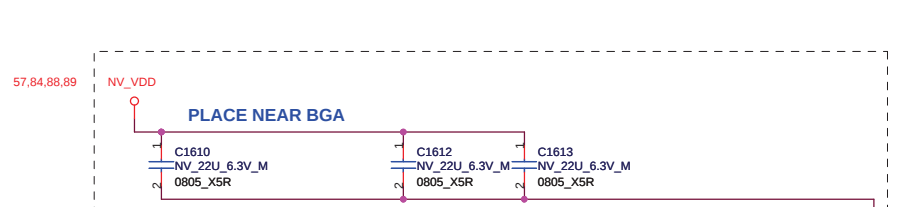
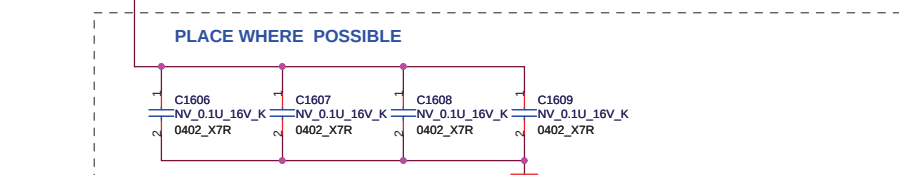
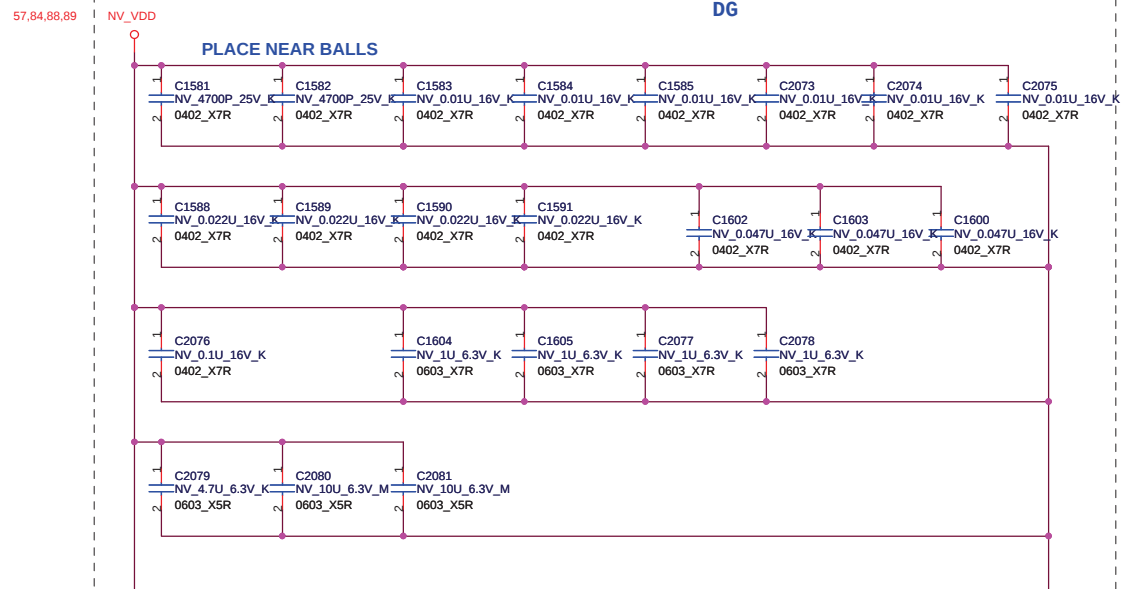
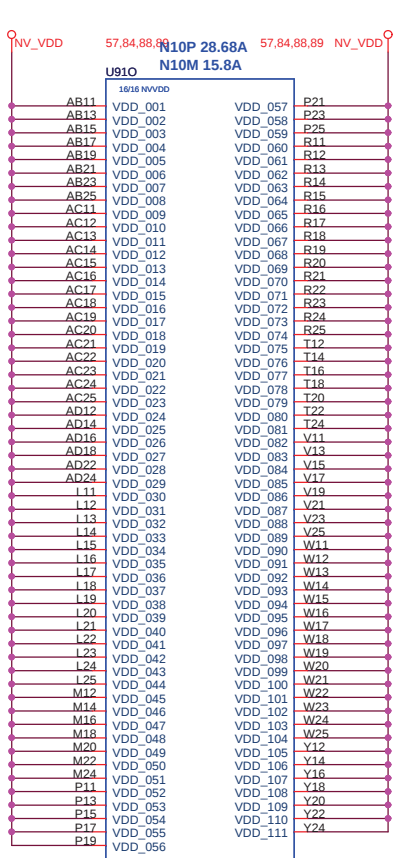
- 06/15
- 1.Change CN56 Pin1 from +5V_ALW to DC_OUT.Change F18 from 1M-F6V0A75-0000 to 1M-F6V0A25-F000.

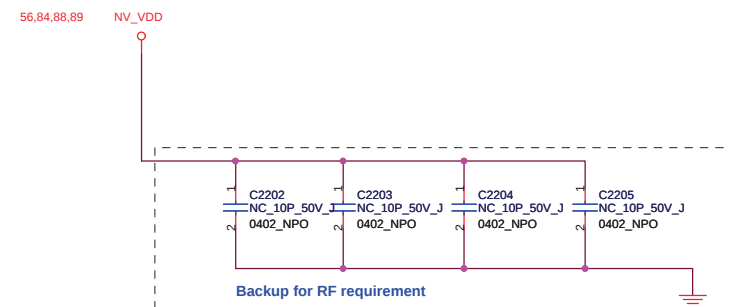
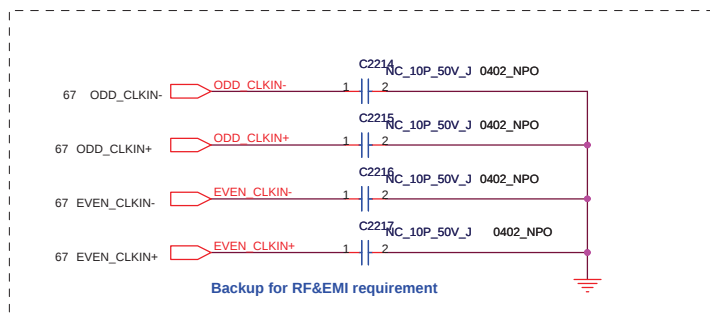
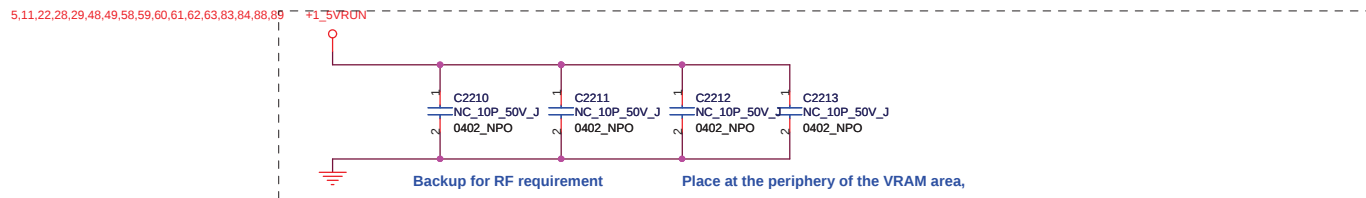
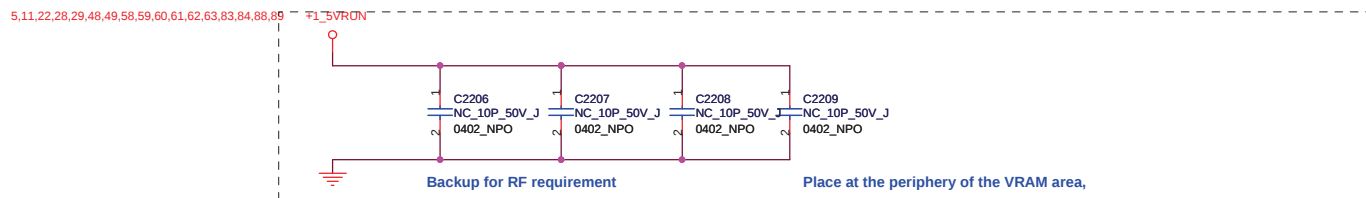
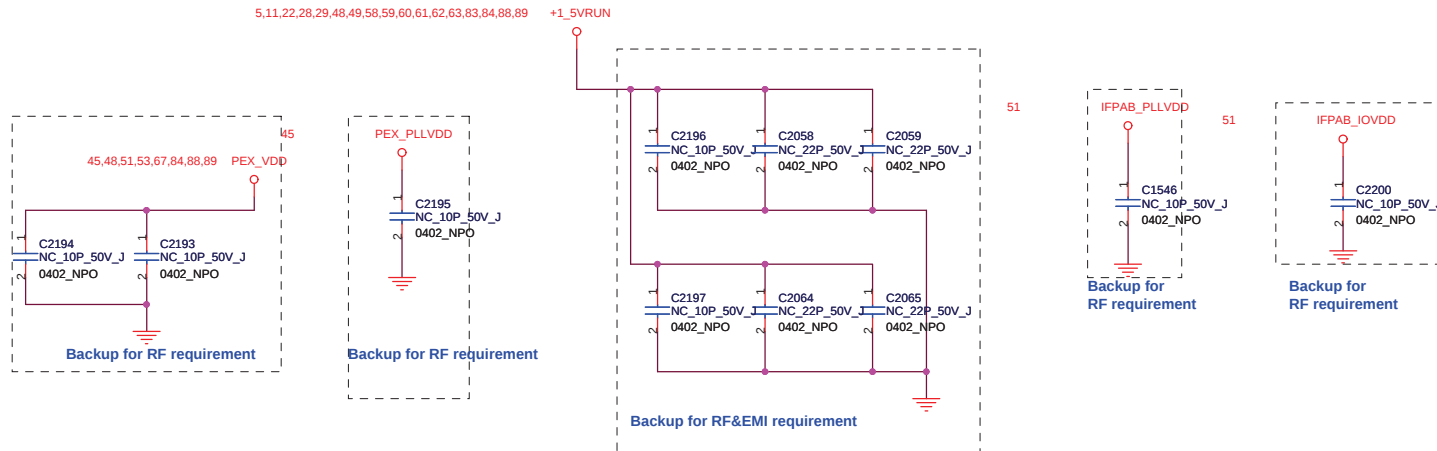
- 06/18
- 1.P67 Change IFPCD_PLLVDD power rail from PEX_VDD to +3VRUN.
 - 2.P53 Change C1568 and C1569 from 1C-2N20200-J600 to 1C-2N20270-J000.

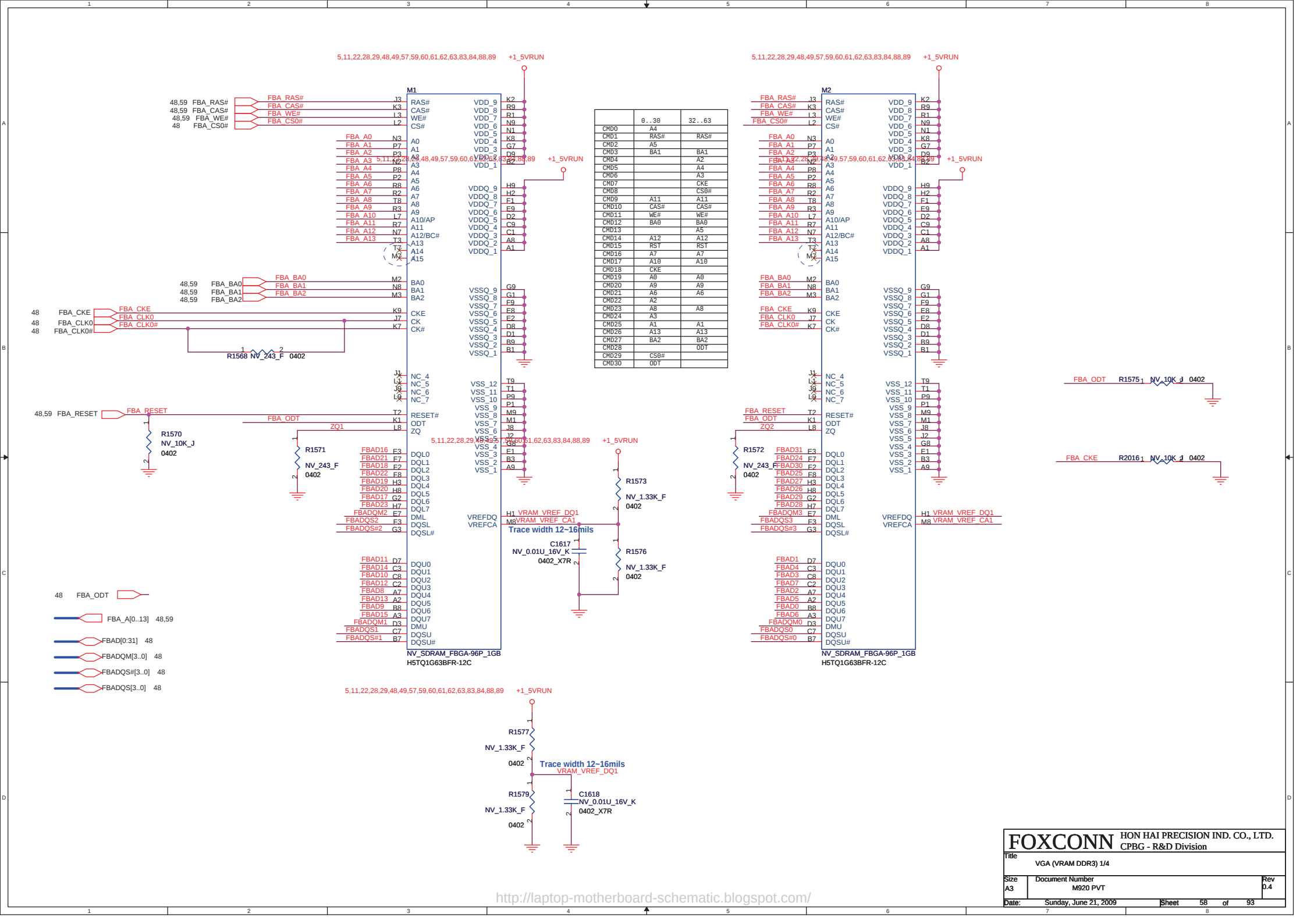
- 06/19
- 1.P64 Add one fuse F? between DC_OUT and CN56.

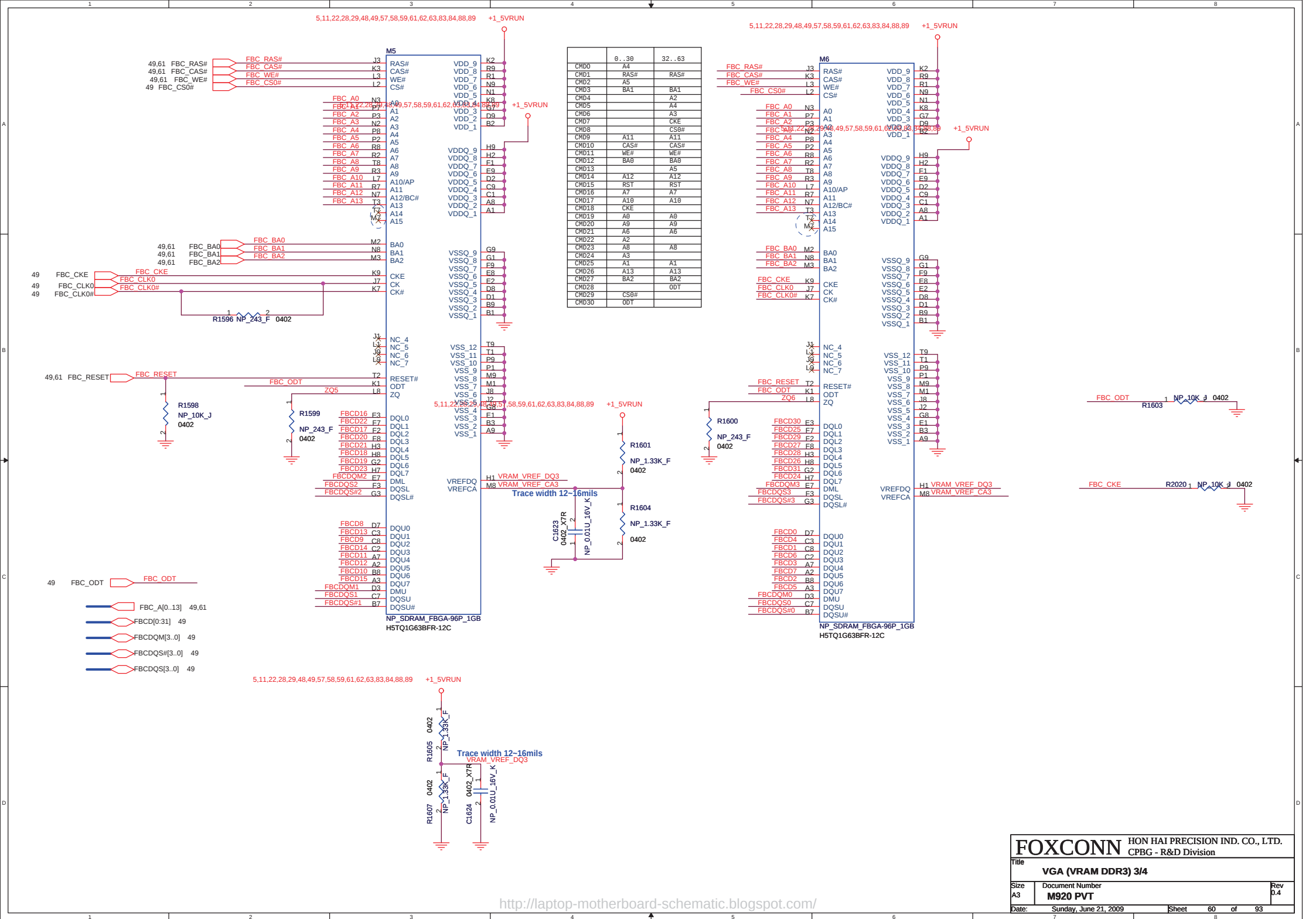
- 06/20
- 1.Add discharge ciruit for IFPAB_IOVDD

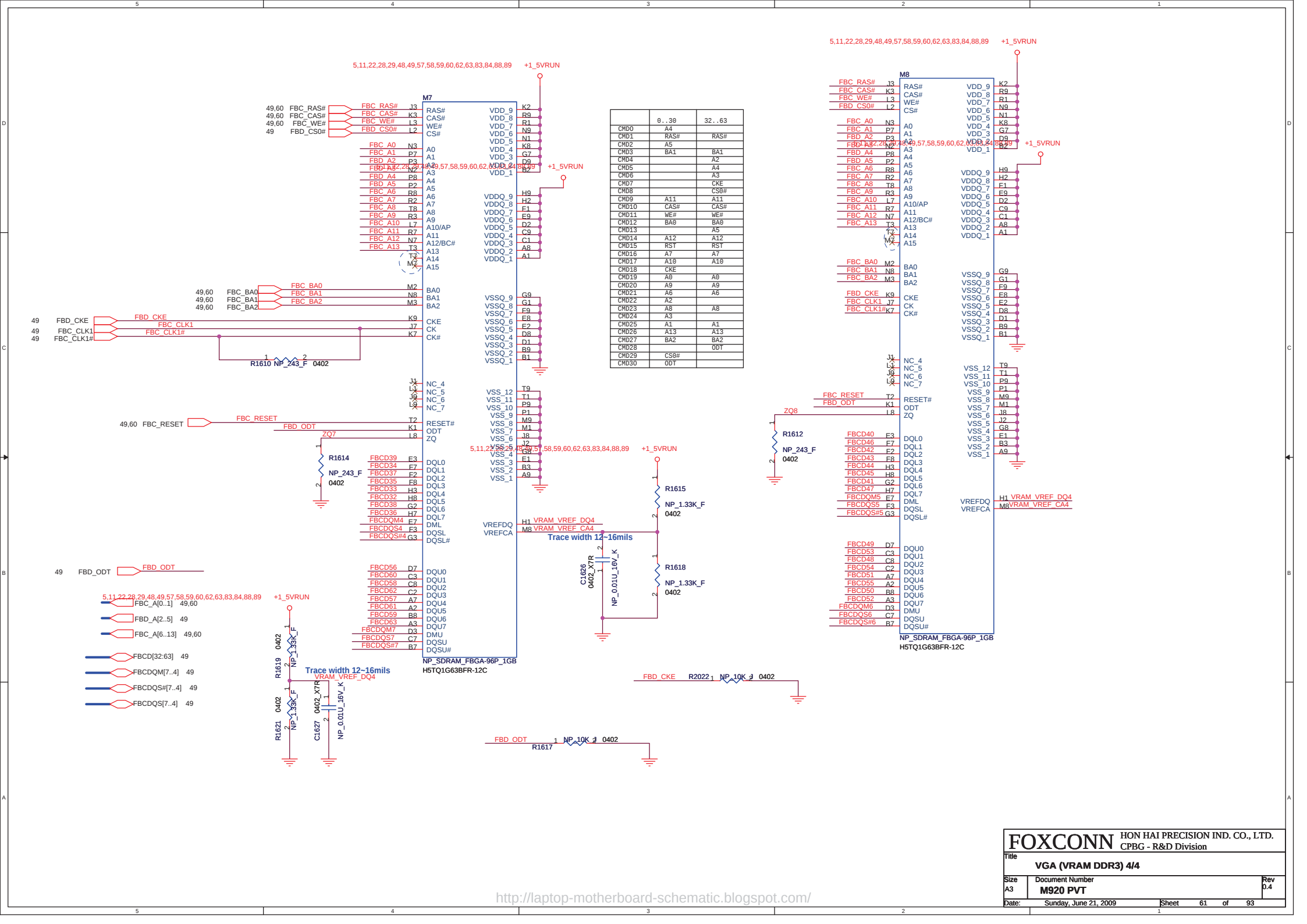
FOXCONN			HON HAI PRECISION IND. CO., LTD.		
Title			CPBG - R&D Division		
VGA (PWR&GND)					
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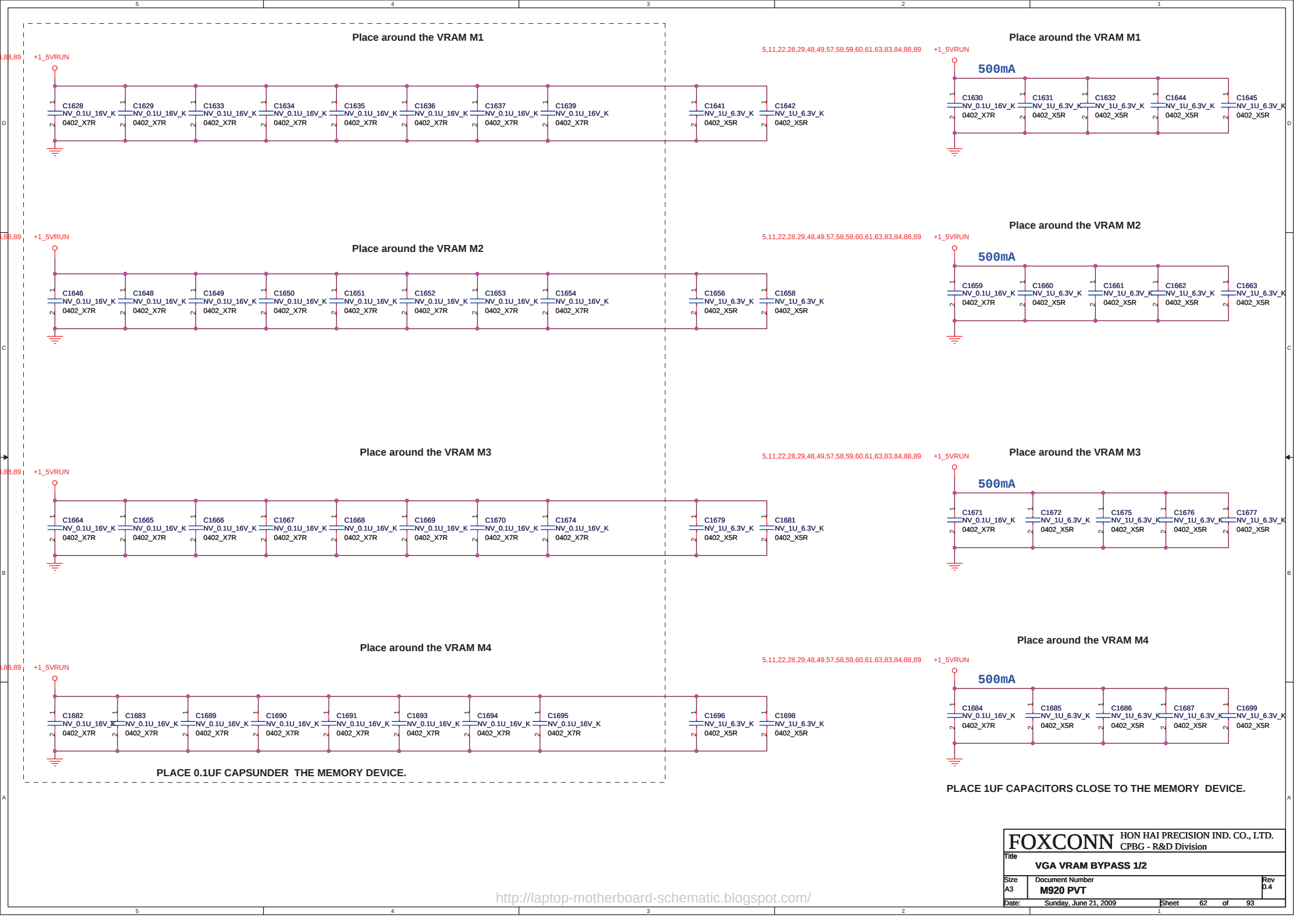


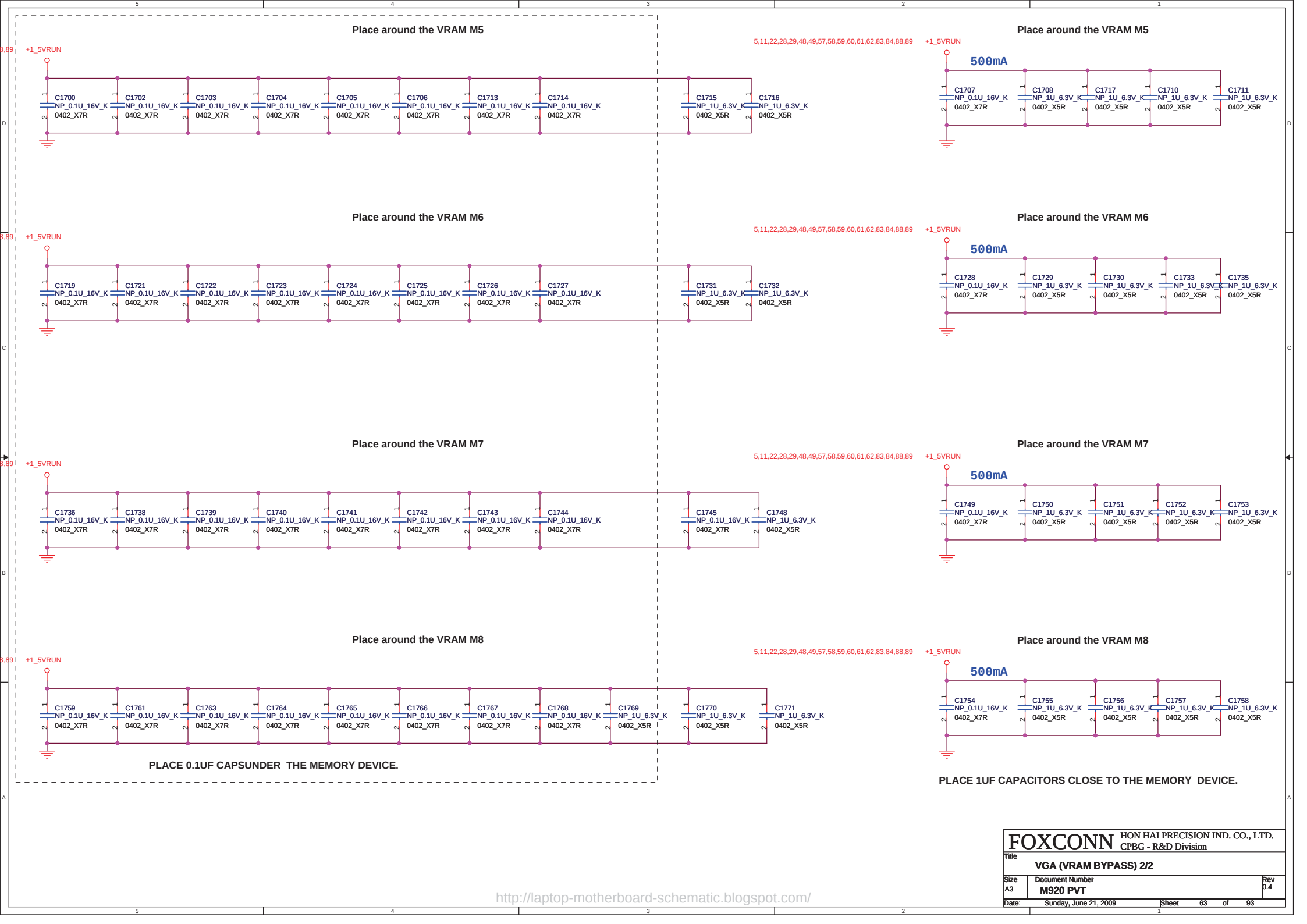












Place around the VRAM M5

Place around the VRAM M5

Place around the VRAM M6

Place around the VRAM M6

Place around the VRAM M7

Place around the VRAM M7

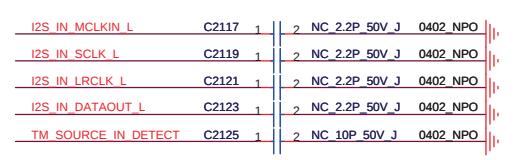
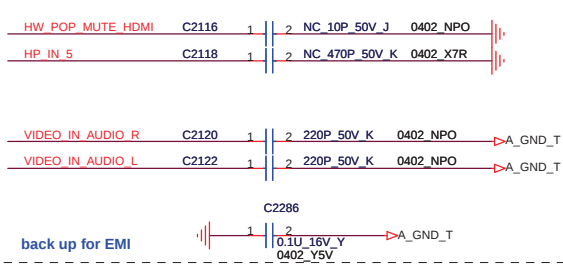
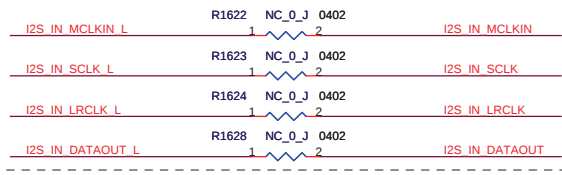
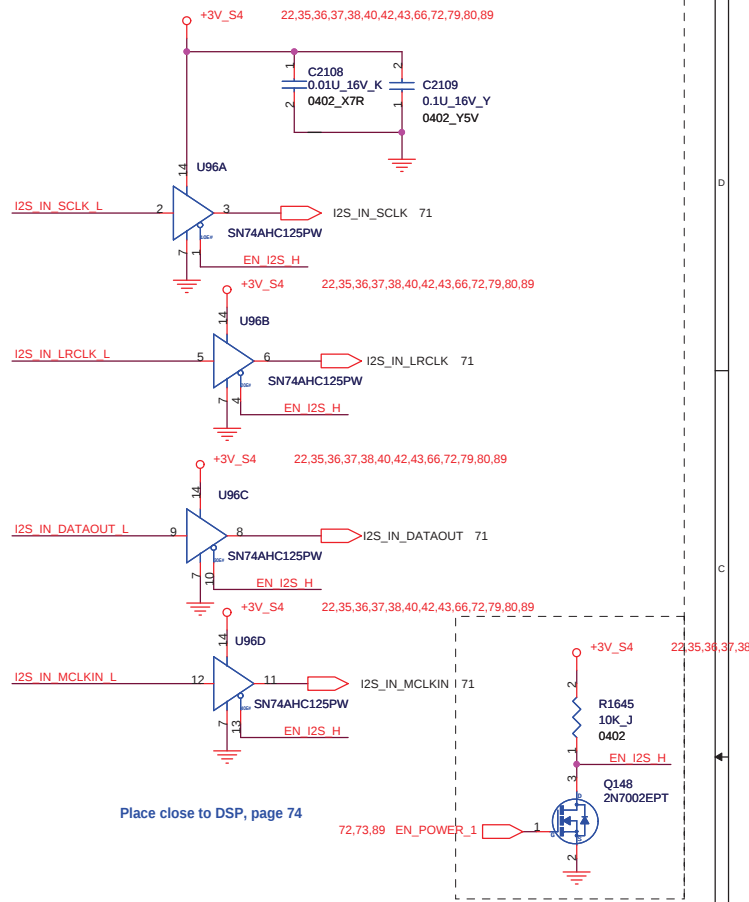
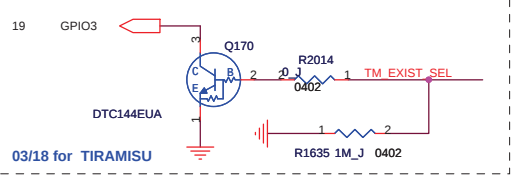
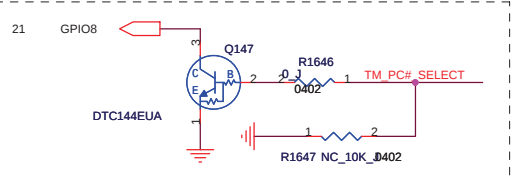
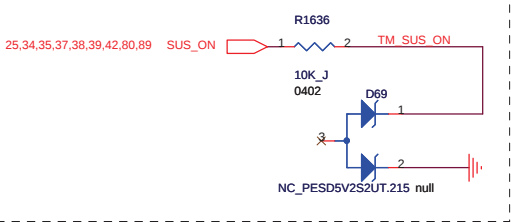
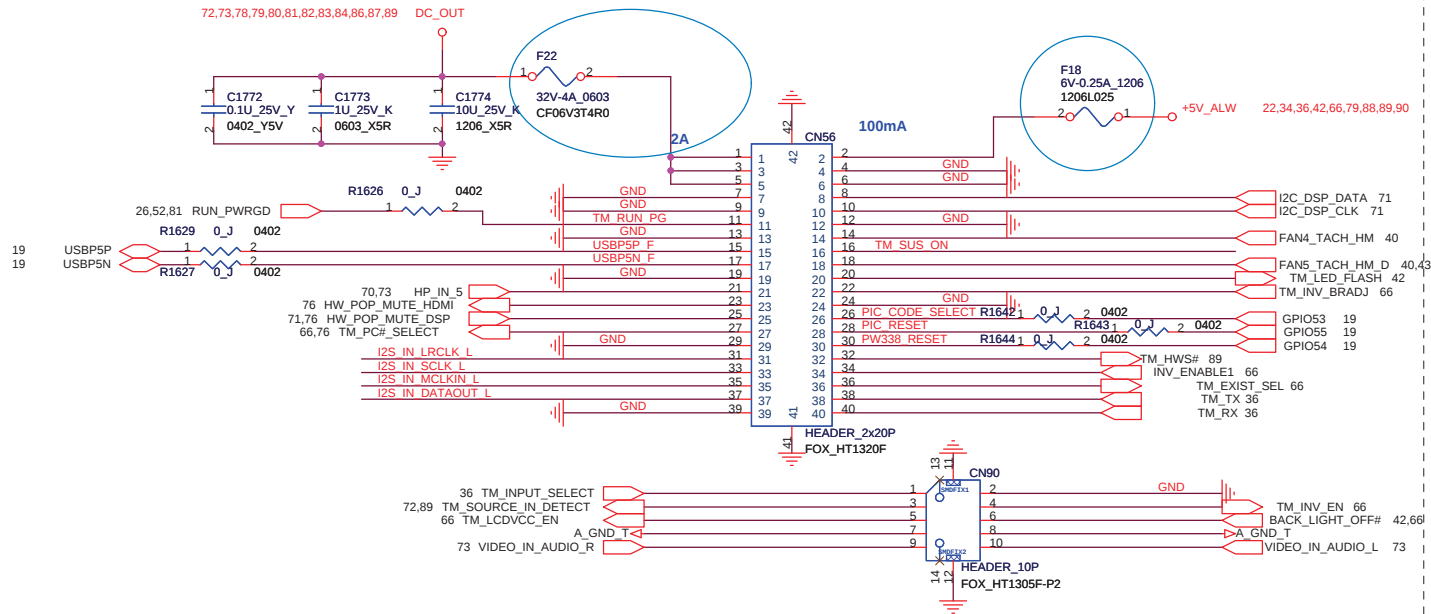
Place around the VRAM M8

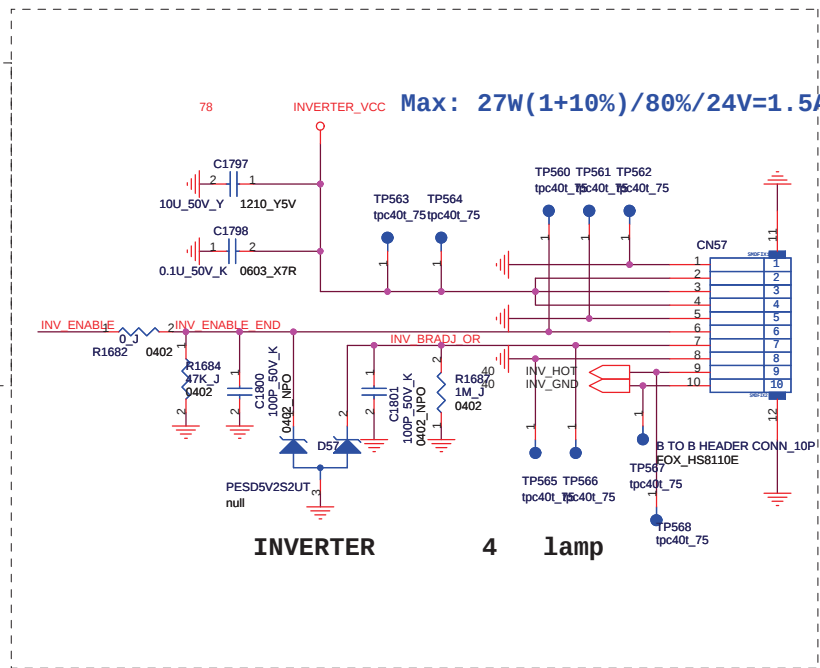
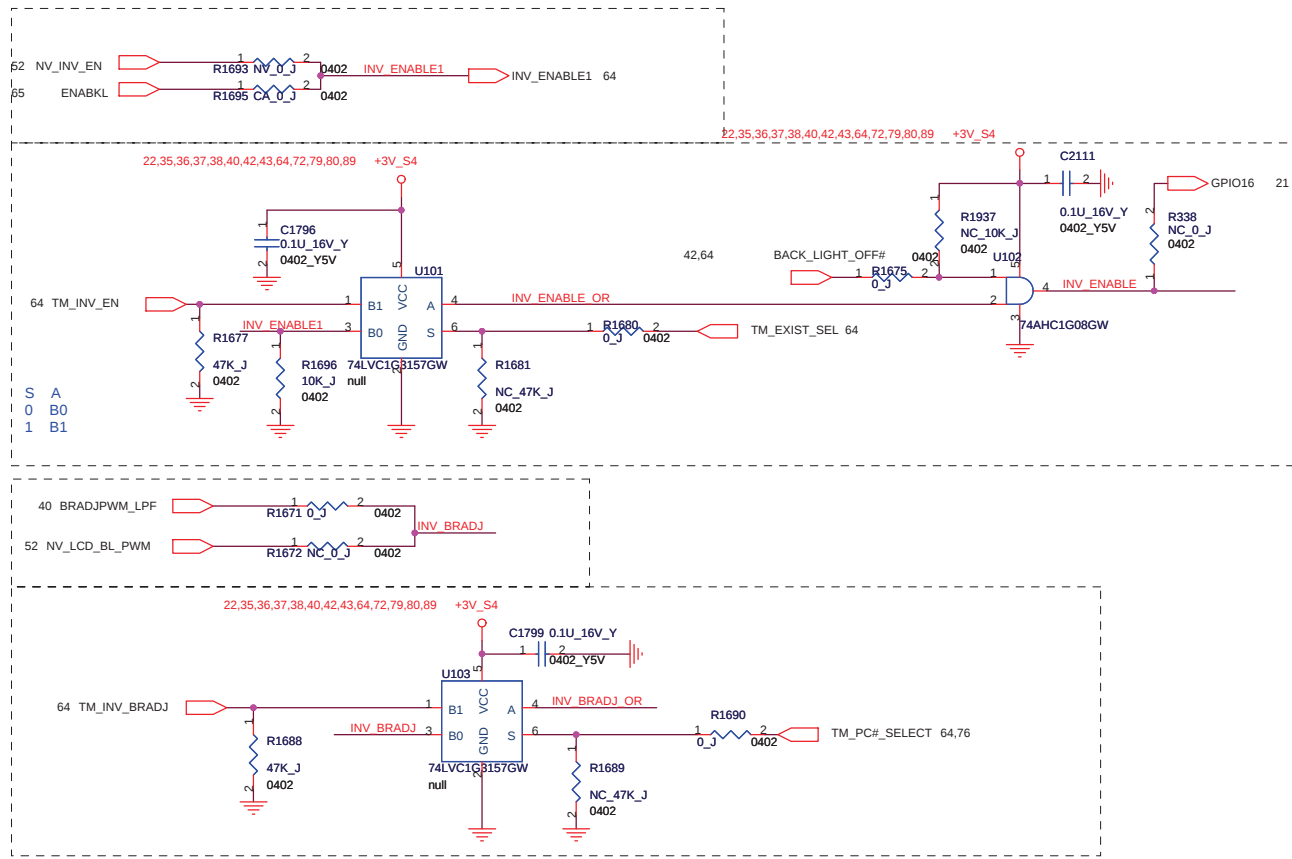
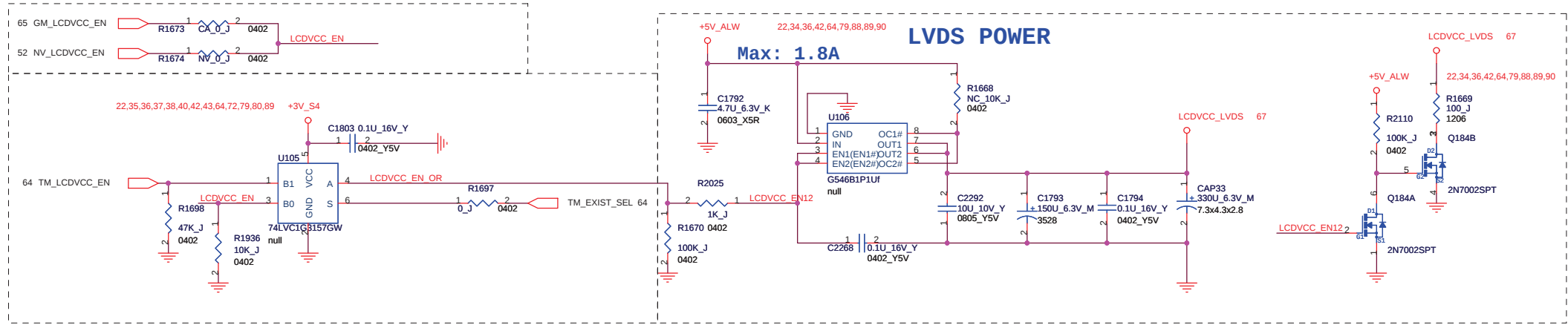
Place around the VRAM M8

PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

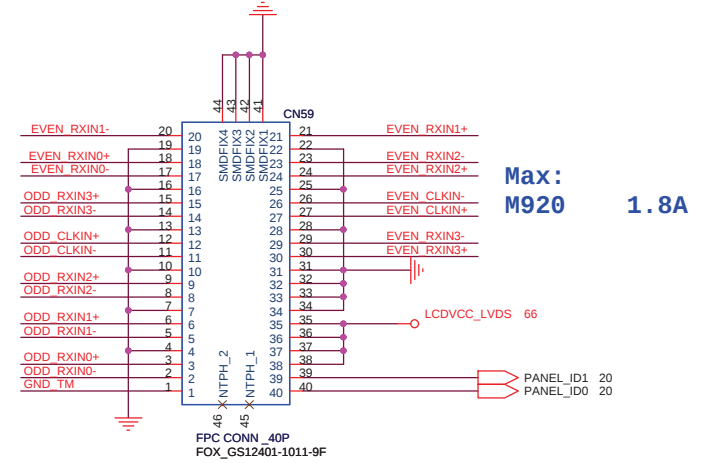
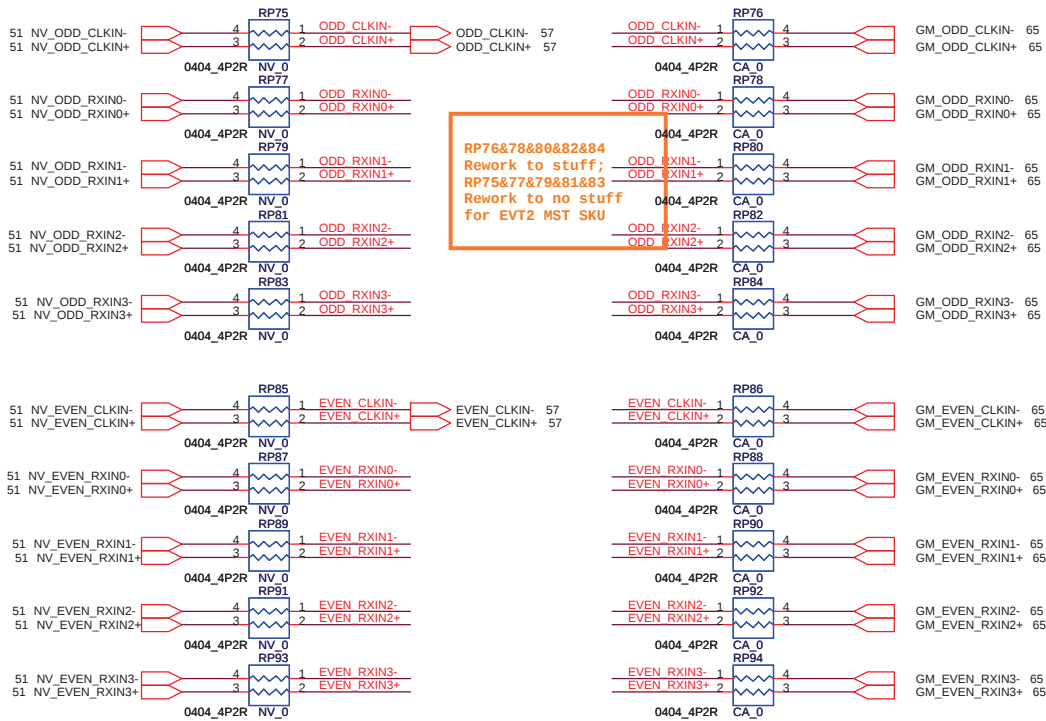
PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

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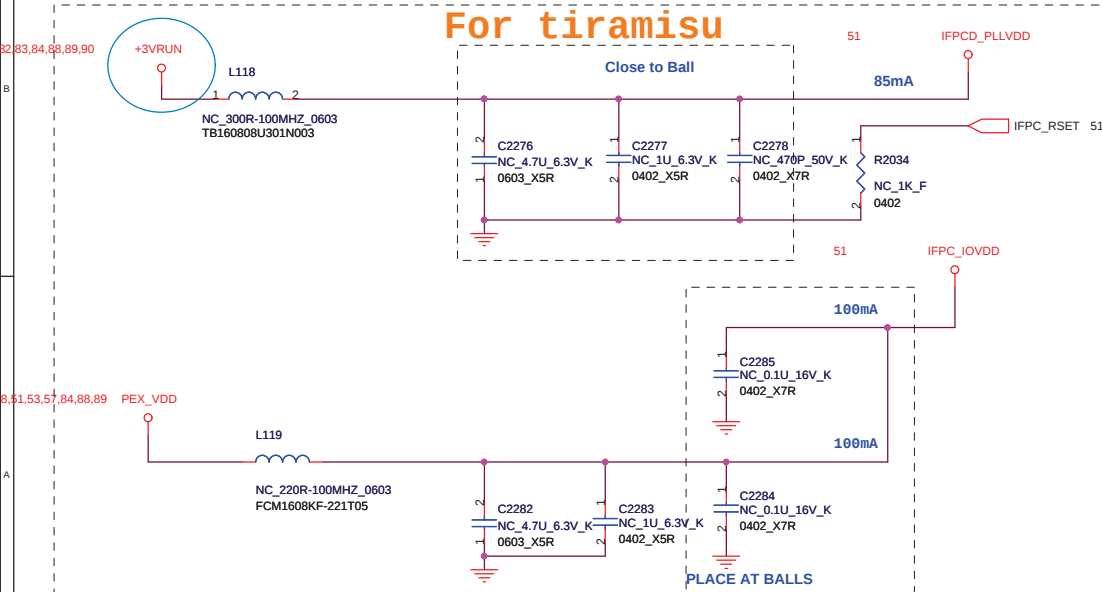


For tiramisu

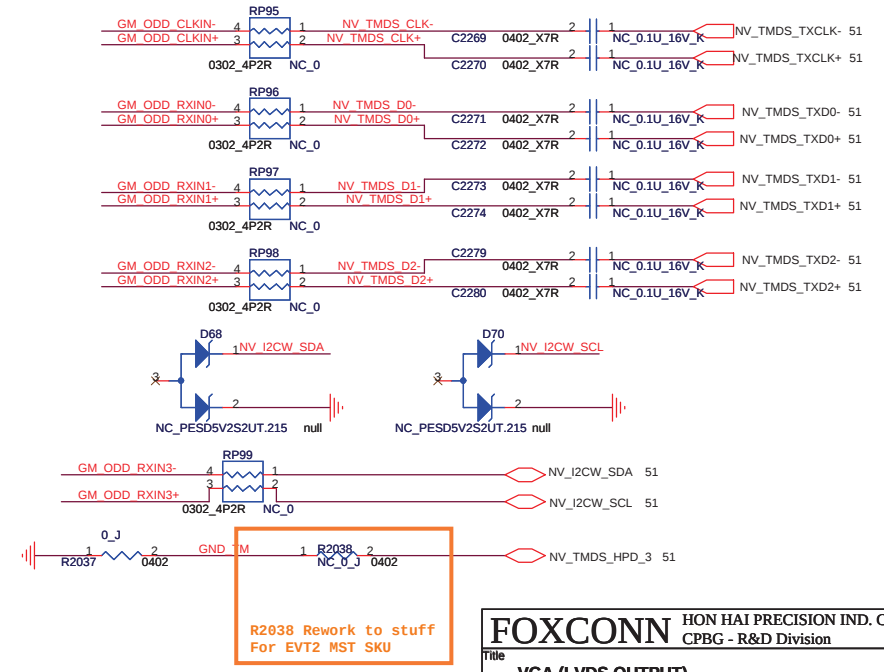


Panel ID		
00	AU0 24" 1920*1080 M240HW01 V0	

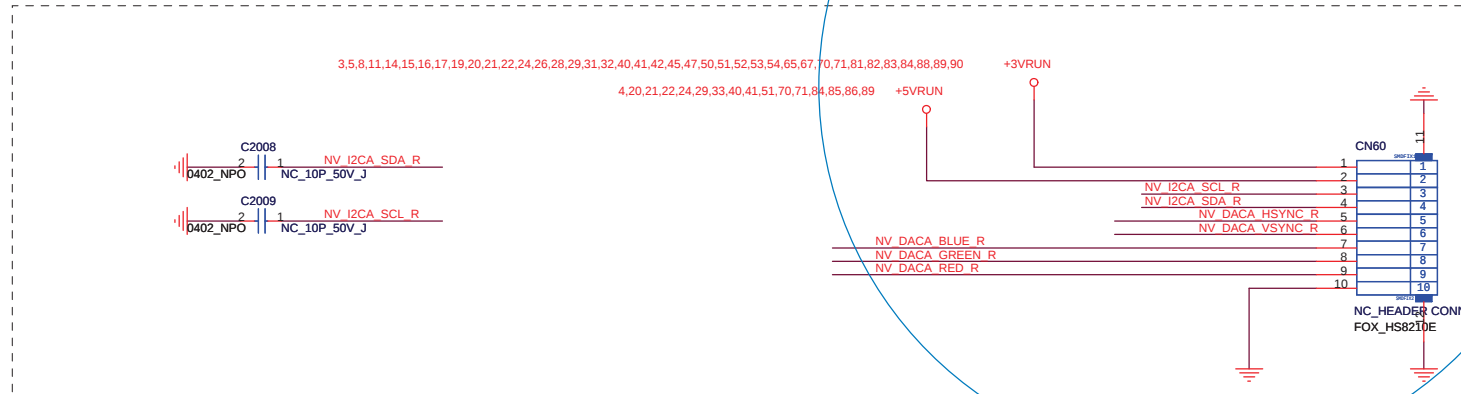
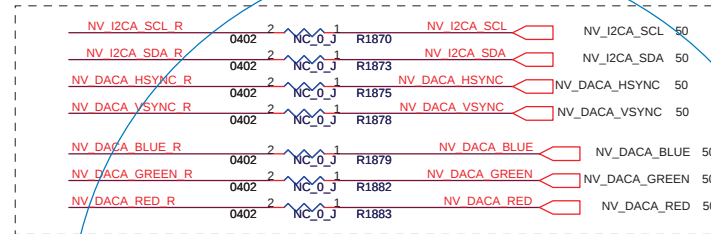
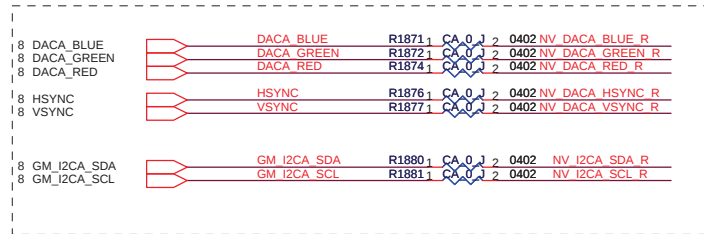
For tiramisu



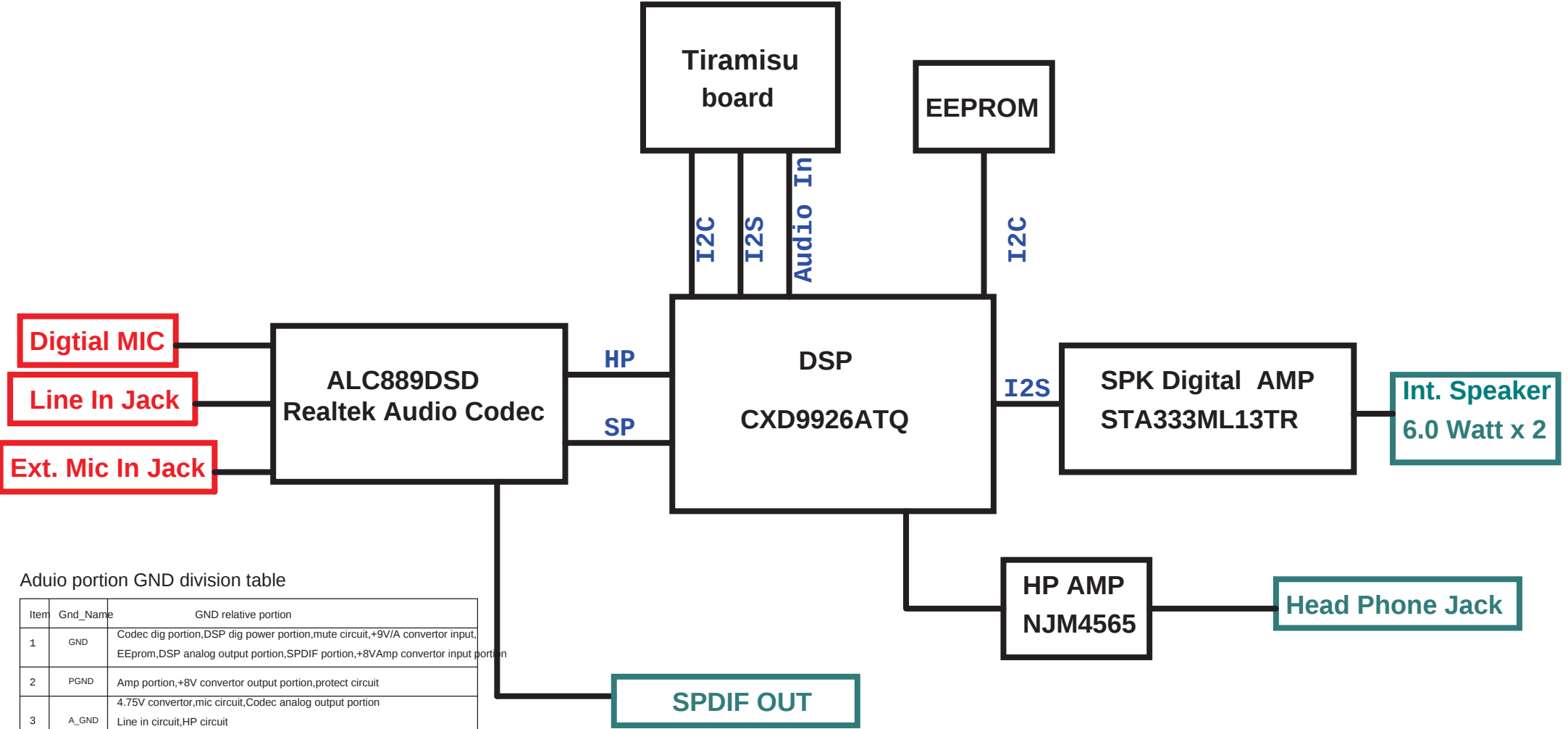
For tiramisu



FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Title	VGA (LVDS OUTPUT)		
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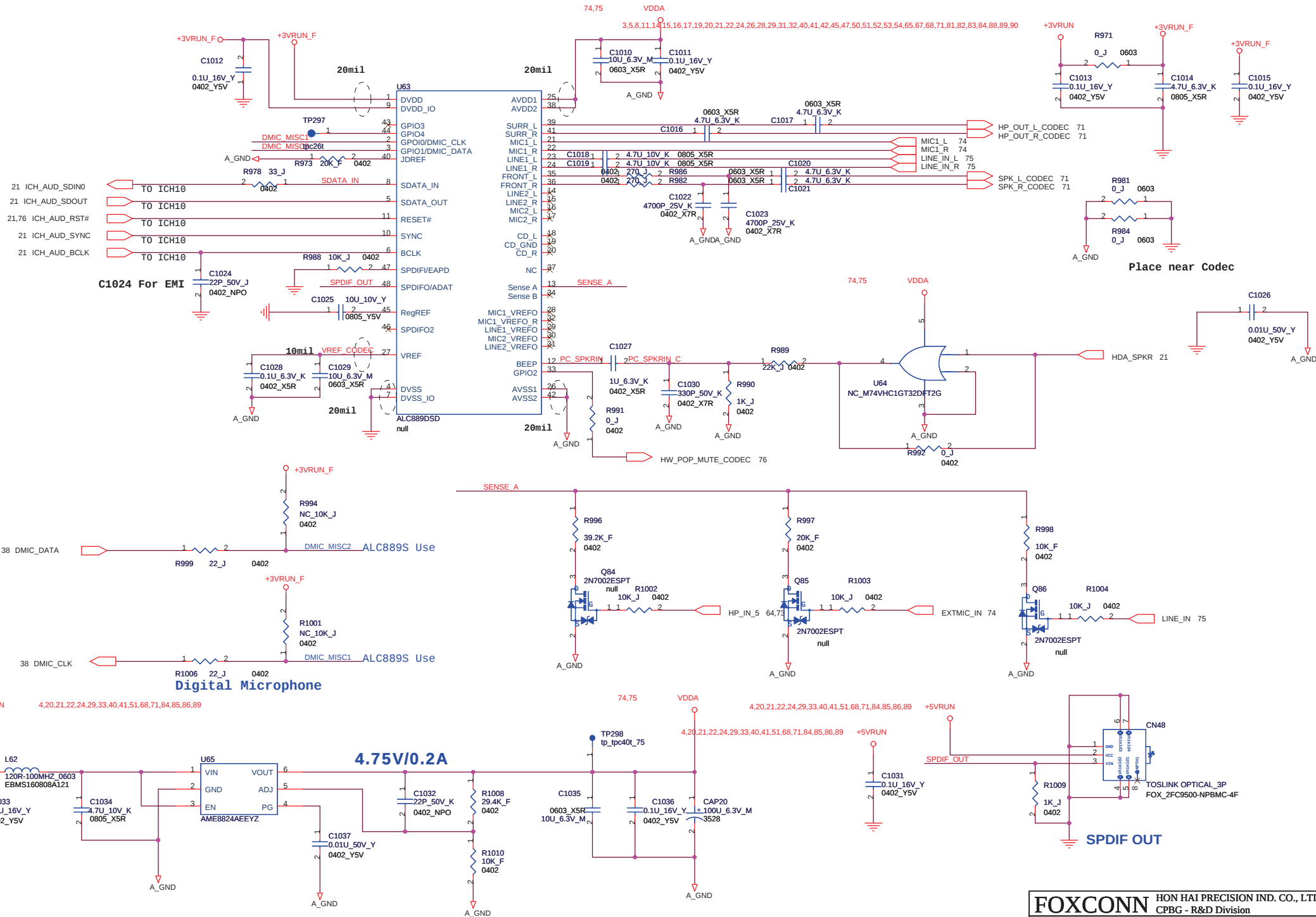


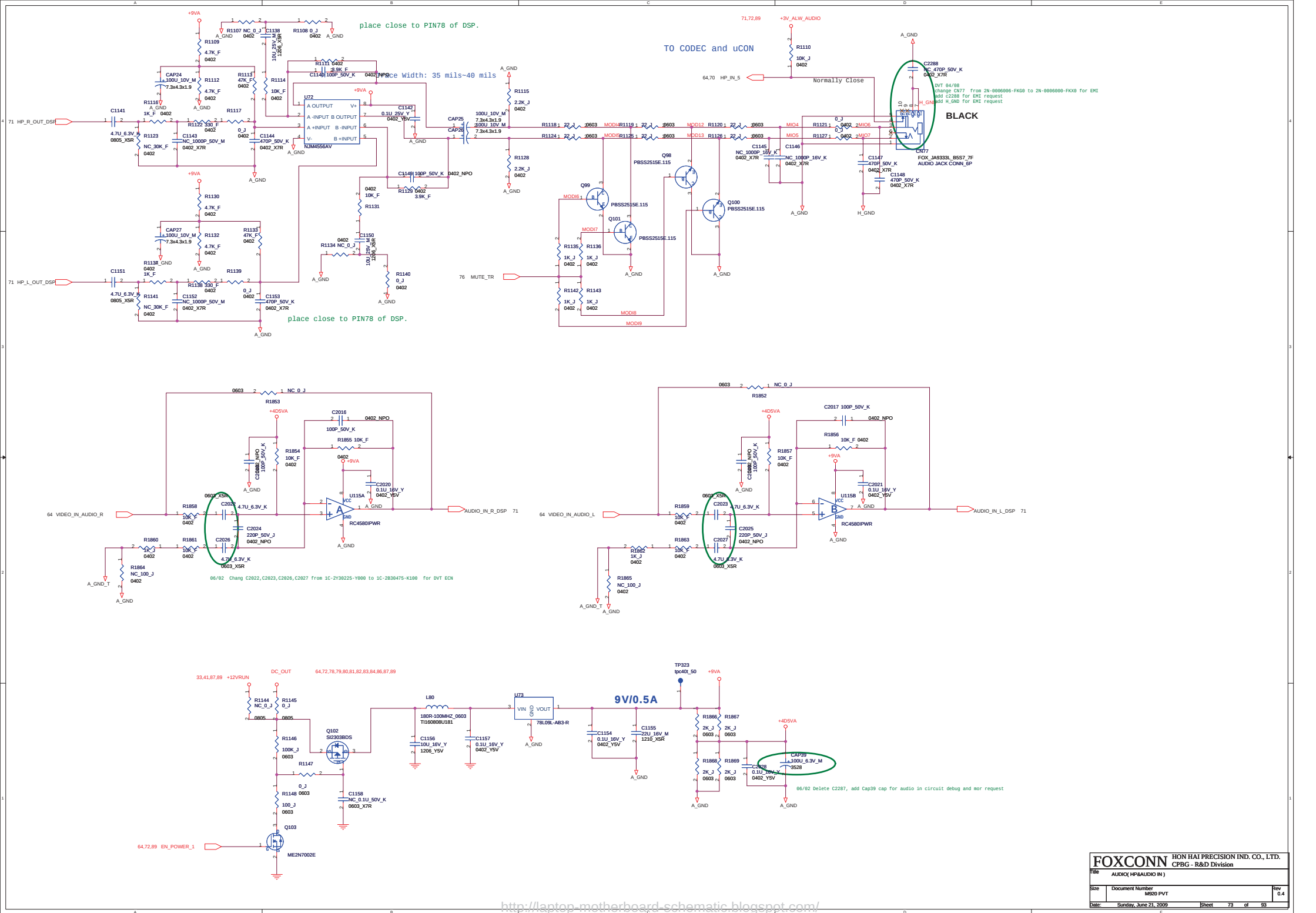
M920 Audio Board Block Diagram

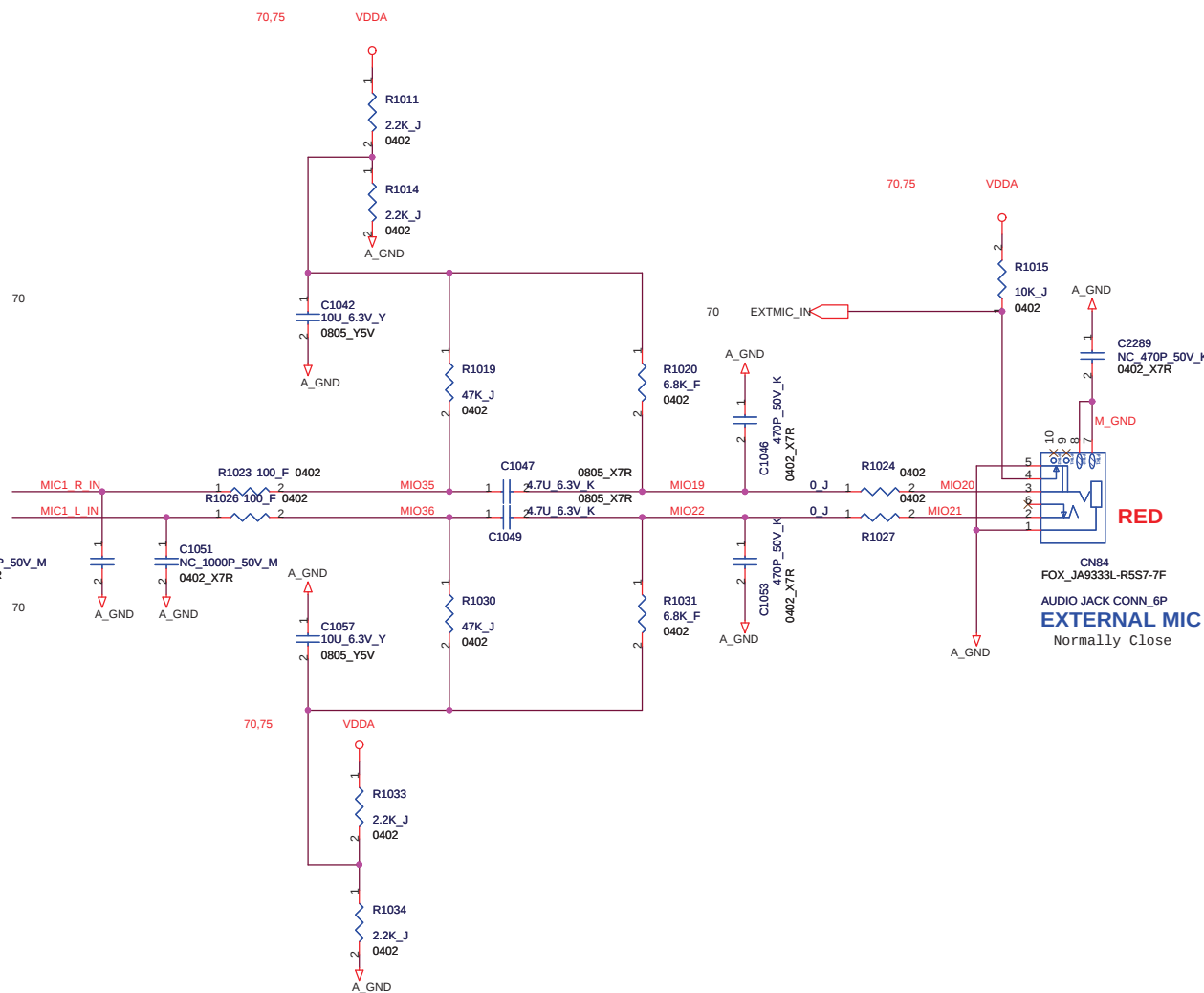
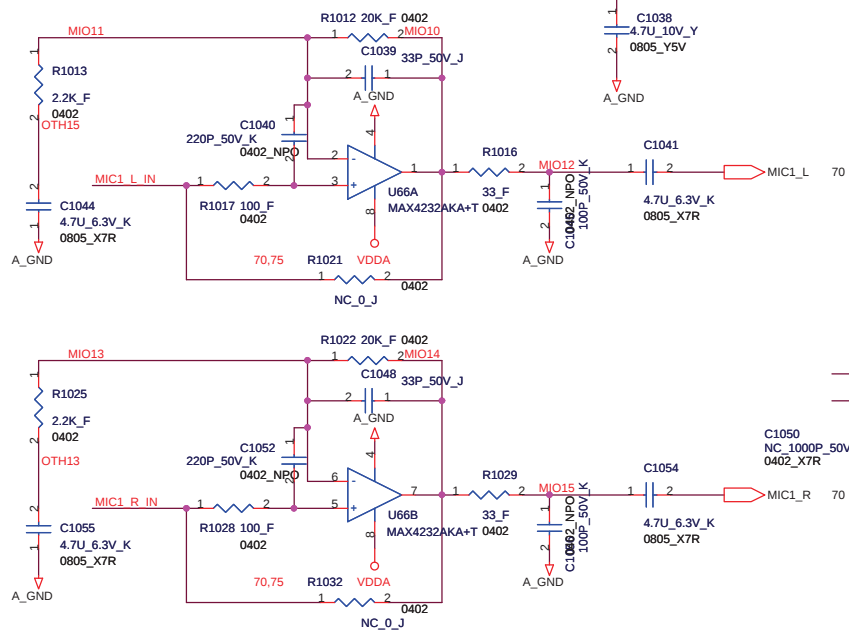


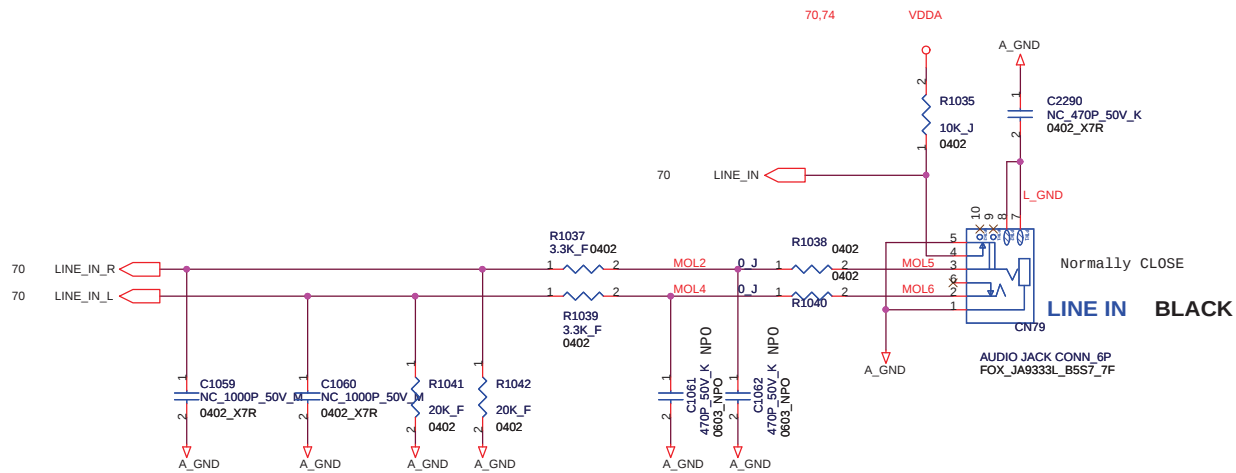
Aduio portion GND division table

Item	Gnd_Name	GND relative portion
1	GND	Codec dig portion,DSP dig power portion,mute circuit,+9V/A convertor input,EEprom,DSP analog output portion,SPDIF portion,+8VAmp convertor input portion
2	PGND	Amp portion,+8V convertor output portion,protect circuit
3	A_GND	4.75V convertor,mic circuit,Codec analog output portion Line in circuit,HP circuit
4	O_GND	DSP osc portion
5	W_GND	DSP PWM power portion

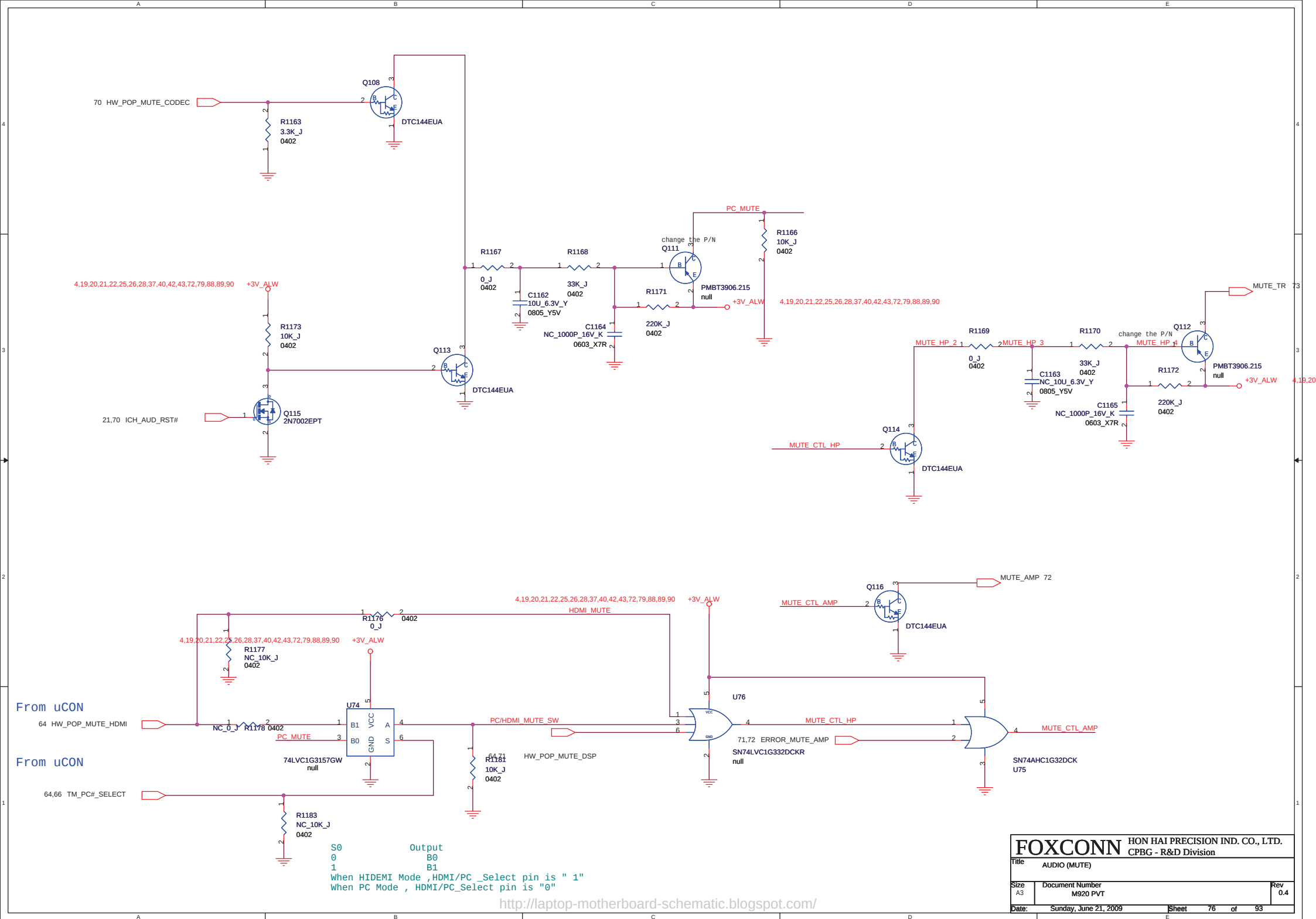


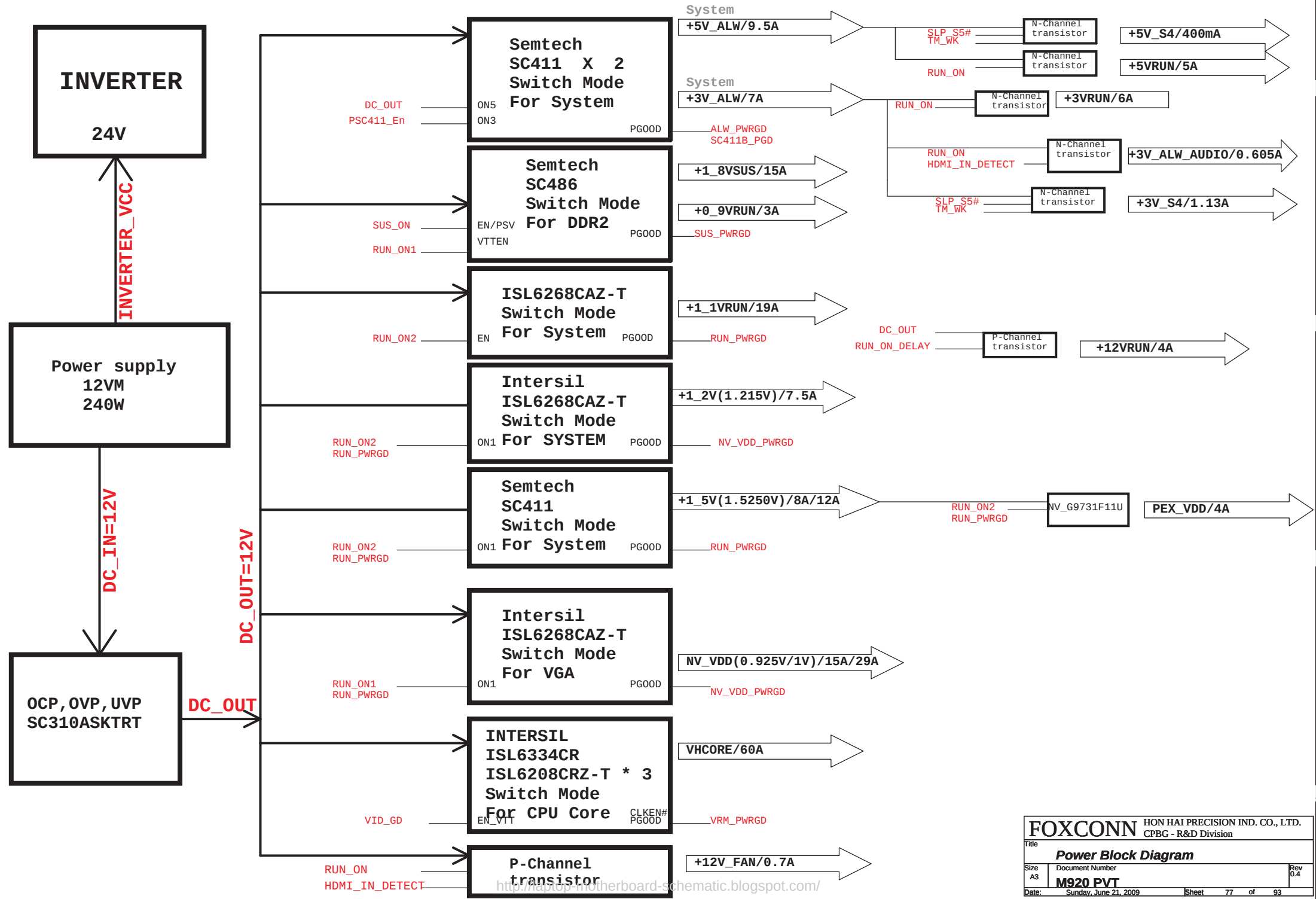


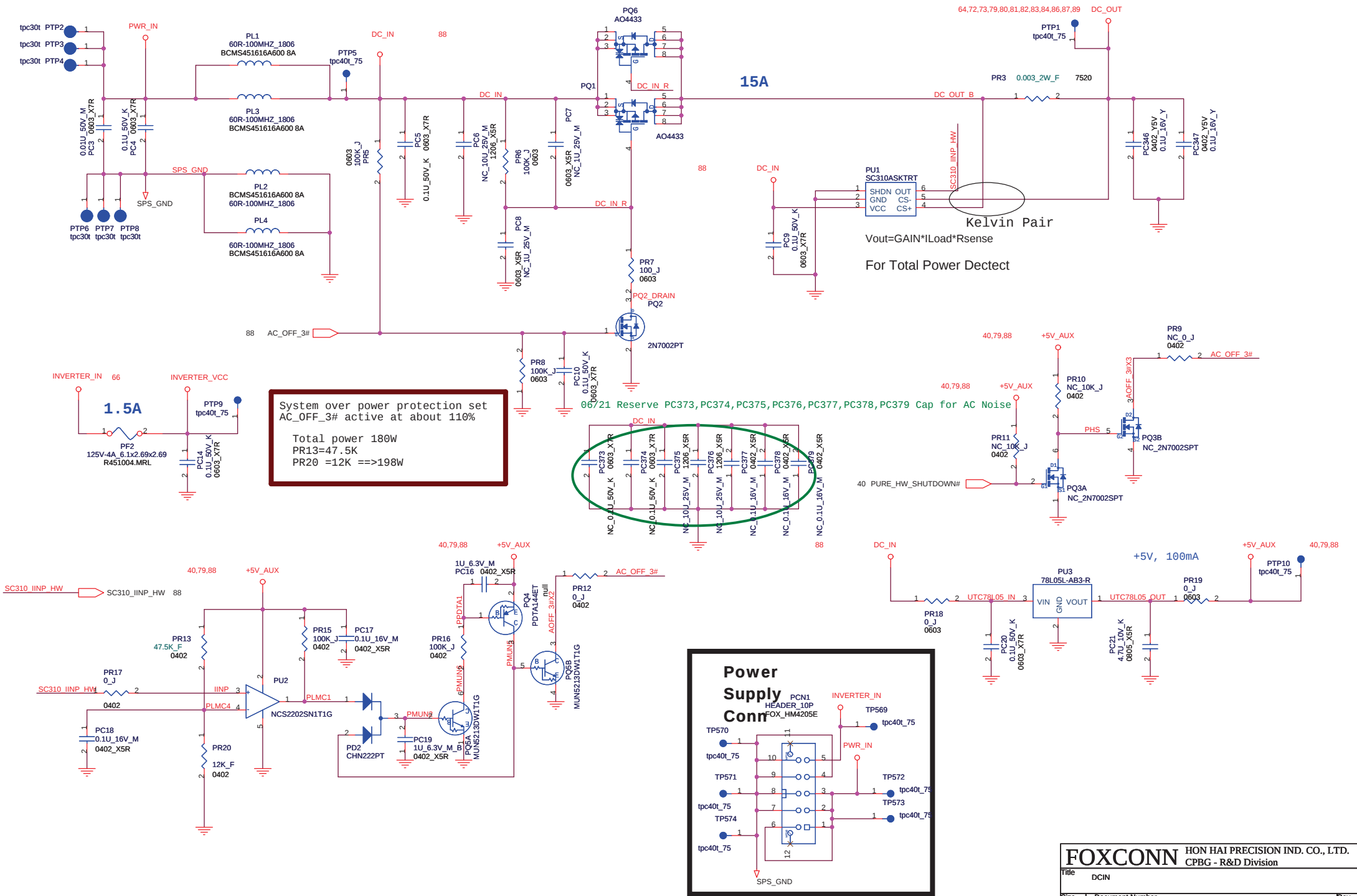




FOXCONN		HON HAI PRECISION IND. CO., LTD.
Title		AUDIO (LINE IN)
Size		Document Number
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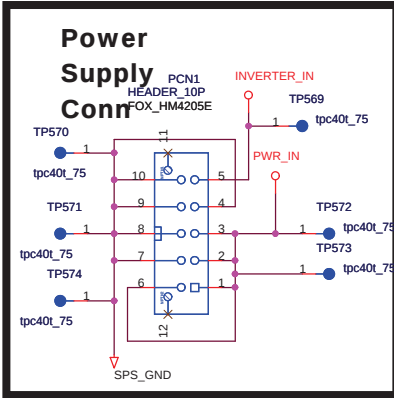




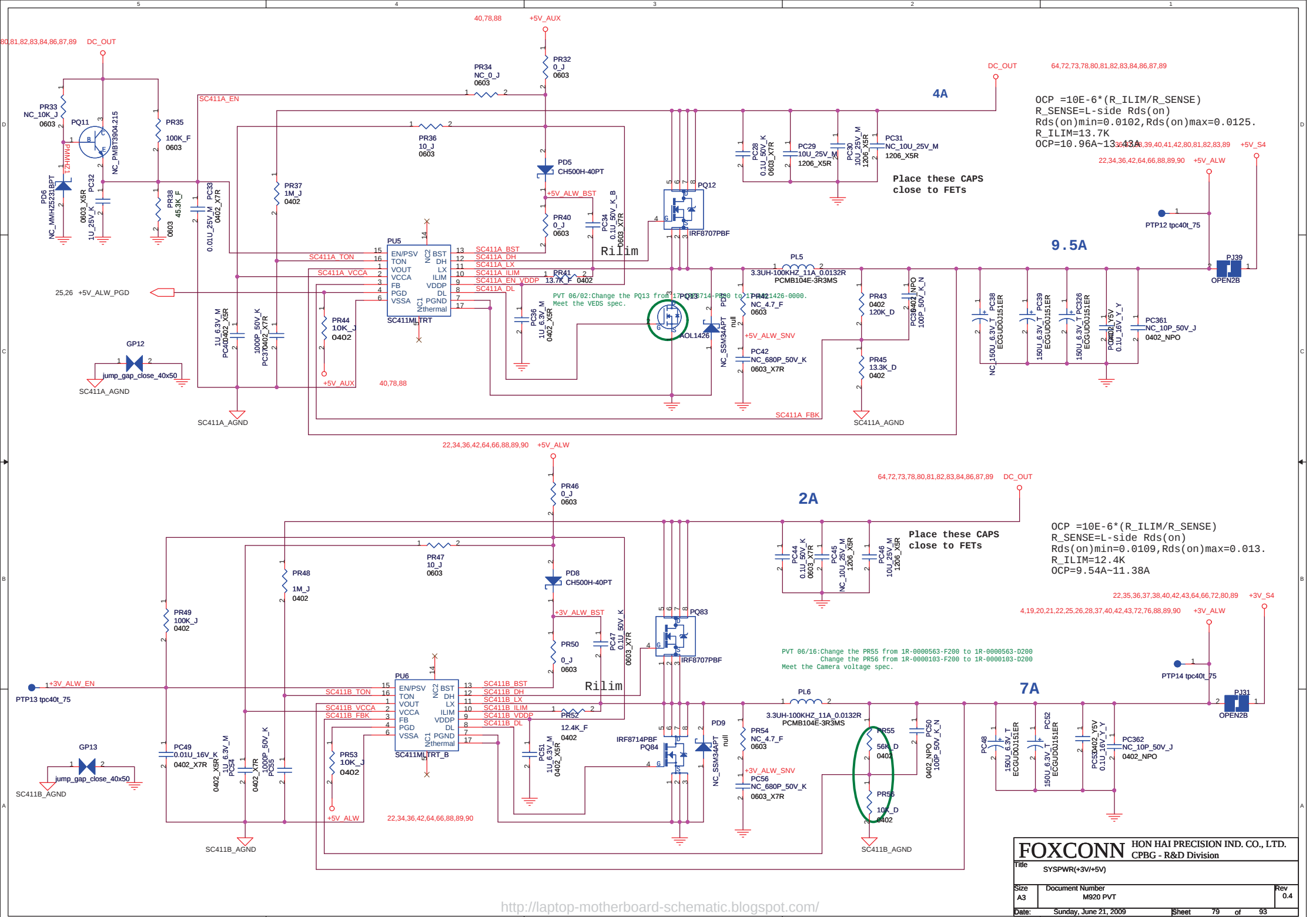


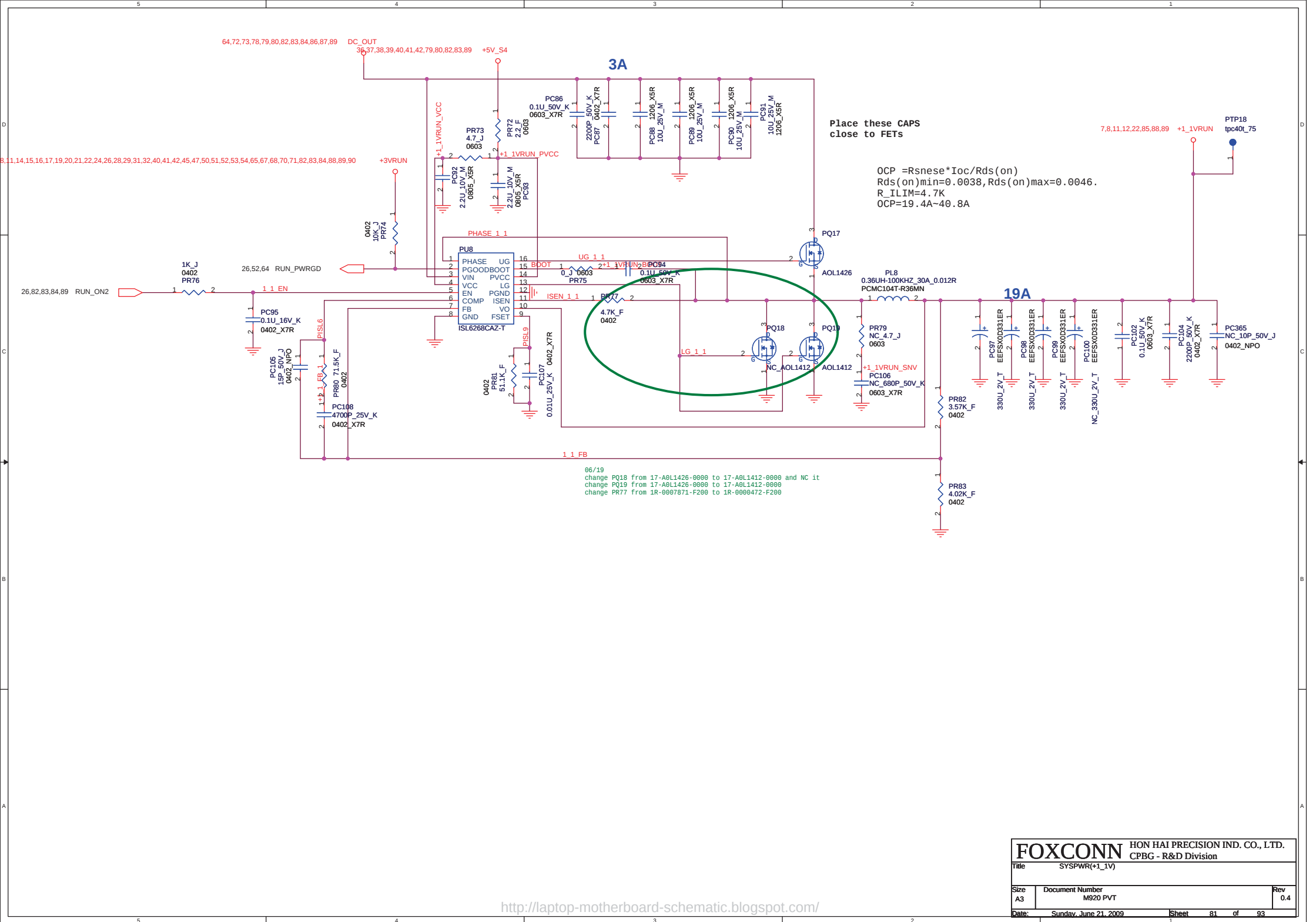
System over power protection set
AC_OFF_3# active at about 110%

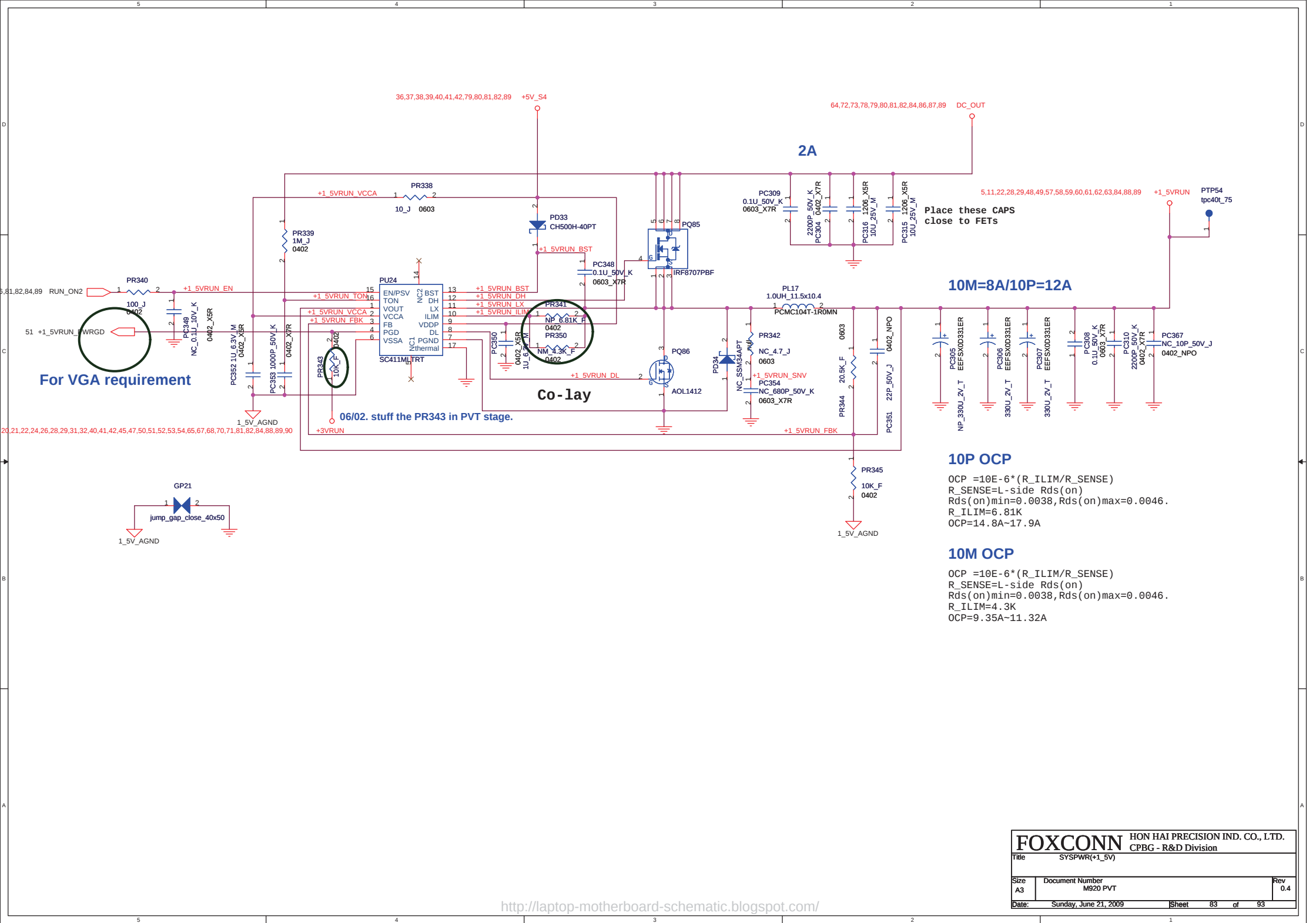
Total power 180W
PR13=47.5K
PR20 =12K ==>198W

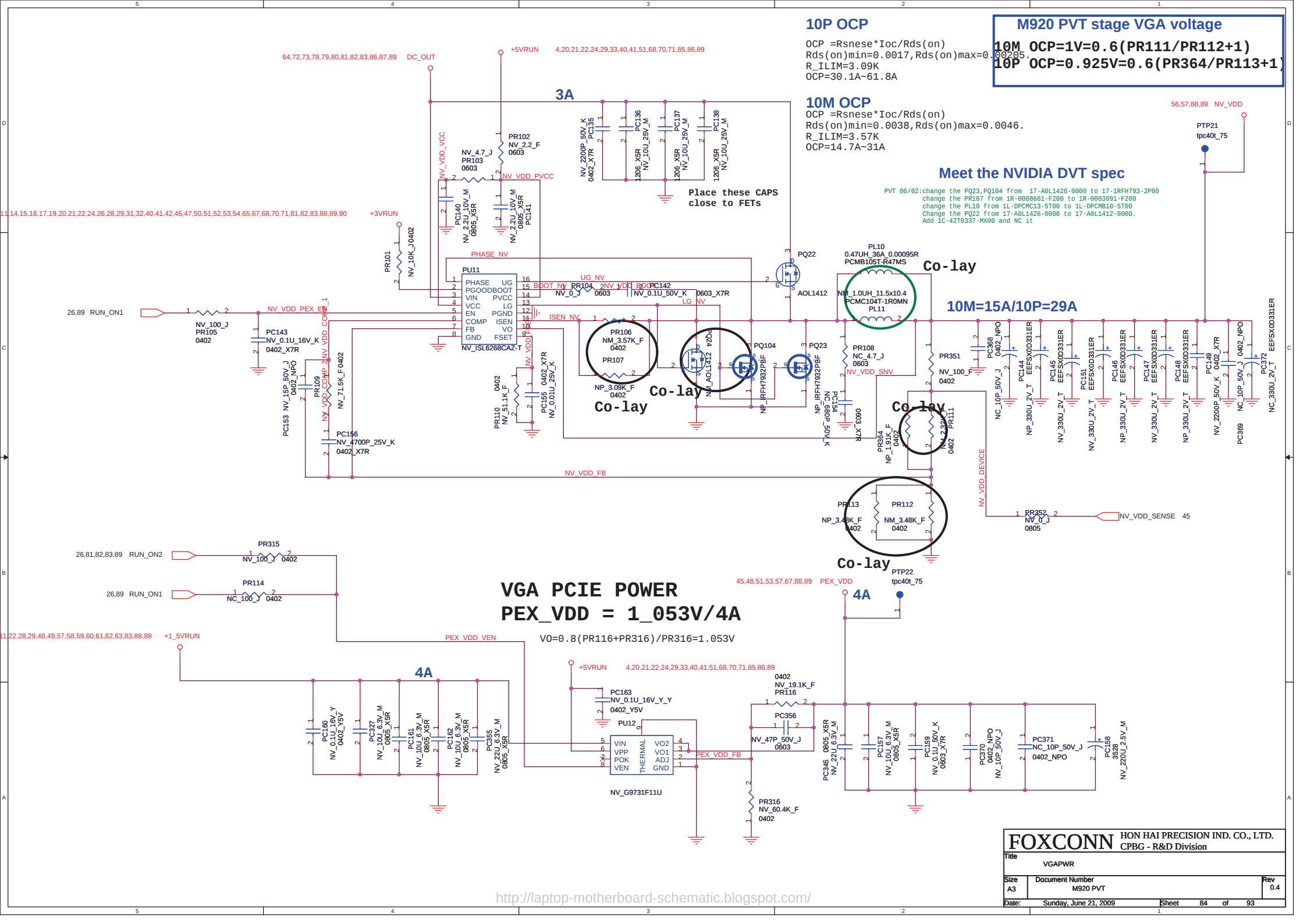


FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Title	DCIN		
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10P OCP

$OCP = R_{snes} \cdot I_{oc} / R_{ds(on)}$
 $R_{ds(on)min} = 0.0017, R_{ds(on)max} = 0.00205$
 $R_{ILIM} = 3.09K$
 $OCP = 30.1A - 61.8A$

10M OCP

$OCP = R_{snes} \cdot I_{oc} / R_{ds(on)}$
 $R_{ds(on)min} = 0.0038, R_{ds(on)max} = 0.0046$
 $R_{ILIM} = 3.57K$
 $OCP = 14.7A - 31A$

M920 PVT stage VGA voltage

10M $OCP = 1V = 0.6 (PR111 / PR112 + 1)$
10P $OCP = 0.925V = 0.6 (PR364 / PR113 + 1)$

Meet the NVIDIA DVT spec

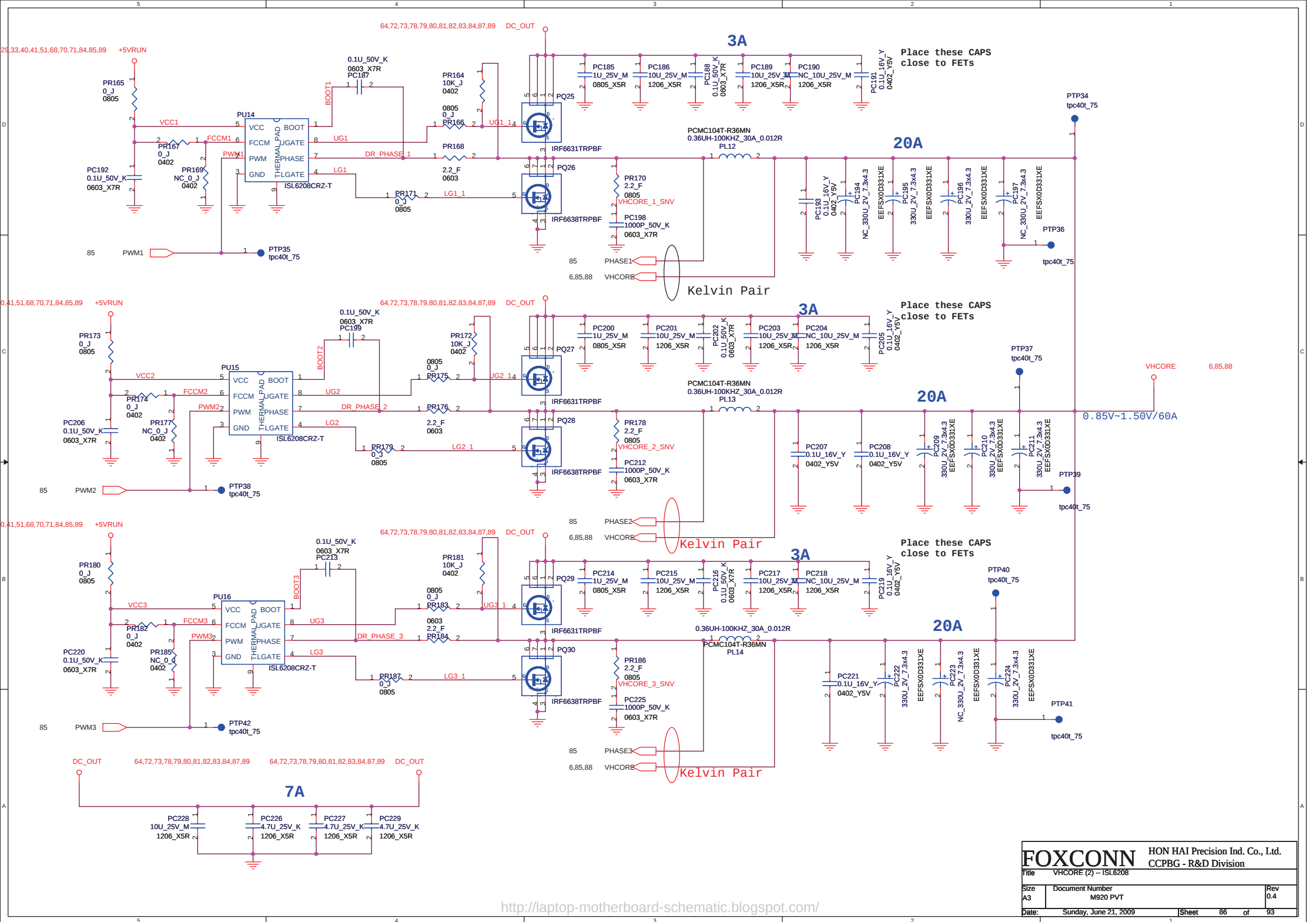
PVT 06/02: change the PQ23, PQ104 from 17-A0L1426-0000 to 17-1RFH793-2P00
change the PR107 from 1R-0008661-F200 to 1R-0003091-F200
change the PL10 from 1L-DPCM13-5T00 to 1L-DPCM10-5T00
Change the PQ22 from 17-A0L1426-0000 to 17-A0L1412-0000.
Add 1C-42T8337-MX00 and NC 1T

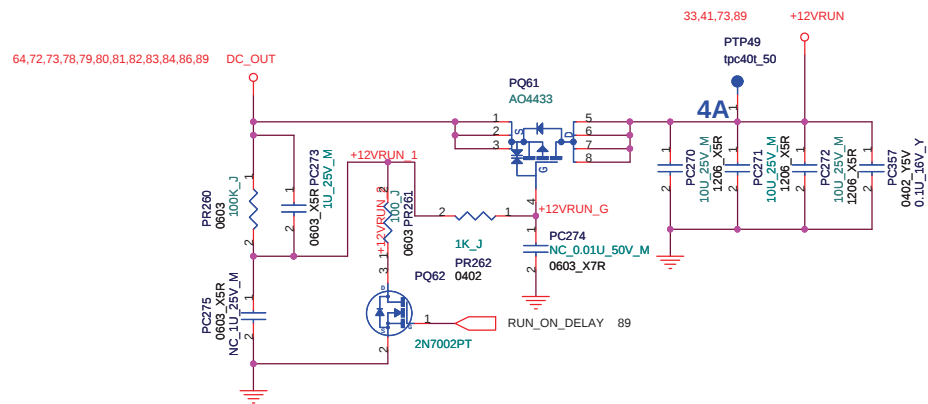
Co-layer
10M=15A/10P=29A

VGA PCIE POWER
PEX_VDD = 1_053V/4A

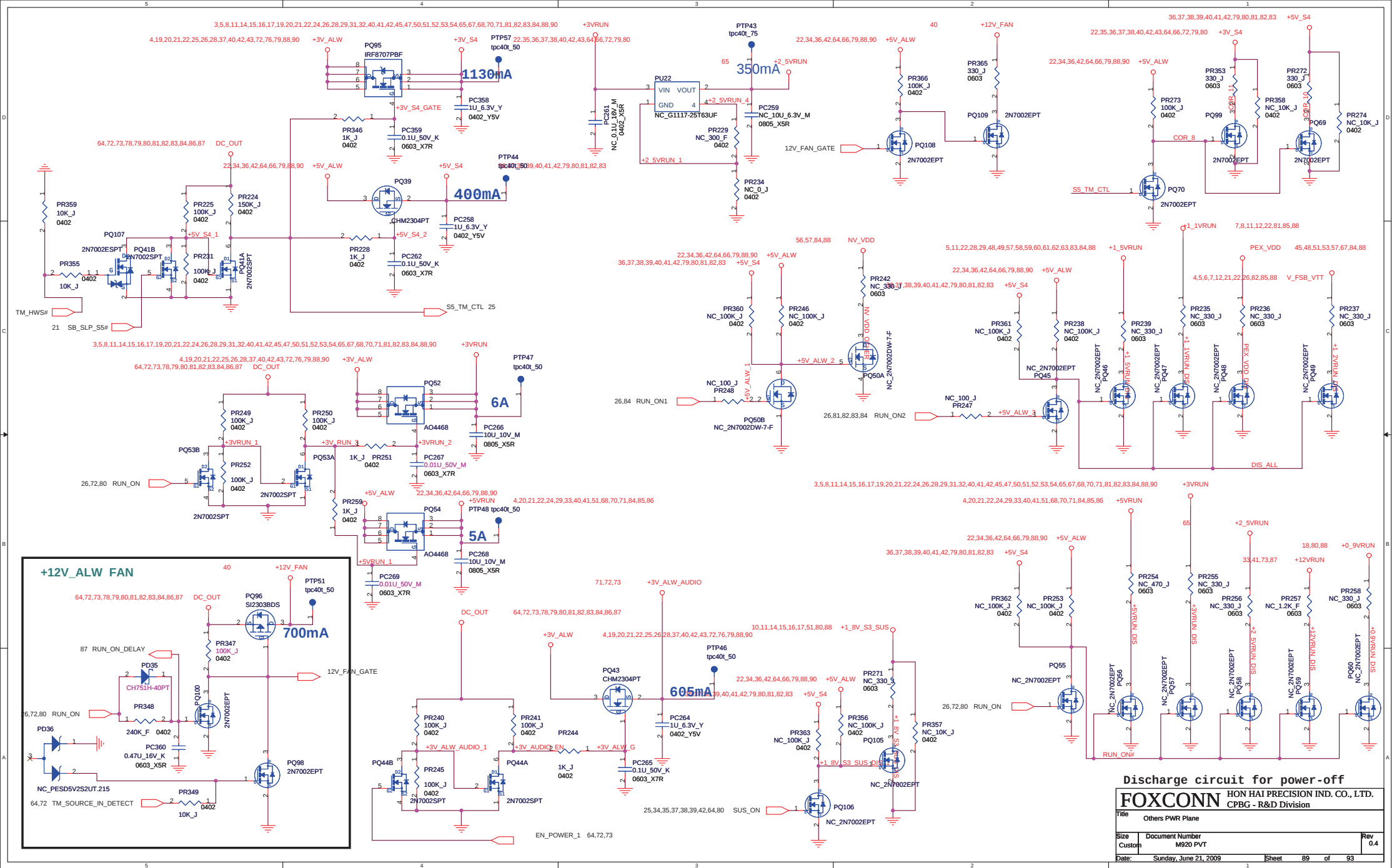
$V0 = 0.8 (PR116 + PR316) / PR316 = 1.053V$

FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title	VGAPWR	
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		CPBG - R&D Division	
Title			
HDD PWR(+12V)			
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Blank Please

M920 Change History
DVT stage

04/08
EE Portion:
Page 3, Change C1832 from 27pf to 30pf according to crystall match test
Page 19, Stuff external SPI BIOS MB_FLASH_EN circuit for MOR request, this circuit will delete from PVT stage.
Page 25, Change RSMRST# timing circuit the same as EVT1 circuit for MOR suggest.
Page 29 Delete Debug component R492,R1994,C356,C357,C358,C359,C360,C361,C1342,
Page 26, Change VRMPWVRGD delay circuit ,change net ' ICH_VRMPWRGD' to ' VRM_PWRGD_U' for EVT2 schematic mistake
Audio Portion:
Page 72 Change cap21,cap22 from 1000u to 470u, Add CAP37,CAP38 470u at Power +8vAMP , Del NC_R1057,NC_R1058
and connected net
Page 73 and Page 75 change CN77 and CN79 from 2N-0006006-FKG0 to 2N-0006000-FKX0
Page 74 change CN84 from 2N-0006002-FRG0 to 2N-0006000-FRX0
Page 73&74&75 Add H_GND,M_GND and L_GND for EMI request
Page 73&74&75 Add C2288,C2289,C2290 470p CAP between H_GND and A_GND,M_GND and A_GND,L_GND and A_GND
for EMI request
Power Portion:
Page 81 change the PQ17 from 17-A044680-0000 to 17-A0L1426-0000. for costdown failure item.
Page 84 change the PQ22 from 17-A044680-0000 to 17-A0L1426-0000. for costdown failure item.
Page 79 change the PR41 from 1R-0001432-F200 to 1R-0001372-F200. Meet the VEDS spec.

04/13
EE Portion:
Page 39 Delete R1396
Page 34 ME request change USB connector CN26,CN27 color from gary to black,change PN
from 2N-0004009-FEG0 to 2N-0004008-FEG0
Page 90 For EMI Request,Mount SPR2 and SPR3
Page 29 For EMI Request add GP22,GP23 between TV_GND and GND

Audio Portion:
Page 76 Delete NC_R1175 for no use
Page 72 Add 1 pcs 0.1U cap and mount C1088,C1079 cap for EMI request.

04/15
EE Portion:
Page 14 Change R209,R208 from 1R-0000102-F200 to 1R-0000102-D200 for improve the VREF margin
Page 16 Change R217,R218 from 1R-0000102-F200 to 1R-0000102-D200 for improve the VREF margin
Page 42 NC R2047,LED3 For MOR request

04/16
Power Portion:
Page 81 Change the PR77 from 1R-0000822-F200 to 1R-0007871-F200
Page 84 Change the PR112 from 1R-0004641-F200 to 1R-0003481-F200
Change the PR113 from 1R-0004641-F200 to 1R-0003481-F200
Change the PR364 from 1R-0002321-F200 to 1R-0001911-F200
Change the PR106 from 1R-0003091-F200 to 1R-0003571-F200

Page 85 For Vcore intel spec change as below:
Change the PR144 from 1R-0008250-F300 to 1R-0000751-F300
Change the PR140,PR143,PR148 from 1R-0000472-F200 to 1R-0003241-F201
Change the PR142 from 1R-0000203-F200 to 1R-0000123-F200
Change the PC175 from 1C-2B20681-K000 to 1C-2N20102-J600
Change the PR147 from 1R-0000201-F200 to 1R-0000510-F300

Page 86 Change the PC194 from 1C-42T0337-MX02 to NC
Change the PC197 from 1C-42T0337-MX02 to NC
Change the PC223 from 1C-42T0337-MX02 to NC
Change the PR182 from NC to 1R-0000000-J200
Change the PR185 from 1R-0000000-J200 to NC
Change the PR174 from NC to 1R-0000000-J200
Change the PR177 from 1R-0000000-J200 to NC
Change the PR167 from NC to 1R-0000000-J200
Change the PR169 from 1R-0000000-J200 to NC

04/17
EE Portion:
Page 20 Stuff for MOR request ,it will be NC at PVT stage.
Page 35 Delete CN89,R2061,R2062 ,2042,2043for desgin change.This connector and resister is no use .
Page 36 Delete R577,C2128,IR_BLAISTER for MOR reconment.
Page 29 Delete R2092 ,R2093 and net VIDEO_COMP1 because AV IN board be canceled
Page 30 Delete all AV_IN function for MOR request
Page 42 Add TP594 For L6 TEST

Audio Portion:
Page 72 change C1100,C1101,C2291 from 0.1U cap to 0.01u cap for MOR request.
change C1088,C1079 ,C1089,C1099 to 470p cap for mor request, and mount C1089,C1099.

04/18
EE Portion:
Page 42 Stuff R2086 and R2105 ,NC R2104 and R2106 for MOR request

04/19
Power Portion:
Page 83 change the PQ86 from 17-1RF8714-PB00 to 17-A0L1412-0000
change the PR341 from 1R-0000183-F200 to 1R-0006811-F200
change the pr350 from 1R-0001372-F200 to 1R-0000432-F200

Page 84.change the pc144 from NC to stuff
change the pc146 from NC to stuff

Page 89 add the 12V_fan discharge circuit.

04/20
EE Portion:
Page 29 Change AV_IN_GND TO TV_GND due to AV_IN/IR Function have been canceled.
Page 40 NC CN37,C523,C497 for thermal suggest

PVT stage

06/02
Power Portion:
Page 79 Change the PQ13 from 17-1RF8714-PB00 to 17-A0L1426-0000. Meet the VEDS spec.
Page 83. Stuff the PR343 (1R-0000103-F200)in PVT stage.for VGA requirement
Page 84 Change the PQ23,PQ104 from 17-A0L1426-0000 to 17-1RFH793-2P00
Change the PR107 from 1R-0008661-F200 to 1R-0003091-F200
Change the PL10 from 1L-DPCMC13-5T00 to 1L-DPCMB10-5T00
Change the PQ22 from 17-A0L1426-0000 to 17-A0L1412-0000.
Add 1C-42T0337-MX00 and NC it .for NVIDIA requirement in PVT stage.

EE Portion:
Page 32 Change CN50 From 1N-1014000-0000 to 1N-1014002-0000 For vendor change material.
Page 36 Add R2111 1K to pull up for Tiramisu suggestion
Page 29 Delete CN69,R1847,R1957,R1958,R1959,R1960,R1961.

Audio Portion:
Page 73 Delete C2287, add Cap39 The cap for audio in circuit debug and mor request
Chang C2022,C2023,C2026,C2027 from 1C-2Y30225-Y000 to 1C-2B30475-K100 for DVT ECN

06/10
EE Portion: Page 20 Add R2118,R2119 and Q185 this portion circuit for system leakgea issue
Page 36 NC R1891 and R700,the TM_RX_CN not use
Page 20 NC CN5,we will use GPIO24 to contorl FLASH_STRAP_SB
Page 19 NC R264,R265,Q9 Confirmed with our SW members, we don't use this function, so we can delete it.
Page 42 NC R680,R679 and SW3 for PVT/MP do not use CRT
Page 29 Change L17 from 1L-BT11608-0800 to 1L-BACMS16-080A for power consumption
Page 27 Change CN9 from 2N-000800F-FKN0 to 2N-0008001-FKN0 for package changed

06/15
EE Portion: Page 19 Add R2120 to boot the pc from external spi card or internal spi rom
Page 27 Change C2161 From 1C-2B20104-K000 to 1C-2N20050-D000 for EMI Request

06/17
Audio Portion: Page 71 Change R1271,R1272 From 1R-0000472-J200 to 1R-0000222-J200 for tiramisu I'C bus test
Power Portion:
1.Page 79. Change the PR55 from 1R-0000563-F200 to 1R-0000563-D200
Change the PR56 from 1R-0000103-F200 to 1R-0000103-D200 Meet the Camera voltage spec.
2.Page 81 and Page 84,change the power budget value.

EE Portion: Page 40 Add +3VALW as another power source for SMSC VCC
Page 41 Add C2295 on Fan3 Tach for EMI request.
Page 36 NC R2111 pull up resistor,because IR receiver have internal pull up.
Page 90 Change H15,H34 and H7 PAD Type for ME request
Page 90 ADD X1,X2 and Delete SPR2 and SPR3 for EMI and ME Request

06/19
Power Portion:
Page 81. change PQ18 from 17-A0L1426-0000 to 17-A0L1412-0000 and NC it
change PQ19 from 17-A0L1426-0000 to 17-A0L1412-0000
change PR77 from 1R-0007871-F200 to 1R-0000472-F200

EE Portion: Page 27 Change C315 and C316 from 1C-2N20150-J000 to 1C-2N20330-J000 for crystal test result
Page 31 Change R1340 and R1341 from 10K_J to 4.7K_J for Vendor suggestion

06/21

EE Portion:
Page 41 Use GPIO solution for QST Fan spin-up noise issue(Mount Q177,Q178,Q179,R2101,R2081,R2099,
R2102,R2082,R2100,R2103,R2080,R2098, NC R2070,R2078,R2071,R2079,R2070)
Page 41 Mount R2063 (GPIO 7 need to pull low)
Page 40 Mount R1800 (GPIO 19 need to pull low)
Page 20 NC R295,R276 (GPIO19 ,GPIO7 need to pull low)

Power Portion: Page 78 Reserve PC373,PC374,PC375,PC376,PC377,PC378,PC379

FOXCONN

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CPBG - R&D Division

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