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16	LVDS	0.1	12/04	51	OVP protection	0.1	12/04
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35	AUDIO(EXTMIC)	0.1	12/04				



Project Code & Schematics Subject: MS72 Main Board

PCB P/N: (FUBAI) 1P-006B100-60SA
(NAN YA) 1P-006B200-60SA
(HANSTAR) 1P-006B500-60SA

P. Leader		Check by	Design by
[Signature]		[Signature]	[Signature]
FOXCONN HON HAI Precision Ind. Co., Ltd CCPBG - R&D Division			
Title Index Page			
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13	DDR2(S0-DIMM_0) 1/3	0.1	12/04	48	DDR2 Power(+1.8V/+0.9V)	0.1	12/04
14	DDR2(S0-DIMM_1) 2/3	0.1	12/04	49	CPU Vcore ---MAX8771	0.1	12/04
15	DDR2(Termination) 3/3	0.1	12/04	50	Others power plan	0.1	12/04
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31	FAN	0.1	12/04				
32	OIDE	0.1	12/04				
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34	AUDIO(AMP & HP & SPK)	0.1	12/04				
35	AUDIO(EXTMIC)	0.1	12/04				



P. Leader	Check by	Design by

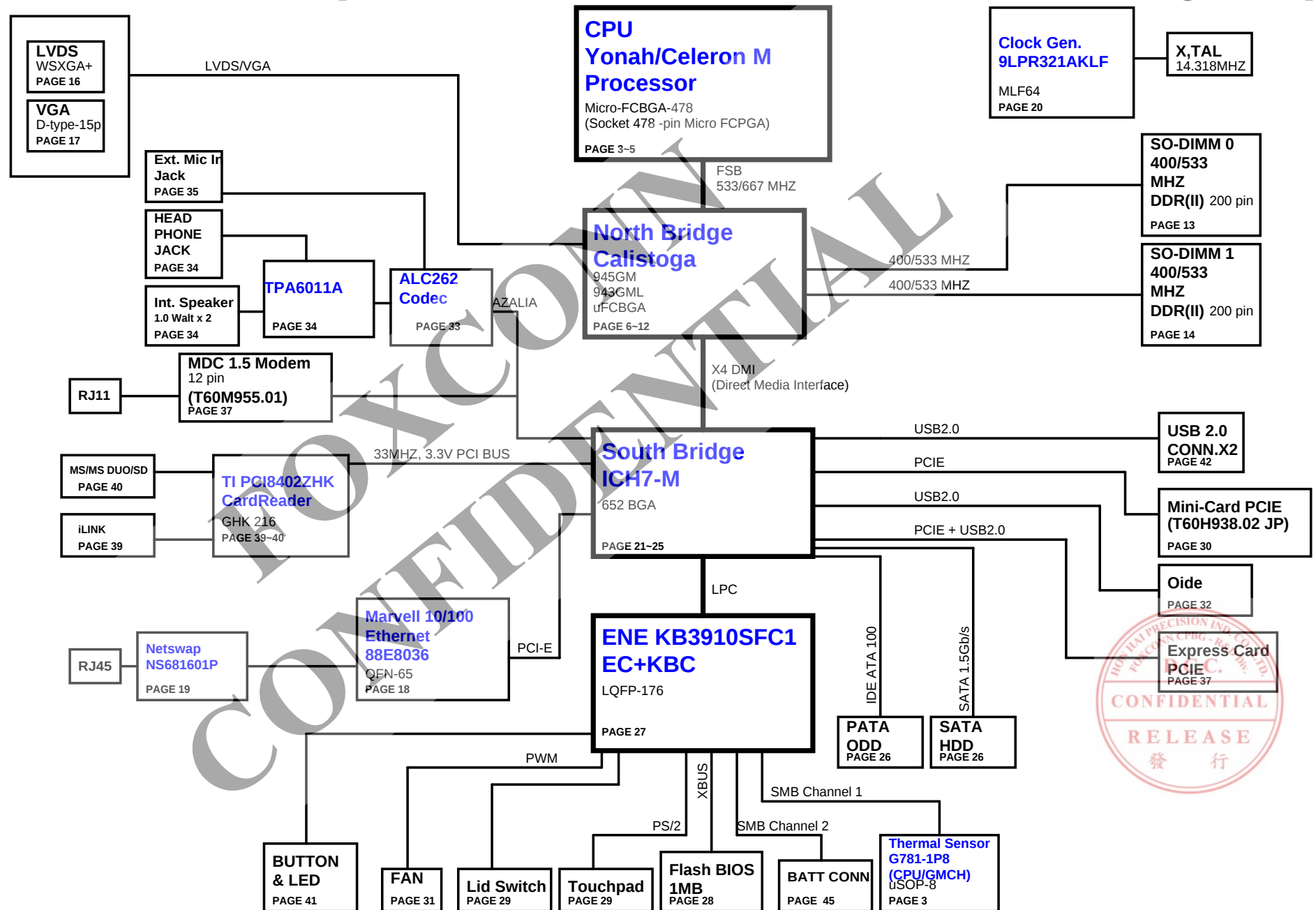
Project Code & Schematics Subject: MS72 Main Board

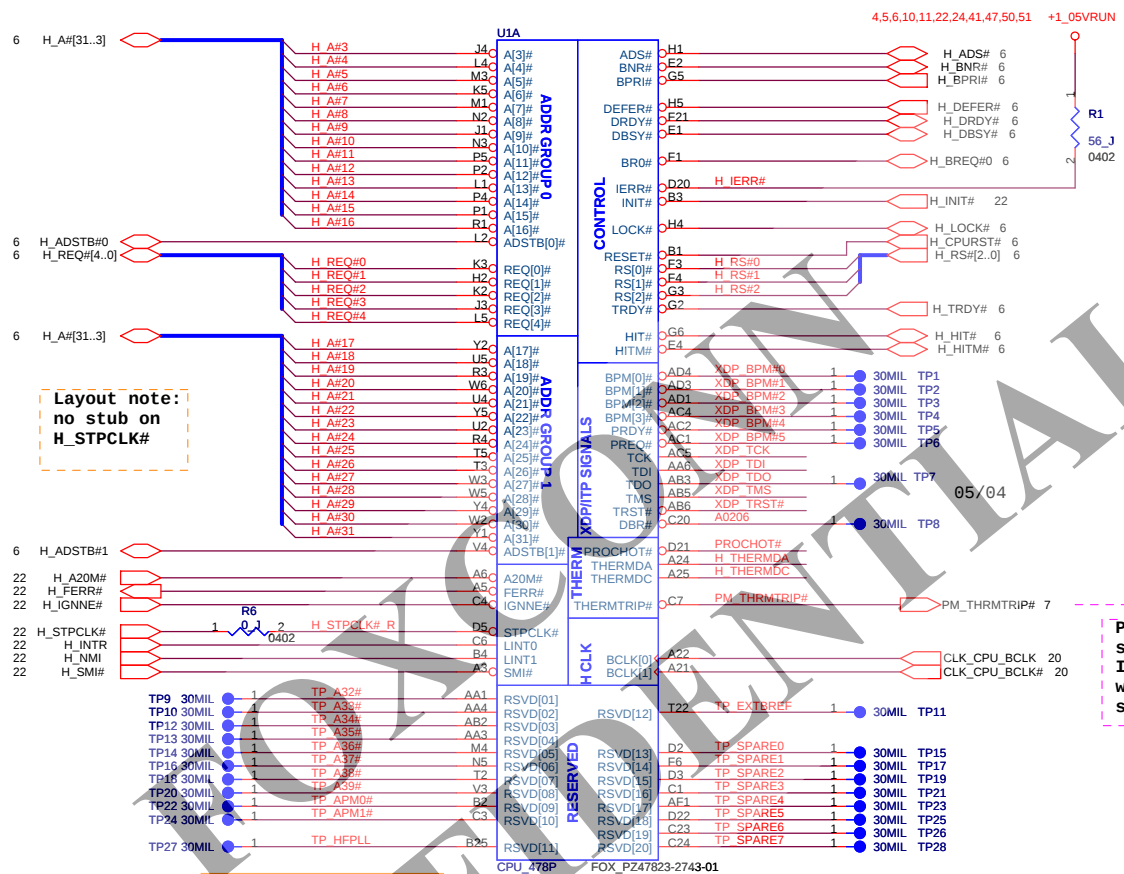
PCB P/N: (FUBAI) 1P-006B100-60SA
(NAN YA) 1P-006B200-60SA
(HANSTAR) 1P-006B500-60SA

<http://mycomp.ru> - Запчасти и комплектующие для ноутбука. Схемы, сервис мануалы, инструкции по разборке ноутбука.

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RAPTOR3/MS72(CALISTOGA GM/GML Block Diagram)

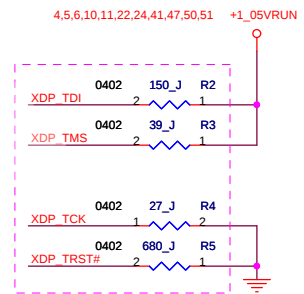




Layout note:
no stub on
H_STPCLK#

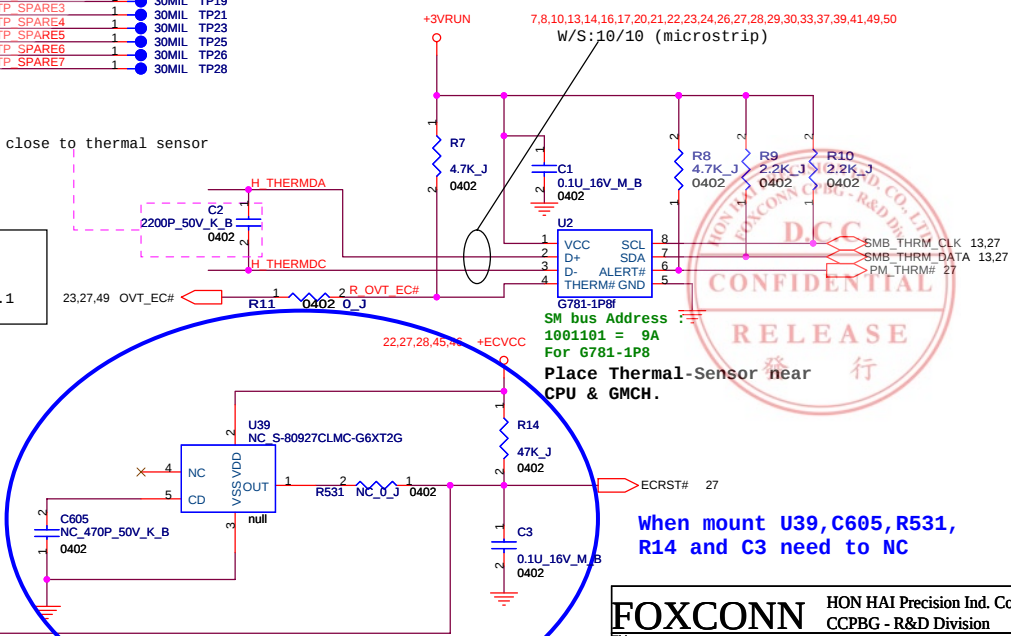
A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

ICH7M's GPIO12: VIL---- -0.5V ~ 0.8V
VIH---- 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL---- -0.1V ~ 0.3*VCCP
VIH---- 0.7*VCCP ~ VCCP+0.1



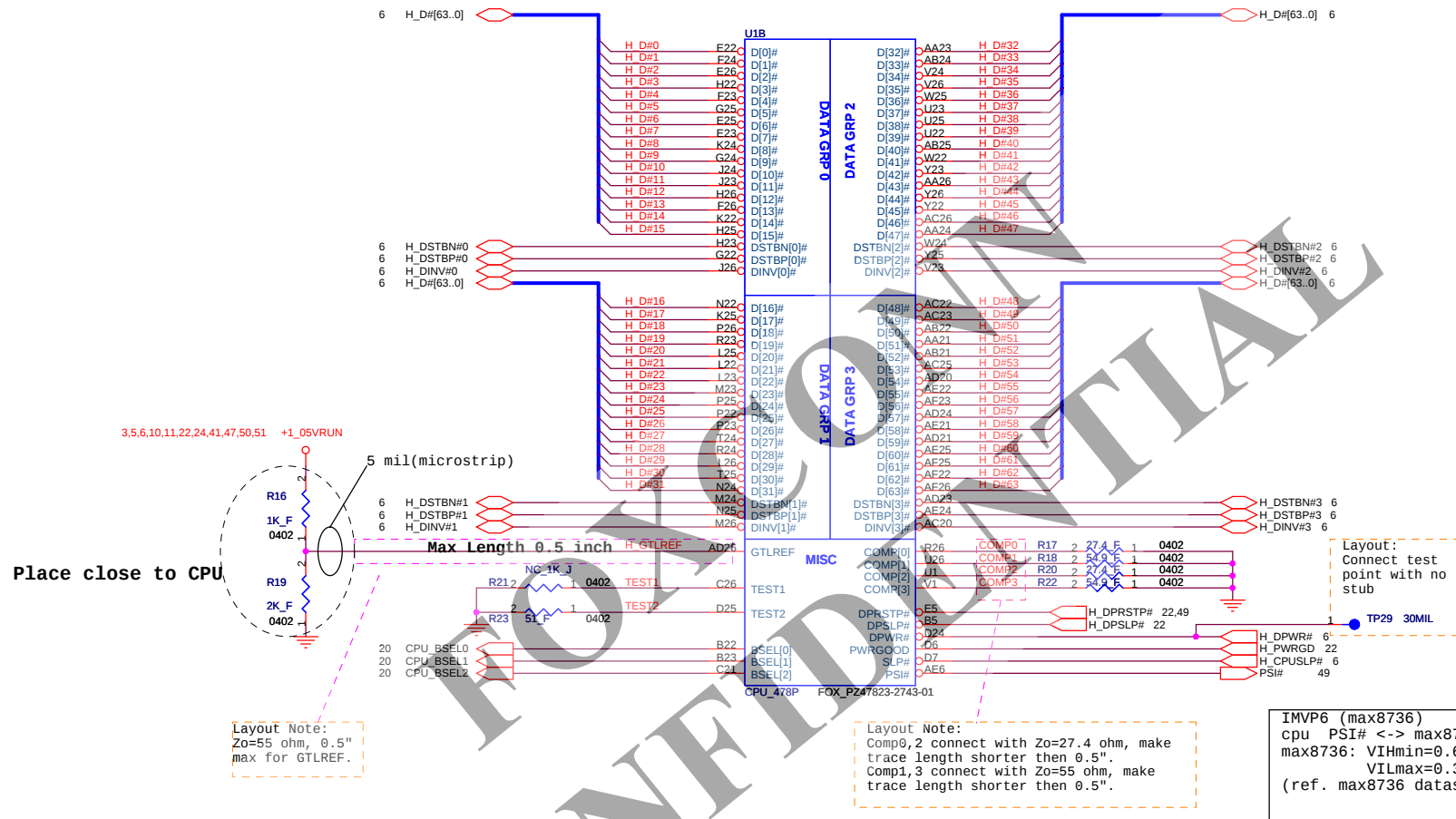
Debug port not used .
resistors close to CPU.

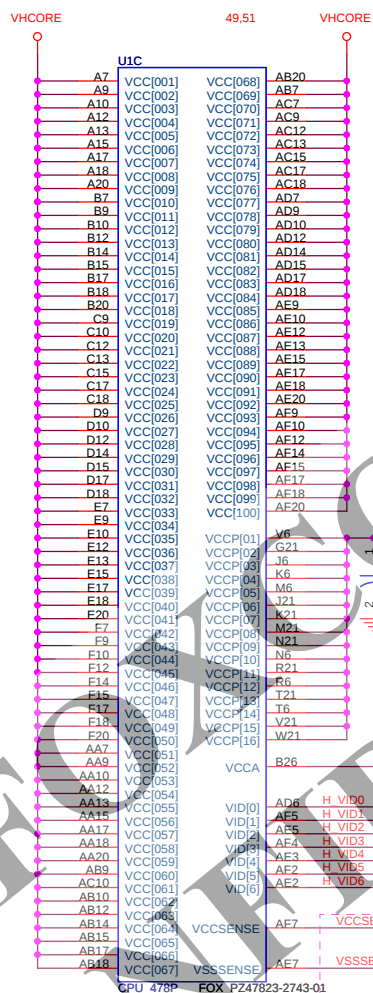
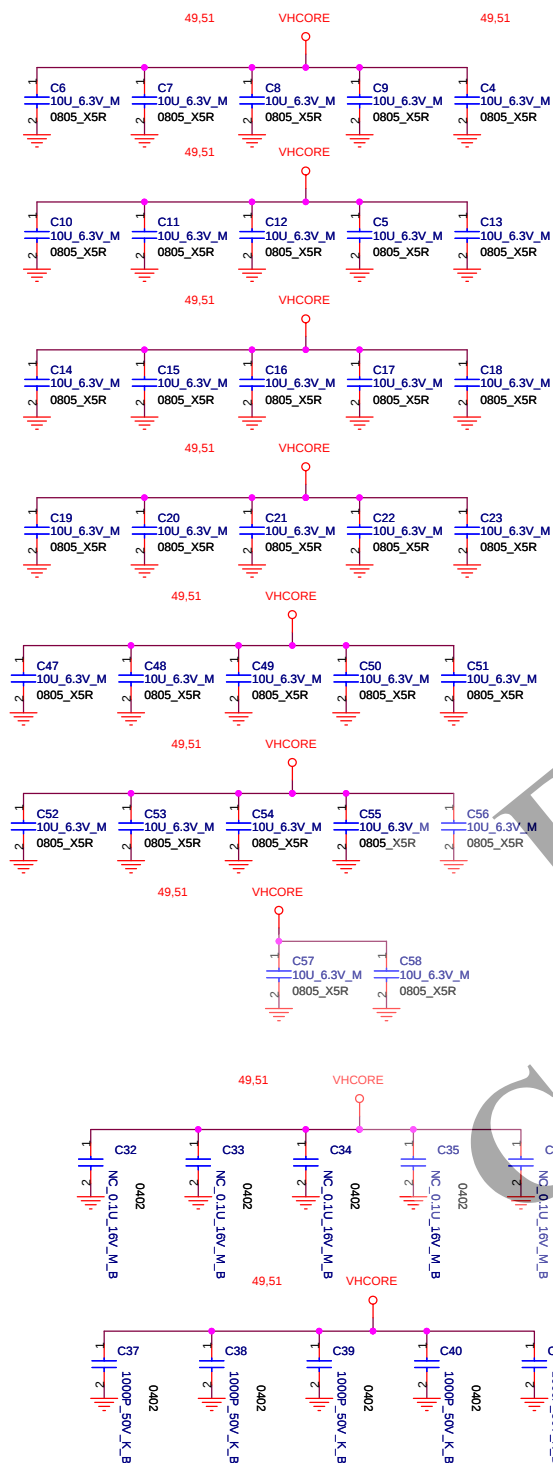
PM_THRMTRIP#
should connect to
ICH7-M and GMCH
without T-ing (No
stub)



When mount U39, C605, R531,
R14 and C3 need to NC

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
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CPU_VCCA---->120mA
CPU_VCCP----->2.5A
CPU_VCC----->36A

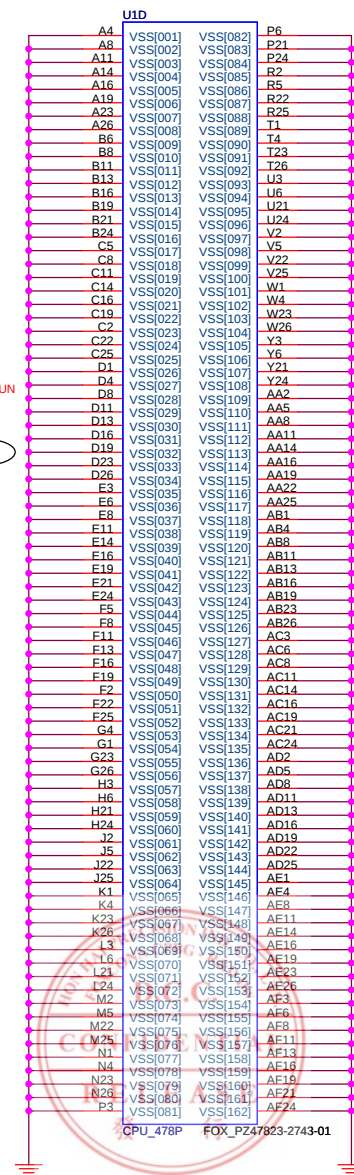
Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.
width=18 mil
spacing=7 mil

LAYOUT NOTE:
Place 0.01uF near PIN B26

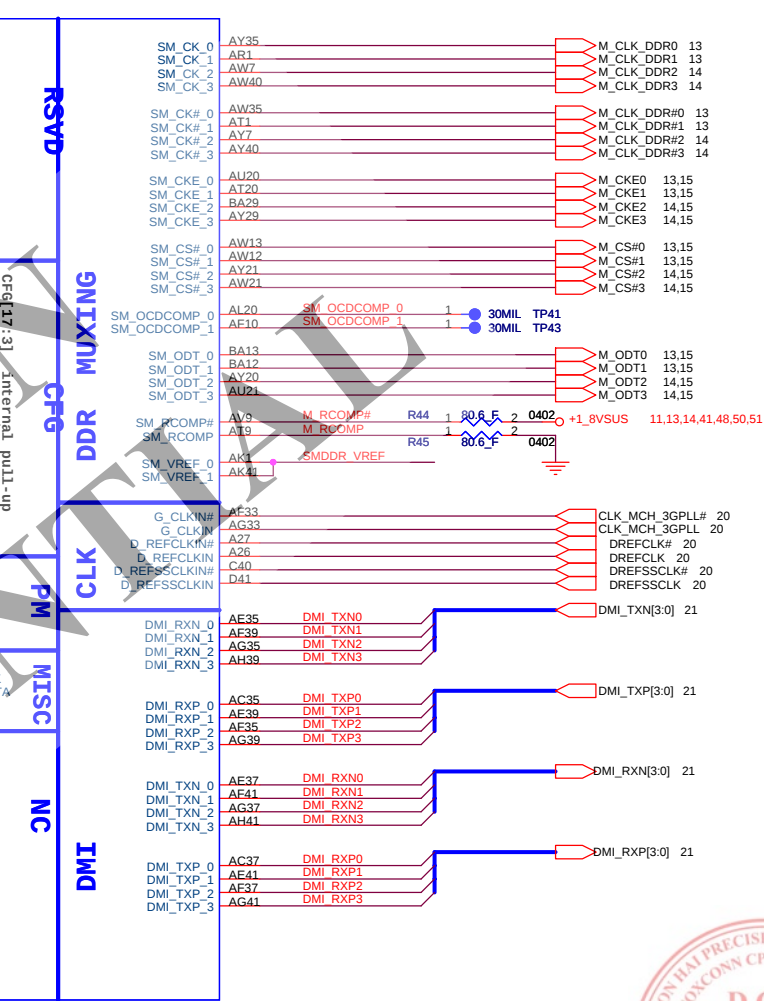
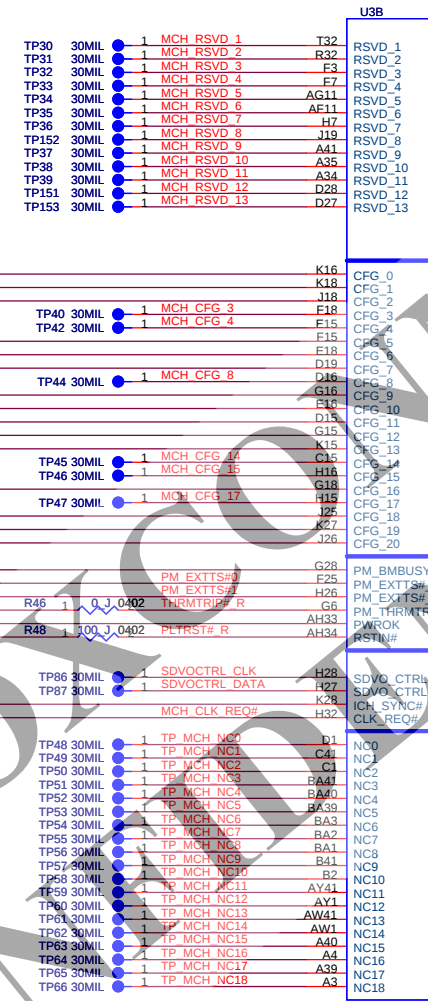
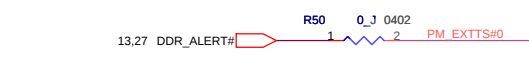
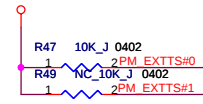
Same Length

LAYOUT NOTE:
Place 0.01uF near PIN B26

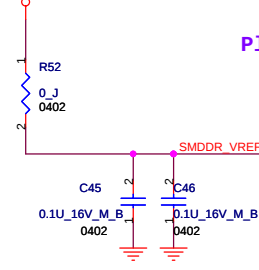
PU & PD avoid to route with stub



+3VVRUN 3.8,10,13,14,16,17,20,21,22,23,24,26,27,28,29,30,33,37,39,41,49,50

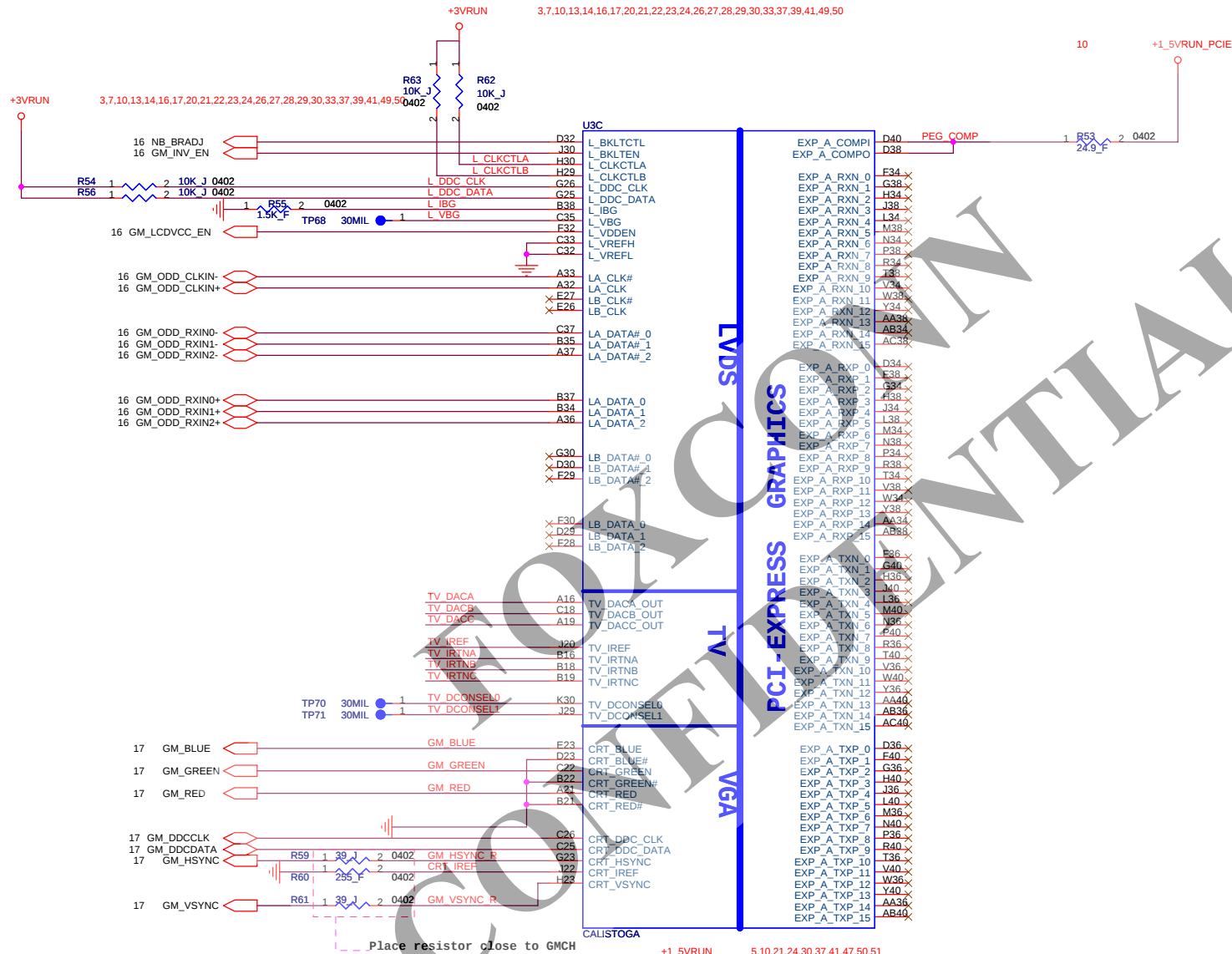


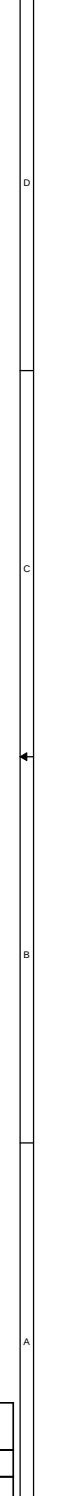
13,48 DDRDIMM_VREF



Place close to chipset







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Title CALISTOGA(VCC CORE) 6 of 7			
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7 MCH_CFG_5 30MIL TP76

MCH_CFG_5 Low = DMIX2
High = DMIX4

MCH_CFG_18 Low = 1.05V(default)
(VCC_CORE Select) High = 1.5V

7 MCH_CFG_18 30MIL TP79

7 MCH_CFG_6 30MIL TP77

MCH_CFG_6 Low = Moby Dick
High = Calistoga
DDR2 select (default high)

MCH_CFG_19 Low = Normal(default)
(DMI LANE REVERSAL) High = LANES REVERSED

7 MCH_CFG_19 30MIL TP80

7 MCH_CFG_7 30MIL TP78

MCH_CFG_7 (CPU Strap) Low = RSVD
High = Mobile Yonah processor

7 MCH_CFG_9 30MIL TP81

MCH_CFG_9 (PCIe Graphics Lane) Low = Reverse Lane
High = Normal operation

MCH_CFG_20 Low = Only SDVO or PCIe x1 is operational (defaults)
High = SDVO and PCIe x1 are operating simultaneously via the PEG port
(PCIe Backward Interoperability mode)

7 MCH_CFG_20 30MIL TP83

7 MCH_CFG_10 30MIL TP82

MCH_CFG_10 (HOST PLL VCC SELECT) Low = RESERVED
High = MOBILITY

7 MCH_CFG_11 30MIL TP84

MCH_CFG_11 (PSB 4x CLK ENABLE) Low = Calistoga
High = Reserved

R93
NC 2.2K_Ω
0402

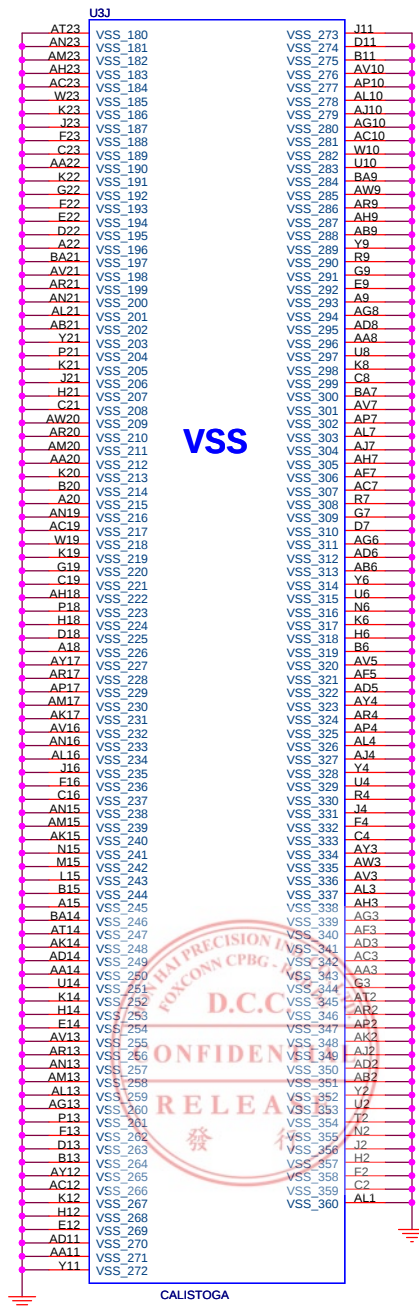
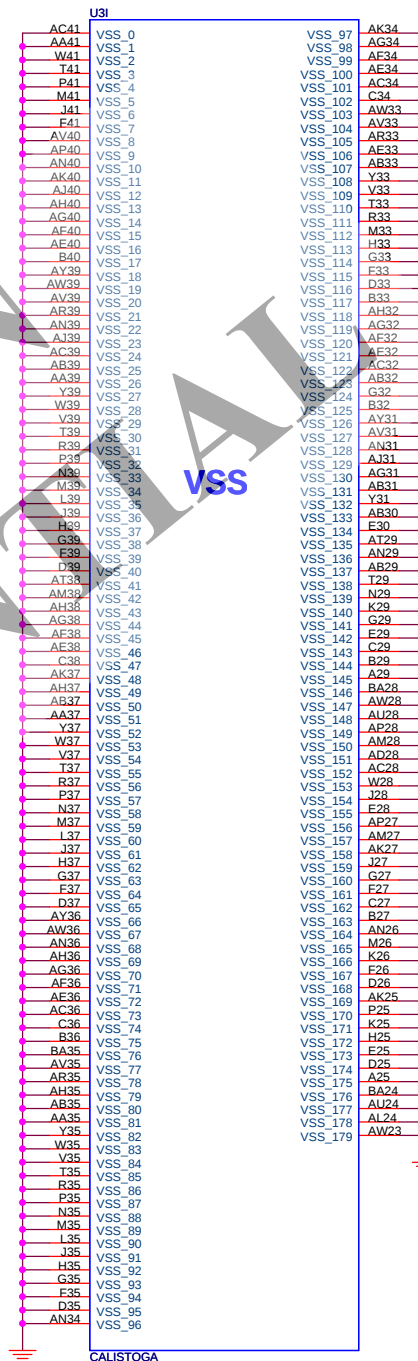
7 MCH_CFG_12 30MIL TP84

7 MCH_CFG_13 30MIL TP85

MCH_CFG [13:12] (XOR/ALLZ) 00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

7 MCH_CFG_16 30MIL TP160

MCH_CFG_16 Low = Dynamic ODT Disabled
(FSB Dynamic ODT) High = Dynamic ODT Enable



7,11,14,41,48,50,51 +1_8VSUS

+1_8VSUS 7,11,14,41,48,50,51

1.8V per DIMM=3.08A

M_A_DM[0..7] 9
M_A_DQ[0..63] 9
M_A_DQS[0..7] 9
M_A_DQS#0..7 9
M_A_A[0..13] 9,15

7,11,14,41,48,50,51 +1_8VSUS

7,48 DDRDIMM_VREF

14 DDR2_VREF

DDR2_VREF

C149 0.1U_16V_M_B 0402

R94 0.1U_16V_M_B 0402

R95 NC_10K_F 0402

R97 NC_10K_F 0402

+3VRUN

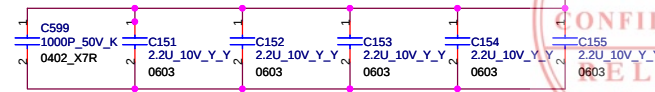
C150 NC_0.1U_16V_M_B 0402

Address: 92H.

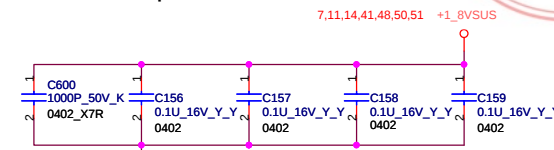
U4
+VS SMBDATA 1
A0 SMBCLK 2
A1 OS 3
A2 GND 4
NC_G751-2P1F

7,11,14,41,48,50,51 +1_8VSUS

Place these Caps near So-Dimm0.



Place these Caps near So-Dimm0.



7,11,14,41,48,50,51 +1_8VSUS

7,15 M_CKE0

9,15 M_A_BS2

9,15 M_A_BS0

9,15 M_A_WE#

9,15 M_A_CAS#

7,15 M_CS#1

7,15 M_ODT1

14,20,23,37 SMB_DATA_SUS

14,20,23,37 SMB_CLK_SUS

+3VRUN

C160 2.2U_10V_Y_Y 0603

C161 0.1U_16V_M_B 0402

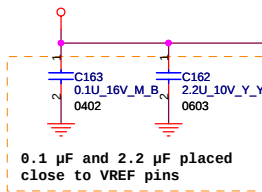
FOX_ASOA426_N4RC_4F

SMBus Address: A0(W)/A1(R)

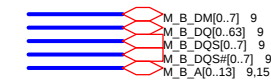
R99 10K_J 0402

R100 10K_J 0402

PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)



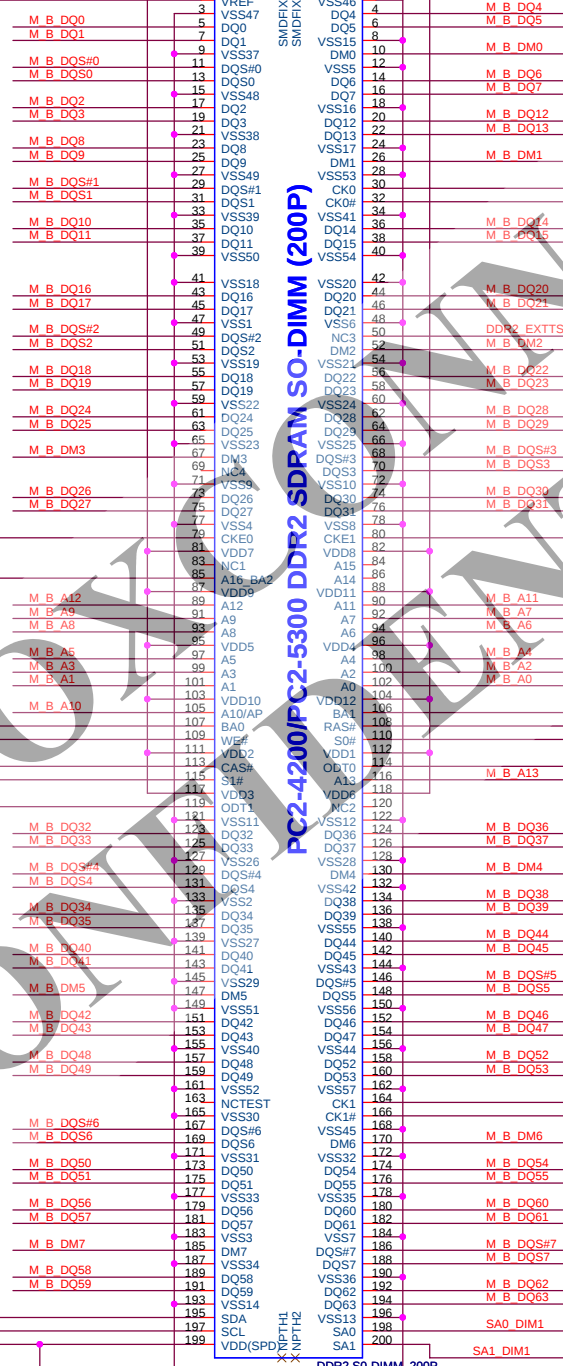
1.8V per DIMM=3.08A



7,15 M_CKE2
9,15 M_B_BS2

9,15 M_B_BS0
9,15 M_B_WE#
9,15 M_B_CAS#
7,15 M_CS#3
7,15 M_ODT3

13,20,23,37 SMB_DATA_SUS
13,20,23,37 SMB_CLK_SUS
+3VRUN



PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)

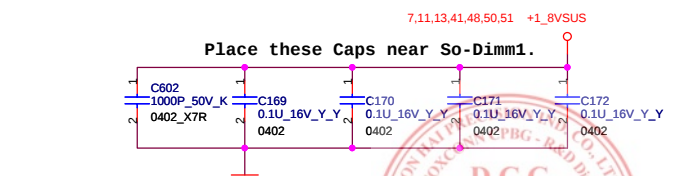
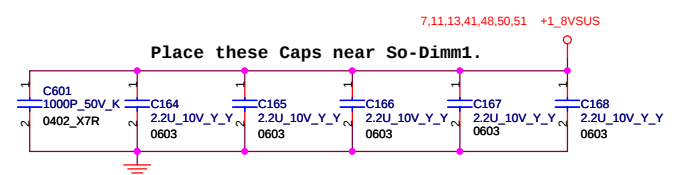
M_CLK_DDR3 7
M_CLK_DDR#3 7

M_CKE3 7,15

M_B_BS1 9,15
M_B_RAS# 9,15
M_CS#2 7,15
M_ODT2 7,15

M_CLK_DDR2 7
M_CLK_DDR#2 7

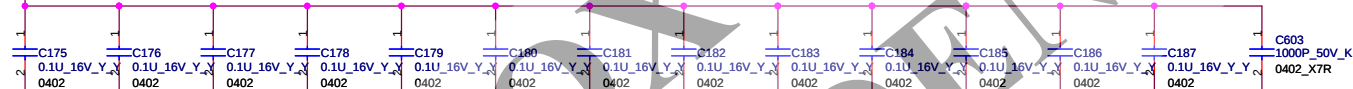
SA0_DIM1
SA1_DIM1



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
File		DDR(I)SO-DIMM 1	
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48,50,51

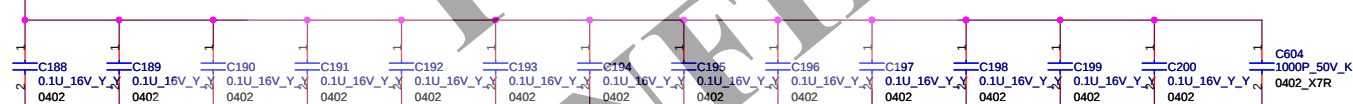
+0_9VSUS



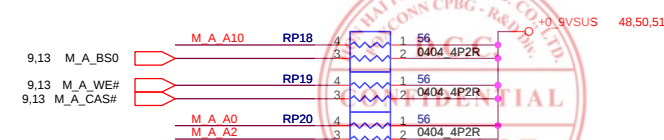
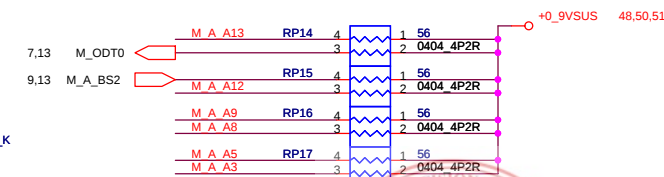
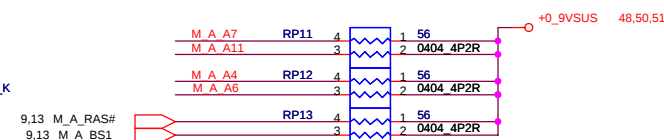
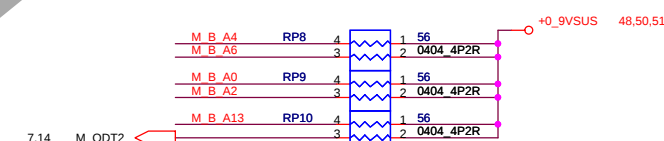
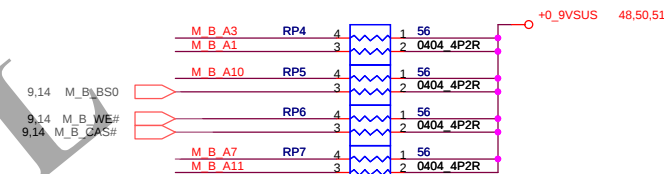
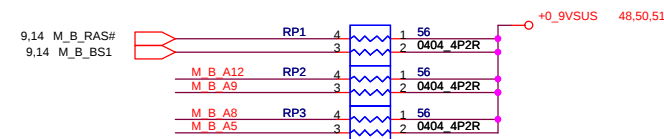
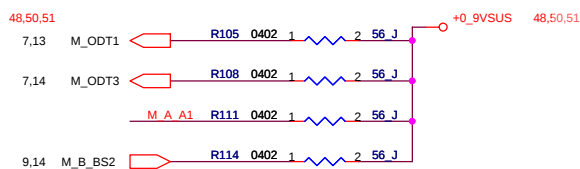
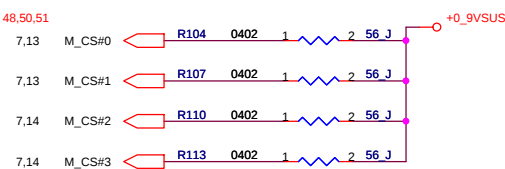
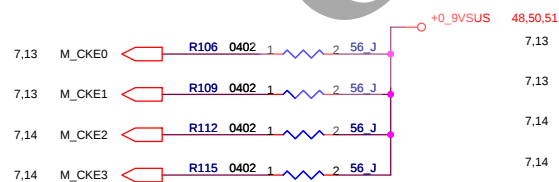
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS

48,50,51

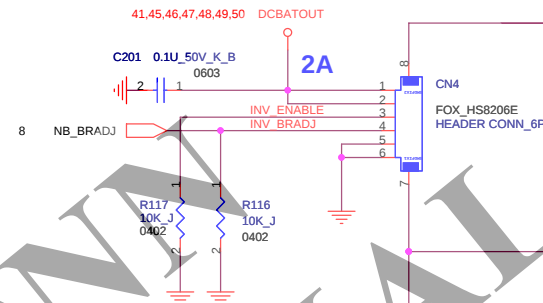
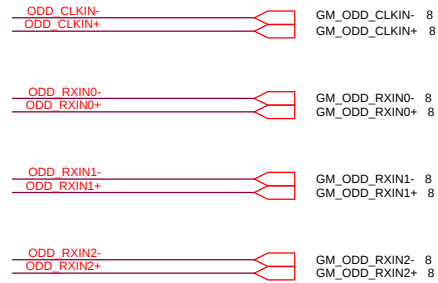
+0_9VSUS



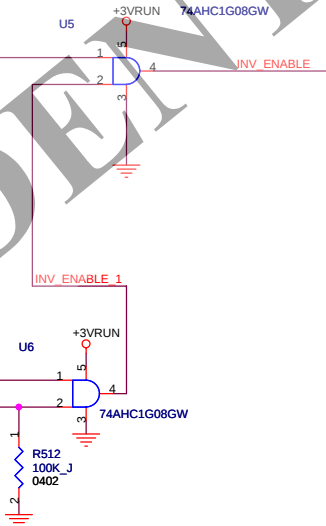
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS



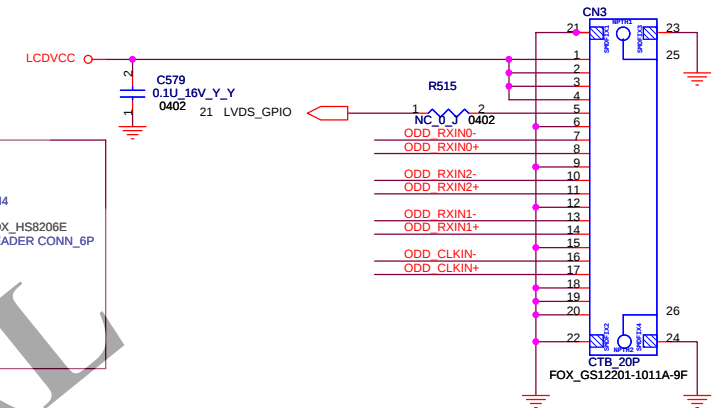
LVDS



INVERTER CONNECTOR



LVDS CONNECTOR



PANEL ID



Type	WXGA	WXGA	WSXGA
Size	15.4" wide	15.4" wide	15.4" wide
Vendor	CPT	QDI	InnoLux
Device Name	CLAA154WA05AN	QDI15TL0703	TBD
Panel ID Check[3..0]	1001	1010	1011

ON=0

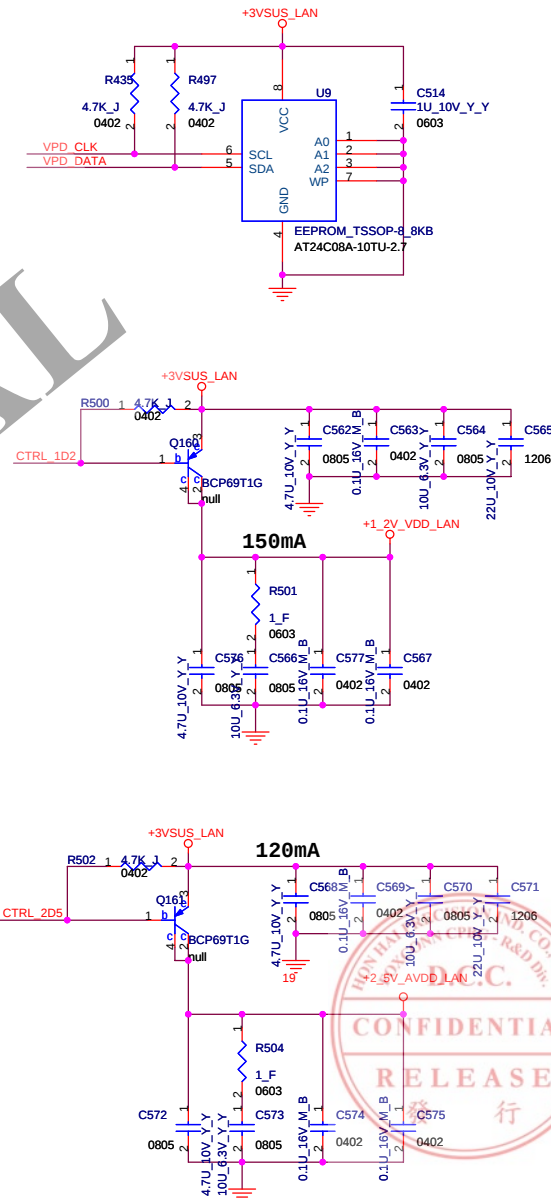
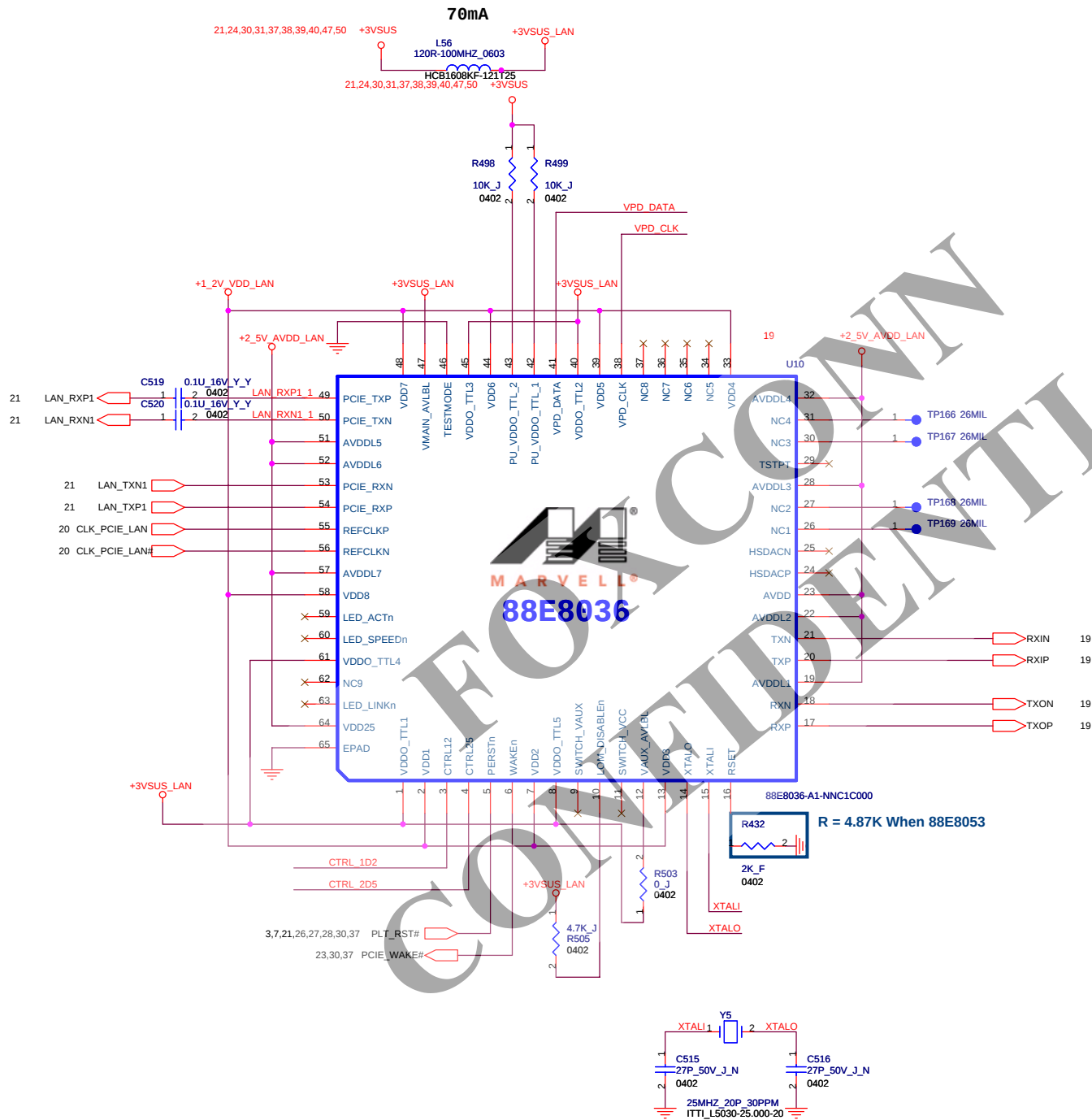
DISCHARGE

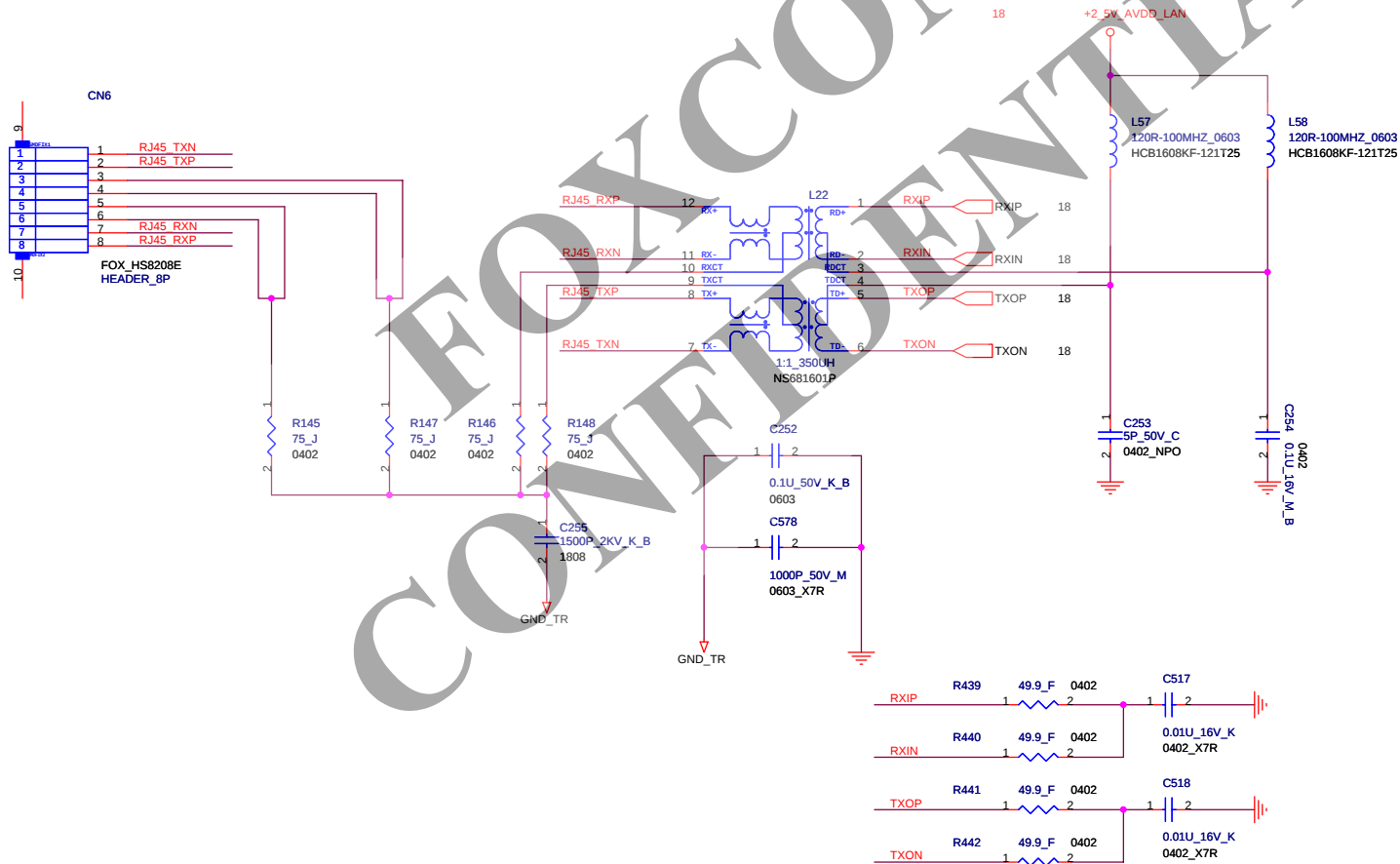
The R461 will consume about
 $0.054 \text{ Watt} (3.3 \times 3.3 / 200 = 0.054 \text{W})$. We changed resistor
 to 0603 size (1/8 Watt)

FOXCONN
 Title **LVDS**
 Size A3
 Date: Tuesday, December 05, 2006

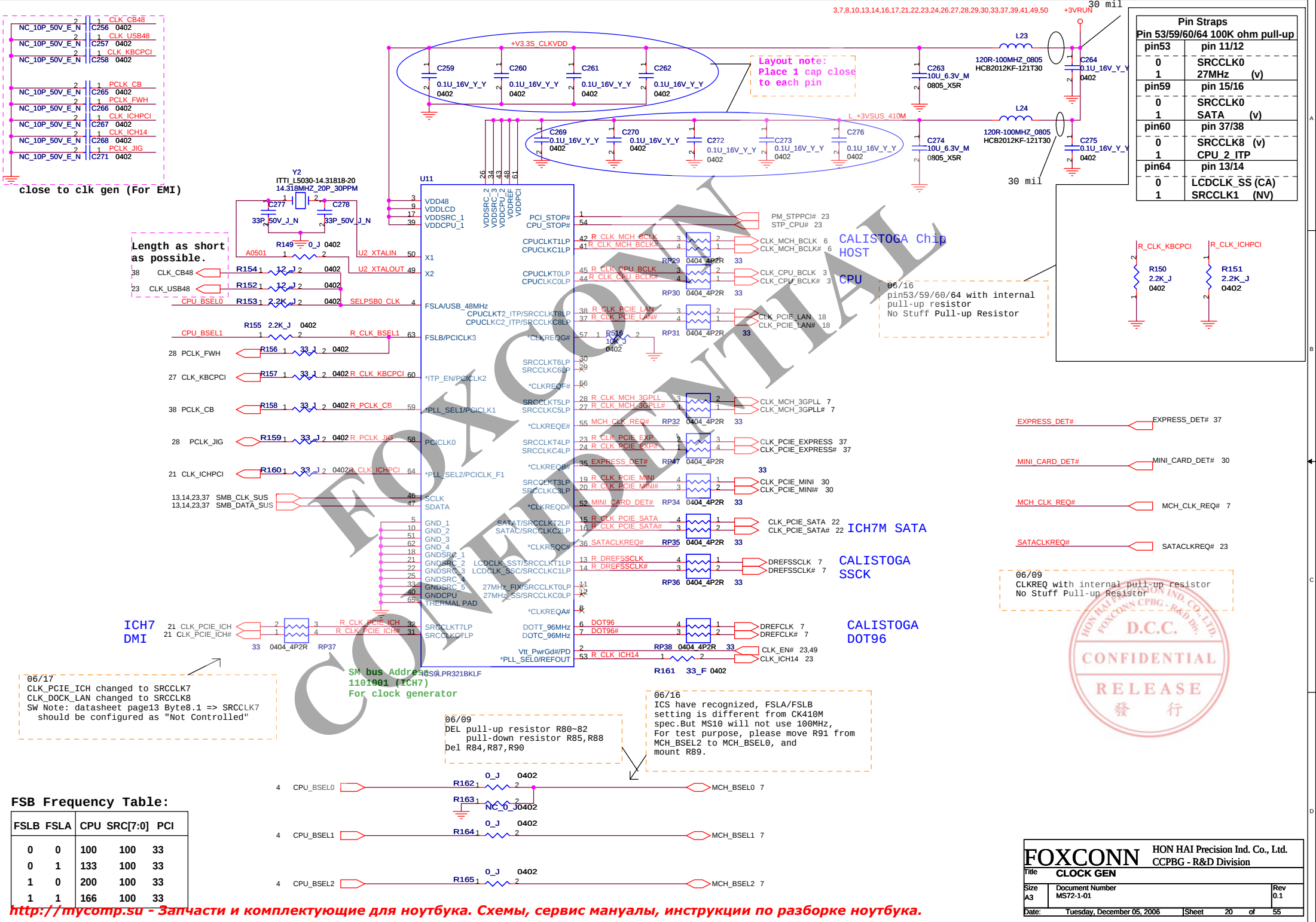
HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division
 Document Number MS72-1-01
 Sheet 16 of 55

Rev 0.1





FOXCONN		HON HAI Precision Ind. Co., Ltd.
Title LAN Transformer		CCPBG - R&D Division
Size A3	Document Number MS72-1-01	Rev 0.1
Date: Tuesday, December 05, 2006	Sheet 19	of 55



NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	CLK_JIG

close to clk gen (For EMI)

Length as short as possible.

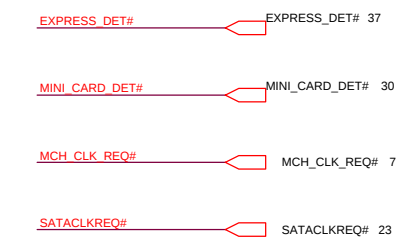
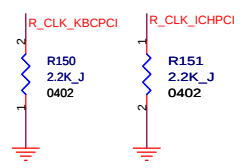
ICH7 DMI

06/17
CLK_PCIE_ICH changed to SRCCLK7
CLK_DOCK_LAN changed to SRCCLK8
SW Note: datasheet page13 Byte8.1 => SRCCLK7 should be configured as "Not Controlled"

FSB Frequency Table:

FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33

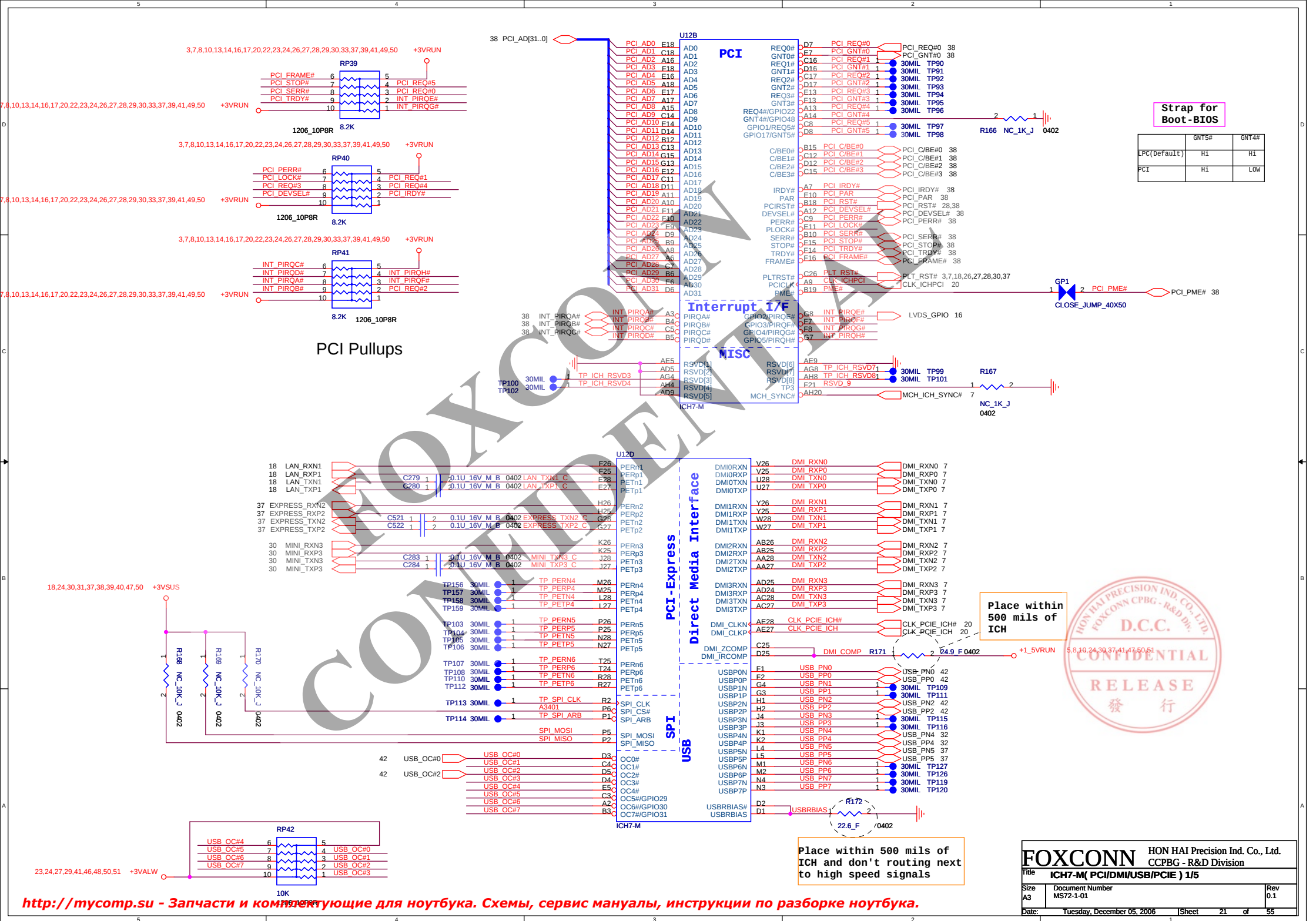
Pin Straps	
Pin	Signal
pin53	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCCLK8 (v)
1	CPU 2 ITP
pin64	pin 13/14
0	LCDCLK_SS (CA)
1	SRCCLK1 (NV)

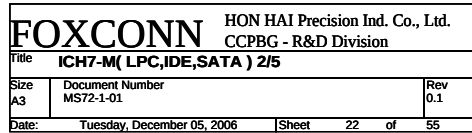


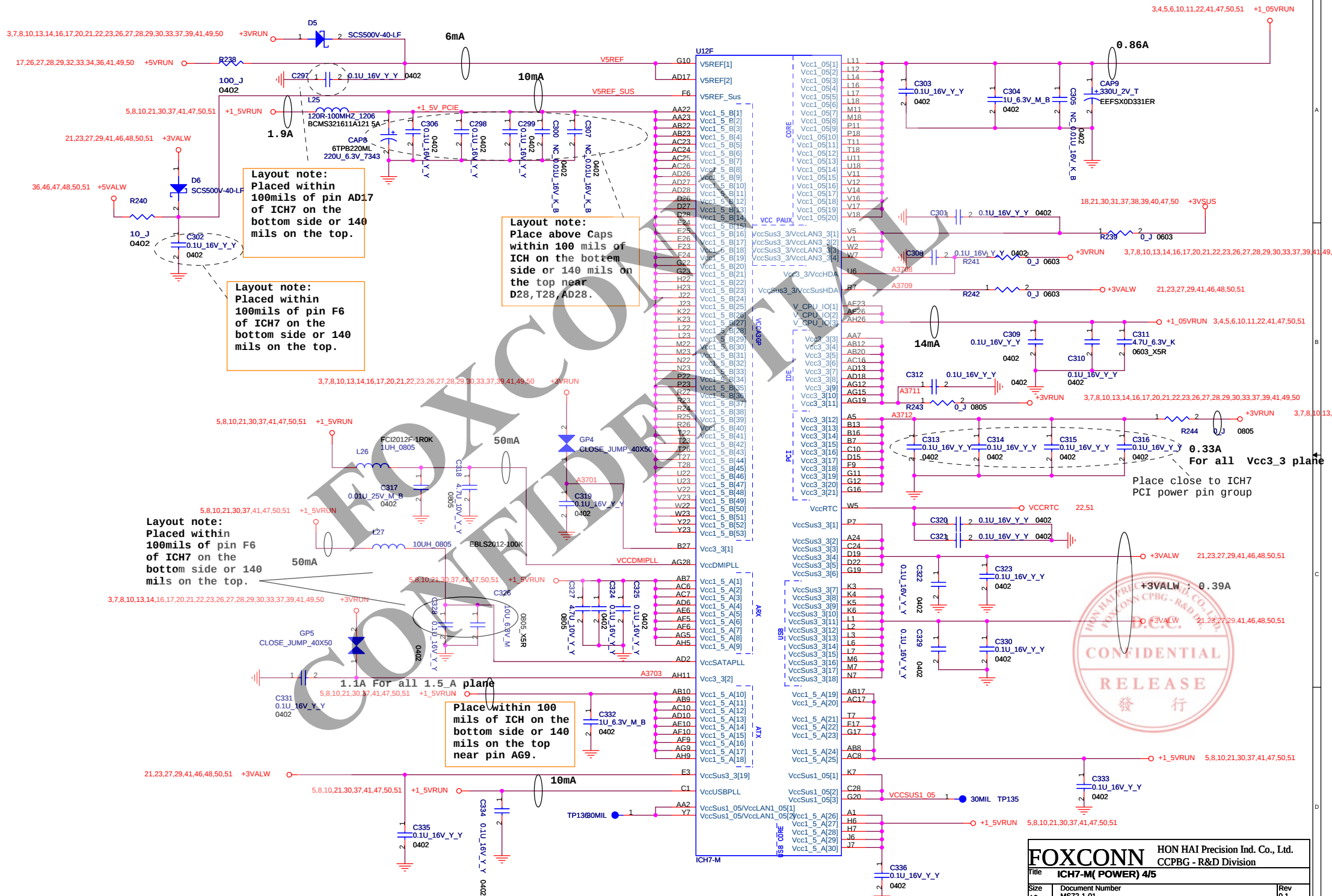
06/09
CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title: CLOCK GEN		
Size: A3	Document Number: MS72-1-01	Rev: 0.1
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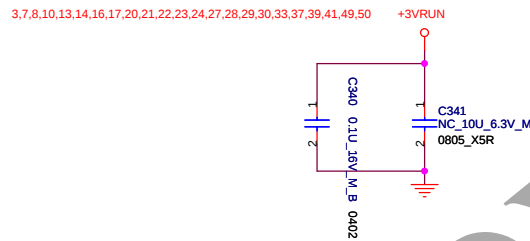
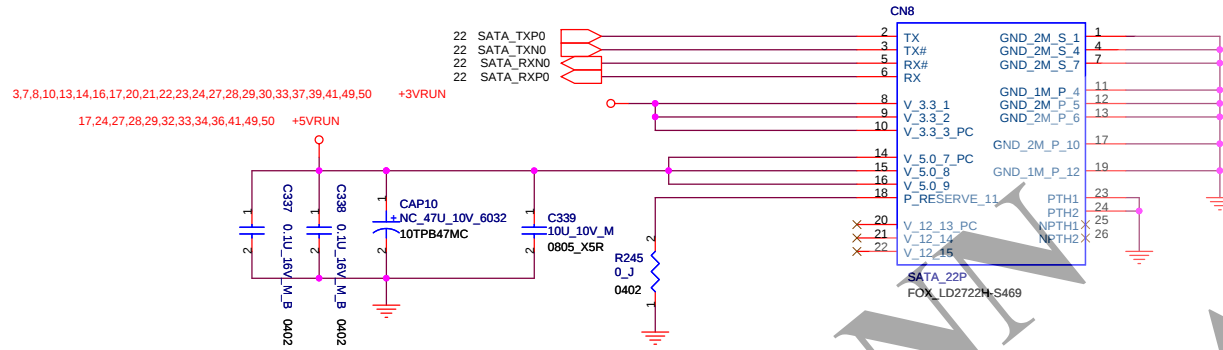
U12E			
A4	VSS[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
B11	VSS[5]	VSS[102]	R13
B14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B26	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T15
D18	VSS[16]	VSS[113]	T16
D21	VSS[17]	VSS[114]	T17
D24	VSS[18]	VSS[115]	U4
E1	VSS[19]	VSS[116]	U12
E2	VSS[20]	VSS[117]	U13
E4	VSS[21]	VSS[118]	U14
E8	VSS[22]	VSS[119]	U15
F15	VSS[23]	VSS[120]	U16
F3	VSS[24]	VSS[121]	U17
F4	VSS[25]	VSS[122]	U24
F5	VSS[26]	VSS[123]	U25
F12	VSS[27]	VSS[124]	U26
F27	VSS[28]	VSS[125]	V2
F28	VSS[29]	VSS[126]	V13
G1	VSS[30]	VSS[127]	V15
G2	VSS[31]	VSS[128]	V27
G5	VSS[32]	VSS[129]	V28
G6	VSS[33]	VSS[130]	W6
G9	VSS[34]	VSS[131]	W24
G14	VSS[35]	VSS[132]	W25
G18	VSS[36]	VSS[133]	W26
G21	VSS[37]	VSS[134]	Y3
G25	VSS[38]	VSS[135]	Y24
G26	VSS[39]	VSS[136]	Y27
G28	VSS[40]	VSS[137]	Y28
H3	VSS[41]	VSS[138]	AA1
H4	VSS[42]	VSS[139]	AA24
H5	VSS[43]	VSS[140]	AA25
H24	VSS[44]	VSS[141]	AA26
H27	VSS[45]	VSS[142]	AB4
H28	VSS[46]	VSS[143]	AB6
J1	VSS[47]	VSS[144]	AB11
J2	VSS[48]	VSS[145]	AB14
J5	VSS[49]	VSS[146]	AB16
J24	VSS[50]	VSS[147]	AB19
J25	VSS[51]	VSS[148]	AB21
J26	VSS[52]	VSS[149]	AB24
K24	VSS[53]	VSS[150]	AB27
K27	VSS[54]	VSS[151]	AB28
K28	VSS[55]	VSS[152]	AC2
L13	VSS[56]	VSS[153]	AC5
L15	VSS[57]	VSS[154]	AC9
L24	VSS[58]	VSS[155]	AC11
L25	VSS[59]	VSS[156]	AD1
L26	VSS[60]	VSS[157]	AD3
M3	VSS[61]	VSS[158]	AD4
M4	VSS[62]	VSS[159]	AD7
M5	VSS[63]	VSS[160]	AD8
M12	VSS[64]	VSS[161]	AD11
M13	VSS[65]	VSS[162]	AD15
M14	VSS[66]	VSS[163]	AD19
M15	VSS[67]	VSS[164]	AD23
M16	VSS[68]	VSS[165]	AE2
M17	VSS[69]	VSS[166]	AE4
M24	VSS[70]	VSS[167]	AE8
M27	VSS[71]	VSS[168]	AE11
M28	VSS[72]	VSS[169]	AE13
N1	VSS[73]	VSS[170]	AE18
N2	VSS[74]	VSS[171]	AE21
N5	VSS[75]	VSS[172]	AE24
N6	VSS[76]	VSS[173]	AE25
N11	VSS[77]	VSS[174]	AE2
N12	VSS[78]	VSS[175]	AE4
N13	VSS[79]	VSS[176]	AF8
N14	VSS[80]	VSS[177]	AF11
N15	VSS[81]	VSS[178]	AF27
N16	VSS[82]	VSS[179]	AF28
N17	VSS[83]	VSS[180]	AG1
N18	VSS[84]	VSS[181]	AG3
N24	VSS[85]	VSS[182]	AG7
N25	VSS[86]	VSS[183]	AG11
N26	VSS[87]	VSS[184]	AG14
P3	VSS[88]	VSS[185]	AG17
P4	VSS[89]	VSS[186]	AG20
P12	VSS[90]	VSS[187]	AG25
P13	VSS[91]	VSS[188]	AH1
P14	VSS[92]	VSS[189]	AH3
P15	VSS[93]	VSS[190]	AH7
P16	VSS[94]	VSS[191]	AH12
P17	VSS[95]	VSS[192]	AH23
P24	VSS[96]	VSS[193]	AH27
P27	VSS[97]	VSS[194]	

ICH7-M



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Title			CCPBG - R&D Division
ICH7-M(GND) 5/5			
Size	Document Number	Rev	
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Date:	Tuesday, December 05, 2006	Sheet	25 of 55

SATA HDD CONN



3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

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3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

CD-ROM CONN

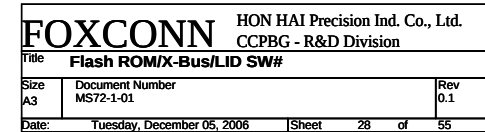
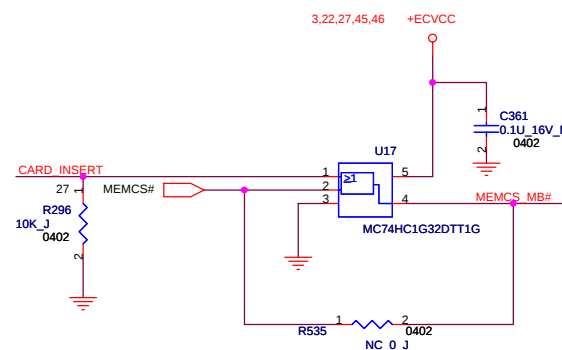
3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

3,7,8,10,13,14,16,17,20,21,22,23,24,27,28,29,30,33,37,39,41,49,50 +3VRUN

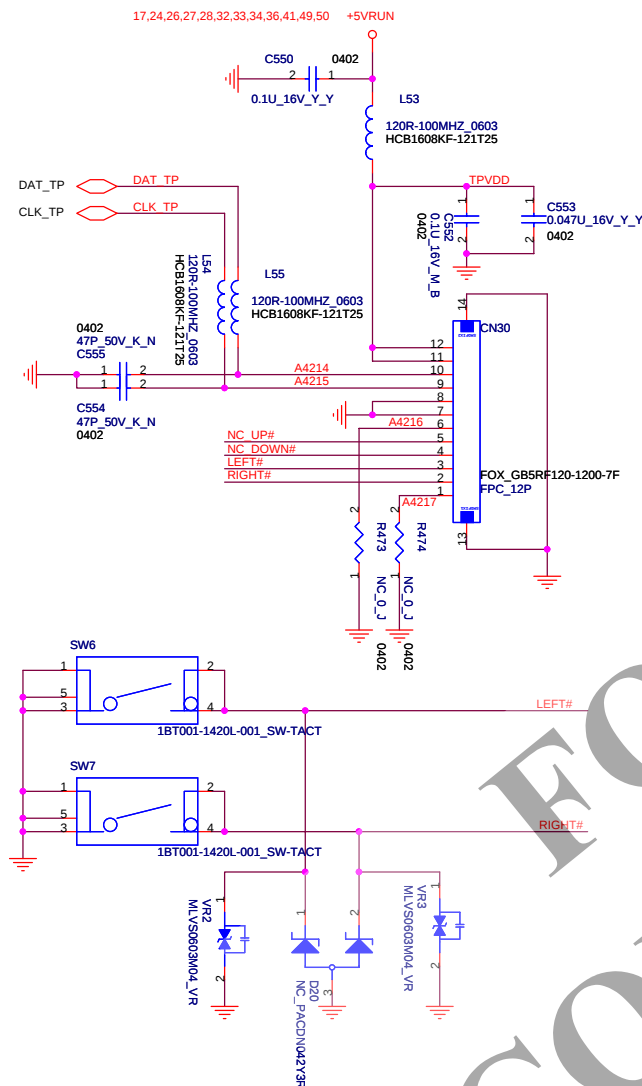


FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	SATA HDD/CD-ROM	
Size	Document Number	Rev
A3	MS72-1-01	0.1
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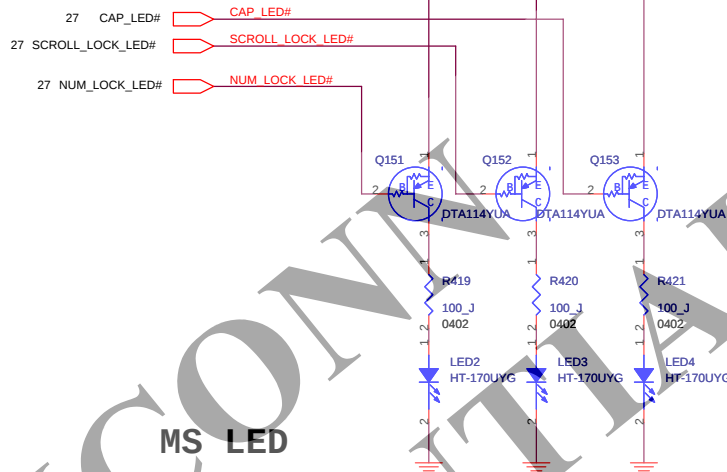




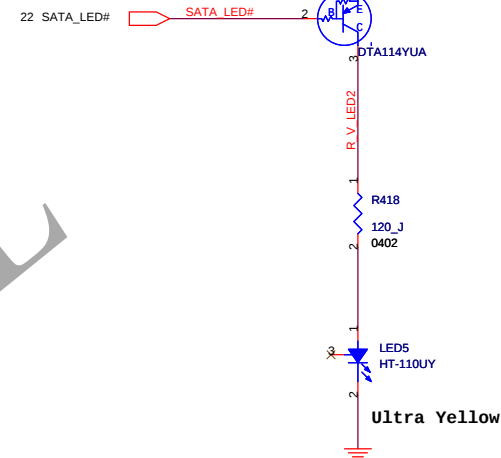
Touch Pad Board



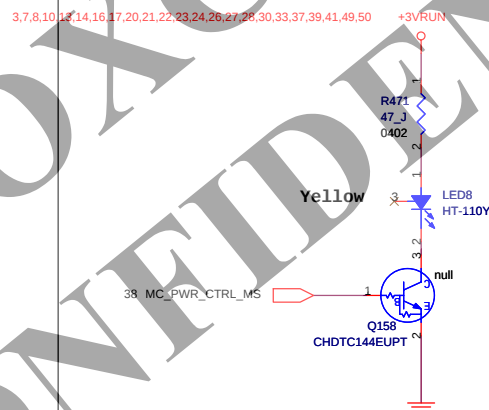
CAP_LED# SCROLL_LOCK_LED# NUM_LOCK_LED#



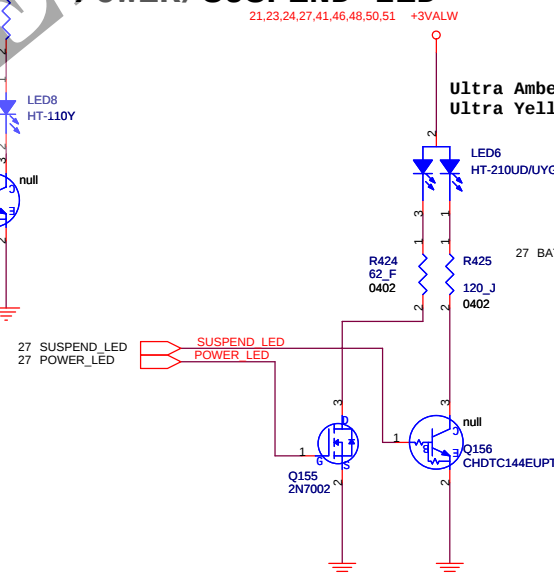
HDD_LED#



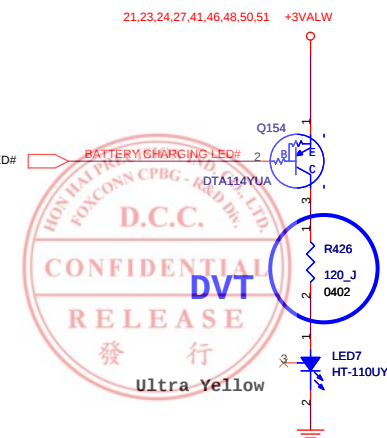
MS LED

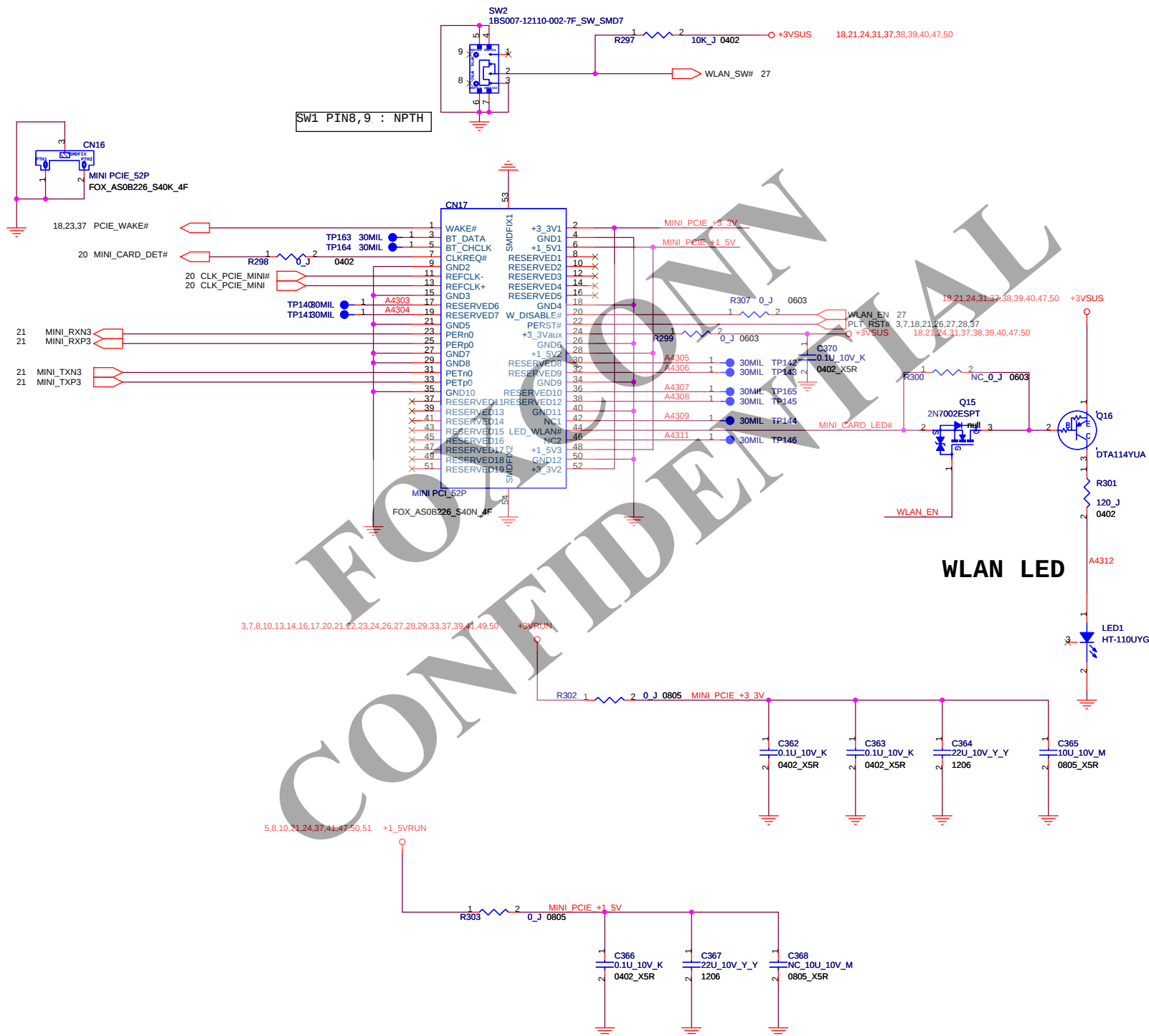


POWER/SUSPEND LED



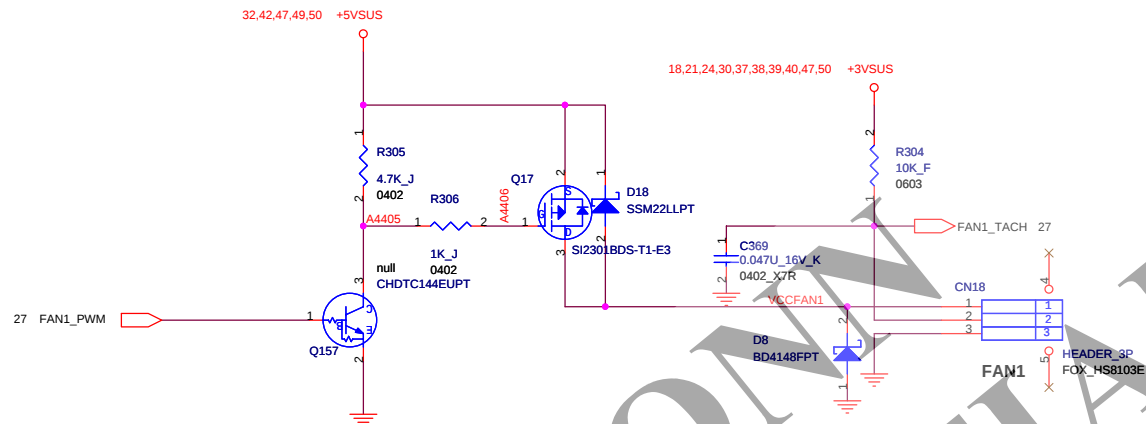
BATTERY CHARGING LED#



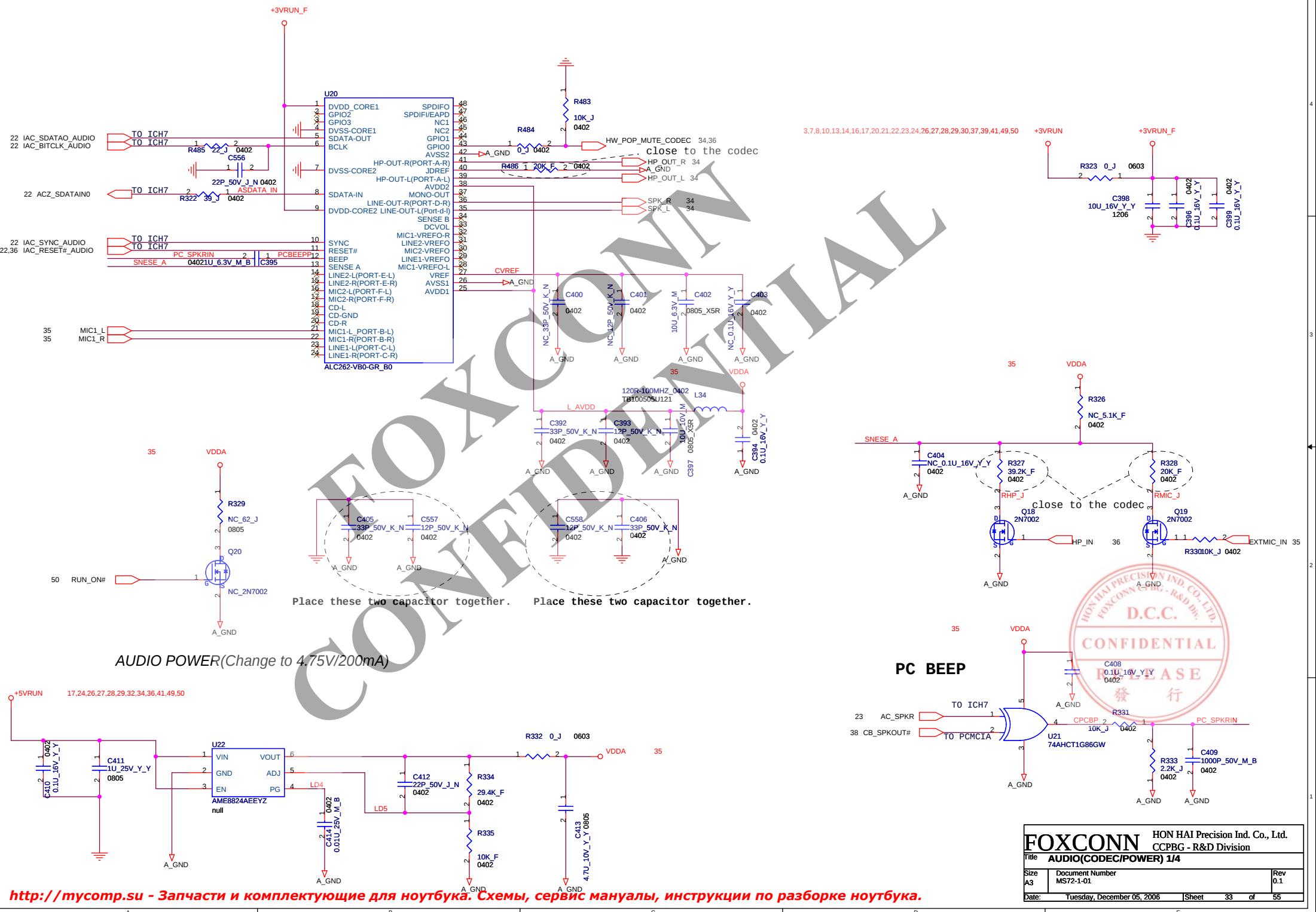


FOXCONN HON HAI Precision Ind. Co., Ltd.		
Mini-PCIE Card		
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FAN1

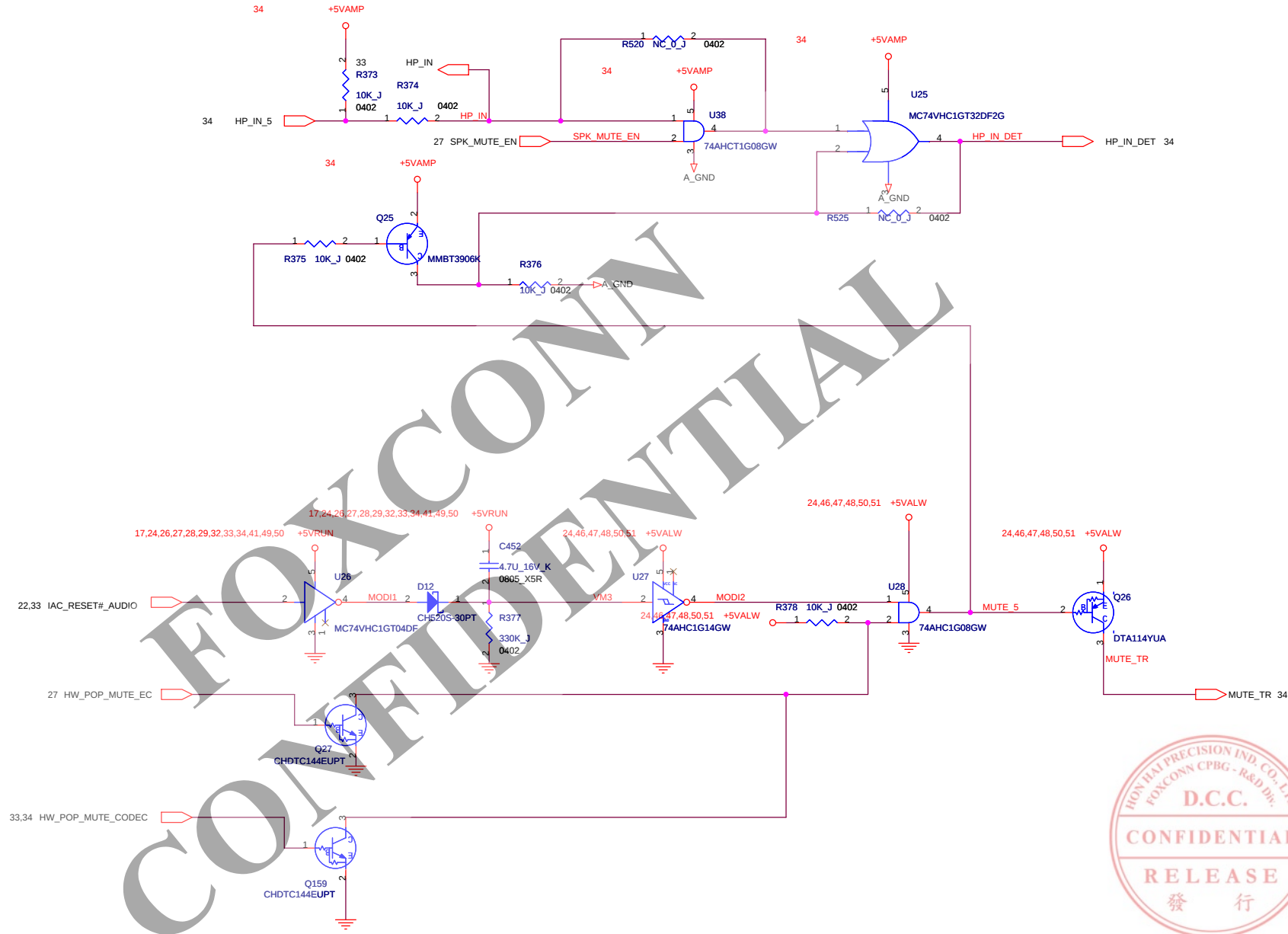


FOXCONN		HON HAI Precision Ind. Co., Ltd.
Title FAN		CCPBG - R&D Division
Size A3	Document Number MS72-1-01	Rev 0.1
Date:	Tuesday, December 05, 2006	Sheet 31 of 55



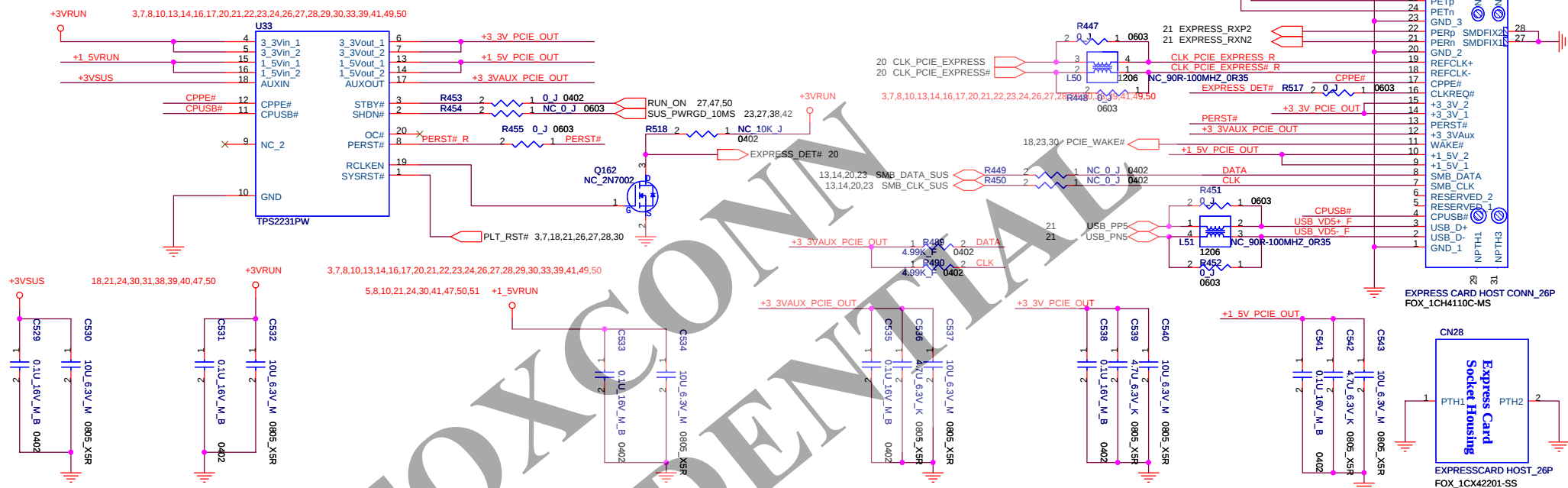
<http://mycomp.ru> - Запчасти и комплектующие для ноутбука. Схемы, сервис мануалы, инструкции по разборке ноутбука.

FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title AUDIO(CODEC/POWER) 1/4		
Size A3	Document Number MS72-1-01	Rev 0.1
Date: Tuesday, December 05, 2006	Sheet 33	of 55

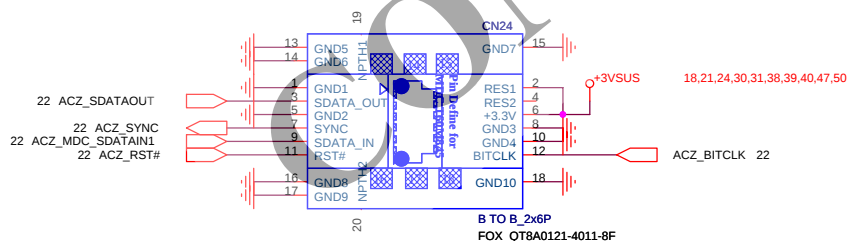


FOXCONN			HON HAI Precision Ind. Co., Ltd.	
Title AUDIO (MUTE) 4/4			CCPBG - R&D Division	
Size A3	Document Number MS72-1-01		Rev 0.1	
Date:	Tuesday, December 05, 2006	Sheet	36	of 55

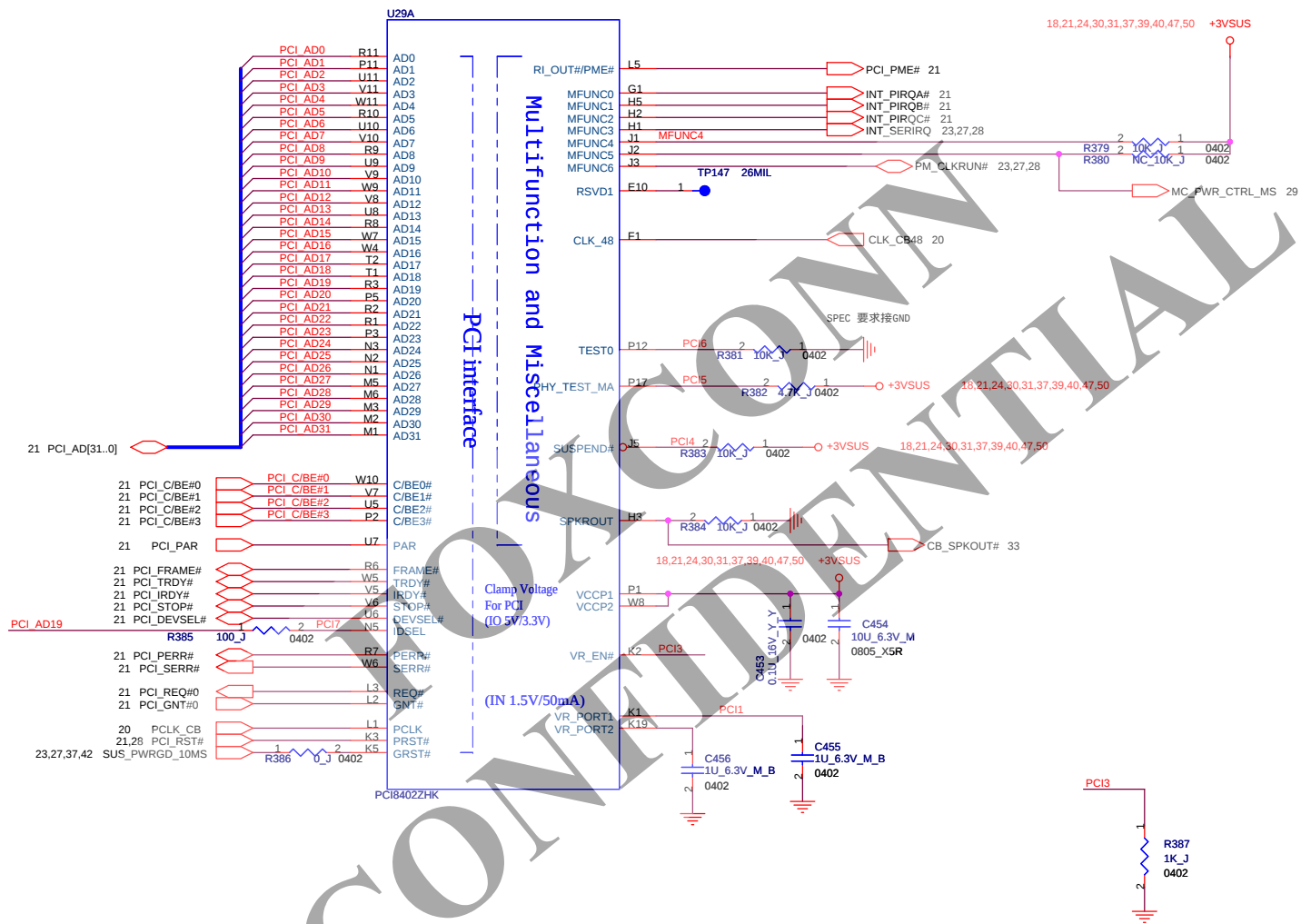
EXPRESS CONN



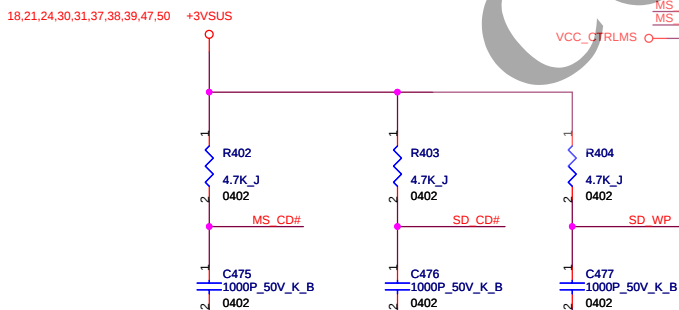
MDC CONN.



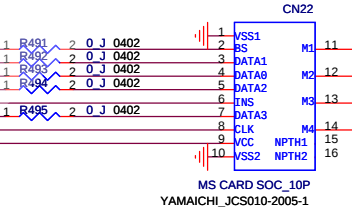
FOXCONN		HON HAI Precision Ind. Co., Ltd.
File EXPRESS CARD		CCPBG - R&D Division
Size A3	Document Number MS72-1-01	Rev 0.1
Date: Tuesday, December 05, 2006	Sheet 37	of 55



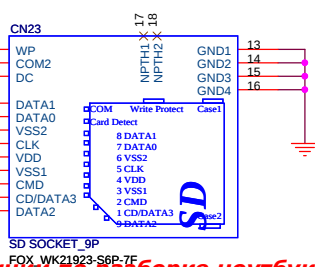
FOXCONN		HON HAI Precision Ind. Co., Ltd.
Title PCI (PCI BUS) 1/3		CCPBG - R&D Division
Size A3	Document Number MS72-1-01	Rev 0.1
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MS STD/DUO CONN.



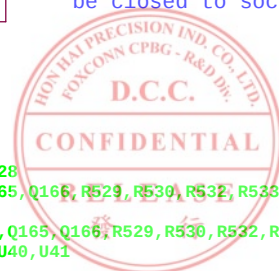
SD CONN.



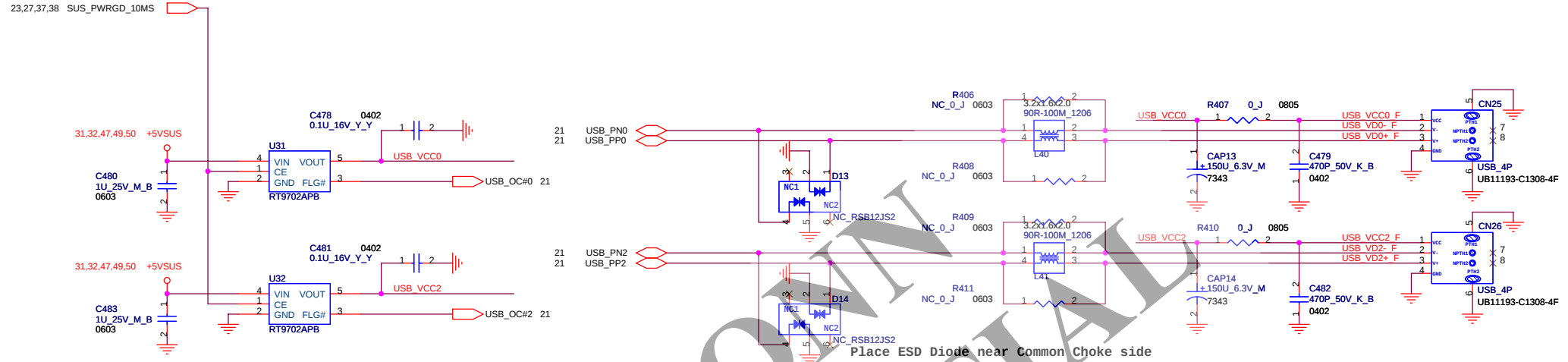
Solution1 :
Mount U36,U37,R527,R528
NC F2,F3,Q163,Q164,Q165,Q166,R529,R530,R532,R533,U40,U41
Solution2 :
Mount F2,F3,Q163,Q164,Q165,Q166,R529,R530,R532,R533
NC U36,U37,R527,R528,U40,U41
Solution3 :
Mount U40,U41,R527,R528
NC U36,U37,F2,F3,Q163,Q164,Q165,Q166,R529,R530,R532,R533

These capacitors should be closed to socket pin

These capacitors should be closed to socket pin

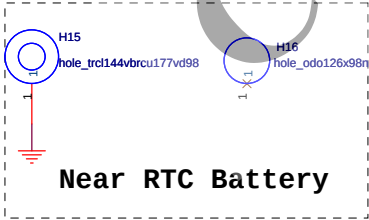
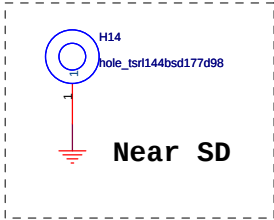
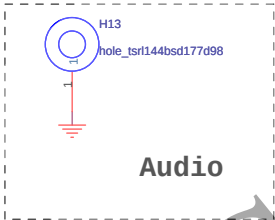
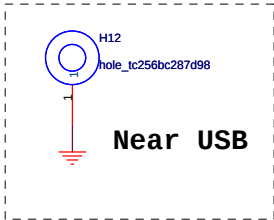
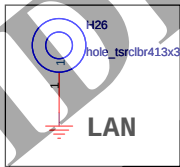
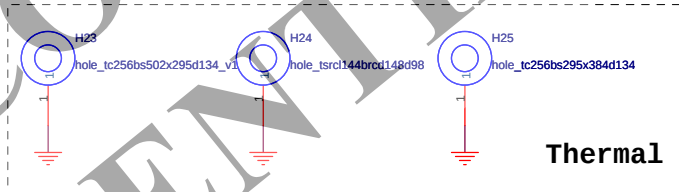
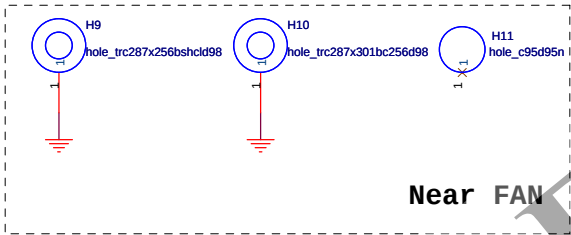
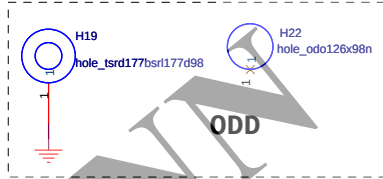
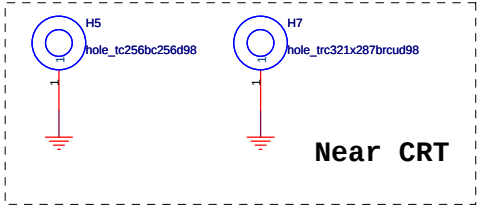
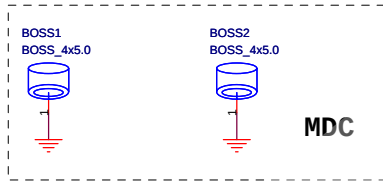
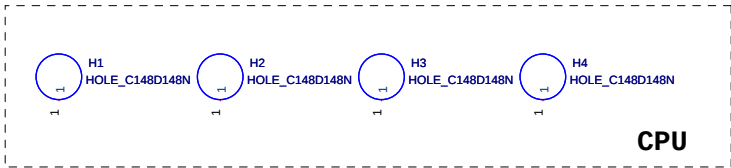


USB CONN X 2

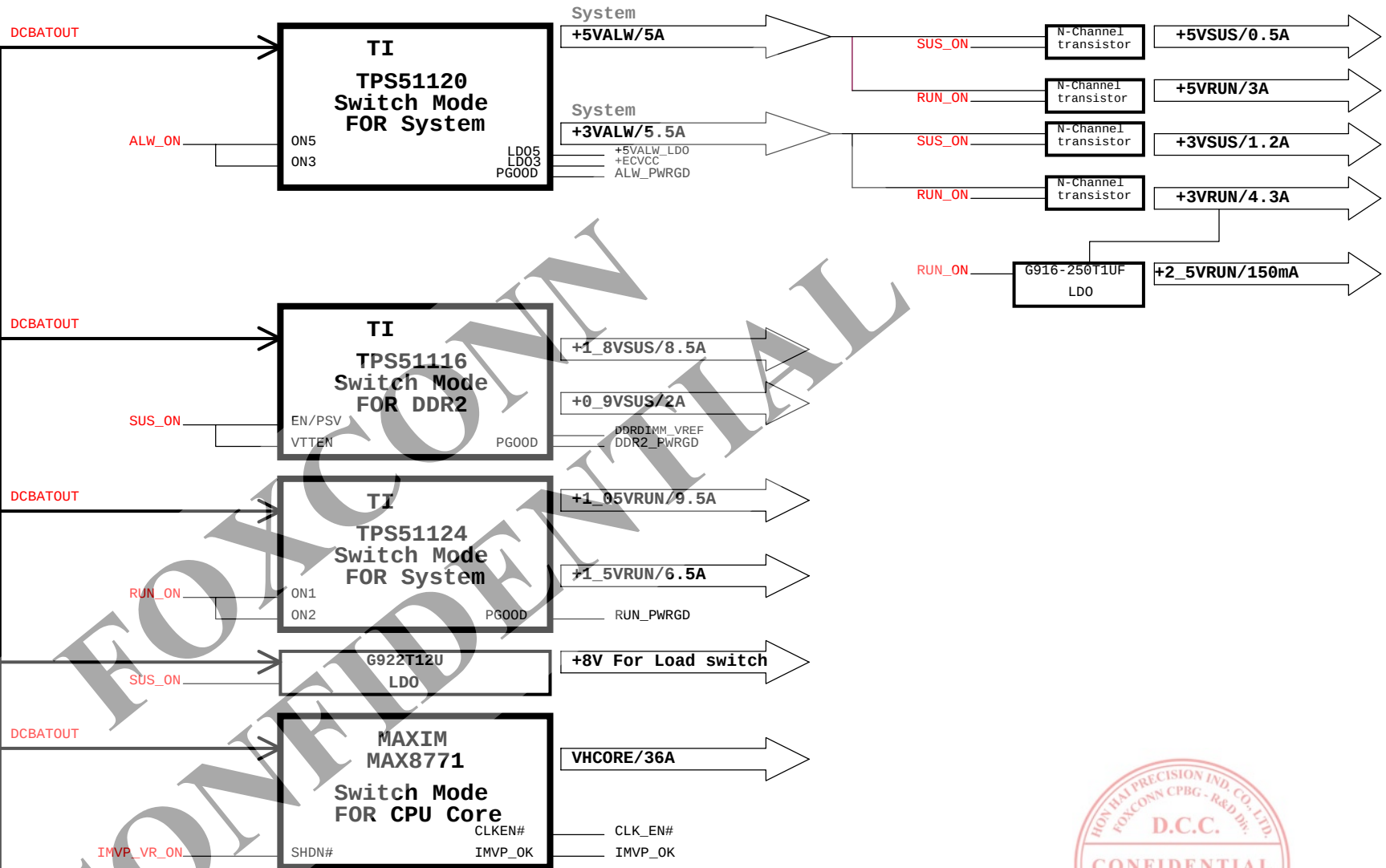
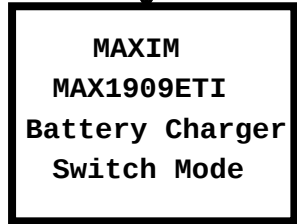
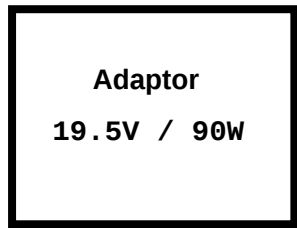


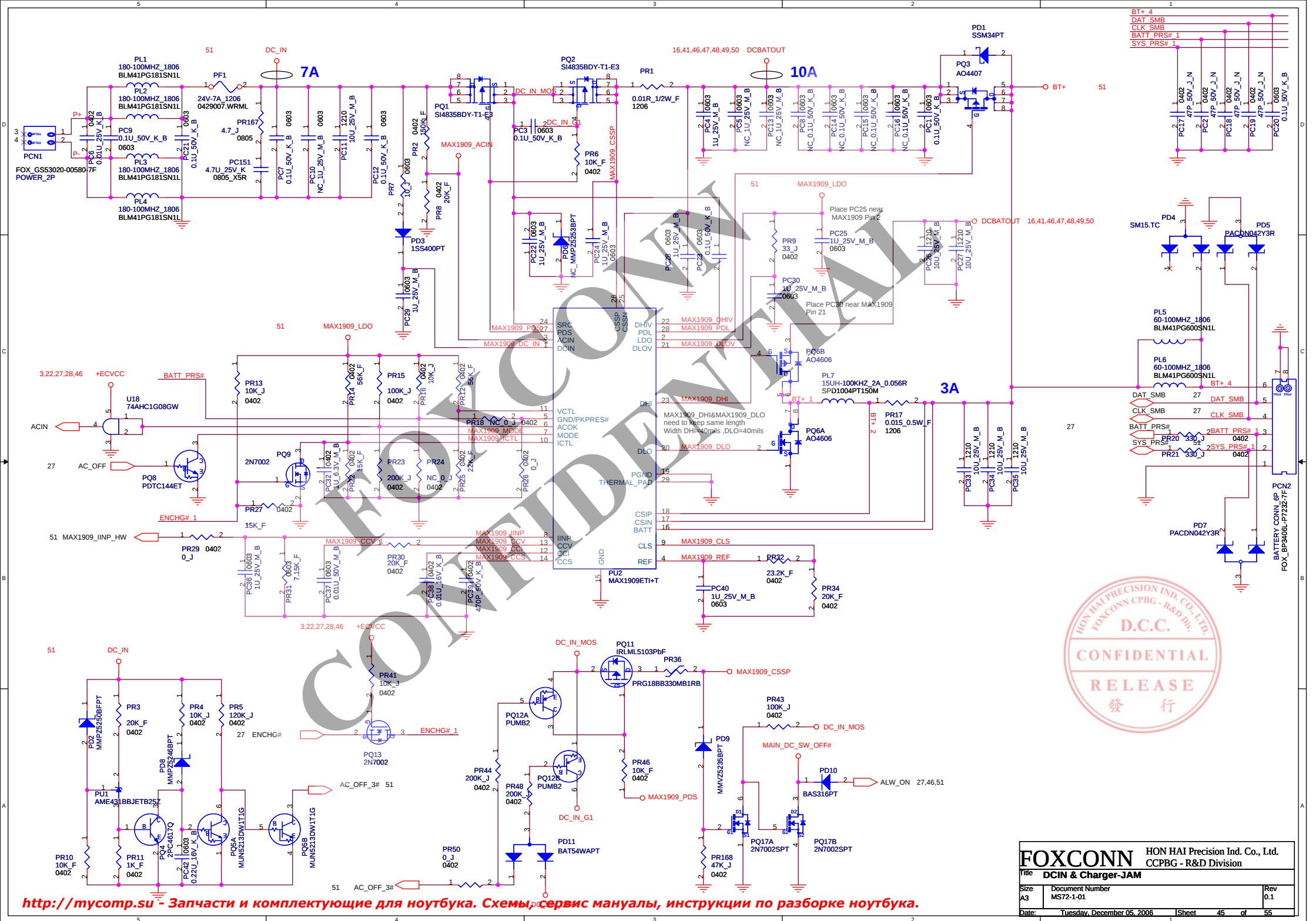
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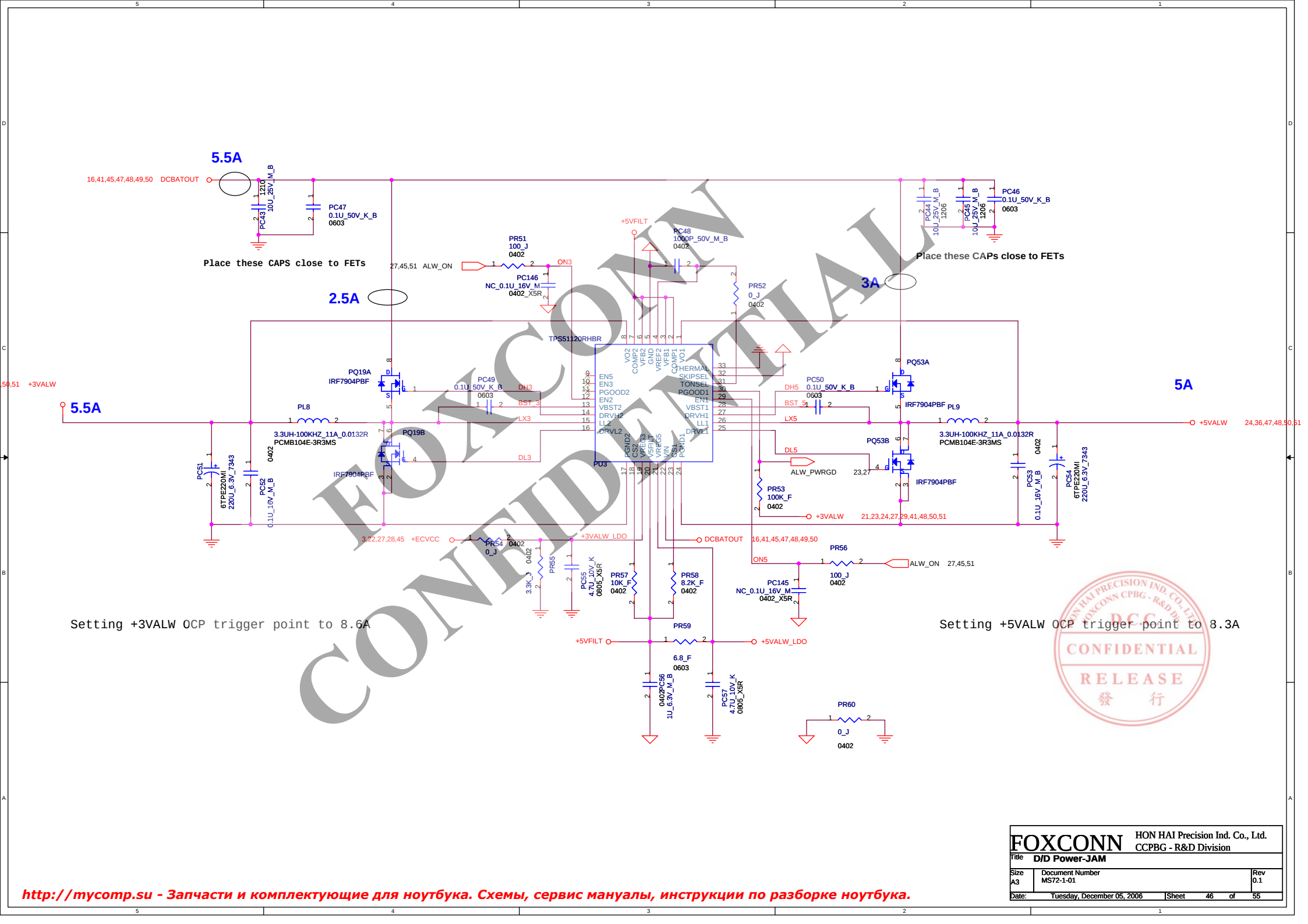


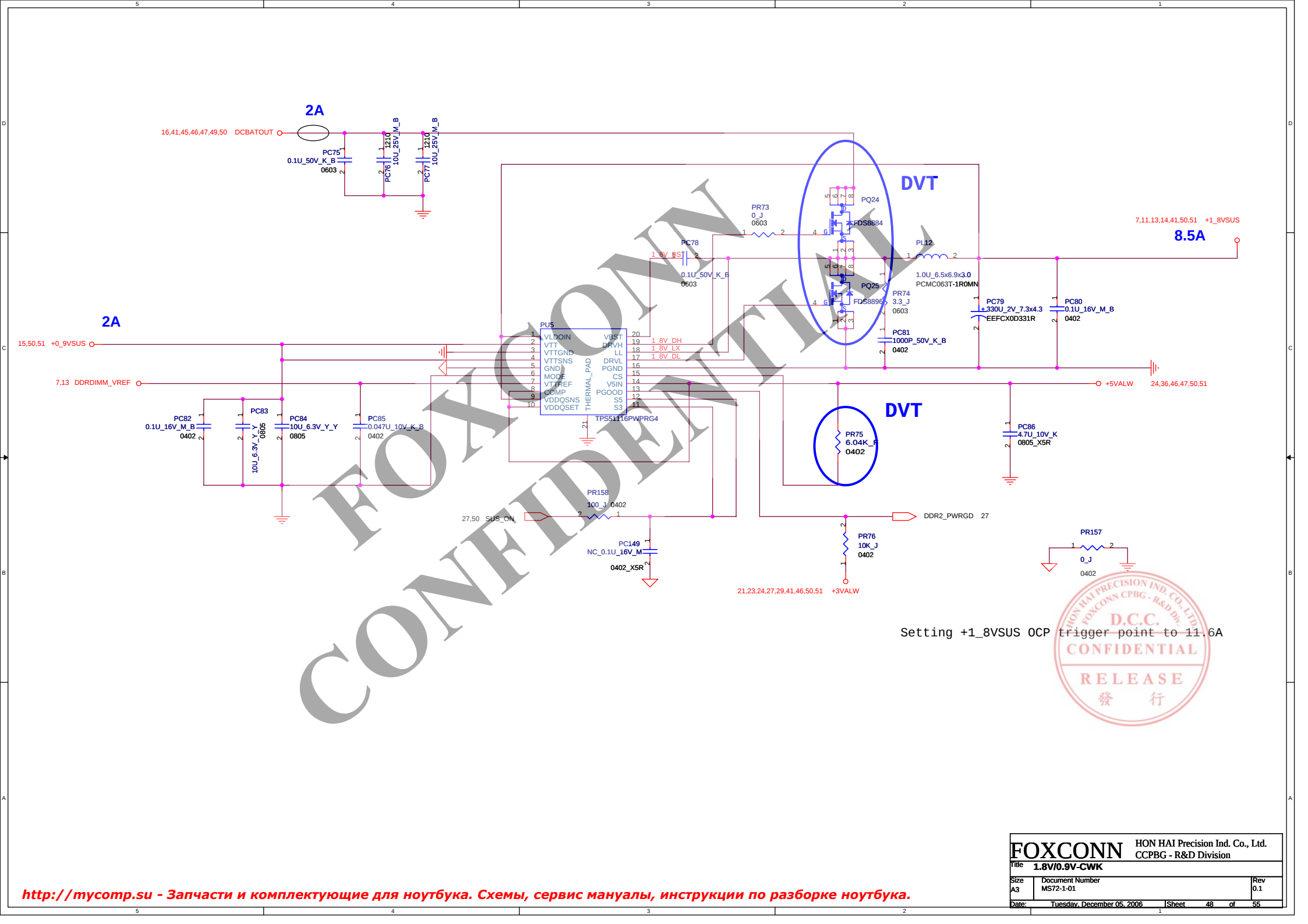


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		HOLE	
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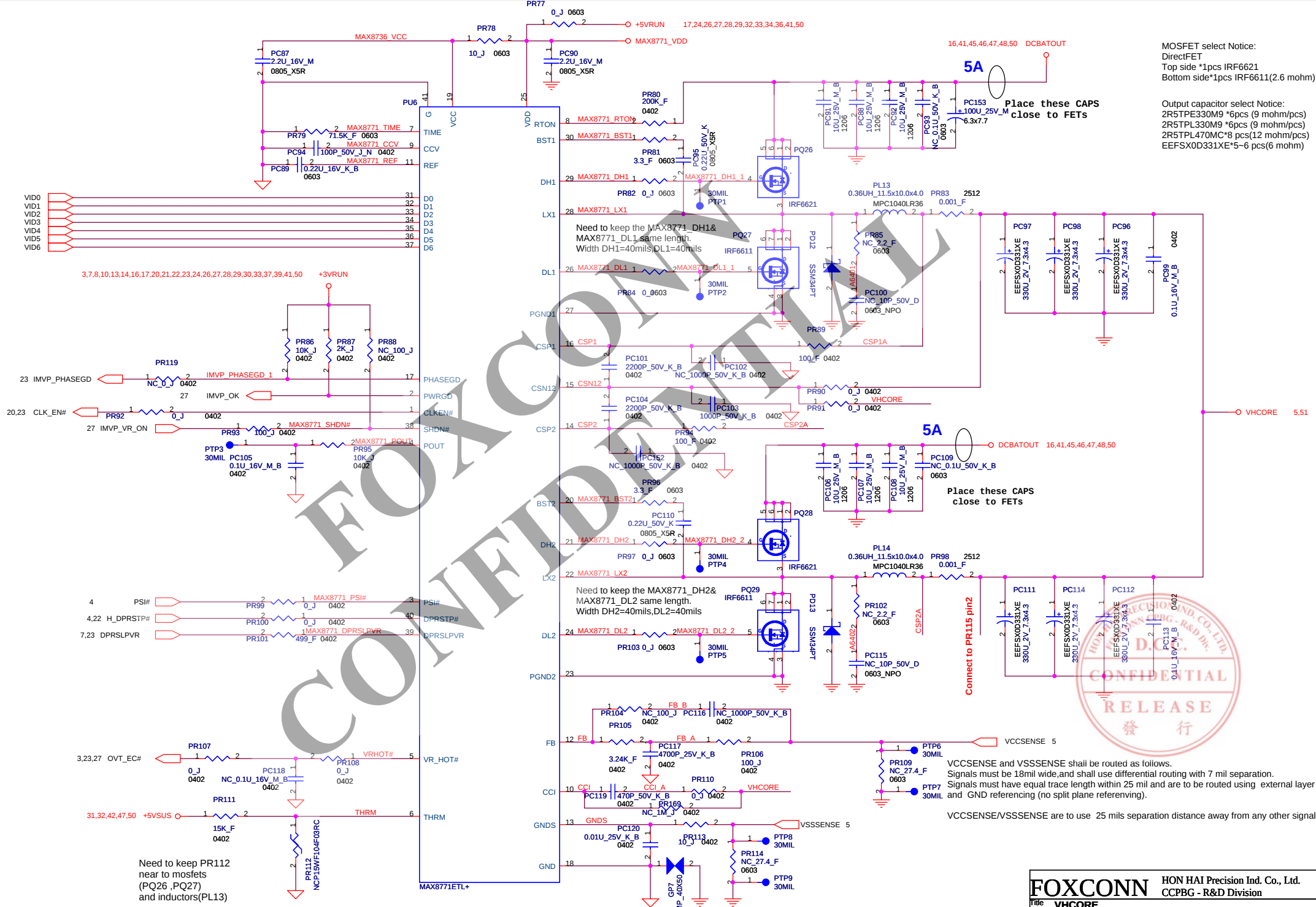




Setting +1_8VSUS OCP trigger point to 11.6A

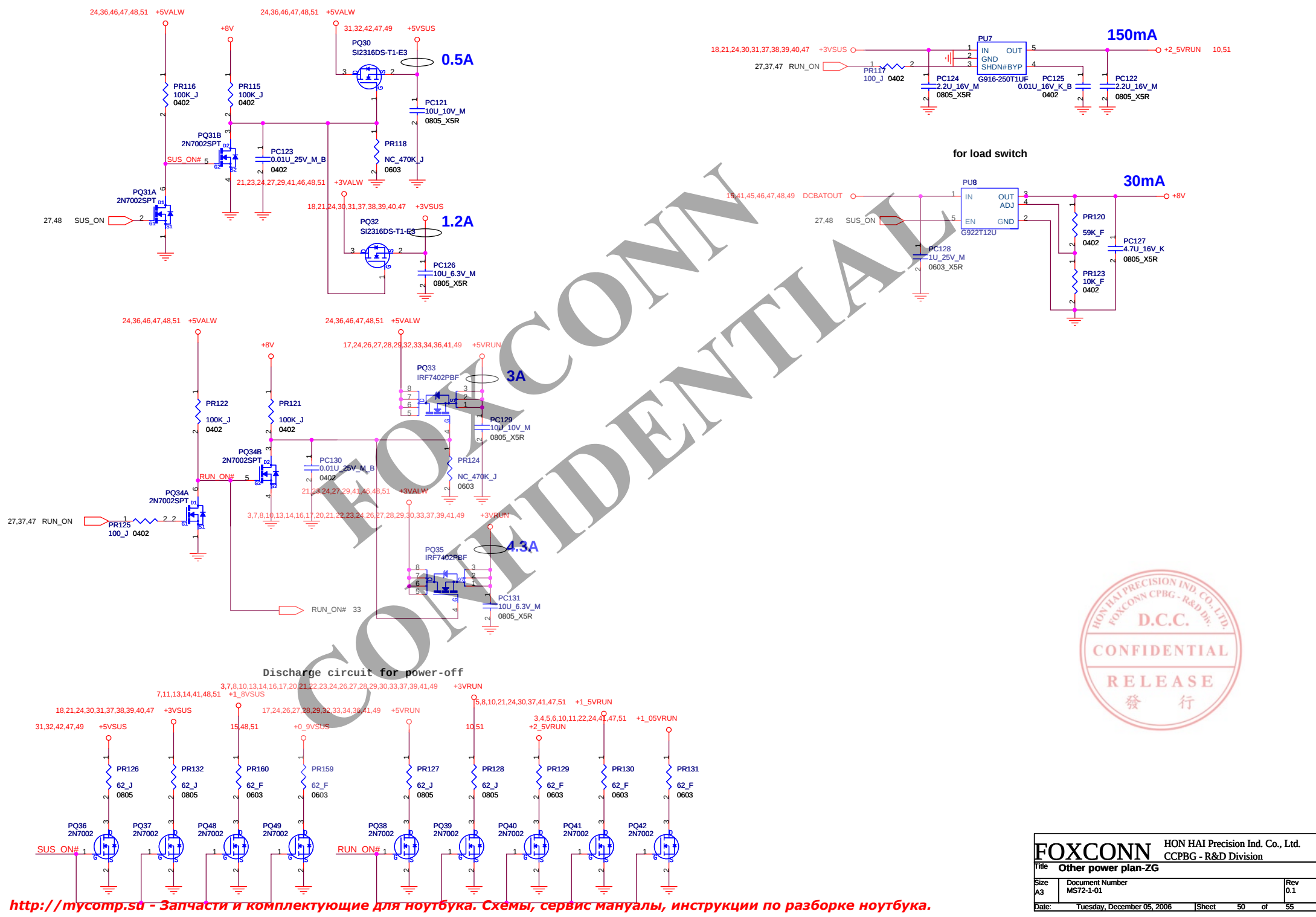


FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
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MOSFET select Notice:
DirectFET
Top side *1pcs IRF6621
Bottom side*1pcs IRF6611(2.6 mohm)

Output capacitor select Notice:
2R5TPE330M9 *6pcs (9 mohm/pcs)
2R5TPL330M9 *6pcs (9 mohm/pcs)
2R5TPL470MC*8 pcs(12 mohm/pcs)
EEFSX0D331XE*5-6 pcs(6 mohm)



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
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HISTORY (1)

DVT

(2006/11/14)
P.11 Add C608 and NC CAP7 for purchase convenient.
P.17 Add R544 and NC R121for CRB requirement(refer to Capell_Valley_CRB_Schematics_Rev1_502 page18)
P.33 NC R483 for Page36 had pull low 10k resistor to GND
P.34 Change CAP11,CAP12 from 1C-31T0337-M101 to 1C-42T0107-M100 for application modification
P.36 Add Q167, Q168, R536 and NC U26, U27,U28, D12, C452, R377,R378 for application modification
Change Q27, Q159, from 17-CHDTC14-4E01 to 17-PMBT390-4200 for application modification
Change Q26 from 17-DTA114Y-UA00 to 17-MMBT390-6K00 for application modification
Add R540,R541,R542,R543,R537,R538,R539,C609 for application modification

(2006/11/15)
P.47 Change PQ22 from 17-1RF7807-2000 to 17-FDS8884-0000 for application modification
Change PQ23 from 17-1RF8113-0000 to 17-FDS8896-0000 for application modification
P.48 Change PQ24 from 17-1RF7807-2000 to 17-FDS8884-0000 for application modification
Change PQ25 from 17-1RF8113-0000 to 17-FDS8896-0000 for application modification

(2006/11/20)
P.11 Del C608 and mount CAP7 for MOR requirement
P.17 Del R544 and mount R121 for MOR requirement
P.47 Change PR67 from 1R-0000472-F200 to 1R-0007321-F200 for power PWM OCP application modification
P.48 Change PR75 from 1R-0000562-F200 to 1R-0006041-F200 for power PWM OCP application modification

(2006/11/21)
P.33 Add R483 for MOR requirement
P.36 Del Q167, Q168, R536 and add U26, U27,U28,D12, C452, R377,R378 for MOR requirement
Change Q27, Q159, from 17-PMBT390-42001 to 17-CHDTC14-4E01for MOR requirement
Change Q26 from 17-MMBT390-6K00 to 17-DTA114Y-UA00 for MOR requirement
Del R540,R541,R542,R543,R537,R538,R539,C609 for MOR requirement

(2006/11/22)
P.28 Add R535 0om for X-BUS CONN del on MP
P.47 Add PC154 and change PR61 from 10k to 100k for RUN_PWRGD glitch issue
Change the power supply of PU4 pin16 from +5VSUS to +5VALW for application modification

(2006/11/23)
P.47 Add PR170,PR171 for MOR requirement

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