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40	ICH7-M(POWER) 4/5	1.1	2006/08/10	80		1.1	2006/08/10

Project Code & Schematics Subject: MS21 MP Main Board

(TYPE 2)

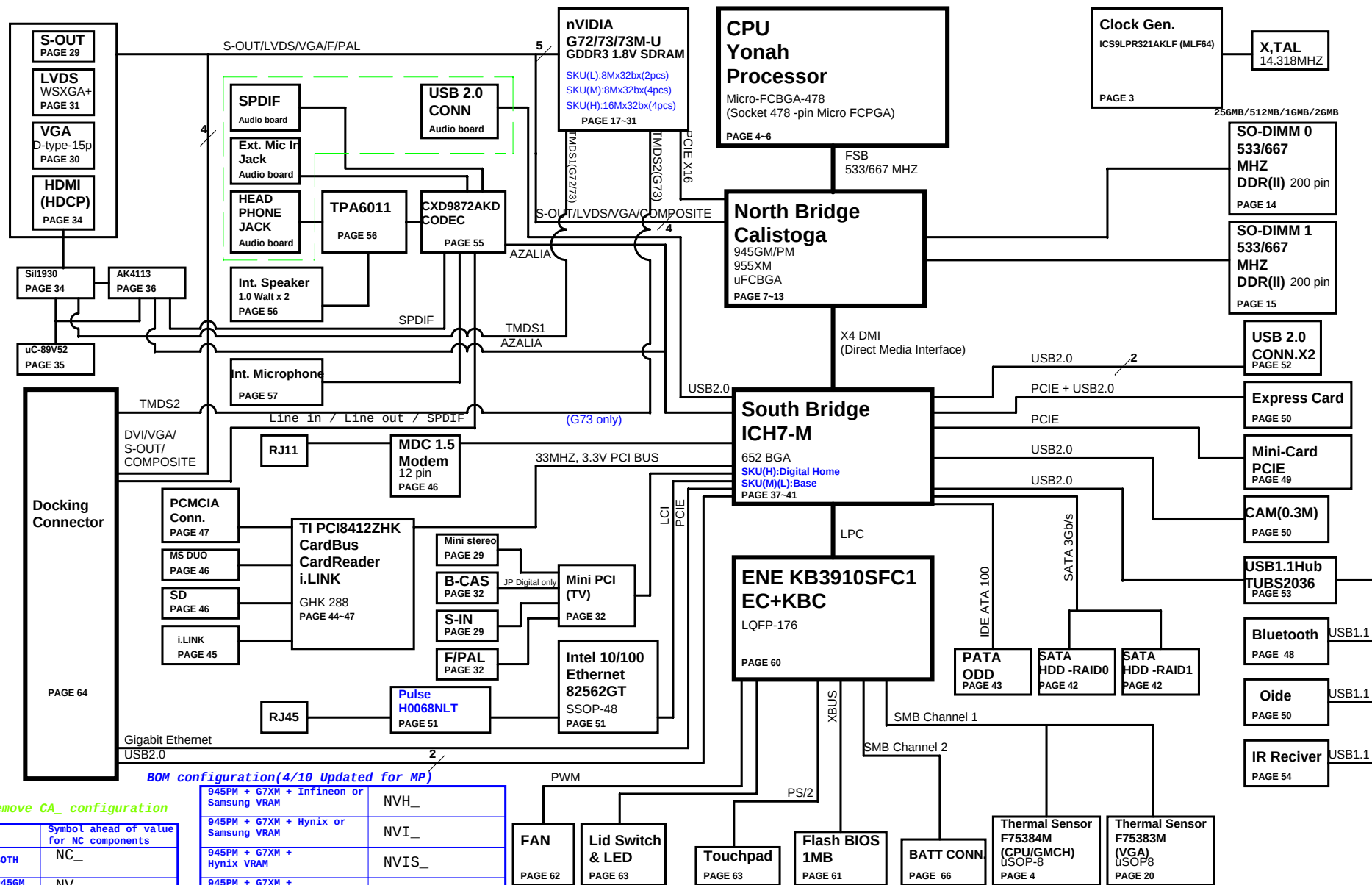
PCB P/N: 1P-0068100-8011 (FUBAI)
1P-0068500-8011 (Hannstar)

P. Leader	Check by	Design by

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
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MS21(CALISTOGA PM+Gfx Block Diagram)

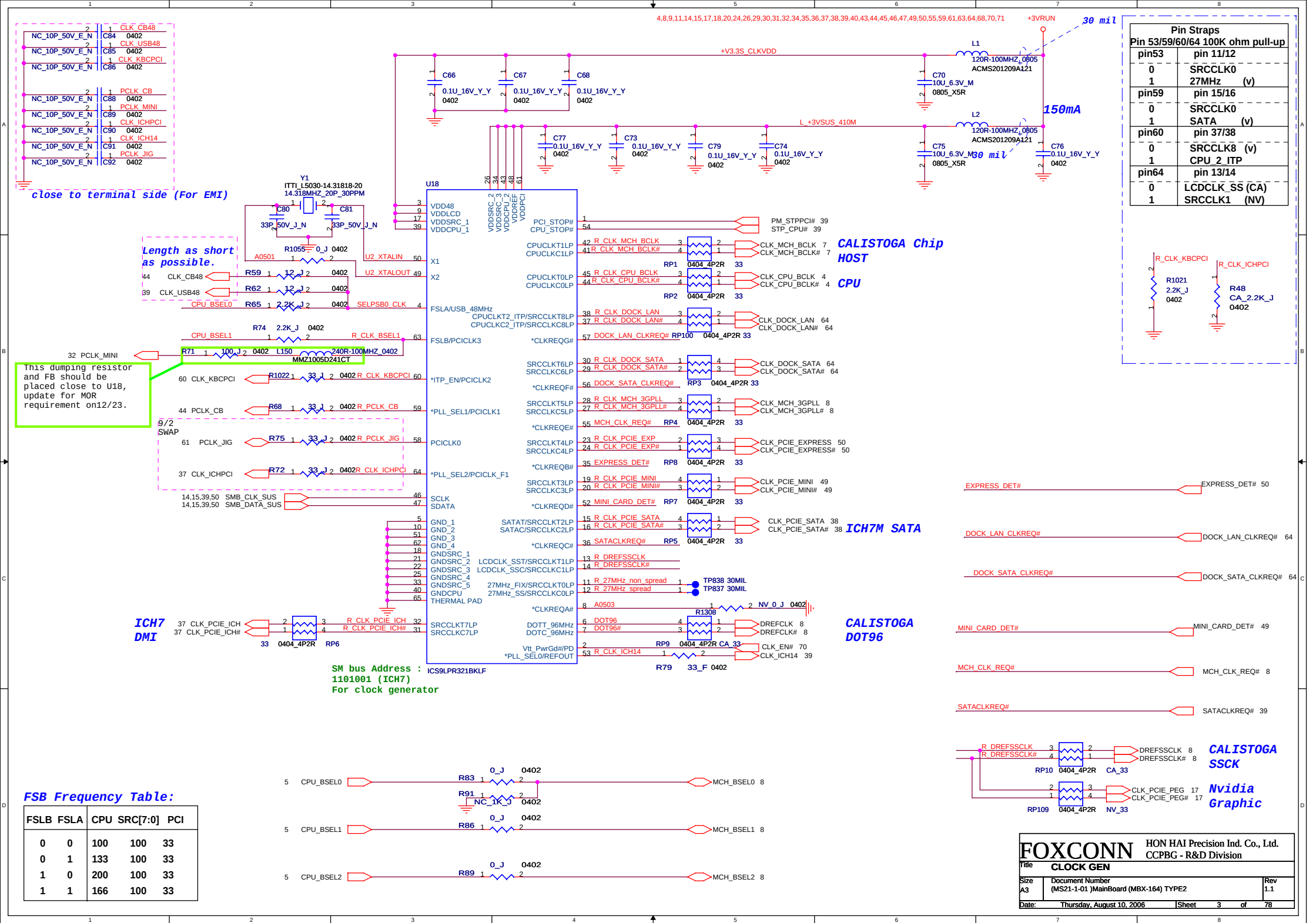
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New modified

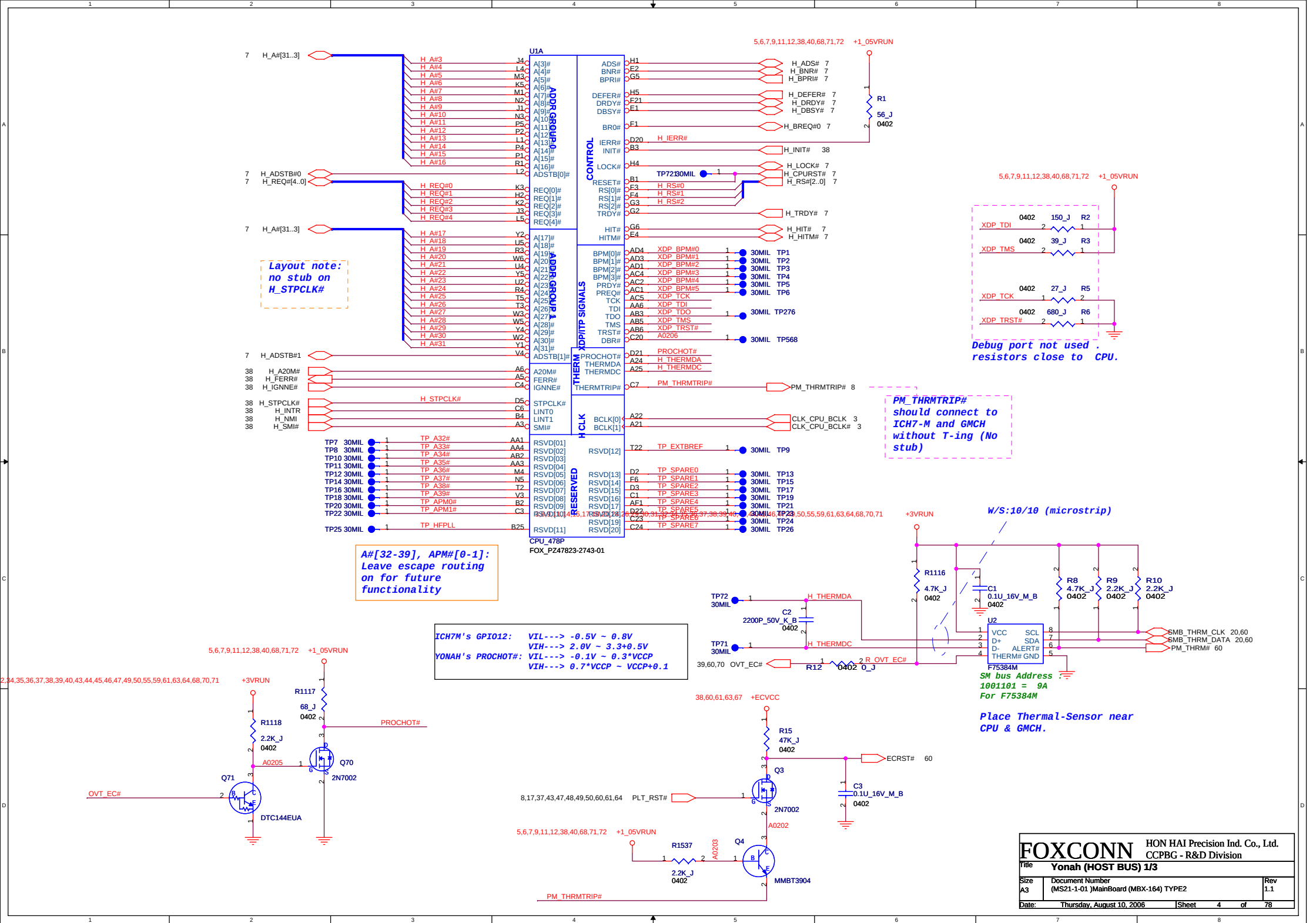


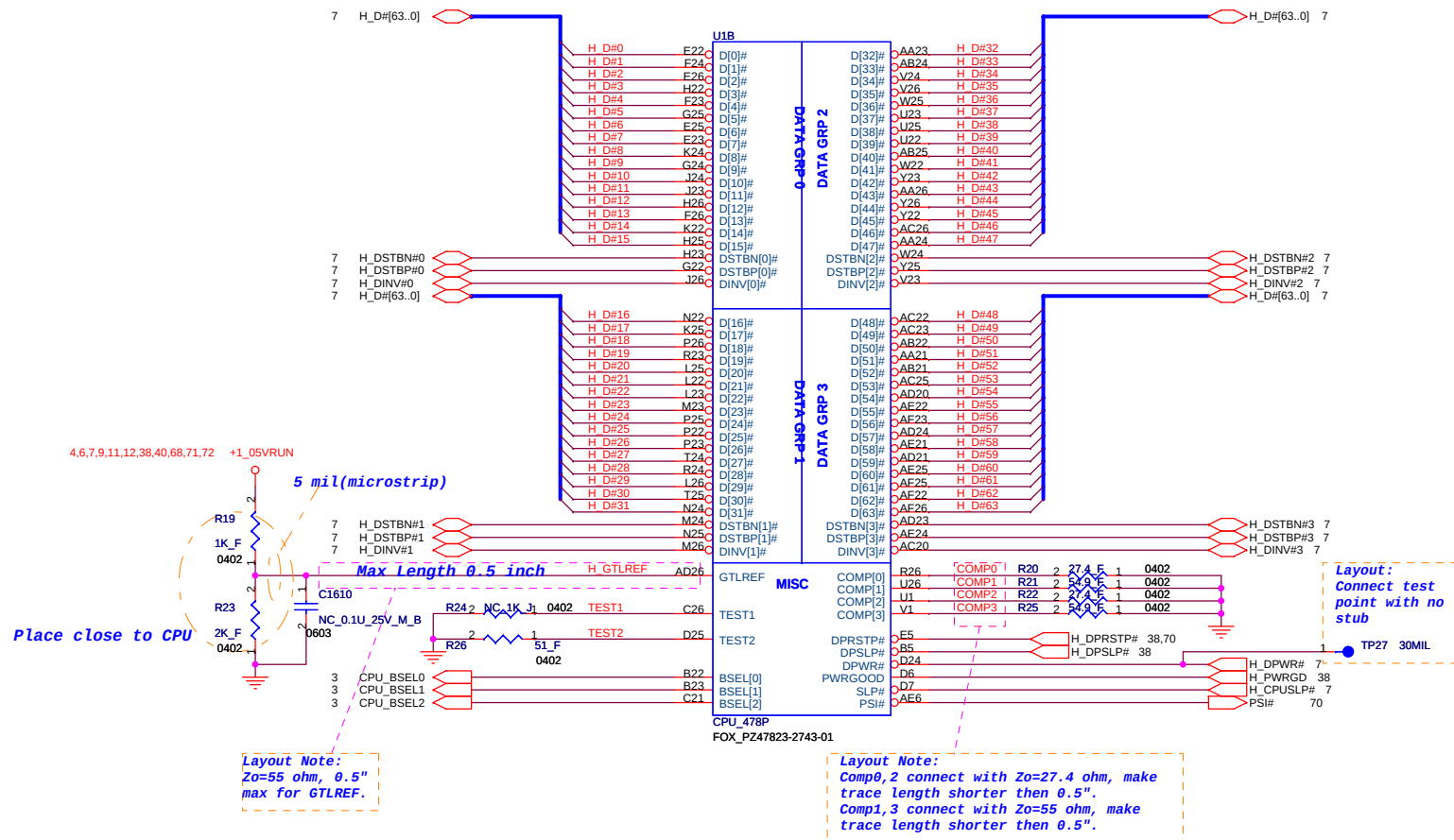
Remove CA configuration

Symbol ahead of value for NC components	
BOTH	NC_
945GM	NV_
945PM + G72M	NV73_
945PM + G73M	NV72_
945PM + G72M or G73M	NV73only_

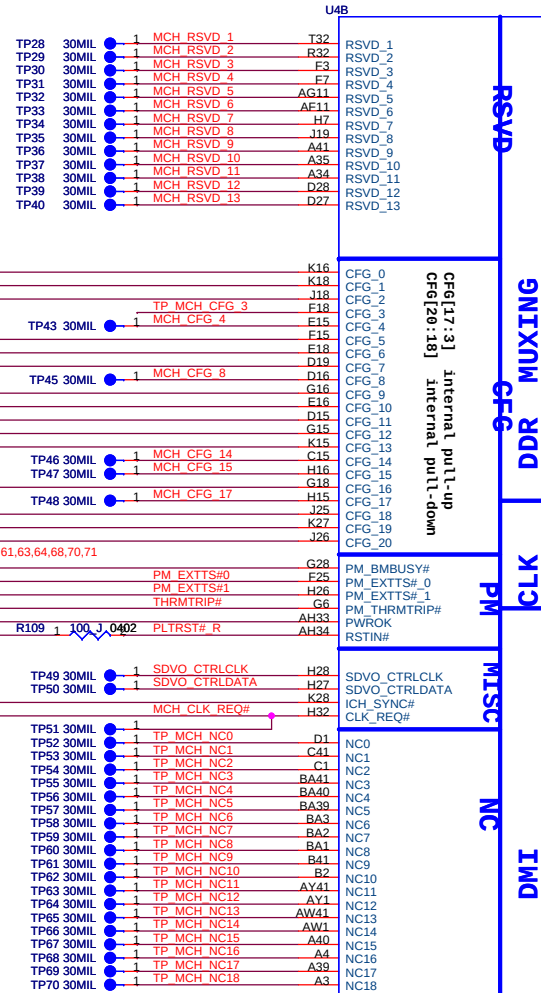
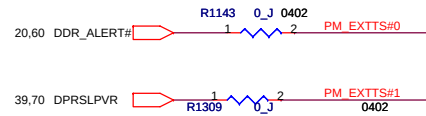
945PM + G7XM + Infineon or Samsung VRAM	NVH_
945PM + G7XM + Hynix or Samsung VRAM	NVI_
945PM + G7XM + Hynix VRAM	NVIS_
945PM + G7XM + Infineon VRAM	NVHS_
945PM + G72M or G73M	NV16M_, NV73U_
945PM + G73M-U	NV8M_, NV7273_
*JP Digital TV Tuner SKU & No Tuner SKU not stick	JDTVNC_



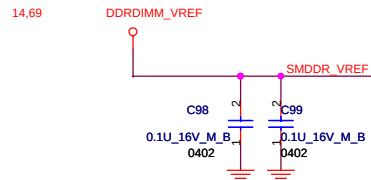
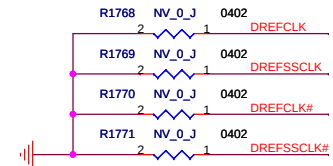


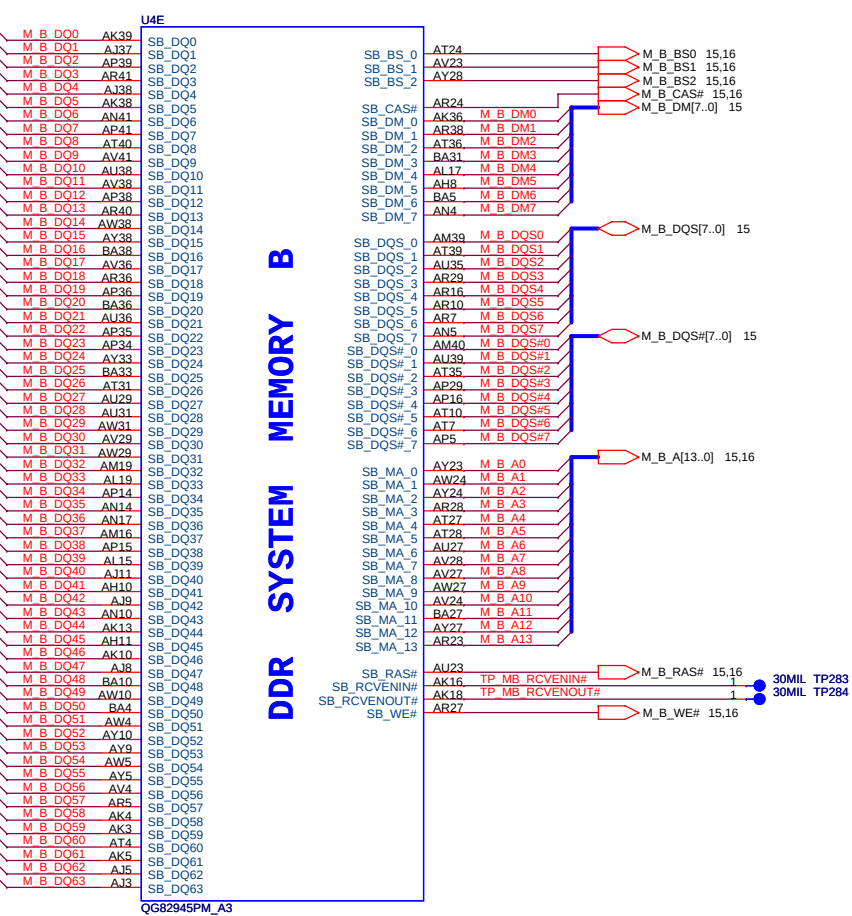
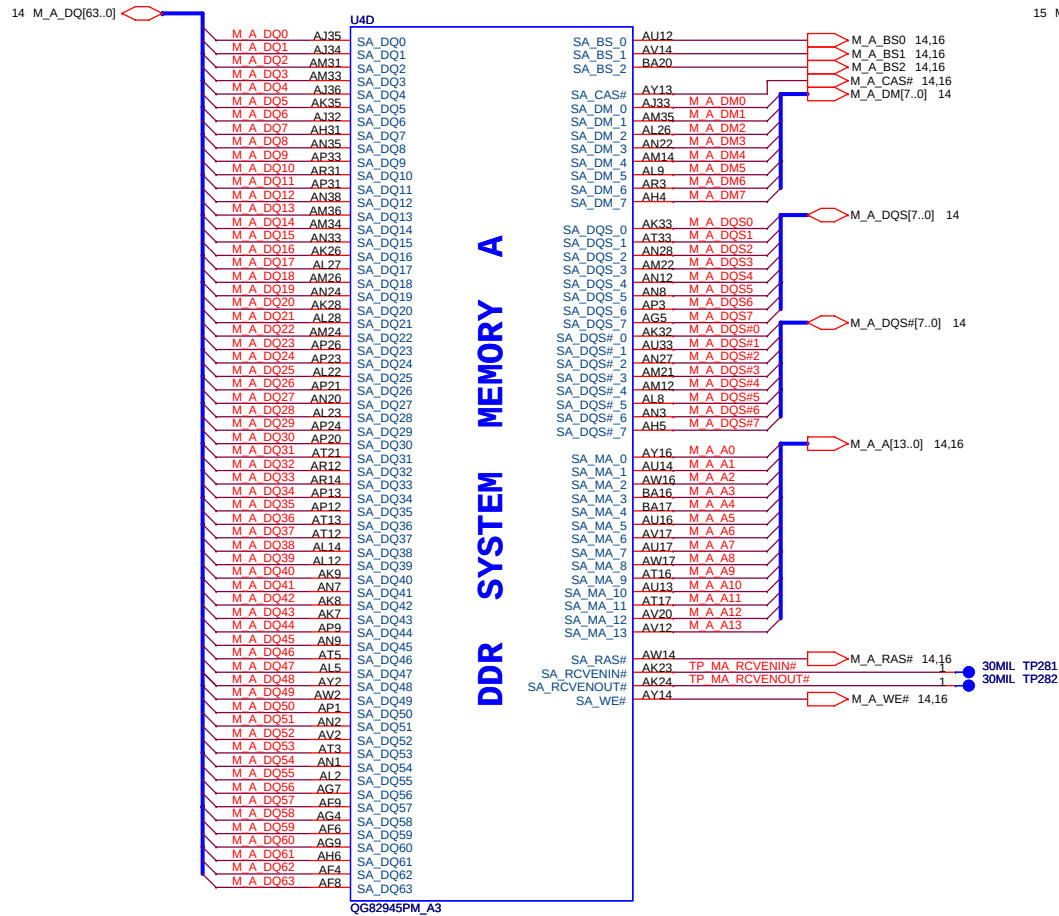


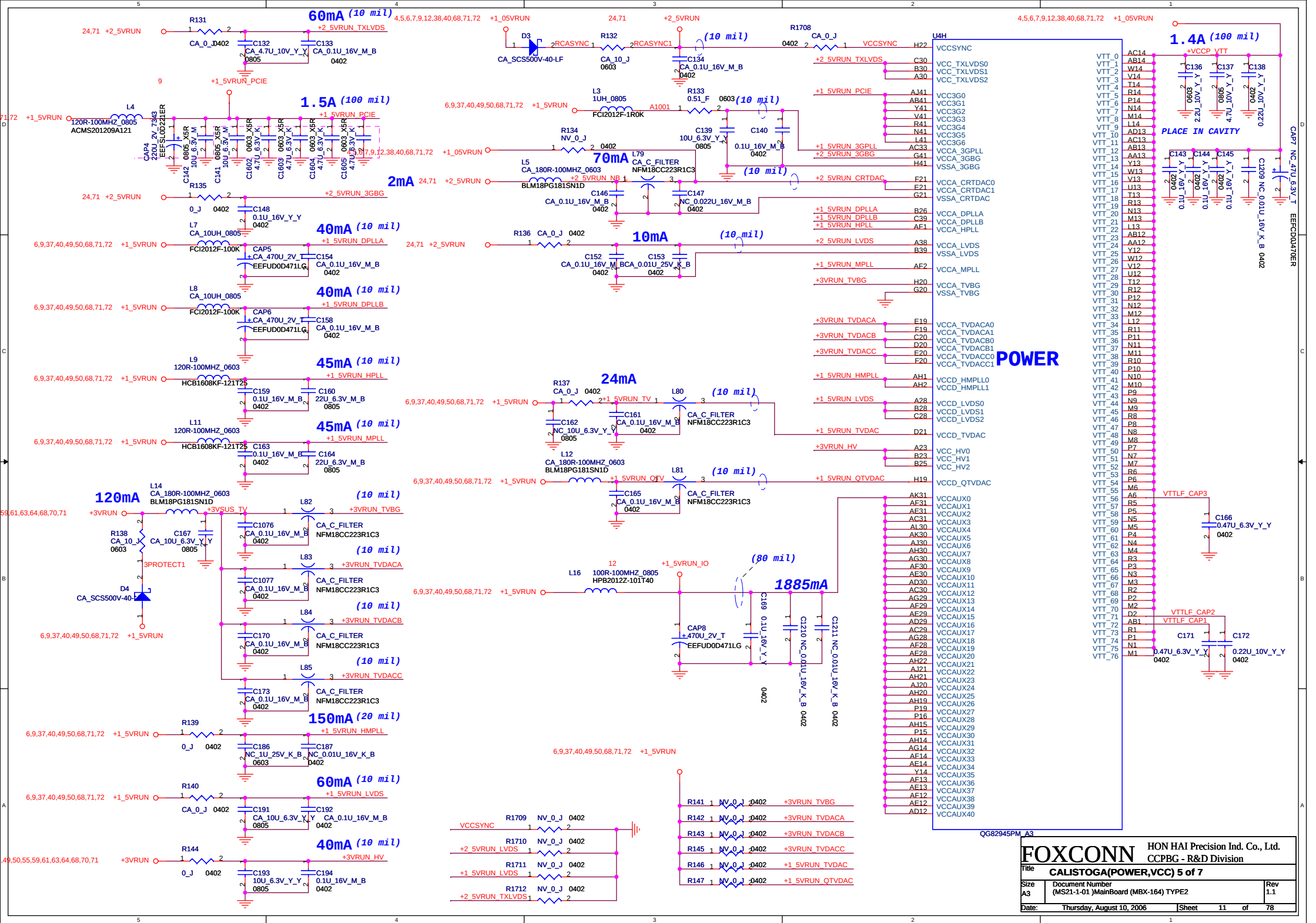
5/5 Remove R110 for PM_EXTTS#1 back up pull up res.
ICH7 (DPRSLPVR) already have internal pull up

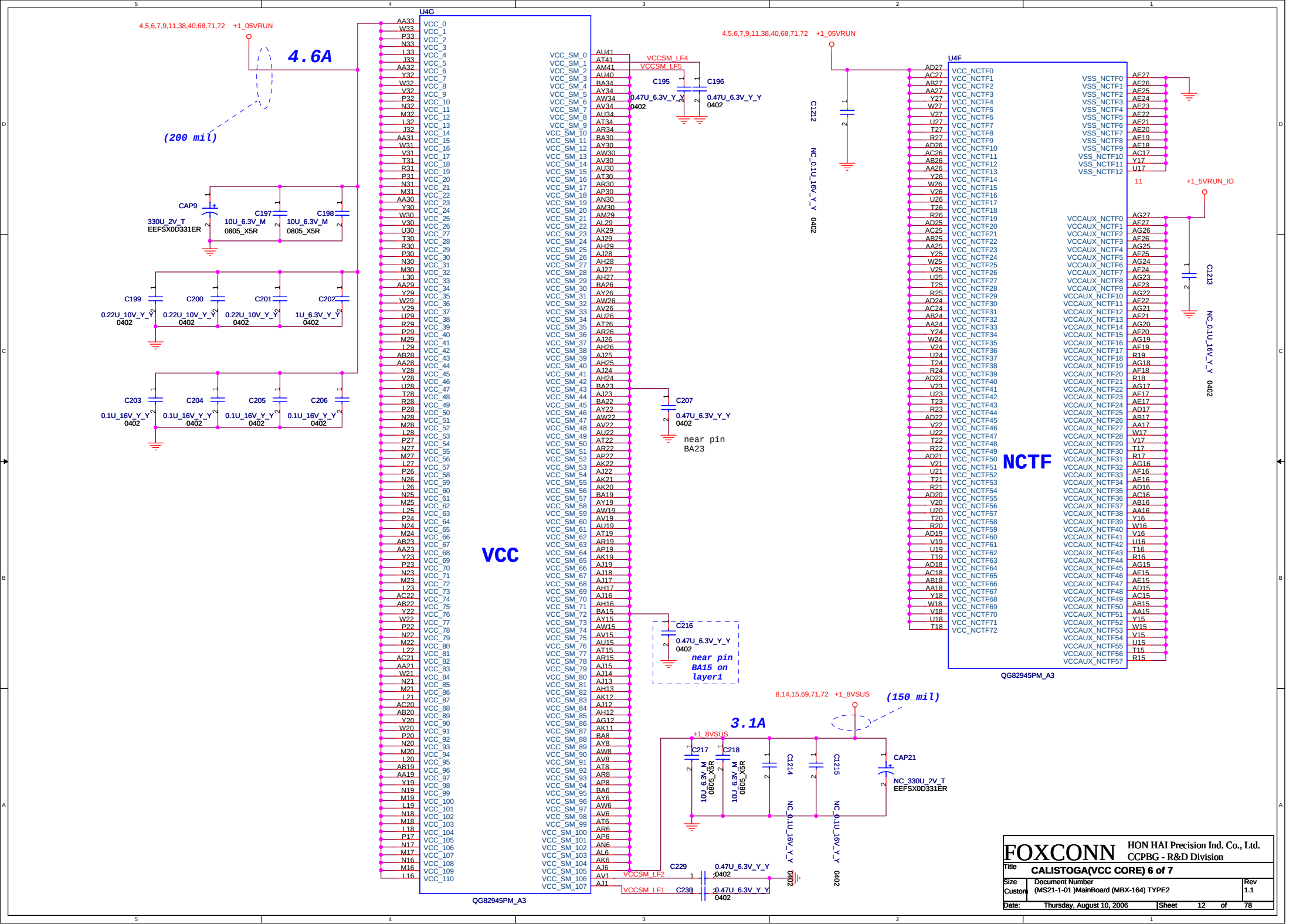


QG82945PM_A3









8 MCH_CFG_5 1 30MIL TP554

MCH_CFG_5 Low = DMIX2 High = DMIX4

8 MCH_CFG_6 1 30MIL TP556

MCH_CFG_6 Low = Moby Dick High = Calistoga DDR2 select (default high)

8 TP_MCH_CFG_7 TP MCH_CFG_7

MCH_CFG_7 (CPU Strap) Low = RSVD High = Mobile Yonah processor

8 MCH_CFG_9 1 30MIL TP559

MCH_CFG_9 (PCIE Graphics Lane) Low = Reverse Lane High = Normal operation For layout convenience

8 MCH_CFG_10 1 30MIL TP560

MCH_CFG_10 (HOST PLL VCC SELECT) Low = RESERVED High = MOBILITY

8 MCH_CFG_11 1 R162 NC 2.2K_1 0402

MCH_CFG_11 (PSB 4x CLK ENABLE) Low = Calistoga High = Reserved

8 MCH_CFG_12 1 30MIL TP562
8 MCH_CFG_13 1 30MIL TP563

MCH_CFG [13:12] 00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)

8 MCH_CFG_16 1 30MIL TP564

MCH_CFG_16 (FSB Dynamic ODT) Low = Dynamic ODT Disabled High = Dynamic ODT Enable

MCH_CFG_18 Low = 1.05V(default) High = 1.5V (VCC_CORE Select)

8 MCH_CFG_18 1 30MIL TP555

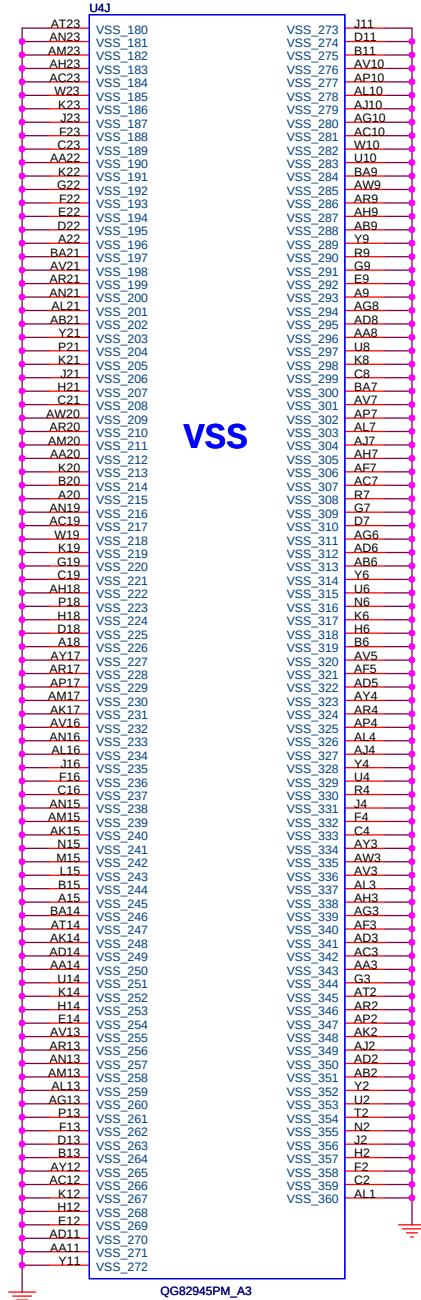
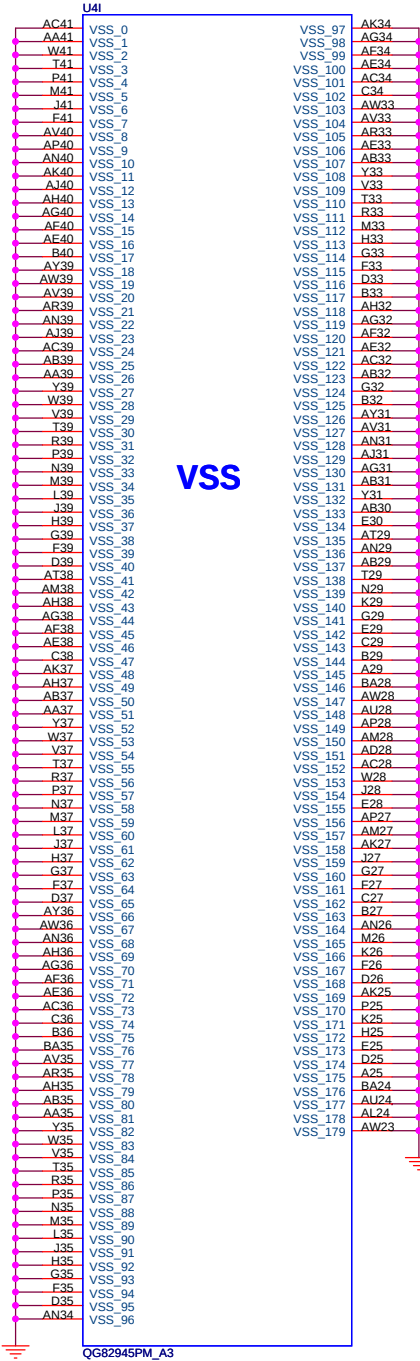
MCH_CFG_19 Low = Normal(default) High = LANES REVERSED (DMI LANE REVERSAL)

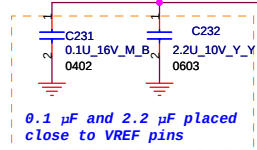
8 MCH_CFG_19 1 30MIL TP558

MCH_CFG_20 Low = Only SDVO or PCIE x1 is operational (defaults) High = SDVO and PCIE x1 are operating simultaneously via the PEG port (PCIE Backward Interoperability mode)

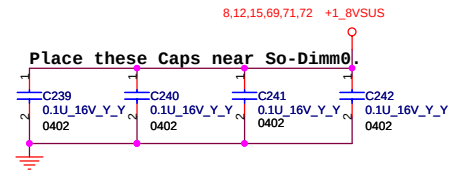
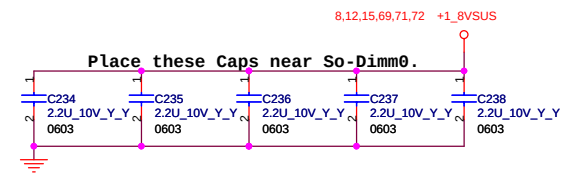
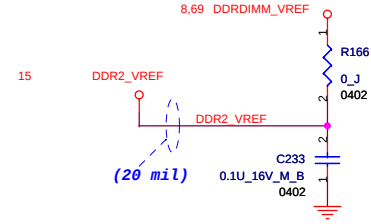
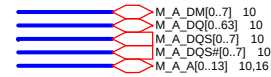
8 MCH_CFG_20 1 30MIL TP561

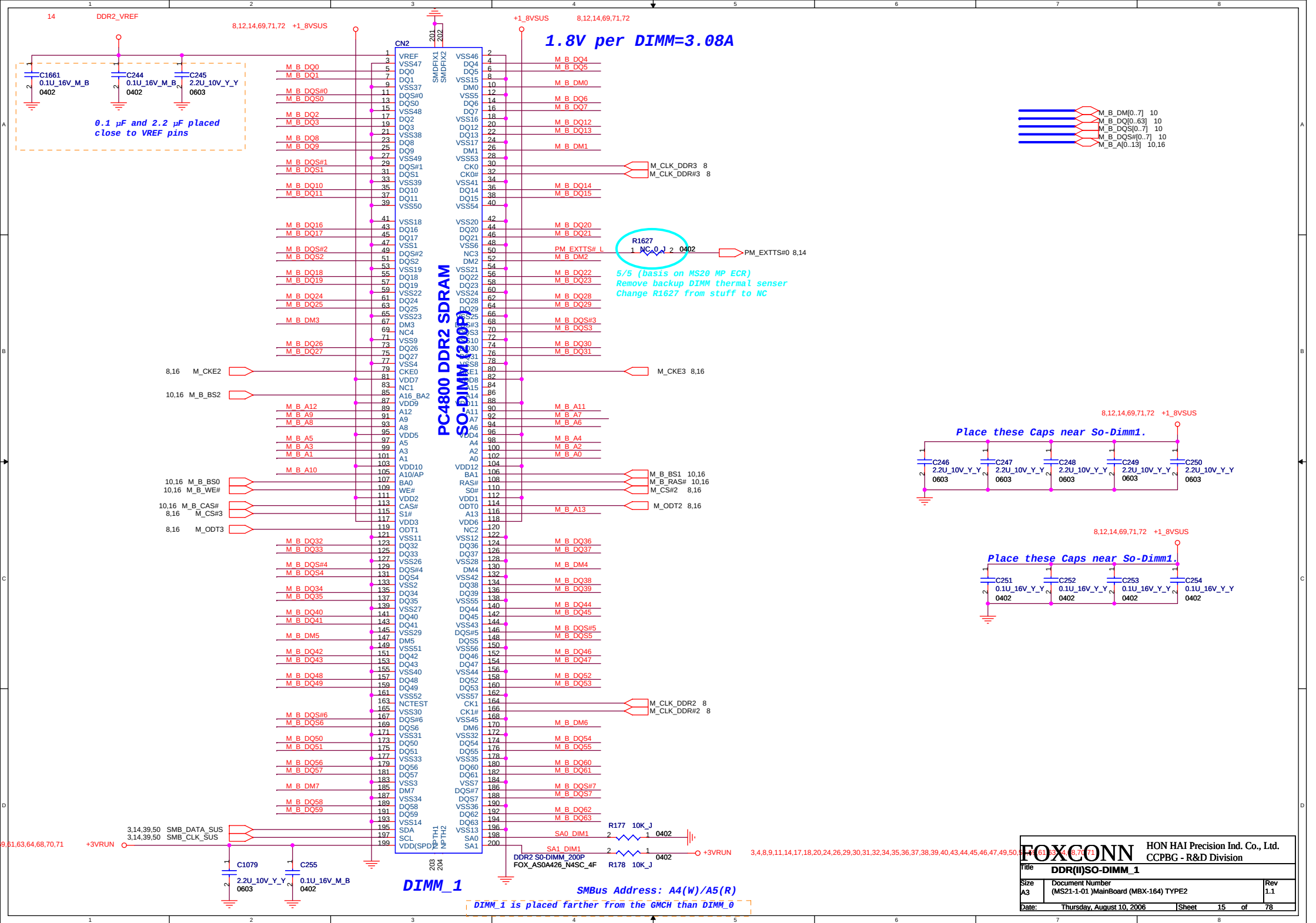
Layout Noe: Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub





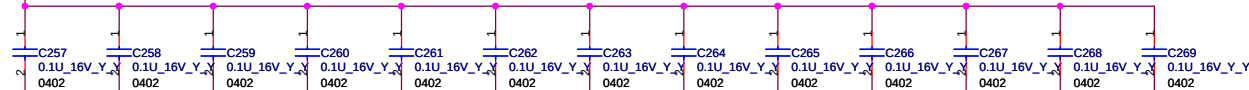
1.8V per DIMM=3.08A





69,72

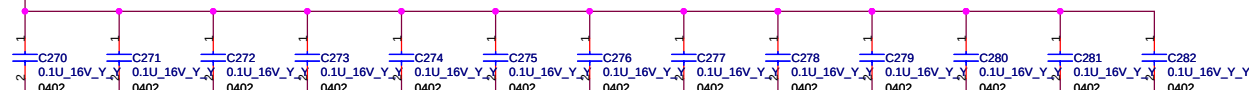
+0_9VSUS



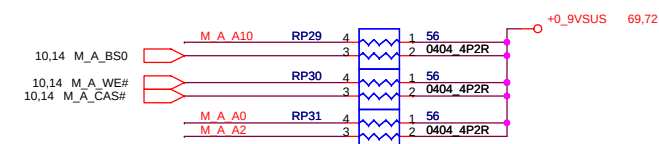
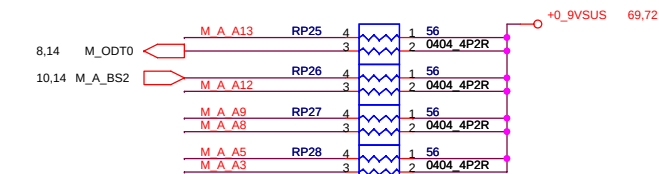
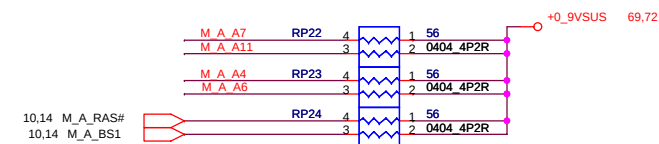
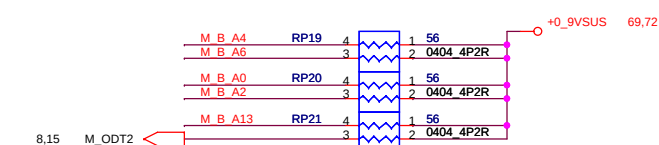
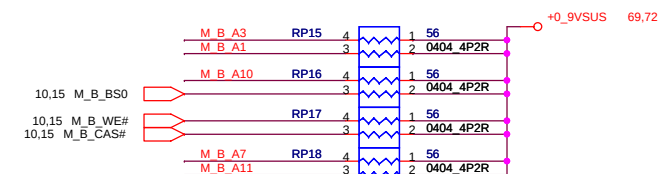
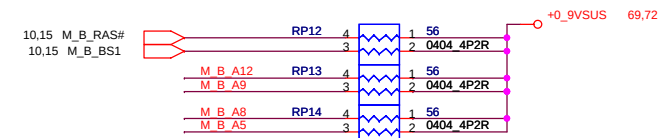
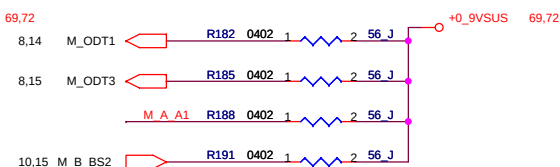
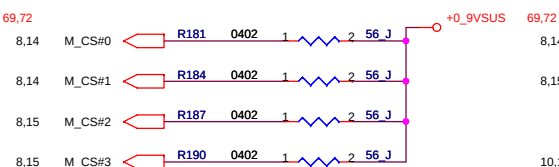
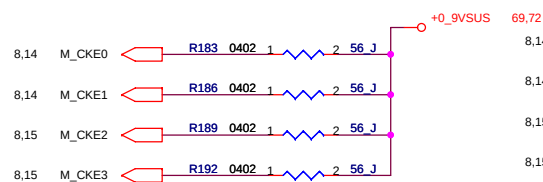
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS

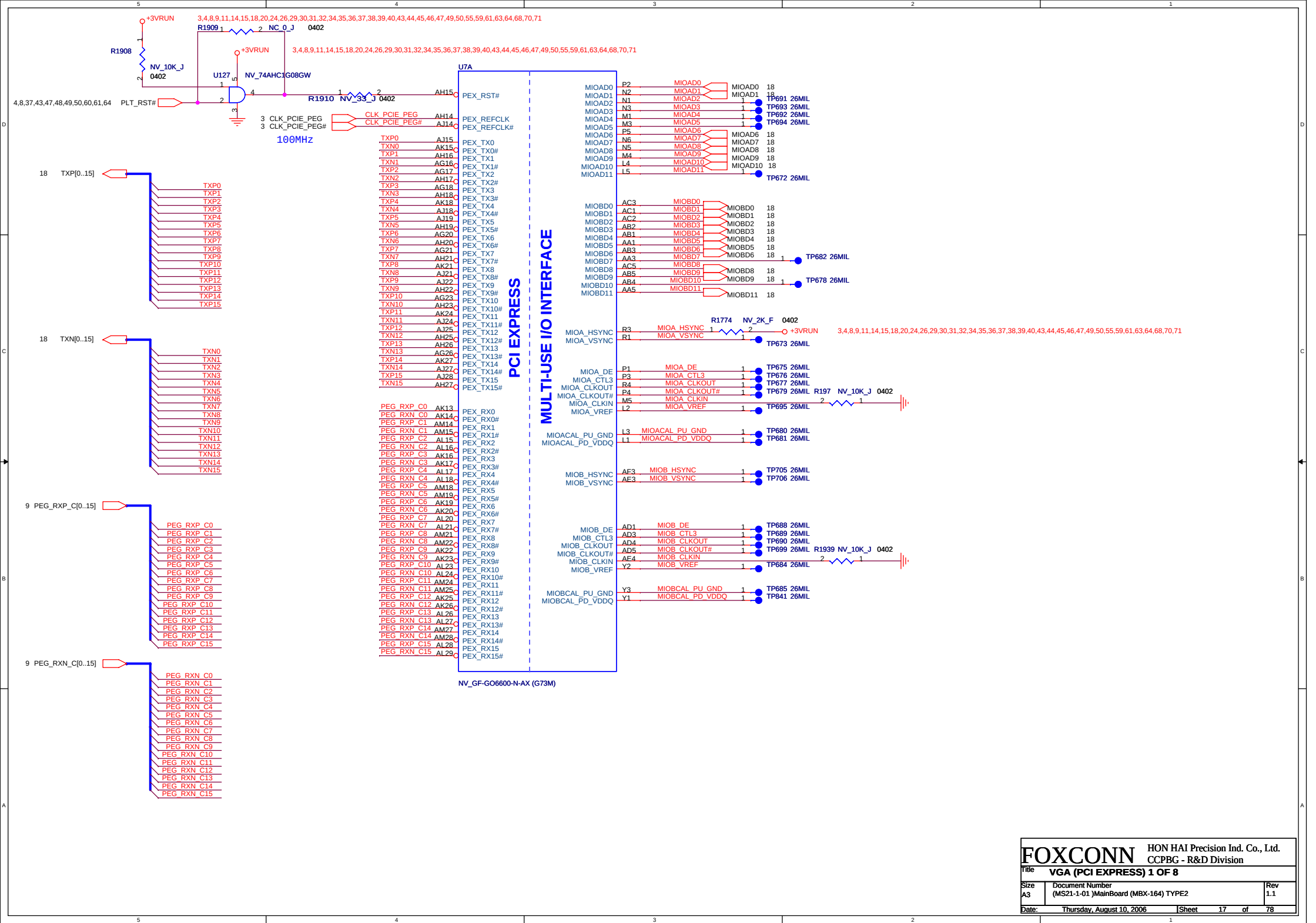
69,72

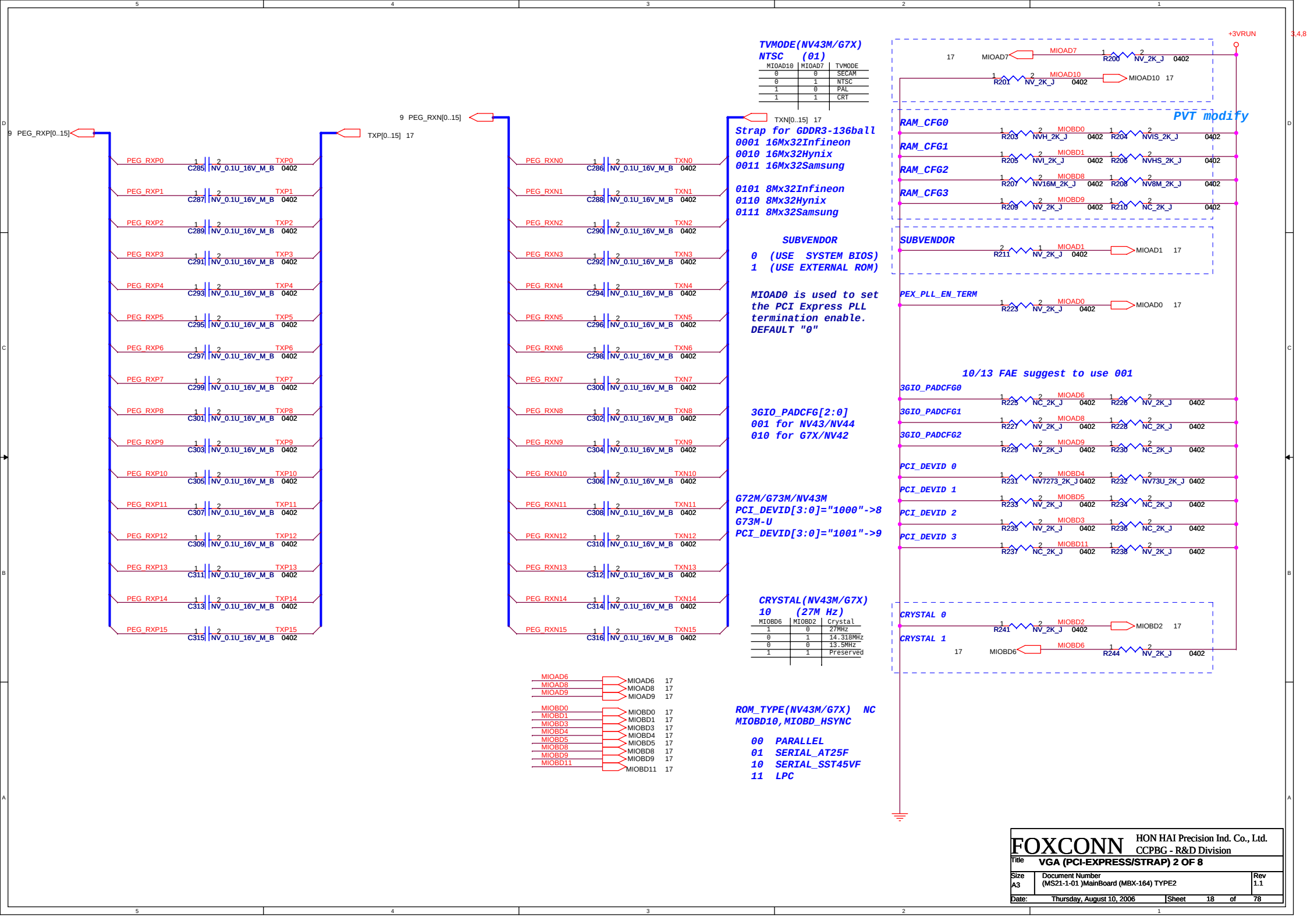
+0_9VSUS

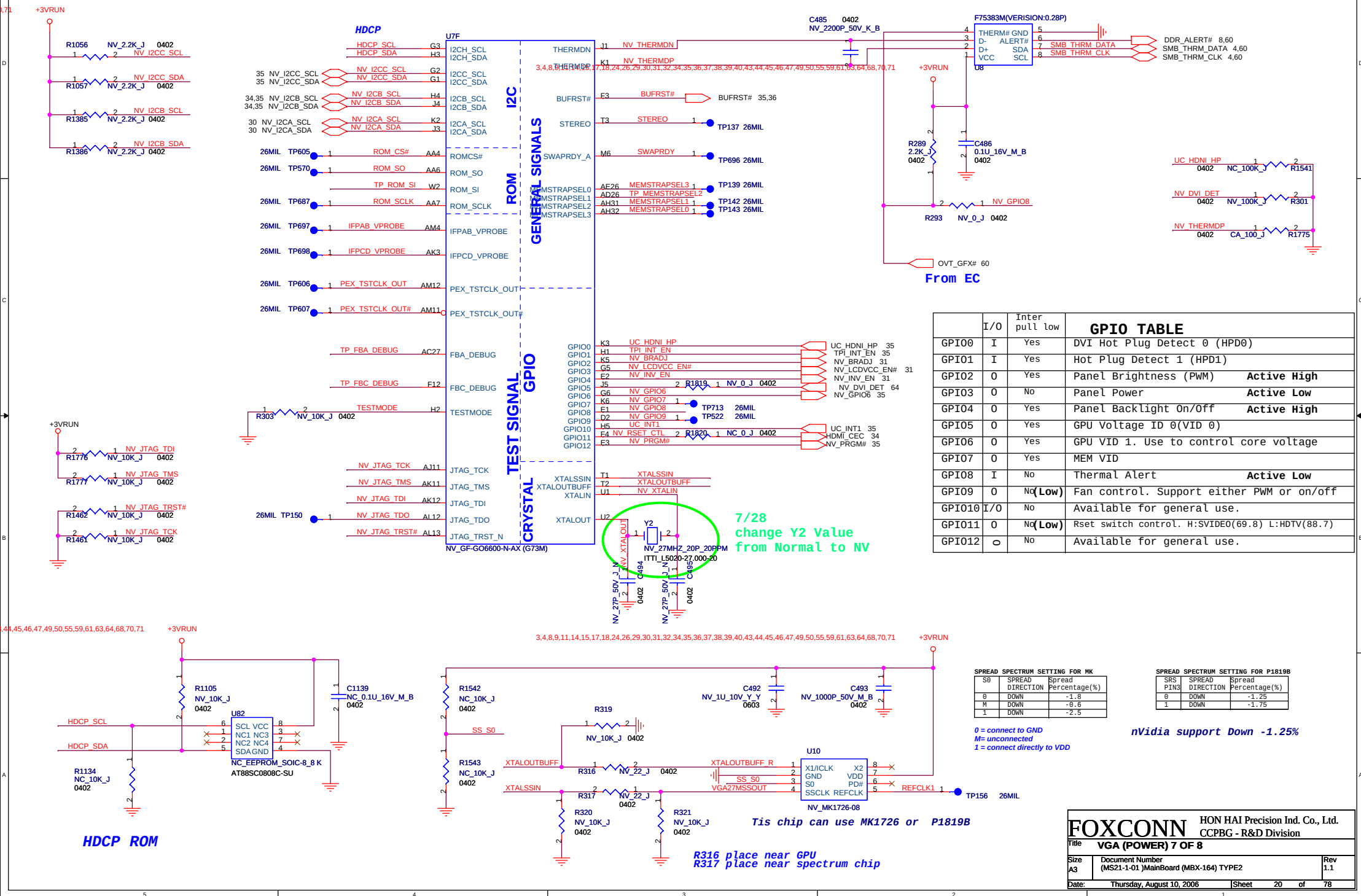


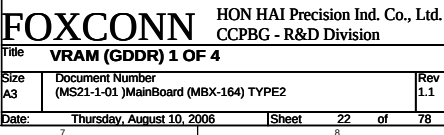
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS

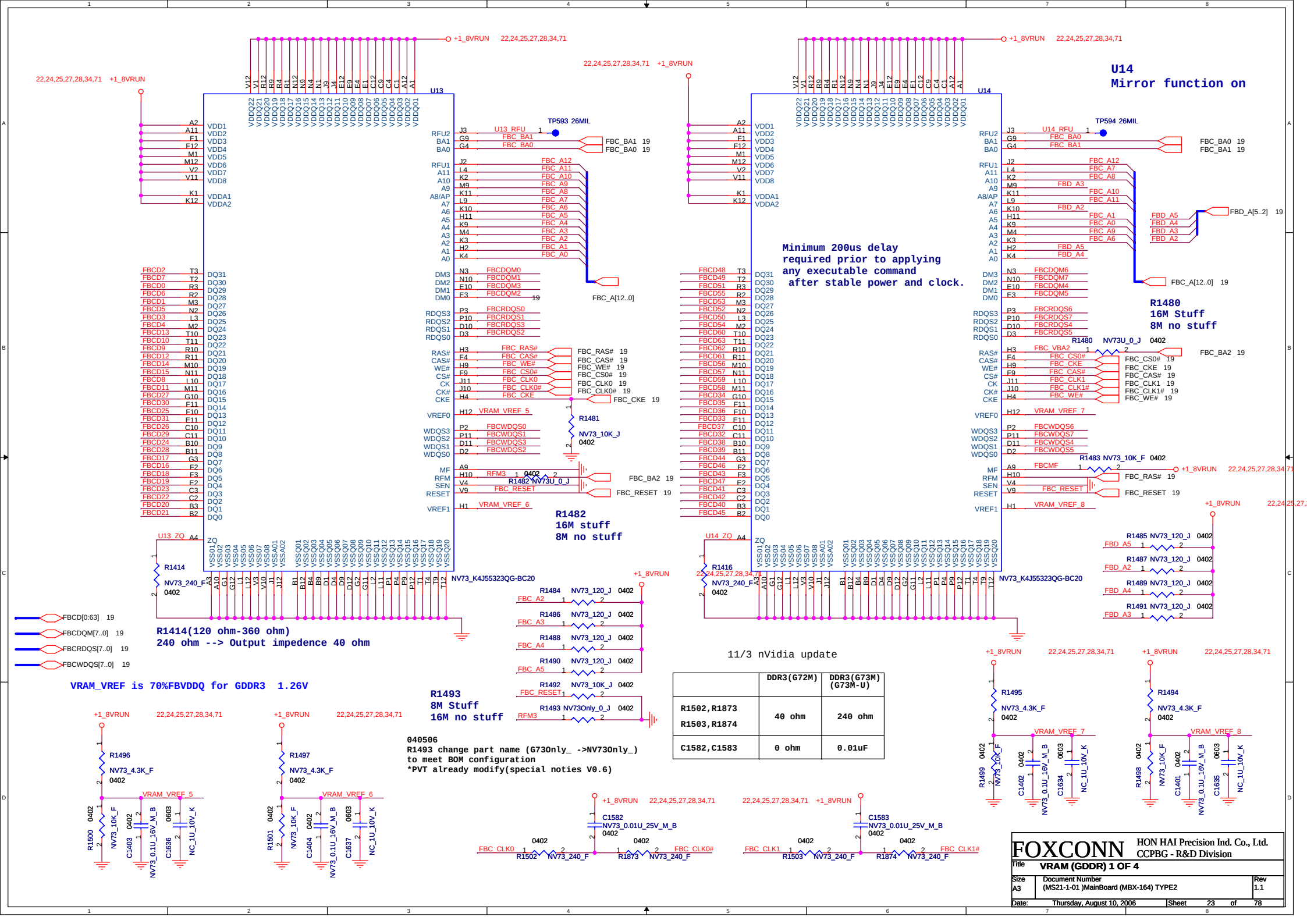


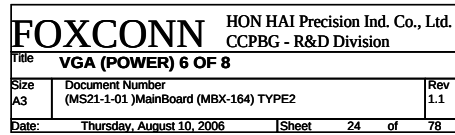












U71



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title VGA (POWER) 5 OF 8			
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1	
Date:	Thursday, August 10, 2006	Sheet	25 of 78

25,72,73

1.2V
PEX_VDD

250mA

25,72,73

1.2V
PEX_VDD

1420mA (I/O Power)

25,72,73

1.2V
PEX_VDD

100mA(Analog Power)

25,72,73

1.2V
PEX_VDD

20mA(Power rail)

1.025V
NV_VDD

(Secondary internal core power)

49,50,55,59,61,63,64,68,70,71

+3VRUN

110mA(3.3V Power rail GPIO,I2C,GPU DIGITAL LOGIC)

G3 design guide require
that PEX_IOVDD/Q directly connect to
PEX_VDD on page 16.

U7B

AD23 PEX_IOVDD0
AE24 PEX_IOVDD1
AE23 PEX_IOVDD2
AG24 PEX_IOVDD3
AG25 PEX_IOVDD4
AG25 PEX_IOVDD5

AC16 PEX_IOVDDQ0
AC17 PEX_IOVDDQ1
AC21 PEX_IOVDDQ2
AC22 PEX_IOVDDQ3
AE18 PEX_IOVDDQ4
AE22 PEX_IOVDDQ5
AE12 PEX_IOVDDQ6
AE18 PEX_IOVDDQ7
AE21 PEX_IOVDDQ8
AE22 PEX_IOVDDQ9
AE22 PEX_IOVDDQ10

POWER

NV_GF-G0600-N-AX (G73M)

8mA(Frame Buffer Analog Power)

1.2V
PEX_VDD

Place close to L102

16.25A(Internal logic core power)

G72M 1.1V
G73M 1.1V
G73M-U 1.2V

CRB circuit 050611

VDD0 K16
VDD1 K17
VDD2 N13
VDD3 N14
VDD4 N16
VDD5 N17
VDD6 N19
VDD7 P13
VDD8 P14
VDD9 P16
VDD10 P17
VDD11 P19
VDD12 P19
VDD13 R16
VDD14 R17
VDD16 T15
VDD17 T18
VDD18 T19
VDD19 T19

VDD20 U13
VDD21 U14
VDD22 U15
VDD23 U18
VDD24 U19
VDD25 V16
VDD26 V17
VDD27 W13
VDD28 W14
VDD29 W16

VDD30 U13
VDD31 W19
VDD32 Y13
VDD33 Y14
VDD34 Y16
VDD35 Y17
VDD36 Y19
VDD37 Y20

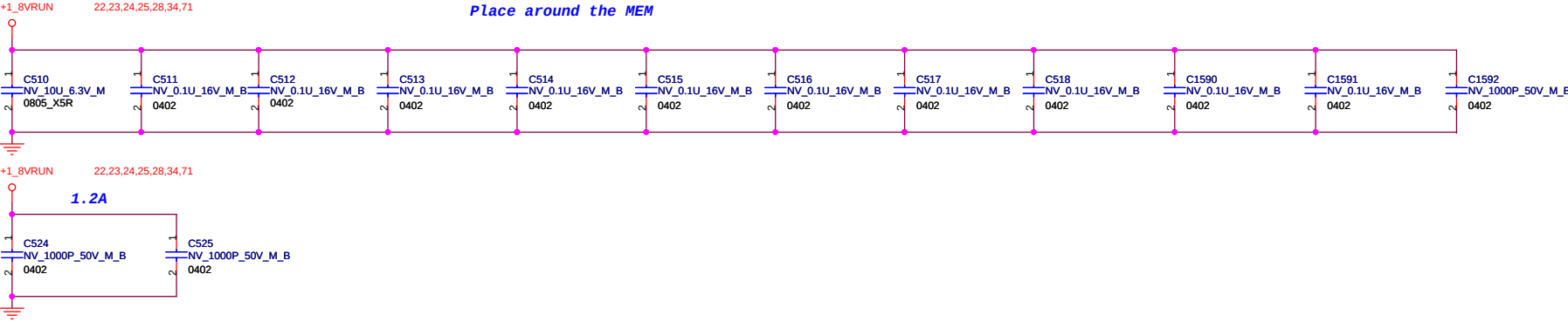
NC13 U4
NC14 V4
NC15 V6
NC16 C20
NC17 W3
NC18 V1
NC19 Y5
NC20 W1
NC21 W4
NC22 W5
NC23 Y6
NC24 W6
NC25 F6
NC26 G8
NC27 G23
NC28 A28
NC29 F1
NC30 A26
NC31

NFNC13 1 TP614 26MIL
NFNC14 1 TP613 26MIL
NFNC15 1 TP616 26MIL
NFNC16 1 TP615 26MIL
NFNC17 1 TP618 26MIL
NFNC18 1 TP617 26MIL
NFNC19 1 TP620 26MIL
NFNC20 1 TP622 26MIL
NFNC21 1 TP623 26MIL
NFNC22 1 TP625 26MIL
NFNC23 1 TP627 26MIL
NFNC24 1 TP631 26MIL
NFNC25 1 TP630 26MIL
NFNC26 1 TP633 26MIL

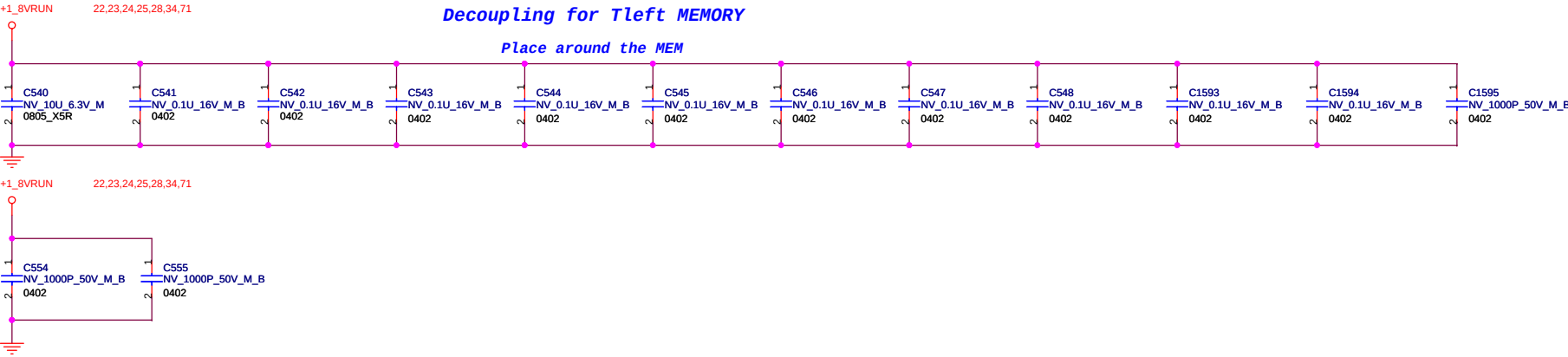
TP_FBC_PLLVDD 1 TP586 26MIL
FBA_PLLVDD 1 TP587 26MIL
FB_VREF2 1 TP590 26MIL
STRAP 1
TESTMEMCLK 1 2

G73M Pin A26-NC
G72M Pin A26 need stuff R305 10K

Decoupling for Tright MEMORY
Place around the MEM

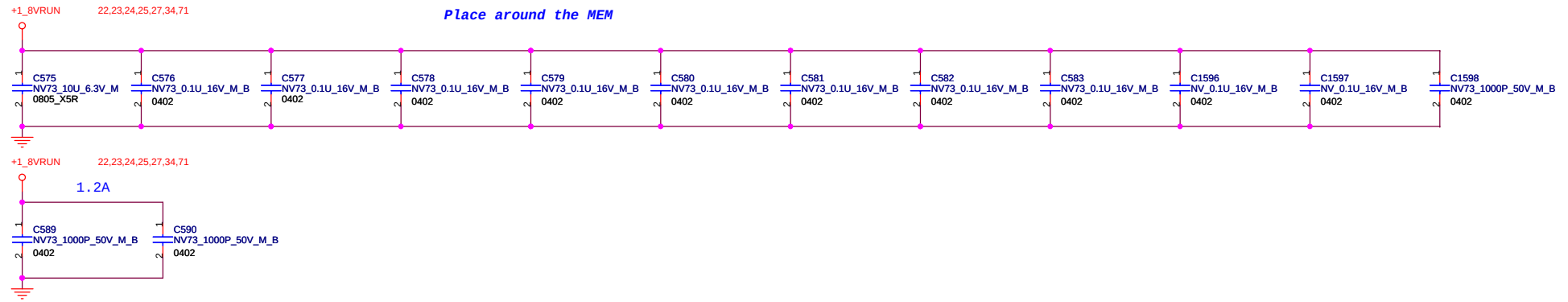


Decoupling for Tleft MEMORY
Place around the MEM



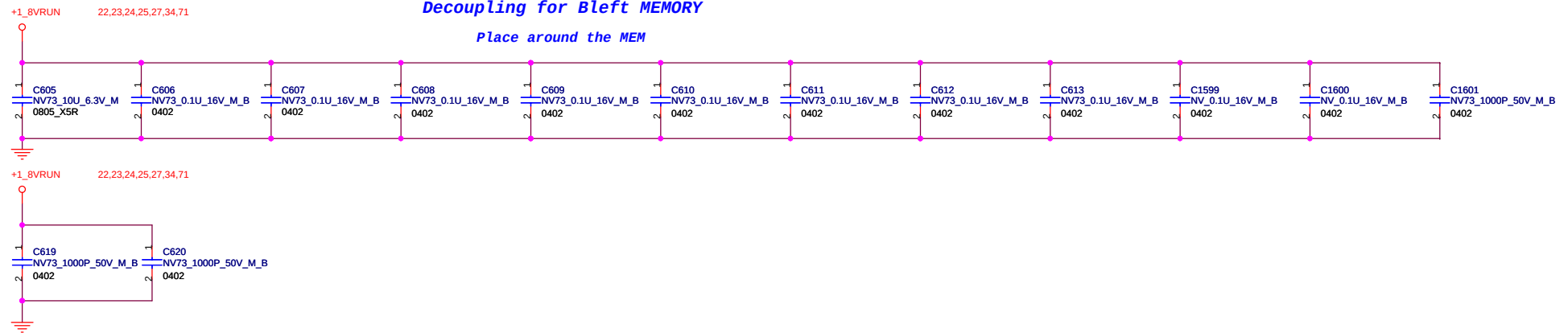
Decoupling for Bright MEMORY

Place around the MEM



Decoupling for Bleft MEMORY

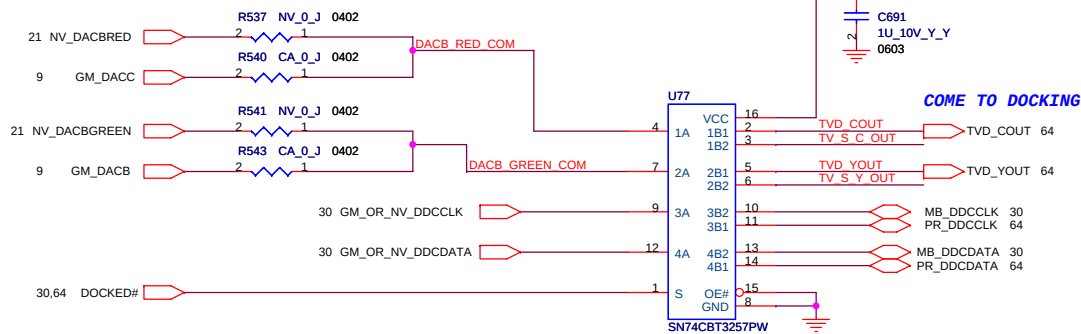
Place around the MEM



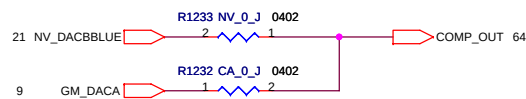
S-VIDEO ANALOG SWITCH

H : S-VIDEO&CVBS
L : PORT REPLICATOR

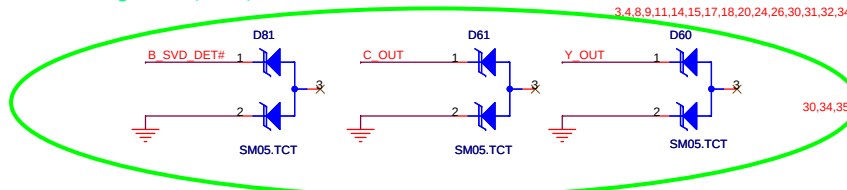
30,34,35,38,40,42,43,47,55,56,57,61,63,70,71,73,74



COME TO DOCKING



2006/8/7
change D60,D61,D81 Value from NV to Normal

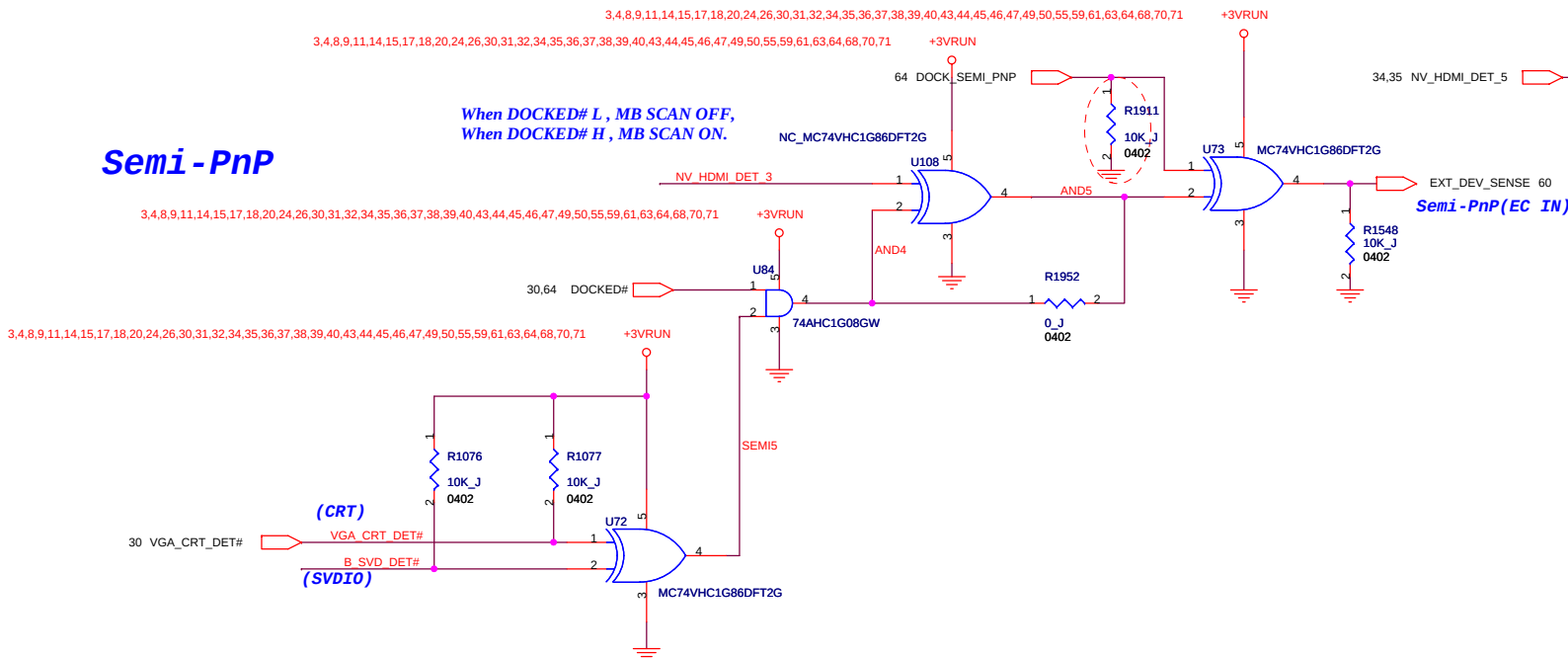


3,4,8,9,11,14,15,17,18,20,24,26,30,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71

3,4,8,9,11,14,15,17,18,20,24,26,30,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71

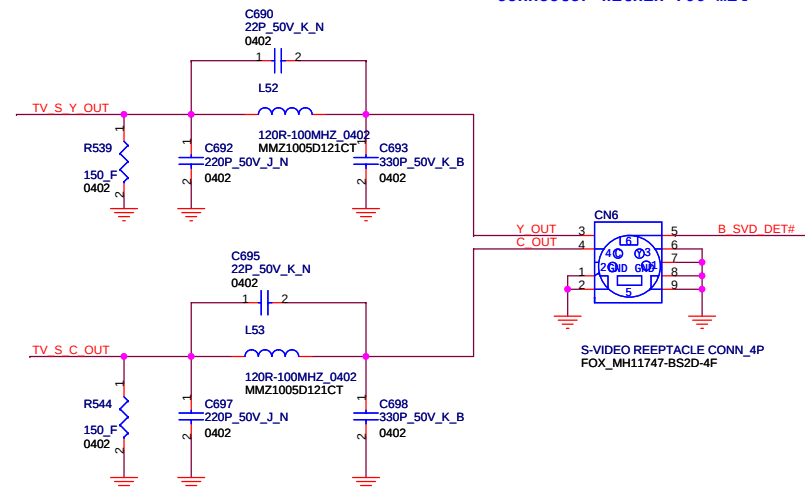
When DOCKED# L, MB SCAN OFF,
When DOCKED# H, MB SCAN ON.

Semi-PnP

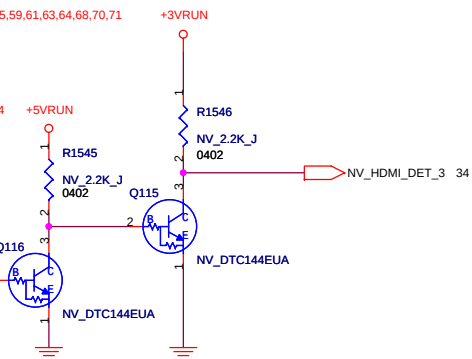


S-VIDEO

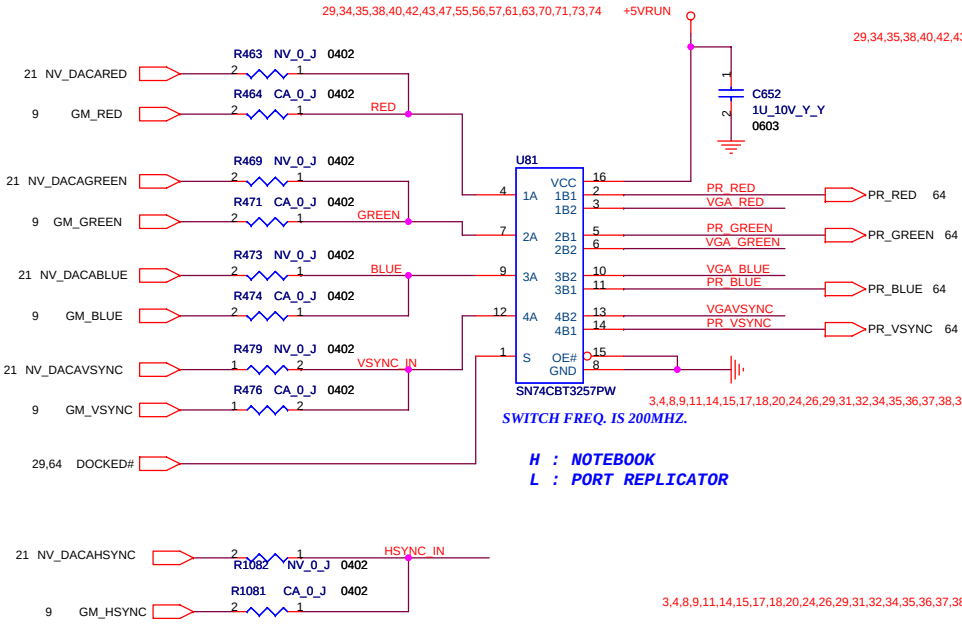
These compoent close to S-Video
connector within 700 mil



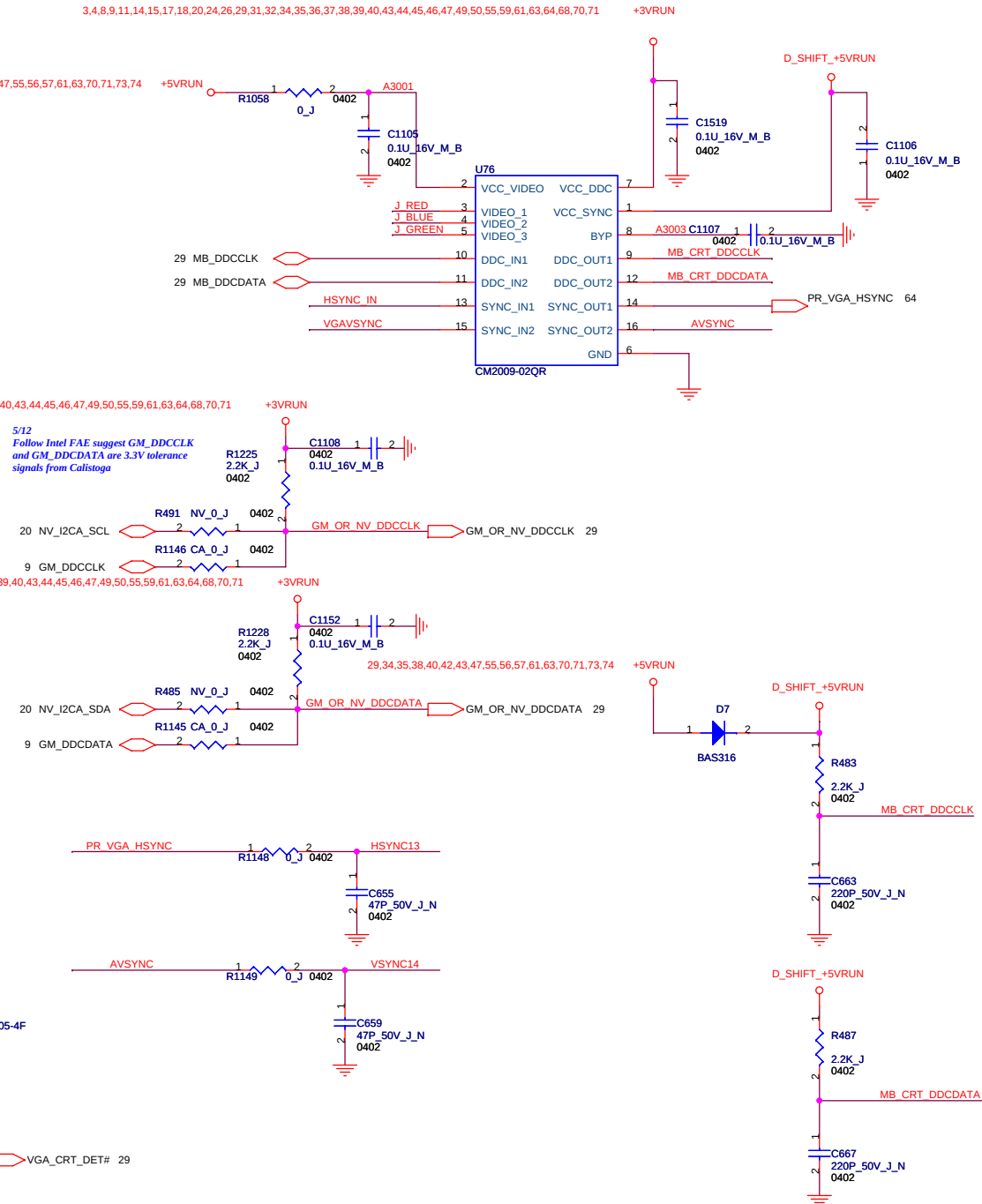
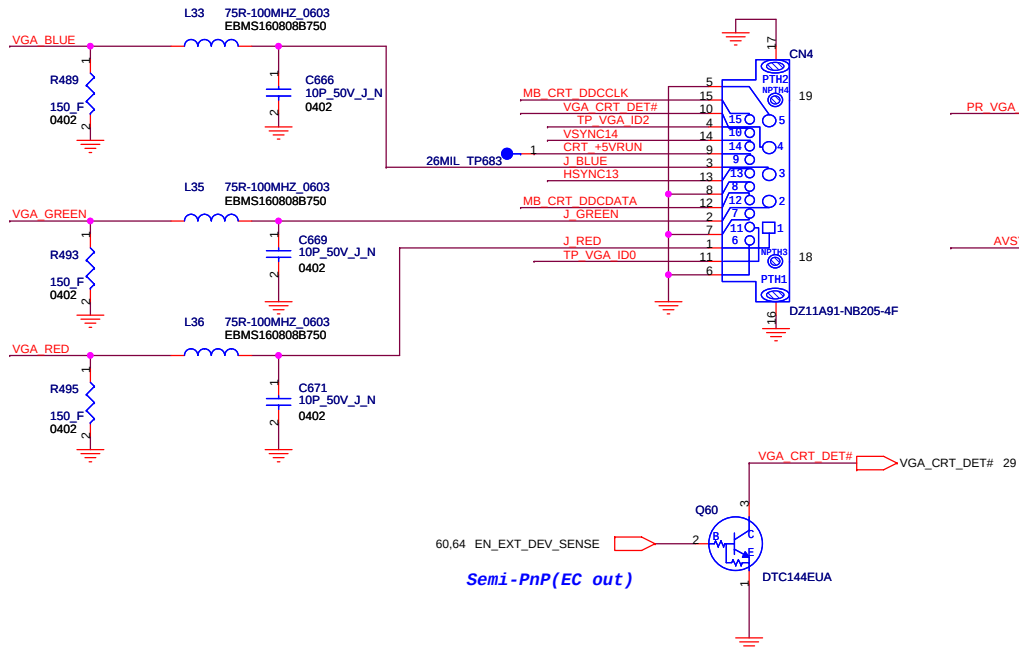
S-VIDEO REEPTACLE CONN_4P
FOX_MH11747-BS2D-4F



CRT ANALOG SWITCH



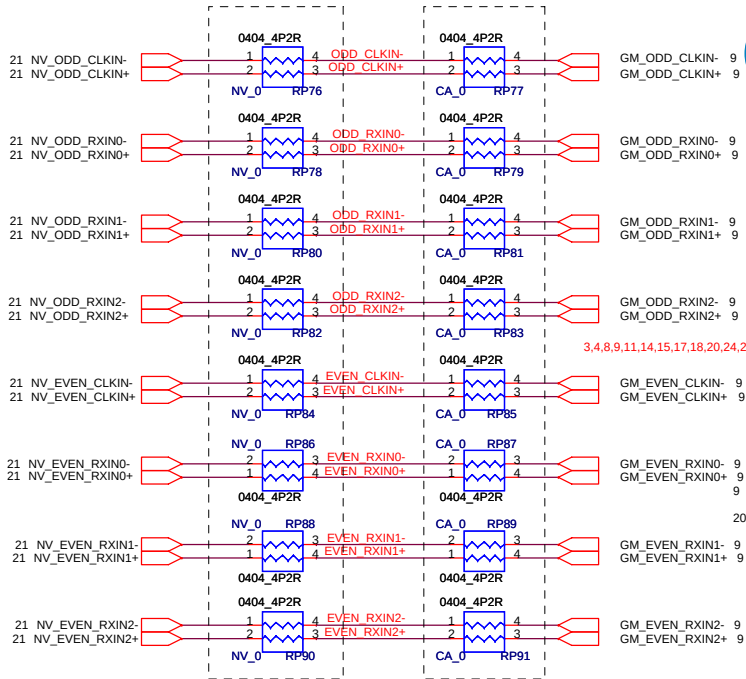
CRT CONNECTOR



LVDS

Group1

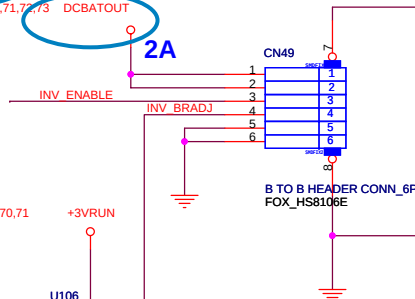
Group2



2006/6/26
(Del inverter boost circuit, after change, the inverter circuit is the same with MS20 MP)
Detail change list
Delete PR426&PR427 and change
C604-1, C1557-1, C1558-1, CN49pin1, pin2
net name INVERTER_VCC to net DCBATOUT.

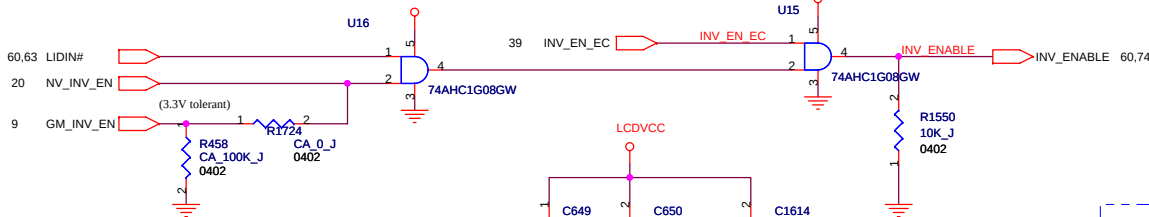
Place C640 and C1558 close to CN49.

66,67,68,69,70,71,72,73 DCBATOUT



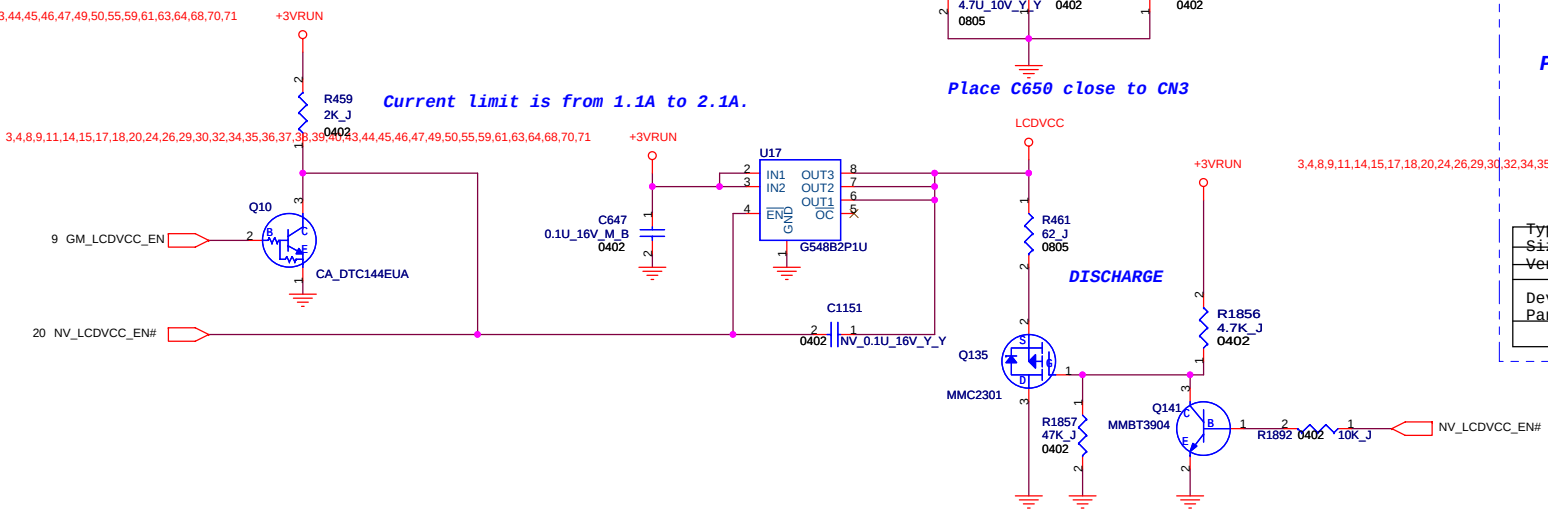
U106,U15,U16 can use QN (MC74VHC1G08DFT2G)
H.H. PN:14-MC74VHC-1G04

3,4,8,9,11,14,15,17,18,20,24,26,29,30,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71



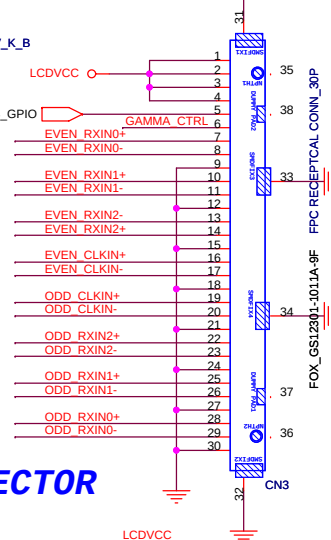
Place C650 close to CN3

DISCHARGE



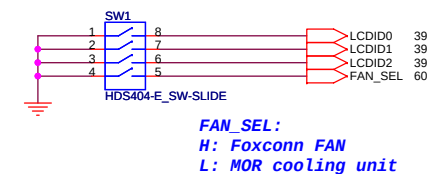
Current limit is from 1.1A to 2.1A.

LVDS CONNECTOR



INVERTER CONNECTOR

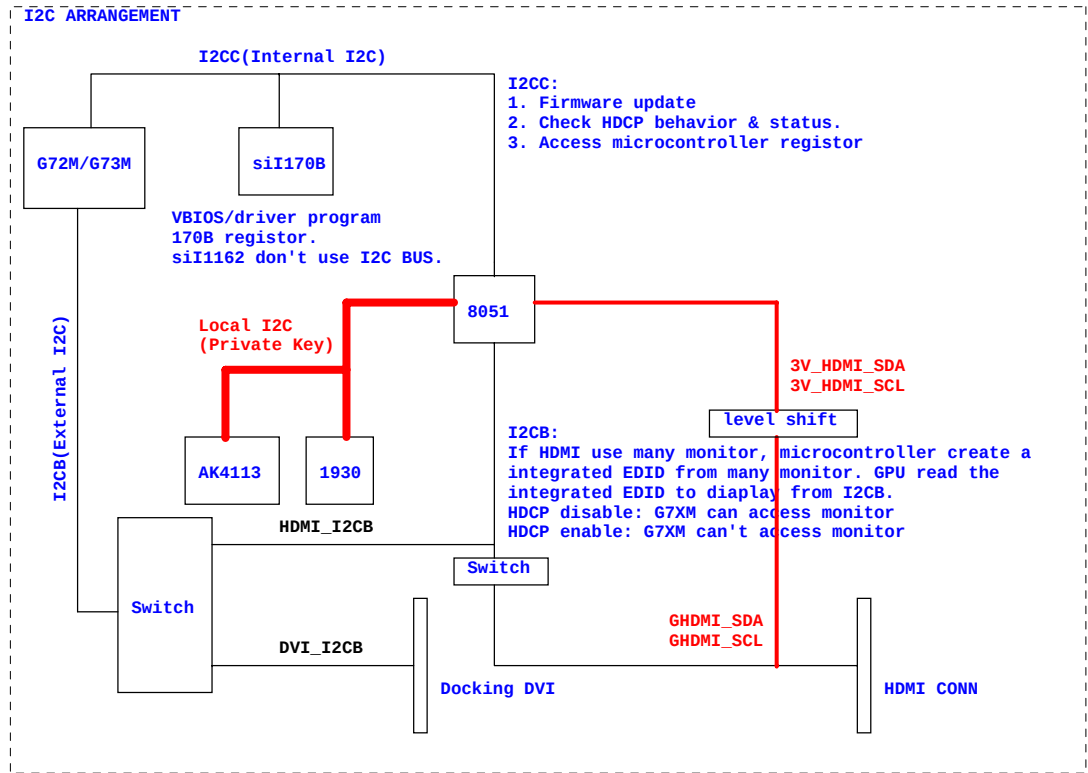
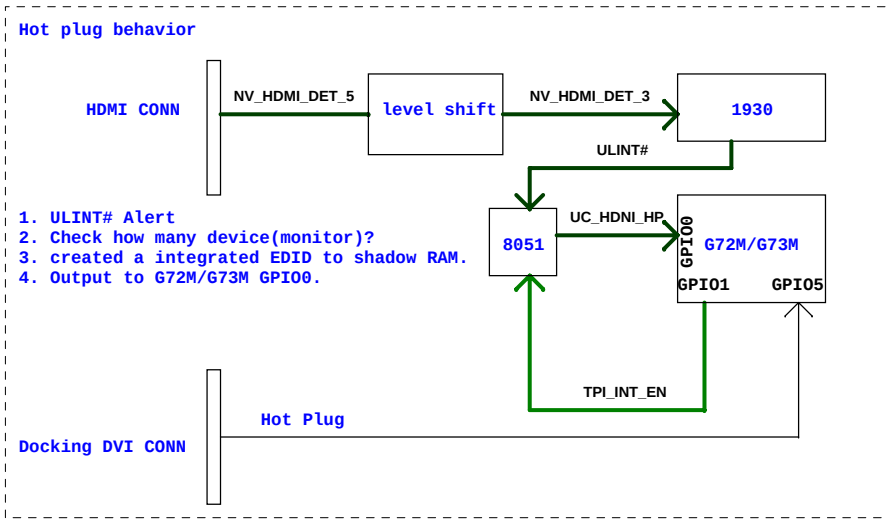
PANEL ID

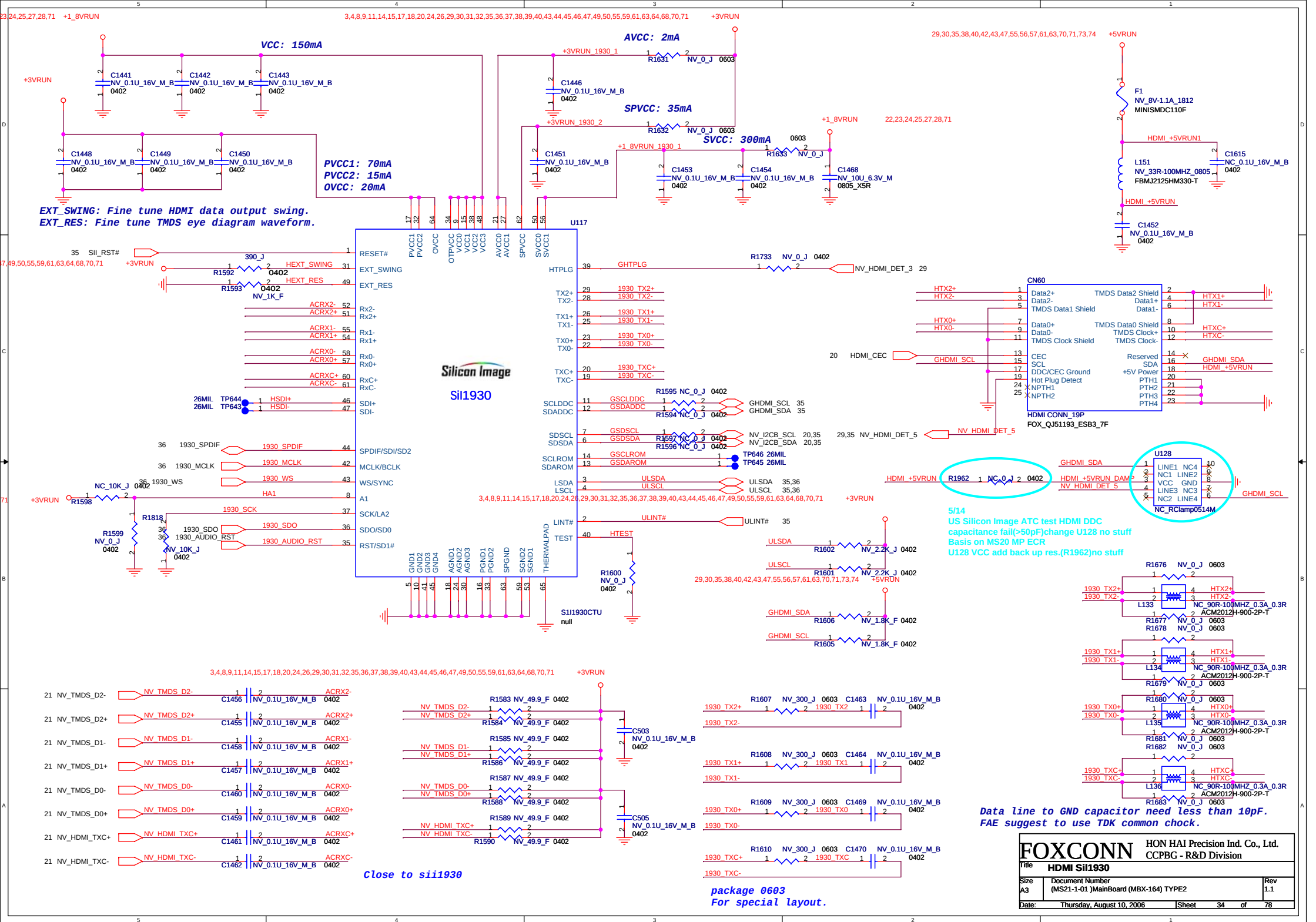


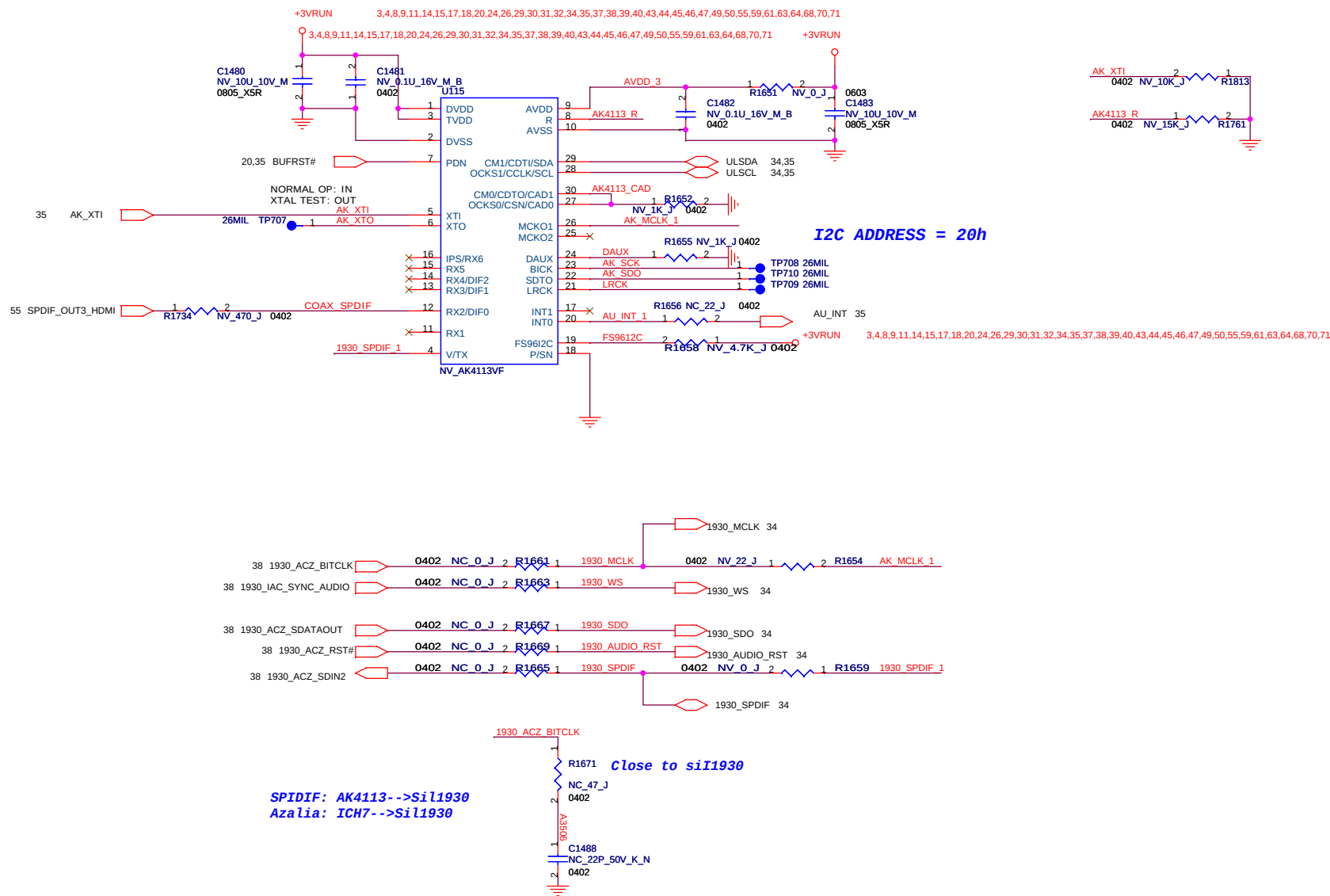
Type	WXGA+	WXGA+	WUXGA
Size	17" wide	17" wide	17" wide
Vender	LG-PHILIPS	LG-PHILIPS	SHARP
Device Name	LP171WP7-TLA	LP171WX2-A4K3	LQ170M1LA04
Panel ID Check[3..0]	2 Lamps 0001	1 Lamps 0010	2 Lamps 0100

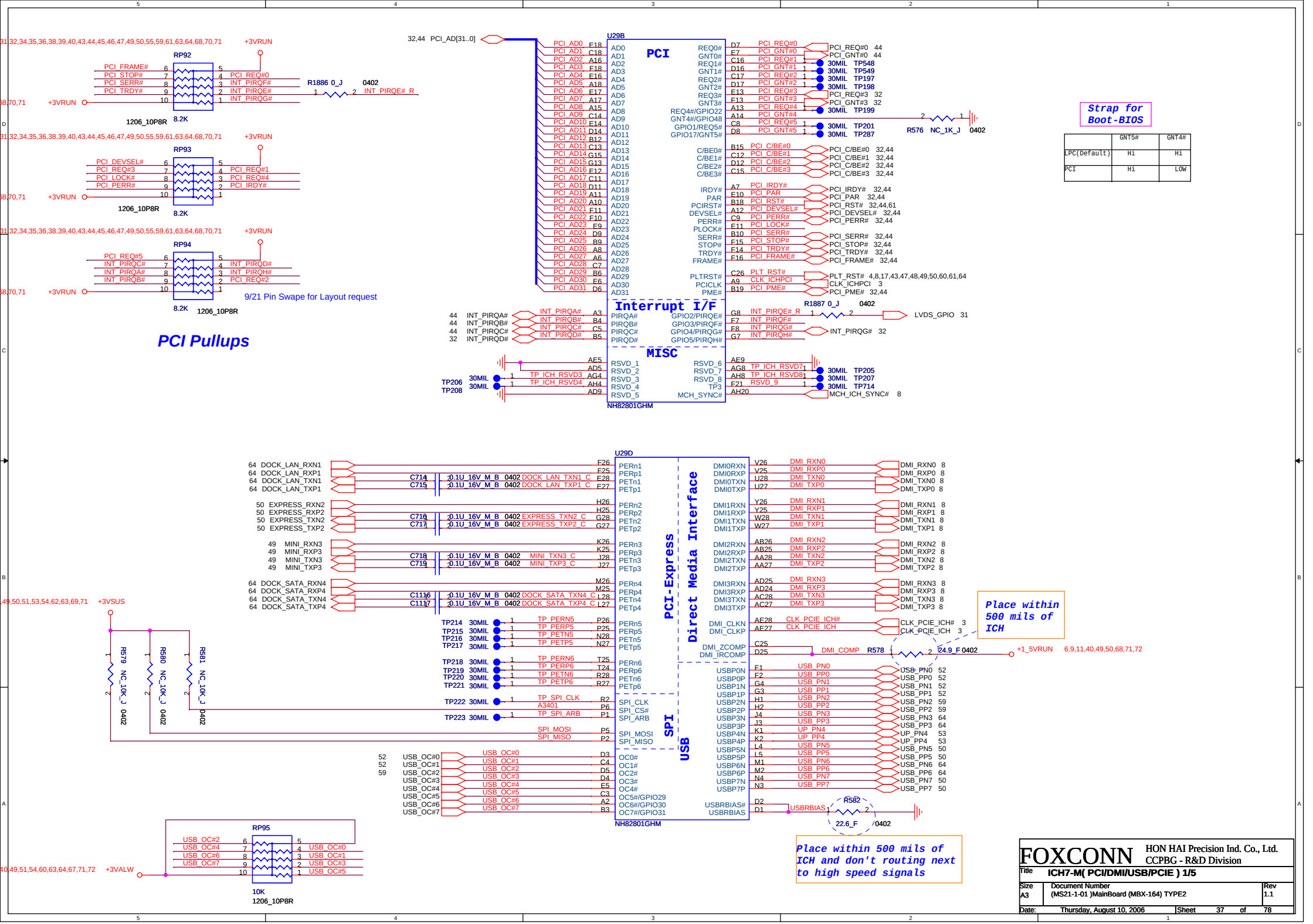
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title LVDS			
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2		Rev 1.1
Date:	Thursday, August 10, 2006	Sheet	31 of 78

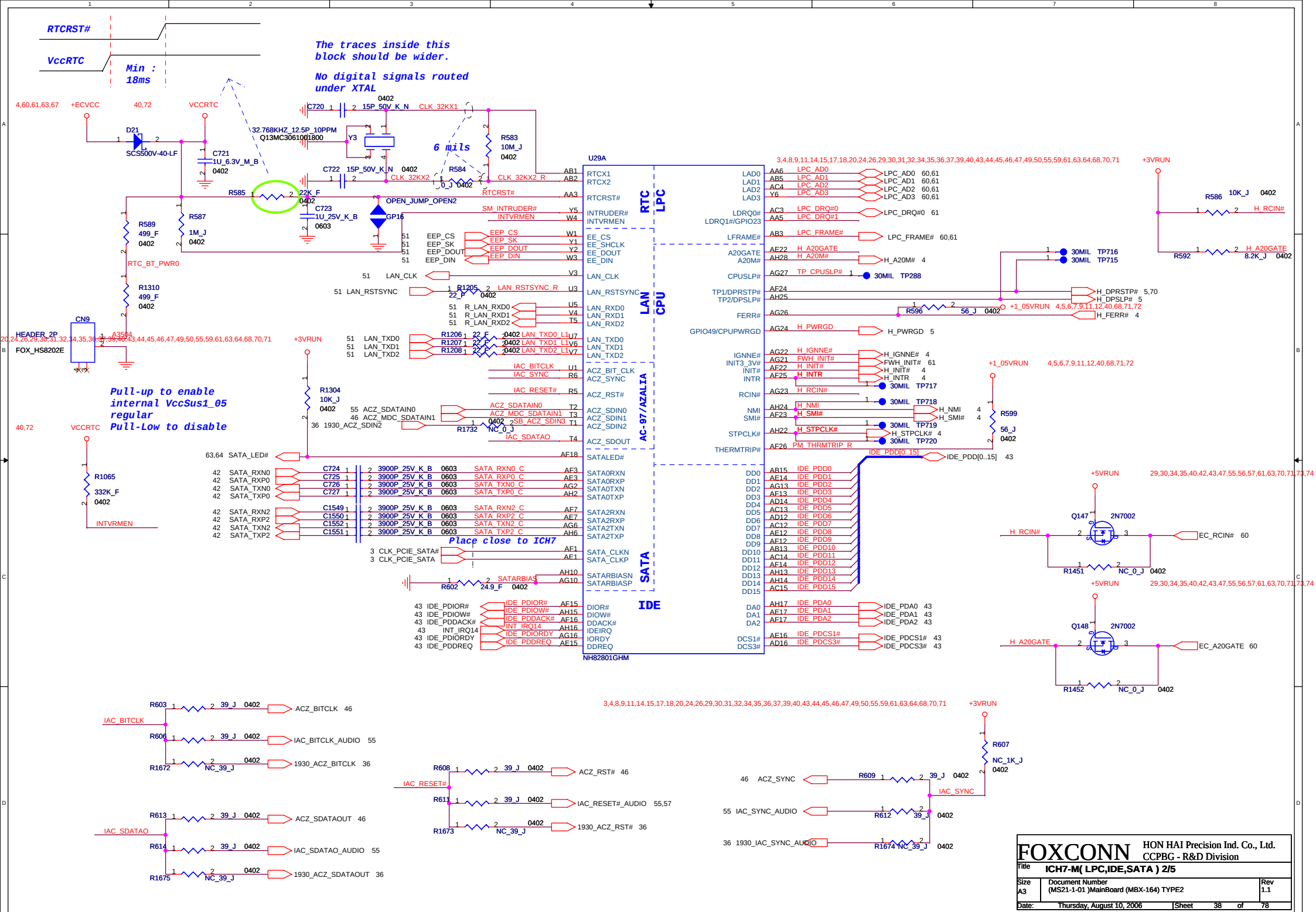
Hot plug behavior & I2C ARRANGEMENT block diagram

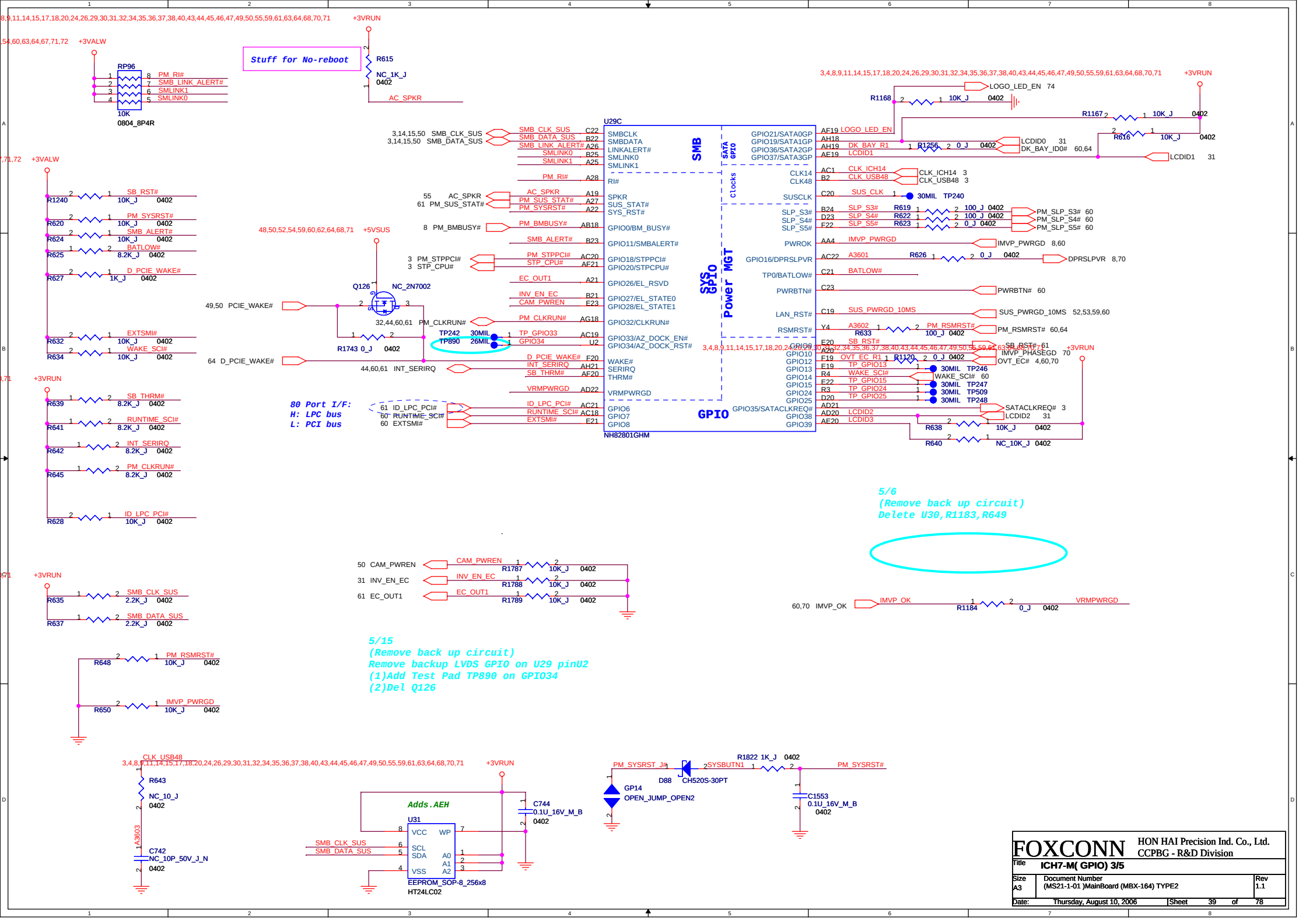


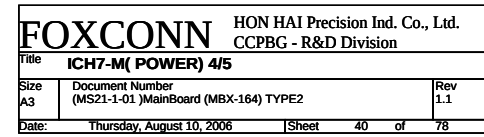


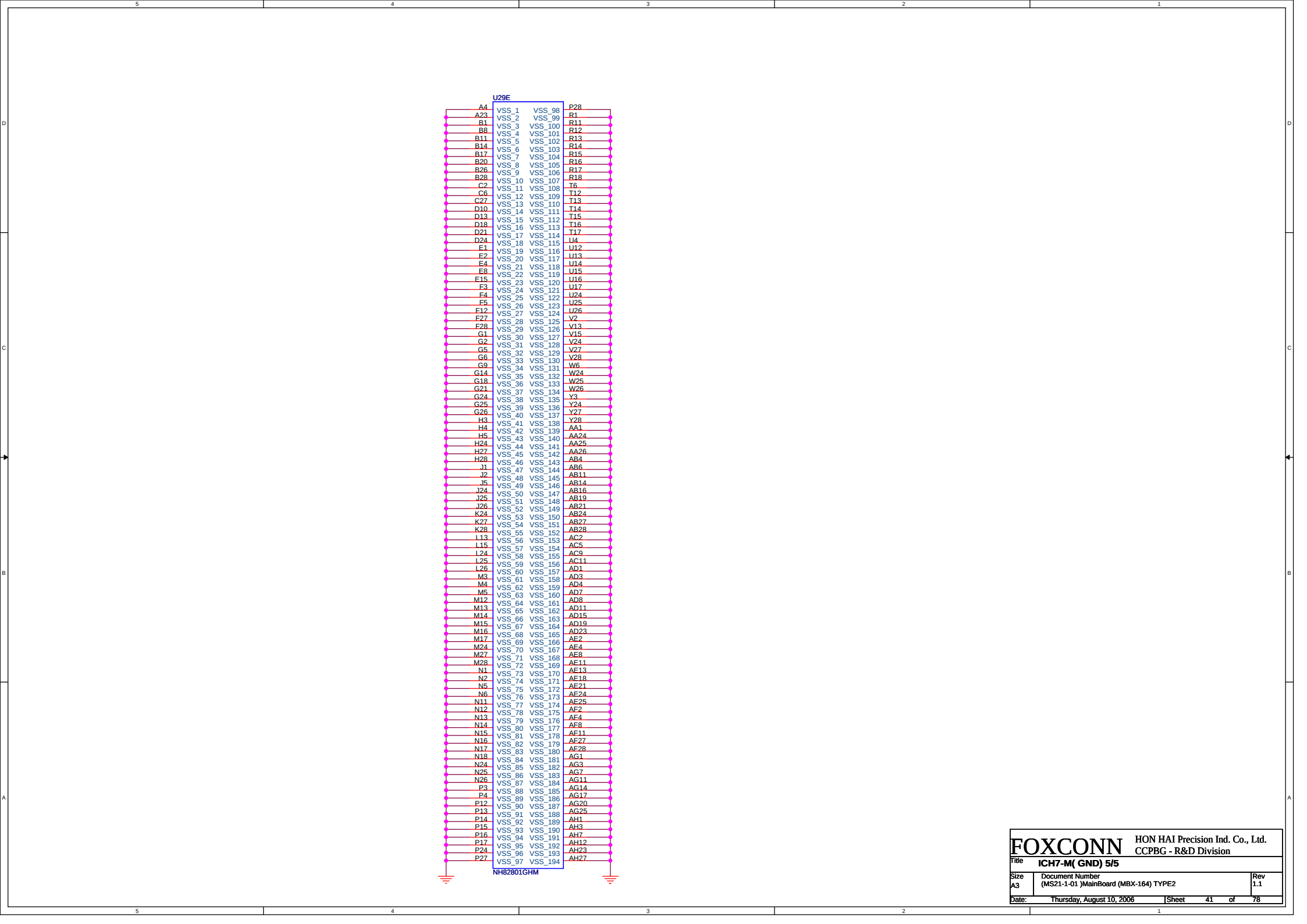






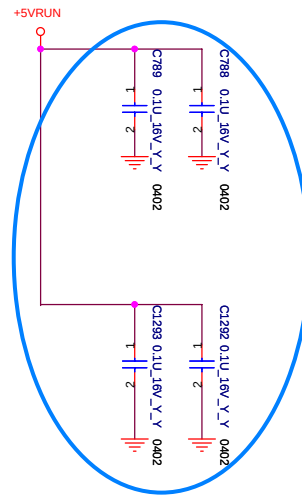






5/6
 For power droup cause 0.16V voltage loss Issue
 (1)F7,F8,F19,F20 no stuff
 (2)Co-layout normal open gap GP17~GP18 with fuse
 5/27 Delete SATA HDD Fuse backup circuit
 (1)Remove F7,F8,F19,F20 Pad
 (2)Remove GP17~GP18 open gap

29,30,34,35,38,40,43,47,55,56,57,61,63,70,71,73,74

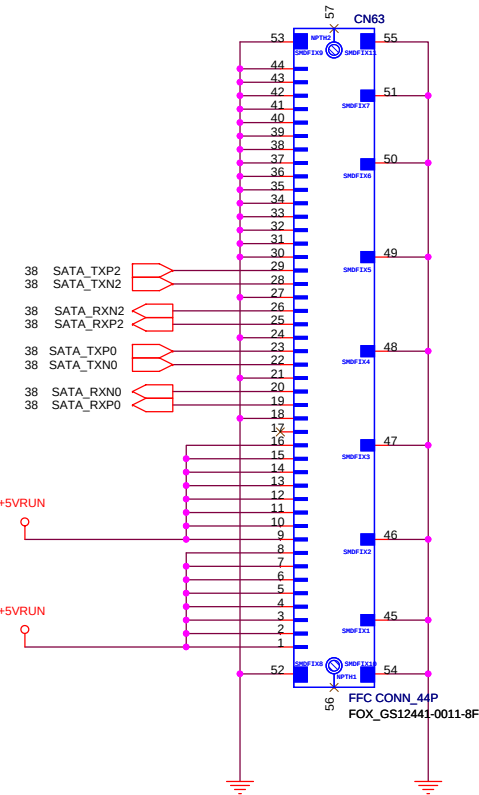


29,30,34,35,38,40,43,47,55,56,57,61,63,70,71,73,74

+5VRUN

29,30,34,35,38,40,43,47,55,56,57,61,63,70,71,73,74

+5VRUN



3,4,8,9,11,14,15,17,18,20,24,26,29,30,31,32,34,35,36,37,38,39,40,44,45,46,47,49,50,55,59,61,63,64,68,70,71

+3VRUN

CD-ROM CONN

38 IDE_PDD[0..15] IDE_PDD[0..15]

H: Slave
L: Master
ODD must Master

38 IDE_PDCS1#
38 IDE_PDA0
38 IDE_PDA1
38 INT_IRQ14
38 IDE_PDIORDY
38 IDE_PDIOW#

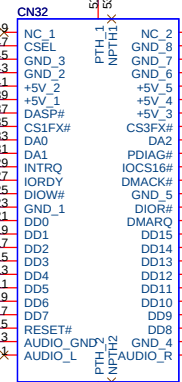
TP IDE_DASP#
IDE_PDCS1#
IDE_PDA0
IDE_PDA1
INT_IRQ14
IDE_PDIORDY
IDE_PDIOW#

IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
ODD_RESET#

4,8,17,37,47,48,49,50,60,61,64 PLT_RST#

R990
47_J
0402
C1668
100P_50V_K
0402_NPO

FOX_QT8H0506-H111R-4E
B TO B CONN_50P



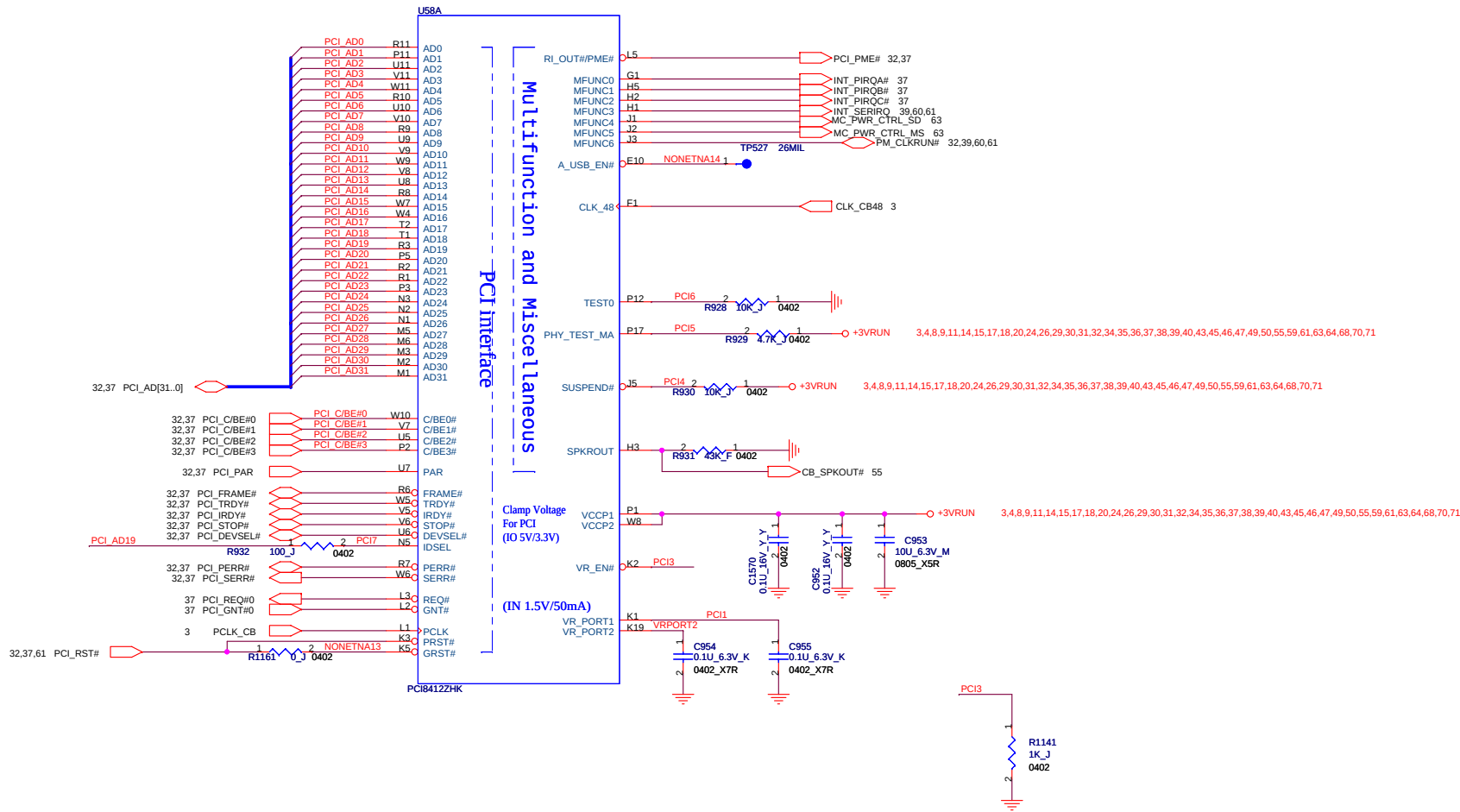
IDE_PDCS3#
IDE_PDA2
TP_PDIAG
IOCS16#
IDE_PDDACK#
IDE_PDIOR#
IDE_PDDREQ#
IDE_PDD15
IDE_PDD14
IDE_PDD13
IDE_PDD12
IDE_PDD11
IDE_PDD10
IDE_PDD9
IDE_PDD8

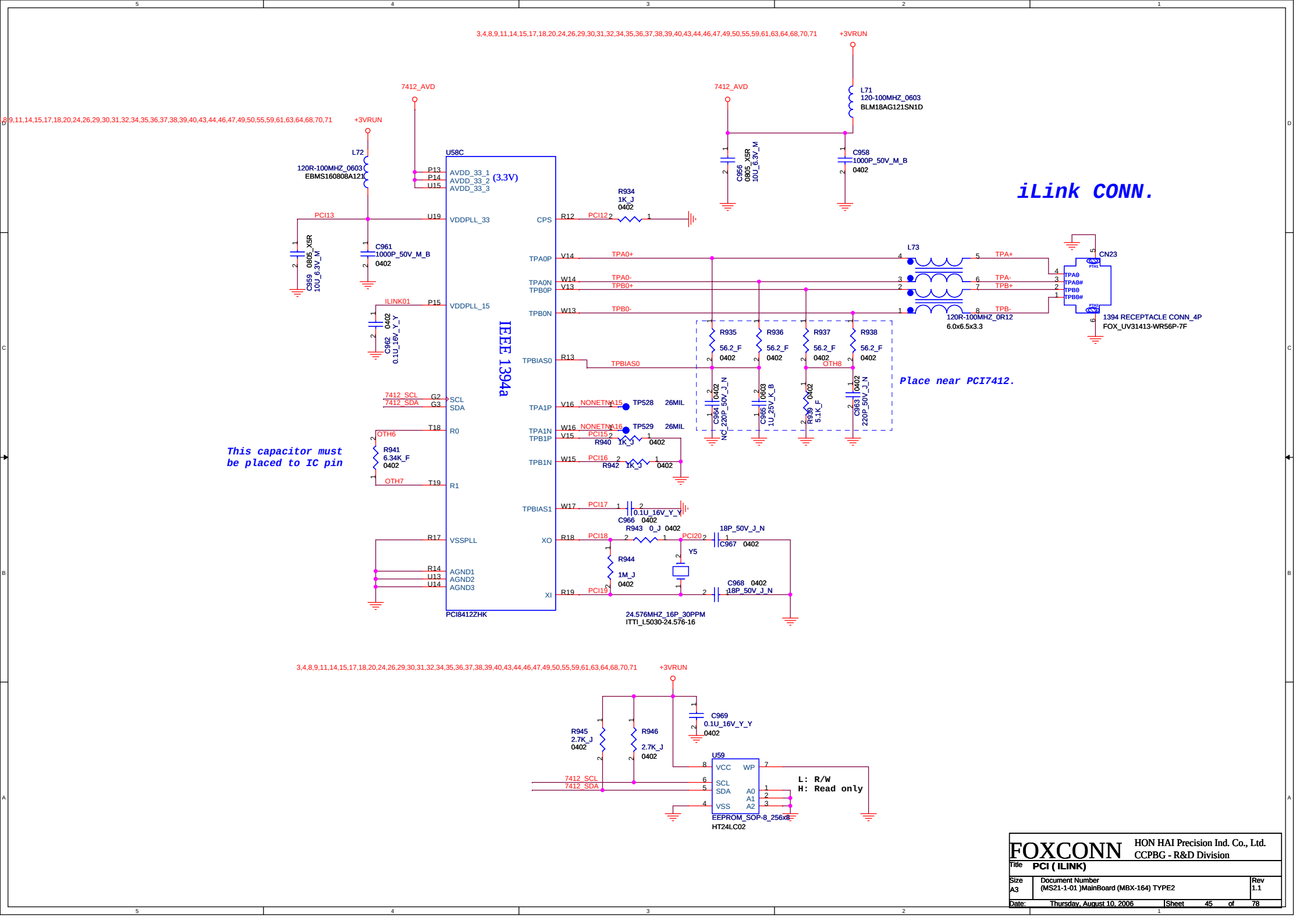
IDE_PDCS3#
IDE_PDA2
TP_PDIAG
IOCS16#
IDE_PDDACK#
IDE_PDIOR#
IDE_PDDREQ#
IDE_PDD15
IDE_PDD14
IDE_PDD13
IDE_PDD12
IDE_PDD11
IDE_PDD10
IDE_PDD9
IDE_PDD8

R995
10K_J
0402

+5VRUN

29,30,34,35,38,40,42,47,55,56,57,61,63,70,71,73,74

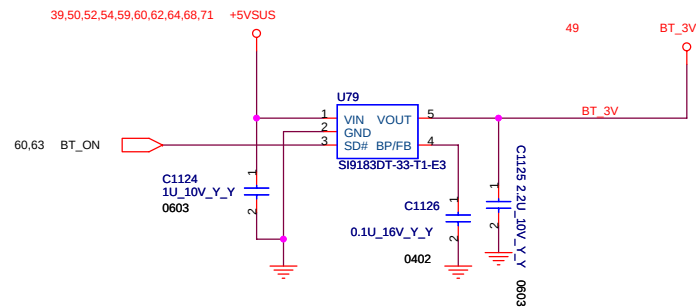




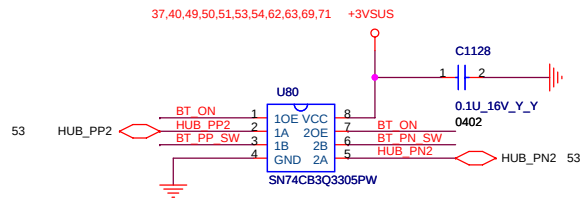
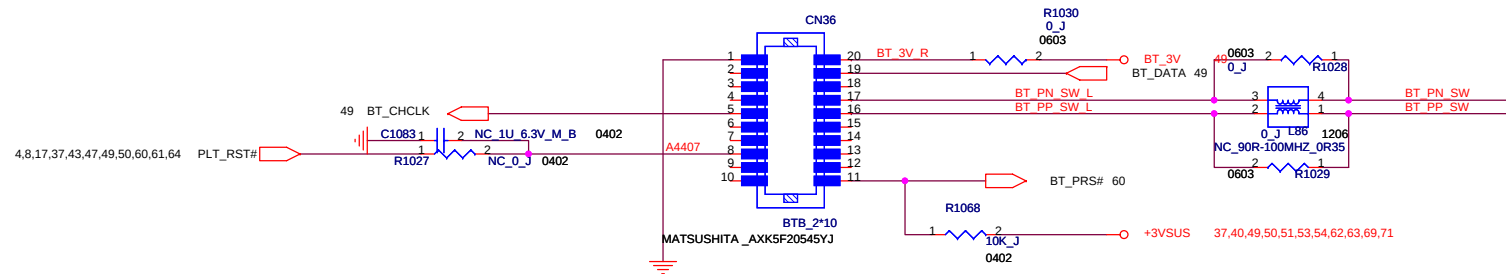
iLink CONN.

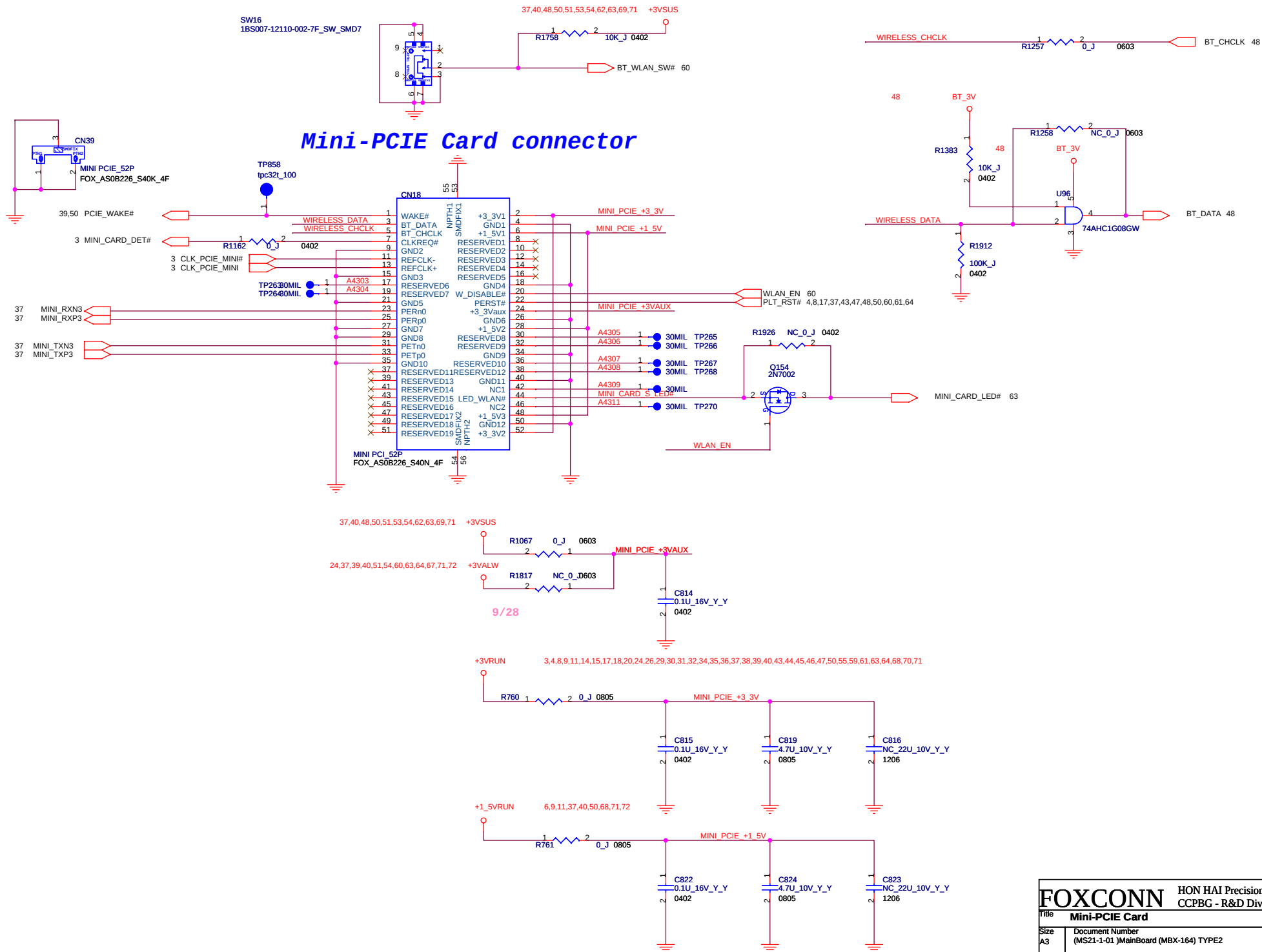
Place near PCI7412.

This capacitor must be placed to IC pin

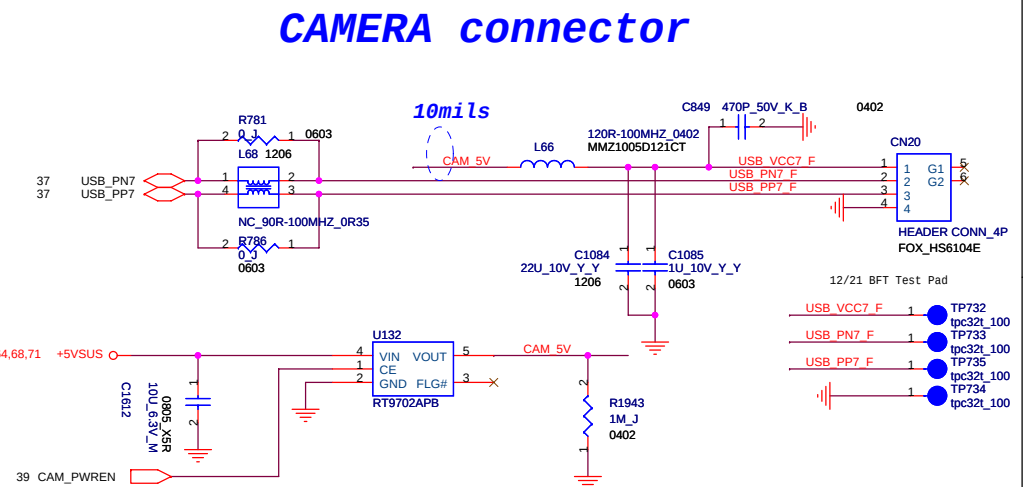
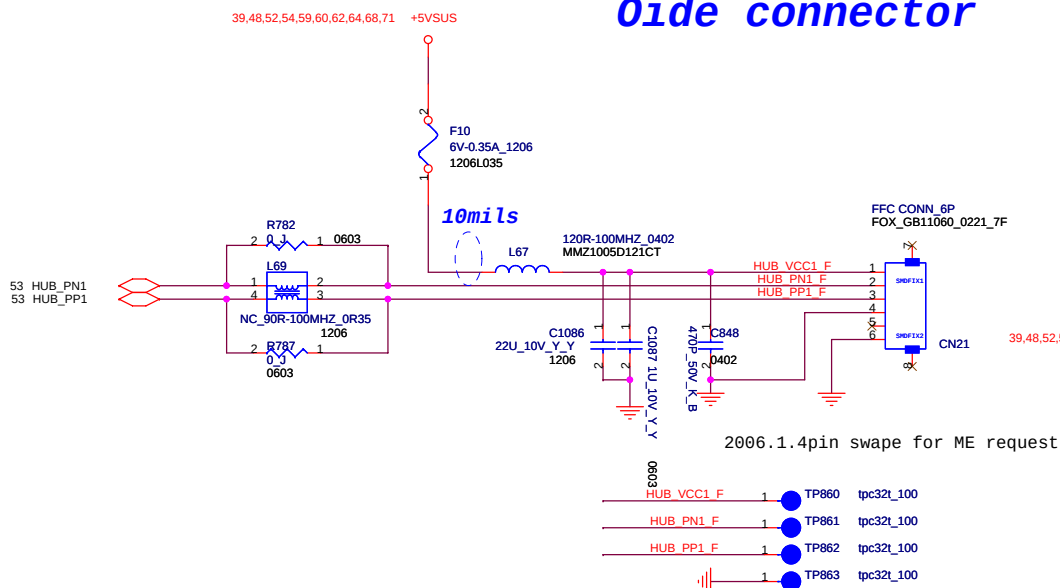
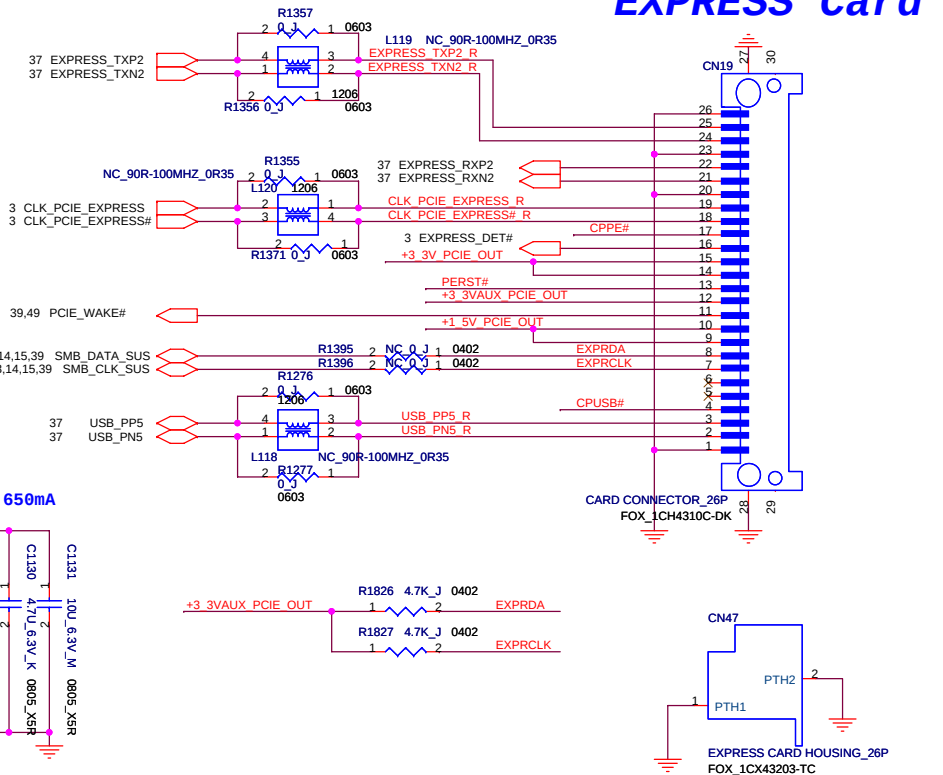
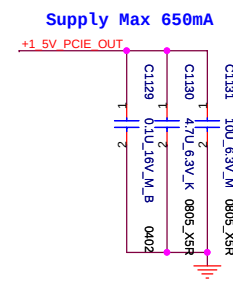
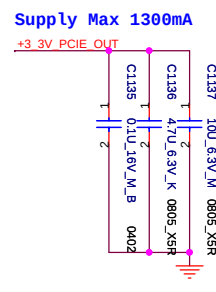
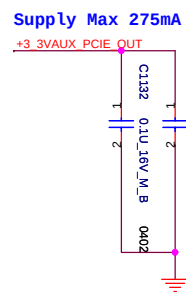
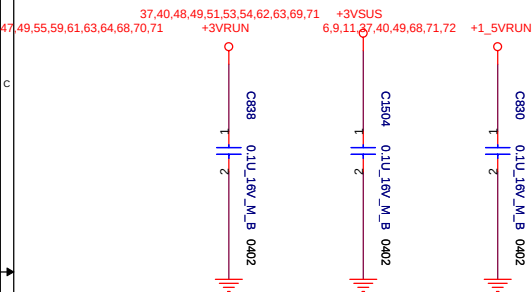
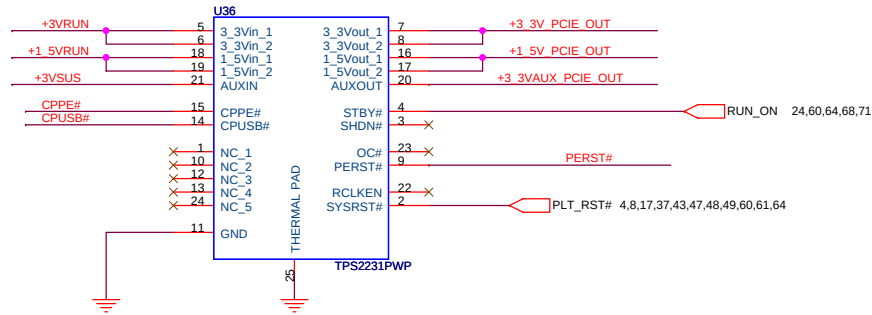


Bluetooth connector

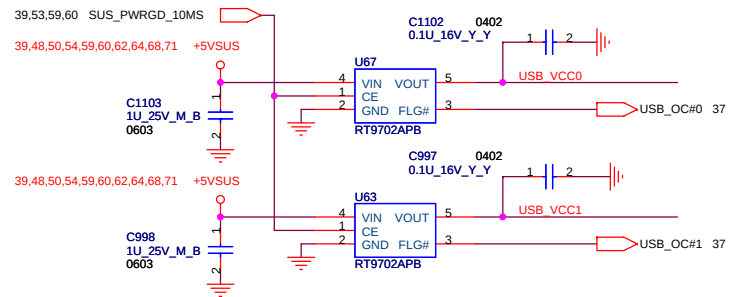
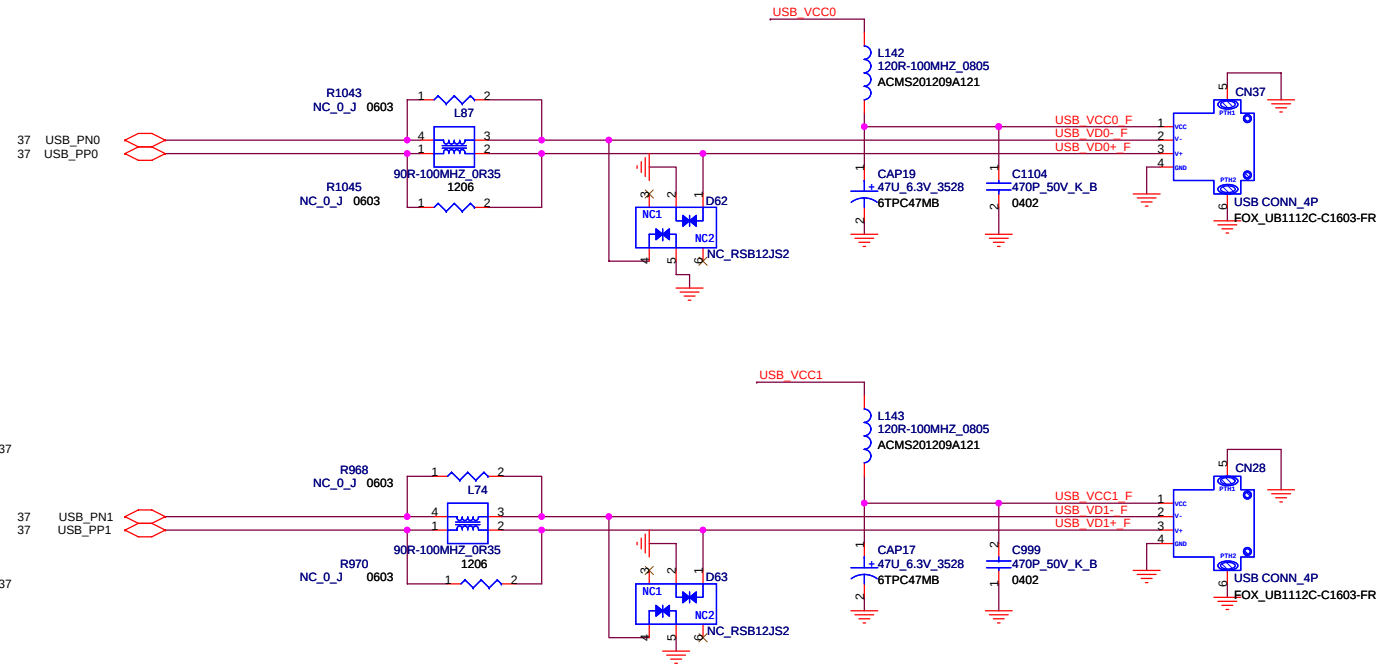




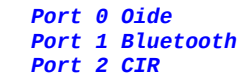
VOLTAGE INPUTS ⁽¹⁾			LOGIC INPUTS			VOLTAGE OUTPUTS ⁽²⁾			MODE ⁽³⁾
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP ⁽⁴⁾	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted



USB connector *2

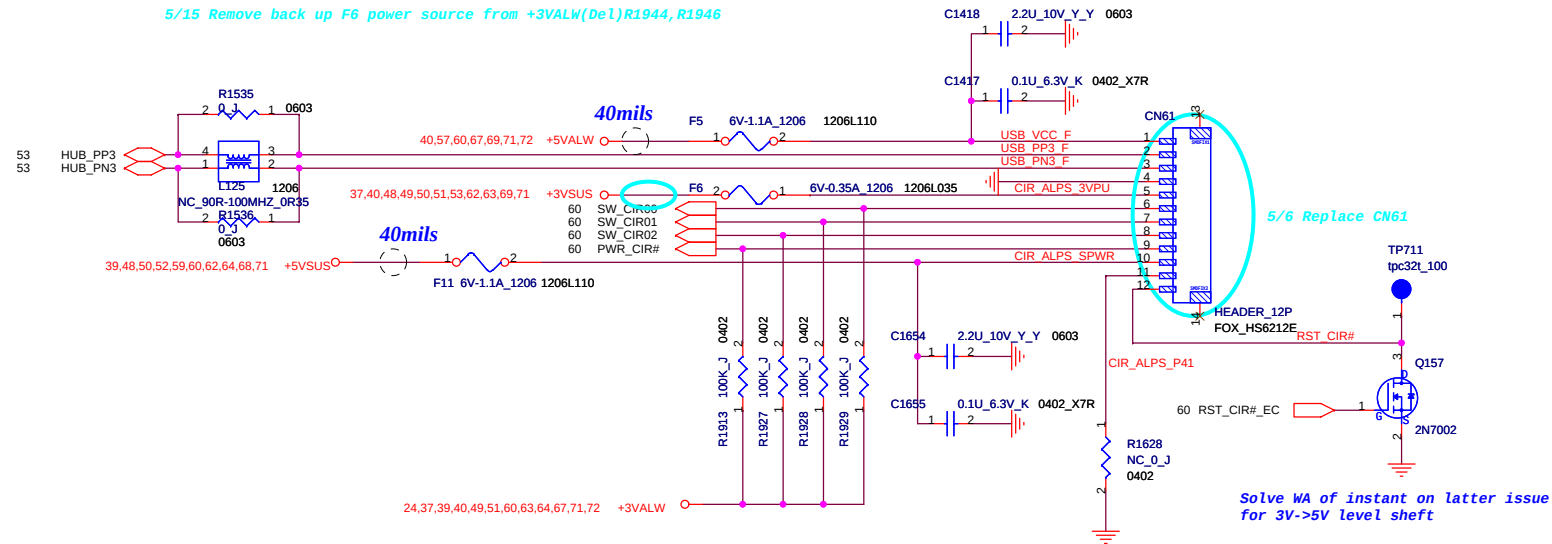


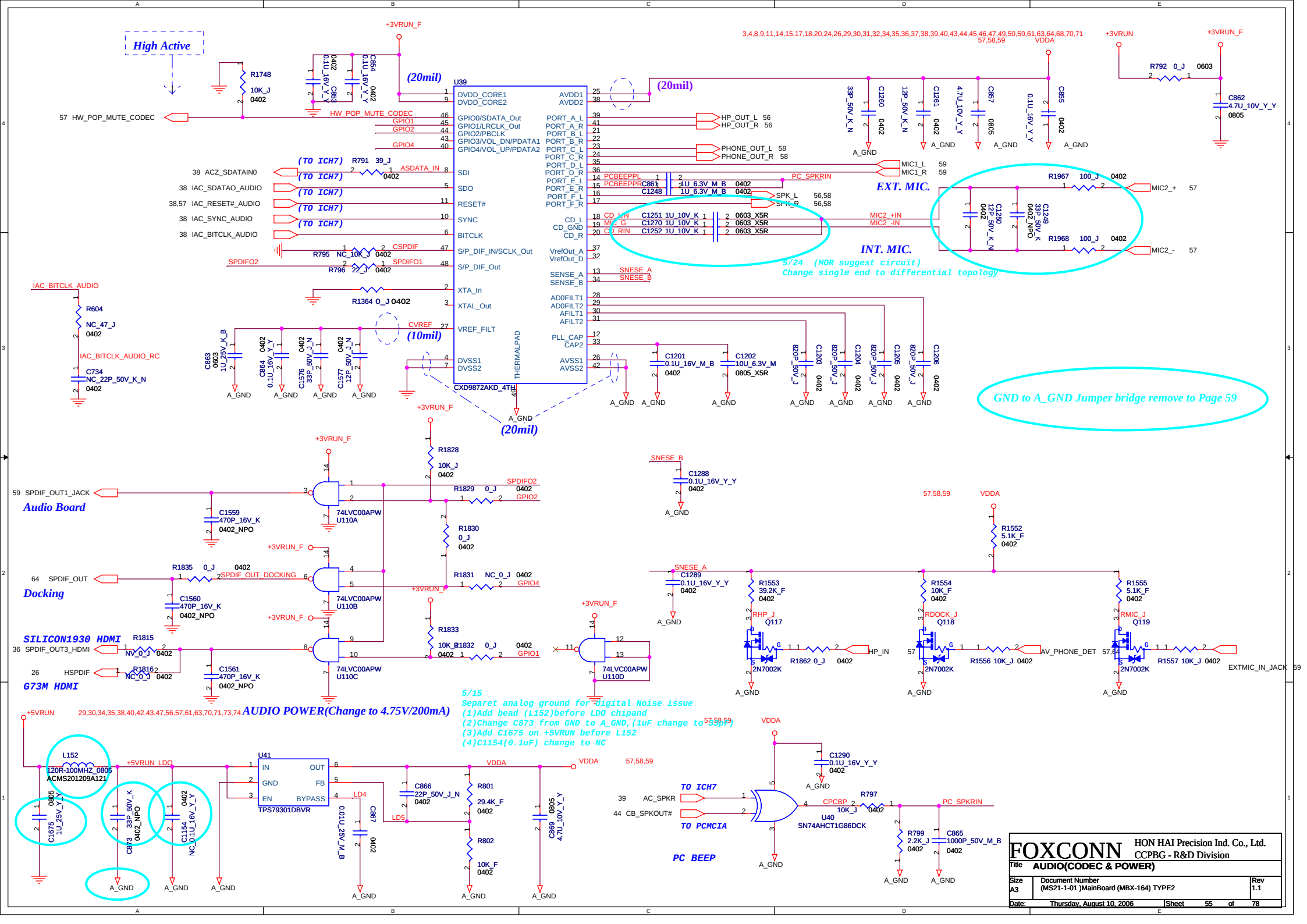
USB 1.1 HUB



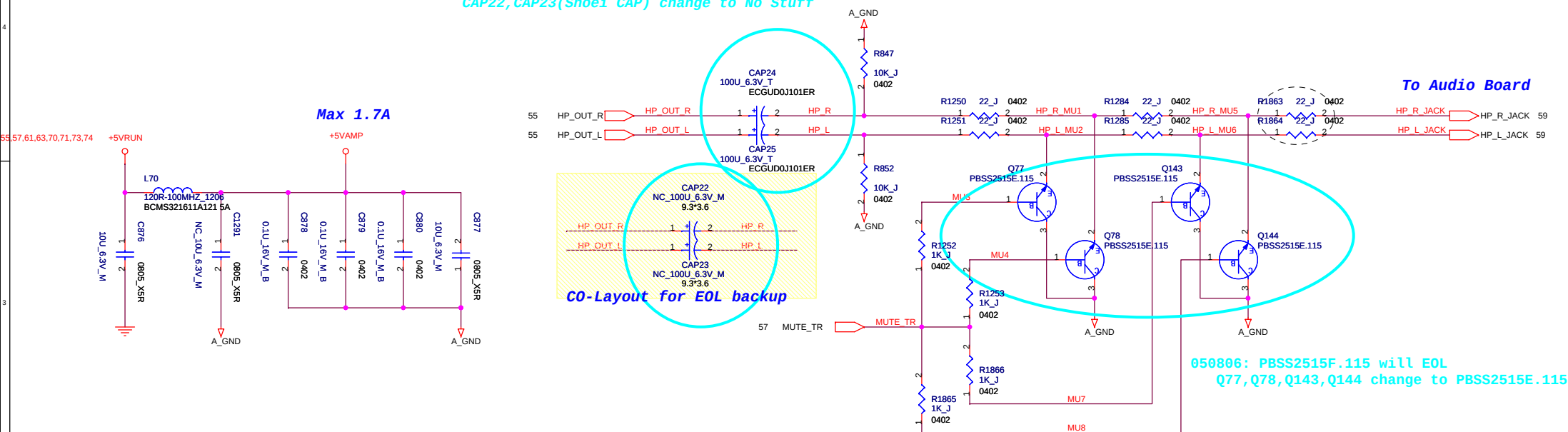
IR Receiver connector

5/15 Remove back up F6 power source from +3VALW(Del)R1944,R1946





```
050806: Shoei CAP will EOL
CAP24,CAP25(SP CAP) change to Stuff
CAP22,CAP23(Shoei CAP) change to No Stuff
```

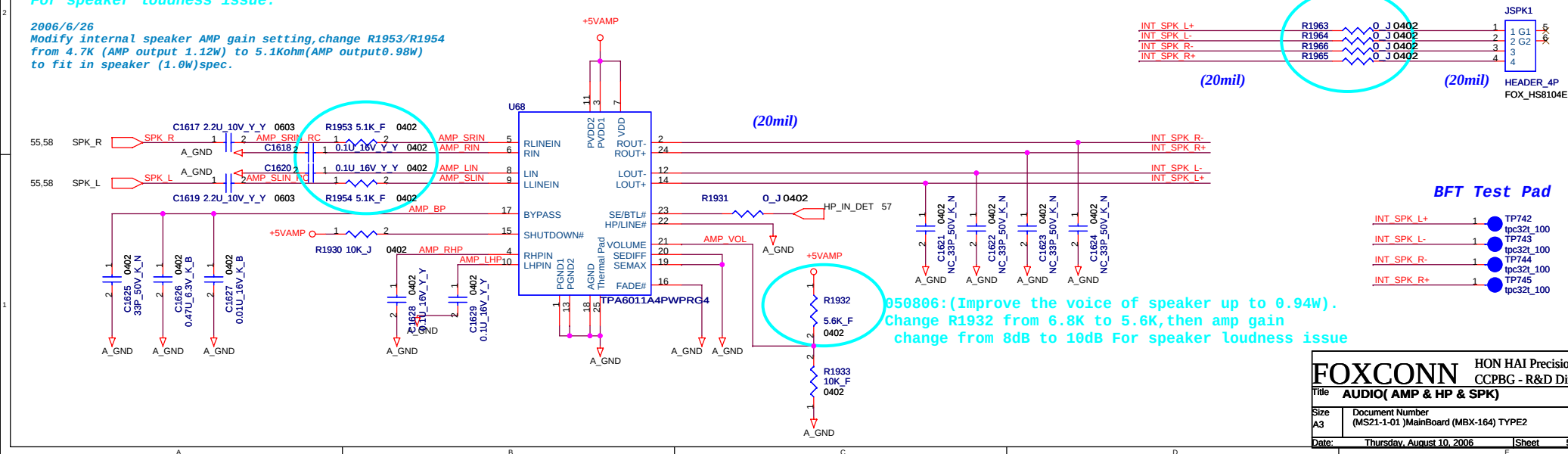


INTERNAL SPEAKER

050806:(Improve the voice of speaker up to 0.94W).
Add damping Resistors R1953 on AMP_SRIN, R1954 on AMP_SLIN
then speaker amp output won't be distorted.
For speaker loudness issue.

2006/6/26
Modify internal speaker AMP gain setting, change R1953/R1954 from 4.7K (AMP output 1.12W) to 5.1Kohm (AMP output 0.98W) to fit in speaker (1.0W) spec.

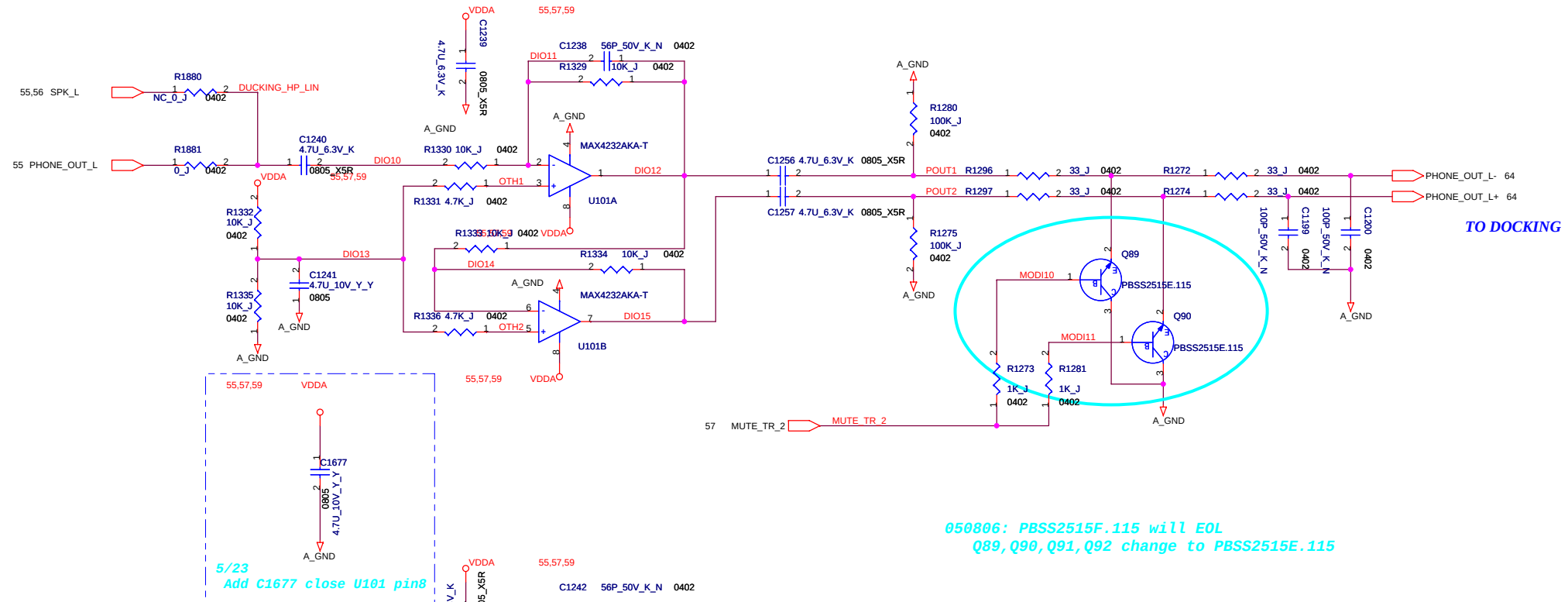
```
050806:(Improve the voice of speaker up to 0.94W).
EMI team confirm whether
it is ok to use 0ohm resistor replacing bead
```



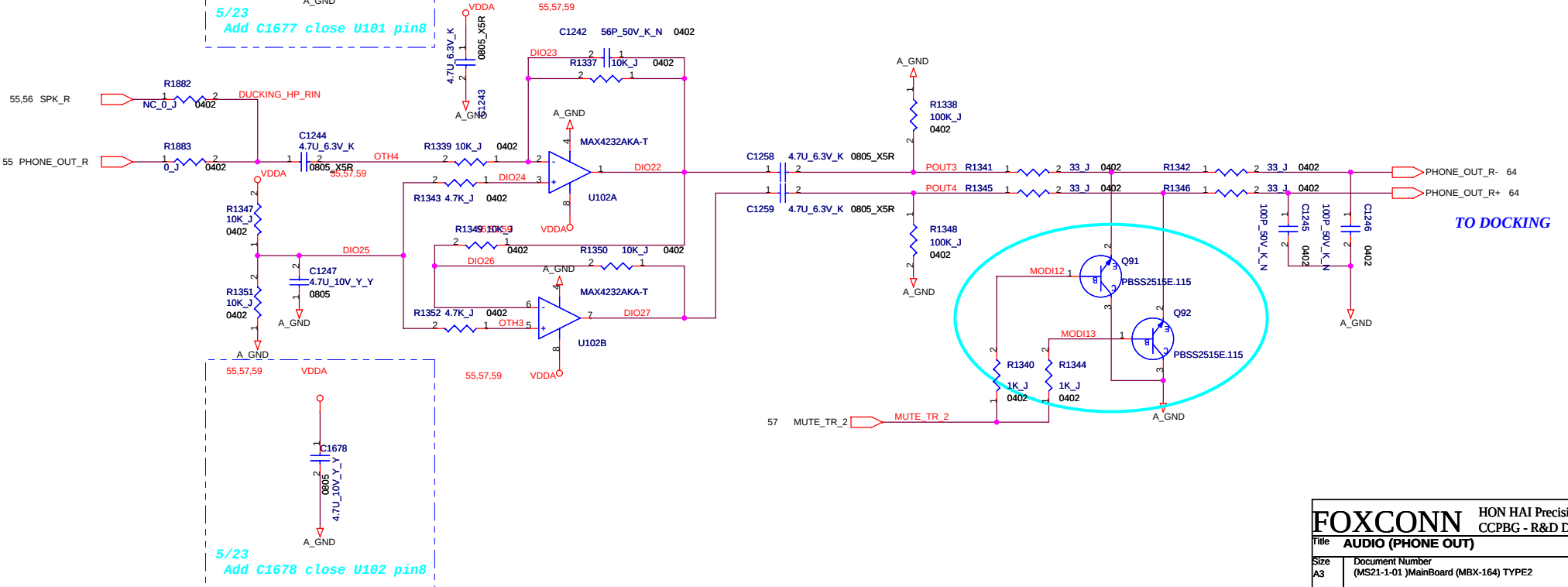
BFT Test Pad

050806:(Improve the voice of speaker up to 0.94W).
Change R1932 from 6.8K to 5.6K,then amp gain
change from 8dB to 10dB For speaker loudness issue

PHONE OUT



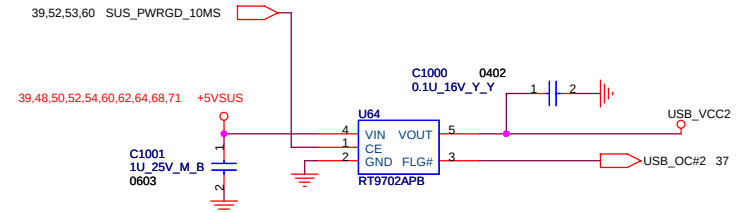
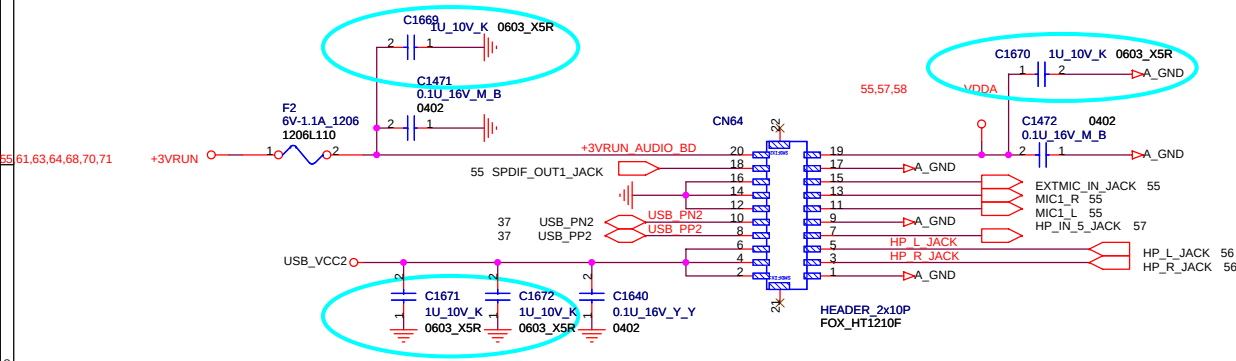
050806: PBSS2515F.115 will EOL
Q89,Q90,Q91,Q92 change to PBSS2515E.115



Audio Board connector

050806: (To improve SNR issue)

Add 1uF capacitors close CN64 :C1671,C1672 on USB_VCC2,
C1669 on +3VRUN_AUDIO_BD, and C1670 on VDDA .



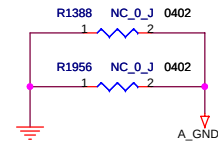
5/6

Separate analog ground for digital Noise issue:

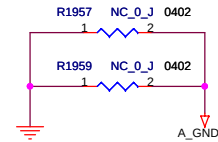
- (1) Remove GP3 (Close Jumper) not bridge between GND and A_GND
- (2) Backup two jumper resistors for bridge between GND and A_GND (C1388, C1966 on Screw hole H3, C1957, C1959 on screw hole H5)
- (3) Isolate screw hole H4, add 100pF capacitors C1673, C1674 for EMI, Zener diode D100 for ESD
- (4) Add jumper resistor for Return patch R1955 close L70 & R1958 close U41(+5VRUN) & R1960 close codec.

Backup two jumper resistors for bridge between GND and A_GND

Close screw hole H3

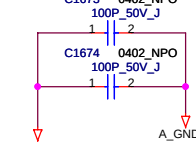


Close screw hole H5

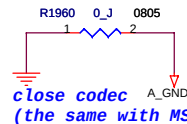
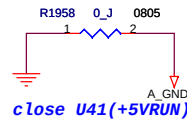
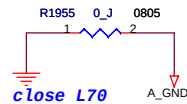


Isolate screw hole H4, and add EMI/ESD solution

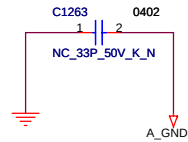
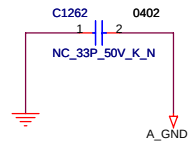
EMI



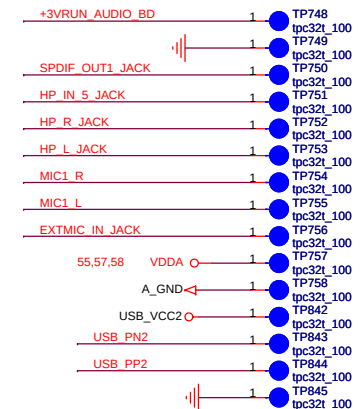
Add jumper resistor for Return patch

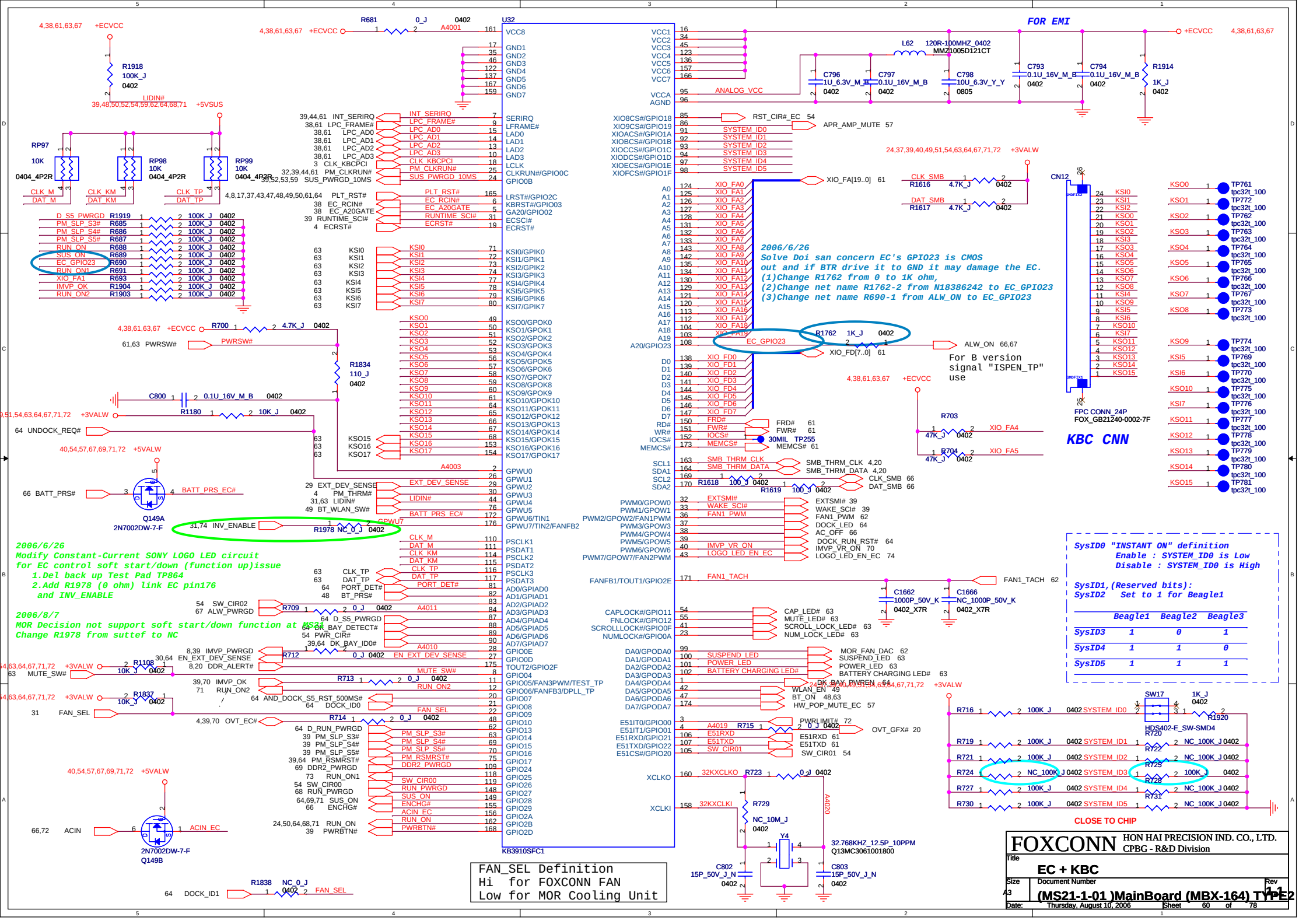


Original EMI back up solution to continue with MS20(bridge between GND and A_GND)

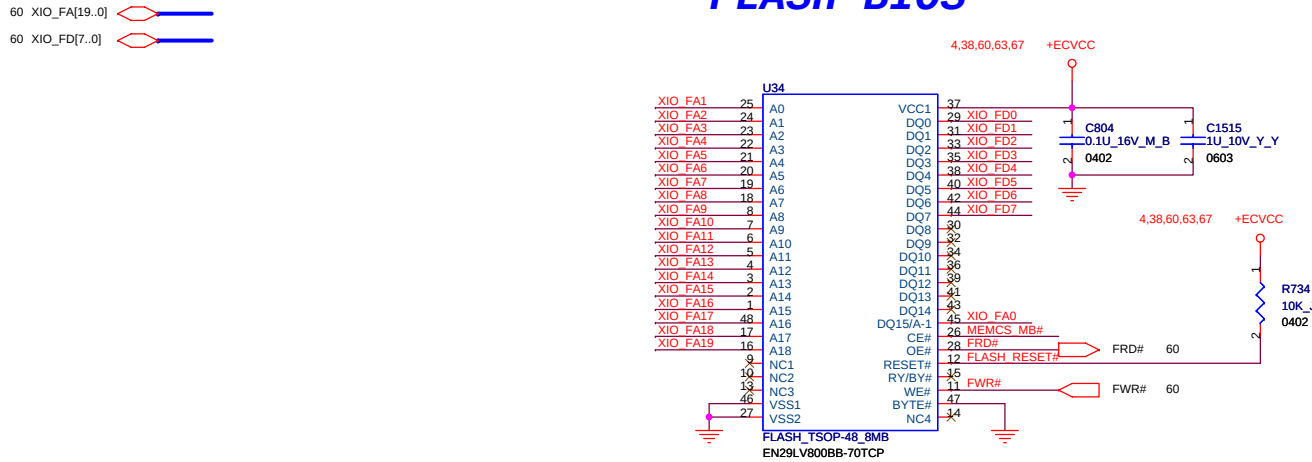


BFT Test Pad

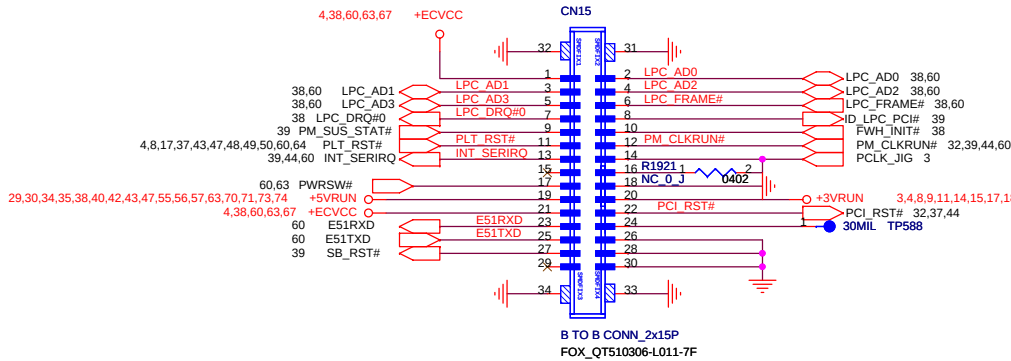




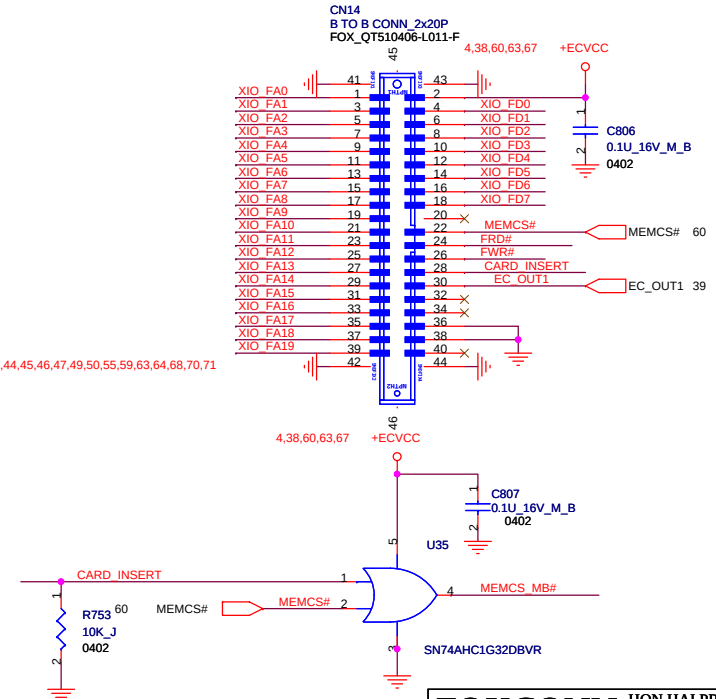
FLASH BIOS



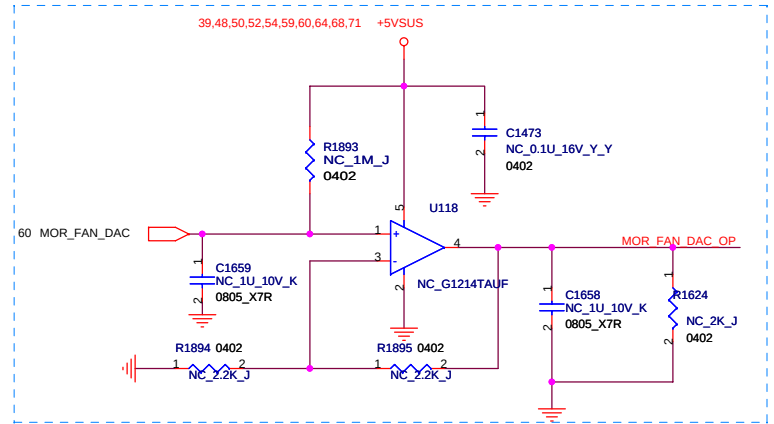
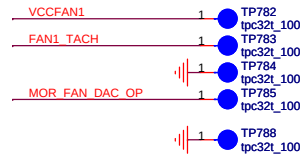
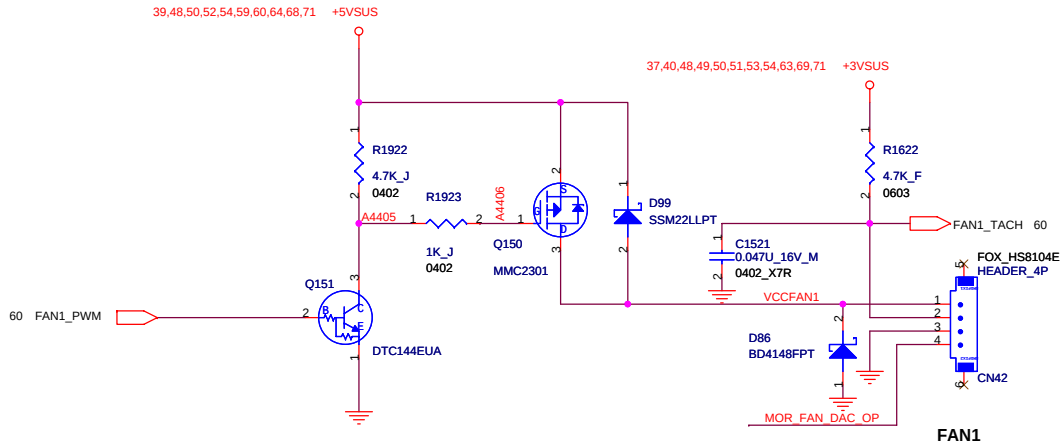
JIG-120



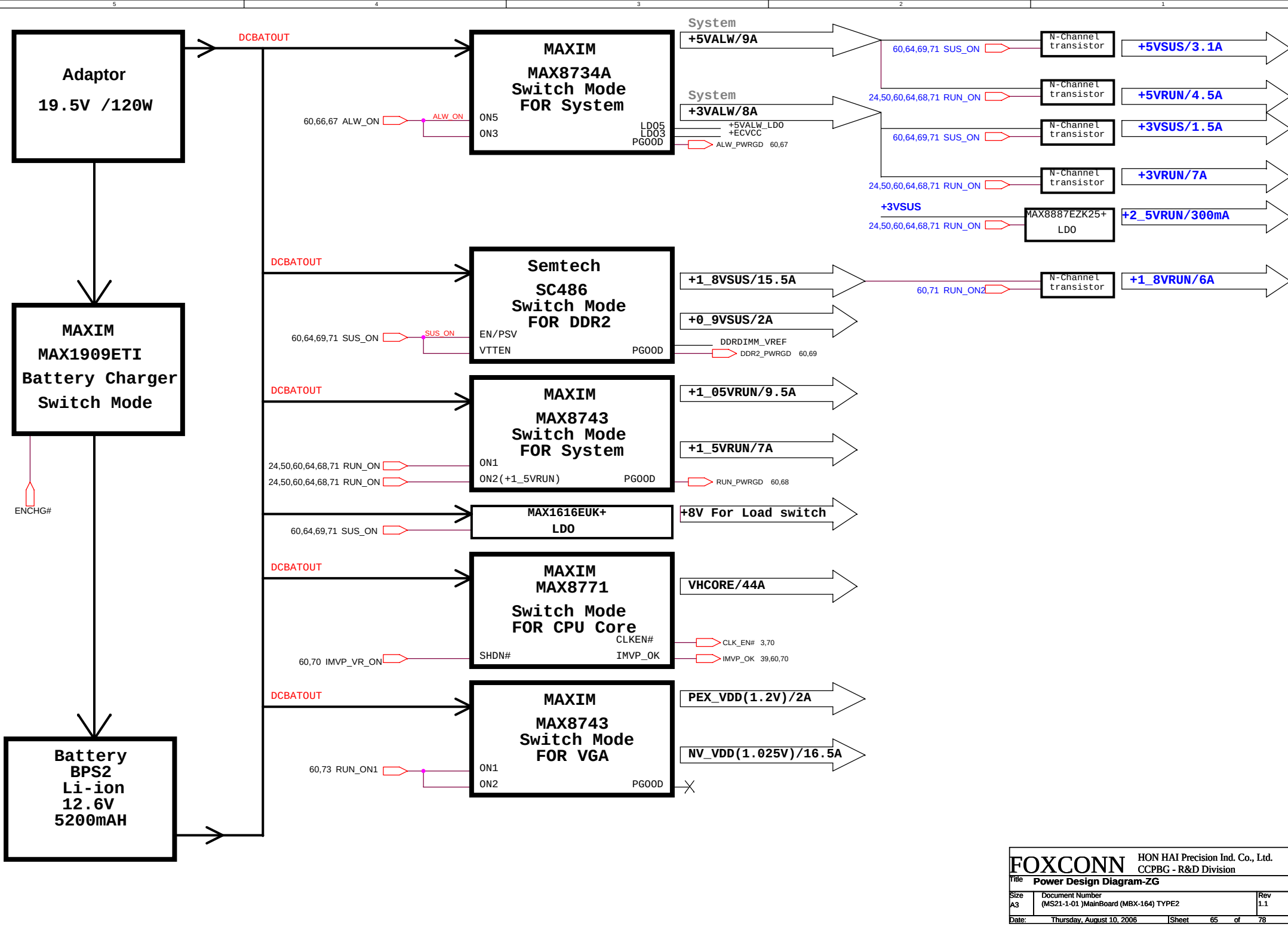
X-BUS



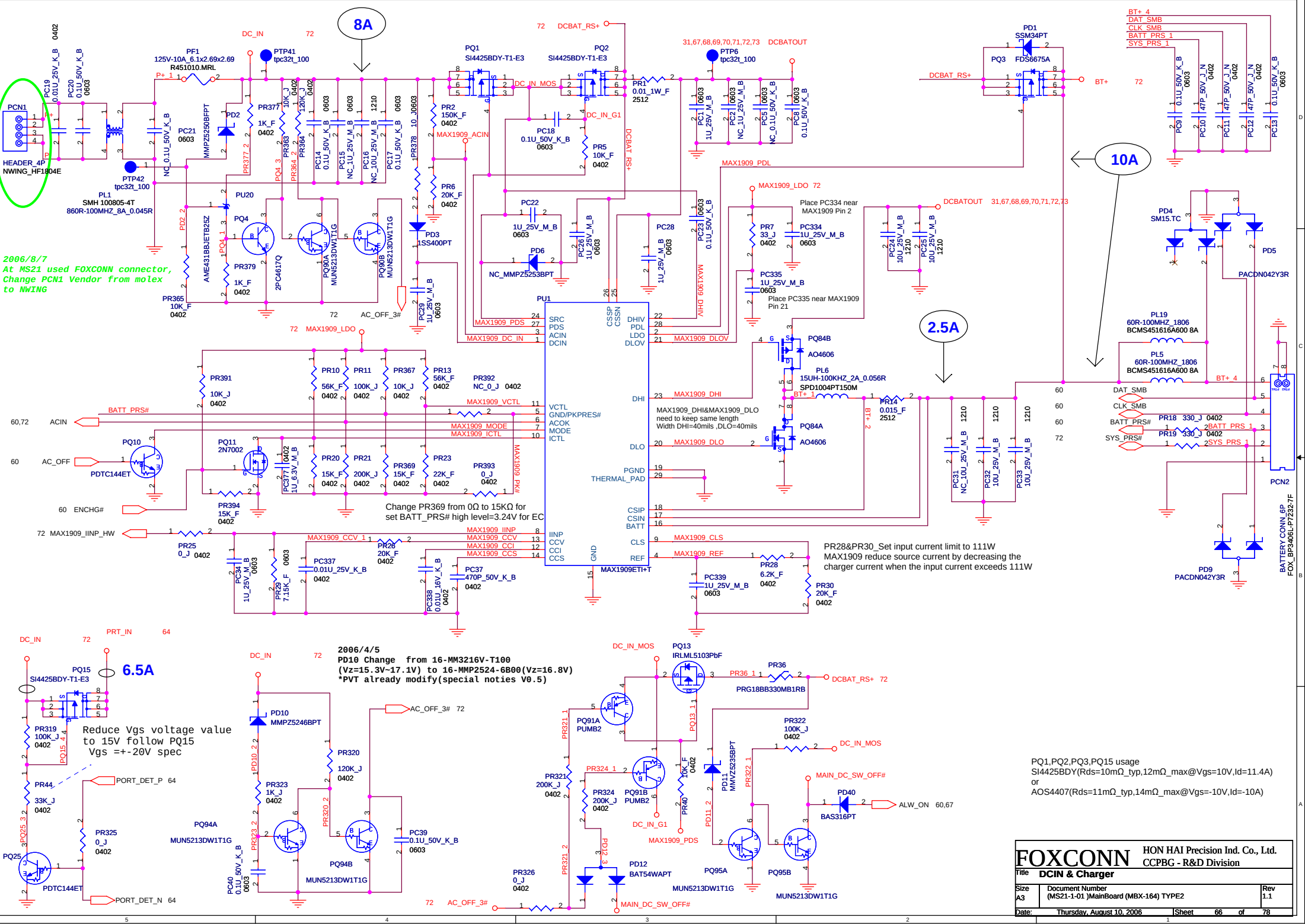
FAN(FAN1+MOR FAN)



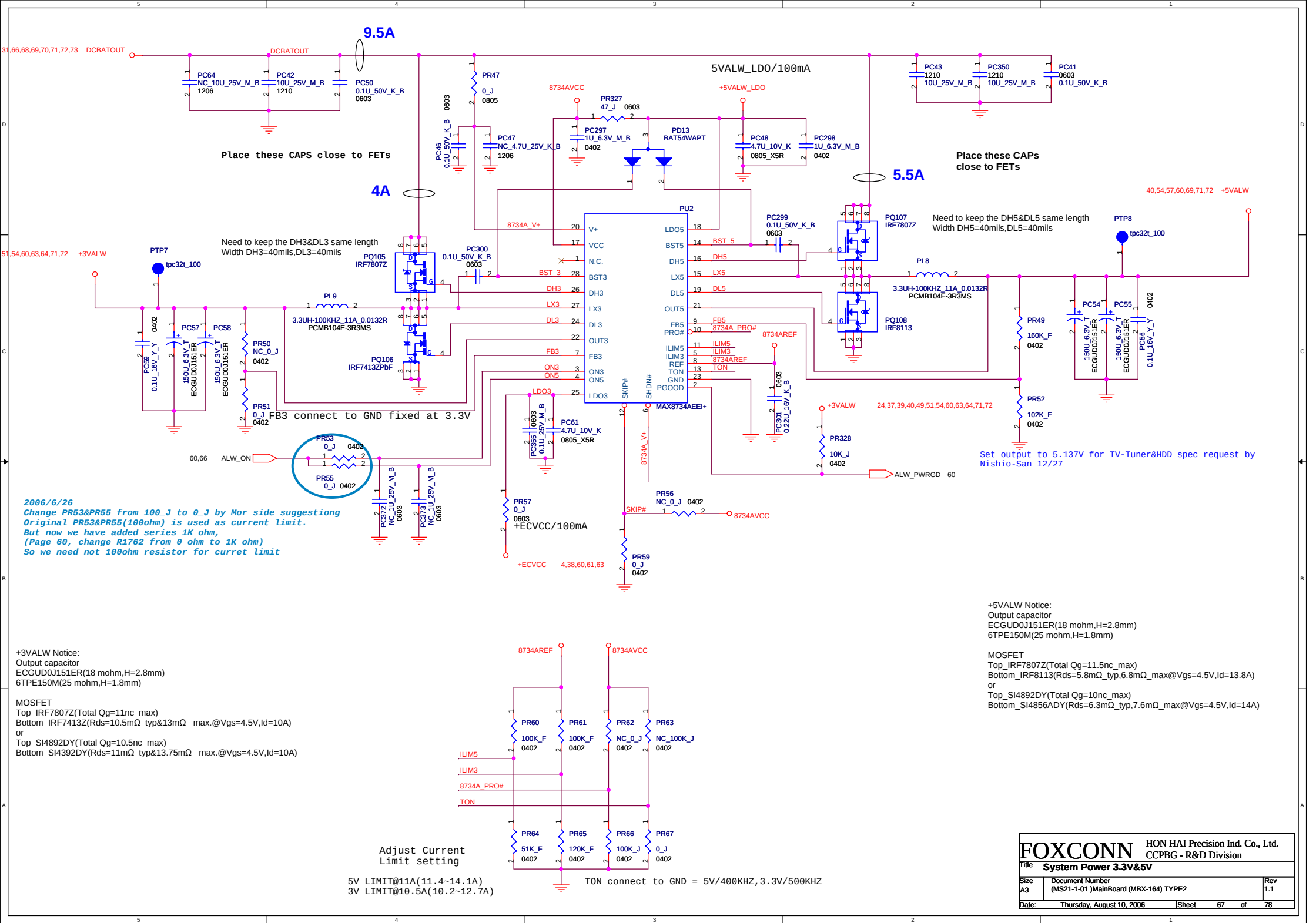
```
6/28 MOR fan circuit modify to backup
(NC)U118
(NC)R1893
(NC)R1894
(NC)R1895
(NC)R1624
(NC)C1473
```

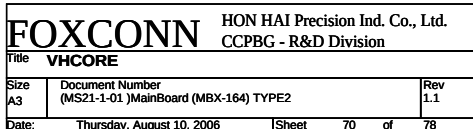



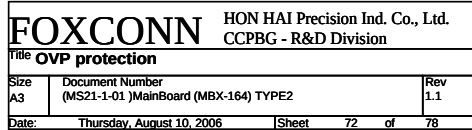
2006/8/7
At MS21 used FOXCONN connector,
Change PCN1 Vendor from molx
to NWING

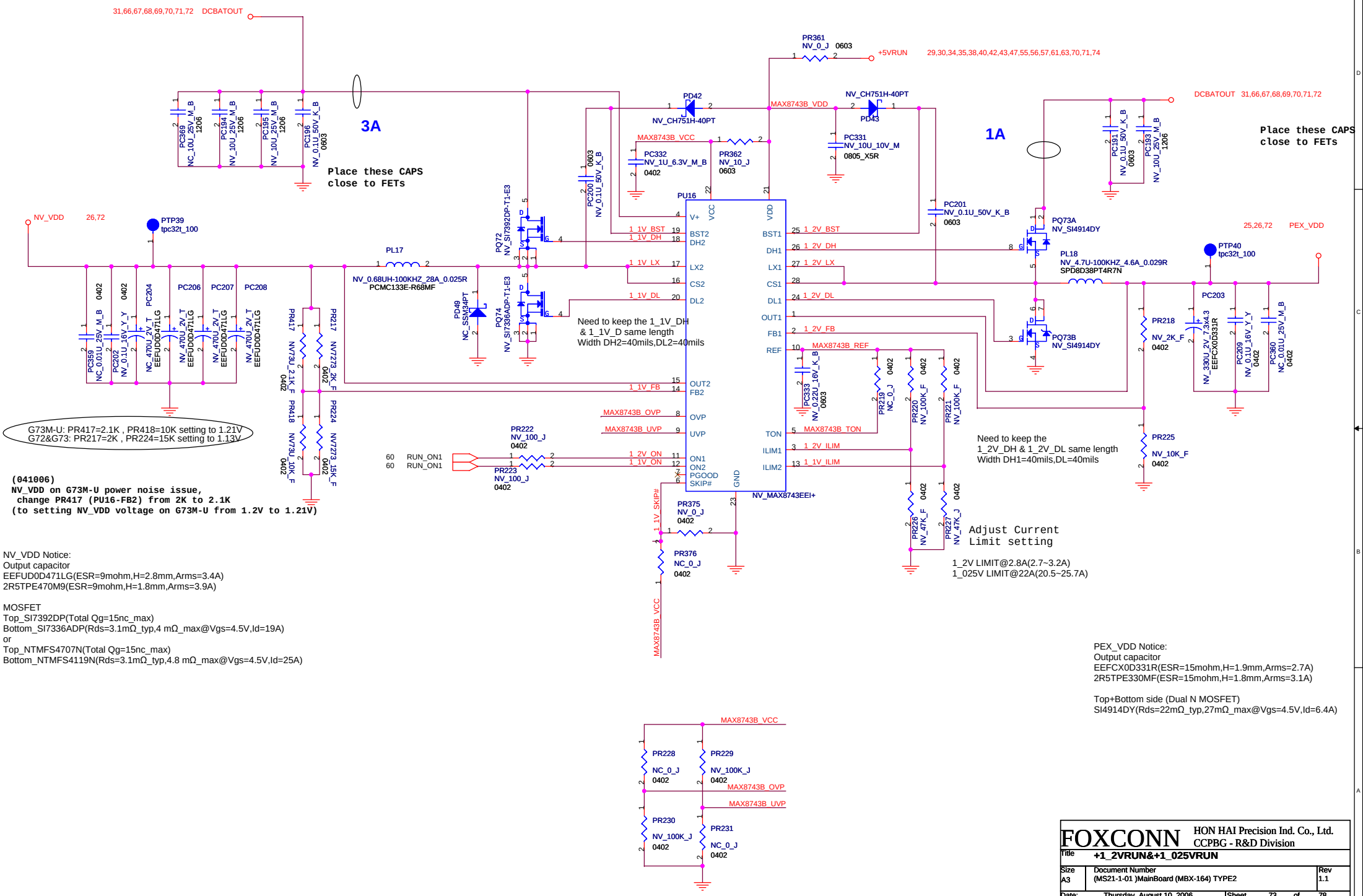


PQ1,PQ2,PQ3,PQ15 usage
SI4425BDY-T1-E3 (Rds=10mΩ_typ,12mΩ_max@Vgs=10V,Id=11.4A)
or
AOS4407(Rds=11mΩ_typ,14mΩ_max@Vgs=-10V,Id=-10A)









G73M-U: PR417=2.1K , PR418=10K setting to 1.21V
G72&G73: PR217=2K , PR224=15K setting to 1.13V

(041006)
NV_VDD on G73M-U power noise issue,
change PR417 (PU16-FB2) from 2K to 2.1K
(to setting NV_VDD voltage on G73M-U from 1.2V to 1.21V)

NV_VDD Notice:
Output capacitor
EEFUD0D471LG (ESR=9mohm,H=2.8mm,Arms=3.4A)
2R5TPE470M9 (ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
Top_Si7392DP (Total Qg=15nc_max)
Bottom_Si7336ADP (Rds=3.1mΩ_typ,4 mΩ_max@Vgs=4.5V,Id=19A)
or
Top_NTMFSA4707N (Total Qg=15nc_max)
Bottom_NTMFSA4119N (Rds=3.1mΩ_typ,4.8 mΩ_max@Vgs=4.5V,Id=25A)

PEX_VDD Notice:
Output capacitor
EEFCX0D331R (ESR=15mohm,H=1.9mm,Arms=2.7A)
2R5TPE330MF (ESR=15mohm,H=1.8mm,Arms=3.1A)

Top+Bottom side (Dual N MOSFET)
SI4914DY (Rds=22mΩ_typ,27mΩ_max@Vgs=4.5V,Id=6.4A)

2006/6/26

Modify Constant-Current SONY LOGO LED circuit

for U138 cost issue

- 1.Back up:U138(MAX1916EZT),R1936 (91K ohm,0402),R1982(0R,NC),R1983(0R,NC)
 - 2.Remove back up solution U139(GMT,G5920TB1UF),C1660(0.1u)
 - 3.Add new Constant-Current circuit (OP + MOS)
- 51K ohm: R1972 ,
1.2K ohm: R1973 ,
1k ohm:R1974 ,
10 ohm: R1975
(NC)0 ohm: R1976(for back up U138 MAX1916)
0.1uF,16V: C1679
(NC)22uF,6.3V: C1680
OP LM358 ADR : U139
N-MOS 2N7002: Q158
N-MOS DTA114YUA:Q159
P-MOS DTC144EUA:Q160

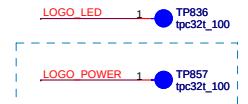
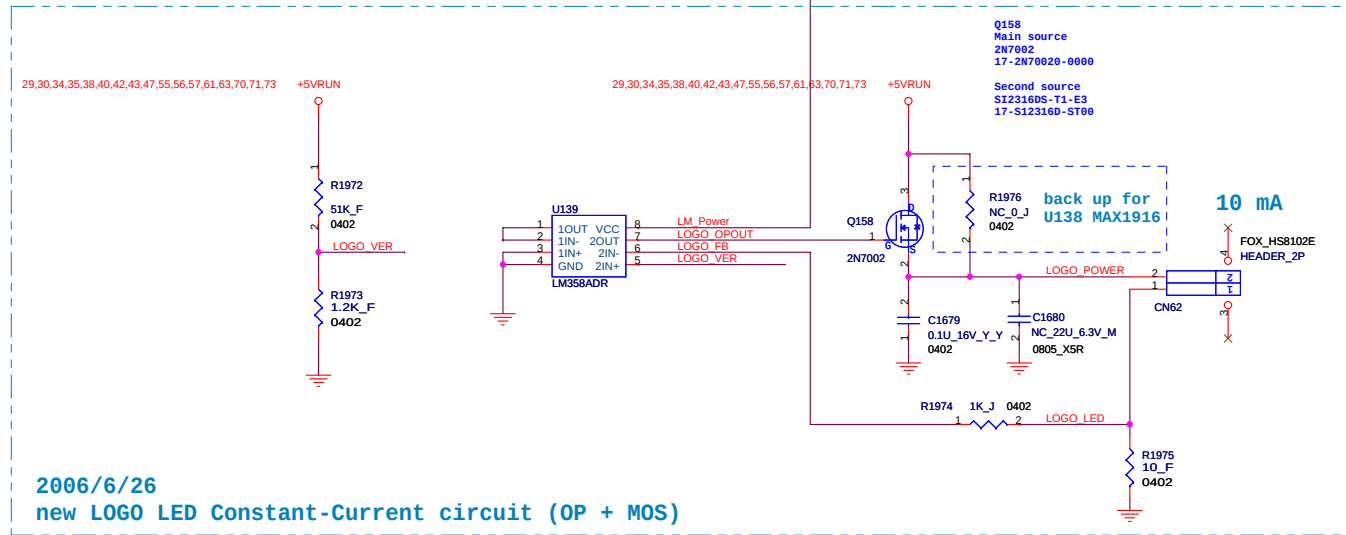
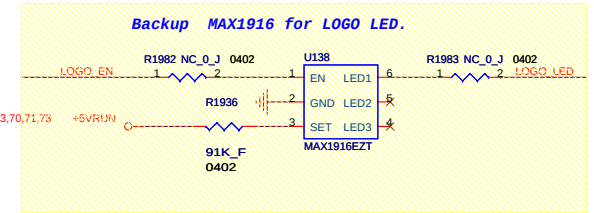
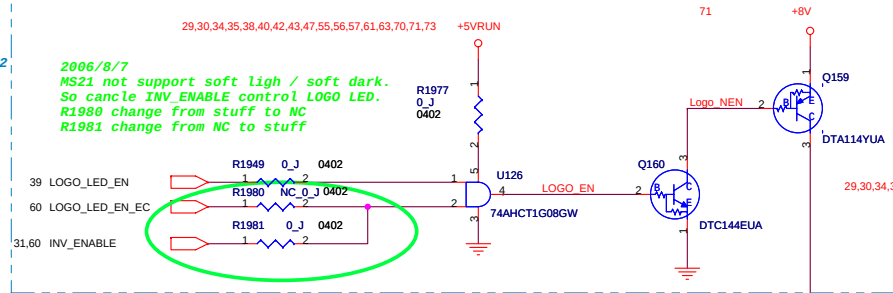
for EC control soft start/down (function up)issue

- 1.Del R1948(back up LOGO_LED_EN_EC to U126 pin1)
- 2.Serial (Back up) R1981 between INV_ENABLE to U126 pin2
- 3.Move net LOGO_LED_EN_EC from R1948 pin1 to R1980 pin1
- 4.Add R1977 between +5VRUN to U126 pin5(VCC)
- 5.Add R1980 between Logo_led_en_ec to U126 pin2

Constant-Current SONY LOGO LED

2006/6/26

EC & SB control soft start/down



2006/6/26
(1)remove TP835(GND Test Pad)
(2)add TP857(LOGO_POWER)

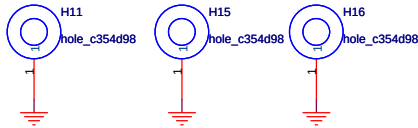
2006/6/26

(Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP)

Detail location

10U_25V_M*9pcs(PC380,PC381,PC382,PC383,PC384,PC385,PC386,PC389,PC390),
0.01U_25V_K*1pcs(PC387),1U_25V_M*1pcs(PC388),0.22U_16V_M*1pcs(PC391),
220P_50V_K*1pcs(PC392),SKS30-04AT-G*1pcs(PD53),8UH-100KHZ_2.5A_0.07R*1pcs(PL22),
2N7002*2pcs(PQ9114,PQ116),FDS6680A*1pcs(PQ117),120K_F*1pcs(PR432),
0.03_F*1pcs(PR434)95.3K_F*1pcs(PR435),10K_F*1pcs(PR436),MAX668EUB+T*1pcs(PU22),

HOLE Type 1



Type 2

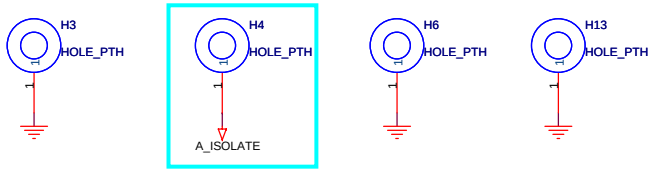
2005/10/24
Remove Screw Hole H2 P/N 1X-HOLE000-0108
because the Hole overlay with CN32 and layout will
modify component screw shipe

Type 3

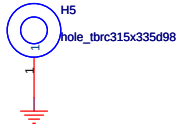
2005/10/24
Remove Screw Hole H1 P/N 1X-HOLE000-0110
because the Hole overlay with CN32 and layout will
modify component screw shipe

2006/5/6
Separet analog ground for digital Noise issue:
Isolate screw hole H4 Change H4 net name from
A_GND to A_ISOLATE

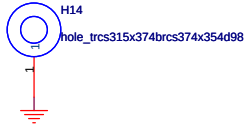
Type 4



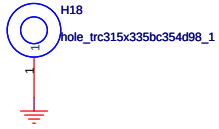
Type 5



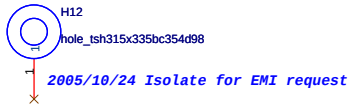
Type 6



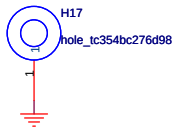
Type 7



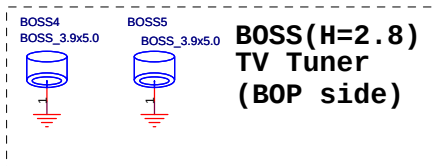
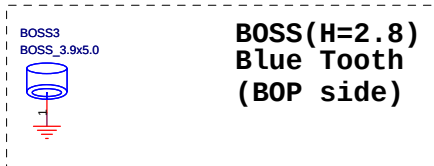
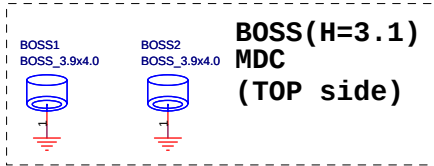
Type 8



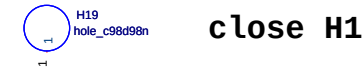
Type 9



Type CPU



Type NPTH Guide (spherical)HOLD



Type NPTH Guide (oval-shaped)HOLD



MS20 MP to MS21 DVT Change History

(2006/5/23)

- (川) 01.(Page08) Remove R110 for PM_EXTTS#1 back up pull up res.ICH7 (DPRSLPVR)already have internal pull up
- (川) 02.(Page14) Remove backup DIMM thermal senser Change R168 from stuff to NC(basis on MS20 MP ECR)
- (川) 03.(Page15) Remove backup DIMM thermal senser Change R1627 from stuff to NC(basis on MS20 MP ECR)
- (蘭) 04.(Page34) US Silicon Image ATC test HDMT DDC capacitance fail(>50pF)change U128 no stuff Basis on MS20 MP ECR
add back up res.(R1962)no stuff for U128 VCC
- (才) 05.(Page39) Delete U30,R1183,R649 (backup circuit)
- (寶) 06.(Page42) For power droup cause 0.16V voltage loss Issue(1)F7,F8,F19,F20 no stuff(2)Co-layout GP17-GP20 with fuse
- (業) 07.(Page55) Separet analog ground for digital Noise issue
(1)Add bead (L152)before L00 chipand
(2)Change C873 from GND to A_GND
(3)Add C1675 on +5VRUN before L152
- (業) 08.(Page56) Shoe1 CAP will EOL. CAP24,CAP25(SP CAP) change to Stuff; CAP22,CAP23(Shoe1 CAP) change to No Stuff
- (業) 09.(Page56) PBSS2515F.115 will EOL ,Q77,Q78,Q143,Q144 change to PBSS2515E.115
- (業) 10.(Page56) Improve the voice of speaker up to 0.94W
(1)Add damping Resistors R1953 on SRIN,R1954 on AMP_SLIN then speaker amp output won't be distorted.
(2)Change R1932 from 6.8K to 5.6K, then amp gain change from 8dB to 10dB.
- (業) 11.(Page57) PBSS2515F.115 will EOL Q89,Q90,Q91,Q92 change to PBSS2515E.115
- (業) 12.(Page59) Improve SNR issue,Add 1uF capacitors close CN64 :C1671,C1672 on USB_VCC2,C1669 on +3VRUN_AUDIO_BD, and C1670 on VDDA .
- (業) 13.(Page59) Separet analog ground for digital Noise issue:
(1)Remove GP3 (Close Jumper)not bridge between GND and A_GND
(2)Backup two jumper resistors for bridge between GND and A_GND
(C1388,C1966 on Screw hole H3,C1957,C1959 on screw hole H5)
(3)Isolate screw hole H4,add 100pF capacitors C1673,C1674 for EMI,Zener diode D100 for ESD
(4)Add jumper resistor for Return patch R1955 close L70(+5VAMP) & R1960 close codec
- (才) 14.(Page39) Remove back up circuit LVDS GPIO on U29 pinU2(1)Add Test Pad TP890 on GPIO32(4)Del Q126
- (寶) 15.(Page54) Remove back up F6 power source from +3VALW (Del)R1944,R1946
- (才) 16.(Page67) Reserve PC64(10U_25V_M_B 1206) for 1210 size shortage. Change PR57 from 0805 size to 0603 size for 0603 size rated current is also enough.
- (青) 17.(Page70) Add PC375 (0.1uF) to avoid IMVP_OK signal 780mV pulse when power on. Change PC107/PC108 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- (青) 18.(Page71) Change PC164/PC165 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- (青) 19.(Page71) Change PC368 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage. Change PU12 from LMC7225IM5X to NCS2202SN1T16 for LMC7225IM5X shortage.
- (才) 20.(Page60) Modify system ID setting. R725 from stuff change to NC,R726 from NC change to stuff
- (蘭) 21.(Page32) CN66,CN67 Change from MOLEX(1N-0010000-MWG0) to FOXCONN(1N-0010000-F0T0)
- (寶) 22.(Page63) CN68 Change from MOLEX(1N-0010000-MWG0) to FOXCONN(1N-0010000-F0T0)
- (業) 23.(Page57) Add C1676 (4.7 uF/bupass cap) close A_ U99 pin8
- (業) 24.(Page58) Add C1677,C1678 (4.7 uF/bupass cap) close A_ U101,U102 pin8
- (青) 25.(Page74) Add Inverter Boost Circuit

(2006/5/24)

- (業) 1.(Page55) According to MOR suggest Change Int MIC topology from single end to differential
(1) C1251 change from 33pF 0402 to 1uF 0603
(2) C1252 change from 12pF 0402 to 1uF 0603
(3) C1270 change from 0.1F 0402 to 1uF 0603
(4) Add R1967, R1968 100 ohm 0402
- 2.(Page57) According to MOR suggest Change Int MIC topology from single end to differential
(1) C1231 change from 4.7uF 0805 to 220pF 0402
(2) C1232 change from 1uF 0805 to 4.7uF 0805
(3) C1233 change from 4.7uF 0805 to NC_33pF 0402
(4) C1234 change from 100pF 0402 to NC_33pF 0402
(5) C1237 change from 100pF 0402 to 33pF 0402
(6) R1318 change from 10Kohm 0402 to 5.1Kohm 0402
(7) R1319 change from 1Kohm 0402 to 4.7Kohm 0402
(8) R1320 change from 33ohm 0402 to 100ohm 0402
(9) R1321 change from NC_0ohm 0402 to 4.7Kohm 0402
(10) R1325 change from 47Kohm 0402 to 4.7Kohm 0402
(11) R1326 change from 7.5Kohm 0402 to 2.2Kohm 0402
(12) R1327 change from 100ohm 0402 to 1Kohm 0402
(13) Add R1970, R1971 100 ohm 0402
(14) Add R1969 4.7 Kohm 0402
(15) R1236 change from 4.7u to 1u

(2006/5/26)

- (業) (1) C1230 change from 2200pF to 4700 pF by MOR request

MS21 DVT to MS21 PVT Change History

(2006/6/26)

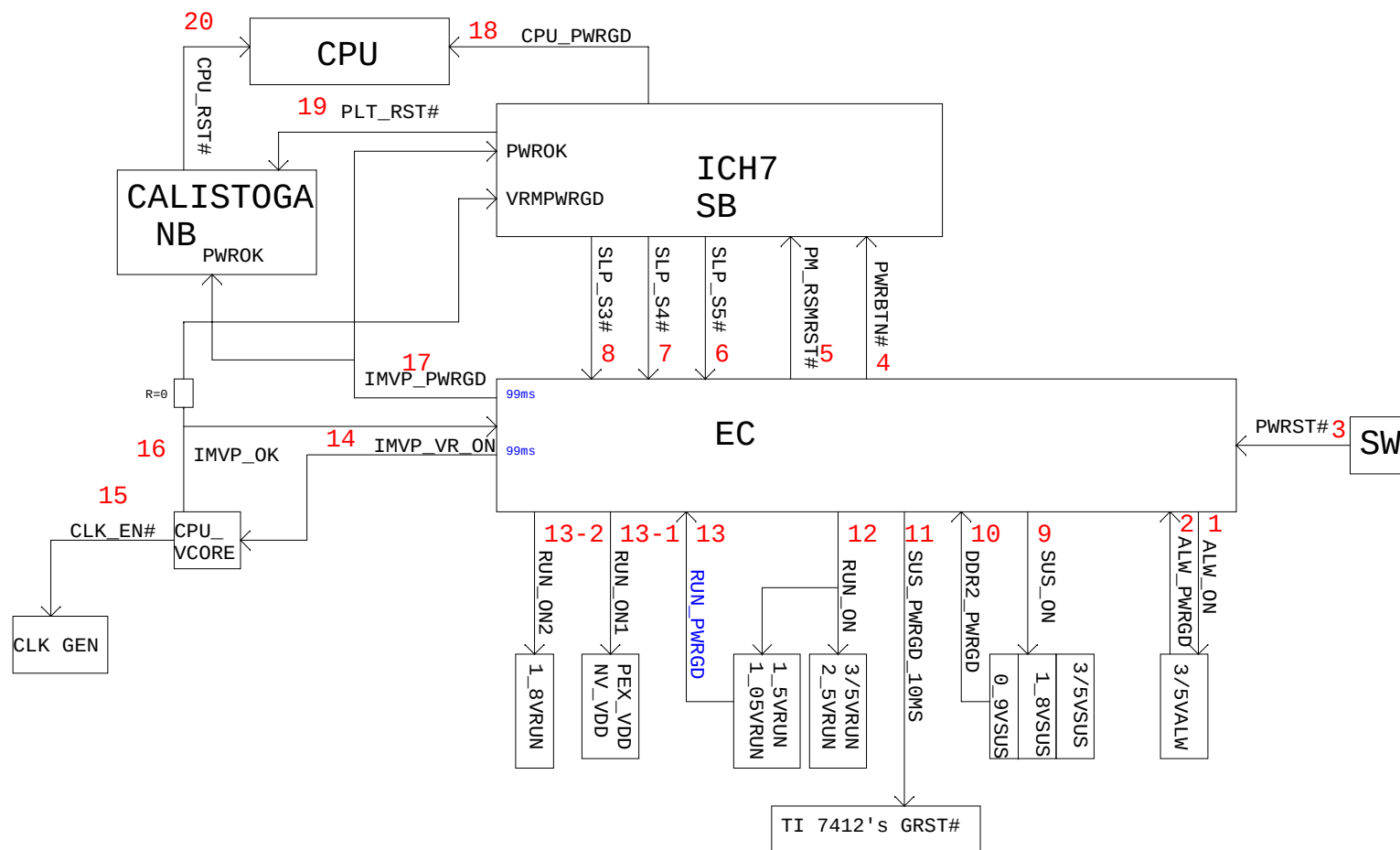
- (才) 01.(Page60) Solve Doi san concern EC's GPIO23 is CMOS out and if BTR drive it to GND it may damage the EC.
(1)Change R1762 from 0 to 1K ohm,
(2)Change net name R1762-2 from N18386242 to EC_GPIO23
(3)Change net name R690-1 from ALW_ON to EC_GPIO23
- (蘭) 02.(Page31) Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP
(1)Delete PR426&PR427
(2)change C604-1,C1557-1,C1558-1,CN49 pin1,pin2 net name INVERTER_VCC to net DCBATOUT.
- (寶) 03.(Page74) Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP
Delete 10U_25V_M*1pcs(PC380,PC381,PC382,PC383,PC384,PC385,PC386,PC389,PC390),
0.01U_25V_K*1pcs (PC387),1U_25V_M*1pcs(PC388),0.22U_16V_M*1pcs(PC391),
220P_50V_K*1pcs(PC392),SKS30-04AT-G*1pcs(PD53),8UH-100KHZ_2.5A_0.07R*1pcs(PL22),
2N7002*2pcs(PQ114,PQ116),FD56680A*1pcs(PQ117),120K_F*1pcs(PR432),
0.03_F*1pcs(PR434)95.3K_F*1pcs(PR435),10K_F*1pcs(PR436),MAX668EUB+T*1pcs(PU22),
100K_J*1pcs (PR428) 100K_J*1pcs (PR429)
- (青) 04.(Page67)Change PR53&PR55 from 100_J to 0_J by Mor side suggestion
Original PR53&PR55(100ohm) is used as current limit.But now we have added series 1K ohm,
(Page 60, change R1762 from 0 ohm to 1K ohm) So we need not 100ohm resistor for curret limit
- (業) 05.(Page56) Modify internal speaker AMP gain setting,change R1953/R1954 from 4.7K (AMP output 1.12W) to 5.1Kohm(AMP output0.98w) to fit in speaker (1.0W)spec.
- (業) 06.(Page57) Modify internal MIC AMP gain setting,change R1318 from 5.1K to 5.9K ohm, To lead TYPE2 board gain (differential type MIC)the same with TYPE1 board single end MIC) (Gain=9.2)
- (才) 07.(Page60) Modify Constant-Current SONY LOGO LED circuit for EC control soft start/down (function up)issue
(1).Del back up Test Pad TP864
(2).Add R1978 (0 ohm) link EC pin176 and INV_ENABLE
- (寶) 08.(Page74) Modify Constant-Current SONY LOGO LED circuit
A.for U138 cost issue
1.Back up:U138(MAX1916EZT),R1936 (91K ohm,0402),R1982(0R,NC),R1983(0R,NC)
2.Remove back up solution U139(GMT,G5920TB1uF),C1660(0.1u)
3.Add new Constant-Current circuit (OP + MOS)
51K ohm: R1972 ,
1.2K ohm: R1973 ,
1k ohm:R1974
10 ohm: R1975
(NC)0 ohm: R1976(for back up U138 MAX1916)
0.1uF,16V: C1679
(NC)22uF,6.3V: C1600
OP LM358 ADP : U139
N-MOS 2N7002: Q158
N-MOS DTA114YUA:Q159
P-MOS DTC144EUA:Q160

B.for EC control soft start/down (function up)issue
1.Del R1948(back up LOGO_LED_EN_EC to U126 pin1)
2.Serial (Back up) R1981 between INV_ENABLE to U126 pin2
3.Move net LOGO_LED_EN_EC from R1948 pin1 to R1980 pin1
4.Add R1977 between +5VRUN to U126 pin5(VCC)
5.Add R1980 between Logo_led_en_ec to U126 pin2
- (寶) 09.(Page 42) Delete SATA HDD Fuse backup circuit
(1)Remove F7,F8,F19,F20 Pad
(2)Remove GP17-GP18 open gap
- (才) 10. (Page 62) MOR fan circuit modify to backup
(NC)U118 (NC)R1893
(NC)R1624 (NC)C1473
(NC)R1894 (NC)R1895

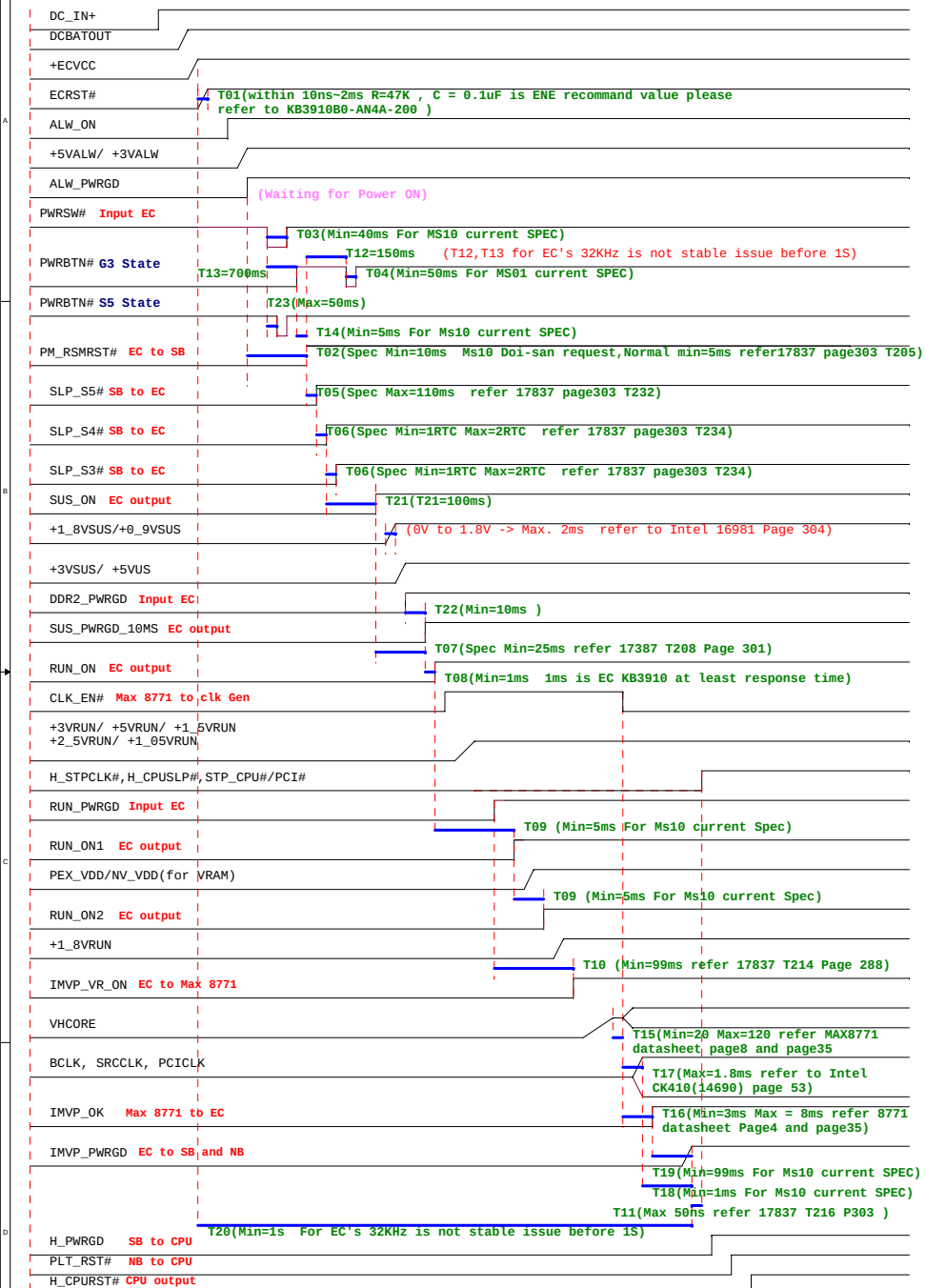
MS21 PVT to MS21 MP Change History

- (寶) 01.(Page74) MS21 not support soft ligh / soft dark. So cancle INV_ENABLE control LOGO LED.
R1900 change from stuff to NC
R1981 change from NC to stuff
- (才) 02.(Page60) MS21 not support soft ligh / soft dark. So cancle INV_ENABLE control LOGO LED.
R1978 Change from stuff to NC
- (業) 03.(Page57) Change C1676 from stuff to NC for MOR suggestion Cost down request.
- (青) 04.(Page66) At MS21 PCN1 used FOXCONN connector, Change PCN1 Vendor from molex to NWING
- (良) 05.(Page29) Change D60,D61,D81 Value from NV to Normal
- (良) 06.(Page20) Change Y2 Value from Normal to NV

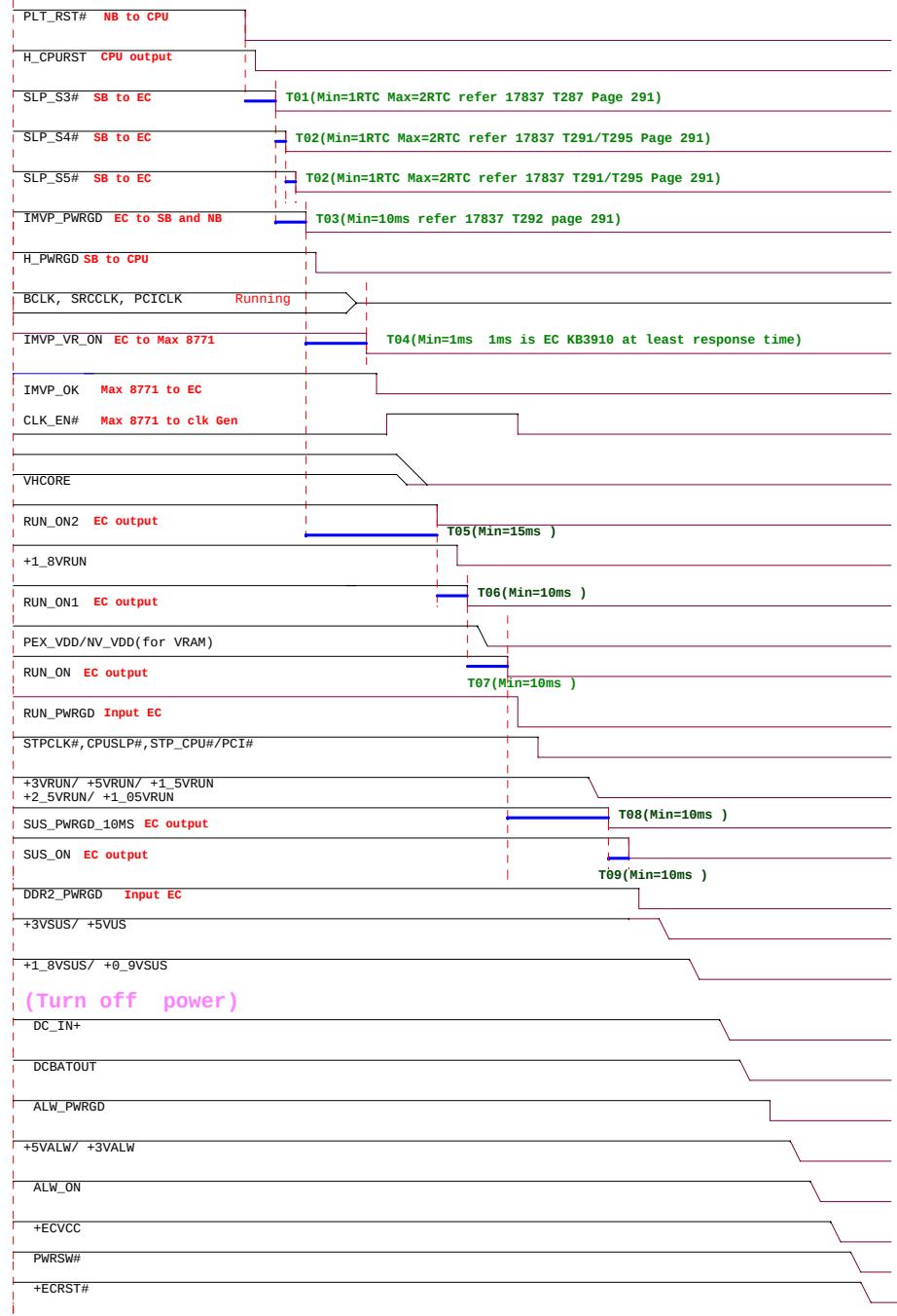
MS21 Power On Sequence Block Diagram



Power On/Off Sequence Specification



T01	T02	T03	T04	T05	T06	T07	T08	T09	T10	T11	
within 10ns-2ms	Min. 10 ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCLK	Min. 25 ms	Min. 1ms	Min. 10ms	Min. 99ms	Max. 50ms	
T12	T13	T14	T15	T16	T17	T18	T19	T20	T21	T22	T23
Min. 150ms	Min 700ms	Min 5ms	Min : 20us Max : 120us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min. 99ms	Min. 1s	100ms	Min. 10ms	Max 50ms



T01	T02	T03	T04	T05	T06	T07	T08	T09
1 - 2 RTCLK	1 - 2 RTCLK	Min. 10ms	Min. 1ms	Min. 15ms	Min. 10ms	Min. 10ms	Min. 10ms	Min. 10ms