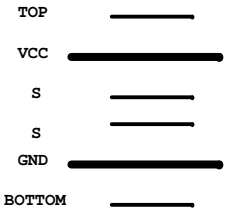
JV42-DN Block Diagram

Project code: 91.4HD01.001
PCB P/N : 48.4GX01.0SA
PCB 版號 : 09919 SA
REVISION : PCB STACKUP



DDR3 16,17 — 800/1066/1333MHz
DDR3 800/1066/1333 MHz 16,17 — 800/1066/1333MHz
AMD Champlain CPU S1G4 (45W)
638-Pin uFCPGA638 4,5,6,7
OUT / IN — HT 3.0 16X16

CLK GEN. 3
ICS9LPRS480BKLFT 71.09480.A03
RTM880N-796-VB-GRT 71.00880.A03

North Bridge
AMD RS880M
CPU I/F LVDS, CRT I/F
INTEGRATED GRAHPICS
8,9,10

16X — PCI EXPRESS GRAPHIC

CRT 20
LCD 19
HDMI 21

Madison
ATI
53,54,55,56,57

DDR3 VRAM 58, 59, 60, 61

LAN Giga LAN BCM57780 26
TXFM 27
RJ45 27

PCIex1 — Mini Card WLAN 33

A-Link 4X1

South Bridge
AMD SB820
USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
ATA 66/100
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
11,12,13,14,15

INT MIC 30 — Codec ALC272 28 — AZALIA
MIC In 30
INT.SPKR 30 — OP AMP 29 — Line Out
30

LPC BUS
KBC Novoton NPCE781B 36
BIOS MXIC MX25L1605 37
LPC DEBUG CONN. 37
Touch Pad 38
INT. KB 36

SATA
HDD SATA 22
ODD SATA 23

USB
Mini USB Blue Tooth 24
USB 3 Port 25
Camera
CardReader AU6433 32
MS/MS Pro/xD /MMC/SD 5 in 1 32

Daughter Board USB Board
Daughter Board PWR+LED Board

SYSTEM DC/DC RT8223 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5.5A) 3D3V_S5(5A)

SYSTEM DC/DC RT8209E 47	
5V_S5	1D5V_S3(14A)
RT9026 47	
5V_S5	0D75_S3(1.2A)

SYSTEM DC/DC RT8209E 48	
INPUTS	
DCBATOUT	1D1V_S0(11A)
RT9025 48	
3D3V_S5	1D1V_S5(1.4A)

RT9025 49	
5V_S5	1D1V_VGA
RT9161 49	
3D3V_S0	2D5V_S0 (200mA)
RT9025 49	
1D5V_S3	1D05V_S0 (1.4A)

CHARGER BQ24745 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.55V 18A VDDNB 0~1.55V 4A

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: JV42-DN | Rev: SA
Date: Wednesday, November 18, 2009 | Sheet 1 of 63

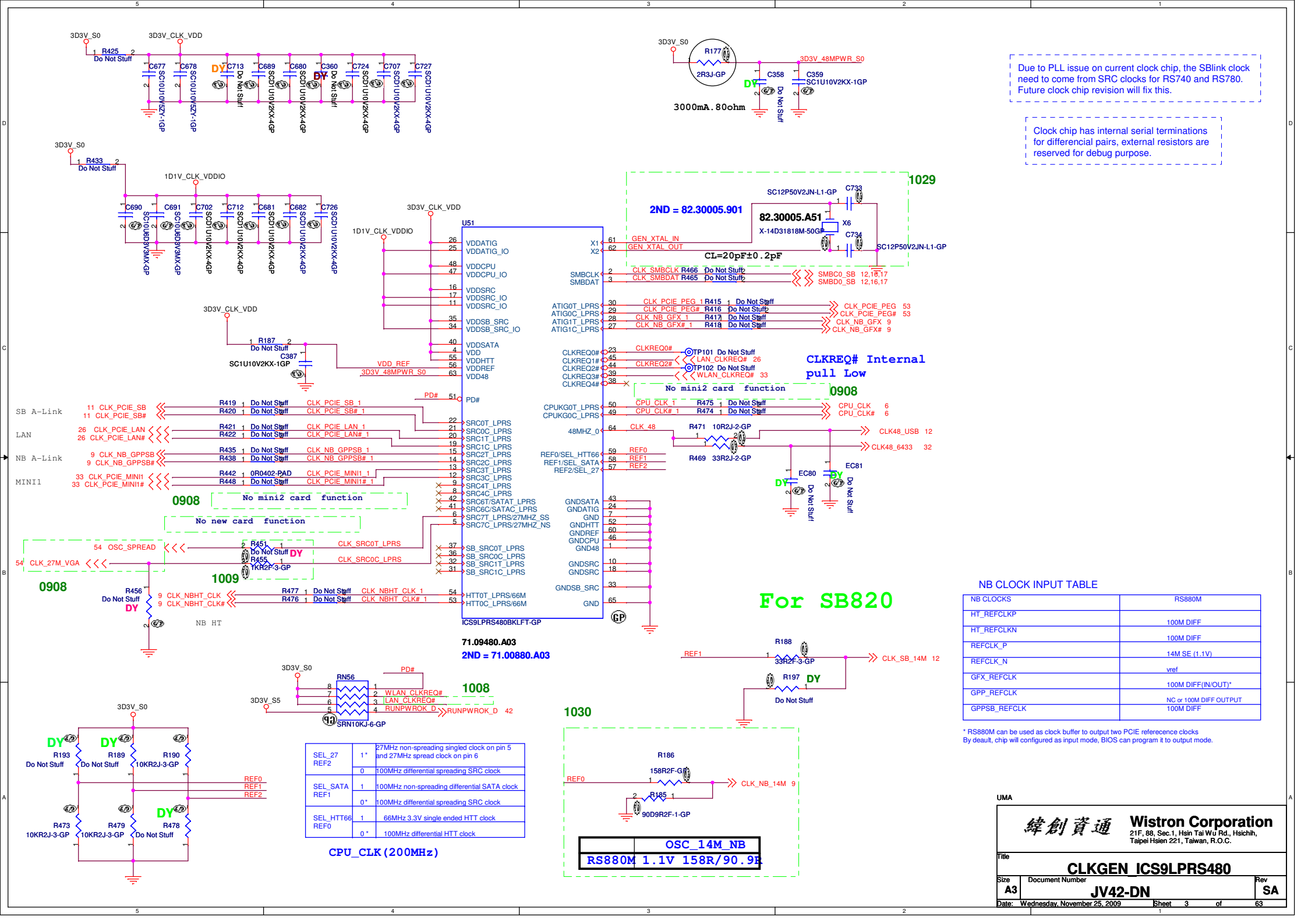
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **History**

Size	Document Number	Rev
A3	JV42-DN	SA

Date: Thursday, November 05, 2009 Sheet 2 of 63

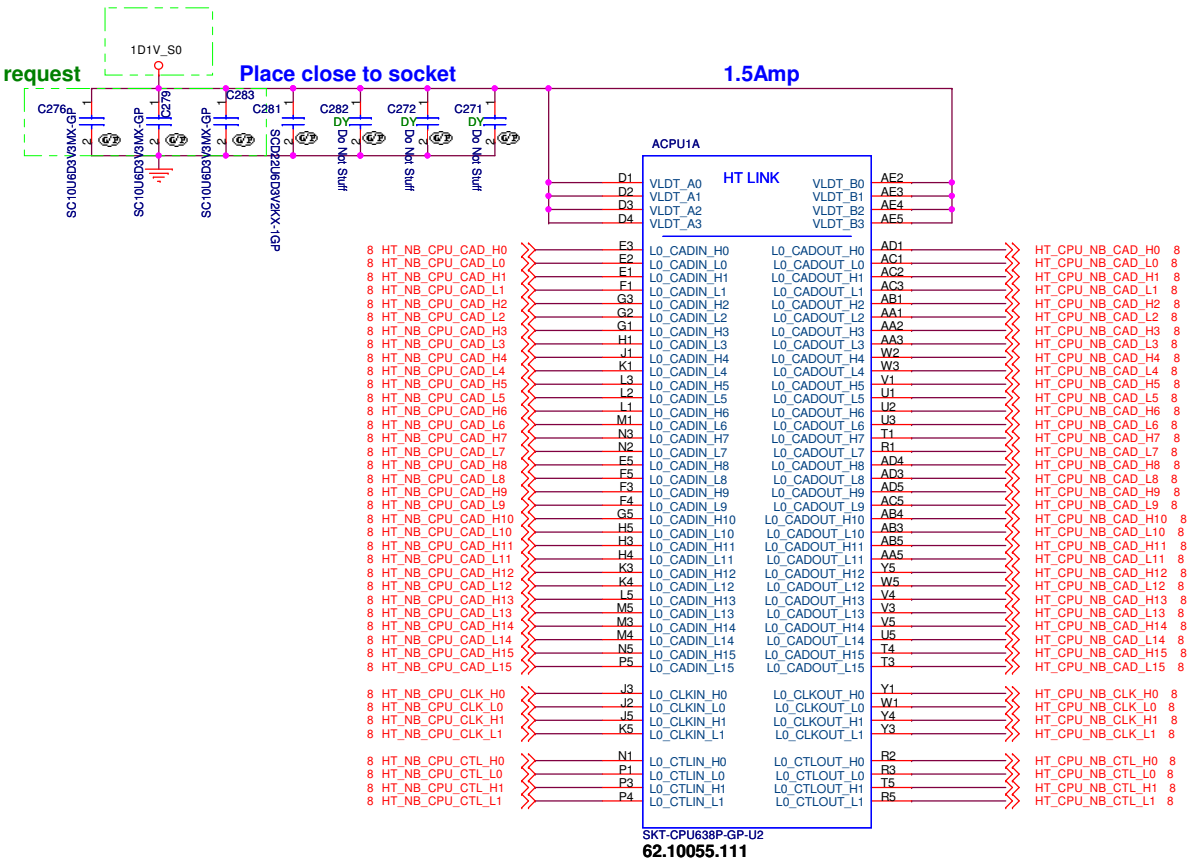

3D3V_S0
3D3V_CLK_VDD
R425 Do Not Stuff
C677 SC10U10V5ZY-1GP
C678 SC10U10V5ZY-1GP
DY C713 Do Not Stuff
C689 SCD1U10V2KX-4GP
C680 SCD1U10V2KX-4GP
DY C360 Do Not Stuff
C724 SCD1U10V2KX-4GP
C707 SCD1U10V2KX-4GP
C727 SCD1U10V2KX-4GP
3D3V_S0
R177 2R3J-GP
3D3V_48MPWR_S0
DY C358 Do Not Stuff
C359 SC1U10V2KX-1GP
3000mA.80ohm
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.
3D3V_S0
R433 Do Not Stuff
1D1V_CLK_VDDIO
C690 C691 C702 C712 C681 C682 C726
SCD1U06D3V3MX-GP
SCD1U10V2KX-4GP
3D3V_CLK_VDD
1D1V_CLK_VDDIO
U51
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDD
VDDHTT
VDDREF
VDD48
PD#
SRC0T_LPRS
SRC0C_LPRS
SRC1T_LPRS
SRC1C_LPRS
SRC2T_LPRS
SRC2C_LPRS
SRC3T_LPRS
SRC3C_LPRS
SRC4T_LPRS
SRC4C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
SRC7T_LPRS/27MHZ_SS
SRC7C_LPRS/27MHZ_NS
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
HTT0T_LPRS/66M
HTT0C_LPRS/66M
GNDSATA
GNDATIG
GND
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSRC
GNDSB_SRC
GND
ICS9LPRS480BKLFT-GP
X1
X2
GEN_XTAL_IN
GEN_XTAL_OUT
SMBCLK
SMBDAT
ATIG0T_LPRS
ATIG0C_LPRS
ATIG1T_LPRS
ATIG1C_LPRS
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
CPUKG0T_LPRS
CPUKG0C_LPRS
48MHZ_0
REF0/SEL_HTT66
REF1/SEL_SATA
REF2/SEL_27
1029
2ND = 82.30005.901
82.30005.A51
SC12P50V2JN-L1-GP
C733
X6
X-14D31818M-50GP
C734
CL=20pF±0.2pF
CLK_SMBCLK R466 Do Not Stuff
CLK_SMBDAT R465 Do Not Stuff
SMBC0_SB 12,16,17
SMBD0_SB 12,16,17
CLK_PCIE_PEG_1 R415 Do Not Stuff
CLK_PCIE_PEG# R416 Do Not Stuff
CLK_NB_GFX_1 R417 Do Not Stuff
CLK_NB_GFX#_1 R418 Do Not Stuff
CLK_PCIE_PEG 53
CLK_PCIE_PEG# 53
CLK_NB_GFX 9
CLK_NB_GFX# 9
CLKREQ# Internal pull Low
CLKREQ0# TP101 Do Not Stuff
CLKREQ2# TP102 Do Not Stuff
LAN_CLKREQ# 26
WLAN_CLKREQ# 33
No mini2 card function
0908
CPU_CLK_1 R475 Do Not Stuff
CPU_CLK#_1 R474 Do Not Stuff
CPU_CLK 6
CPU_CLK# 6
CLK_48
R471 10R2J-2-GP
R469 33R2J-2-GP
CLK48_USB 12
CLK48_6433 32
EC80 DY Do Not Stuff
EC81 DY Do Not Stuff
3D3V_CLK_VDD
R187 Do Not Stuff
C387 SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
SB A-Link
LAN
NB A-Link
MINI1
R419 R420 Do Not Stuff CLK_PCIE_SB_1 CLK_PCIE_SB#_1
11 CLK_PCIE_SB
11 CLK_PCIE_SB#
R421 R422 Do Not Stuff CLK_PCIE_LAN_1 CLK_PCIE_LAN#_1
26 CLK_PCIE_LAN
26 CLK_PCIE_LAN#
R435 R438 Do Not Stuff CLK_NB_GPPSB_1 CLK_NB_GPPSB#_1
9 CLK_NB_GPPSB
9 CLK_NB_GPPSB#
R442 0R0402-PAD CLK_PCIE_MINI1_1
R448 Do Not Stuff CLK_PCIE_MINI1#_1
33 CLK_PCIE_MINI1
33 CLK_PCIE_MINI1#
0908
No mini2 card function
No new card function
54 OSC_SPREAD
54 CLK_27M_VGA
R451 Do Not Stuff
R455 1K2R2-3-GP
DY
CLK_SRC0T_LPRS
CLK_SRC0C_LPRS
1009
0908
R456 Do Not Stuff DY
9 CLK_NBHT_CLK
9 CLK_NBHT_CLK#
NB HT
R477 R476 Do Not Stuff CLK_NBHT_CLK_1 CLK_NBHT_CLK#_1
71.09480.A03
2ND = 71.00880.A03
For SB820
3D3V_S0
3D3V_S5
RN56
PD#
WLAN_CLKREQ#
LAN_CLKREQ#
RUNPWROK_D
RUNPWROK_D 42
SRN10KJ-6-GP
1008
R188 33R2F-3-GP
REF1
CLK_SB_14M 12
R197 DY Do Not Stuff
1030
R186 158R2F-GP
REF0
CLK_NB_14M 9
R185 90D9R2F-1-GP
OSC_14M_NB
RS880M 1.1V 158R/90.9R
3D3V_S0
DY R193 Do Not Stuff
DY R189 Do Not Stuff
R190 10KR2J-3-GP
REF0
REF1
REF2
R473 10KR2J-3-GP
R479 10KR2J-3-GP
DY R478 Do Not Stuff
SEL_27 REF2
1* 27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
0 100MHz differential spreading SRC clock
SEL_SATA REF1
1 100MHz non-spreading differential SATA clock
0* 100MHz differential spreading SRC clock
SEL_HTT66 REF0
1 66MHz 3.3V single ended HTT clock
0* 100MHz differential HTT clock
CPU_CLK(200MHz)
NB CLOCK INPUT TABLE
NB CLOCKS | RS880M
HT_REFCLKP | 100M DIFF
HT_REFCLKN | 100M DIFF
REFCLK_P | 14M SE (1.1V)
REFCLK_N | vref
GFX_REFCLK | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF
* RS880M can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CLKGEN_ICS9LPRS480
Size A3
Document Number JV42-DN
Rev SA
Date: Wednesday, November 25, 2009
Sheet 3 of 63

0904

1027 For AMD review request

Place close to socket

1.5Amp



SKT-BGA638H176

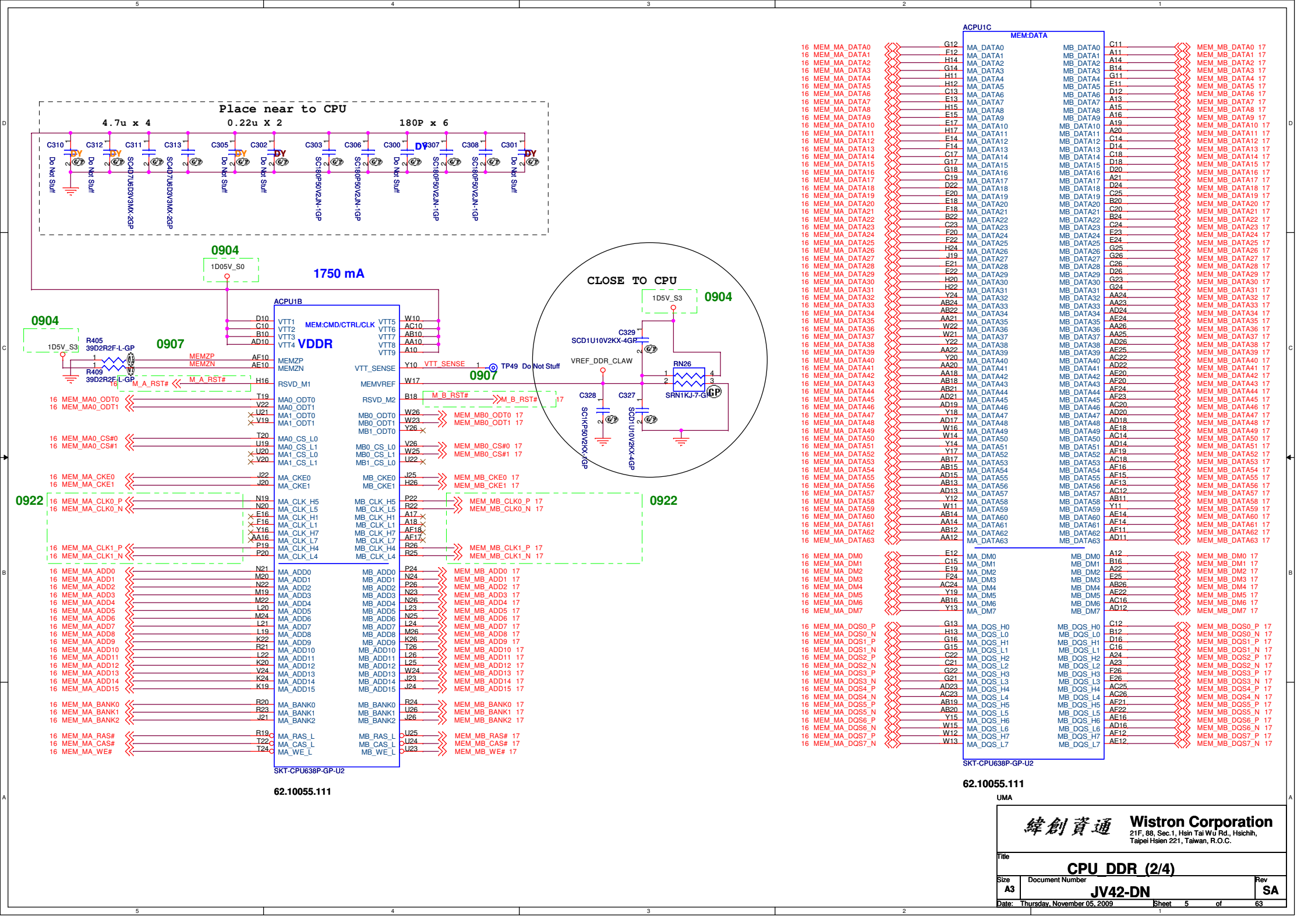
UMA

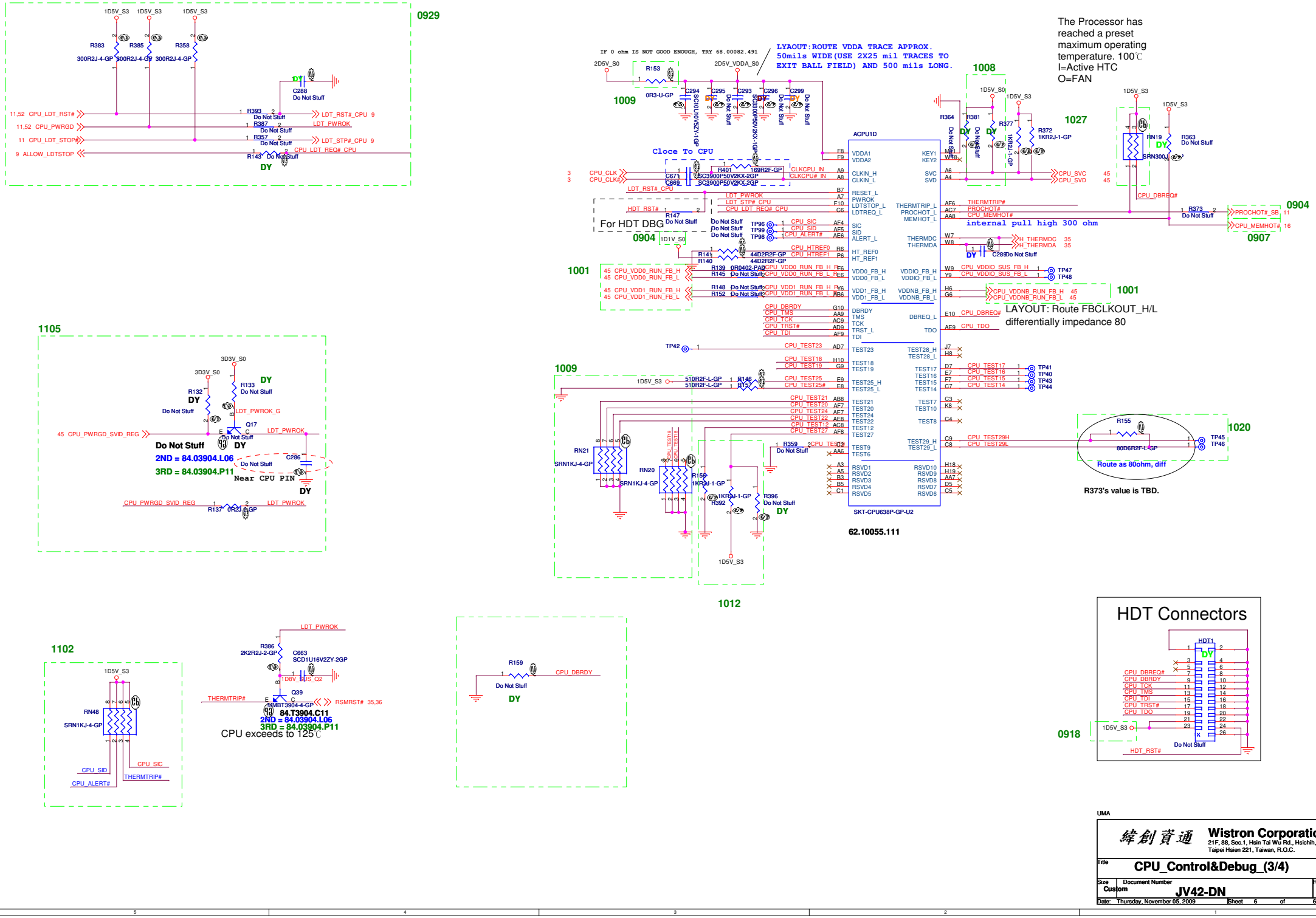
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_HT_LINK I/F_(1/4)

Size: A3 | Document Number: JV42-DN | Rev: SA

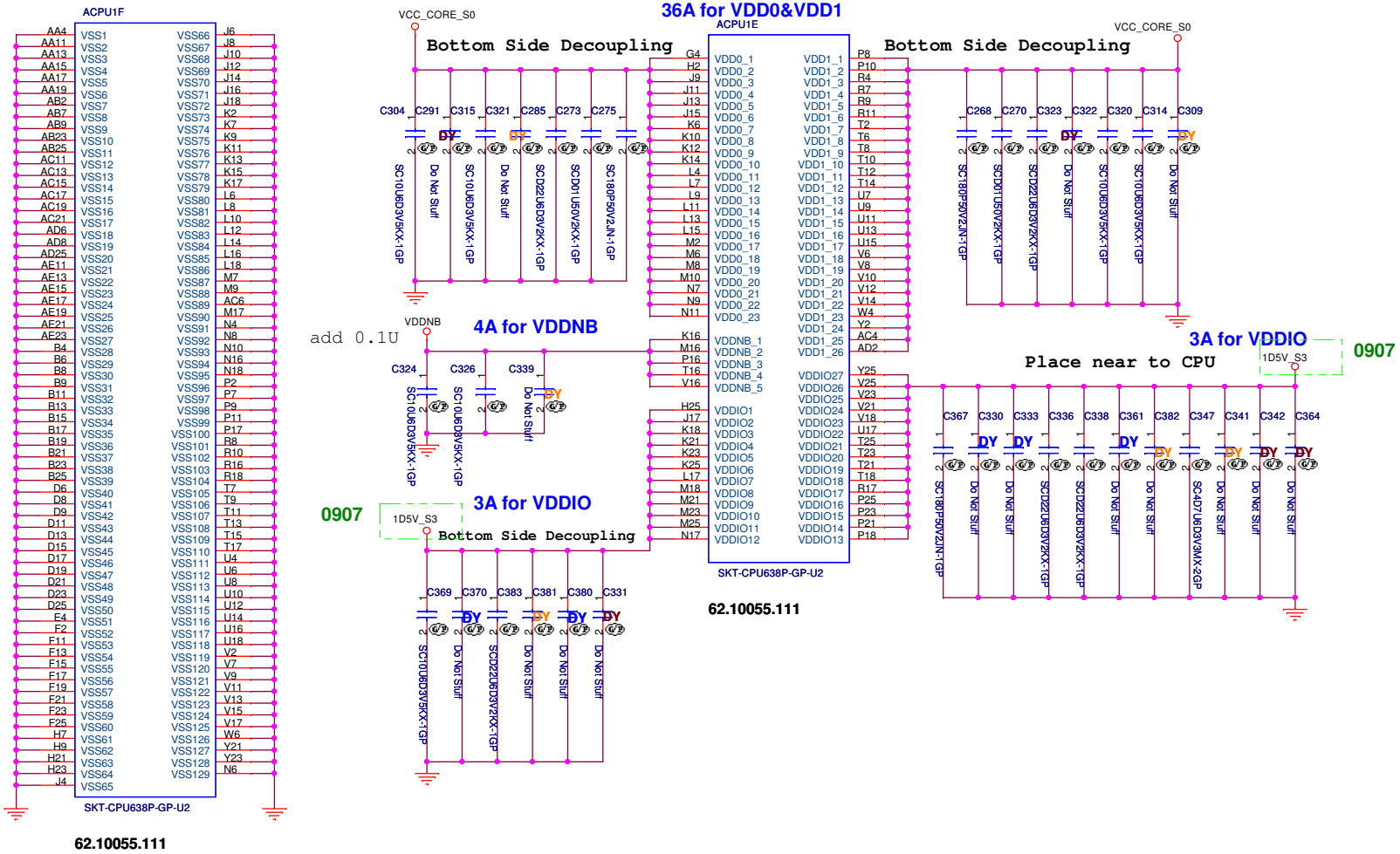
Date: Thursday, November 05, 2009 | Sheet 4 of 63


Place near to CPU
4.7u x 4
0.22u X 2
180P x 6
C310
C312
C311
C313
C305
C302
C303
C306
C300
C307
C308
C301
DY
Do Not Stuff
SC407U6D3V3MX-2GP
SC180P50V2JN-1GP
0904
1D05V_S0
1750 mA
ACPU1B
MEM:CMD/CTRL/CLK
VDDR
0907
R405
R409
39D2R2F-L-GP
MEMZP
MEMZN
M_A_RST#
M_B_RST#
VTT_SENSE
TP49 Do Not Stuff
CLOSE TO CPU
1D5V_S3
C329
SCD1U10V2KX-4GP
VREF_DDR_CLAW
RN26
SRN1KJ-7-GP
C328
C327
SC1KP50V2KX-2GP
SCD1U10V2KX-4GP
0922
SKT-CPU638P-GP-U2
62.10055.111
ACPU1C
MEM:DATA
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU_DDR_(2/4)
Size
A3
Document Number
JV42-DN
Rev
SA
Date: Thursday, November 05, 2009
Sheet 5 of 63



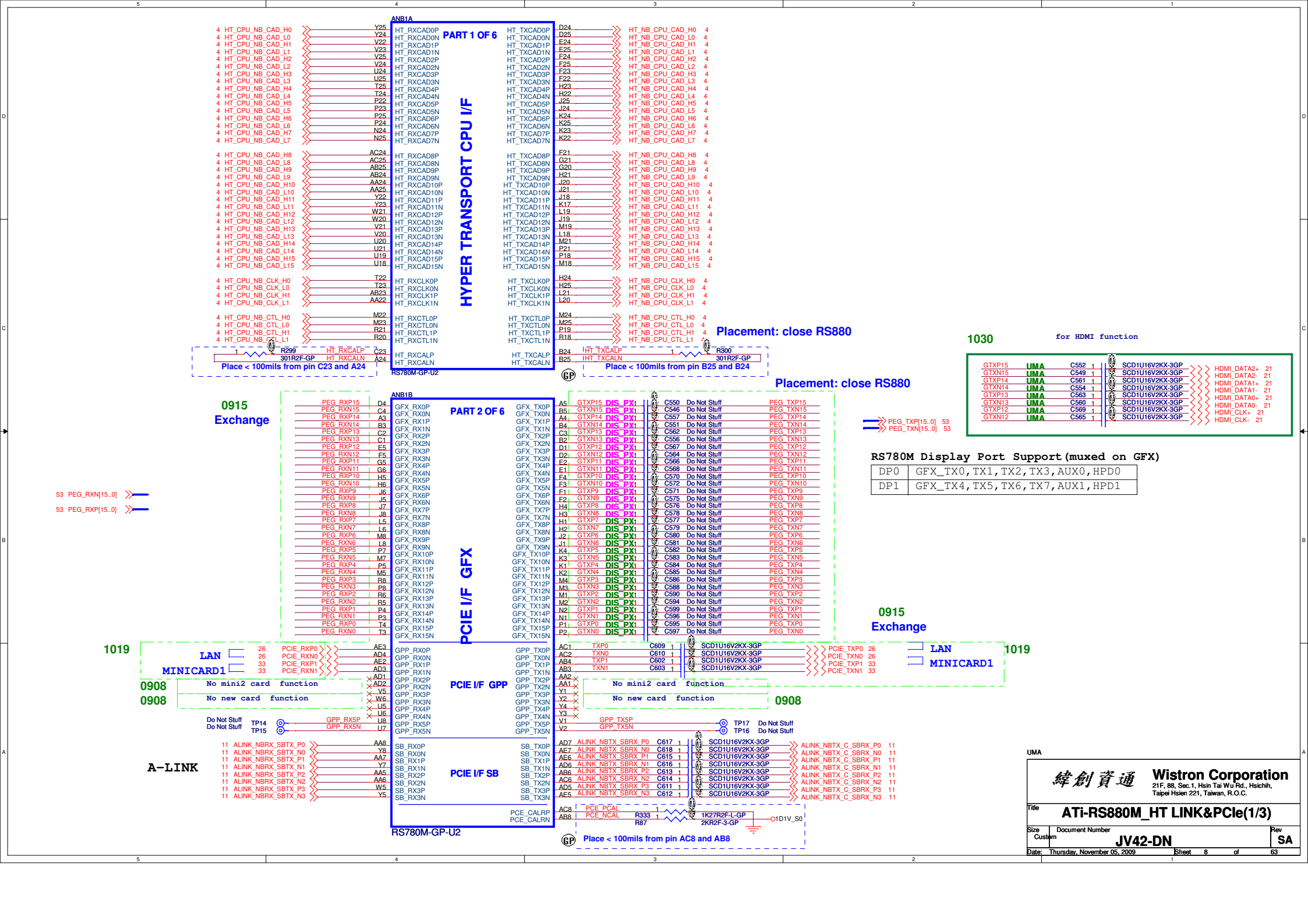
UMA

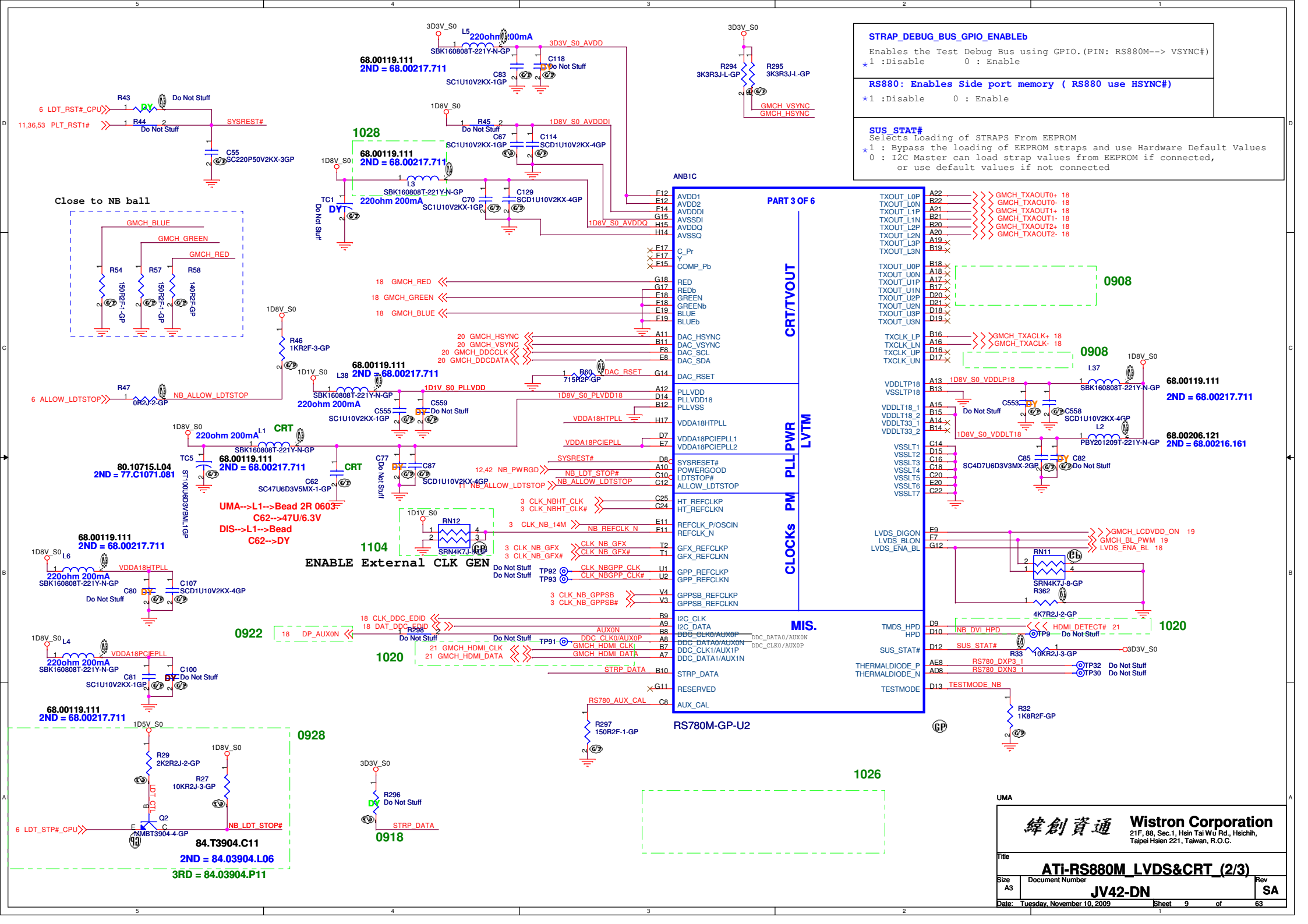
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU_Control&Debug_(3/4)	
Size: Custom	Document Number: JV42-DN	Rev: SA
Date: Thursday, November 05, 2009	Sheet 6 of 63	



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU_Power_(4/4)**	
Size A3	Document Number **JV42-DN**	Rev **SA**
Date: Thursday, November 05, 2009	Sheet 7 of 63	


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Placement: close RS880
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
0915 Exchange
1030
for HDMI function
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
1019
LAN
MINICARD1
0908
No mini2 card function
No new card function
A-LINK
Place < 100mils from pin AC8 and AB8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_HT LINK&PCIe(1/3)
Size Custom
Document Number
JV42-DN
Rev SA
Date: Thursday, November 05, 2009
Sheet 8 of 63


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS880M--> VSYNC#)
*1 :Disable 0 : Enable
RS880: Enables Side port memory (RS880 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
ANB1C
PART 3 OF 6
CRT/TVOUT
PWR
LVTM
PLL
PM
CLOCKs
MIS.
RS780M-GP-U2
Close to NB ball
ENABLE External CLK GEN
UMA-->L1-->Bead 2R 0603
C62-->47U/6.3V
DIS-->L1-->Bead
C62-->DY
0908
1028
1104
0922
1020
0928
0918
1026
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS880M_LVDS&CRT_(2/3)
JV42-DN
SA
Tuesday, November 10, 2009
Sheet 9 of 63

1027 For AMD review request

0.6A per ANT Rev1.1, Page3

0.45A per ANT Rev1.1, Page3

0910

80mil Width

300mil Width

1103

10A per ANT Rev1.1, Page3

Per check list (Rev 0.02)

RS780M: 1V ~ 1.1V, check PWR team

+NB_VCORE

1027 For AMD review request

MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

ANB1E

PART 5/6

POWER

RS780M-GP-U2

ANB1F

PART 6/6

GROUND

RS780M-GP-U2

ANB1D

PAR 4 OF 6

SBD_MEM/DVO_I/F

RS780M-GP-U2

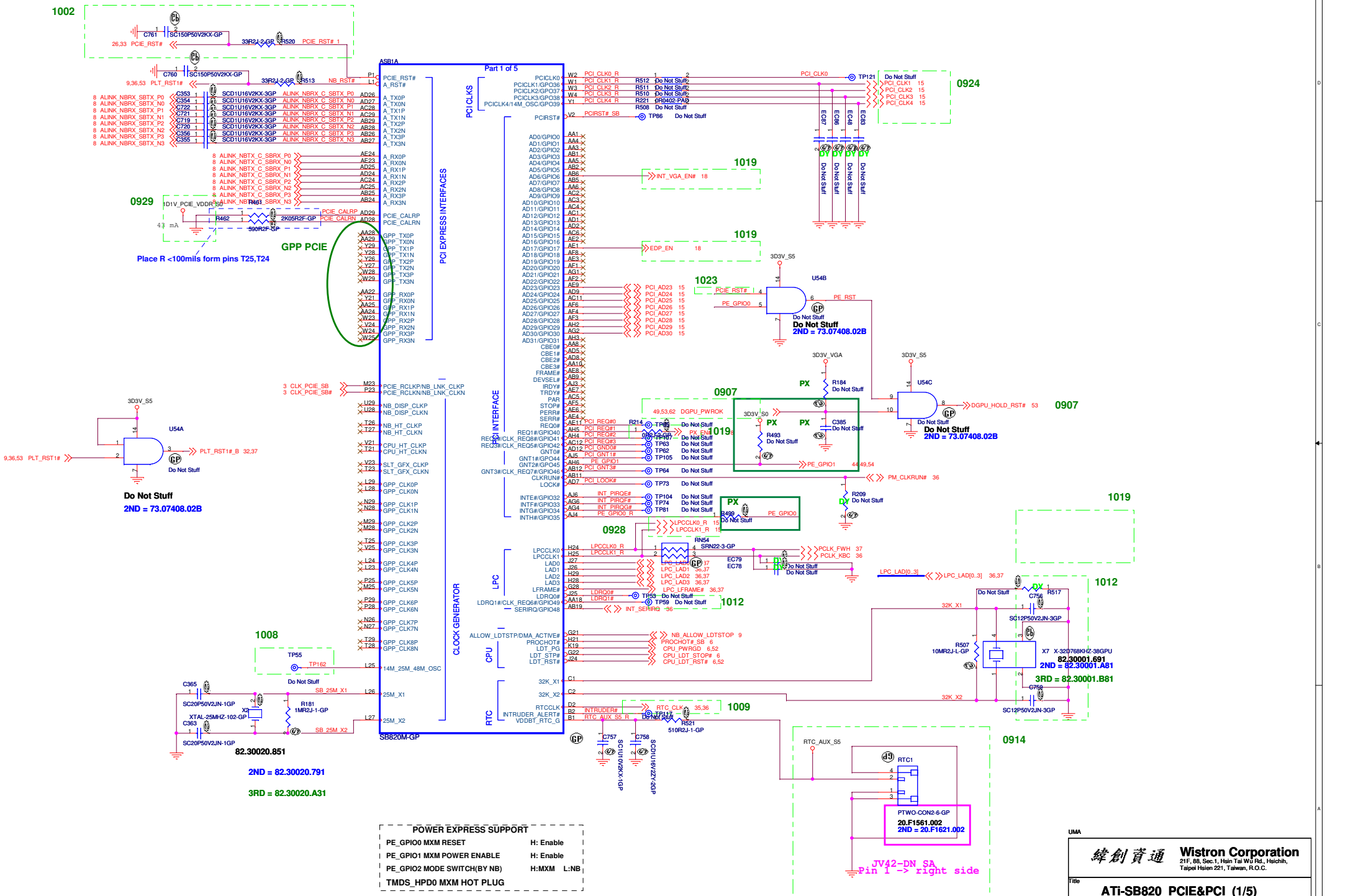
UMA

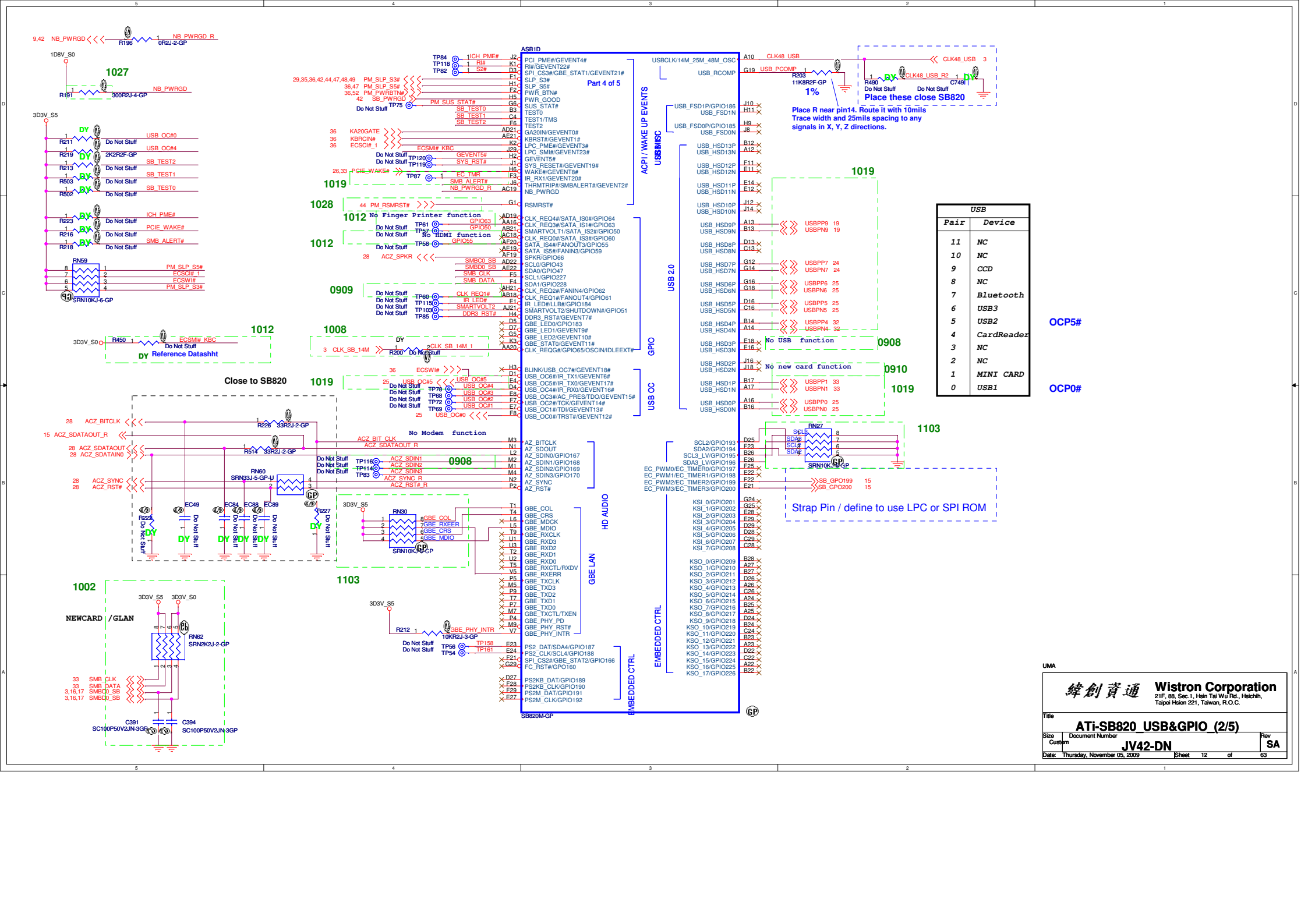
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

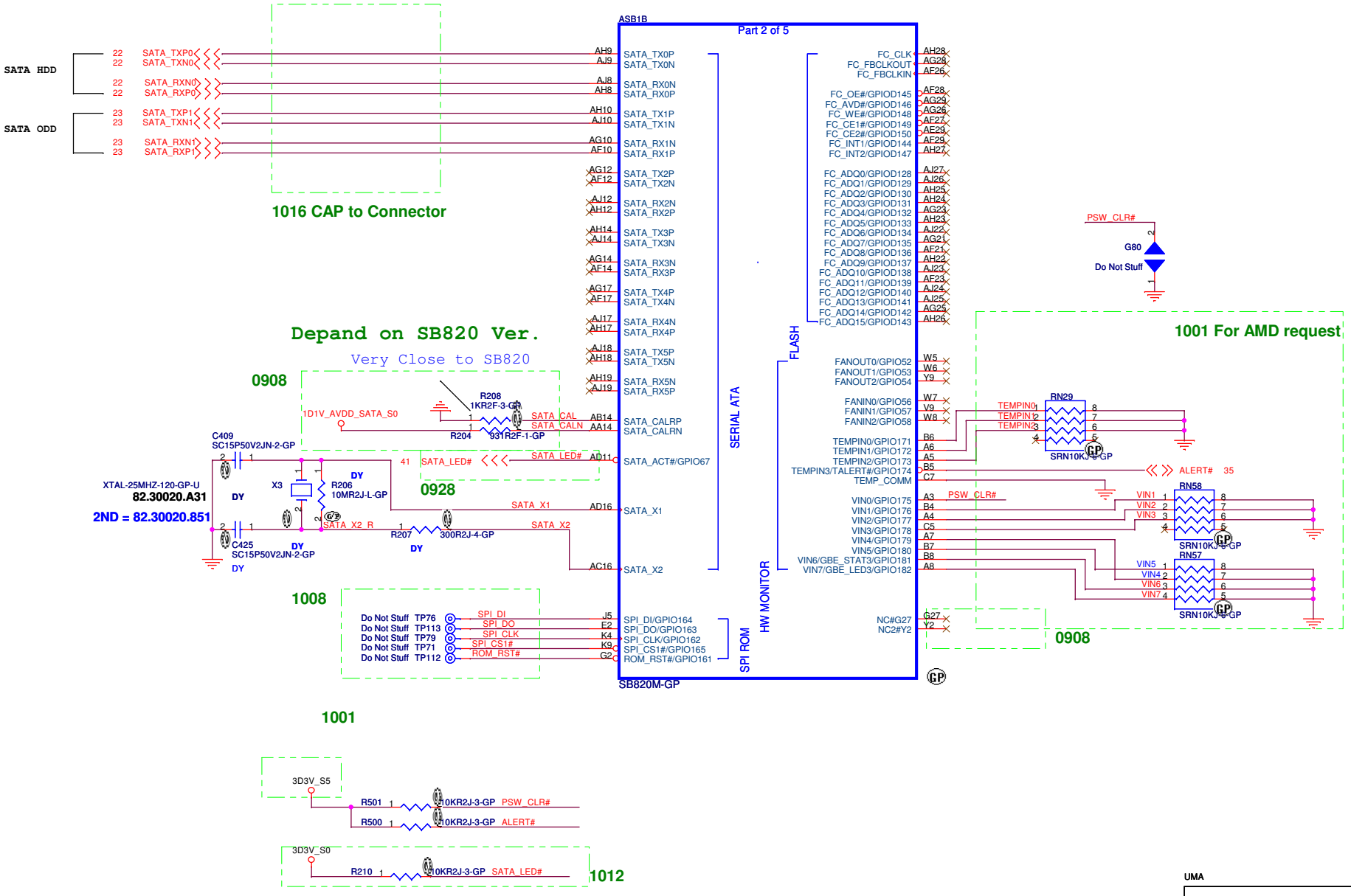
Title: ATi-RS880M_Side Port&PWR&GND(3/3)

Size: A3 | Document Number: JV42-DN | Rev: SA

Date: Thursday, November 05, 2009 | Sheet 10 of 63

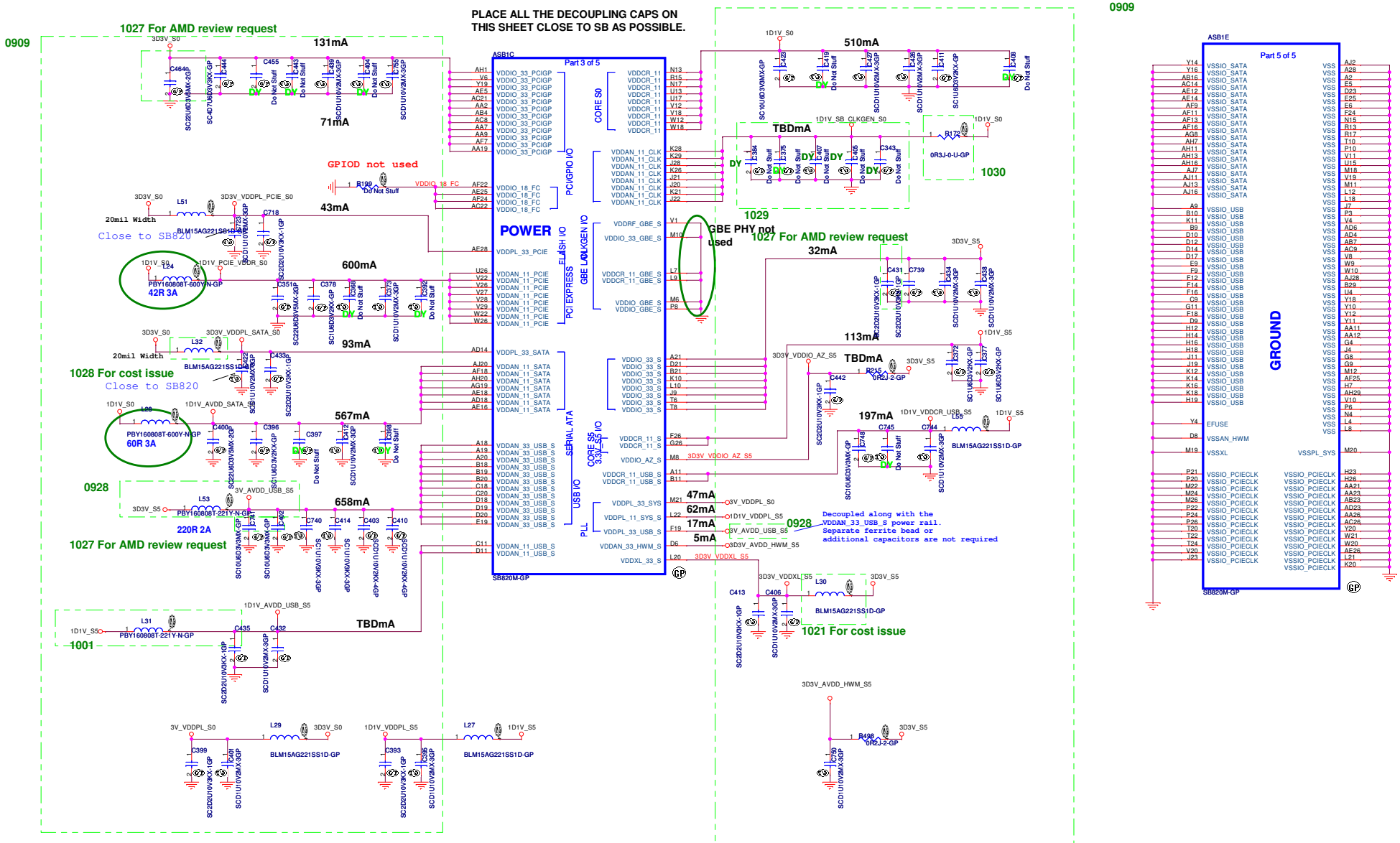

1002
C761
SC150P50V2KX-GP
26,33 PCIE_RST#
33R2J-2-GP
R520
PCIE_RST# 1
C760
SC150P50V2KX-GP
9,36,53 PLT_RST1#
33R2J-2-GP
R513
NB_RST#
ASB1A
Part 1 of 5
PCIE_RST#
A_RST#
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
SB820M-GP
0929
D1V_PCIE_VDDR_SW
R462
590R2F-GP
R461
2K05R2F-GP
PCIE_CALRP
PCIE_CALRN
GPP PCIE
Place R <100mils form pins T25,T24
0924
PCI_CLK0
TP121
PCI_CLK1 15
PCI_CLK2 15
PCI_CLK3 15
PCI_CLK4 15
Do Not Stuff
EC87
EC86
EC48
EC83
DY
Do Not Stuff
1019
INT_VGA_EN# 18
EDP_EN 18
1023
U54B
PCIE_RST#
PE_GPIO0
PE_RST
Do Not Stuff
2ND = 73.07408.02B
3D3V_S5
3D3V_VGA
0907
PX
R184
R493
C385
U54C
DGPU_HOLD_RST# 53
2ND = 73.07408.02B
49,53,62 DGPU_PWROK
PX_EN#
PE_GPIO1
PM_CLKRUN# 36
R209
0928
PE_GPIO0_R
R499
RN54
SRN22-3-GP
PCLK_FWH 37
PCLK_KBC 36
EC79
EC78
LPC_LAD[0..3] 36,37
1012
1019
1008
TP55
TP162
14M_25M_48M_OSC
SB_25M_X1
SB_25M_X2
25M_X1
25M_X2
C365
SC20P50V2JN-1GP
XTAL-25MHZ-102-GP
X3
R181
1MR2J-1-GP
C363
SC20P50V2JN-1GP
82.30020.851
2ND = 82.30020.791
3RD = 82.30020.A31
32K_X1
32K_X2
R507
10MR2J-L-GP
X7 X-32D768KHZ-38GPU
82.30001.691
2ND = 82.30001.A81
3RD = 82.30001.B81
R517
C756
C758
SC12P50V2JN-3GP
1009
RTC_CLK 35,36
INTRUDER_ALERT#
R521
510R2J-1-GP
C757
C758
SCD1U16V2ZY-2GP
SC1U10V2KX-1GP
0914
RTC_AUX_S5
RTC1
PTWO-CON2-6-GP
20.F1561.002
2ND = 20.F1621.002
JV42-DN SA
Pin 1 -> right side
U54A
PLT_RST1#_B 32,37
Do Not Stuff
2ND = 73.07408.02B
POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH(BY NB) H:MXM L:NB
TMDS_HPD0 MXM HOT PLUG
UMA
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB820 PCIE&PCI (1/5)
Size
Document Number
JV42-DN
Rev
SA
Date: Thursday, November 26, 2009
Sheet 11 of 63


ASB1D
Part 4 of 5
SB820M-GP
ACPI / WAKE UP EVENTS
USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
No Finger Printer function
No HDMI function
No Modem function
No USB function
No new card function
Close to SB820
Reference Datashht
Place these close SB820
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
Strap Pin / define to use LPC or SPI ROM
NEWCARD /GLAN
USB
Pair Device
11 NC
10 NC
9 CCD
8 NC
7 Bluetooth
6 USB3
5 USB2
4 CardReader
3 NC
2 NC
1 MINI CARD
0 USB1
OCP5#
OCP0#
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB820_USB&GPIO_(2/5)
Size Custom
Document Number
JV42-DN
Rev
SA
Date: Thursday, November 05, 2009
Sheet 12 of 63



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ATi-SB820_SATA-IDE (3/5)		
Size: A3	Document Number: JV42-DN	Rev: SA
Date: Thursday, November 19, 2009	Sheet 13 of 63	

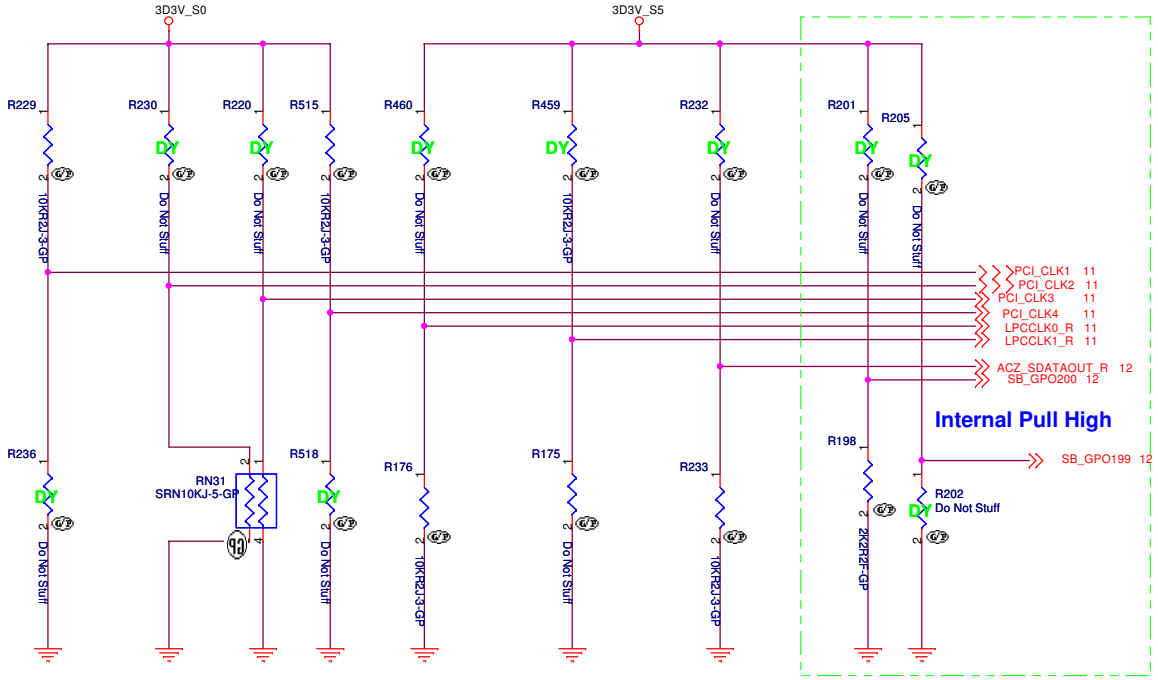


UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ATI-SB820_POWER&GND_(4/5)		
Size: Custom	Document Number: JV42-DN	Rev: SA
Date: Tuesday, November 10, 2009	Sheet 14 of 63	

REQUIRED STRAPS

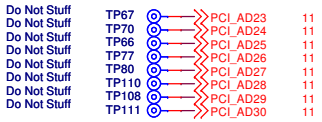
REQUIRED SYSTEM STRAPS



1002

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

UMA

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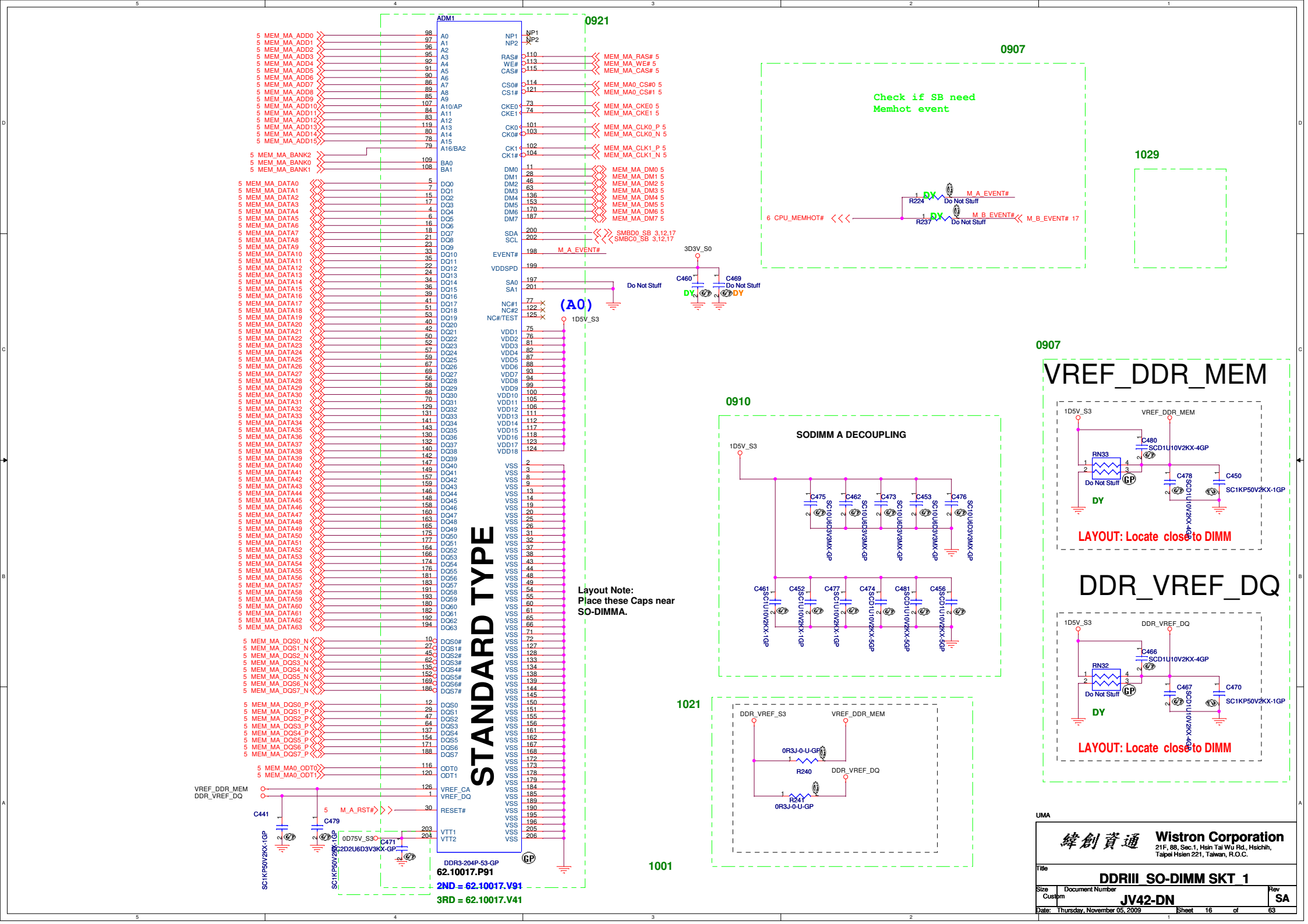
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB820_STRAPPING_(5/5)

Size: A3 | Document Number: JV42-DN | Rev: SA

Date: Wednesday, November 18, 2009 | Sheet 15 of 63


ADM1
STANDARD TYPE
DDR3-204P-53-GP
62.10017.P91
2ND = 62.10017.V91
3RD = 62.10017.V41
0921
0907
Check if SB need
Memhot event
1029
0907
VREF_DDR_MEM
LAYOUT: Locate close to DIMM
DDR_VREF_DQ
LAYOUT: Locate close to DIMM
0910
SODIMM A DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA.
1021
1001
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRIII_SO-DIMM SKT_1
JV42-DN
Rev SA
Thursday, November 05, 2009
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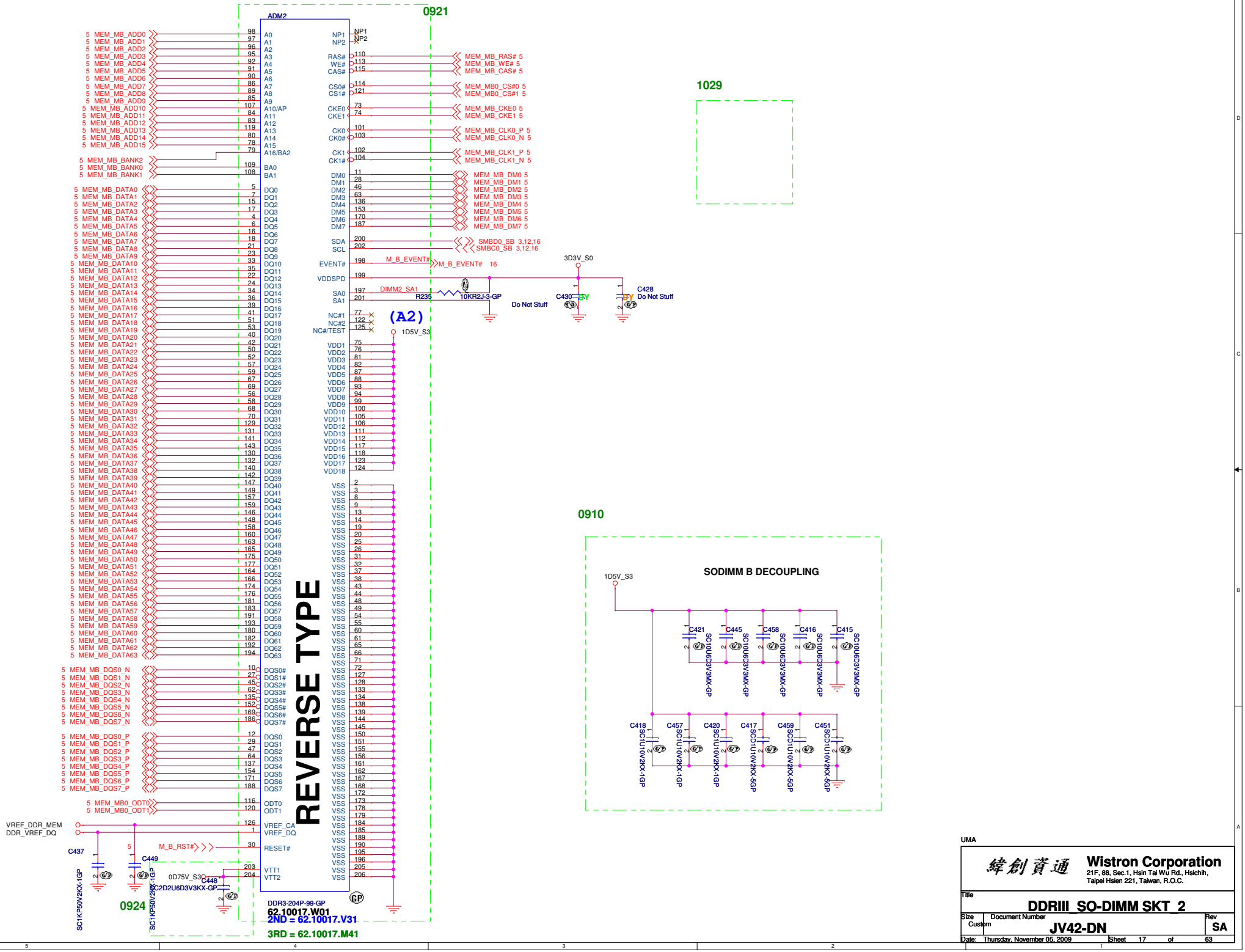

UMA

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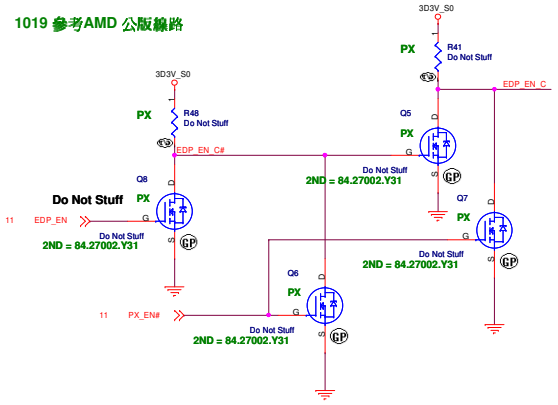
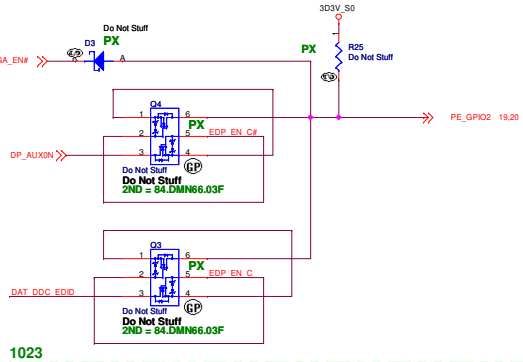
Title	DDRIII_SO-DIMM SKT_2	
Size: Custom	Document Number: JV42-DN	Rev: SA
Date: Thursday, November 05, 2009	Sheet 17 of 63	

1019 參考AMD 公版線路





Truth Table

LVDS

Function	SEL
A_N to $_NB_1$	L
A_N to $_NB_2$	H

CRT

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

EDID

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level

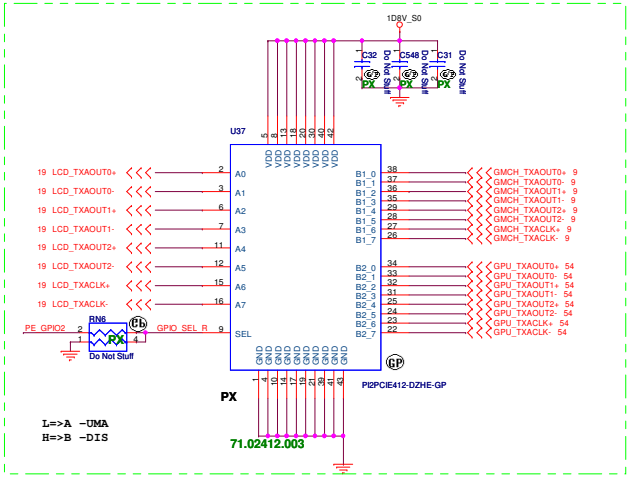
BLON_IN

Function Table

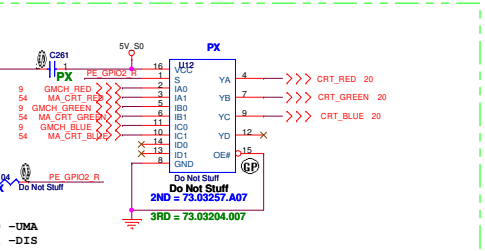
Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level

1023



0924



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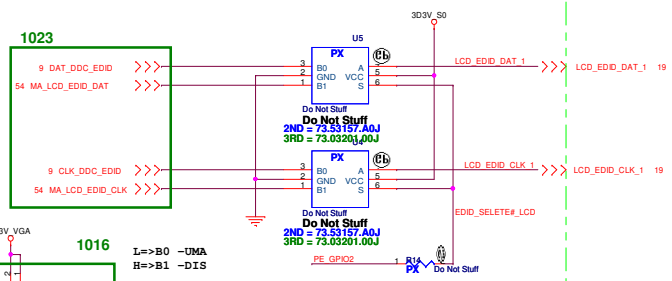
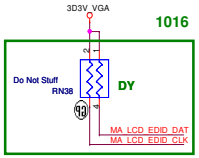
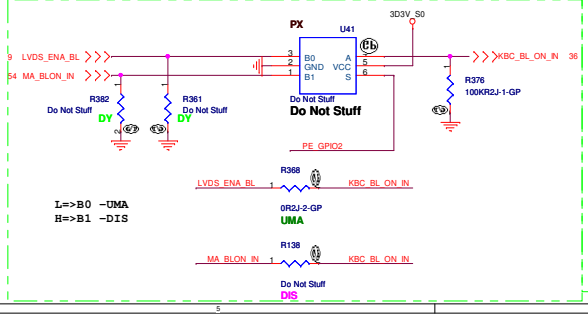


1016

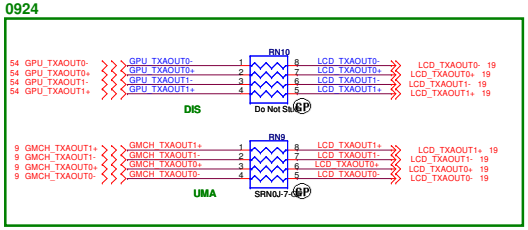


L=>B0 -UMA
H=>B1 -DIS

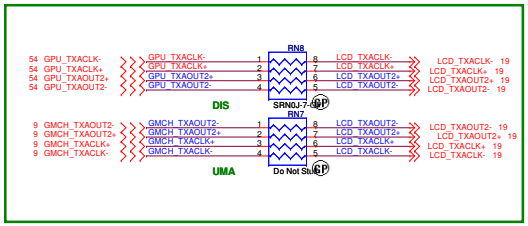
1026



0924

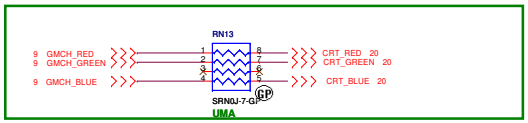


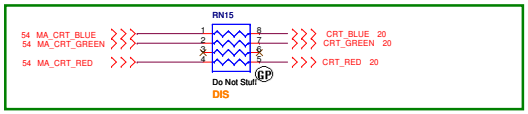
None PX



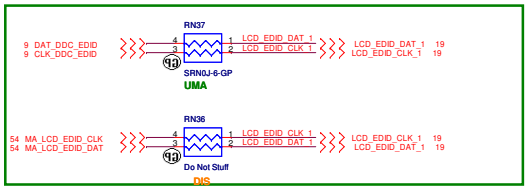
None PX

0924





None PX



None PX

UMA

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PX

Size: A2 Document Number: JV42-DN Rev: SA

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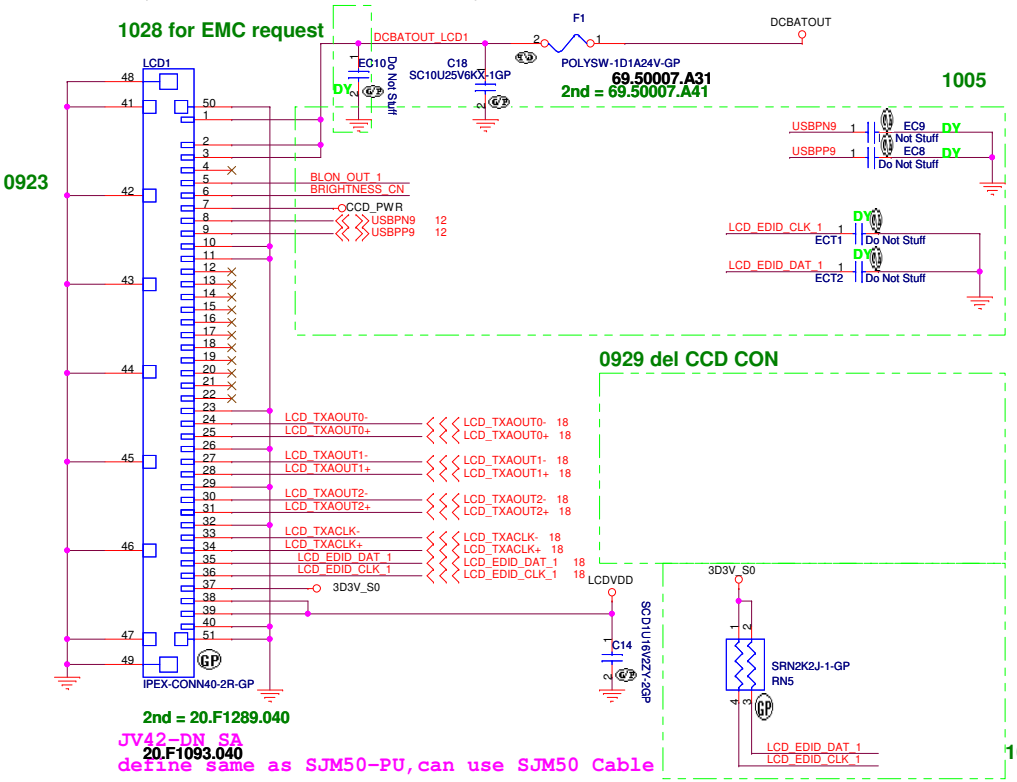
LCD/INVERTER/CCD CONN

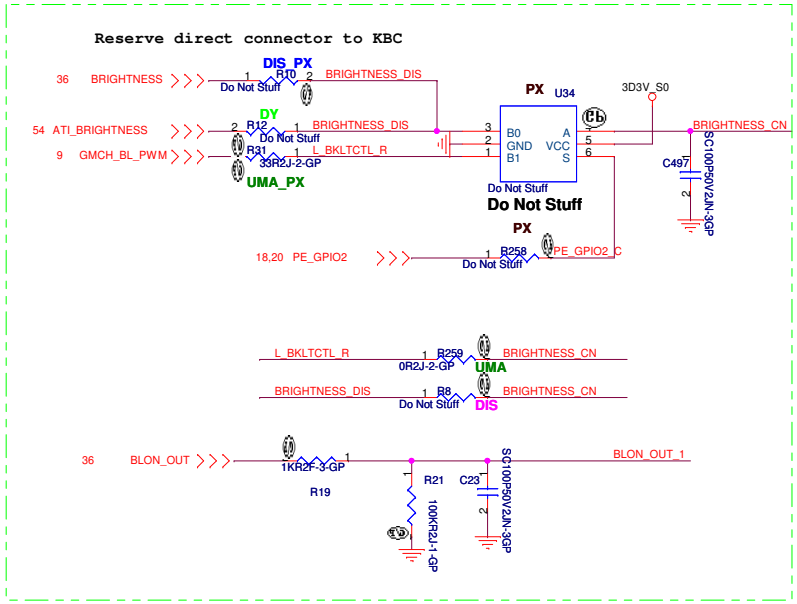
Change PX

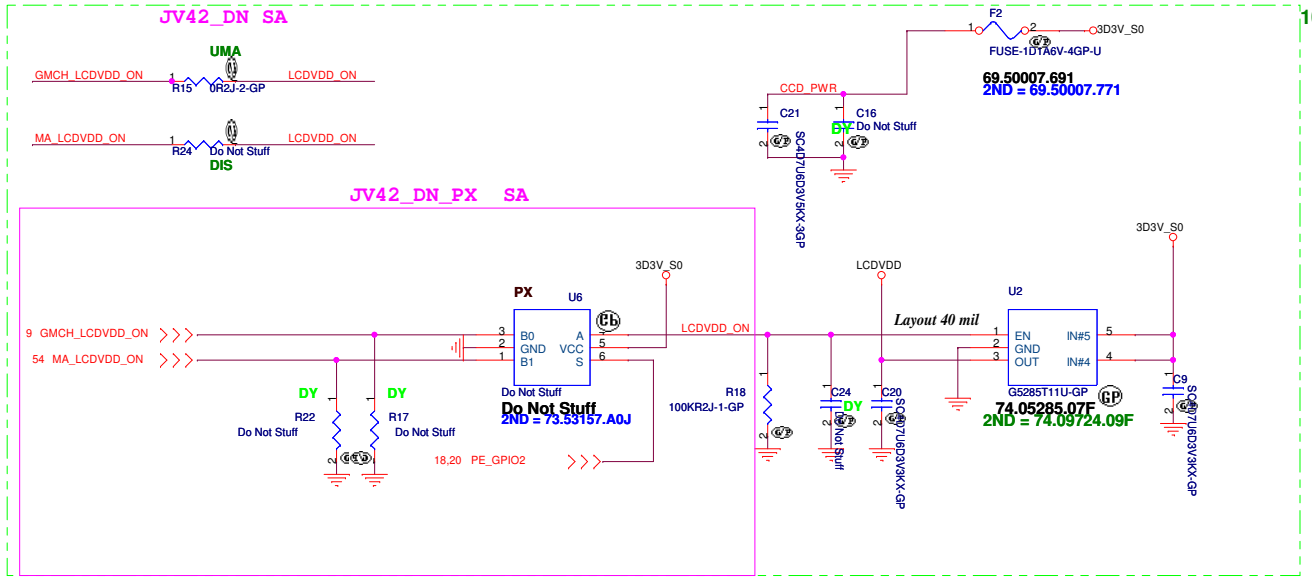
0922

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND







UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

Size: Custom | Document Number: JV42-DN | Rev: SA

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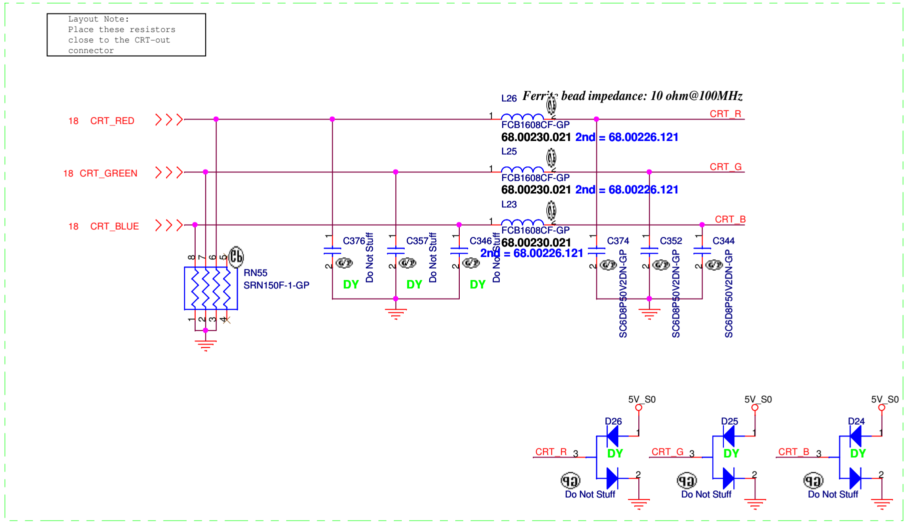
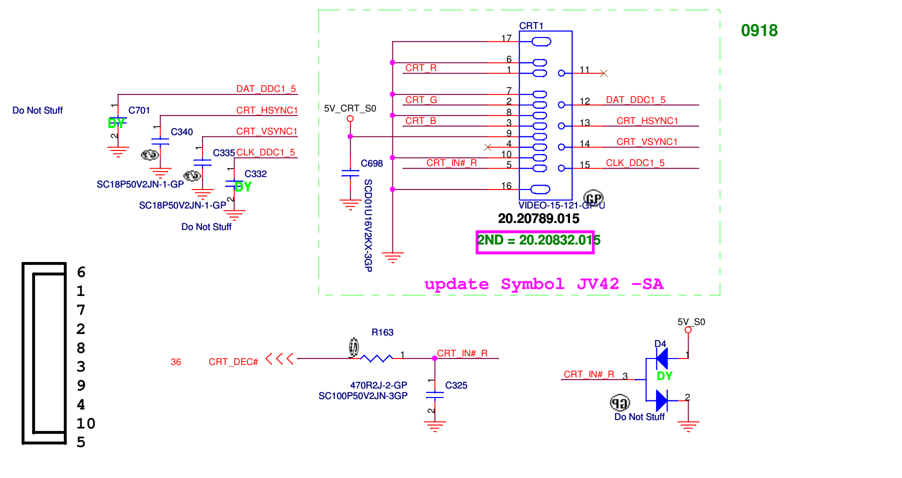
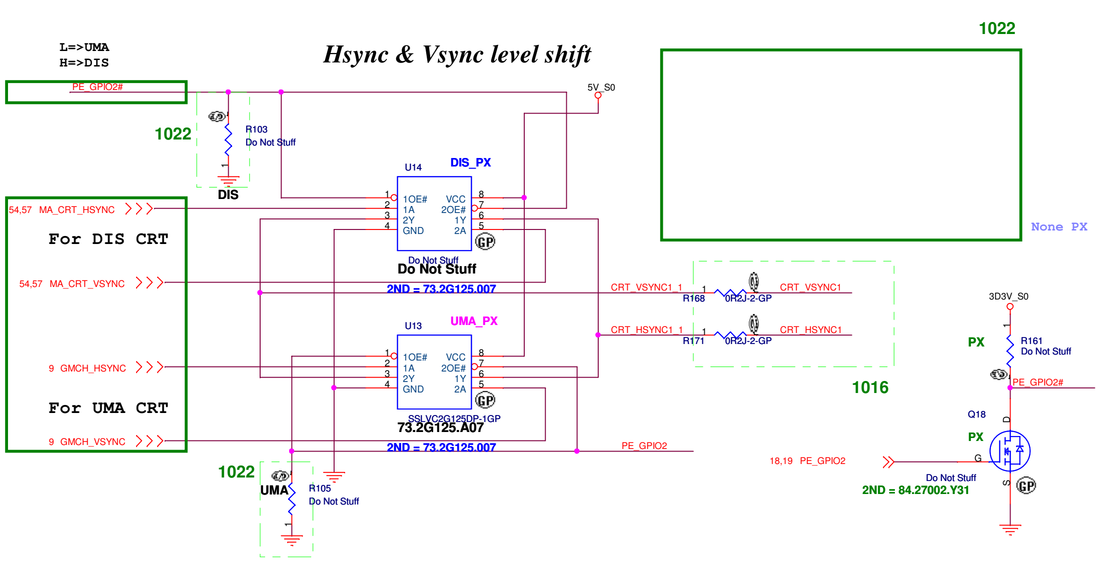
Layout Note:
Place these resistors close to the CRT-out connector


Ferrite bead impedance: 10 ohm@100MHz
18 CRT_RED
18 CRT_GREEN
18 CRT_BLUE
L26 FCB1608CF-GP 68.00230.021 2nd = 68.00226.121
L25 FCB1608CF-GP 68.00230.021 2nd = 68.00226.121
L23 FCB1608CF-GP 68.00230.021 2nd = 68.00226.121
CRT_R
CRT_G
CRT_B
RN55 SRN150F-1-GP
C376 Do Not Stuff
C357 Do Not Stuff
C346 Do Not Stuff
C374 SC6D8P50V2DN-GP
C352 SC6D8P50V2DN-GP
C344 SC6D8P50V2DN-GP
DY
D26 D25 D24
5V_S0
Do Not Stuff
0924

Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR


0918
CRT1
VIDEO-15-121-GP-U
20.20789.015
2ND = 20.20832.015
update Symbol JV42 -SA
5V_CRT_S0
C698 SCD01U16V2KX-3GP
CRT_R CRT_G CRT_B CRT_IN#_R
DAT_DDC1_5 CRT_HSYNC1 CRT_VSYNC1 CLK_DDC1_5
C701 C340 C335 C332
SC18P50V2JN-1-GP
Do Not Stuff
36 CRT_DEC#
R163 470R2J-2-GP
C325 SC100P50V2JN-3GP
D4 DY 5V_S0
Do Not Stuff
6 1 7 2 8 3 9 4 10 5


1012
L=>UMA
H=>DIS
Hsync & Vsync level shift
PE_GPIO2#
R103 Do Not Stuff
DIS
1022
54,57 MA_CRT_HSYNC
For DIS CRT
54,57 MA_CRT_VSYNC
9 GMCH_HSYNC
For UMA CRT
9 GMCH_VSYNC
U14 DIS_PX
Do Not Stuff
2ND = 73.2G125.007
U13 UMA_PX
SSLVC2G125DP-1GP
73.2G125.A07
2ND = 73.2G125.007
CRT_VSYNC1_1 R168 0R2J-2-GP CRT_VSYNC1
CRT_HSYNC1_1 R171 0R2J-2-GP CRT_HSYNC1
1016
PE_GPIO2
R105 Do Not Stuff
UMA
1022
None PX
3D3V_S0
PX R161 Do Not Stuff
PE_GPIO2#
Q18 PX
18,19 PE_GPIO2
Do Not Stuff
2ND = 84.27002.Y31
5V_S0

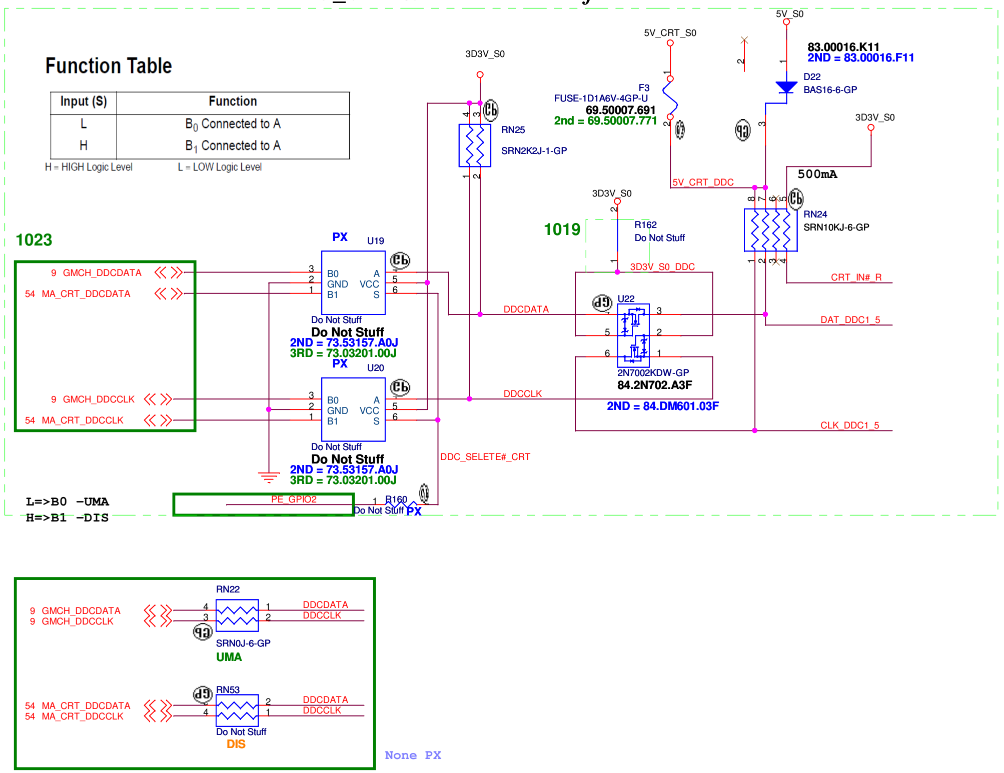
0924

DDC_CLK & DATA level shift

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level   L = LOW Logic Level

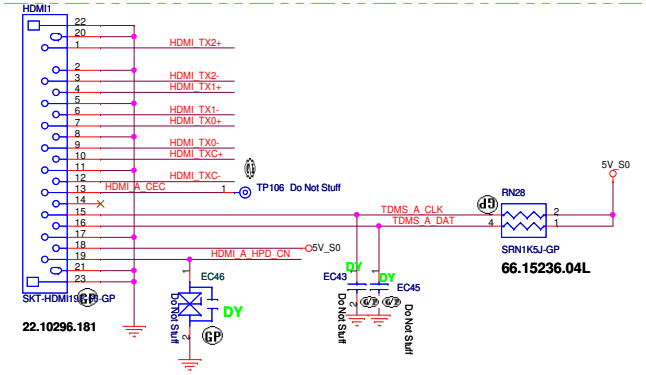

3D3V_S0
5V_CRT_S0
5V_S0
F3 FUSE-1D1A6V-4GP-U 69.50007.691 2nd = 69.50007.771
83.00016.K11 2ND = 83.00016.F11
D22 BAS16-6-GP
RN25 SRN2K2J-1-GP
500mA
RN24 SRN10KJ-6-GP
5V_CRT_DDC
R162 Do Not Stuff
1019
3D3V_S0_DDC
1023
9 GMCH_DDCDATA
54 MA_CRT_DDCDATA
9 GMCH_DDCCLK
54 MA_CRT_DDCCLK
PX U19
Do Not Stuff
2ND = 73.53157.A0J
3RD = 73.03201.00J
PX U20
Do Not Stuff
2ND = 73.53157.A0J
3RD = 73.03201.00J
DDCDATA
DDCCLK
U22 2N7002KDW-GP 84.2N702.A3F
2ND = 84.DM601.03F
CRT_IN#_R
DAT_DDC1_5
CLK_DDC1_5
DDC_SELETE#_CRT
L=>B0 -UMA
H=>B1 -DIS
PE_GPIO2
R160 Do Not Stuff PX
RN22 SRN0J-6-GP UMA
RN53 Do Not Stuff DIS
None PX

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CRT Connector**
Size / Document Number	**JV42-DN**
Rev	**SA**
Date:	Tuesday, November 10, 2009
Sheet	20 of 63

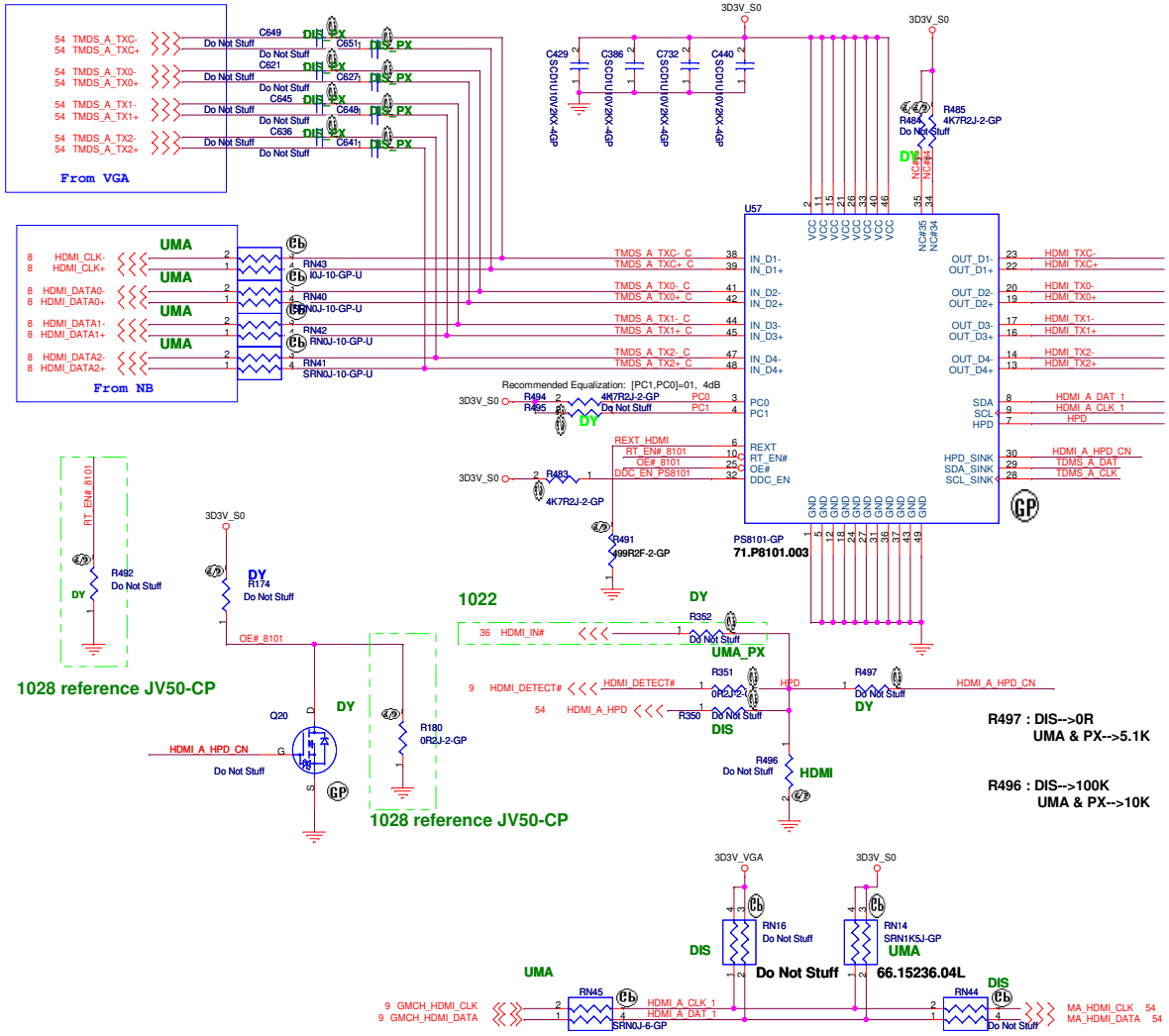
1026 for Layout request

1012



1026 for Layout request

1026 for Layout request



1026 for Layout request

UMA

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Title: HDMI Connector

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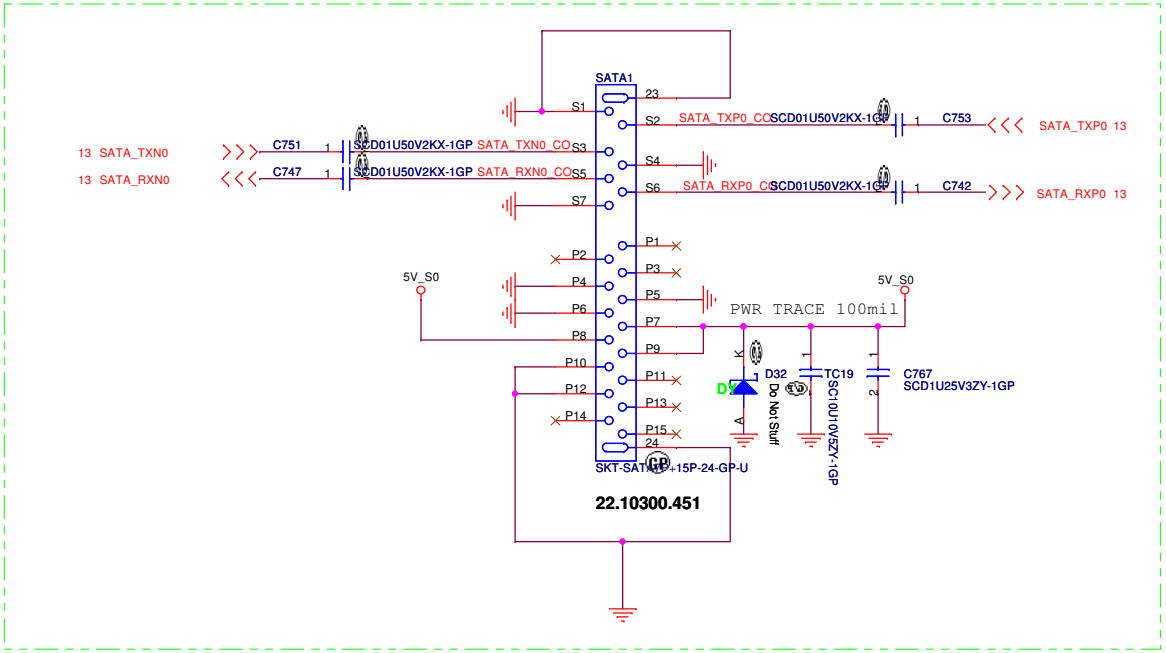
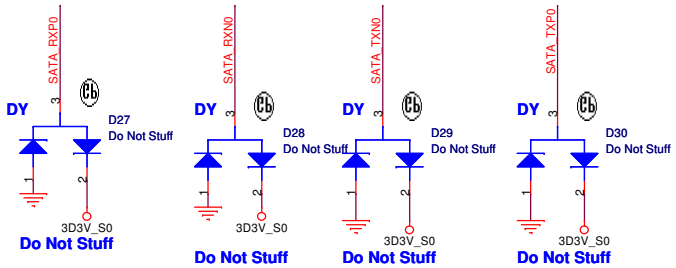
SATA Connector

0923





UMA

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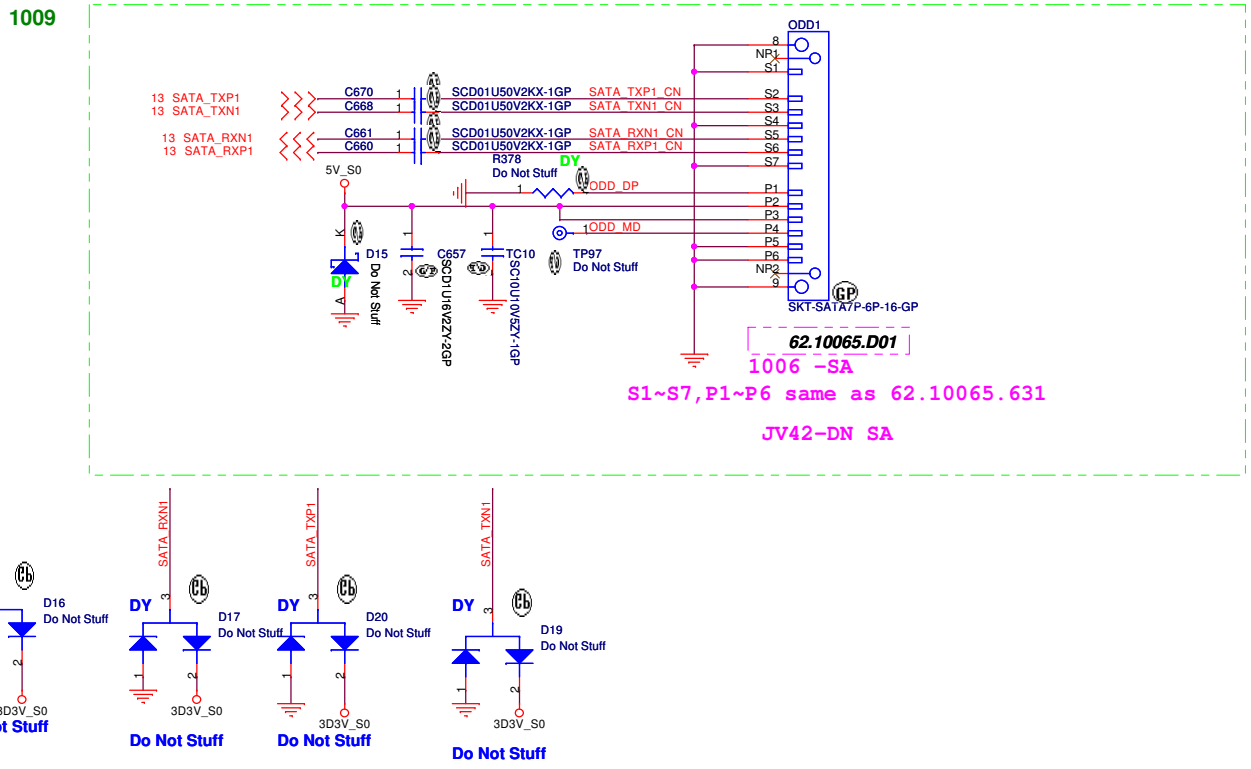
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD		
Size	Document Number	Rev
	JV42-DN	SA
Date: Thursday, November 05, 2009	Sheet 22 of 63	

ODD Connector



UMA

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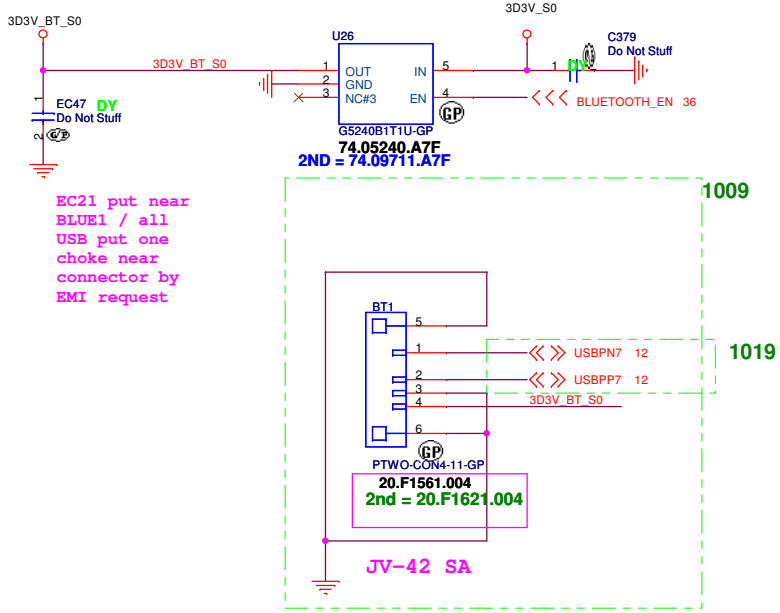
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ODD		
Size	Document Number	Rev
	JV42-DN	SA
Date: Thursday, November 05, 2009	Sheet 23 of 63	

BLUETOOTH MODULE

1.5A / High Active Voltage 2V



Pin 1 ->right side
20.D0197.104 Pin1 -> left side
change net sequence
can us JV50-CP Cable

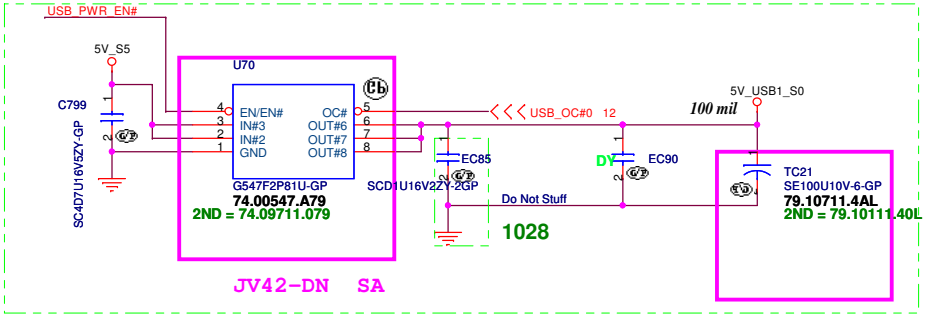
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

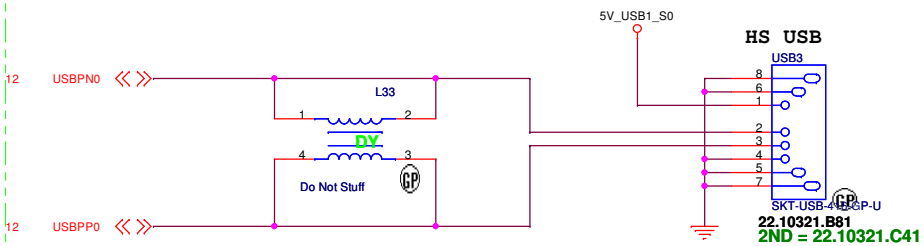
Title	BLUETOOTH	
Size	Document Number JV42-DN	Rev SA
Date: Thursday, November 05, 2009	Sheet 24 of 63	

0910

0914

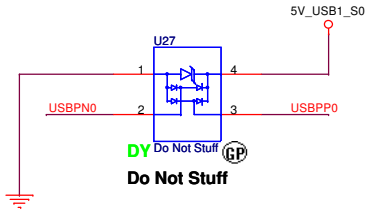


1028 for EMC request



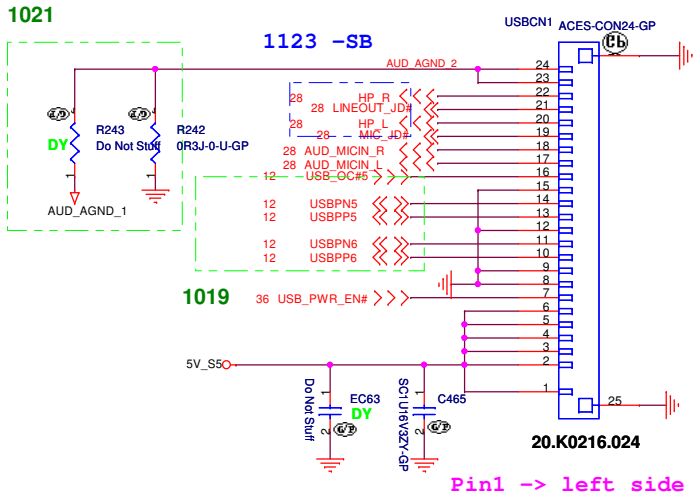
Pin1 -> right side
22.10218.T51 Pin1 -> left side (JV42-DN)

change Net sequence



0910

1021



Pin1 -> left side

UMA

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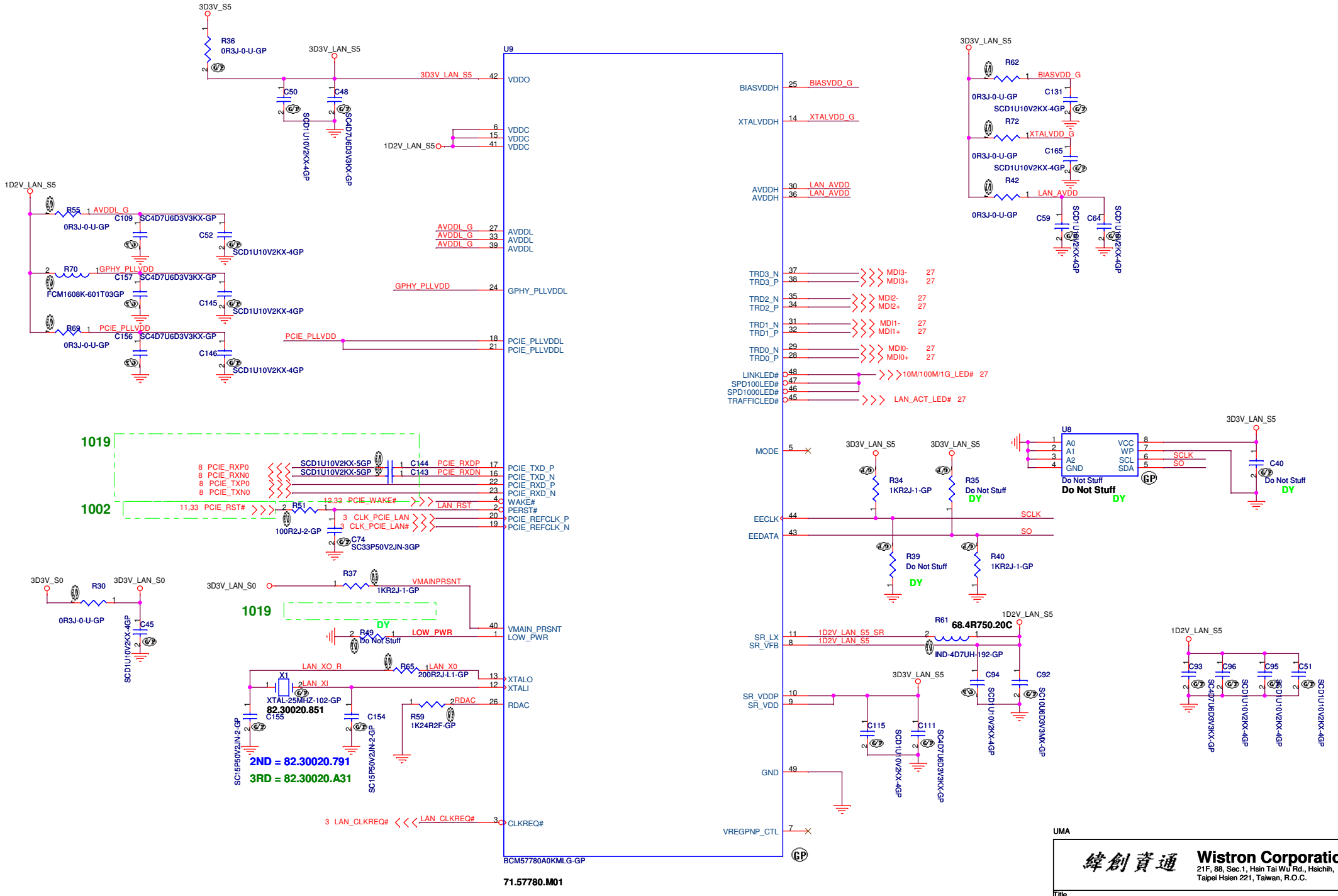
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB	
Size	Document Number: JV42-DN	Rev: SA
Date: Monday, November 23, 2009	Sheet 25 of 63	



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **BCM57780**

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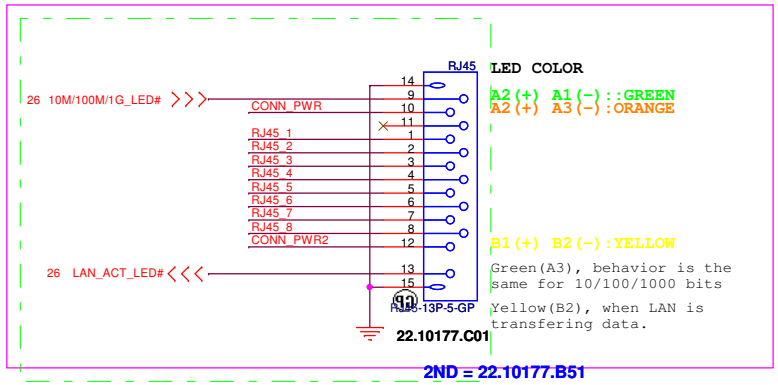
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

LAN Connector

0923

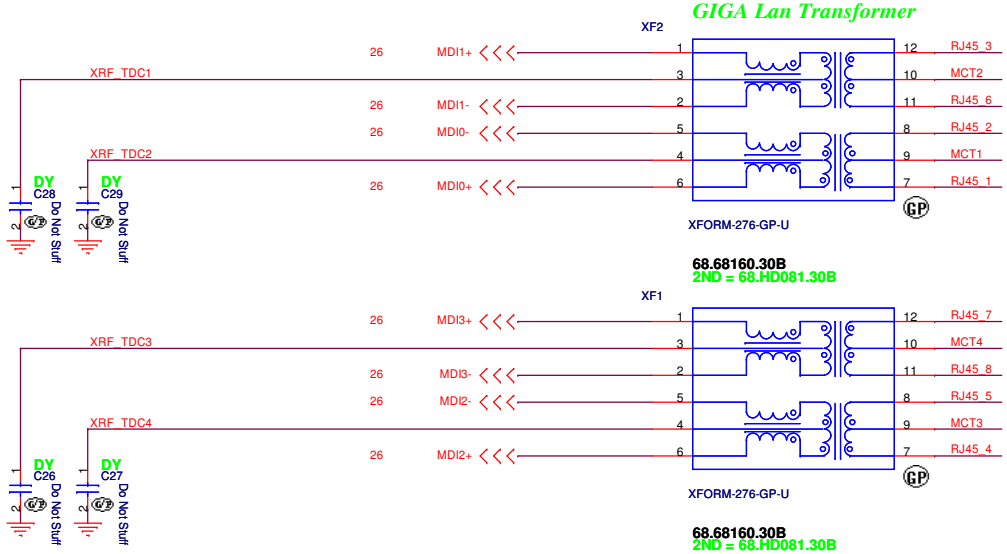


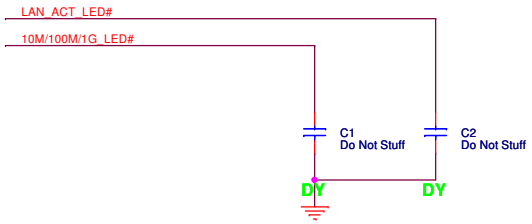
2ND = 22.10177.B51

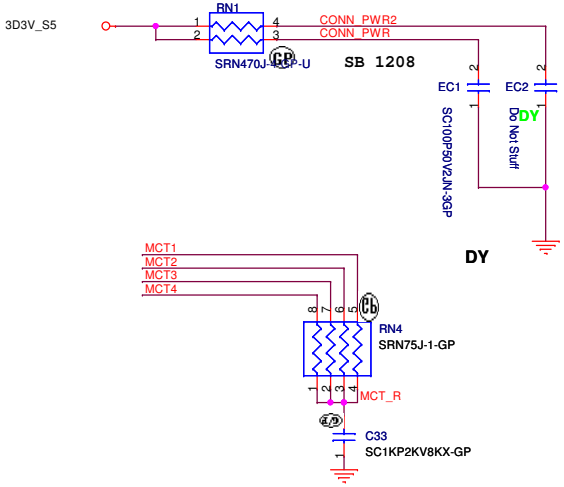
3RD = 22.10177.C21(lab 未上)

4TH = 22.10177.B81

GIGA Lan Transformer







UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

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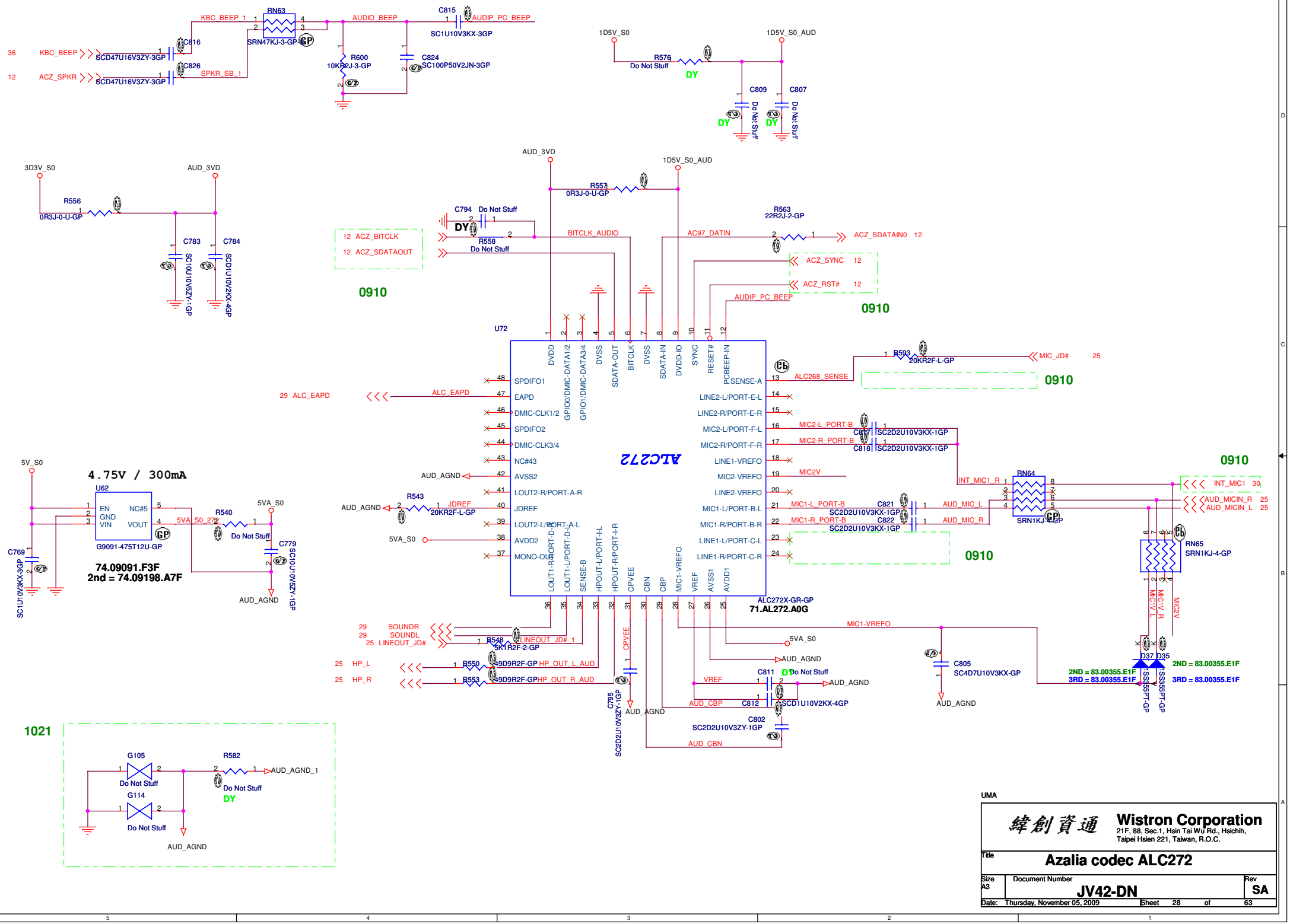

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC272**

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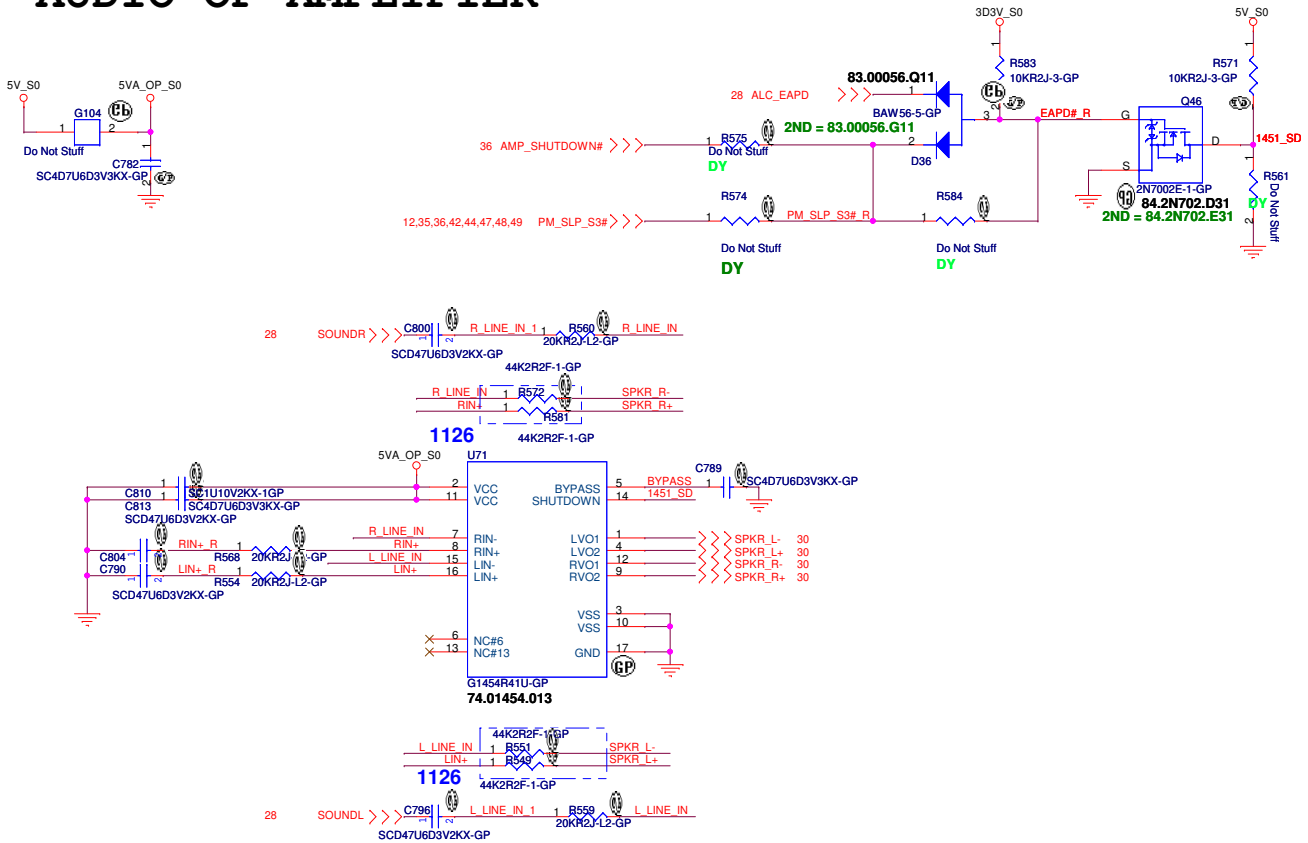
AUDIO OP AMPLIFIER




```
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If  VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W
```

UMA

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Title	AUDIO AMP
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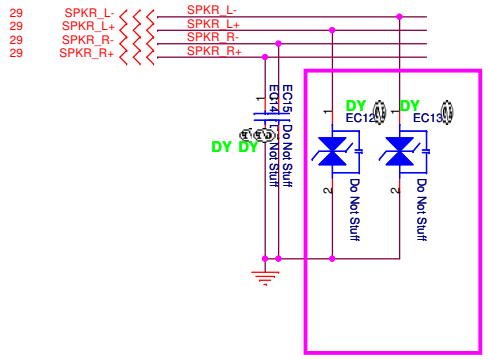
Date: Thursday, November 26, 2009	Sheet 29 of 63

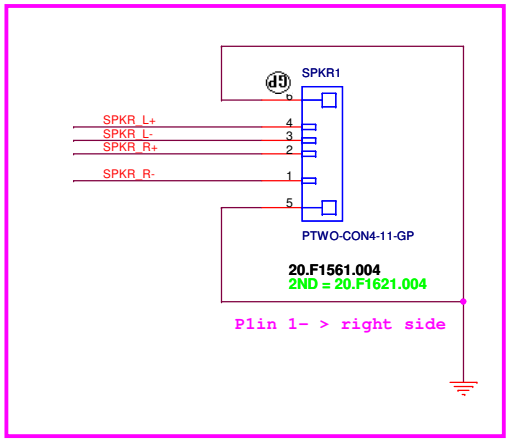
Internal Speaker

0910



JV42-DN SA

0914



JV42-DN SA

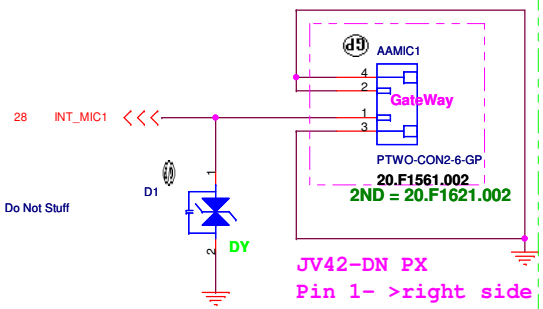
0910

LINE OUT

0911

1016

Internal Mic



JV42-DN PX
Pin 1- >right side
20.F1240.002 Pin1->left side

same as JV70-CP

UMA

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Title		
AUDIO JACK		
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No Modem Function

UMA

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Title: **MDC**

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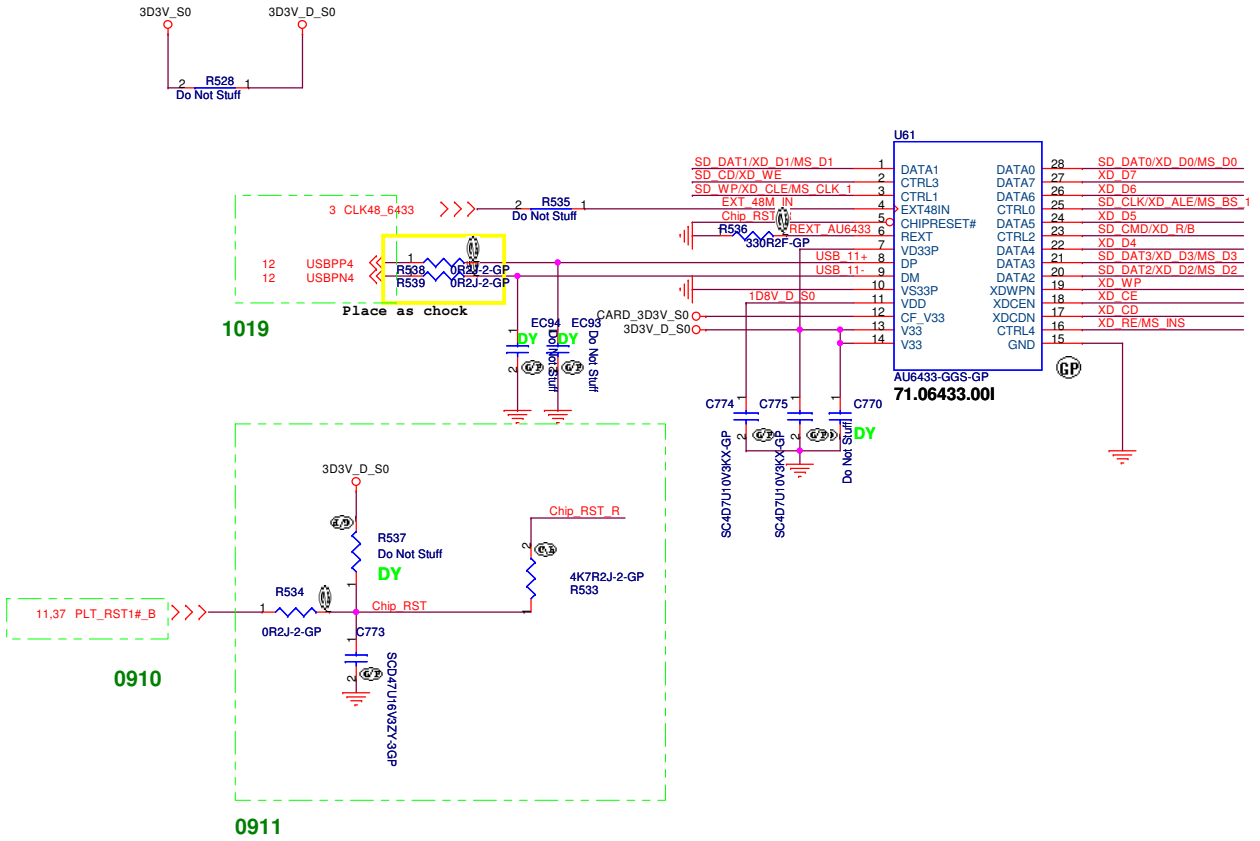
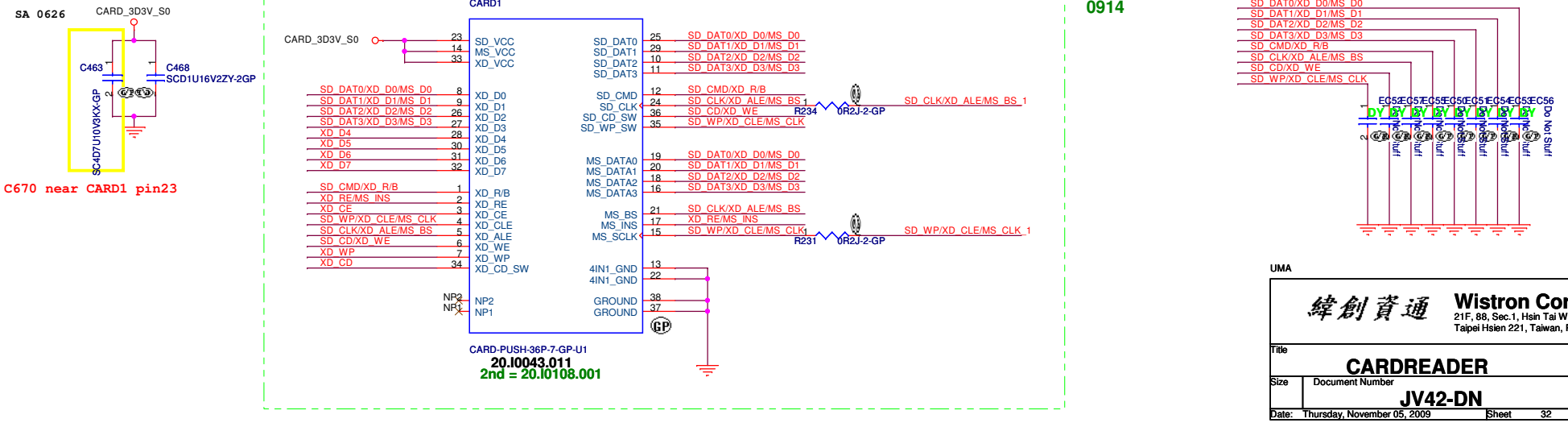


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



UMA

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Title: **CARDREADER**

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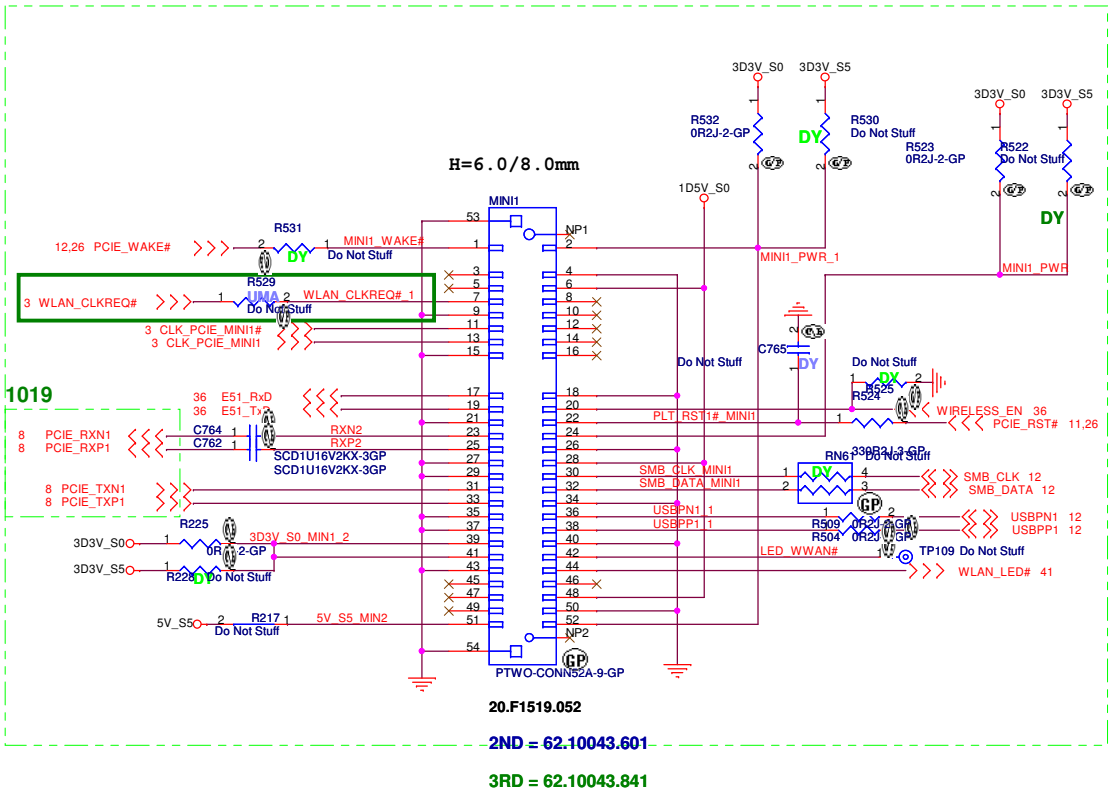
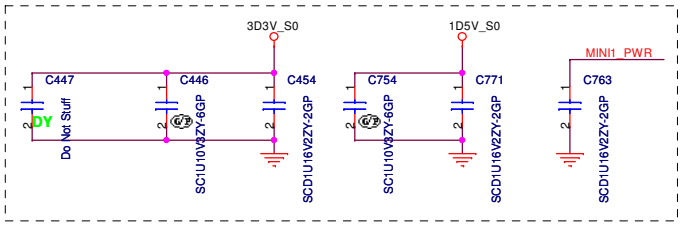
Mini Card Connector(WLAN)

0923



Place near MINI1



No Mini Card Function (Robson2 and 3G)

UMA

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Title: MINI CARD		
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No NEWCARD Function

UMA

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Title	NEW CARD	
Size	Document Number: JV42-DN	Rev: SA
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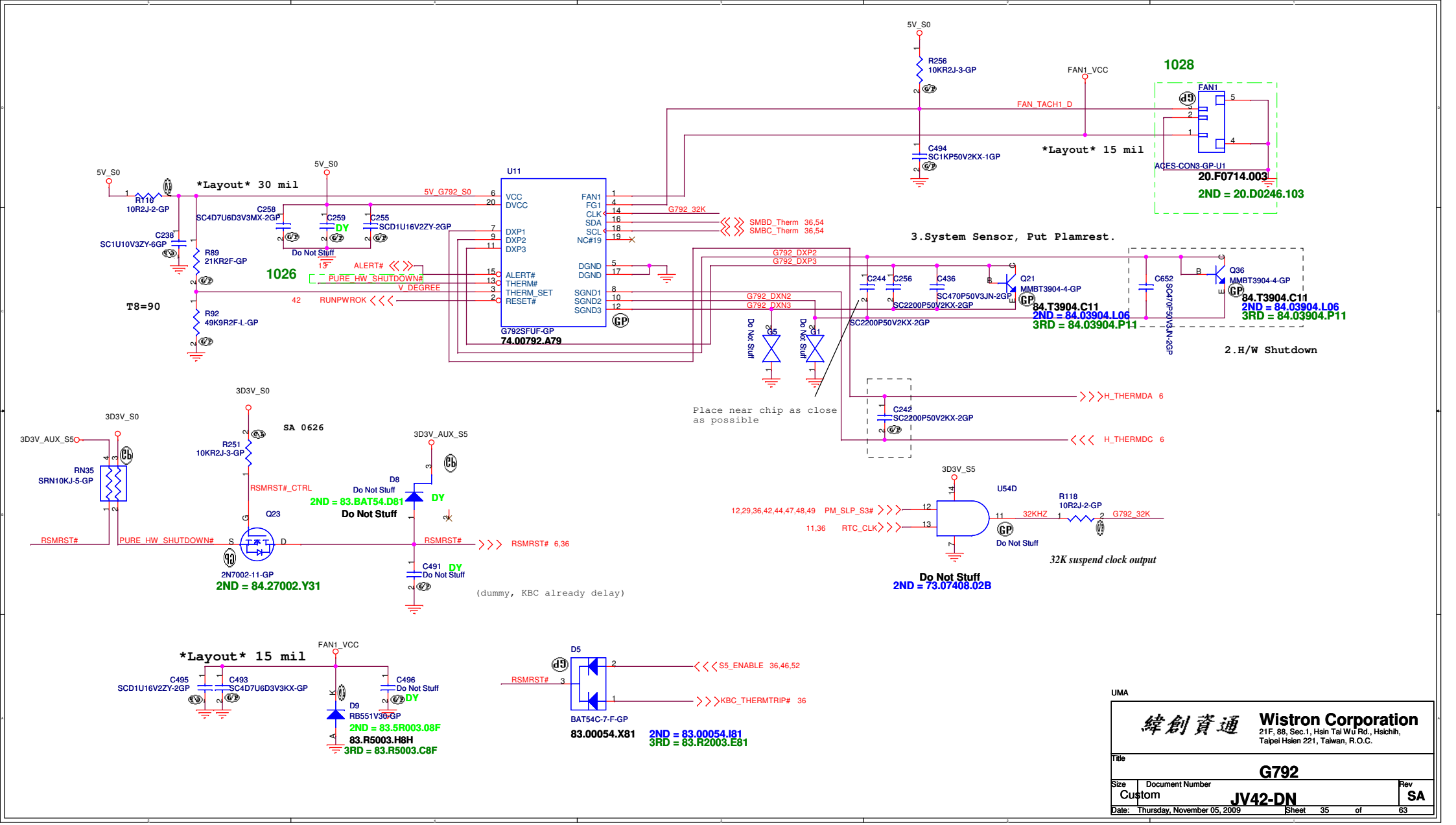

UMA

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Title	G792	
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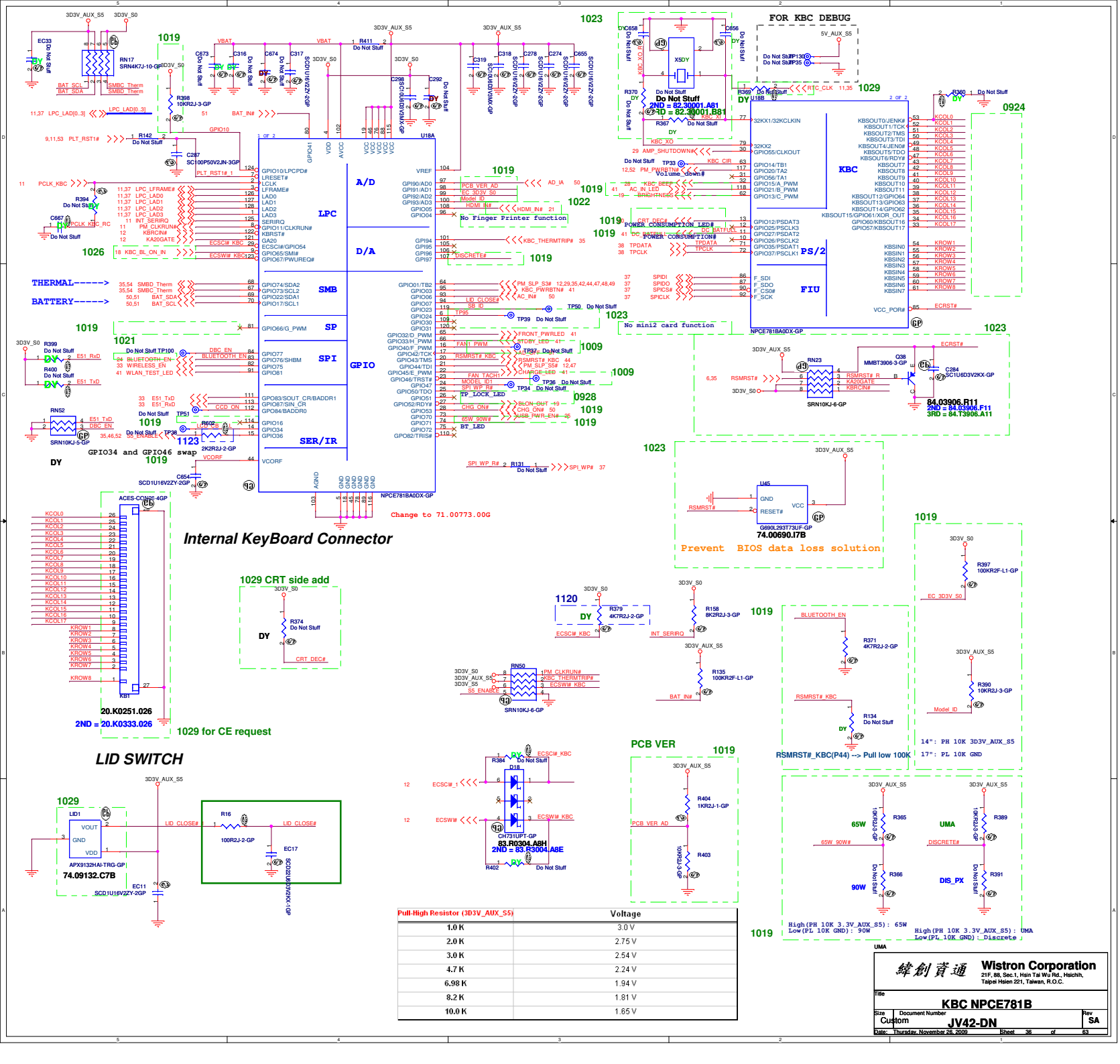
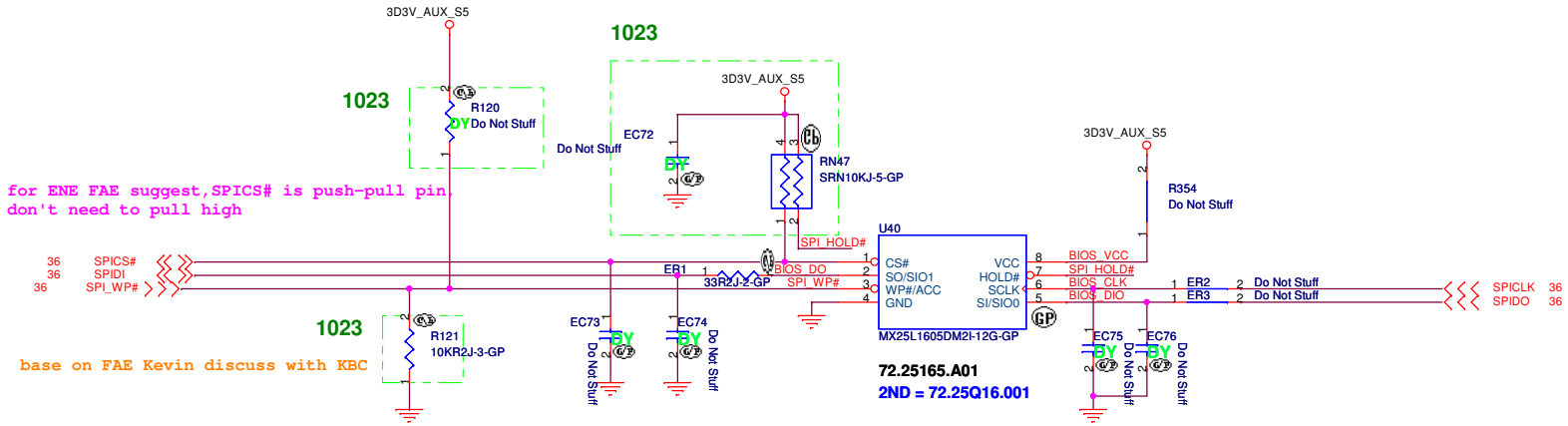


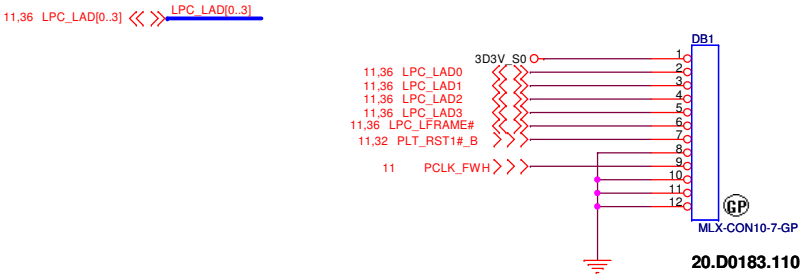
Pull-High Resistor (3D3V_AUX_S5)	Voltage
1.0 K	3.0 V
2.0 K	2.75 V
3.0 K	2.54 V
4.7 K	2.24 V
6.98 K	1.94 V
8.2 K	1.81 V
10.0 K	1.65 V



16M Bits

SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

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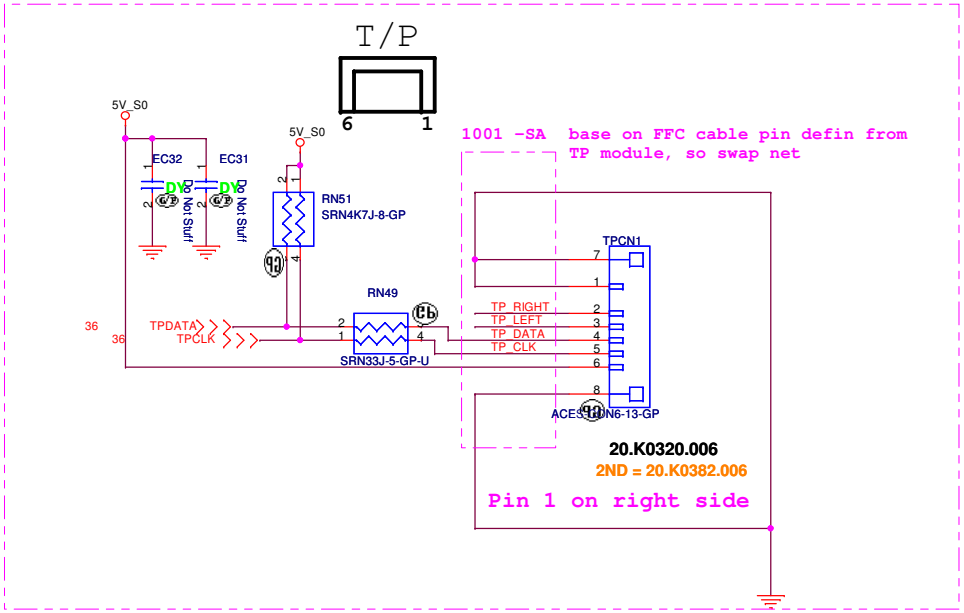

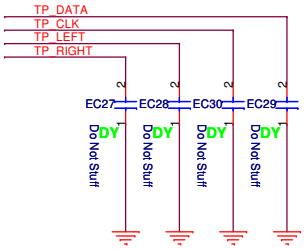

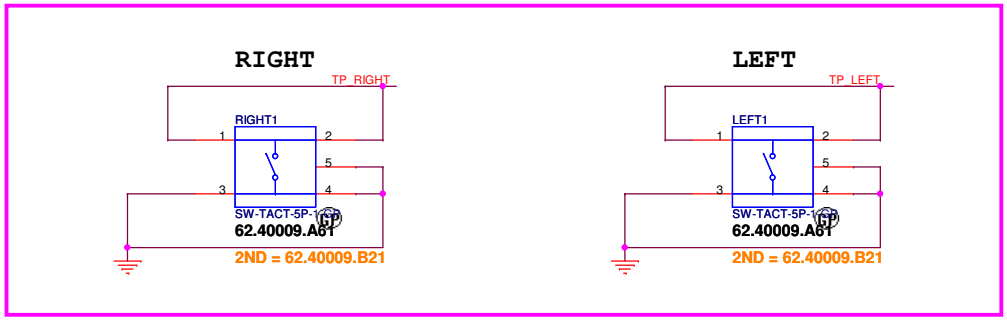

No Finger printer Function

UMA

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Title: Touch PAD

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NONE BOARD

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Title: NONE BOARD

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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SWITCH		
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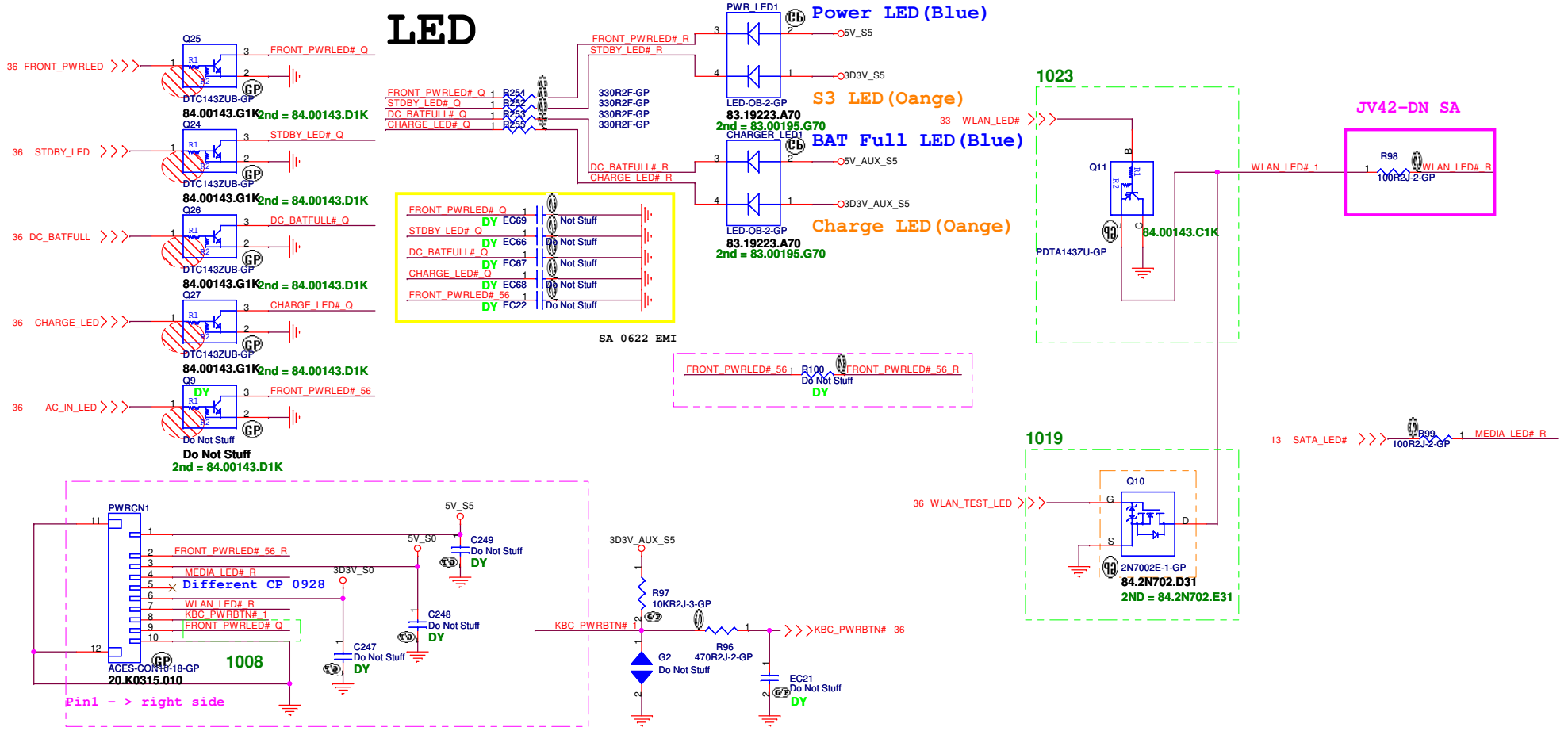
LED



Pin 1	5V_S5	
Pin 2	(DY)FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	NC	
Pin 10	GND	

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Title: LED			
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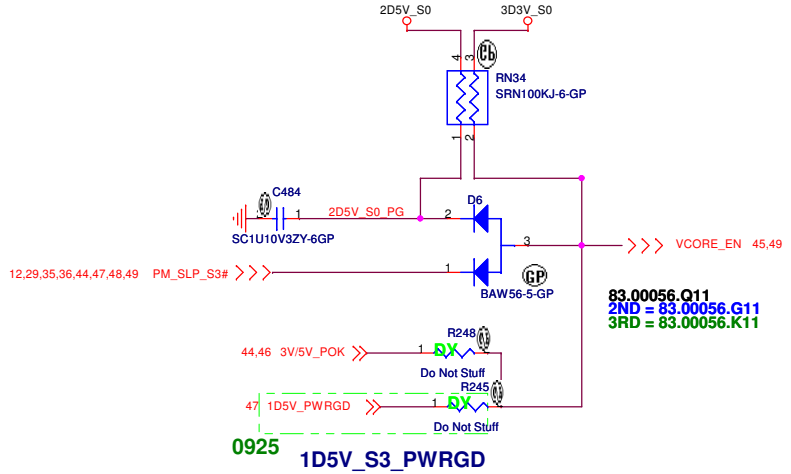
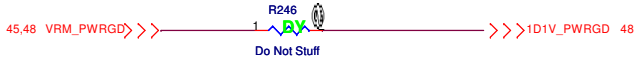
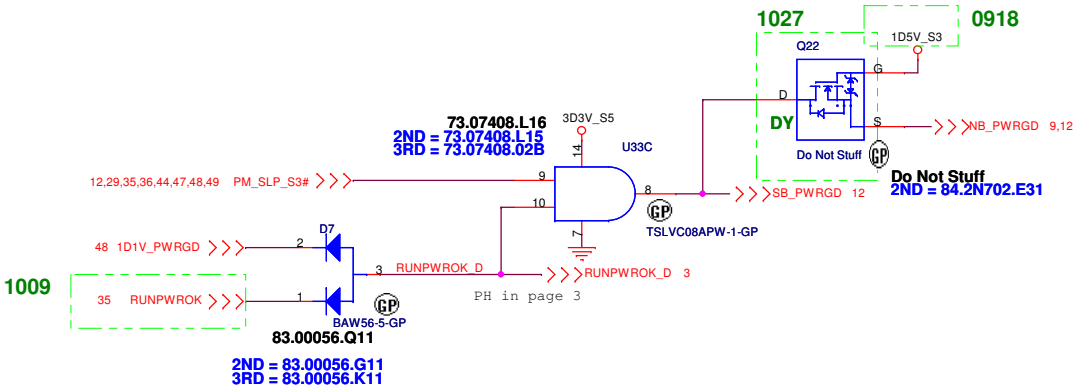


P/H @ 1D8V_S3 PAGE





UMA

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Title: POWER ON LOGIC		
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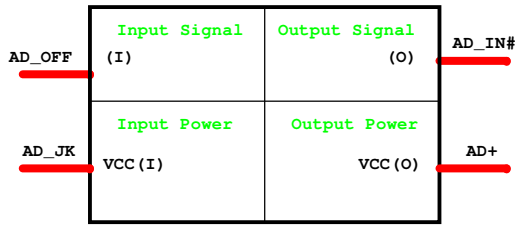
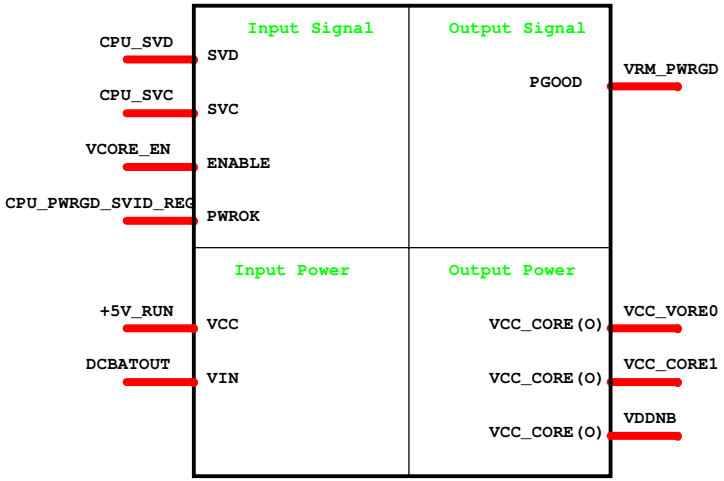
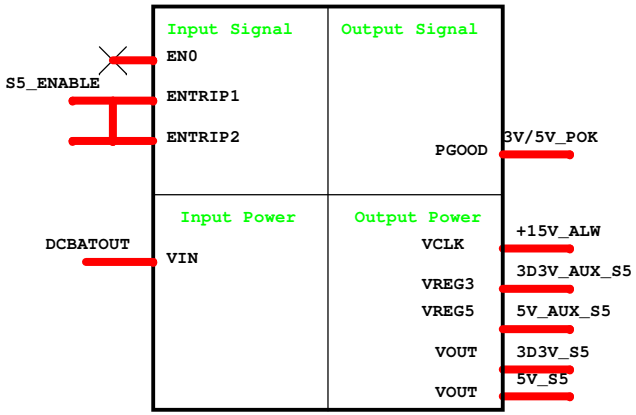
Adapter



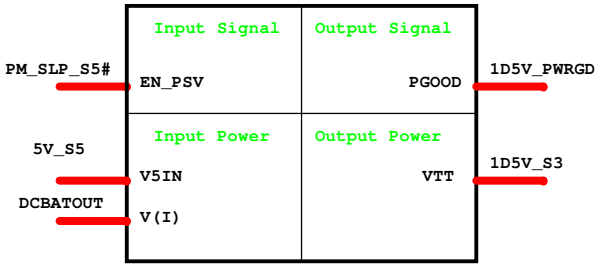
CPU_CORE
ISL6265HRTZ



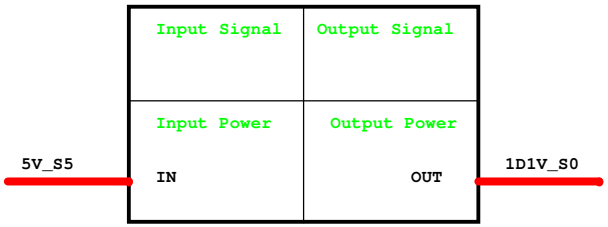
DCDC 5V/3D3V(RT8223)



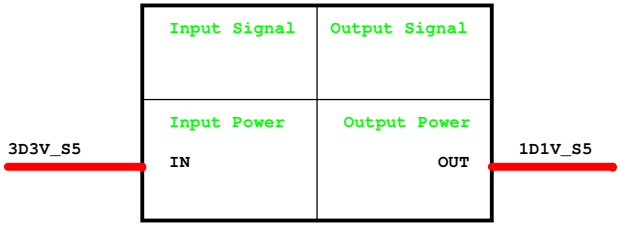
DCDC 1D5V(RT8209E)



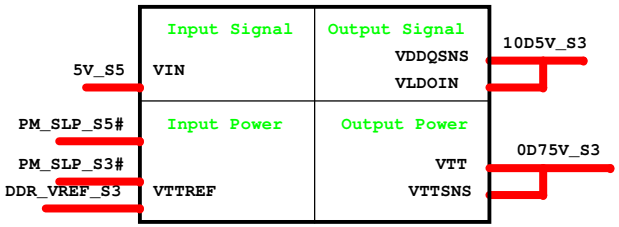
1D1V LDO RT8209E



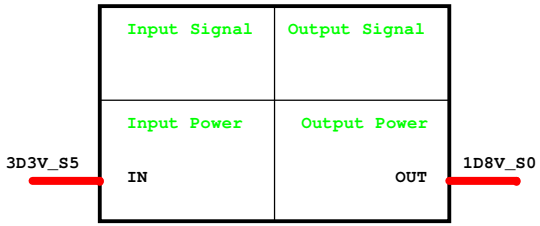
1D1V LDO RT9025



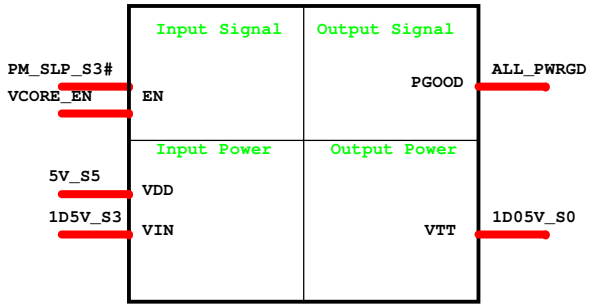
0D75V LDO RT9026



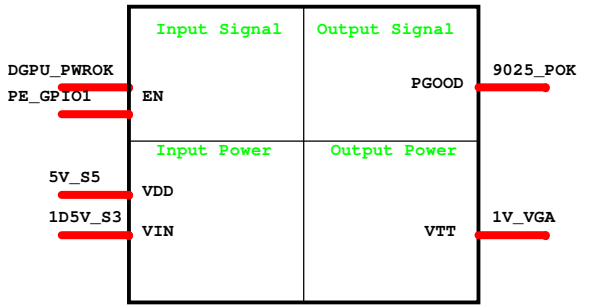
1D8V LDO RT8015A



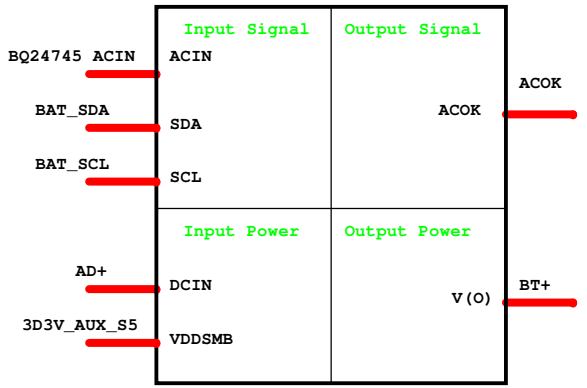
DCDC 1D05V_S0(RT9025)



DCDC 1V_VGA(RT9025)



CHARGER BQ24745



UMA

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Title: **Power Block Diagram**

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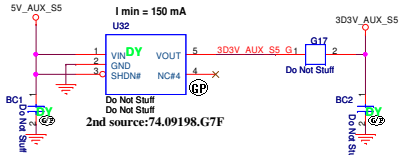
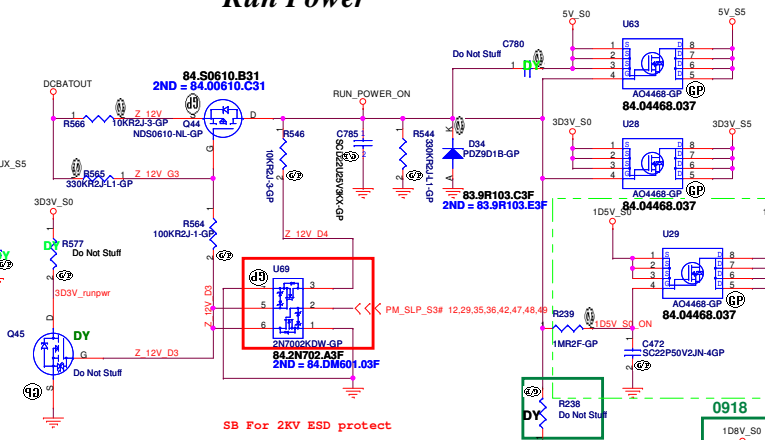
Run Power

Aux Power

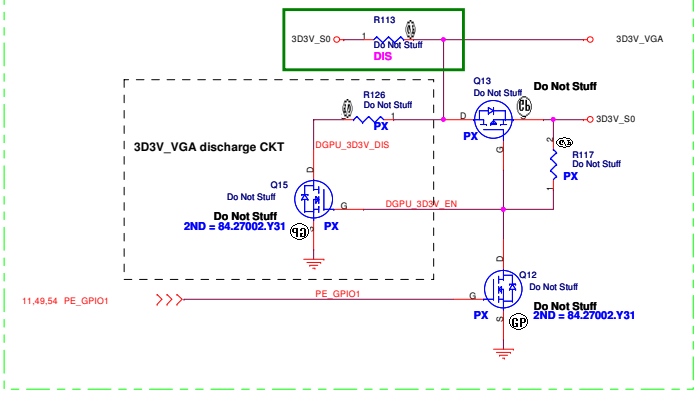
3D3V_AUX_S5



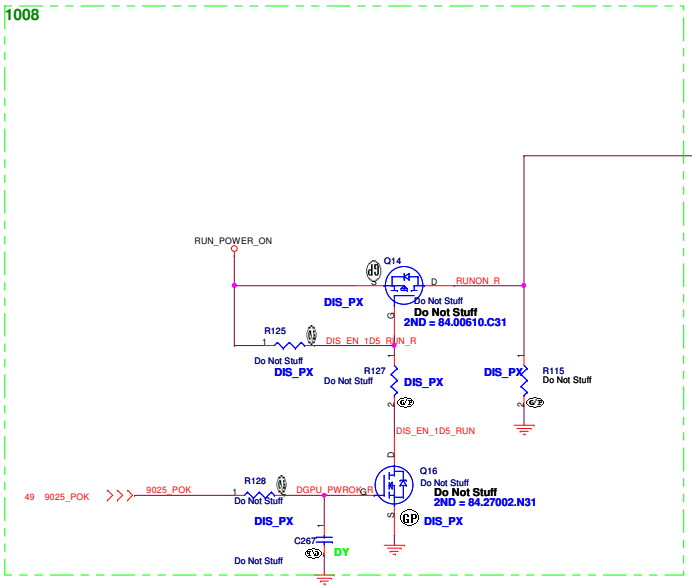


+3VS to 3.3V_DELAY Transfer

1008



1008



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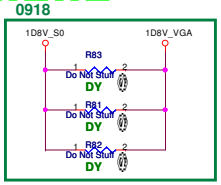

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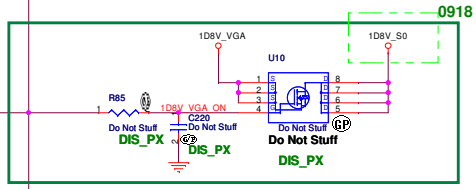
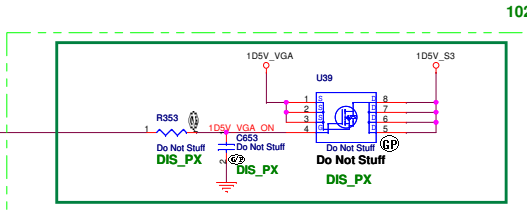
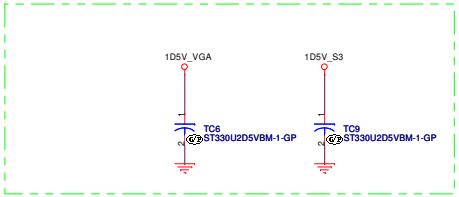


1021

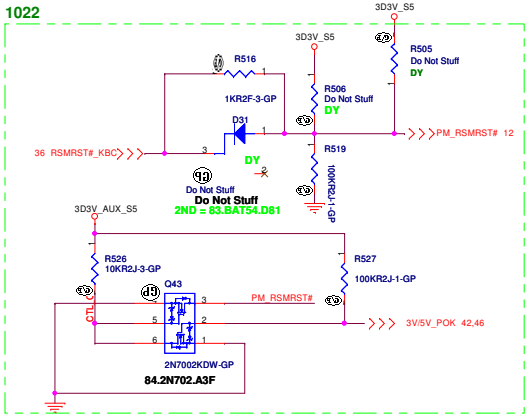


1021

Please closed U77 for Park issue

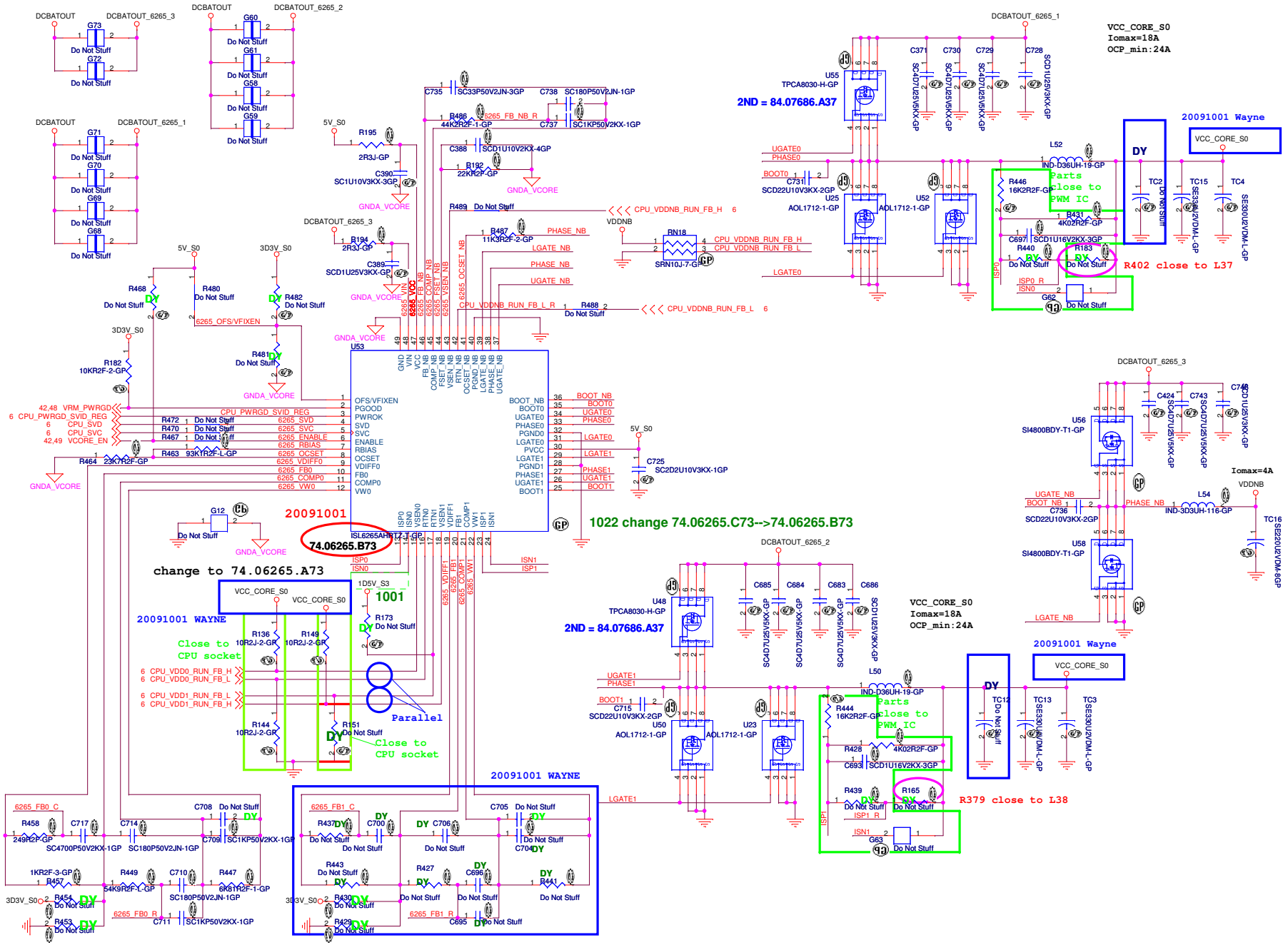


1022



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RUN AND AUX POWER		
Size: Custom	Document Number: JV42-DN	Rev: SA
Date: Tuesday, November 10, 2009	Sheet 44 of 63	


VCC_CORE_S0
Iomax=18A
OCP_min:24A
2ND = 84.07686.A37
20091001 Wayne
R402 close to L37
1022 change 74.06265.C73-->74.06265.B73
20091001
74.06265.B73
change to 74.06265.A73
20091001 WAYNE
Close to CPU socket
Parallel
1001
R379 close to L38
Parts close to PWM IC
ISL6265AHRTZ-T-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JV42-DN
Tuesday, November 10, 2009
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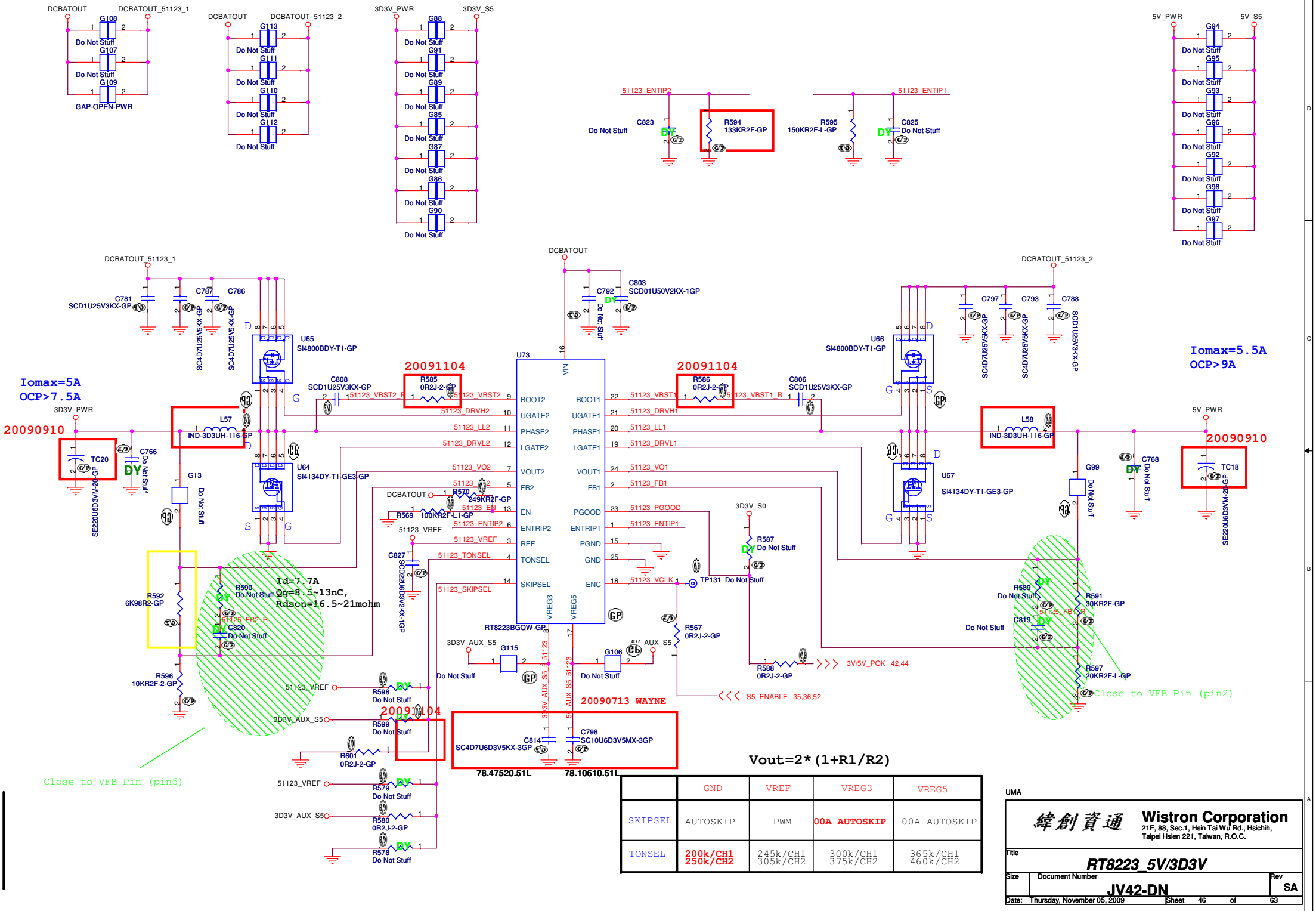

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

UMA

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Title: RT8223_5V/3D3V

Size | Document Number: JV42-DN | Rev: SA

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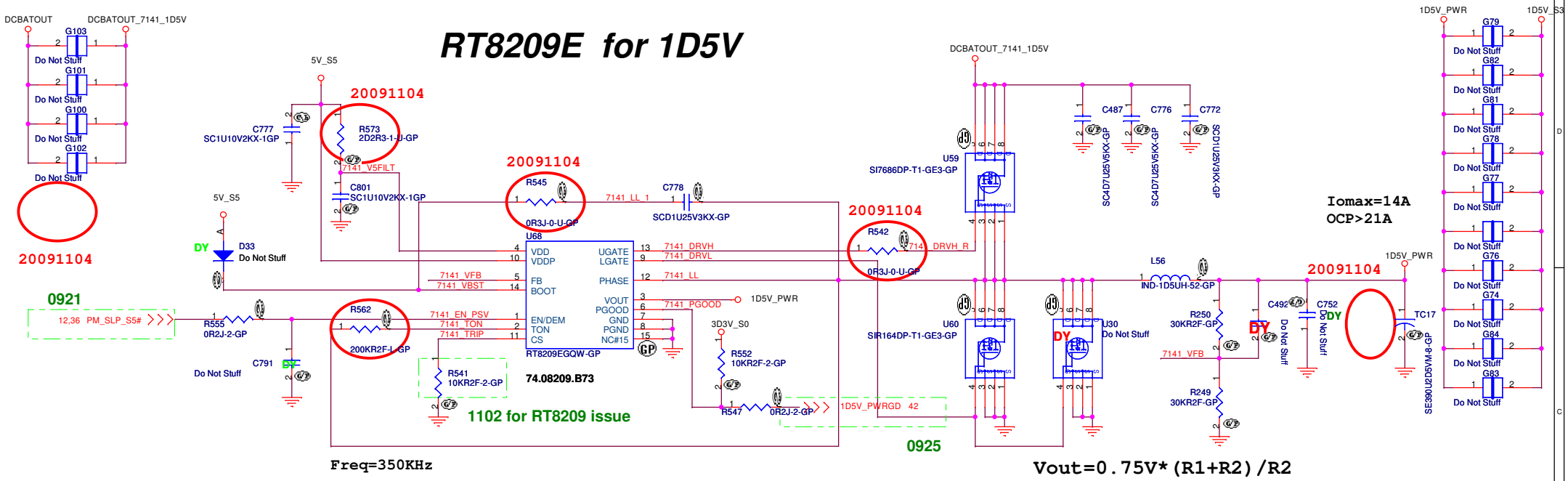
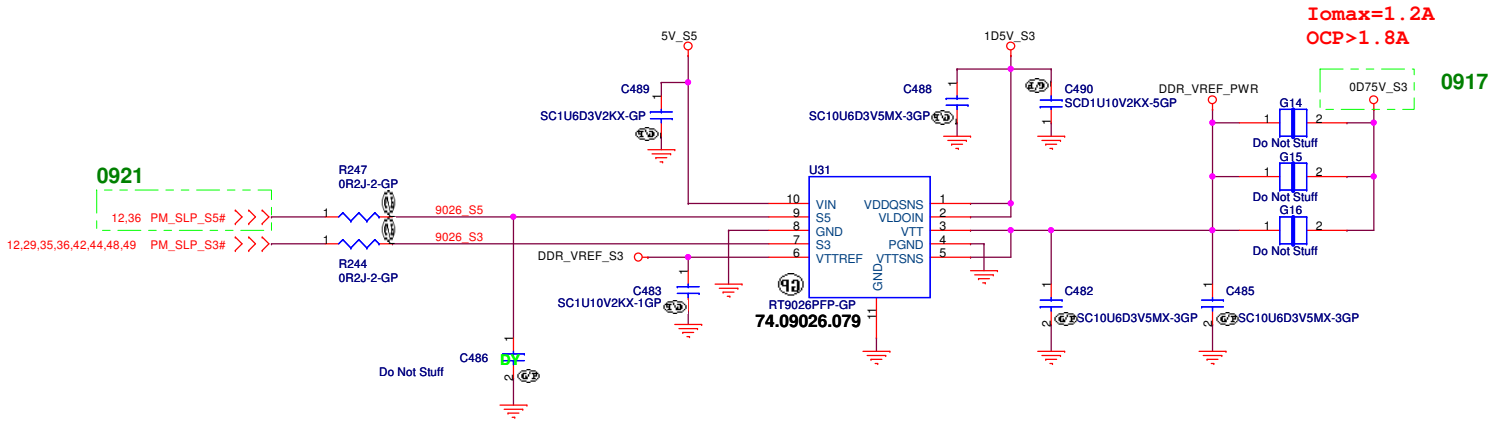
RT8209E for 1D5V



RT9026 for 0D75V_S3



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8209E 1D5V	
Size	Document Number	Rev
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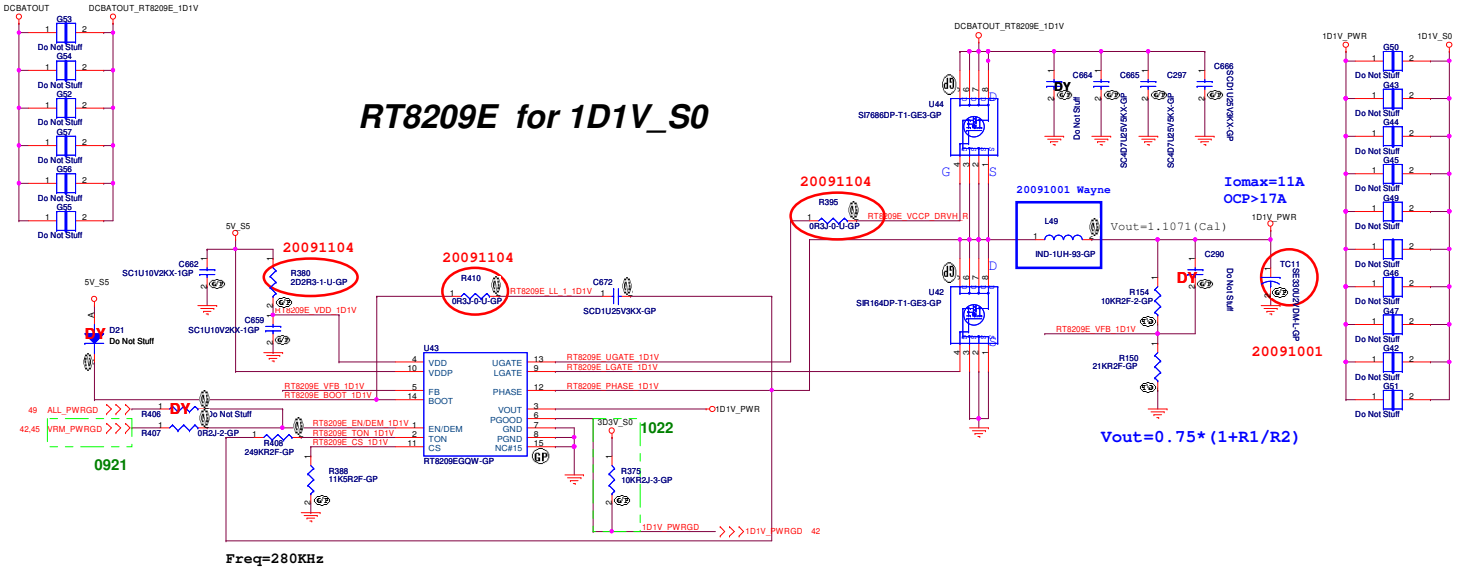
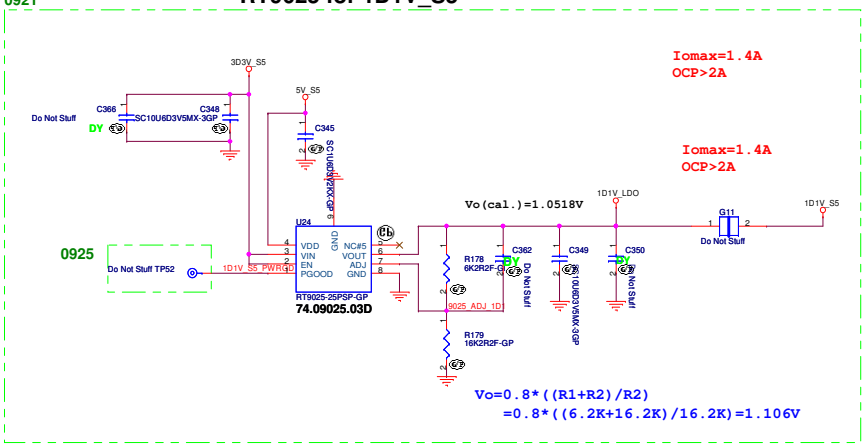
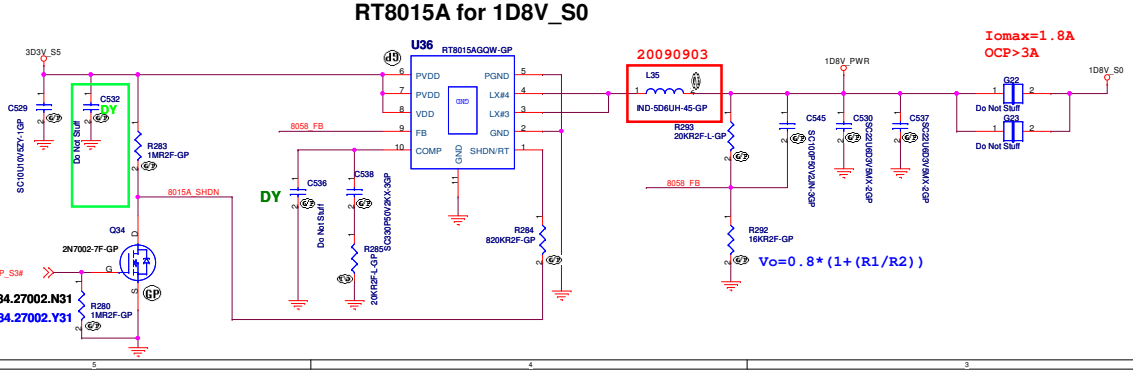
RT8209E for 1D1V_S0



RT9025 for 1D1V_S5



RT8015A for 1D8V_S0



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Title: 1D1V_S0 & 1D1V_S5 & 1D8V_S0

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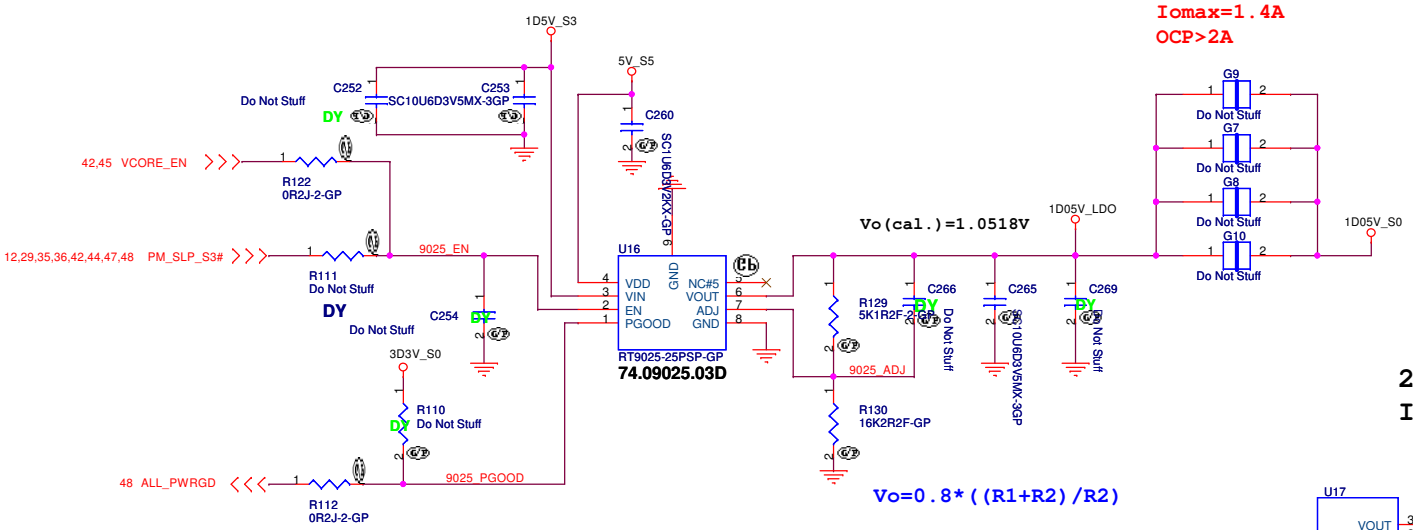
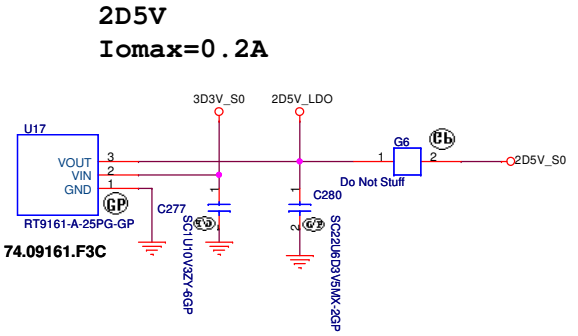
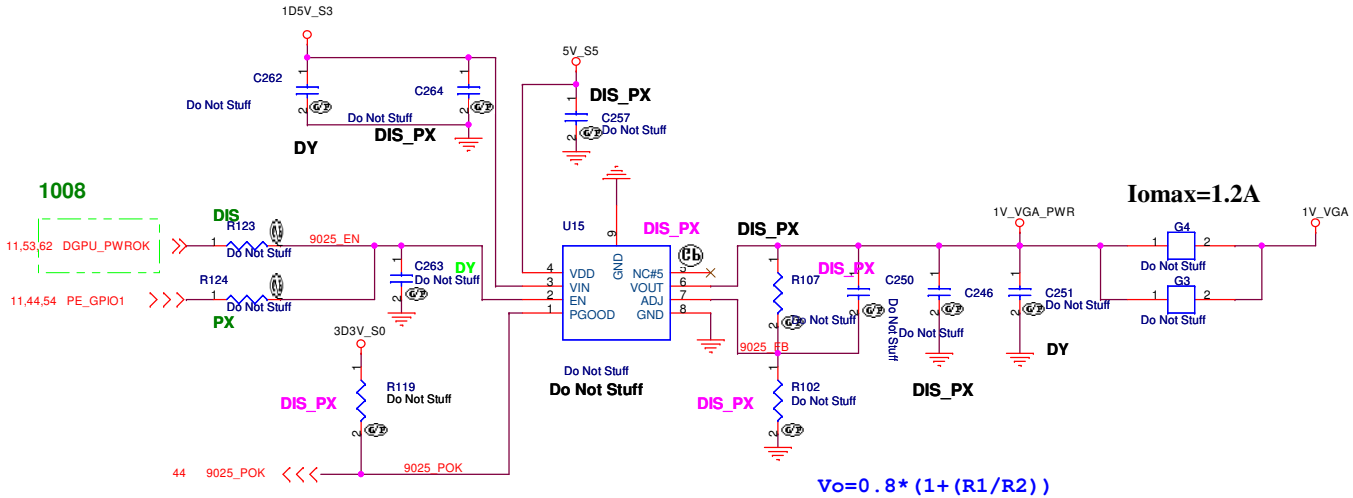
RT9025 for 1D05V_S0







UMA

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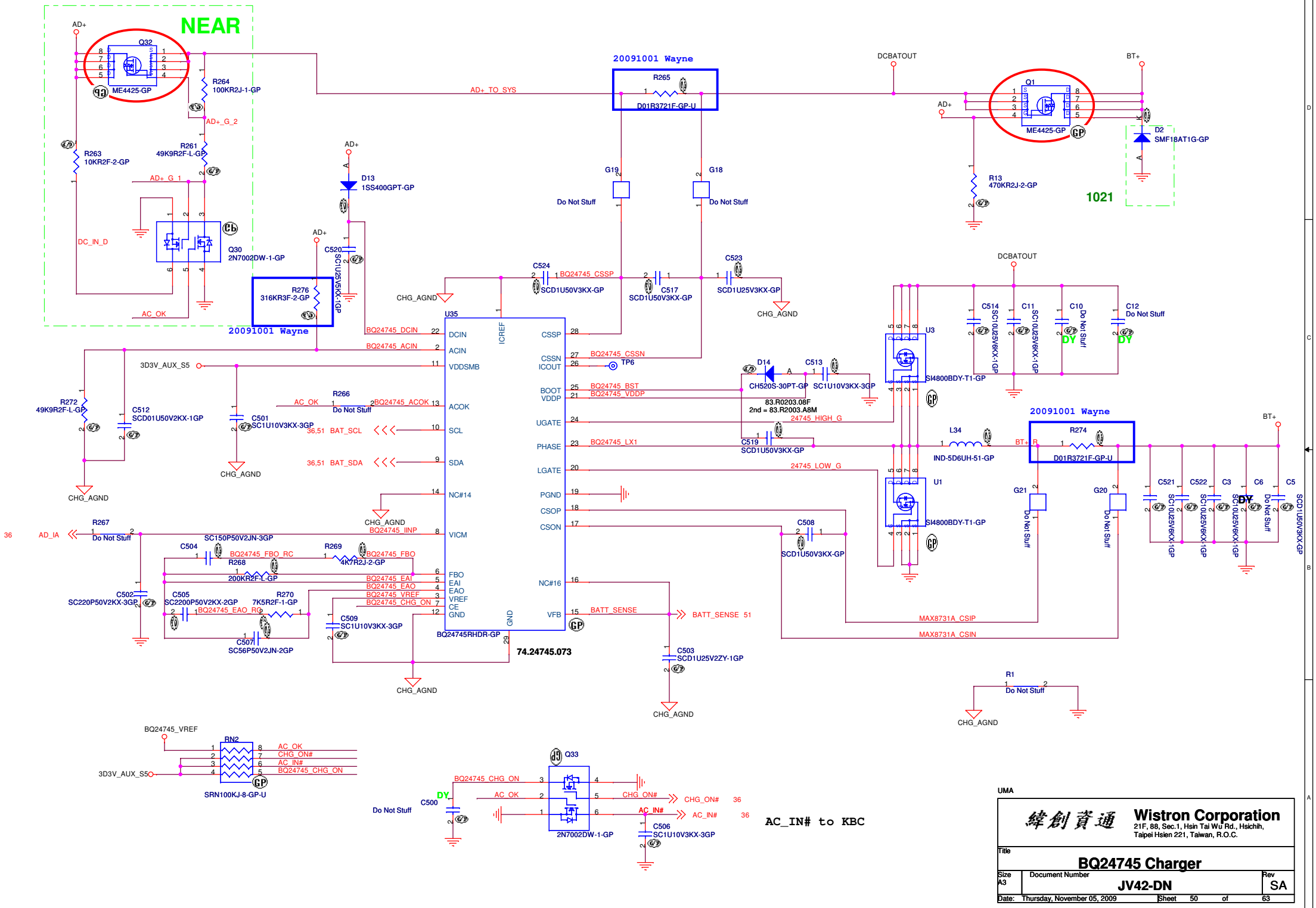
Title: LDO 1D05V/2D5V/1V		
Size: A3	Document Number: JV42-DN	Rev: SA
Date: Thursday, November 05, 2009	Sheet 49 of 63	


NEAR
AD+
Q32
ME4425-GP
R264
100KR2J-1-GP
AD+_G_2
R263
10KR2F-2-GP
R261
49K9R2F-L-GP
AD+_G_1
DC_IN_D
Q30
2N7002DW-1-GP
AC_OK
R276
316KR3F-2-GP
20091001 Wayne
D13
1SS400GPT-GP
C520
SCD1U25V3KX-1GP
AD+_TO_SYS
R265
D01R3721F-GP-U
G19
G18
Do Not Stuff
C524
SCD1U50V3KX-GP
C517
SCD1U50V3KX-GP
C523
SCD1U25V3KX-GP
CHG_AGND
DCBATOUT
BT+
Q1
ME4425-GP
D2
SMF18AT1G-GP
R13
470KR2J-2-GP
1021
U35
BQ24745RHDR-GP
ICREF
GND
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
BQ24745_DCIN
BQ24745_ACIN
BQ24745_CSSP
BQ24745_CSSN
BQ24745_BST
BQ24745_VDDP
BQ24745_LX1
BQ24745_IINP
BQ24745_FBO
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
BATT_SENSE
74.24745.073
3D3V_AUX_S5
R272
49K9R2F-L-GP
C512
SCD01U50V2KX-1GP
C501
SC1U10V3KX-3GP
R266
Do Not Stuff
AC_OK
BQ24745_ACOK
36,51 BAT_SCL
36,51 BAT_SDA
TP6
D14
CH520S-30PT-GP
C513
SC1U10V3KX-3GP
83.R0203.08F
2nd = 83.R2003.A8M
C519
SCD1U50V3KX-GP
24745_HIGH_G
24745_LOW_G
U3
U1
SI4800BDY-T1-GP
L34
IND-5D6UH-51-GP
R274
D01R3721F-GP-U
C514
C11
C10
C12
C521
C522
C3
C6
C5
DY
Do Not Stuff
C508
SCD1U50V3KX-GP
MAX8731A_CSIP
MAX8731A_CSIN
G21
G20
R267
SC150P50V2JN-3GP
AD_IA
C504
R268
200KR2F-1-GP
R269
4K7R2J-2-GP
C502
SC220P50V2KX-3GP
C505
SC2200P50V2KX-2GP
R270
7K5R2F-1-GP
C507
SC56P50V2JN-2GP
C509
SC1U10V3KX-3GP
C503
SCD1U25V2ZY-1GP
R1
BQ24745_VREF
RN2
SRN100KJ-8-GP-U
AC_IN#
CHG_ON#
Q33
2N7002DW-1-GP
C500
C506
SC1U10V3KX-3GP
AC_IN# to KBC
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size
A3
Document Number
JV42-DN
Rev
SA
Date: Thursday, November 05, 2009
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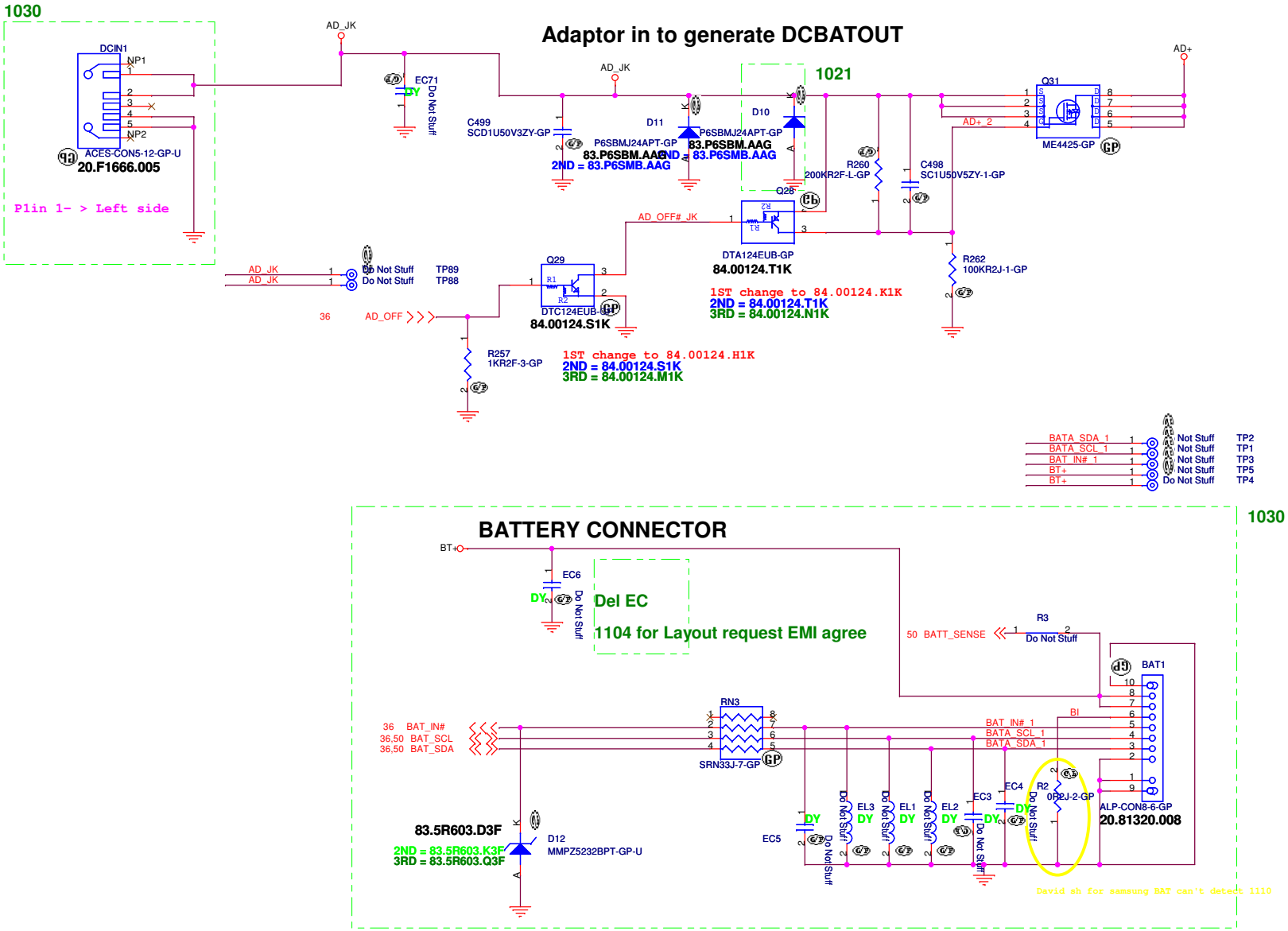

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
	JV42-DN	SA

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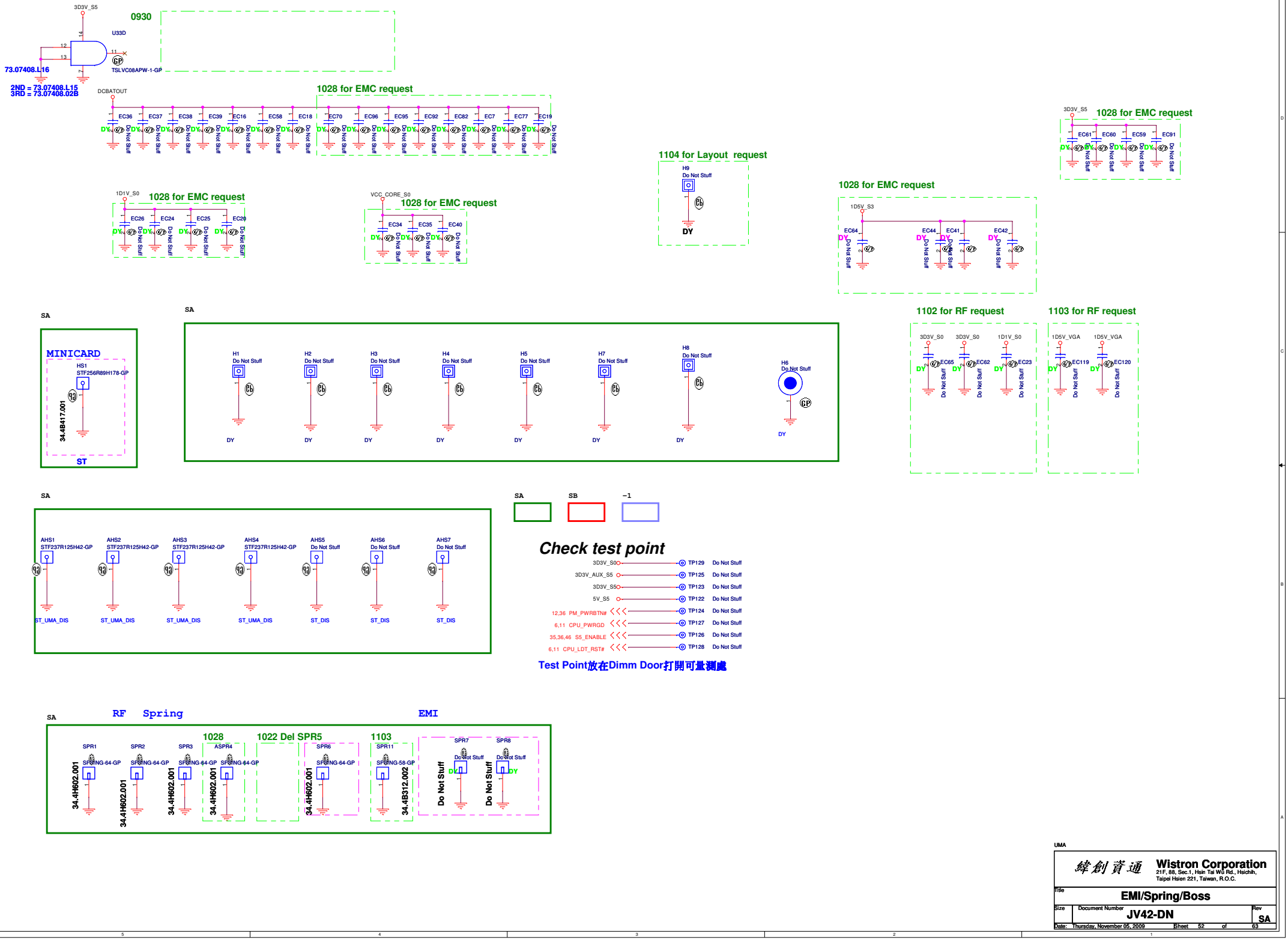
3D3V_S5
0930
U33D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
DCBATOUT
1028 for EMC request
EC36 EC37 EC38 EC39 EC16 EC58 EC18 EC70 EC96 EC95 EC92 EC82 EC7 EC77 EC19
1D1V_S0
1028 for EMC request
EC26 EC24 EC25 EC20
VCC_CORE_S0
1028 for EMC request
EC34 EC35 EC40
1104 for Layout request
H9
Do Not Stuff
DY
1028 for EMC request
1D5V_S3
EC64 EC44 EC41 EC42
3D3V_S5
1028 for EMC request
EC61 EC60 EC59 EC91
SA
MINICARD
HS1
STF256R89H178-GP
34.4B417.001
ST
SA
H1 H2 H3 H4 H5 H7 H8
Do Not Stuff
DY
H6
Do Not Stuff
1102 for RF request
3D3V_S0 3D3V_S0 1D1V_S0
EC65 EC62 EC23
1103 for RF request
1D5V_VGA 1D5V_VGA
EC119 EC120
SA
AHS1 AHS2 AHS3 AHS4 AHS5 AHS6 AHS7
STF237R125H42-GP
Do Not Stuff
ST_UMA_DIS
ST_DIS
SA SB -1
Check test point
3D3V_S0 TP129 Do Not Stuff
3D3V_AUX_S5 TP125 Do Not Stuff
3D3V_S5 TP123 Do Not Stuff
5V_S5 TP122 Do Not Stuff
12,36 PM_PWRBTN# TP124 Do Not Stuff
6,11 CPU_PWRGD TP127 Do Not Stuff
35,36,46 S5_ENABLE TP126 Do Not Stuff
6,11 CPU_LDT_RST# TP128 Do Not Stuff
Test Point放在Dimm Door打開可量測處
SA
RF Spring
EMI
1028
1022 Del SPR5
1103
SPR1 SPR2 SPR3 ASPR4 SPR6 SPR11 SPR7 SPR8
SPRING-64-GP
SPRING-58-GP
34.4H602.001
34.4B312.002
Do Not Stuff
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
JV42-DN
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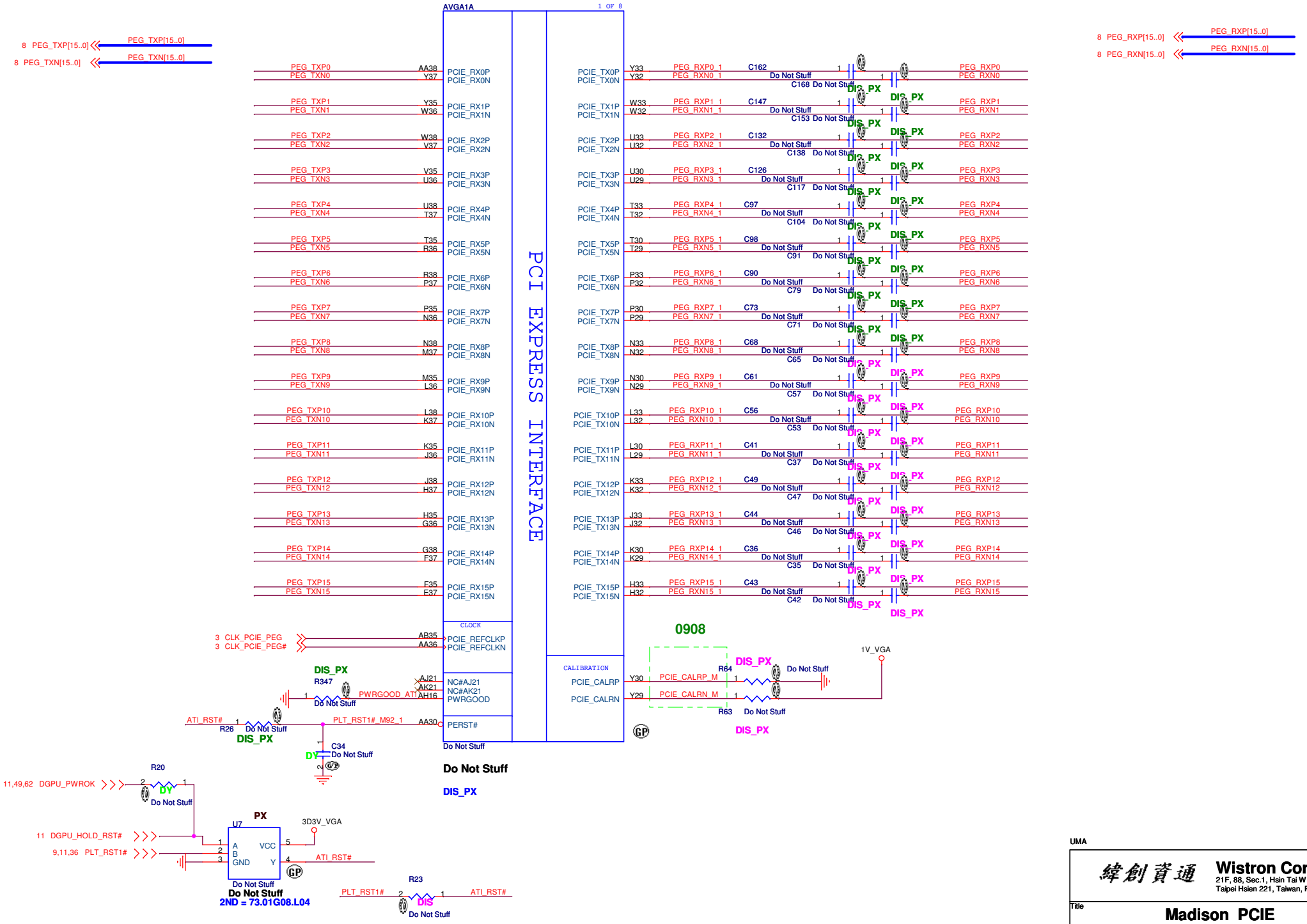

UMA

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Title: Madison PCIE		
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Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)

It's strap for GDDR3-136ball
Need to Clarify

1102 DEL FOR VGA PLANE

VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

For Thermal_sensor

SB 0817

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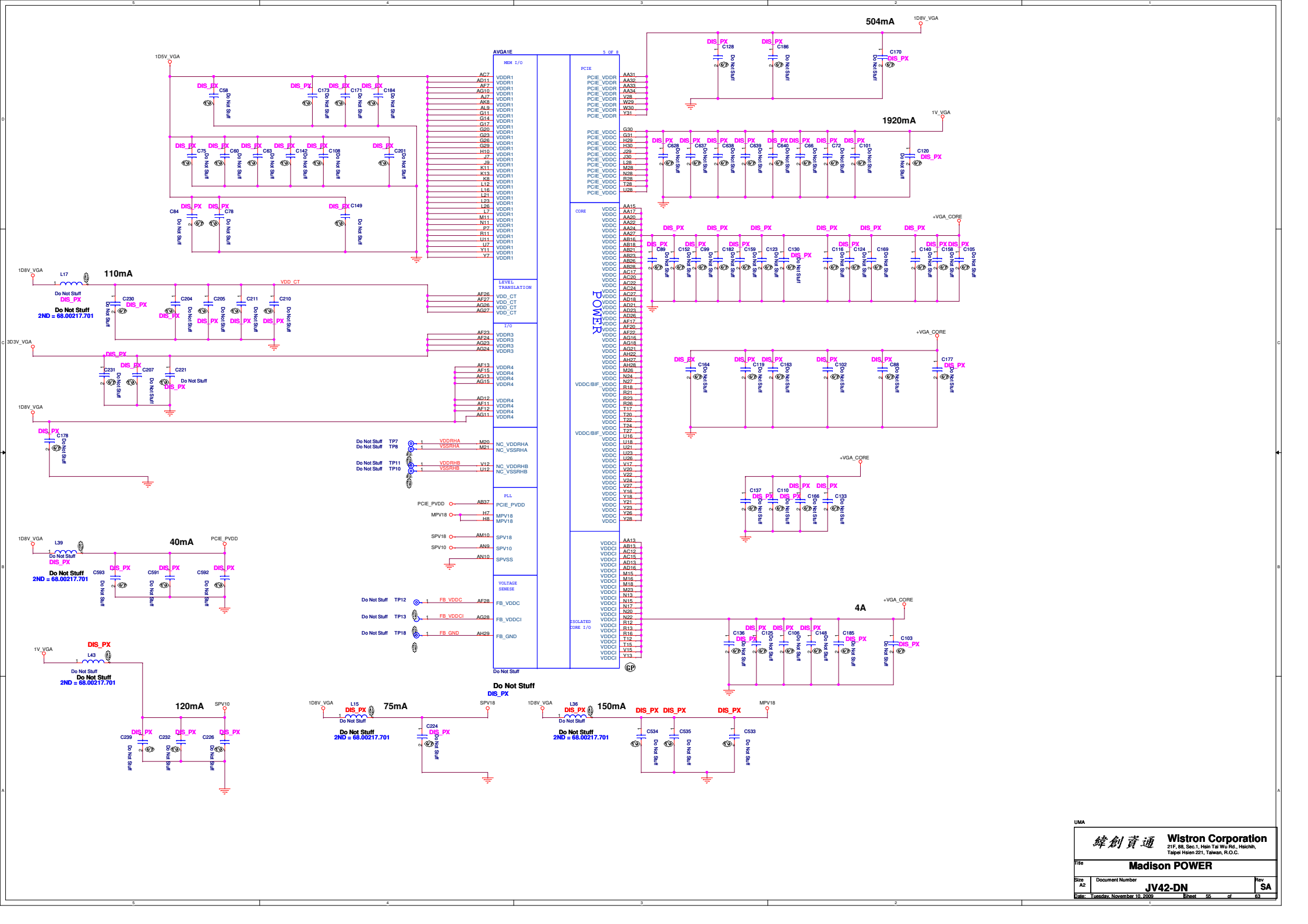
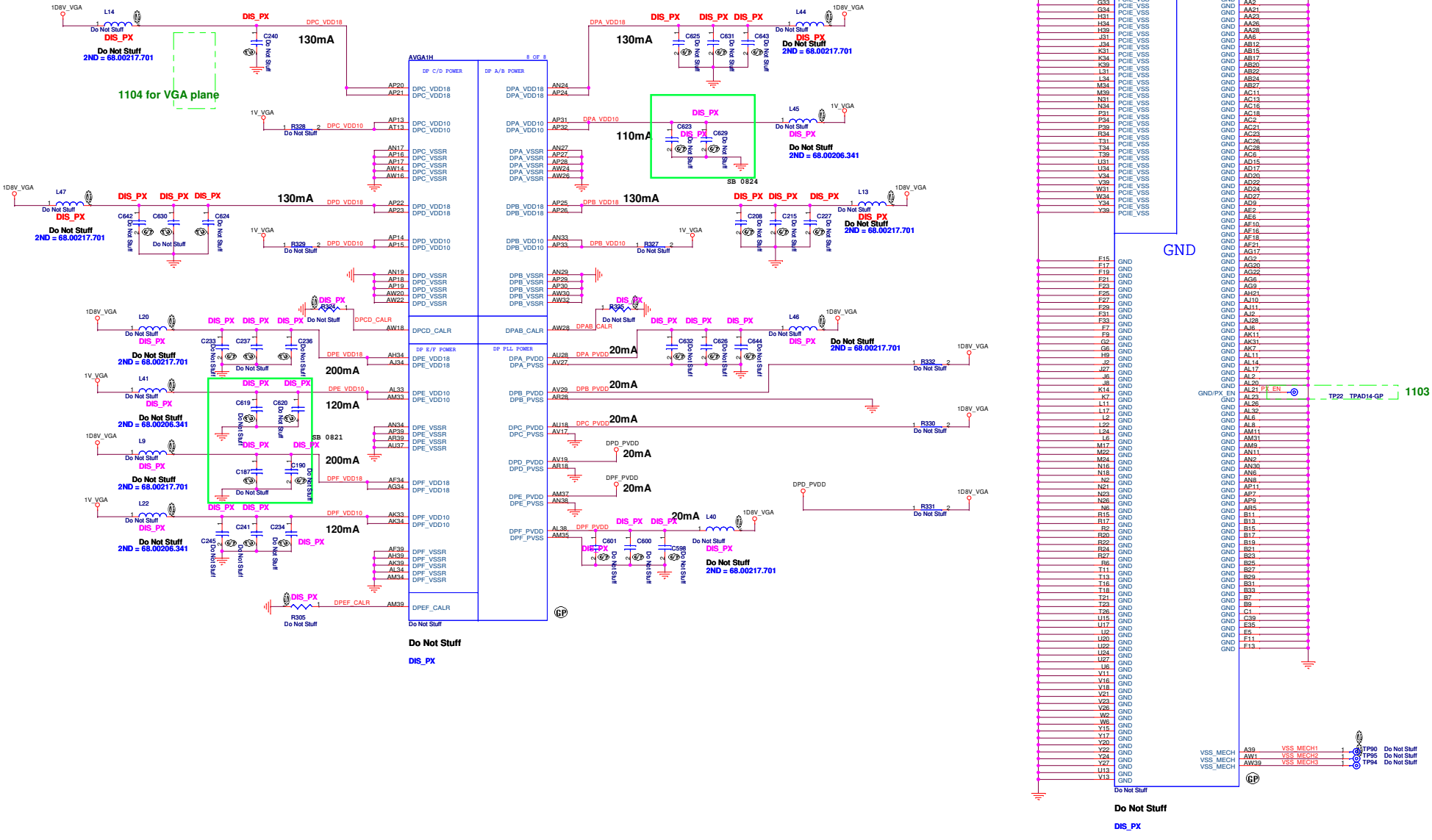
Title: Madison IO
Size: Document Number: JV42-DN Rev: SA
Date: Tuesday, November 10, 2009 Sheet 54 of 63


504mA
1920mA
+VGA_CORE
4A
110mA
40mA
120mA
75mA
150mA
Do Not Stuff
2ND = 68.00217.701
AVGA1E
MEM I/O
PCIE
CORE
POWER
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENSE
ISOLATED CORE I/O
1D5V_VGA
1D8V_VGA
1V_VGA
3D3V_VGA
PCIE_PVDD
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison POWER
JV42-DN
SA
Tuesday, November 10, 2009


1104 for VGA plane
130mA
110mA
200mA
120mA
20mA
SB 0824
SB 0821
Do Not Stuff
DIS_PX
2ND = 68.00217.701
2ND = 68.00206.341
GND
1103
TP22 TPAD14-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DP POWER_GND
JV42-DN
SA
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63

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used

Madison->71.MDSON.M01, Park->71.0PARK.M04

Do Not Stuff

DIS_PX

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

1029 for A11

1103

1026

1009 for A11

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

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Title: Madison Memory / Straps

Size: A2 | Document Number: JV42-DN | Rev: SA

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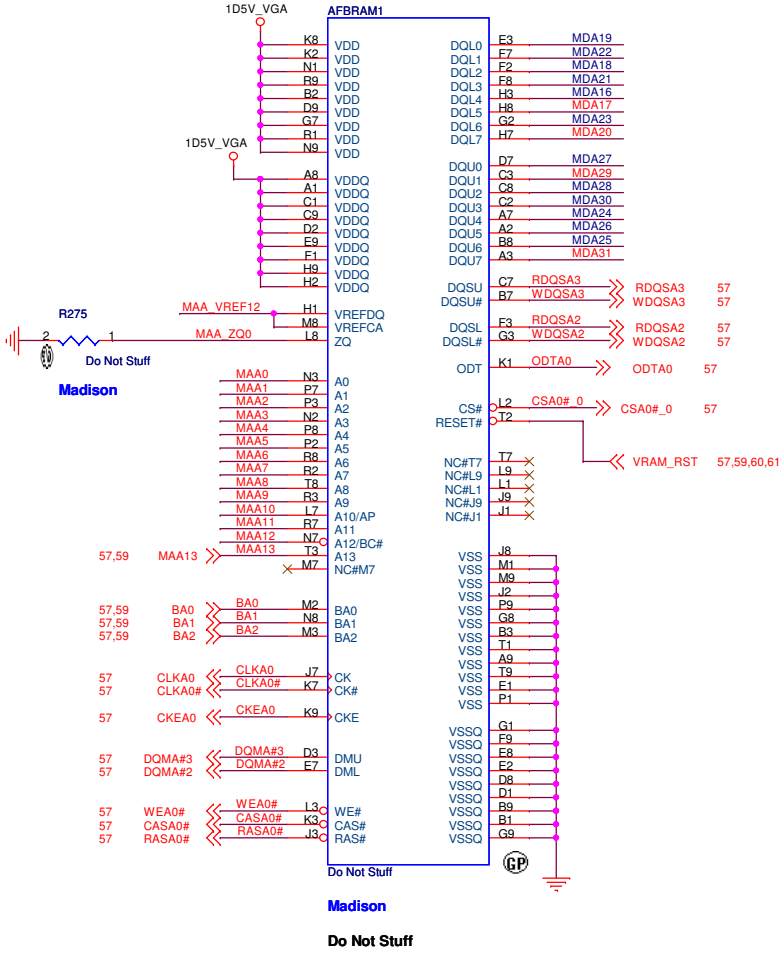
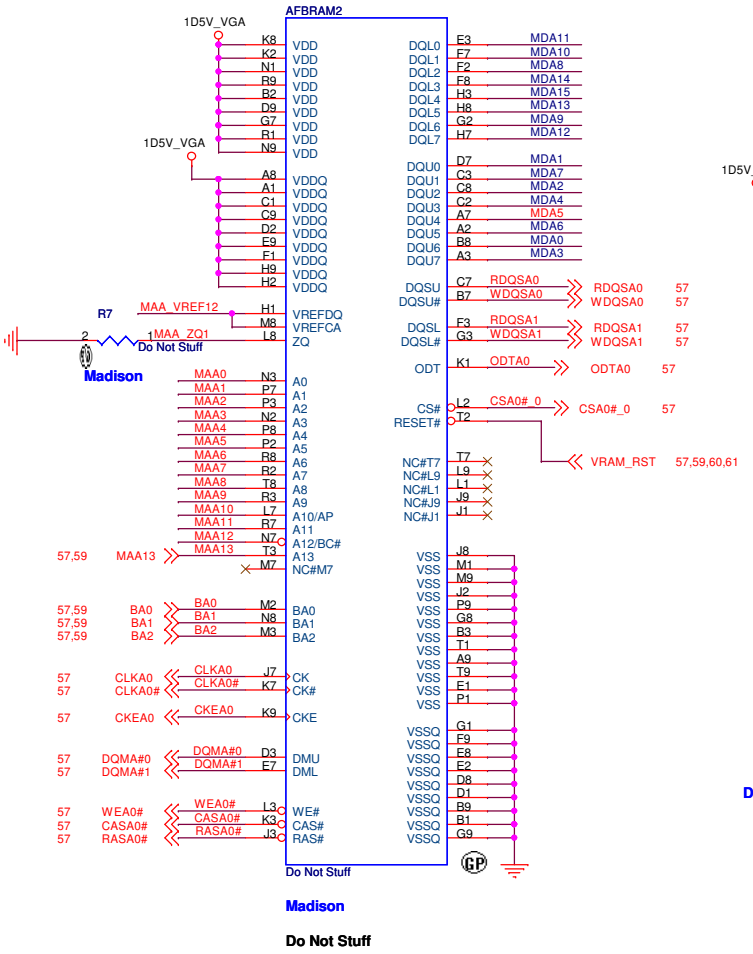
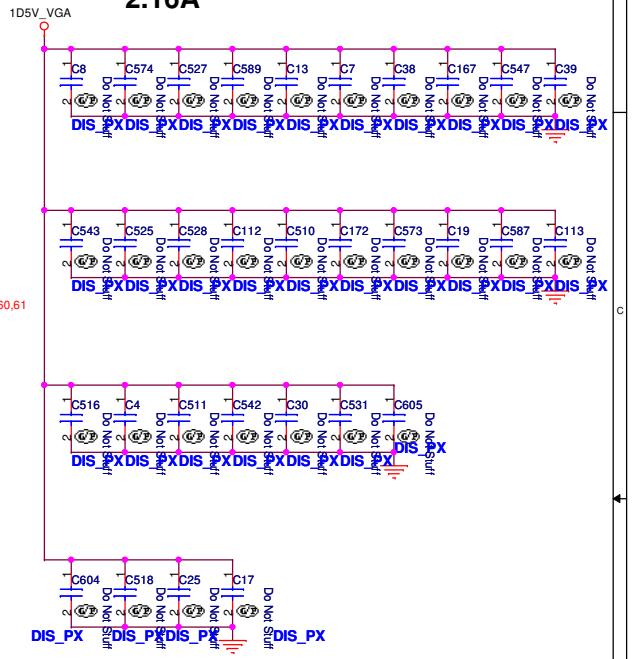
DDR3



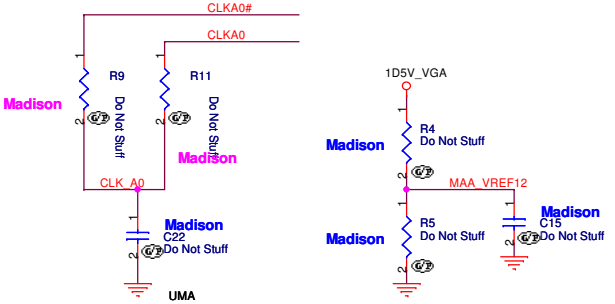


2.16A



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

57,59 DQMA#[0..7]
57,59 RDQSA[0..7]
57,59 WDQSA[0..7]
57,59 MAA[0..12] MAA[0..12]
57,59 MDA[0..63] MDA[0..63]



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM(1/4)**

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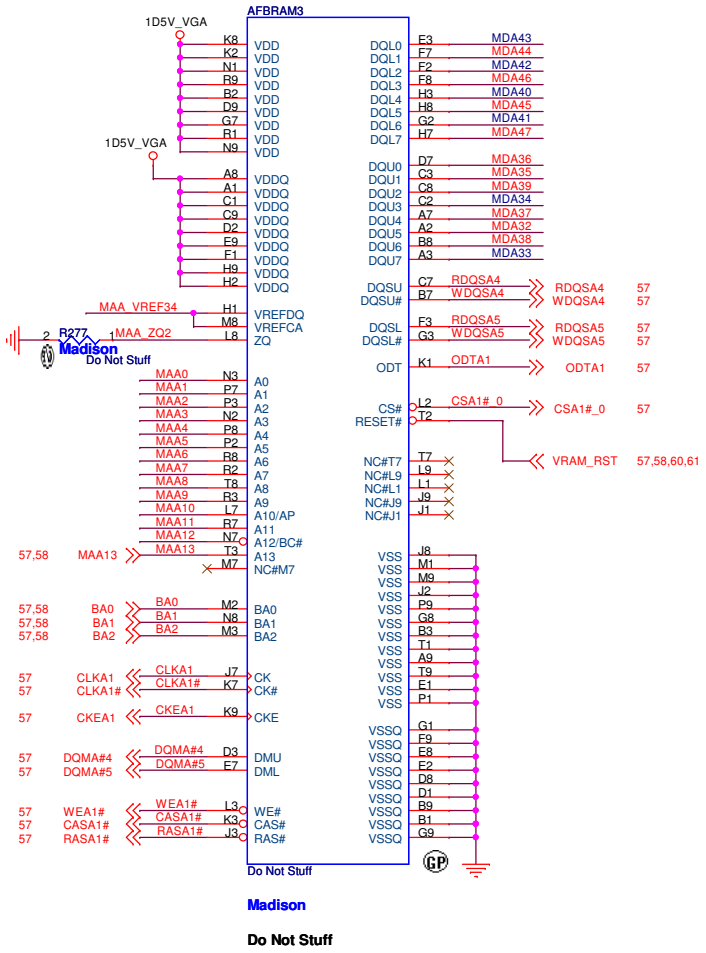
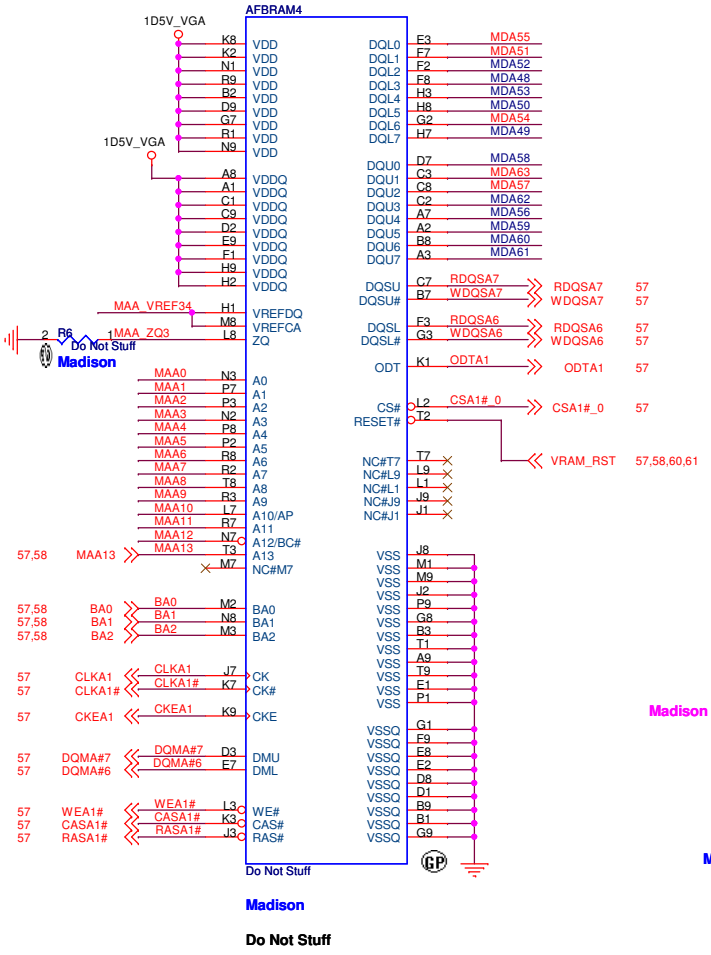
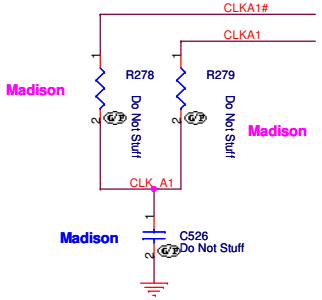
DDR3







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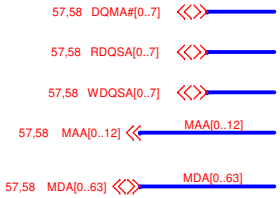
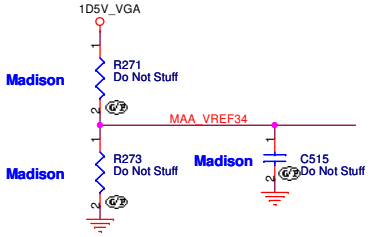
HYNIX: 72.51G63.C0U





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Title: ***VRAM(2/4)***

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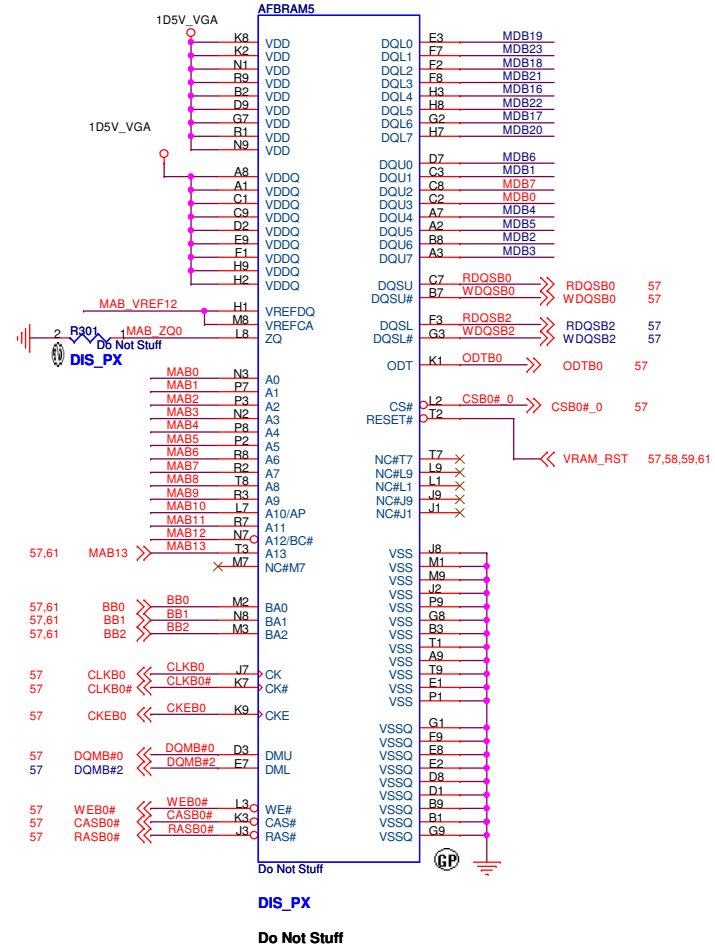
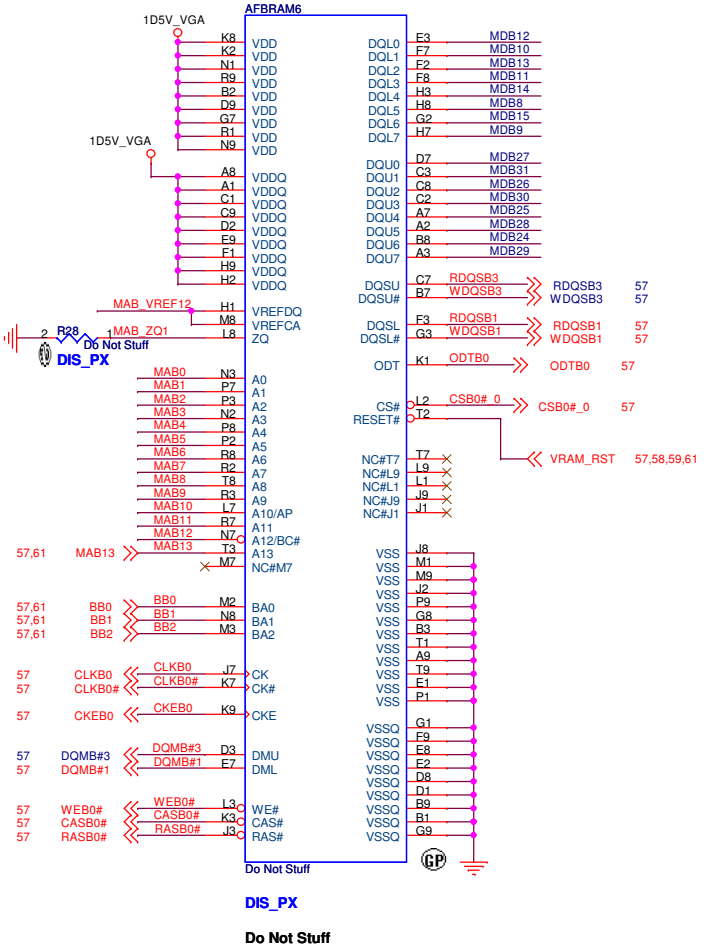
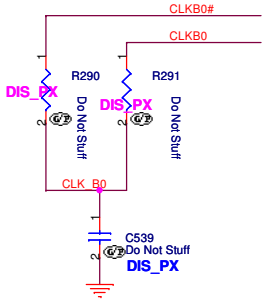
DDR3







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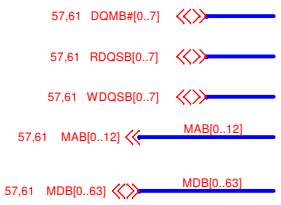

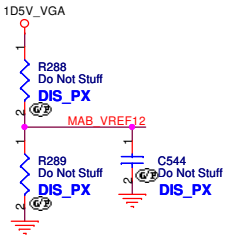

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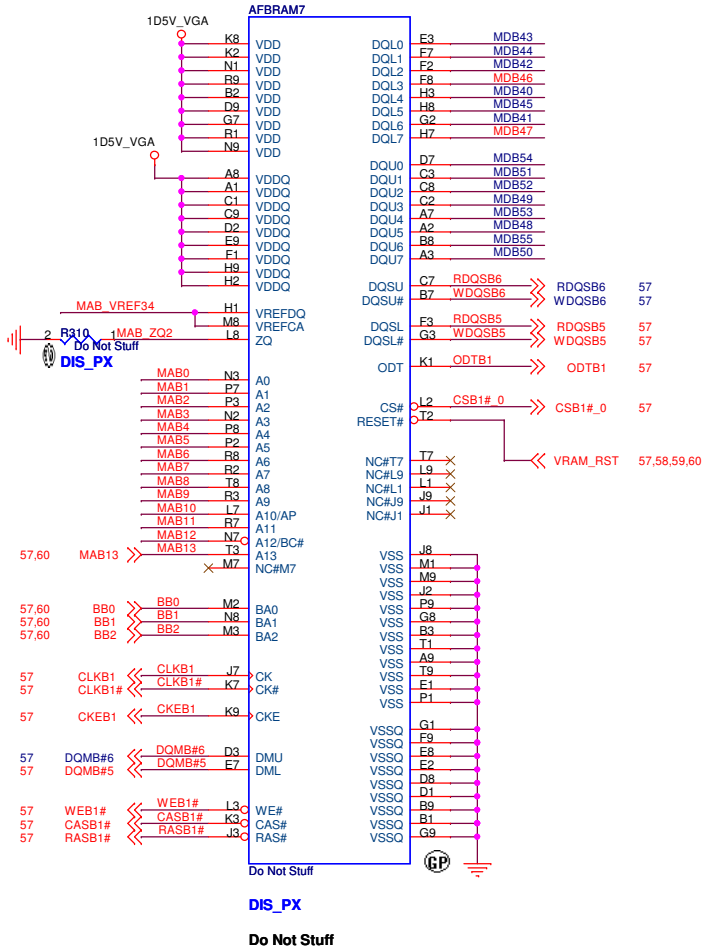
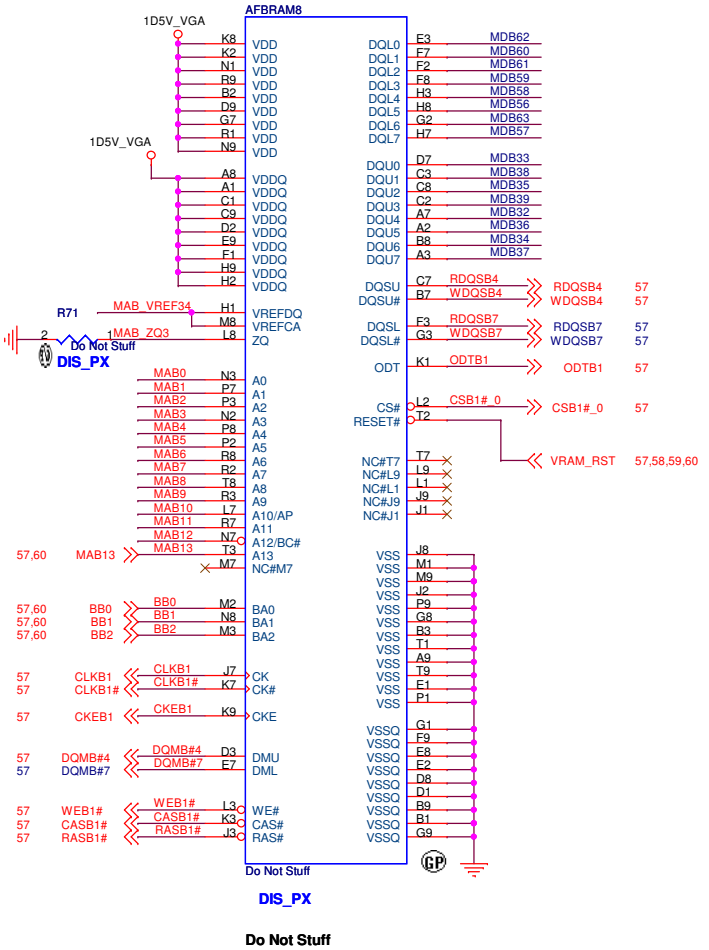
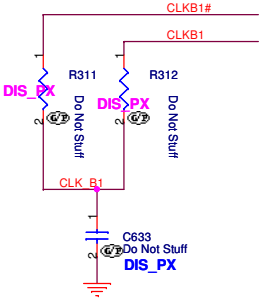
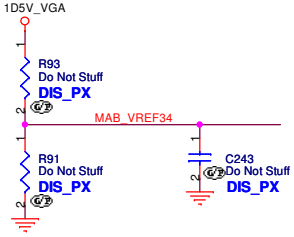
DDR3









SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

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57,60 WDQSB[0..7]
57,60 MAB[0..12] — MAB[0..12]
57,60 MDB[0..63] — MDB[0..63]

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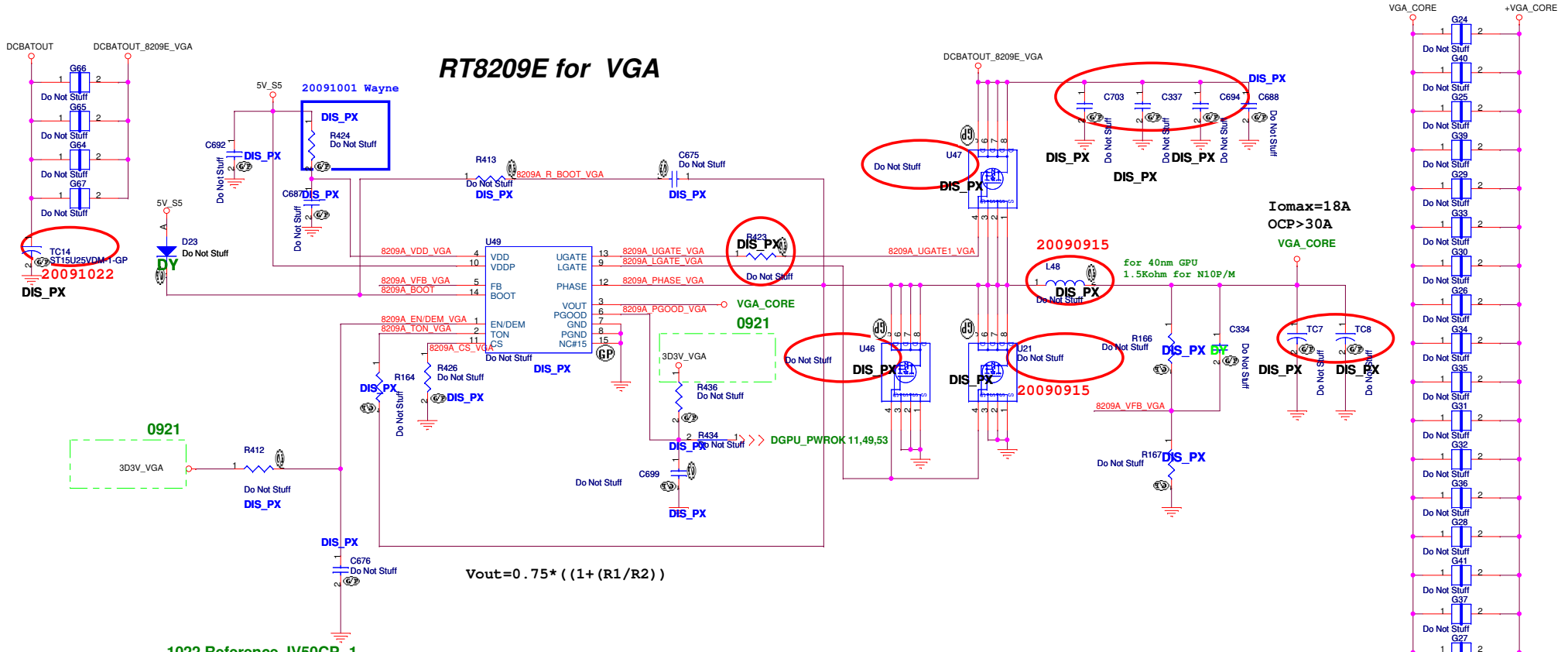
RT8209E for VGA



	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V

	R432
MADSION PRO	15KR2F 64.15025.6DL
PARK XT	6R81K 64.68115.6DL

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Title: RT8209E_VGA_CORE

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NB

RS780-->RS880M

71.RS780.M02-->71.RS880.M02

SB

SB820M-1-GP

71.SB820.00U-->71.SB820.M03

SATA_CALRP

A11: 80歐姆 1% resistor to GND

A12: TBD歐姆 1% resistor to GND

SATA_CALRN

A11:A11: 931歐姆1% resistor to VDDAN_11_SATA

A12: TBD歐姆 1% resistor to VDDAN_11_SATA.

VGA

Madison--> PN:71.MDSON.M01

Park--> PN:71.0PARK.M04

VRAM

Samsung-->VRAM FBRAM1~8 PN:VR.1GB0B.006

Hynix--> VRAM FBRAM1~8 PN:VR.1GB0G.004

CRT

UMA-->L1-->2R 0603

C62-->47U/6.3V

DIS-->L1-->Bead(L1 68.00217.711 L1608-UH38 SBK160808T-221Y-N-GP)

C62-->DY

HDMI

R497 : DIS-->0R

UMA & PX-->5.1K (R497 63.51234.1DL R402H16 5K1R2J-4-GP)

R496 : DIS-->100K

UMA & PX-->10K(R496 63.10334.1DL R402H16 10KR2J-3-GP)

R432(MAD/PARK)

Madison-->V15KR2F 64.15025.6DL

Park-->R432 64.68115.6DL

BOM

1st -> Diserete Madison Hynix(S02G)

2nd -> UMA (S01G)

1st +3rd -> Diserete Park Hynix(S03G)

1st +3rd -> Diserete Park Samsung(S04G)

1st -> Diserete Madison Samsung (S05G)

PX=PARK+Hynix(1st +3rd)

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Title: NOTE

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