

Discrete/UMA Schematics Document

Sandy Bridge

Intel PCH

2011-01-04

REV : A00

DY :None Installed

UMA:UMA ONLY installed

DN15: ONLY FOR DN15 installed.

DQ15:ONLY FOR DQ15 installed.

PSL: KBC795 PSL circuit for 10mW solution installed.

10mW: External circuit for 10mW solution installed.

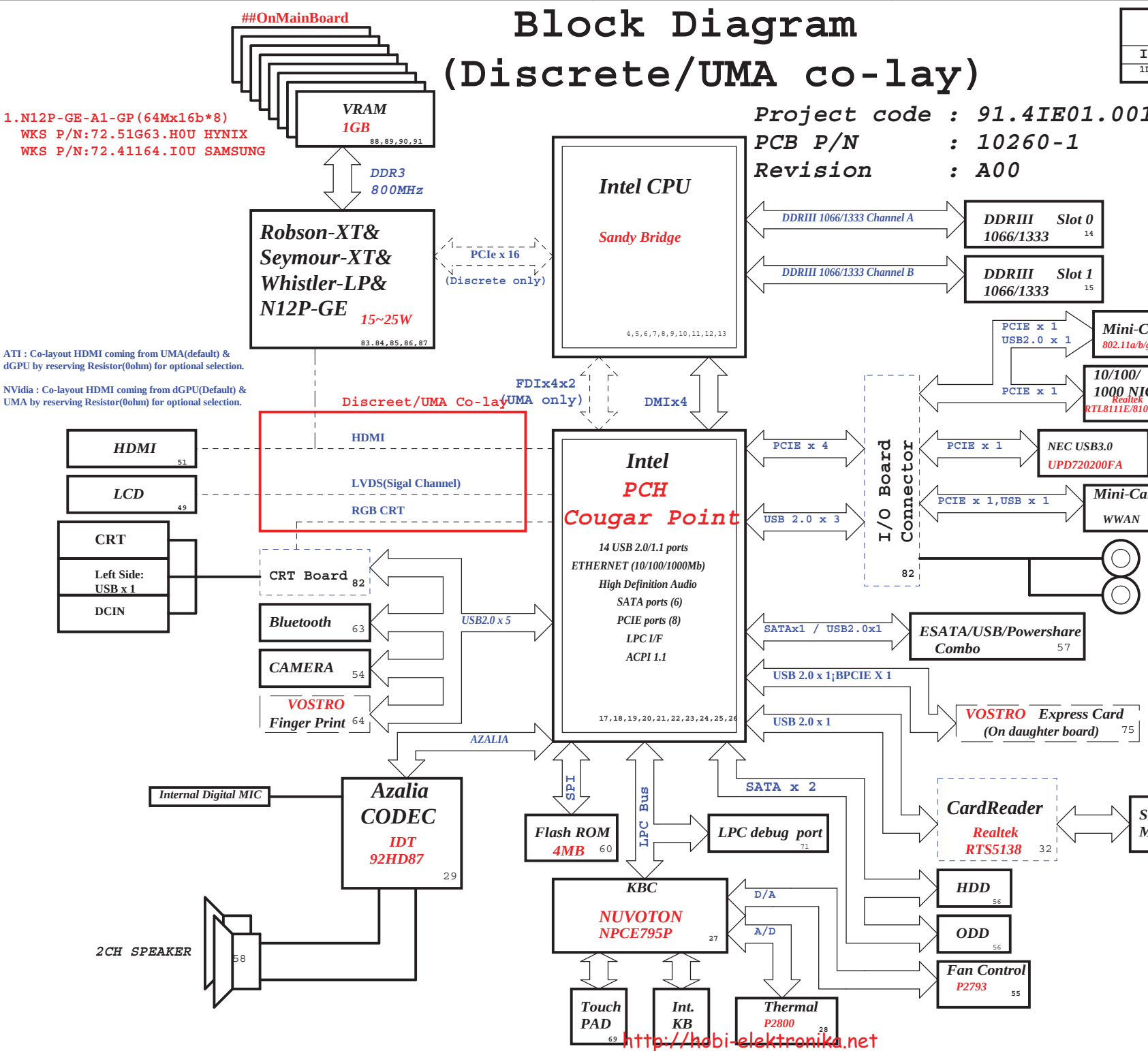
MUXLESS:MUXLESS solution installed.

OPTIMUS:OPTIMUS solution installed.



Block Diagram (Discrete/UMA co-lay)

SYSTEM LDO APL5916 48		CPU DC/DC ISL95831HRTZ 42~43	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D05V_VTT	0D85V_S0	DCBATOUT	VCC_CORE
SYSTEM DC/DC TPS51218 45		SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT	DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5
SYSTEM DC/DC TPS51216RUKR 46		SYSTEM DC/DC ISL95831HRTZ 44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3	DCBATOUT	VCC GFXCORE
VGA RT8208B 92		TI CHARGER BQ24745 40	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	VGA_CORE	+DC_IN_S5 +PBATT	DCBATOUT
SYSTEM DC/DC TPS51311 47		SYSTEM DC/DC G9731 93	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1D8V_S0	1D5V_S3	1V_VGA_S0
SYSTEM DC/DC G9731 93		Switches	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0	1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0
PCB LAYER		PCB LAYER	
L1:Top	L4:Signal	L1:Top	L4:Signal
L2:VCC	L5:GND	L2:VCC	L5:GND
L3:Signal	L6:Bottom	L3:Signal	L6:Bottom



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Block Diagram

Size A3 Document Number **QUEEN 15** Rev **A00**

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A B C D E
PCH Strapping Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kf[- 10-kf[weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

PCIE Routing

LANE1	Card Reader
LANE2	Mini Card1(WLAN)
LANE3	Mini Card2(WWAN)
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	Express Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	Express Card

Processor Strapping Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. 1: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	

POWER PLANE	VOLTAGE	Voltage Rails	DESCRIPTION
		ACTIVE IN	
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_OFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	HURON RIVER ORB
Device	Address	Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

Variant Name>



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SSID = CPU

Note:
Intel DMI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Intel FDI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Lane reversal does not apply to
FDI sideband signals.

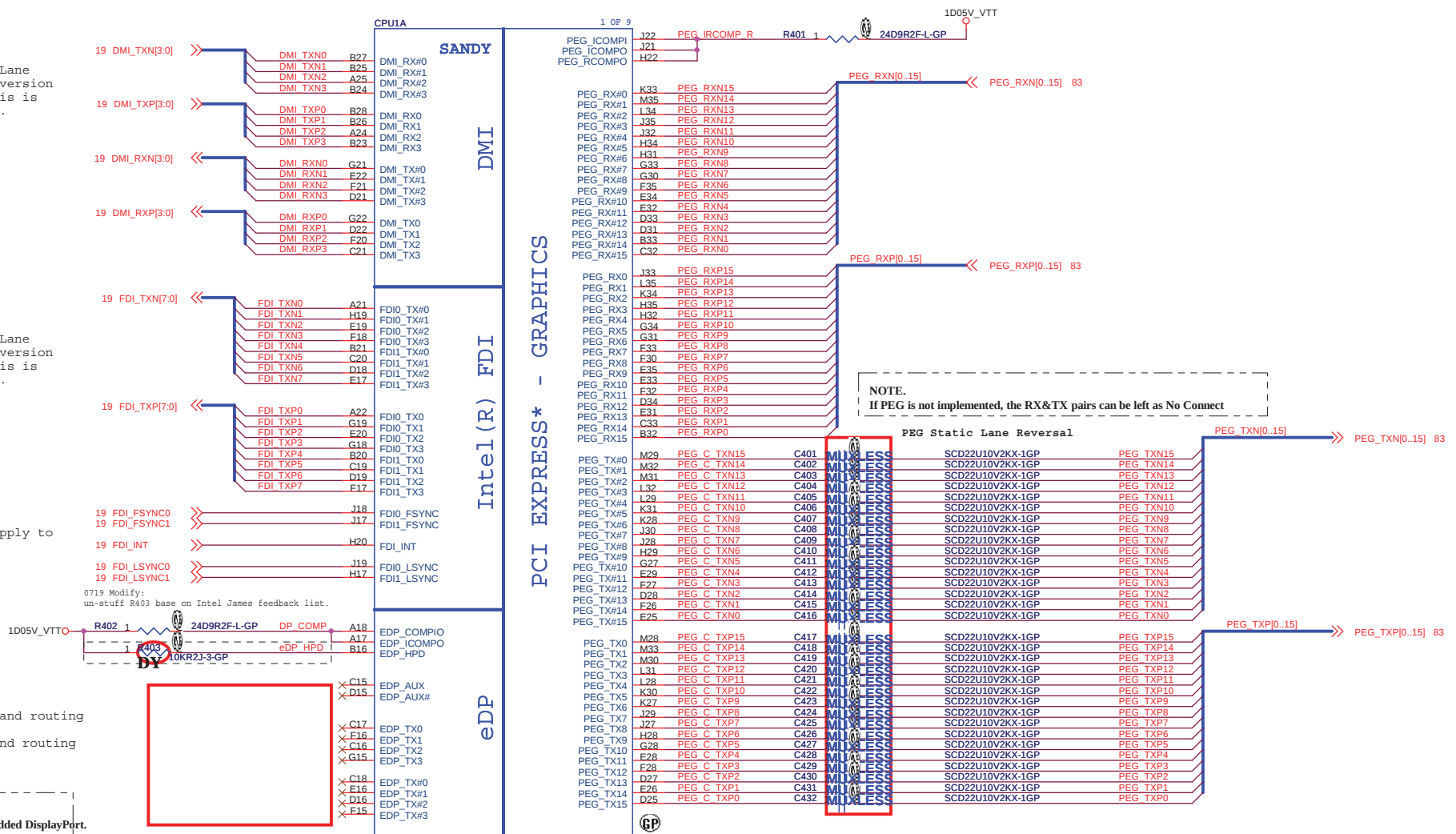
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing
length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing
length less than 500 mils.

NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics
function for power saving.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/
fall time is less than 6 ns. If HPD on eDP interface is
disabled, connect it to CPU VCCIO via a 10-k Ω pull-Up
resistor on the motherboard.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



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Variant Name

DELL

CPU (PCIe/DMI/FDI)

QUEEN 15

Document Number

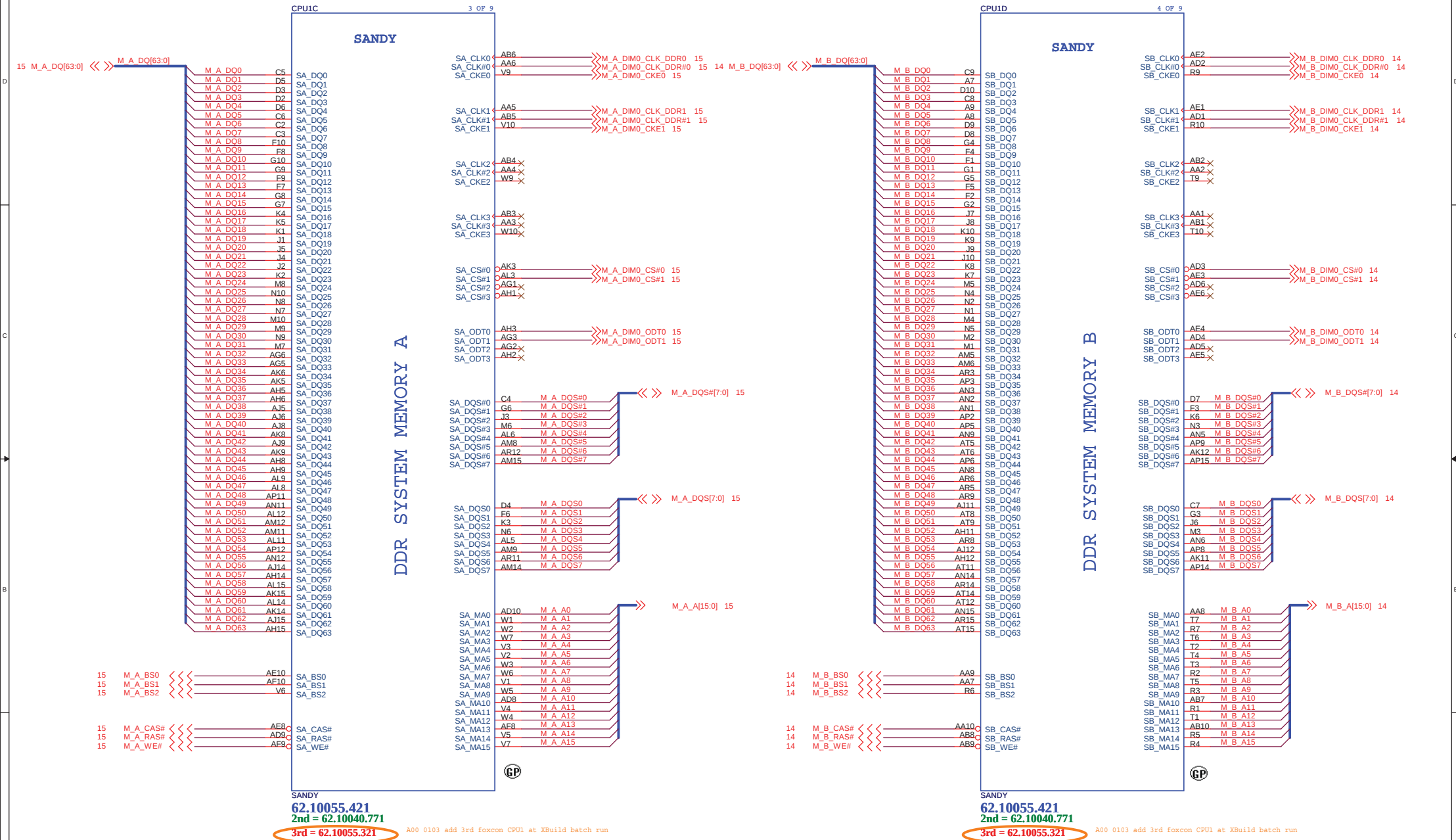
Rev

A00

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SSID = CPU



<Variant Name>

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Title CPU (DDR)					
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SSID = CPU

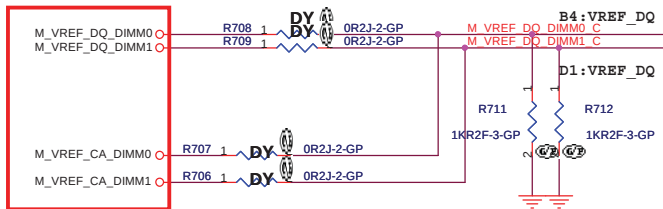
0630 Modify:
Reserved TP715 on CFG0.

TPAD14-GP TP715

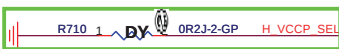
0707 Modify:
Removed CFG1,CFG3,CFG8-17 TP.

0617 Modify:
Joseph Change M_VREF_DQ_DIMM0,M_VREF_DQ_DIMM1,
M_VREF_CA_DIMM0,M_VREF_CA_DIMM1
from net to power.

M3 - Processor Generated SO-DIMM VREF_DQ



0629 Modify:
Reserved R710 0ohm to GND to
follow EV board schematic.



1D05V_VTT



0719 Modify:
Reserved EC701 0.1uF near
R711(BOTTOM) for EMC NEO suggestion.

CPU1E

5 OF 9

SANDY

RESERVED

SANDY SKT-BGA989C470395-1H180

62.10055.421

2nd = 62.10040.771

3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run

RSVD#L7
RSVD#AG7
RSVD#AE7
RSVD#AK2
RSVD#W8

RSVD#AT26
RSVD#AM33
RSVD#AJ27

RSVD#T8
RSVD#J16
RSVD#H16
RSVD#G16

RSVD#AR35
RSVD#AT34
RSVD#AT33
RSVD#AP35
RSVD#AR34

RSVD#B34
RSVD#A33
RSVD#A34
RSVD#B35
RSVD#C35

RSVD#AJ32
RSVD#AK32

RSVD#AH27

0702 Modify:
AN35 TP713
AM35 TP714

RSVD#AT2
RSVD#AT1
RSVD#AR1

GP

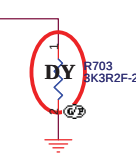
CFG2



PEG Static Lane Reversal

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

CFG4

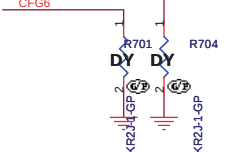


Display Port Presence Strap

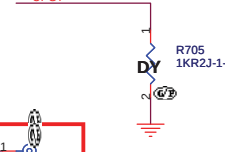
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG5

CFG6



CFG7



PCIe Port Bifurcation Straps

CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

PEG DEPER TRAINING

CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

0630 Modify:
Removed CLK_XDP ITP PnW
and reserved TP713,TP714.

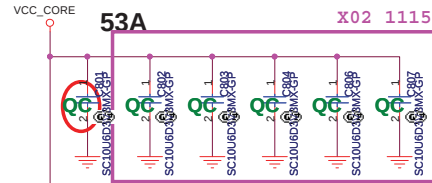
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DELL		Wistron Corporation	
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Title CPU (RESERVED)			
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Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

1115 X02 Modify:
Reserved C802-C804, C806, C807 10uF 0603
for power team fine tune Vcore quality.

PROCESSOR CORE POWER



0713 Modify:
Removed C802, C811 10uF 0603
cap base on layout limitation.

0713 Modify:
Removed C818 10uF 0603 cap
base on layout limitation.

0726 Modify:
un-stuff C826

0721 Modify:
Removed C836

0726 Modify:
un-stuff C837

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCC_CORE

AG35 VCC
AG34 VCC
AG33 VCC
AG32 VCC
AG31 VCC
AG30 VCC
AG29 VCC
AG28 VCC
AG27 VCC
AG26 VCC
AF35 VCC
AF34 VCC
AF33 VCC
AF32 VCC
AF31 VCC
AF30 VCC
AF29 VCC
AF28 VCC
AF27 VCC
AF26 VCC
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AC27 VCC
AC26 VCC
AA35 VCC
AA34 VCC
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AA32 VCC
AA31 VCC
AA30 VCC
AA29 VCC
AA28 VCC
AA27 VCC
AA26 VCC
V35 VCC
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V32 VCC
V31 VCC
V30 VCC
V29 VCC
V28 VCC
V27 VCC
V26 VCC
U35 VCC
U34 VCC
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U32 VCC
U31 VCC
U30 VCC
U29 VCC
U28 VCC
U27 VCC
U26 VCC
R35 VCC
R34 VCC
R33 VCC
R32 VCC
R31 VCC
R30 VCC
R29 VCC
R28 VCC
R27 VCC
R26 VCC
P35 VCC
P34 VCC
P33 VCC
P32 VCC
P31 VCC
P30 VCC
P29 VCC
P28 VCC
P27 VCC
P26 VCC

SANDY

62.100551421

2nd = 62.10040172

POWER

SANDY

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

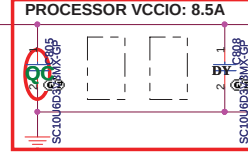
VCCIO AH13
VCCIO AH10
VCCIO AG10
VCCIO AG10
VCCIO Y10
VCCIO U10
VCCIO P10
VCCIO J10
VCCIO J14
VCCIO J12
VCCIO J11
VCCIO H14
VCCIO H12
VCCIO H11
VCCIO G14
VCCIO G13
VCCIO G12
VCCIO F14
VCCIO F13
VCCIO F12
VCCIO F11
VCCIO E14
VCCIO E12
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VCCIO D14
VCCIO D13
VCCIO D12
VCCIO D11
VCCIO C14
VCCIO C13
VCCIO C12
VCCIO C11
VCCIO B14
VCCIO B12
VCCIO A14
VCCIO A13
VCCIO A12
VCCIO A11
VCCIO J23

VIDALERT#
VIDSCCLK
VIDSOUT

VCC_SENSE
VSS_SENSE

VCCIO_SENSE
VSSIO_SENSE

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top



0713 Modify:
Removed C810, C806, C807 10uF 0603 cap
base on layout limitation.

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

0617 Modify:
Joseph Removed C812,
C813, C814

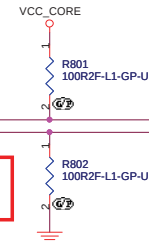
For CRB VIDSOUT need to pull high 130 ohm closer to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

H_CPU_SVIDDAT R804 130R2F-1-GP

20100610 V1.0

0705 Modify:
Removed R805, R806, already PH closed PWM side.

AJ29 H_CPU_SVIDALRT# R803 43R2J-GP
AJ30 H_CPU_SVIDCLK VR_SVID_ALERT# 42
AJ28 H_CPU_SVIDDAT H_CPU_SVIDCLK 42
H_CPU_SVIDDAT 42



VCCSENSE 42
VSSSENSE 42

VCCIO_SENSE 45
VSSIO_SENSE 45

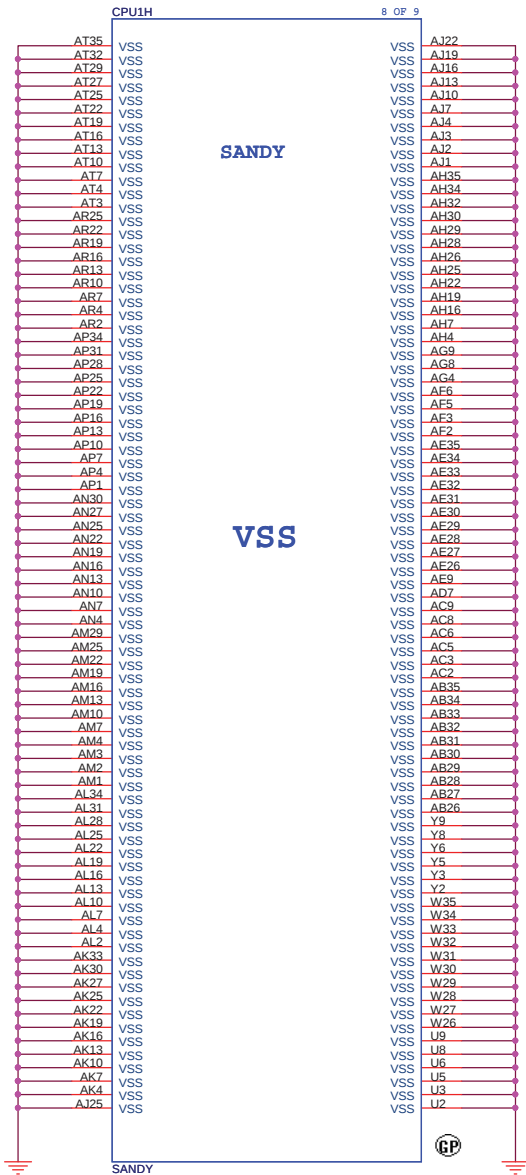
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Custn	QUEEN 15	A00
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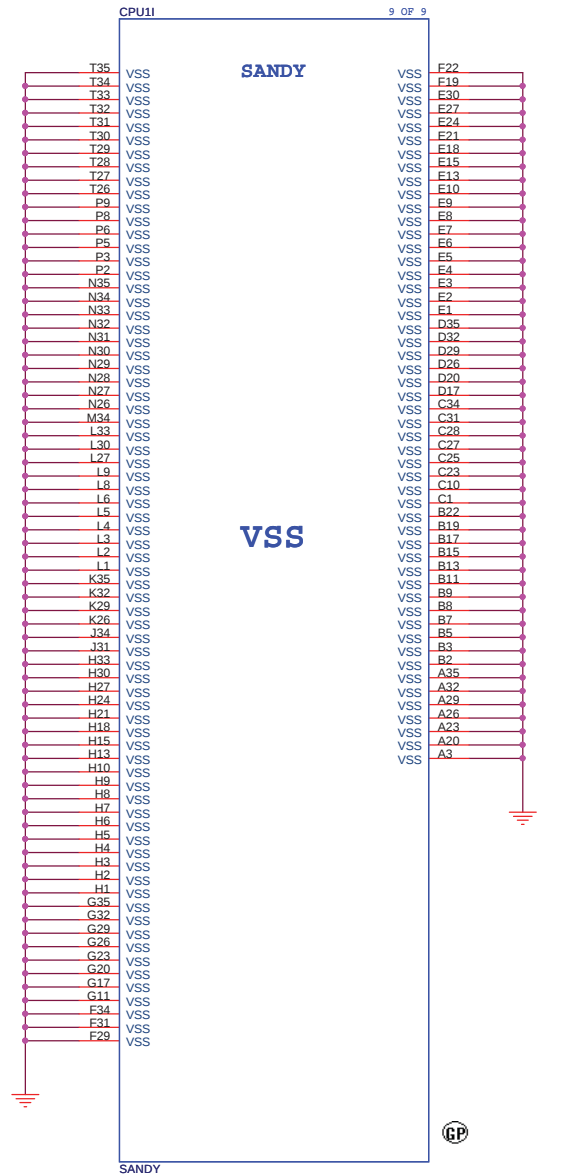


SANDY
62.10055.421

2nd = 62.10040.771

3rd = 63.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run



SANDY
62.10055.421

2nd = 62.10040.771

3rd = 62.10055.321

A00 0103 add 3rd foxconn CPU1 at XBuild batch run

<Variant Name>

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<Variant Name>



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Title

XDP

Size
A3

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Title

Reserved

Size
A3

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QUEEN 15

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<Core Design>



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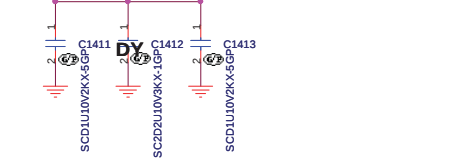
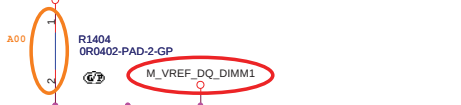
SSID = MEMORY

0624 Modify:
SWAP DM1 and DM2 location.

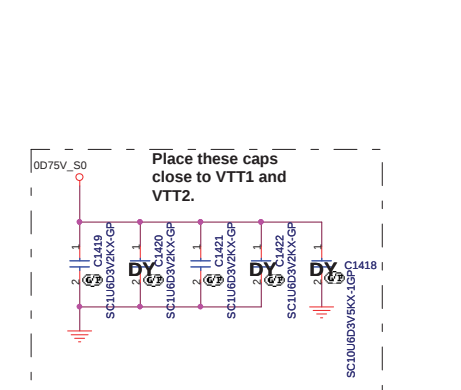
0617 Modify:
Joseph Change M_VREF_DQ_DIMM0, M_VREF_DQ_DIMM1,
M_VREF_CA_DIMM0, M_VREF_CA_DIMM1
from net to power.



0617 Modify:
Joseph Change M_VREF_DQ_DIMM0, M_VREF_DQ_DIMM1,
M_VREF_CA_DIMM0, M_VREF_CA_DIMM1
from net to power.



0707 Modify:
Change R1404, R1405 to 0ohm 0402 from short pad.



Place these caps
close to VTT1 and
VTT2.



0617 Modify:
Joseph Change M_VREF_DQ_DIMM0, M_VREF_DQ_DIMM1,
M_VREF_CA_DIMM0, M_VREF_CA_DIMM1
from net to power.



- M_B A0 98
- M_B A1 97
- M_B A2 96
- M_B A3 95
- M_B A4 92
- M_B A5 91
- M_B A6 86
- M_B A7 89
- M_B A8 89
- M_B A9 85
- M_B A10 107
- M_B A11 94
- M_B A12 83
- M_B A13 119
- M_B A14 80
- M_B A15 78
- A16/BA2 79

- M_B DQ0 109
- M_B DQ1 108
- M_B DQ2 5
- M_B DQ3 7
- M_B DQ4 15
- M_B DQ5 17
- M_B DQ6 4
- M_B DQ7 16
- M_B DQ8 12
- M_B DQ9 21
- M_B DQ10 23
- M_B DQ11 35
- M_B DQ12 22
- M_B DQ13 24
- M_B DQ14 34
- M_B DQ15 36
- M_B DQ16 39
- M_B DQ17 41
- M_B DQ18 51
- M_B DQ19 53
- M_B DQ20 40
- M_B DQ21 42
- M_B DQ22 50
- M_B DQ23 57
- M_B DQ24 57
- M_B DQ25 59
- M_B DQ26 67
- M_B DQ27 56
- M_B DQ28 68
- M_B DQ29 68
- M_B DQ30 68
- M_B DQ31 106
- M_B DQ32 106
- M_B DQ33 131
- M_B DQ34 141
- M_B DQ35 143
- M_B DQ36 130
- M_B DQ37 132
- M_B DQ38 140
- M_B DQ39 142
- M_B DQ40 147
- M_B DQ41 149
- M_B DQ42 157
- M_B DQ43 159
- M_B DQ44 148
- M_B DQ45 148
- M_B DQ46 158
- M_B DQ47 160
- M_B DQ48 163
- M_B DQ49 165
- M_B DQ50 175
- M_B DQ51 177
- M_B DQ52 164
- M_B DQ53 166
- M_B DQ54 174
- M_B DQ55 176
- M_B DQ56 181
- M_B DQ57 183
- M_B DQ58 191
- M_B DQ59 193
- M_B DQ60 180
- M_B DQ61 182
- M_B DQ62 182
- M_B DQ63 194

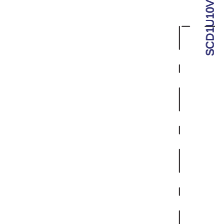
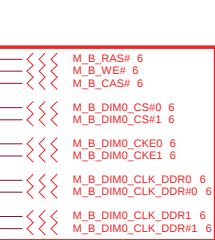
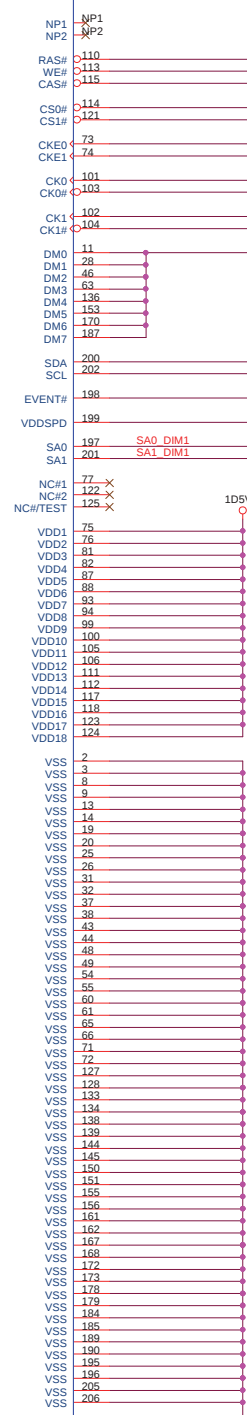
- M_B DQS#0 100
- M_B DQS#1 270
- M_B DQS#2 450
- M_B DQS#3 620
- M_B DQS#4 1350
- M_B DQS#5 1520
- M_B DQS#6 1690
- M_B DQS#7 1860
- M_B DQS0 12
- M_B DQS1 29
- M_B DQS2 47
- M_B DQS3 64
- M_B DQS4 137
- M_B DQS5 154
- M_B DQS6 171
- M_B DQS7 188

- M_B_DIM0_ODT0 116
- M_B_DIM0_ODT1 120
- M_VREF_CA_DIMM1O 126
- M_VREF_DQ_DIMM1O 1
- 15,37 DDR3_DRAMRST# 30

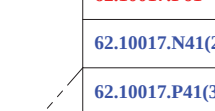


H =5.2mm
DDR3-204P-48-GP
62.10017.P61

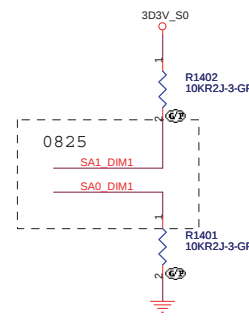
2nd = 62.10017.N41
3rd = 62.10017.P41
4th = 62.10024.E21



Layout Note:
Place these Caps near
SO-DIMMA.



1110 X02 Modify:
DM2 1st change to 62.10017.P61; 2nd change
to 62.10017.N41 on ST stage from ME updated
connector list.



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

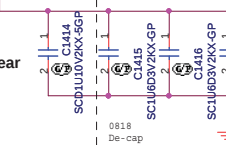
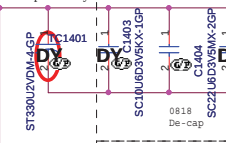
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT



SODIMM A DECOUPLING

0617 Modify:
Joseph dummy TC1401 default un-stuff.



PART NUMBER	Height	TYPE
62.10017.P61	5.2mm	REVERSED
62.10017.N41(2nd)	5.2mm	REVERSED
62.10017.P41(3rd)	5.2mm	REVERSED
62.10024.E21(4th)	5.2mm	REVERSED

<Variant Name>

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Title

DDR3-SODIMM2

Size Custom

Document Number

QUEEN 15

Date

Tuesday, January 04, 2011

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of

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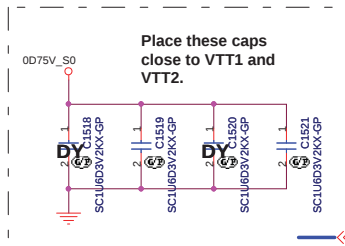
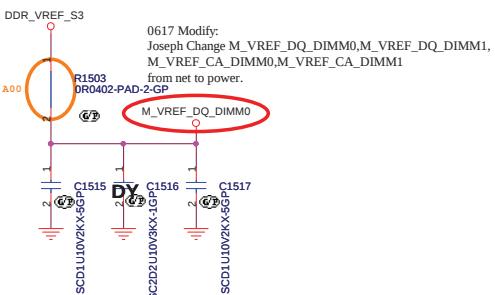
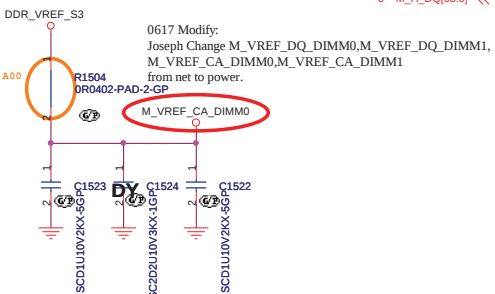
Rev

A00

SSID = MEMORY

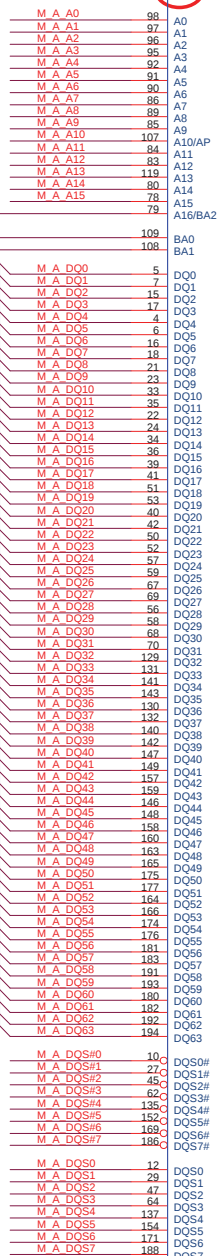


0707 Modify:
Change R1503,R1504 to 0ohm 0402 from short pad.

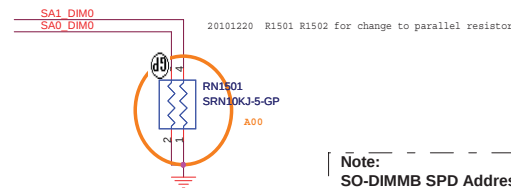
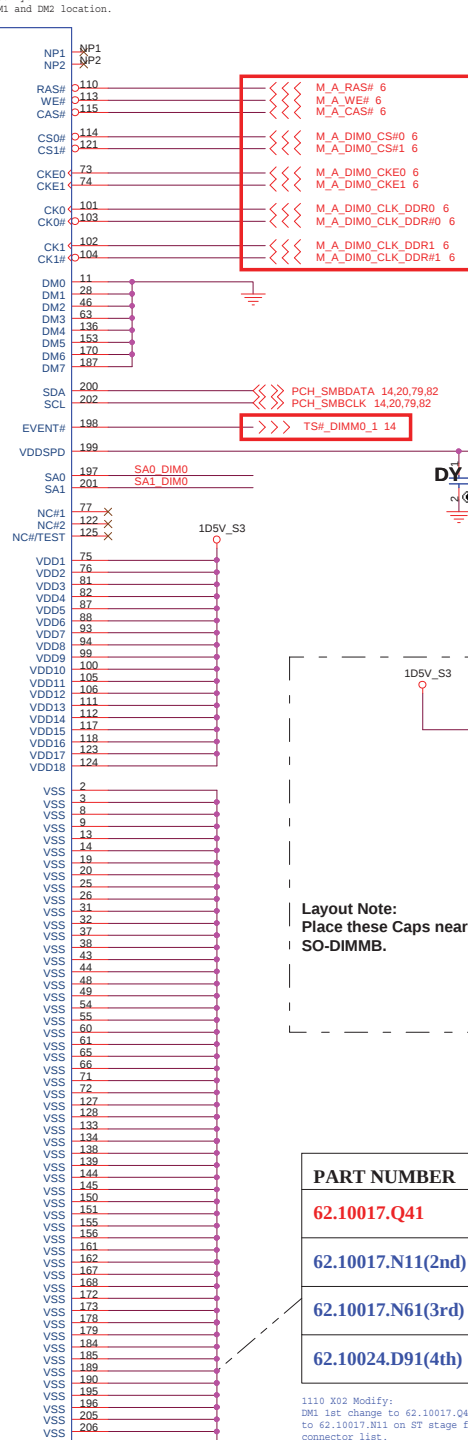


0617 Modify:
Joseph Change M_VREF_DQ_DIMM0,M_VREF_DQ_DIMM1,
M_VREF_CA_DIMM0,M_VREF_CA_DIMM1
from net to power.

H = 9.2mm

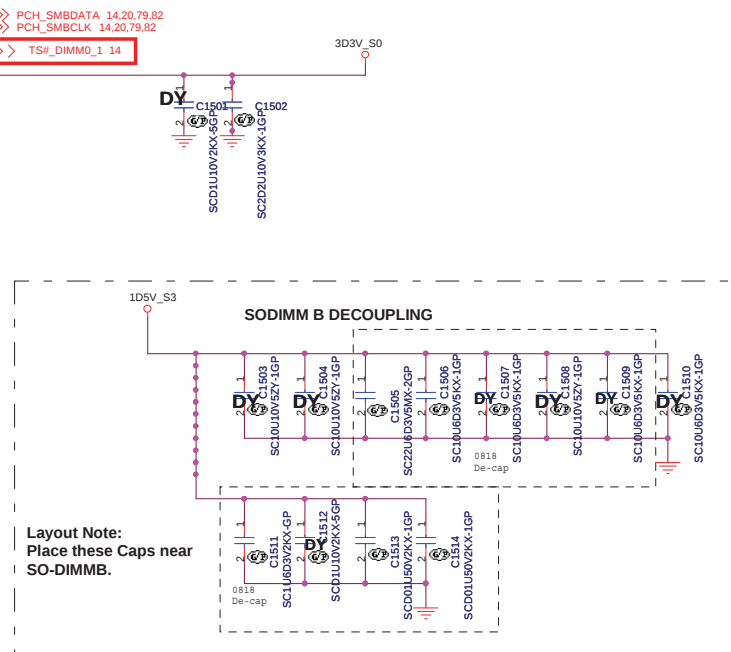


62.10017.Q41
2nd = 62.10017.N11
3rd = 62.10017.N61
4th = 62.10024.D91



Note:
SO-DIMMB SPD Address is 0xA
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



Layout Note:
Place these Caps near
SO-DIMMB.

PART NUMBER	Height	TYPE
62.10017.Q41	9.2mm	REVERSED
62.10017.N11(2nd)	9.2mm	REVERSED
62.10017.N61(3rd)	9.2mm	REVERSED
62.10024.D91(4th)	9.2mm	REVERSED

1110 X02 Modify:
DM1 1st change to 62.10017.Q41; 2nd change
to 62.10017.N11 on ST stage from ME updated
connector list.



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Title			
DDR3-SODIMM1			
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(Blanking)

<Core Design>



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Title

Reserved

Size
A3

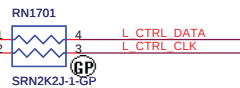
Document Number
QUEEN 15

Date: Tuesday, January 04, 2011

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3D3V_S0



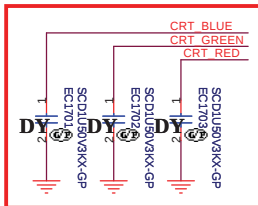
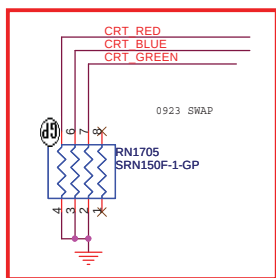
L_DDC_DATA(PAGE17):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is
used for the local flat panel display



Place near PCH

Impedance: 90 ohm

Close to PCH side



Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402

0917 X01 Modify:
Add R1703-R1705 on RGB signal and reserved
EC1701-EC1703 0.1u from EMC Neo suggestion.

82 CRT_BLUE N48
82 CRT_GREEN P49
82 CRT_RED T49

82 CRT_DDC_CLK
82 CRT_DDC_DATA

82 CRT_HSYNC
82 CRT_VSYNC

DAC_IREF_R
T43
T42

Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402

Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402

Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402

Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402

Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402

Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402

Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402

Notes:
1K 0.5% 0402.
CHIP RES 1K D 1/16W 0402

PCH1D

Cougar Point

L_BKLTEN

L_VDD_EN

L_BKLT_CTRL

LVDS DDC CLK R

LVDS DDC DATA R

L_CTRL_CLK

L_CTRL_DATA

LVDS_IBG

LVDS_VBG

LVDS_VREFH

LVDS_VREFL

LVDSA_CLK#

LVDSA_CLK

LVDSA_DATA#0

LVDSA_DATA#1

LVDSA_DATA#2

LVDSA_DATA#3

LVDSA_DATA0

LVDSA_DATA1

LVDSA_DATA2

LVDSA_DATA3

LVDSB_CLK#

LVDSB_CLK

LVDSB_DATA#0

LVDSB_DATA#1

LVDSB_DATA#2

LVDSB_DATA#3

LVDSB_DATA0

LVDSB_DATA1

LVDSB_DATA2

LVDSB_DATA3

CRT_BLUE

CRT_GREEN

CRT_RED

CRT_DDC_CLK

CRT_DDC_DATA

CRT_HSYNC

CRT_VSYNC

DAC_IREF_R

CRT_IRTN

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

COUGAR-GP-U2-NF

LVDS

Digital Display Interface

4 OF 10

SDVO_TVCLKINN

SDVO_TVCLKINP

SDVO_STALLN

SDVO_STALLP

SDVO_INTN

SDVO_INTN

SDVO_CTRLCLK

SDVO_CTRLDATA

DDPB_AUXN

DDPB_AUXP

DDPB_HPDP

DDPB_0N

DDPB_0P

DDPB_1N

DDPB_1P

DDPB_2N

DDPB_2P

DDPB_3N

DDPB_3P

DDPC_CTRLCLK

DDPC_CTRLDATA

DDPC_AUXN

DDPC_AUXP

DDPC_HPDP

DDPC_0N

DDPC_0P

DDPC_1N

DDPC_1P

DDPC_2N

DDPC_2P

DDPC_3N

DDPC_3P

DDPD_CTRLCLK

DDPD_CTRLDATA

DDPD_AUXN

DDPD_AUXP

DDPD_HPDP

DDPD_0N

DDPD_0P

DDPD_1N

DDPD_1P

DDPD_2N

DDPD_2P

DDPD_3N

DDPD_3P

DDPD_0N

DDPD_0P

DDPD_1N

DDPD_1P

DDPD_2N

DDPD_2P

DDPD_3N

DDPD_3P

DDPD_0N

DDPD_0P

DDPD_1N

DDPD_1P

DDPD_2N

DDPD_2P

DDPD_3N

DDPD_3P

DDPD_0N

DDPD_0P

DDPD_1N

DDPD_1P

DDPD_2N

DDPD_2P

DDPD_3N

DDPD_3P

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIIB_CTRLDATA
	DDPB_HPDP	NA	DDPB_HPDP	HDMIIB_HPDP
	DDPB_0N	NA	DDPB_0N	NA
	DDPB_0P	NA	DDPB_0P	NA
	DDPB_1N	NA	DDPB_1N	NA
	DDPB_1P	NA	DDPB_1P	NA
	DDPB_2N	NA	DDPB_2N	NA
	DDPB_2P	NA	DDPB_2P	NA
	DDPB_3N	NA	DDPB_3N	NA
	DDPB_3P	NA	DDPB_3P	NA

<Variant Name>

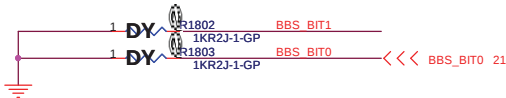
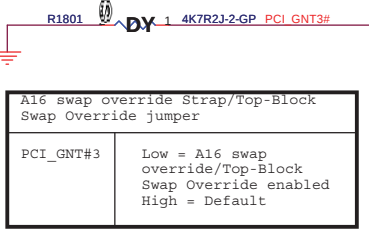
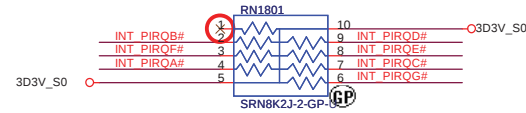


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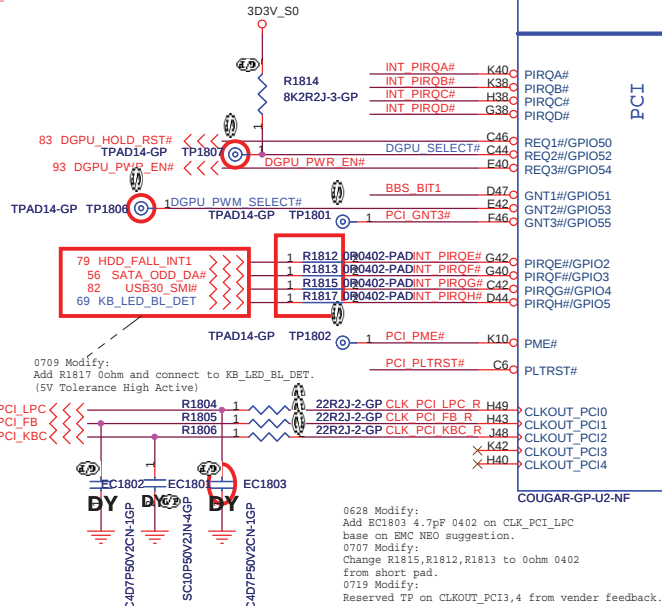
Title	PCH (LVDS/CRT/DDI)		
Size A3	Document Number	QUEEN 15	Rev A00
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SSID = PCH

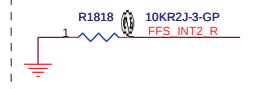
0709 Modify:
Removed INT_PIRQH# on RN1801 pin1.



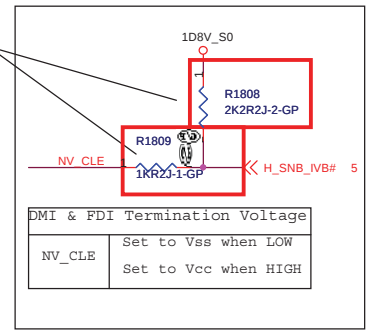
BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



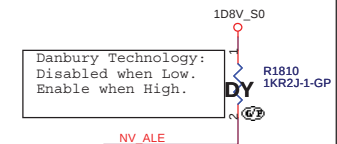
0908 X01 Modify:
Add R1818 10K PL on FFS INT2 R (GPIO14)



0719 Modify:
DP_TVS (NV_CLE) connect PROC_SELECT# (H_SNB_IVB#) with R1808 2.2K(05% pull up resistor to PCH VCCPND rail and a R1809 1K(05% series resistor base on Intel feedback.



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGE
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	Express Card

1120 X02 Modify:
Reserved USB_OC#0_1 connect from PCH GPIO59.

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used



Title		PCH (PCI/USB/NVRAM)	
Size A3	Document Number	Rev	A00
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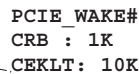
4 DMI_RXN[3:0]   

4 DMI_RXP[3:0]   

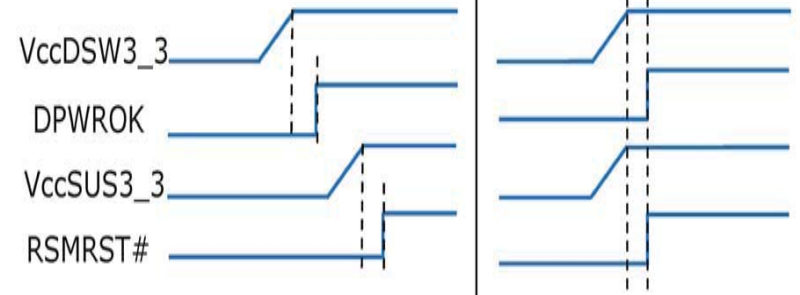
4 DMI_TXN[3:0]   

4 DMI_TXP[3:0]   

4	DMI_RXN0	>>>	_____
4	DMI_RXN1	>>>	_____
4	DMI_RXN2	>>>	_____
4	DMI_RXN3	>>>	_____
4	DMI_RXP0	>>>	_____
4	DMI_RXP1	>>>	_____
4	DMI_RXP2	>>>	_____
4	DMI_RXP3	>>>	_____
4	DMI_TXN0	<<<	_____
4	DMI_TXN1	<<<	_____
4	DMI_TXN2	<<<	_____
4	DMI_TXN3	<<<	_____
4	DMI_TXP0	<<<	_____
4	DMI_TXP1	<<<	_____
4	DMI_TXP2	<<<	_____
4	DMI_TXP3	<<<	_____



0621 Modify:
Joseph removed Q1901/R1909/R1916 3V_5V_POK
and PM_RSMRST# related control circuit.

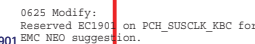


For platforms not supporting Deep S4/S5

- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP_SUS# and SUSACK# are left as ¡no connect;¡
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

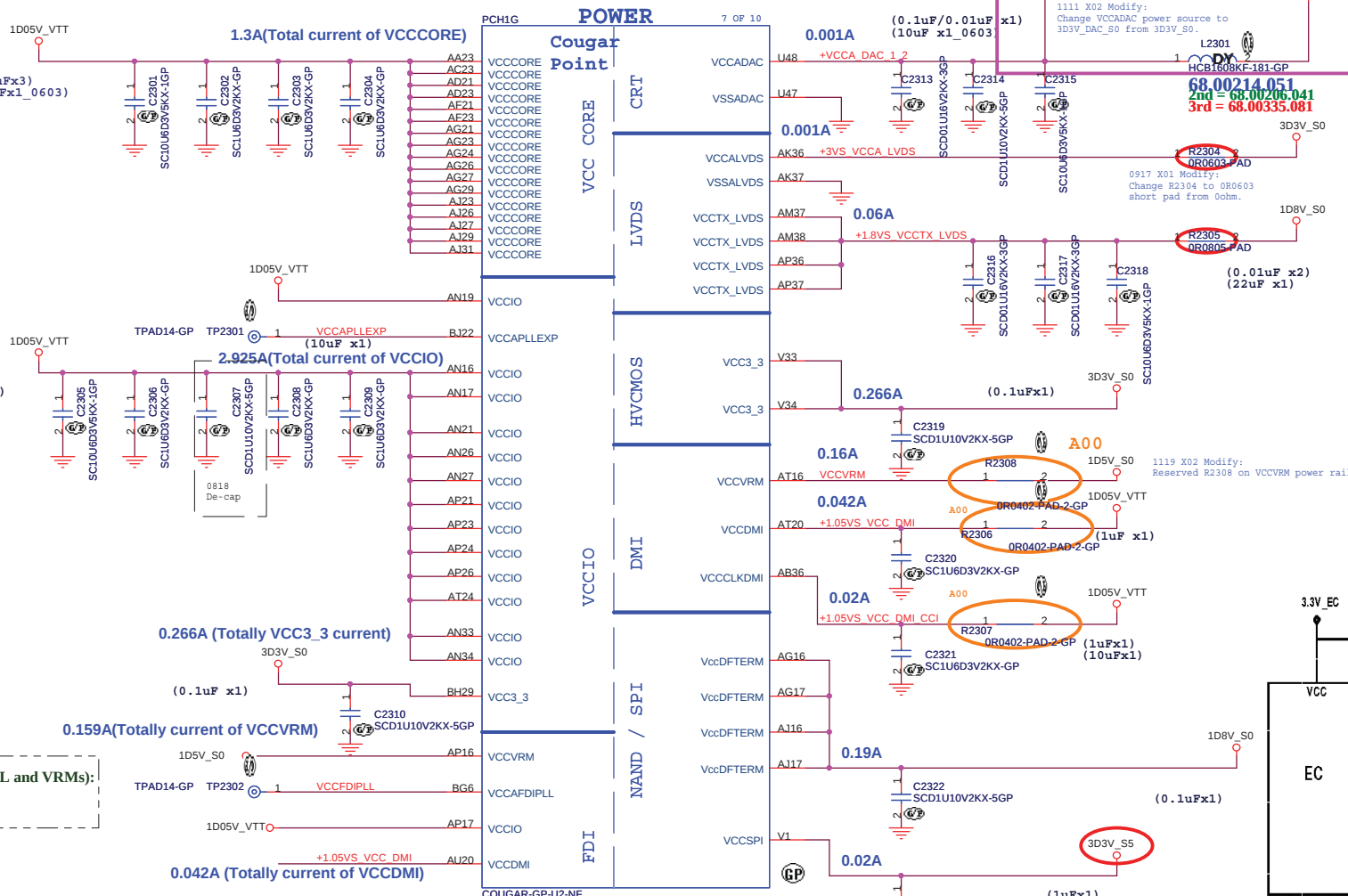
The diagram shows a red line labeled **DSWODVREN** connected to pin **R1918** of a relay labeled **330KR2J-1-LP**. The relay is marked with a large **DY**. Pin **R1917** of the relay is connected to pin **RTC_AUX_S5** of the RTC. The other side of the relay is connected to ground.





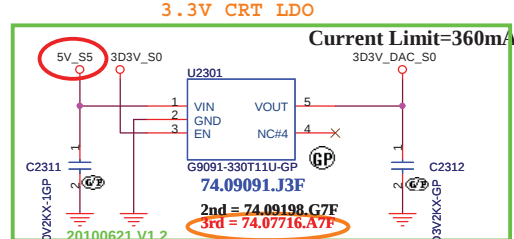
<http://hobi-elektronika.net>

SSID = PCH 6A



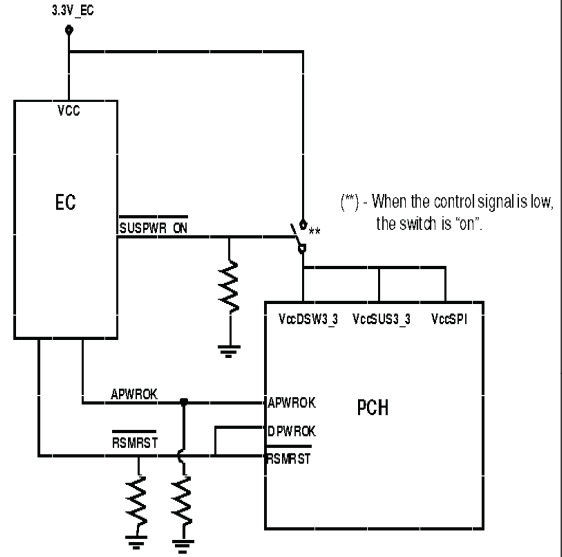
VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop

1122 X02 Modify:
Removed U2302 LDO for VCCVRM.



Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLb	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture



<Variant Name>

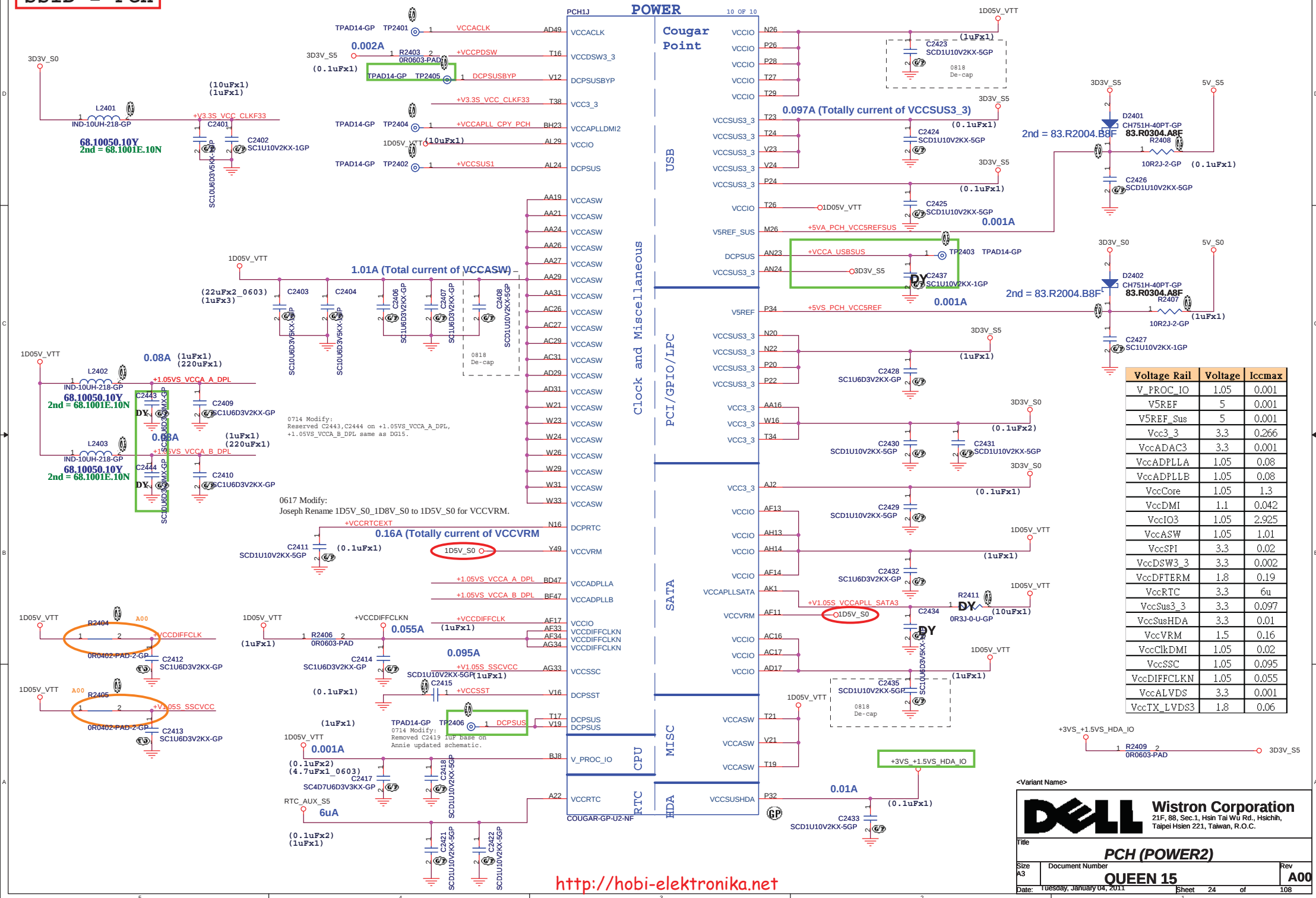
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Taipei Hsien 221, Taiwan, R.O.C.

Title **PCH (POWER1)**

Size A3 Document Number **QUEEN 15** Rev **A00**

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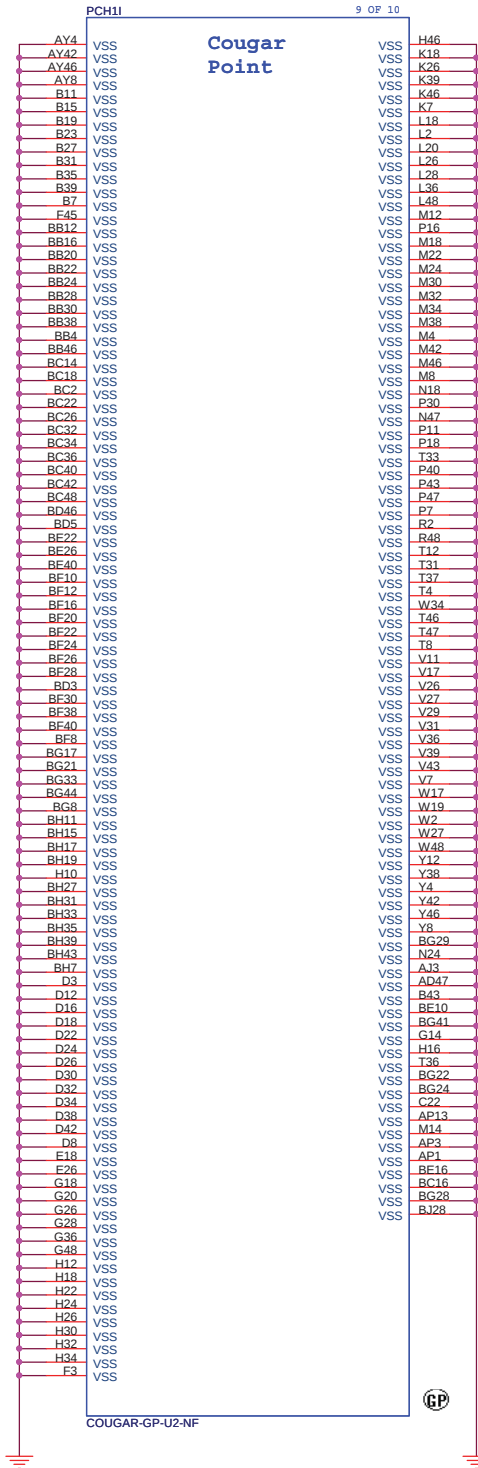
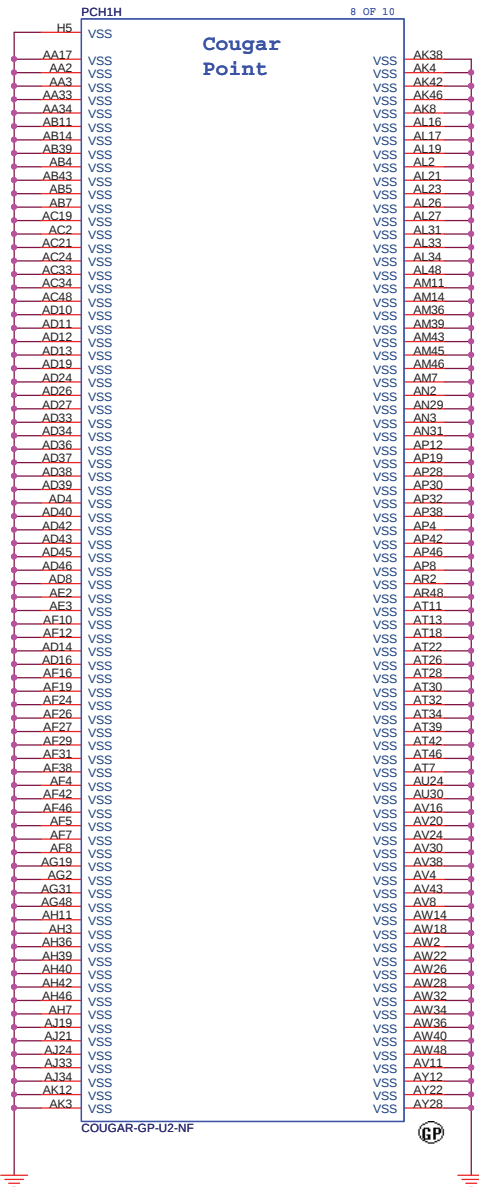
SSID = PCH



Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

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Title			
PCH (POWER2)			
Size A3	Document Number	QUEEN 15	Rev A00
Date:	Tuesday, January 04, 2011	Sheet 24 of	108

SSID = PCH



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<Variant Name>

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Title

PCH (VSS)

Size A3 Document Number **QUEEN 15** Rev **A00**

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<Variant Name>



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Title

Reserved

Size
A3

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QUEEN 15

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Rev
A00

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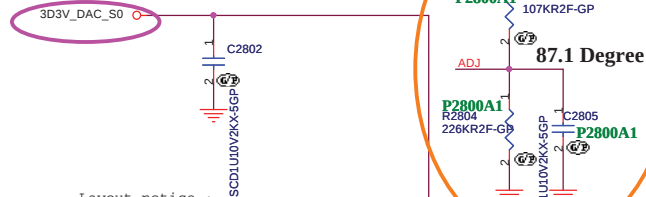
SSID = Thermal

Thermal sensor P2800

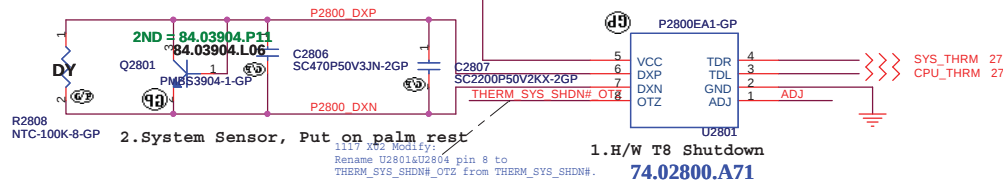
0705 Modify:
R2802 change to 0ohm 0402 from short pad and default un-stuff.

Fan controller P2793

1119 X02 Modify:
Change U2801,U2804,U2805 VCC power to 3D3V_DAC_S0 from 3D3V_S0.



Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.



ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

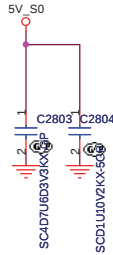
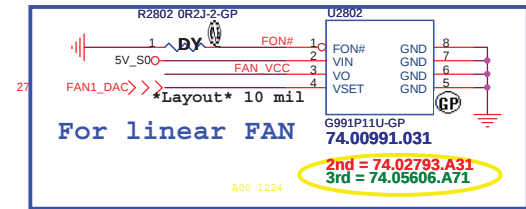
A00 1228 Cancel VGA Thermal sensor P2800 circuit

	Pin-1	Definition
P2793A	/FON	Low(<0.4V): VOUT =Vin and the fan is fully-on High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm
P2793B	EN	Low (<0.4): IC is shutdown. High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm

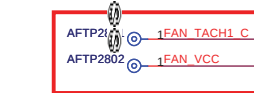
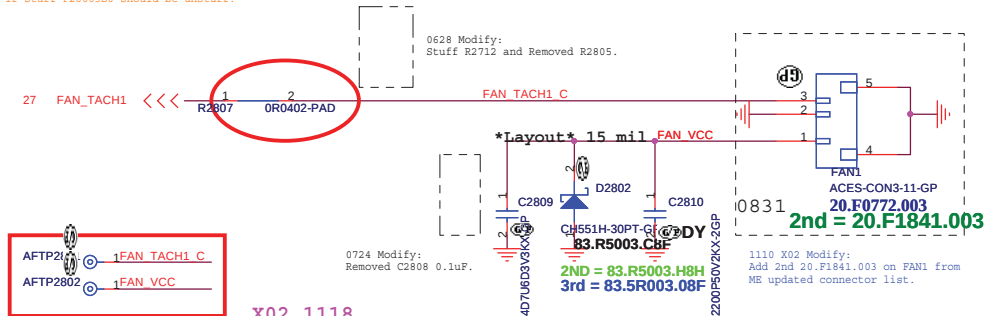
A00 1227

1111 X02 Modify:
ADJ&ADJ_VGA power source change to 3D3V_DAC_S0
from 3D3V_S0 to solve T8 shut down issue.

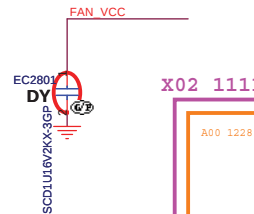
1227 A00 Modify:
If stuff P2800E21 then must stuff R2803,R2804,C2805 but if stuff P2800E30 should be unstuff.



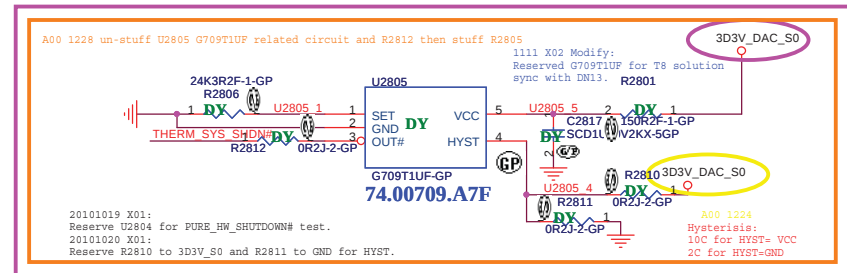
0614 Modify:
Change FAN1 connector part number to 20.D0210.103 base on ME EMN and DXF.
0712 Modify:
Change FAN1 part number to 20.F1639.004
from 20.D0210.103 base on latest EMN and DXF.



EMI/ESD



X02 1111



1111 X02 Modify:
ADJ&ADJ_VGA power source change to 3D3V_DAC_S0
from 3D3V_S0 to solve T8 shut down issue.

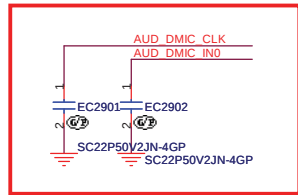
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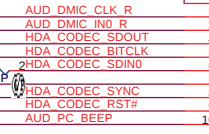
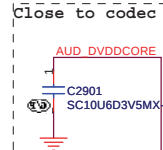
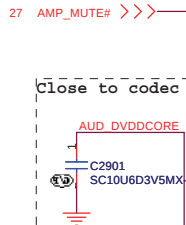
Title	Thermal P2800/Fan Controller P2793	Rev	A00
Size	Document Number	Rev	A00
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SSID = AUDIO

For EMI



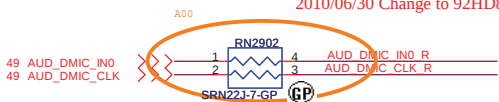
1122 X02 Modify:
change R2920, R2921 to 22ohm from 0ohm and
stuff EC2901, EC2902 22p from EMC Neo updated.



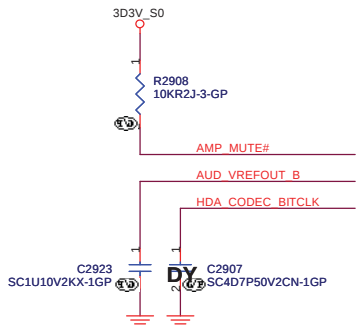
0707 Modify:
updated U2901 part number from data base.

92HD87B1A5NDGXTB8-GP

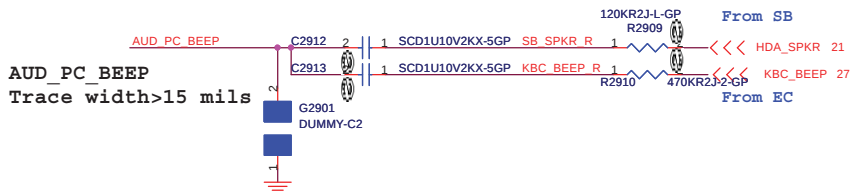
2010/06/30 Change to 92HD87 (71.92H87.A03)



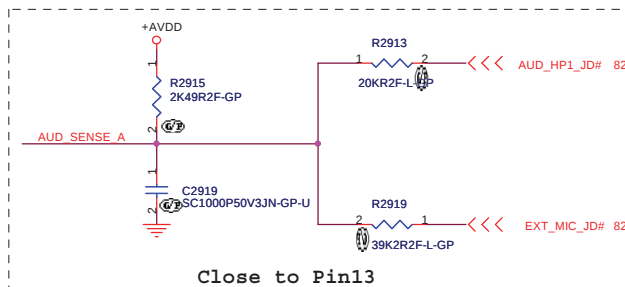
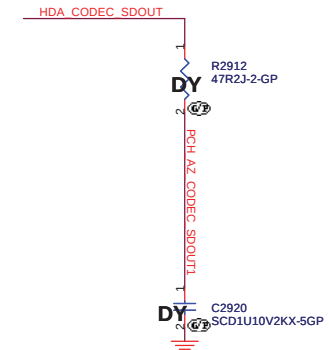
20101220 R2920 R2921 for change to parallel resistor



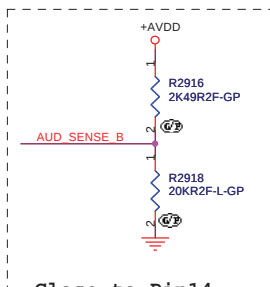
AUD_PC_BEEP
Trace width>15 mils



Azalia I/F EMI

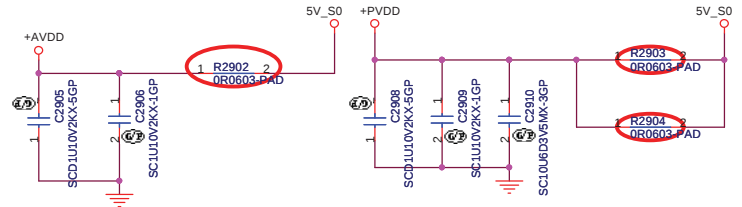


Close to Pin13

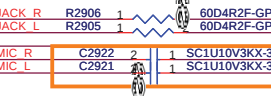


Close to Pin14

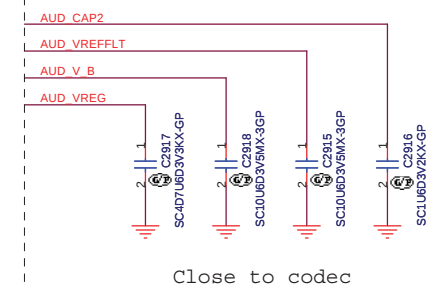
<http://hobi-elektronika.net>



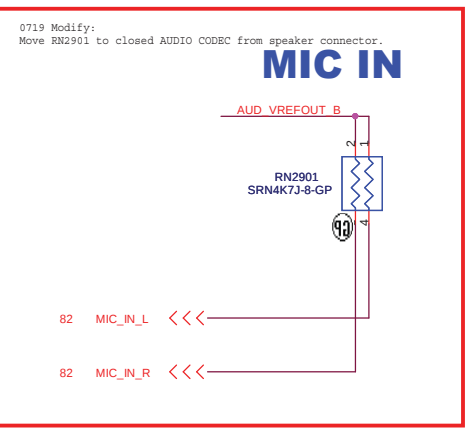
0707 Modify:
Change R2911, R2914, R2917 change
to 0ohm 0603 from short pad.
0726 Modify:
Removed all of AUD_AGND and R2911, R2914, R2917.



Put C2921 and C2922 close to codec



Close to codec



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<Core Design>



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Title

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<Core Design>



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Title

Reserved

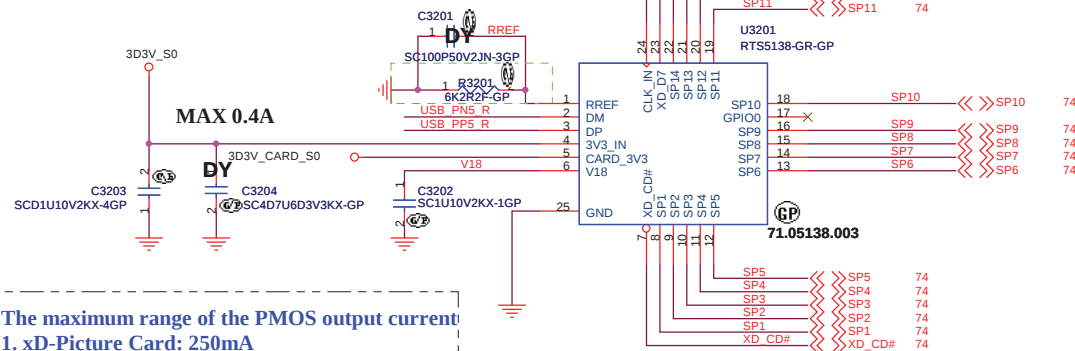
Size	Document Number	Rev
A3	QUEEN 15	A00

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SSID = SDIO

48MHz clock input trace of characteristic impedance (Z_0) must be 50 Ω $\pm$ 15%.

PCH GPIO67(48M) confirm with SW

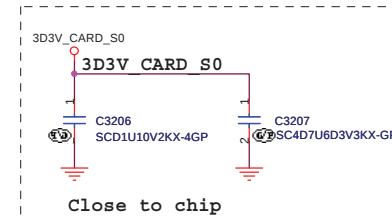


The maximum range of the PMOS output current

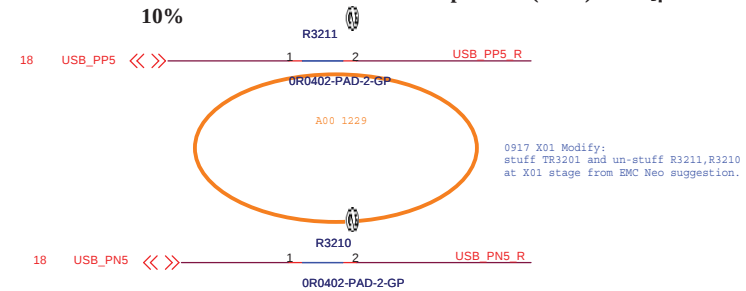
1. xD-Picture Card: 250mA
2. SD/MMC Card: 250mA
3. MS/MSPRO/Duo-HG: 250mA

POWER TRACE

1. RTS5138: pin 4 (3V3_IN) trace fixed width is 30 mils (minimum).
2. RTS5138: pin 5 (CARD_3V3) trace fixed width is 30 mils (minimum).
3. RTS5138: pin 6 (V18) trace fixed width is 12 mils (minimum). Keep the trace routing lengths as short as possible.
4. RTS5138: pin 1(RREF) trace fixed width is 12 mils (minimum).
5. RTS5138: pin 1(RREF) trace must far away 48MHz clock trace.
6. De-coupling and Bulk capacitor should place near to RT5138 chip and Combo Socket.
7. It is recommended that use of ferrites bead on power trace.
8. Via size: Pad>=32 mils, Finished hole>=16 mils.



The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance (Z_{diff}) is 90 Ω $\pm$ 10%



<Core Design>

DELL		Wistron Corporation	
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Title: Card Reader-RTS5138			
Size: A3	Document Number: QUEEN 15	Rev: A00	
Date: Tuesday, January 04, 2011	Sheet: 32	of: 108	

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

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<Core Design>



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Title

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<Core Design>



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Title

Reserved

Size
A3

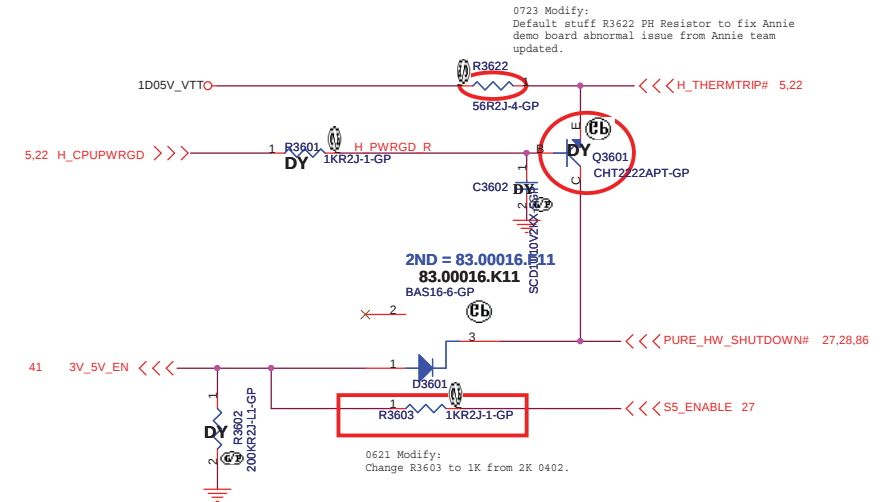
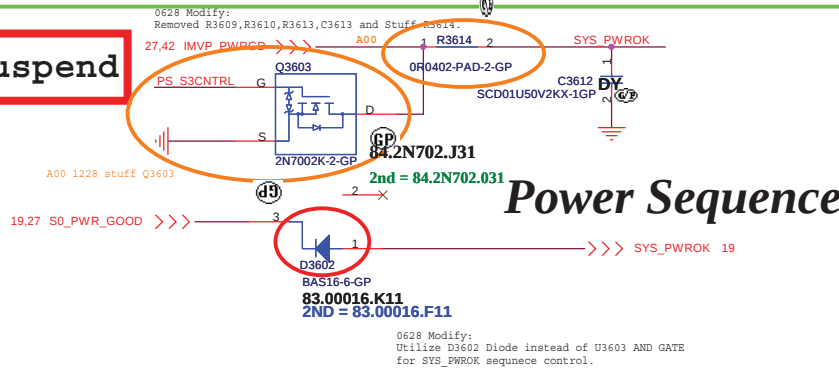
Document Number
QUEEN 15

Rev
A00

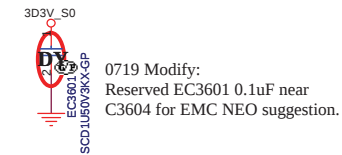
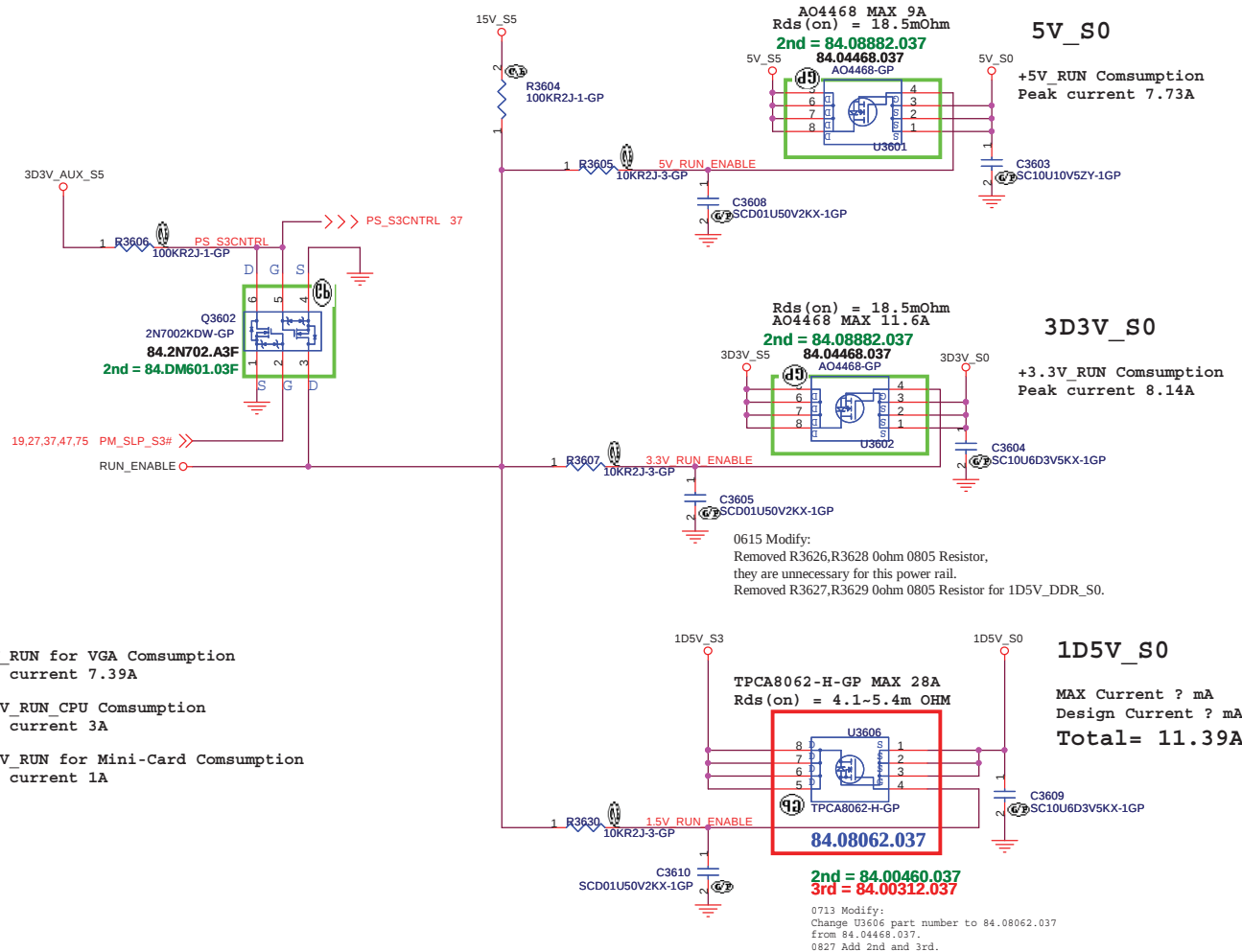
Date: Tuesday, January 04, 2011

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SSID = Reset.Suspend

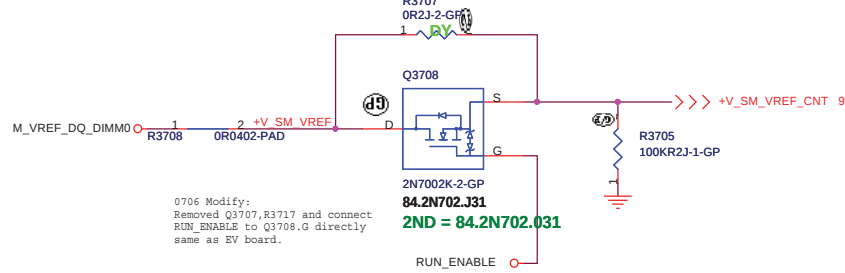


ROSA Run Power



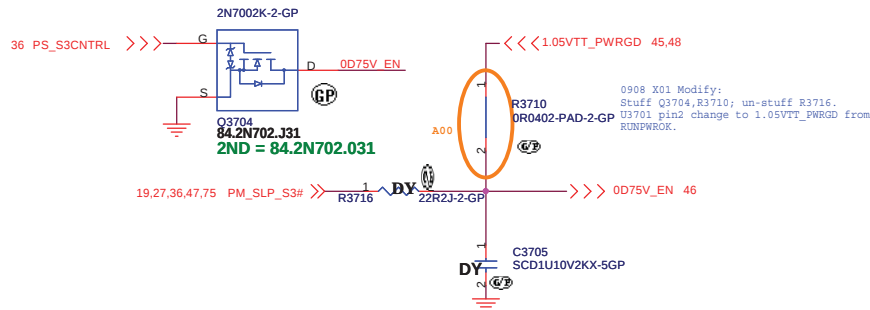
DELL			
Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title Power Plane Enable			
Size A3	Document Number	Rev A00	
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**Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation**



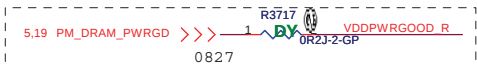
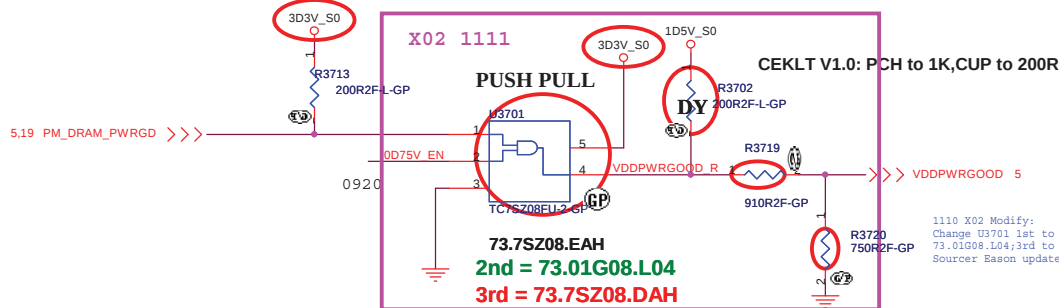
5 S3 Power Reduction X01 20091111

0730



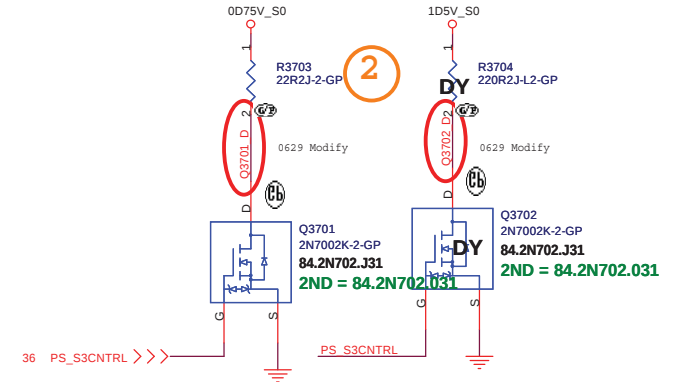
0709 Modify:
Change U3701 pin1,5 to 3D3V_S0 from 3D3V_S5.

**Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK**

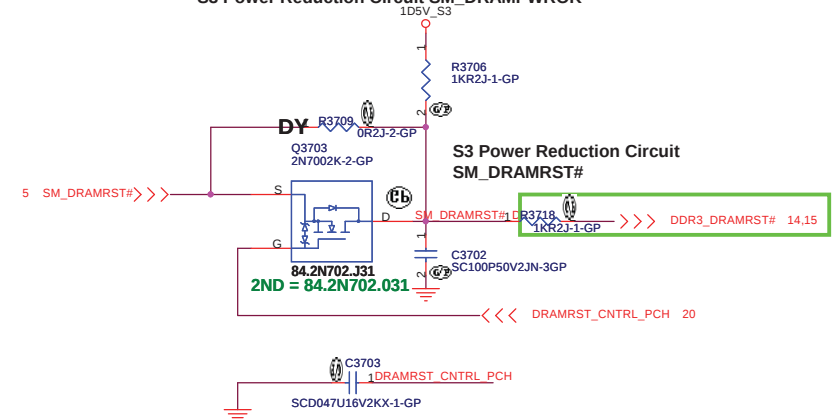


SM DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55; 200mV and the edge must be monotonic

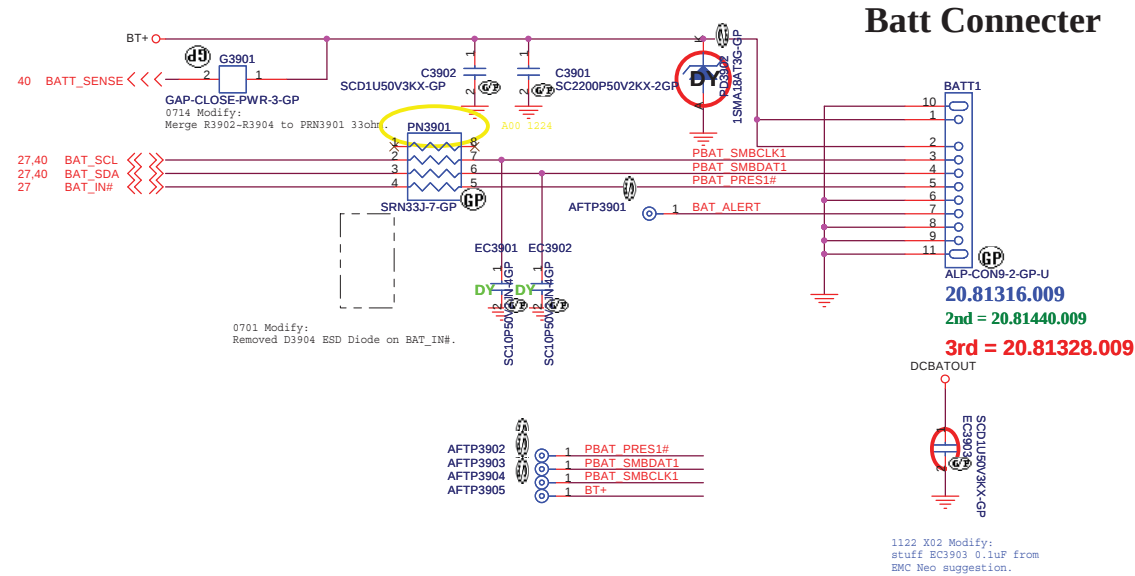
**Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK**



**Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK**

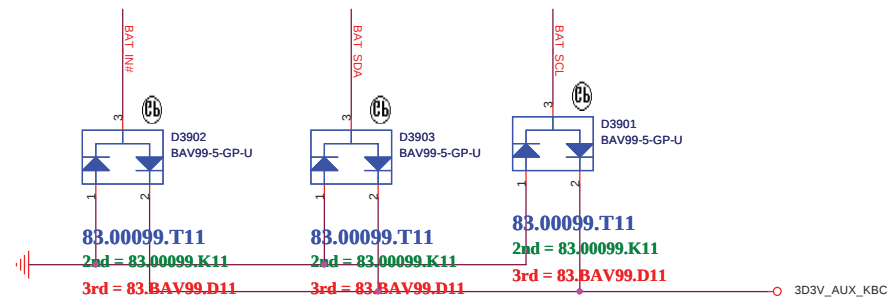


DN15ATI



For actual location, need to be swap all pin

Close to Batt Connector



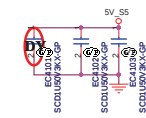
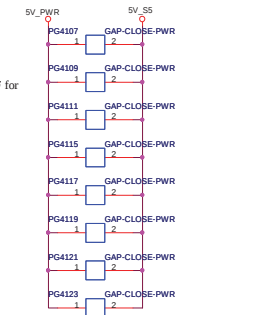
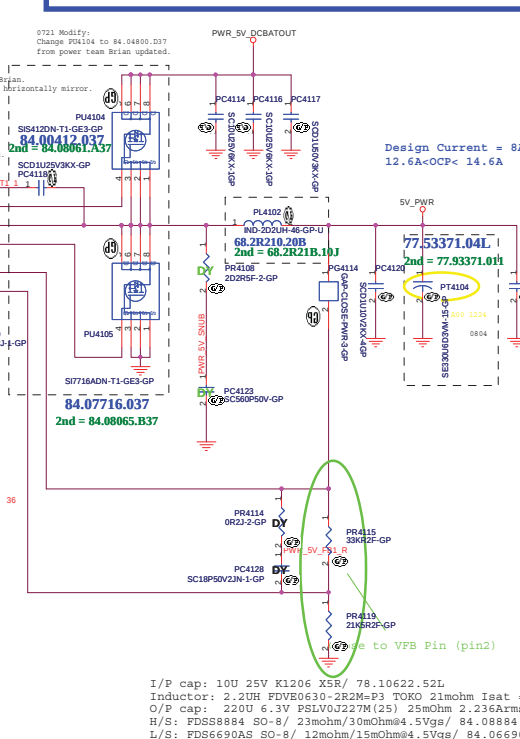
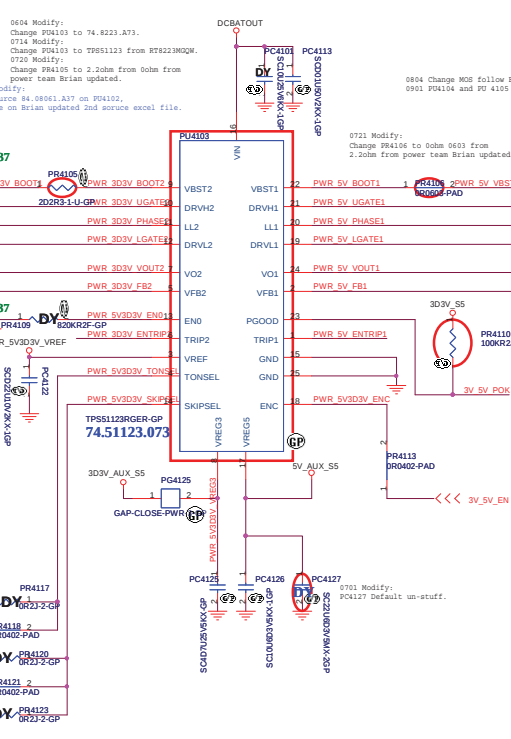
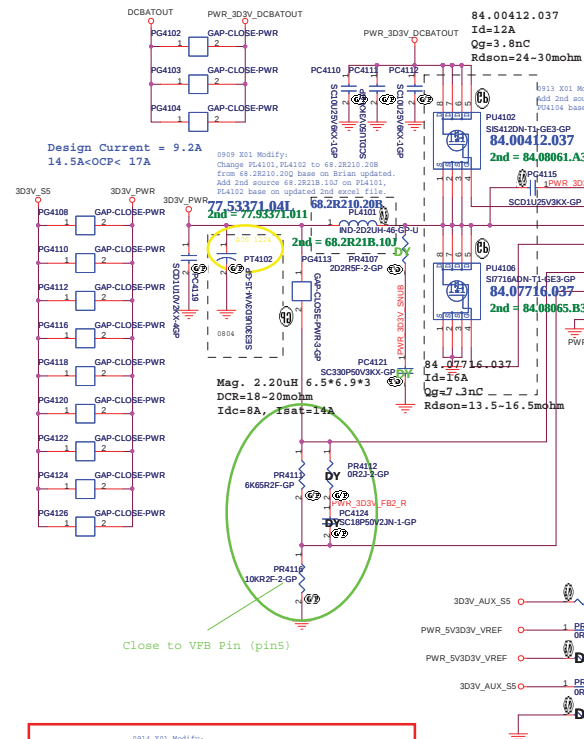
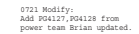
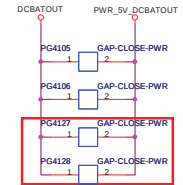
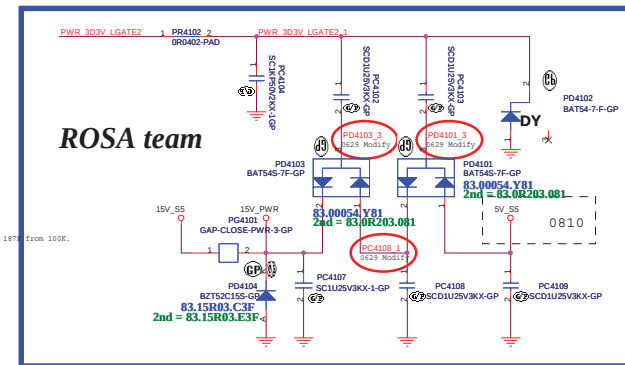
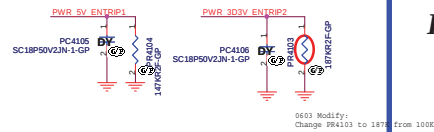
0930 X01 Modify:
Change D3901-D3903 main source to 83.00099.T11
for 83.BAV99.D11 shortage issue.

<http://hobi-elektronika.net>

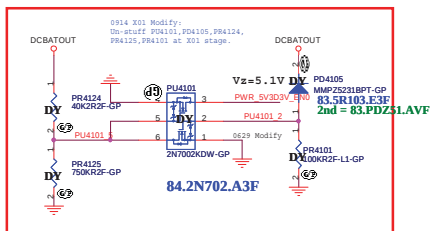
<Core Design>

DELL		Wistron Corporation	
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Title			
BATT CONN			
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```
SSID = PWR.Plane.Regulator 5v3p3v
```



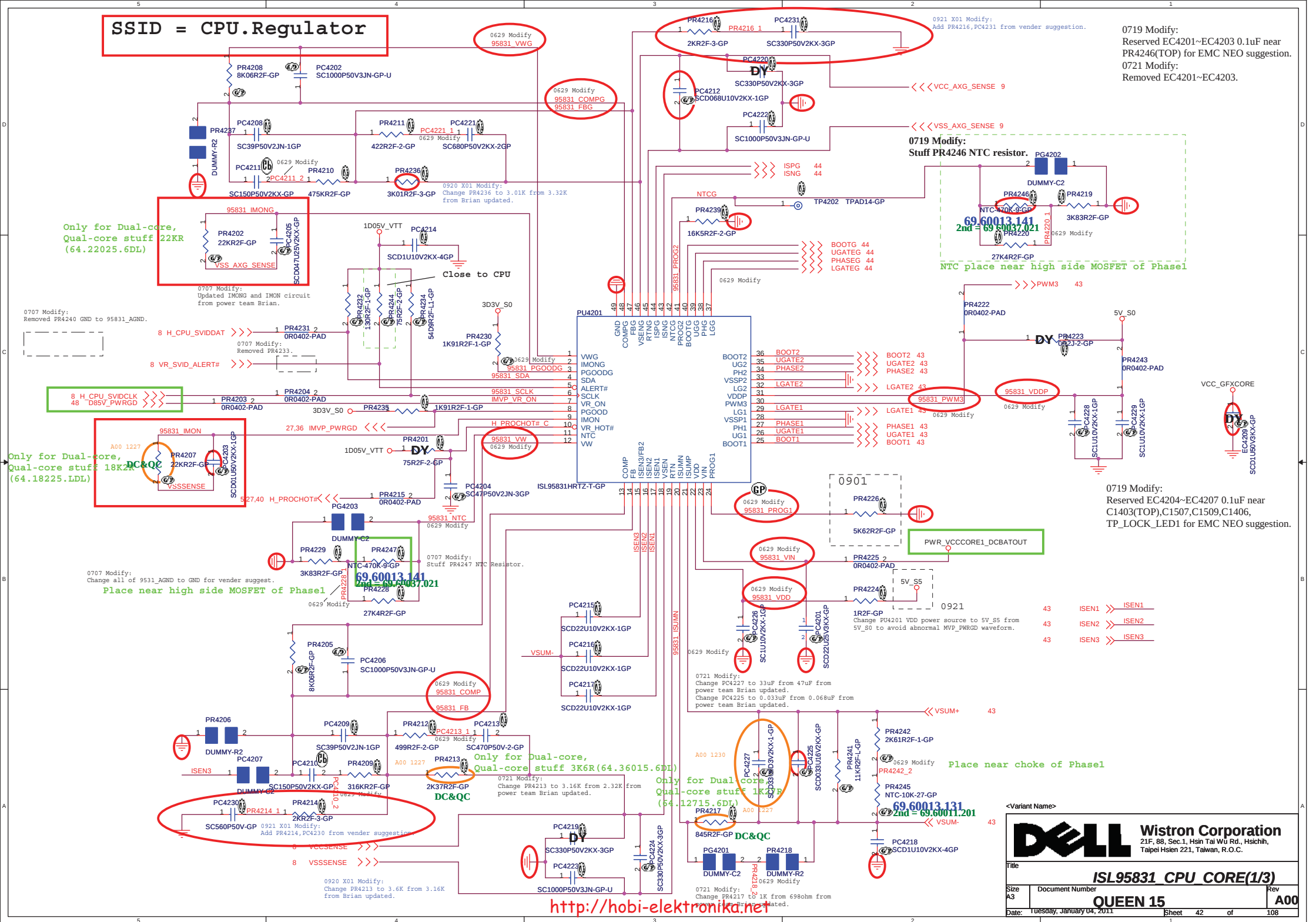
0719 Modify:
Reserved EC4101~EC4106 0.1uF near
PTC4101,PC4119 for EMC NEO suggestion.

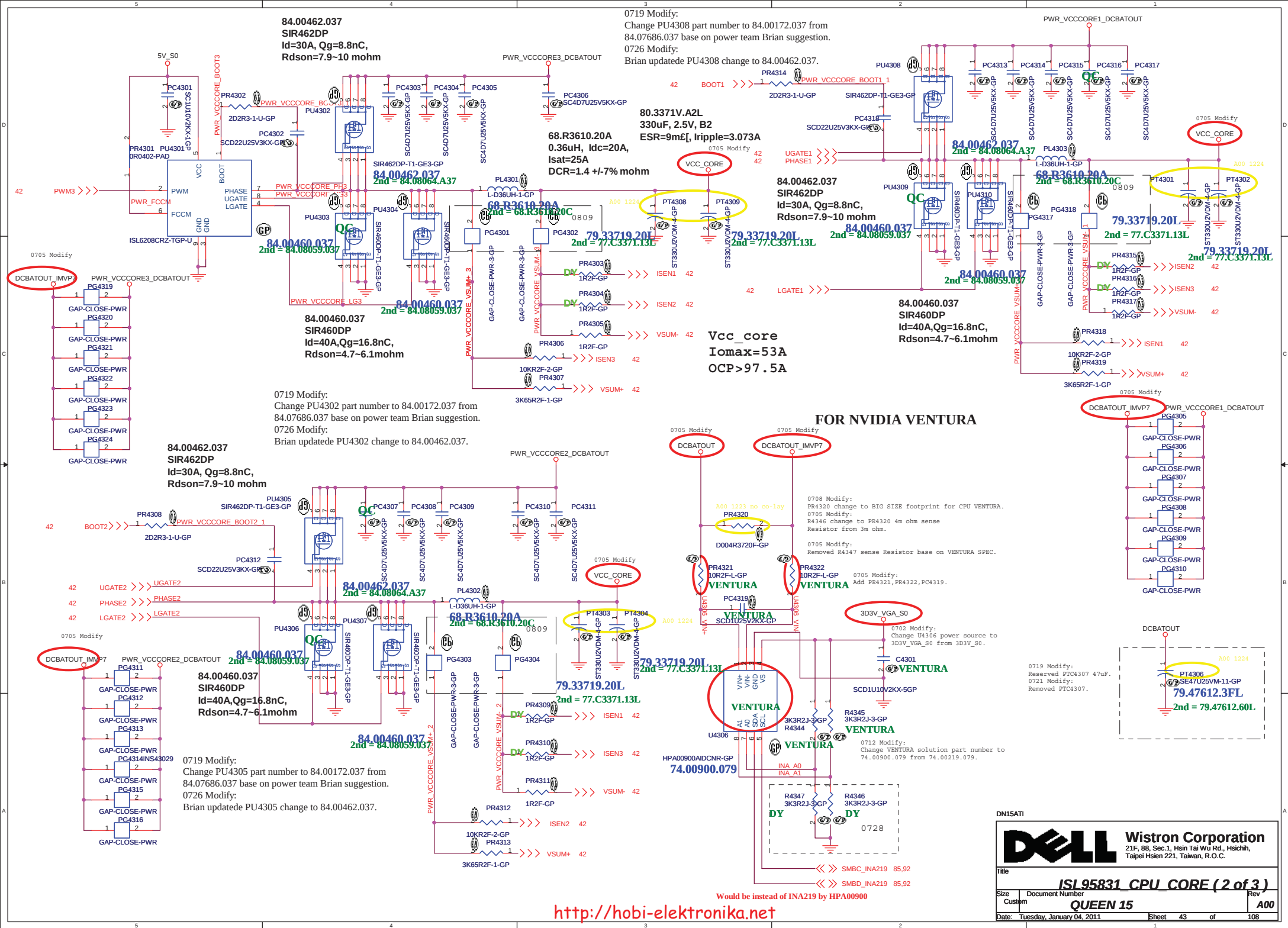


TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

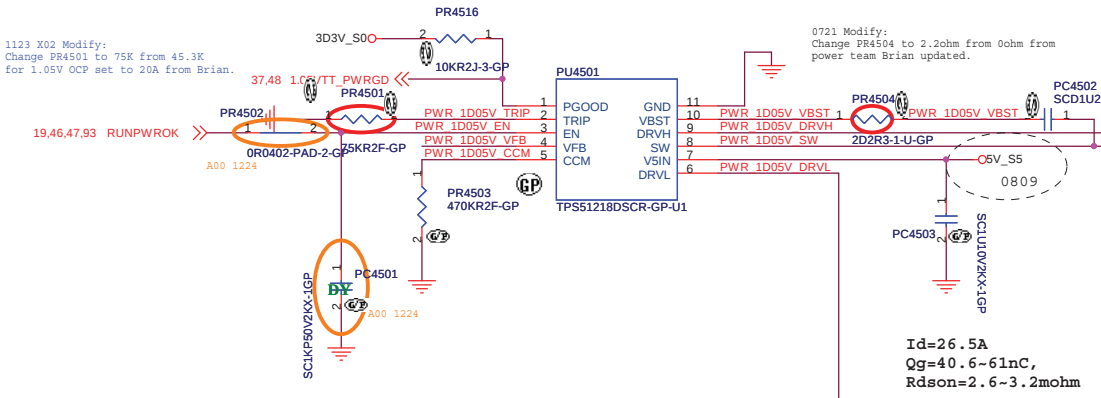
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVBE0630-2R2M(3) TOKO 21mohm Isat =8.7A rms 68.2R21B.10A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDS58884 SO-8 / 23mohm/30mohm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8 / 12mohm/15mohm@4.5Vgs/ 84.06690.E37





TPS51218 for 1D05V

1123 X02 Modify:
Change PR4501 to 75K from 45.3K
for 1.05V OCP set to 20A from Brian.



84.00172.037
BSZ115N03MSC
Id=20A, Qg=9.8nC,
Rdson=8.9 mOhm

0721 Modify:
Change PR4504 to 2.2ohm from 0ohm from
power team Brian updated.

Id=26.5A
Qg=40.6~61nC,
Rdson=2.6~3.2mOhm

0719 Modify:
Change PU4502 part number to 84.00172.037 from
84.07686.037 base on power team Brian suggestion.

1122 X02 Modify:
stuff EC4501 0.1uF from
BMC Neo suggestion.

84.00172.037
2nd = 84.08065.037

Mag. 2.20uH 10*11.5*4
DCR=6.7~7mOhm
Idc=12A, Isat=27A

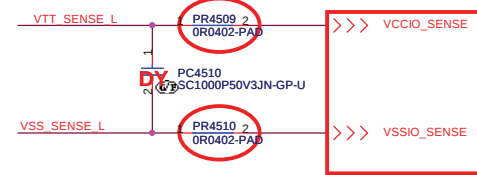
Design Current = 9.9A
15.6A<OCP< 18.3A

0909 X01 Modify:
Change PL4501 to 68.2R210.20C
from IND-D56UH-27-GP base on
Brian updated.

68.2R210.20C
2nd = 68.2R21B.101

79.3971V.30L
2nd = 77.93971.02L

0721 Modify:
Brian suggest change PU4503 to 84.00460.037.
Change PR4506 to 9.76K from 10K from
power team Brian updated.



$$V_{out} = 0.704V * (R1 + R2) / R2$$

0617 Modify:
Joseph Change PTC4502 to 330uF from 390uF
base on layout placement status.

0721 Modify:
Brian Add PC4511 1uF.
Change PTC4502 to 330uF 79.33719.L01.

0719 Modify:
Reserved EC4502, EC4503 0.1uF near
PG4516(TOP) for EMC NEO suggestion.

0727 Modify:
PR4505, PR4508 change to 100ohm from 10ohm.
stuff PR4509, PR4510 0ohm from Brian updated.

0901 X01 Modify:
Change PTC4502 to 79.3371V.30L from
79.33719.L01 from power team Brian updated.
0913 X01 Modify:
Add 2nd source 77.93971.02L on PTC4502
base on Brian updated 2nd source excel file.

SSID = PWR.Plane.Regulator_1p5v0p75v

0719 Modify:
Change PU4602 part number to 84.00172.037 from 84.07686.037 base on power team Brian suggestion.

84.00172.037
BSZ115N03MSC
Id=20A, Qg=9.8nC,
Rdson=8.9 mohm

0630 modify
PU4602
84.00172.037
2nd = 84.08065.037

84.00460.037
SIR460DP-T1-GE3
Id=40A, Qg=16.8nC,
Rdson=4.7~6.1 mohm

84.00460.037
2nd = 84.08059.037

0913 X01 Modify:
Add 2nd source 68.R681A.10Q on PL4601
base on Brian updated 2nd source excel file.

PL4601
IND-D68UH-51-GP-U
68.R6810.20G
2nd = 68.R681A.10Q
Id=22~39A
DCR=2.4~2.7mohm
Size=10X11.5X4

Design Current = 14.45A
22.71A<OCP< 26.84A

79.3971V.30L
2nd = 77.93971.02L

0902 X01 Modify:
Change PTC4602 to 79.3971V.30L from 79.22719.20L sync with DQ15-NV
Add 2nd source 77.93971.02L on PTC4602.

79.3971V.30L
390uF, 2.5V, 6.3X5.7
ESR=10mE, Iripple=3.87A

0630 Modify:
ADD PC4604 1uF0603 on PWR_1D5V_VTTIN.

0721 Modify:
Removed PR4615, PR4616 and connect 0D75V_EN to VTTEN directly.

0721 Modify:
Removed PR4615, PR4616 and connect 0D75V_EN to VTTEN directly.

0721 Modify:
Change PR4602 to 68K from 6.2K from power team Brian updated.

0920 X01 Modify:
Change PR4602 to 110K from 68K from Brian updated.

0630 Modify:
Change 1D5V power solution to TPS51216 from TPS5116 follow power team Brian suggest.

0630 Modify:
Change PC4610 to 0.22u 0402 from 0603 from Brian.

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	Frequency	Discharge Mode
PR5003	400kHz	Tracking Discharge
200k ohm	300kHz	
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

DDR_VREF_S3
PWR_1D5V_VTTREF 1 PR4611 2 0R0603-PAD
0702 Modify:
Add PR4611 0ohm 0603 pad on PWR_1D5V_VTTREF.

19.27,75 PM_SLP_S4#

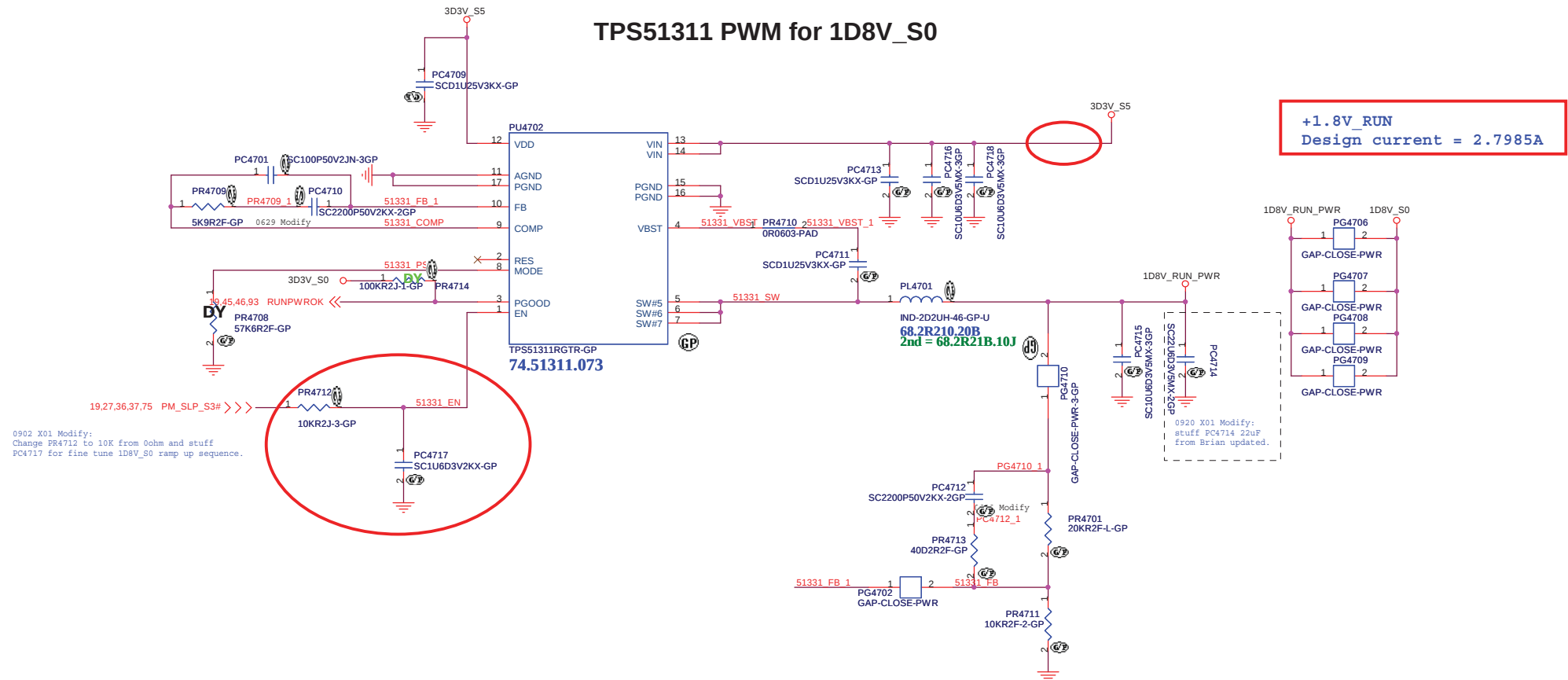
PR4607
0R0402-PAD-2-GP
A00 1224
PWR_1D5V_EN
PC4606
SCD1U10V2KX-5GP

<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
		TPS51116 +1.5V SUS	
Size A3	Document Number	Rev	
Date: Tuesday, January 04, 2011		A00	
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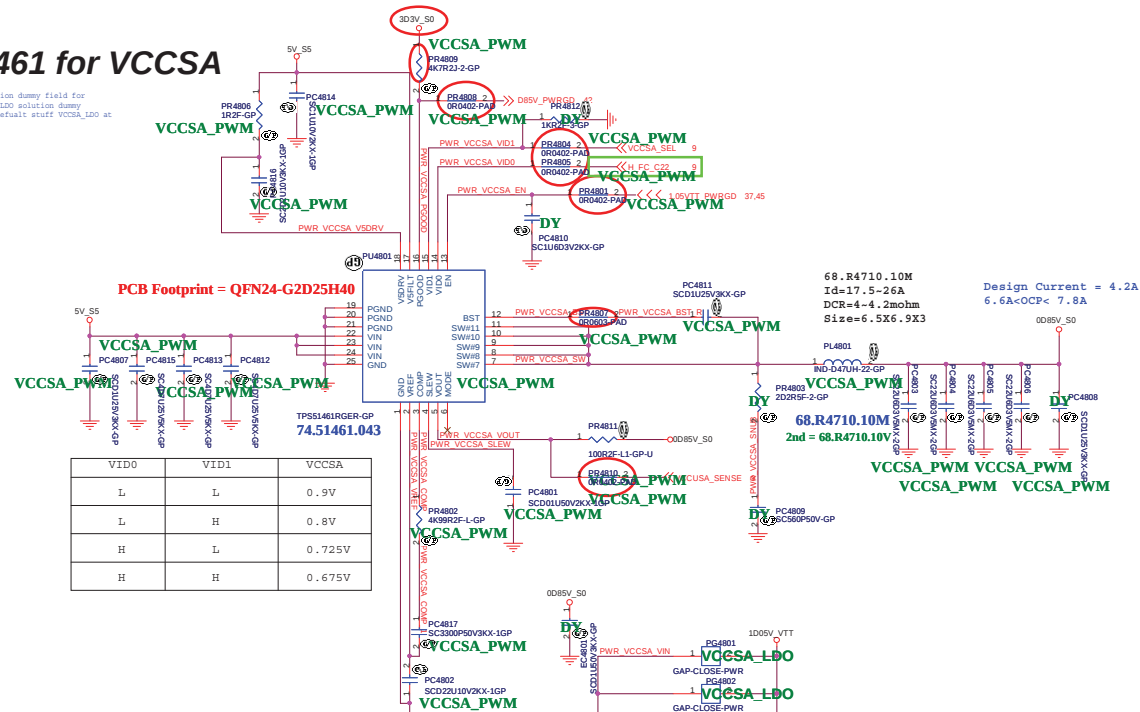
```
SSID = PWR.Plane.Regulator_1D8V_S0
```

TPS51311 PWM for 1D8V_S0



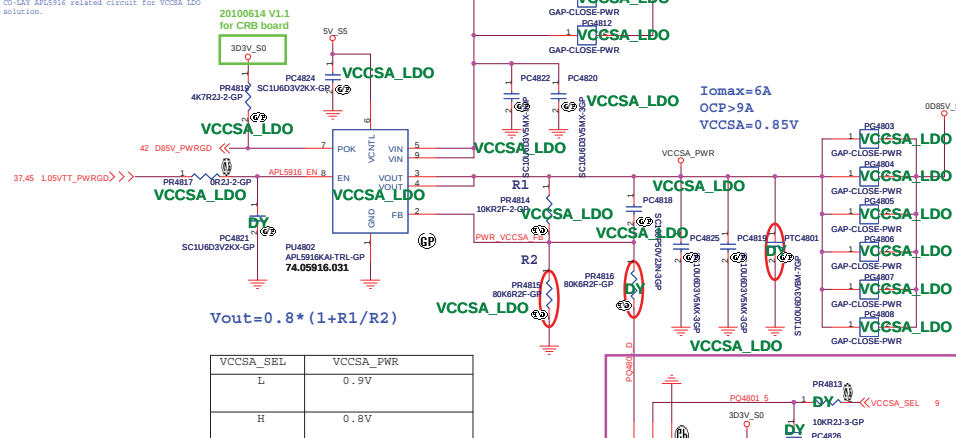
TPS51461 for VCCSA

1112 X02 Modify:
set 79B1461 PWM solution dummy field for
VCCSA_PWM and 30V55 100 solution dummy
field for VCCSA_LDO. default stuff VCCSA_LDO at
ST stage.



APL5916 for VCCSA

1112 X02 Modify:
CD-LAY APL5916 related circuit for VCCSA_LDO
solution.

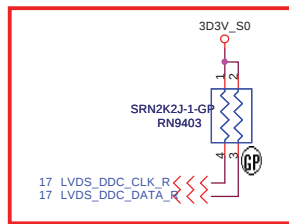


<Core Design>

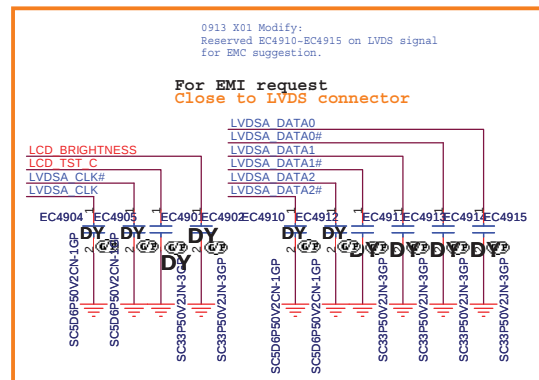
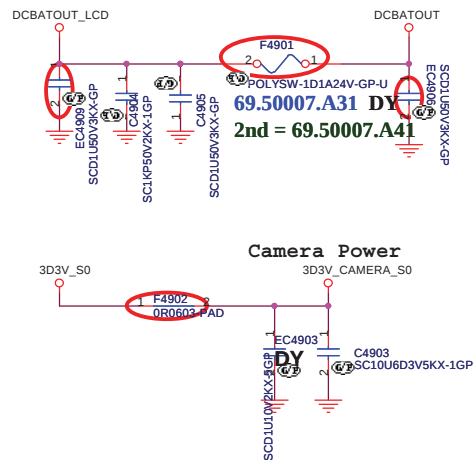
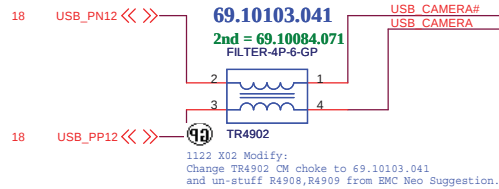
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsueh,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51461 VCCSA**
Size: **Document Number**
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0909 X01 Modify:
Change LCD1 to 20.F1816.030 for 30pin
Re-assign LCD1 pin define base on Roy updated
cable pin define list.

[illegible]

(MB Pin Define)	
MB CONN. (WIRE)	
Pin 1	DCBATOUT_LCD
Pin 2	DCBATOUT_LCD
Pin 3	DCBATOUT_LCD
Pin 4	NC
Pin 5	LCD_BRIGHTNESS
Pin 6	3D3V_CAMERA_S0
Pin 7	USB_CAMERA#
Pin 8	USB_CAMERA
Pin 9	GND
Pin 10	GND
Pin 11	AUD_DMIC_CLK
Pin 12	AUD_DMIC_IN0
Pin 13	LVDSA_CLK
Pin 14	LVDSA_CLK#
Pin 15	BLON_OUT_C
Pin 16	LVDSA_DATA2
Pin 17	LVDSA_DATA2#
Pin 18	GND
Pin 19	LVDSA_DATA1
Pin 20	LVDSA_DATA1#
Pin 21	GND
Pin 22	LVDSA_DATA0
Pin 23	LVDSA_DATA0#
Pin 24	LVDS_DDC_DATA_R
Pin 25	LVDS_DDC_CLK_R
Pin 26	LCD_TST_C
Pin 27	3D3V_S0
Pin 28	LCDVDD
Pin 29	LCDVDD
Pin 30	LCDVDD



BATS4CPT-GP

17 LVDS_VDD_EN >>> 1

27 LCD_TST_EN >>> 2

3 LCDVDD_EN

D4901

83.R2003.E81
2ND = 83.00054.Q81

Layout 40 mil

U4901
G5285T11U-GP

1 EN
2 GND
3 OUT
4 IN#4
5 IN#5

74.05285.07F
2nd = 74.09724.09F

SC4907
7406D3KX-GP

C4908
SC4907
7406D3KX-GP

R4905
48K9R2F-L-GP

SC4907
7406D3KX-GP

1122 X02 Modify:
stuff EC4907 0.1uF from
EMC Neo suggestion.

R4907
100KR2J-1-GP

BLON_OUT_C
LCD_TST_C

RN4901

SRN1003-3 GP
1122 X02 Modify:
Change RN4901 to 100ohm 4p from 8p
for improve layout place.

BLON_OUT 27
LCD_TST 27

CLOSED TO LVDS CONN LCD1

TPNL

5

1

2 USB PNO_C

3 USB PP0_C

4

6

1122 X02 Modify:
stuff C4908 0.1uF from
EMC Neo suggestion.

GP

ACES-CON4-17-GP-U

20.F1621.004

2nd = 20.F1561.004

3rd = 20.F1686.004

1621.004 from
(F.

161.004;3rd source
i from updated

TPNL 5V

TPNL

TPNL 5V

TPNL

R4904

5V_S0

TPNE

OR0402-PAD-2-GP

A00 1230

SCD1U10V2KX-4GP

C4910

SCD1U10V2KX-1GP

USB_PNO_C

USB_PP0_C

A00 1229

TR4901

TPNE

FILTER-4P-6-GP

69.10103.041

2nd = 69.10084.071

1122 X02 Modify:
Swap TR4901 pin4,3 and pin2,1 each other
base on Connie swap report.
Change TR4901 CH choke to 69.10103.041
and un-stuff R4911,R4912 from EMC Neo Suggestion.
Change R4911,R4912 to 0603 from 0402.

DN15ATI Whistler

```
0916 X01 Modify:
Change TPNL1 to 20.F1621.004 from
Double updated EMN&DXF.
0917 X01 Modify:
Add 2nd source 20.F1561.004;3rd source
20.F1686.004 on TPNL1 from updated
connector list.
```

DN15ATI Whistler



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Title			
LCD Connector			
Size A3	Document Number		Rev
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<Variant Name>



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Title

CRT Connector

Size
A3

Document Number
QUEEN 15

Rev
A00

Date: Tuesday, January 04, 2011

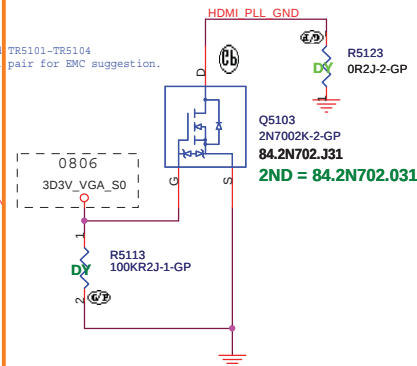
Sheet 50 of 108

SSID = VIDEO

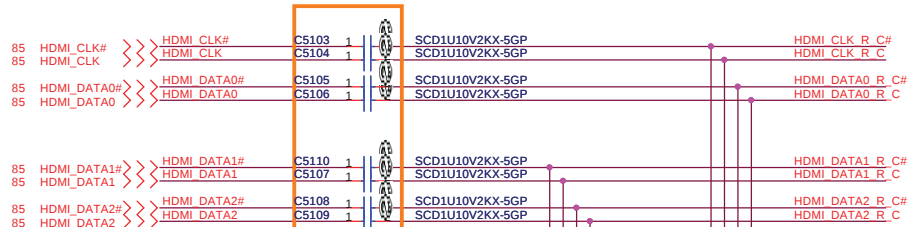
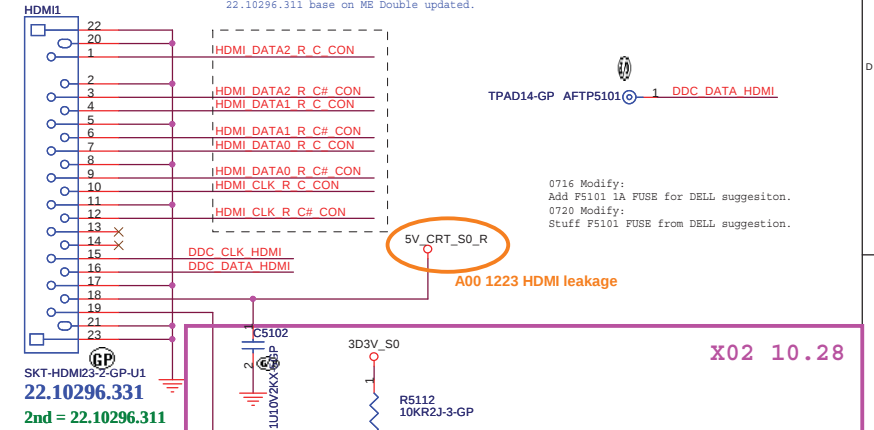
HDMI Level Shifter & CONNECTOR



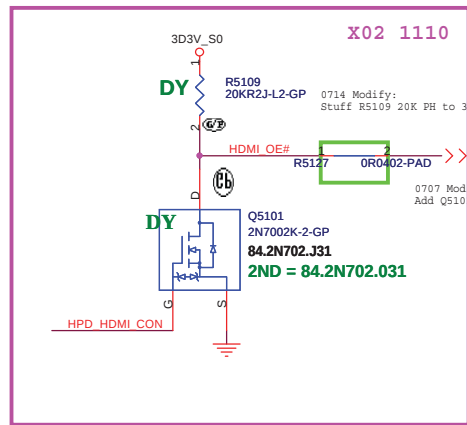
A00 1229



HDMI CONN



Close to HDMI Connector



Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<http://hobi-elektronika.net>

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: HDMI Level Shifter/Connector			
Size: A3	Document Number: QUEEN 15	Rev: A00	
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<Core Design>



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Title

Reserved

Size
A3

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<Core Design>



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Title

LVDS Switch

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

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Rev
A00

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SSID = User.Interface

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

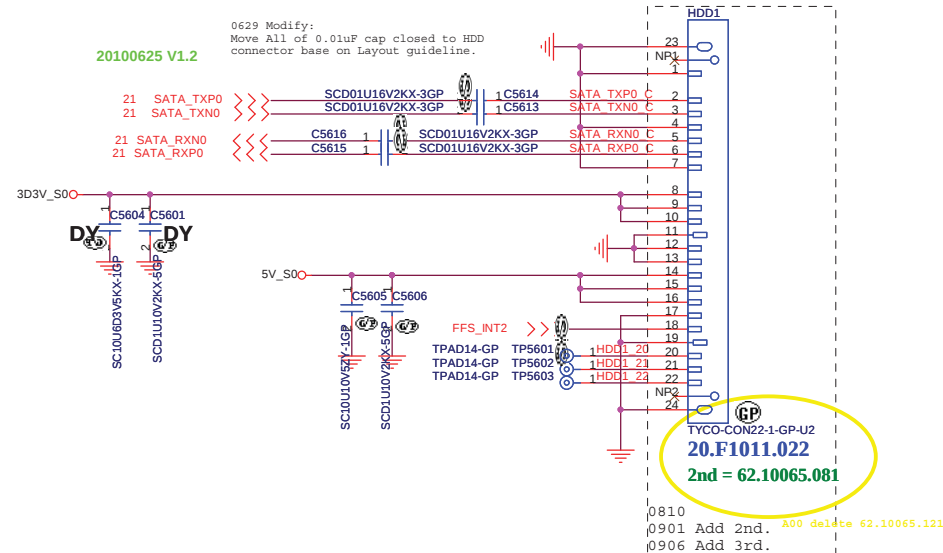
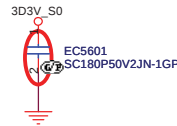
ITP/Fan Connector

Size	Document Number	Rev
A3	QUEEN 15	A00
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SSID = SATA

SATA HDD Connector

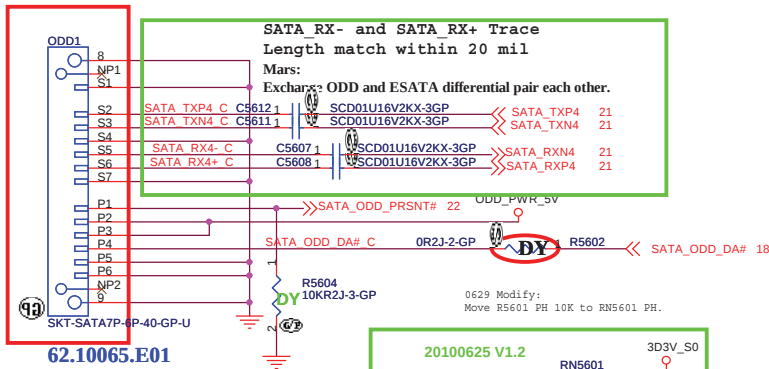
1123 X02 Modify:
stuff EC5601 180pF from RF
fine tune result.



ODD Connector

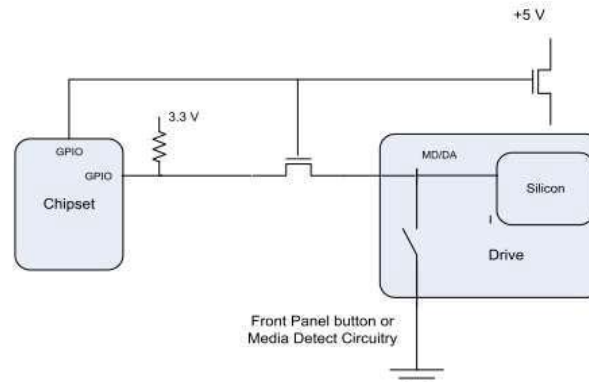
20100625 V1.2

0629 Modify:
Move All of 0.01uF cap closed to ODD
connector base on Layout guideline.

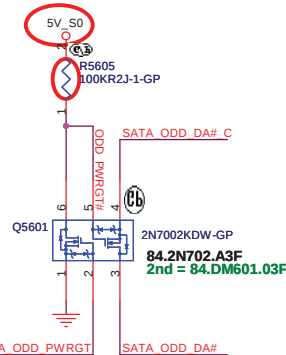


0614 Modify:
Change ODD1 connector part number to
22.10300.421 base on ME BMN and DXF.
0707 Modify:
Change ODD1 connector part number to
62.10065.E01 base on latest BMN and DXF.

SUPPORT ZERO SATA ODD



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

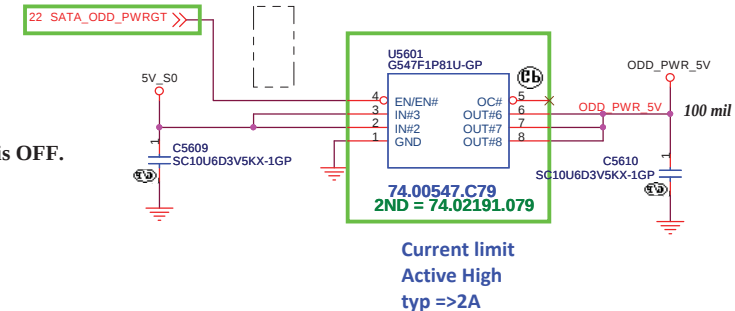


0707 Modify:
Change R5601 to 10K to 100K for use in the MD/DA signal between PCH and ODD.

<http://hobi-elektronika.net>

SATA Zero Power ODD

0629 Modify:
Move R5601 PH 10K to RN5601 PH.



Current limit
Active High
typ =>2A

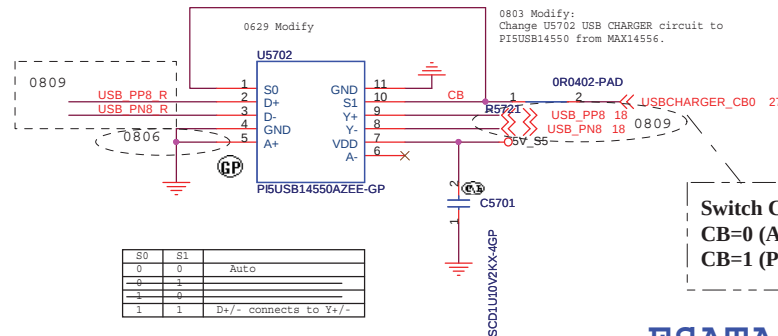
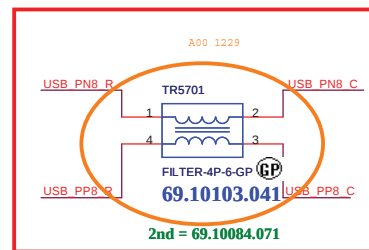
<Variant Name>

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title HDD/ODD			
Size A3	Document Number QUEEN 15	Rev A00	
Date: Tuesday, January 04, 2011	Sheet 56	of 108	

SSID = ESATA

USB CHARGER

1122 X02 Modify:
Change TR5701CM choke to 69.10103.041
and un-stuff R5718,R5719 from BMC Neo Suggestion.
1123 X02 Modify:
Change R5718,R5719 to 0603 from 0402.

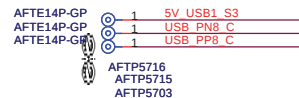


Switch Control Bit:

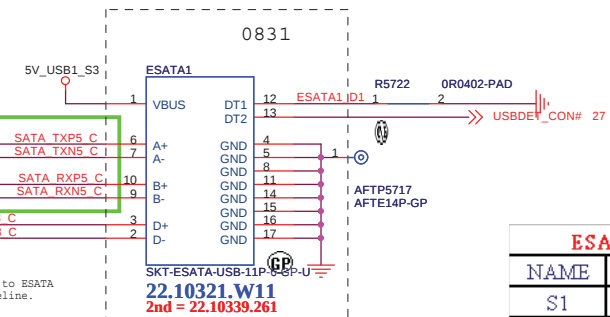
CB=0 (AM):auto detection charger identification active.
CB=1 (PM):connect DP/DM to TDP/TDM.

ESATA CONN

close to ESATA1



0629 Modify:
Move All of 0.01uF cap closed to ESATA
connector base on Layout guideline.
0706 Modify:
Change ESATA1 part number to 22.10321.F71
base on latest BMN and DXF.
0713 Modify:
Add USBDET_CON# on ESATA1 pin15 for
USB temporary detect solution ESATA1 CONN
should be searched for detect type connector.
0719 Modify:
ME Double provide temporary foxconn ESATA conn
22.10290.141 for SSI stage function test.



E-SATA USB 2.0 Combo

CE/H=-0.16/2.83mm with detect function

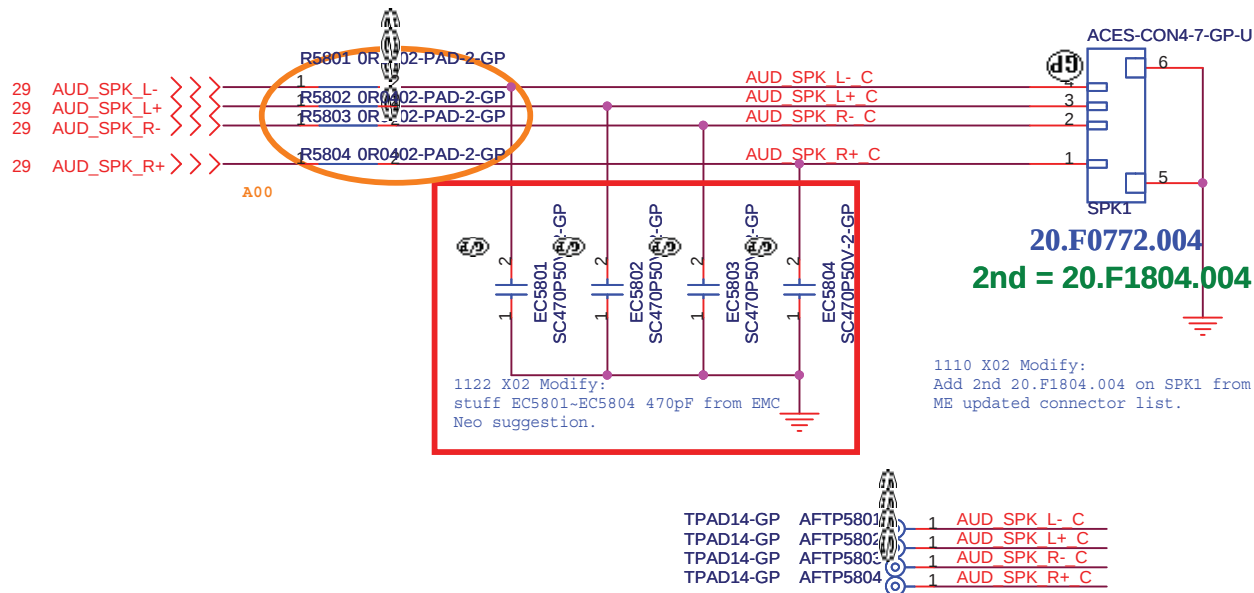
ESATA	
NAME	TYPE
S1	GND
S2	A+
S3	A-
S4	GND
S5	B-
S6	B+
S7	GND
USB	
NAME	TYPE
U1	VBUS
U2	D-
U3	D+
U4	GND

<Core Design>

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Title ESATA			
Size A3	Document Number	QUEEN 15	Rev A00
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SSID = AUDIO

Speaker Connector



MB CONN. (WIRE)

Pin 4	AUD_SPK_L-C
Pin 3	AUD_SPK_L+C
Pin 2	AUD_SPK_R-C
Pin 1	AUD_SPK_R+C

0913 X01 Modify:
Change SPK1 to 20.F0772.004 from
20.F1647.004 from Double updated.
0914 X01 Modify:
Re-assign SPK1 pin define base on
Roy updated excel file for 20.F0772.004

1110 X02 Modify:
Add 2nd 20.F1804.004 on SPK1 from
ME updated connector list.

<Core Design>



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Title

SPEAKER CONN

Size
A4

Document Number

QUEEN 15

Rev

A00

Date: Tuesday, January 04, 2011

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
QUEEN 15

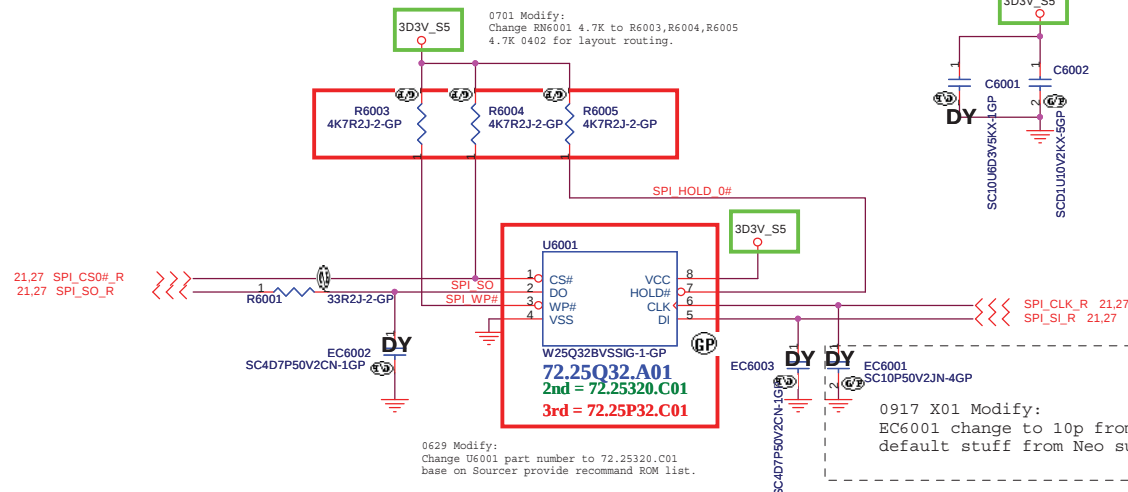
Date: Tuesday, January 04, 2011

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A00

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SSID = Flash.ROM

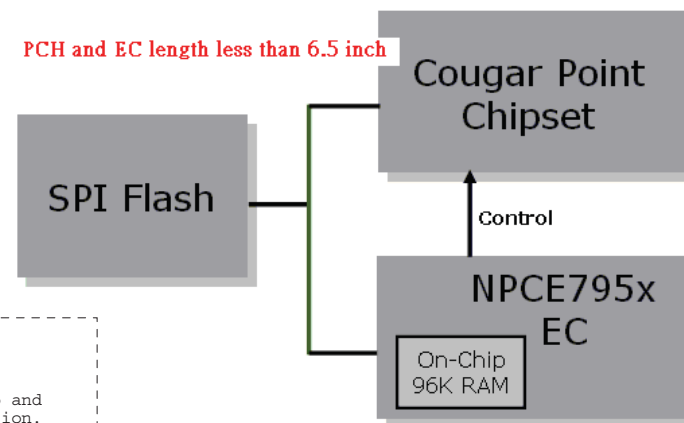
SPI FLASH ROM (4M byte) for PCH



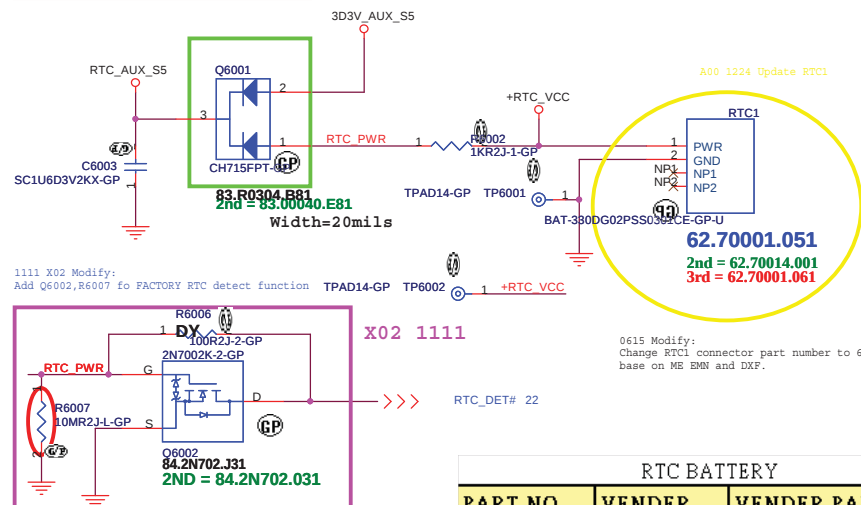
	Priority	Wistron P/N	Manufacturer	Vendor P/N
X02	1	72.25Q32.A01	WINBOND	W25Q32BVSSIG
	2	72.25320.C01	MXIC	MX25L3206EM2L-12G
X02	3	72.25P32.C01	Numonyx	M25PX32-VMWV6F

Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

PCH and EC length less than 6.5 inch



SSID = RBATT



RTC BATTERY		
PART NO	VENDER	VENDER PART NO.
23.20023.311	MITSUBISHI	CR2032 MITSUBISHI
23.20023.341	HENSHEN	CR-2032L/DBE
23.20068.001	KTS	BBBCR2032BX

<http://hobi-elektronika.net>

VccRTC is now connected to VccDSW3_3 through the Schottky diode instead of the 3.3V Sus well.

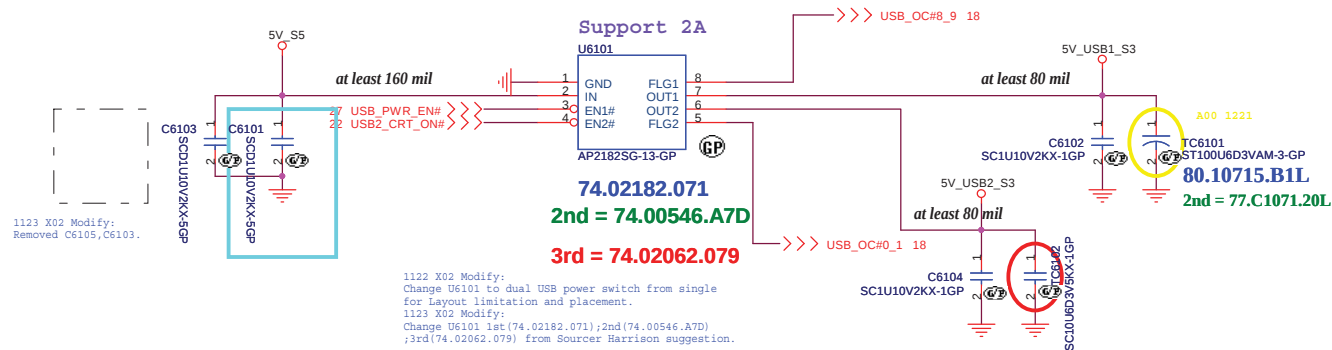
<Variant Name>

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Title: **Flash/RTC**
Size: A3 Document Number: **QUEEN 15** Rev: **A00**
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SSID = USB

CRT Board and COMBO USB Power



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<Core Design>

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Title			
USB Power SW			
Size	Document Number		Rev
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<Core Design>



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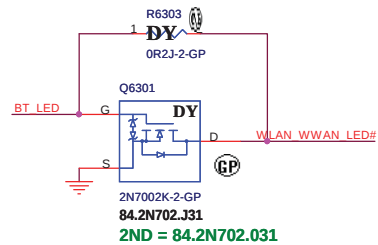
Title

Reserved

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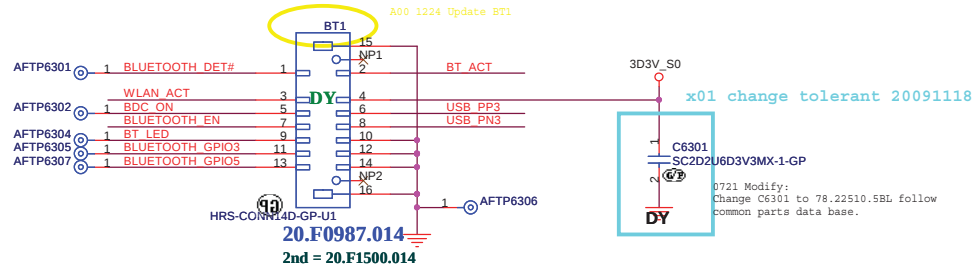
SSID = User.Interface



0722 Modify:
Add Q6301 and combine BT_LED to
WLAN_WWAN_LED#.

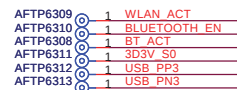


Bluetooth Module conn.



0721 Modify:
Change C6301 to 78.22510.58L follow
common parts data base.

0709 Modify:
PM confirmed there is no stand-alone BT module,
so DY BT1 connector, add BT enable signal
and 5V_S5 power option on WLAN connector pin 51.
0712 Modify:
Stuff BT relatex component to verify function.



<Core Design>

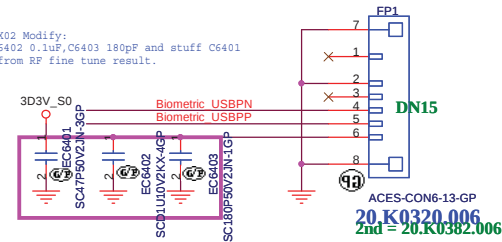


Title		Bluetooth	
Size	Document Number	Rev	
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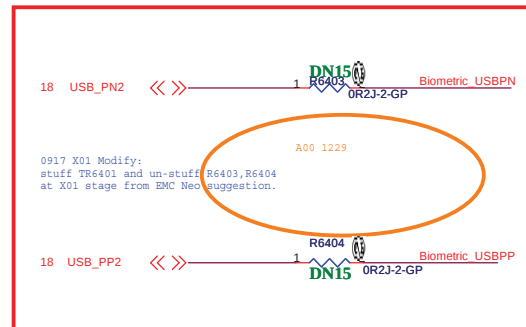
Finger Printer Connector

0707 Modify:
Add FP_DET# signal on FP1 pin1.
0715 Modify:
Add FP_DET# signal on FP1 pin1.
0806 Swap pin.
0810 Change to 4 pin.
0827 Change to 6 pin.

1123 X02 Modify:
Add C6402 0.1uF, C6403 180pF and stuff C6401
47pF from RF fine tune result.



MB CONN.(FFC)	
Pin1	NC
Pin2	GND
Pin3	NC
Pin4	Biometric_USBPN
Pin5	Biometric_USBPP
Pin6	3D3V_S0



0917 X01 Modify:
stuff TR6401 and un-stuff R6403, R6404
at X01 stage from EMC Neo suggestion.

AFTP42 1 3D3V_S0
AFTP43 1 Biometric_USBPN
AFTP44 1 Biometric_USBPP

0615 Modify:
Change FP1 connector part number to 20.K0320.004
base on ME EMN and DXF.
0630 Modify:
Change FP1 connector part number to 20.K0320.006
base on ME EMN and DXF.
0707 Modify:
Reassign Finger print pin define base on EXCEL FILE.
0713 Modify:
Reassign Finger print pin define base on EXCEL FILE.
Removed FP_DET# on FP1.

<Core Design>

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<Core Design>



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Title

RESERVED

Size
A3

Document Number
QUEEN 15

Rev
A00

Date: Tuesday, January 04, 2011

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<Core Design>



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Title

Reserved

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<Core Design>



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Title

Reserved

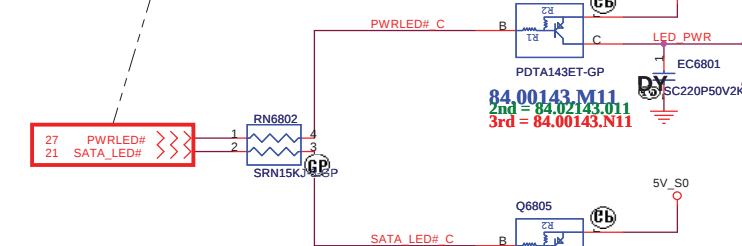
Size	Document Number	Rev
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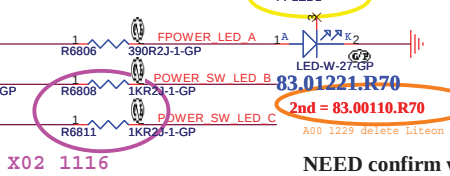
SSID = User.Interface

FRONT POWER LED

Need change to LOW acted from KBC GPIO



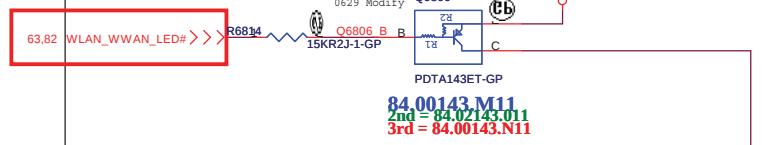
NEED confirm with ME actual
FPOWER_LED part number.



0706 Modify:
Change FPOWER_LED part number to
83.01221.R70 base on latest EMN and DXF.

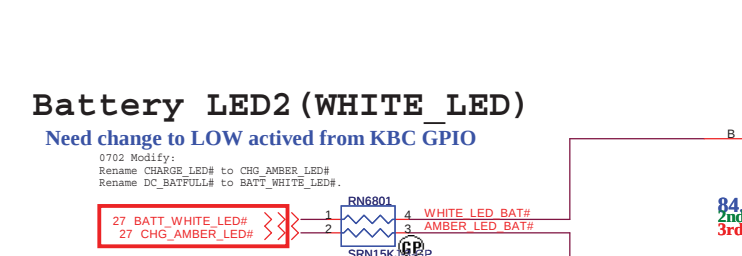
WLAN_LED

0706 Modify:
WLAN_LED# rename to WLAN_WWAN_LED#.

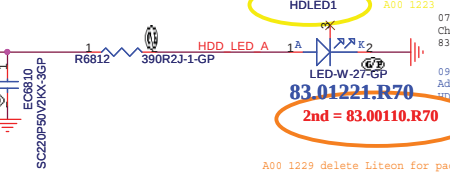


SATA HDD LED(White)

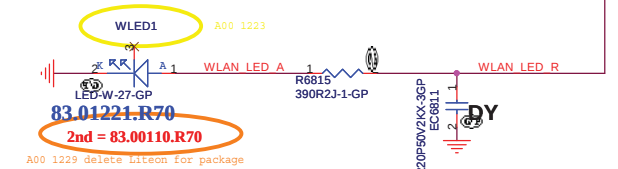
Need change to LOW acted from KBC GPIO



NEED confirm with ME actual
HDD_LED part number.

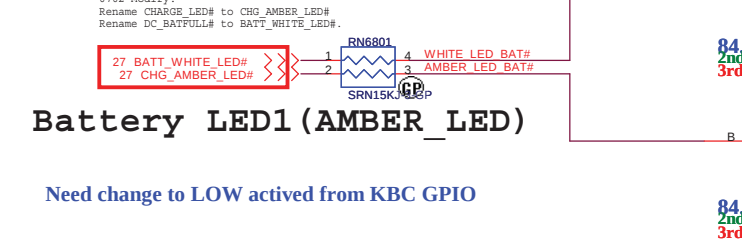


0706 Modify:
Change HDD_LED part number to
83.01221.R70 base on latest EMN and DXF.

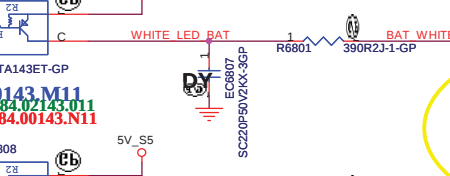


Battery LED2 (WHITE_LED)

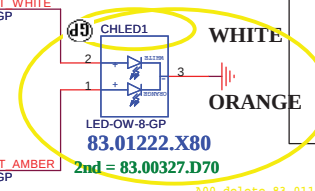
Need change to LOW acted from KBC GPIO



NEED confirm with ME actual
HDD_LED part number.

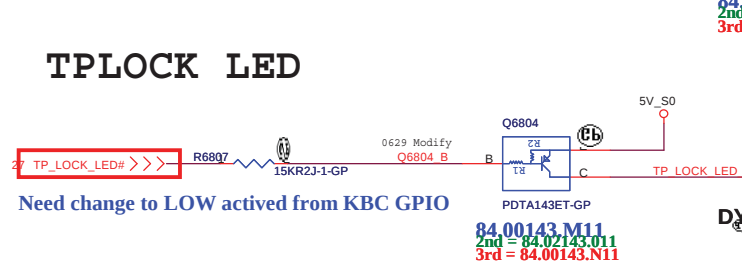


0706 Modify:
Change HDD_LED part number to
83.01221.R70 base on latest EMN and DXF.

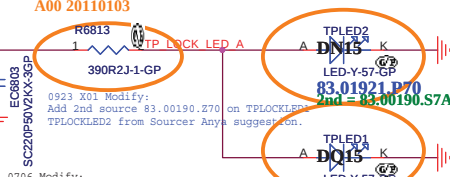


Battery LED1 (AMBER_LED)

Need change to LOW acted from KBC GPIO



NEED confirm with ME actual
HDD_LED part number.

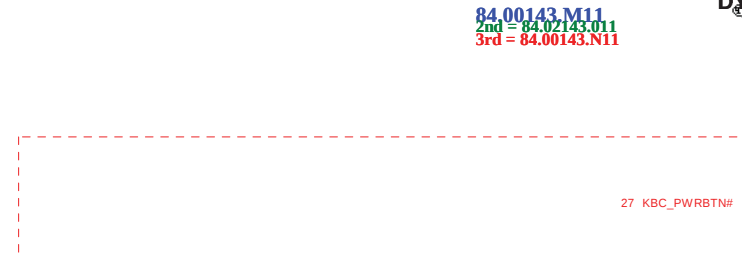


0706 Modify:
Change HDD_LED part number to
83.01221.R70 base on latest EMN and DXF.

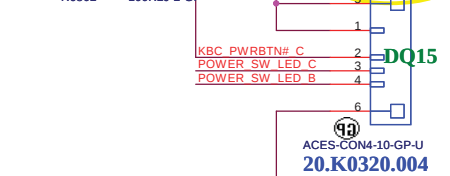
SKEW	ITEM1	ITEM2
DQ15	PWRBTN1	TP_LOCK_LED1
DN15	PWRBTN2	TP_LOCK_LED2

TPLOCK LED

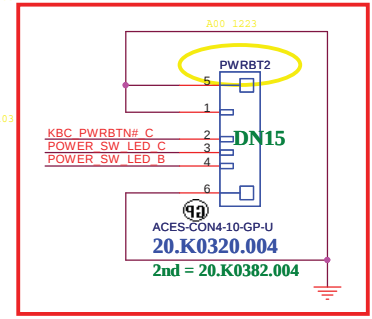
Need change to LOW acted from KBC GPIO



NEED confirm with ME actual
HDD_LED part number.



0706 Modify:
Change TP_LOCK_LED part number to
83.19217.J70 base on latest EMN and DXF.



0715 Modify:
Removed PWR_BTN_LED# control circuit
base on Dell feedback.

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File: **LED Bard/Power Button**

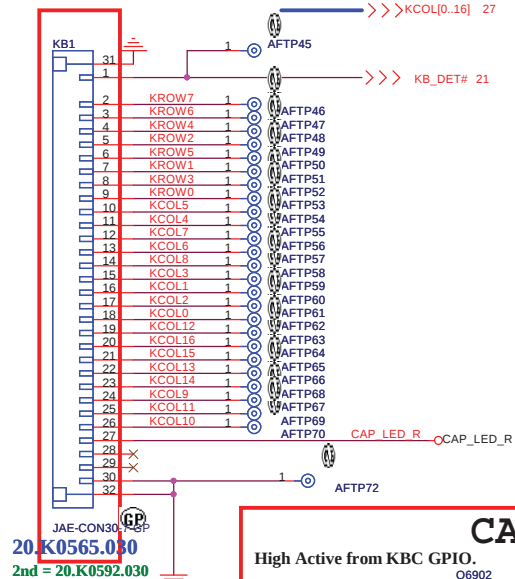
Size A3 Document Number: **QUEEN 15** Rev: **A00**

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SSID = KBC

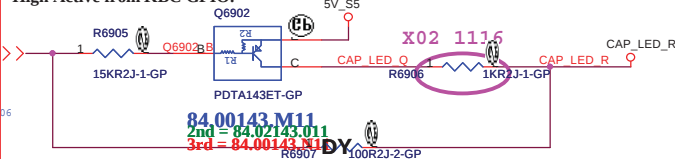
Internal KeyBoard Connector

0630 Modify:
Change KB1 part number to 20.K0565.030
base on ME updated EMN and DXF.

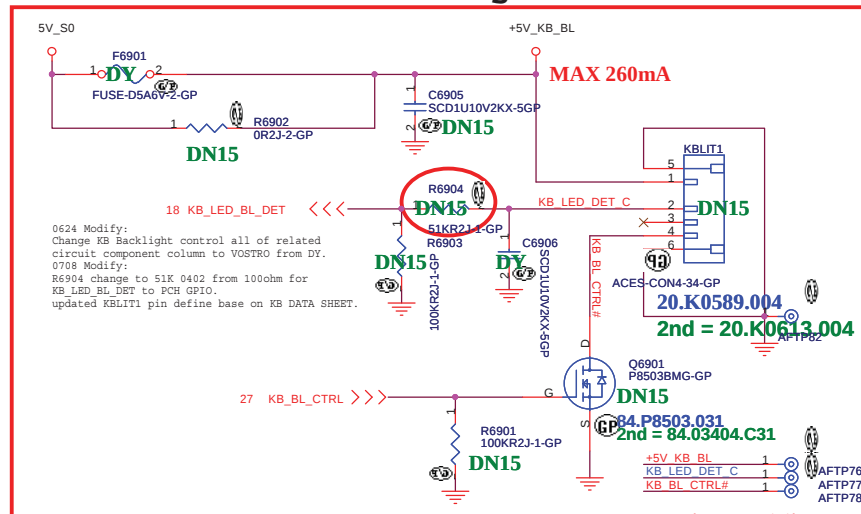


CAP LED CONTROL

High Active from KBC GPIO.



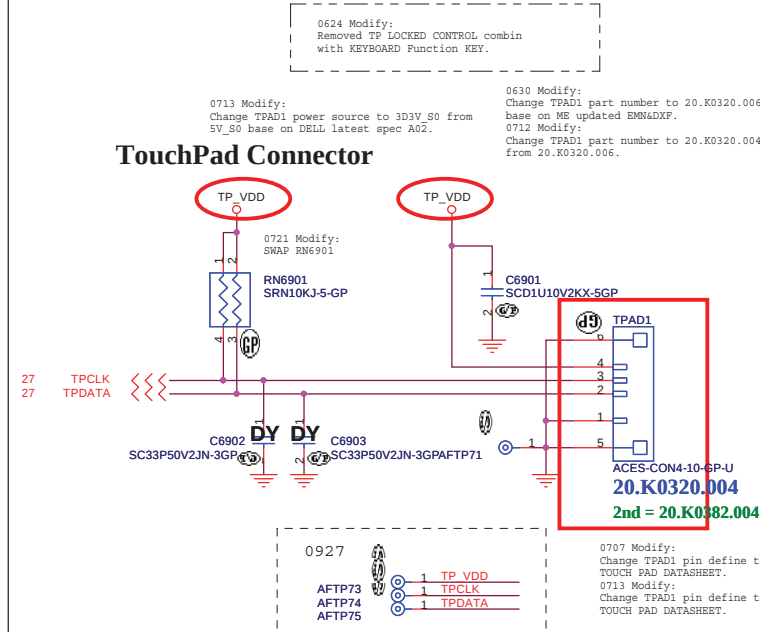
KB Backlight Connector



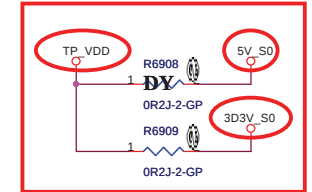
MB Pin	Description
1	Diag_Loop3 = GPIO_1 (TPC)
2	KSII[7] = KBD S8
3	KSII[6] = KBD S7
4	KSII[4] = KBD S5
5	KSII[2] = KBD S3
6	KSII[5] = KBD S6
7	KSII[1] = KBD S2
8	KSII[3] = KBD S4
9	KSII[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[7] = KBD D8
13	KSO[6] = KBD D7
14	KSO[8] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[12] = KBD D13
20	KSO[16] = KBD D17
21	KSO[15] = KBD D16
22	KSO[13] = KBD D14
23	KSO[14] = KBD D15
24	KSO[9] = KBD D10
25	KSO[11] = KBD D12
26	KSO[10] = KBD D11
27	NC (reserved for Caps LK LED)
28	NC (reserved for Num LK LED)
29	NC (reserved for Scroll LK LED)
30	GND

SSID = Touch.Pad

TouchPad Connector



0715 Modify:
Add R6908, R6909 for TPAD1 co-lay power option.



MB CONN.	(FFC)
Pin 4	TP_VDD
Pin 3	TPCLK
Pin 2	TPDATA
Pin 1	GND

SKEW	OPTION1	OPTION2	PIN	Feature	REMARK
DQ13	C12S		30		S is mean small
DN13	C12S	C12SB	30/25	Backlight	SB is mean small with backlight
DN15	C12S	C12SB	30/25	Backlight	
DQ15	C12SN		30	KB_DET#,CAP LED	SN is mean small with numpad

MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#

0901 X01 Modify:
Change KBLIT1 to 20.K0320.004 from
20.K0218.004 base on ME updated X01 DXF&EMN.
Re-assign KBLIT1 pin define sync with DQ15_NV.

0914 X01 Modify:
Add 2nd source 20.K0382.004 on KBLIT1
base on updated connector list.

0923 X01 Modify:
Change KBLIT1 part number to 20.K0589.004
and re-assign pin define base on Roy updated.

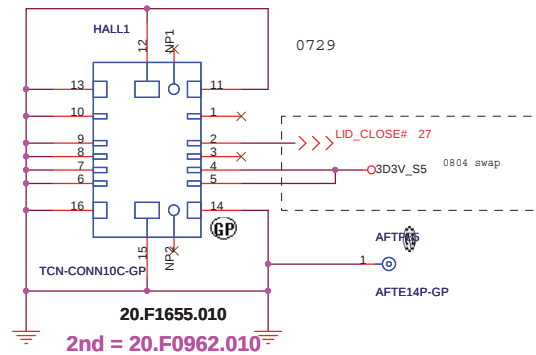
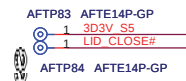
<Core Design>

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Title: **Key Board/Touch Pad**

Size A3 Document Number: **QUEEN 15** Rev: **A00**

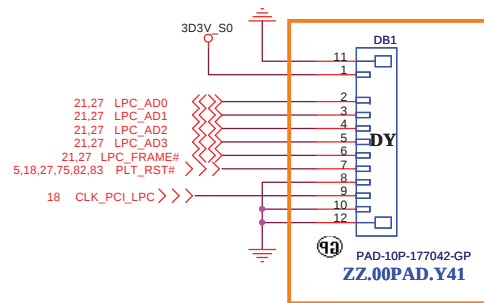
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1110 X02 Modify:
Add 2nd 20.F0962.010 on HALL1 from
ME updated connector list.

<Core Design>

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Hall Sensor			
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A00 1229 DB1 change to ZZ.00PAD.Y41(solder kmask type)
and keep un-stuffat X-Build stage

<Core Design>

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		Dubug connector	
Size A3	Document Number QUEEN 15	Rev A00	
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Title

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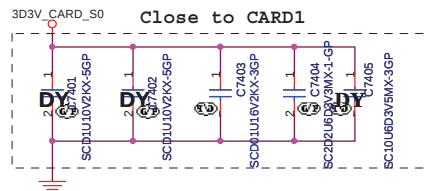
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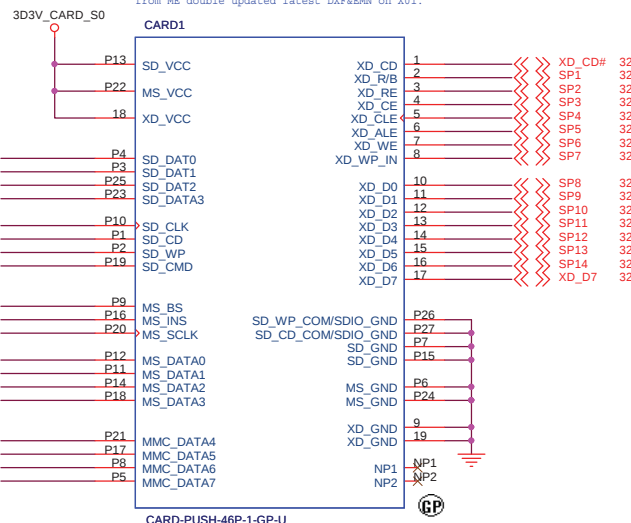
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SSID = SDIO



SD/XD/MS/MMC+ Card Reader

0906 X01 Modify:
Change CARD1 to 20.10129.001 from 62.10051.931
from MS double updated latest DXF&EMN on X01.

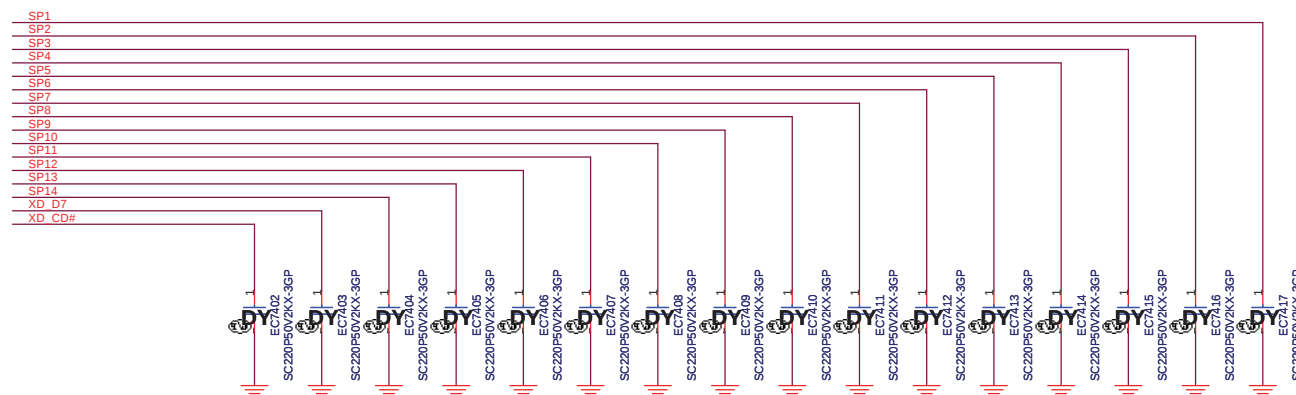


20.10129.001

2nd = 20.10135.001

1119 X02 Modify:
Add 2nd 20.10135.001 on HALL1 from
MS updated connector list.

For EMI Reserved



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20.10129.001			
Pin	TYPE	FUNCTION	RTS5138 NET
P1	SD	SD-CD	SP6
P2	SD	SD-WP	SP1
P3	SD	SD-DAT1	SP3
P4	SD	SD-DAT0	SP4
P5	MMC_PLUS	MMC-DATA7	SP5
P6	MemoryStick	MS-GND	GND
P7	SD	SD-GND	GND
P8	MMC_PLUS	MMC-DATA6	SP7
P9	MemoryStick	MS-BS	SP14
P10	SD	SD-CLK	SP8
P11	MemoryStick	MS-DATA1	SP12
P12	MemoryStick	MS-DATA0	SP9
P13	SD	SD-VCC	3D3V_CARD_S0
P14	MemoryStick	MS-DATA2	SP8
P15	SD	SD-GND	GND
P16	MemoryStick	MS-INS	SP2
P17	MMC_PLUS	MMC-DATA5	SP9
P18	MemoryStick	MS-DATA3	SP5
P19	SD	SD-CMD	SP10
P20	MemoryStick	MS-SCLK	SP1
P21	MMC_PLUS	MMC-DATA4	SP11
P22	MemoryStick	MS-VCC	3D3V_CARD_S0
P23	SD	SD-DATA3	SP12
P24	MemoryStick	MS-GND	GND
P25	SD	SD-DAT2	SP13
P26	SD	SD-WP COM /SDIO GND	GND
P27	SD	SD-CD COM /SDIO GND	GND
#1	XD	XD-CD	XD_CD#
#2	XD	XD-R/B	SP1
#3	XD	XD-RE	SP2
#4	XD	XD-CE	SP3
#5	XD	XD-CLE	SP4
#6	XD	XD-ALE	SP5
#7	XD	XD-WE	SP6
#8	XD	XD-WP-IN	SP7
#9	XD	XD-GND	GND
#10	XD	XD-D0	SP8
#11	XD	XD-D1	SP9
#12	XD	XD-D2	SP10
#13	XD	XD-D3	SP11
#14	XD	XD-D4	SP12
#15	XD	XD-D5	SP13
#16	XD	XD-D6	SP14
#17	XD	XD-D7	XD-D7
#18	XD	XD-VCC	3D3V_CARD_S0
#19	XD	XD-GND	GND

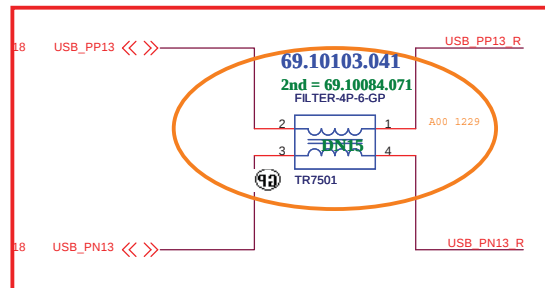
<Core Design>



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Title			
SD/XD/MS/MMC Card CONN			
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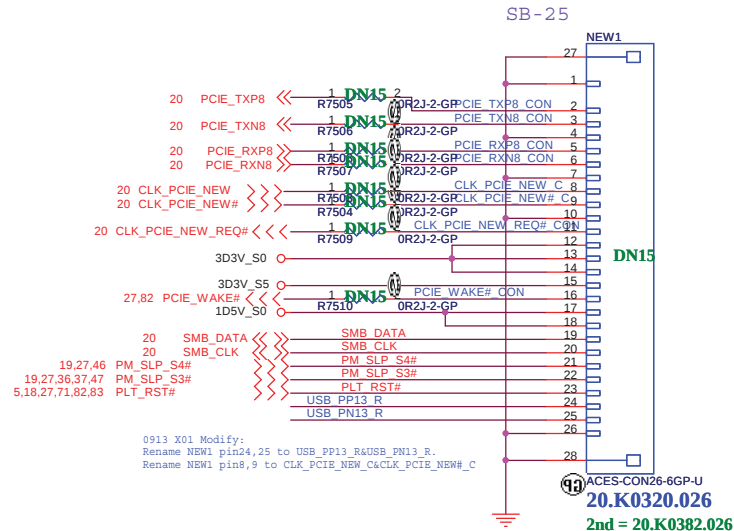
1122 X02 Modify:
Change TR7501 CN choke to 69.10103.041
and un-stuff R7501, R7502 from EMC Neo Suggestion.
Change R7501, R7502 to 0603 from 0402.



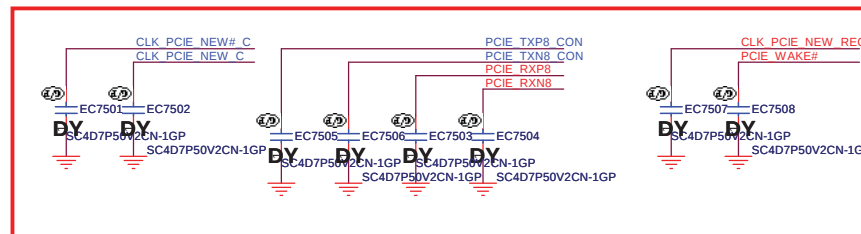
AFTE14P-GP AFTP107	1	3D3V S5
AFTE14P-GP AFTP108	1	3D3V S0
AFTE14P-GP AFTP109	1	1D5V S0
AFTE14P-GP AFTP110	1	USB PN13 R
AFTE14P-GP AFTP111	1	USB PP13 R
AFTE14P-GP AFTP112	1	CLK_PCIE_NEW_REQ# CON
AFTE14P-GP AFTP113	1	SMB_CLK
AFTE14P-GP AFTP114	1	SMB_DATA
AFTE14P-GP AFTP115	1	PM_SLP_S3#
AFTE14P-GP AFTP116	1	PM_SLP_S4#
AFTE14P-GP AFTP117	1	PLT_RST#
AFTE14P-GP AFTP118	1	CLK_PCIE_NEW# C
AFTE14P-GP AFTP119	1	CLK_PCIE_NEW C
AFTE14P-GP AFTP120	1	PCIE_TXN8 CON
AFTE14P-GP AFTP121	1	PCIE_TXP8 CON
AFTE14P-GP AFTP122	1	PCIE_RXN8 CON
AFTE14P-GP AFTP123	1	PCIE_RXP8 CON
AFTE14P-GP AFTP124	1	PCIE_WAKE# CON

1D5V_S0_CARD Max. 650mA, Average 500mA.
3D3V_S0_CARD Max. 1300mA, Average 1000mA
3D3V_S5_CARDAUX Max. 275mA

0824 X01 Modify:
Due to our NEW1 change to Express card to bottom side so re-assign NEW1 pin define same as DQ15-WY.
0906 X01 Modify:
Add 2nd source 20.K0382.026 on NEW1 base on updated connector list.



For EMI



0913 X01 Modify:
Add R7503, R7504 and reserved EC7501, EC7502 on CLK_PCIE_NEW & CLK_PCIE_NEW# for EMC suggestion.
0921 X01 Modify:
Add R7505-R7508 0ohm and reserved EC7503-EC7506 on PCIE_TXN8&PCIE_TXP8 signal base on EMC Lance suggestion.
Add R7509, R7510 0ohm and reserved EC7507, EC7508 on CLK_PCIE_NEW_REQ#&PCIE_WAKE# signal base on EMC Lance suggestion.

<Core Design>

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Title: Express Card			
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<Core Design>



Wistron Corporation
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Title

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<Core Design>



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Title

Reserved

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A3

Document Number
QUEEN 15

Date: Tuesday, January 04, 2011

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A00

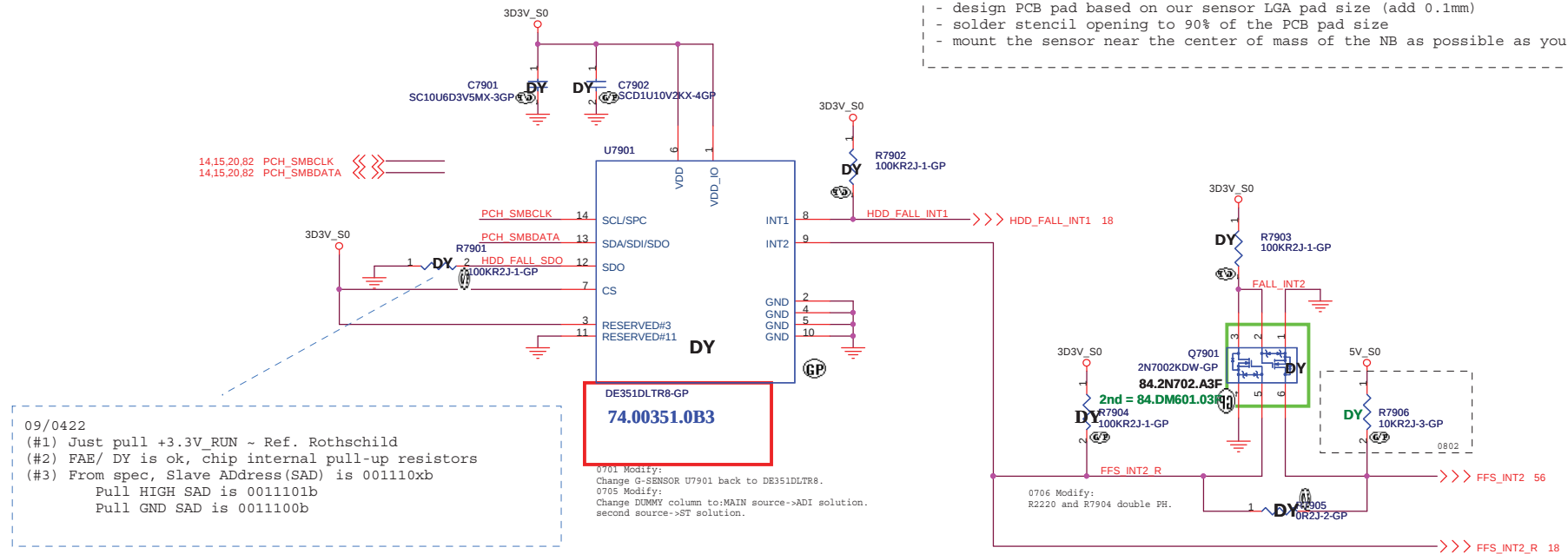
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```
SSID = User.Interface
```

Free Fall Sensor

| Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

<Core Design>



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Free Fall Sensor

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<Core Design>



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Title

Reserved

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<Core Design>

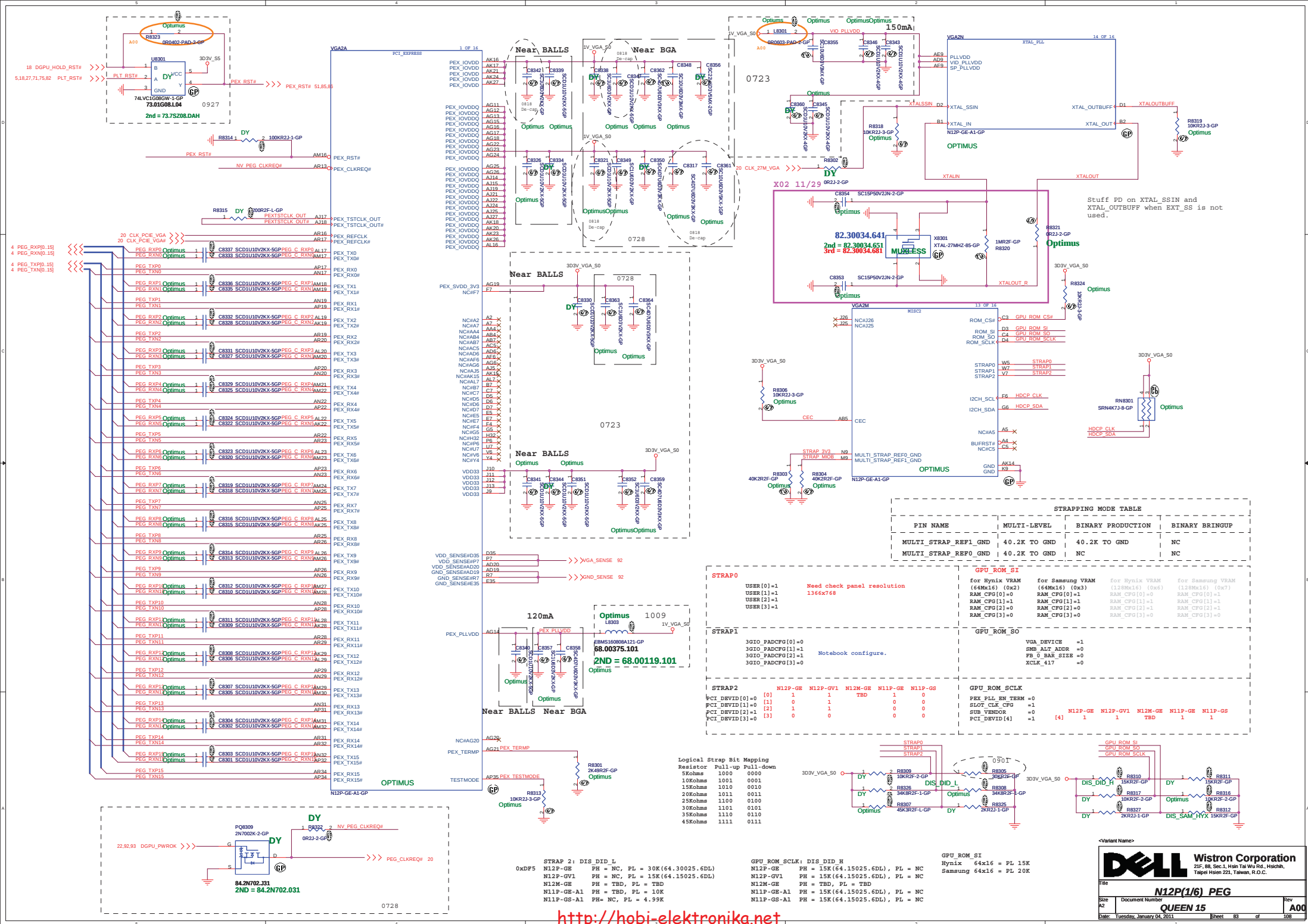


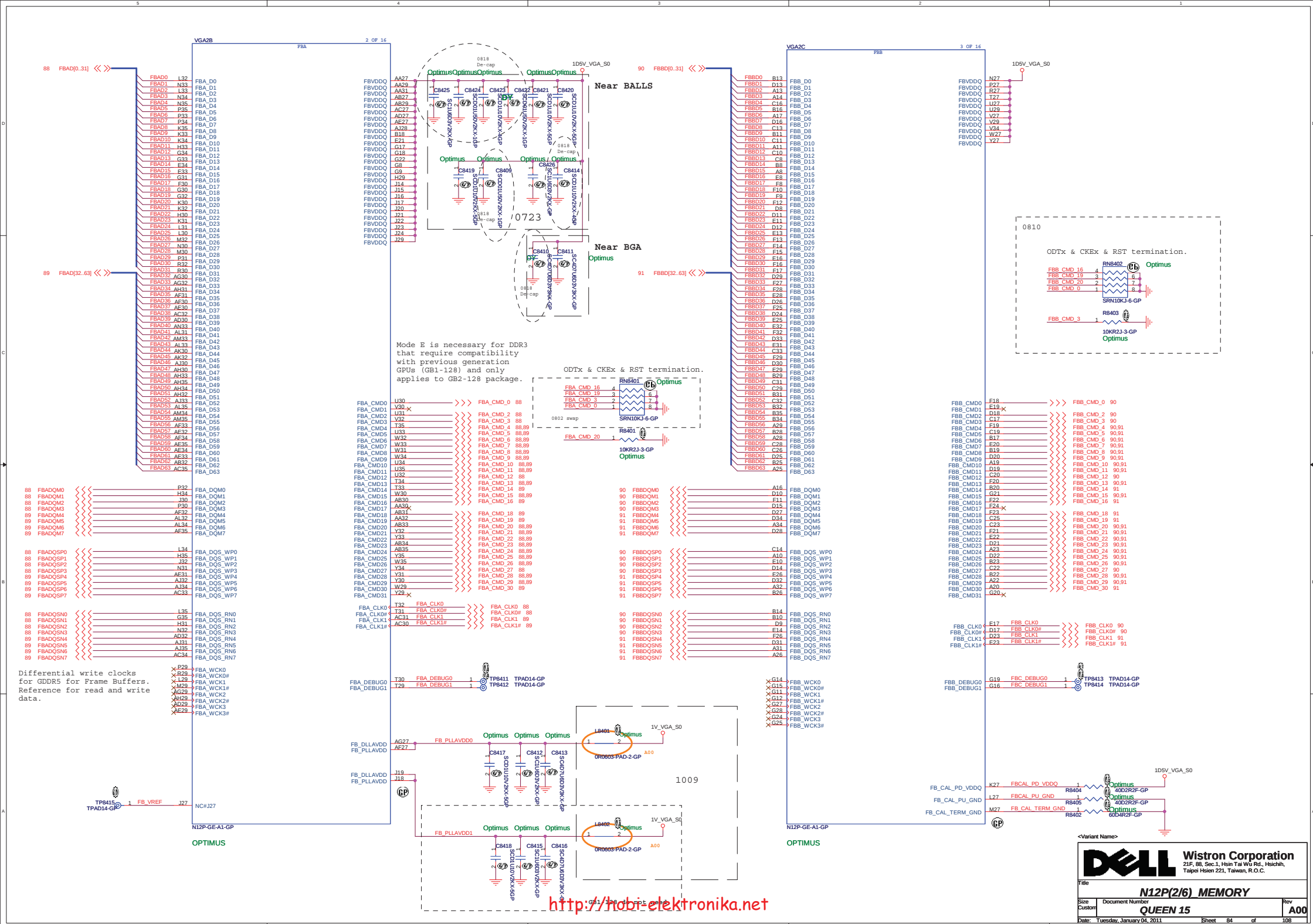
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

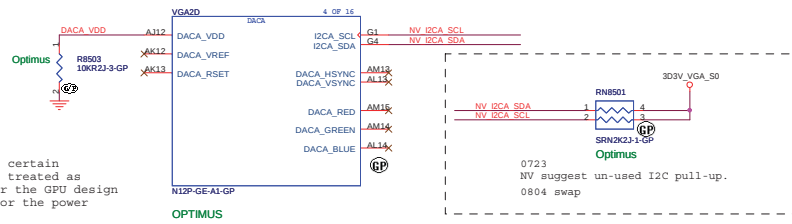
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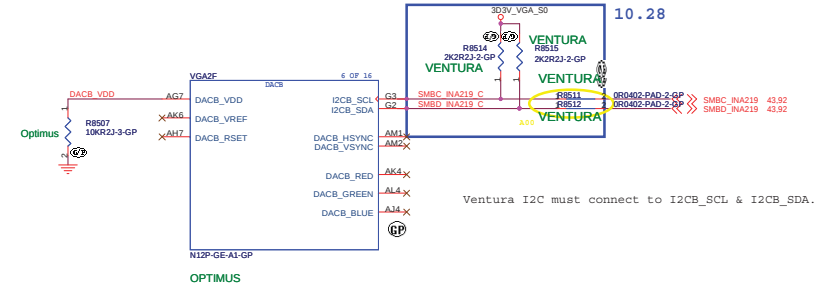


If a DAC interface is not required, it should be disabled by:
 1. Adding a pull-down to the DACx_VDD with a 10 kilohm resistor to GND.
 2. All other DAC I/O pins can be left floating.

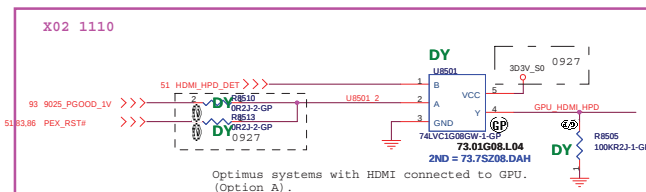
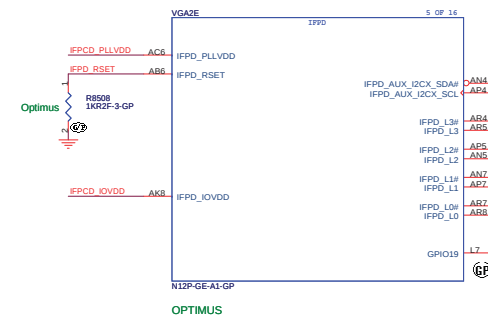
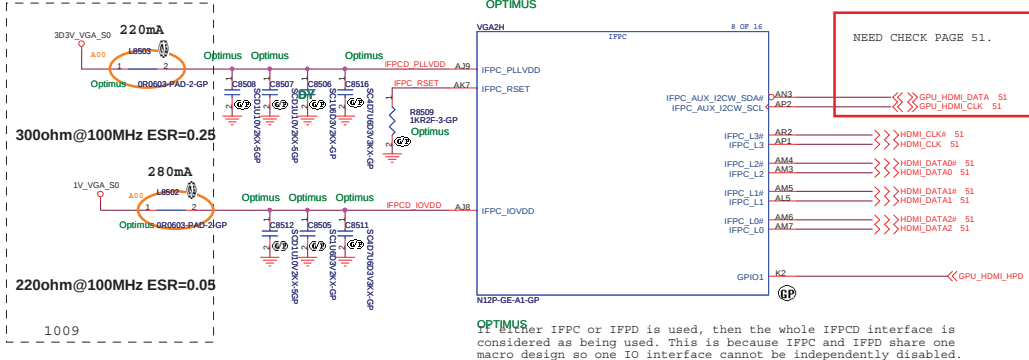
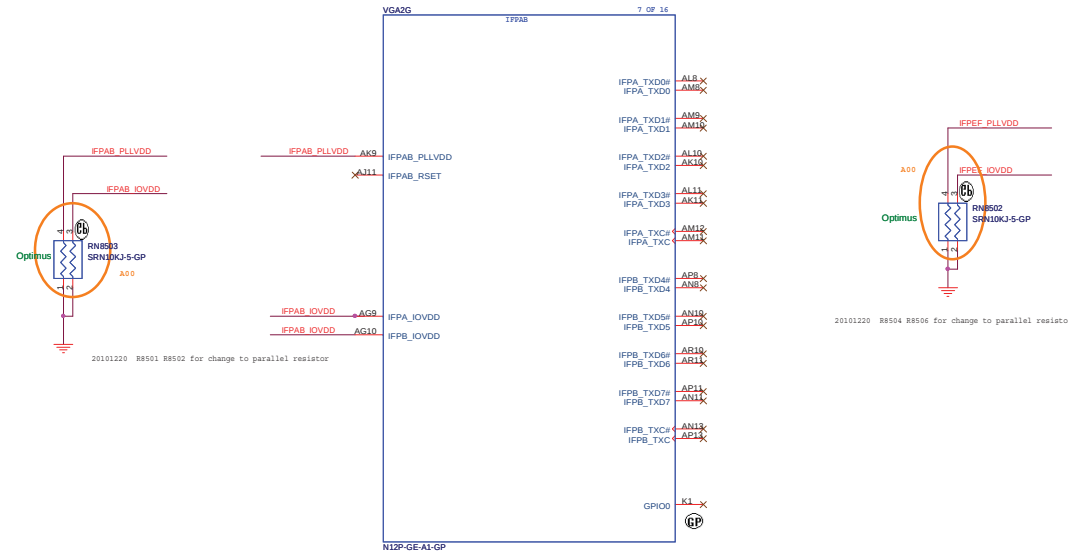


In Optimus mode the GPU does not drive certain interfaces. These interfaces should be treated as unused and appropriate terminations per the GPU design guide should be applied to the signal or the power supply block.

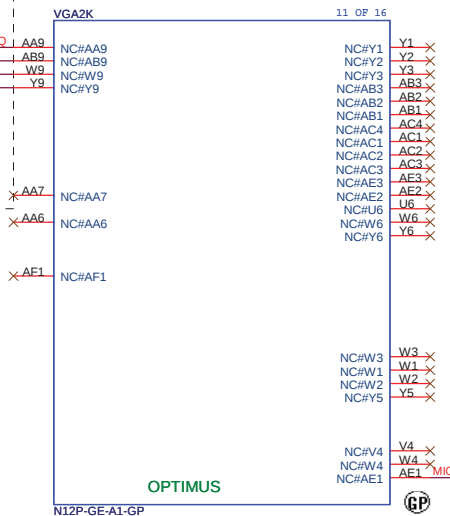
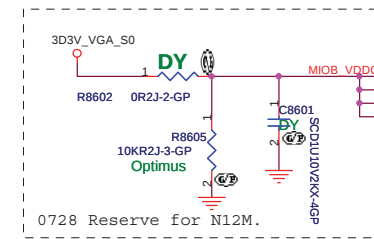
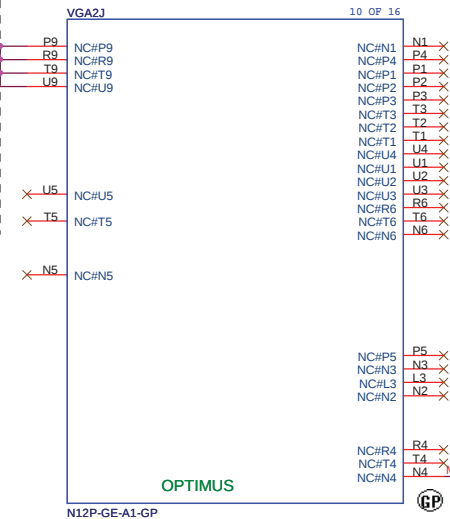
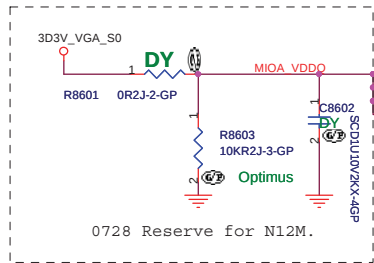
The following guidelines only apply to a fully unused IFP macro:
 1. Pull down IFPxy_IOVDD with 10 kilohm resistor.
 2. Pull down IFPxy_PLLVDD with 10 kilohm resistor.
 3. The other IO pins can be NC; this includes unused data lines.



Ventura I2C must connect to I2CB_SCL & I2CB_SDA.



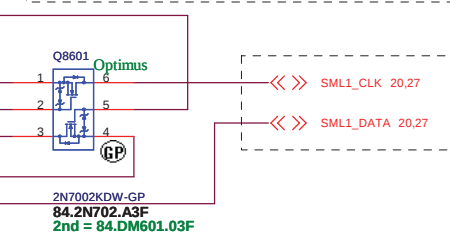
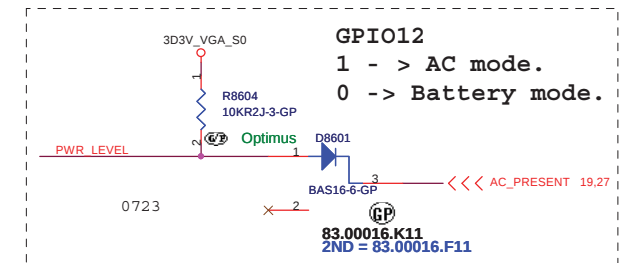
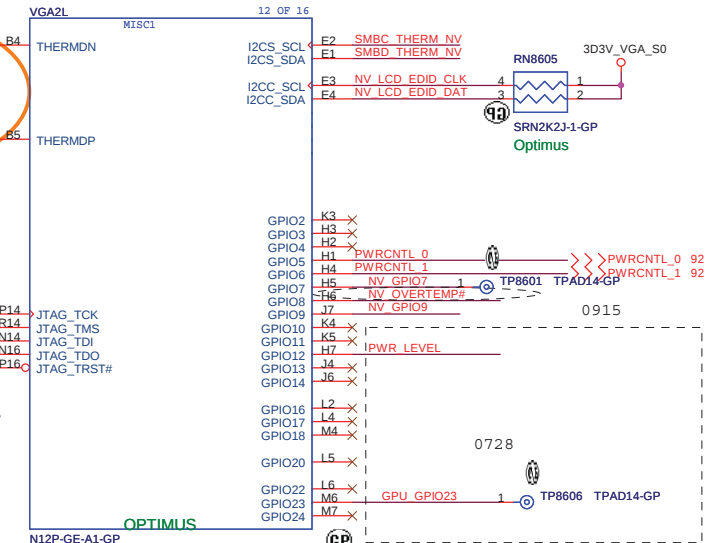
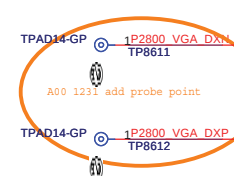
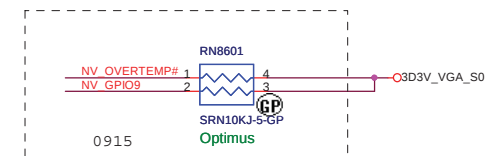
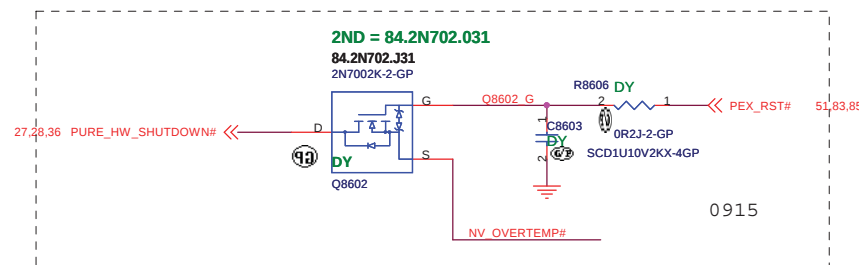
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MIOA/B Support

Package	MIOA	MIOB
GB1-192	15-bit, available	TBD
GB2-128	Not available	Not available

MIOx_CLKIN signals should have 10K pull-down resistors.



Frame Buffer Partition A Lower 32 bits.

2nd = 72.41164.IOU
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMY-BGA96D075133B48) from BGA96D0913H48

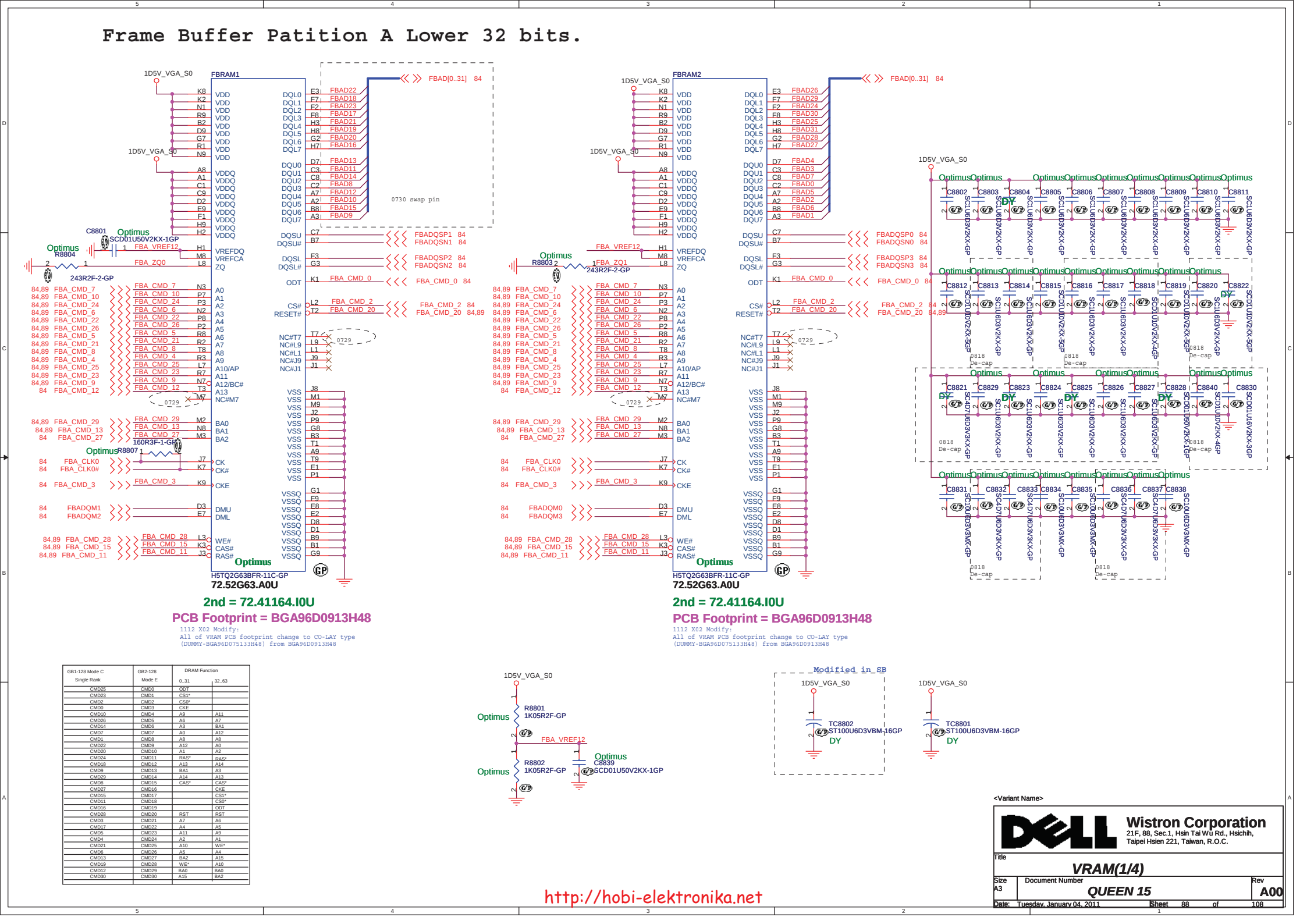
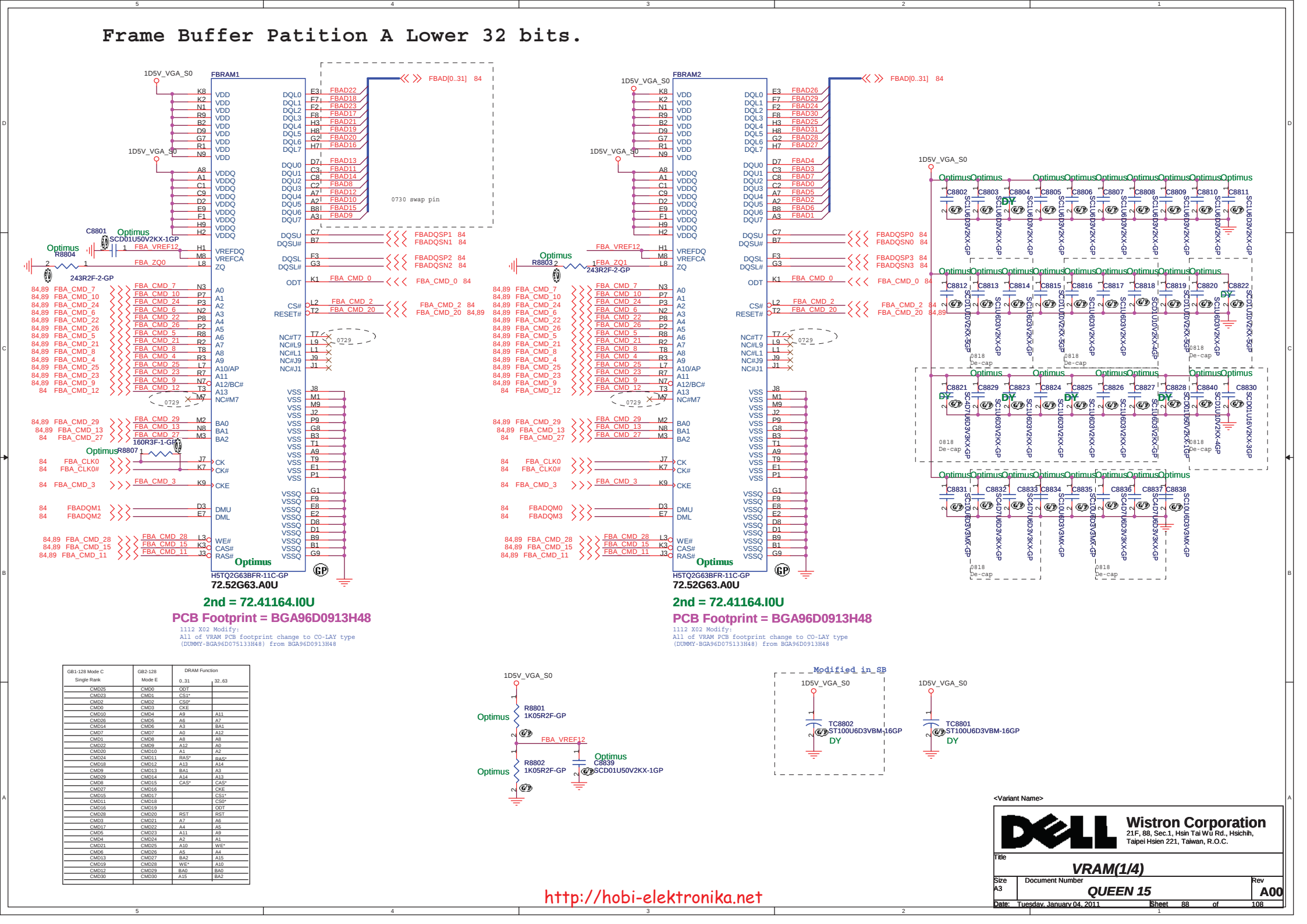
GBl-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function	32.63
CMD05	CMD00	ODT*	
CMD29	CMD01	CS1*	A11
CMD01	CMD02	OSP*	A7
CMD00	CMD03	CKE	BA1
CMD10	CMD04	A9	A12
CMD08	CMD05	A8	A0
CMD14	CMD06	A3	A2
CMD07	CMD07	A0	A3
CMD01	CMD08	A8	A10
CMD22	CMD09	A12	A1
CMD00	CMD10	A1	A2
CMD04	CMD11	RAS*	BAB*
CMD18	CMD12	A13	A14
CMD09	CMD13	BA1	A3
CMD09	CMD14	A1A	A13
CMD09	CMD15	CAS*	CAS*
CMD27	CMD16	CKE	
CMD15	CMD17	CS1*	
CMD11	CMD18	CS0*	
CMD16	CMD19	ODT	
CMD28	CMD20	RST	RST
CMD01	CMD21	A7	A6
CMD17	CMD22	A4	A5
CMD05	CMD23	A11	A9
CMD04	CMD24	A2	A1
CMD21	CMD25	A10	WE*
CMD06	CMD26	A5	A4
CMD13	CMD27	BA2	A13
CMD19	CMD28	WE*	A10
CMD12	CMD29	BA0	BA0
CMD09	CMD30	A15	BA2

<Variant Name>

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Title	VRAM(1/4)		
Size	Document Number		
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Frame Buffer Partition A Lower 32 bits.

Optimus
H5TQ2G63BFR-11C-GP
72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMY-BGA96D075133B48) from BGA96D0913H48

GBl-128 Mode C Single Rank	GBl-128 Mode E	DRAM Function	32.63
CMD25	CMD0	ODT	
CMD29	CMD1	CS1*	A11
CMD3	CMD2	CS0*	A11
CMD0	CMD3	CKE	
CMD10	CMD4	A9	A11
CMD8	CMD5	A8	A11
CMD14	CMD6	A3	BA1
CMD7	CMD7	A0	A12
CMD1	CMD8	A8	A8
CMD22	CMD9	A12	A0
CMD20	CMD10	A1	A2
CMD24	CMD11	BA0*	A12
CMD18	CMD12	A13	A13
CMD9	CMD13	BA1	A3
CMD29	CMD14	A14	A13
CMD5	CMD15	CAS*	CAS*
CMD27	CMD16	CKE	
CMD15	CMD17	CS1*	
CMD11	CMD18	CS0*	
CMD16	CMD19	ODT	
CMD28	CMD20	RST	RST
CMD1	CMD21	A7	A6
CMD17	CMD22	A4	A5
CMD5	CMD23	A11	A9
CMD4	CMD24	A2	A1
CMD21	CMD25	A10	WE*
CMD6	CMD26	A5	A4
CMD13	CMD27	BA2	A13
CMD19	CMD28	WE*	A10
CMD12	CMD29	BA0	BA0
CMD30	CMD30	A15	BA2

Modified in GB

1D5V_VGA_S0

Optimus R8801 1K05R2F-GP

FBA VREF12

Optimus R8802 1K05R2F-GP

Optimus C8839 SCDD01U50V2KX-1GP

TC8802 ST100U6D3VBW-16GP DY

TC8801 ST100U6D3VBW-16GP DY

<Variant Name>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinshih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **VRAM(1/4)**

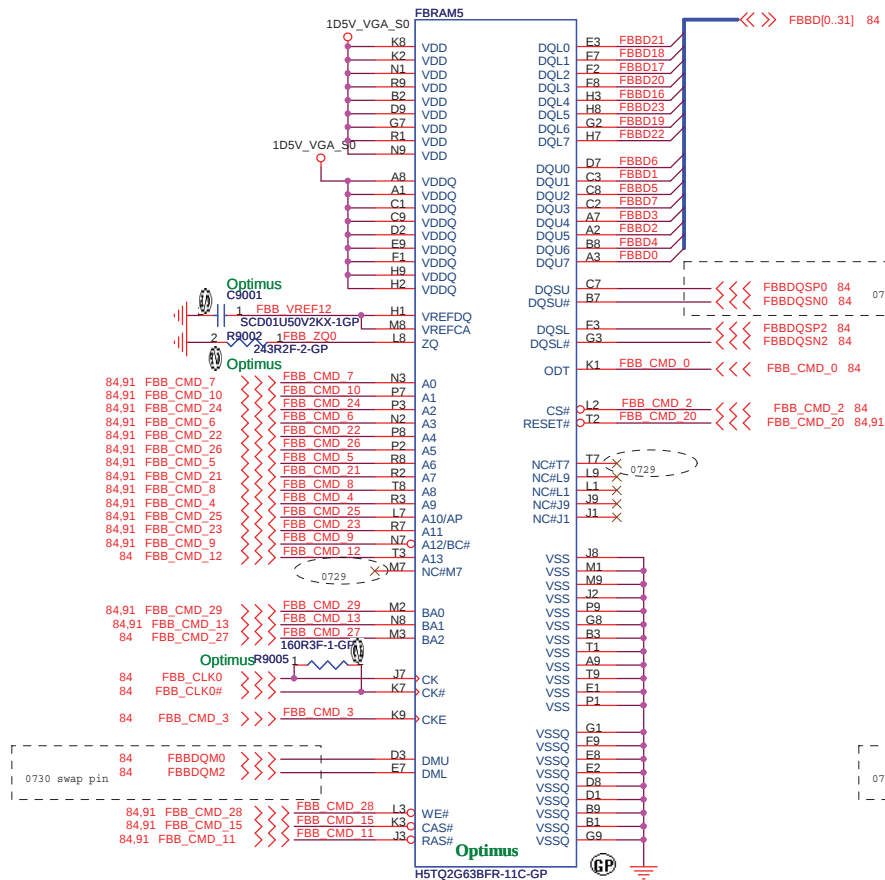
Size A3 Document Number **QUEEN 15** Rev **A00**

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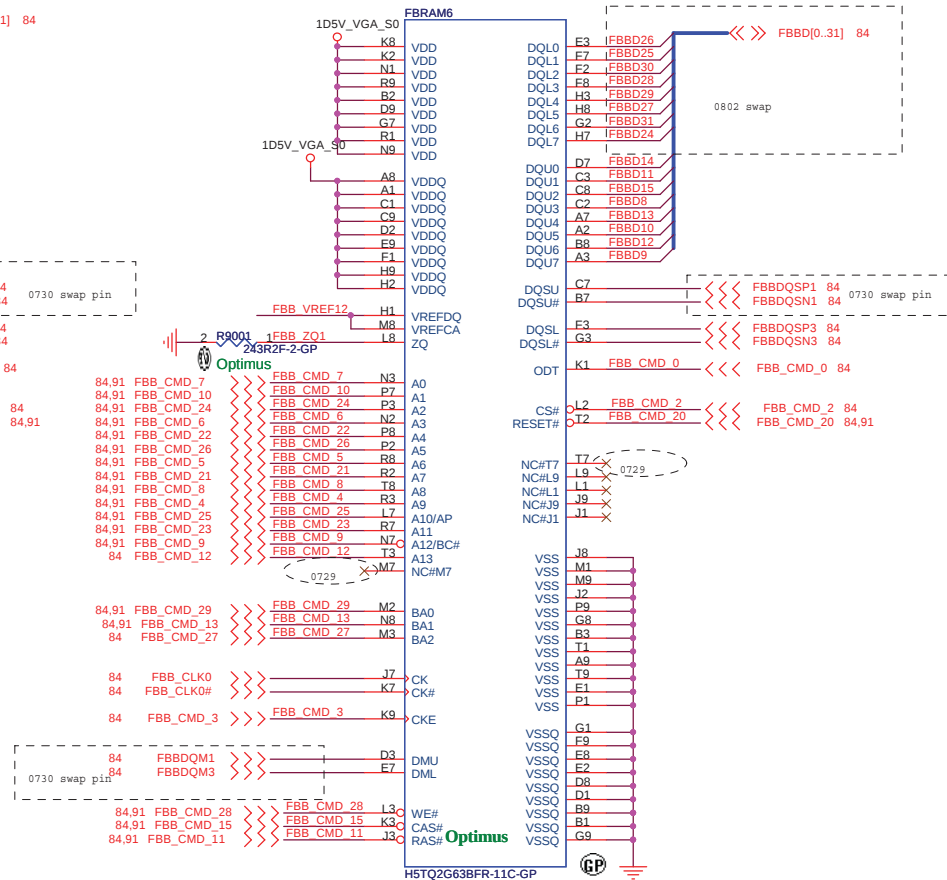
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Frame Buffer Partition B Lower 32 bits.



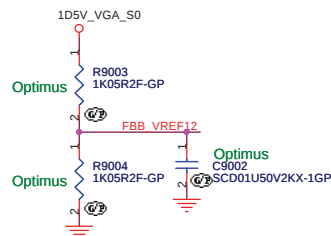
72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(D0UMWY-BGA96D075133B48) from BGA96D0913H48



72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(D0UMWY-BGA96D075133B48) from BGA96D0913H48

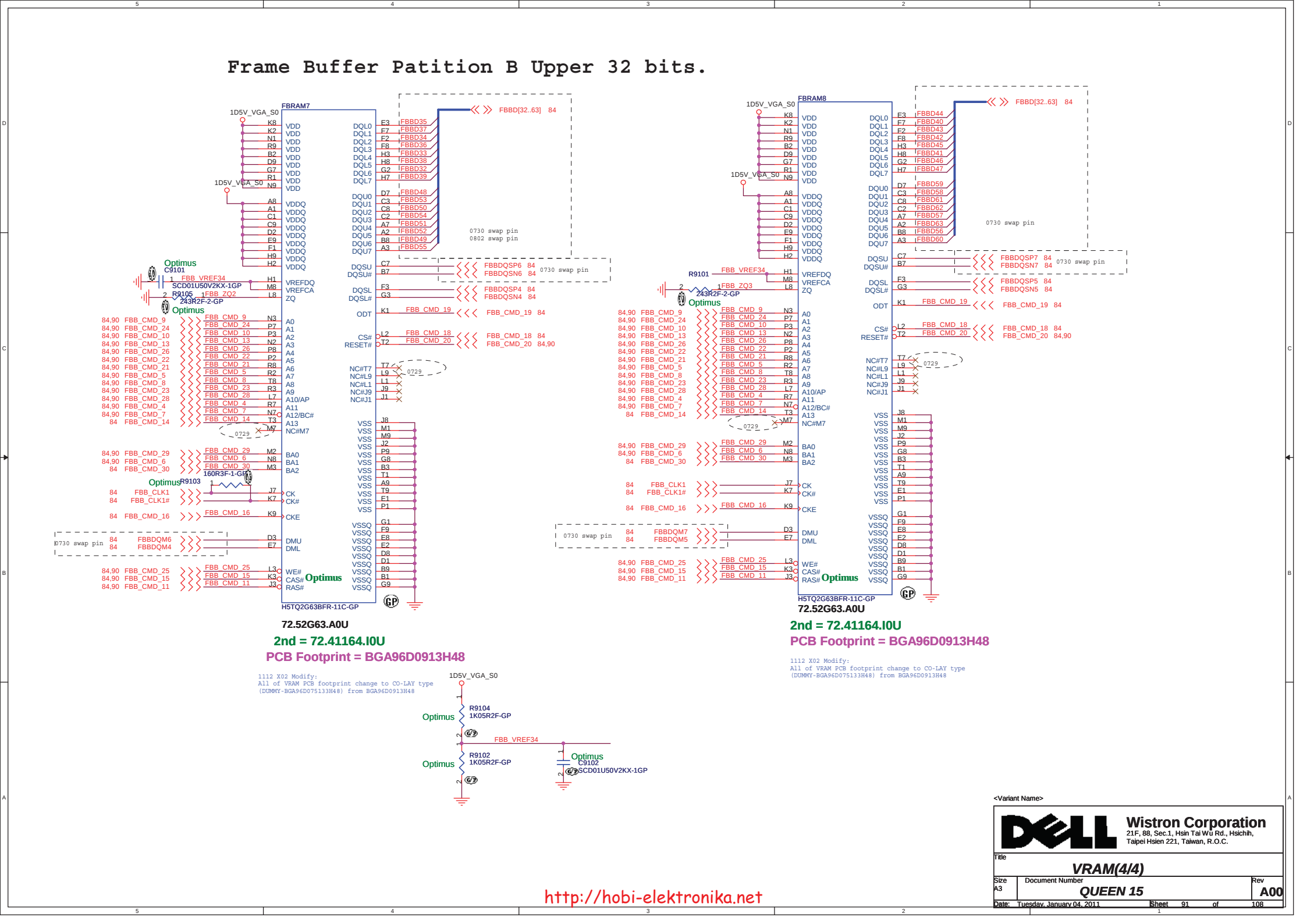


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<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
VRAM(3/4)					
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Frame Buffer Partition B Upper 32 bits.

[illegible][illegible][illegible]

Frame Buffer Partition B Upper 32 bits.

72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
 All of VRAM PCB footprint change to CO-LAY type
 (DUMMT-BGA96D075133H48) from BGA96D0913H48

1112 X02 Modify:
 All of VRAM PCB footprint change to CO-LAY type
 (DUMMT-BGA96D075133H48) from BGA96D0913H48

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<Variant Name>

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Title: **VRAM(4/4)**

Size A3 Document Number: **QUEEN 15** Rev: **A00**

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Frame Buffer Partition B Upper 32 bits.

Frame Buffer Partition B Upper 32 bits.

72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMT-BGA96D075133H48) from BGA96D0913H48

72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMT-BGA96D075133H48) from BGA96D0913H48

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<Variant Name>

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Title		VRAM(4/4)	
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Frame Buffer Partition B Upper 32 bits.

Frame Buffer Partition B Upper 32 bits.

[illegible]

Frame Buffer Partition B Upper 32 bits.

72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMT-BGA96D075133H48) from BGA96D0913H48

72.52G63.A0U
2nd = 72.41164.I0U
PCB Footprint = BGA96D0913H48

1112 X02 Modify:
All of VRAM PCB footprint change to CO-LAY type
(DUMMT-BGA96D075133H48) from BGA96D0913H48

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<Variant Name>

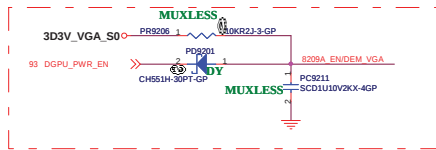
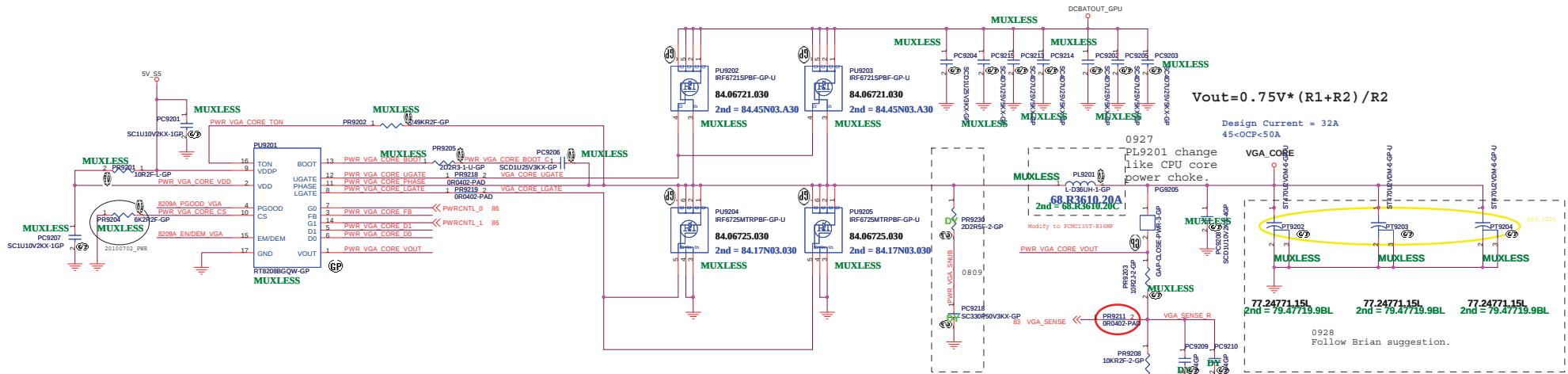
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM(4/4)		
Size A3	Document Number	Rev	
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Frame Buffer Partition B Upper 32 bits.

Frame Buffer Partition B Upper 32 bits.

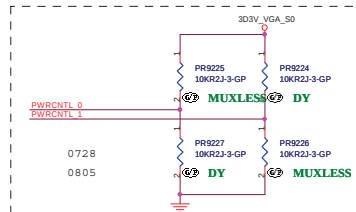
SSID = PWR.Plane.Regulator_GFX



RT8208B

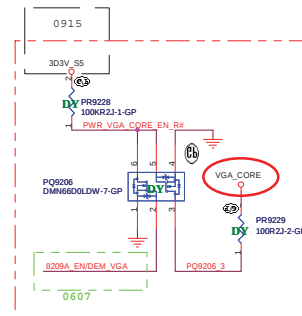
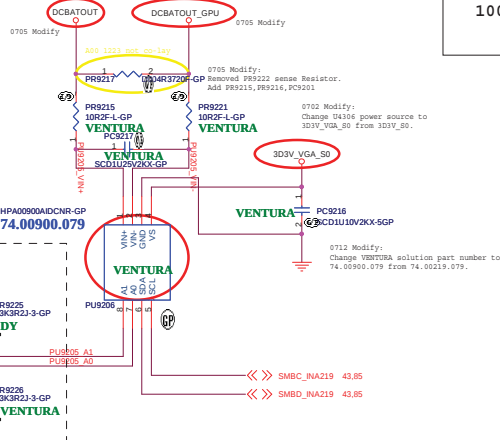
P-State	PWRCNTL_1 (GPIO6)	PWRCNTL_0 (GPIO5)	VGA_CORE_PWR
P0 (Cold)	L	L	0.975V
P0 (Hot)	L	H	0.954V (default boot up)
ES	H	L	0.878V
P8 & P12	H	H	0.853V

0923 update table



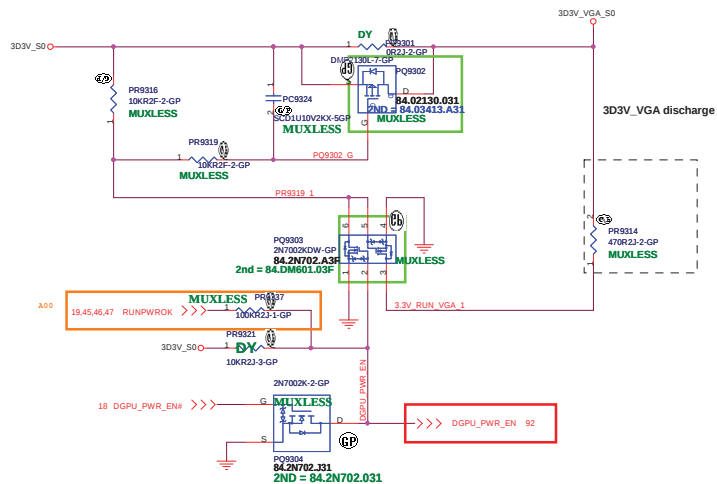
Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

FOR NVIDIA VENTURA



JV10-CS

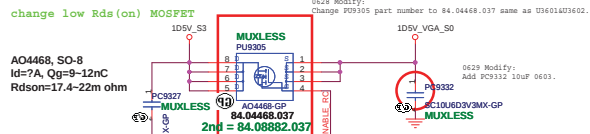
3D3V_S0 to 3D3V_VGA_S0 Transfer



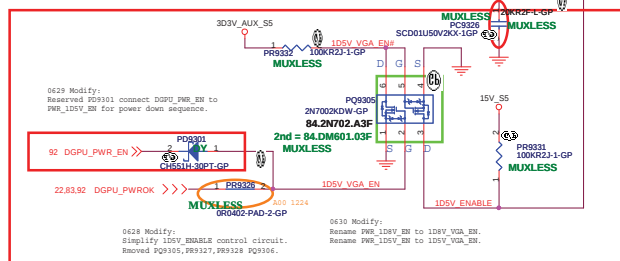
	DGPU_PWR_EN#
dGPU mode	L
IGPU	H
IGPU with BACO	L

NV do not need 1.8V

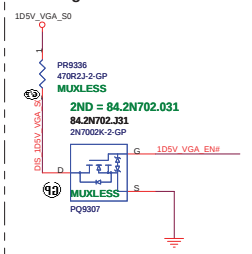
1D5V_VGA_S0



Park Madison Does Not Support BACO, So follow Old Sequence
Seymour Whistler Robson Support BACO, So Change Sequence



Discharge Circuit

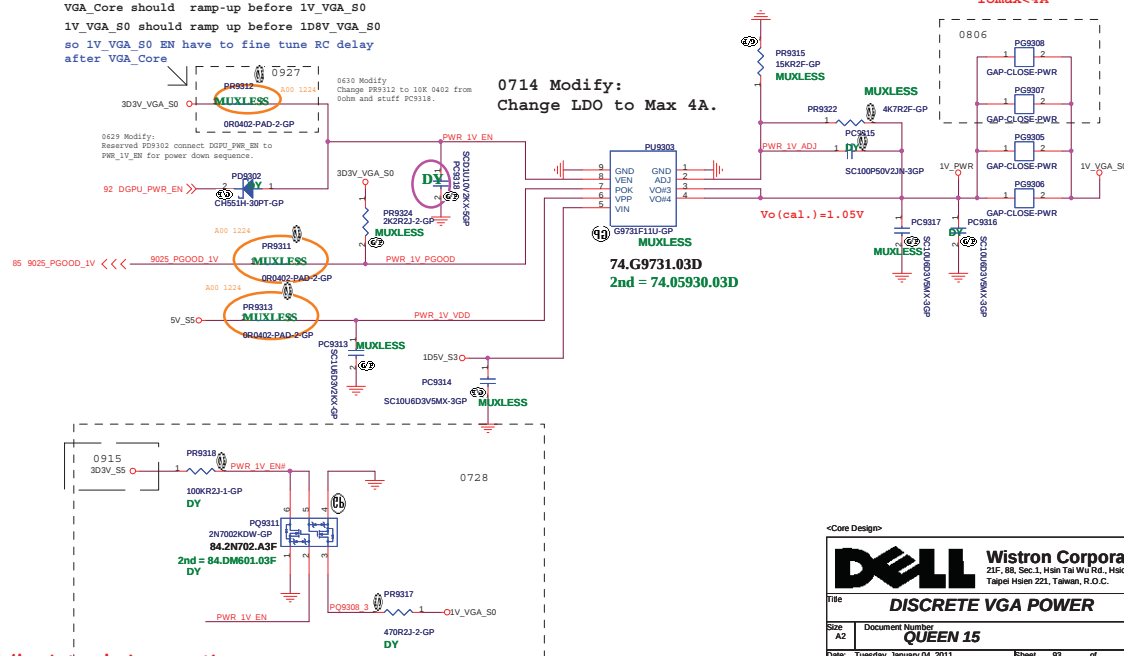


G9731F11U-GP for 1V_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0
so 1V_VGA_S0 EN have to fine tune RC delay
after VGA_Core

$$V_{out} = 0.8 \times \frac{\text{high-side } R + \text{low-side } R}{\text{low-side } R}$$

0714 Modify:
Change LDO to Max 4A.



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<Core Design>

Wistron Corporation 21F, 6th, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.		
DISCRETE VGA POWER		
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<Variant Name>		
		
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
LVDS Switch		
Size A3	Document Number QUEEN 15	Rev A00
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<Variant Name>



Wistron Corporation
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Title

CRT Switch

Size
A3

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SSID = SDIO

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<Variant Name>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

TOUCH PANEL

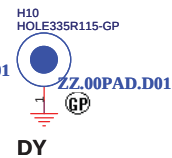
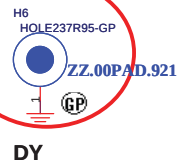
Size
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Document Number
QUEEN 15

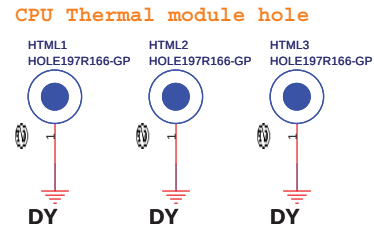
Rev
A00

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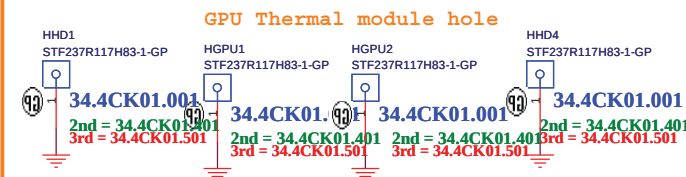
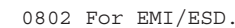
0624 Modify:
Removed AFTP1,AFTP7~AFTP13.



0721 Modify:
Removed SPR1



The schematic diagram illustrates the electrical connections for a power supply unit. It features a central power transformer with multiple secondary windings. The primary winding is connected to a 230V AC source. The secondary windings provide various output voltages: 5V, 3.3V, 1.8V, 1.2V, 0.9V, 0.6V, 0.3V, 0.1V, and 0.05V. These outputs are connected to a network of capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100) and inductors (L1, L2, L3, L4, L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L21, L22, L23, L24, L25, L26, L27, L28, L29, L30, L31, L32, L33, L34, L35, L36, L37, L38, L39, L40, L41, L42, L43, L44, L45, L46, L47, L48, L49, L50, L51, L52, L53, L54, L55, L56, L57, L58, L59, L60, L61, L62, L63, L64, L65, L66, L67, L68, L69, L70, L71, L72, L73, L74, L75, L76, L77, L78, L79, L80, L81, L82, L83, L84, L85, L86, L87, L88, L89, L90, L91, L92, L93, L94, L95, L96, L97, L98, L99, L100). The components are connected to a common ground plane. The diagram also shows the connection of the power supply to a DC output terminal block. The output voltages are labeled as 5V, 3.3V, 1.8V, 1.2V, 0.9V, 0.6V, 0.3V, 0.1V, and 0.05V. The diagram is a detailed representation of the power supply's internal circuitry, showing the flow of current from the AC input through the transformer and various filtering components to the DC output.



HBT1
STF237R117H123-GP
DY
34.4DM11.001
2nd = 34.4A902.001
0818

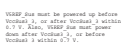
DELL **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title UNUSED PARTS/EMI Capacitors			
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(AC mode)

(DC mode)

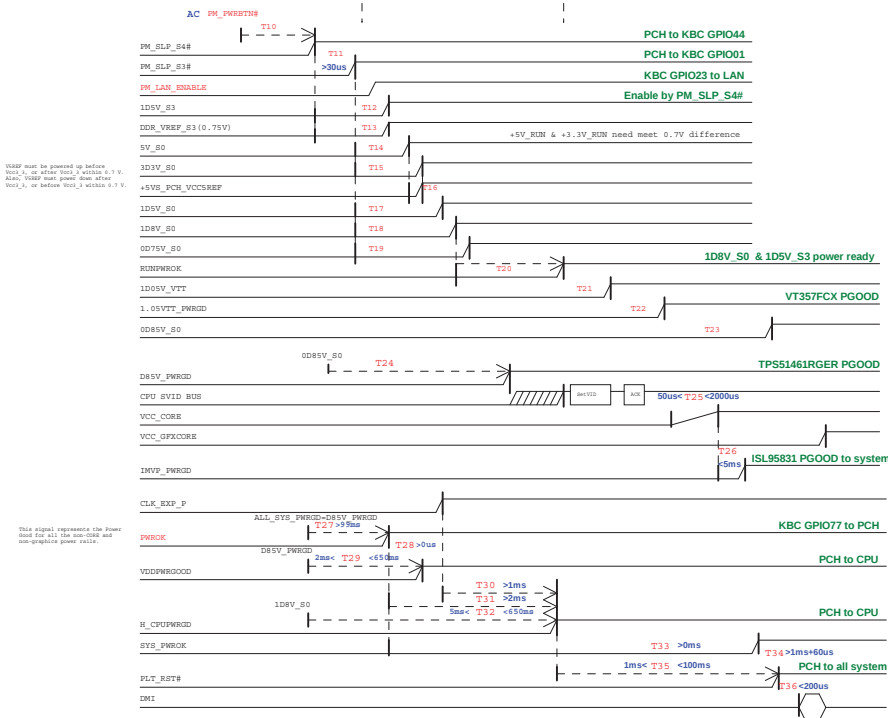
Within logic high level and disable 1
it is less than the logic low level.



Not floating.

Sense the power button status

This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.



This signal represents the Power Good for all the non-CORE and non-graphics power rails.

Timing diagram for VGA Core power-up sequence. The diagram shows the relationship between several signals:

- DGPU_PWR_ENH (Discrete only)**: A pulse that occurs before the power rails are enabled.
- 3D3V_VGA_S0 (VDE33)**: A signal that transitions from low to high.
- #209A_EN/DEM_VGA (Discrete only)**: A signal that transitions from low to high.
- VGA_CORE (#VVD)**: A signal that transitions from low to high. The timing constraint $t_{\#VVD} > 0ms$ is indicated.
- DGPU_PWROK (Discrete only)**: A signal that transitions from low to high.
- 1D5V_VGA_S0 (#FVSDQ)**: A signal that transitions from low to high. The timing constraint $t_{\#V - FVSDQ} > 0ms$ is indicated.
- PCH GPMU54 output**: A signal that transitions from low to high.

Additional timing constraints and labels:

- RT8208 PGOD**: A signal that transitions from low to high.
- VGA_CORE.1V_VGA_S0** and **1D5V_VGA_S0_3D3V_VGA_S0**: Signals that transition from low to high.
- First rail to power down**: A label for the first rail to power down.
- Last rail to power down**: A label for the last rail to power down.
- tPOWER-OFF < 10ms**: A timing constraint for the power-off time.

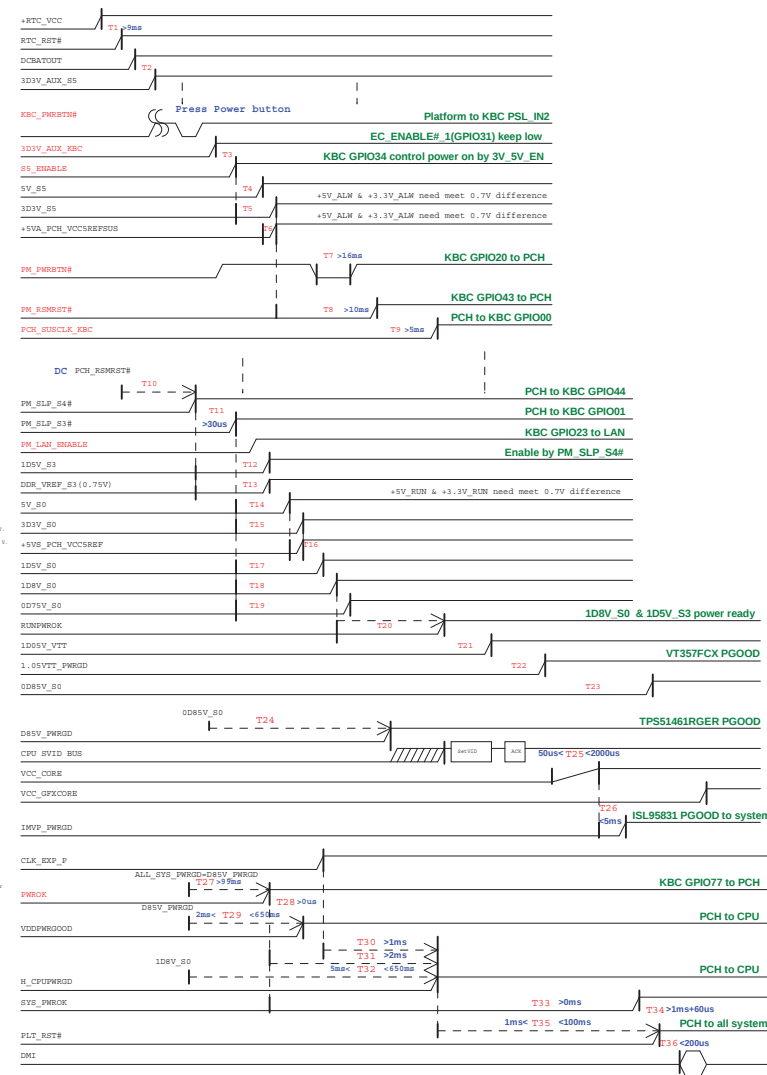
For power-down, reversing the ramp-up sequence is recommended.



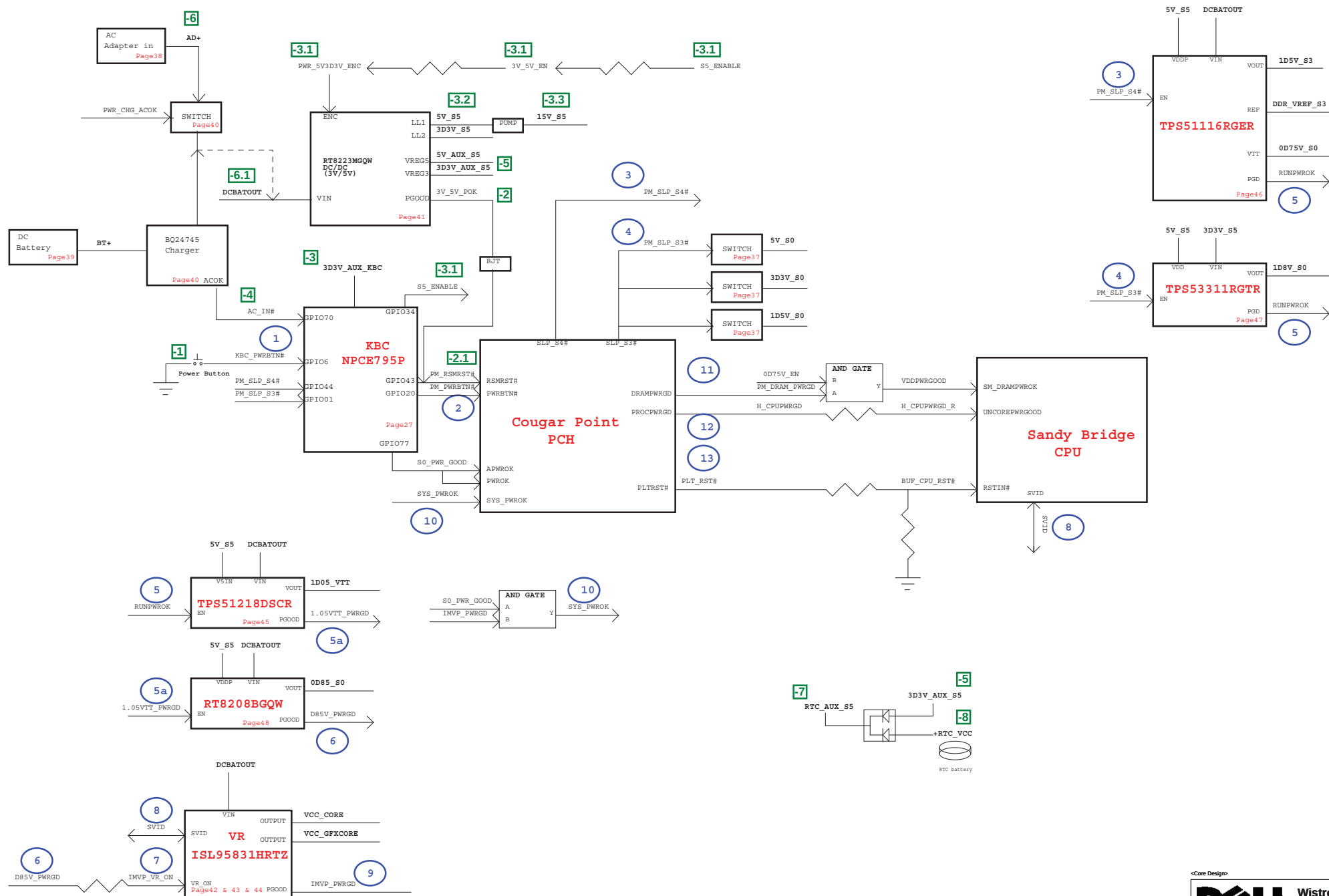
VREF Bus must be powered up before VccBus1_1, or after VccBus1_1 within 0.7 V. Also, VREF Bus must power down after VccBus1_1, or before VccBus1_1 within 0.7 V.

VSG2P must be powered up before Voc1 2, or after Voc1 2 within 0.2 V. Also, VSG2P must power down after Voc1 2, or before Voc1 2 within 0.2 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.

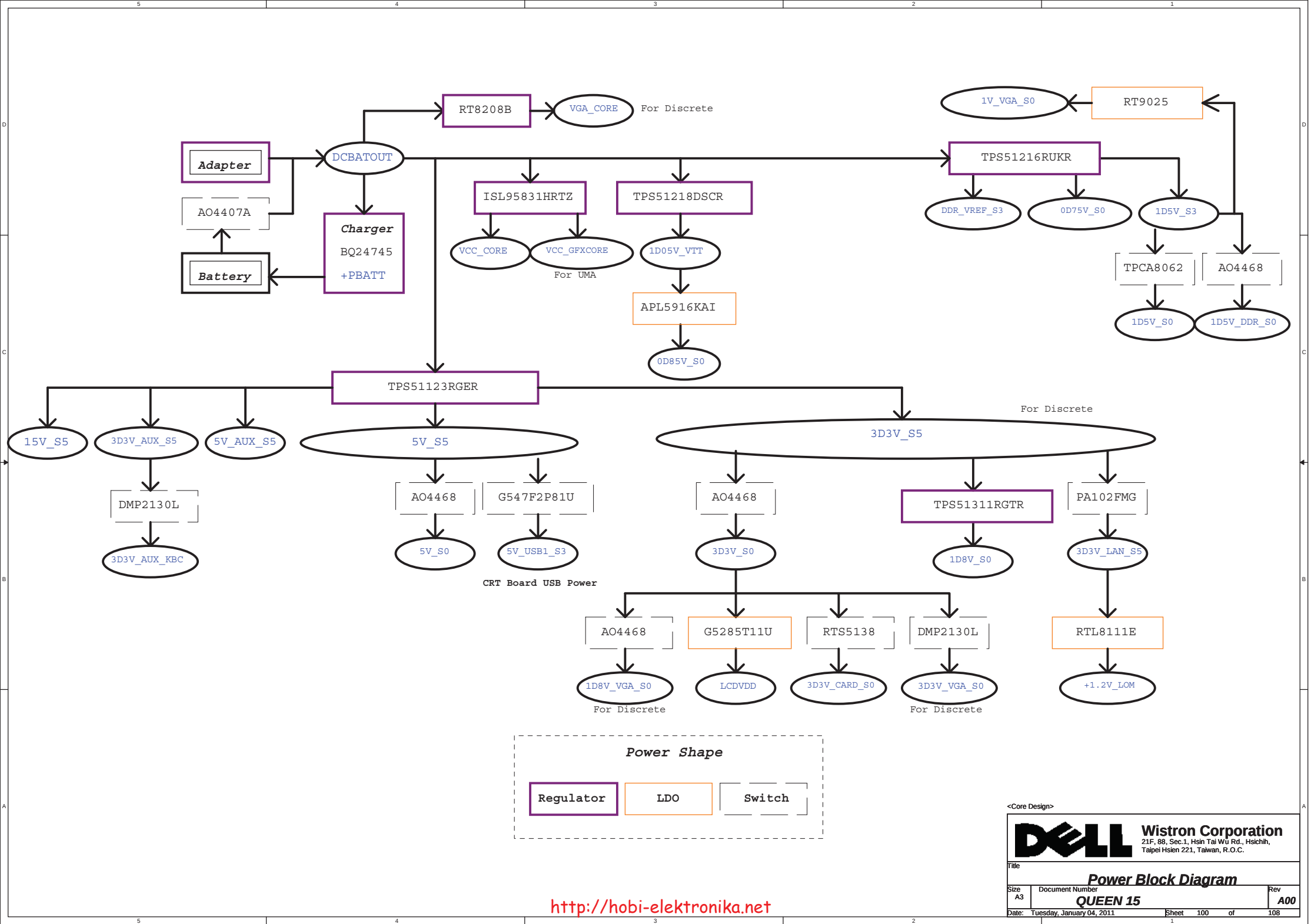


Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM

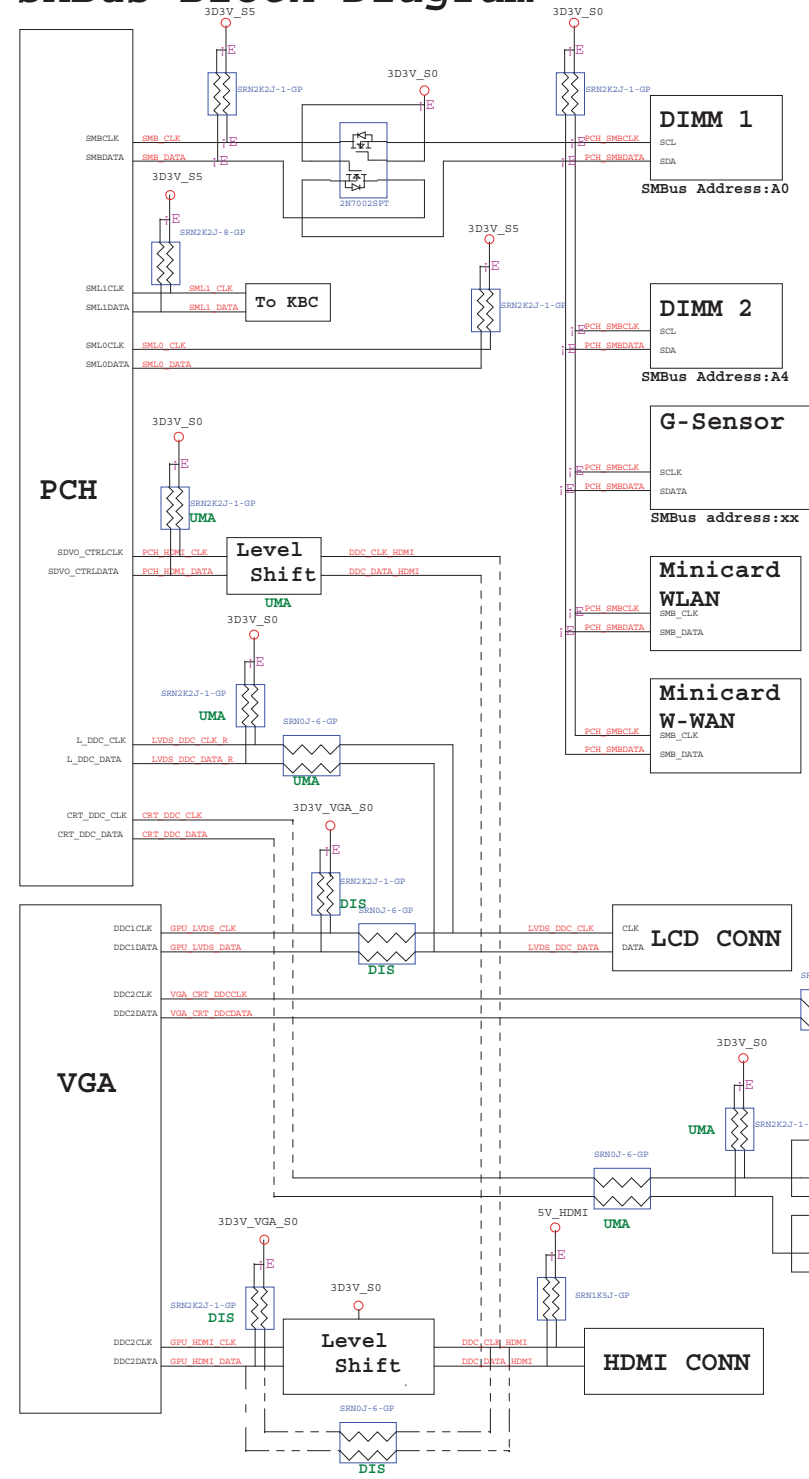


Power Up Sequence: -8 ~ 13

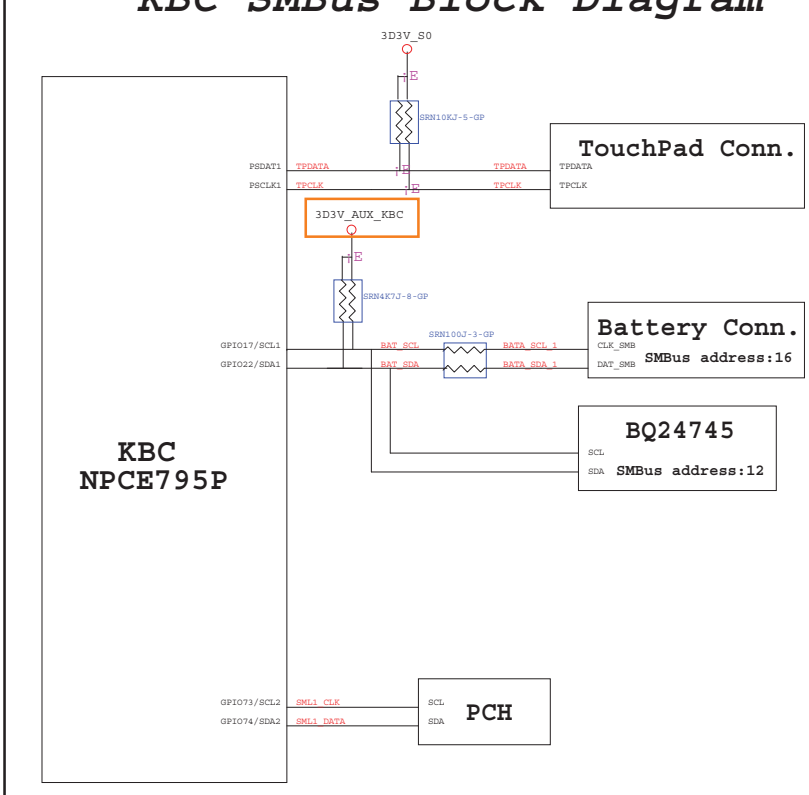
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PCH SMBus Block Diagram

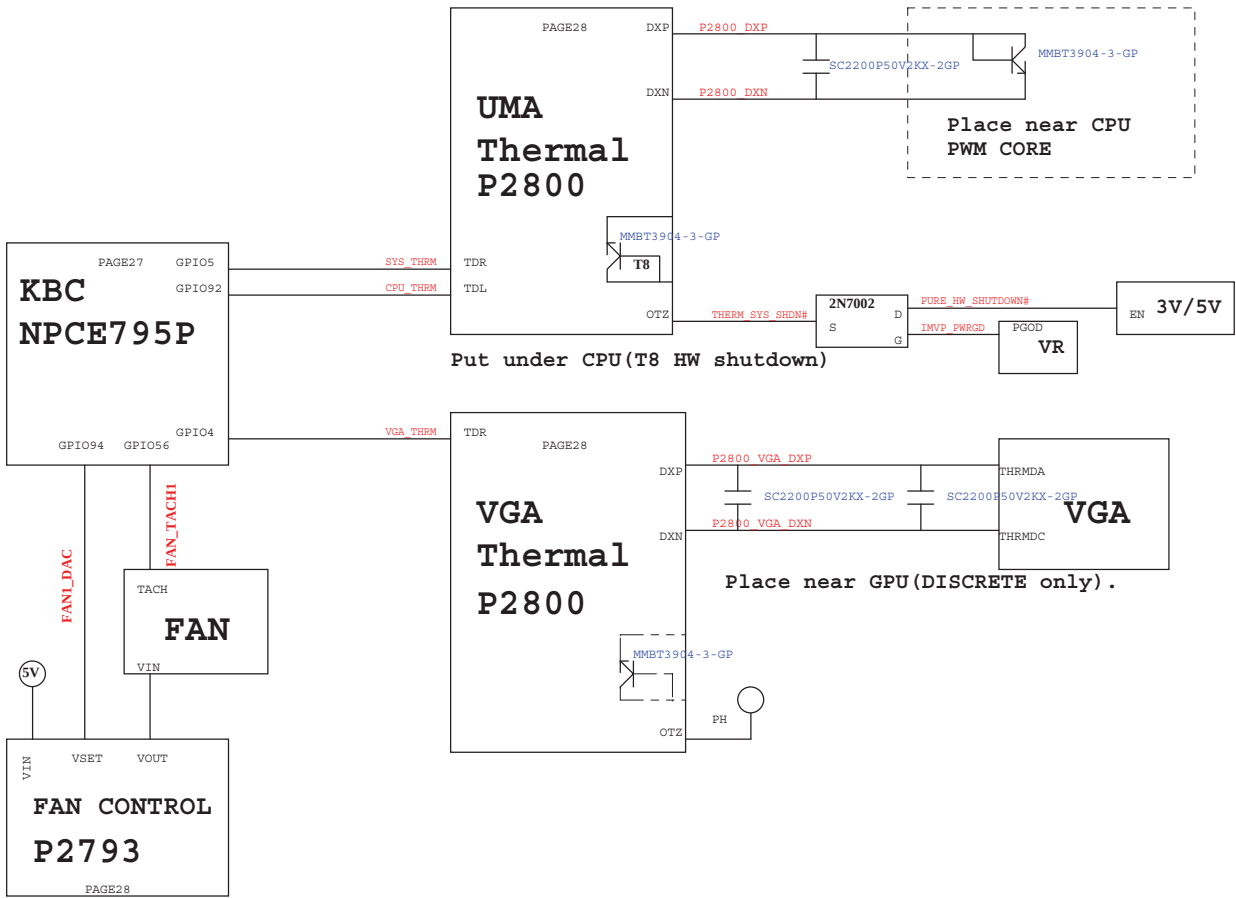


KBC SMBus Block Diagram

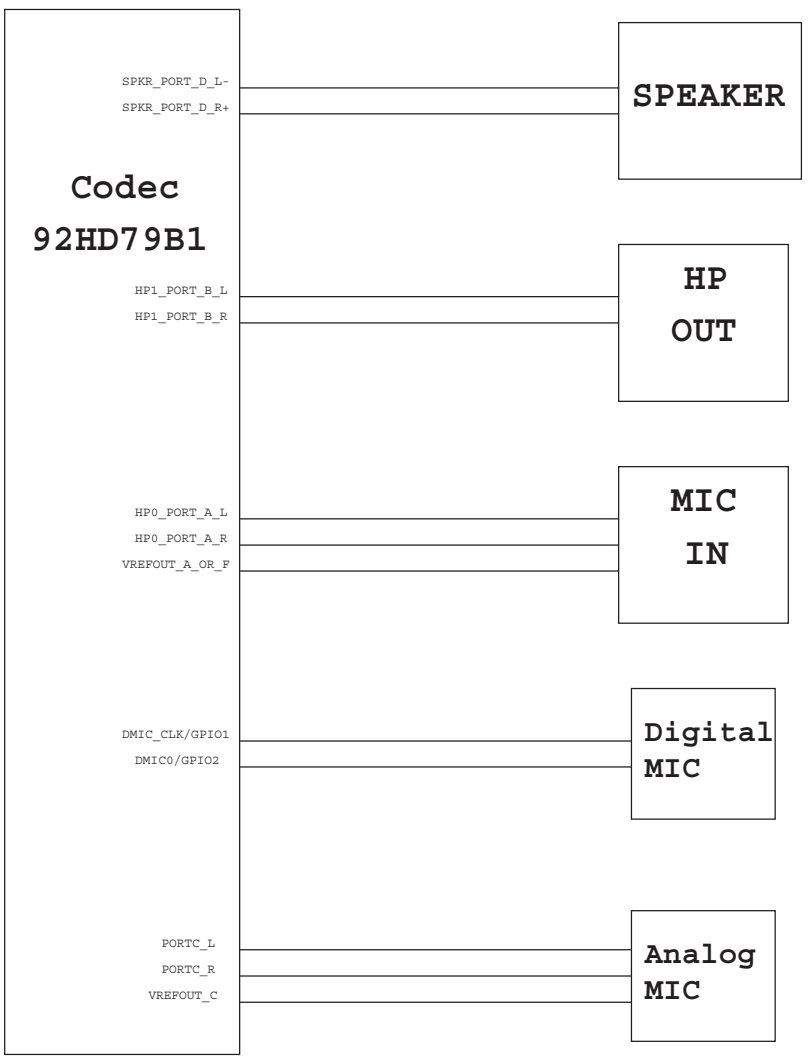


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Thermal Block Diagram



Audio Block Diagram



VERSION	DATA	PAGE	Change Item
X01	08/25	14	SWAP SA0_DM1 and SA1_DIM1 each other for DM2 can't boot up issue.
	08/29	28	Change U2802 Main source to 74.00991.031, 2nd 74.02793.A31,3rd 74.05606.071
	08/29	61	Add 2nd 77.C1071.20L on TC6101.
	08/29	64	Re-assign FP1 pin define.
	08/29	71	Un-stuff Debug port connector(DB1) on X01.
	08/29	37	Change U3701 pin2 to RUNPWROK from 0D75V_EN. Reserved R3717 0ohm between PM_DRAM_PWRGD and VDDPWRGOOD_R.
	08/29	37	Change R2724 to 20K 0402 from 10K for X01 stage.
	08/29	40	Change 3D3V_AUX_S5 to 3D3V_AUX_KBC to avoid leakage Voltage to 3D3V_AUX_KBC under DC mode.
	08/31	51	HDMI1 change to 22.10296.311 from 22.10296.271
	08/31	28	FAN1 change to 20.F0772.003 from 20.F1639.004
	08/31	57	E-SATA1 change to 22.10321.W11 from 22.10290.141
	09/01	41	PU4104 and PU 4105 horizontally mirror.
	09/01	83	R8305 Change to 30K ohm.
	09/01	97	H1, H5, H13, H7 and H15 change to ZZ.00PAD.J91 from ZZ.00PAD.D01.
	09/01	56	HDD1 add 2nd=62.10065.121.
	09/01	79	U7901 change main source to 74.00351.0B3.
	09/01	42	PR4226 change to 5.62K ohm.
	09/01	45	PTC4502 change to 79.3971V.30L.
	09/03	61	U6101 add 2nd=74.00547.079.
	09/03	49	U4901 add 2nd=74.09724.09F.
	09/03	40	PU4002 and PU4003 add 2nd=84.P1403.B37.
	09/03	24	L2401,L2402,L2403 add 2nd=68.10090.10B.
	09/03	27	DY C2713. Add C2722.
	09/03	47	Add PR4702
	09/03	22	Change FFS_INT2_R from PCH GPIO48 to GPIO15 Removed R2220 and change R2201 default pull up to pull down.
	09/06	20	X2001 add 3rd=82.30020.A31.
	09/06	56	U5601 add 2nd=74.02191.079.
	09/06	93	PU9303 add 2nd=74.05930.03D.
	09/06	37	U3701 add 2nd=73.75Z08.DAH.
	09/06	23	Add 2nd and 3rd for L2301.
	09/06	23	R434 change name to PR9321. Add PC9324 and PR9319 for soft start.
	09/06	61	TC6101=80.10715.B1L, 2nd=77.C1071.21L, 3rd=77.C1071.20L.
	09/06	56	ODD1 add 2nd and 3rd source. HDD1 add 3rd source.
	09/06	49	LCD1 add 2nd source.
	09/06	69	TPAD1 add 2nd.

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VERSION	DATA	PAGE	Change Item
X01	09/06	15	DM1 2nd=62.10017.Q31, 3rd=62.10017.K01.
	09/06	14	DM2 2nd=62.10017.P31, 3rd=62.10017.K11.
	09/07	68	Add 2nd source 20.K0343.004 on PWRBTN1& PWRBTN2 base on updated connector list.
	09/07	69	Add 2nd source 20.K0343.004 on KBLIT1 base on updated connector list.
	09/07	82	Add 2nd source 20.F0085.040 on CRTBD1 base on updated connector list.
	09/07	64	Add 2nd source 20.K0382.006 on FP1 base on updated connector list.
	09/07	75	Add 2nd source 20.K0382.026 on NEW1 base on updated connector list.
	09/07	4~10	Updated CPU1 footprint to SKT-BGA989C470395-1H180 from SKT-BGA989C470395-1H186 base on data base updated. Add 2nd source 62.10040.771 on CPU1 base on updated connector list.
	09/07	75	Change CARD1 to 20.10129.001 from 62.10051.931 from ME double updated latest DXF&EMN on X01.
	09/07	93	PQ9308 change name to PQ9311.
	09/07	ALL	Change all of single 2N7002 to 84.2N702.J31 from 84.2N702.D31 due to 84.2N702.D31 will EOL.
	09/07	28	Change U2801,U2803 to 74.02800.A71 from 74.02800.071 from vender updated parts. Change R2803&R2817 to 107K from 499K,R2804&R2818 to 226K from 102K base on updated ADJ Table.
	09/08	18, 22	Change FFS_INT2_R from PCH GPIO48 to GPIO14 Keep PCH_GPIO5 PH R2201,PCH_GPIO48 PH R2220. Add R1818.
	09/08	82	1.Rename IOBD1 pin20,22,26,28 to IOBD1_20,22,26,28 from PCIE_TXN5,PCIE_TXP5,PCIE_RXP5,PCIE_RXN5. 2.Add RN8207,RN8208 for optional USB3.0 PCIE or USB2.0 signal.
	09/08	18	Reserved USBP9~USBP10 to IOBD1 pin20,22,26,28.
	09/08	37	Stuff Q3704,R3710; un-stuff R3716. U3701 pin2 change to 1.05VTT_PWRGD from RUNPWROK.
	09/08	20	DY R2002.
	09/08	47	Mount PC4710.
	09/08	98	Update N12P power sequence.
	09/09	82	R8201, R8202 and R8203 change to 62 ohm.
	09/10	45	Change PL4501 to 68.2R210.20C from IND-D56UH-27-GP base on Brian updated.
	09/10	41	Change PL4101,PL4102 to 68.2R210.20B from 68.2R210.20Q base on Brian updated.
	09/10	82	Rename IOBD1 pin14 to IOBD1_14 from USB30_SMI#. Add R8207 for USB20 USB_OC#10_11 Add R8206 for USB30 USB30_SMI# Add R8208 for USB20 USB signal. Add R8207 for USB30 PCIE signal.
09/10	49	Add TPNL1 for touch panel solution 4pin connector. Change LCD1 to 20.F1816.030 for 30pin Re-assign LCD1 pin define base on Roy updated cable pin define list.	
09/10	51	Change HDMI1 part number to 22.10296.331 from 22.10296.311 base on ME Double updated.	

VERSION	DATA	PAGE	Change Item
X01	09/13	83	Change X8501 to 82.30034.641;2nd 82.30034.651;3rd 82.30034.681 from sourcer suggestion.
	09/13		Change KBLIT1, PWRBTN2 and TPAD1 2nd source from 20.K0343.004 to 20.K0382.004.
	09/13	47	Change 1.8V power solution.
	09/14	82	Change R8201~R8203 to 470ohm from 100ohm. Add RN8209 PH 5V_S5 on MEDIA_LED1~3# for PWM OD mode.
	09/14	40	Add 2nd source 84.04835.H37 on PU4002,PU4003 base on Brian updated 2nd source excel file.
	09/14	58	Change SPK1 to 20.F0772.004 from 20.F1647.004 from Double updated.
	09/14	51	Add R5101~R5108and reserved TR5101~TR5104 on all of HDMI differential pair for EMC suggestion. Rename HDMI1 CONN NET name.
	09/14	29	Add R2920,R2921 and reserved EC2901,EC2902 on AUD_DMIC_CLK &AUD_DMIC_IN0 for EMC suggestion.
	09/14	75	Add R7503,R7504 and reserved EC7501,EC7502 on CLK_PCIE_NEW &CLK_PCIE_NEW# for EMC suggestion. Rename NEW1 pin24,25 to USB_PP13_R&USB_PN13_R. Rename NEW1 pin8,9 to CLK_PCIE_NEW_C&CLK_PCIE_NEW#_C
	09/14	20	Reserved EC2004,EC2005 on CLK_PCIE_NEW &CLK_PCIE_NEW# for EMC suggestion.
	09/14	49	Reserved EC4910~EC4915 on LVDS signal for EMC suggestion.
	09/15	58	Re-assign SPK1 pin define base on Roy updated excel file for 20.F0772.004
	09/15	51	Add 2nd source 22.10296.311 on HDMI1 from updated connector list.
	09/15	68	Add 2nd source 20.K0382.004 on PWRBTN1& PWRBTN2 base on updated connector list.
	09/15	82	Re-assign CRTBD1 pin define base on EMC suggestion.
	09/15	49	Change BLON_OUT_C to pin 15 and pin 4 to NC on LCD1.
	09/15	28, 51,82	Add test point for WKS AFTE request.
	09/15	All	ADD 2nd source follow Power team suggestion.
	09/15	92, 93	Modify PR9318 and PR9228 power source from 3D3V_AUX_S5 to 3D3V_S5.
	09/15	86	Reserve Q8602, C8603 and R8606 for VGA over temp.
	09/15	20	RN2005 swap net.
	09/15	19	RN2005 swap net.
	09/15	48	Change PR4809 to 10K from 100K PH power source change to 3D3V_S0 from S5.
	09/15	82	Re-assign CRTBD1 pin define base on EMC suggestion.
	09/15	97	Reserved EC9701~EC9723 0.1uF for RF suggestion.
	09/15	41	Un-stuff PU4101,PD4105,PR4124, PR4125,PR4101 at X01 stage for 5mW issue.
	09/15	69	un-stuff R6907 and stuff R6905,Q6902,R6906 for 5V drive CAP LED.
	09/17	82	Change IOBD1 part number to 20.F1849.080 base on Double updated latest DXF&EMN.
	09/17	49,57 32,64	stuff TR4901 and un-stuff R4911,R4912 at X01 stage from EMC Neo suggestion. stuff TR4902 and un-stuff R4908,R4909 at X01 stage from EMC Neo suggestion. stuff TR5701 and un-stuff R5718,R5719 at X01 stage from EMC Neo suggestion. stuff TR3201 and un-stuff R3211,R3210 at X01 stage from EMC Neo suggestion. stuff TR6401 and un-stuff R6403,R6404 at X01 stage from EMC Neo suggestion.
	09/17	20	Change RN2010~RN2016 to 33ohm from 0ohm from EMC Neo suggestion.
	09/17	37	Change R3710 to 100K from 0ohm to avoid impact 1.05VTT_PWRGD turn off sequence directly.
	09/17	17	Add R1703~R1705 on RGB signal and reserved EC1701~EC1703 0.1u from EMC Neo suggestion.

VERSION	DATA	PAGE	Change Item
X01	09/17	40,41	Stuff EC4002 0.1uF from EMC Neo suggestion. Stuff EC4008 0.1uF from EMC Neo suggestion. Stuff EC4102,EC4103 0.1uF from EMC Neo suggestion. Stuff EC4107 0.1uF from EMC Neo suggestion. Stuff PC4119,PC4120 0.1uF from EMC Neo suggestion. Stuff EC4006,EC4007 0.1uF from EMC Neo suggestion.
	09/17	60,18	EC6001 change to 10p from 4.7p and default stuff from Neo suggestion. EC1801 change to 10p from 4.7p and default stuff from Neo suggestion.
	09/17	44	default stuff EC4407,EC4405,EC4403,EC4410 base on EMC Neo suggestion.
	09/17	49	Add 2nd source 20.F1561.004;3rd source 20.F1686.004 on TPNL1 from updated connector list.
	09/17	49	Add 2nd source 20.F1561.004;3rd source 20.F1686.004 on TPNL1 from updated connector list.
	09/17	82	Change R8201~R8203 to 430ohm.
	09/17	48	Change PR4809 to 4.7K from 100K PH power source change to 3D3V_S0 from S5.
	09/17	40,27,83	Rename PCIE_RST# to AD_IA_HW2 on KBC GPIO50 for power Tom suggest. Reserved PQ4004,PR4036,PR4037 for AD_IA_HW2 function.
	09/17	68	Rename CHARGER_LED1 to CHARGERLED1. Rename FPOWER_LED1 to FPOWERLED1. Rename HDD_LED1 to HDDLED1. Rename TP_LOCK_LED1 to TPLOCKLED1. Rename TP_LOCK_LED2 to TPLOCKLED2. Rename WLAN_LED1 to WLANLED1
	09/17	21,22	Base on layout routing,Add RN2104 10K instead of R2111 10K. Move EC_SCI#,DBC_EN to RN2201. Move S_GPIO to RN2103. Move PSW_CLR# to RN2104.
	09/17	56	Change R5605 to 100K from 10K and PH to 5V_S0 from 3D3V_S0 to meet Vgs>2V turn on.
	09/17	56	Add Q2706 2N7002 to avoid leakage loop from 3D3V_S5 to 3D3V_AUX_KBC issue when 10mW latched fail timing.
	09/17	ALL	Change all of 0402 0ohm to 0R0402 short pad. PR4008,PR4010,PR4012,PR4020,PR4023,PR4024,PR4027,PR4028,PR4029,PR4225PR4102,PR4113,PR4118, PR4121,PR4203,PR4204,PR4215,PR4222,PR4231,PR4243,PR4301,PR4509,PR4510,PR4801,PR4804,PR4805, PR4808,PR4810,PR9211 F4902,PR4017,PR4018,PR4106,PR4611,PR4710,PR4807,R2304,R2403,R2406,R2409,R2702,R2902,R2903,R2904 R2305
	09/20	9	Add 2nd for TC901.
	09/20	83	Add 2nd for L8303.
	09/20	82	Add 2nd for LD8201.
	09/20	86	Add 2nd for Q8601.
	09/20	83	Add R8321. C8353 and C8354 change to 12pF.
	09/20	82	Redefine IOBD1.
	09/20	75	AFTP111 and AFTP110 connect to USB_PP13_R and USB_PN13_R.
	09/20	51	Change P/N of Q5102.
	09/21	42	Change PU4201 VDD power source to 5V_S5 from 5V_S0 to avoid abnormal MVP_PWRGD waveform.
	09/21	47	stuff PC4714 22uF from Brian updated.

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

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X01	09/21	45	Change PR4507 to 20K from 20.5K from Brian updated.
	09/21	46	Change PR4602 to 110K from 68K from Brian updated.
	09/21	42	Change PR4217 to 1.27K from 1K from Brian updated. Change PR4213 to 3.6K from 3.16K from Brian updated. Change PR4236 to 3.01K from 3.32K from Brian updated.
	09/21	44	Change PC4410 to 0.01u from 0.022uF from Brian updated.
	09/21	39	Add 2nd 83.00099.K11;3rd 83.00099.T11 on D3901,D3902,D3903 from Sourcer Eden suggestion.
	09/21	39	Add 2nd 84.02143.011;3rd 84.00143.N11 on 6801,Q6804,Q6805,Q6806,Q6807,Q6808 from Sourcer Eden suggestion.
	09/21	43	Change PU4303,PU4306,PU4309 dummy field only for QC CPU stuff. Change PC4307,PC4316 dummy field only for QC CPU stuff. Add 2nd for PTC4306.
	09/21	41	PD4101, PD4103, PD4104 and PD4105 add 2nd source.
	09/21	69	Q6902 add 2nd source.
	09/21	40	PD4001 add 2nd source.
	09/21	19	move PCH_WAKE# to RN1901 pin4;Add R1909 PH 100K on AC_PRESENT.
	09/21	37	R3710 change to 0ohm. Remove R3701 and C3701.
	09/21	42	Add PR4214, PC4230, PR4216 and PC4231 from Brian updated.
	09/23	20	RN2016, RN2010, RN2011, RN2012, RN2014 and RN 2013 keep 0ohm.
	09/23	ALL	PR9216, R504, R1812,R1813,R1815,R1817, R1903, R1906,R1910,R1912,R1913,R1924,R1925, R2213,R2219, R2711,R2720,R2733,R2761, R2807,R2814, R3708, R5125, R5127, R5721, R5722.
	09/23	75	Add R7505~R7508 0ohm and reserved EC7503~EC7506 on PCIE_TX8&RX8 signal base on EMC Lance suggestion. Add R7509,R7510 0ohm and reserved EC7507,EC7508 on CLK_PCIE_NEW_REQ#&PCIE_WAKE# signal base on EMC Lance suggestion.
	09/23	ALL	RN5101, RN2201, RN1702, RN1901, RN1705 swap pin.
	09/23	79	DUMMY G-SENSOR.
	09/23	92	Update value of PR9210, PR9209 and PR9213 for N12P.
	09/23	43	PR4320 change to 4 m ohm.
	09/23	68	Add 2nd source 83.00110.J70 on FPOWERLED1,HDDLED1,WLANLED1 from Sourcer Anya suggestion. Add 2nd source 83.00326.G70 on CHARGERLED1from Sourcer Anya suggestion. Add 2nd source 83.00190.Z70 on TPLOCKLED1,TPLOCKLED2 from Sourcer Anya suggestion.
	09/23	69	Change KBLIT1 part number to 20.K0589.004 and re-assign pin define base on Roy updated.
	09/23	42, 44	Add 2nd source 69.60011.201 on PR4405,PR4245 from Sourcer Kitty suggestion.
	09/23	42	Add 2nd source 69.60037.021 on PR4246,PR4247 from Sourcer Kitty suggestion.
	09/24	23	Add 2nd source 68.00214.211 on L2301 updated from DN13ATI.
	09/24	68, 69	Change R6806,R6808,R6811~R6813,R6801,R6803,R6815,R6906 to 390ohm from 1K to fine tune all of MB LED for 5mA spec.
	09/27	51	Reserve R5114 and R5115.
	09/27	85	Reserve R8510 and R8513.
	09/27	83	DY U8301, mount R8323.
	09/27	92	R9206 change to 10K, PC9211 mount 0.1u.
	09/27	93	R9312 change to 1K.

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X01	09/27	49, 57 32, 64	TR4901, TR4902, TR5701, TR3201 and TR6401 DY. Stuff 0 ohm.
	09/27	69	AFTP73 connect to TP_VDD.
	09/27	85	U8501 power change to 3D3V_S0.
	09/27	92	PL9201 change like CPU core power choke.
	09/28	83, 84	L8303, L8401, L8402, L8502 and L8503 follow NV DG spec.
	09/28	46	Change PR4606 to 4.02K from 240ohm for fine tune 1.5V output Voltage.
	09/28	92	PTC9202, PTC9203 and PTC9204 2nd=79.47719.9BL
	09/28	22	Change R2220 to 10K from 100K.
	09/28	60	EC6001 change to 10p from 4.7p and default un-stuff from Neo suggestion. EC1801 change to 10p from 4.7p and default un-stuff from Neo suggestion
	09/28	27	Change R2710, R2739, R2724 and R2726 change to 1%.
	09/29	27	Default mount R2756, Dummy R2734.
	10/04	24	Add 2nd source 68.1001E.10N on L2401,L2402,L2403 from sourcer Renee Lee updated.
	10/07	43	PTC4306 cahnge second source to 79.47612.60L.
	10/09	85	Change L8503 to 68.00375.091,and add second source 68.00206.171
	10/09	85	Change L8502 to 68.00115.191,and add second source 68.00206.131
	10/09	84	Change L8401 and L8402 to 68.00115.181,and add second source 68.00206.341
	10/09	83	Change L8303 to 68.00375.101,and add second source 68.00119.101
	10/09	83	Change L8301 to 68.00115.161,and add second source 68.00206.111
	10/09	42	Change PR4217 to 64.84505.6DL for Dual-core OCP
	10/09	42	Change PR4213 to 64.23715.6DL for Dual-core loadline
	10/09	42	Change PR4207 to 64.22025.6DL for CPU(35W) Turbo setting
	10/09	42	Change PR4202 to 64.22025.6DL for GFX Turbo setting
	10/09	20,83	Dummy R2004 R2003 and PQ8309, stuff R2005
	10/19	28	Change R2817 from 107K to 124K (64.12435.6DL) for VGA temperature setting change
	10/25	84	Change R8402 from 40D2R to 60D4R (64.60R45.6DL) for meeting the spec
	10/25	14 15	Add DM1 and DM2 second source:62.10017.Q41 and 62.10017.P61
X02	10/25	85	Ventura SMBC_INA219_C and SMBD_INA219_C add 3.3V pull high schematic
	11/01	51 85	Change HDMI HPD schematic for cost down
	11/10	27	Change R2724 to 64.33025.6DL for PCB version change
	11/10	83	Change L8301 to 68.00115.181,and add second source 68.00206.341

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X02	11/11	14	DM2 1st change to 62.10017.P61; 2nd change to 62.10017.N41 on ST stage from ME updated connector list.
	11/11	15	DM1 1st change to 62.10017.Q41; 2nd change to 62.10017.N11 on ST stage from ME updated connector list.
	11/11	60	U6001 1st change to 72.25Q32.A01; 2nd change to 72.25320.C01; 3rd change to 72.25P32.C01 on ST stage
	11/11	68	Change CHARGERLED1 2nd to 83.00327.D70 from Sourcer updated.
	11/11	37	Change U3701 1st to 73.7SZ08.EAH;2nd to 73.01G08.L04;3rd to 73.7SZ08.DAH from Sourcer Eason updated.
	11/11	69	Add 2nd 20.K0592.030 on KB1 from ME updated connector list.
	11/11	82	Add 2nd 20.K0465.008 on MEDIA1 from ME updated connector list.
	11/11	58	Add 2nd 20.F1804.004 on SPK1 from ME updated connector list.
	11/11	28	Add 2nd 20.F1841.003 on FAN1 from ME updated connector list.
	11/11	70	Add 2nd 20.F0962.010 on HALL1 from ME updated connector list.
	11/11	23	Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue. Change VCCADAC power source to 3D3V_DAC_S0 from 3D3V_S0.
	11/11	60	Add Q6002,R6007 fo FACTORY RTC detect function
	11/11	28	ADJ&ADJ_VGA power source change to 3D3V_DAC_S0 from 3D3V_S0 to solve T8 shut down issue.
	11/11	28	Reserved G709T1UF for T8 solution sync with DN13.
	11/12	82	Change R8201, R8202, R8203 from 430 ohm to 1K ohm (63.10234.1DL) for soluting media board LED brightness is too light issue
	11/15	49	Add 2nd 20.F1860.030 on LCD1 from ME updated connector list.
	11/15	8	Reserved C802~C804,C806,C807 10uF 0603 for power team fine tune Vcore quality
	11/15	88 89 90 91	All of VRAM(VRAM1~VRAM8) PCB footprint change to CO-LAY type (DUMMY-BGA96D075133H48) from BGA96D0913H48 same as DW30.
	11/15	68 69	Change R6813, R6906 from 390 ohm to 1K ohm (63.10234.1DL) for soluting LED brightness is too light issue
	11/15	20	Dell required us to disable PCIE port of WWAN slot ,If PCIE port 1 is disabled, it will cause all PCIE port disabled,so change WWAN to PCIE port 3 from port1 at ST stage.
	11/16	97	Change HHD1 HDD4 HGPU1 HGPU2 2nd from 34.4CK01.201 to 34.4CK01.401 from ME update connector list
	11/16	68	Change R6808, R6811 from 390 ohm to 1K ohm (64.10234.1DL) for soluting LED brightness is too light issue
	11/16	28	stuff both G709T1UF and P2800 related circuit, add R2805 0ohm default un-stuff at ST stage.
	11/17	48	CO-LAY APL5916 related circuit for VCCSA LDO solution.
	11/18	23	Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue. Change VCCADAC power source to 3D3V_DAC_S0 from 3D3V_S0. Stuff R2301 and un-stuff L2301.
	11/18	28	Add R2805 0hm between THERM_SYS_SHDN#_OTZ and THERM_SYS_SHDN#. Add R2812 0ohm between THERM_SYS_SHDN# and U2805 pin3.

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X02	11/18	28	Rename U2801&U2804 pin 8 to THERM_SYS_SHDN#_OTZ from HERM_SYS_SHDN#.
	11/18	20	Change X2001 to 82.30020.D41 from 82.30020.851 from Sourcer Dick updated.
	11/18	23	Reserved R2308,R2309 on VCCVRM power rail.Reserved U2302 LDO circuit on VCCVRM power rail
	11/18	22 82	Rename USB3_PWR_ON to PCH_GPIO57. Add R8209,R8210 for PM_SLP_S4# and VGA_THRM to control USB3_PWR_ON
	11/18	48	Change PTC4801 to 100u(77.21071.07L) from 150u from power team Brian updated
	11/19	74	Add 2nd 20.10135.001 on CARD1 from ME updated connector list.
	11/19	82	Add 2nd 20.F1908.080 on IOBD1 from ME updated connector list.
	11/20	3	Updated PCIE ROUTING
	11/20	28	Change U2801,U2804,U2805 VCC power to 3D3V_DAC_S0 from 3D3V_S0. Stuff R2812, un-stuff R2805
	11/20	23	Reserved R2308 on VCCVRM power rail. Reserved U2302 LDO circuit on VCCVRM power rail.
	11/20	48	Set TPS51461 PWM solution dummy field for VCCSA_PWM and APL5916 LDO solution dummy field for VCCSA_LDO. default stuff VCCSA_LDO at ST stage
	11/20	22	Rename GFX_CRB_DET to GSENSOR_DET on GPIO39.
	11/20	60	Un-stuff R6007 10M.
	11/20	82	Reserved EC8201,EC8202 0.1u(closed H3) between AGND and GND from EMC Neo suggestion.
	11/20	82	Reserved EC8203~EC8205 470p on all of MEDIA_LED# signal from EMC Neo suggestion.
	11/20	82	Add RN8205 base on HSYNC&VSYNC report
	11/20	61	Removed R6101 and connect USB_PWR_EN# to U6101 pin4 directly.
	11/20	22	Rename PCH_GPIO12 to RTC_DET# on GPIO12.
	11/20	61 22 18	Reserved U6102 USB POWER related circuit to separate EATA and CRT USB power in ST build. Reserved USB2_CRT_ON# to control U6102 USB power switch from PCH GPIO57. Reserved USB_OC#0_1 connect from PCH GPIO59.
	11/20	82	Reserved R8211,R8212 0ohm 0805 on CRTBD1 pin37,39 to separate EATA and CRT USB power in ST build.
	11/22	82	Swap RN8205 pin4,3 and pin2,1 each other base on Connie swap report.
	11/22	82	stuff EC8201,EC8202 0.1u(closed H3) between GND and GND from EMC Neo suggestion. stuff EC8206 between 3D3V_S5 and GND from EMC Neo suggestion.
	11/22	23	base on layout condition change 3D3V_DAC_S0 circuit. Stuff R2301 and un-stuff L2301.
	11/22	82	stuff EC8203~EC8205 470p on all of MEDIA_LED# signal from EMC Neo suggestion.
	11/22	23	Removed U2302 LDO for VCCVRM.

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X02	11/22	29	change R2920,R2921 to 22ohm from 0ohm and stuff EC2901,EC2902 22p from EMC Neo updated.
	11/22	61	Change U6101 to dual USB power switch from single for Layout limitation and placement. Reserved USB2_CRT_ON# to control U6102 USB power switch from PCH GPIO57. Reserved USB_OC#0_1 connect from PCH GPIO59.
	11/22	49	stuff C4908 0.1uF from EMC Neo suggestion.
	11/22	57	Change TR5701 to 69.10103.041 and un-stuff R5718,R5719 from EMC Neo Suggestion.
	11/22	49	Change TR4902 CM choke to 69.10103.041 and un-stuff R4908,R4909 from EMC Neo Suggestion.
	11/22	49	Swap TR4901 pin4,3 and pin2,1 each other base on Connie swap report. Change TR4901 CM choke to 69.10103.041 and un-stuff R4911,R4912 from EMC Neo Suggestion.
	11/22	75	Change TR7501 CM choke to 69.10103.041 and un-stuff R7501,R7502 from EMC Neo Suggestion.
	11/22	58	stuff EC5801~EC5804 470pF from EMC Neo suggestion.
	11/22	9 39 45 49	stuff EC901, EC3903, EC4501, EC4909, EC4907 0.1uF from EMC Neo suggestion.
	11/22	49	Change RN4901 to 100ohm 4p from 8p for improve layout place.
	11/22	48	Updated VCCSA_LDO circuit from Power team Brian updated.
	11/22	83 84 85	Change L8301 L8401 L8402 to 0 ohm resistor (63.00000.00L)
	11/22	60	stuff R6007 10M.
	11/23	49 57 75	SWAPTR4901 TR4902 TR5701 TR7501 pin1&4 and pin2&3 each other base on Connie swap report.
	11/23	60	Change U6101 1st(74.02182.071);2nd(74.00546.A7D);3rd(74.02062.079) from Sourcer Harrison suggestion.
	11/23	64	Add C6402 0.1uF,C6403 180pF and stuff C6401 47pF from RF fine tune result.
	11/23	57 49 75	Change R5718,R5719,R4908,R4909,4911,R4912,R7501,R7502 to 0ohm 0603 from 0402.
	11/23	56 97	stuff EC9739,EC9737,EC9735 47pF from RF fine tune result. stuff EC5601 180pF from RF fine tune result. Stuff EC9738 0.22uF closed EC9739 from RF fine tune result.
	11/23	97	stuff ECEC9729,EC9730 470pF from EMC Neo suggestion.
	11/23	45	Change PR4501 to 75K from 45.3K for 1.05V OCP set to 20A from Brian.
	11/23	82	Removed R8211,R8212 and connect 5V_USB2_S3 to CRTBD1 pin 37 directly.
	11/23	61	Removed C6105,C6103.
	11/23	69 70	Change AFTP 80 81 to AFTP 83 84; change AFTP 83 to AFTP82; change AFTP 82 to AFTP85.
	11/24	20	Add 2nd(82.30020.G71);3rd(82.30020.G61) on X2001 from Sourcer Dick updated.
	11/24	69	Add 2nd(20.K0613.004)on KBLIT1 from Karl updated.

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X02	11/24	57	Add 2nd(22.10339.261)on ESATA1 from Karl updated.
	11/24	28	un-stuff VGA P2800 related circuit from Niki confirmed.
	11/24	64	rename C6401,C6402,C6403 to EC6401,EC6402,EC6403
	11/24	22	Dummy R2206
	11/25	28	Dummy R2817 R2818 C2816
	11/25	69	Add 3rd(83.00110.R70) on FPOWERLED1,HDDLED1,WLANLED1 from Anya provide
	11/25	69	Add 3rd(83.00192.J70) on TPLOCKLED1 and TPLOCKLED2 from Anya provide.
	11/25	69	Add 3rd(83.01108.070) on CHARGERLED1 from Anya provide.
	11/26	43 92	Change PC9217 PC4319 to 0.1u 50V
	11/29	83	Change C8353 C8354 to 15PF ,R8320 stuff from vendor suggestion.
	11/29	36	Stuff D3602
	11/30	68	Change 2nd source to 83.00322.070 from 83.00110.J70
	11/30	85	Change L8502 L8503 to 0 ohm
	11/30	92	Stuff PR9237 DY PR9321
	12/01	8	Change C837,C826 to 22uF from 10uF and default stuff from Power Brian updated.
	12/01	8	Change C801~C807 and C817 10uF stuff at QC CONFIG from power Brian updated.
A00	12/21	ALL	Change 0402 pad(ZZ.00PAD.M11): R1404 R1405 R1503 R1504 R1703 R1704 R1705 R1807 R2301 R2306 R2307 R2308 R2404 R2405 R2735 R2737 R2758 R2759 R2760 R2762 R3614 R3710 R5114 R5801 R5802 R5803 R5804 R8210 R8323 R8511 R8512
	12/21	82	Change 0603 pad(ZZ.00PAD.M21): R8206 R8207
	12/21	17 20	Change resistor pad(ZZ.0R04P.ZZZ): RN1704 RN2010 RN2011 RN2012 RN2013 RN2014 RN2015 RN2016
	12/21	83 84 85	Change L8301, L8401,L8402,L8502,L8503 to 0R0603 pad(ZZ.00PAD.M21)
	12/21	ALL	Change to Parallel resistor R1501 ,R1502; R2739 ,R2774;R8202 ,R8203;R8501 ,R8502;R8506 ,R8507;R2123 ,R2124
	12/21	82	RN8205 change to R8201, R8202
	12/21	93	PR9237 rename to PR9337
	12/21	56 61 68	Delete 77.C1071.21L(TC6101), delete 83.01108.070(CHARGERLED) , delete 62.10065.121(HDD1)

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A00	12/22	27	R2724 change to 47K resistor for XBulid
	12/22	27	R2301 change to 0 resistor for CRT debug
	12/22	40	1.Change PR4032,PR4034,PR4037 to ZZ.00PAD.M11 2.Stuff PQ4003,PQ4004 3.Change PR4047 to 174K(64.17435.6DL) 4.Change PR4035 to 300K(64.30035.6DL) 5.Change PR4036 t0 76.8K(64.76825.6DL) 6.Change PR4031 to 150K(64.15035.6DL)
	12/23	68	1.FPOWERLED1 rename to FPLED1 2.HDDLED1 rename to HDLED1 3.CHARGERLED1 renamtpe to CHLED1 4.WLANLED1 rename to WLED1 5.TPLOCKLED2 rename to TPLED2 6.TPLOCKLED1 rename to TPLED1 7.PWRBTN1 rename to PWRBT1 8.PWRBTN2 rename to PWRBT2
	12/23	43	Delete PR4323,PR4324,PR4325; Stuff PR4320 for all BOM ,not co-lay Ventura
	12/23	92	Delete PR9220,PR9222,PR9223; Stuff PR9217 for all BOM ,not co-lay Ventura
	12/23	51	Change 5V_HDMI to 5V_CRT_S0_R for HDMI power leakage
	12/24	All	PRN3901 rename to PN3901 PTC9202~04 rename to PT9202~04 PTC4301~04 rename to PT4301~04 PTC4306 rename to PT4306 PTC4308~09 rename to PT4308~09 PTC4401~03 rename to PT4401~03 PTC4502 rename to PT4502 PTC4602 rename to PT4602 PTC4102 rename to PT4102 PTC4104 rename to PT4104
	12/24	28	Change U2802 3rdto 74.05606.A71 at X-Build batch run
	12/24	82	Change RN8205 to 66.22036.04L from 66.22036.040at X-Build stage
	12/24	82	Reserved R8211 0603 0ohm on F8201
	12/24	36	Reserved Q3603 2N702 on IMVP_PWRGD to fine tune glitch waveform when AC lose and DC lose.
	12/24	28	Change 3D3V_S0 to 3D3V_DAC_S0
	12/24	45 46 93	Change to short pad: PR4502,PR4607,PR9311,PR9312,PR9326. DUMMY PC4501
	12/27	28	If stuff P2800EA1 then must stuff R2803,R2804,C2805 but if stuff P28003B0 should be unstuff.
	12/27	42	PR4207,PR4213,PR4217 DUMMY field set to DC&QC option
	12/28	51	Change 5V_HDMI to 5V_CRT_S0_R on RN5101
	12/28	28	Un-stuff U2805 G709T1UF related circuit and R2812 then stuff R2805 at XBuild

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A00	12/28	27	Change R2756, R2763, R2766 to short pad
	12/28	36	Stuff Q3603
	12/28	28 86	Cancel VGA Thermal sensor P2800 circuit
	12/28	27 28 82	Change to VGA_THRM to USB3_PWR_ON
	12/28	23	Change R2301 to short pad
	12/29	51	Change HDMI resistor to short pad
	12/29	49,57,75	Delete USB DUMMY resistor for no-lay
	12/29	32	Change USB 0 resistor to short pad for no-lay
	12/29	5	Reserve EC502 ,EC504 for EMI suggestion,add DUMMY EC505 for EMI
	12/29	82	Delete PM_SLP_S4# line, directly link to USB3_PWR_ON
	12/29	23	Add 3rd Richtek(74.09198.G7F) on U2301 at XBuild batch run config
	12/29	68	Not use Liteon LED(83.00322.070) for package
	12/30	5	Add DUMMY diode EC506 for BUF_CPU_RST# as EMI suggestion
	12/30	42	PC4227 change to 78.33420.5FL as 78.33423.5FL obsoleted
	12/30	49	Change R4904 to short pad
	12/31	86	Add probe point for P2800_VGA_DNX/P2800_VGA_DXP
	01/03	68	Change TPLED1,2 1st to 83.01921.P70 ,2nd to 83.00190.S7A,3rd to 83.00191.H70; R6813 change to 390R from 1K same as DN13 LED part.
	01/03	49	Delete R4908, R4909 for USB_Camera not co-lay
	01/03	4~10	Add 3rd foxconn(62.10055.321) on CPU1 at X-Build batch run config
	01/03	82	Add 3rd T-conn(20.F1932.040) on CRTDB1at X-Build batch run config
	01/03	97	Add 3rd LIDON(34.4CK01.501) on HHD1,HHD4,HGPU1,HGPU2 at X-Build batch run config
	01/04	68	Delete 83.00191.H70 for TPLED1,2 as cost high
	01/04	49,57,75	Add 2nd TAI-TECH(69.10084.071) on TR4901,TR4902,TR5701,TR7501 at X-Build batch run config

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