FOOSE UMA Schematics Document (AMD 15.4")

AMD Giffin CPU S1G2

AMD RS780 +SB700

2008-01-04

REV : SB

```
DY : Nopop Component
5761 : Use BCM5761E
5756 : Use BCM5756M
B_TPM : Use LOM TPM
C_TPM : Use China TPM
```

<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	COVER PAGE	
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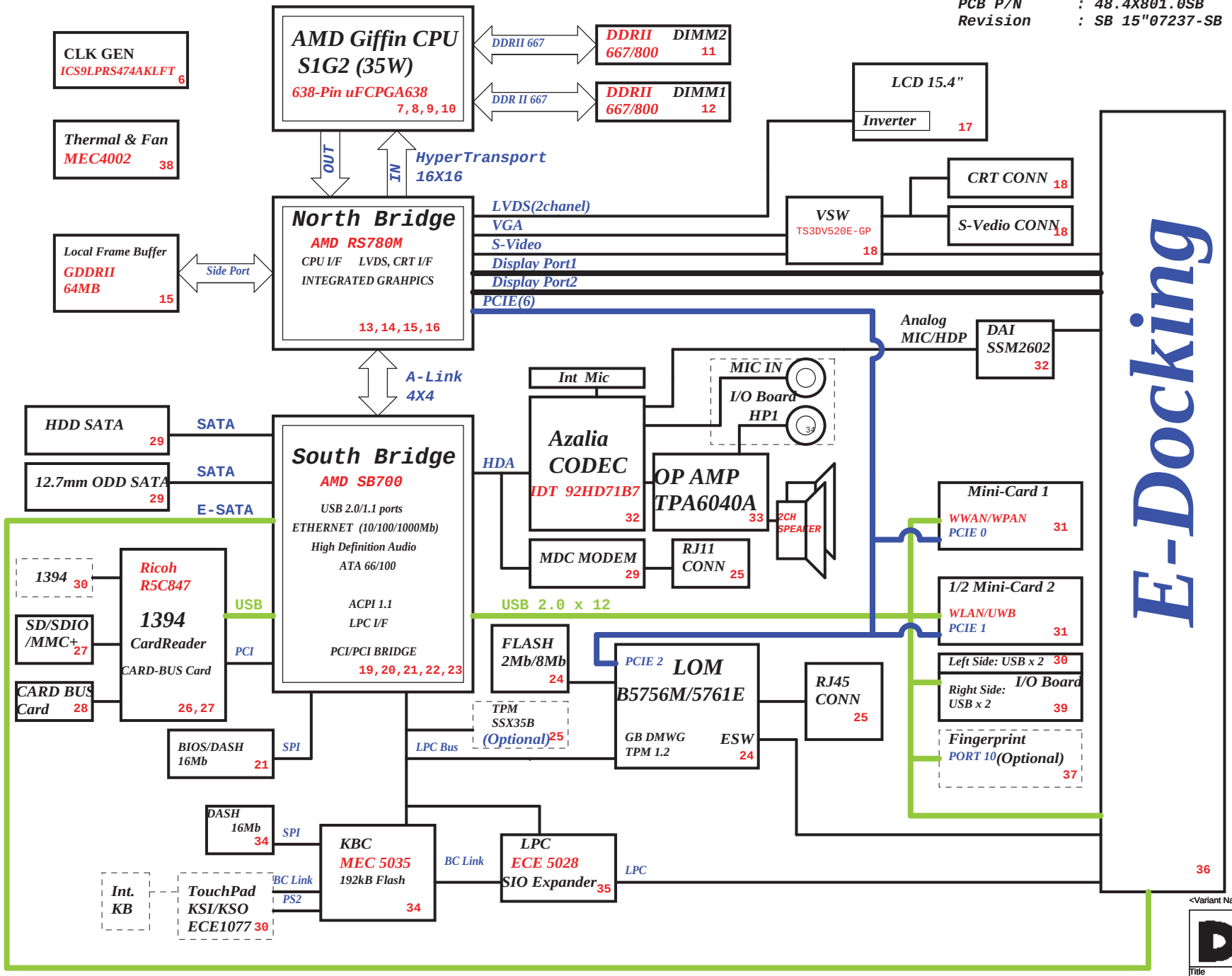
FOOSE AMD 15 UMA Block Diagram

Project code : 91.4X801.001
PCB P/N : 48.4X801.0SB
Revision : SB 15"07237-SB



CHARGER BQ24745RHDR-GP 41	
INPUTS	OUTPUTS
+DC_IN_SS +CHAGER_SRC	+PWR_SRC

CPU CORE ISL6265HRTZ-T-GP 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE0 +VCC_CORE1 +VDDNB

SYSTEM DC/DC SN0608098-GP 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW +3.3V_ALW

SYSTEM DC/DC TPS51116PWPR 45	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS +0.9V_DDR_VTT

SYSTEM DC/DC L6935TR 44	
INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN

SYSTEM DC/DC TPS51117PWR-GP 43	
INPUTS	OUTPUTS
+PWR_SRC	+1.2V_ALW_SUS

SYSTEM DC/DC TPS51117PWR-GP 42	
INPUTS	OUTPUTS
+PWR_SRC	+1.1V_RUN

SYSTEM DC/DC EMC4002 38	
INPUTS	OUTPUTS
+3.3V_RUN	+2.5V_RUN

PCB LAYER

L1:TOP
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Bottom

<Variant Name>

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Title: System Block Diagram
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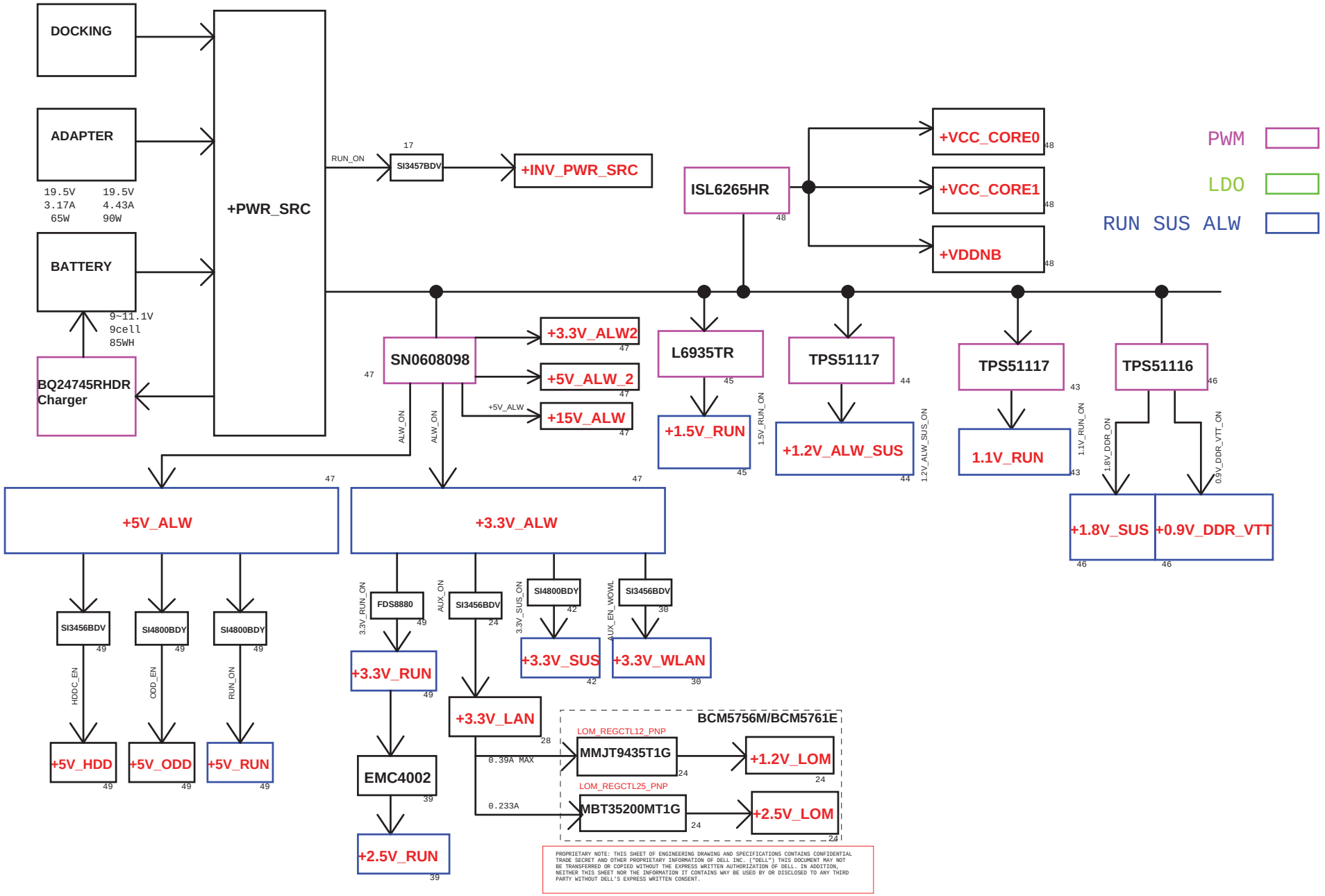

<Variant Name>

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Title: Power Block Diagram

Size	Document Number	Rev
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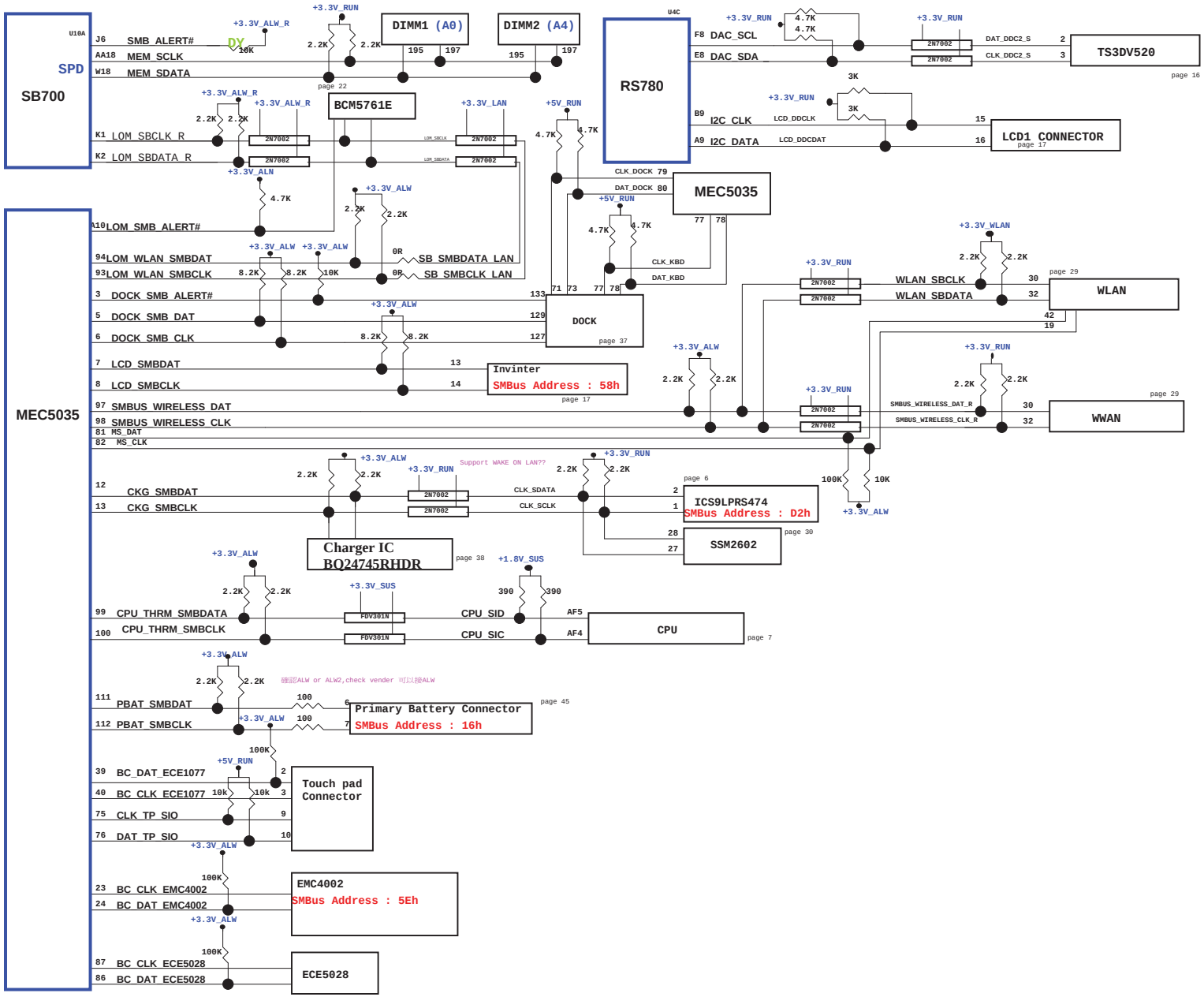

POWER STATES

	State \ Signal	SLP S3#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
RUN	S0 (Full ON)	H	H	ON	ON	ON	ON
SUS	S3 (Suspend to RAM)	L	H	ON	ON	OFF	OFF
ALW	S4 (Suspend to DISK)	L	H	ON	OFF	OFF	OFF
ALW	S5 (SOFT OFF)	L	L	ON	OFF	OFF	OFF

Power Management TABLE

	State \ power plane	ALW_2 (AUX)	ALW	SUS	RUN
		+DC_IN +PWR_SRC +5V_ALW_2 +3.3V_ALW_2 +RTC_CELL	+15V_ALW +5V_ALW +3.3V_ALW +3.3V_WLAN +3.3V_LAN +2.5V_LOM +1.2V_LOM	+5V_SUS +3.3V_SUS +3.3V_ALW_R +1.8V_SUS +1.2V_ALW_SUS +1.2V_SUS +0.9V_DDR_VTT +V_DDR_VREF_M	+5V_RUN +5V_HDD +5V_ODD +3.3V_RUN +2.5V_RUN +1.8V_RUN +1.8V_MEM_VDDQ +1.5V_RUN +1.2V_RUN +1.1V_RUN +0.9V_MEM_VTT +VCC_CORE0 +VCC_CORE1 +VDDNB +INV_PWR_SRC
RUN	S0	ON	ON	ON	ON
SUS	S3	ON	ON	ON	OFF
ALW	S5 S4/AC	ON	ON	OFF	OFF
ALW	S5 S4 on Battery	ON	OFF	OFF	OFF

		USB PORT#	DESTINATION
SB700	2.0	0	Left Side Top
		1	Left Side Bottom
		2	Right Side Top
		3	Right Side Bottom
		4	MINI CARD 2 (WLAN)
		5	MINI CARD 1 (WWAN/Bluetooth)
		6	Reserve
		7	Card Bus
		8	Dock_1
		9	Dock_2
		10	Biometric
		11	LOM
	1.1	12	NC
		13	NC

PCI EXPRESS	DESTINATION
Lane 0	MINI CARD-1 WWAN
Lane 1	MINI CARD-2 WLAN
Lane 2	LOM
Lane 3	RESERVED
Lane 4	RESERVED
Lane 5	RESERVED

19,34,35,39 +RTC_CELL → +RTC_CELL
13,14,15,16,43 +1.1V_RUN → +1.1V_RUN
22,44,49 +1.2V_ALW_SUS → +1.2V_ALW_SUS
31,45,49 +1.5V_RUN → +1.5V_RUN
17,22,24,31,37,47,49 +15V_ALW → +15V_ALW
7,9,16,19,21,22,49,50 +1.2V_RUN → +1.2V_RUN
17,41,42,43,44,46,47,48,51 +PWR_SRC → +PWR_SRC
11,12 +VREF_DDR_MEM → +VREF_DDR_MEM
8,11,12,15,46,49 +0.9V_DDR_VTT → +0.9V_DDR_VTT
17 +LCDVDD → +LCDVDD
10,48 +VCC_CORE0 → +VCC_CORE0
10,48 +VCC_CORE1 → +VCC_CORE1
17 +INV_PWR_SRC → +INV_PWR_SRC
8,9,10,11,12,39,45,46,48,49,50 +1.8V_SUS → +1.8V_SUS
18,22,28,30,31,33,34,37,38,39,48,49,50 +5V_RUN → +5V_RUN
9,17,19,30,38,40,41,42,44,47,49,50,51 +5V_ALW → +5V_ALW
6,17,19,22,24,29,30,31,34,35,37,38,39,40,41,42,47,49,50,51 +3.3V_ALW → +3.3V_ALW
9,20,22,29,30,35,39,43,44,46,49,50 +3.3V_SUS → +3.3V_SUS
6,9,11,12,14,16,17,18,19,20,21,22,23,24,25,26,27,28,31,32,34,35,37,38,39,40,48,49,50,51 +3.3V_RUN → +3.3V_RUN

PCI ROUTING TABLE (By SB700 side)

PCI DEVICE	IDSEL	REQ#/GNT#	VD100/SIRQ	INT#	
RICOH R5C833	AD17	REQ1# GNT1#	SERIRQ	INTE#	INTF#
1394				SD	

<Variant Name>

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Title: Table of Content

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CLK GEN

SSID = CLOCK

CLKREQ# MAP

CLKREQ0#	No use
CLKREQ1#	CLKSRC 1 MINI1
CLKREQ2#	No use
CLKREQ3#	CLKSRC 3 LOM
CLKREQ4#	CLKSRC 4 MINI3
CLKREQ5#	No use
CLKREQ6#	No use
CLKREQ7#	No use

X01
Vendor suggest.

+3.3V_CLK_VDD (40 mils)

C849 SCD1U10V2KX-4GP, C344 SCD1U10V2KX-4GP, C322 SCD1U10V2KX-4GP, C349 SCD1U10V2KX-4GP, C303 SCD1U10V2KX-4GP, C273 SC1U6D3V2KX-GP, C276 SC1U6D3V2KX-GP, C351 SC1U6D3V2KX-GP, C320 SC2D2U6D3V2KX-GP, C350 SC22U6D3V5MX-2GP

+3.3V_CLK_VDD

L28 BLM18PG121SN1D-GP

+3.3V_RUN

X01
Vendor suggest.

+3.3V_CLK_VDDREF

C801 SCD1U10V2KX-4GP, C272 SCD1U10V2KX-4GP, C264 SC2D2U6D3V3KX-GP

L10 BLM18PG121SN1D-GP

+3.3V_CLK_VDDA

C306 SCD1U10V2KX-4GP, C314 SC10U6D3V3MX-GP

L20 BLM18PG121SN1D-GP

X01
Change to PSL part.

14 CLK_NB_GFX
14 CLK_NB_GFX#
RN34 SRN0J-6-GP
CLK_NB_GFX_R
CLK_NB_GFX# R

+3.3V_RUN

RN18 SRN10KJ-5-GP, RN24 SRN10KJ-5-GP, RN37 SRN10KJ-5-GP, R250 10KR2J-3-GP (DY), R249 10KR2J-3-GP (DY)

31 WWAN_CLKREQ#
24 LOM_CLKREQ#
31 WLAN_CLKREQ#

CLKREQ0#, CLKREQ2#, EXP_CLKREQ#, CLKREQ#33, CLKREQ#40

U33

ATIG0C_LPRS, ATIG0T_LPRS, ATIG1C_LPRS, ATIG1T_LPRS, ATIG2C_LPRS, ATIG2T_LPRS

VDDSB_SRC, VDDSATA, VDDREF, VDDHTT, VDDCPU, VDDATIG, VDDSRC, VDDSRC, VDD48, VDDA, VDD

CLKREQ0#, CLKREQ1#, CLKREQ2#, CLKREQ3#, CLKREQ4#, CLKREQ5#, CLKREQ6#, CLKREQ7#

SC12P50V2JN-3GP C254

X2 X-14D31818M-43GP

R173 1MR2F-GP (DY)

X01

CLK_X2 — R831 0R2J-2-GP — CLK_X1

C250 SC12P50V2JN-3GP

SB700_USB(48MHz)

20 CLK48_USB — 22R2J-2-GP R174 — CLK_48

EC10 (DY)

48MHZ_0_2X, 48MHZ_1_2X

CLK_X1, CLK_X2_R

SC4D7P50V2CN-1GP

X1, X2

ICS9LPRS474BKLFT-GP

NB ALINK(100MHz)

SB PCIE(100MHz)

14 CLK_NB_GPPSB#
14 CLK_NB_GPPSB
RN26 SRN0J-6-GP
CLK_NB_GPPSB# R
CLK_NB_GPPSB R
SB_SRC0C_LPRS
SB_SRC0T_LPRS

19 CLK_PCIE_SB#
19 CLK_PCIE_SB
RN33 SRN0J-6-GP
CLK_PCIE_SB# R
CLK_PCIE_SB R
SB_SRC1C_LPRS
SB_SRC1T_LPRS

FS0, FS1, FS2

REF0_2X/SEL_HTT66
REF1_2X/SEL_SATA
REF2_2X/SEL_27

SRC0C_LPRS, SRC0T_LPRS — CLK_SRC0C_LPRS, CLK_SRC0T_LPRS — RN32 SRN0J-6-GP — CLK_NBGPP_CLK# 14, CLK_NBGPP_CLK 14 — **NBGPP(100MHz)**

SRC1C_LPRS, SRC1T_LPRS — CLK_PCIE_WWAN# R, CLK_PCIE_WWAN R — RN31 SRN0J-6-GP — CLK_PCIE_WWAN# 31, CLK_PCIE_WWAN 31 — **WWAN(100MHz)**

SRC2C_LPRS, SRC2T_LPRS — CLK_PCIE_MINI2# R, CLK_PCIE_MINI2 R — TP32, TP31

SRC3C_LPRS, SRC3T_LPRS — CLK_PCIE_LOM# R, CLK_PCIE_LOM R — RN25 SRN0J-6-GP — CLK_PCIE_LOM# 24, CLK_PCIE_LOM 24 — **LOM(100MHz)**

SRC4C_LPRS, SRC4T_LPRS — CLK_PCIE_WLAN# R, CLK_PCIE_WLAN R — RN23 SRN0J-6-GP — CLK_PCIE_WLAN# 31, CLK_PCIE_WLAN 31 — **WLAN(100MHz)**

SRC5C_LPRS, SRC5T_LPRS — CLK_PCIE_EXP# R, CLK_PCIE_EXP R — TP29, TP30

EXPRESS CARD (100MHz)

SRC6C/SATAC_LPRS, SRC6T/SATAT_LPRS

SRC7C_LPRS/27MHZ_NS, SRC7T_LPRS/27MHZ_SS

X01
Change to 0 ohm with D version CLK gen.

CPUKG0T_LPRS, CPUKG0C_LPRS — CPU_CLK R, CPU_CLK# R — RN20 SRN0J-6-GP — CPU_CLK 9, CPU_CLK# 9 — **CPU_CLK(200MHz)**

GND, GNDA, GND48, GNDHTT, GNDCPU, GNDATIG, GNDSRC, GNDSRC, GNDREF, GNDREF, GNDSATA, GNDSB_SRC

HTT0T_LPRS/66M, HTT0C_LPRS/66M

SMBDAT, SMBCLK, PD#

71.09474.A03

+3.3V_RUN

R170 10KR2J-3-GP (DY)

CLOCK_EN# 34

* default

SEL_HTT66 FS0	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA FS1	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock

35 CLK_SIO_14M — R140 33R2J-2-GP

KBC 5035(14MHz)

+3.3V_RUN

R137 8K2R2J-3-GP (DY), R138 8K2R2J-3-GP, R136 8K2R2J-3-GP (DY), R139 8K2R2J-3-GP

NB OSCIN (14MHz)

14 CLK_NB_14M — R171 158R2F-GP — R166 90D9R3F-GP

CLK_NB_14M	
RS780M	1.1V=(90.9/(90.9+158))*3.3V

14 CLK_NBHT_CLK
14 CLK_NBHT_CLK#
RN19 SRN0J-6-GP
CLK_NBHT_CLK_R
CLK_NBHT_CLK# R

CLK_SCLK
CLK_SDATA

+3.3V_RUN, +3.3V_RUN, +3.3V_ALW

RN21 SRN2K2J-1-GP, RN22 SRN2K2J-1-GP

U29 2N7002DW-7F-GP

32 CLK_SCLK — CLK_SCLK — CKG_SMBCLK 34,42

32 CLK_SDATA — CLK_SDATA — CKG_SMBDAT 34,42

<Variant Name>

Wistron Corporation
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Title: Clock generator ICS9LPR474

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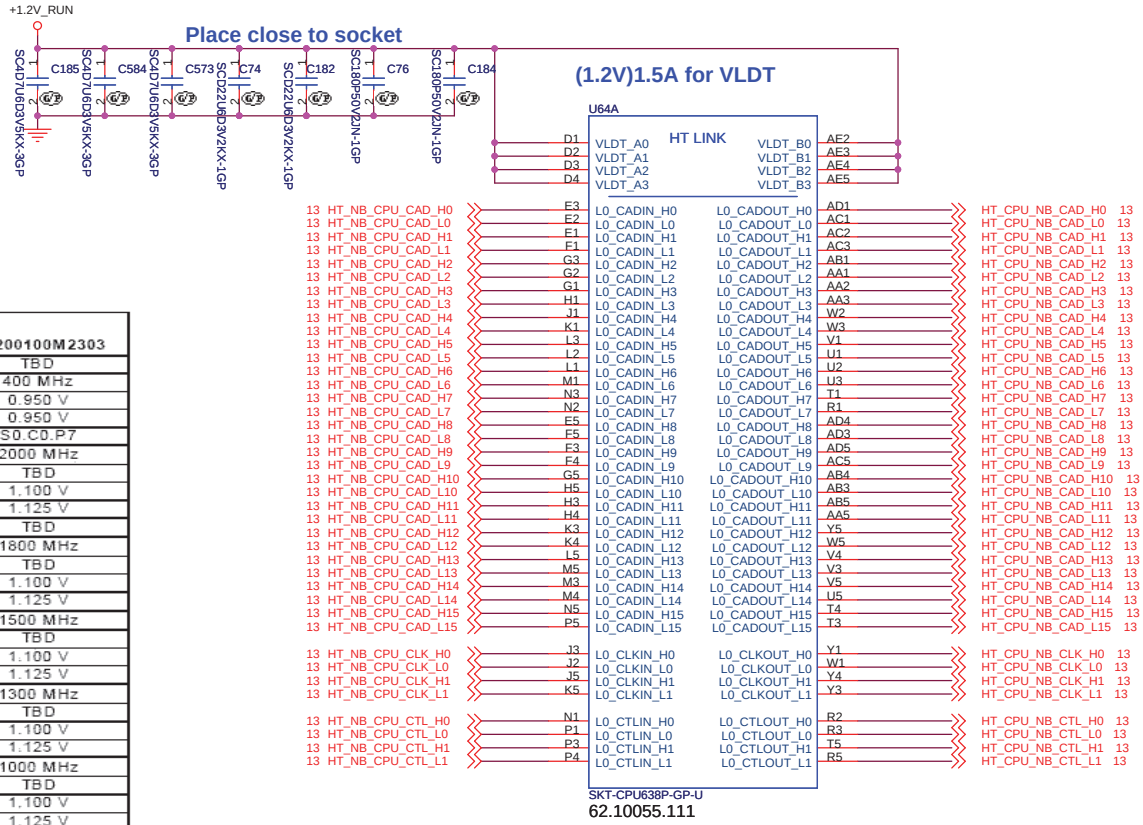
CPU / HT3.0

SSID = CPU



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Variant Name>

Wistron Corporation
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Title: CPU_HT_LINK I/F (1/4)

Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB

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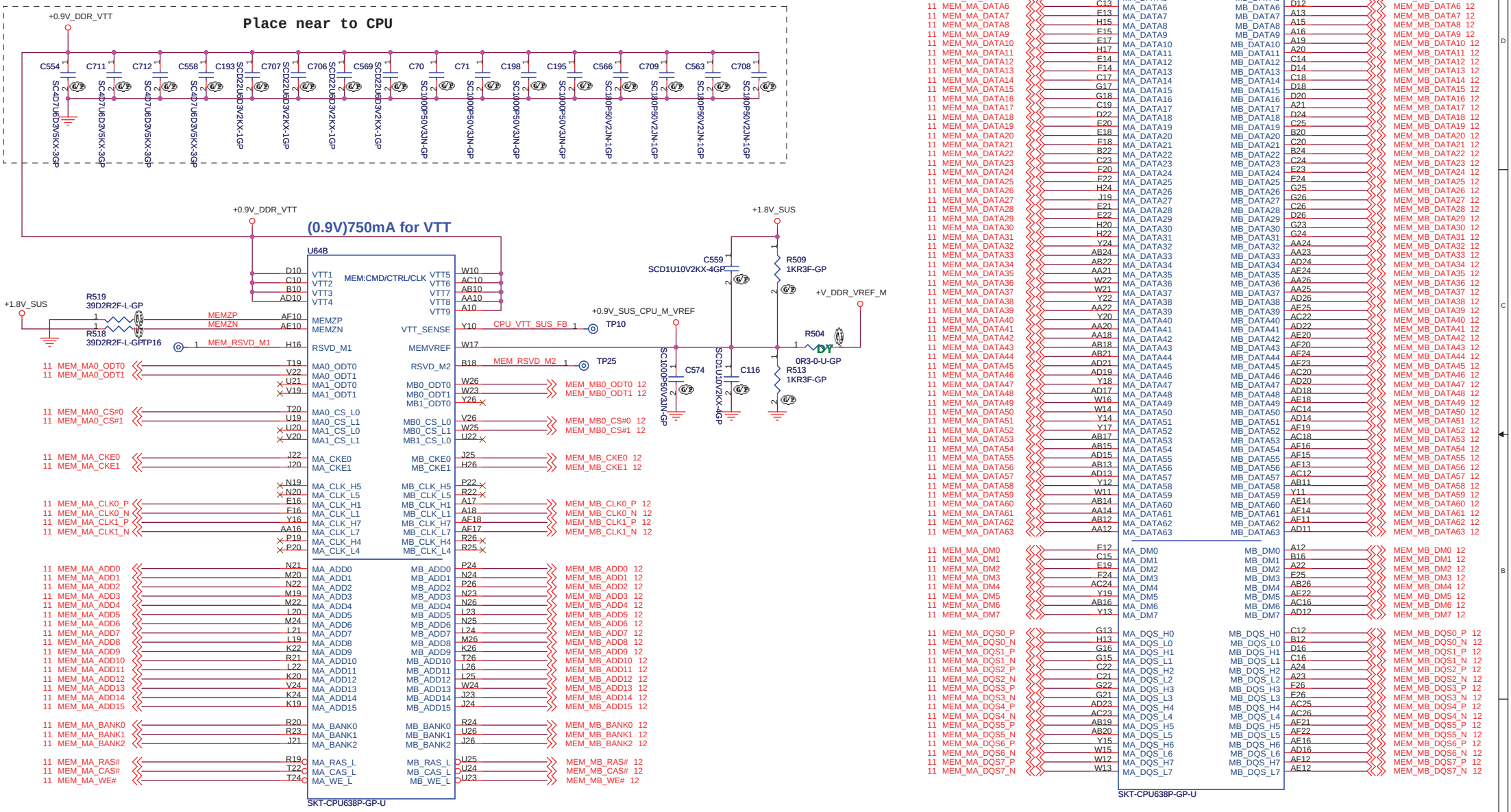
CPU / DDR2

SSID = CPU



<variant_name>

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Title	CPU_DDR_(2/4)	
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SSID = CPU

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

(2.5V)250mA for VDDA

Cloce To CPU

CPU_CLK(200MHz)

For HDT DBG

X01
G.G. list 10/06

X01
Smooth signal.

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

2.09V for Gate

Sideband temperature

CPU temperature sensor
driver INT event to EC

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

CPU exceeds to 125℃

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

HDT Connectors

SKT-CPU638P-GP-U

SMC-CONN26A-FP
20.F0357.025

<Variant Name>

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Title: CPU_Control&Debug_(3/4)

Size	Document Number	Rev
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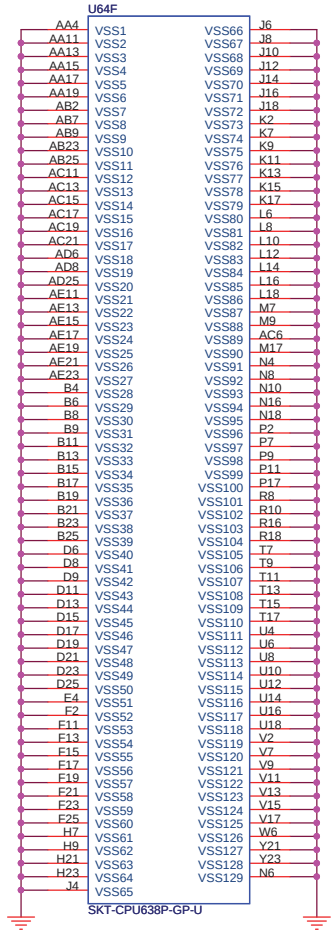
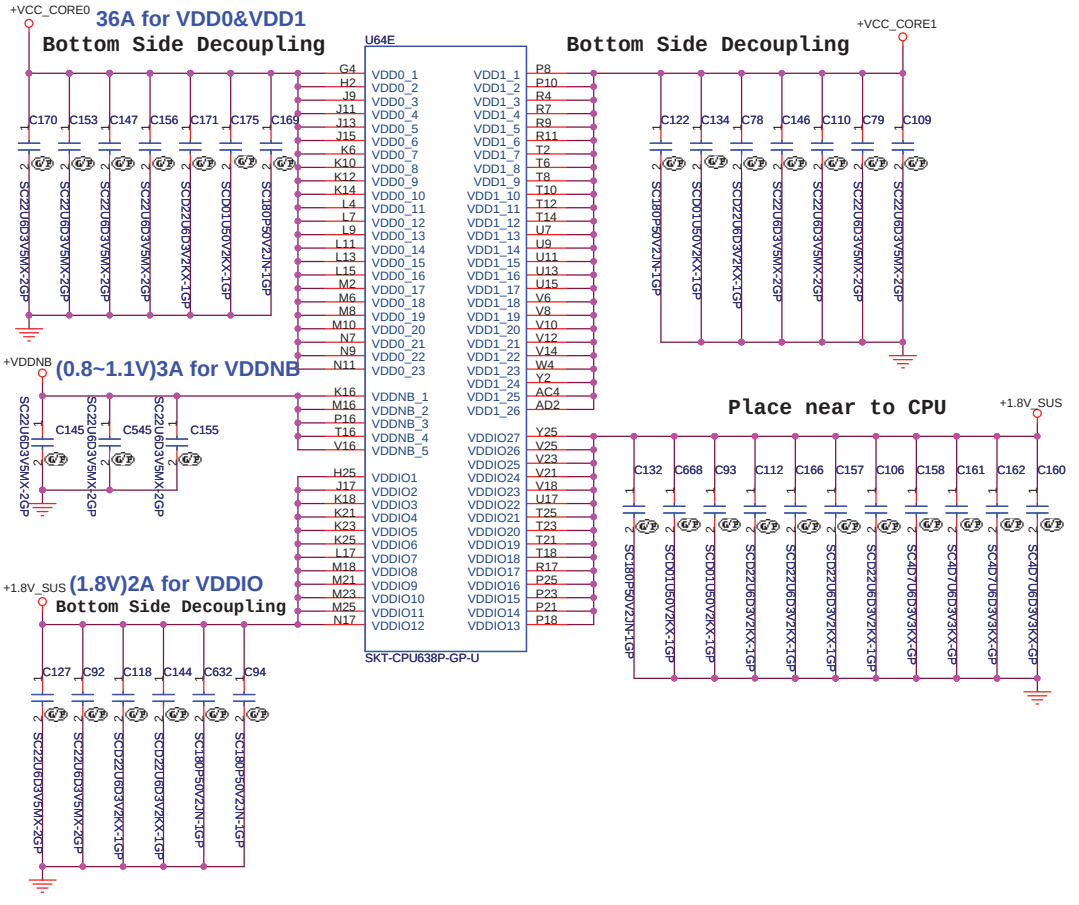
SSID = CPU





<Variant Name>

Wistron Corporation
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Title	CPU_Power_(4/4)	
Size: A3	Document Number: FOOSE-AMD 15.4"	Rev: SB
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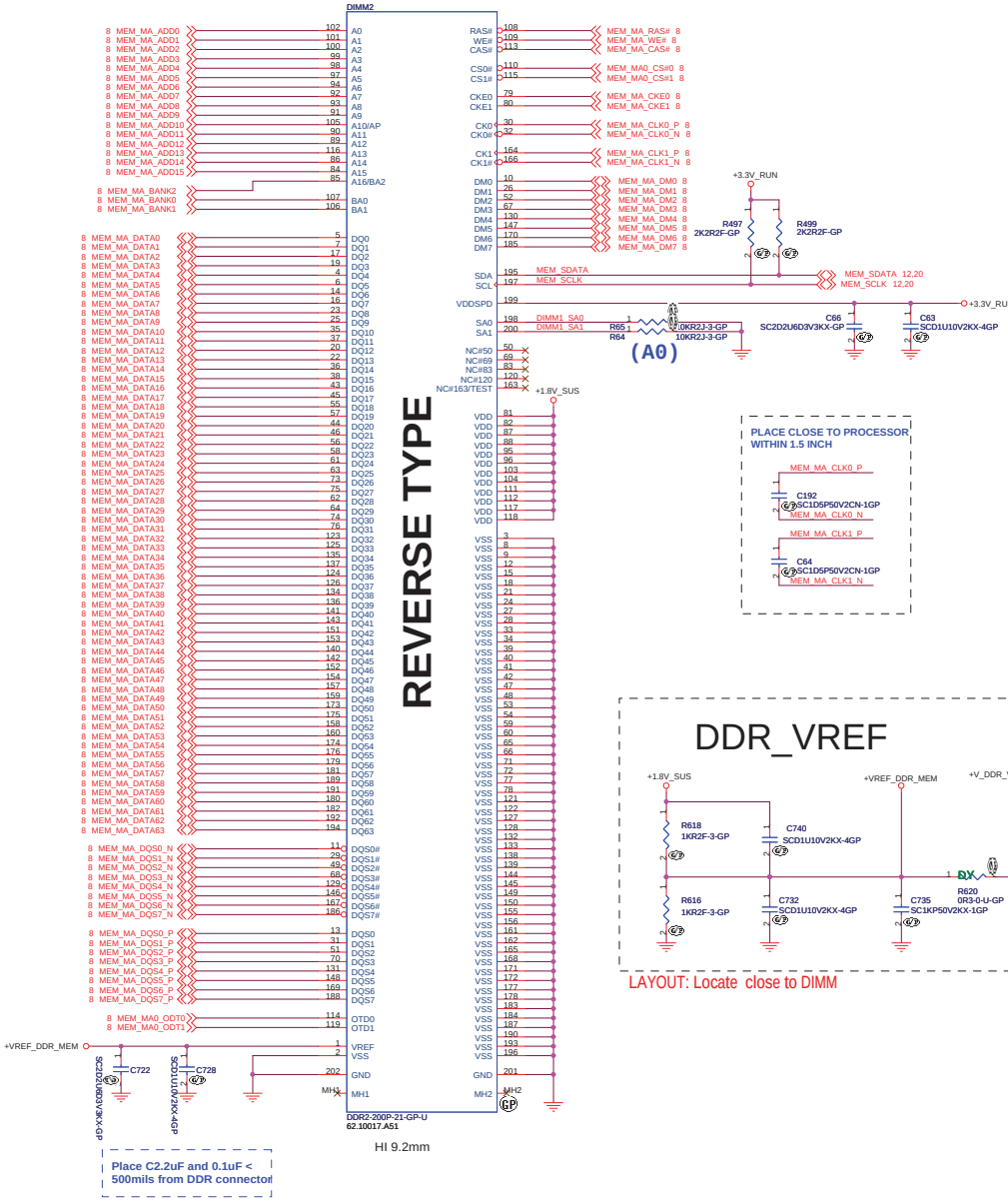
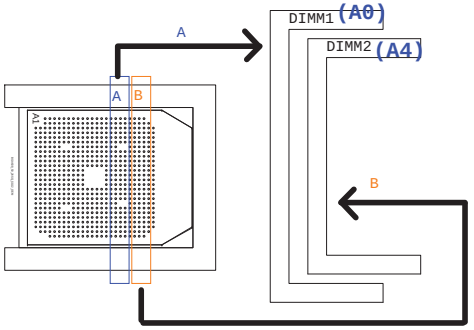
SSID = MEMORY

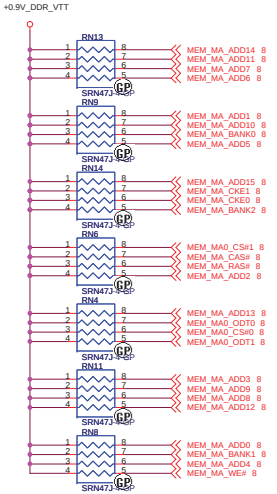




PARALLEL TERMINATION

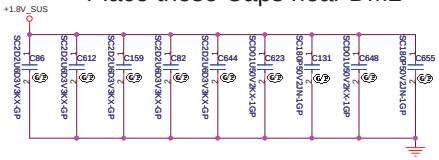
Put decap near power(0.9V) and pull-up resistor

Do not share the Term resistor between the DDR addess and Control Signals.

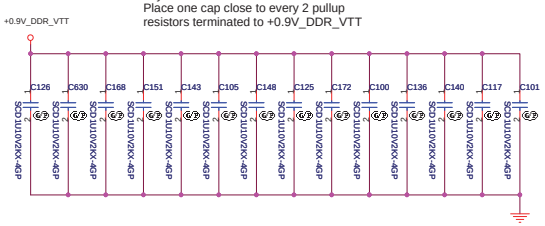


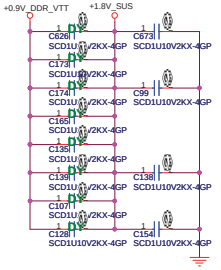
Decoupling Capacitor

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT





DDR_VREF

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR DIMM1

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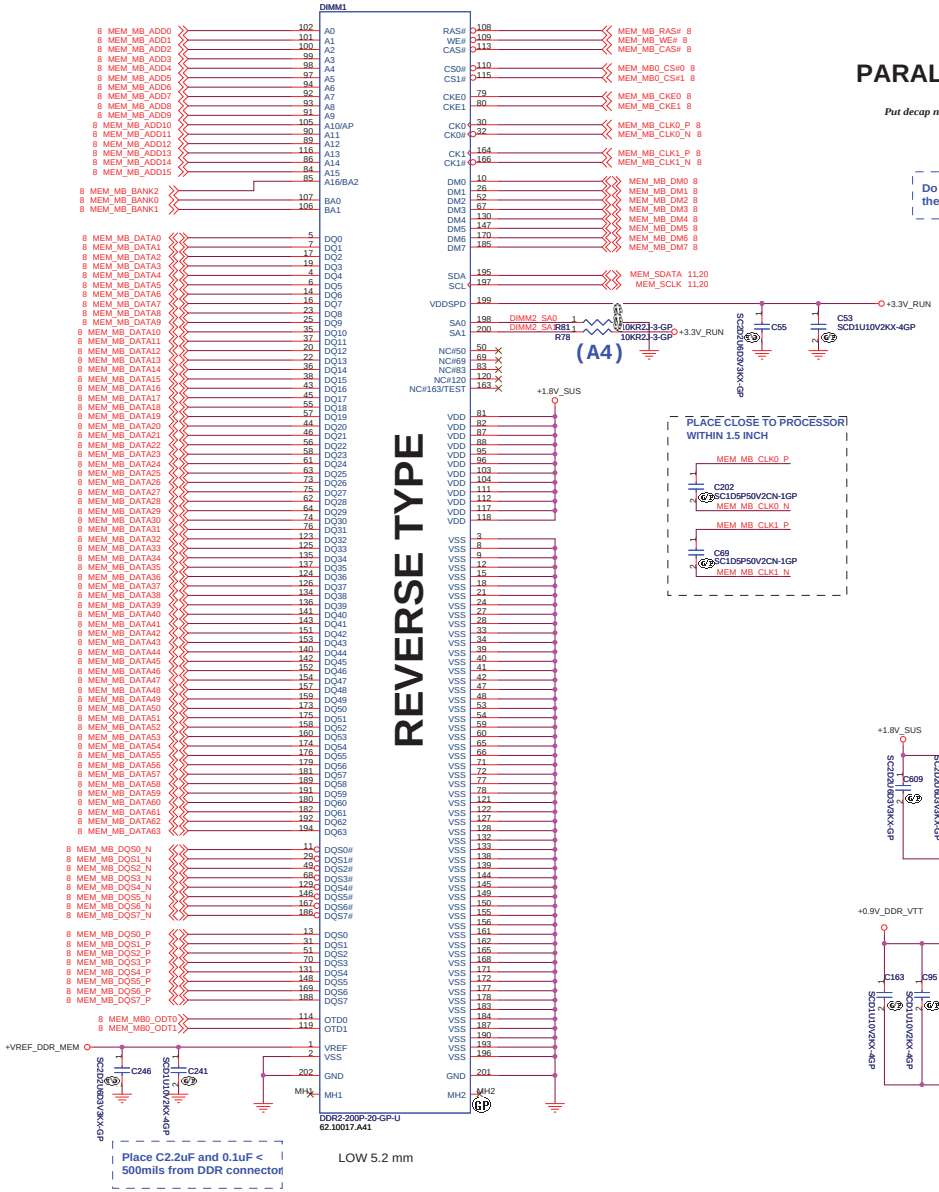
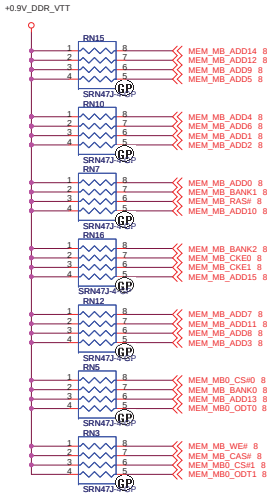
SSID = MEMORY



PARALLEL TERMINATION

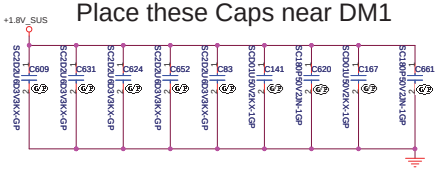
Put decap near power(0.9V) and pull-up resistor

Do not share the Term resistor between the DDR addess and Control Signals.

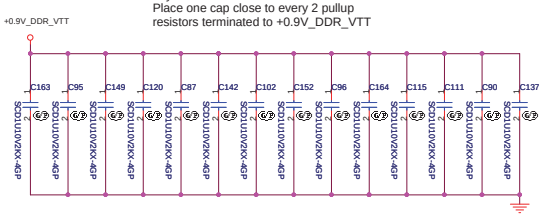


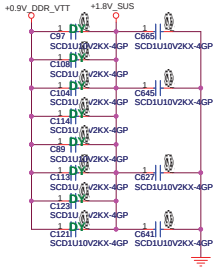
Decoupling Capacitor

Place these Caps near DM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT





<Variant Name>

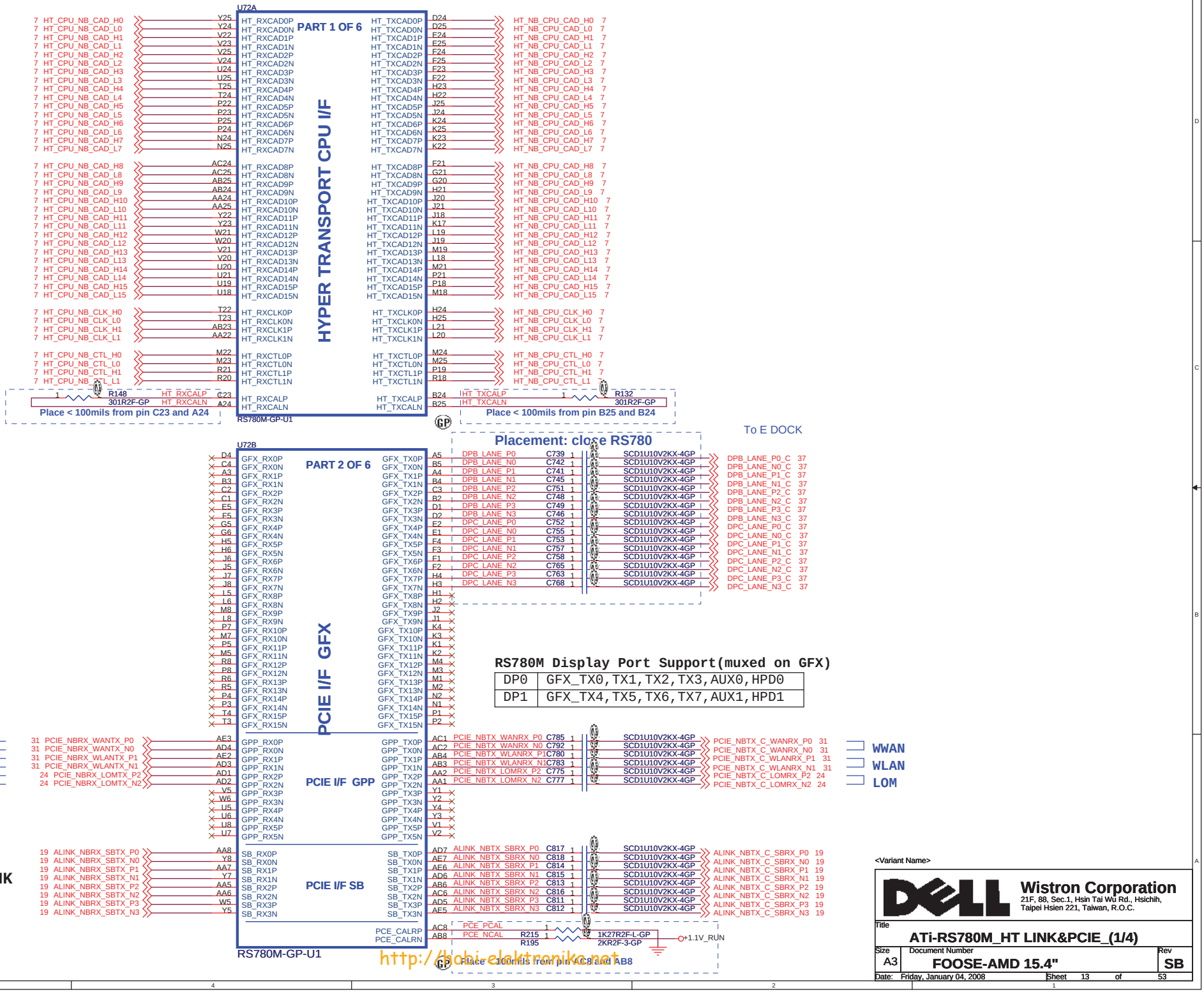
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR DIMM2

Size	Document Number	Rev
A2	FOOSE-AMD 15.4"	SB

Date: Friday, January 04, 2008 Sheet 12 of 53

SSID = N.B



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ATi-RS780M_HT LINK&PCIE_(1/4)	
Size: A3	Document Number: FOOSE-AMD 15.4"	Rev: SB
Date: Friday, January 04, 2008	Sheet 13 of 53	

SSID = N.B

Close to NB ball

STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC)
0 : Enable * 1 : Disable

RS780: Enables Side port memory (RS780 use HSYNC)

*0 : Enable 1 : Disable

SUS_STAT#

Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

Remove R240 at X01.
G.G list 10/06.

ENABLE External CLK GEN

	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.0V	1.1V

X01
AMD schematic review 11/19.

pull up from SB

Ati:0~30n sec

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_LVDS&CRT_(2/4)

Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB

Date: Friday, January 04, 2008 | Sheet 14 of 53

SSID = N.B

+1.8V_RUN — L58 BLM21PG221SN-1GP — 220 ohm @ 100MHz,2A — +1.8V_MEM_VDDQ

TC19 DY ST330U2D5VCM-GP

C300 SC10U6D3V5KX-1GP; C788 SC10U6D3V5KX-1GP; C798 SC1U10V2KX-4GP; C784 SC1U10V2KX-4GP; C834 SC1U6D3V2KX-GP; C833 SC1U6D3V2KX-GP

U72D — PAR 4 OF 6 — SBD_MEM/DVO_I/F — RS780M-GP-U1

MEM_A0	AB12	MEM_A0	MEM_DQ0/DVO_VSYNC AA18 MEM_DQ0
MEM_A1	AE16	MEM_A1	MEM_DQ1/DVO_HSYNC AA20 MEM_DQ1
MEM_A2	V11	MEM_A2	MEM_DQ2/DVO_DE AA19 MEM_DQ2
MEM_A3	AE15	MEM_A3	MEM_DQ3/DVO_D0 Y19 MEM_DQ3
MEM_A4	AA12	MEM_A4	MEM_DQ4 V17 MEM_DQ4
MEM_A5	AB16	MEM_A5	MEM_DQ5/DVO_D1 AA17 MEM_DQ5
MEM_A6	AB14	MEM_A6	MEM_DQ6/DVO_D2 AA15 MEM_DQ6
MEM_A7	AD14	MEM_A7	MEM_DQ7/DVO_D4 Y15 MEM_DQ7
MEM_A8	AD13	MEM_A8	MEM_DQ8/DVO_D3 AC20 MEM_DQ8
MEM_A9	AD15	MEM_A9	MEM_DQ9/DVO_D5 AD19 MEM_DQ9
MEM_A10	AC16	MEM_A10	MEM_DQ10/DVO_D6 AE22 MEM_DQ10
MEM_A11	AE13	MEM_A11	MEM_DQ11/DVO_D7 AC18 MEM_DQ11
MEM_A12	AC14	MEM_A12	MEM_DQ12 AB20 MEM_DQ12
MEM_A13	Y14	MEM_A13	MEM_DQ13/DVO_D9 AD22 MEM_DQ13
			MEM_DQ14/DVO_D10 AC22 MEM_DQ14
MEM_BA0	AD16	MEM_BA0	MEM_DQ15/DVO_D11 AD21 MEM_DQ15
MEM_BA1	AE17	MEM_BA1	
MEM_BA2	AD17	MEM_BA2	MEM_DQS0P/DVO_IDCKP Y17 MEM_DQS0P
			MEM_DQS0N/DVO_IDCKN W18 MEM_DQS0N
RAS#	W12	MEM_RAS#	MEM_DQS1P AD20 MEM_DQS1P
CAS#	Y12	MEM_CAS#	MEM_DQS1N AE21 MEM_DQS1N
WE#	AD18	MEM_WE#	
CS#	AB13	MEM_CS#	MEM_DM0 W17 MEM_DM0
CKE	AB18	MEM_CKE	MEM_DM1/DVO_D8 AE19 MEM_DM1
ODT	V14	MEM_ODT	
			IOPLLVDD18 AE23 +1.8V_IOPLLVDD18
MEM_CLKP	V15	MEM_CKP	IOPLLVDD AE24 +1.1V_IOPLLVDD
MEM_CLKN	W14	MEM_CKN	
			IOPLLVSS AD23
MEM_COMPP	AE12	MEM_COMPP	
MEM_COMPN	AD12	MEM_COMPN	MEM_VREF AE18 MEM_VREF_NB

TP27

+1.8V_MEM_VDDQ — R663 40D2R2F-GP — R660 40D2R2F-GP — MEM_COMPP AE12 — MEM_COMPN AD12

MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

15 mils width — L64 BLM15AG221SN-GP — +1.8V_RUN — C821 SC2D2U6D3V3KX-GP

15 mils width — L60 BLM15AG221SN-GP — +1.1V_RUN — C787 SC2D2U6D3V3KX-GP — C794 SCD1U10V2KX-4GP

+1.8V_MEM_VDDQ — R661 1KR2F-3-GP — C809 SCD1U10V2KX-4GP — R654 1KR2F-3-GP — C820 SCD1U10V2KX-4GP

U34 — HY5PS121621CFP-25-GP

MEM_BA0	L2	BA0	DQ15 B9 MEM_DQ15
MEM_BA1	L3	BA1	DQ14 B1 MEM_DQ14
			DQ13 D9 MEM_DQ13
MEM_A12	R2	A12	DQ12 D1 MEM_DQ12
MEM_A11	P7	A11	DQ11 D3 MEM_DQ11
MEM_A10	M2	A10/AP	DQ10 D7 MEM_DQ10
MEM_A9	P3	A9	DQ9 C2 MEM_DQ9
MEM_A8	P8	A8	DQ8 C8 MEM_DQ8
MEM_A7	P2	A7	DQ7 F9 MEM_DQ7
MEM_A6	N7	A6	DQ6 F1 MEM_DQ6
MEM_A5	N3	A5	DQ5 H9 MEM_DQ5
MEM_A4	N8	A4	DQ4 H1 MEM_DQ4
MEM_A3	N2	A3	DQ3 H3 MEM_DQ3
MEM_A2	M7	A2	DQ2 H7 MEM_DQ2
MEM_A1	M3	A1	DQ1 G2 MEM_DQ1
MEM_A0	M8	A0	DQ0 G8 MEM_DQ0
MEM_CLKN	K8	CK	VDDQ1 A9
MEM_CLKP	J8	CK	VDDQ2 C1
CKE	K2	CKE	VDDQ3 C3
			VDDQ4 C7
CS#	L8	CS	VDDQ5 C9
WE#	K3	WE	VDDQ6 F9
RAS#	K7	RAS	VDDQ7 G1
CAS#	L7	CAS	VDDQ8 G3
MEM_DM0	F3	LDM	VDDQ9 G7
MEM_DM1	B3	UDM	VDDQ10 G9
ODT	K9	ODT	VDD1 A1
			VDD2 F1
MEM_DQS0P	F7	LDQS	VDD3 J9
MEM_DQS0N	F8	LDQS	VDD4 M9
			VDD5 R1
MEM_DQS1P	B7	UDQS	VDDL J1
MEM_DQS1N	A8	UDQS	VSSDL J7
MEM_VREF_CHIP	J2	VREF	VSSQ1 A7
			VSSQ2 B2
	A2	NC#A2	VSSQ3 B8
	E2	NC#E2	VSSQ4 D2
	L1	NC#L1	VSSQ5 D8
	R3	NC#R3	VSSQ6 E7
	R7	NC#R7	VSSQ7 F2
	R8	NC#R8	VSSQ8 F8
			VSSQ9 H2
MEM_BA2			VSSQ10 H8
			VSS1 A3
			VSS2 E3
			VSS3 J3
			VSS4 N1
			VSS5 P9

R667 100R2F-L1-GP-U

+1.8V_MEM_VDDQ

L59 BLM18AG601SN-3GP — 600 ohm @ 100MHz,200mA — VDDL_VRAM

C786 SC1U6D3V3KX-1GP

Layout Note: 50 mil for VSSDL

+1.8V_MEM_VDDQ — R646 1KR2F-3-GP — C804 SCD1U10V2KX-4GP — R643 1KR2F-3-GP — C797 SCD1U10V2KX-4GP

+0.9V_MEM_VTT

RN53 SRN47J-4GP: CS# MEM_A0 MEM_A4 MEM_A8 — C375 SC10U6D3V5KX-1GP; C324 SCD1U10V2KX-4GP; C325 SCD1U10V2KX-4GP

RN36 SRN47J-4GP: RAS# CAS# MEM_A11 MEM_A6 — C352 SCD1U10V2KX-4GP; C348 SCD1U10V2KX-4GP

RN29 SRN47J-4GP: MEM_A12 MEM_A7 MEM_A3 MEM_BA0 — C363 SCD1U10V2KX-4GP; C355 SCD1U10V2KX-4GP

RN47 SRN47J-4GP: MEM_BA1 WE# MEM_A10 MEM_BA2 — C366 SCD1U10V2KX-4GP; C374 SCD1U10V2KX-4GP

RN35 SRN47J-4GP: MEM_A2 MEM_A1 MEM_A5 MEM_A9 — C822 SCD1U10V2KX-4GP; C806 SCD1U10V2KX-4GP

RN27 SRN47J-4GP: CKE ODT — C825 SCD1U10V2KX-4GP; C830 SCD1U10V2KX-4GP

+1.8V_MEM_VDDQ

Design current: 1400mA
Max current: 2000mA

+15V — 49 1.8V_RUN_ENABLE — U27 SI3456BDV-T1-GP — 2Amp

+0.9V_DDR_VTT — +0.9V_MEM_VTT

C262 SC470P50V2KX-3GP DY — C280 SC10U6D3V5KX-1GP

Local Frame Buffer Strapping List
Copy from Becks.

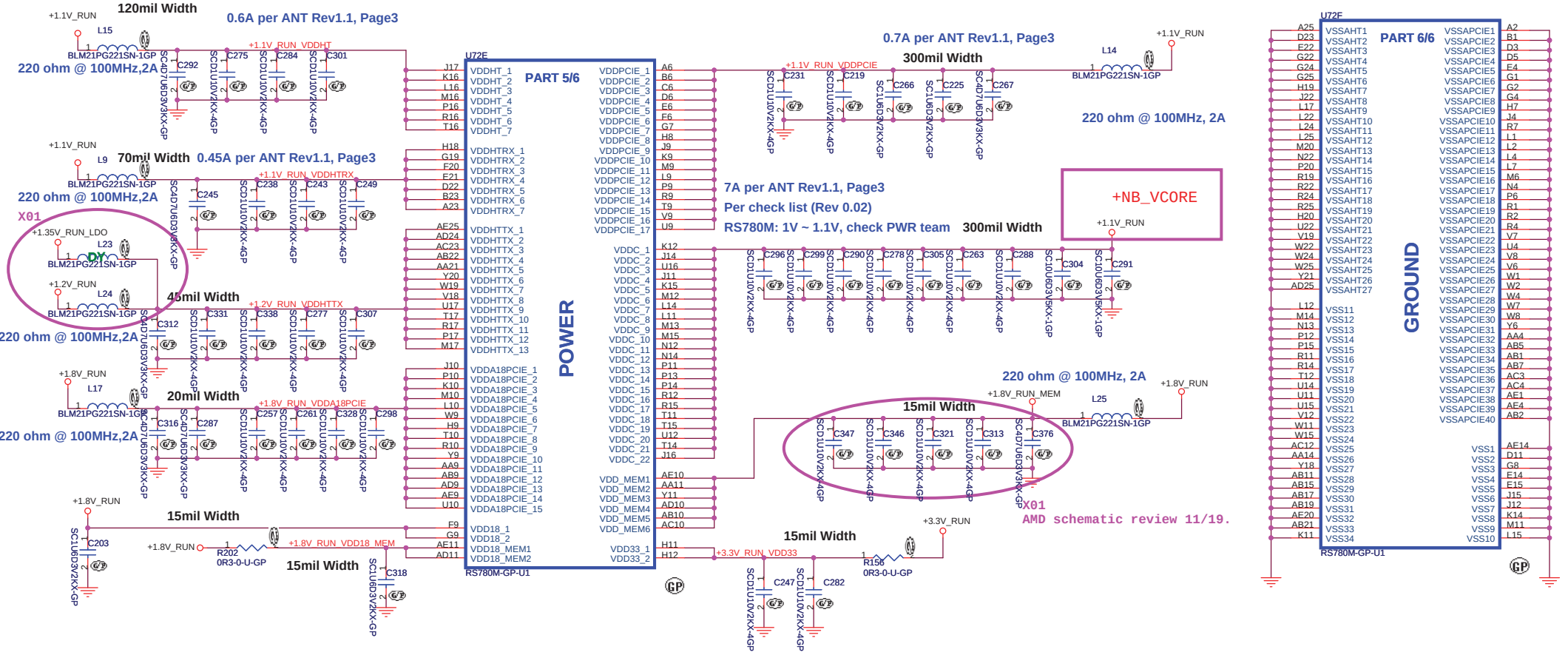
	LFB_ID2	LFB_ID1	LFB_ID0	Vendor Part Number	Wistron Part Number
Hynix	0	0	0	HY5PS121621CFP-25	72.51216.F0U
Main Source Qimonda	0	0	1	HYB18T512161B2F-25	72.18512.M0U
2nd Source Samsung	0	1	0	K4N51163QE-ZC25	72.45116.A0U

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 14_ATi-RS780M_SidePort_(3/4)
Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB
Date: Friday, January 04, 2008 | Sheet 15 of 53

SSID = N.B

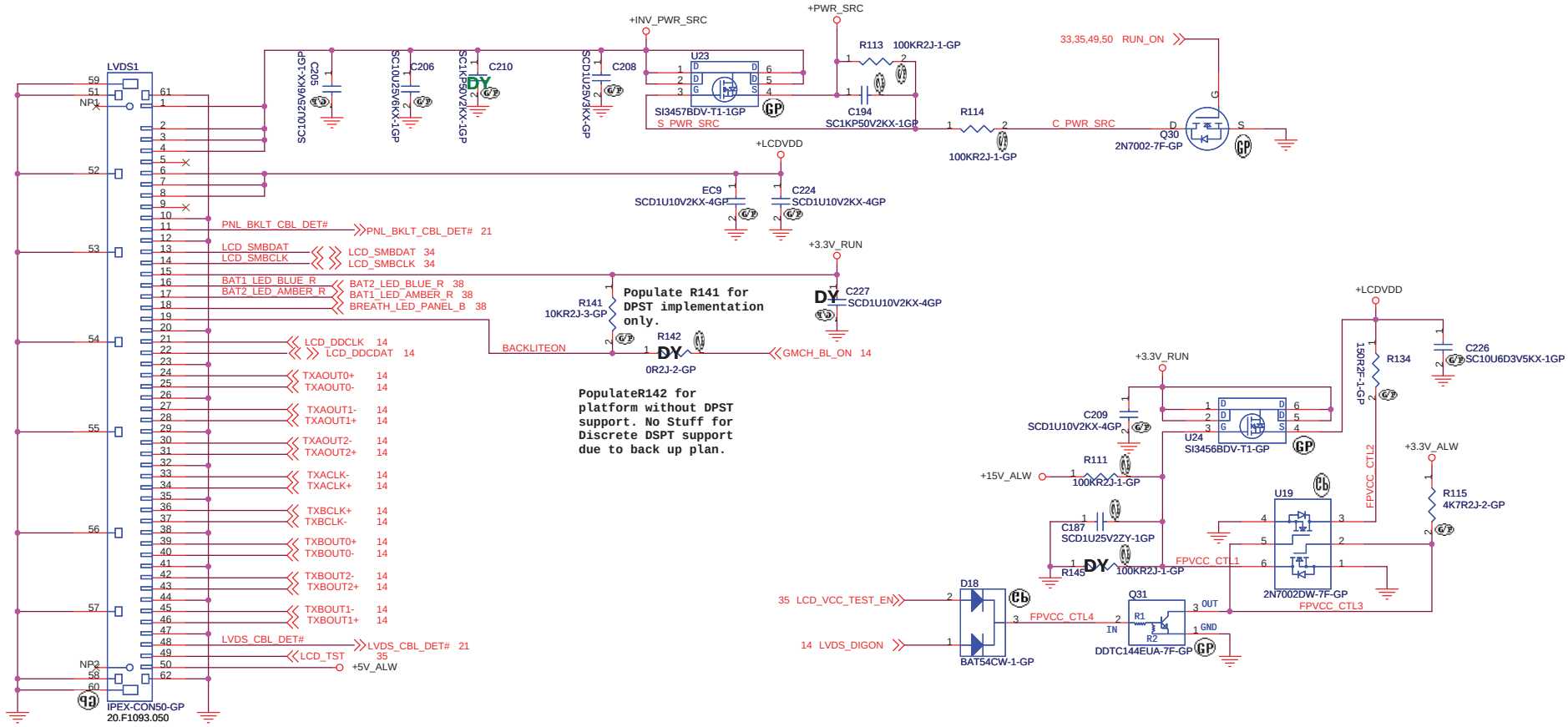


<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ATi-RS780M_PWR&GD_(4/4)	
Size: A3	Document Number: FOOSE-AMD 15.4"	Rev: SB
Date: Friday, January 04, 2008	Sheet 16 of 53	

SSID = VIDEO



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD Connector	
Size: A3	Document Number: FOOSE-AMD 15.4"	Rev: SB
Date: Friday, January 04, 2008	Sheet 17 of 53	

CRT I/F & CONNECTOR

SSID = VIDEO

X01
The solution of leakage.

X01
CRT EA solution.

X01
Remove S-vedio function from DOCK.

X01
TV EA solution.

S-Video I/F & CONNECTOR

Hsync & Vsync level shift

S-Video Connector

X01
G.G list 10/06.

CRT_MUX_SWITCH		
SEL	CRT	TV
0	MB	Dock
1	Dock	MB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<variant_name>

Title: CRT Connector
Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB
Date: Friday, January 04, 2008 | Sheet 18 of 53

SSID = S.B

X01
0R2J-2-GP
R322
14,34,35,50 PLTRST#
NB_RST#

U81A
SB700
Part 1 of 5
A_RST#

ALINK_NBRX_SBTX_P0 … ALINK_NBRX_SBTX_N3 — SCD1U10V2KX-4GP
ALINK_NBRX_C_SBTX_P0 … ALINK_NBRX_C_SBTX_N3
PCIE_TX0P … PCIE_TX3N

ALINK_NBTX_C_SBRX_P0 … ALINK_NBTX_C_SBRX_N3
PCIE_RX0P … PCIE_RX3N

R269 562R2F-GP PCIE_CALRP
R267 2K05R2F-GP PCIE_CALRN
PCIE_CALRP
PCIE_CALRN
PCIE_PVDD 40mA
PCIE_PVSS

PCI EXPRESS INTERFACE

+1.2V_RUN
+1.2V_RUN_PCIE_PVDD
+1.2V_PCIE_VDDR
L31
BLM21PG221SN-1GP
200 ohm 2A
20mil Width
C391
SC2D2U6D3V3KX-GP
Place R <100mils form pins T25,T24

X01
AMD schematic review 11/19.

PU to +1.8V_SUS
+5V_ALW
+3.3V_ALW
R679 10KR2J-3-GP
R691 10KR2J-3-GP
CPU_PWRGD#
CPU_PWRGD_Q 34
CPU_PWRGD
R672 1KR2F-3-GP
CPU_PWRGD_R
Q79 MMBT3904-7-F-GP NPN
Q81 2N7002-7F-GP
Place the translation circuit for CPU_PWRGD close to the SB700 to minimize stubbs when the circuit is No Stuff.

6 CLK_PCIE_SB
6 CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
25M_48M_66M_OSC
25M_X1
25M_X2

CLOCK GENERATOR

R757 DX 20MR3-GP
C880 SC12P50V2JN-3GP
32K_X1
R758 20MR3-GP
X7 X-32D768KHZ-38GPU
C882 SC12P50V2JN-3GP
32K_X2
0R2J-2-GP R754
32K_X2_R
+1.8V_RUN
R659 300R2J-4-GP
X01
AMD schematic review 11/19.

X1
X2
RTC XTAL

9,14 ALLOW_LDTSTOP
9 CPU_PROCHOT#
9 CPU_PWRGD
9 CPU_LDT_STOP#
9 CPU_LDT_RST#
ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#

CPU

SB700-1-GP-U

PCI CLKS
PCICLK0 … PCICLK4
PCICLK5/GPIO41
PCI_CLK0_R … PCI_CLK5_R
R336 … R330 49D9R2F-GP
CLK_PCI_DOCK 37
CLK_PCI_LOM 23,24
CLK_PCI_5035 23,34
CLK_PCI_5028 23,35
CLK_PCI_PCCARD 23,26
C_TPM_LCLK 25

X01
C459 C462 C458 C461 C463 C650
DY DY DY DY DY
SC22P50V2JN-4GP … SC12P50V2JN-3GP

PCIRST#
PCIRST# SB
R340 33R2J-2-GP
PCI_RST# 26,37

X01
Delete RP1 by AMD suggestion.

PCI INTERFACE
AD0 … AD31
PCI_AD0 … PCI_AD31 26 / 23,26
CBE0# … CBE3#
PCI_C/BE#0 … PCI_C/BE#3 26
FRAME#
PCI_FRAME# 26
DEVSEL#
IRDY#
TRDY#
PAR
STOP#
PERR#
SERR#
PCI_DEVSEL# … PCI_SERR# 26

REQ0# … REQ2#
PCI_REQ0# TP97
PCI_REQ2# TP54
PCI_REQ1# 26
REQ3#/GPIO70
REQ4#/GPIO71
KB_DET# TP57
PCI_GNT0# TP98
BIO_DET# 38
GNT0# … GNT2#
SB700_GNT2# TP52
PCI_GNT1# 26
CDD_VDD_ON
GNT3#/GPIO72
GNT4#/GPIO73
CLKRUN#
LOCK#
PCI_LOCK# TP49
PM_CLKRUN# 25,26,34,35

INTE#/GPIO33 … INTH#/GPIO36
PCI_PIRQA# … PCI_PIRQD#
PCI_PIRQA# … PCI_PIRQC# 26
TP155

LPC
LPCCLK0 G22
LPCCLK1 E22
LPCCLK0_R R690 22R2J-2-GP
LPCCLK1_R R681 22R2J-2-GP
LPCCLK0 23
LPCCLK1 23
LAD0 … LAD3
LPC_LAD0 … LPC_LAD3 24,25,34,35
LFRAME#
LPC_LFRAME# 24,25,34,35
LDRQ0#
LPC_LDRQ0# 35
LDRQ1#/GNT5#/GPIO68
LPC_LDRQ1# 35
BMREQ#/REQ5#/GPIO65
SB700_GPIO65
R298 8K2R2J-3-GP
+3.3V_RUN
SERIRQ
IRQ_SERIRQ 24,25,26,34,35

RTC
RTCCLK
INTRUDER_ALERT#
VBAT
RTCCLK
+VBAT_IN
R765 49K9R2F-1-GP DY
+RTC_CELL
R770 510R2J-1-GP
X01
C898 SCU1U603V2KX-GP
C897 SCD1U16V2KX-3GP

BIO_DET#
R297 100KR2J-1-GP
+3.3V_RUN
CDD_VDD_ON
R308 DX 100KR2J-1-GP
R307 10KR2J-3-GP DY
+COIN_CELL
R534 1MR2F-GP
RTC_BAT_DET#
R548 DY 0R2J-2-GP
RTC_BAT_DET# R
Q68 2N7002-7F-GP
R551 1KR2J-1-GP

SSID =RBATT

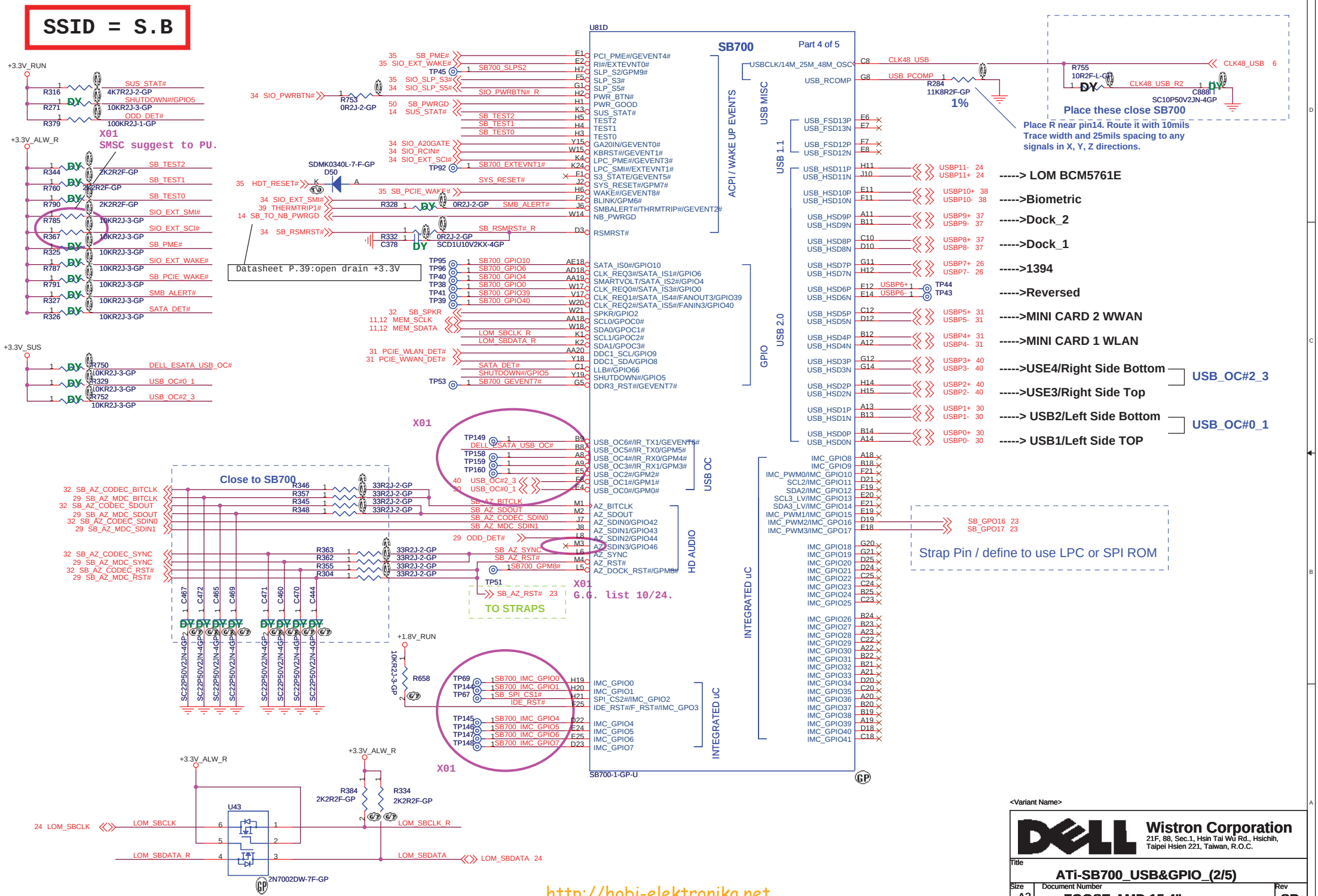
+3.3V_ALW_2
R541 0R2J-2-GP
+COIN_CELL
D38 BAT54CW-1-GP
+3.3V_ALW_2_R
VBAT_R
R537 390R2J-1-GP
RTC_BAT_DET# R
VBAT
RTC1
MLX-CON3-9-GP
20.D0198.103
EC16 SC100P50V2JN-3GP
EC17 SCD1U16V2KX-3GP

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_PCIE&PCI_(1/5)
Size: A3
Document Number: FOOSE-AMD 15.4"
Rev: SB
Date: Friday, January 04, 2008
Sheet 19 of 53

SSID = S.B



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_USB&GPIO_(2/5)

Size	Document Number	Rev
A3	FOOSE-AMD 15.4"	SB

Date: Friday, January 04, 2008 Sheet 20 of 53

SSID = S.B

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

U81B

SB700
Part 2 of 5

SATA HDD
SATA ODD
Dock eSATA

X01

SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR

SB700-1-GP-U

X01
AMD schematic review 11/19.

X01
G.G. list 10/24.

X01
G.G. list 11/07.

LFB_ID0 to LFB_ID2 got internal PU to S5.

Layout connect to Cap then GND

Local Frame Buffer Strapping List
Copy from Becks.

	LFB_ID2	LFB_ID1	LFB_ID0	Vendor Part Number
Hynix	0	0	0	HY5PS121621CFP-25
Main Qimonda	0	0	1	HYB18T512161B2F-25
2nd Samsung	0	1	0	K4N51163QE-ZC25

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_SATA-IDE_(3/5)
Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB
Date: Friday, January 04, 2008 | Sheet 21 of 53

SSID = S.B

U81C SB700 Part 3 of 5

POWER

X01 AMD schematic review 11/19.

Use Flash I/O:+1.8V / IDE:+3.3V

50mil Width

220 ohm 2A

Use Plane Shape for +3.3V_AVDD_USB

AVDDTX:330mA
AVDDRT:209mA

Design current: 682mA

U81E SB700 Part 5 of 5 GROUND

SB700-1-GP-U

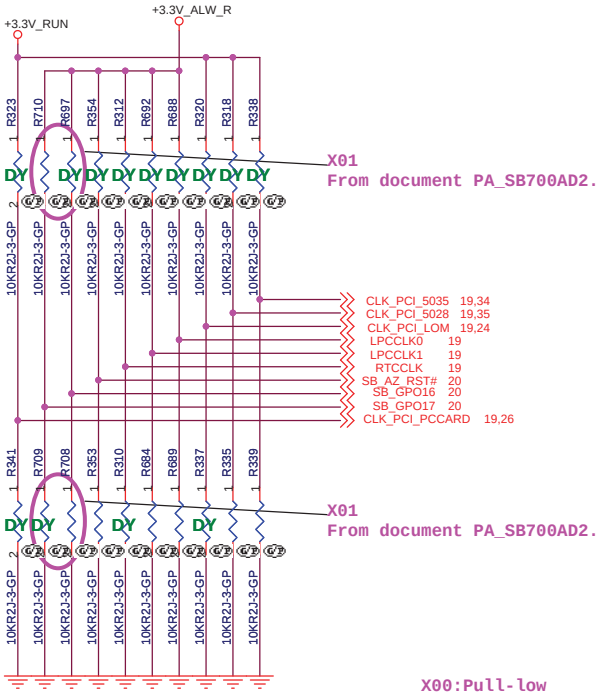
http://hobi-elektronika.net

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_POWER&GND_(4/5)
Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB
Date: Friday, January 04, 2008 | Sheet 22 of 53

SSID = S.B

REQUIRED STRAPS



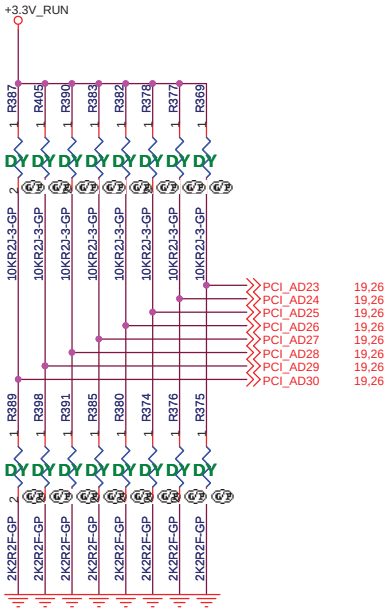
REQUIRED SYSTEM STRAPS

X00:Pull-low
X01:Pull-low
From document PA_SB700AD2

	CLK_PCI_5035	CLK_PCI_5028	CLK_PCI_LOM CLK_PCI_PCCARD	LPCCLK0	LPCCLK1	RTCCLK	AZ_RST#	SB_GPO17 , SBGPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

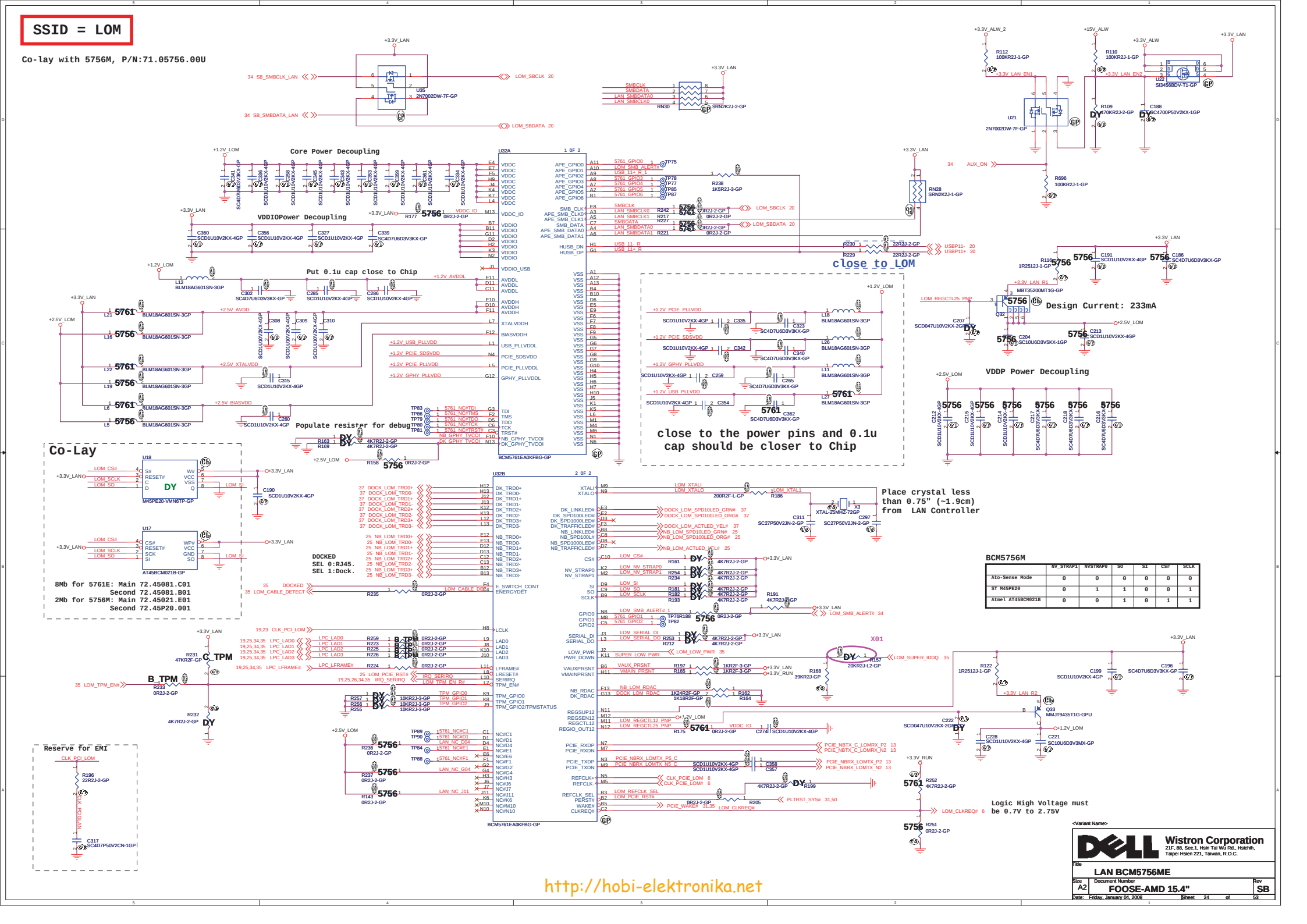
Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB

Date: Friday, January 04, 2008 | Sheet 23 of 53

SSID = LOM

Co-lay with 5756M, P/N:71.05756.00U

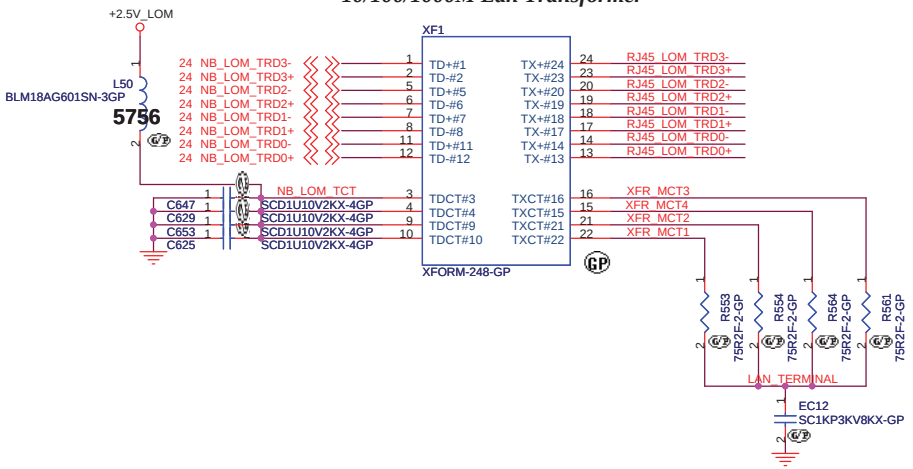


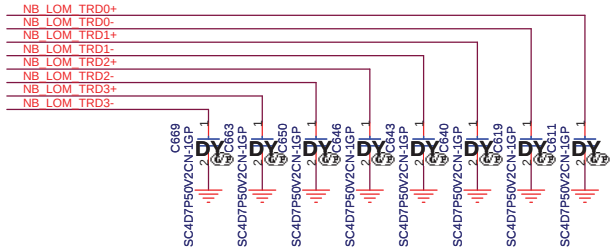
	NV_STRAP1	NVSTRAP0	SO	SI	CS#	SCLK
Ato-Sense Mode	0	0	0	0	0	0
ST M45PE20	0	1	1	0	0	1
Atmel AT45BCM021B	0	0	1	0	1	1

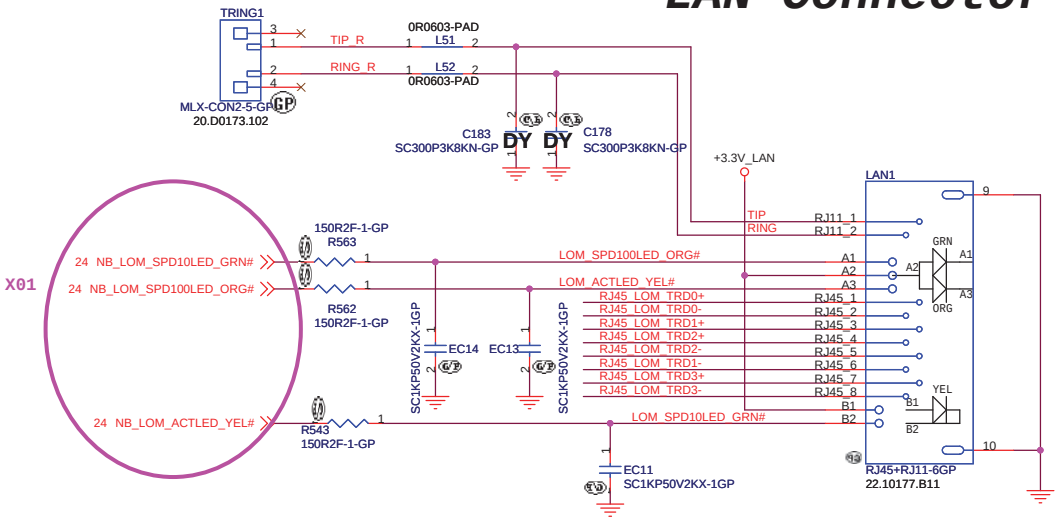
SSID = LOM

LAN Connector

10/100/1000M Lan Transformer







The blowout from the LAN magnetics to the RJ45 connector maintining the distance between the two to be within 1 inch.

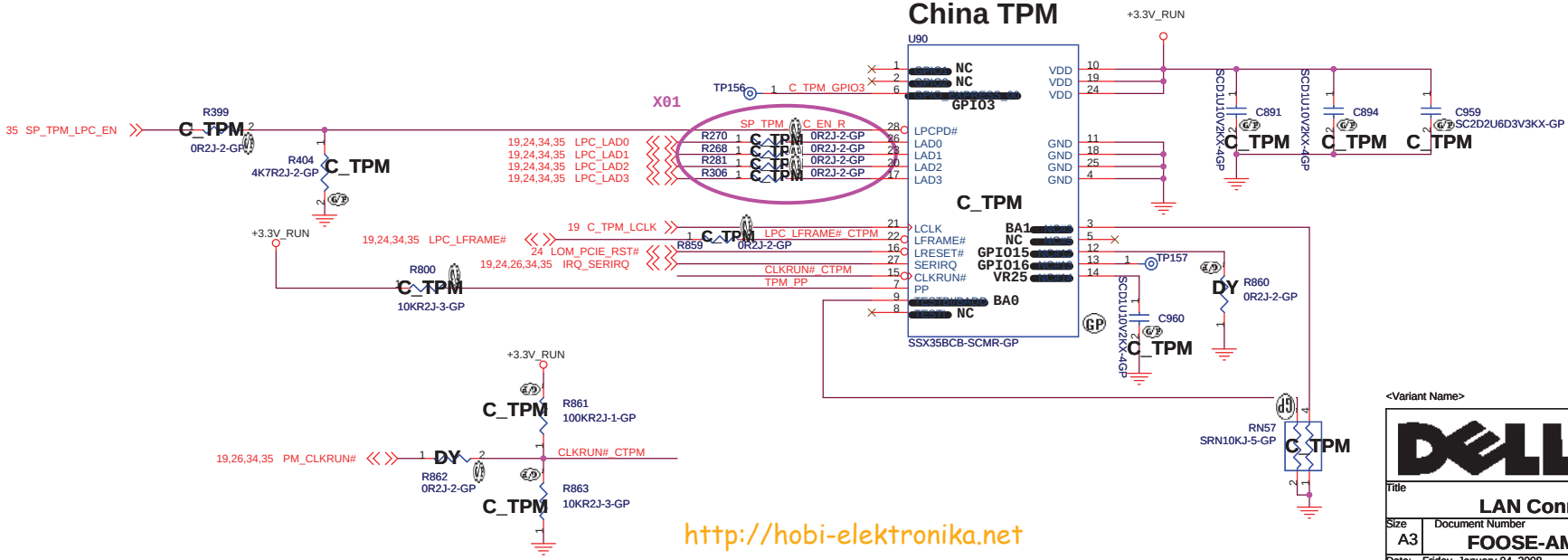
Hipot layout guide line update space > 50mil

Rj11 layout guide line update > 100mil

Yellow LED:TX/RX
Amber LED:Speed 100
Green LED:Speed 10

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

China TPM



<Variant Name>

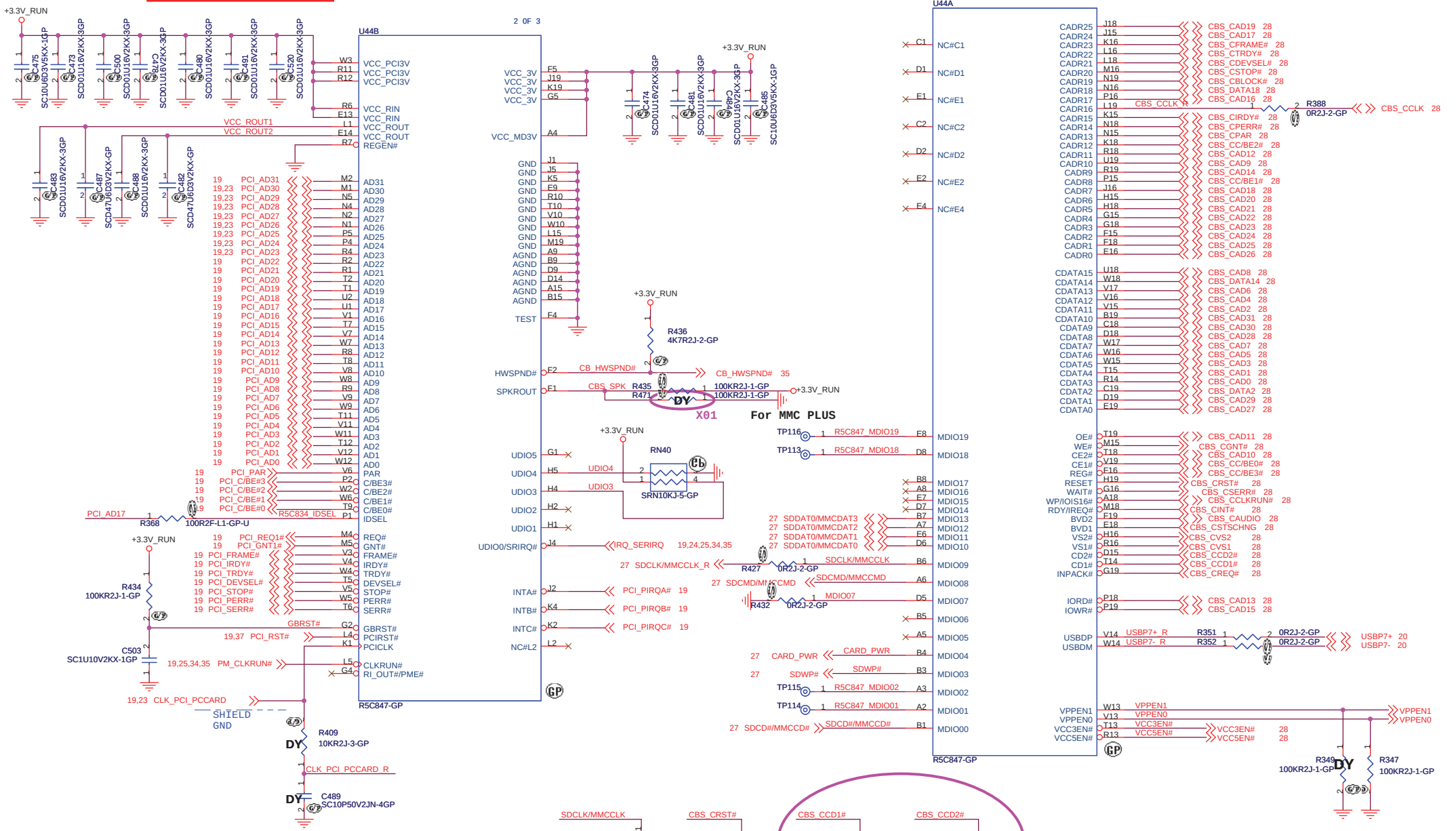
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector&TPM

Size	Document Number	Rev
A3	FOOSE-AMD 15.4"	SB

Date: Friday, January 04, 2008 Sheet 25 of 53

SSID = 1394



<Variant Name>

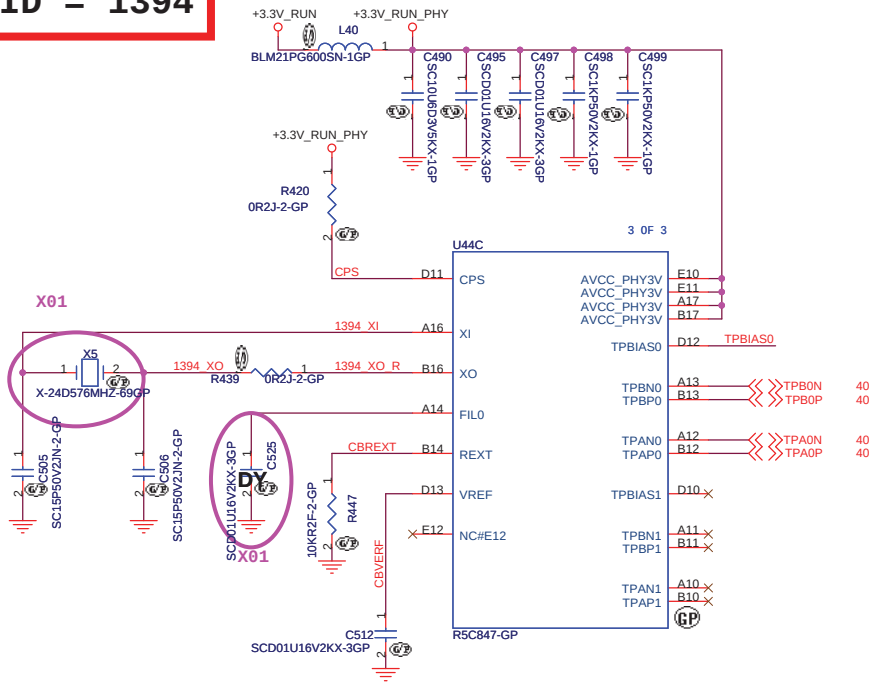
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

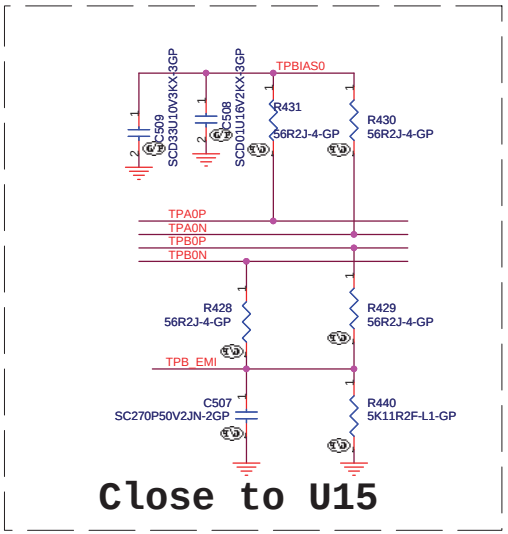
Title: **R5C833/PCI**

Size	Document Number	Rev
A3	FOOSE-AMD 15.4"	SB

Date: Friday, January 04, 2008 Sheet 26 of 53

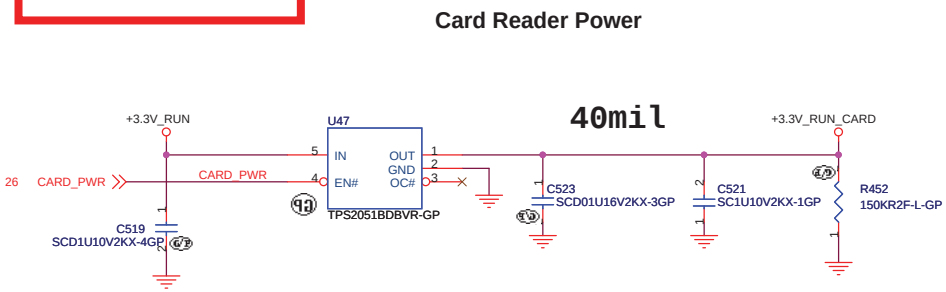
SSID = 1394

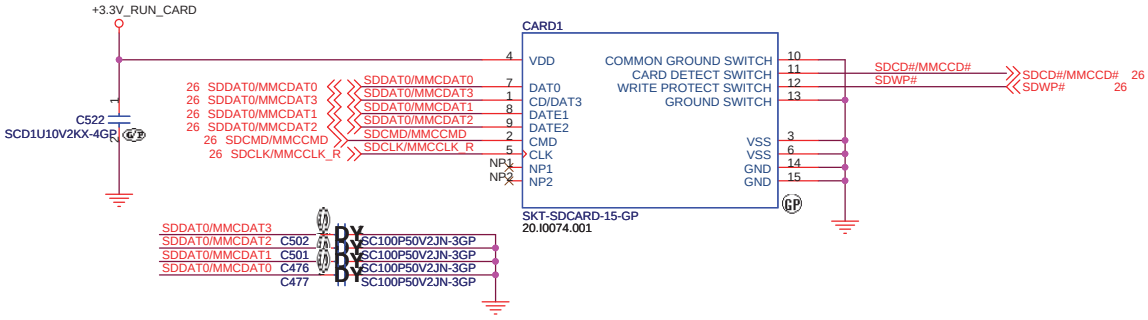




SSID = SDIO

Card Reader Power





<Variant Name>

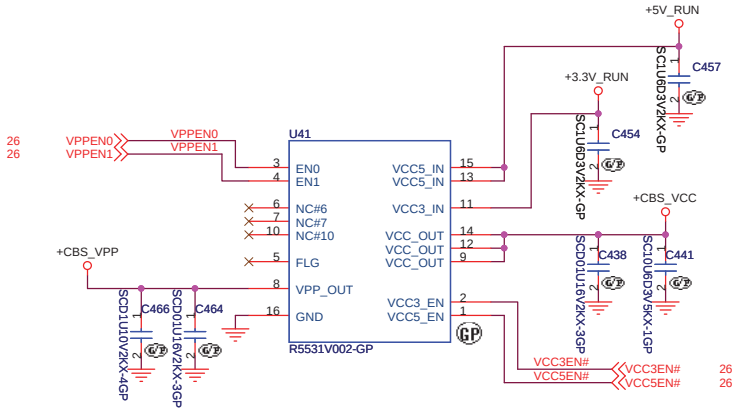
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

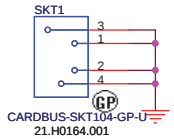
Title: FLASH CARD CONN .

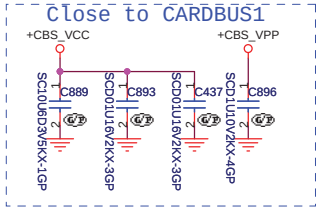
Size	Document Number	Rev
A3	FOOSE-AMD 15.4"	SB

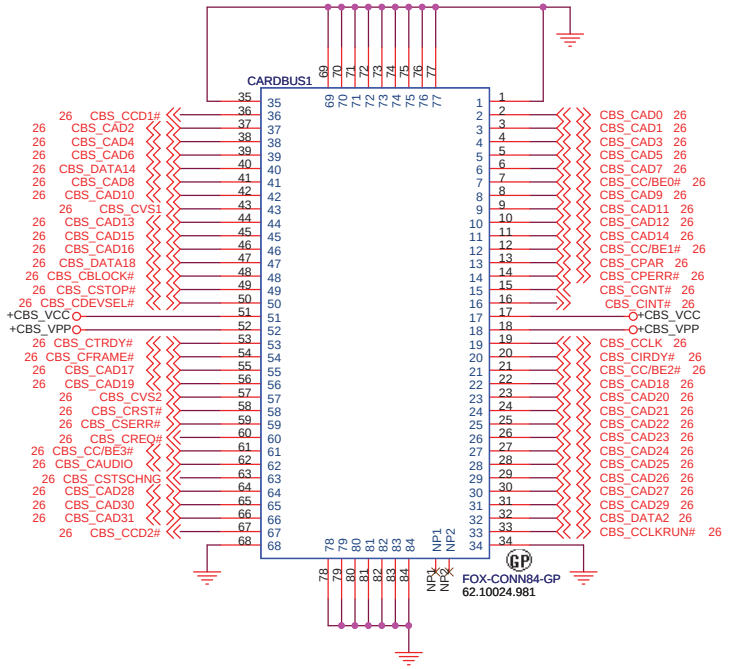
Date: Friday, January 04, 2008 Sheet 27 of 53

SSID = CARDBUS









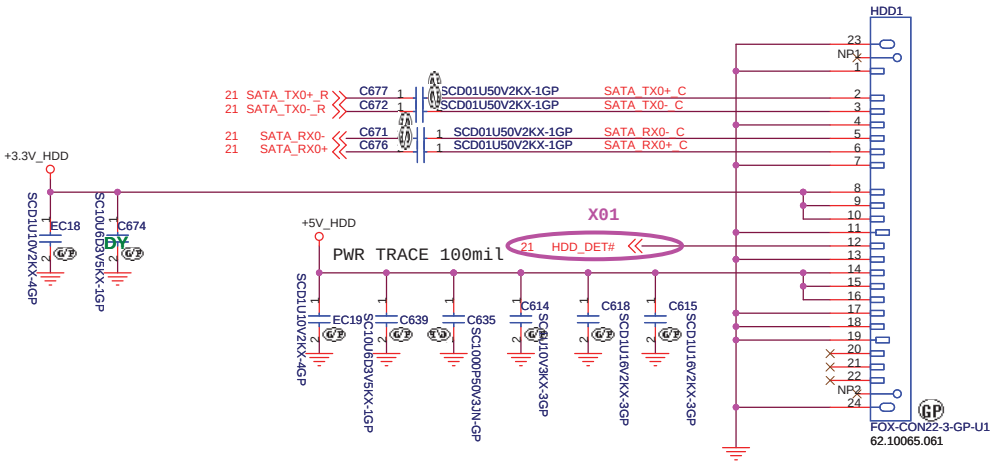
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	R5C847 PCI_CARD	
Size: A3	Document Number: FOOSE-AMD 15.4"	Rev: SB
Date: Friday, January 04, 2008	Sheet 28 of 53	

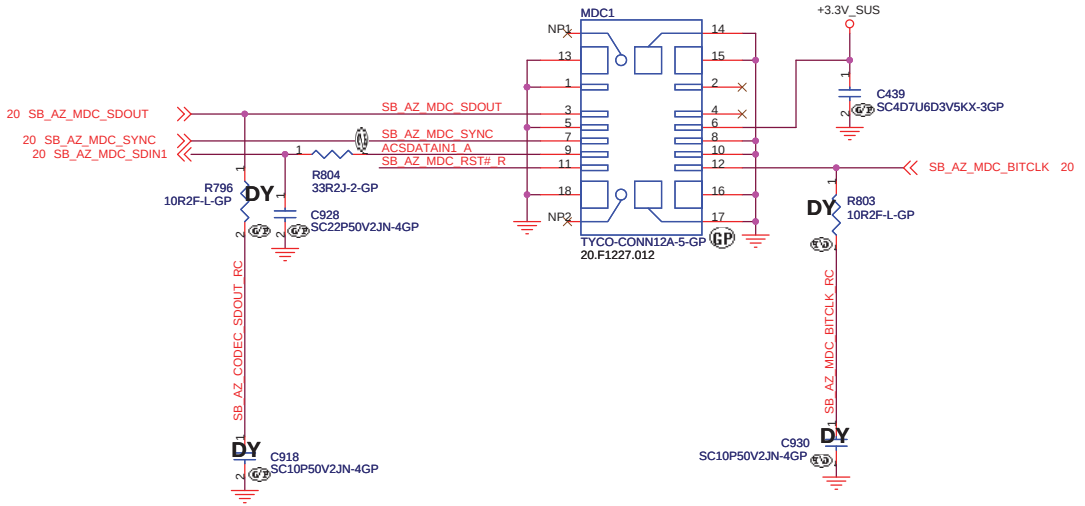
SSID = SATA

SATA HDD Connector



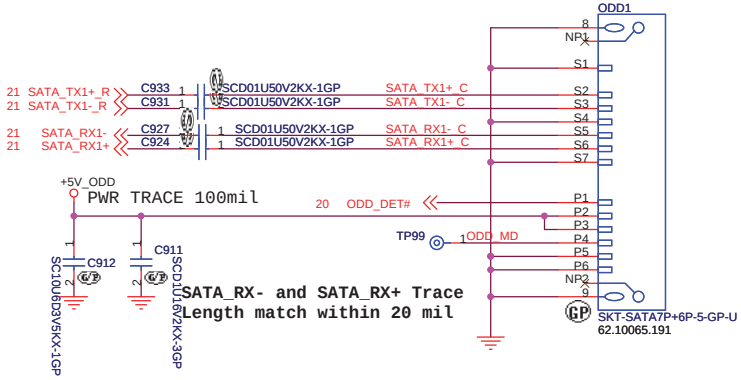
SSID = MDC

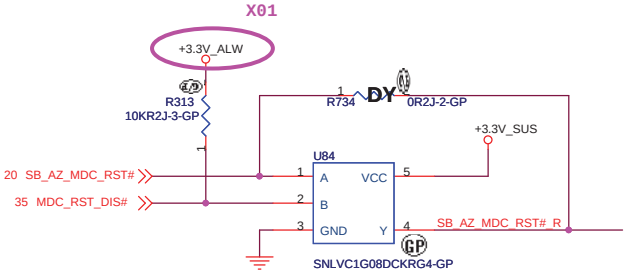
15"MDC Board Connector



SSID = SATA

SATA ODD Connector





AND Gate

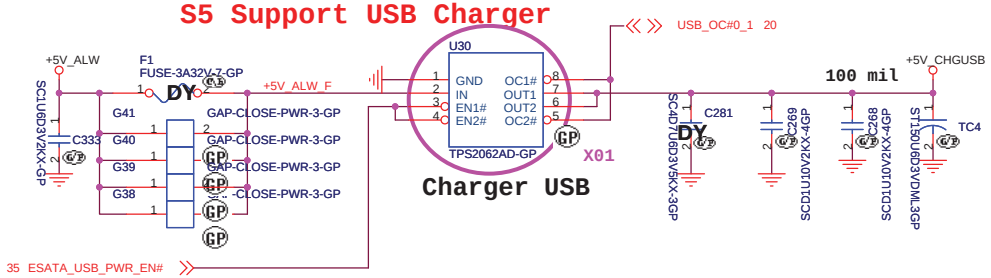
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

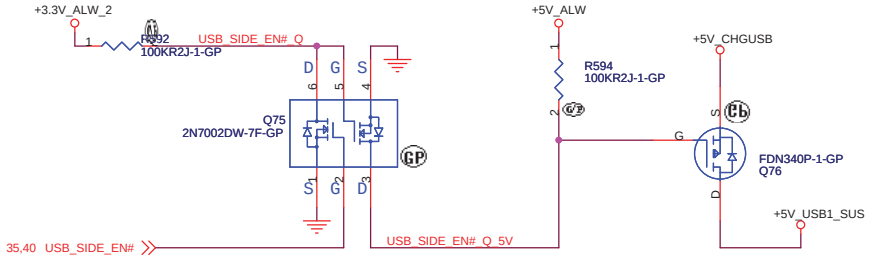
Title	HD/CDROM/MDC	
Size: A3	Document Number: FOOSE-AMD 15.4"	Rev: SB
Date: Friday, January 04, 2008	Sheet 29 of 53	

SSID = USB

S5 Support USB Charger

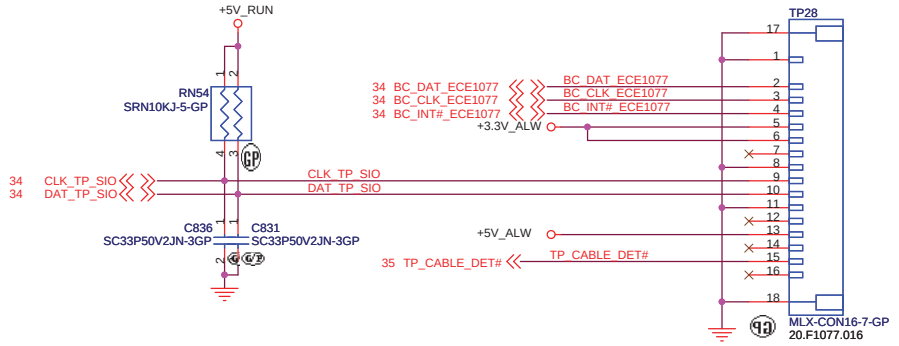


Charger USB



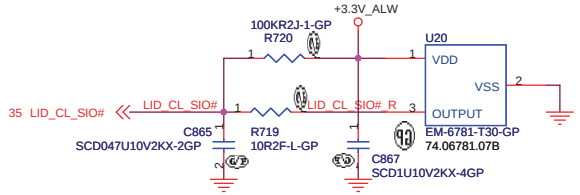
SSID = TOUCH.PAD

TouchPad Connector

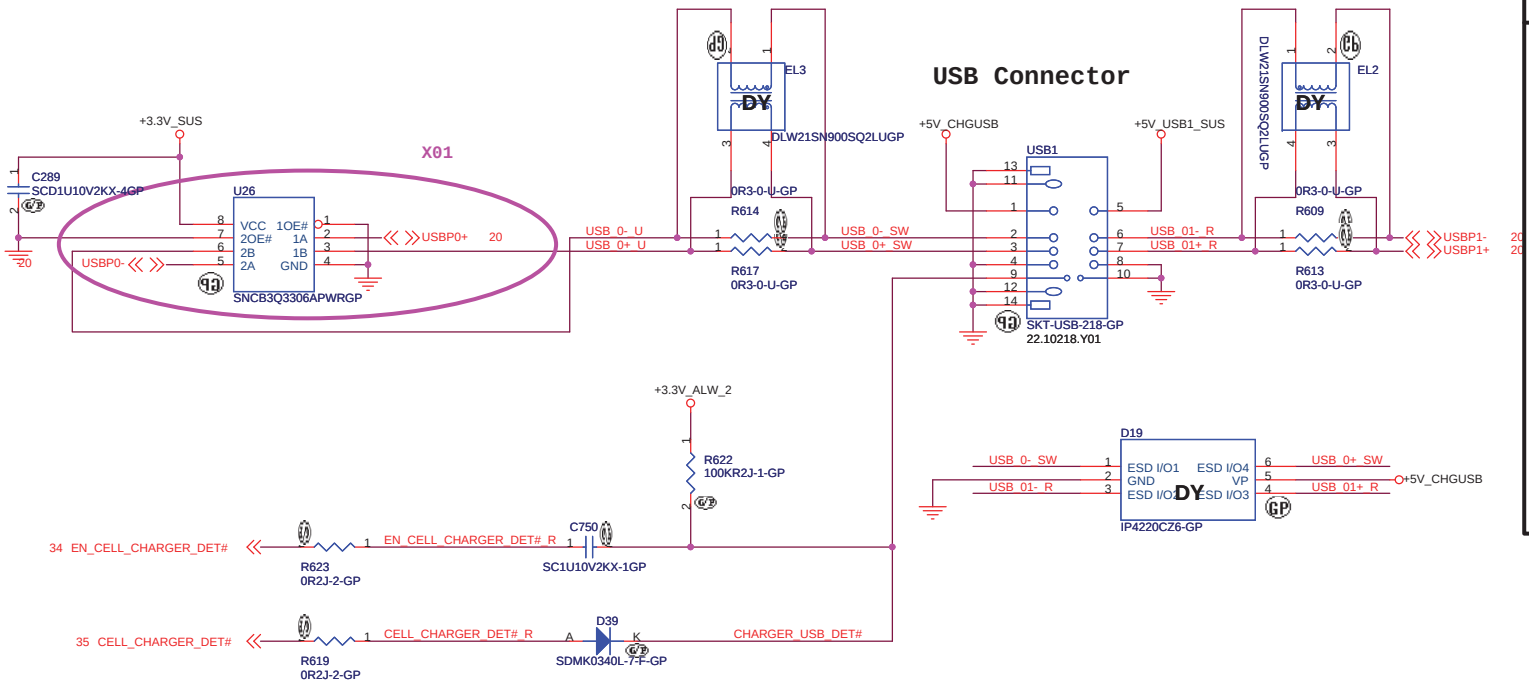


SSID = User.Interface

Hall Switch

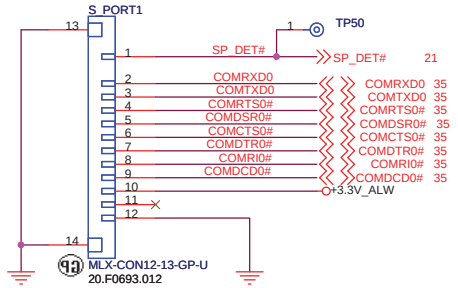


USB Connector



SSID = Legacy

15"Serial port connector



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB charger PORT

Size	Document Number	Rev
A3	FOOSE-AMD 15.4"	SB

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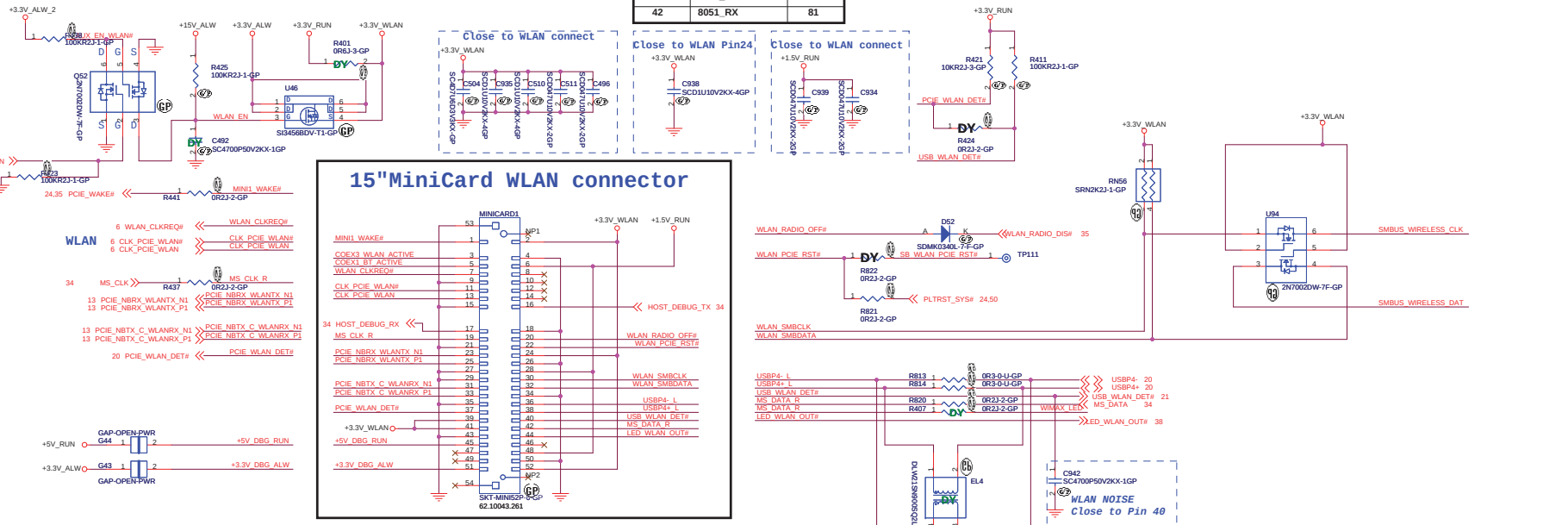
SSID = Wireless

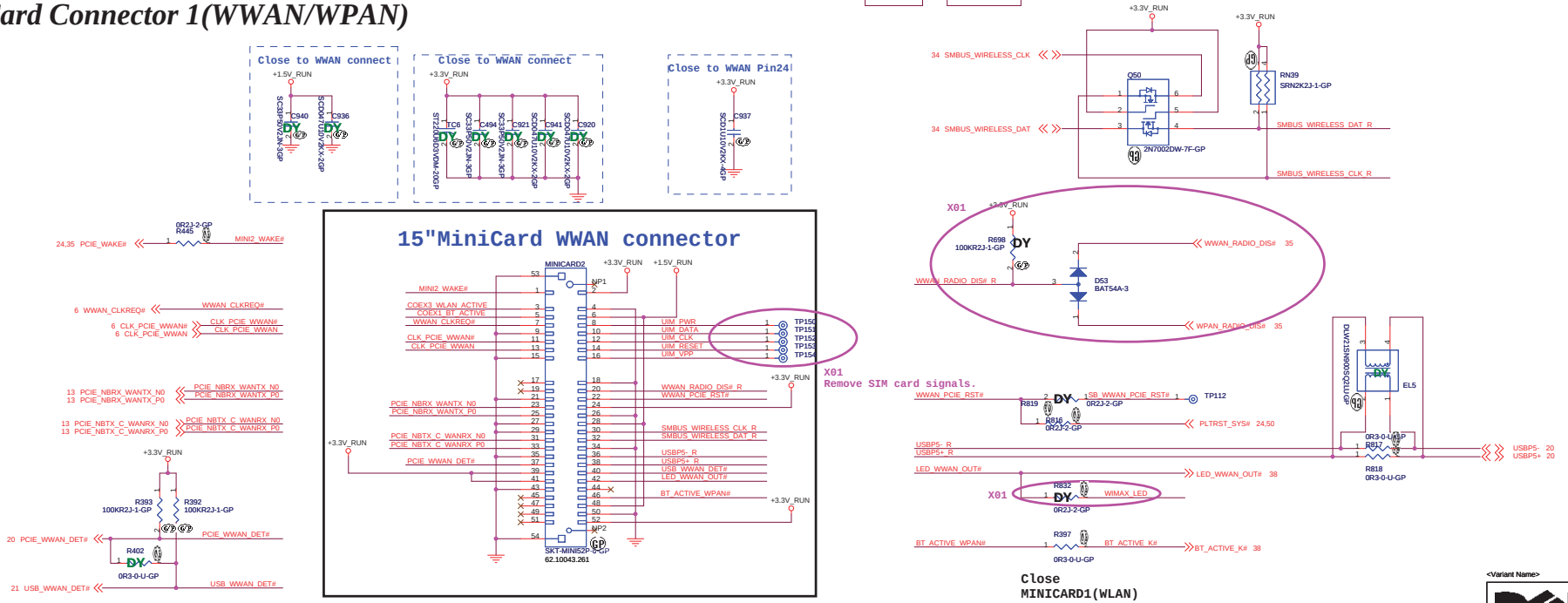
Mini Card Connector 2(WLAN/UWB)

DEBUG_PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



Mini Card Connector 1(WWAN/WPAN)



Layout Note:
Place resistors close to choke as possible to minimize stubs.

<Variant Name>

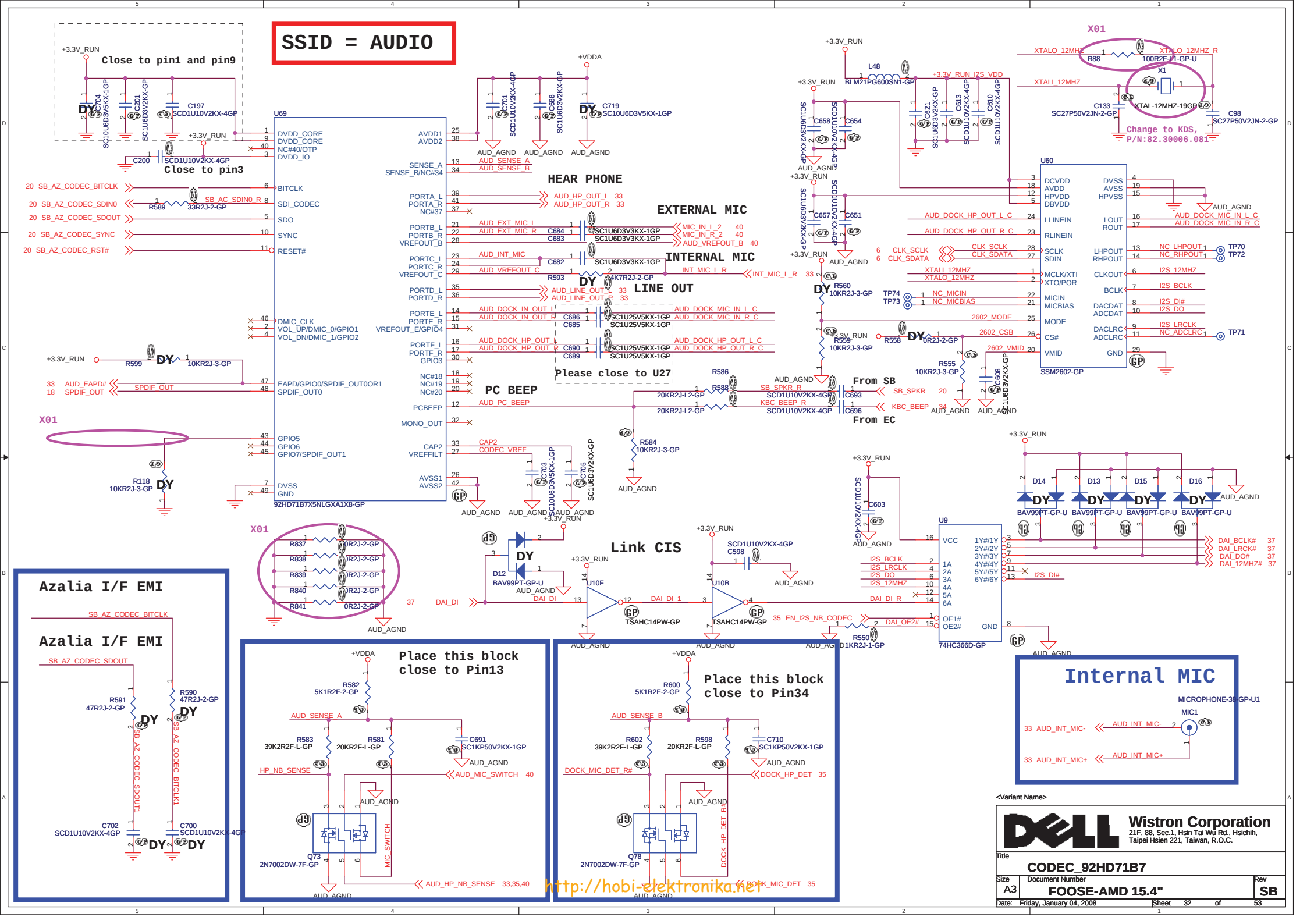
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN .

Size	Document Number	Rev
A2	FOOSE-AMD 15.4"	SB

Date: Friday, January 04, 2008 Sheet 31 of 53

SSID = AUDIO



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CODEC_92HD71B7	
Size: A3	Document Number: FOOSE-AMD 15.4"	Rev: SB
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SSID = AUDIO

60ohm 100MHz
3000mA 0.05ohm DC

Close to Pin8

Close to Pin18

Close to Pin9

X01

1st TPA6040A:74.06040.013
2nd MAX9789A:74.09789.013

NOTE: For MAX9789A
No-stuff R585,C656,C664
stuff R587,R568,R569

Speaker

For EMI

AND Gate for HP Mute Function

GAIN SETTING

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown

From EC

From CODEC

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB

Date: Friday, January 04, 2008 | Sheet 33 of 53

SSID = KBC

X01

+3.3V_ALW
R656 4K3R3-U-GP
RC_ID
C846 SC4700P50V2KX-1GP

For RC_ID and new SUSPWROK

+5V_RUN
RN52 CLK_KBD DAT_KBD SRN4K7J-8-GP
RN50 CLK_DOCK DAT_DOCK SRN4K7J-8-GP
+3.3V_ALW
RN43 PBAT_SMBDAT PBAT_SMBCLK SRN2K2J-1-GP

+RTC_CELL
R635 0R2J-2-GP
+RTC_CELL_R
C776 SCD1U16V2KX-3GP

+3.3V_ALW
C842 C839 C795 C819 C851 C832 C796 C844 C808 SCD1U10V2KX-4GP
SC10U6D3V6MX-2GP

+3.3V_ALW
R359 10KR2J-3-GP
C468 SCD1U10V2KX-4GP
R364 100KR2J-1-GP
R371 10KR2J-3-GP
EC_SPI_CS#
EC_FLASH_SPI_DIN
R342 15R2J-GP
SPI1
SPI_SO0
SPI_WP#0
SPI_HOLD#0
SPI_CLK0
SPI_SI0
W25X16VSSIG-GP
X01

U77

VBAT
VTR[1] VTR[2] VTR[3] VTR[4] VTR[5] VTR[6] VTR[7] VTR[8]

PS/2 INTERFACE
GPIO007/I2C1D_DATA/PS2_CLK0B
GPIO010/I2C1D_CLK/PS2_DAT0B
GPIO110/PS2_CLK2/GPTP-IN6
GPIO111/PS2_DAT2/GPTP-OUT6
GPIO112/PS2_CLK1A
GPIO113/PS2_DAT1A
GPIO114/PS2_CLK0A
GPIO115/PS2_DAT0A
GPIO154/I2C1C_DATA/PS2_CLK1B
GPIO155/I2C1C_CLK/PS2_DAT1B

TP36 5035_GPIO007
TP91 5035_GPIO010
CLK_TP_SIO
DAT_TP_SIO
CLK_KBD
DAT_KBD
CLK_DOCK
DAT_DOCK
PBAT_SMBDAT
PBAT_SMBCLK

JTAG INTERFACE
GPIO145/I2C1K_DATA/JTAG_TDI
GPIO146/I2C1K_CLK/JTAG_TDO
GPIO147/I2C1J_DATA/I2C2C_DATA/JTAG_CLK
GPIO150/I2C1J_CLK/I2C2C_CLK/JTAG_TMS
JTAG_RST#

JTAG1 MLX-CON6-9-GP 20.D0198.106
JTAG_PWR
JTAG_TDI
JTAG_TMS
JTAG_CLK
JTAG_TDO
R649 49D9R2F-GP
RN42 SRN10KJ-6-GP
R639 10KR2J-3-GP
R642 10KR2J-3-GP
C781 SCD1U10V2KX-4GP
0 = Reset JTAG I/F
1 = Disable

FAN PWM & TACH
GPIO050/FAN_TACH1
GPIO051/FAN_TACH2
GPIO052/FAN_TACH3
GPIO053/PWM0
GPIO054/PWM1
GPIO055/PWM2
GPIO056/PWM3

DOCK_POR_RST#
BREATH_LED#
SB_ALW_ON
5035_GPIO054
EC_SPI_CS#
TP94

BC-LINK
GPIO022/BCM_B_CLK/V_CLK
GPIO023/BCM_B_DAT/V_DATA
GPIO024/BCM_B_INT#/V_FRAME
GPIO042/BCM_C_INT#
GPIO043/BCM_C_DAT
GPIO044/BCM_C_CLK
GPIO045/LSBCM_D_INT#
GPIO046/LSBCM_D_DAT
GPIO047/LSBCM_D_CLK
GPIO121/BCM_A_INT#
GPIO122/BCM_A_DAT
GPIO123/BCM_A_CLK

BC_CLK_EMC4002
BC_DAT_EMC4002
BC_INT#_EMC4002
BC_INT#_ECE1099
BC_DAT_ECE1099
BC_DAT_ECE1077
BC_DAT_ECE5028
LPC_LDRQ#
IRQ_SERIRQ
R701 R702 R703 R666 R712 R715 100KR2J-1-GP

HOST INTERFACE
GPIO011/nSMI
GPIO061/LPCPD#
LDRQ#
SER_IRQ
LRESET#
PCI_CLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
CLKRUN#
GPIO100/nEC_SCI

SIO_EXT_SMI#
SIO_RCIN#
LPC_LDRQ#
IRQ_SERIRQ
PLTRST#
CLK_PCI_5035
LPC_LFRAME#
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
PM_CLKRUN#
SIO_EXT_SCI#

JDBG1 MLX-CON5-10-GP 20.D0198.105
HOST_DEBUG
MS_DATA
MS_CLK
HOST_DEBUG_RX
R789 0R2J-2-GP

MASTER CLOCK
XTAL1
XTAL2
GPIO160/32KHZ_OUT

MEC5035_XTAL1
MEC5035_XTAL2_R
EC_32KHZ_OUT
R644 0R2J-2-GP
X6 X-32D768KHZ-40GPU
C791 C802 SC33P50V2JN-3GP
CLK_PCI_5035_R
R695 10R2F-L-GP
C841 SC4D7P50V2CN-1GP
Place close to Pin58

+RTC_CELL
+3.3V_ALW
R633 100KR2J-1-GP
R634 100KR2J-1-GP
C770 SCD1U10V2KX-4GP

AGND VSS[1] VSS[2] VSS[3] VSS[4] VSS[5] VSS[7] VSS[8] VSS VR_CAP[1] VSS_RO
MEC5035-NZW-REV-B-GP
MEC_AGND
5035_VR_CAP1
5035_VSS_RO
L63 BLM18AG121SN-1GP
L62 BLM18AG121SN-1GP
C837 SC4D7U6D3V3KX-GP
C827 SC1U6D3V2KX-GP
C823 SC1U6D3V2KX-GP

MISC INTERFACE
GPIO021/RC_ID
GPIO025/UART_CLK
VCC_PRWGD
GPIO060/KBRST
GPIO101/ECGP_SCLK
GPIO102/ECGP_SOUT
GPIO103/ECGP_SIN
GPIO104/UART_TX
GPIO105/UART_RX
GPIO106/nRESET_OUT
GPIO116/MSDATA
GPIO117/MSCLK
GPIO127/A20M
GPIO153/LED3
GPIO156/LED1
GPIO157/LED2
nFWP

RC_ID
1.8V_DDR_ON
RUNPWROK
1.2V_SUS_ON
EC_FLASH_SPI_CLK
EC_FLASH_SPI_DO
EC_FLASH_SPI_DIN
SPI_CLK0
SPI_SI0
R370 R373 15R2J-GP
X01
HOST_DEBUG_TX
HOST_DEBUG_RX
RESET_OUT#
MS_DATA
MS_CLK
SIO_A20GATE
PS_ID
BAT1_LED#
BAT2_LED#
FWP#
TP33

GENERAL PURPOSE I/O
GPIO001
GPIO002
GPIO014/GPTP-IN7
GPIO015/GPTP-OUT7
GPIO016/GPTP-IN8
GPIO017/GPTP-OUT8
GPIO020
GPIO026/GPTP-IN1
GPIO027/GPTP-OUT1
GPIO030/GPTP-IN2
GPIO031/GPTP-OUT2
GPIO032/GPTP-IN3
GPIO040/GPTP-OUT3
GPIO041
GPIO107
GPIO120
GPIO124/GPTP-OUT5
GPIO125/GPTP-IN5
GPIO126
GPIO151/GPTP-IN4
GPIO152/GPTP-OUT4

SB_TO_EC_PWRGD
NB_VCORE_PWRGD
LOM_SMB_ALERT#
1.2V_RUN_ON
ALW_PWRGD_3V_5V
SUSPWROK
SIO_SLP_S5#
KBC_BEEP
AUX_ON
5035_GPIO041
5035_GPIO107
TP93
TP37
AUX_EN_WOW_LAN
1.1V_RUN_ON
1.2V_ALW_SUS_ON
SB_RSMRST#
CLOCK_EN#
SIO_PWRBTN#

SMBUS INTERFACE
GPIO003/I2C1A_DATA
GPIO004/I2C1A_CLK
GPIO005/I2C1B_DATA
GPIO006/I2C1B_CLK
GPIO012/I2C1H_DATA/I2C2D_DATA
GPIO013/I2C1H_CLK/I2C2D_CLK
GPIO130/I2C2A_DATA
GPIO131/I2C2A_CLK
GPIO132/I2C1G_DATA
GPIO140/I2C1G_CLK
GPIO141/I2C1F_DATA/I2C2B_DATA
GPIO142/I2C1F_CLK/I2C2B_CLK
GPIO143/I2C1E_DATA
GPIO144/I2C1E_CLK

DOCK_SMB_DAT
DOCK_SMB_CLK
LCD_SMBDAT
LCD_SMBCLK
CKG_SMBDAT
CKG_SMBCLK
LOM_WLAN_SMBDAT
LOM_WLAN_SMBCLK
R239 R222 0R2J-2-GP
ACAV_IN_NB
SB_SMBDATA_LAN
SB_SMBCLK_LAN
5035_GPIO140
TP35
SMBUS_WIRELESS_DAT
SMBUS_WIRELESS_CLK
CPU_THRM_SMBDATA
CPU_THRM_SMBCLK

DELL PWR SW INF
BGPO0
VCI_IN2#
VCI_OUT
VCI_IN1#
VCI_IN0#
VCI_OVRD_IN
VCI_IN3#

RSVD_RTC
TP34
5035_VCI_IN2#
ALW_ON
EN_CELL_CHARGER_DET#
MAIN_PWR_SW#
ACAV_IN
DOCK_PWR_SW#

+RTC_CELL
R686 R669 100KR2J-1-GP
R676 1KR2J-1-GP
R678 1KR2J-1-GP
MAIN_PWR_SW#
DOCK_PWR_SW#
POWER_SW#_MB
DOCK_PWR_BTN#

+3.3V_ALW
R641 10KR2J-3-GP
FWP#
R638 10KR2J-3-GP
JDEBUG

DOCK_SMB_ALERT# R652
HOST_DEBUG_TX R358
HOST_DEBUG_RX R682
BC_DAT_EMC4002 R683
MS_DATA R664
MS_CLK R657
10KR2J-3-GP
LCD_SMBCLK LCD_SMBDAT RN51 SRN8K2J-3-GP
LOM_WLAN_SMBCLK LOM_WLAN_SMBDAT RN46 SRN2K2J-1-GP
SMBUS_WIRELESS_CLK SMBUS_WIRELESS_DAT RN44 SRN2K2J-1-GP
CPU_THRM_SMBCLK CPU_THRM_SMBDATA RN45 SRN2K2J-1-GP
DOCK_SMB_CLK DOCK_SMB_DAT RN49 SRN8K2J-3-GP

+3.3V_RUN
SB_TO_EC_PWRGD R283 10KR2J-3-GP

1.2V_RUN_ON R677
SUS_ON R343
1.8V_DDR_ON R687
1.1V_RUN_ON R665
1.2V_ALW_SUS_ON R662
100KR2J-1-GP

+RTC_CELL
D41 SDMK0340-7-F-GP
EN_CELL_CHARGER_DET#
5035_VCI_IN2#
R636 R627 200KR2J-1-GP 100KR2J-1-GP

X01
Remove U37 and C904 from DELL command.

<Variant Name>

DELL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_EMC5035
Size: A3
Document Number: FOOSE-AMD 15.4"
Rev: SB
Date: Friday, January 04, 2008
Sheet 34 of 53

SSID = SIO

Wireless Switch

SW1 — SW-SLIDE-GP — 62.40083.001

WIRELESS_ON/OFF# R — R828 33R2J-2-GP — WIRELESS_ON/OFF#

+3.3V_RUN — R350 100KR2J-1-GP — C946 SC1U10V3KX-3GP

+3.3V_ALW

R315	100KR2J-1-GP	PWR_BTN_BD_DET#
R793	100KR2J-1-GP	SLICE_BAT_PRES#
R408	10KR2J-3-GP	PCIE_WAKE#
R794	100KR2J-1-GP	DELL_ESATA_PWR_EN#
R228	100KR2J-1-GP	NB_HP_MUTE#
R842	100KR2J-1-GP	CELL_CHARGER_DET#
R468	10KR2J-3-GP	DOCK_DET#

+3.3V_ALW_2 — X01

R769	100KR2J-1-GP	USB_SIDE_EN#
R808	100KR2J-1-GP	ESATA_USB_PWR_EN#

+RTC_CELL — R356 DY 10KR2J-3-GP — DOCK_DET#

+3.3V_RUN — R372 100KR2J-1-GP — AUD_HP_NB_SENSE

RN38 — HDDC_EN, ODD_EN — SRN100KJ-6-GP

+3.3V_ALW — R317 100KR2J-1-GP — LID_CL_SIO# — C864 SCD047U10V2KX-2GP

+3.3V_ALW — R774 10KR2J-3-GP — HDT_RESET# — R777 100KR2J-1-GP DY — C305 SC1U10V3KX-3GP — C302 SC1U10V3KX-3GP

Board ID

X01

+3.3V_ALW — R418 10KR2J-3-GP — R416 10KR2J-3-GP — R414 10KR2J-3-GP — BID2, BID1, BID0 — R419 10KR2J-3-GP — R417 10KR2J-3-GP — R415 10KR2J-3-GP

+3.3V_ALW — R810 10KR2J-3-GP — R412 10KR2J-3-GP — CHIPSET_ID0, CHIPSET_ID1, VGA_IDENTIFY — R811 100KR2J-1-GP — R812 10KR2J-3-GP — R413 10KR2J-3-GP

+3.3V_ALW — C917, C910, C883, C923 SCD1U10V2KX-4GP — VCC1 (34, 57, 85, 108)

U42 — ECE5028-NU-GP

41	PBAT_PRES#	GPIOA0
38	SCRL_LED#	GPIOA1
38	NUM_LED#	GPIOA2
TP68	5028_GPIOA3	GPIOA3
41	PBATT_OFF	GPIOA4
29	MDC_RST_DIS#	GPIOA5
24,31	PCIE_WAKE#	GPIOA6
30	ESATA_USB_PWR_EN#	GPIOA7
X01	31 WPAN_RADIO_DIS#	GPIOH0
TP98	5028_GPIOH4	GPIOH1
TP59	5028_GPIOH5	GPIOH4
34	BC_INT# ECE5028	GPIOH5
34	BC_DAT ECE5028	BC_INT#
34	BC_CLK ECE5028	BD_DAT
		BC_CLK
30	COMRXD0	GPIOE0/RXD
30	COMTXD0	GPIOE1/TXD
30	COMRTS0#	GPIOE2/RTS#
30	COMDSR0#	GPIOE3/DSR#
30	COMCTS0#	GPIOE4/CTS#
30	COMDTR0#	GPIOE5/DTR#
30	COMRI0#	GPIOE6/RI#
30	COMDCD0#	GPIOE7/DCD#
TP100	30,40 USB_SIDE_EN#	GPIOB0/INIT#
26	CB_HWSPND#	GPIOB1/SLCTIN#
41	EN_DOCK_PWR_BAR	GPIOC2/SLCT
42	ADAPT_OC	GPIOC3/PE
		GPIOC4/BUSY
20	HDT_RESET#	GPIOC5/ACK#
17	LCD_TST	GPIOC6/ERROR#
		GPIOC7/ALF#
40	PS_ID_DISABLE#	GPIOD0/STROBE#
14	PANEL_BKEN	GPIOC1/PD7
24	DOCKED	GPIOC0/PD6
37,41	DOCK_DET#	GPIOB7/PD5
33	NB_HP_MUTE#	GPIOB6/PD4
30	CELL_CHARGER_DET#	GPIOB5/PD3
17	LCD_VCC_TEST_EN	GPIOB4/PD2
TP61	5028_GPIOB4	GPIOB3/PD1
32,33,40	AUD_HP_NB_SENSE	GPIOB2/PD0
TP101	DELL_ESATA_PWR_EN#	
30	LID_CL_SIO#	GPIOD1
		GPIOD2
43,50	1.1V_RUN_PWRGD	GPIOD3
		GPIOD4
34	NB_VCORE_PWRGD	GPIOD5
49	HDDC_EN	GPIOD6
49	ODD_EN	GPIOD7
37	SLICE_BAT_PRES#	GPIOH6
40	PWR_BTN_BD_DET#	GPIOH7
24	LOM_LOW_PWR	GPIOG0
38	CAP_LED#	GPIOG1
TP63	5028_GPIOG2	GPIOG2
43,50	1.1V_RUN_PWRGD	GPIOG3
20	SIO_EXT_WAKE#	GPIOG4
20	SB_PME#	GPIOG5
20	SB_PCIE_WAKE#	GPIOG6
31	WLAN_RADIO_DIS#	GPIOG7
31	WWAN_RADIO_DIS#	SYSOPT1/GPIOH2
24	LOM_CABLE_DETECT	SYSOPT0/GPIOH3
24	LOM_TPM_EN#	GPIOF7
24	LOM_SUPER_IDDQ	GPIOF6
		GPIOF5
		GPIOF4
TP110	5028_IRTX	IRTX
	IRRX	IRRX
		GPIOF3/IRMODE/IRRX3B
	BID2	GPIOF2/IRTX2
	BID1	GPIOF1/IRRX2
	BID0	GPIOF0/IRMODE/IRRX3A
		VCC1
	DOCK_MIC_DET# 32	GPIOJ7
	CPU_THERM_ALERT# 9	GPIOK4
	1.8V_RUN_ON 49	GPIOI1
TP66	5028_GPIOJ2	GPIOJ2
TP65	5028_GPIOJ3	GPIOJ3
	DOCK_HP_DET 32	GPIOJ6
	CRT_MUX_SWITCH 18	GPIOJ5
TP62	SBAT_DSCHG_EN	GPIOK0
	NB_AC_OFF 40,41,42	GPIOK1
TP60	DP_PRIORITY	GPIOK3
	2.5V_RUN_PWRGD 39,50	GPIOK2
	RUN_ON 17,33,49,50	GPIOK5
	1.5V_RUN_ON 45	GPIOK6
R394 0R2J-2-GP	CPU_VCORE_ENABLE_R	GPIOI6
	CPU_VCORE_PWRGD 48,50	GPIOI5
	0.9V_DDR_VTT_ON 46	GPIOI2
	CAP_LDO	CAP_LDO
	DP_MUX_PD	GPIOJ0
R766 1KR2F-3-GP	TEST_PIN	TEST_PIN
	DOCK_AC_OFF_EC 37	GPIOI7
	SIO_SLP_S3# 20	GPIOI4
	3.3V_RUN_ON 49	GPIOI3
	LPC_LAD0 19,24,25,34	LAD0
	LPC_LAD1 19,24,25,34	LAD1
	LPC_LAD2 19,24,25,34	LAD2
	LPC_LAD3 19,24,25,34	LAD3
	LPC_LFRAME# 19,24,25,34	LFRAME#
	PLTRST# 14,19,34,50	LRESET#
	CLK_PCI_5028 19,23	PCICLK
	PM_CLKRUN# 19,25,26,34	CLKRUN#
	LPC_LDRQ0# 19	LDRQ0#
	LPC_LDRQ1# 19	LDRQ1#
	IRQ_SERIRQ 19,24,25,26,34	SER_IRQ
	CLK_SIO_14M 6	14_318MHZ
		VSS
	D_LAD0 37	DLAD0
	D_LAD1 37	DLAD1
	D_LAD2 37	DLAD2
	D_LAD3 37	DLAD3
	D_LFRAME# 37	DLFRAME#
	D_CLKRUN# 37	DCLKRUN#
	D_DLDRQ1# 37	DLDRQ1#
	D_SERIRQ 37	DSER_IRQ
	RUNPWROK 34,50	PWRGD
TP64	SP_TPM_LPC_EN 25	OUT65
	PSID_SELECT 40	GPIOJ4
	EC_NB_PWRGD 14	VSS
		GPIOK7
		VSS
		VSS
		VSS
		VSS
		VSS
	TP_CABLE_DET# 30	GPIOJ1

+3.3V_ALW — C914 SC4D7U6D3V3KX-GP — C448 SCD1U10V2KX-4GP

+3.3V_RUN — SP_TPM_LPC_EN R403 10KR2J-3-GP — D_CLKRUN# R33 100KR2J-1-GP — D_SERIRQ R19 100KR2J-1-GP — D_DLDRQ1# R25 100KR2J-1-GP

+3.3V_ALW — CPU_THERM_ALERT# R360 4K7R2J-2-GP — CRT_MUX_SWITCH R797 10KR2J-3-GP — TP_CABLE_DET# R386 100KR2J-1-GP

+3.3V_SUS — X01 — 2.5V_RUN_PWRGD R178 10KR2J-3-GP

LOM solution selection

+3.3V_ALW — R395 5761 10KR2J-3-GP — DP_MUX_PD — R396 5756 10KR2J-3-GP

EC_NB_PWRGD — R792 DY 100KR2J-1-GP

0.9V_DDR_VTT_ON — R406 100KR2J-1-GP

DP_PRIORITY — R366 DY 100KR2J-1-GP

RN55 — RUN_ON, 1.5V_RUN_ON, 3.3V_RUN_ON, 1.8V_RUN_ON — SRN100KJ-6-GP

Place closely pin 64

CLK_SIO_14M — R763 10R2F-L-GP DY — 1CLK_SIO_14M_R_2 — C890 SC10P50V2JN-4GP DY

Place closely pin 56

CLK_PCI_5028 — R762 6D8R2F-GP — 1CLK_PCI_5028_R_2 — EC15 SC4D7P50V2CN-1GP

MB VERSION ID

BID2	BID1	BID0	REV
0	0	0	X00
0	0	1	X01
0	1	0	X02
0	1	1	A00

CHIPSET_ID1	CHIPSET_ID0	NOTE
0	0	Intel CPU and Intel chipset
0	1	AMD CPU and AMD chipset

<Variant Name>

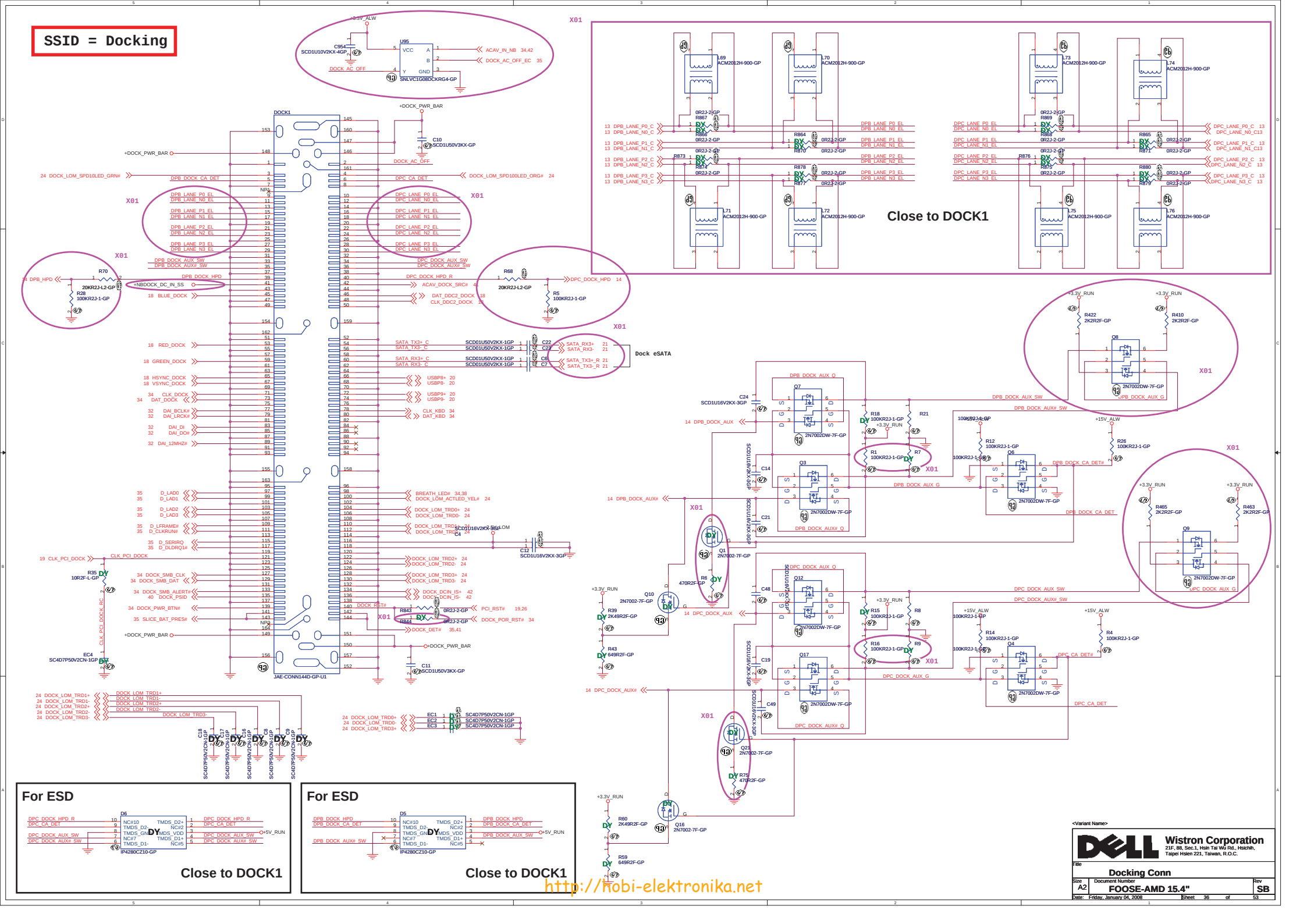
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMC-5028

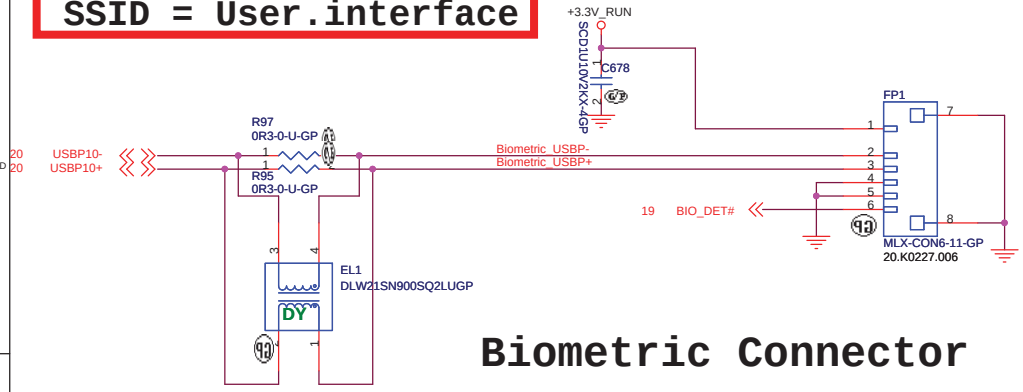
Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB

Date: Friday, January 04, 2008 | Sheet 35 of 53

SSID = Docking



SSID = User.interface

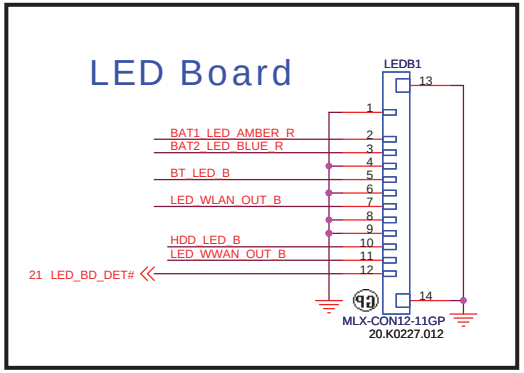


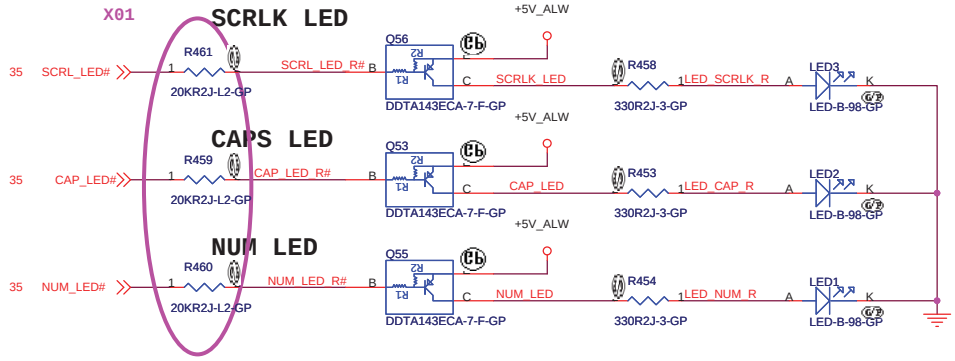
Biometric Connector

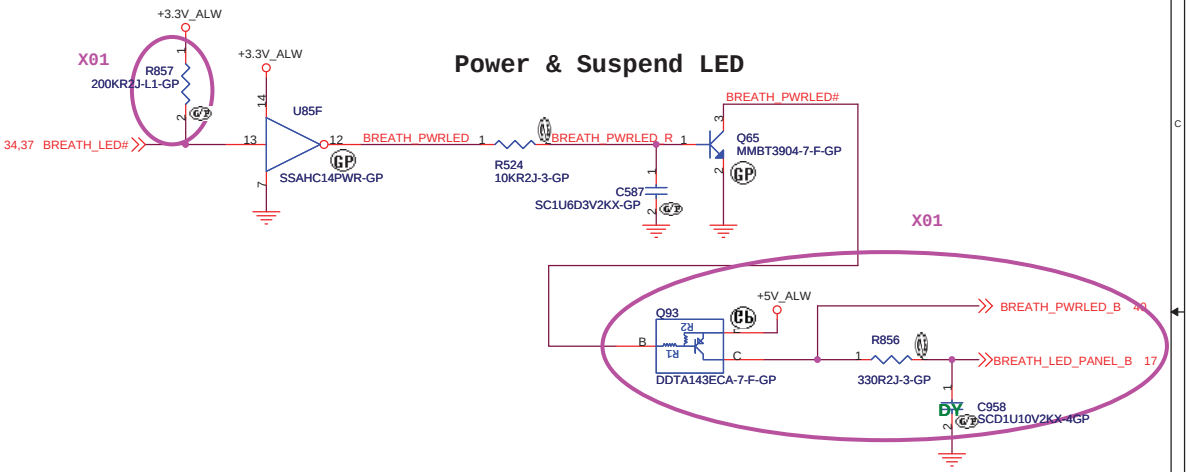
LED BD Connetor

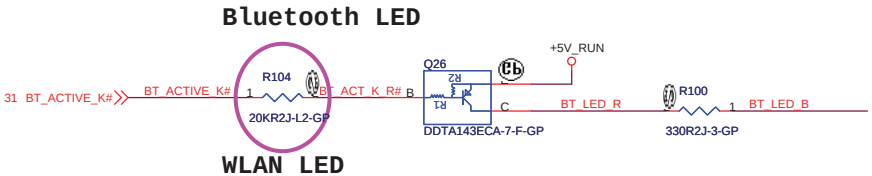
LED Location from left to right

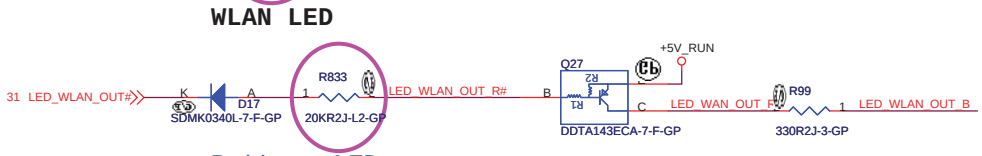
HDD	BATTERY	WLAN	BLUE TOOTH	WWAN

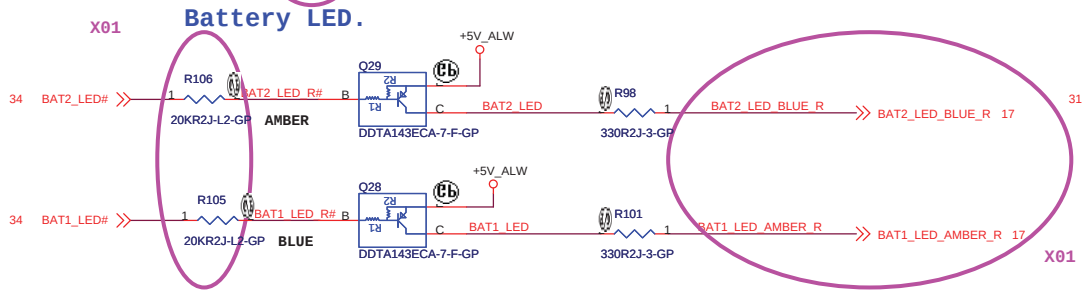


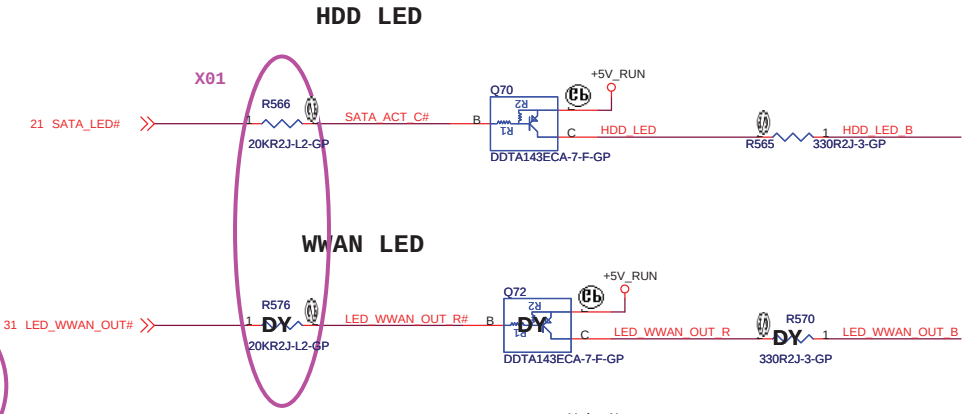












<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BOARD to BOARD		
Size: A3	Document Number: FOOSE-AMD 15.4"	Rev: SB
Date: Friday, January 04, 2008	Sheet 37 of 53	

SSID = THERMAL

REM_DIODE3_N, REM_DIODE3_P routing together.
Trace width / Spacing = 10 / 10 mil
Place near the bottom SODIMM

Place close to the Guardian pins as possible

Diode circuit at DP4/DN4 is used for skin temp sensor (placed optimally between CPU, MCH and GPU).

CAP close to diode

Place close to the Guardian pins as possible

Place close to the Guardian pins as possible

1.Place under CPU
2.Place CAP close to Q24

Close to the Guardian pins

Q74 place near DIMM

U31

EMC4002-HZH-REV-C-GP

Pull-up Resistor on ADDR_MODE/XEN	Remote mode	SMBUS Address
<= 4.7K	DIODE	5F(r/w)
10K	DIODE	5E(r/w)
18K	Thermistor	5F(r/w)
>= 33K	Thermistor	5E(r/w)

Voltage margining circuit for LDO output.
For Vmargin, stuff Ra=31.6K and Rb=30K.
Rb=1K for production

At maximum load current of 600mA, the voltage drop across the should be keep in the range of 0.5V to 1V

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC4002
Size: A3
Document Number: FOOSE-AMD 15.4"
Rev: SB
Date: Friday, January 04, 2008
Sheet 38 of 53

SSID = PWR.Support

TABLE
MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL	TI
R505	8.45K 1%	DUMMY	DUMMY
C56	0.01uF	0.1uF	0.1uF
C562	0.1uF 10V	DUMMY	200P 10V
C576	1uF 10V	DUMMY	1uF 10V
R525	365K 1%	215K 1%	309K 1%
R490	0 5%	10 5%	0 5%
R510	0 5%	10 5%	0 5%
C549	DUMMY	0.22uF	0.1uF
C564	DUMMY	0.22uF	0.1uF
C579	0.01uF	DUMMY	DUMMY
C567	0.1uF 10V	DUMMY	DUMMY
C548	220pF 50V	DUMMY	DUMMY
D32	RB751V-40	DUMMY	RB751V-40
C30	3.3nF	DUMMY	DUMMY
R500	1 1%	0 5%	0 5%
R17	100 5%	0 5%	0 5%
R71	0 5%	8.45K 1%	8.45K 1%
R527	10K 5%	2.2K 5%	4.7K 5%
C588	0.01uF	0.01uF	DUMMY
C585	0.01uF	0.01uF	DUMMY
R22	1K 5%	DUMMY	DUMMY
Q8	ISS355	DUMMY	DUMMY
C557	1uF 10V	1uF 10V	DUMMY
R507	33 1%	33 1%	DUMMY
R515	DUMMY	DUMMY	0 5%
R523	DUMMY	DUMMY	200K 5%
R530	DUMMY	DUMMY	7.5K 5%
C575	DUMMY	DUMMY	51P 10V
C580	DUMMY	DUMMY	2000P 10V
C586	DUMMY	DUMMY	130P 10V
C568	DUMMY	DUMMY	0.1uF
C540	DUMMY	DUMMY	0.1uF
R508	10K 1%	10K 1%	DUMMY
R475	DUMMY	DUMMY	10k 5%
R503	15.8K 1%	15.8K 1%	DUMMY
R514	DUMMY	10K 5%	DUMMY
R517	0 5%	10 5%	0 5%
C541	DUMMY	DUMMY	DUMMY
C561	DUMMY	DUMMY	DUMMY
R491	0 5%	10 5%	0 5%

PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL	BQ24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	IINP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSON	CSON
18	CSIP	CSOP	CSOP
20	DLO	LGATE	LGATE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGSTE
25	BST	BOOT	BOOT
26	VCC	VCC	ICOUT

"NC" means no-connect

MAX 8731A/ISL88731

Adapter (W)	Trip Current (A)	R67	R485	R484	R489
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

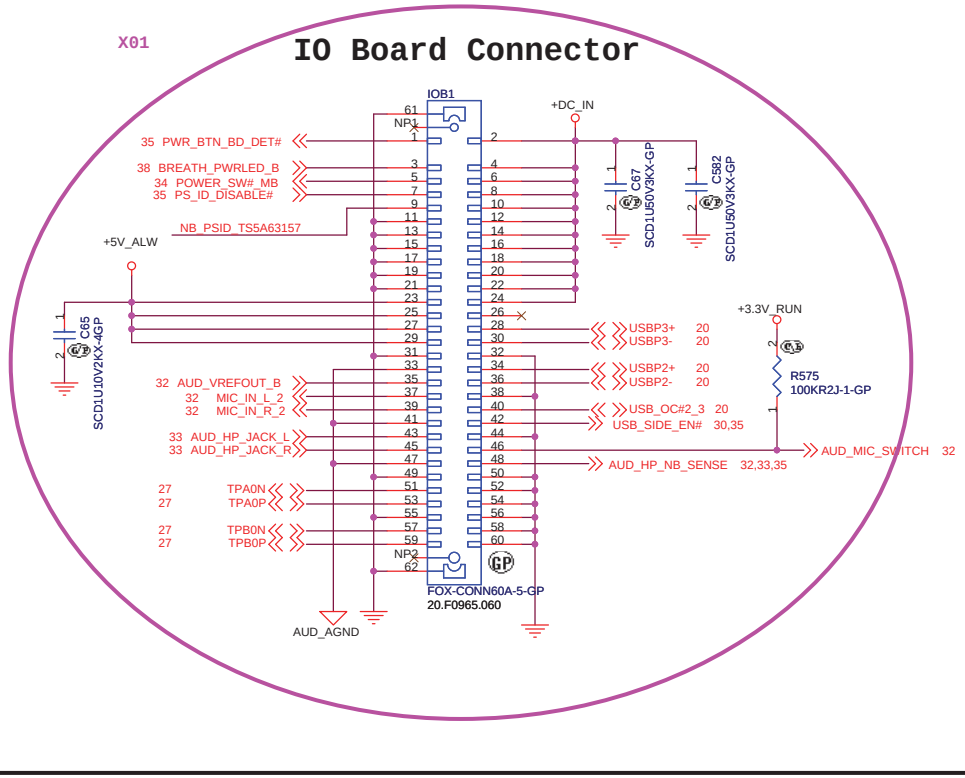
*R489 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

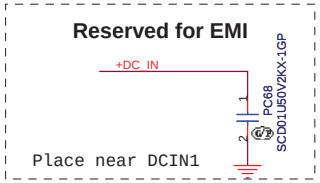
BQ247451

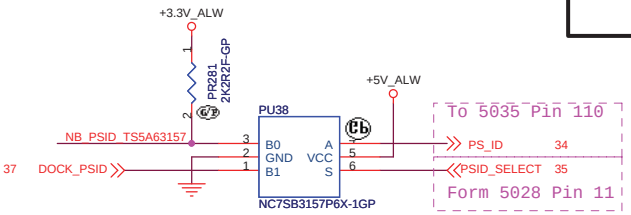
Adapter (W)	Trip Current (A)	R67	R485	R484	R489
65	3.17	57.6K	12.4K	205	24.3K
90	4.43	51.1K	16.9K	499	32.4K

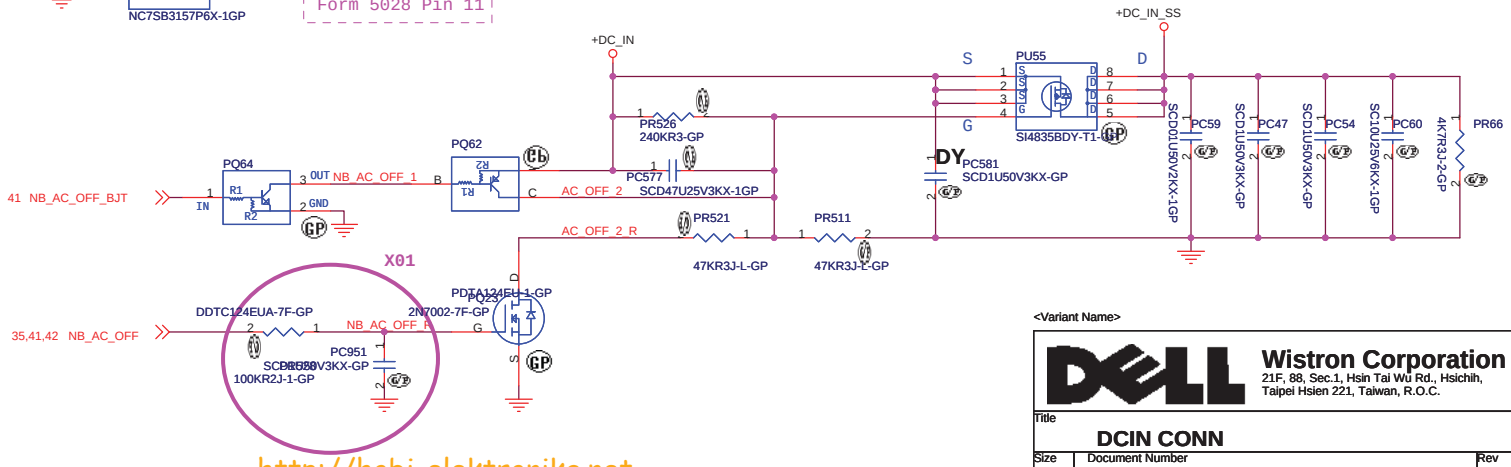
*R489 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

SSID = User.Interface









<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN CONN
Size: A3
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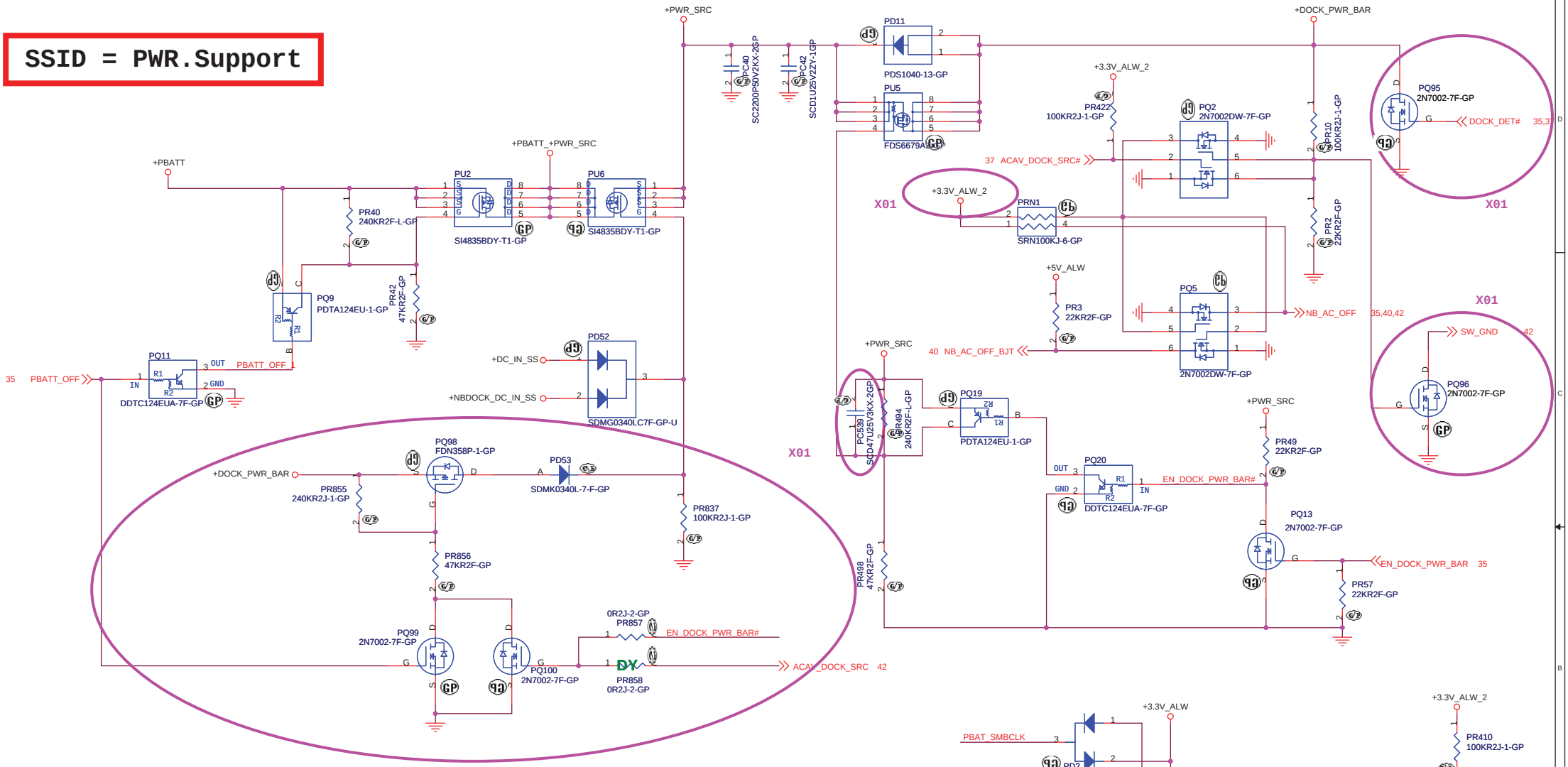
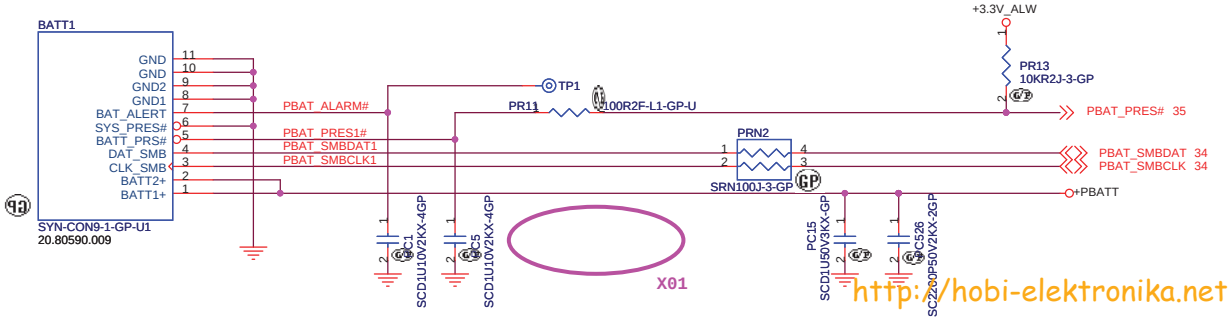
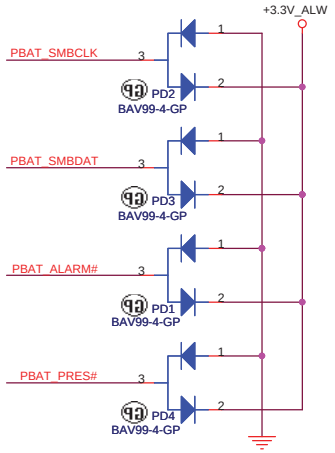
SSID = PWR.Support

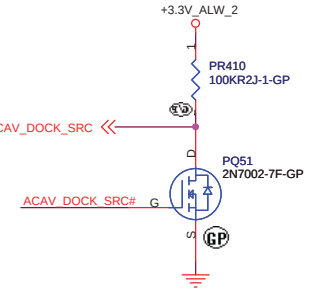


SSID = RBATT

Batt Connecter







<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

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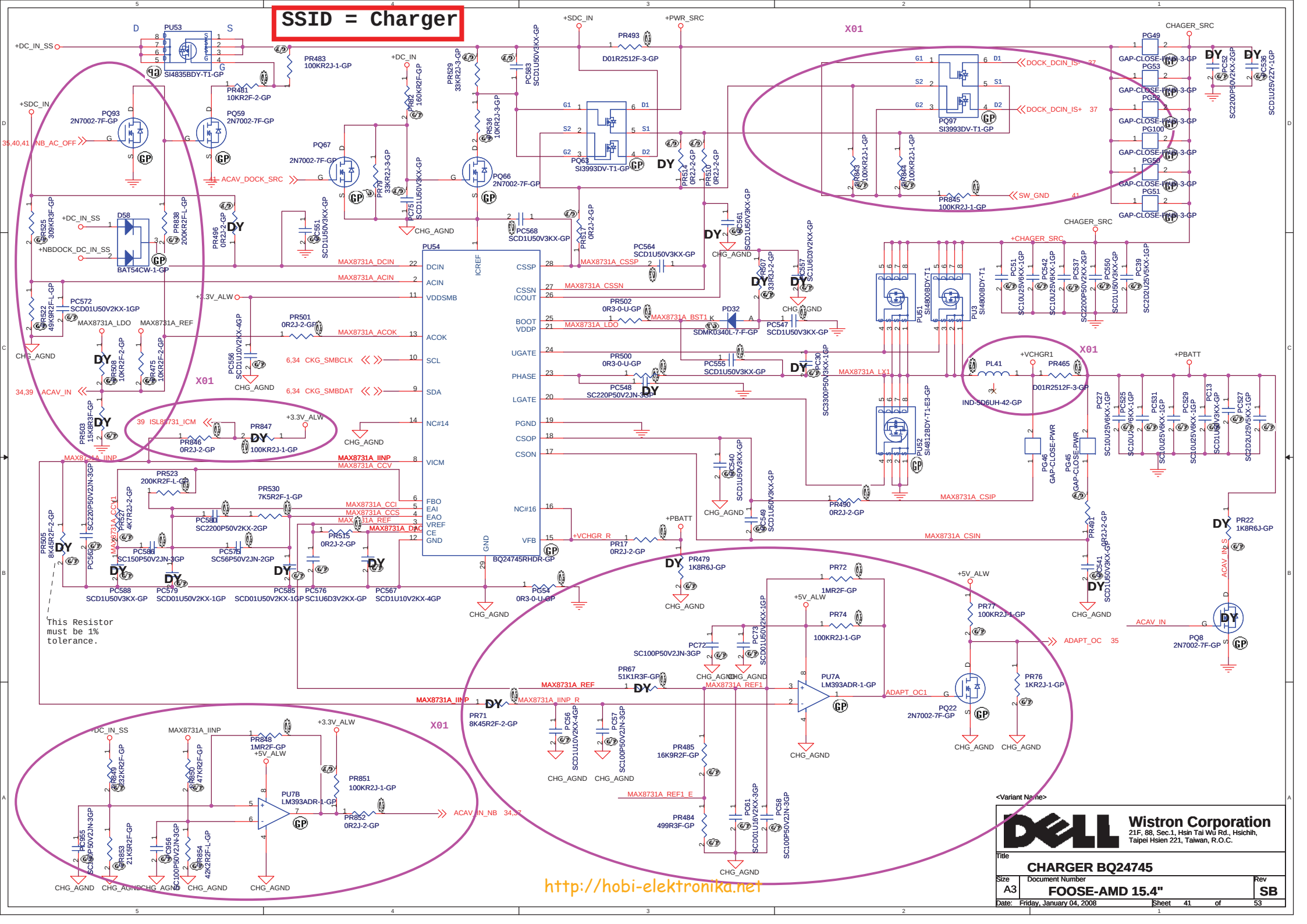
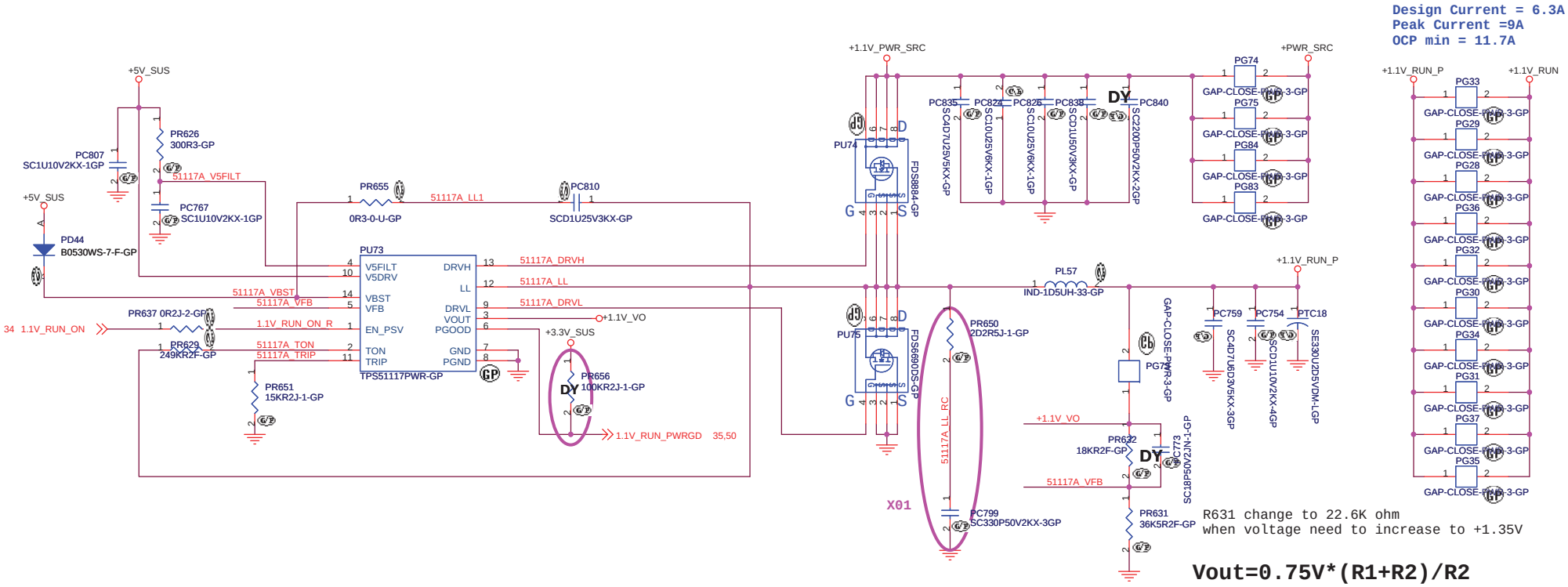
SSID = Charger



SSID = PWR.Plane.Regulator_1p1v



R631 change to 22.6K ohm
when voltage need to increase to +1.35V

Vout=0.75V*(R1+R2)/R2

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH MPLC0730L1R5 NEC_TOKIN 8.8Arms 68.1R510.20C
O/P cap: 330U 2.5V 2R5TPE330MF 15mOhm 3.1Arms Sanyo/ 77.23371.L01
H/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37
Ton = 249KOhm --> 300KHz

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	1D1V(TPS5117)	
Size A3	Document Number FOOSE-AMD 15.4"	Rev SB
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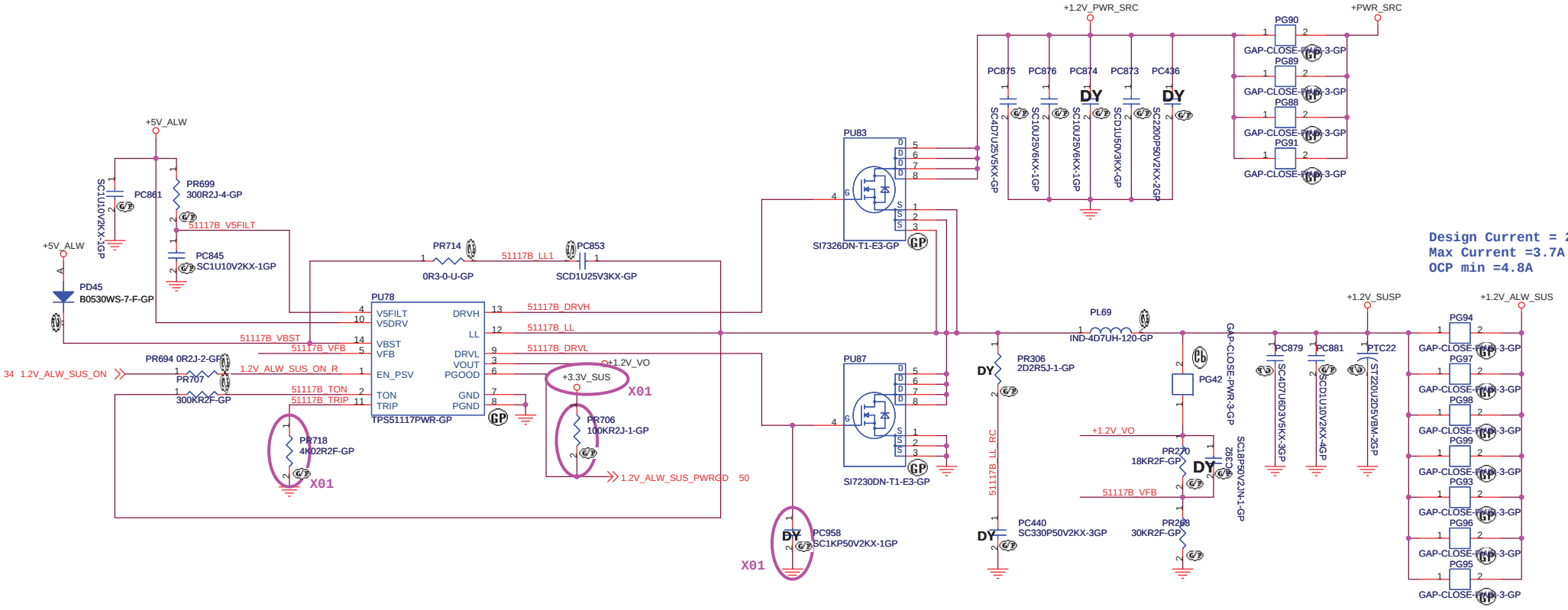
SSID = PWR.Plane.Regulator_1p2v



Design Current = 2.6A
Max Current =3.7A
OCP min =4.8A

Vout=0.75V*(R1+R2)/R2

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 4.7UH MPLC0730L4R7 NEC_TOKIN 5.6Arms 68.4R710.20G
O/P cap: 220U 2.5V 2R5TPE220MAZB 35mOhm 1.4Arms Sanyo/ 77.22271.18L
H/S: SI7326 / 30mOhm/ 4.5Vgs/ 84.07326.037
L/S: Si7326 / 30mOhm/ 4.5Vgs/ 84.07326.037
Ton = 249KOhm --> 250KHz

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 1D2V(TPS5117)
Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB
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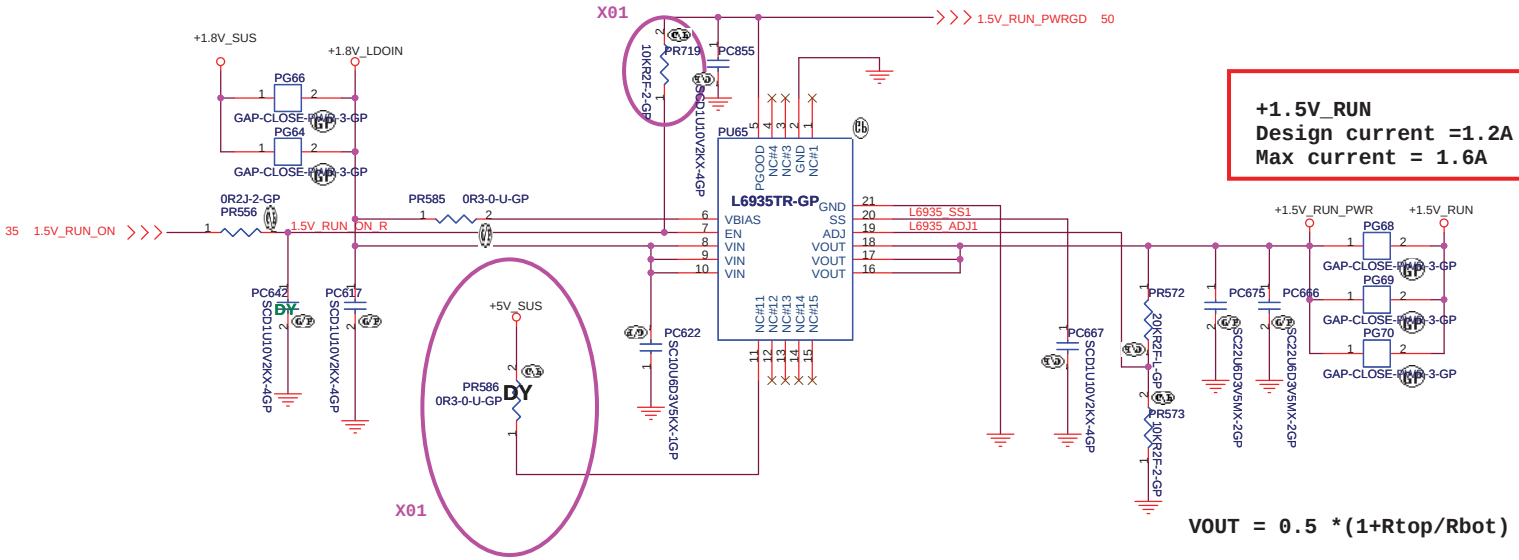
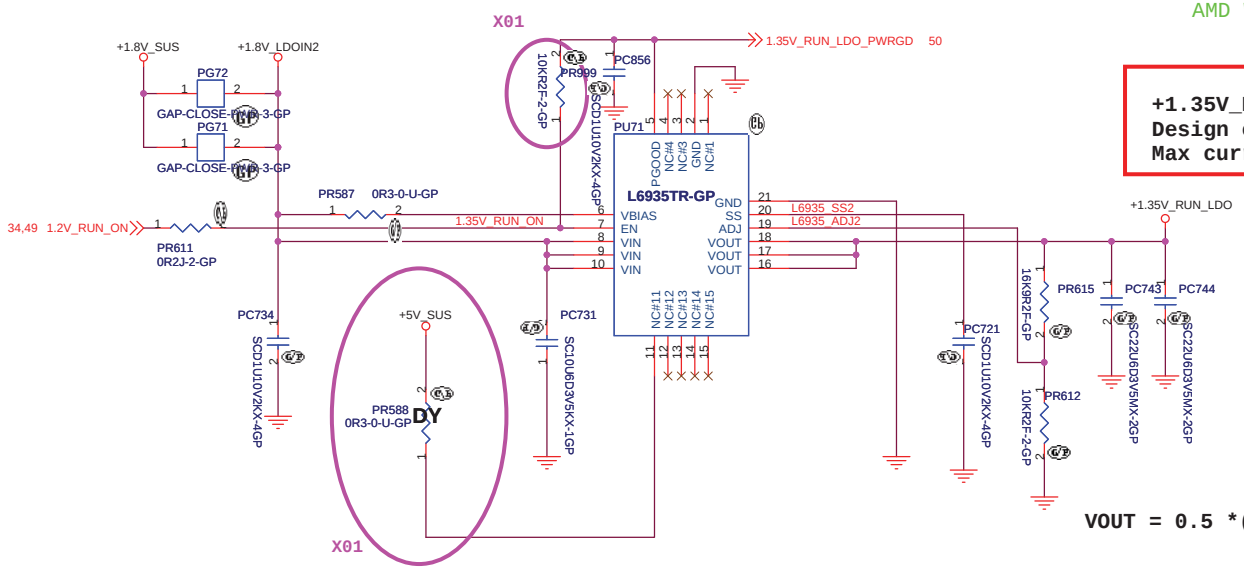
SSID = PWR.Plane.Regulator_1p2v1p5v



+1.5V_RUN
Design current =1.2A
Max current = 1.6A

VOUT = 0.5 *(1+Rtop/Rbot)

AMD WORK AROUNT



+1.35V_RUN_LDO
Design current =1A
Max current = 1A

VOUT = 0.5 *(1+Rtop/Rbot)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1.2/1.5V_LDO (L6935TR)

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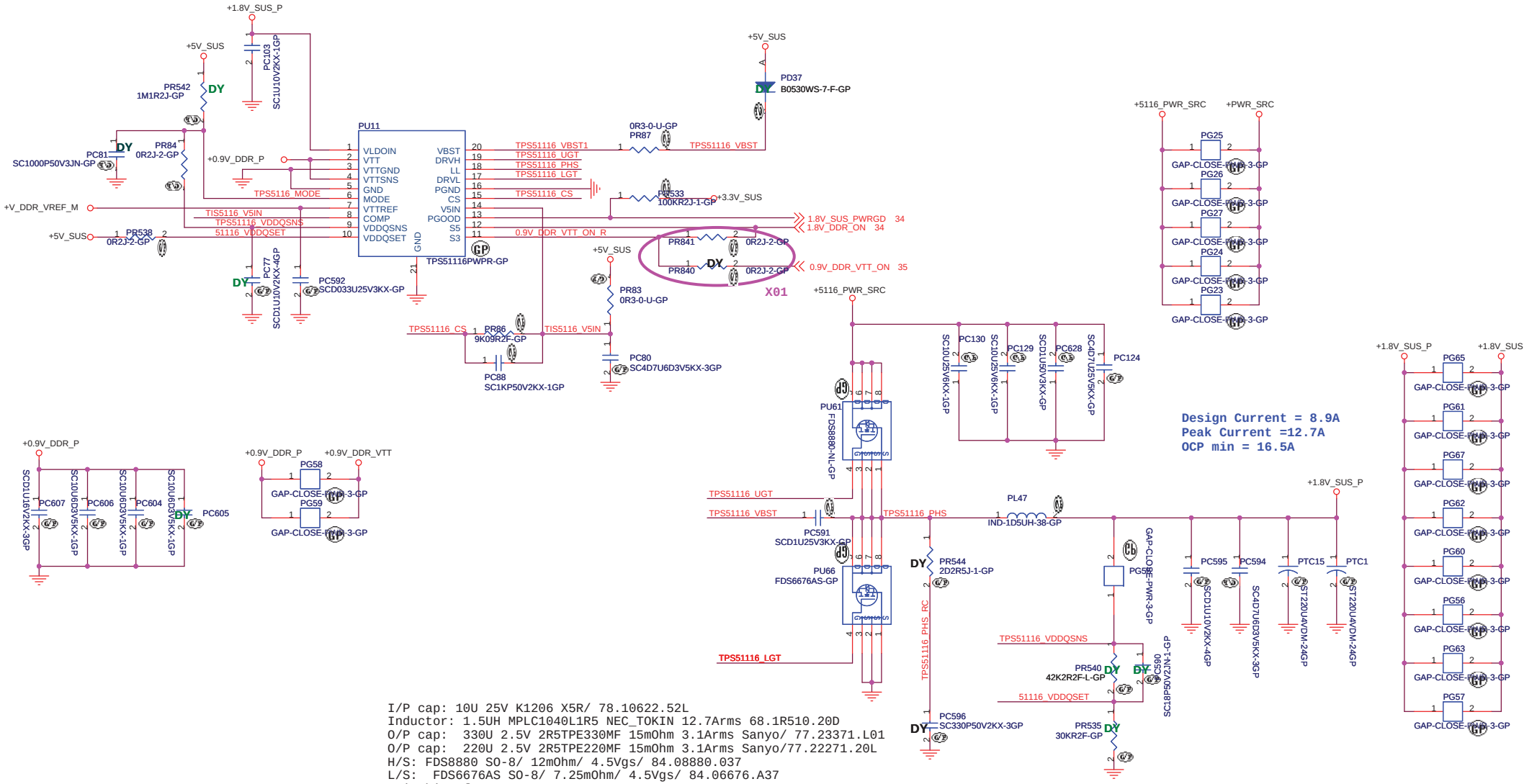
TI TPS51116 for 1.8V and 0.9V

SSID = PWR.Plane.Regulator_1p8v0p9v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH MPLC1040L1R5 NEC_TOKIN 12.7Arms 68.1R510.20D
O/P cap: 330U 2.5V 2R5TPE330MF 15mOhm 3.1Arms Sanyo/ 77.23371.L01
O/P cap: 220U 2.5V 2R5TPE220MF 15mOhm 3.1Arms Sanyo/77.22271.20L
H/S: FDS8880 SO-8/ 12mOhm/ 4.5Vgs/ 84.08880.037
L/S: FDS6676AS SO-8/ 7.25mOhm/ 4.5Vgs/ 84.06676.A37
Switching freq-->400KHz

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 1D8V/0D9V(TPS5116)
Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB
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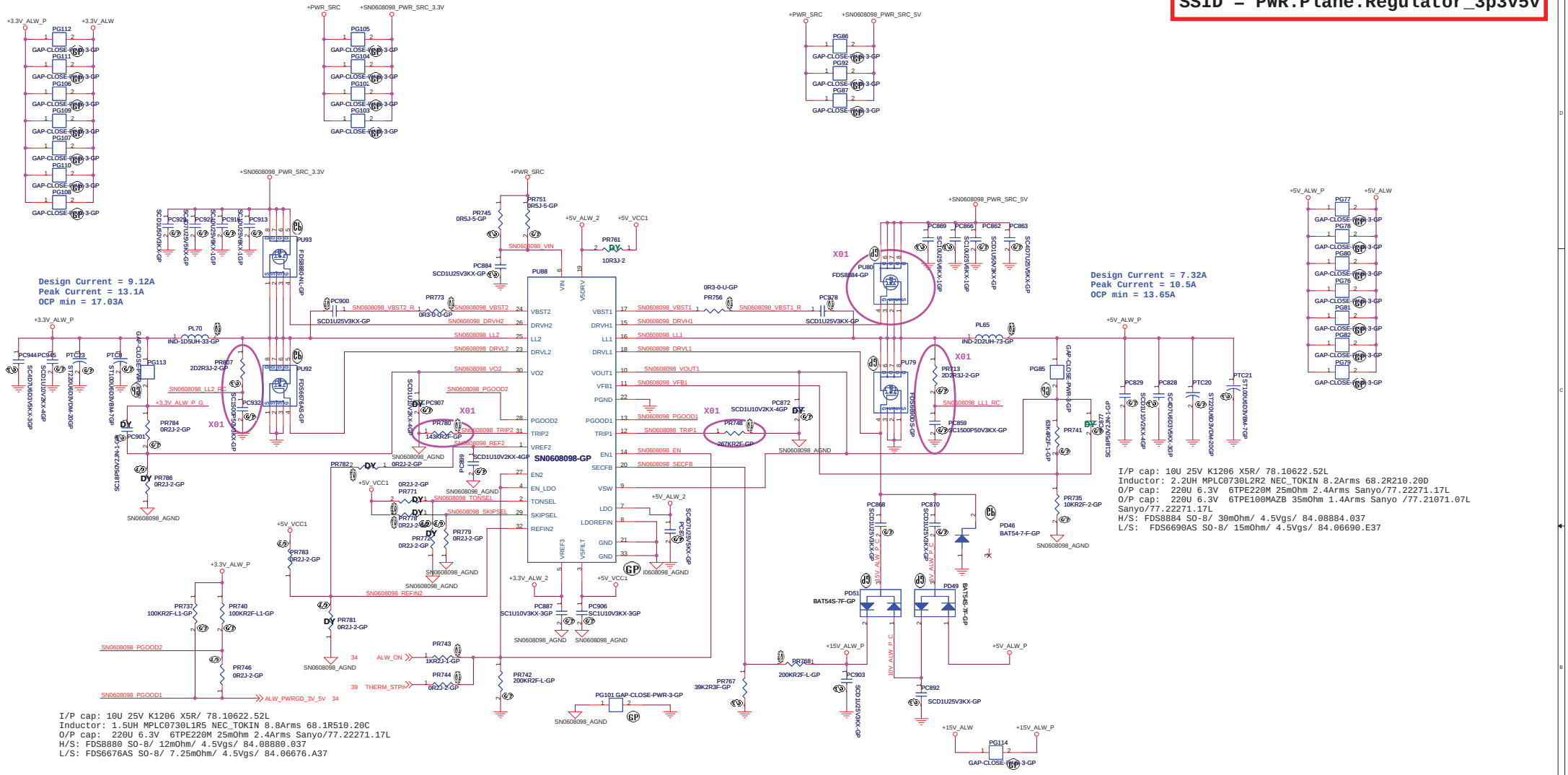
SSID = PWR.Plane.Regulator_3p3v5v



SKIPSEL	GND	FLOAT/VREF2	V5IN
Operating Mode	Auto Skip	OATM	PWM

TONSEL	GND	VREF2 or Float	V5FILT
CH1 Freq	400kHz	400kHz	200kHz
CH2 Freq	500kHz	300kHz	300kHz

	TABLE1 MAXIM ,INTERSIL & TI BOM differences		
	MAXIM	INTERSIL	TI
R	10ohm	NO STUFF	NO STUFF
C	1uF	0.1uF	1uF

		Min	Typ	Max
VOUT2 Output	3.3V Preset Output: REFIN2 = 5V, VIN = 5.5V to 28V, SKIPSEL = 5V	3.285 (-1.4%)	3.33	3.375 (+1.4%)
	1.05V Preset Output: REFIN2 = 3.3V, VIN = 5.5V to 28V, SKIPSEL=5V	1.038 (-1.2%)	1.05	1.062 (+1.2%)
	Tracking Output: REFIN2 = 1.0V, VIN = 5.5V to 28V, SKIPSEL = 5V	0.99 (-1%)	1.00	1.01 (+1%)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

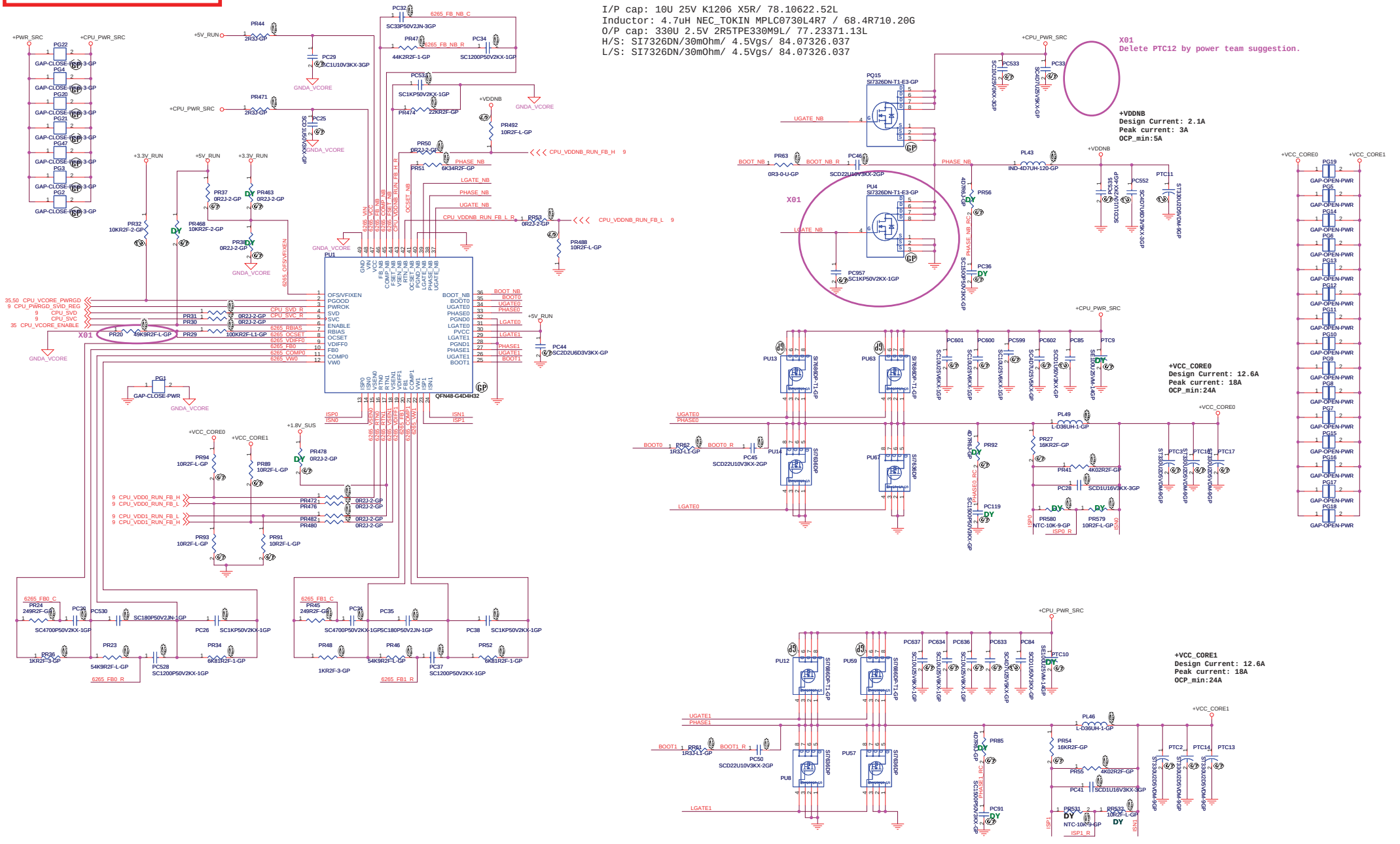
Title: DCDC 5V/3D3V (TPS51125)

Size: A2 | Document Number: FOOSE-AMD 15.4" | Rev: SB

Date: Friday, January 04, 2008 | Sheet 46 of 53

SSID = CPU.Regulator

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 4.7uH NEC_TOKIN MPLC0730L4R7 / 68.4R710.20G
O/P cap: 330U 2.5V 2R5TPE330M9L/ 77.23371.13L
H/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037
L/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36uH ETQP4LR36WFC / 68.R3610.20A
O/P cap: 330U 2.5V 2R5TPE330M9L/ 77.23371.13L
H/S: SI7686DP/ POWERPAK-8/ 14mOhm/ 4.5Vgs/ 84.07686.037
L/S: SI7636ADP/ POWERPAK-8/ 4.8mOhm/ 4.5Vgs/ 84.07636.037

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: +VCC_CORE(ISL6265HR)

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SSID = Reset.Suspend

+3VSUS Source
Design current: 210mA
Max current: 300mA

+5VSUS Source
Design current: 700mA
Max current: 1005mA

+1.2VSUS Source
Design current: 75mA
Max current: 100mA

+5VRUN Source
Design current: 2096mA
Max current: 2994mA

+3.3V_RUN Source
Design current: 5309mA
Max current: 7585mA

+1.8V_RUN Source
Design current: 1305mA
Max current: 1864mA

SUS Power Discharge

RUN Power Discharge

ODD PWR
Design current: 1050mA
Max current: 1500mA

HDD PWR
Design current: 840mA
Max current: 1200mA

+1.2V_RUN Source
Design current: 1883mA
Max current: 2690mA

Wistron Corporation
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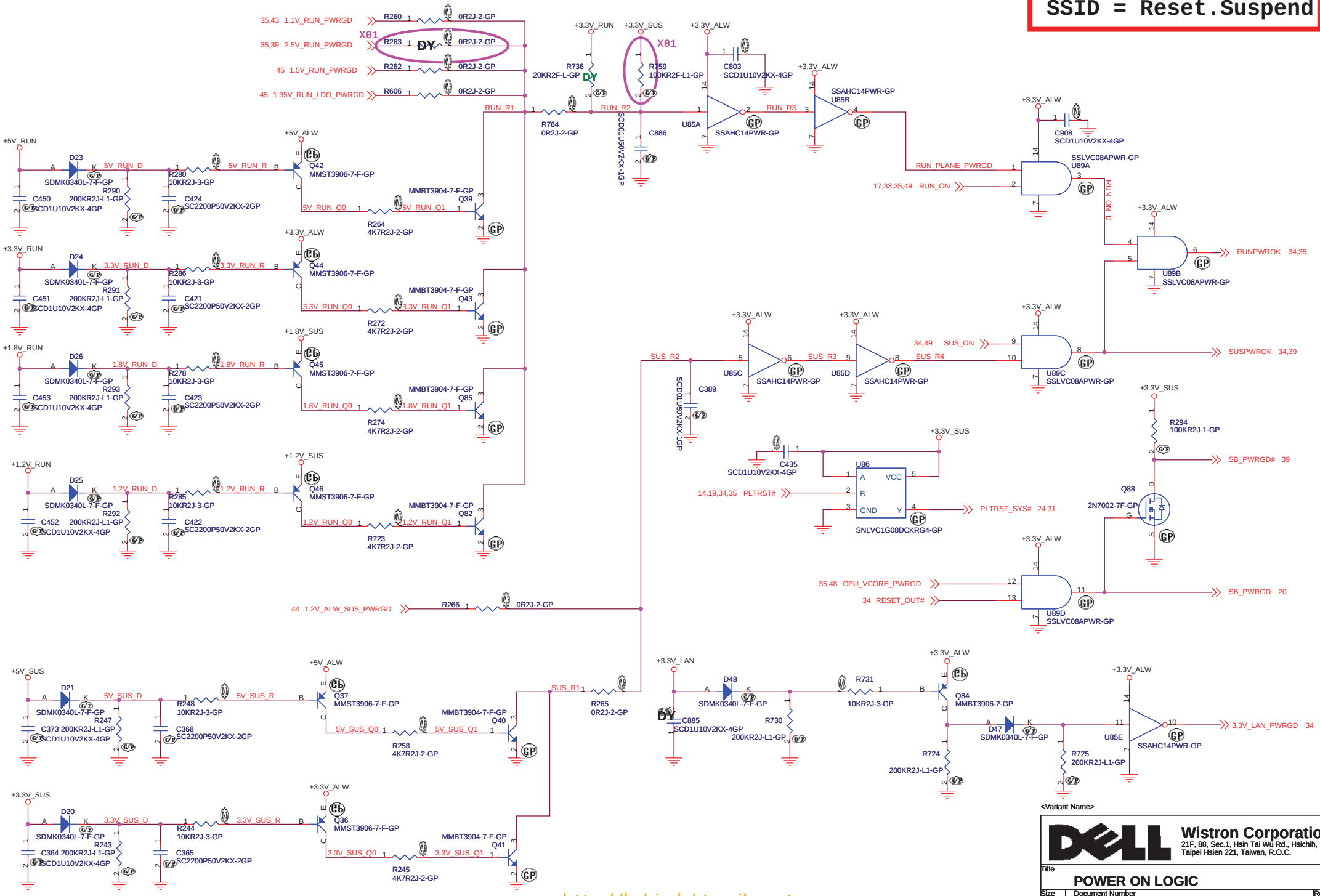
Taipei Hsien 221, Taiwan, R.O.C.

Title: PWRPLANE&RESETLOGIC
Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB
Date: Friday, January 04, 2008 | Sheet 48 of 53

SSID = Reset.Suspend



<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER ON LOGIC

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A3	FOOSE-AMD 15.4"	SB

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SSID=Mechanical

H1 HOLE
H2 HOLE
H3 HOLE
H4 HOLE
H5 HOLE
H6 HOLE
H7 HOLE
H8 HOLE
H9 HOLE
H11 HOLE 34.4H103.001
H12 HOLE
H13 HOLE
H14 HOLE
H15 HOLE
H16 HOLE
H17 HOLE 34.4X801.001
H18 HOLE 34.4X801.001
H19 HOLE 34.4X802.001
H20 HOLE
H21 HOLE
H22 HOLE

H10
GEN8

+3.3V_RUN
U10A TSAHC14PW-GP
U10C TSAHC14PW-GP
U10D TSAHC14PW-GP
U10E TSAHC14PW-GP
AUD_AGND

+5V_CRT_RUN
U56C SSAHCT125PWR-GP
U56D SSAHCT125PWR-GP

SSID=EMI

SPR1 SPRING-24-GP 34.45T31.001
SPR2 SPRING-7 34.49U26.001
SPR3 SPRING-24-GP 34.45T31.001
SPR4 SPRING-24-GP 34.45T31.001
SPR8 SPRING-58-GP 34.4B312.002
SPR5 SPRING-24-GP 34.45T31.001
SPR6 SPRING-24-GP 34.45T31.001
SPR7 SPRING-58-GP 34.4B312.002
SPR9 SPRING-24-GP 34.45T31.001
SPR10 SPRING-24-GP 34.45T31.001
SPR11 SPRING-24-GP 34.45T31.001

+PWR_SRC
EC21 EC22 EC23 EC24 EC25 EC26 SCD1U25V3KX-GP
+5V_ALW
EC27 EC28 SCD1U10V2KX-4GP
+3.3V_ALW
EC29 EC30 EC31 SCD1U10V2KX-4GP
+3.3V_RUN
EC32 EC33 EC34 EC35 EC36 EC37 EC38 EC39 SCD1U10V2KX-4GP
+DOCK_PWR_BAR
EC40 EC41 EC42 SCD1U25V3KX-GP
+3.3V_RUN
EC43 EC44 SCD1U10V2KX-4GP

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: MISC
Size: A3 | Document Number: FOOSE-AMD 15.4" | Rev: SB
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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
11/08	X01	1	06	Add R831 for CLK gen. X'tal. Add C801 and C849 for CLK gen. +3.3V power.	Follow vendor suggestion.	EE
		2	06	Change L10, L20, L28 to Muruta material.	Change material to meet PSL.	EE
		3	14	Remove R240 and short R674 pin 1 (page 9) and R241 pin1.	R240 is extra 0 ohm resistor. R241 is enough.	EE
		4	19	Delete RP1 by AMD suggestion.	Pin INT# already have internal PU.	EE
		5	20	Connect USB_OC#2_3 to SB700 pin F8 and E4. Connect USB_OC#0_1 to SB700 pin A9.	Follow GPIO table.	EE
		6	21	Add test pad TP117~TP143 commanded from GG list.	Follow AMD check list.	EE
		7	40	Change RN1 pull-high power to +3.3V_ALW_2.	Change to +3.3V_ALW_2 to prevent NB_AC_OFF floating under battery mode.	EE
		8	40	Change C539 from 0.47U 16V to 0.47U 25V cap.	The cap connect to 19.5V power, the spec of original cap is only 16V	EE
		9	21, 29	Add HDD_DET# connect from HDD to SB700 pin C4, change PU power to +3.3V_ALW_R.	Follow GG list.	EE
		10	34	Change MEC5035 pin 19 to RC_ID, pin 30 to SUSPWROK.	Follow GG list and GPIO table.	EE
		11	34	JDBG1 pin 2 connect to R789 and then connect to HOST_DEBUG_RX.	Follow GG list.	EE
		12	29, 35	MDC_RST_DIS# change from SB700 to 5028 pin 102 and change pull-high power to +3.3V_ALW	Follow GG list.	EE
		13	35, 49	No populate R263 and populate R178.	For 2.5V_RUN_PWRGD issue.	EE
		14	31	Connect WIMAX_LED to LED_WWAN_OUT# through a 0 ohm resistor R832.	Follow GG list. Implement WiMAX LED.	EE
		15	36	Add a net "+NBDOCK_DC_IN_SS" to dock connector pin 41 for battery protection.	Follow GG list.	EE
		16	18, 32	Delete SPDIF_SHDN circuit at page 18. Short SPDIF_OUT and R643 pin 1.	SPDIF_SHDN is no longer used in Dell's M09 audio architecture. This signal can be deleted. The SPDIF output will be turned off whenever a DRM event occurs.	EE
		17	31, 35	Add a net "WPAN_RADIO_DIS#" from ECE5028 pin 25 to D53 pin 2. Add D53 to be a OR gate to or WWAN_RADIO_DIS# and WPAN_DARIO_DIS# GPIO signals from ECE5028. Also pull-high D53 pin 3 to +3.3V_RUN but no pop.	In Foose there are WWAN and WPAN module will co-use a WWAN mini card slot. This change is for disable WWAN and WPAN module properly.	EE
		18	20, 21	Remove the second SPI ROM SPI2.	Follow GG list.	EE
		19	06	Change RN20 from 33 ohm to 0 ohm.	Vendor change chipset version to D.	EE
		20	09	Change RN48 pull-high power from +1.8V_SUS to +1.8V_RUN.	Follow AMD suggestion.	EE
		21	20	Add test pad from TP69, TP144~TP148 for integrated uC.	Follow AMD check list.	EE
		22	22	Change L29 from max current 300mA to 2A.	Follow AMD suggestion.	EE
		23	19	No populate R765 suggested by AMD.	No populate R765 suggested by AMD.	EE
		24	30	Swap U26 pin 2 and pin 6.	1A connect to 1B, and 2A connect to 2B from spec.	EE
		25	48	Populate C434 with 0.1U 16V cap.	Solution for +1.2V_RUN issue.	EE
		26	40	Remove C2 and C3.	Pop these cap will cause the problem to read SMBus.	EE
		27	14	Change R607 pull-high power from +3.3V_RUN to +1.8V_RUN.	Follow AMD suggestion.	EE
		28	14	Add U96 for PWRGD signal from SB to NB and EC. Because EC need +3.3V power, SB and NB only need +1.8V power.	Follow AMD suggestion.	EE
		29	34	Change X6 to vendor EPSON, C791 and C802 from 22pF to 33pF.	Follow vendor suggestion.	EE
		30	27	Change X5 from CL=20pF to CL=12pF.	Follow vendor suggestion.	EE
		31	32	Change R88 from 0 ohm to 100 ohm.	Follow vendor suggestion.	EE
		32	34	Add R841 for PWRGD circuit.	Follow AMD suggestion.	EE
		33	37	Change R104 R105 R106 R459 R460 R461 R566 R576 R833 from 10K ohm to 20K ohm.	LEDs have leakage issue.	EE
		34	32	Add 100K ohm resistor R834 for internal MIC feedback circuit.	Follow vendor suggestion.	EE
11/23		35	25	Change LED signal of LOM connector.	Design error.	EE
		36	30	Change U30 to TPS2062A command by DELL.	Follow DELL command.	EE
		37	14	Add R203 but no pop for SUS_STAT# suggested by AMD.	Follow AMD suggestion.	EE
		38	35	Populate R419 and no populate R418 for changing board ID to X01.	Change board ID to X01.	EE
11/29		39	21	Change R700 from 15 ohm to 33 ohm resistor.	For improving SIV signal.	EE
		40	38	Change R362 from 22 ohm to 0 ohm. Add AND gate for POWER_SW_IN3#_IN#.	Follow GG list.	EE

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List

Size	Document Number	Rev
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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
11/29	X01	41	24	No pop R157 by Broadcom suggestion.	Make sure the PWR_DOWN pin is only pulled to GND and never asserted (Sighting S2_5761_31695).	EE
		42	34	Change ACAV_IN circuit net name.	Follow GG list.	EE
		43	38	MAX8731A_IINP change from EMC4002 pin 48 to pin 45. Change R160 to 4.7K ohm.	Follow GG list.	EE
		44	36	Pop R1,R16 and no pop R7,R9.	Follow GG list.	EE
		45	19	Change R322 from 33 ohm to 0 ohm.	Improve signal measured by SIV team.	EE
		46	41	No pop R489 to let ADAPT_TRIP_SEL NC.	Follow GG list.	EE
		47	23	Change ROM strip PU and PD resistor from 2.2K to 10K.	AMD chipset SB700 change version from A11 to A12.	EE
		48	22	Change power for SB700 VDD from +1.2V_ALW_SUS to +1.2V_RUN.	AMD chipset SB700 change version from A11 to A12.	EE
		49	48	Short +1.2V_SUS and +1.2V_ALW_SUS by L68, no pop enable related circuit.	Solution of +1.2V_SUS leakage.	EE
12/05		50	45	Add R840 and R841 for +0.9V_DDR_VTT, and no pop R840.	Correct DDR power sequence to SUS plan.	EE
		51	20	Pop R367 and R785 to PU EC5035 pin11 and pin66 by vendor suggestion.	Follow vendor suggestion.	EE
12/10		52	16	No pop L23 and populate L24 for RS780 version changed from A11 to A12.	AMD chipset RS780 change version from A11 to A12.	EE
		53	36	No pop Q1 Q21 R6 R85 for RS780 version changed from A11 to A12.	AMD chipset RS780 change version from A11 to A12.	EE
		54	39	Change I/O board pin define for solution of audio noise.	The solution for MIC noise when recording.	EE
		55	18	Remove S-vedio signal from U28, and short to connector side directly. Add D57 and remove R185 for power leakage.	DELL will remove S-vedio function from DOCK at next version.	EE
		56	36	Modify DPC_DOCK_HPD and DPB_HPD circuit from DELL command.	Follow DELL command.	EE
12/13		57	19	Change R336, R319, R321, R331, R324, R830 from 22 ohm to 49.9 ohm. C950 change from 22pF to 12pF and populate it.	Solution of PCICLK EA.	EE
		58	34	Remove U37 and C904 from DELL command.	Follow GG list.	EE
		59	35	No connect SIO5028 pin 70.	Follow GG list.	EE
		60	33	Add R626 and R629 for AUD_HP1_OUT_R1 and AUD_HP1_OUT_L1.	Follow GG list.	EE
12/20		61	32,33	Separate analog ground form digital ground for audio.	Solution of audio noise.	EE
		62	37	Use BAT2_LED# to control blue LED, and use BAT1_LED# to control amber LED.	Correct KBC GPIO for controlling battery LED.	EE
		63	09	Add R686, R694, R699 to protect noise for CPU and HDT.	Follow AMD suggestion.	EE
		64	18	Change L42, L44, L45 from 47 ohm bead to 22 ohm bead. No pop C538, R553, C565. Populate C534, C546, C560 with 5.6pF cap.	Solution of CRT EA.	EE
		65	14,18	Change RN41 from 33 ohm to 0 ohm. Change R151 from 715 ohm to 768 ohm.	Solution of CRT EA.	EE
		66	25	Add R268, R270, R281, R306.	Prevent noise if another TPM is not populated.	EE
12/21		67	36	Swap E-SATA Tx and Rx signals.	E-SATA Tx and Rx signals are wrong.	EE
		68	37	Add Q93, R856, C958, R857.	Synchronize the LED for I/O board and LCD inverter.	EE
		69	36	Add Q8 and Q9 related circuit for DVI signal.	Follow DELL command.	EE
12/26		70	35	No populate PH resistor R356 and add a new 100K PH resistor R468 to +3.3V_ALW for DOCK_DET#.	Change DOCK_DET# PH from +RTC_CELL to +3.3V_ALW to prevent RTC leakage when docked.	EE
		71	35,36	Add C13 and R858 and R844 for DOCK_RST# circuit.	Follow GG list.	EE
12/27		72	35	Change USB_SIDE_EN# and ESATA_USB_PWR_EN# PH from +3.3V_ALW to +3.3V_ALW2.	Follow GG list.	EE
		73	26,27	Add R471 and C525 but no-pop, add C807 and C810.	Follow GG list.	EE
		74	25	Change C_TPM circuit.	C_TPM part is changed, so change the circuit.	EE
		75	44	Remove +1.35V_RUN_LDO circuit.	AMD chipset change to A12 and no need to use +1.35V.	EE
12/31		76	14	Change R607 from 4.7K ohm to 300 ohm.	Follow AMD suggestion.	EE
		77	21	Remove R729, R733, R739, R749.	Remove 0ohm and route the trace in the same layer.	EE
01/02		78	36	Add EL69~EL74 for Dock display port EMI.	For Dock display port EMI.	EE

<Variant Name>

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
11/08	X01	1	40	Add a circuit for battery protection.	The command from DELL.	Power Team
		2	41	Change L41 and R465.	Follow power team suggestion.	Power Team
		3	47	Change R20 from 18K ohm to 49.9K ohm.	Follow power team suggestion.	Power Team
		4	39	Add R528 and C951 by power team suggestion.	Add R528 and C951 by power team suggestion.	Power Team
		5	41	Connect U53 drain and R525 pin 1 by power team suggestion. Add Q93 and R838 by power team.	Connect U53 drain and R525 pin 1 by power team suggestion.	Power Team
12/05		6	40	Add Q96, and let its drain connect to R845 at page 42.	The command from DELL.	Power Team
		7	40	Add Q95, and connect gate to DOCK_DET# to prevent +DOCK_PWR_BAR leakage.	Solution of +DOCK_PWR_BAR leakage.	Power Team
		8	41	Change R508 pin2 and Q8 gate from ACAV_IN_NB to ACAV_IN by power team at page42.	A common signal name for all modules.	Power Team
		9	41	Change power +CHAGER_SRC to CHAGER_SRC by power team.	A common signal name for all modules.	Power Team
		10	41	Add Q97 related circuit for net DOCK_DCIN_IS.	The command from DELL.	Power Team
		11	41	Add U7B related circuit for net ACAV_IN_NB.	The command from DELL.	Power Team
		12	41	Add R846 and R847, and connect ISL88731_ICM to R160 pin1.	Follow power team suggestion.	Power Team
		13	41	No pop ADAPT_OC related circuit.	The command from DELL.	Power Team
12/11		14	42	Populate PR650 and PC699.	Follow power team suggestion.	Power Team
		15	43	Change PR718 from 6.2K ohm to 4.02K ohm. Add PC958 but no-pop. Change PR706 PU power from +3.3V_ALW to +3.3V_SUS.	Follow power team suggestion.	Power Team
		16	44	Add PR719 and PR999.	Follow power team suggestion.	Power Team
		17	46	Populate PR807 and PC932. Change PR780 from 240K ohm to 143K ohm. Change PU80 to FDS8884.	Follow power team suggestion.	Power Team
		18	47	Add PC957 and change PU4 same as PQ15.	Follow power team suggestion.	Power Team
12/13		19	47	Remove PTC12 by power team suggetion.	Follow power team suggestion.	Power Team
		20		Change all open-gap to close-gap except the close-gap for VCORE1 and VCORE2.	Follow power team suggestion.	Power Team
12/20		21	49	Change R759 from 20K to 100K.	Follow power team suggestion for L6935 PGOOD issue.	Power Team
		22	44	Add PR585~PR588 by power team suggestion.	Follow power team suggestion.	Power Team
		23	42,43	Change PR656 and PR706 from 200K to 100K ohm.	Follow power team suggestion.	Power Team
12/28		24	40	Add PR855, PQ98, PR856, PD53, PQ99, PQ100, PR857, PR858.	Follow power team suggestion.	Power Team
01/02		25	46	Populate PR713, and populate PC859 from 330pF 50V to 1500pF 50V.	Follow power team suggestion.	Power Team
		26	46	Change PR748 from 249k to 267k ohm.	This is for OCP solution.	Power Team

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