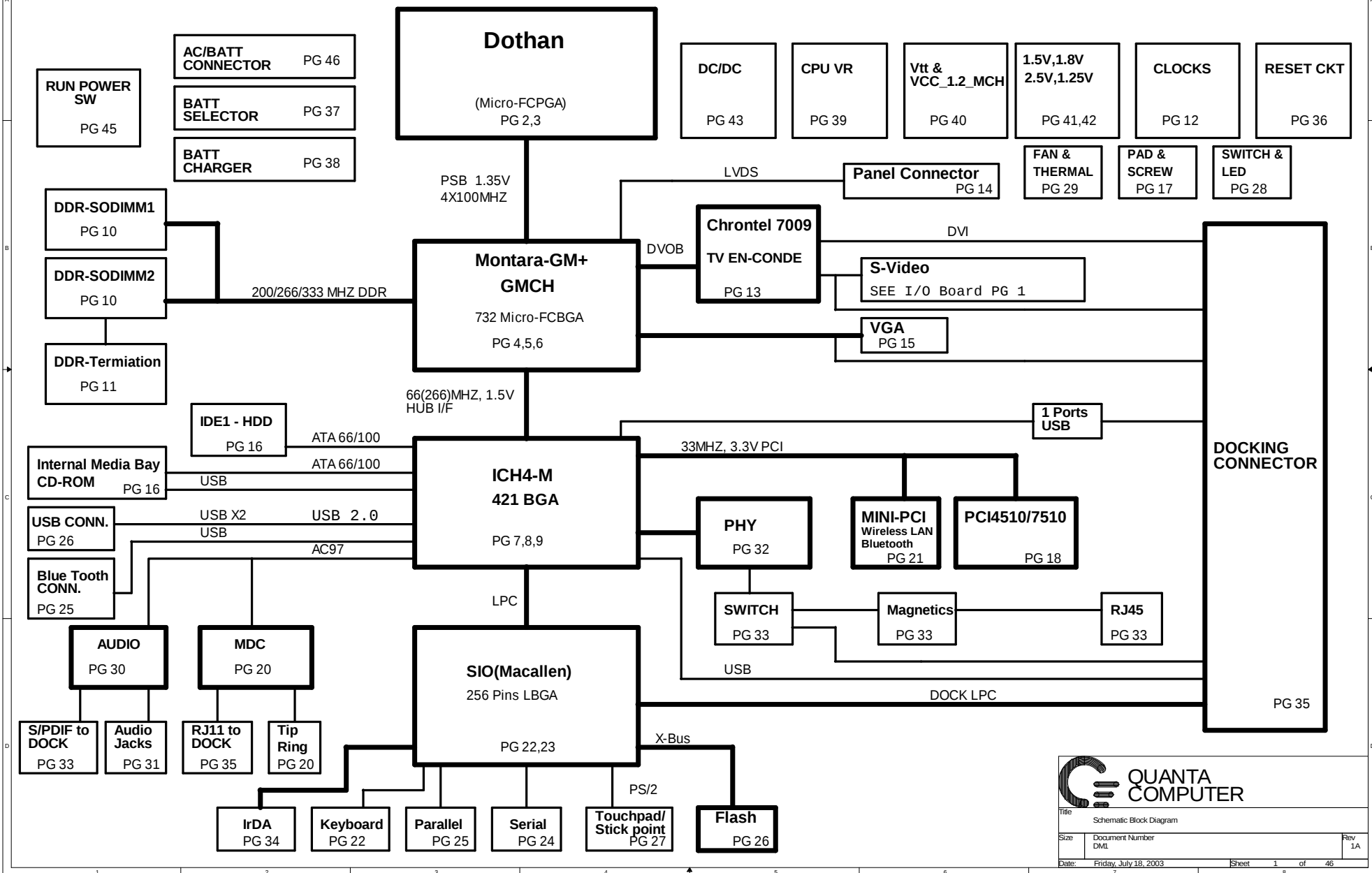
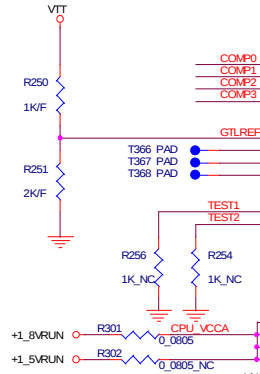
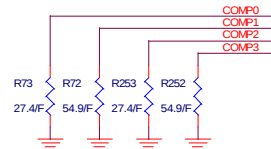


DM1

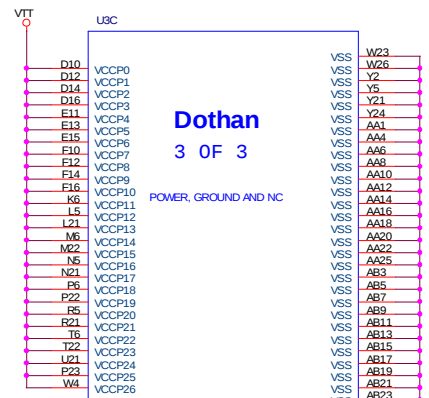
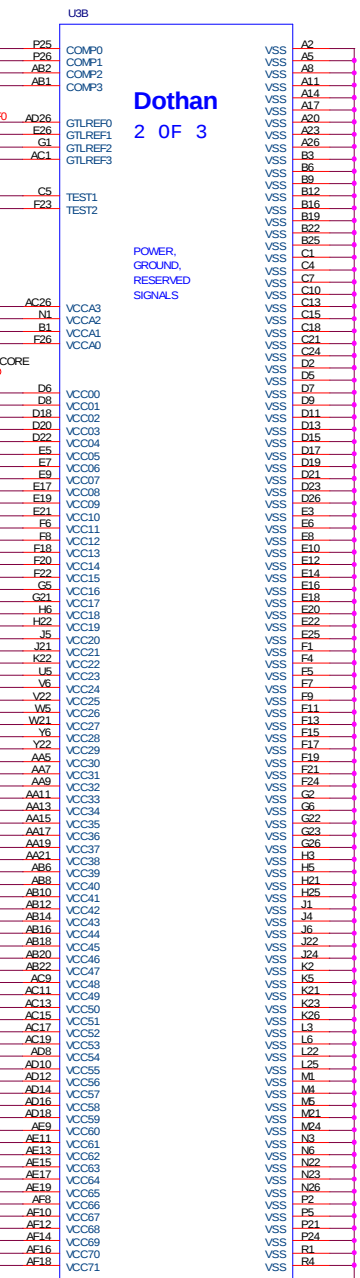


These 4 Resistors need to place with 0.5" of CPU.
Comp0,2 trace need to be zo=27.4 ohm,
comp1,3 traces need to be zo=55 ohm.



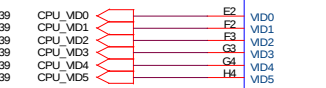
Dothan
2 OF 3

POWER,
GROUND,
RESERVED
SIGNALS

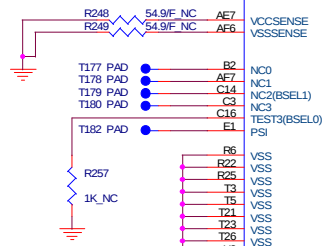


Dothan
3 OF 3

POWER, GROUND AND NC



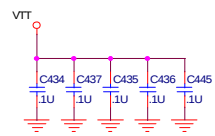
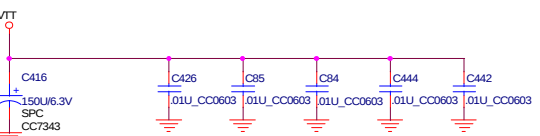
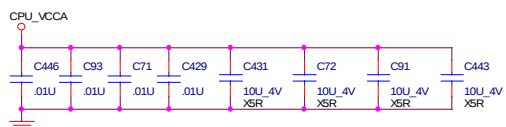
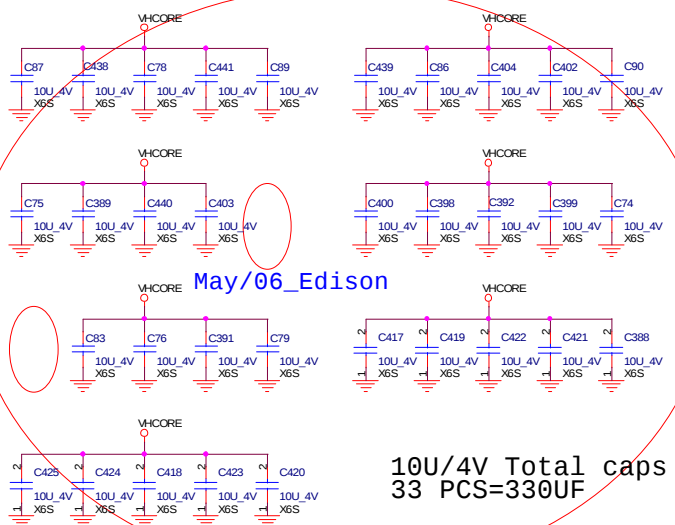
VID



Dothan_Processor

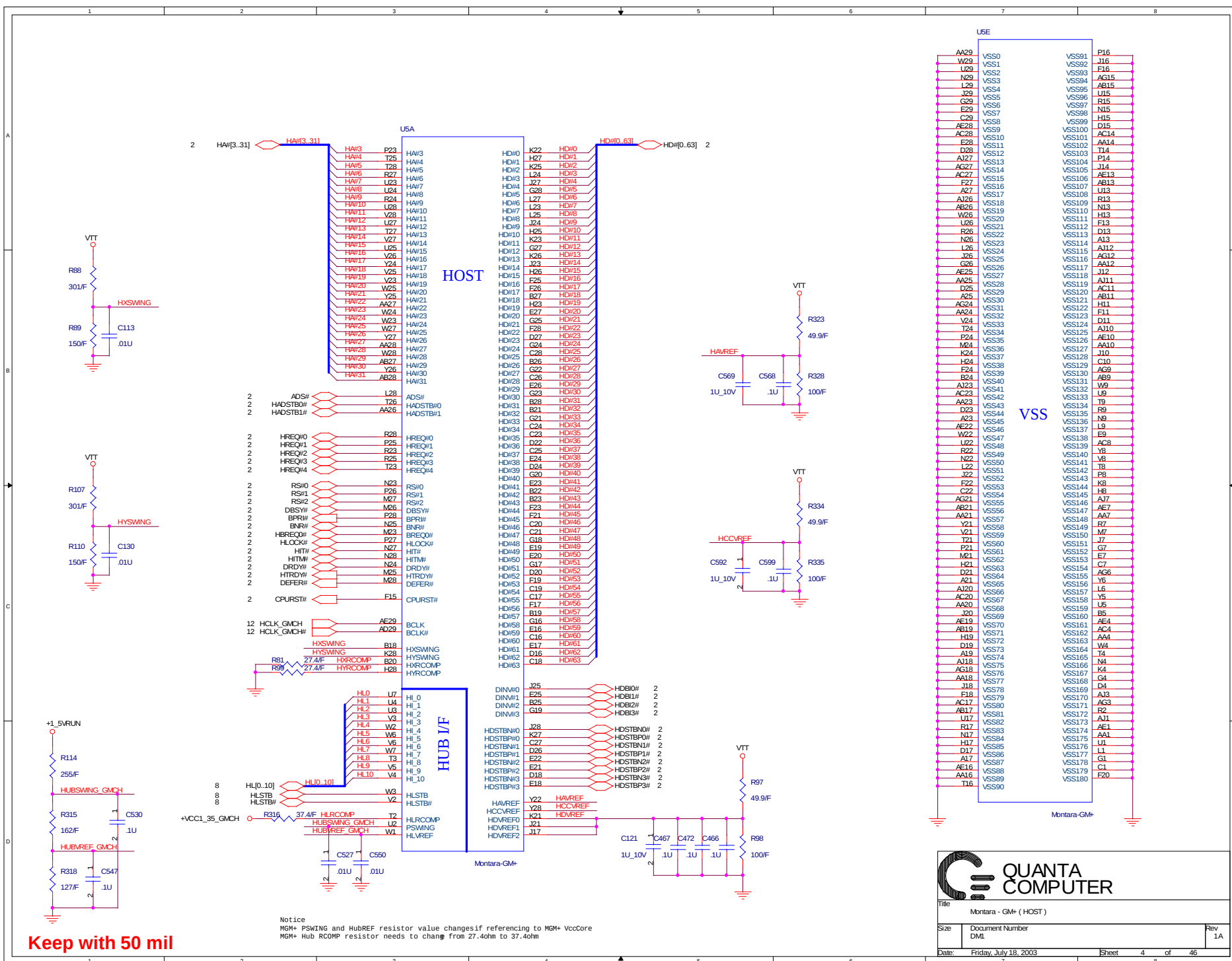
May/06_Edison

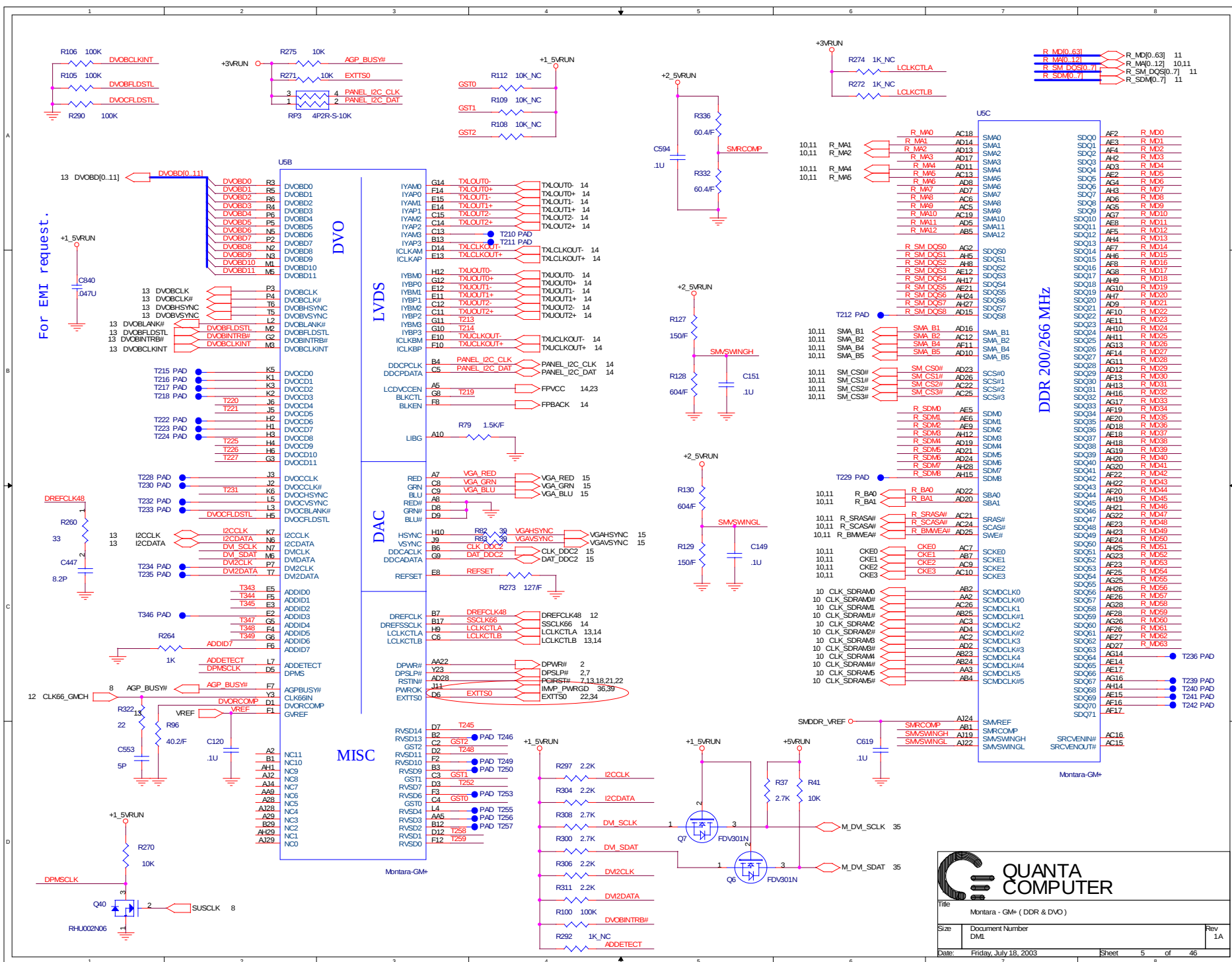
100U/4V Total caps
33 PCS=330UF



**QUANTA
COMPUTER**

Title: Dothan Processor (POWER)		
Size: DMT	Document Number: DMT	Rev: 1A
Date: Friday, July 18, 2003	Sheet: 3	of 46

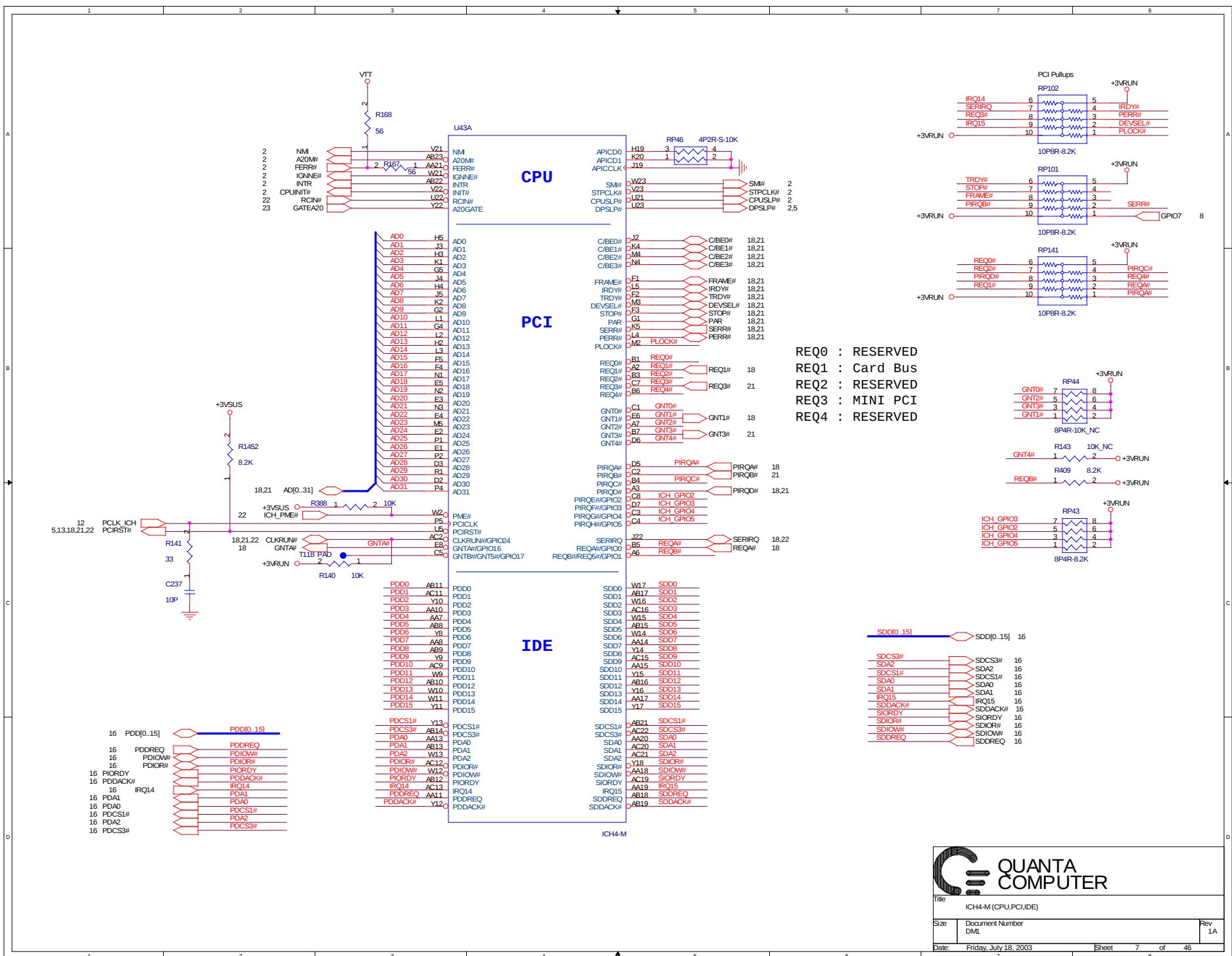


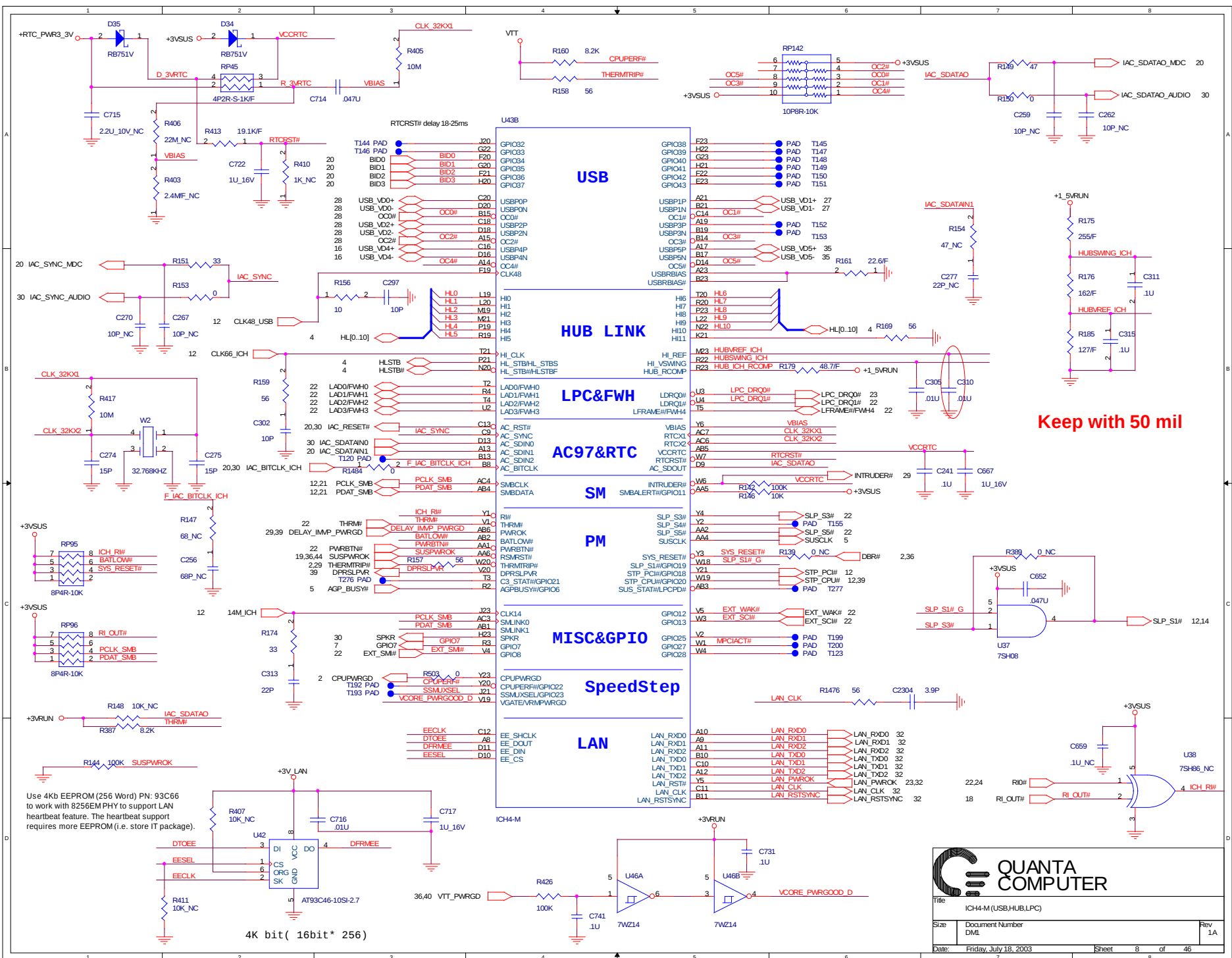


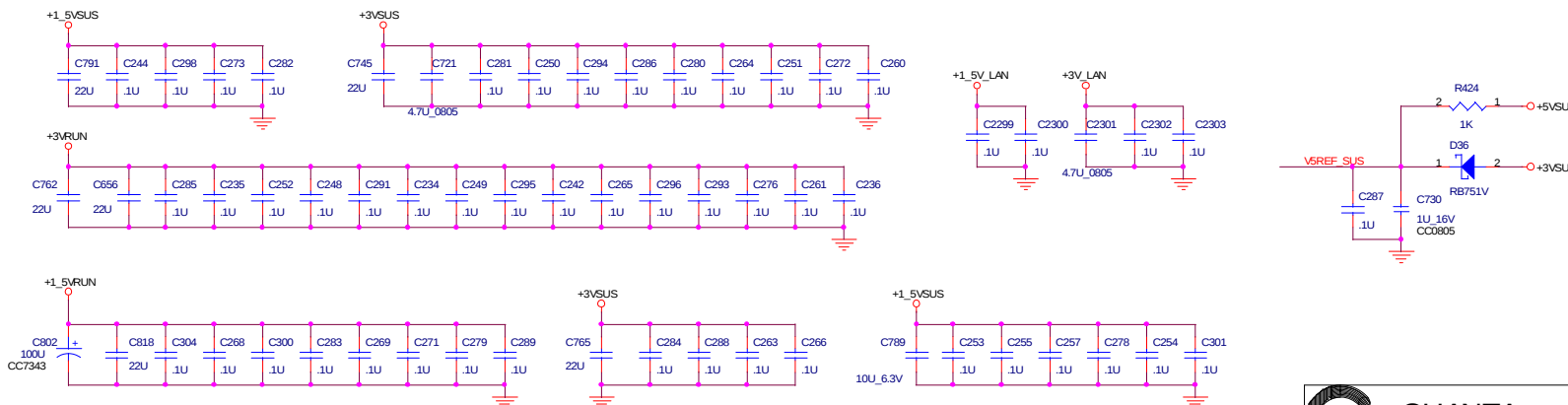
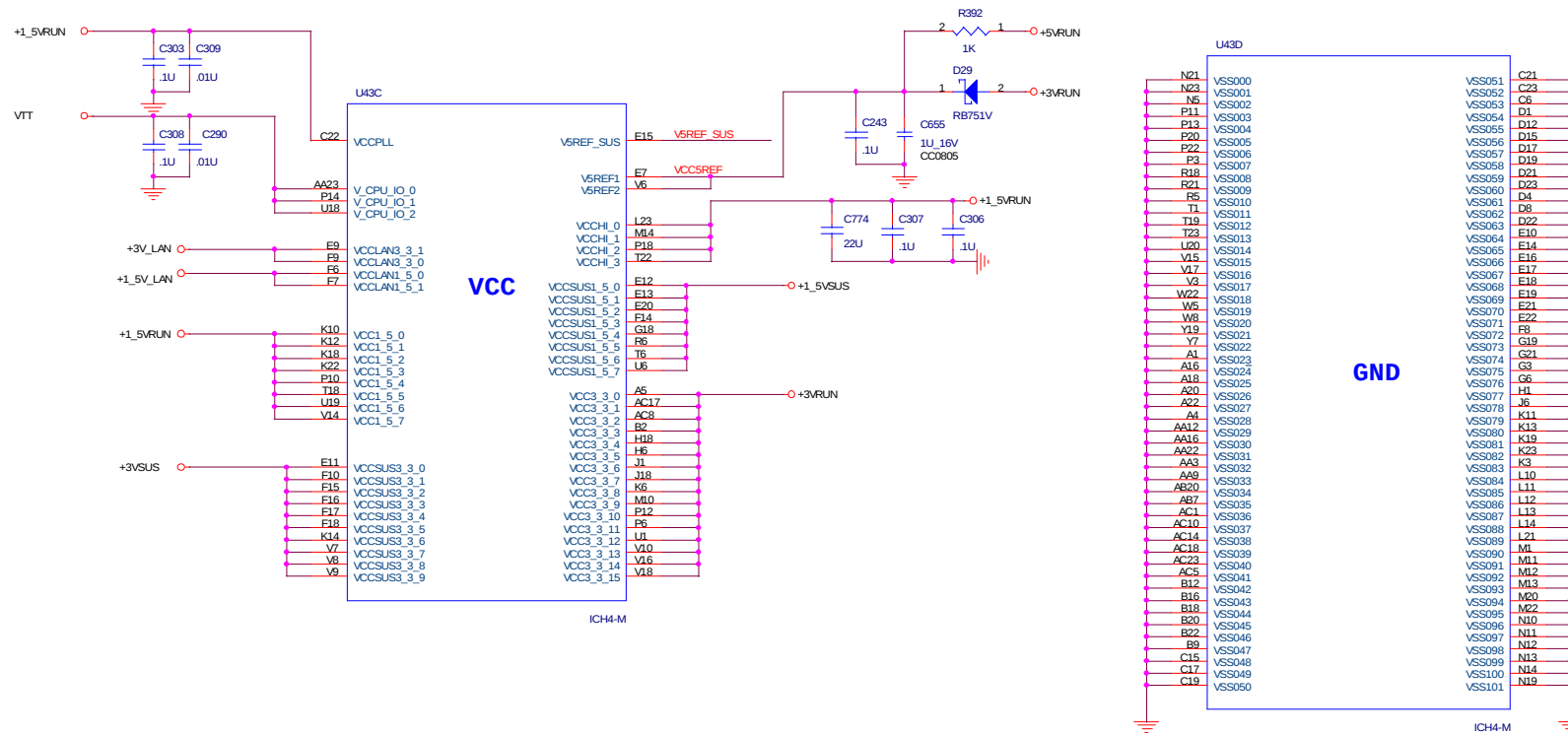
PSLB20G157M(150U_4V)

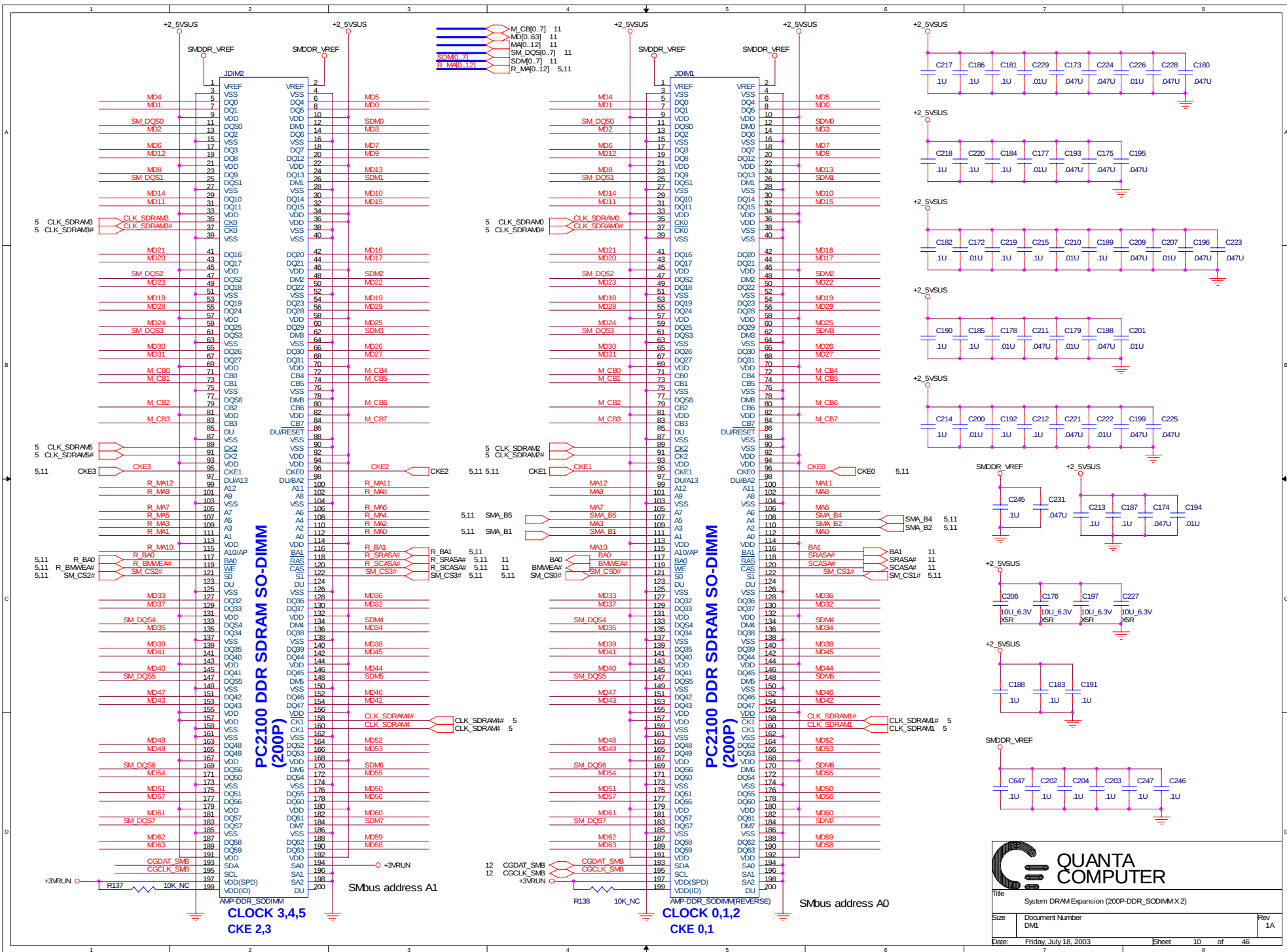
POWER

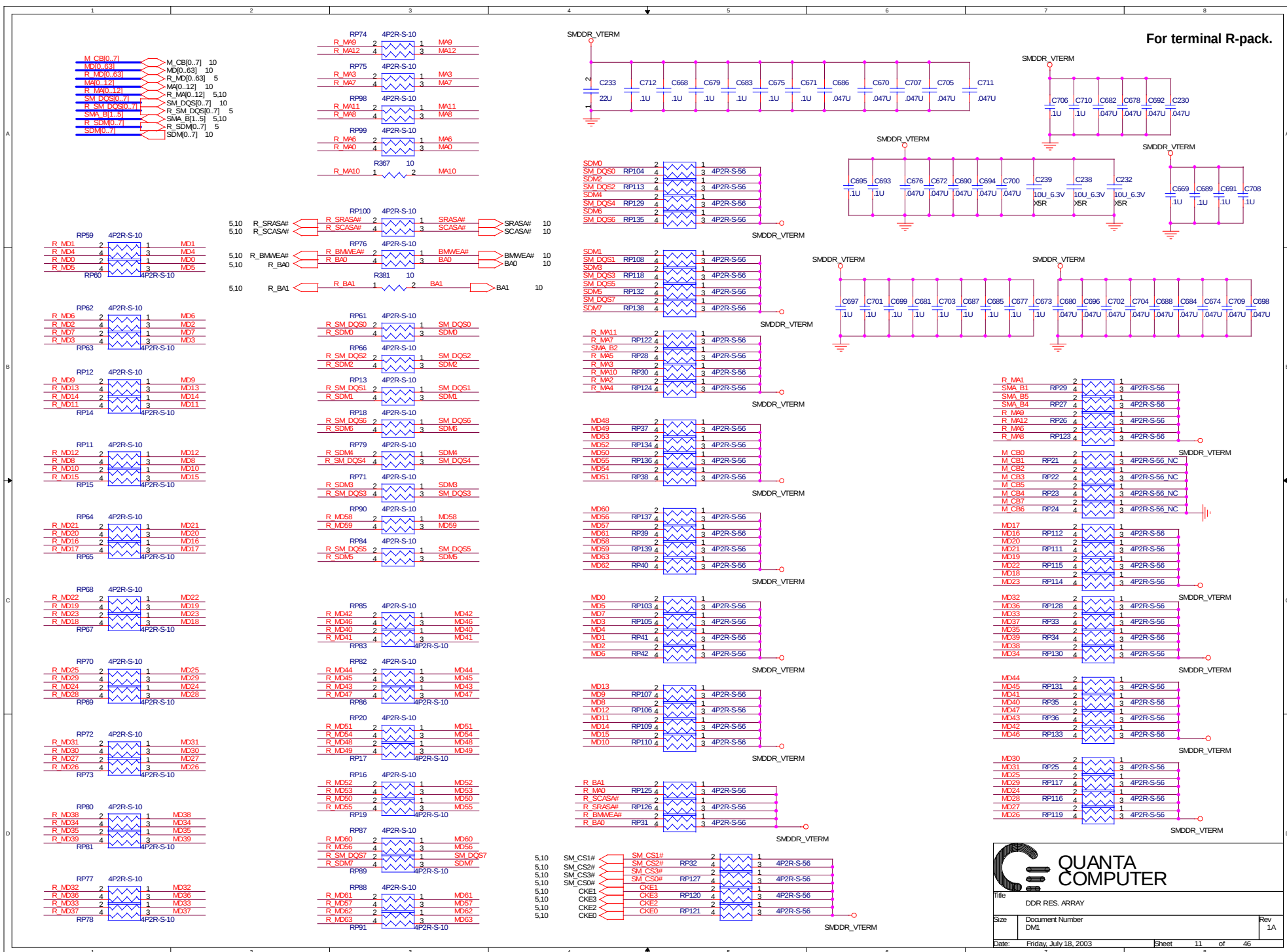




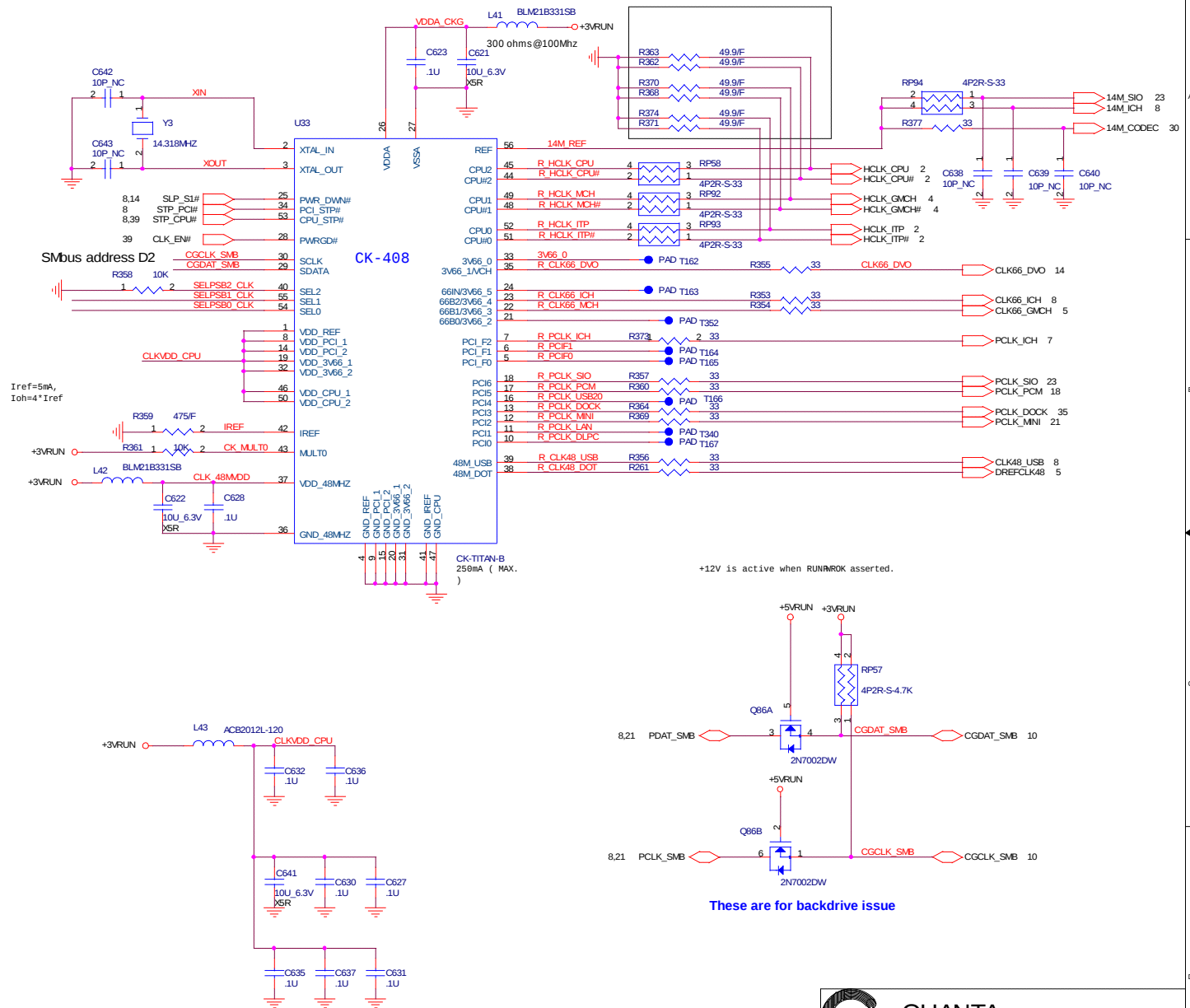




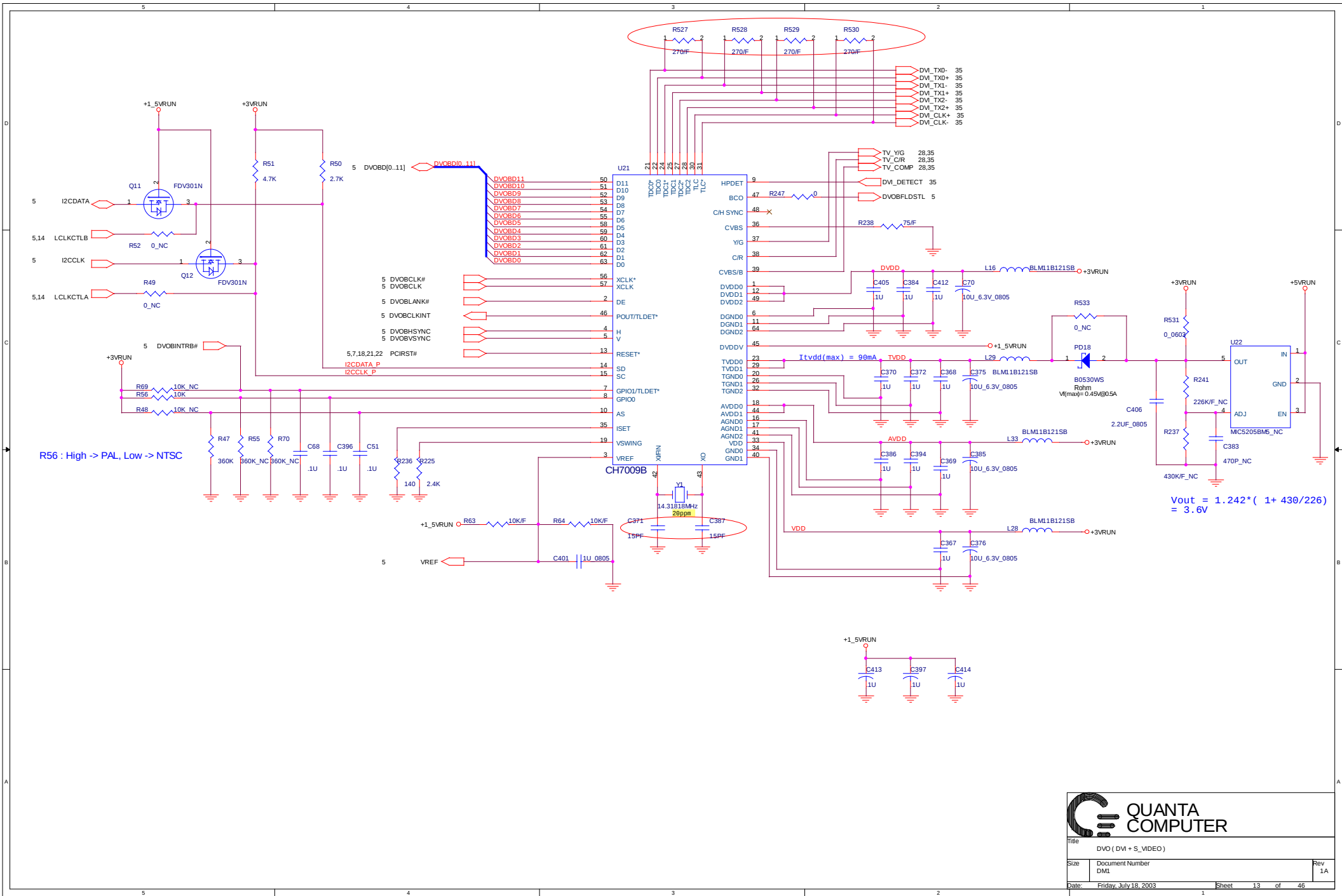


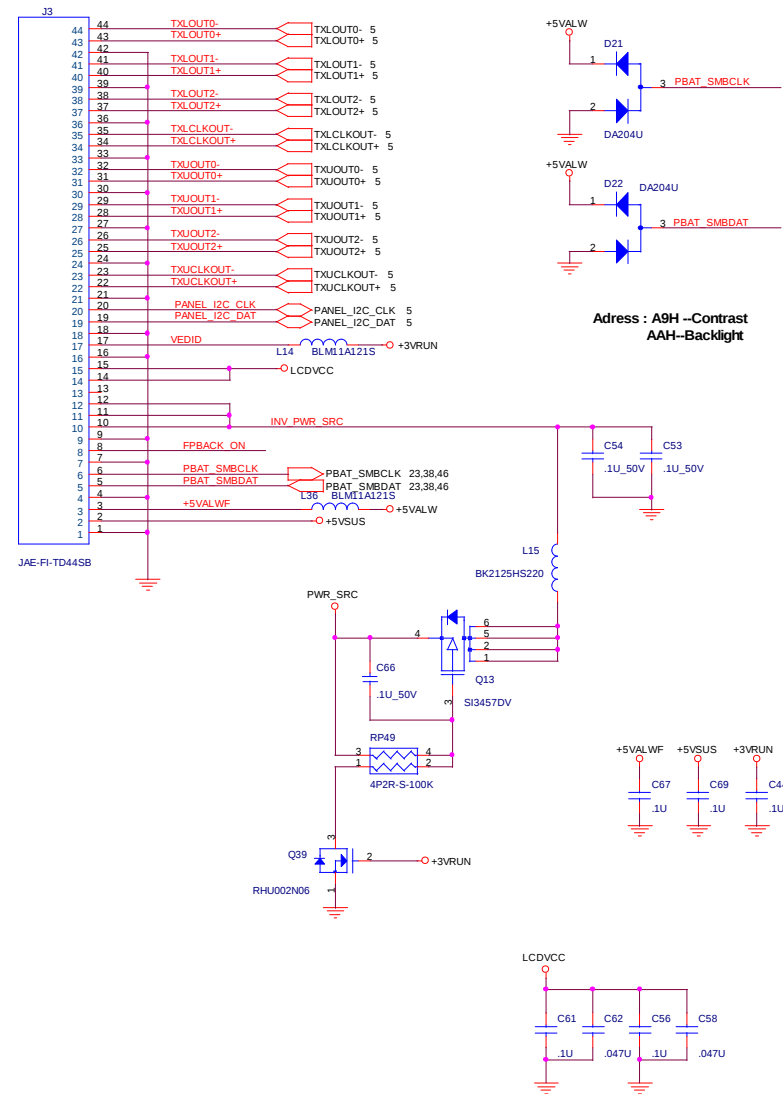
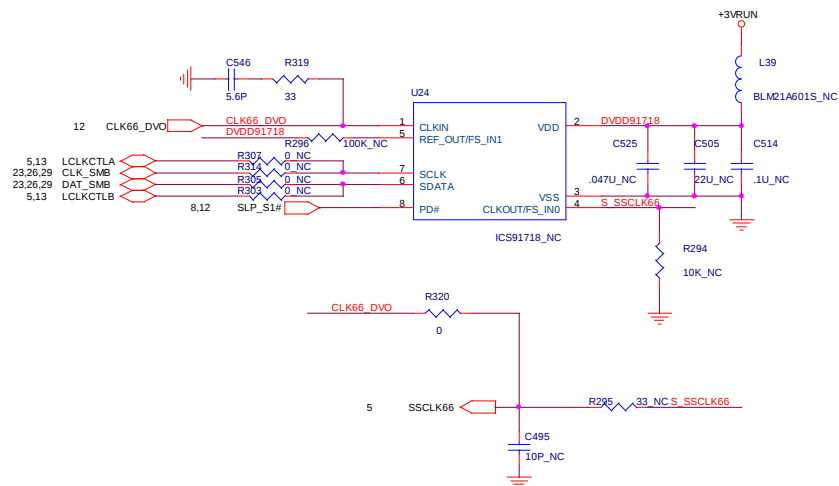
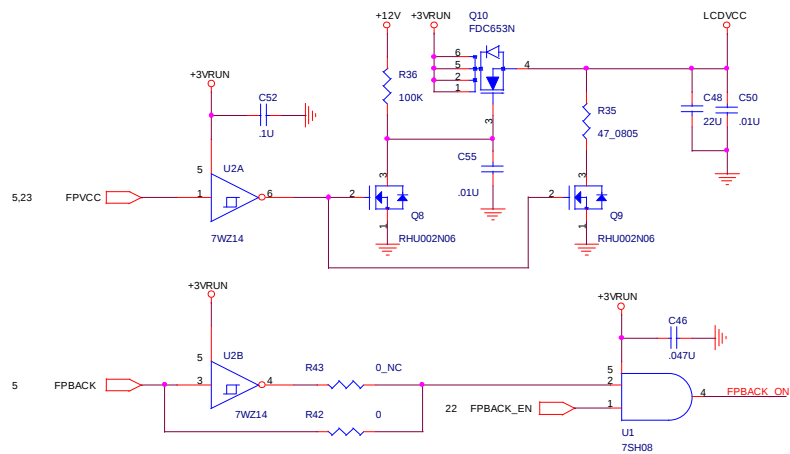


S2	S1	S0	CPU	3V66[0..4]	3V66_5/66IN
1	0	0	66	66IN	66 Input
1	0	1	100	66IN	66 Input
1	1	0	200	66IN	66 Input
1	1	1	133	66IN	66 Input
0	0	0	66	66	66 Input
0	0	1	100	66	66 Input
0	1	0	200	66	66 Input
0	1	1	133	66	66 Input

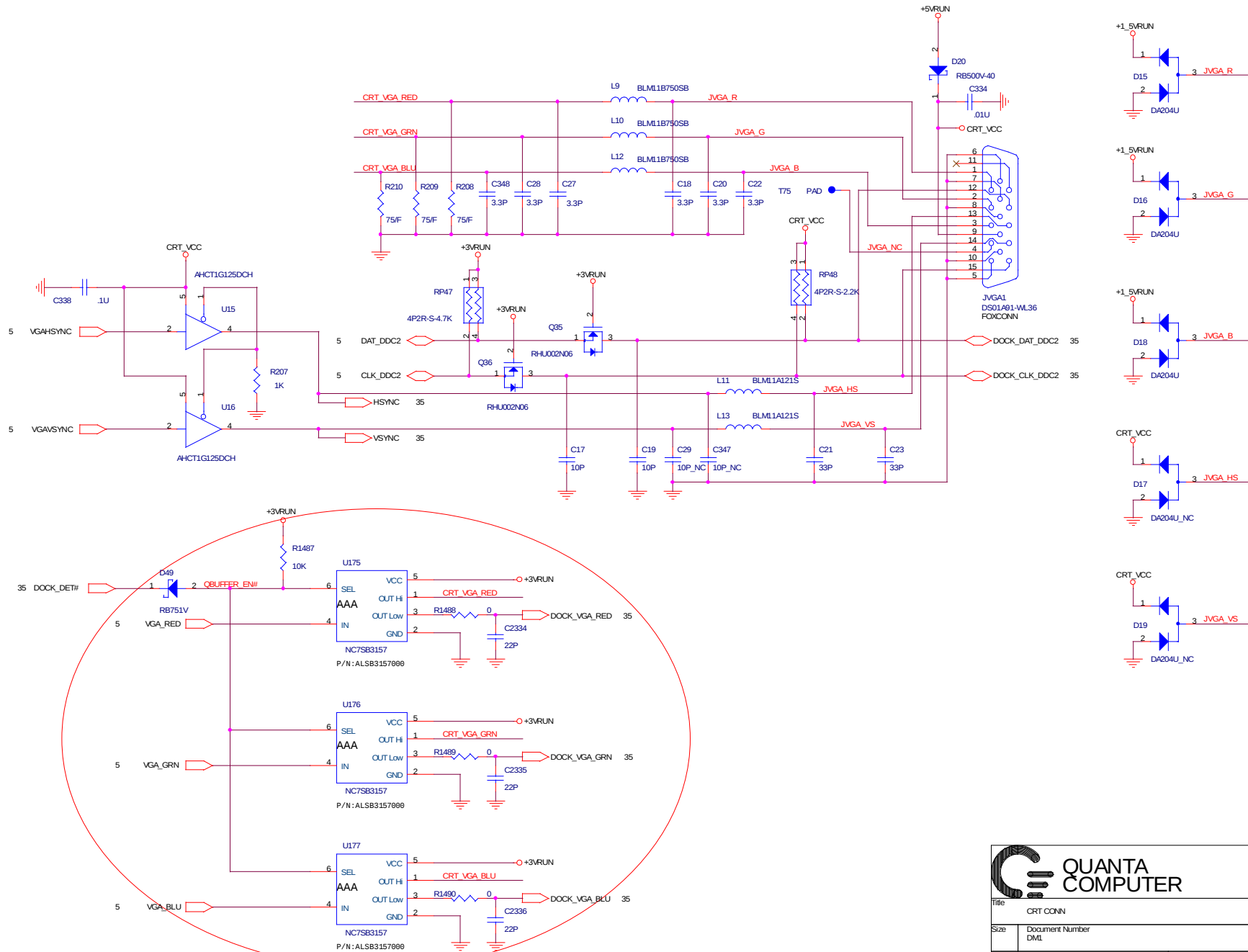


Title			
CLOCK GENERATOR			
Size	Document Number DML		Rev 1A
Date:	Friday, July 18, 2003	Sheet	12 of 46

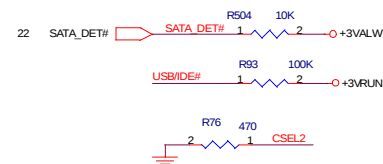
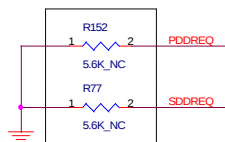
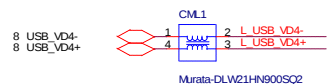
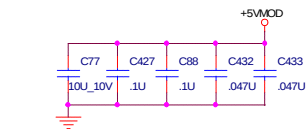
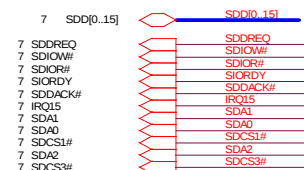
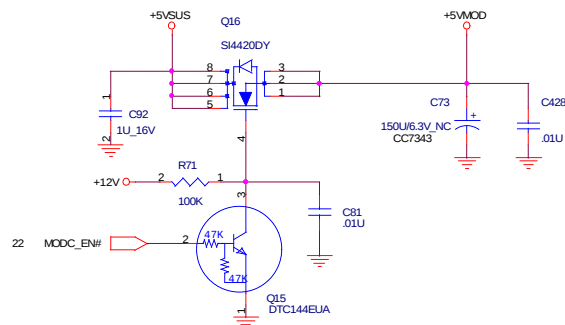
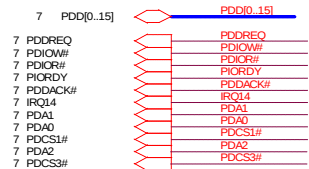
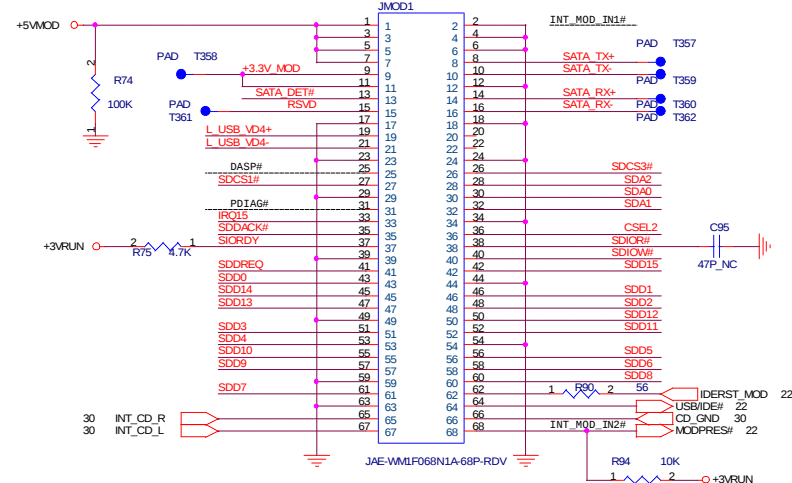
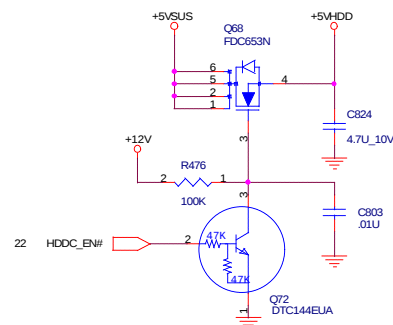
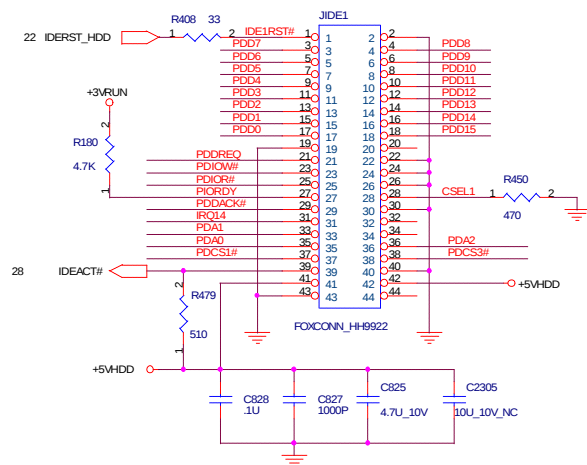
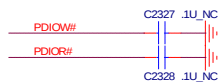




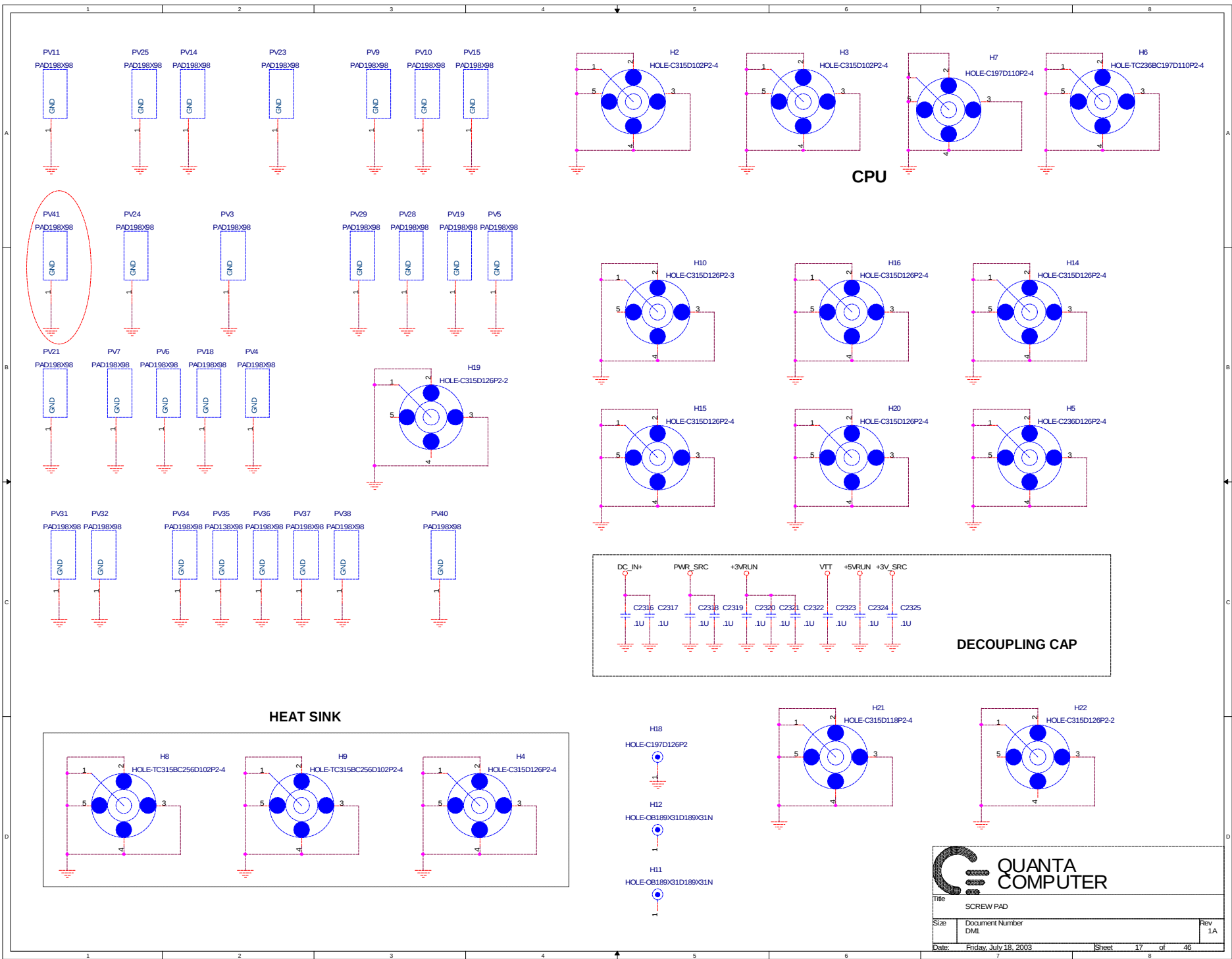
Address : A9H --Contrast
AAH--Backlight

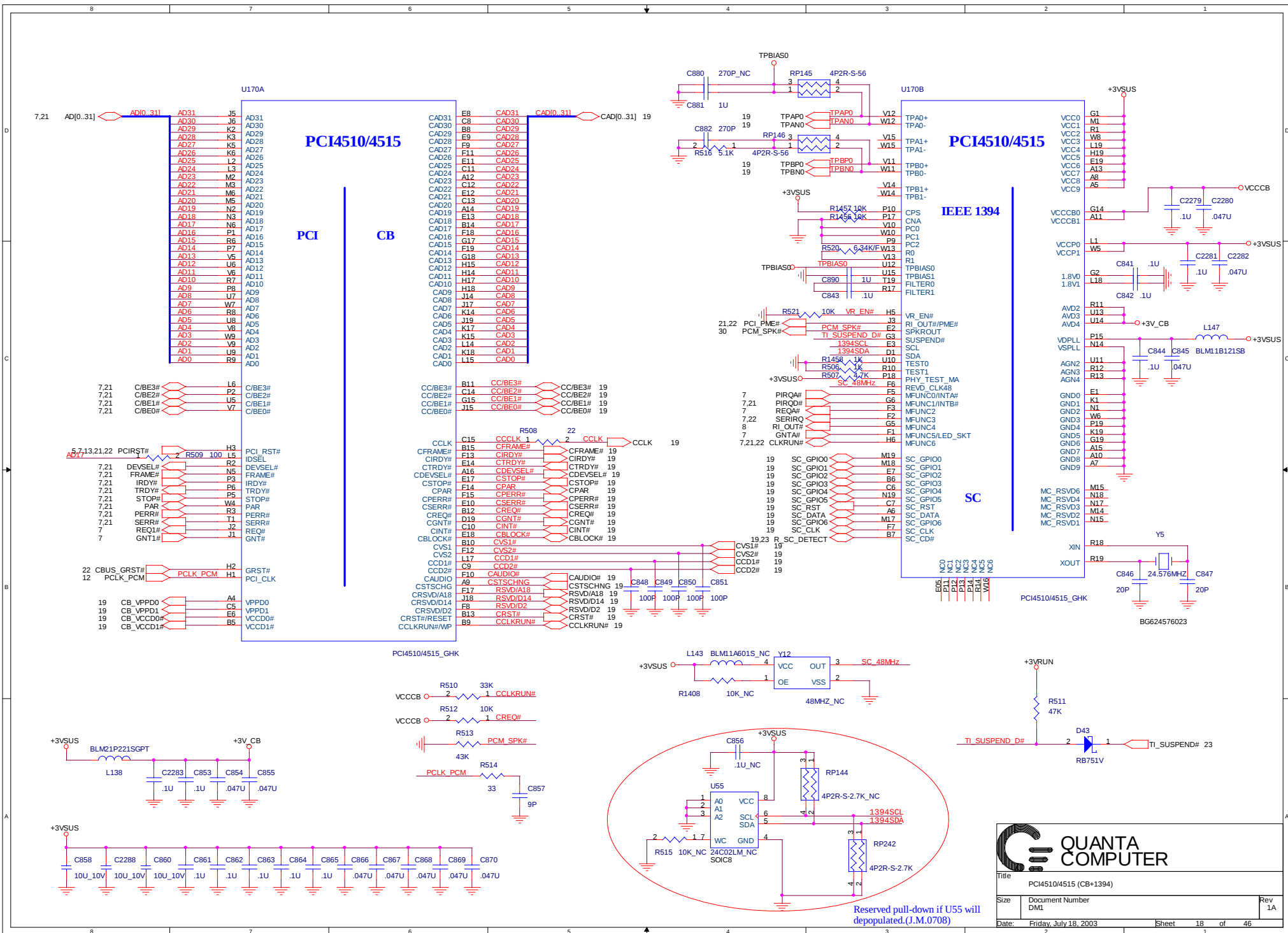


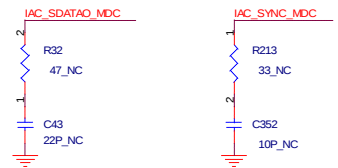
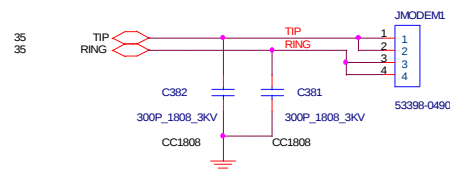
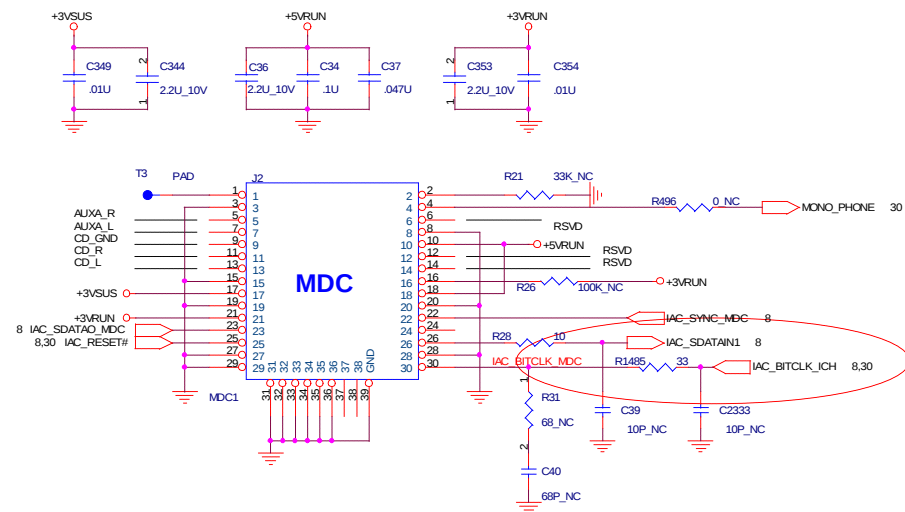
Title			CRT CONN
Size	Document Number	Rev	
	DMT	1A	
Date:	Friday, July 18, 2003	Sheet	15 of 46



Title			IDE (HDD&CD_ROM)
Size	Document Number	Rev	
	DML	1A	
Date:	Friday, July 18, 2003	Sheet	16 of 46

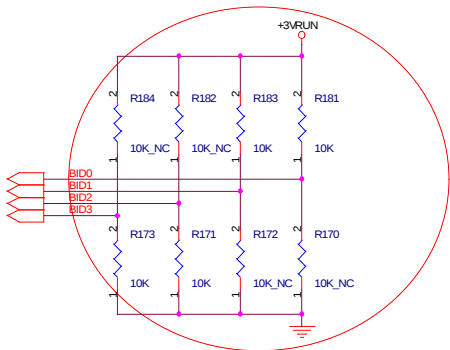


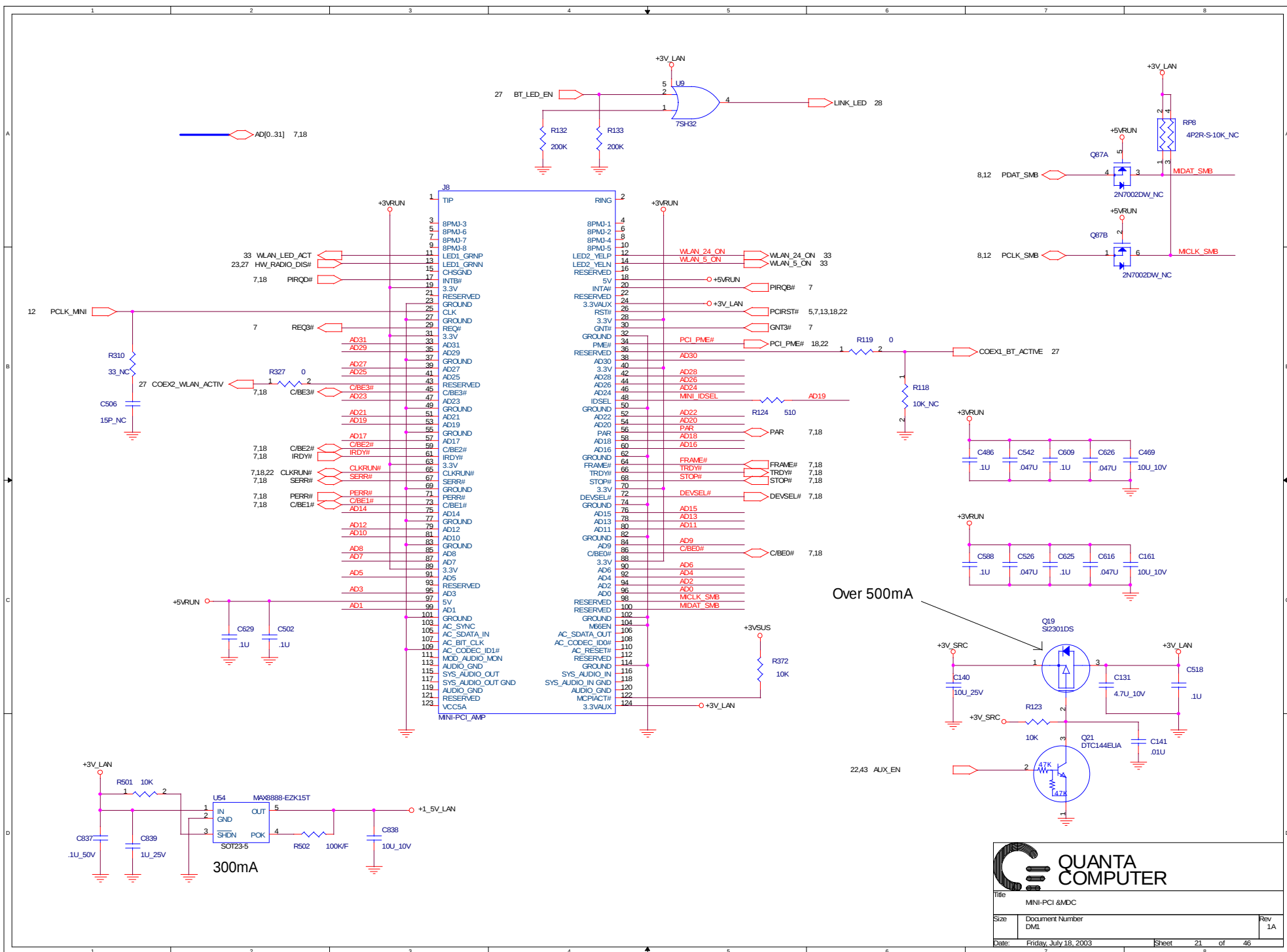


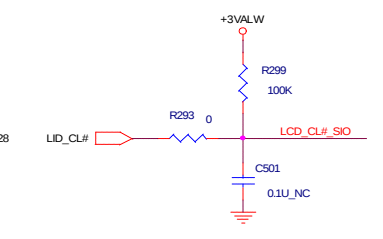
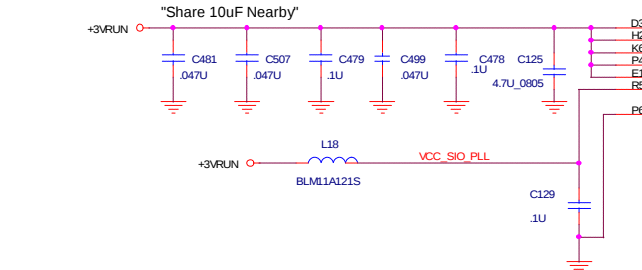
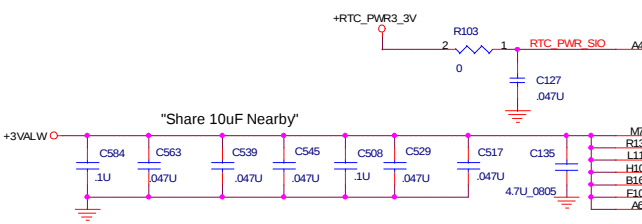
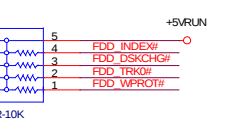
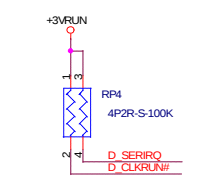
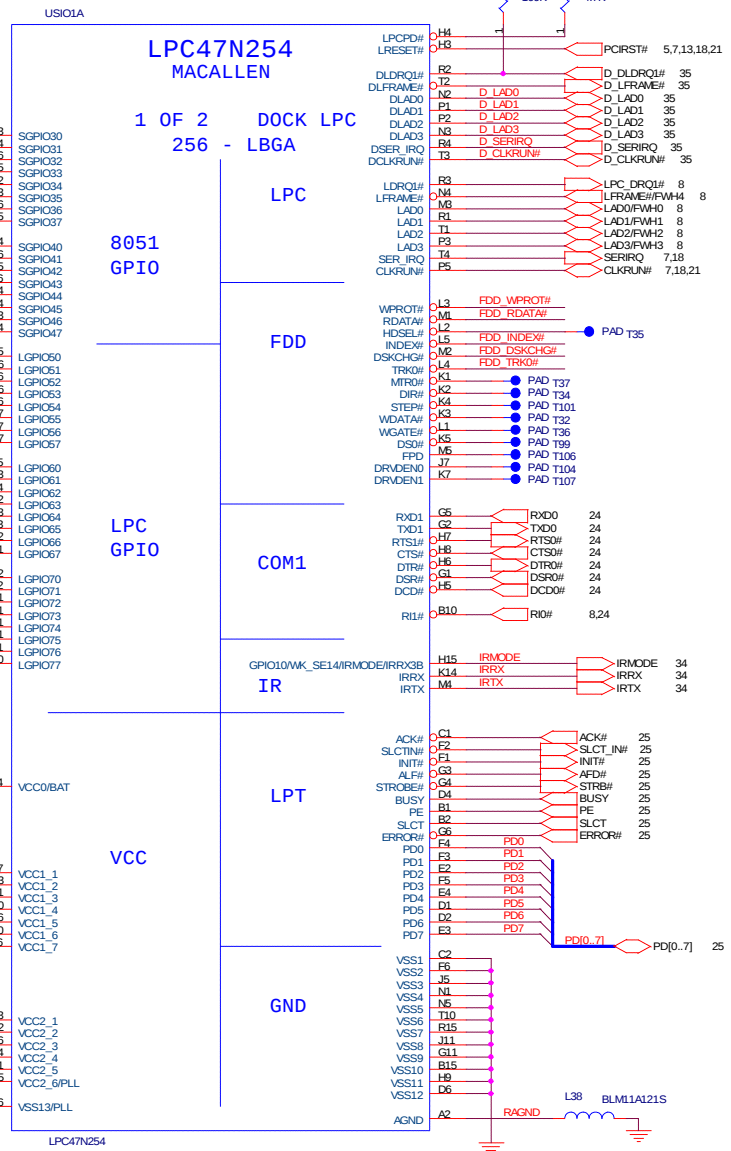
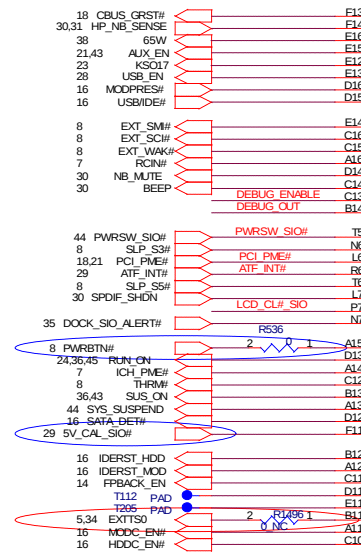
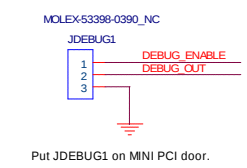
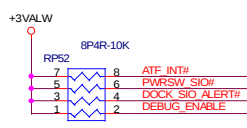
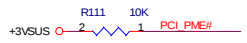


BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	PROTOL
0	0	1	0	PROT02
0	0	1	1	PROT03
0	1	0	0	PROT04
0	1	0	1	QT1
0	1	1	0	RAMP

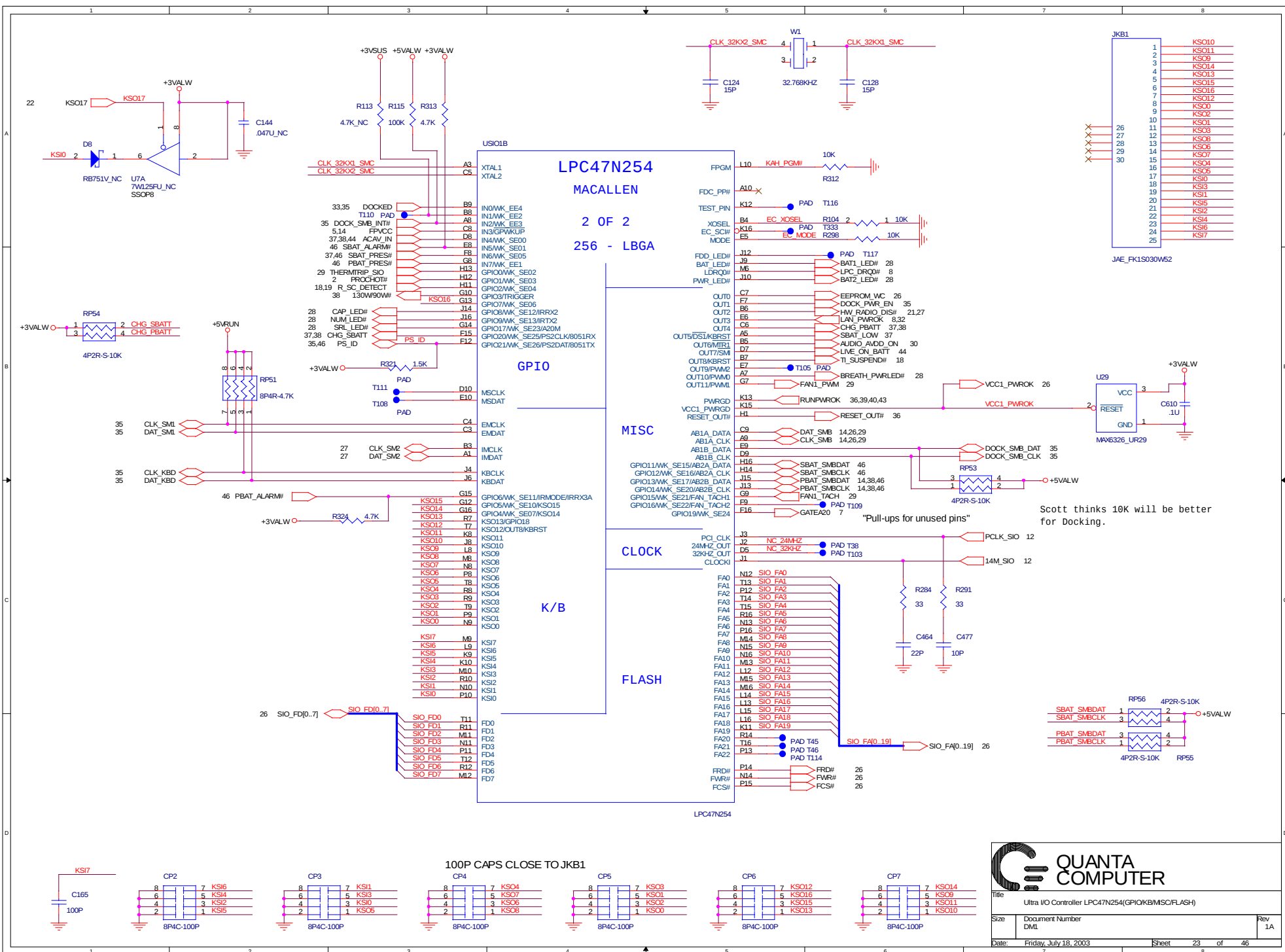
8 BID0
8 BID1
8 BID2
8 BID3

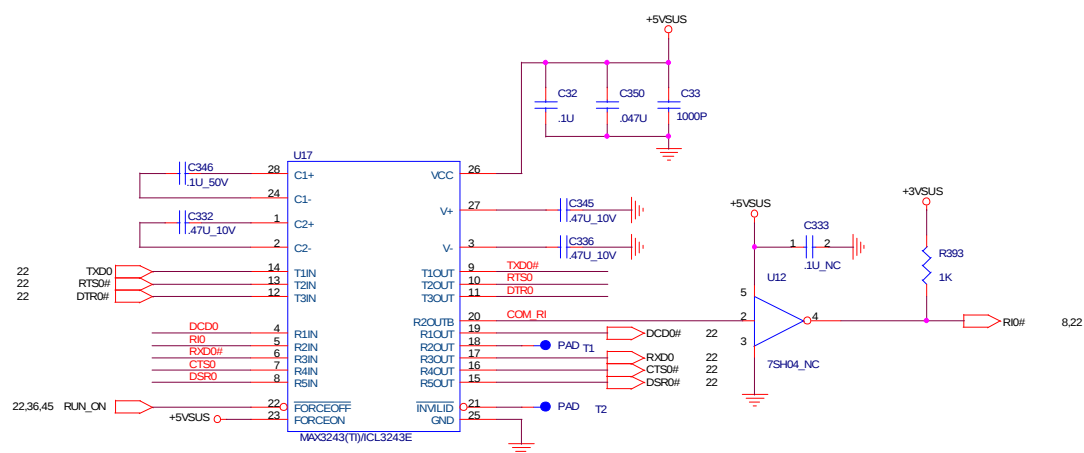




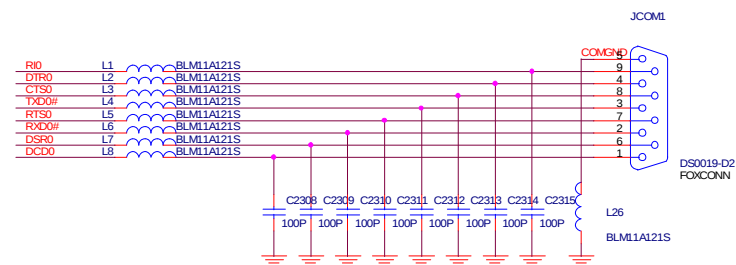


Title			Ultra I/O Controller LPC47N254
Size	Document Number	Rev	
	DMT	1A	
Date:	Friday, July 18, 2003	Sheet	22 of 46

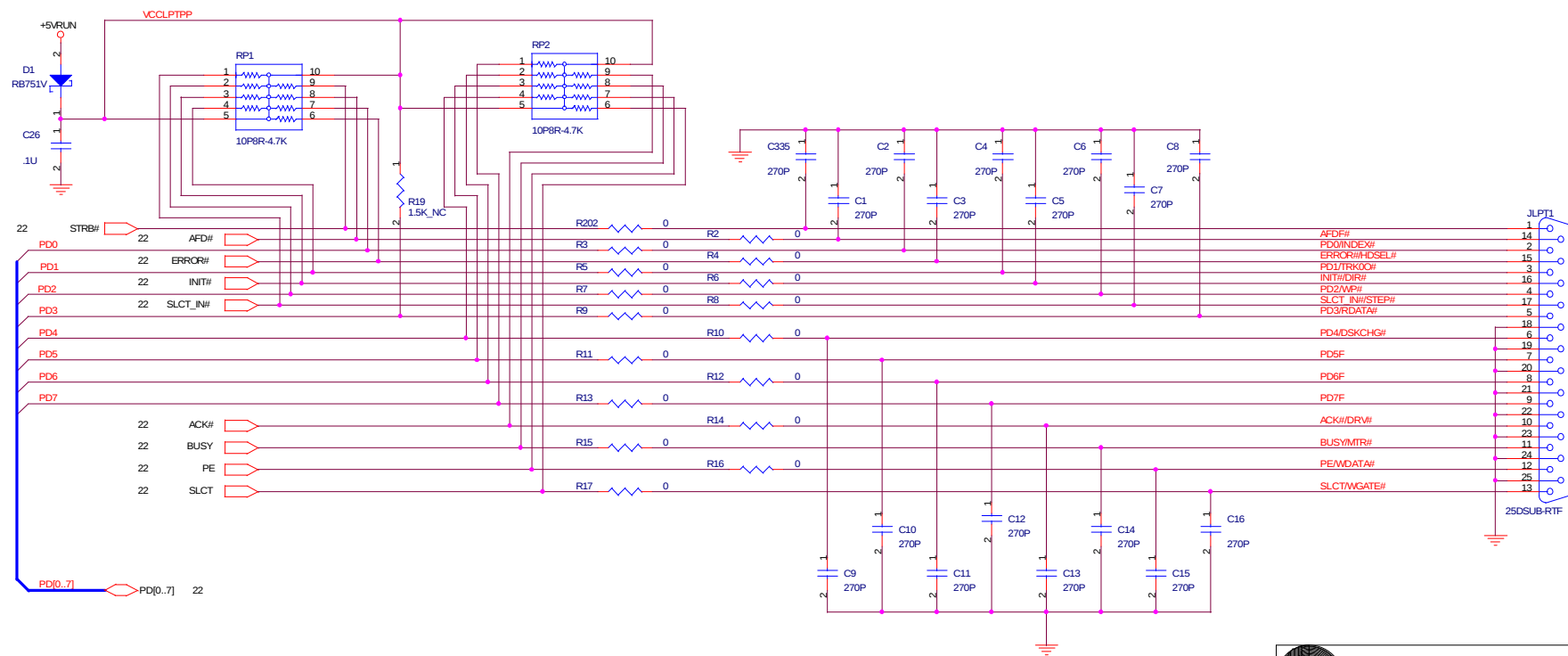




If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out

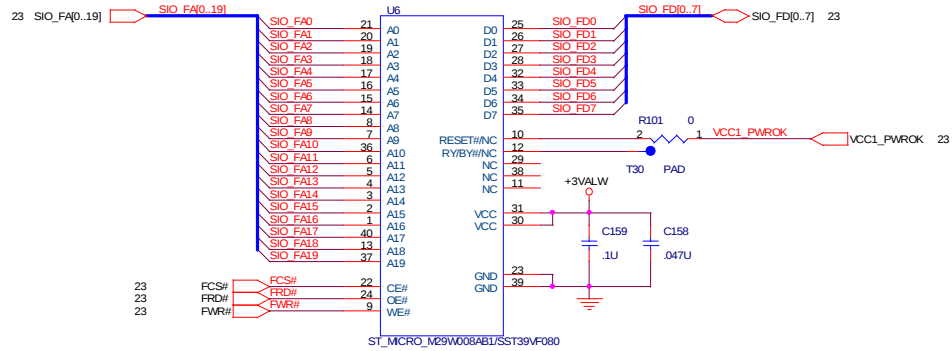


Place these beads to JCOM1 as close as possible



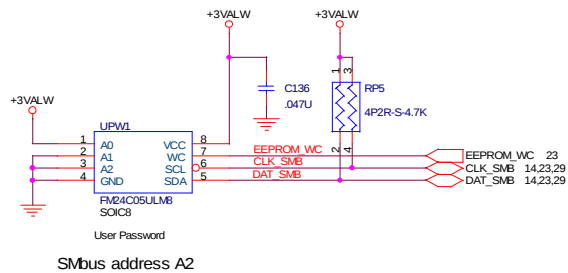
Title			PARALLEL CONN.
Size	Document Number	Rev	
	DMT	1A	
Date:	Friday, July 18, 2003	Sheet	25 of 46

8Mbit (1MByte),NO PLCC TYPE



SST :Pin10,12 are NC

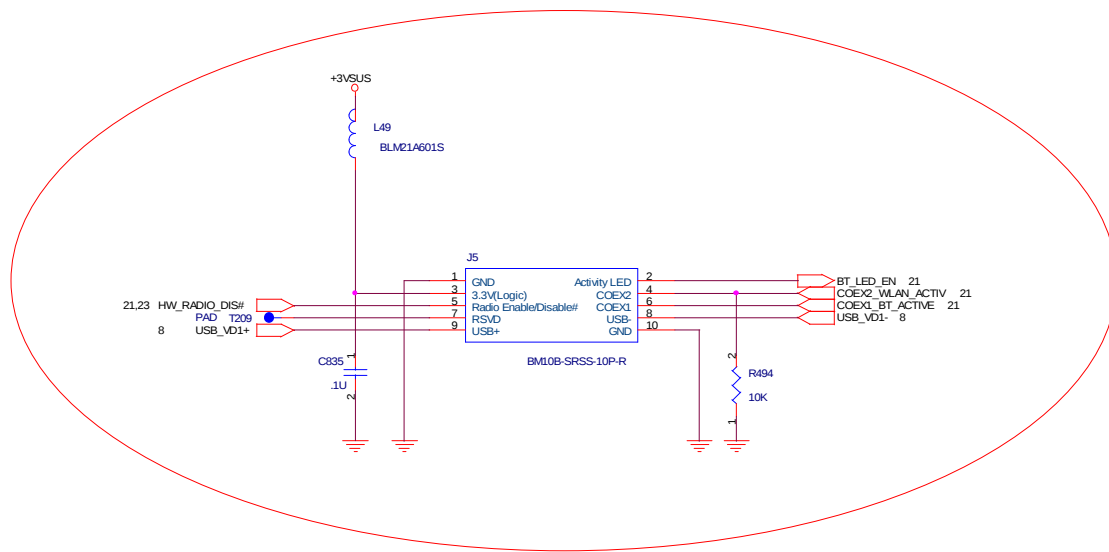
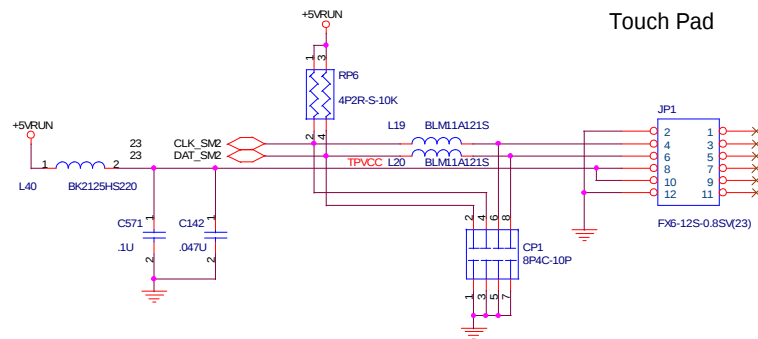
- 1.MAX6326 UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK



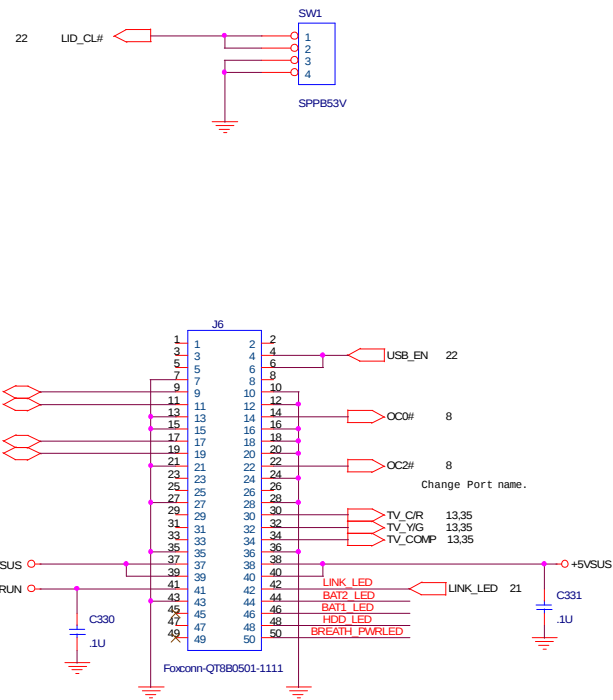
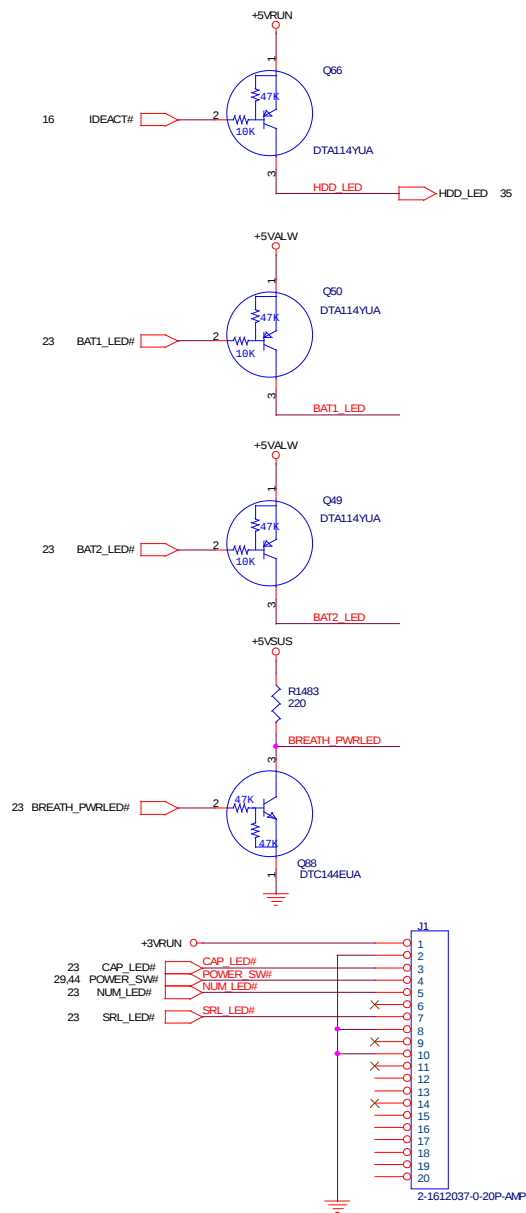
SMbus address A2



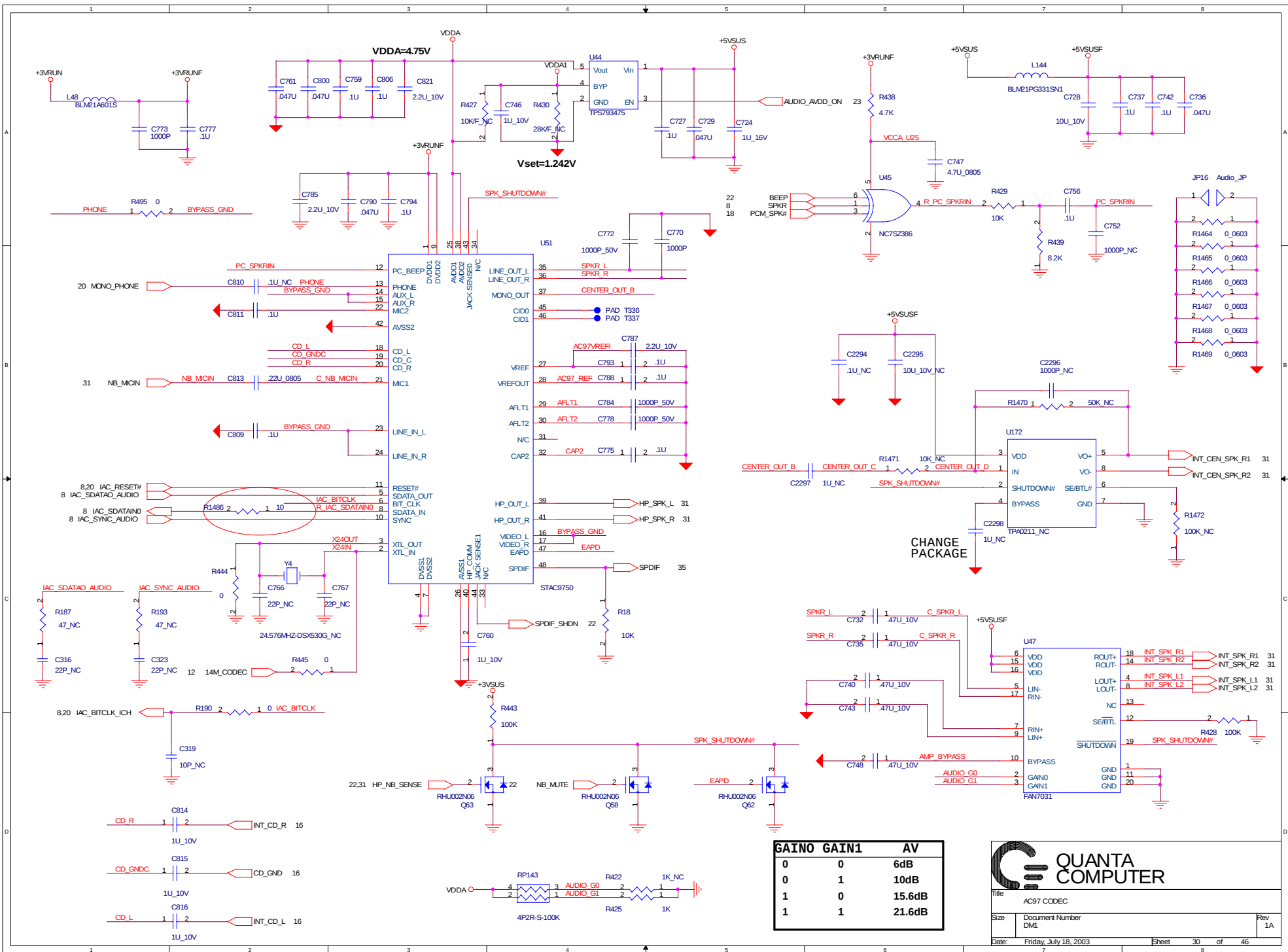
Title FLASH		
Size	Document Number DMT	Rev 1A
Date:	Friday, July 18, 2003	Sheet 26 of 46

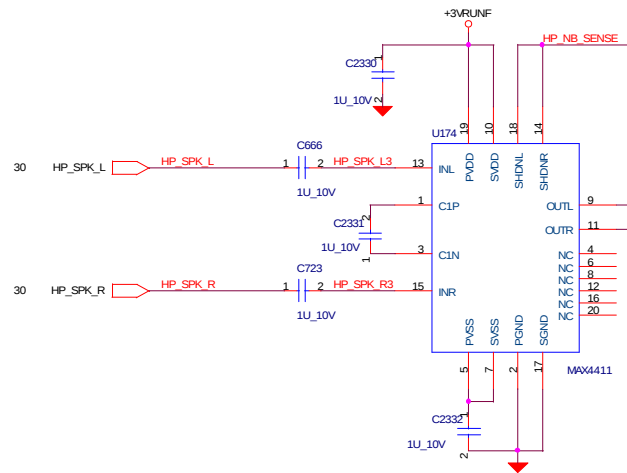
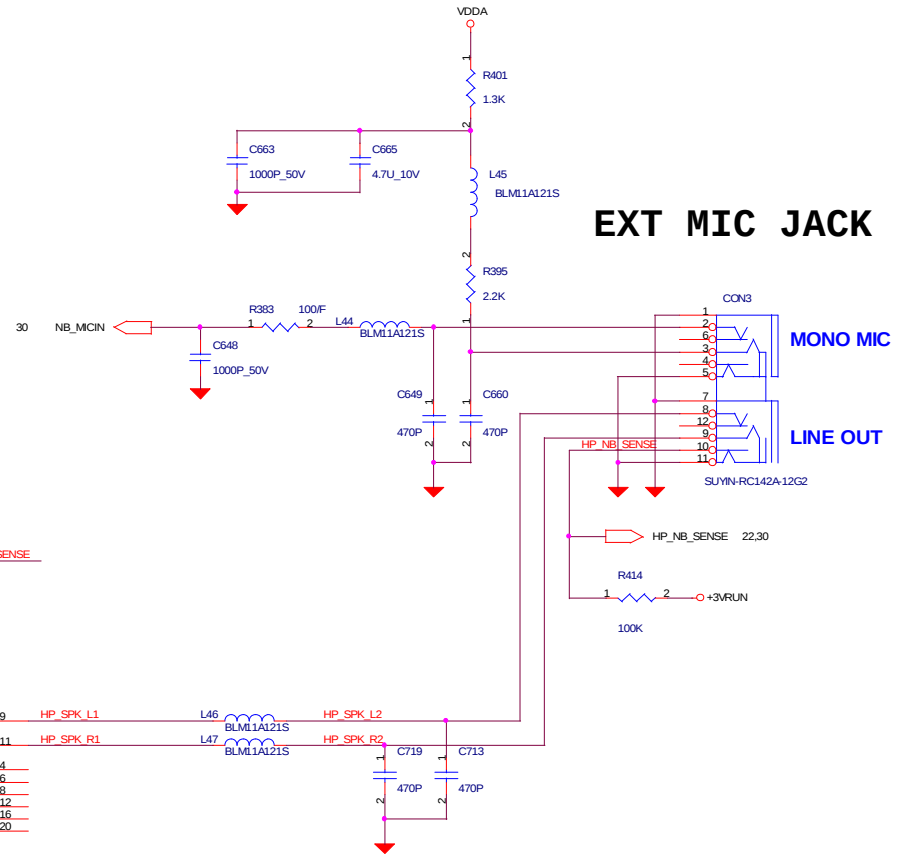
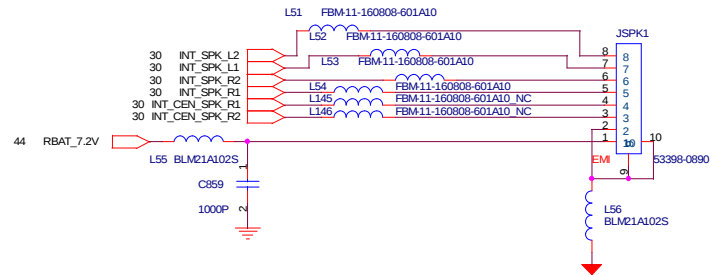


Title			TOUCH PAD & BULE TOOTH
Size	Document Number	Rev	
	DM1	1A	
Date:	Friday, July 18, 2003	Sheet	27 of 46

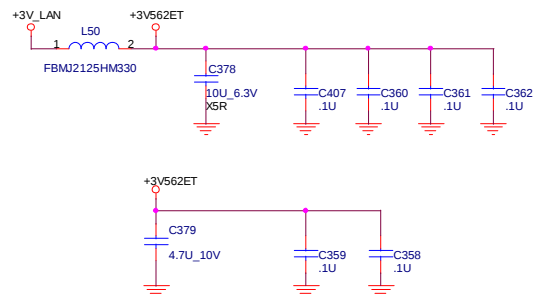
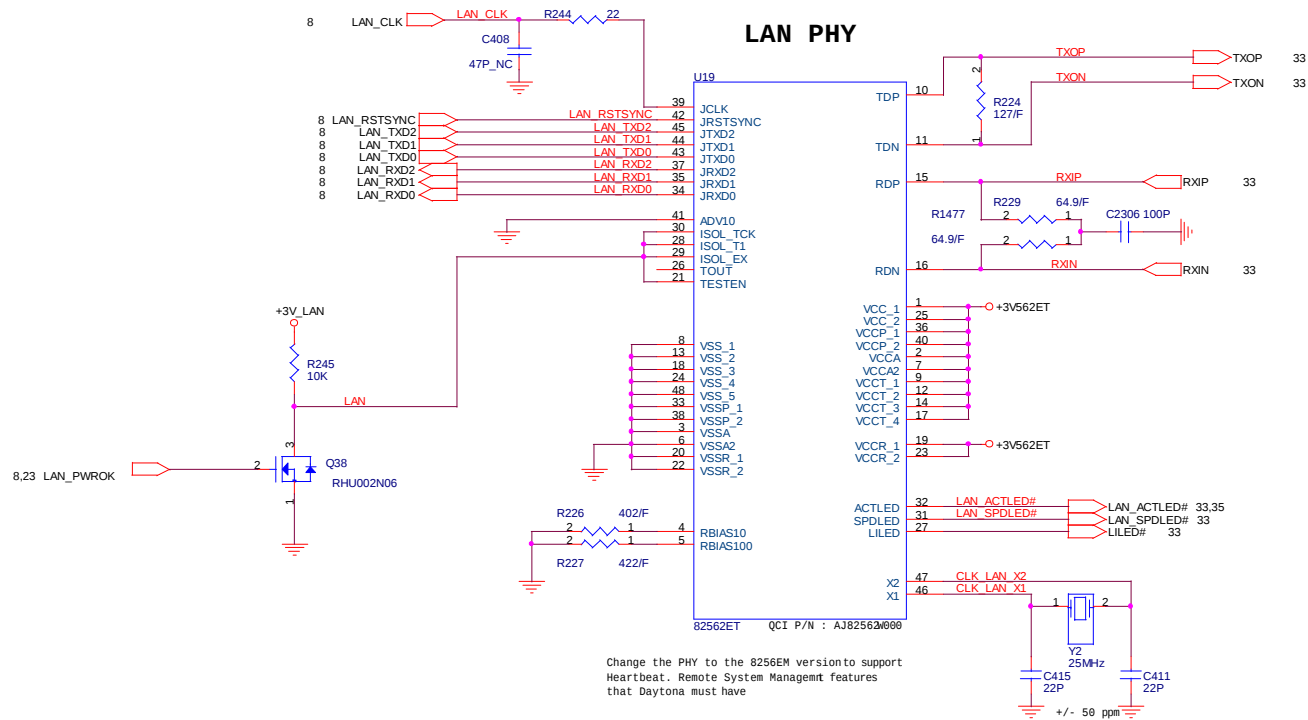


Title			SWITCH & LED
Size	Document Number	Rev	
	DMT	1A	
Date:	Friday, July 18, 2003	Sheet	28 of 46



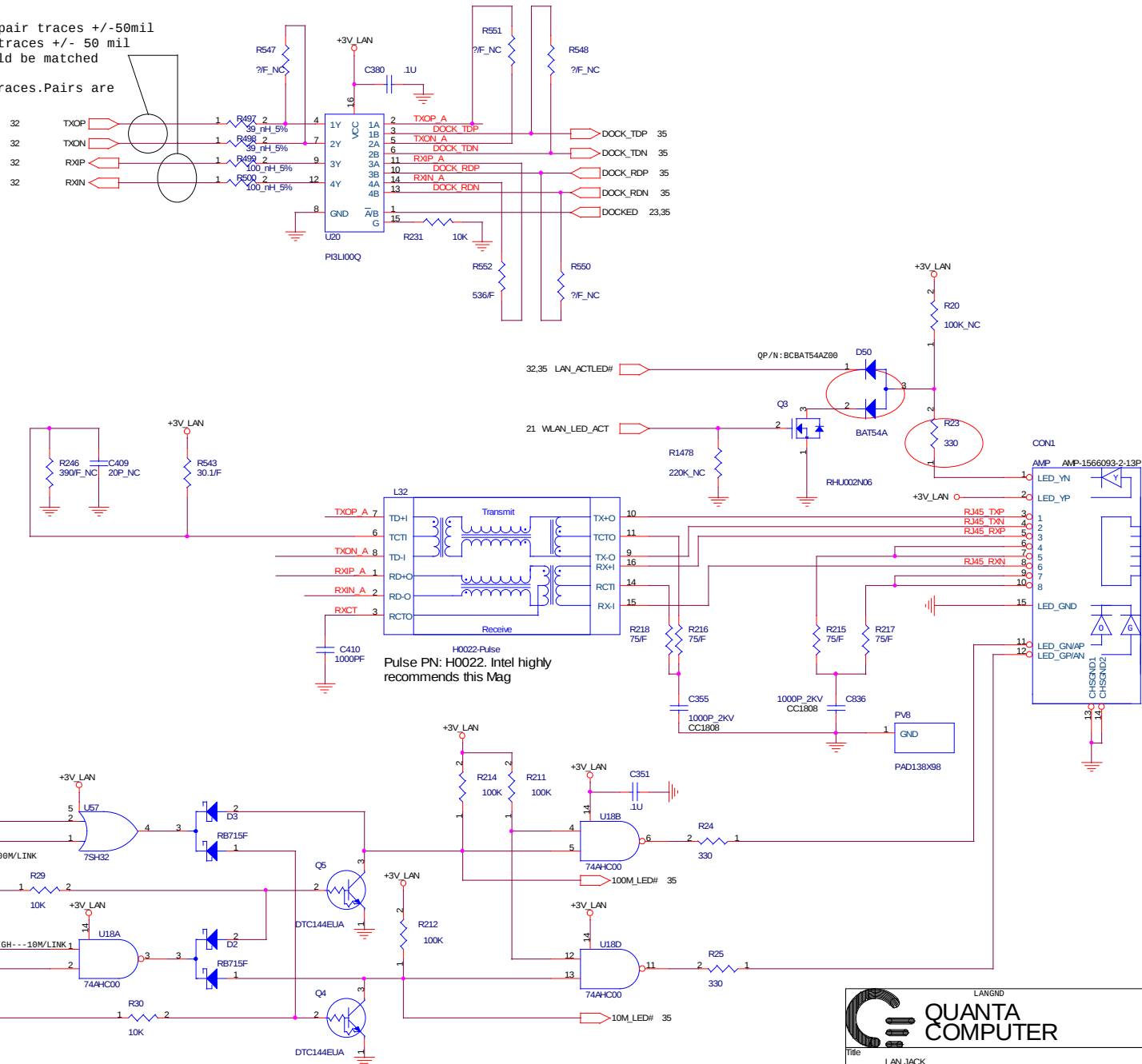


Title			AUDIO CONN
Size	Document Number	Rev	
	DMT	1A	
Date:	Friday, July 18, 2003	Sheet	31 of 46

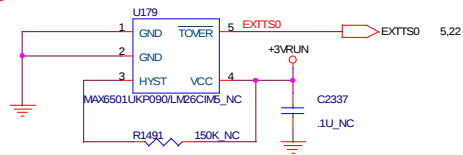
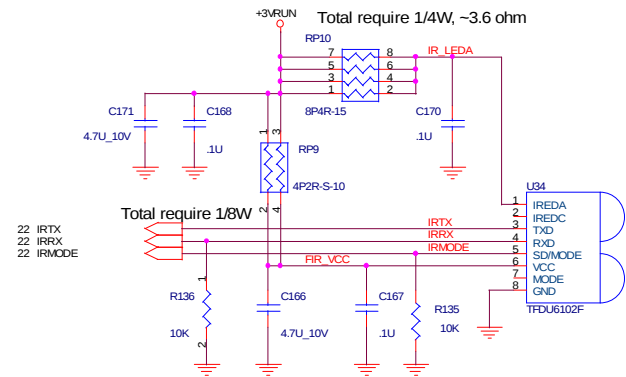


Title			LAN INTERFACE
Size	Document Number	Rev	
Custom	DM1	1A	
Date:	Friday, July 18, 2003	Sheet	32 of 46

LAYOUT NOTES:
Match total length of chip side Rx and Tx pair traces +/-50mil
Match length of cable side Rx and Tx pair traces +/- 50 mil
Total line TX+ to TX- and RX- and RX+ should be matched within 50 mils.
Keep 50mil space between pairs and other traces.Pairs are 100ohm differential,



LAN_SPDLED#	SPEED
HI	10M
LO	100M

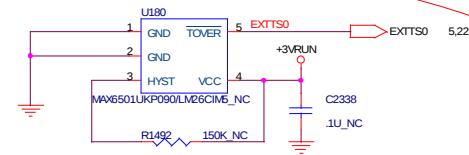


U136=LM26

	GND	VCC
HYST	10 degree	2 degree

U136=MAX6501

	GND	VCC
HYST	2 degree	10 degree



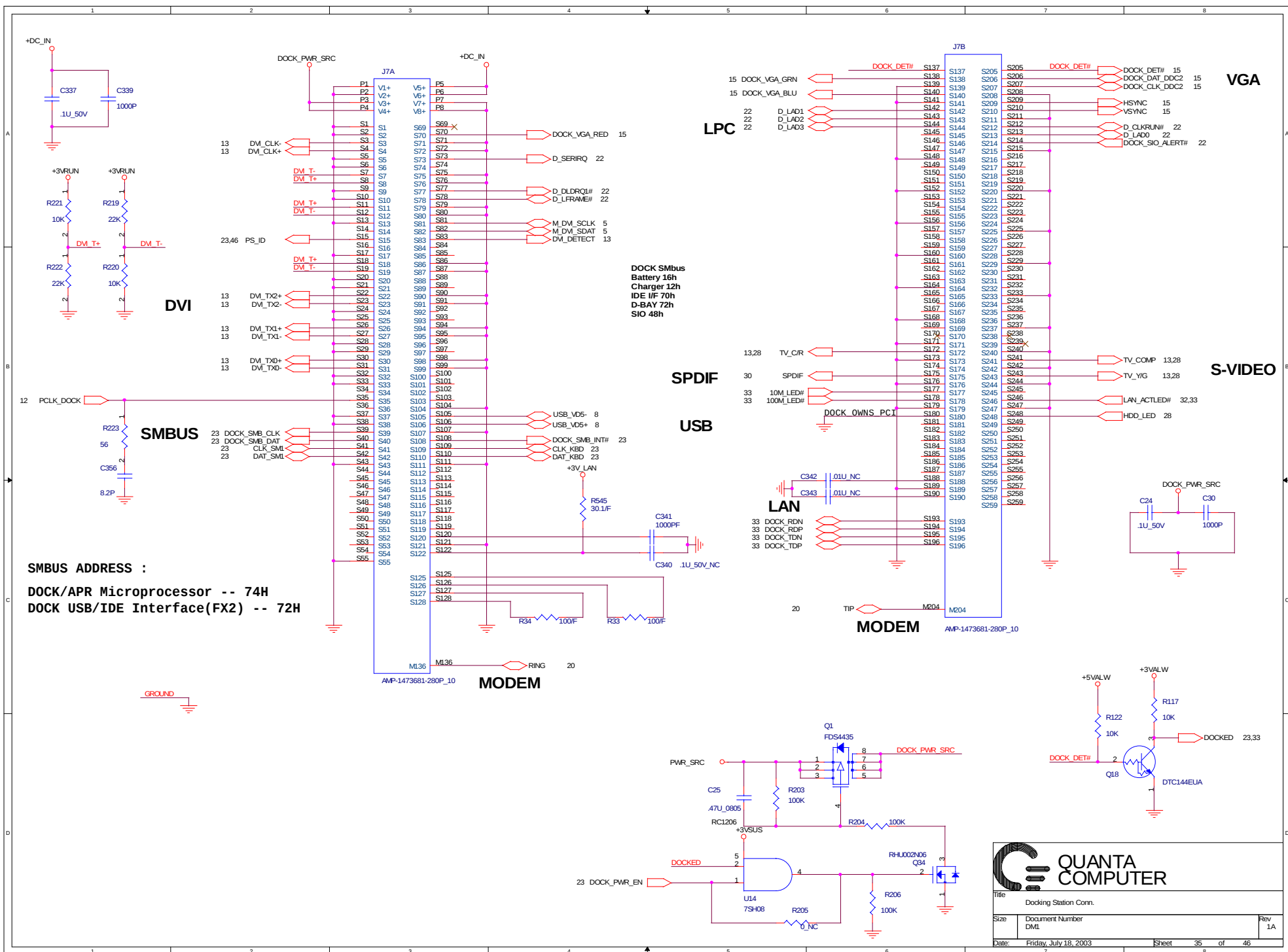
U136=LM26

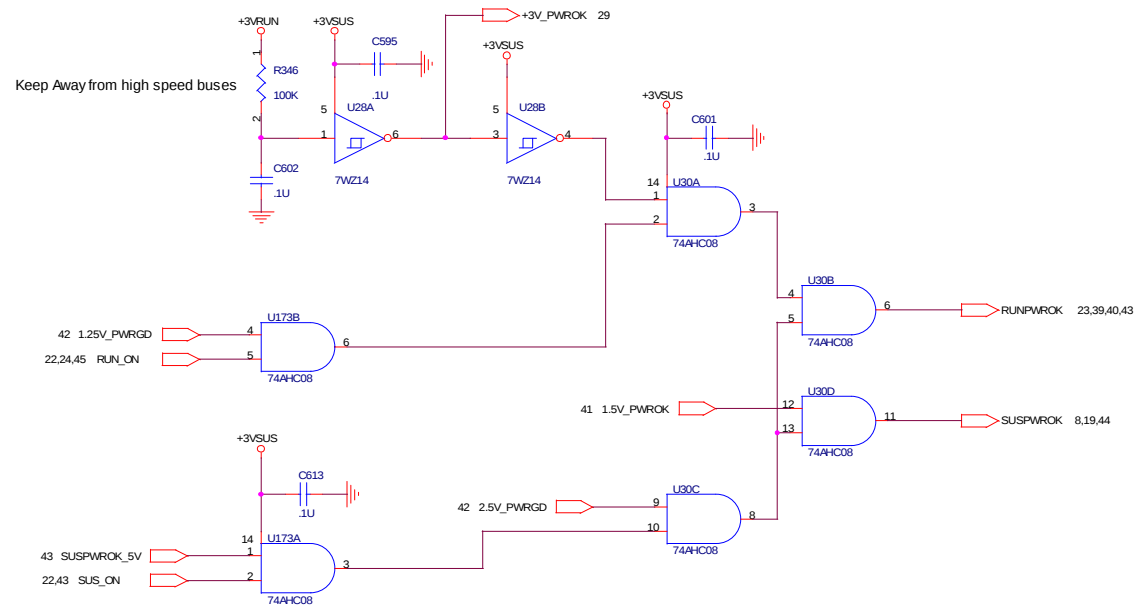
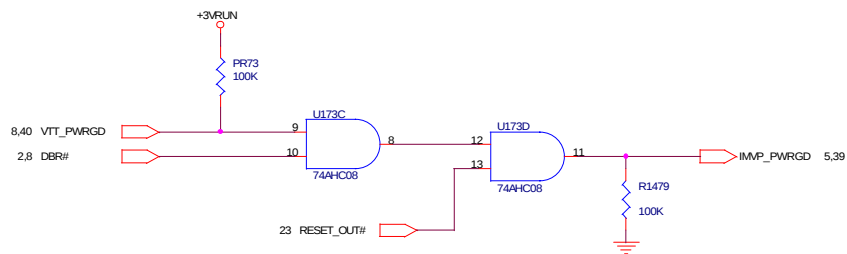
	GND	VCC
HYST	10 degree	2 degree

U136=MAX6501

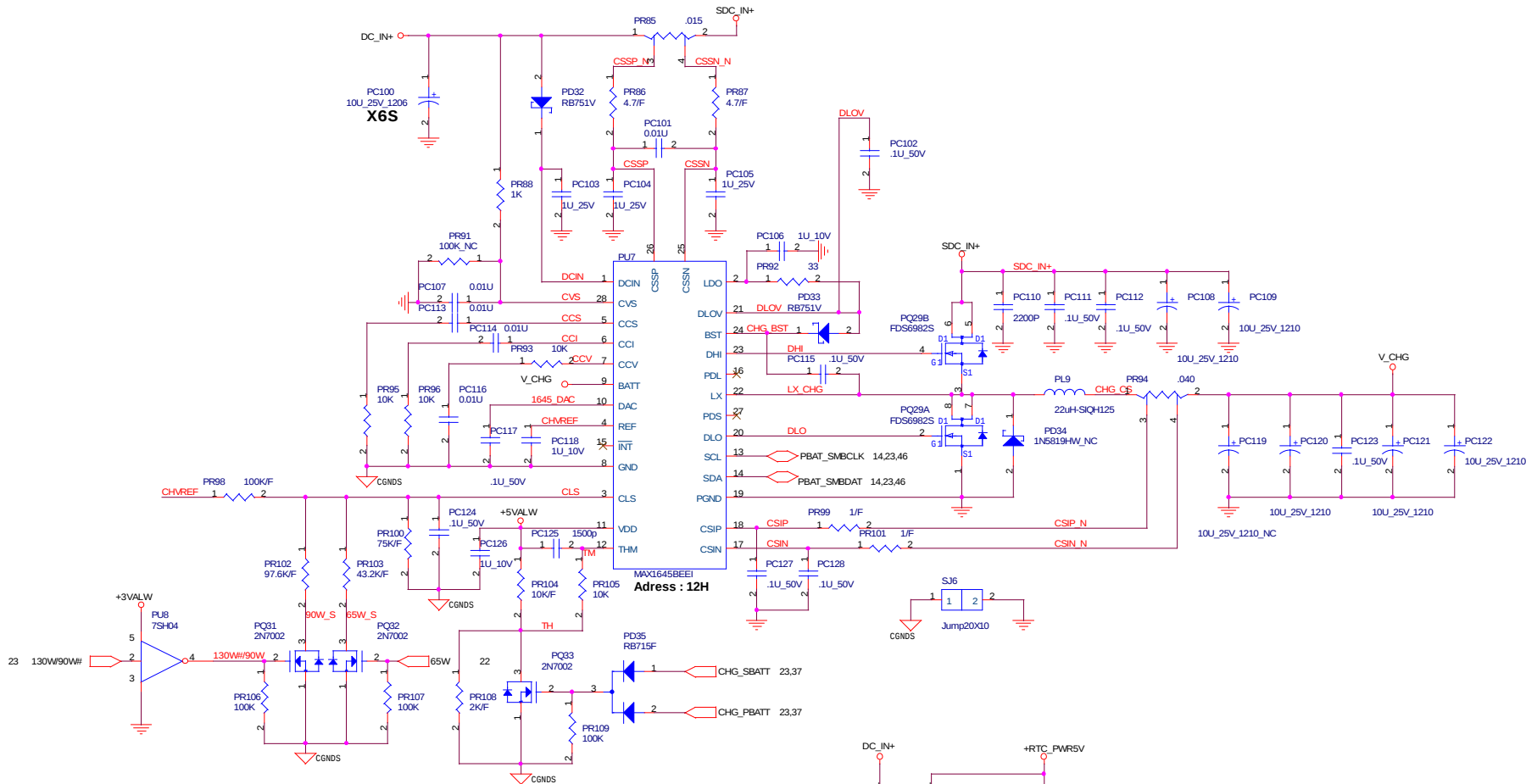
	GND	VCC
HYST	2 degree	10 degree





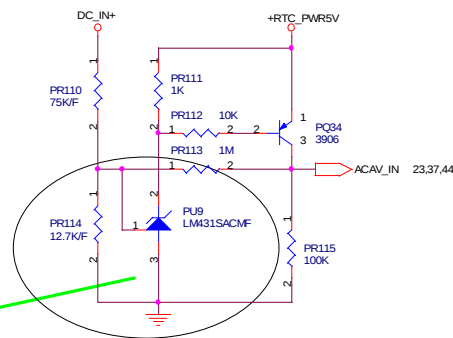


Title			POWER GOOD
Size	Document Number	Rev	
	DMT	1A	
Date:	Friday, July 18, 2003	Sheet	36 of 46



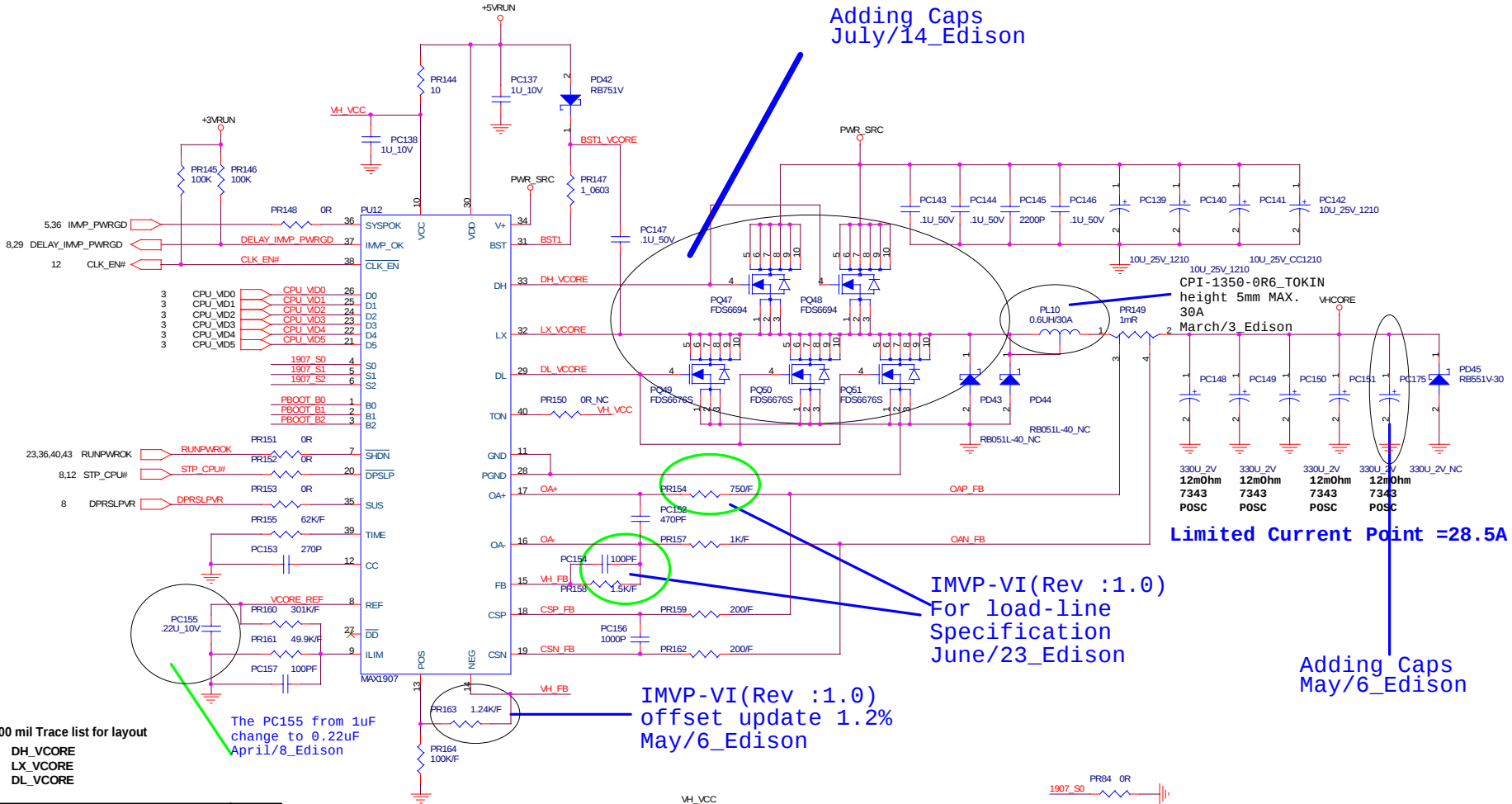
	65W (2.93A)	90W (4.2A)	130W (5.8A)
65W	H	L	L
130W/90W#	H	L	H

The library of PU9
will modify
April/8_Edison



QUANTA
COMPUTER

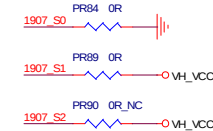
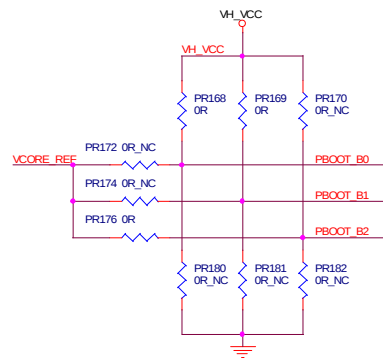
Adding Caps
July/14_Edison



100 mil Trace list for layout
DH_VCORE
LX_VCORE
DL_VCORE

The PC155 from 1uF
change to 0.22uF
April/8_Edison

V I D							Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V	
0	0	1	1	1	1	1	1.468
0	1	0	1	1	1	1	1.340
0	1	1	0	0	0	0	1.324
0	1	1	0	1	0	0	1.292
0	1	1	1	0	0	0	1.260
0	1	1	1	0	1	1	1.244
0	1	1	1	1	1	1	1.212
1	0	0	0	0	1	1	1.180
1	0	0	0	1	1	1	1.148
1	0	0	1	1	0	0	1.100
1	0	1	0	0	1	1	1.052
1	0	1	0	1	1	1	1.020
1	0	1	1	1	0	0	0.972
1	1	0	0	0	0	0	0.940



QUANTA
COMPUTER

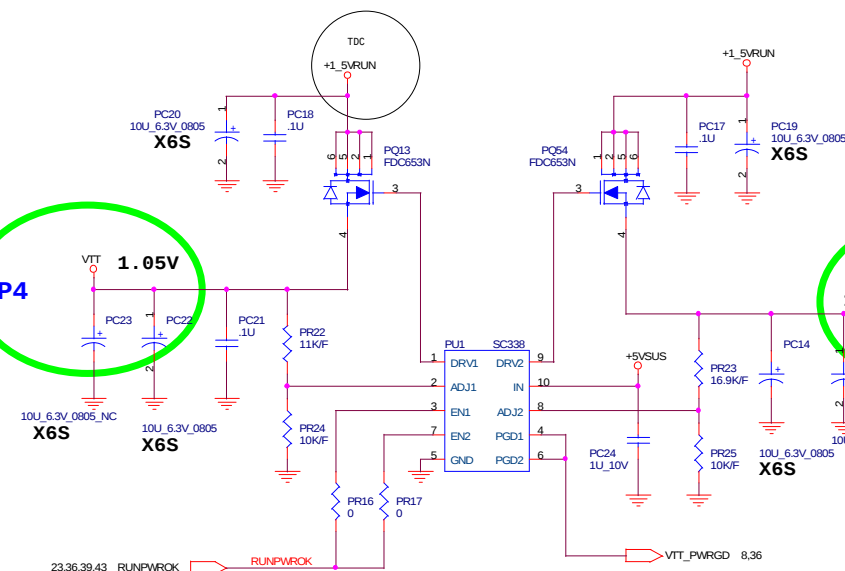
Title CPU POWER

Size Document Number DMI

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Rev 1A

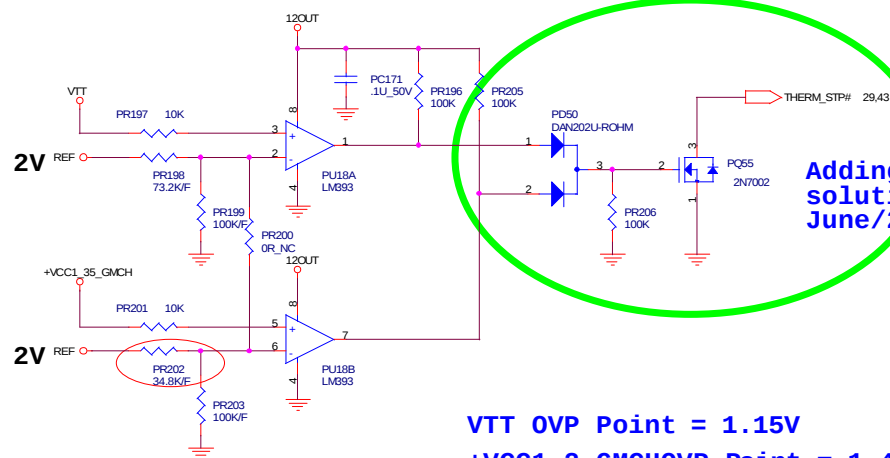
Remove JP2 and JP4
June/23 Edison



Remove JP3 and JP5
June/23 Edison

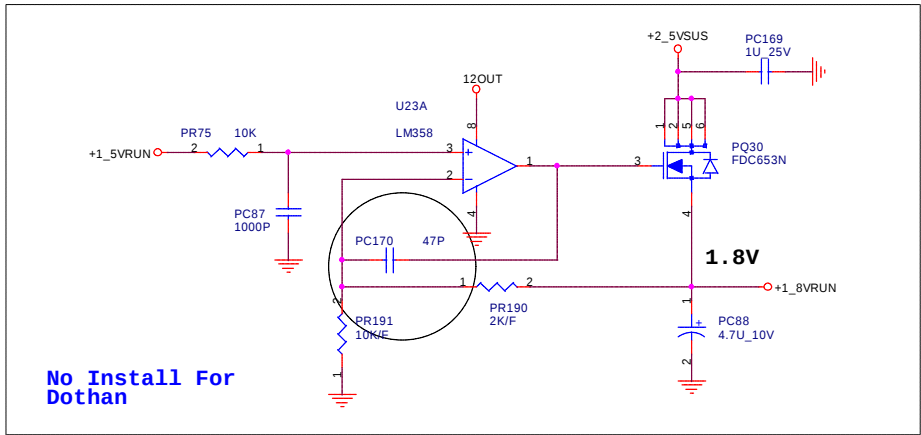
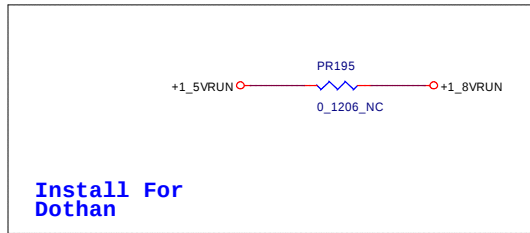
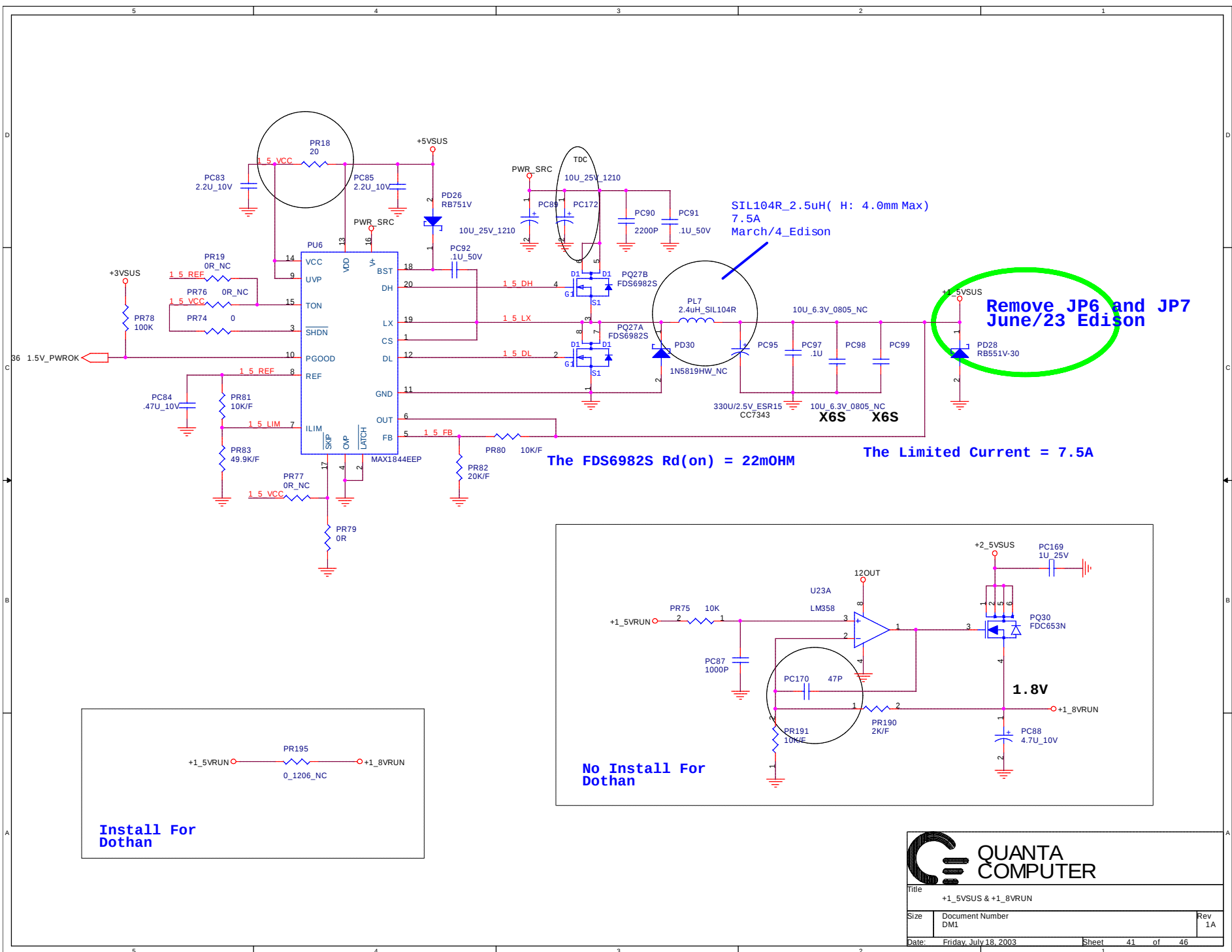
VTT Current Limite 3.2A

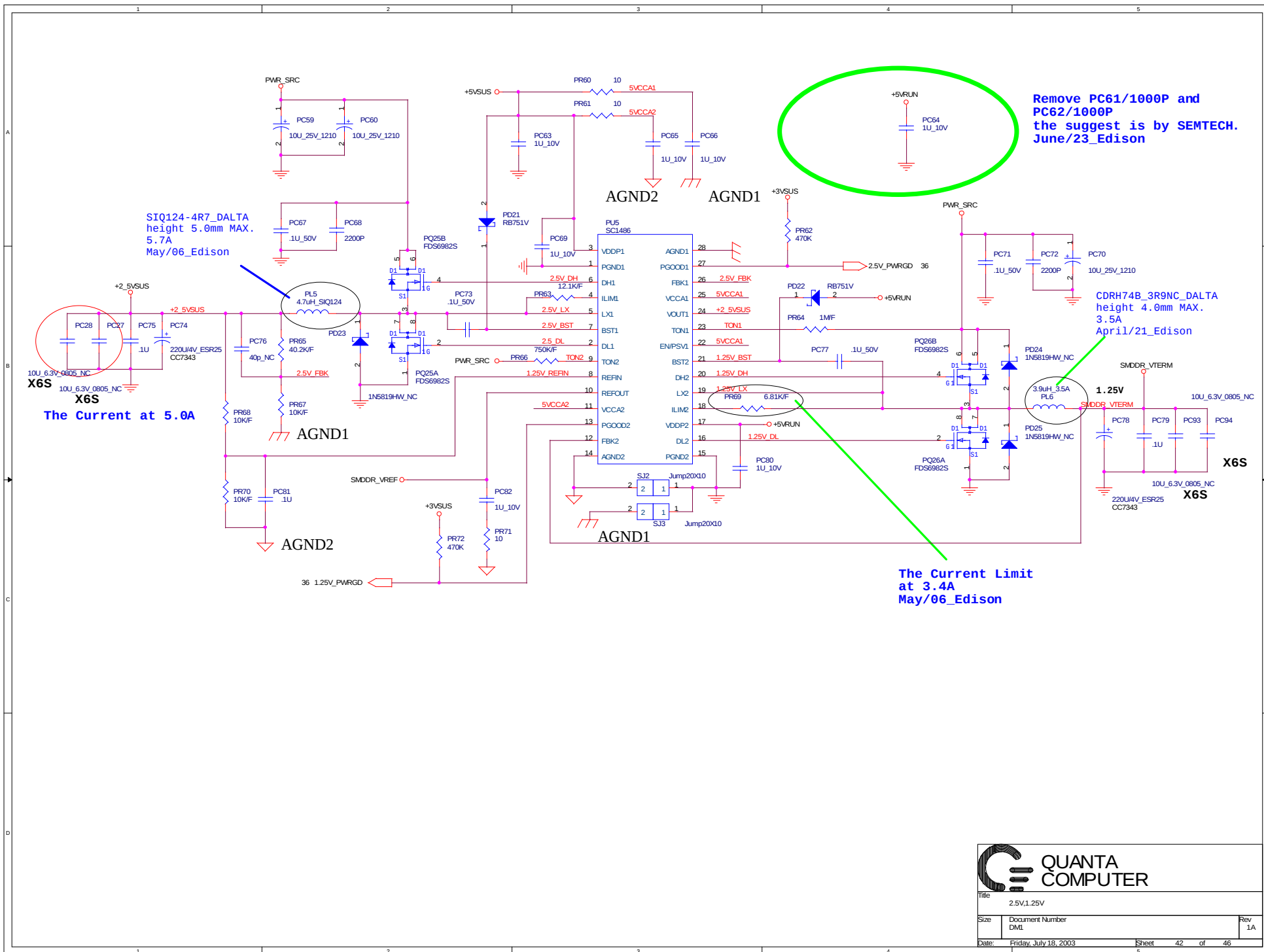
1.20V - GM PR23=14.0K/F
1.35V - GM+ PR23=16.9K/F
+VCC1_2_GMCH Current Limite 3.2A



Adding The OVP
solution
June/23 Edison

VTT OVP Point = 1.15V
+VCC1_2_GMCHOVP Point = 1.48V





Remove JP12 and JP14
June/23 Edison

Current limit at 4A for +3.3V

Place these CAPs close to FETs
SIL104R_100NC_DELTA
height 4.0mm MAX.
4.4A
April/8_Edison

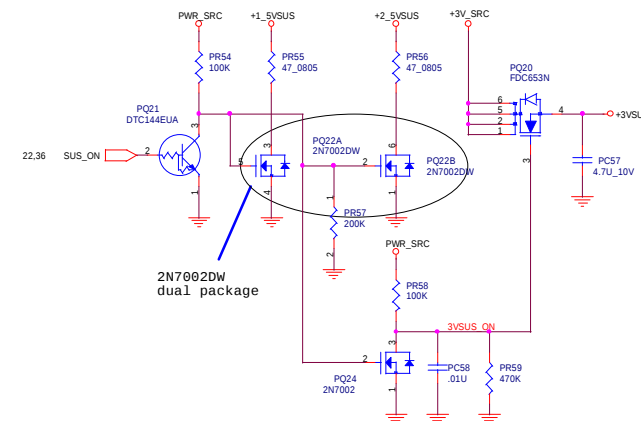
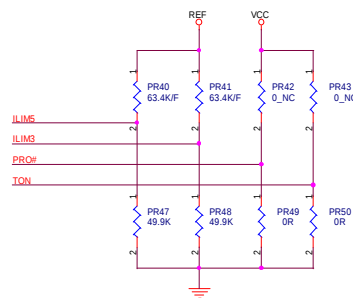
Place these CAPs close to FETs

Current limit at 4A for +5VSUS

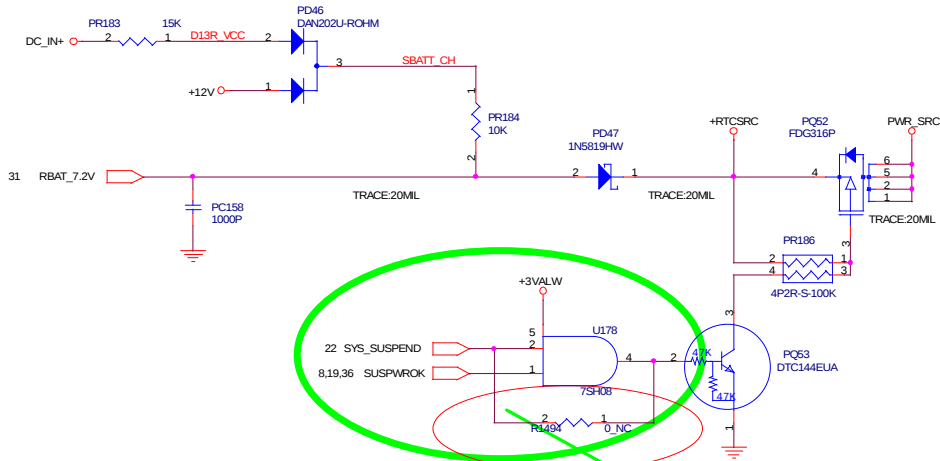
Remove JP13 and JP15
June/23 Edison

From CC1206 change to CC0805
April/8_Edison

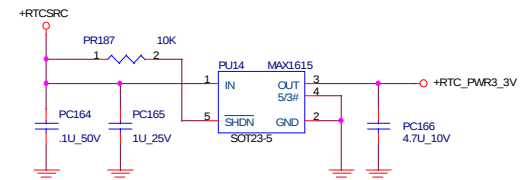
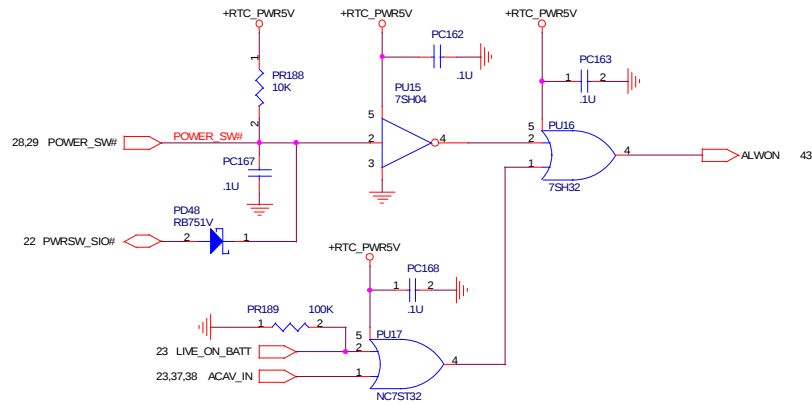
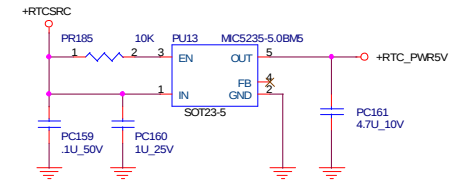
STQ125-1022A
height 6mm MAX.
4.3A
March/3_Edison



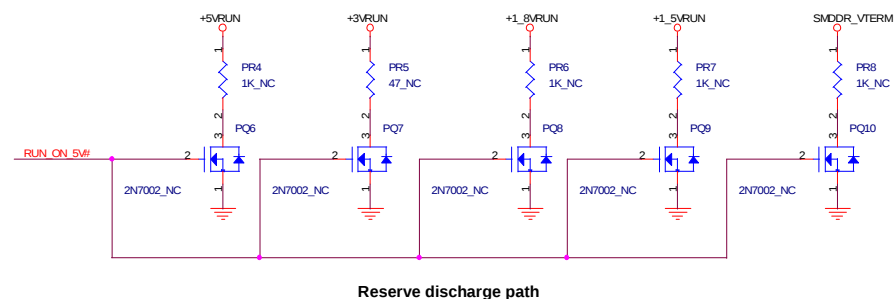
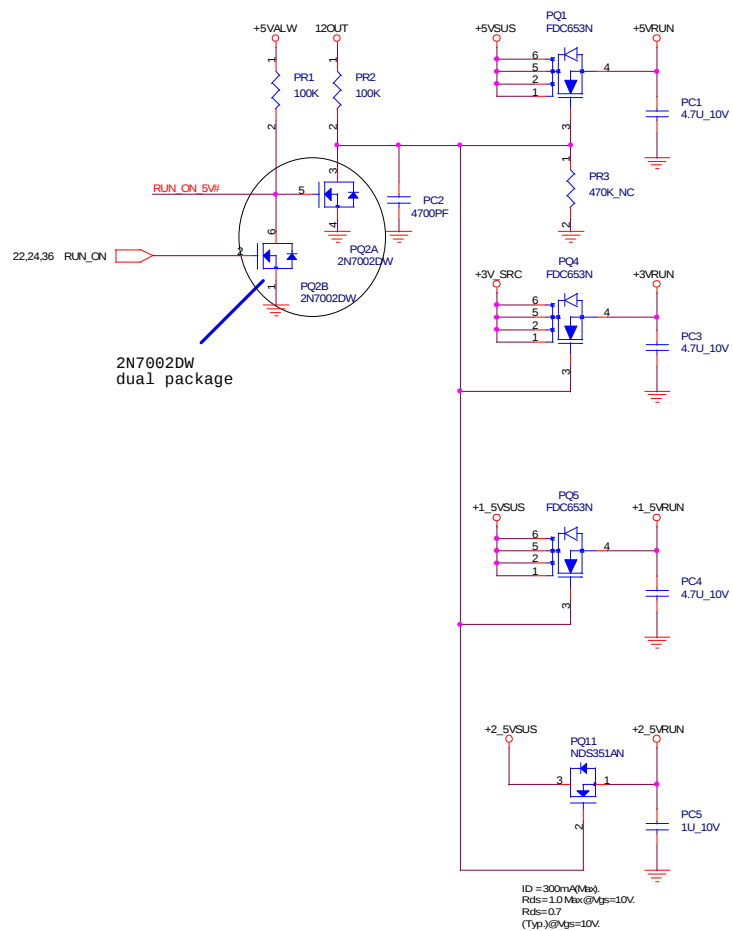
Title				
+3VSRC & +3VSUS & +5VSUS				
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Adding RBATT protection
Edison_July/08/2003



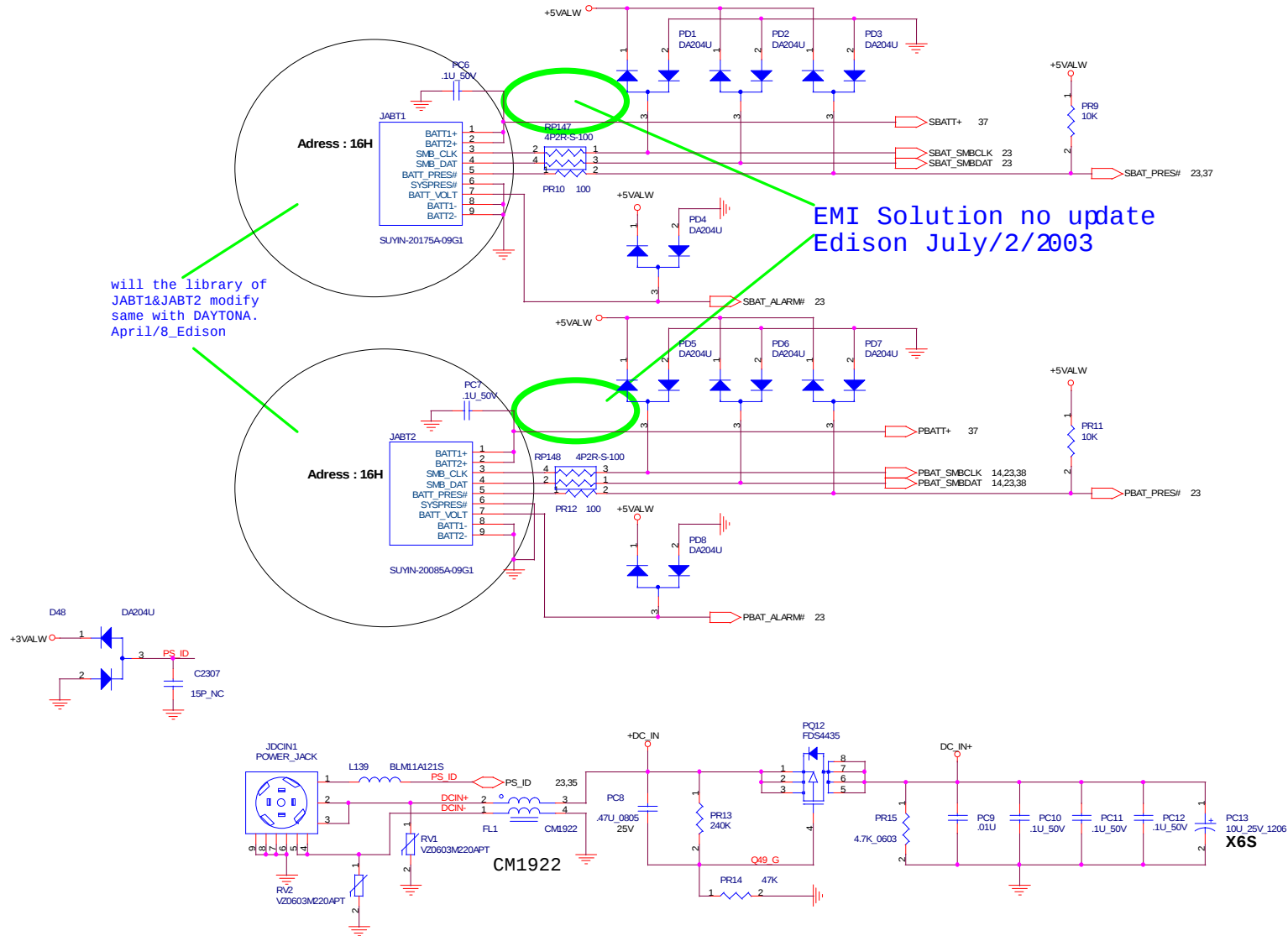
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Size	Document Number	Rev	
	DM1	1A	
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Title			RUN POWER SW	
Size	Document Number	Rev		
	DMT	1A		
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will the library of
JABT1&JABT2 modify
same with DAYTONA.
April/8_Edison

EMI Solution no update
Edison July/2/2003



Title			DCIN.BATT CONNECTOR
Size	Document Number	Rev	
	DMT	1A	
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