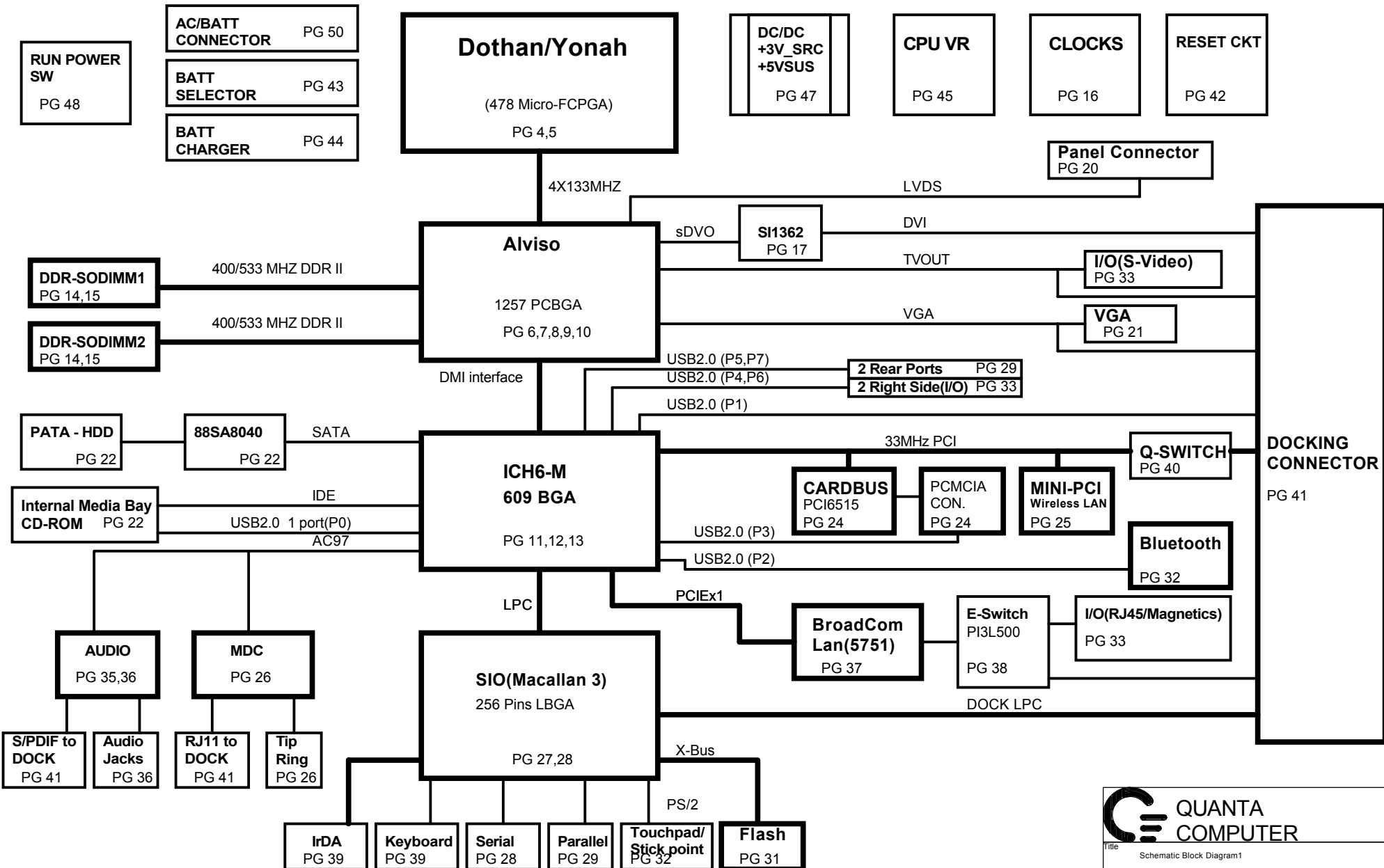


AZEDA-INTEGRATED

PWA: K3885, SCHEM: J3964
VER : 3A



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Pg#	Description	DNI LIST
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2	Blank Page	
3	Front Page	
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6-10	Alviso	
11-13	ICH6	
14-15	DDRII SO-DIMM(200P)	
16	Clock Generator	
17	CH7306/7	
18-19	Blank Pages	
20	LCD Conn. & SSP	
21	CRT & TV Conn.	
22	SATA & IDE Conn.	
23	Screw Hole	
24	TI PIC6515	
25	Mini PCI Conn.	
26	MDC Conn.	
27-28	SIO (LPC47N354)	
29	SERIAL PORT & USB	
30	PARALLEL CONN.	
31	Flash ROM	
32	TOUCH PAD & BLUE TOOTH	
33	Switch Board Conn. & LED	
34	FAN & Thermal	
35-36	Audio CODEC (STAC9751) & Phone Jack	
37-38	LOM (BCM5751), Switch	
39	FIR	
40-41	Docking Conn. & Q-Switch	
42	Power Good	
43-44	Battery Selector & Charger	
45	CPU Power	
46	1.8V,0.9V,1.5V,1.05V	
47	3VALW/5V/3V/Power ON	
48	RUN Power Switch	
49	VGA DC/DC	
50	DCIN/Batt Conn.	

Power & Ground			
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~20V)	
RTC_PWR3_3V		RTC & PCL POWER (3_3V)	
+12V		+12V	DRUNPWROK
VHORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
V1_2RUN		AGTL+ POWER (1.2V)	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VFAN1, +5VFAN2		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		AGP I/O POWER	
 GND	ALL PAGES	DIGITAL GROUND	
 GNDP		CPU POWER GND	
 CGNDP		CHARGER GND	
 DGNDP		DC/DC POWER GND	
 LANGND		COMBO CONN GND	



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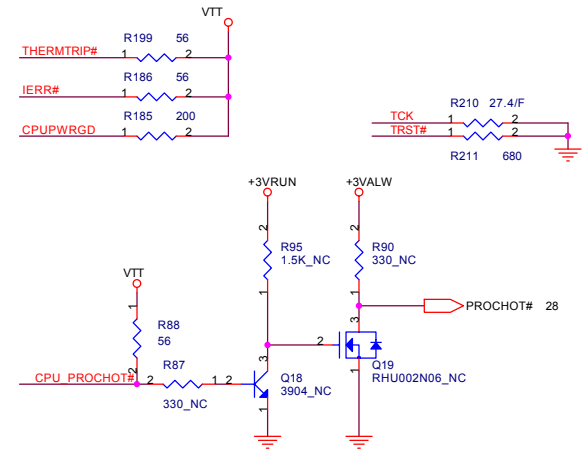
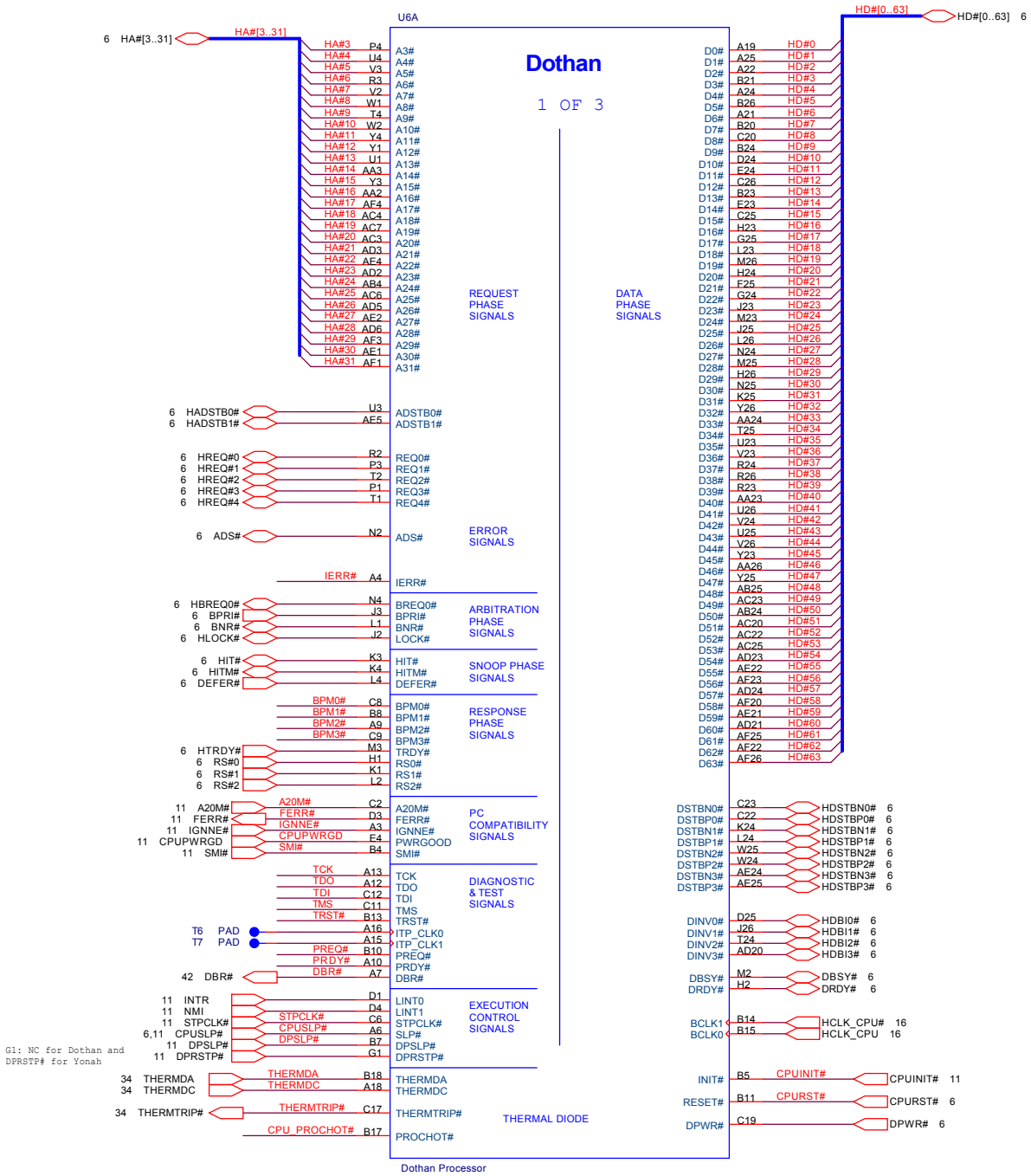
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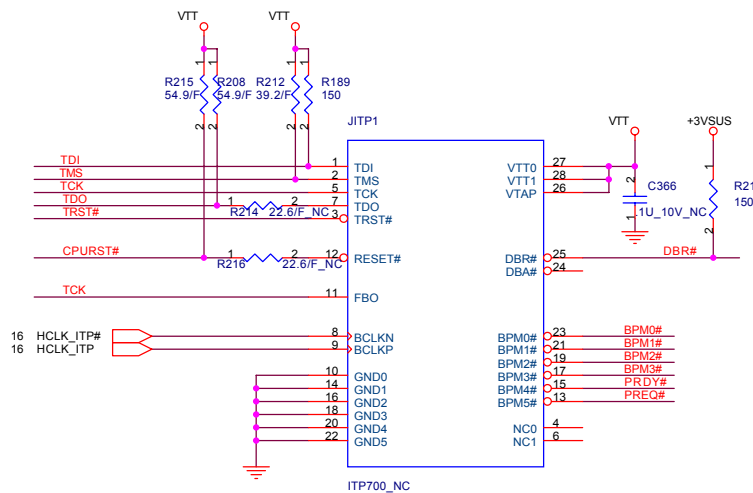
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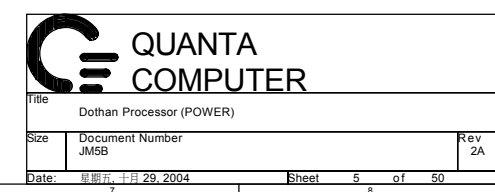
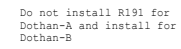
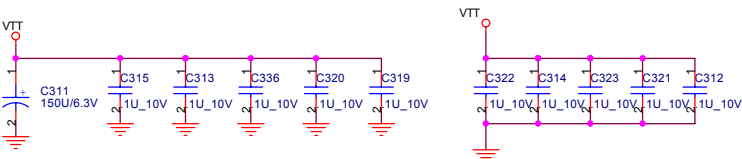
ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	VTT	Within 2.0" of the CPU
ITP_EN	R268 Depop	+3VRUN	Close to CR410M Pin8

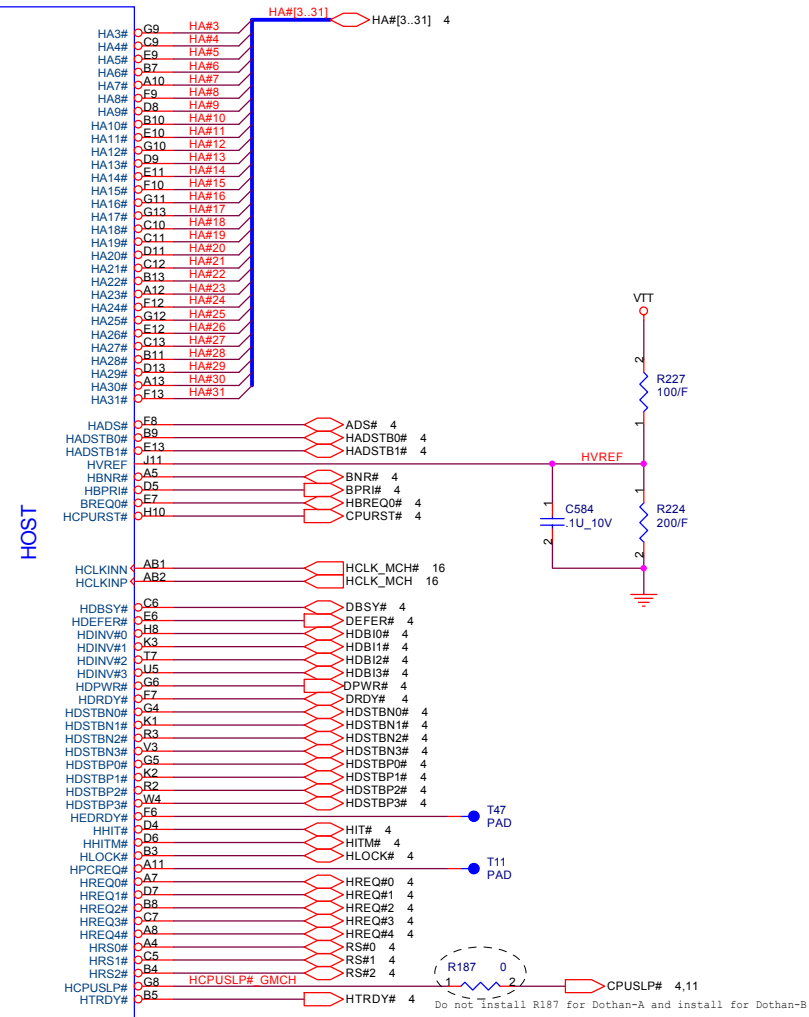
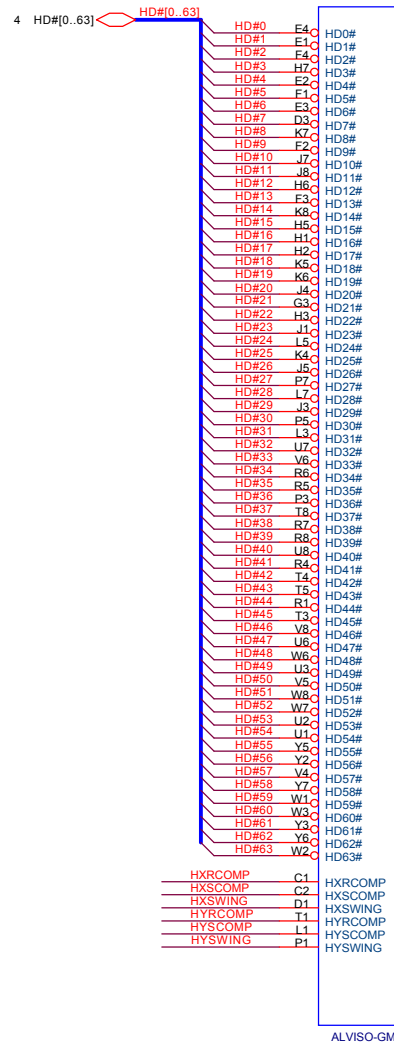
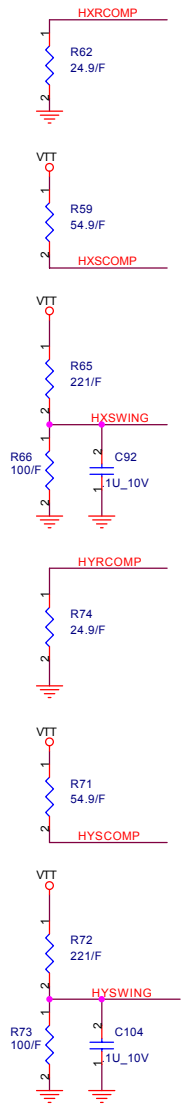
Note: Populate R214, R216, C366, and R268 when ITP connector is populated.



G1: NC for Dothan and DPRSTP# for Yonah

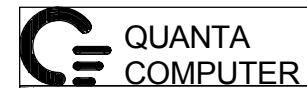
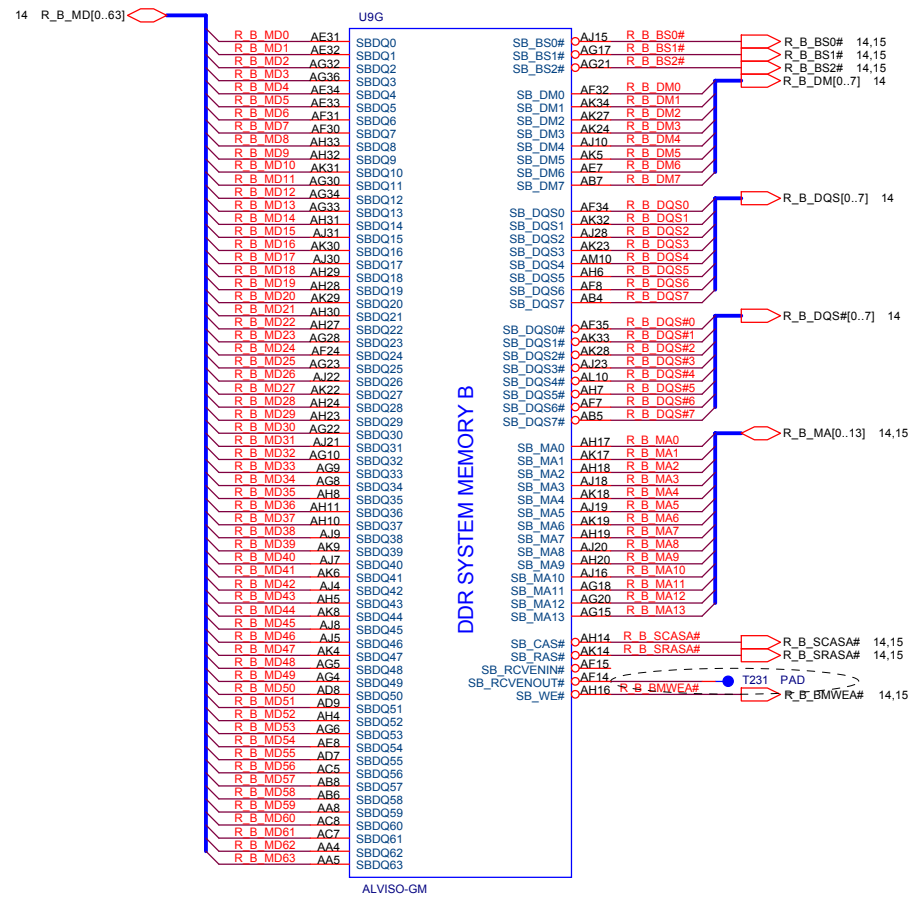
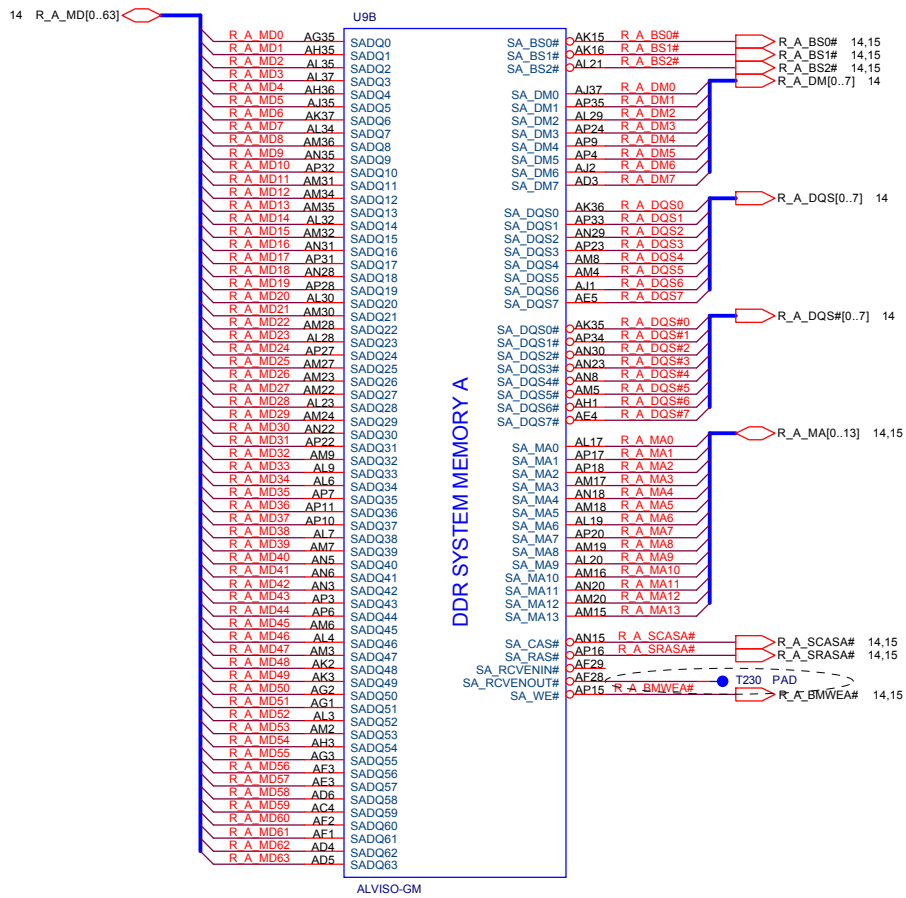


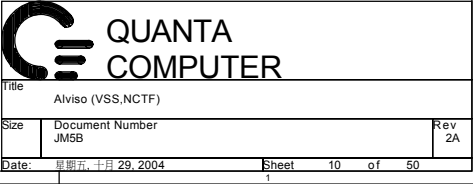


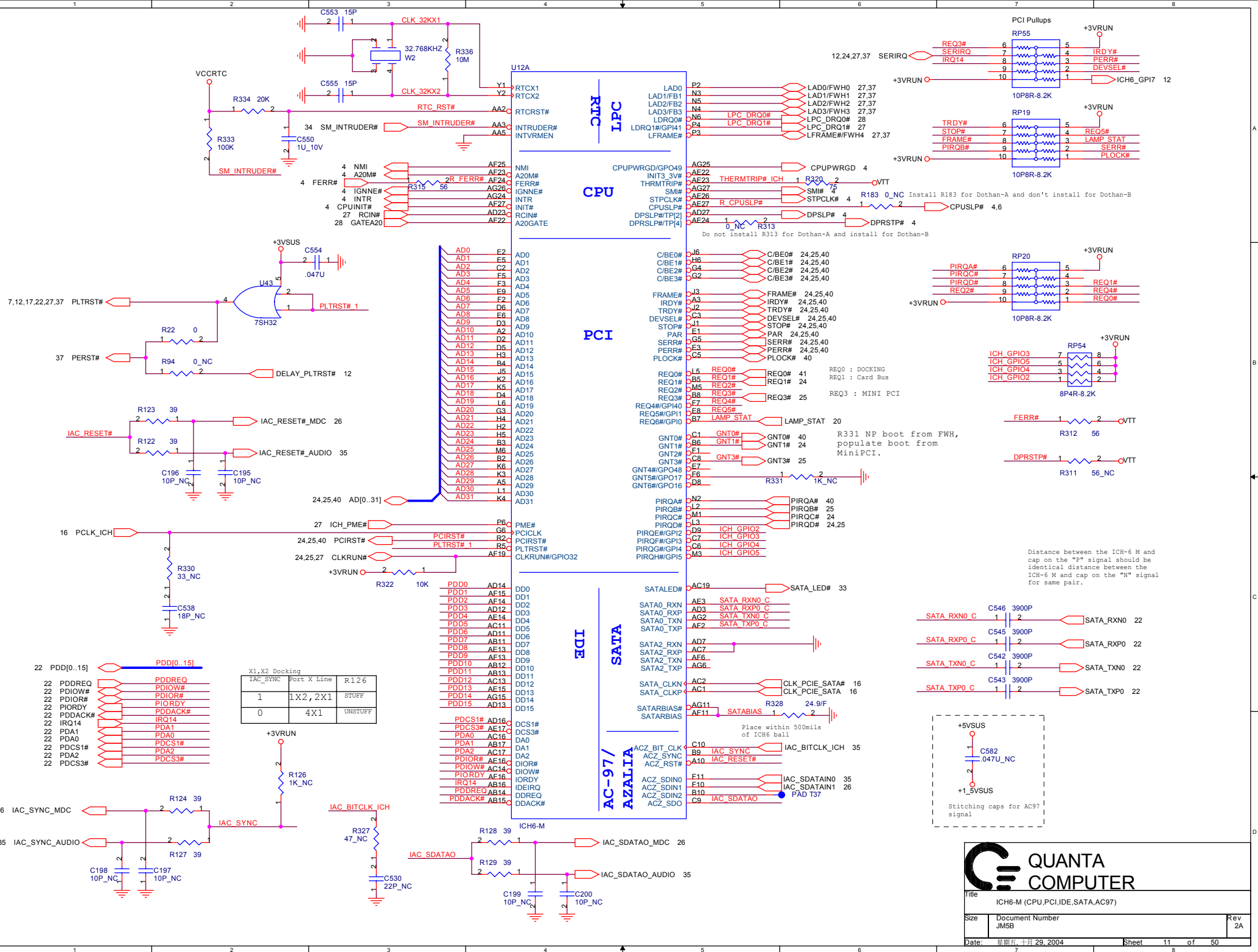


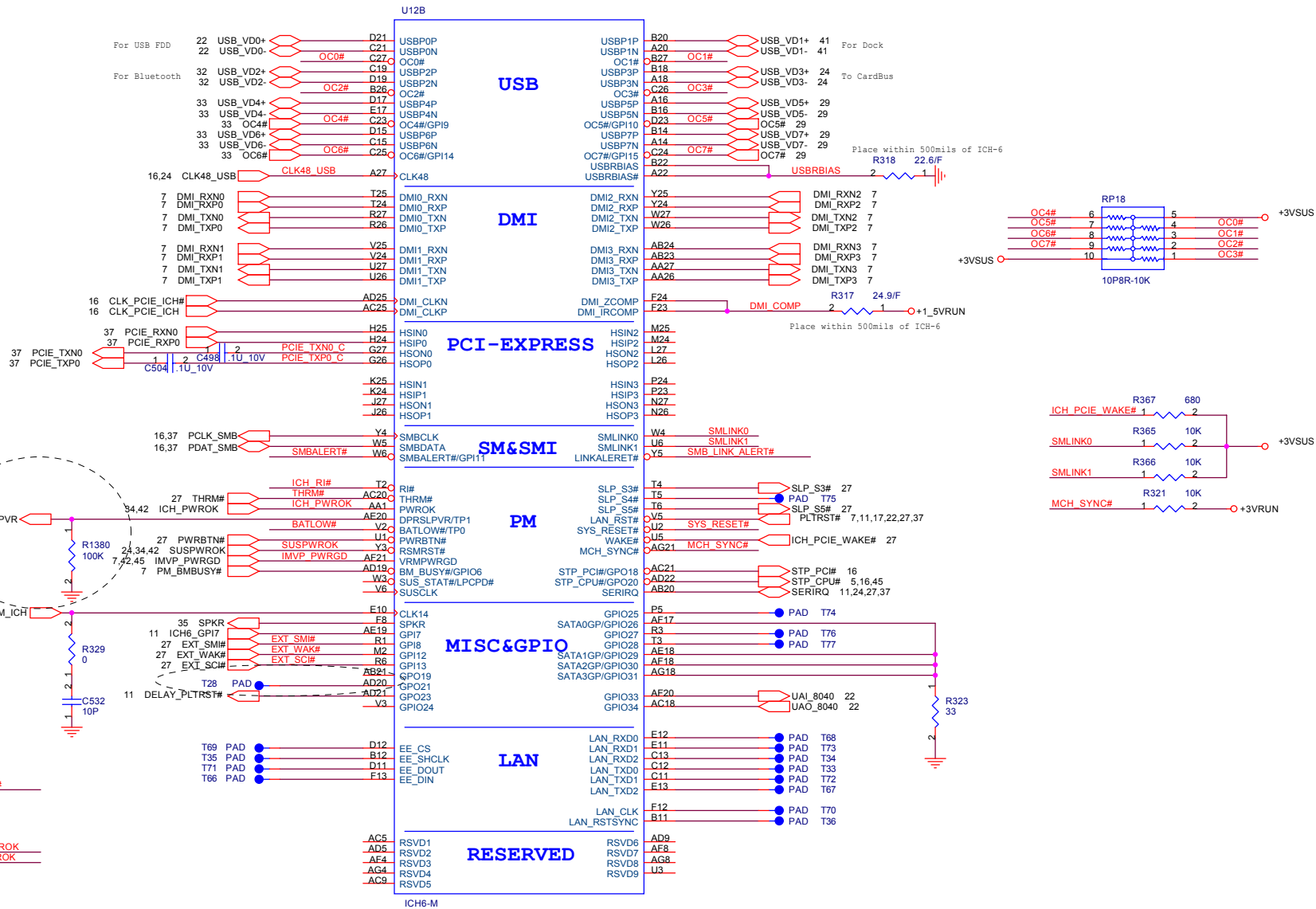


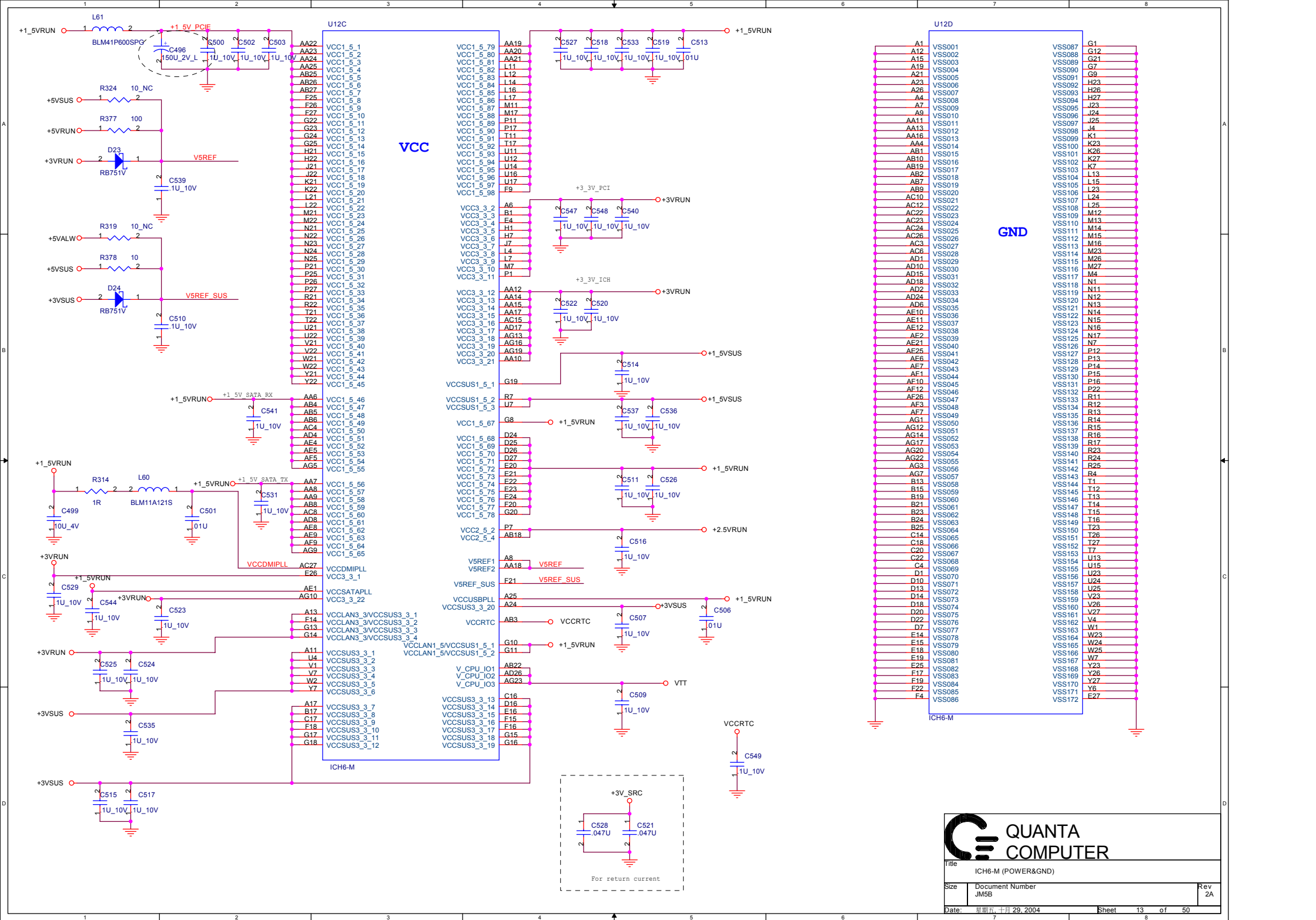
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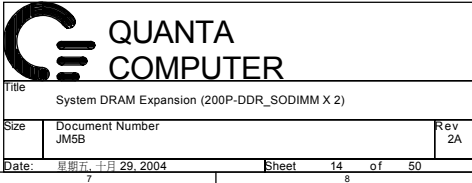






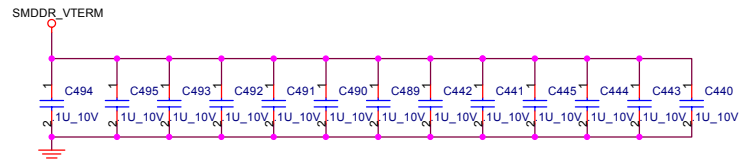




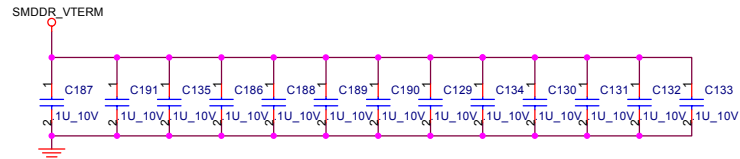


R_A_MA[0..13] 8,14

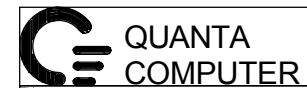
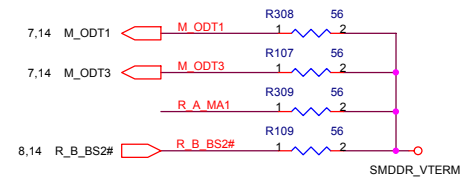
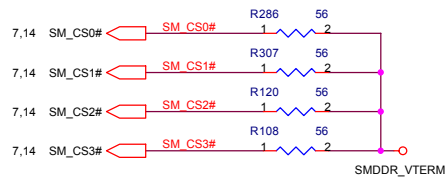
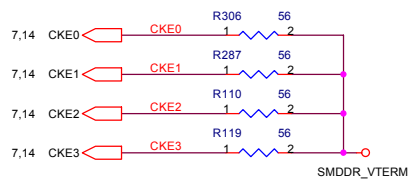
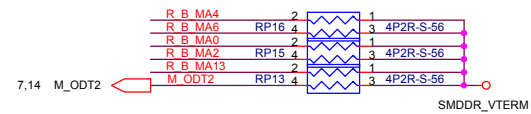
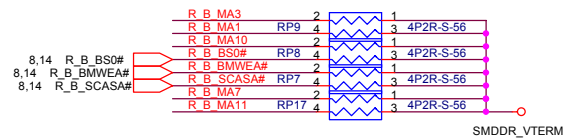
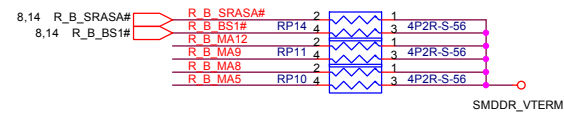
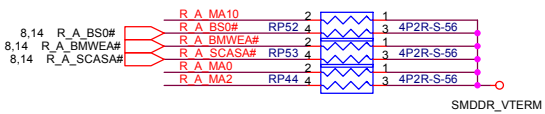
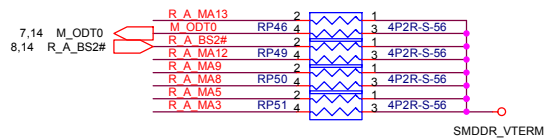
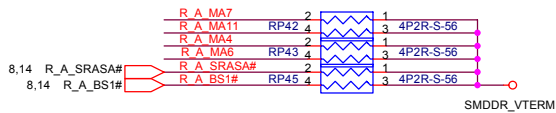
R_B_MA[0..13] 8,14

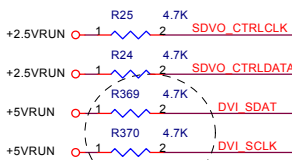


Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

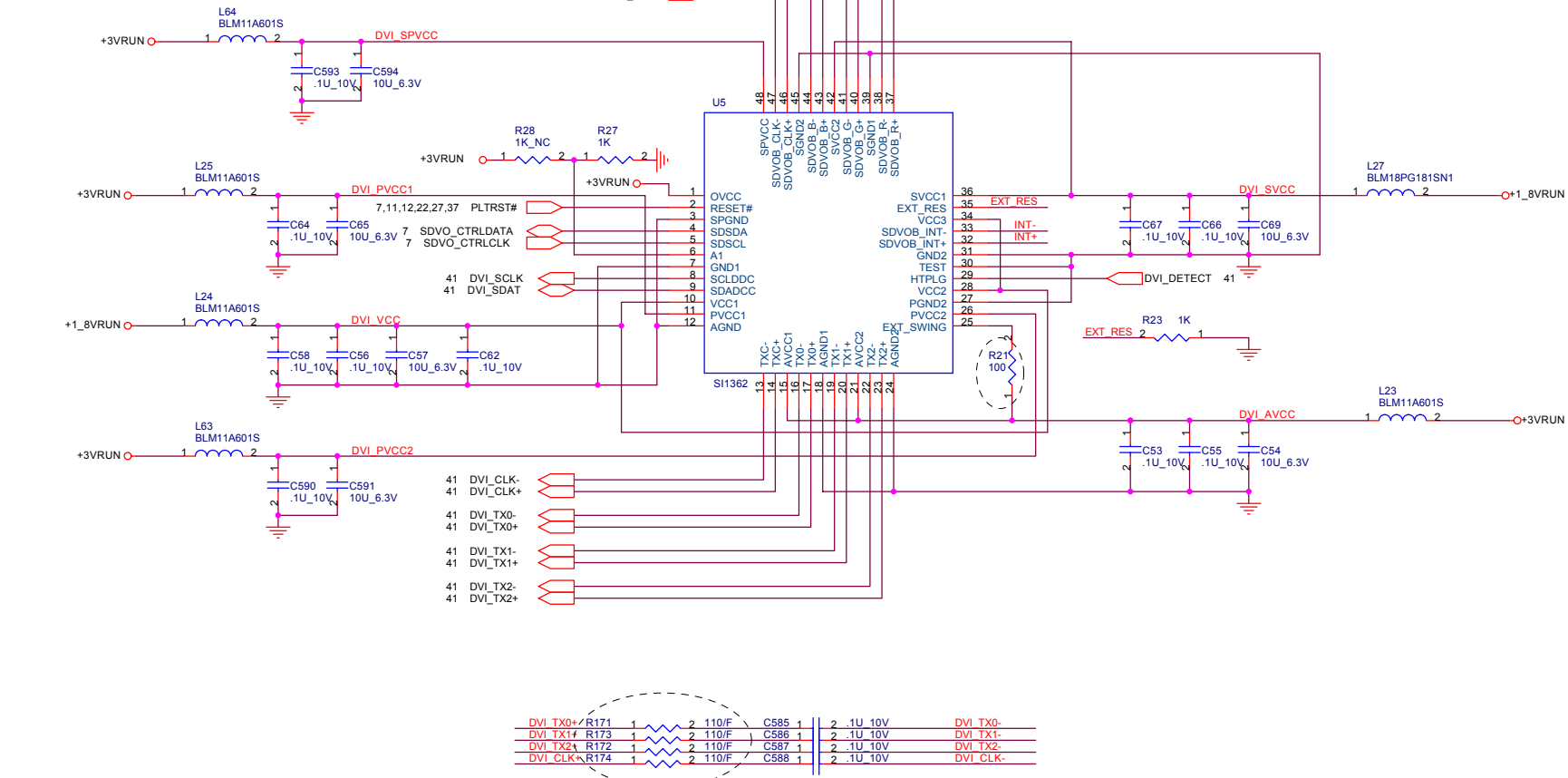
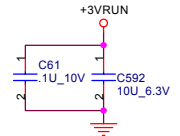


Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.





Placed this capacitor close to OVCC.



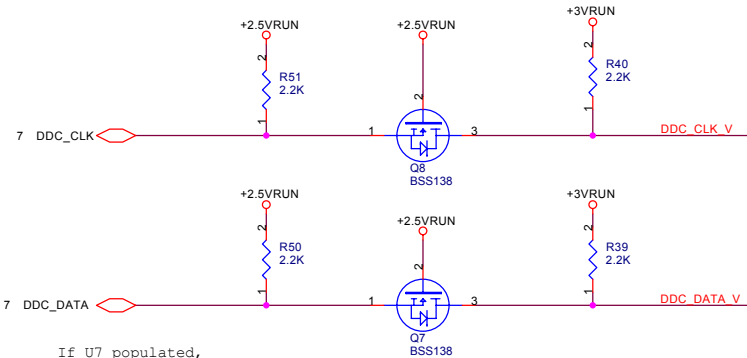
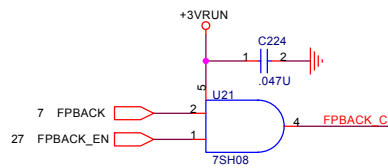
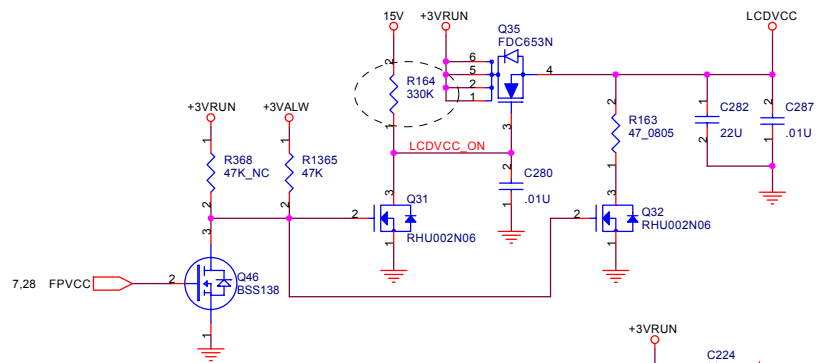
Put these 4 Resistors and 4 Capacitors close to the TX pin of SDVO device



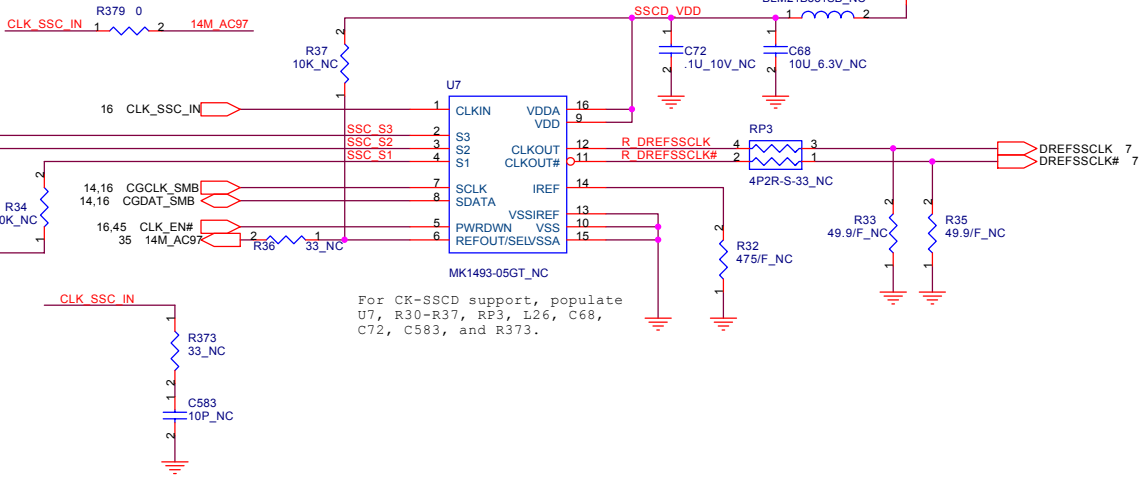
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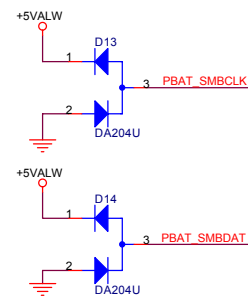
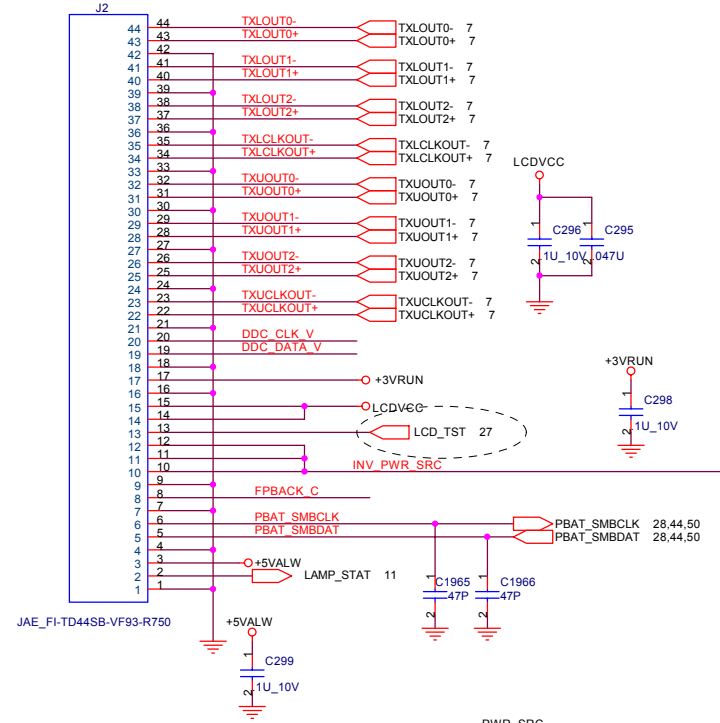
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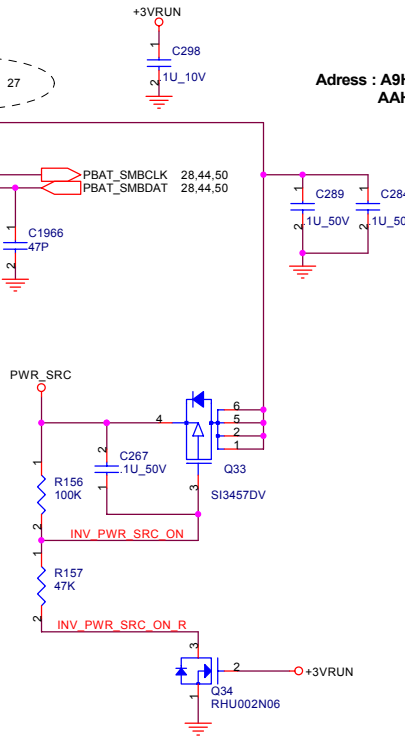
If U7 populated,
R379=NC; If U7=NC,
R379=0-ohm

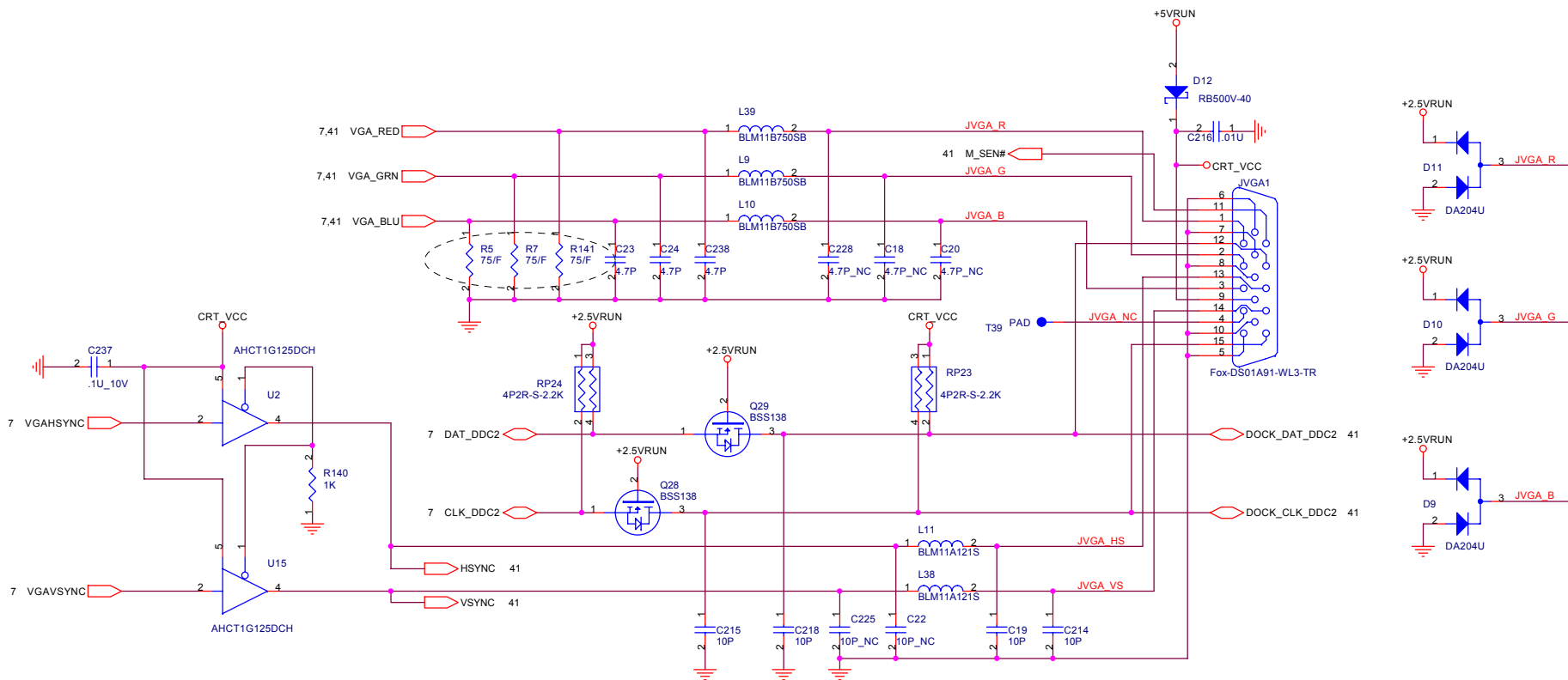


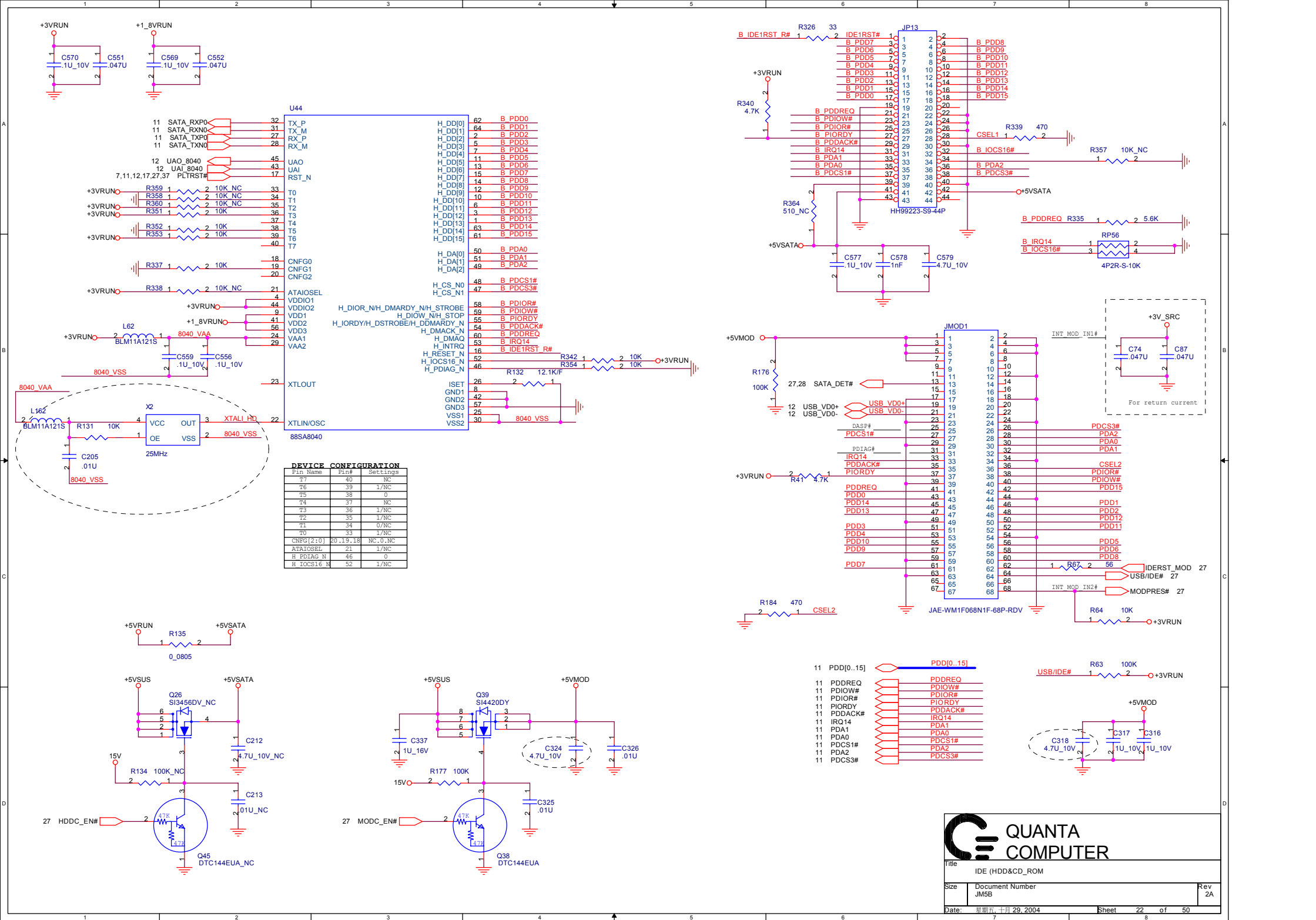
For CK-SSCD support, populate
U7, R30-R37, RP3, L26, C68,
C72, C583, and R373.

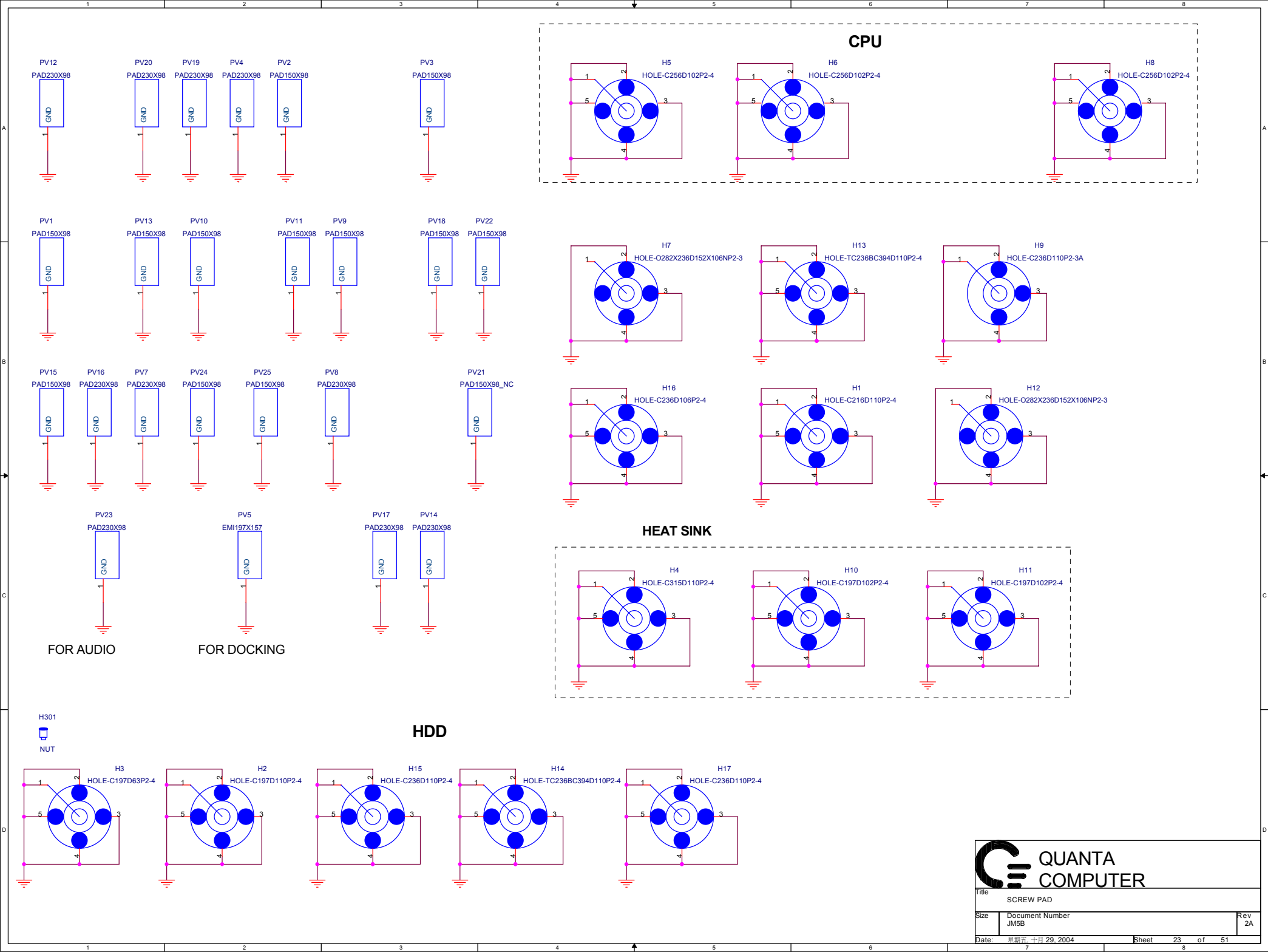


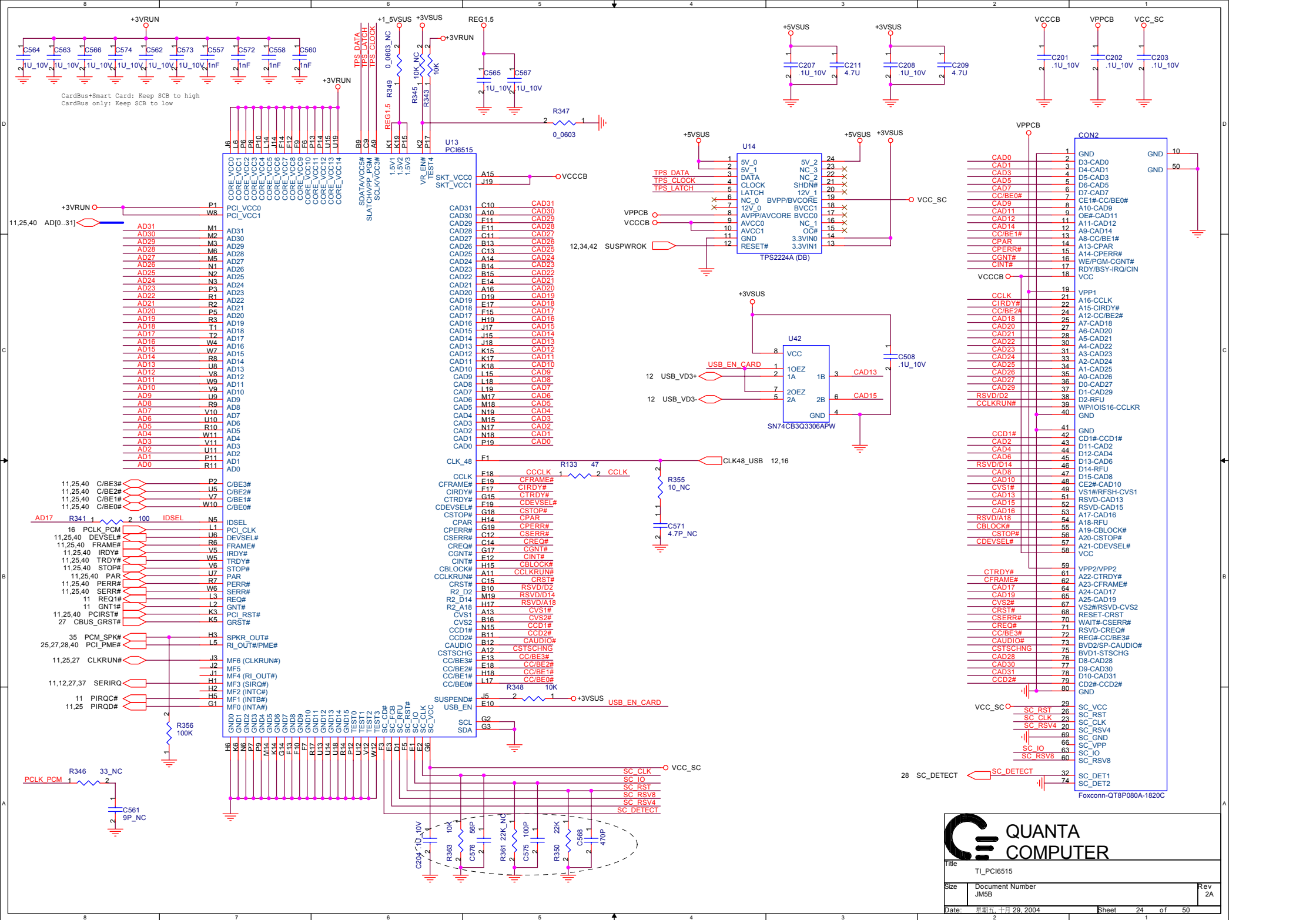
Adress : A9H --Contrast
AAH --Backlight

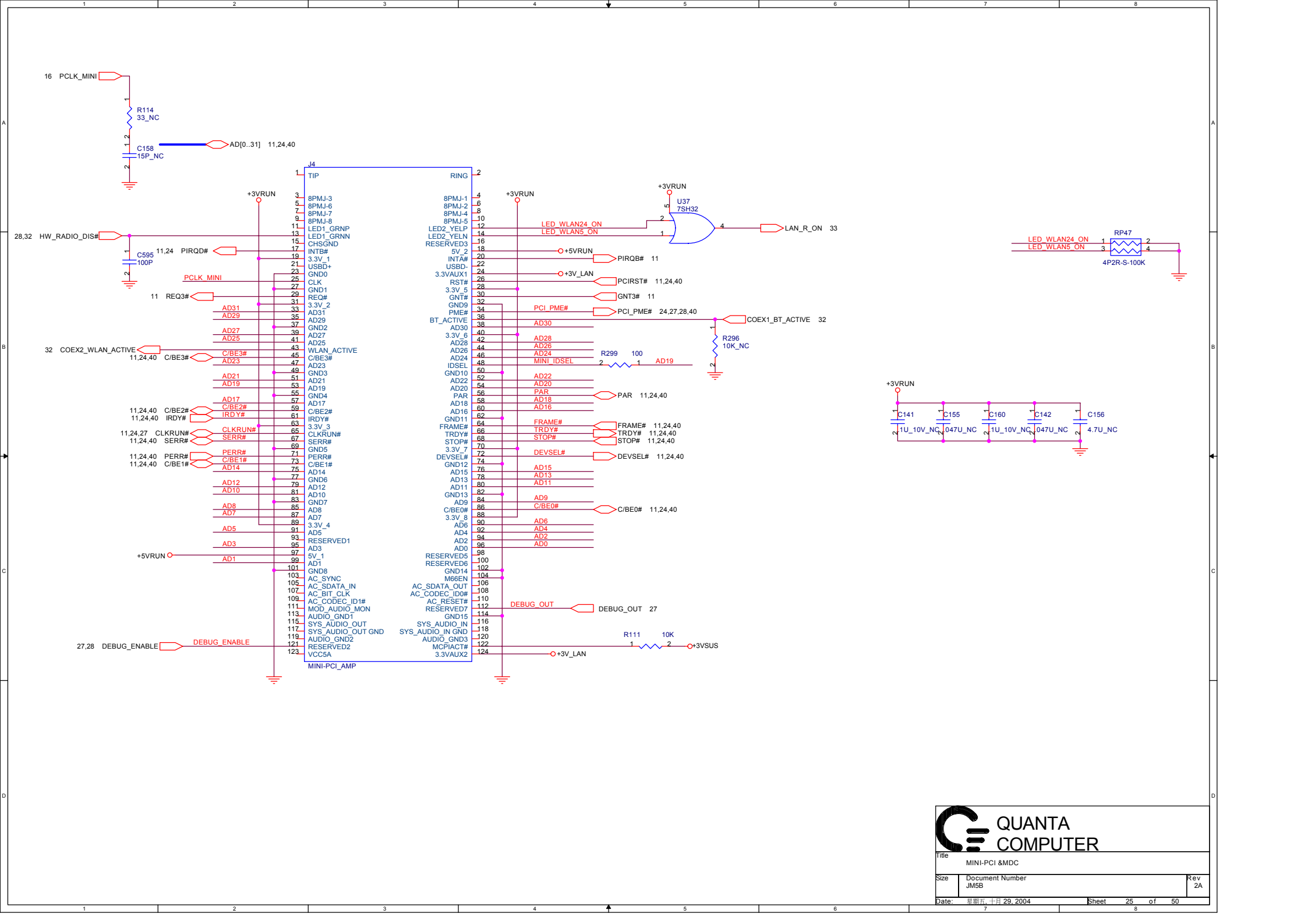


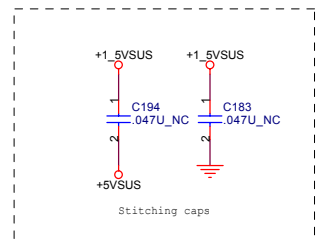




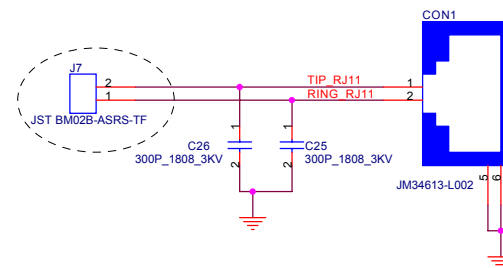
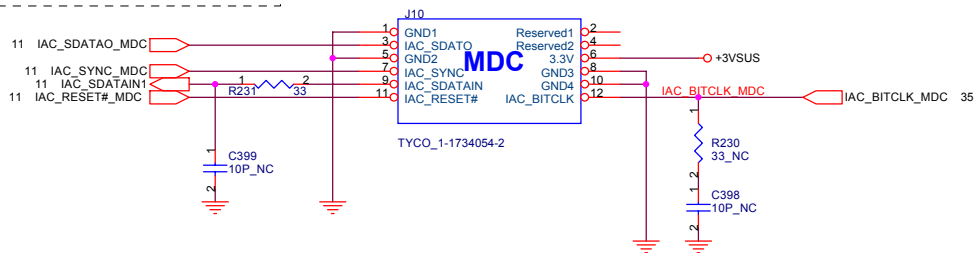
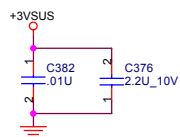


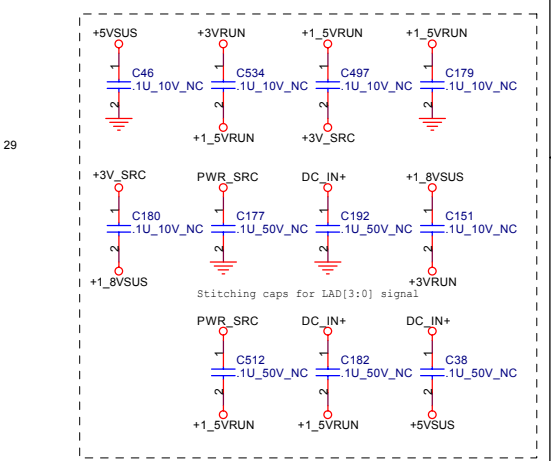
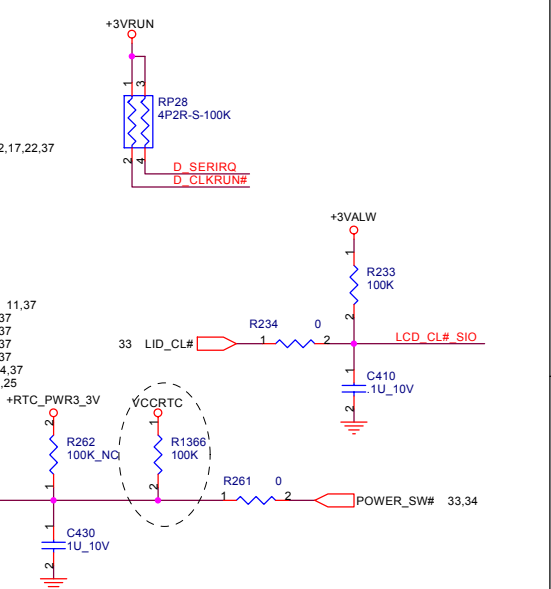
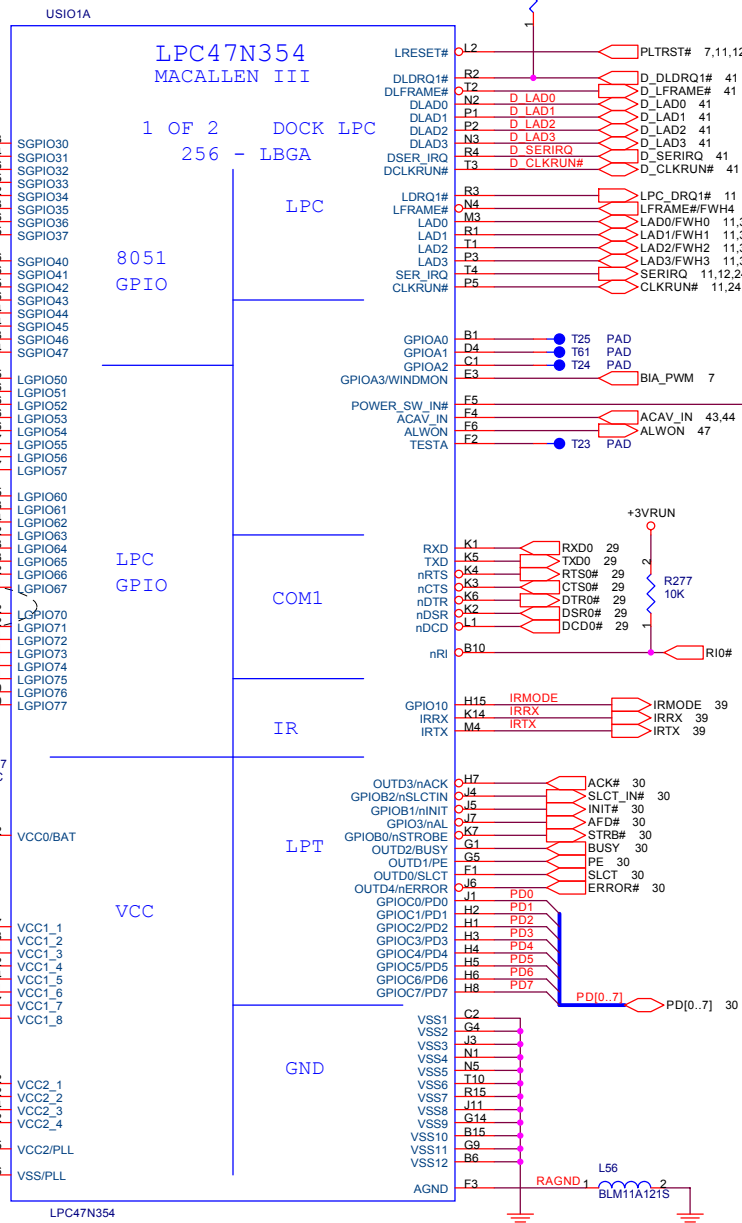
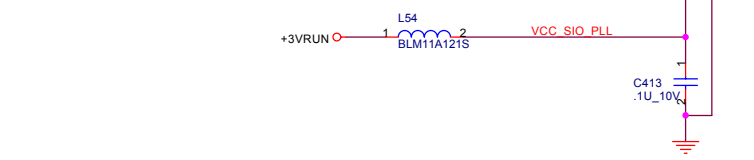
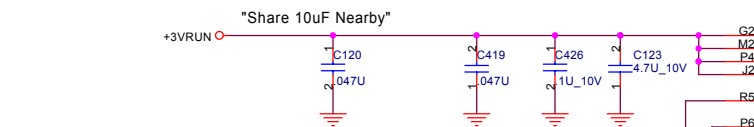
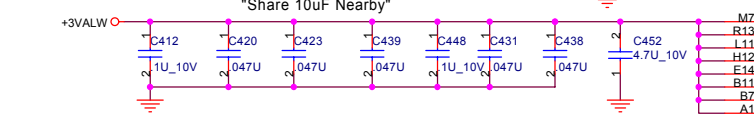
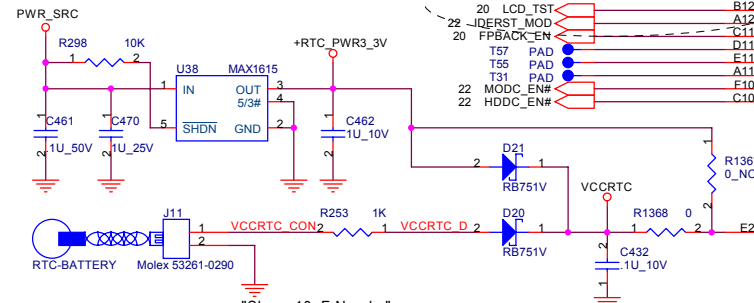
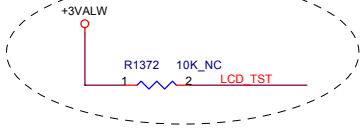
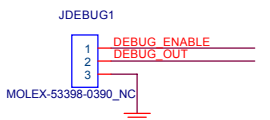
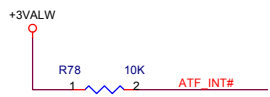


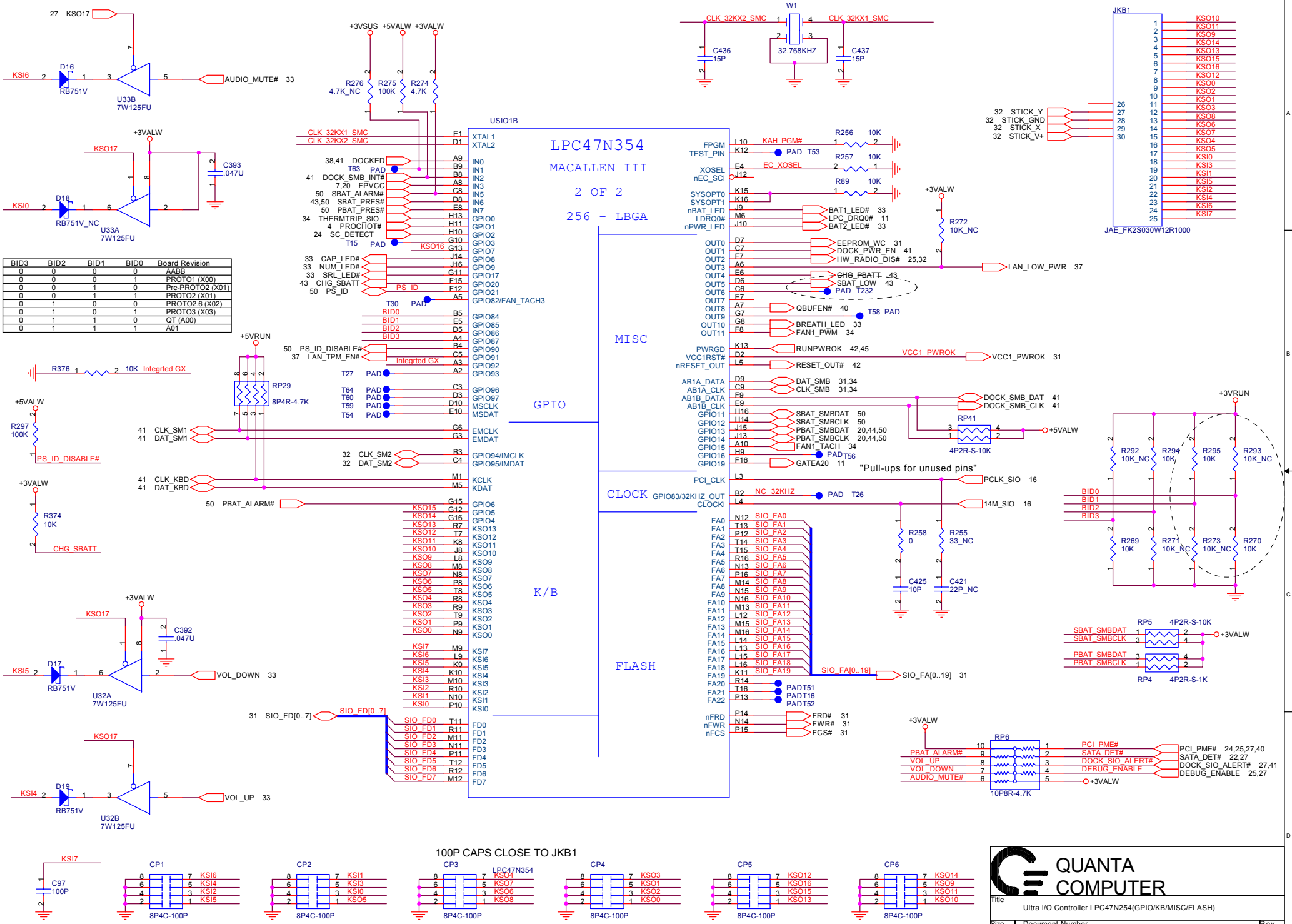




J1001
MDC_NUT







BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	A00
0	0	0	1	Pre-PROTO1 (X00)
0	0	1	0	Pre-PROTO2 (X01)
0	0	1	1	PROTO2.6 (X02)
0	1	0	0	PROTO3 (X03)
0	1	0	1	QT (A00)
0	1	1	0	A01



QUANTA

COMPUTER

Title

Ultra I/O Controller LPC47N254 (GPIO/KB/MISC/FLASH)

Size

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Date

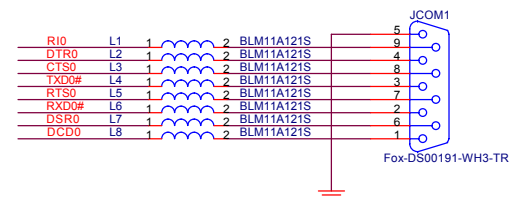
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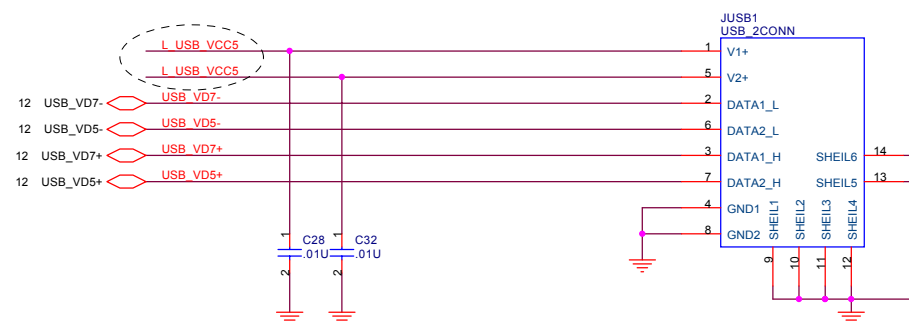
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of

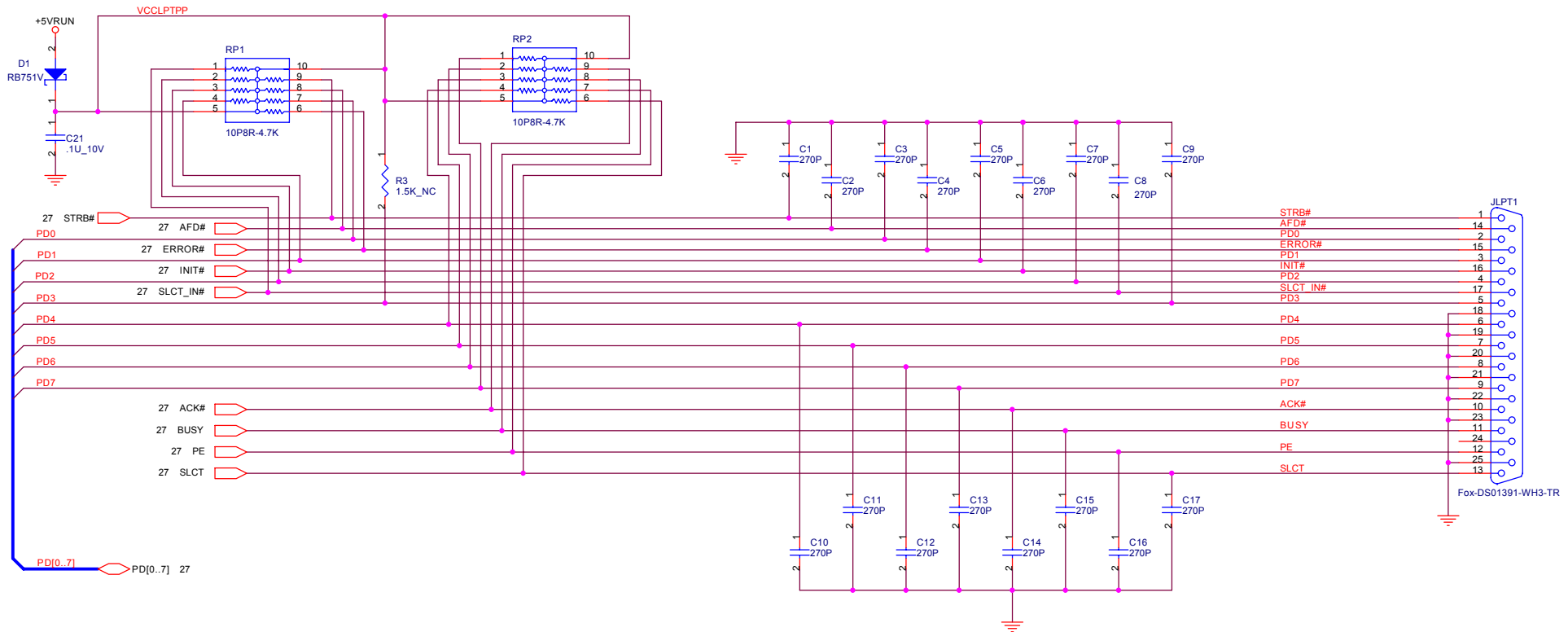
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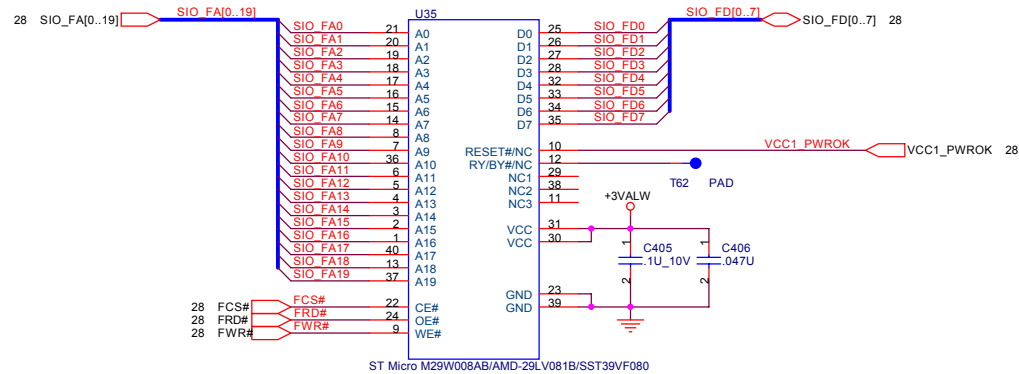
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out



Each channel is
1A



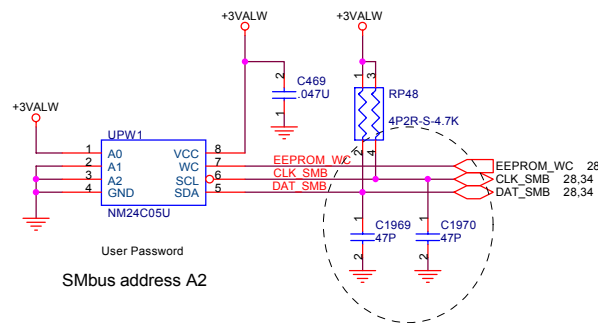
8Mbit (1M Byte),NO PLCC TYPE



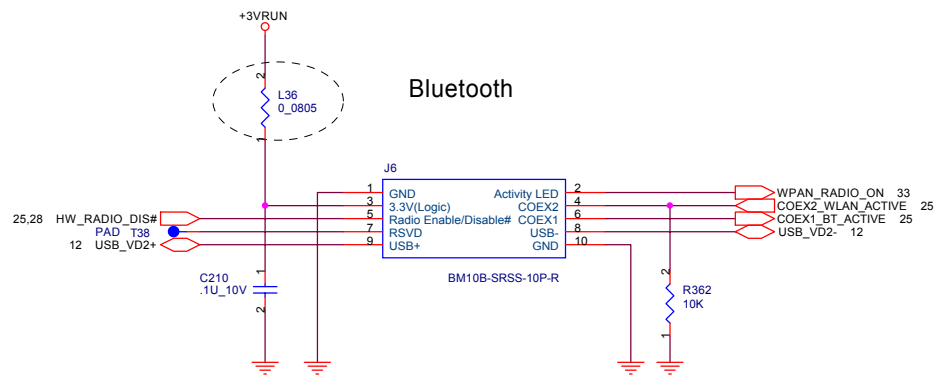
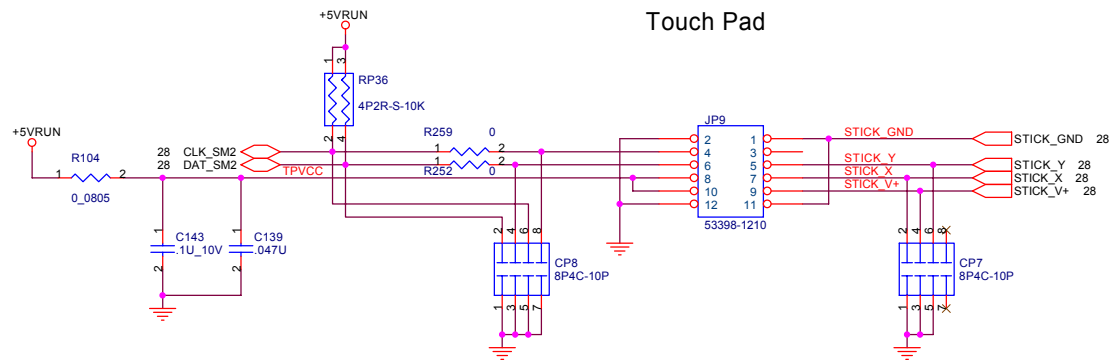
ST Micro M29W008AB/AMD-29LV081B/SST39VF080

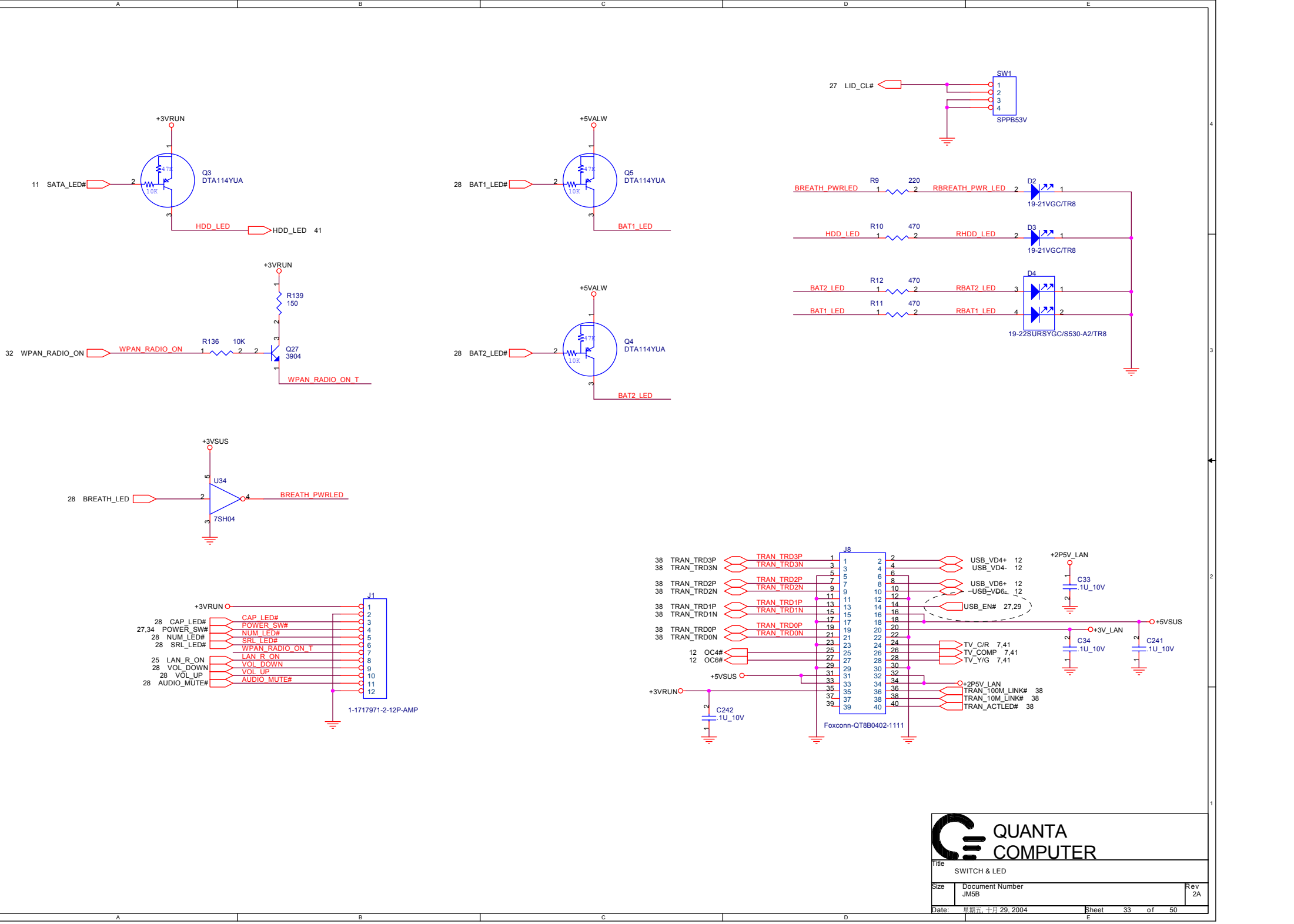
AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

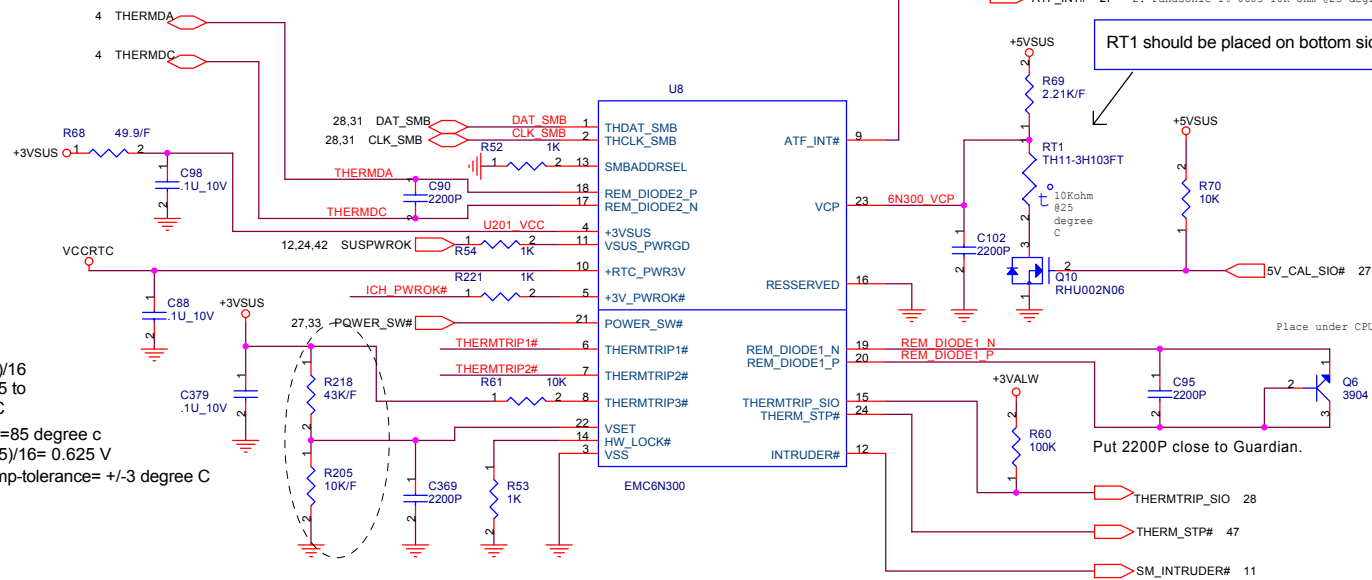
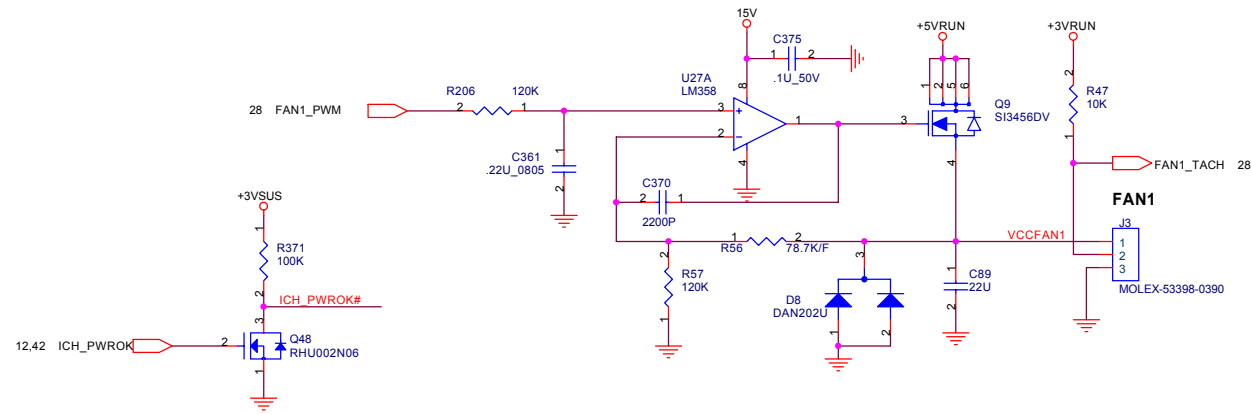
- 1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK



User Password
SMBus address A2







Notes:

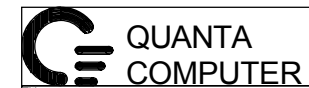
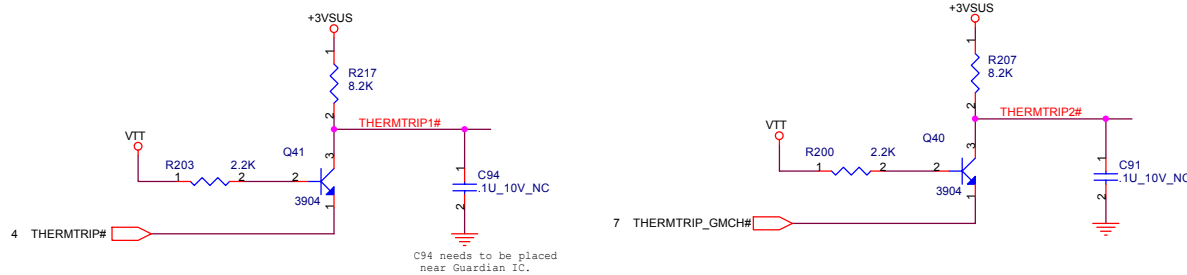
$V_{set} = (T_p - 75) / 16$

Where $T_p = 75$ to 106 degree C

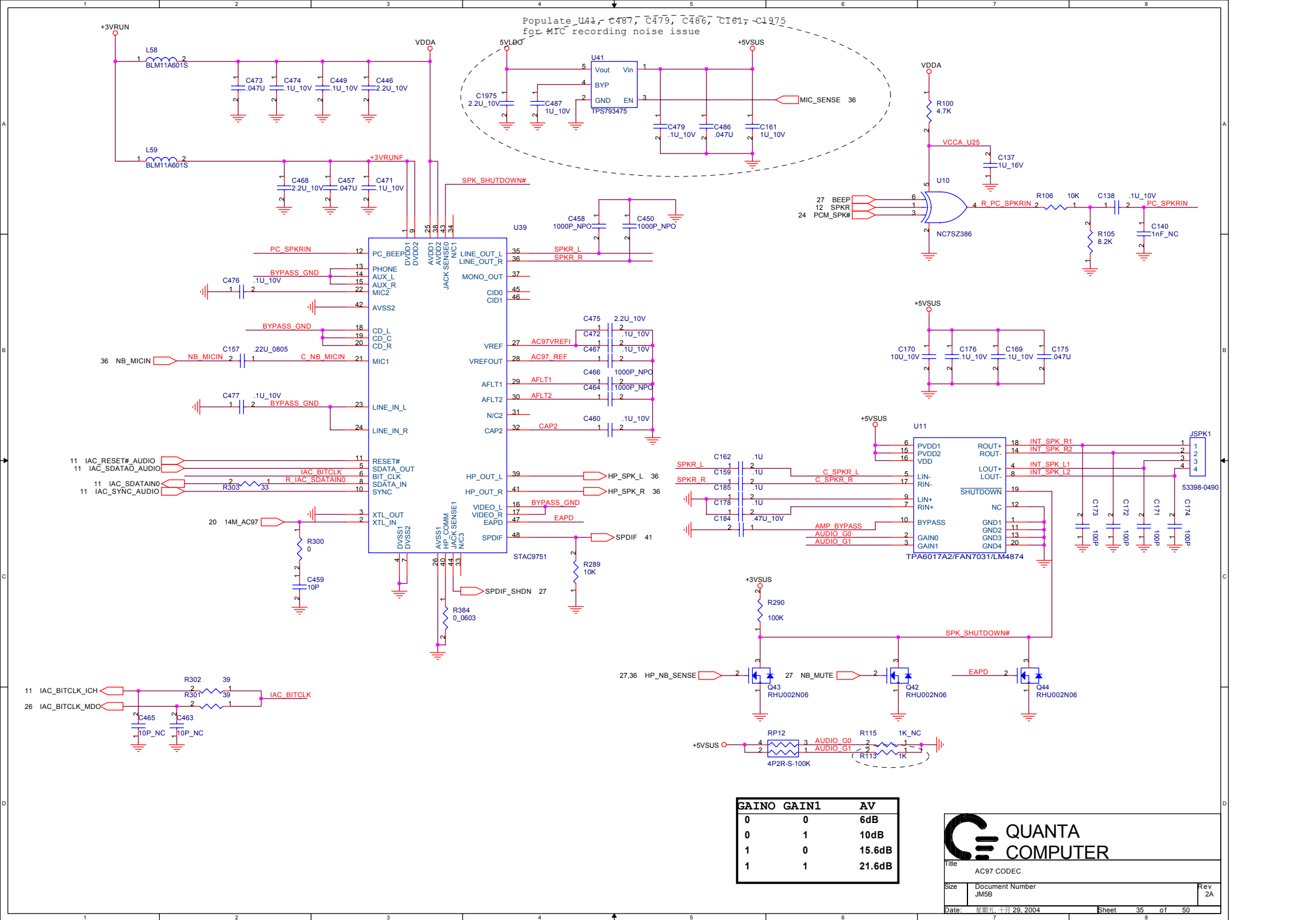
Set trip point = 85 degree C

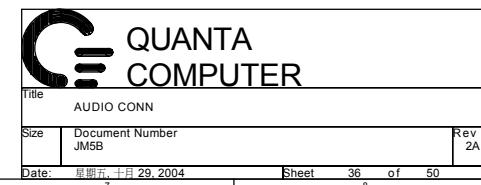
$V_{set} = (85 - 75) / 16 = 0.625$ V

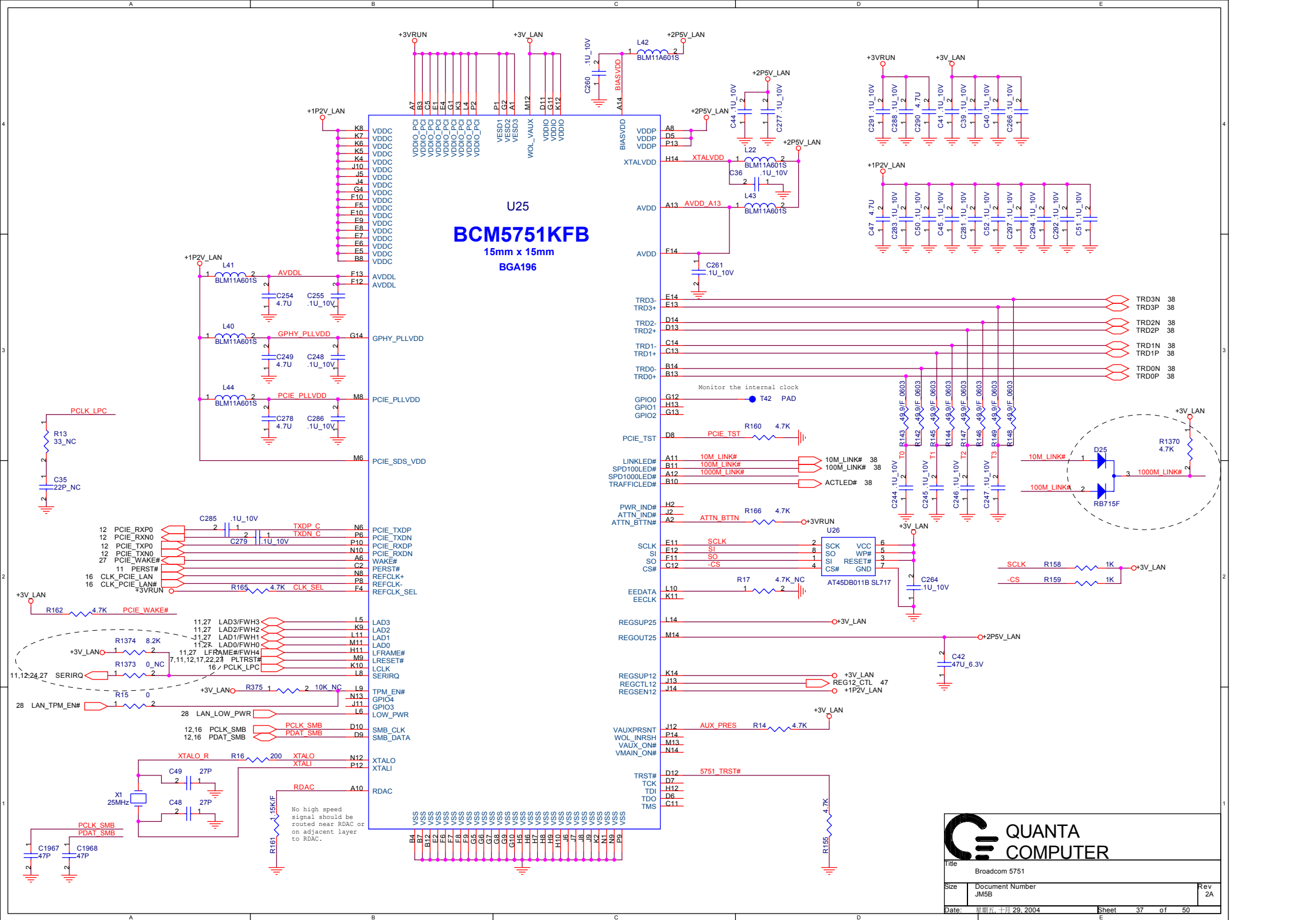
Guardian temp-tolerance = ± 3 degree C



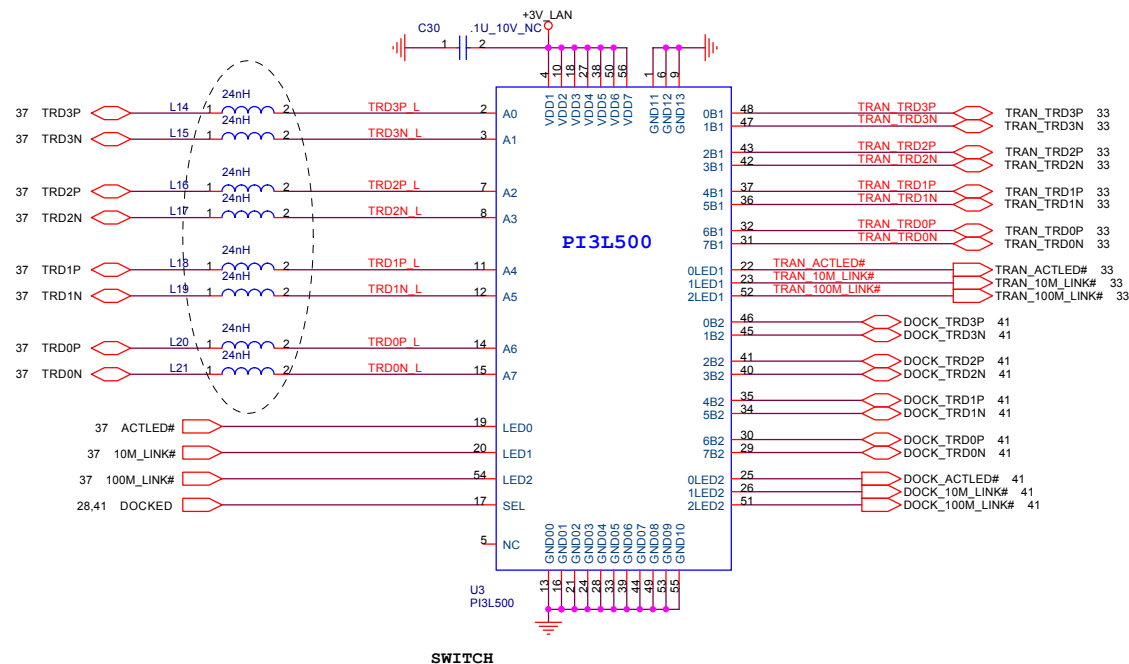
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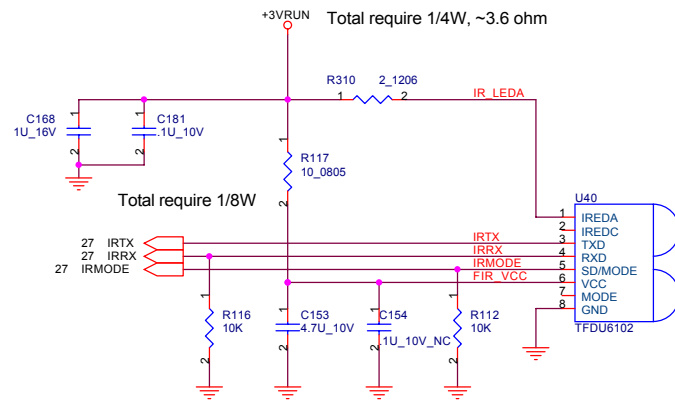


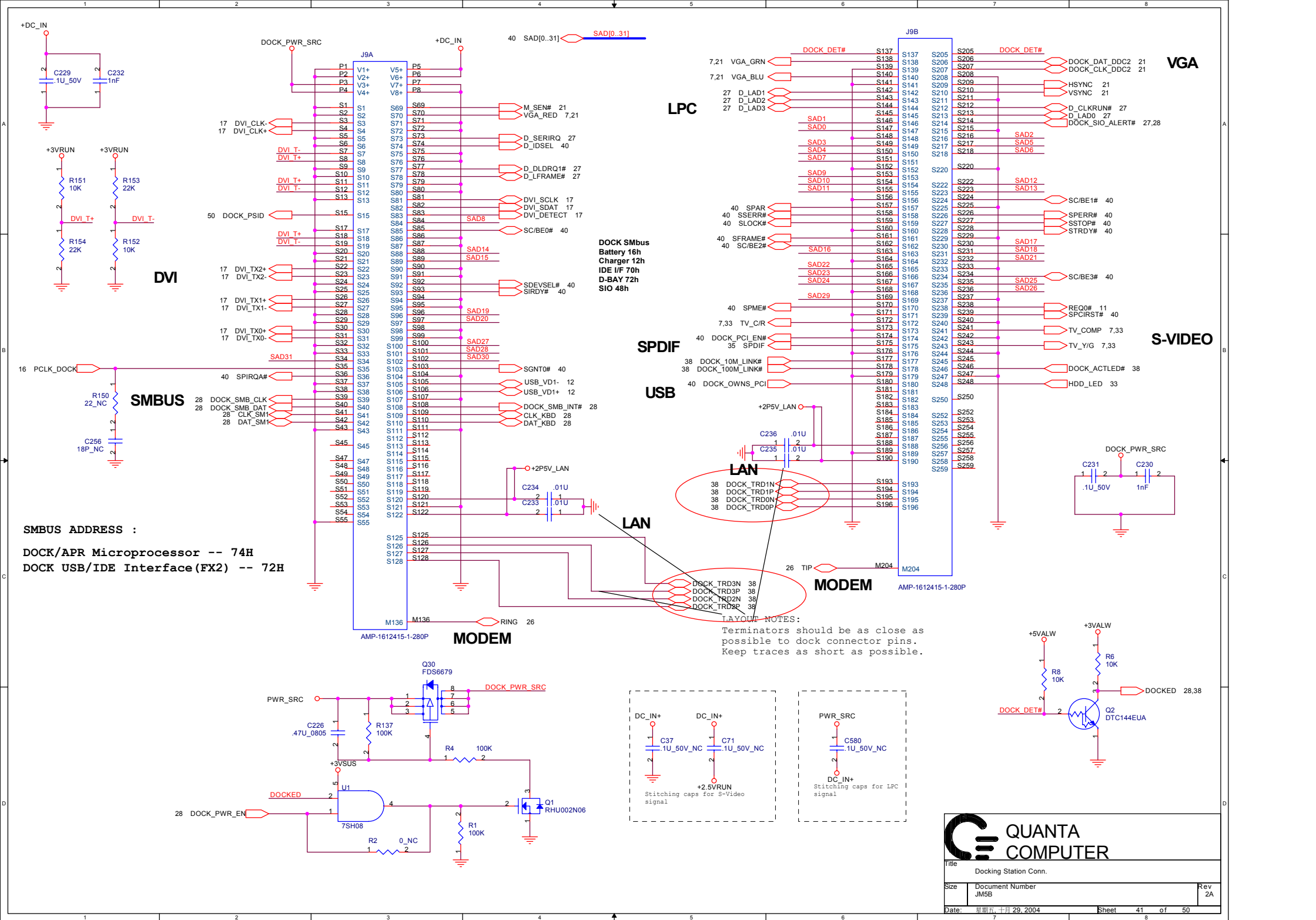


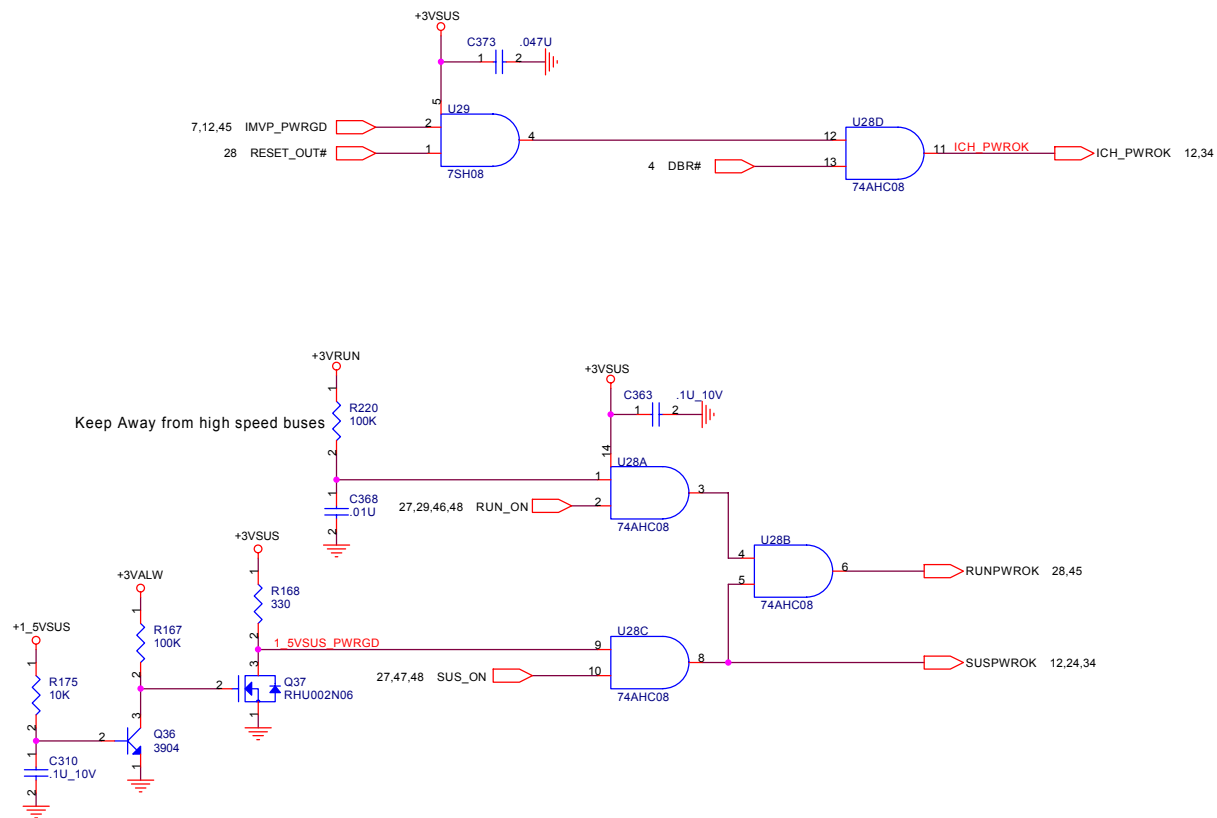


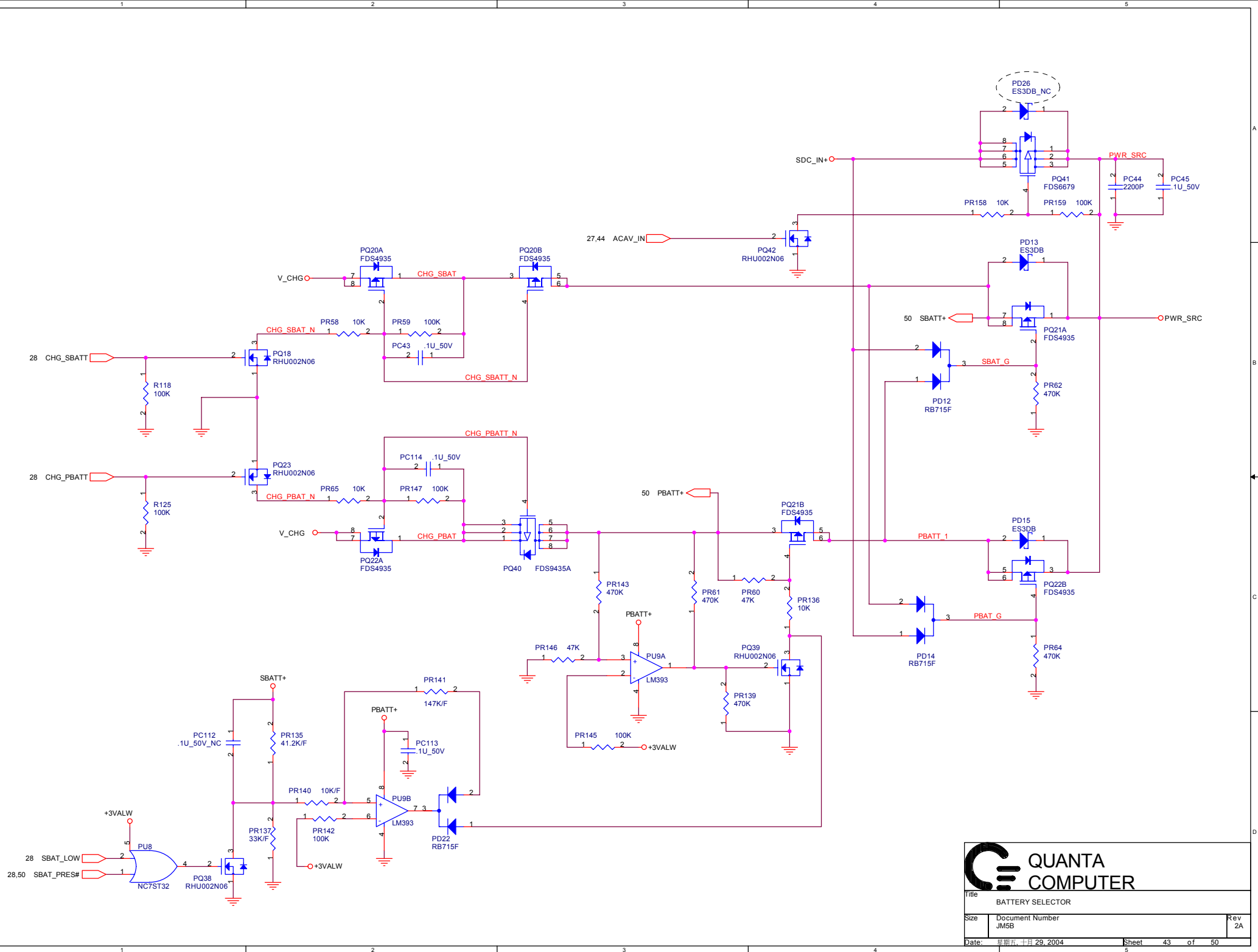
L14/L15/L16/L17/L18/L19/L20/L21 must be 0603







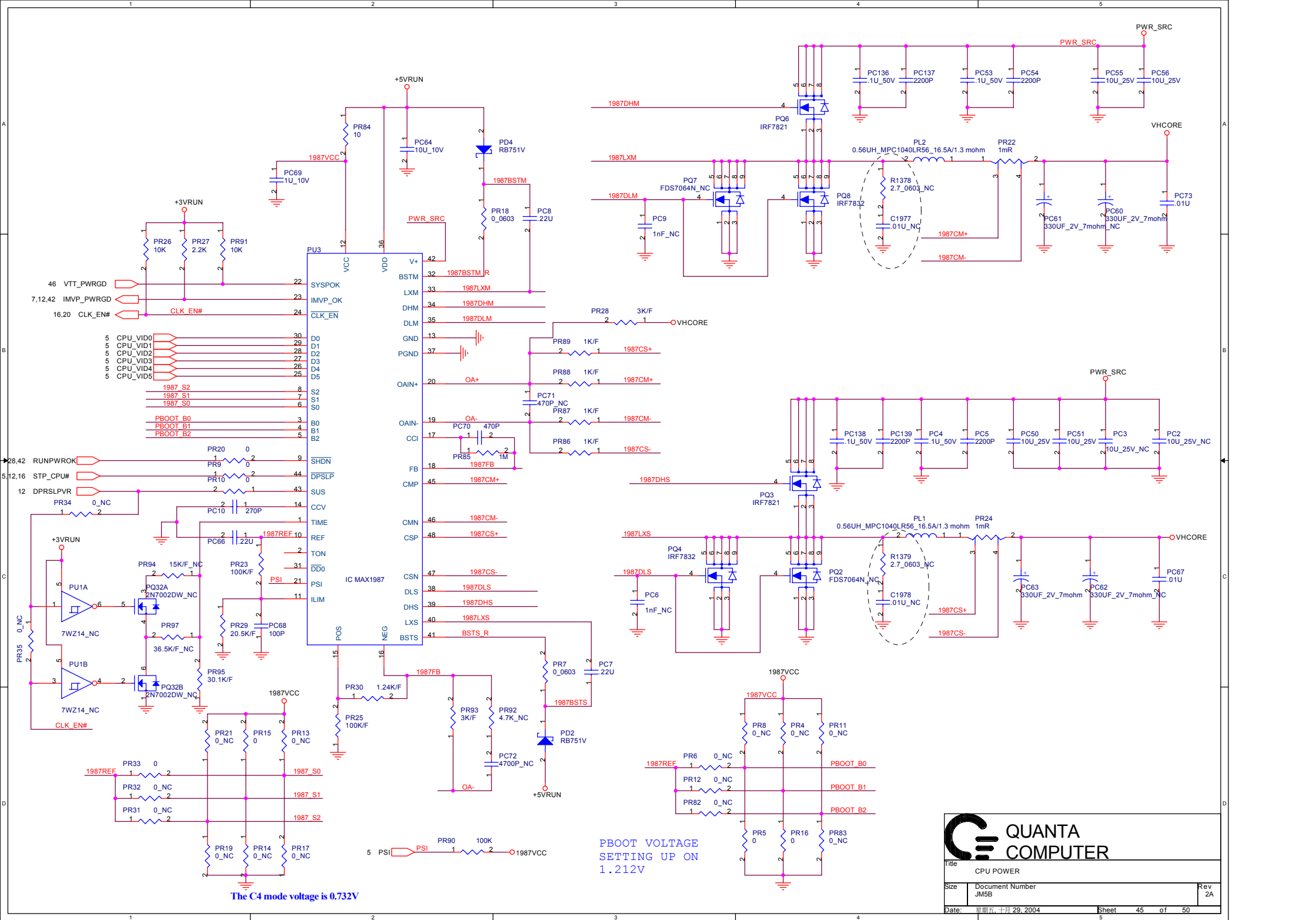


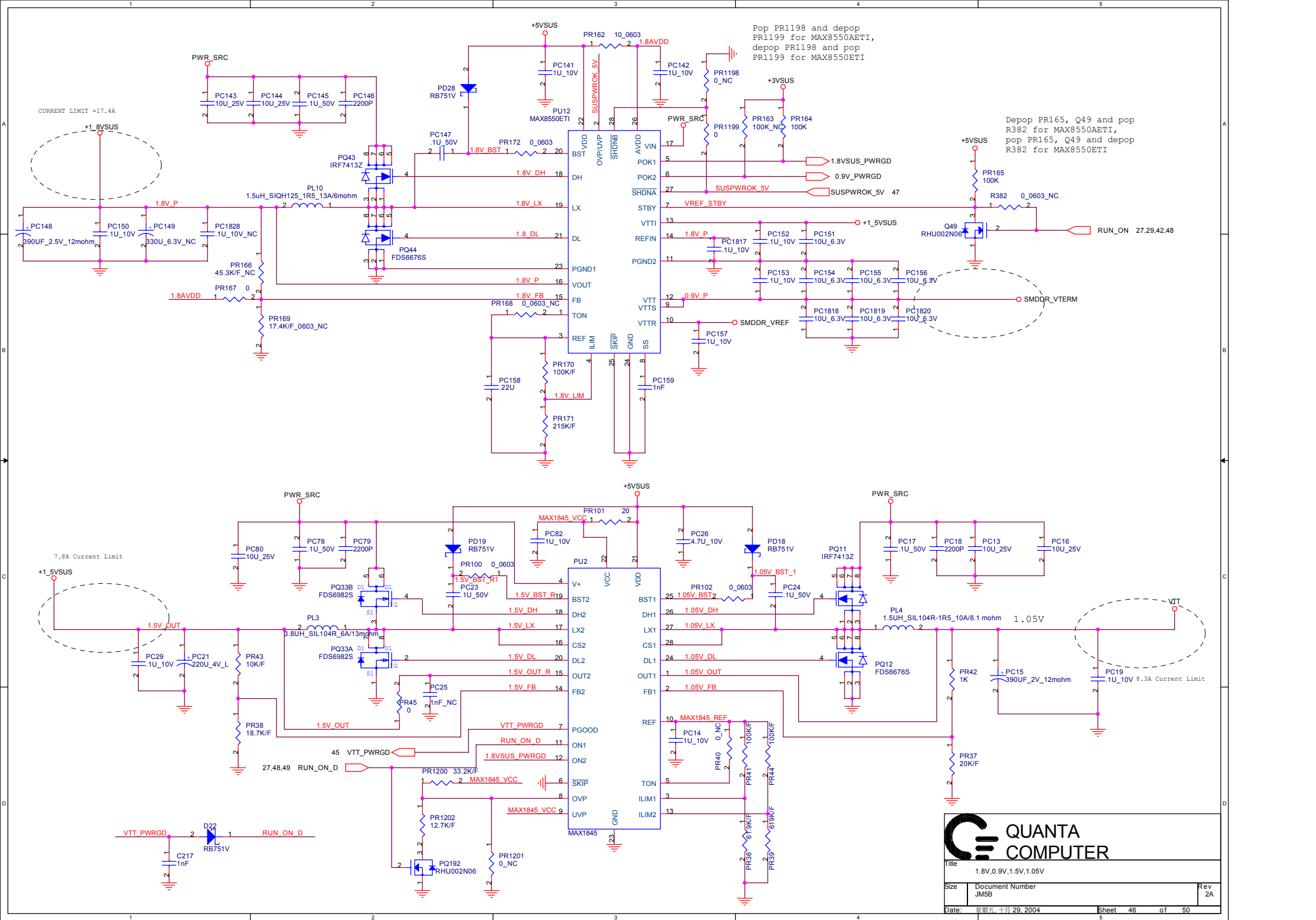


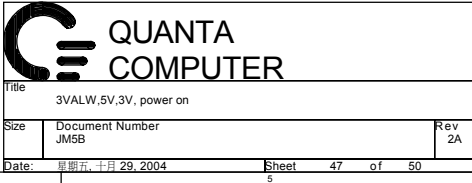


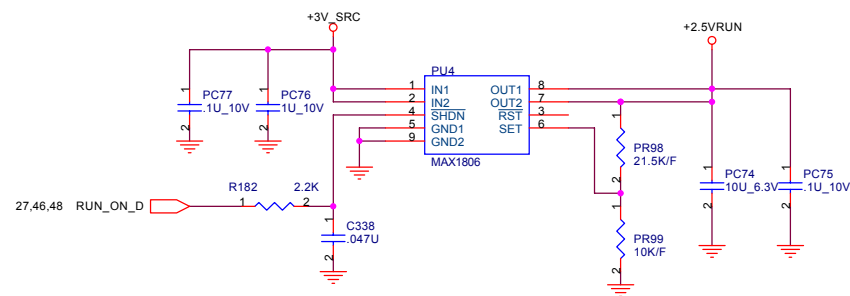
QUANTA
COMPUTER

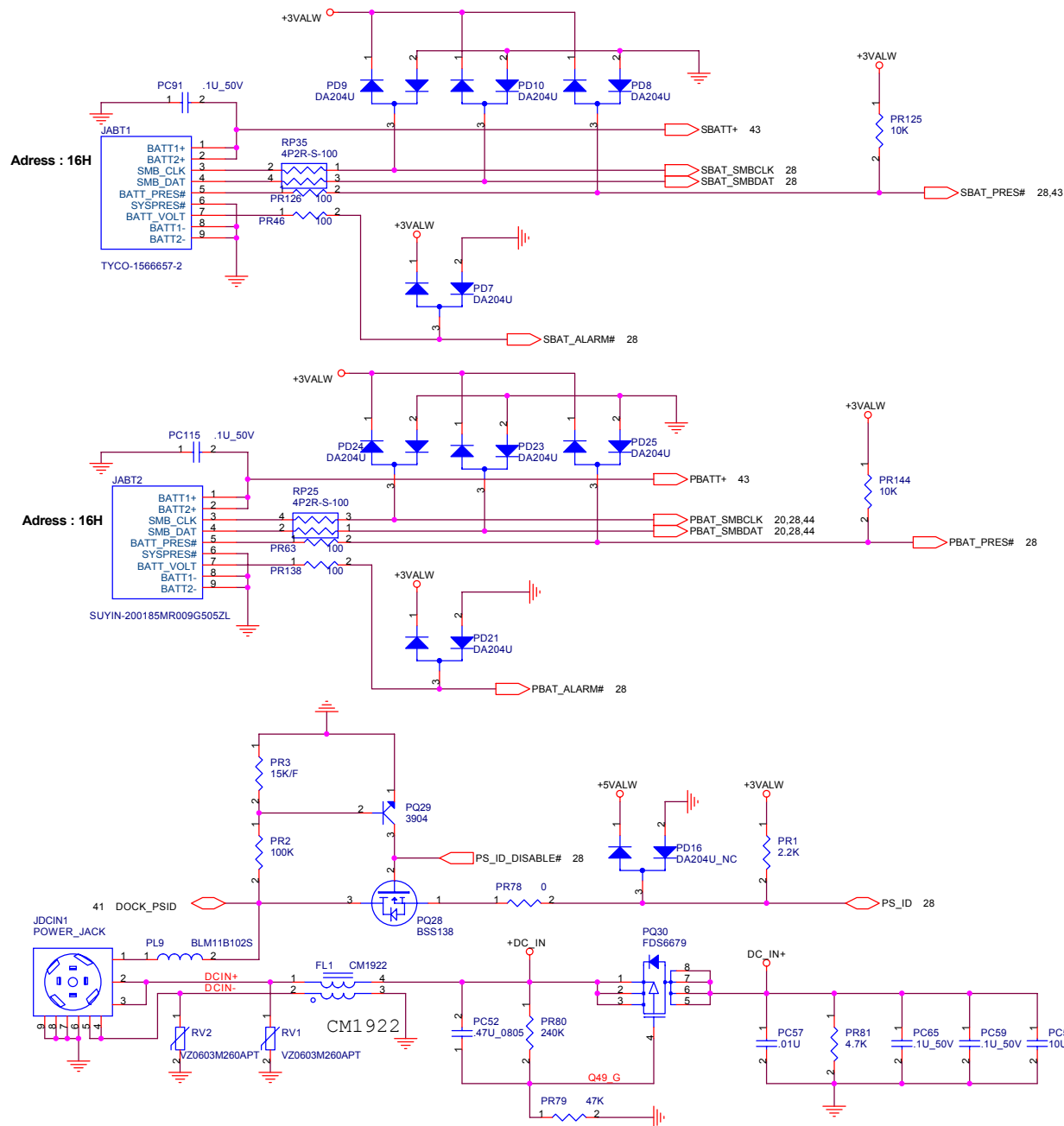
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