

Spears Intel UMA Block Diagram 2007/08/29

Project code : 91.4W001.001
PCB P/N : 07211
Revision : -1

CLK GEN
ICS9LPRS365
4

Intel CPU
Merom 4M
FSB:667MHz/800MHz
5, 6, 7

DDRII Slot 0
533/667
14

DDRII Slot 1
533/667
15

Crestline-GM
AGTL+ CPU I/F DDR I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
8, 9, 10, 11, 12, 13

DMI I/F
100MHz

INTEL
ICH8-M
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
ATA 66/100
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
19, 20, 21, 22

1394
26

1394
25, 26

Ricoh
R5C833
CardReader

SD/SDIO/MMC
MS/MS Pro/xD
26

RJ11 CONN
(Option)
31

MDC MODEM
(Option)
31

Digital Mic Array

MIC IN

HP1

HP2

Internal Analog MIC

Azalia
CODEC
Sigmatel
STAC 9228
32

2CH
SPEAKER

OP AMP
MAX9789A
33

SATA

PATA

HDD
24

ODD
24

Capacity
Button
37

Touch
Pad
37

Int.
KB
37

S/W
CIR
37

Thermal
& Fan
G792
36

Flash ROM
1MB
35

KBC
Winbond WPC8763L
34

SPI

RGB CRT

LVDS

S-Video
(Upsell)

SDVO

Sii 1392
(Upsell)

23

HDMI
(Upsell)

16

Power SW
TI TPS2231
28

New Card
28

10/100 NIC
Marvell 88E8040
27

RJ45 CONN
28

Mini-Card X2
802.11a/b/g
BT/USB/Robson
29
30

Mini-Card X1
WWAN(Upsell)
30

CAMERA
(Option)
24

Lift Side: USB x 2
Right Side:
USB x 1
USB x 1(Upsell)
24

CPU DC/DC ISL6262A	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS5117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 5V_S5 3D3V_S5

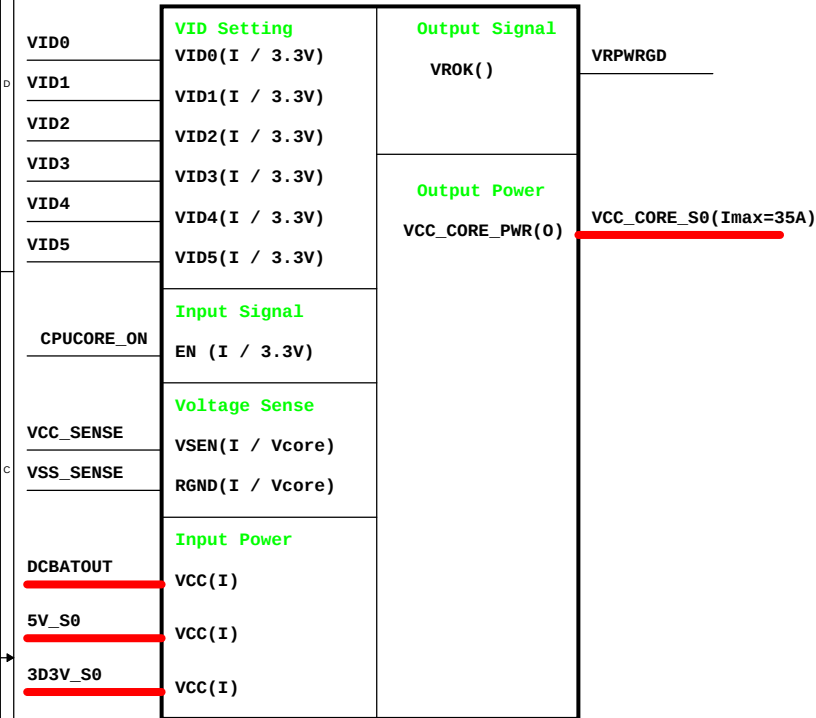
SYSTEM DC/DC TPS51100	
INPUTS	OUTPUTS
1D8V_S3	0D9V_S3

SYSTEM DC/DC LDO	
INPUTS	OUTPUTS
3D3V 1D8V	2D5V 1D5V_S0

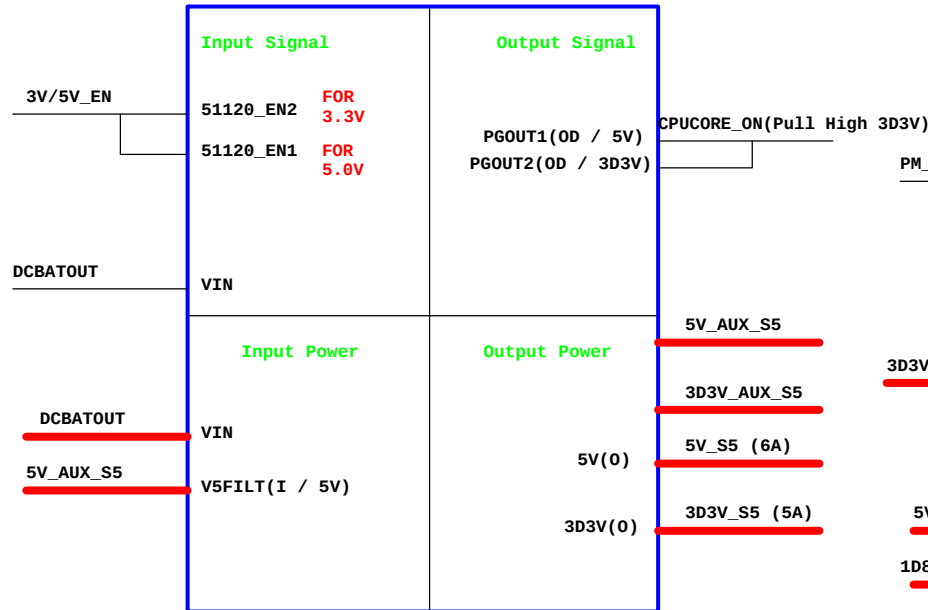
SYSTEM DC/DC LDO	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 1D5V_S0

MAXIM CHARGER MAX8731A	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

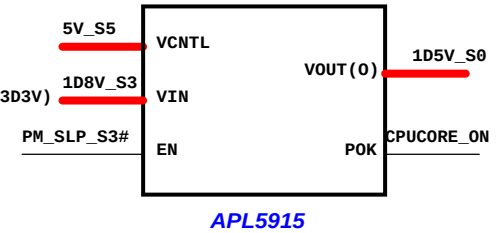
CPU_CORE
ISL6262A



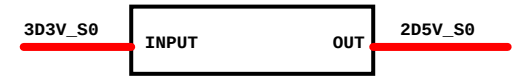
TI TPS51120
3D3V/5V



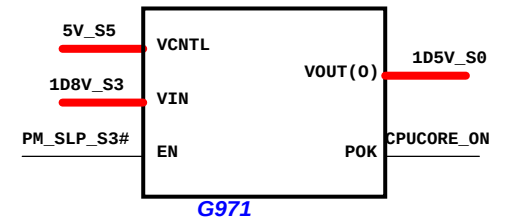
1D5V_S0



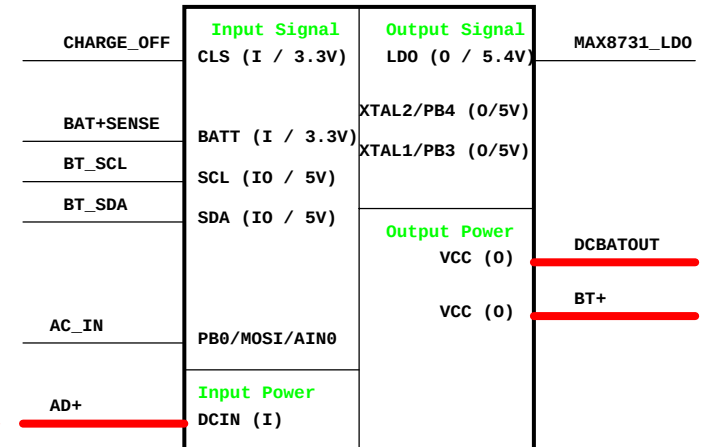
2D5V_S0



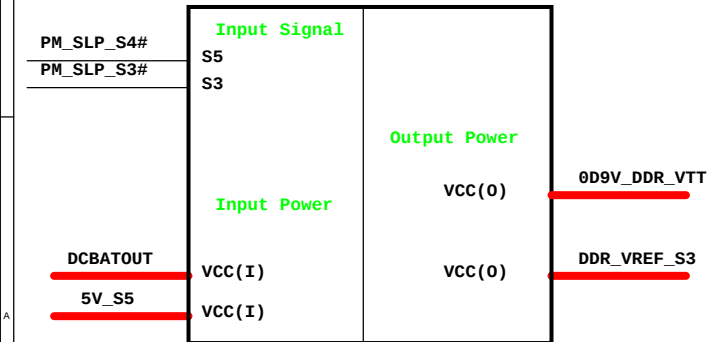
1D25V_S0



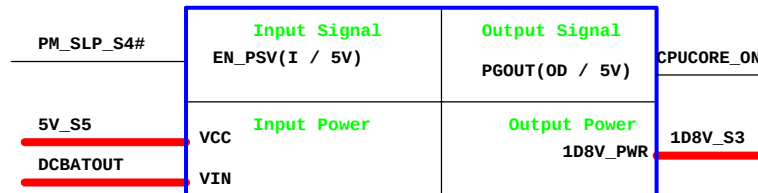
Charger_MAX8731A



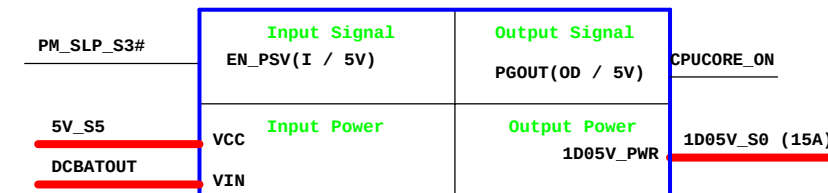
TI TPS51100
0.9V/DDR_VREF_S3



TPS51117_1D8V_S3



TPS51117_1D05V



INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPI020	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RSVDTP3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIe port config bit1

A16 swap override strap	
PCT_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable Low=Disable	
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable Low=Disable	

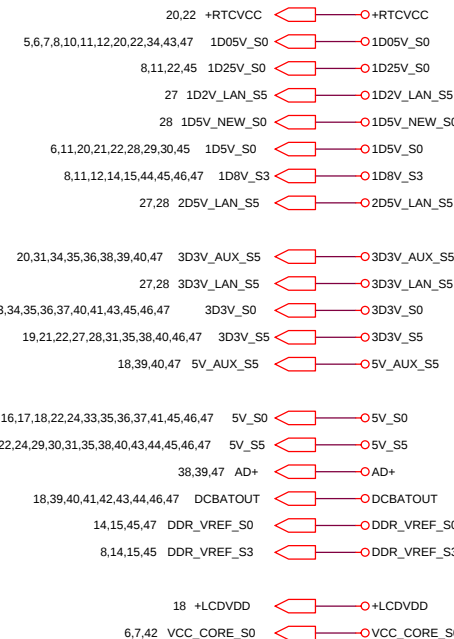
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPI0[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPI023	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

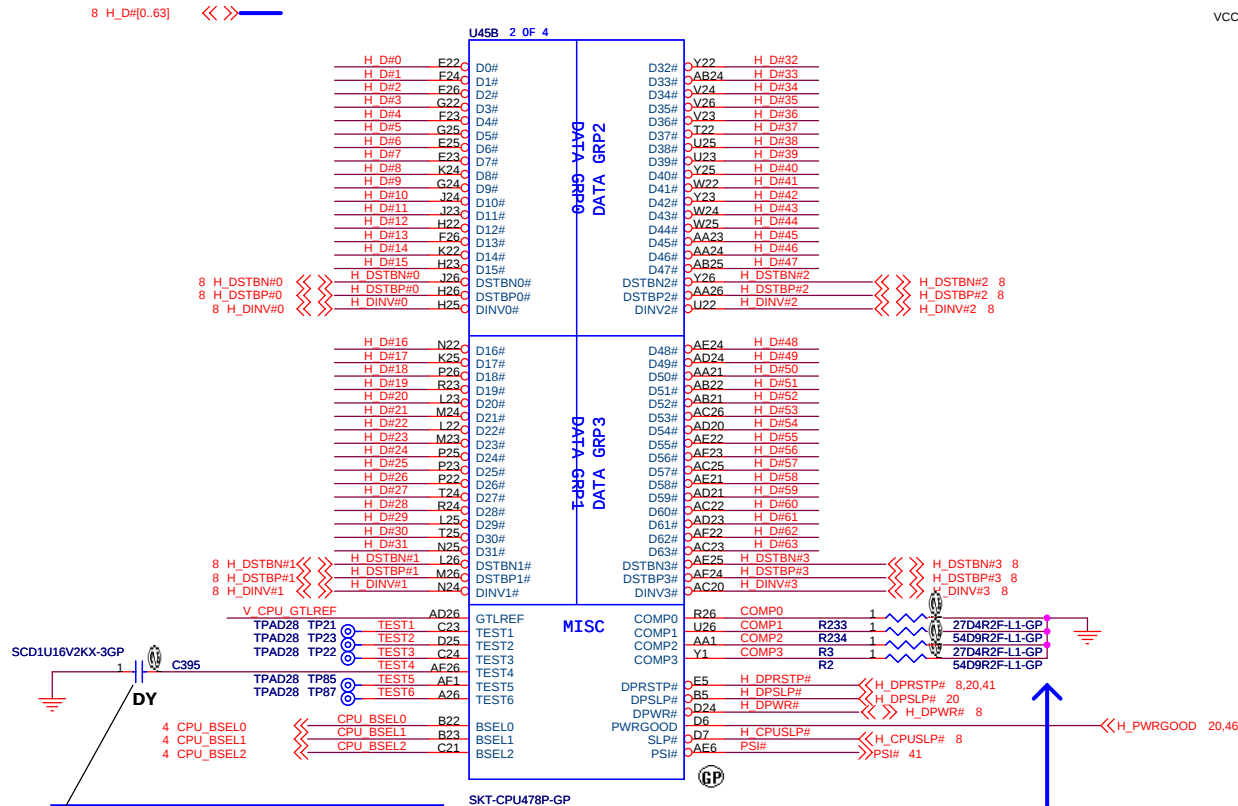


INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5		
CFG 8	DMI X 2	DMI X 4
CFG 9	Low Power PCI Express	Normal
CFG 9	PCI Express Graphics Lane Reversal	Normal Mode(Lanes number in order)
CFG 16	FSB Dynamic ODT	Disabled
CFG 19	DMI Lane Reserved	Enabled
CFG 20	Only PCIe or SDVO is operation	Reserved Lane
CFG 20	Concurrent SDVO/PCIe	PCIe and SDVO are operation simultaneous
SDVO_CTRL_DATA	NO SDVO Card Present	SDVO Card Present

CFG 12	XOR/ALL-Z
CFG 13	
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

<Core Design>		
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Table of Content		
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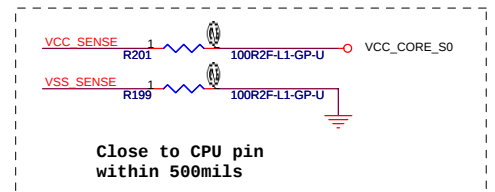
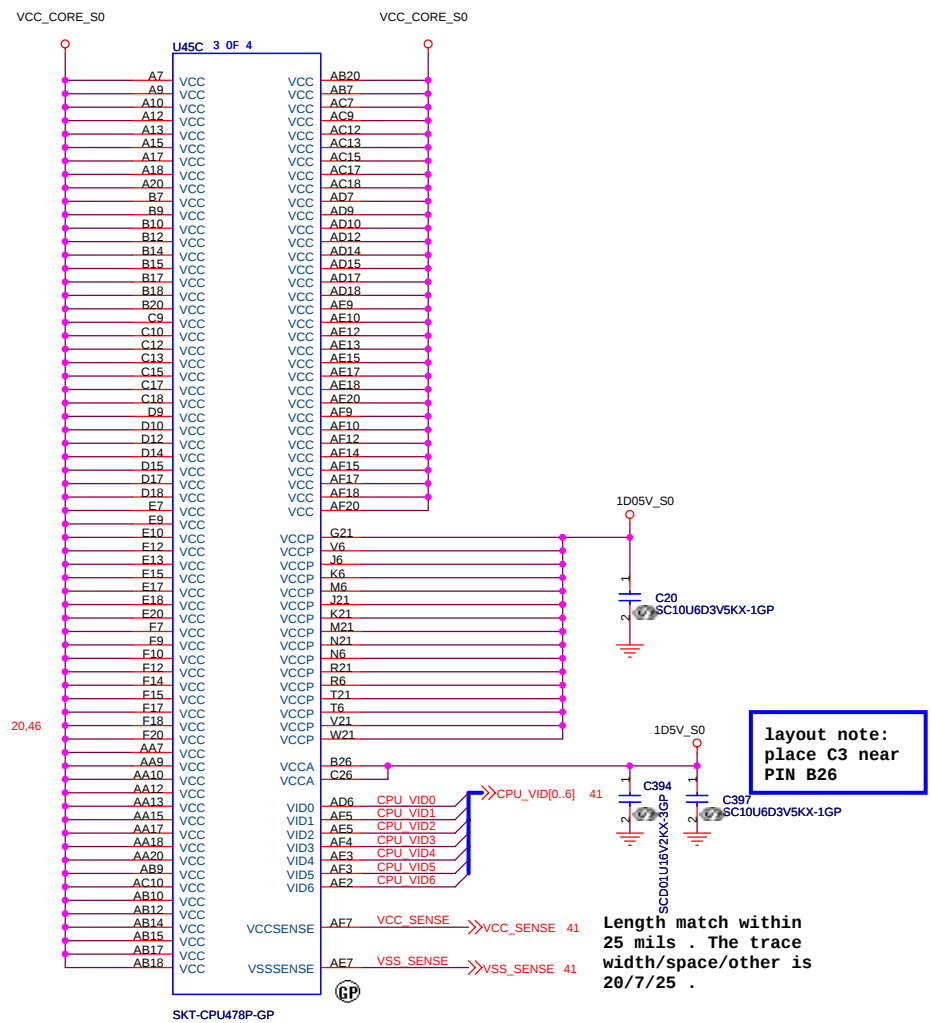
PLACE C25 close to the TEST4 PIN, make sure TEST3,TEST4,TEST5 trace routing is reference to GND and away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

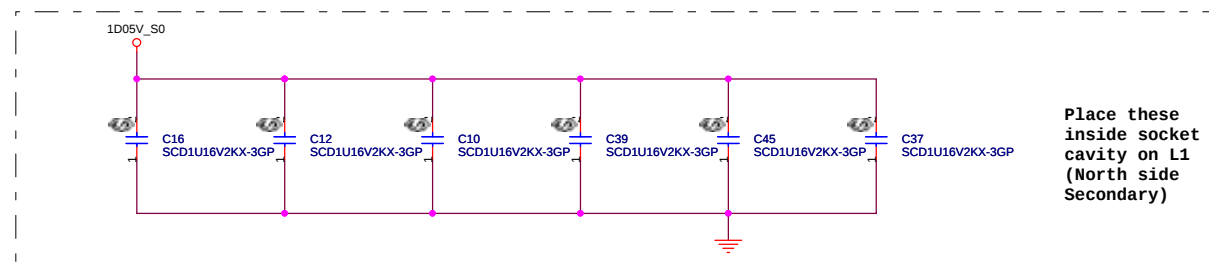
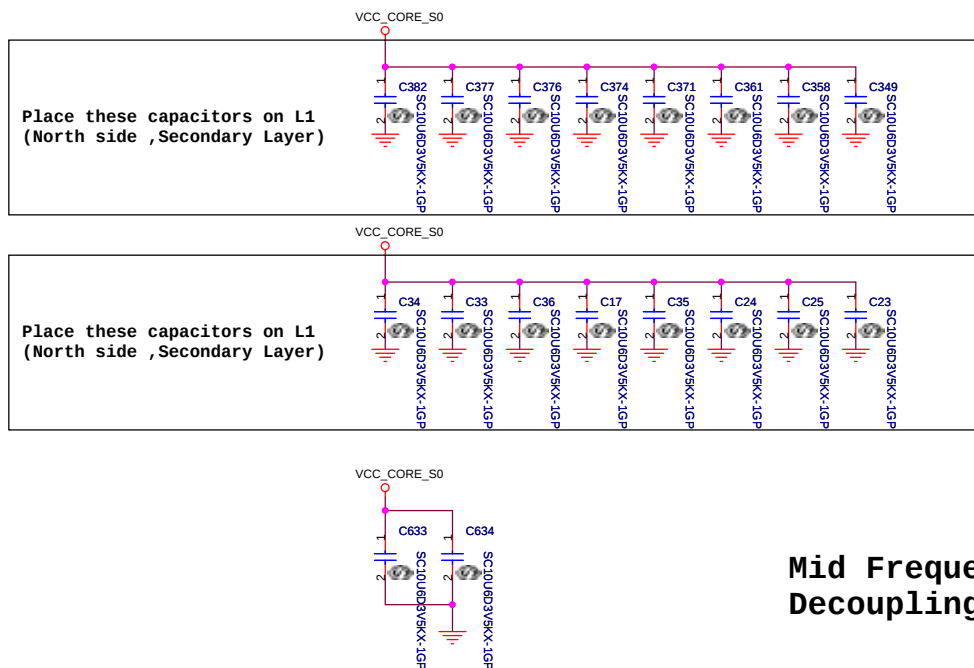
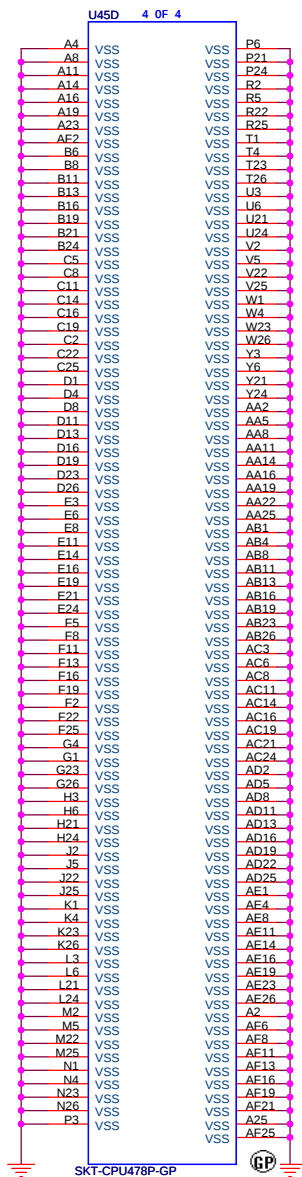
Resistor Placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Close to CPU pin AD26
Z0=55 ohm
with in 500mils.

Place C635 near R238 and R239



<Core Design>



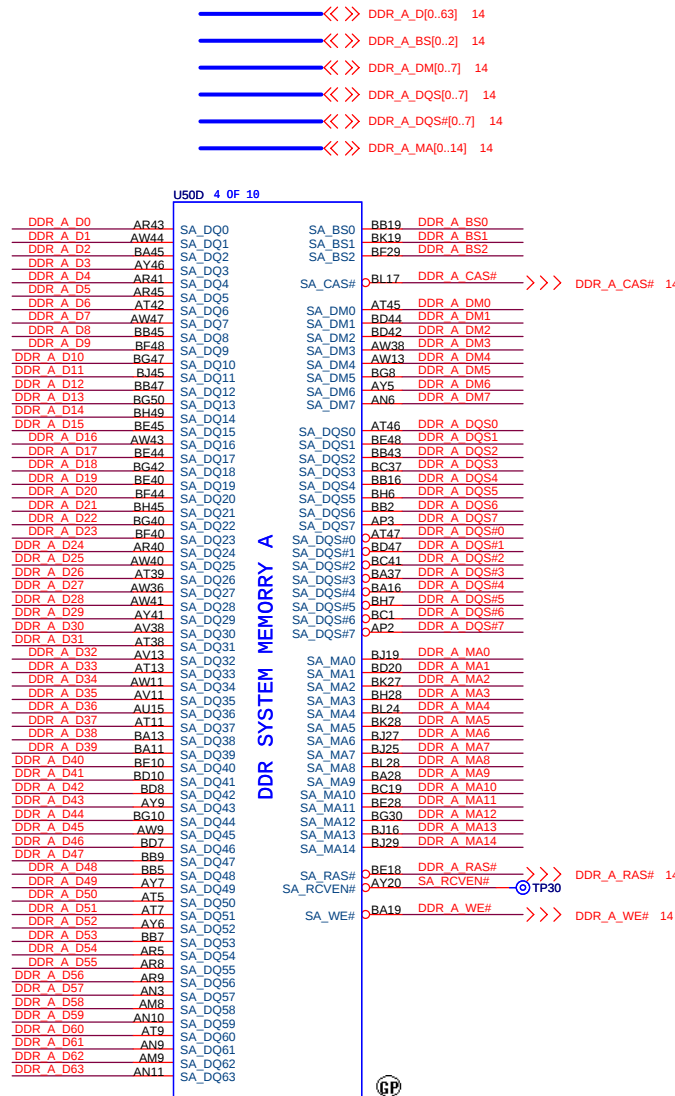


D

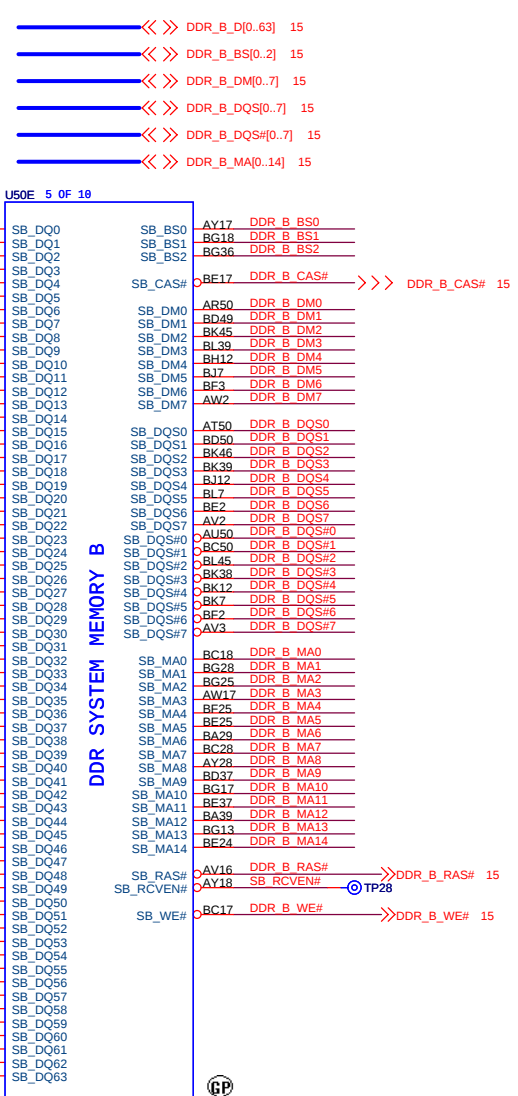
C

B

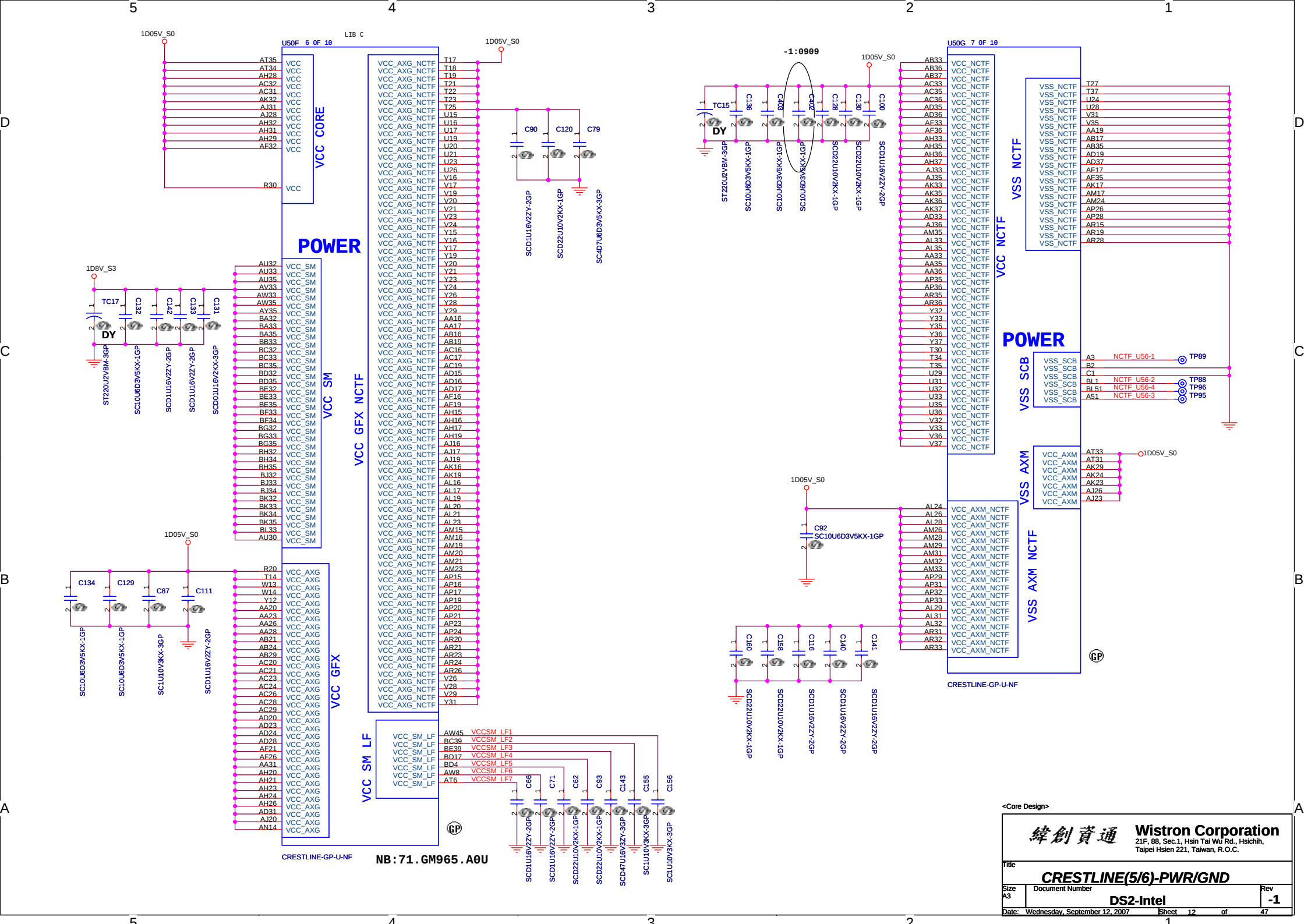
A



CRESTLINE-GP-U-NF
NB: 71.GM965.A0U



CRESTLINE-GP-U-NF
NB: 71.GM965.A0U



U50I 9 OF 10

A13	VSS	AW24
A15	VSS	AW29
A17	VSS	AW32
A24	VSS	AW5
AA21	VSS	AW7
AA24	VSS	AY10
AA29	VSS	AY24
AB20	VSS	AY37
AB23	VSS	AY42
AB26	VSS	AY43
AB28	VSS	AY45
AB31	VSS	AY47
AC10	VSS	AY50
AC13	VSS	B10
AC3	VSS	B20
AC39	VSS	B24
AC43	VSS	B29
AC47	VSS	B30
AD1	VSS	B35
AD21	VSS	B38
AD26	VSS	B43
AD29	VSS	B46
AD3	VSS	B5
AD41	VSS	B8
AD45	VSS	BA1
AD49	VSS	BA17
AD5	VSS	BA18
AD50	VSS	BA2
AD8	VSS	BA24
AE10	VSS	BB12
AE14	VSS	BB25
AE6	VSS	BB40
AE20	VSS	BB44
AE23	VSS	BB49
AE24	VSS	BB8
AE31	VSS	BC16
AG2	VSS	BC24
AG38	VSS	BC25
AG43	VSS	BC36
AG47	VSS	BC40
AG50	VSS	BC51
AH3	VSS	BD13
AH40	VSS	BD2
AH41	VSS	BD28
AH7	VSS	BD45
AH9	VSS	BD48
AJ11	VSS	BD5
AJ13	VSS	BE1
AJ21	VSS	BE19
AJ24	VSS	BE23
AJ29	VSS	BE30
AJ32	VSS	BE42
AJ43	VSS	BE51
AJ45	VSS	BE8
AJ49	VSS	BF12
AK20	VSS	BF16
AK21	VSS	BF36
AK26	VSS	BG19
AK28	VSS	BG2
AK31	VSS	BG24
AK51	VSS	BG29
AL1	VSS	BG39
AM11	VSS	BG48
AM13	VSS	BG5
AM3	VSS	BG51
AM4	VSS	BH17
AM41	VSS	BH30
AM45	VSS	BH44
AN1	VSS	BH46
AN38	VSS	BH8
AN39	VSS	BJ11
AN43	VSS	BJ13
AN5	VSS	BJ38
AN7	VSS	BJ4
AP4	VSS	BJ42
AP48	VSS	BJ46
AP50	VSS	BK15
AR11	VSS	BK17
AR2	VSS	BK25
AR39	VSS	BK29
AR44	VSS	BK36
AR47	VSS	BK40
AR7	VSS	BK44
AT10	VSS	BK6
AT14	VSS	BK8
AT41	VSS	BL11
AT49	VSS	BL13
AU1	VSS	BL19
AU23	VSS	BL22
AU29	VSS	BL37
AU3	VSS	BL47
AU36	VSS	C12
AU49	VSS	C16
AU51	VSS	C19
AV39	VSS	C28
AV48	VSS	C29
AW1	VSS	C33
AW12	VSS	C36
AW16	VSS	C41

CRESTLINE-GP-U-NF
NB: 71 . GM965 . A0U

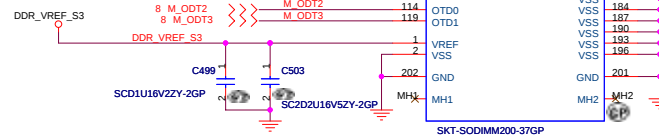
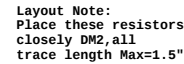
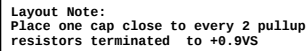
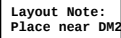
U50J10 OF 10

C46	VSS	W11
C50	VSS	W39
C7	VSS	W43
D13	VSS	W47
D24	VSS	W5
D3	VSS	W7
D324	VSS	Y13
D39	VSS	Y2
D45	VSS	Y41
D49	VSS	Y45
E10	VSS	Y49
E16	VSS	Y5
E24	VSS	Y50
E28	VSS	Y11
E32	VSS	P29
E47	VSS	T29
F19	VSS	T31
F36	VSS	T33
F4	VSS	R28
F40	VSS	
F50	VSS	
G1	VSS	
G13	VSS	
G16	VSS	AA32
G19	VSS	AB32
G24	VSS	AD32
G28	VSS	AE28
G29	VSS	AE29
G33	VSS	AT27
G42	VSS	AV25
G45	VSS	H50
G48	VSS	
GB44	VSS	
H24	VSS	
H28	VSS	
H4	VSS	
H45	VSS	
J11	VSS	
J16	VSS	
J2	VSS	
J24	VSS	
J28	VSS	
J33	VSS	
J35	VSS	
J39	VSS	
K12	VSS	
K47	VSS	
K8	VSS	
L1	VSS	
L17	VSS	
L20	VSS	
L24	VSS	
L28	VSS	
L3	VSS	
L33	VSS	
L49	VSS	
M28	VSS	
M42	VSS	
M46	VSS	
M49	VSS	
M5	VSS	
M50	VSS	
M9	VSS	
N11	VSS	
N14	VSS	
N17	VSS	
N29	VSS	
N32	VSS	
N36	VSS	
N39	VSS	
N44	VSS	
N49	VSS	
N7	VSS	
P19	VSS	
P2	VSS	
P23	VSS	
P3	VSS	
P50	VSS	
R49	VSS	
T39	VSS	
T43	VSS	
T47	VSS	
U41	VSS	
U46	VSS	
U50	VSS	
V2	VSS	
V3	VSS	

CRESTLINE-GP-U-NF
NB: 71 . GM965 . A0U

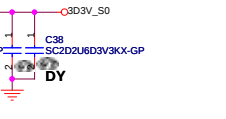
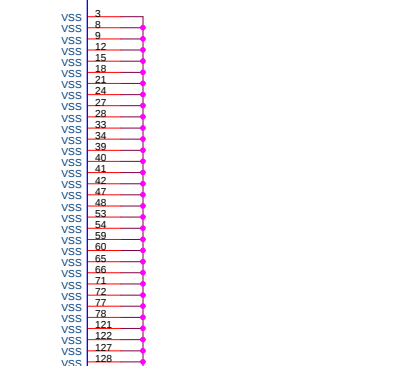
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Size		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
A3		Document Number	
Date: Wednesday, September 12, 2007		Sheet 13 of 47	
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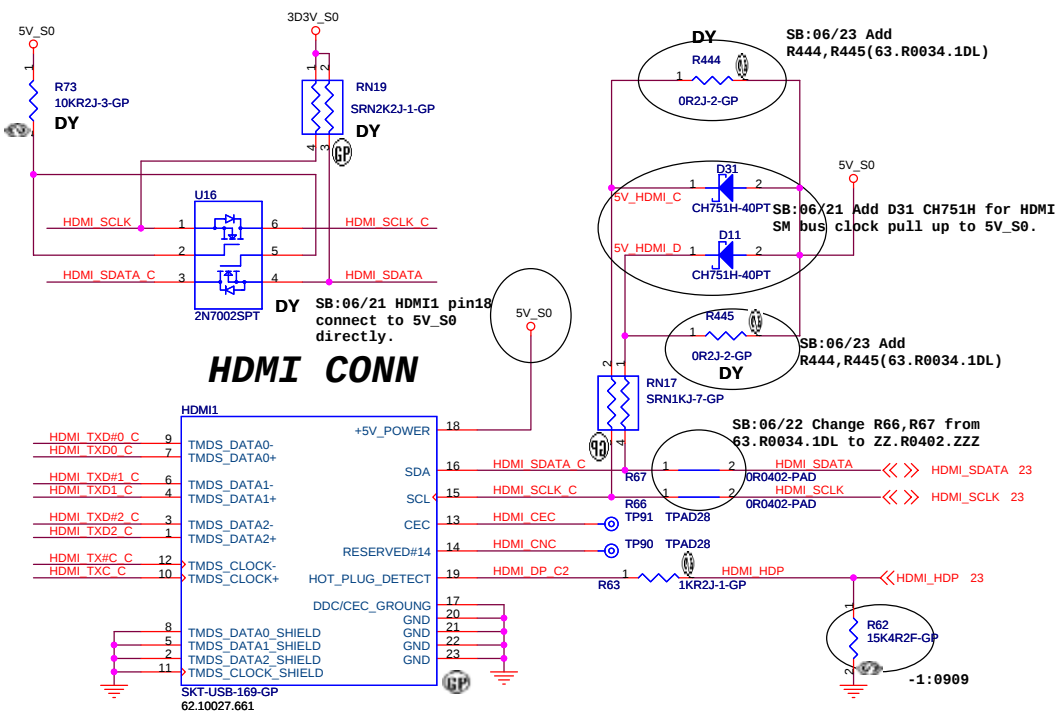
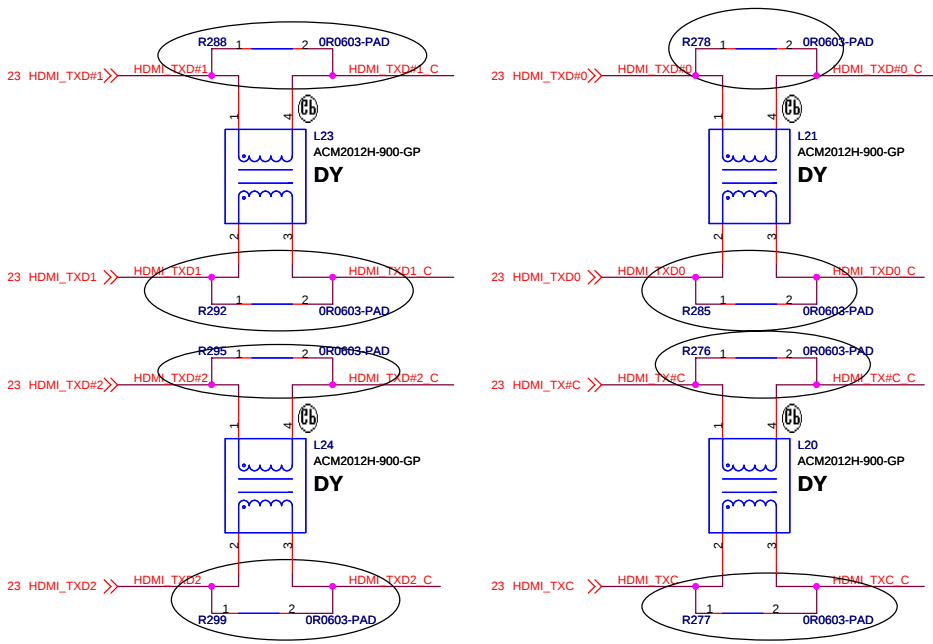


DDR B DQS#0	11	DQS0#
DDR B DQS#1	29	DQS1#
DDR B DQS#2	49	DQS2#
DDR B DQS#3	68	DQS3#
DDR B DQS#4	129	DQS4#
DDR B DQS#5	146	DQS5#
DDR B DQS#6	167	DQS6#
DDR B DQS#7	186	DQS7#
DDR B DQSO	13	DQSO
DDR B DQS1	31	DQS1
DDR B DQS2	51	DQS2
DDR B DQS3	70	DQS3
DDR B DQS4	131	DQS4
DDR B DQS5	148	DQS5
DDR B DQS6	169	DQS6
DDR B DQS7	188	DQS7

VSS	3
VSS	8
VSS	9
VSS	12
VSS	15
VSS	18
VSS	21
VSS	24
VSS	27
VSS	28
VSS	33
VSS	34
VSS	38
VSS	40
VSS	41
VSS	42
VSS	47
VSS	48
VSS	53
VSS	54
VSS	59
VSS	60
VSS	65
VSS	66
VSS	71
VSS	72
VSS	77
VSS	78
VSS	121
VSS	122
VSS	127
VSS	128

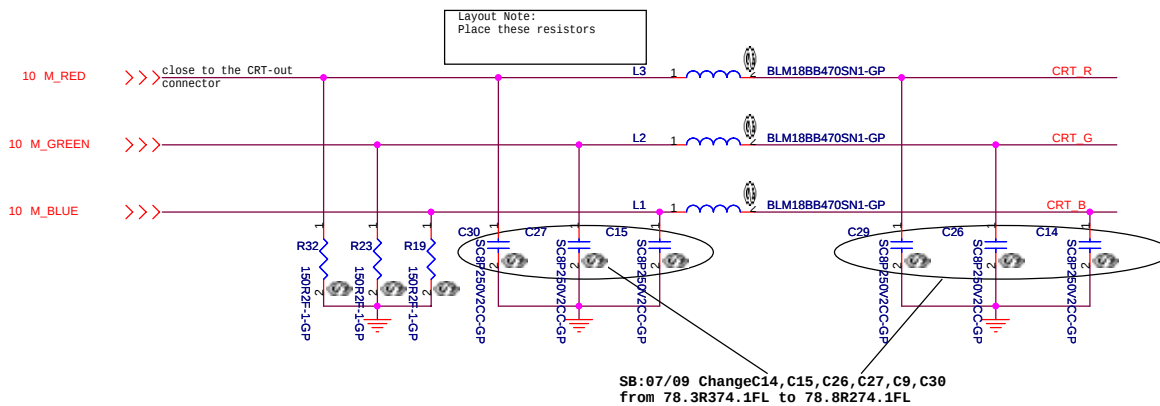


HDMI I/F & CONNECTOR

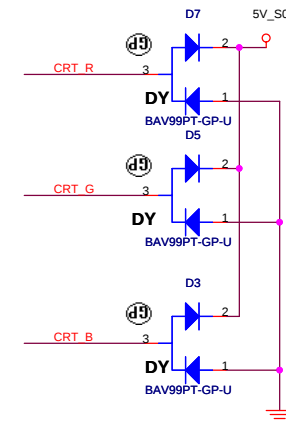
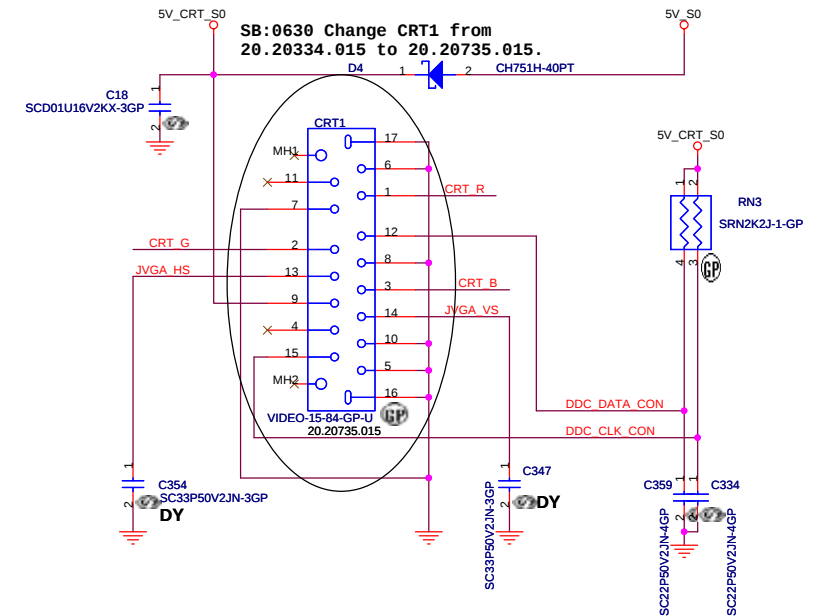
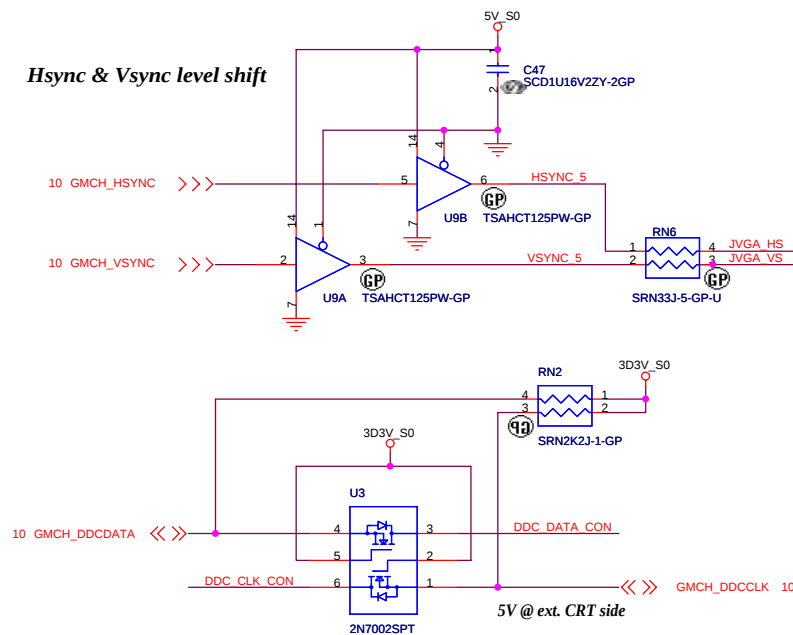


TV OUT CONN (Optional) Move to Right I/O Board

CRT I/F & CONNECTOR



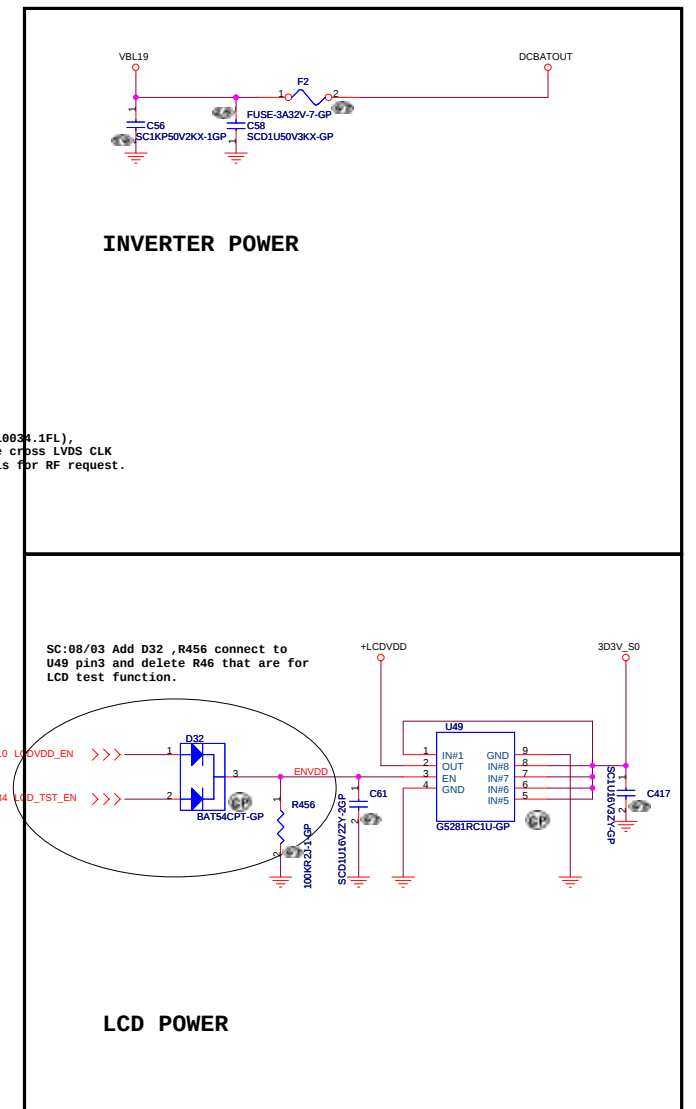
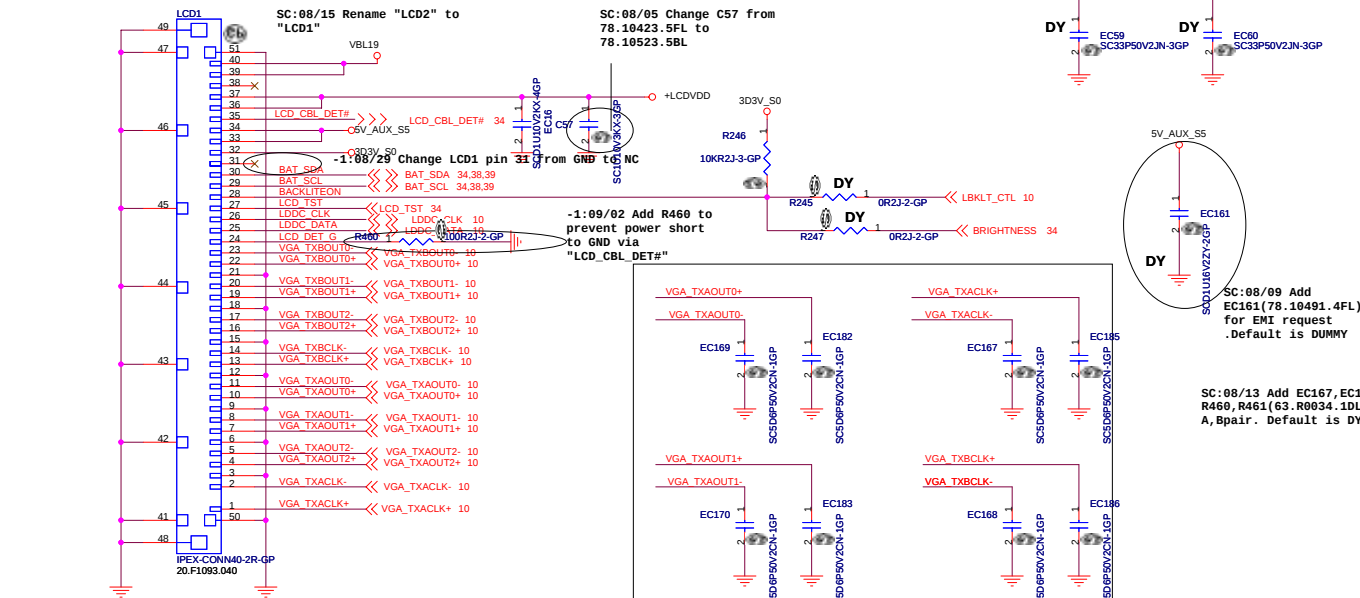
Hsync & Vsync level shift



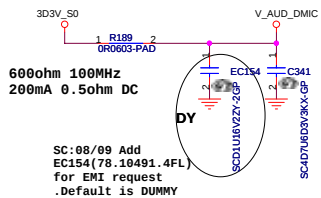
<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Connector			
Size A3	Document Number DS2-Intel		Rev -1
Date:	Wednesday, September 12, 2007	Sheet 17 of 47	

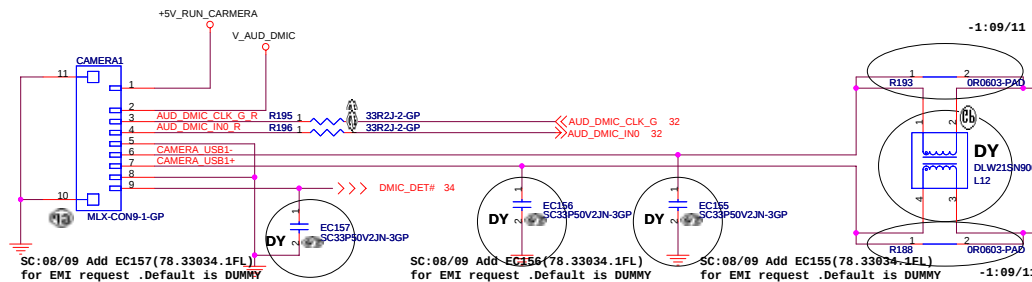
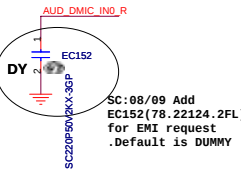
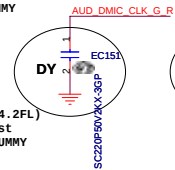
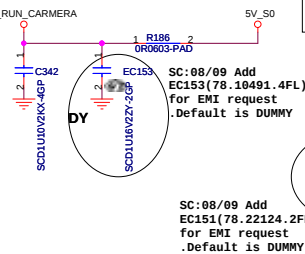
SC:08/09 Add LCD2 (20.F1093.040) ,please check LCD1 and LCD 2 layout overlap possibility.



Mic Power



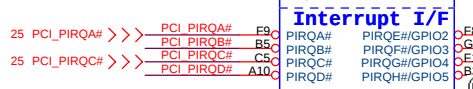
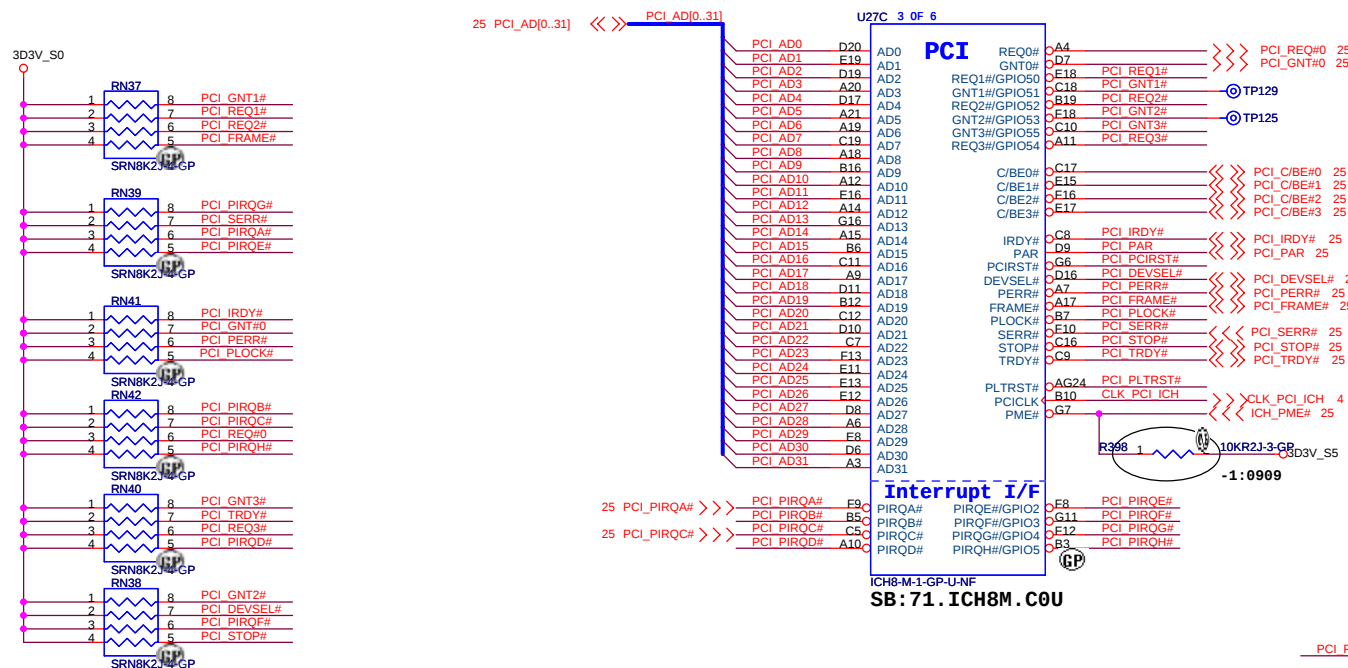
CAMERA Power



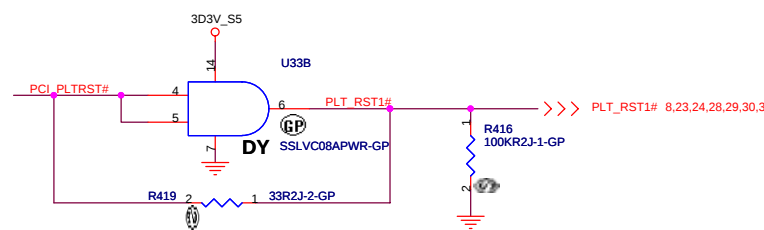
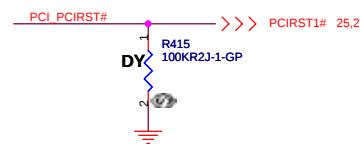
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

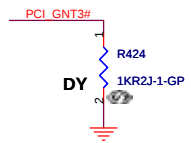
LCD/Inverter Connector		
Size	Document Number	Rev
Custom	DS2-Intel	-1
Date: Wednesday, September 12, 2007 Sheet 18 of 47		



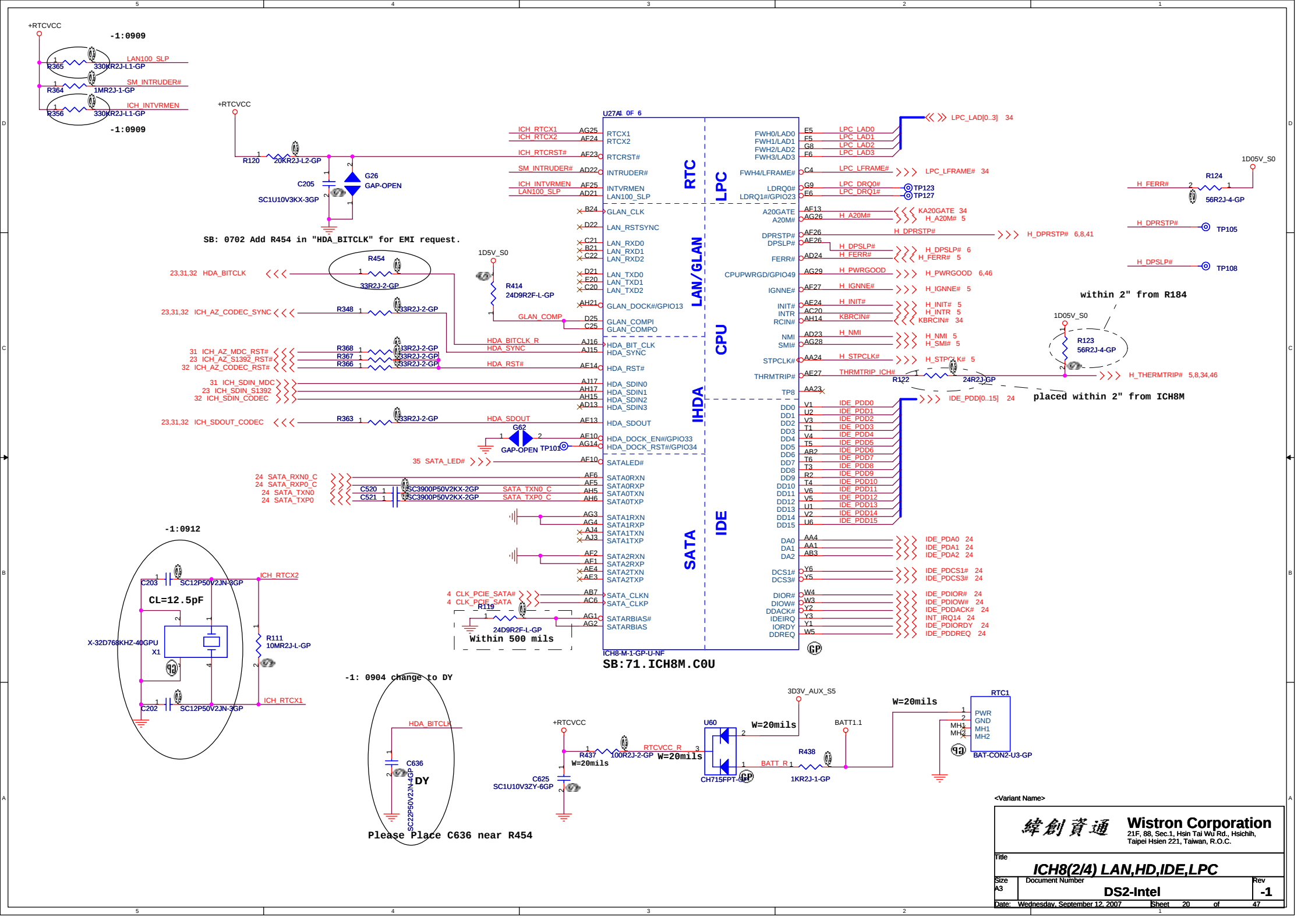
ICH8-M-1-GP-U-NF
SB: 71. ICH8M.C0U

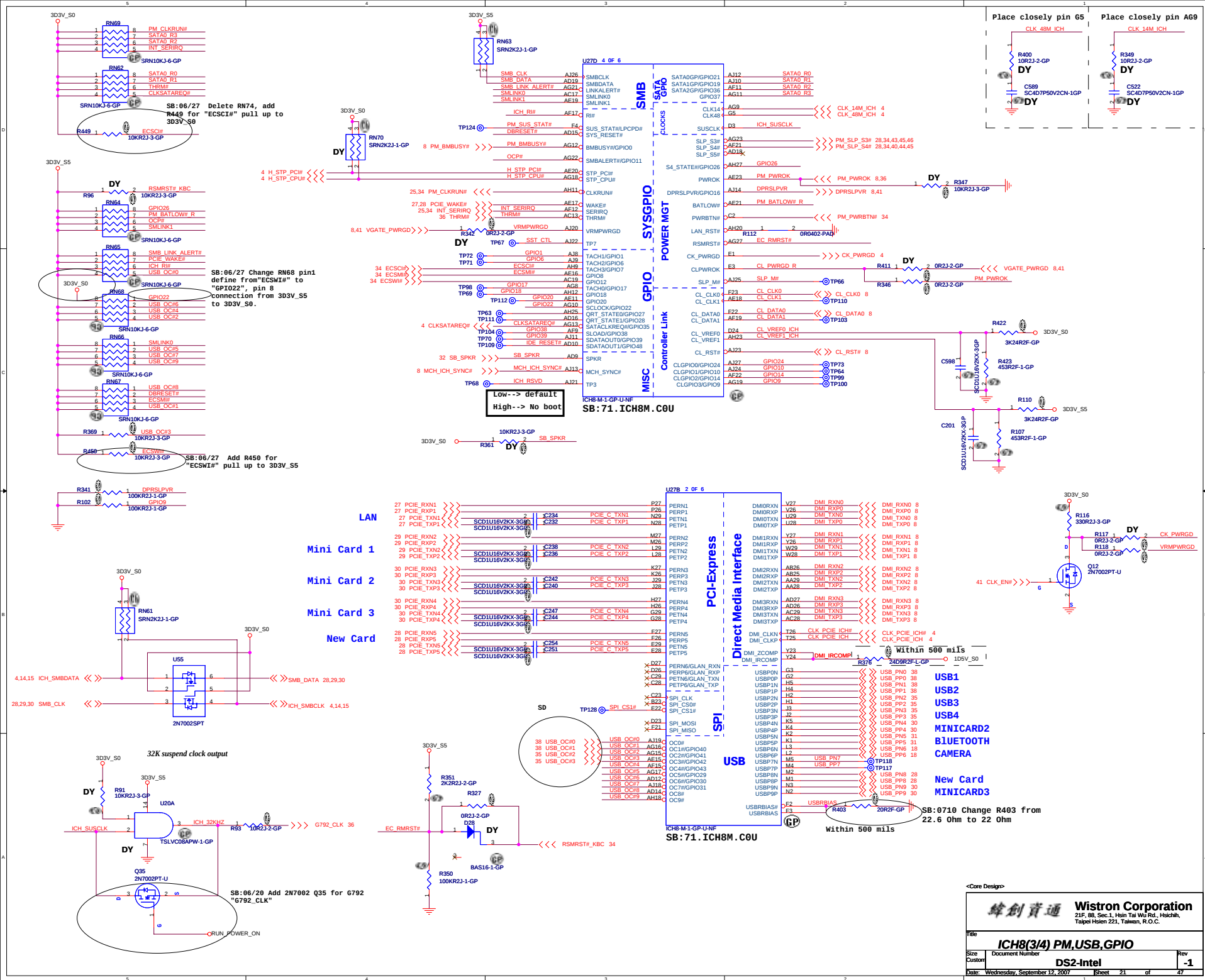


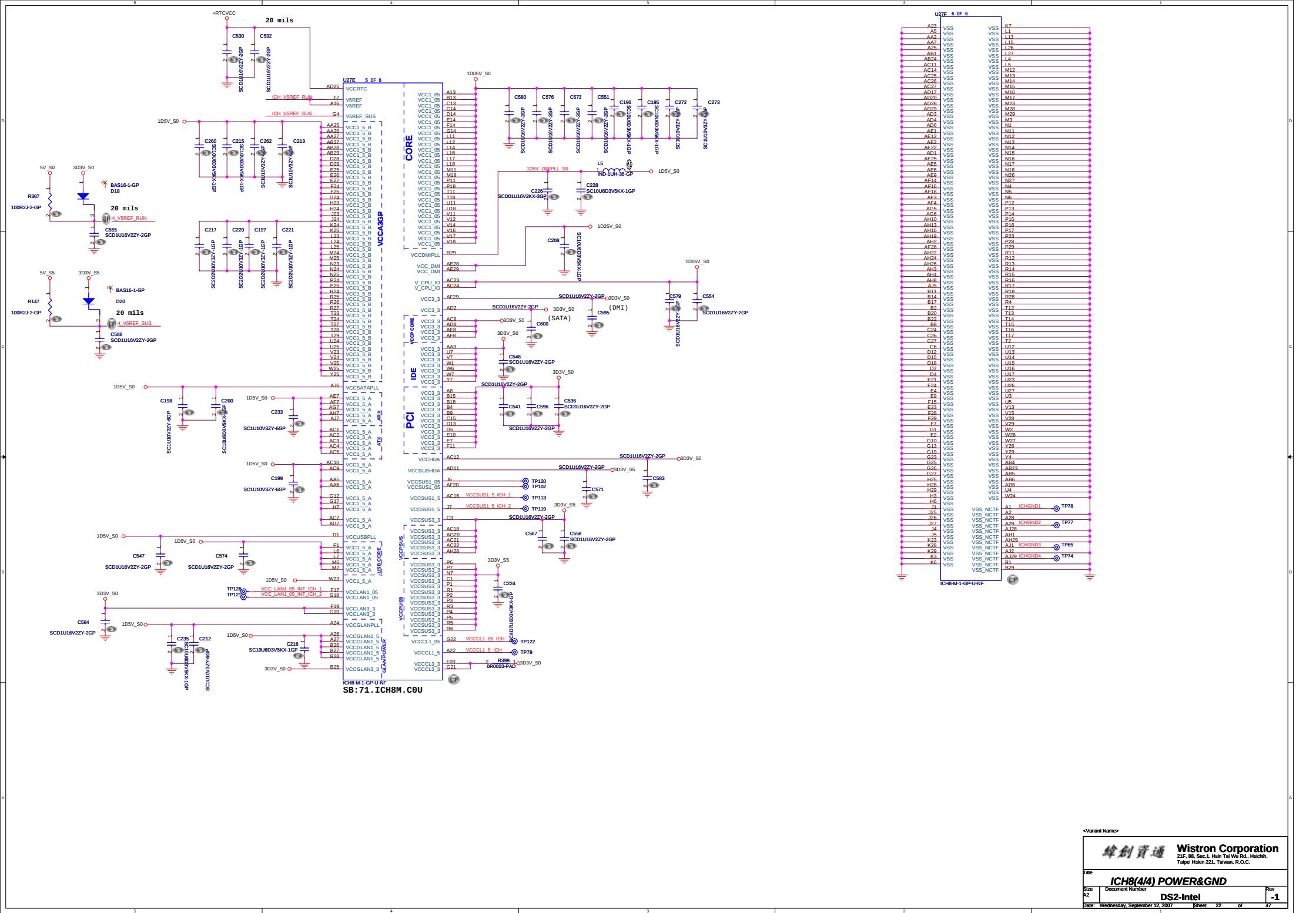
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



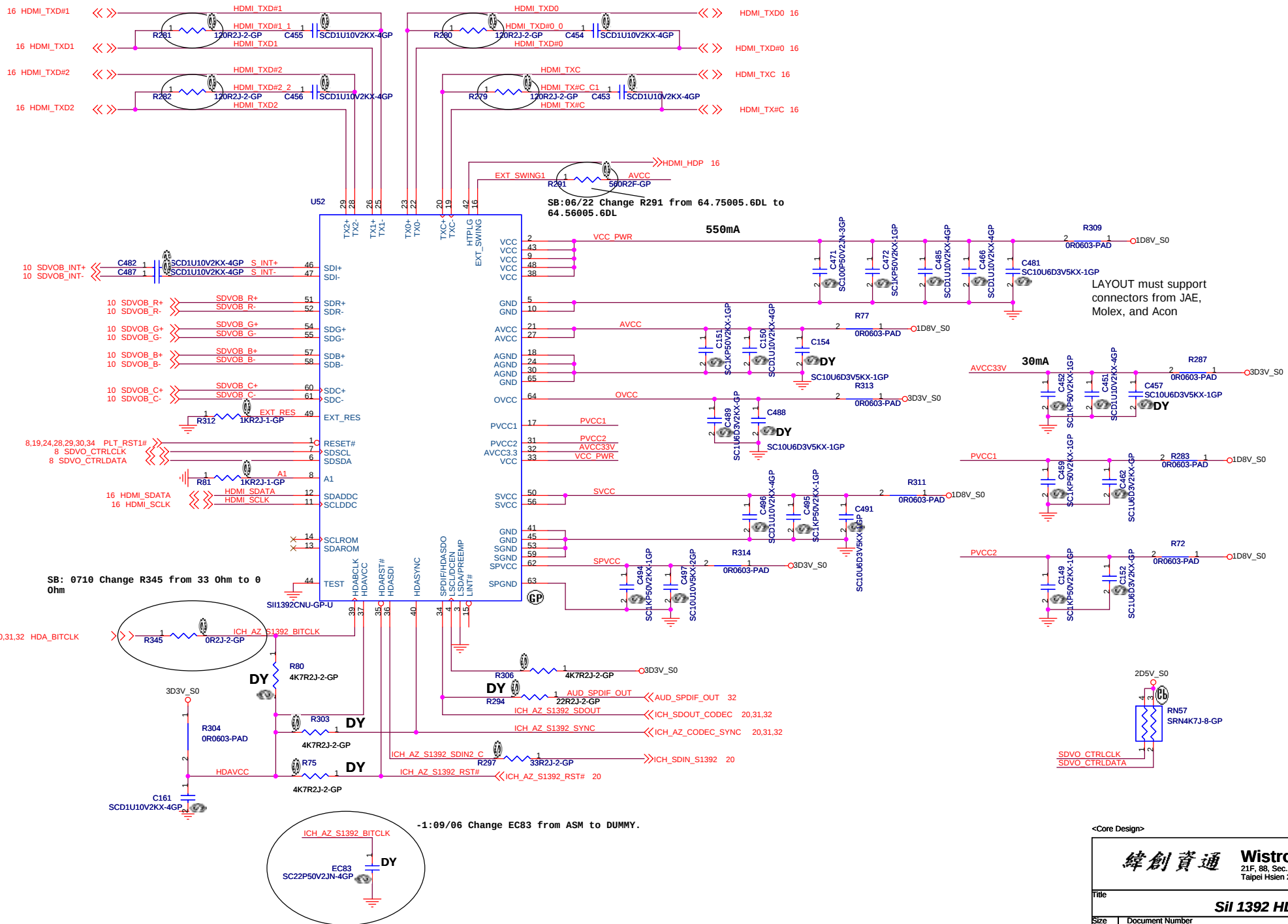
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *







SB:06/22 Change R279,R280,R281,R282 from 63.30134.1DL
to 63.12134.1DL

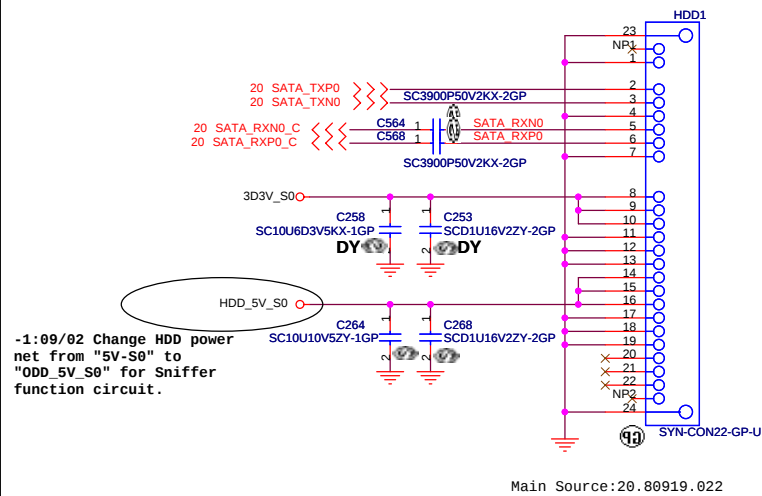


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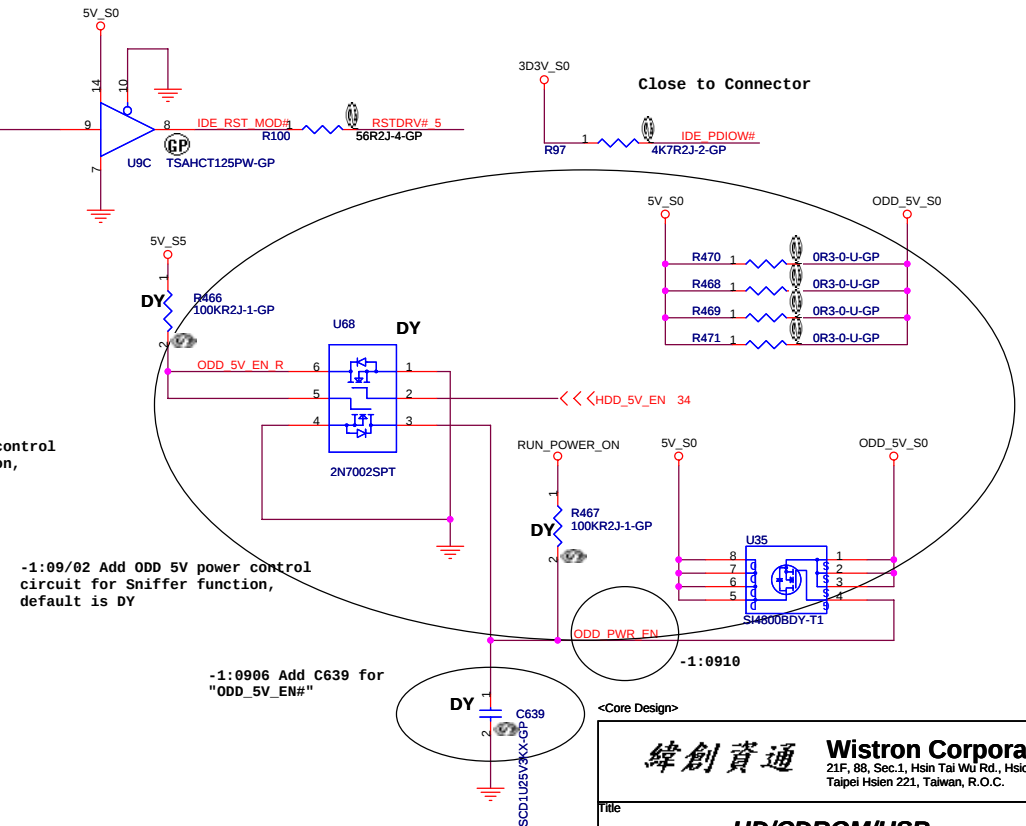
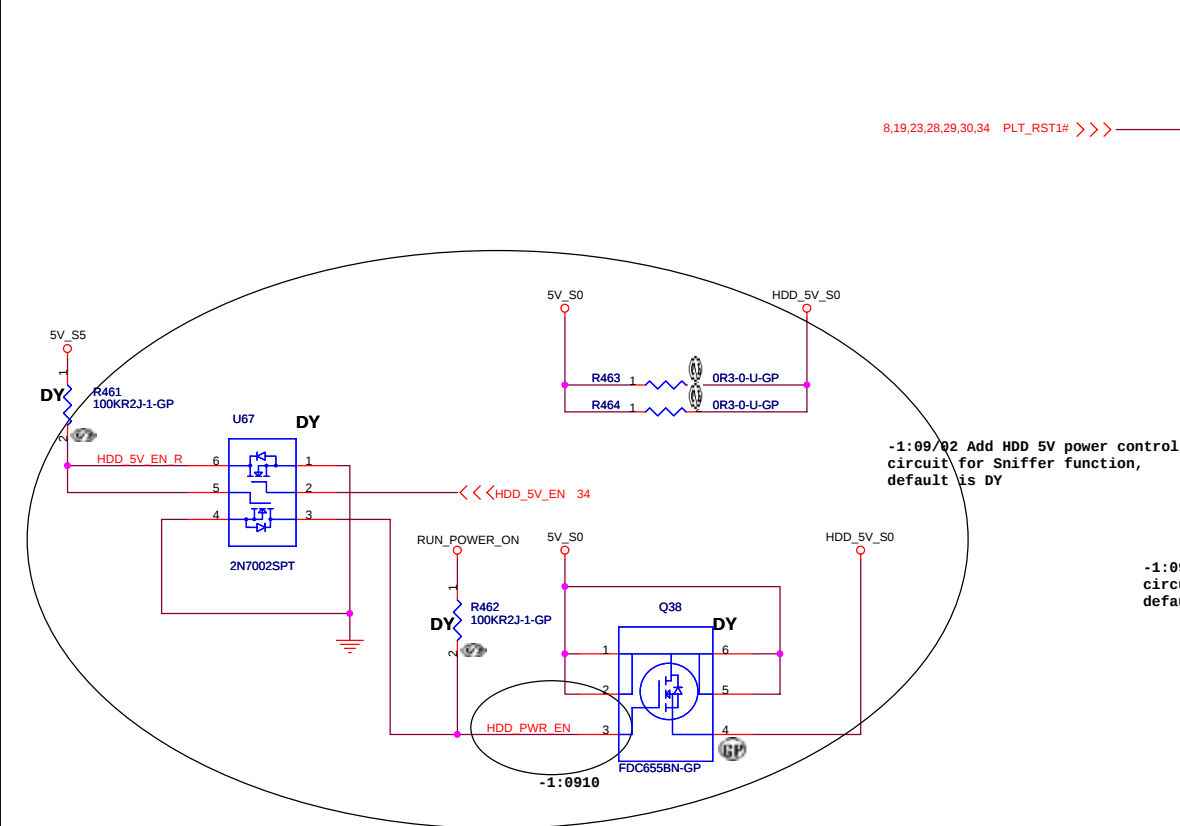
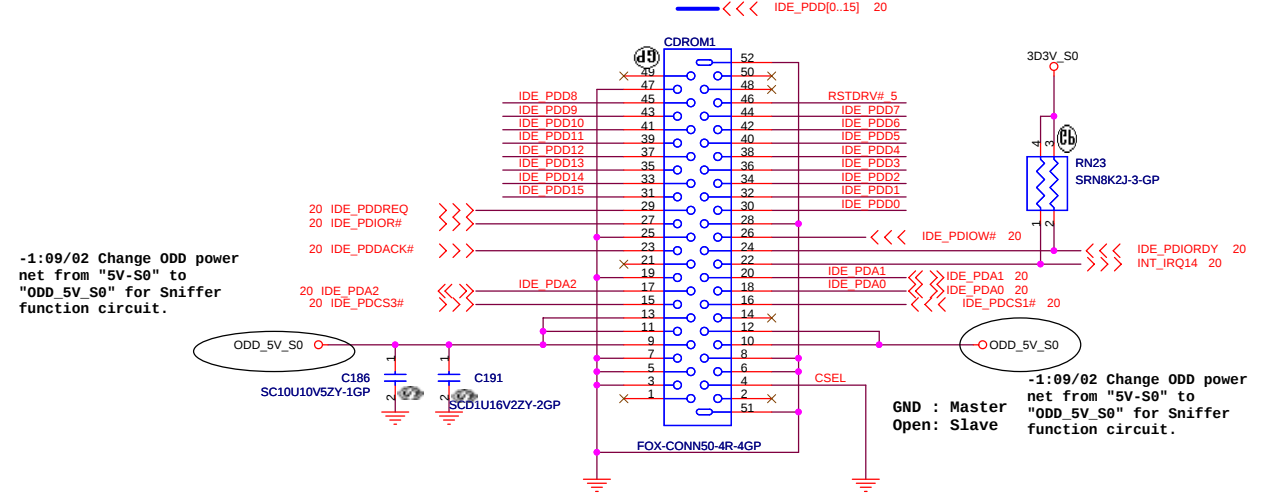
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

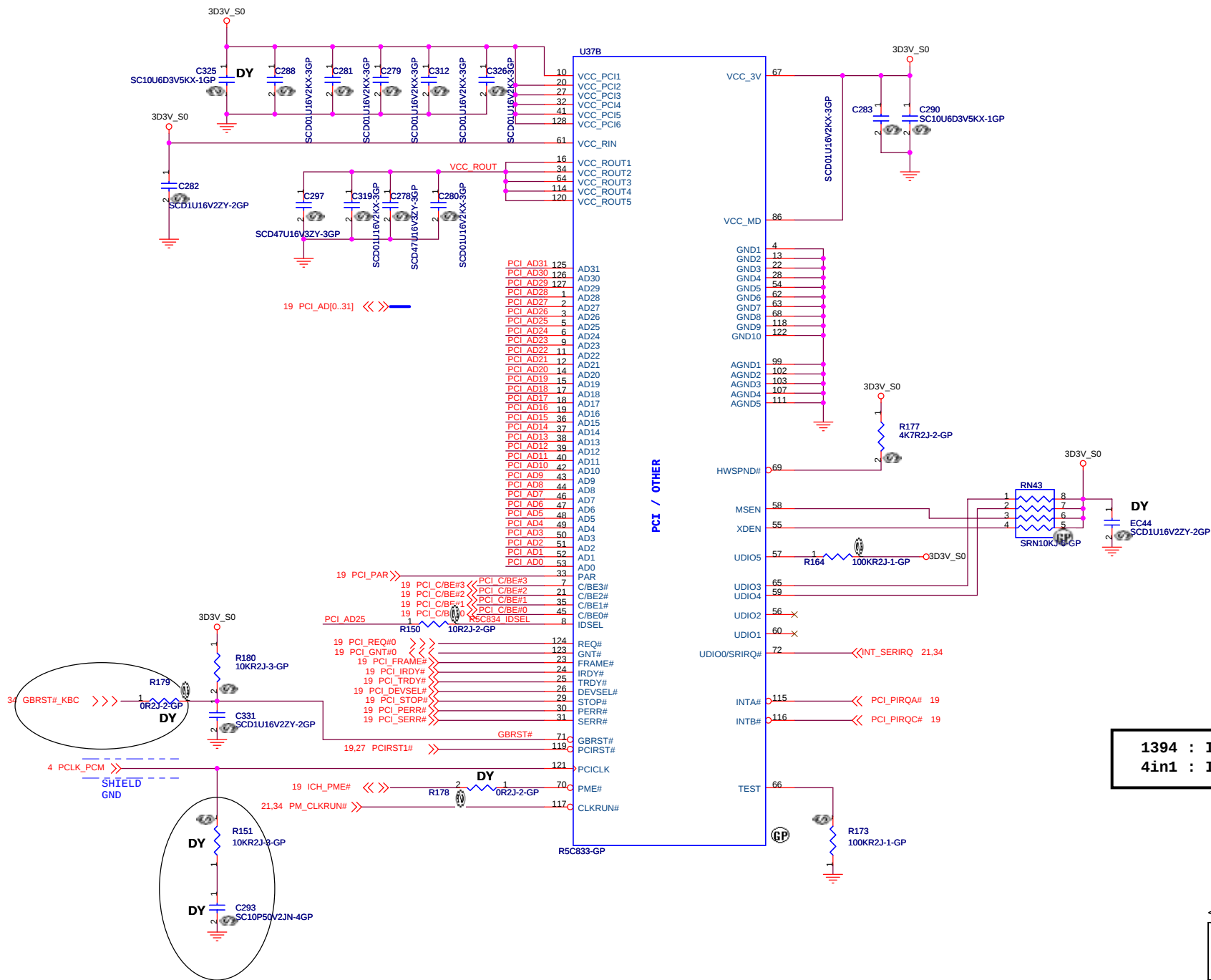
Title			
Si1 1392 HDMI			
Size A3	Document Number		Rev
	DS2-Intel		-1
Date: Wednesday, September 12, 2007	Sheet	23	of 47

SATA HD Connector



CD-ROM Connector





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

	Title
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R5C833/PCISize
18

Document Number

Rev

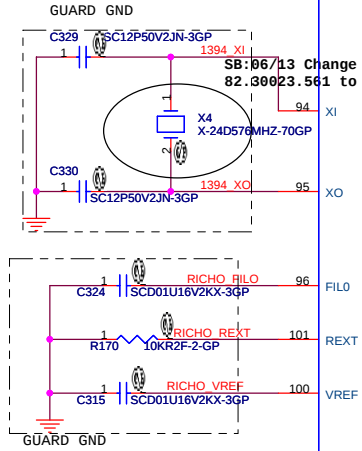
DS2-Intel

-1

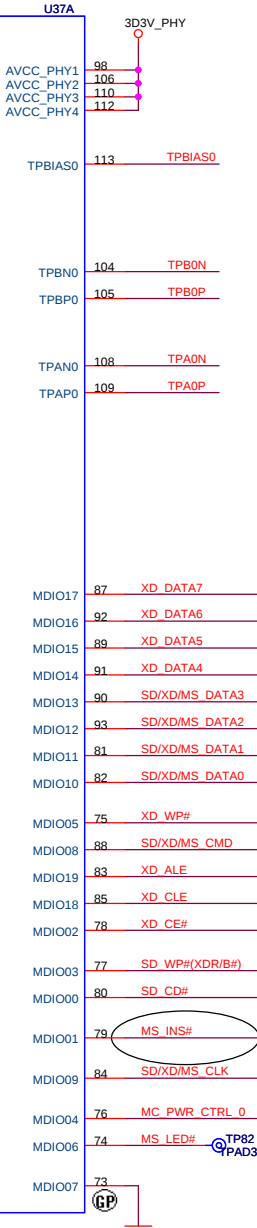
Date: Wednesday, September 12, 2007

Sheet 25 of

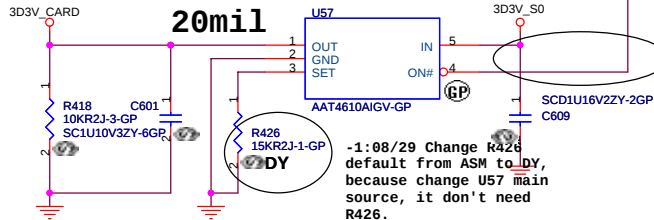
47



IEEE1394/SD

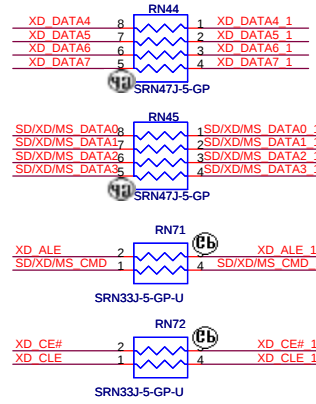
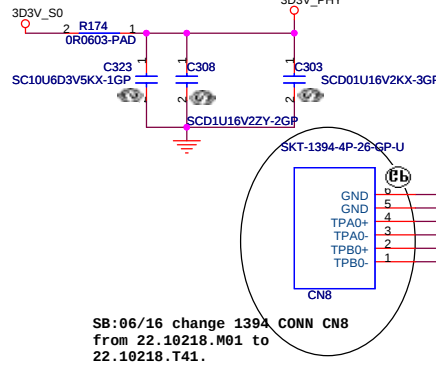


For SD Card Power

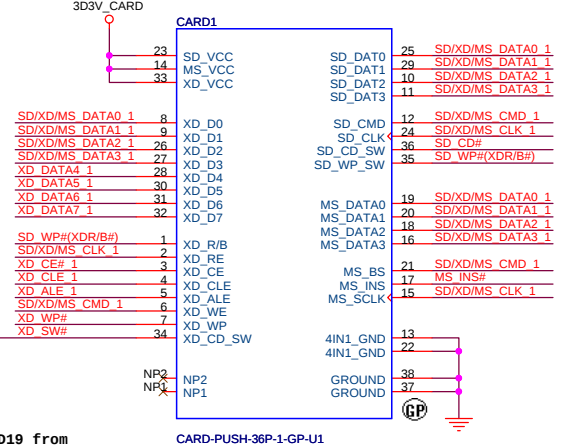
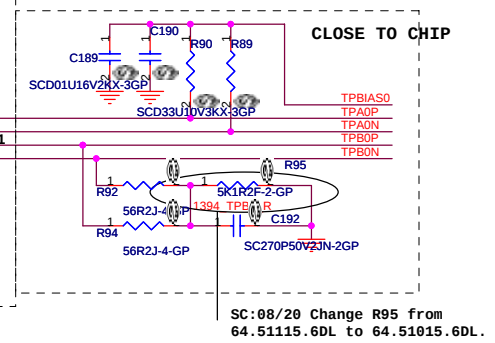
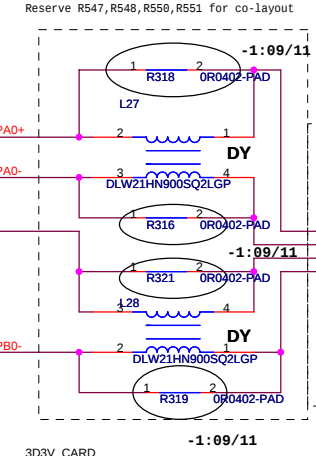
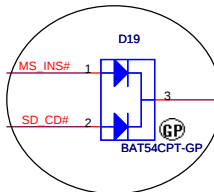


SB:06/20 Remove R427 and change U57 pin4 connect to "MC_PWR_CTRL_0"

AAT4610AIGV	R426
RT9711DPBG	15K
G5240D2T1U	DY

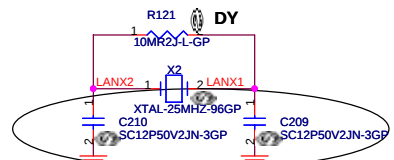


SB:06/20 Remove U35,R148 and change D19 from 83.R0304.A6H to 83.R2003.E81.

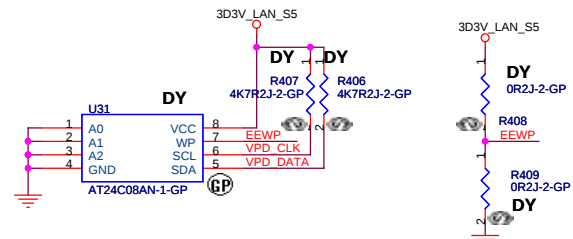


	R394	R354	R357	R362	R372	R377	C528	C544
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01u
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY

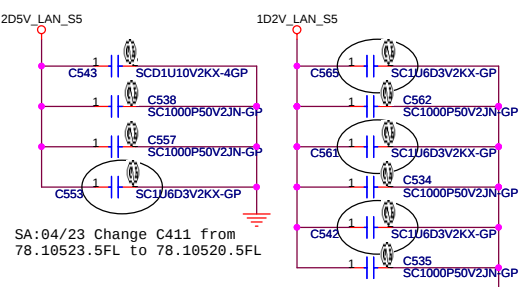
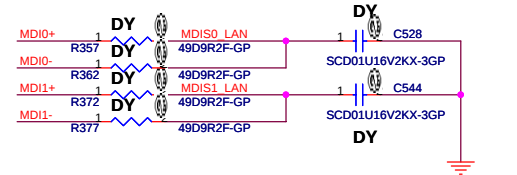
Note:Default is 88E8040



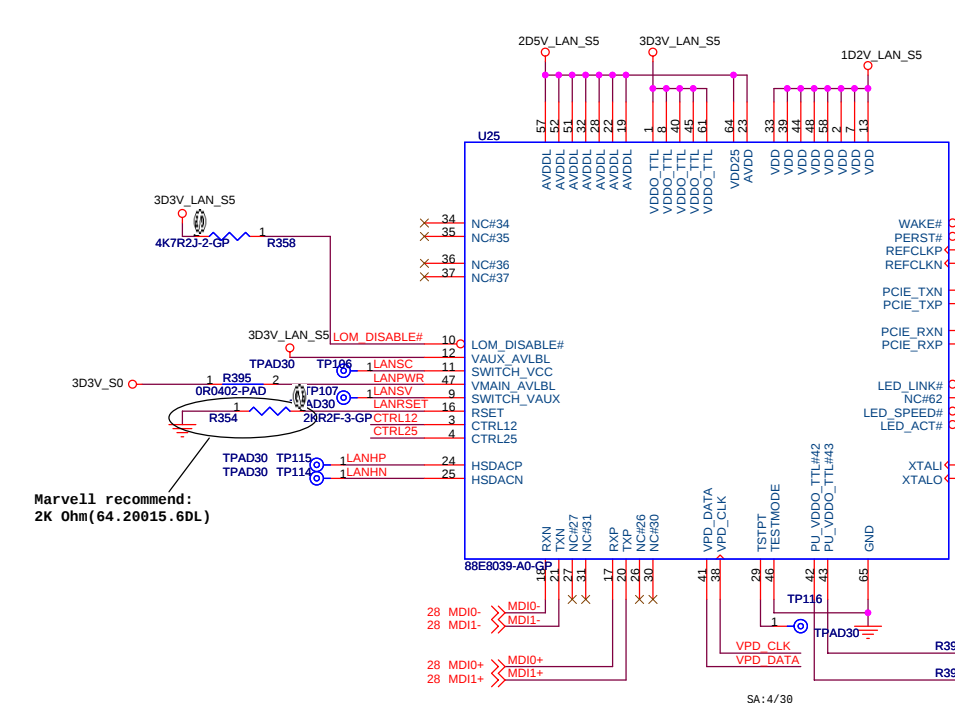
SB:06/13 Change C209,C210 from 27P to 12P



Pull up for AT24C08 another pull low

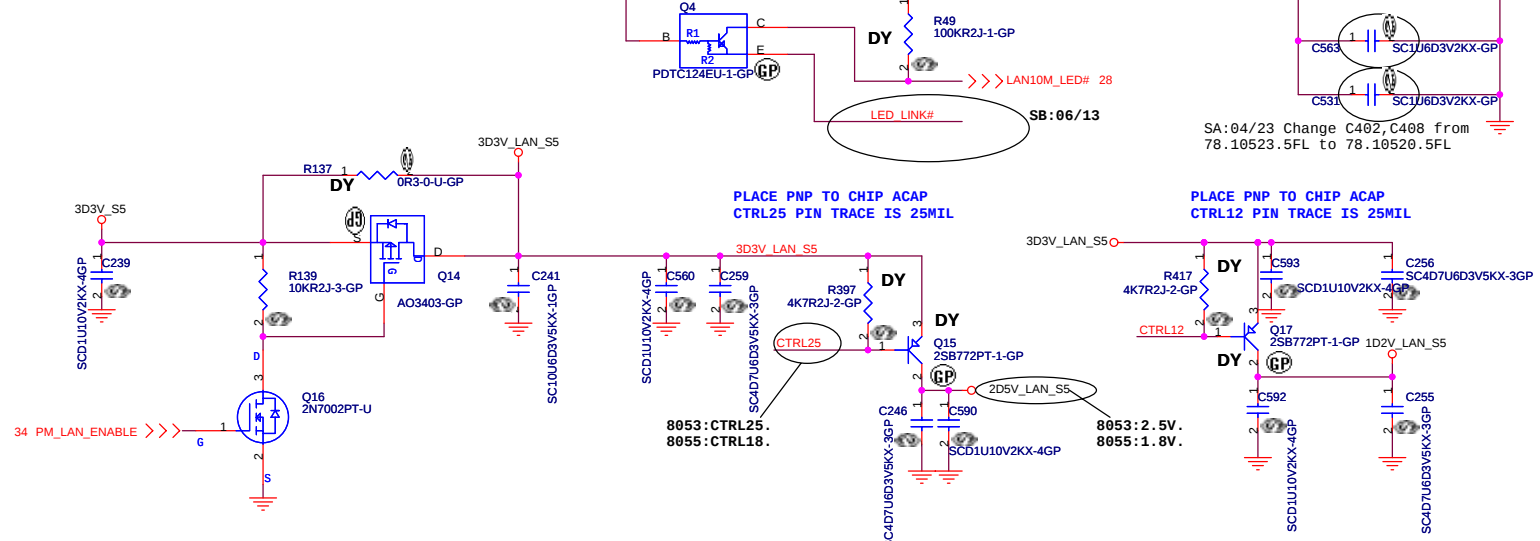


SA:04/23 Change C411 from 78.10523.5FL to 78.10520.5FL



Marvell recommend:
2K Ohm(64.20015.6DL)

	R397	Q15	R417	Q17
88E8039	4K7	2SB772PT	4K7	2SB772PT
88E8040	DY	DY	DY	DY



PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL

PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL

<Core Design>

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Title: **LAN MARVELL**

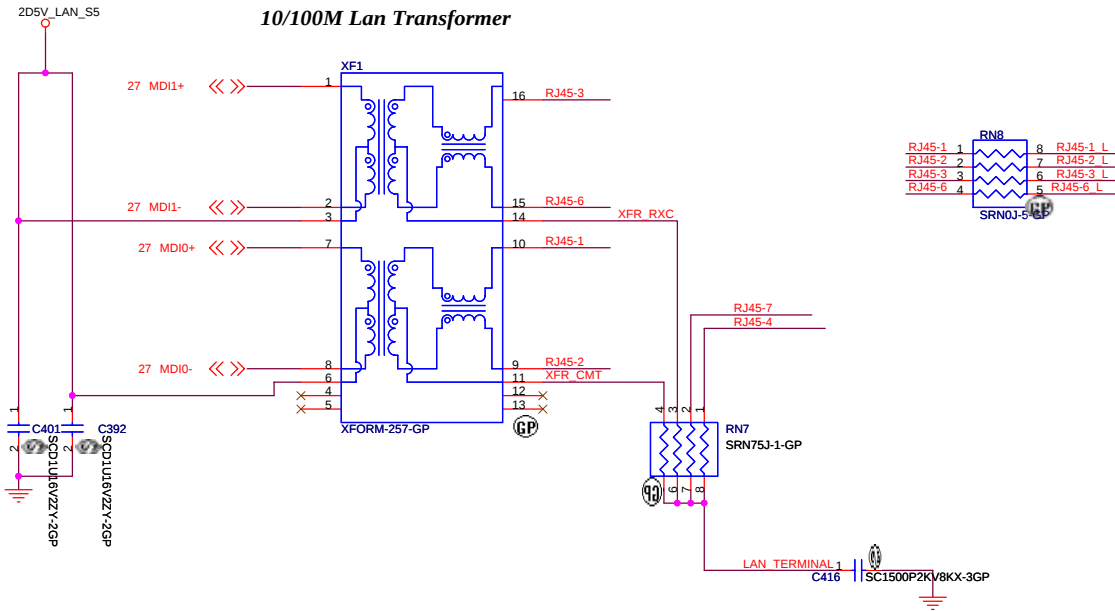
Size A3 Document Number: **DS2-Intel**

Date: Wednesday, September 12, 2007 Sheet 27 of 47

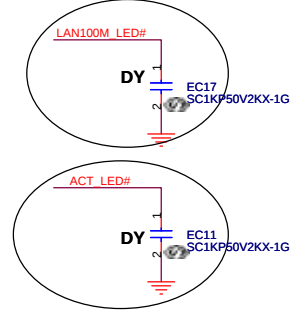
Rev: **-1**

RJ45 Connector

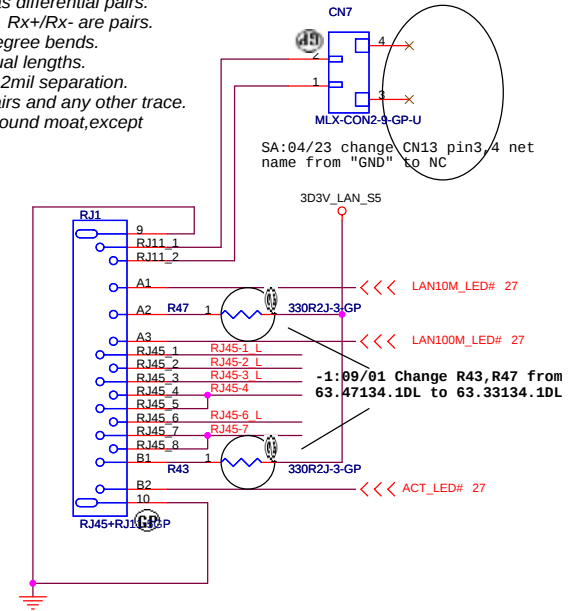
10/100M Lan Transformer



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

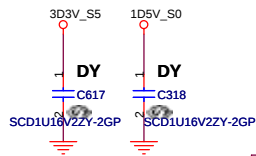


Green : Link up
Blinking : TX/RX activity

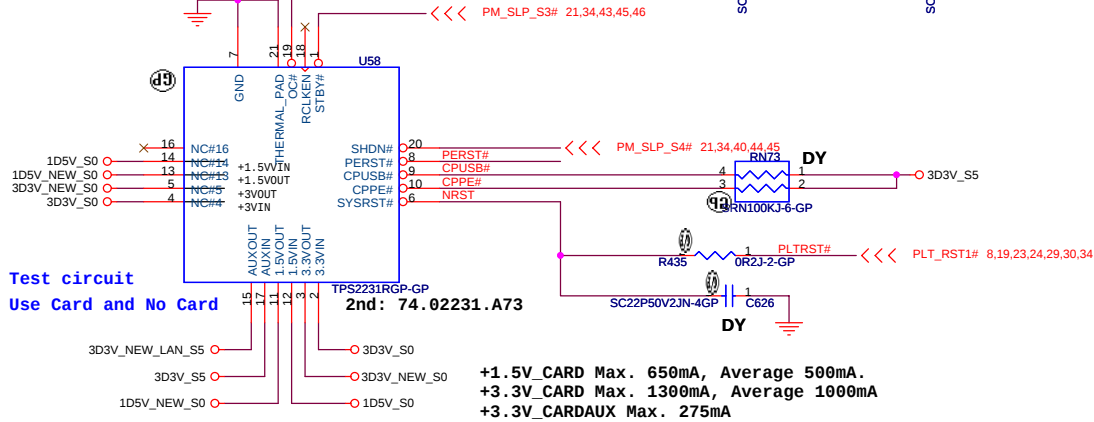
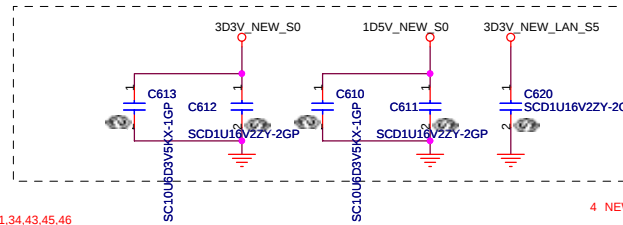


NEWCARD Connector

Place them Near to Chip

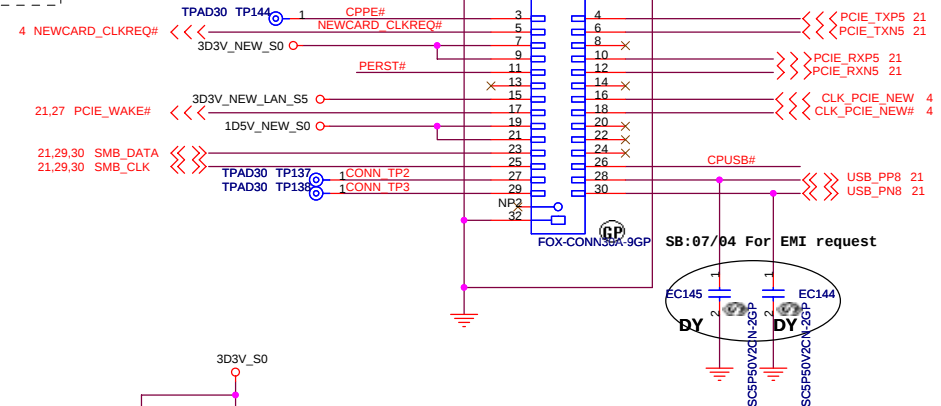


Place them Near to Connector



Test circuit
Use Card and No Card

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

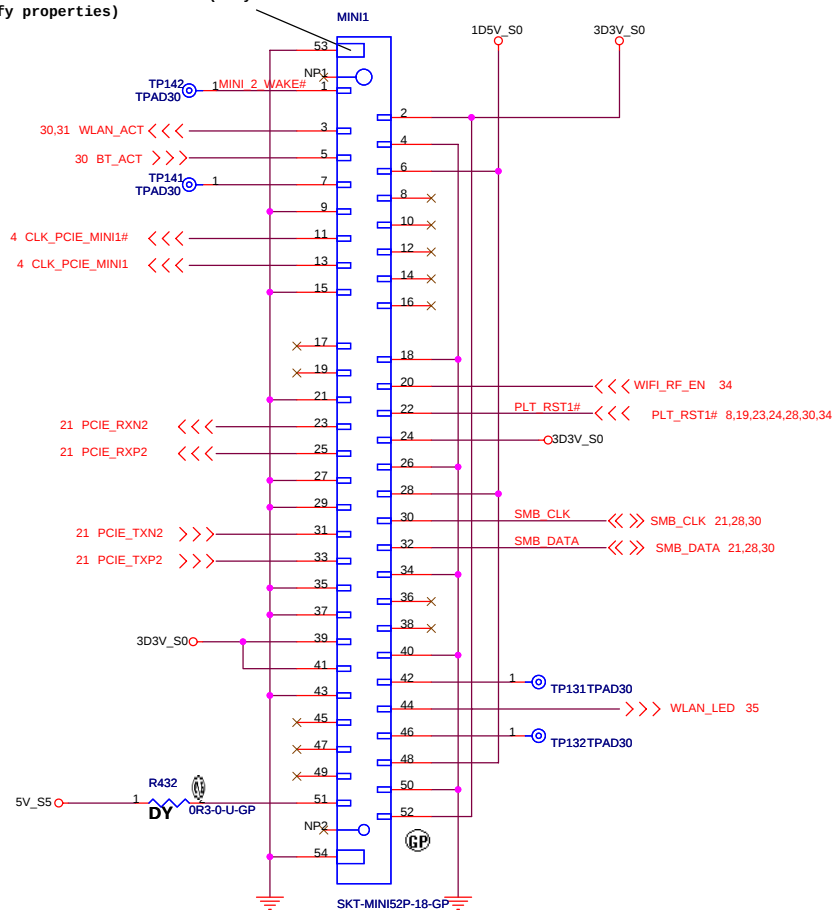


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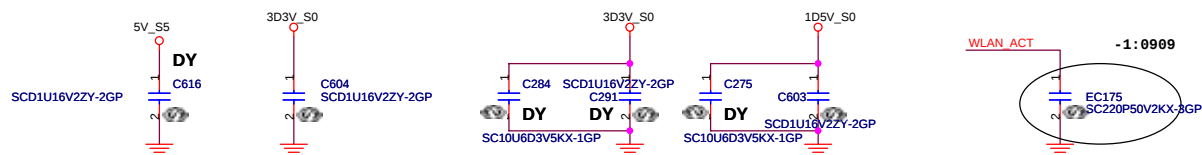
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Title	
Size A3	
Document Number	
Date: Wednesday, September 12, 2007	
Sheet 26 of 47	
LAN connector/NEW CARD/SIM DS2-Intel Rev -1	

Mini Card Connector 1(802.11a/b/g)

SB:06/22 Change MINI1,2,3 slot from
62.10043.431 to 62.10043.551(only
modify properties)



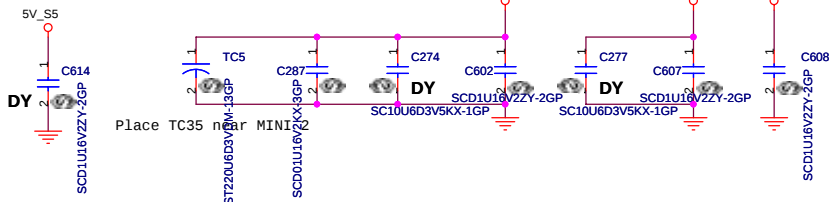
Main Source:62.10043.431
2nd Source: 20.F0992.052



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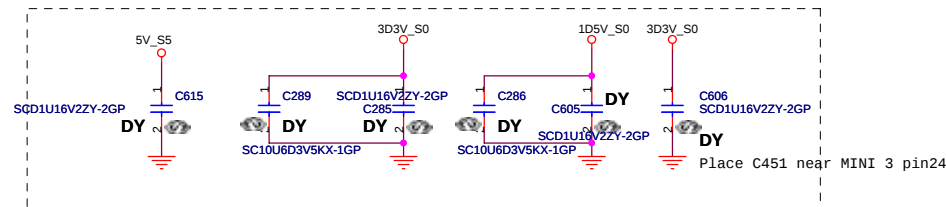
Title		Wistron Corporation	
Size		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
A3		MINI CARD CONN 1	
Date: Wednesday, September 12, 2007		Sheet 29 of 47	
Document Number		DS2-Intel	
Rev		-1	

SB:06/22 Change MINI1,2,3 slot from
62.10043.431 to 62.10043.551(only
modify properties)



Main Source:62.10043.431
2nd Source: 20.F0992.052

SB:06/22 Change MINI1,2,3 slot from
62.10043.431 to 62.10043.551(only
modify properties)



緯創資通

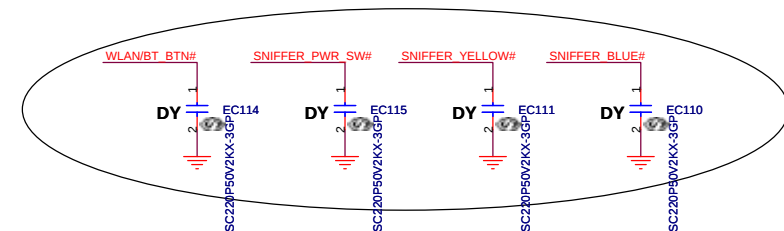
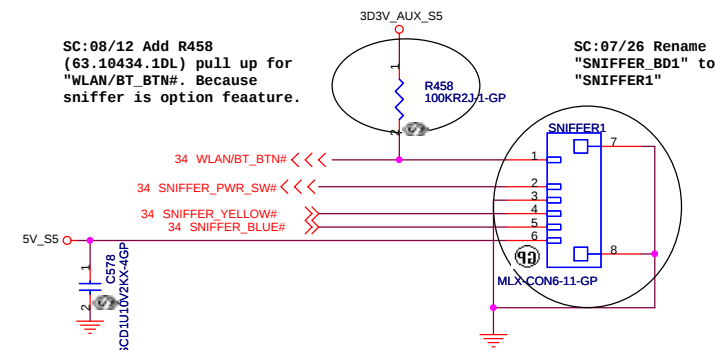
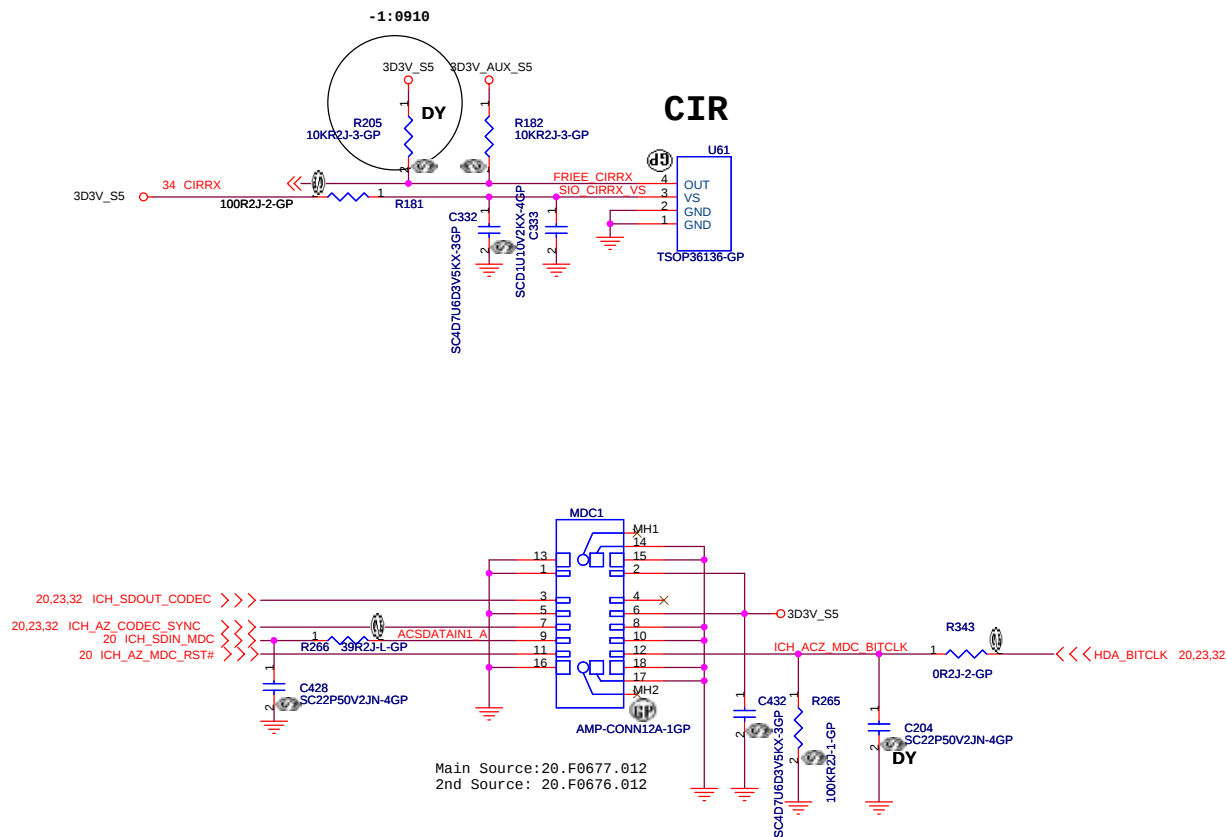
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

MINI CARD CONN 2 & 3

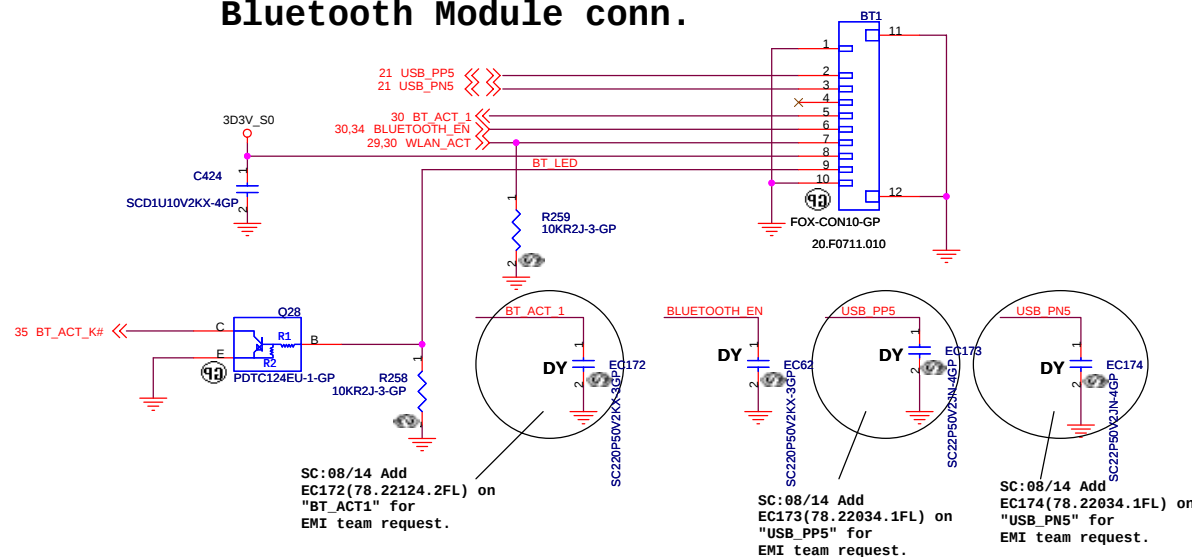
DS2-Intel

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Rev	1
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Bluetooth Module conn.

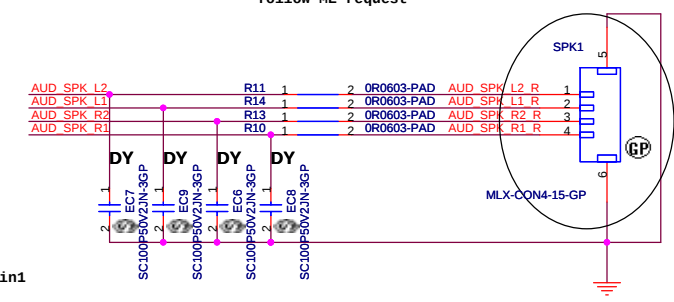


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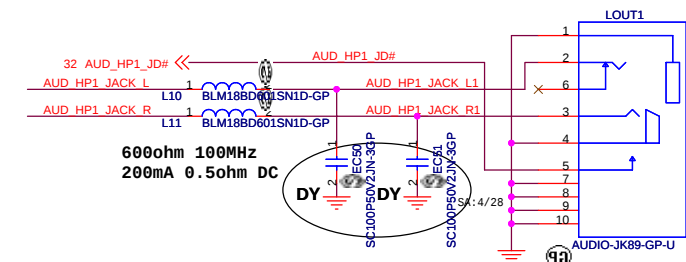
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MDC&RJ11 CONN			
Size	Document Number	Rev	
A3		DS2-Intel -1	
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Speaker

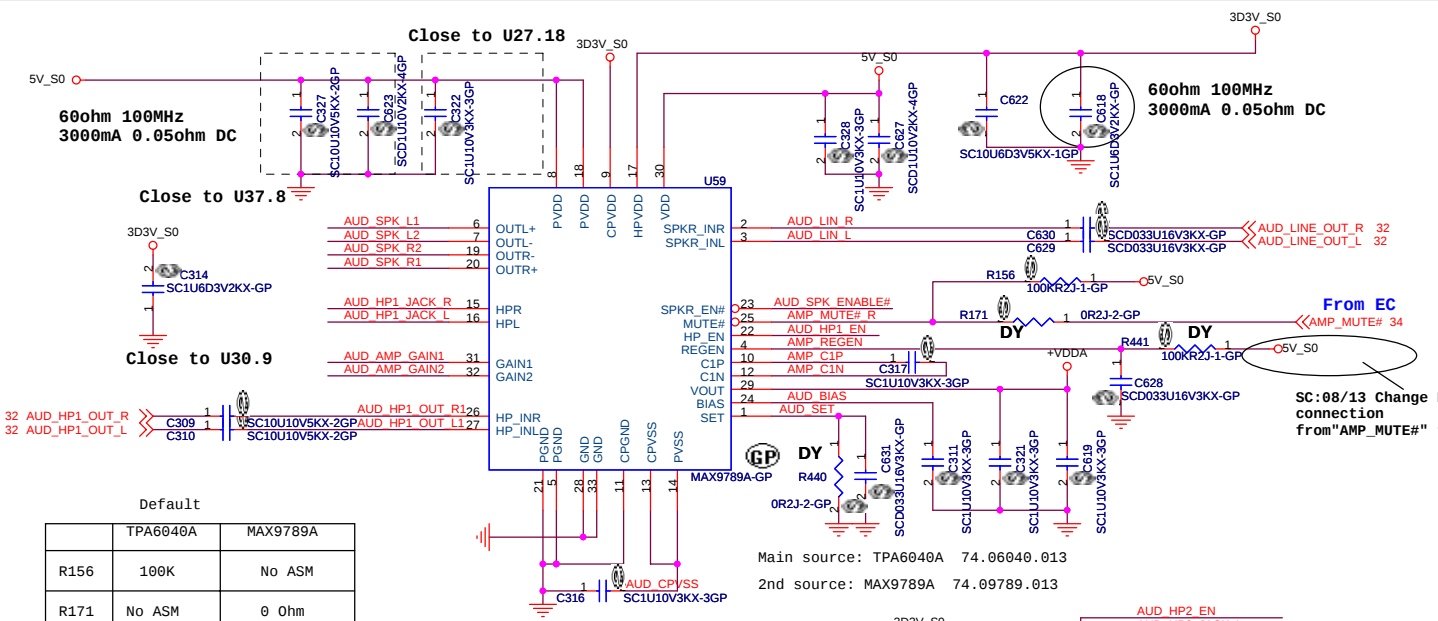
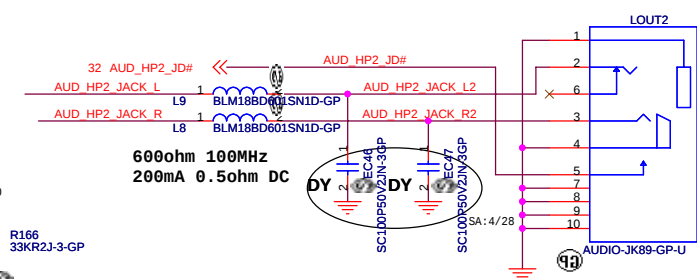
SC:08/11 Change SPK1 pin define that follow ME request



LINE1 OUT



LINE2 OUT



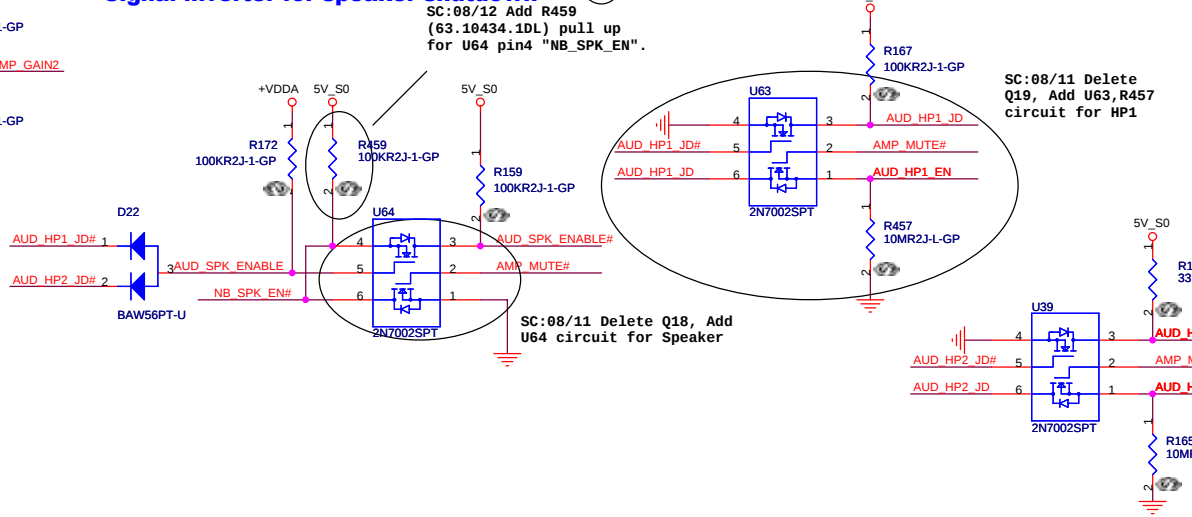
Default

	TPA6040A	MAX9789A
R156	100K	No ASM
R171	No ASM	0 Ohm
R440	No ASM	0 Ohm
R441	No ASM	100K
C631	0.33uF	No ASM
C628	0.33uF	No ASM

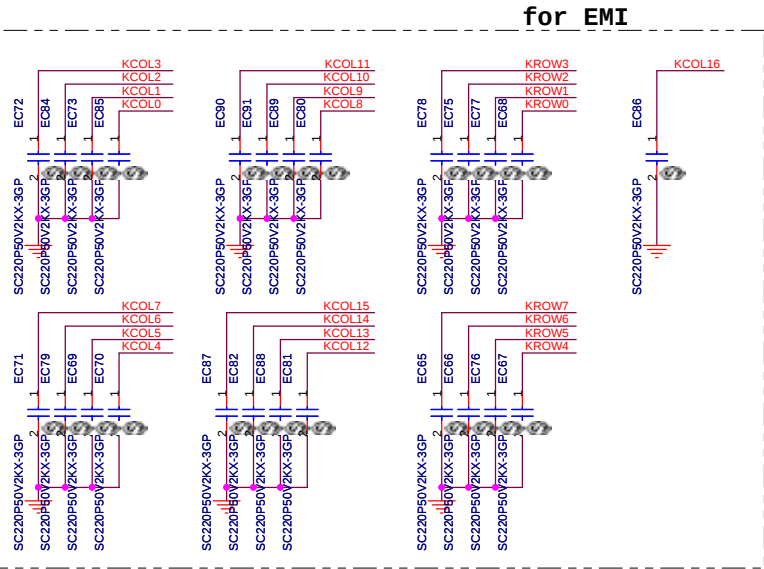
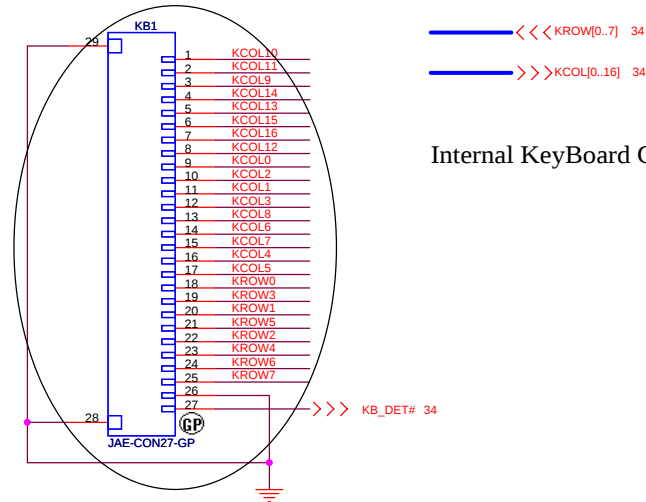
GAIN SETTING

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

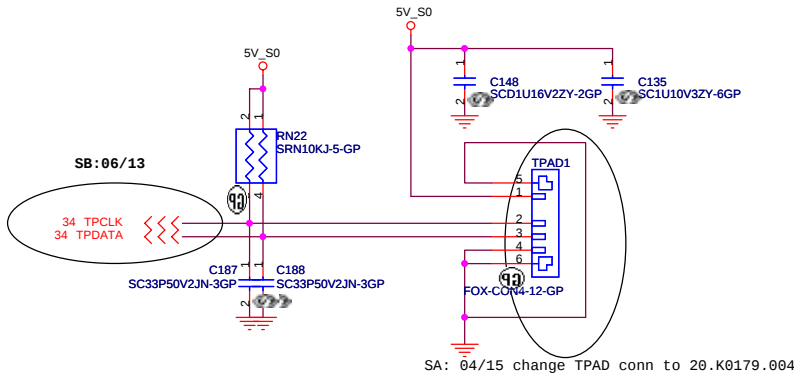
Signal inverter for speaker shutdown



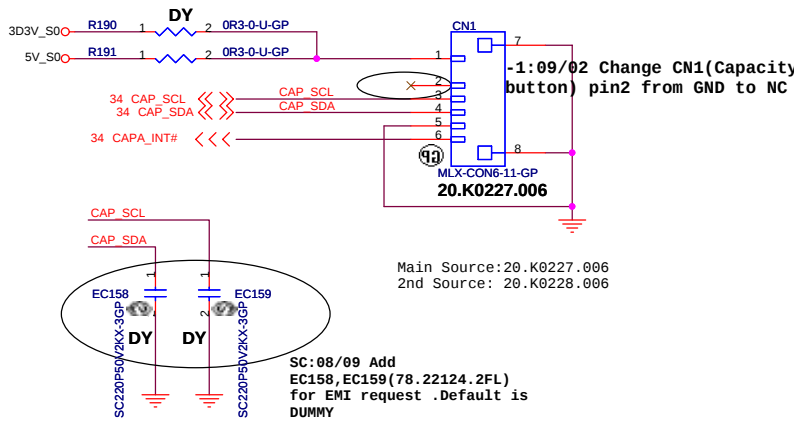
SB:06/27 Change K/B connector from 20.F0694.025 to 20.K0291.027 .



TouchPad Connector

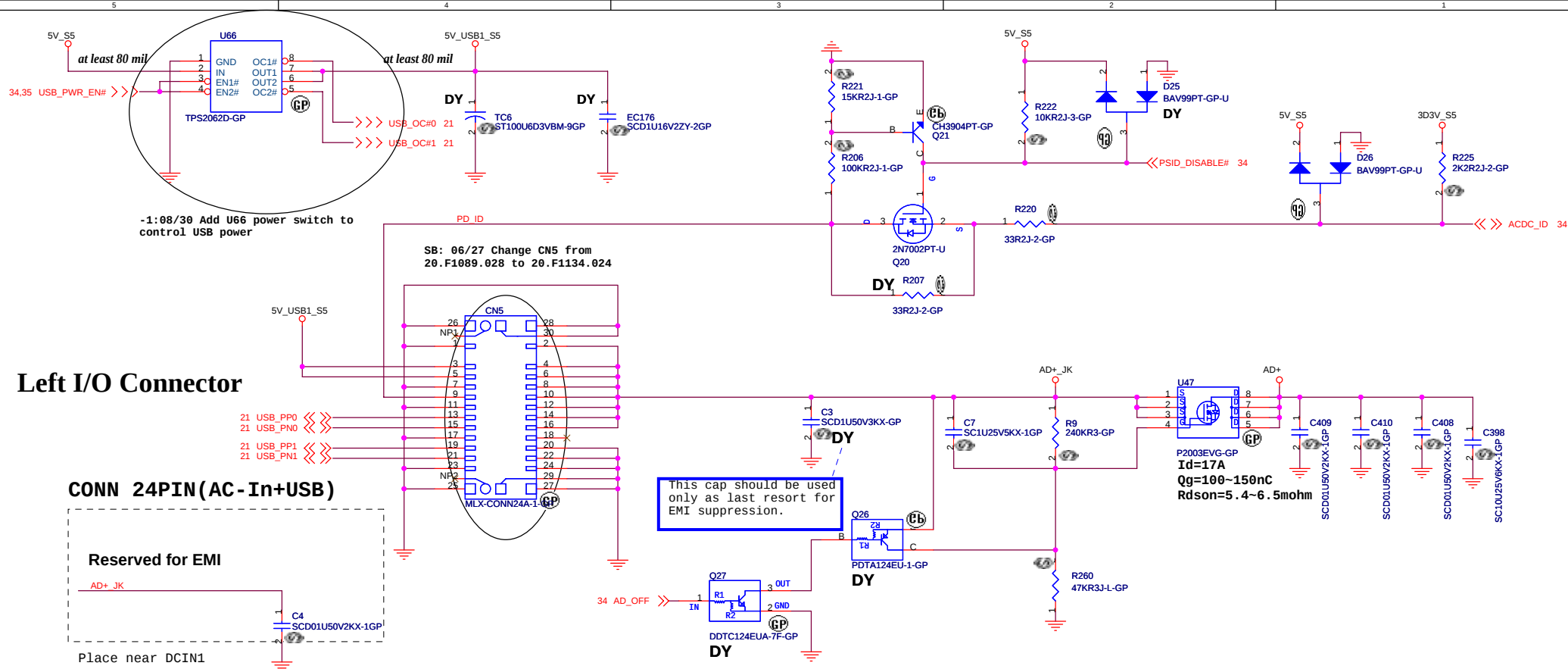


CAPACITY BUTTON



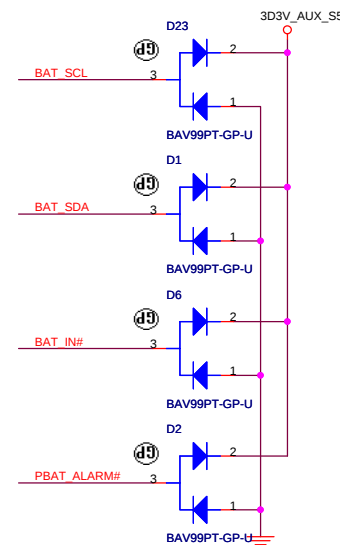
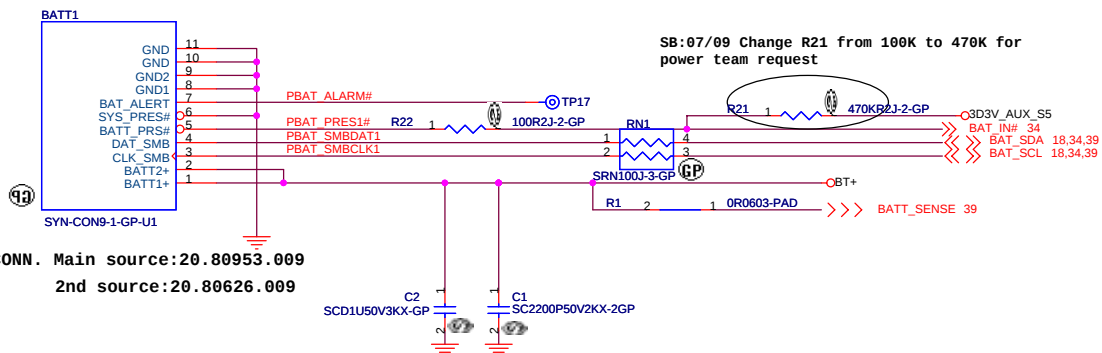
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
KeyBoard-CONN			
Size	Document Number		Rev
A3			
DS2-Intel		-1	
Date:	Wednesday, September 12, 2007	Sheet 37 of	47



Left I/O Board to Board CONN

Batt Connector



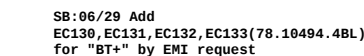
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緯創資通

Wistron Corporation

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Title			
AD/BATT CONN			
Size	Document Number	Rev	
A3		-1	
Date:	Wednesday, September 12, 2007	Sheet	38 of 47



Layout Trace 300mil



Title

Size	
Custom	

Document Number

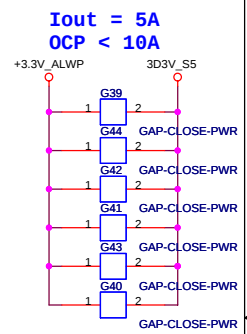
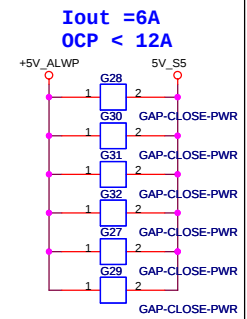
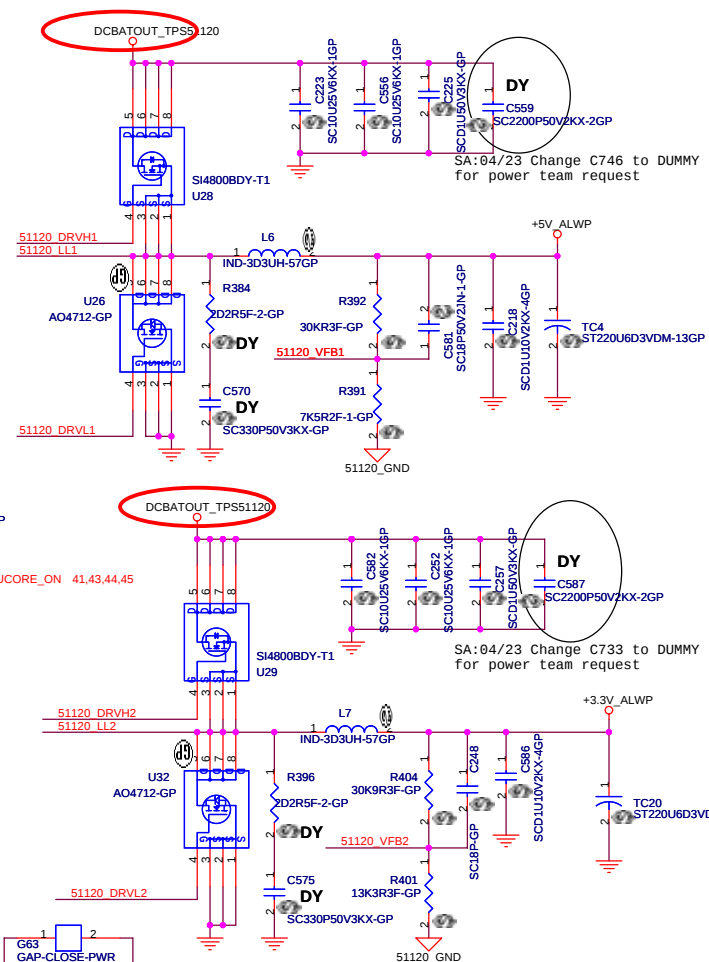
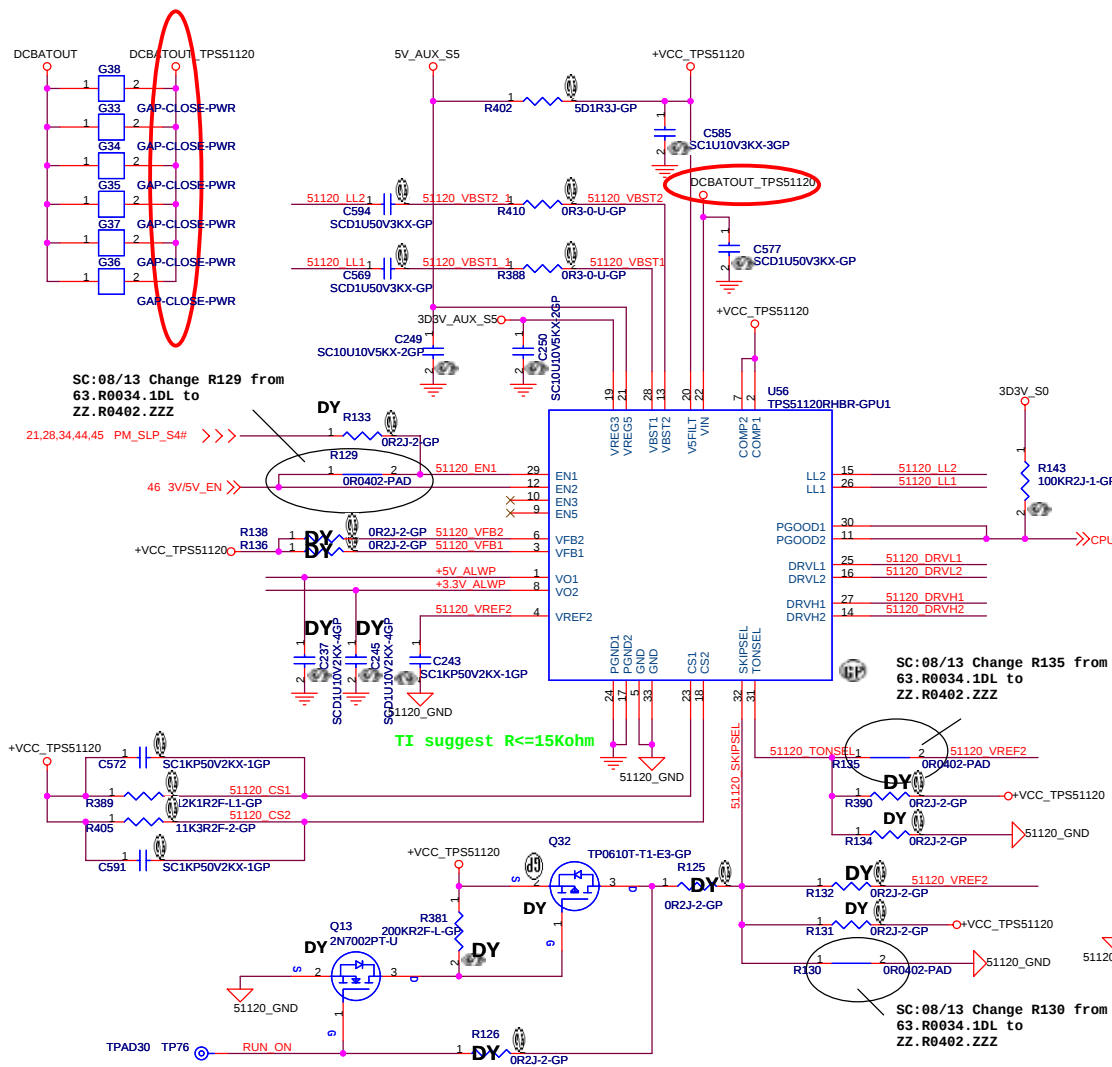
DS2 - Intel

Rev	
-1	

Date: Wednesday, September 12, 2007

She

47



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 3.3UH CYNTEC 11Arms 14.5Apeak
 O/P cap: 220U6.3V 6TPE220M 25mOhm 2.4Arms/ 77.22271.17L
 H/S: A04468 S0-8/ 30mOhm/ 4.5Vgs
 L/S: A04712 S0-8/ 7.3mOhm/ 4.5Vgs

$$V_{out} = 1V * (R1 + R2) / R2$$

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	5V ADJ.	Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

<Core Design>

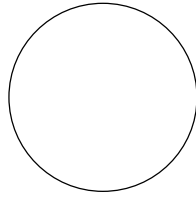
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 3.3V & 5V**

Size: Document Number
 Custom: **DS2-Intel** Rev: **-1**

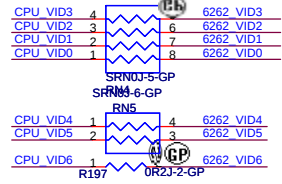
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SB:06/17 Remove R205,C348,TP86 power monitor circuit.



Place close to phase 1 choke
5 CPU_PROCHOT# <<< R185 4K02R3F-GP
470K /0402 size
If NTC=330Kohm, R10=8.66K
SB:06/17 Change R12,R16,R17 R198 from 0402 0 Ohm to 0402 close pad.

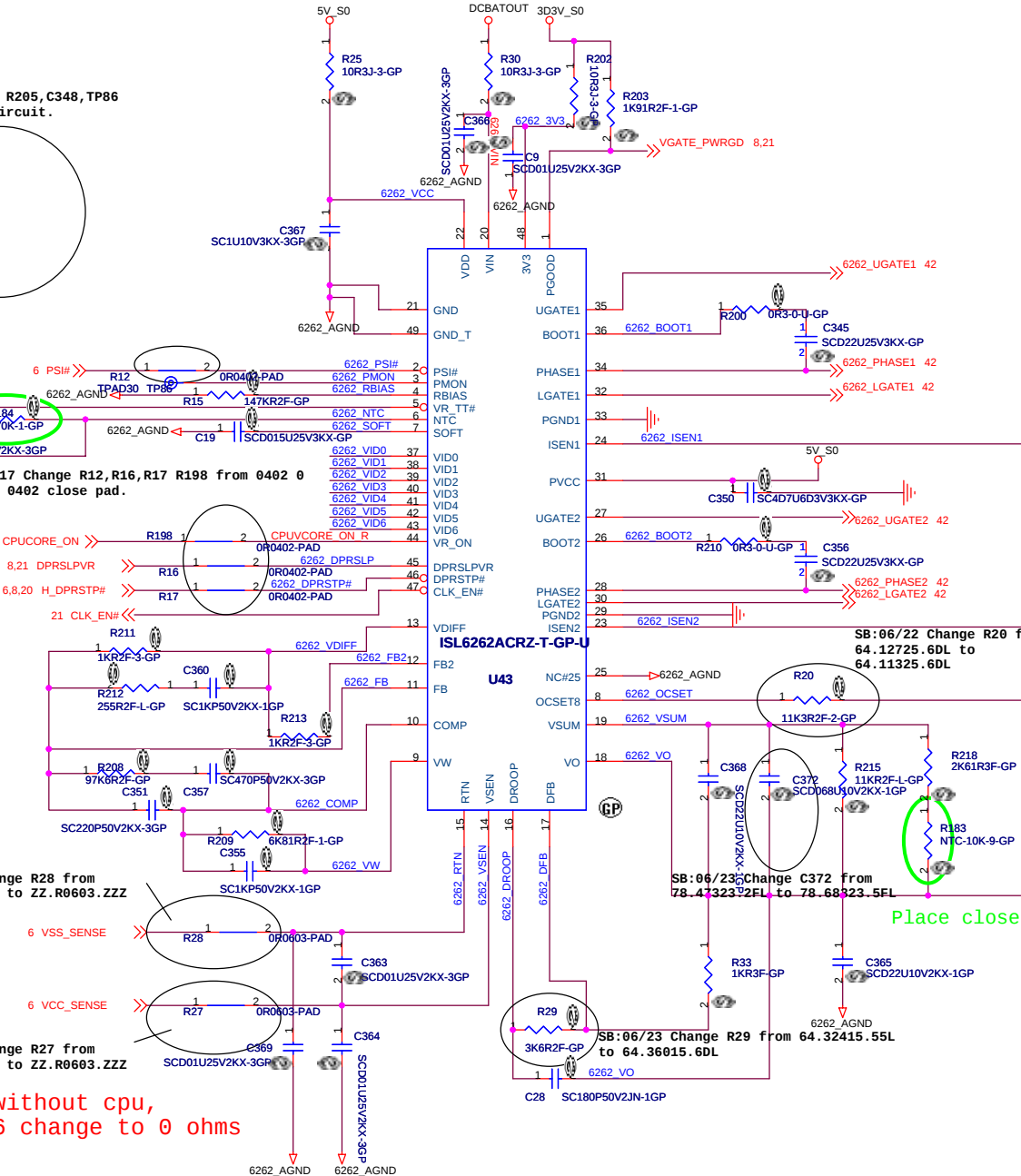
6 CPU_VID[0..6] >>>



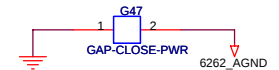
SC:08/13 Change R28 from 63.00000.00L to ZZ.R0603.ZZZ

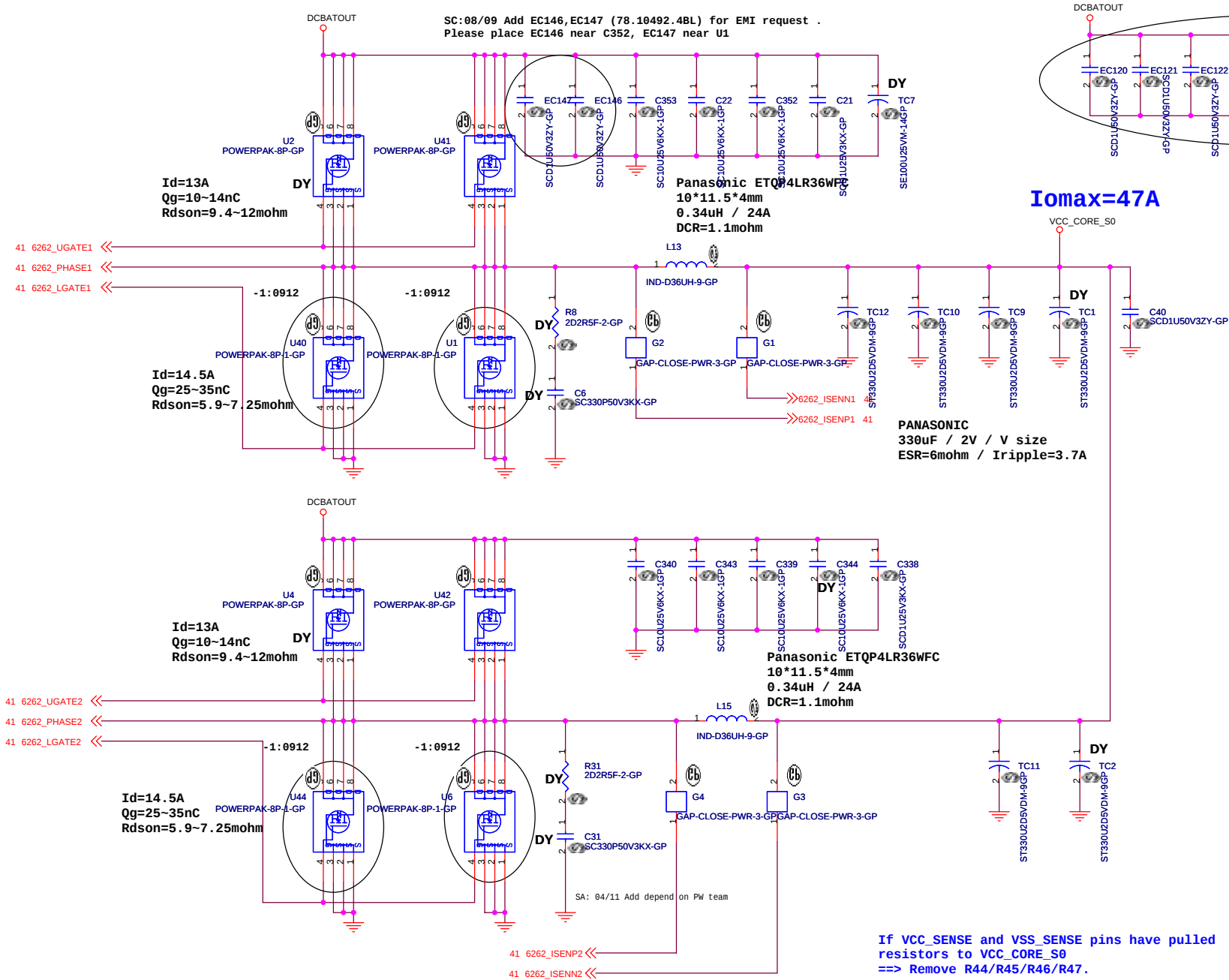
SC:08/13 Change R27 from 63.00000.00L to ZZ.R0603.ZZZ

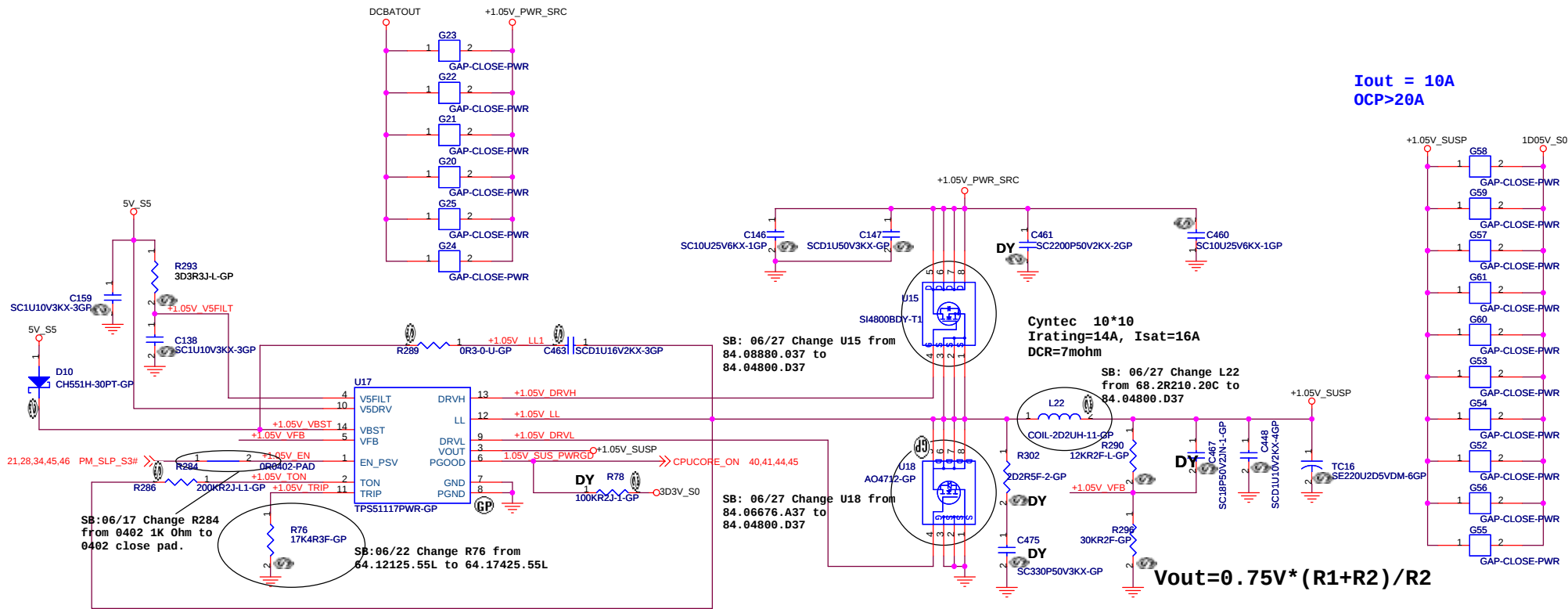
When test without cpu,
R483 & R486 change to 0 ohms



Place close to phase 1 choke







Iout = 10A
OCP>20A

$$V_{out} = 0.75V * (R1 + R2) / R2$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
O/P cap: 220U 4V 4TPE220MF 15m0hm 3.1Arms/ 77.22271.161
H/S & L/S: FDS8884 S0-8/ 30m0hm/ 4.5Vgs/ 84.08884.037
L/S: FDS8896 S0-8/ 7.3m0hm/ 4.5Vgs/ 84.08896.037
Ton = 200K0hm --> 330KHz

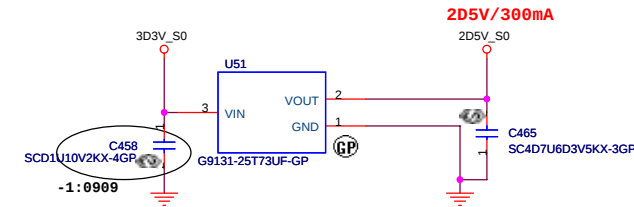
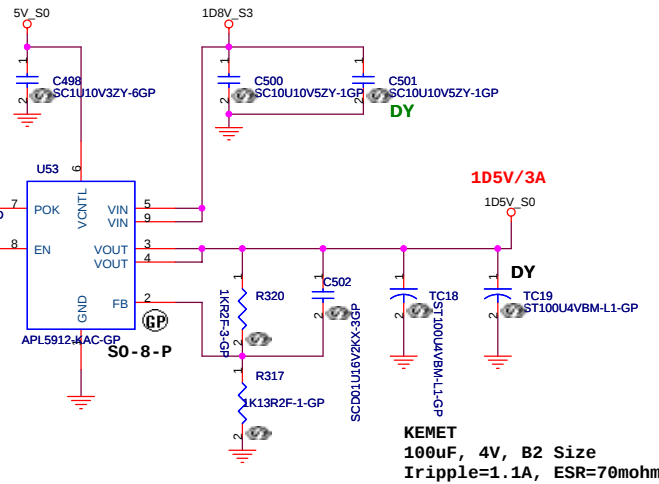
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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DCDC 1.05V			
Size A3	Document Number		Rev -1
DS2-Intel			
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1D5V_SB

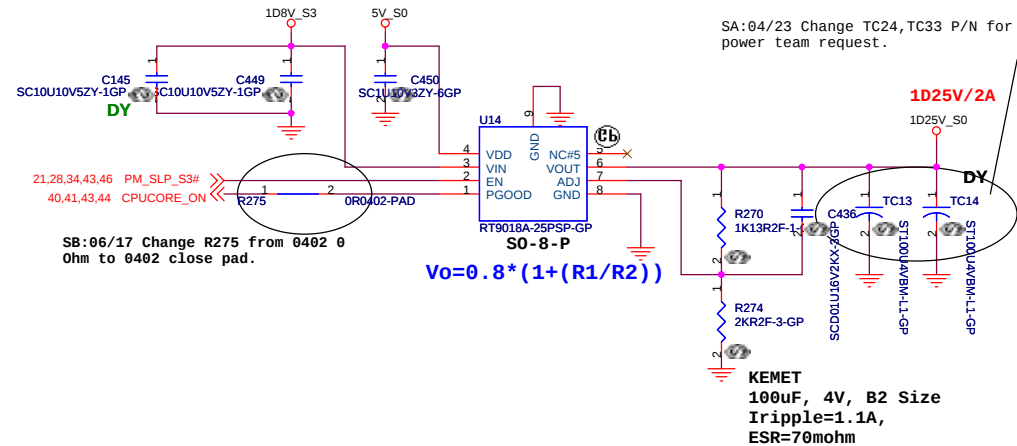
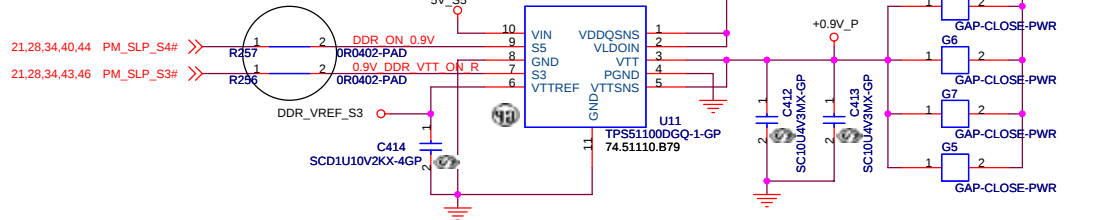
SB:06/17 Change R315 from 0402 0 Ohm to 0402 close pad.

40,41,43,44 CPUCORE_ON << R315 0R0402-PAD
21,28,34,43,46 PM_SLP_S3# >>
 $V_O = 0.8 * (1 + (R1/R2))$



SSID = PWR.Plane.Regulator_0.9V

SB:06/17 Change R256, R257 from 0402 0 Ohm to 0402 close pad.

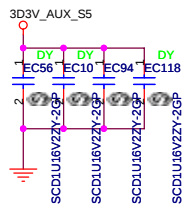


SA:04/23 Change TC24, TC33 P/N for power team request.

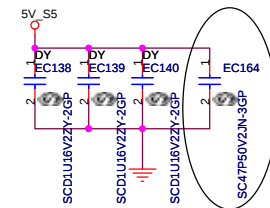
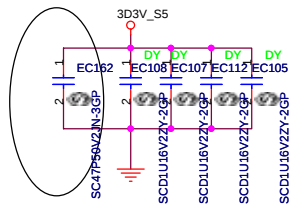
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Taipei Hsien 221, Taiwan, R.O.C.

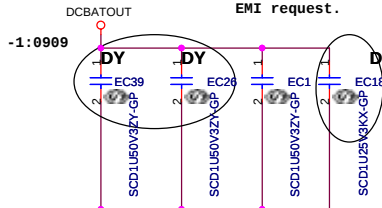
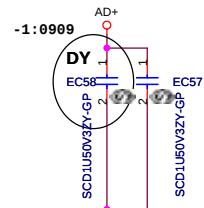
Title		DC/DC 1D8V	
Size	Document Number	DS2-Intel	
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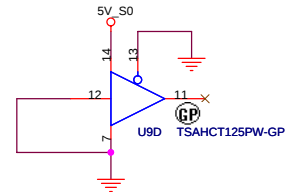
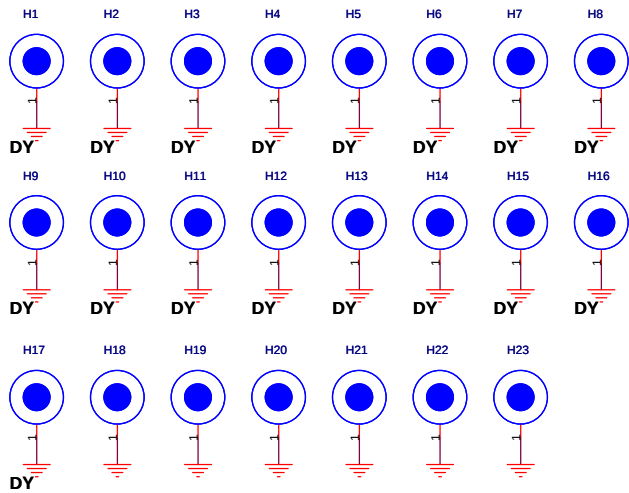
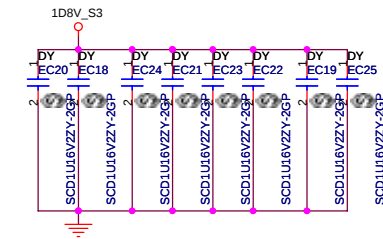
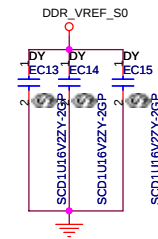
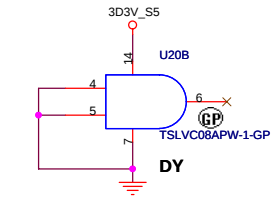
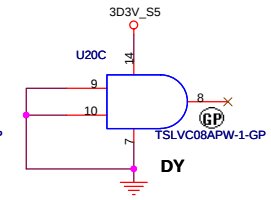
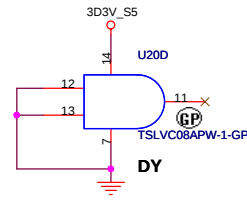
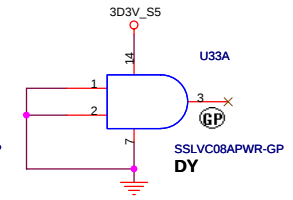
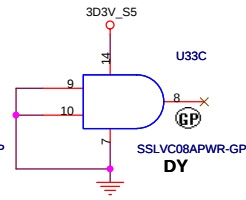
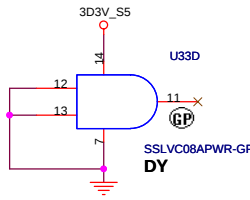
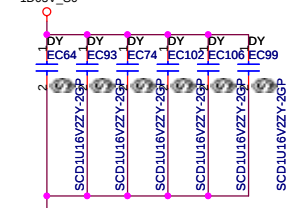
SC:08/11 Add EC162 on 3D3V_S5 for RF team Request.



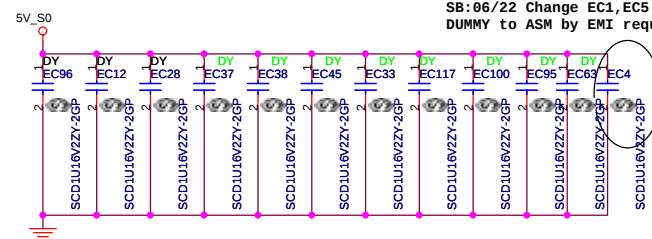
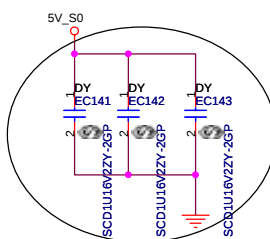
SC:08/11 Add EC164 on 5V_S5 for RF team Request.



-1:0904 Add EC187(78.10422.2BL) for DCBATOUT decoupling, this is for EMI request.

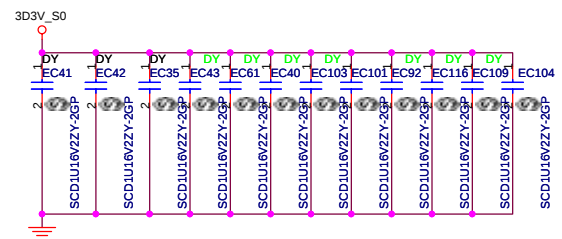
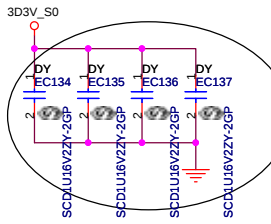


SB:06/29 Add EC141, EC142, EC143(78.10491.4FL) for EMI request

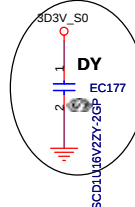


SB:06/22 Change EC1, EC5 from DUMMY to ASM by EMI request.

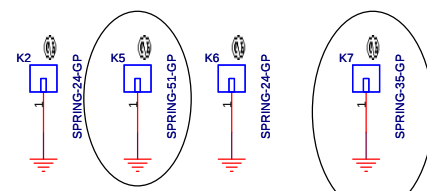
SB:06/29 Add EC134, EC135, EC136, EC137(78.10491.4FL) for EMI request



SC:08/15 Add EC177(78.10491.4FL) on 3D3V_S0, this is for EMI request. Default is DY



SC:08/09 Change K5 spring from 34.45T31.001to 34.48312.002 for ME request



Place this spring near U40(bottom side)

SC:08/11 Change K7 from 34.39S07.001 to 34.41P18.001.This change is for EMI request