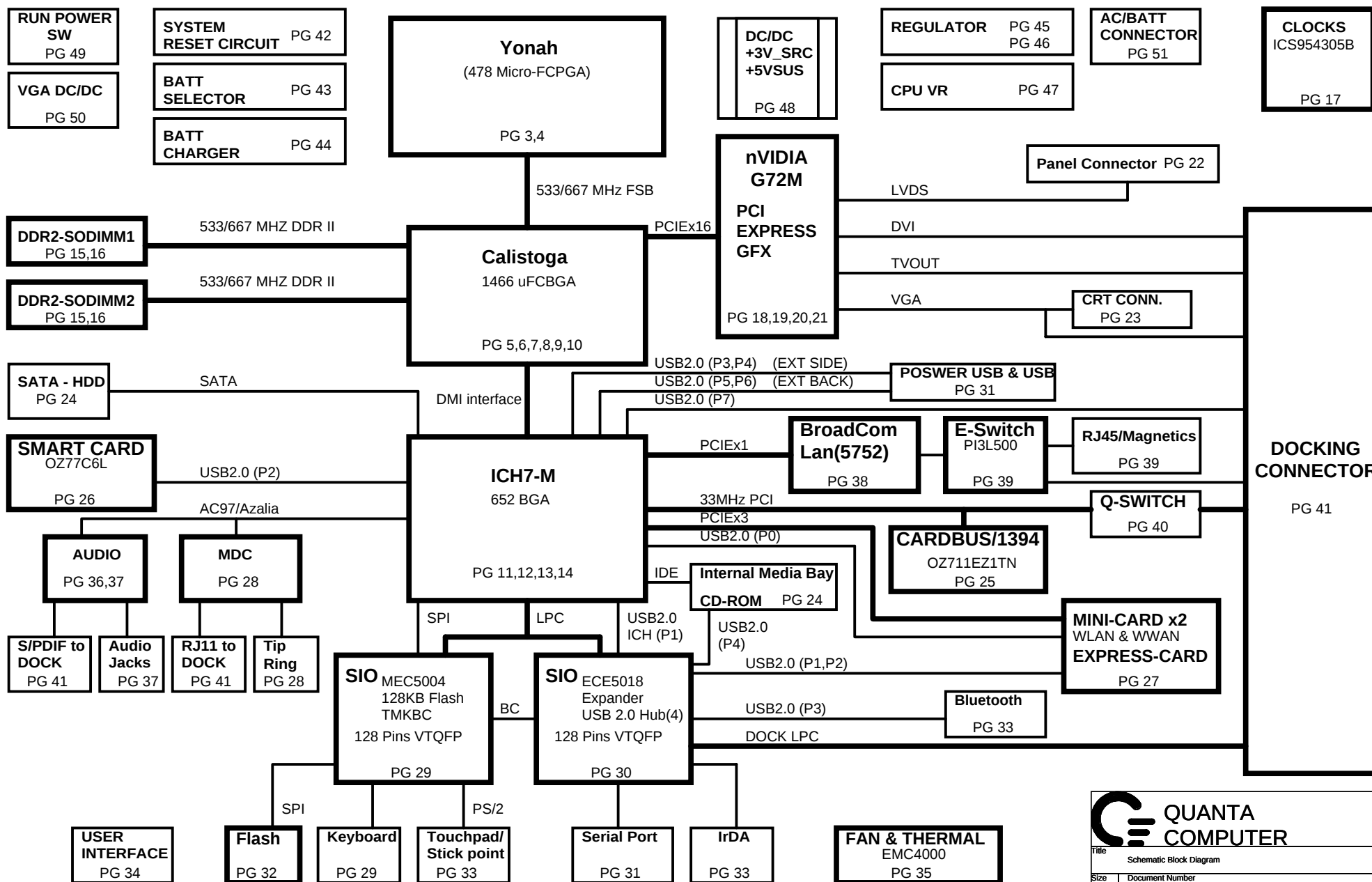


BREWSTER-DISCRETE GFX

PWA XD617, PWB FF094,
SCHEM YD536. (256MB)
VER : 2A



INDEX		
Pg#	Description	DNI LIST
1	Schematic Block Diagram	
2	Front Page	
3-4	Yonah	
5-10	Calistoga	
11-14	ICH7	
15-16	DDRII SO-DIMM(200P)	
17	Clock Generator	
18-21	VGA	
22	LCD Conn. & SSP	
23	CRT Conn	
24	SATA & IDE Conn	
25	PCCARD/Conn & 1394	
26	Express Card & Smart Card	
27	Mini Card	
28	MDC Conn.	
29	SIO (MEC5004)	
30	SIO (MEC5018)	
31	SERIAL PORT & USB	
32	Flash ROM & RTC Circuit	
33	TP,BT & FIR	
34	Switch,Keyboard & LED	
35	FAN & Thermal	
36-37	Audio CODEC(STAC9200)/Phone Jack	
38-39	LOM (BCM5752)/Switch	
40-41	Docking Conn/Q-Switch	
42	System Reset Circuit	
43-44	Battery Selector & Charger	
45	DDR2_1.8VSUS, 0.9V	
46	1.5VSUS,1.05V(VTT)	
47	CPU Power	
48	D/D Power	
49	RUN Power Switch	
50	VGA DC/DC	
51	DCIN/Batt Conn.	
52	PAD& SCREW	
53	SMBUS BLOCK	

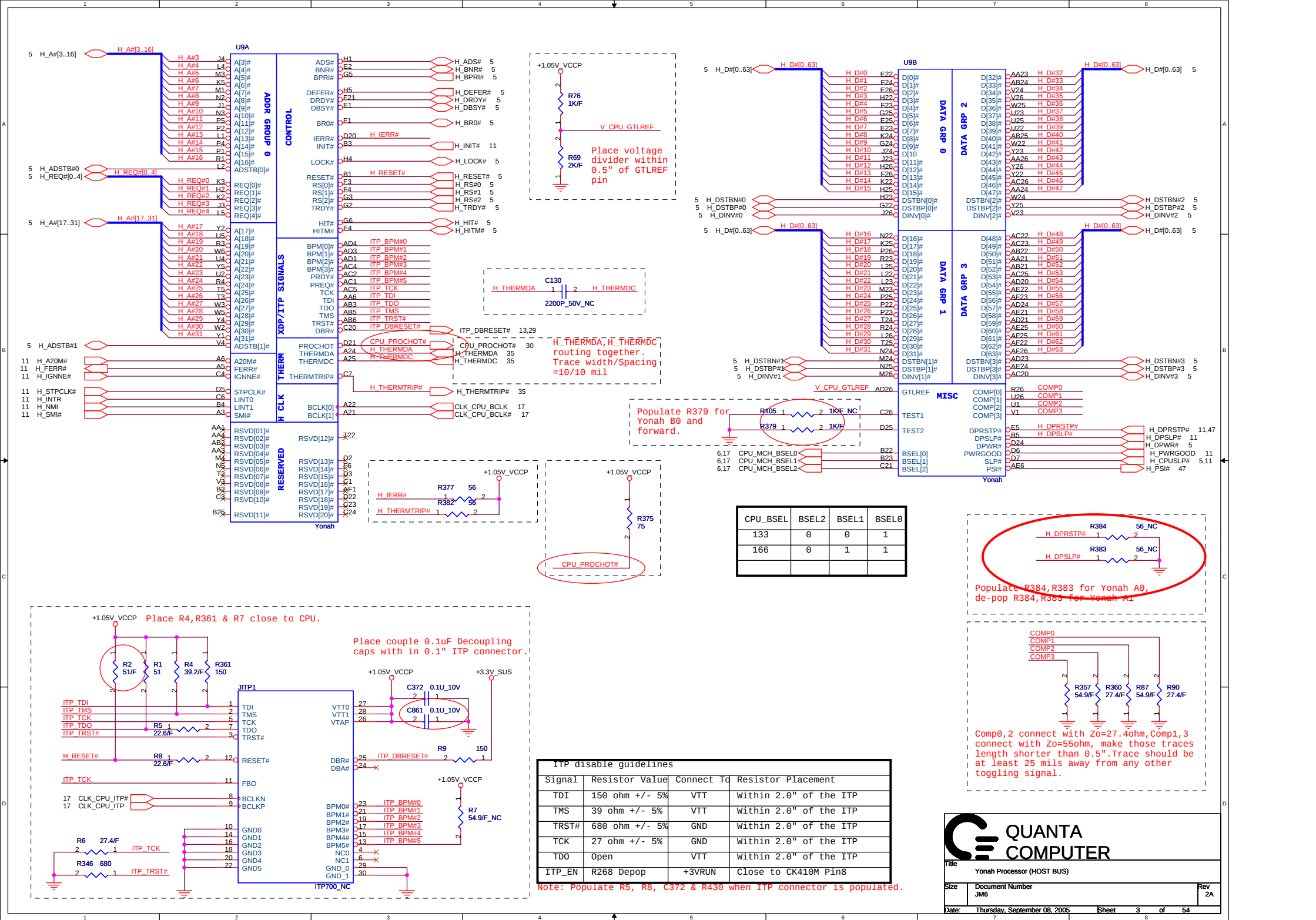
Power & Ground			
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~20V)	
RTC_PWR3_3V		RTC & PCL POWER (3.3V)	
+12V		+12V	DRUNPWROK
VHCORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
V1_2RUN		AGTL+ POWER (1.2V)	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VFAN1, +5VFAN2		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		AGP I/O POWER	
 GND	ALL PAGES	DIGITAL GROUND	
 GNDP		CPU POWER GND	
 CGNDP		CHARGER GND	
 DGNDP		DC/DC POWER GND	
LANGND		COMBO CONN GND	

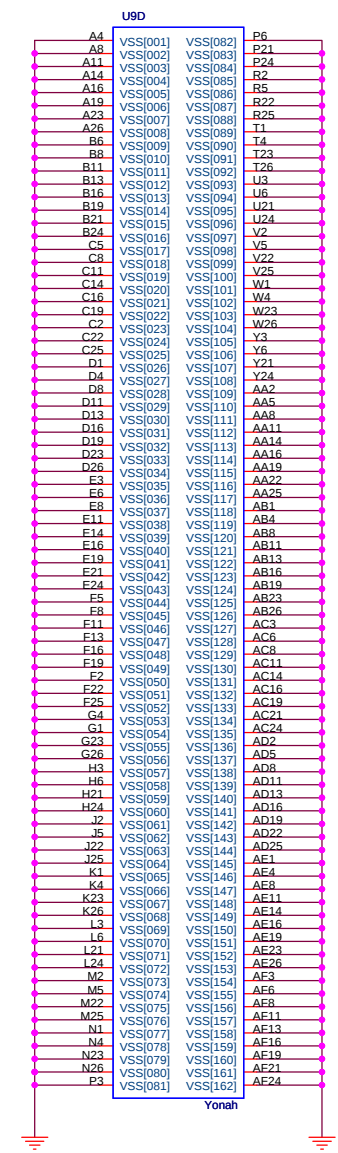
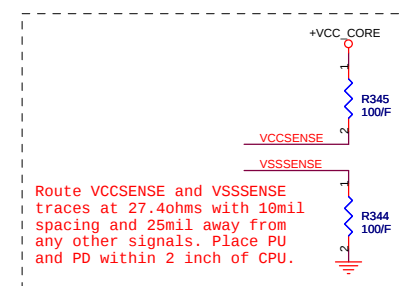
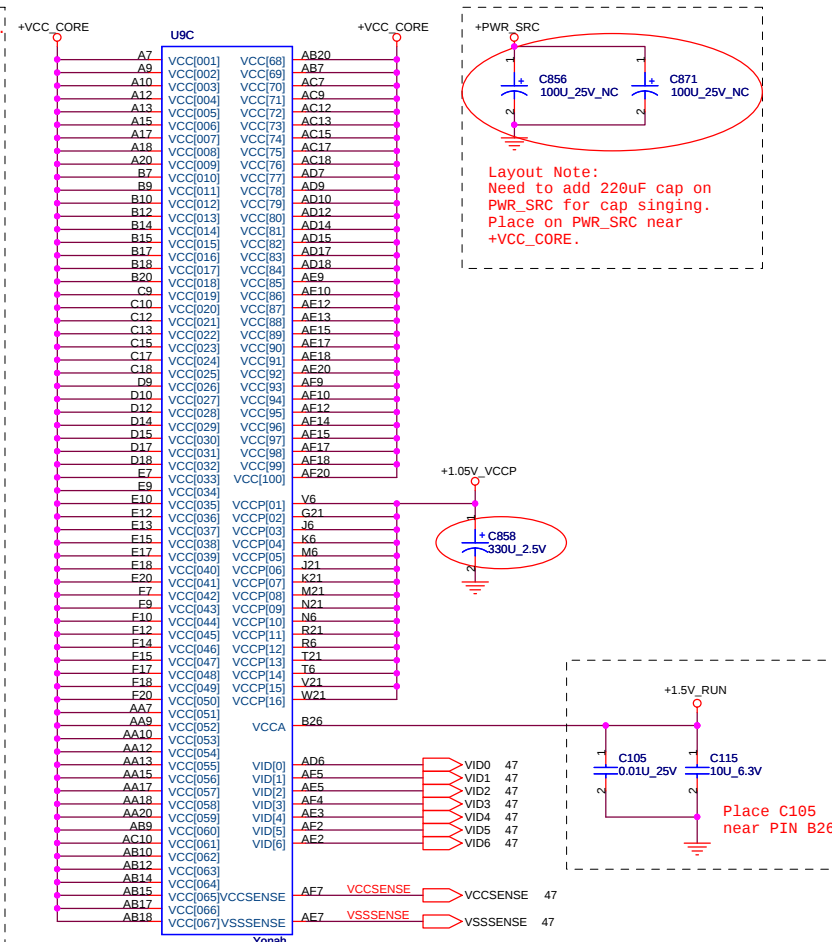
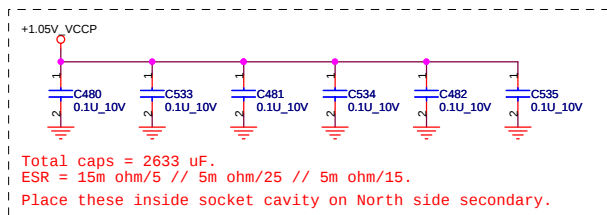
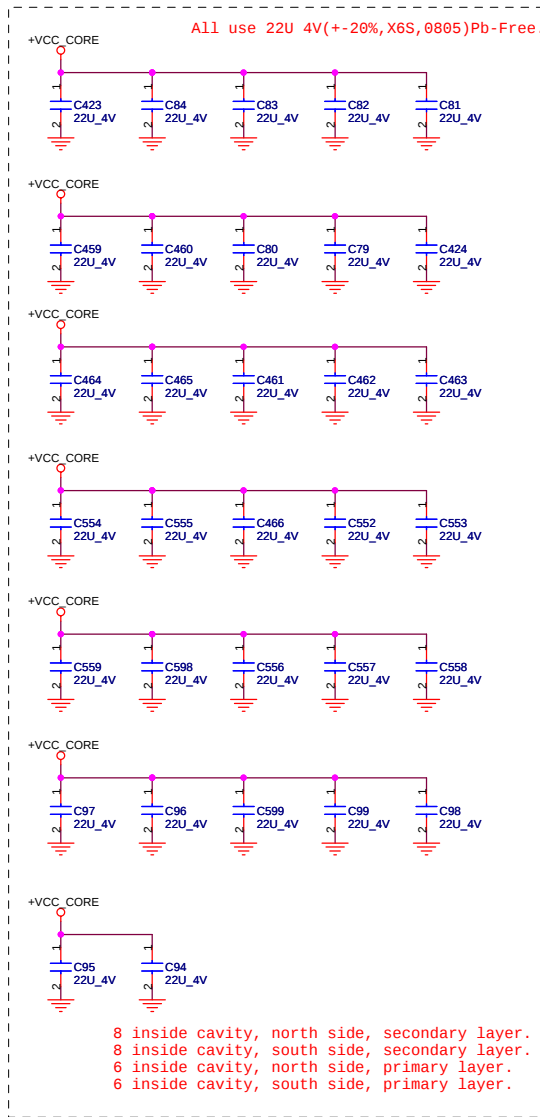


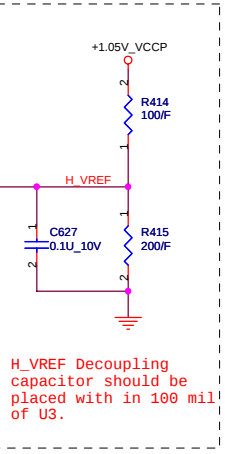
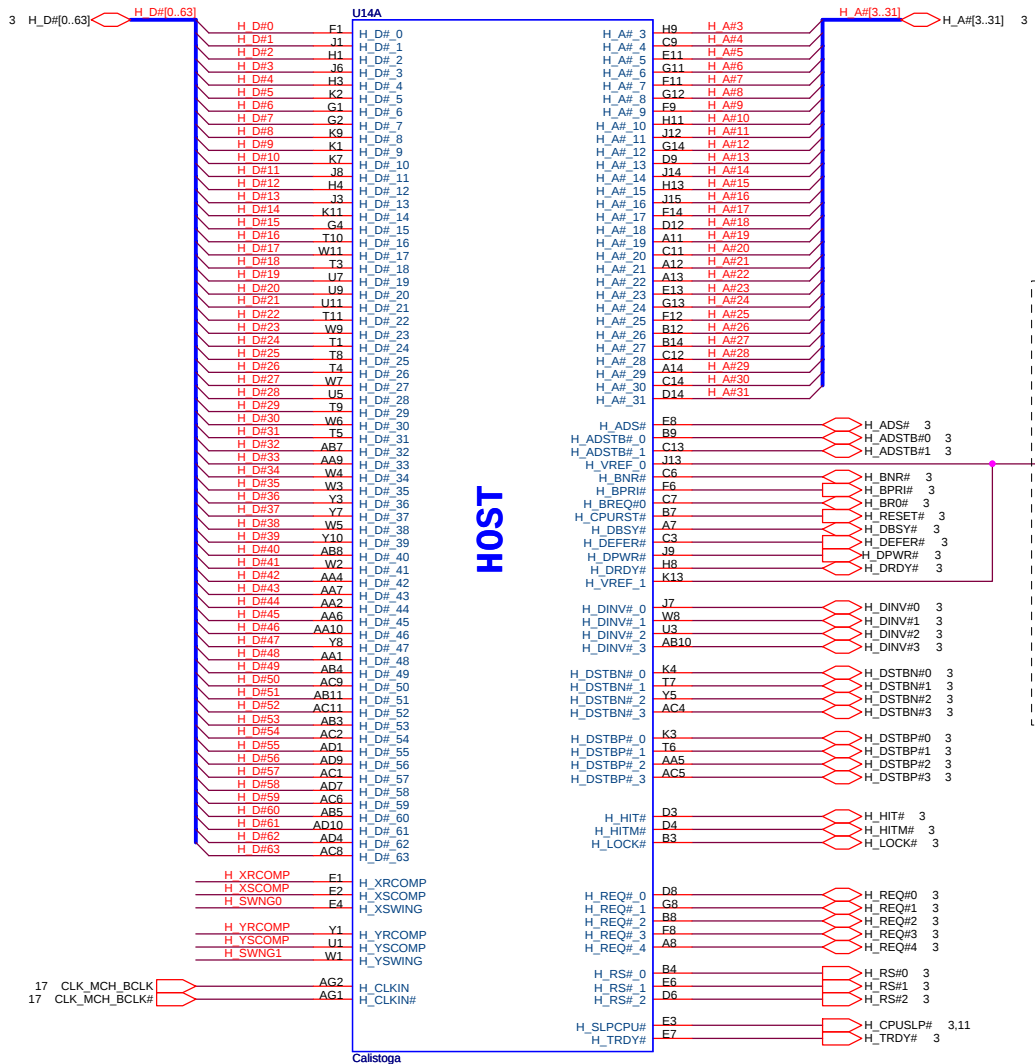
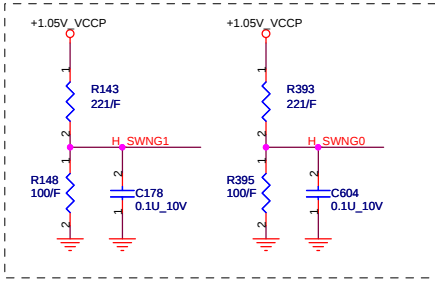
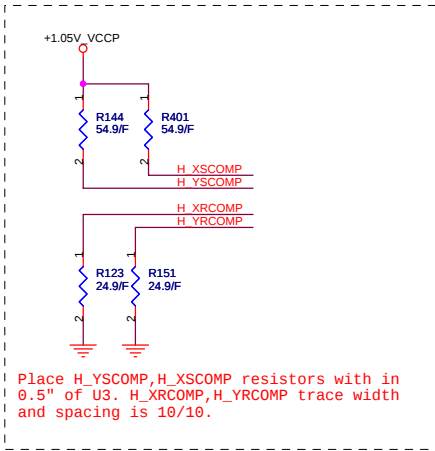
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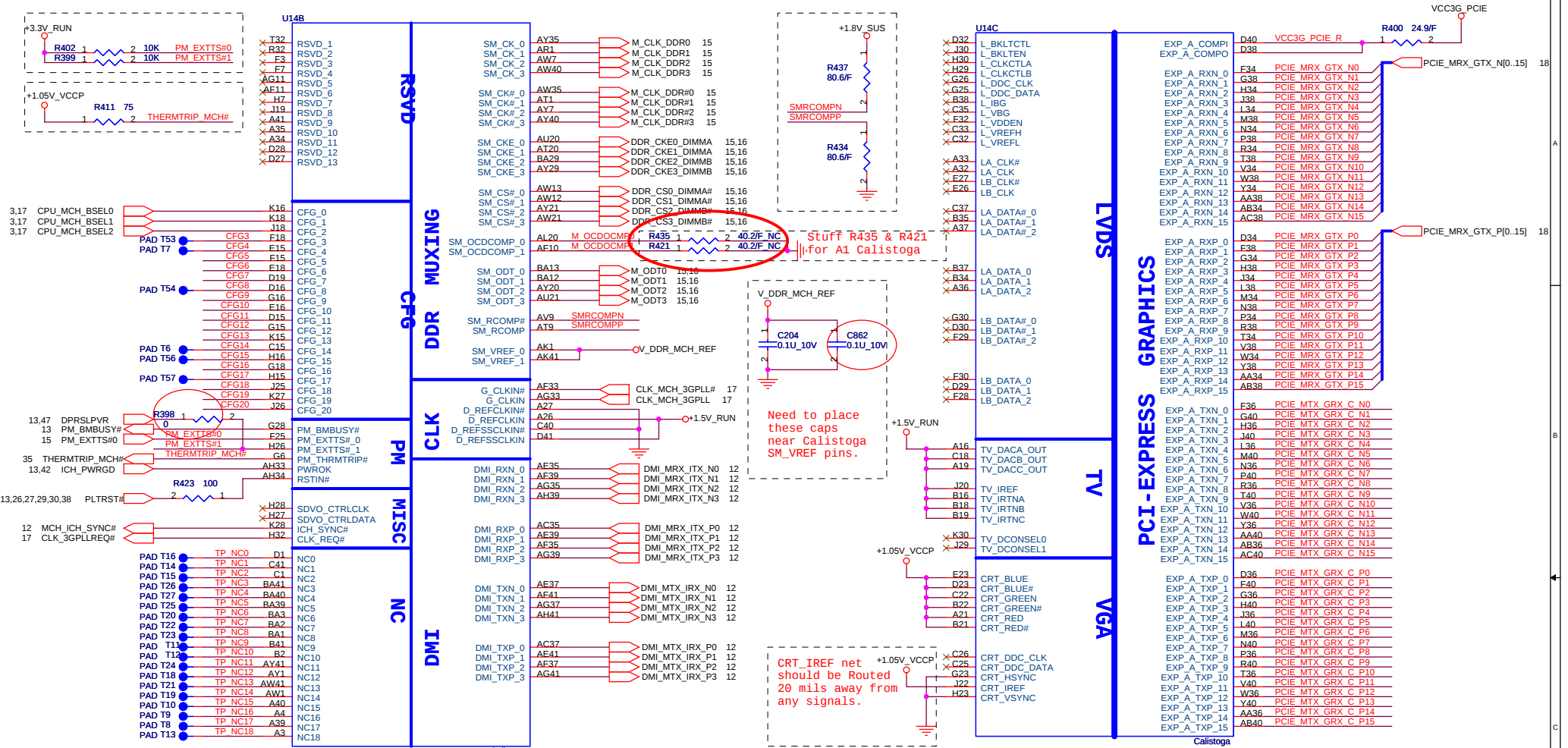
COMPUTER

Title		
Index, DNI, Power & Ground		
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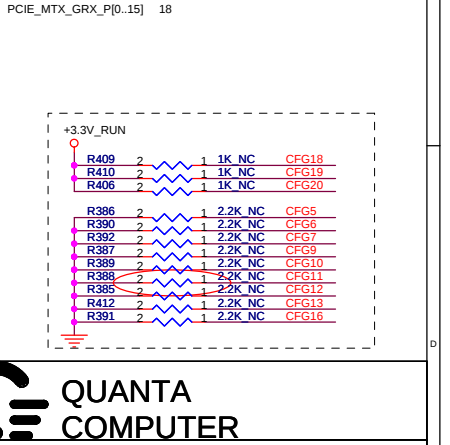
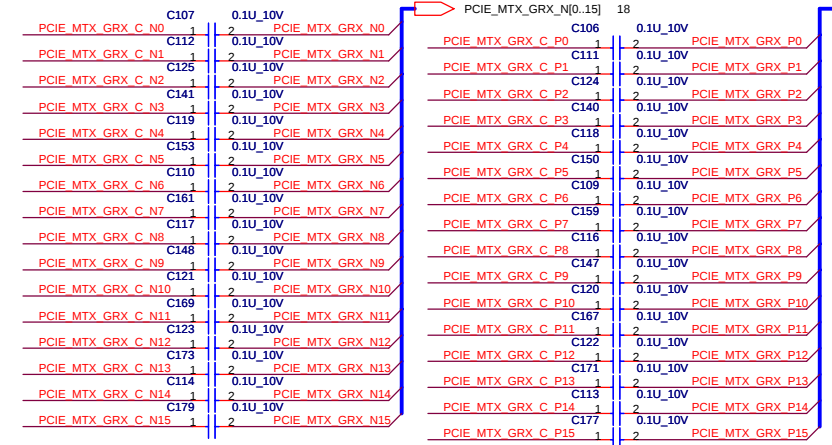








CFG5	Low=DMIX2 High=DMIX4
CFG6	Low=Moby Disk High=Calistoga.
CFG7 CPU_Strap	Low=RSVD High=Mobile CPU
CFG9 PCIe Graphics Lane	Low= Reveise Lane High=Normal operation
CFG10 Host PLL VCC Select	Low=Reserved High=Mobility
CFG11 PSB 4X CLK Enable	Low=Calistoga High=Reserved
CFG[13:12]	00=Reserved. 01=XOR Mode Enable. 11=Normal operation.
CFG16 FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable
CFG18 VCC Select	Low=1.05V High=1.5V
CFG19 DMI Lane Reversal	Low=Normal High=Lane Reversed
CFG20 PCIe Backward Interpoerability mode	Low=Only SDVO or PCIeX1 is operational (defaults) High=SDVO and PCIeX1 are operating simultaneously via PEG port
SDVO_CTRLDATA	Low=No SDVO device present. High=SDVO device present.





QUANTA

COMPUTER

Title

Calistoga (VGA,DMI)

Size

Document Number

JM6

Rev

2A

Date:

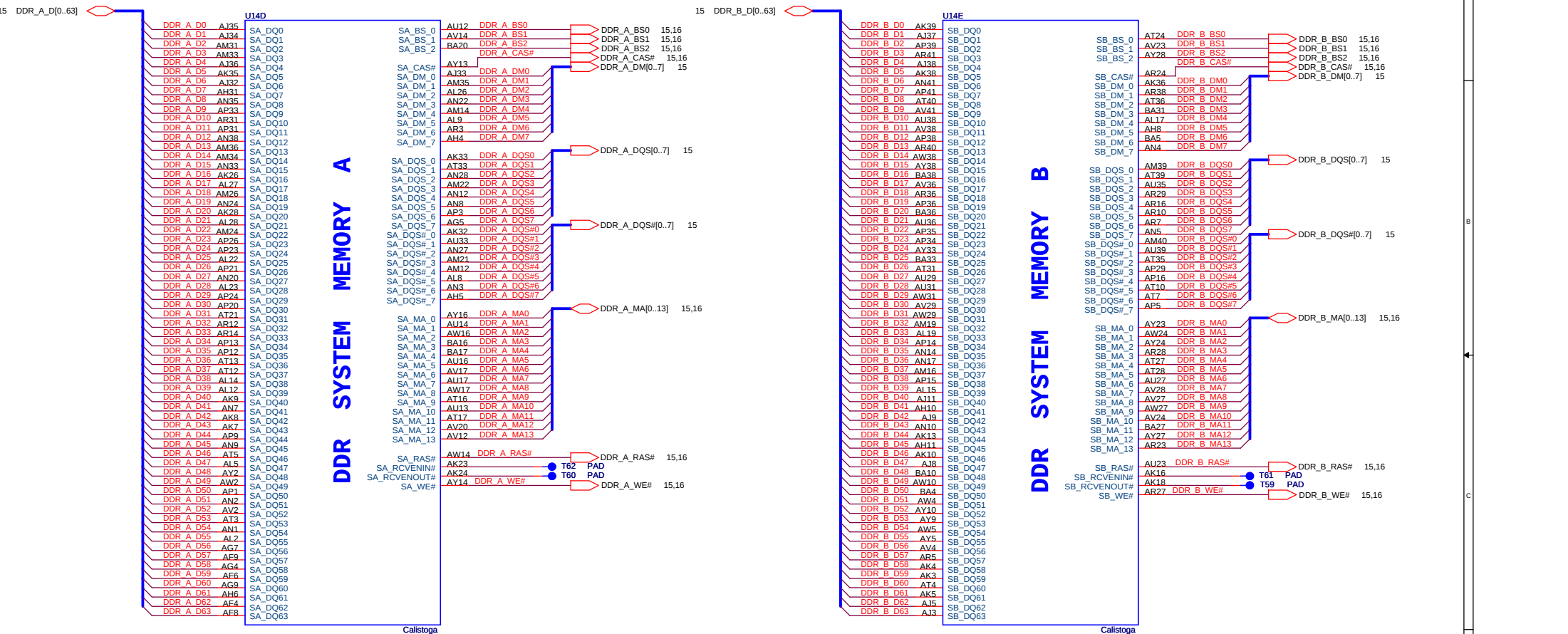
Thursday, September 08, 2005

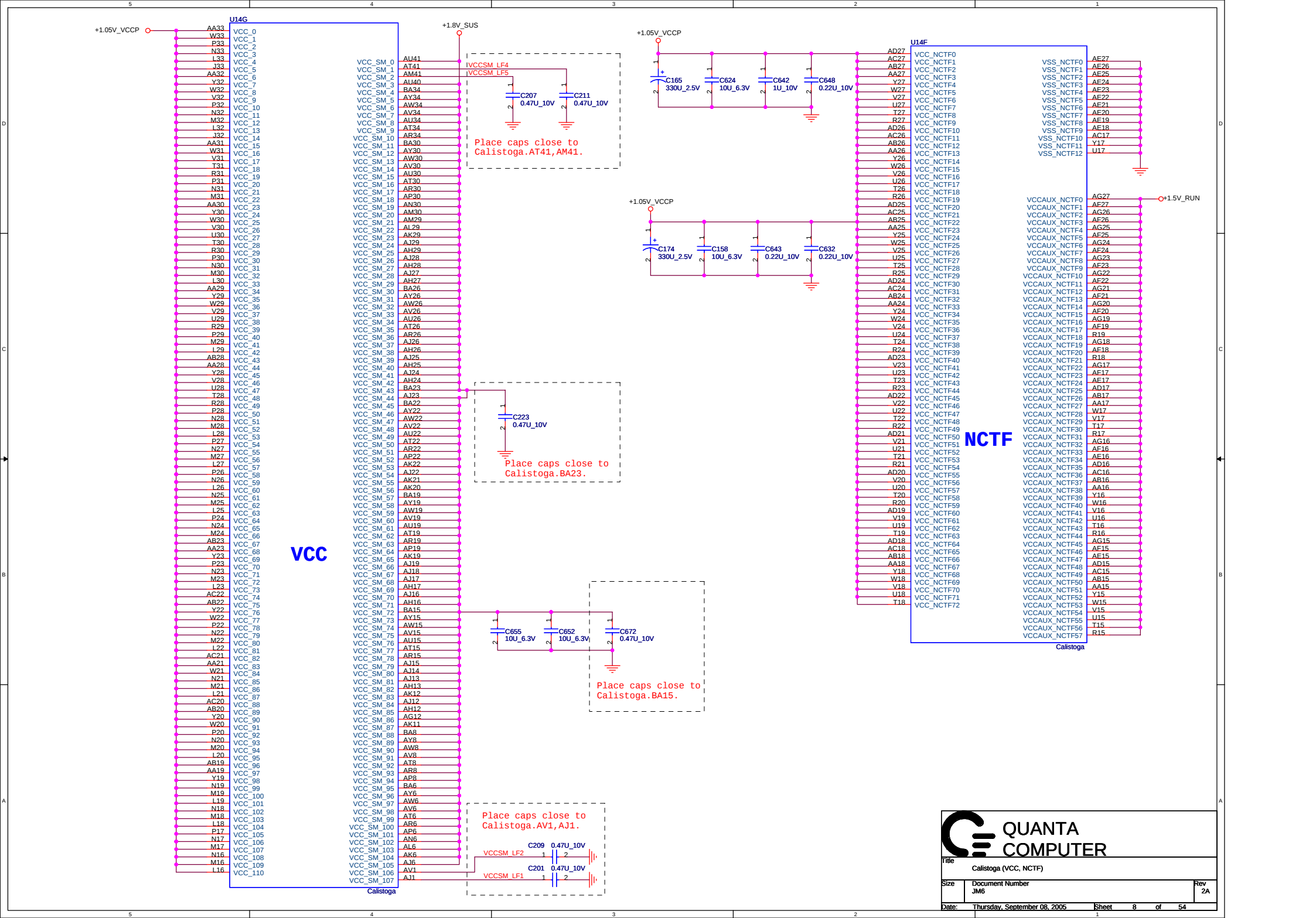
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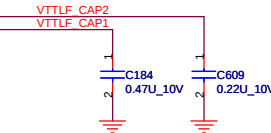
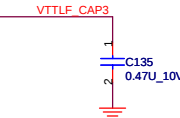
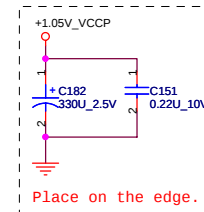
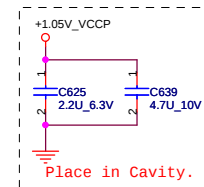
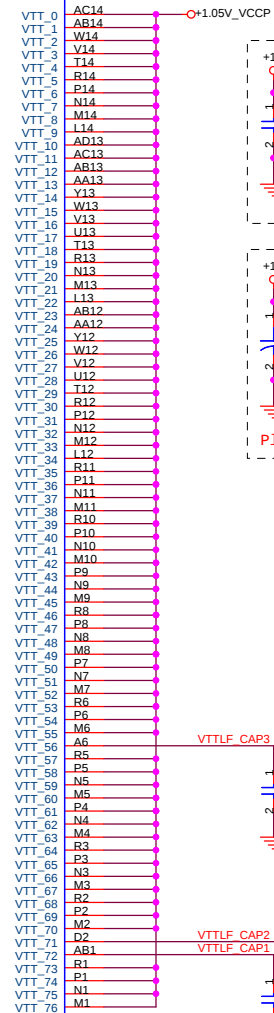
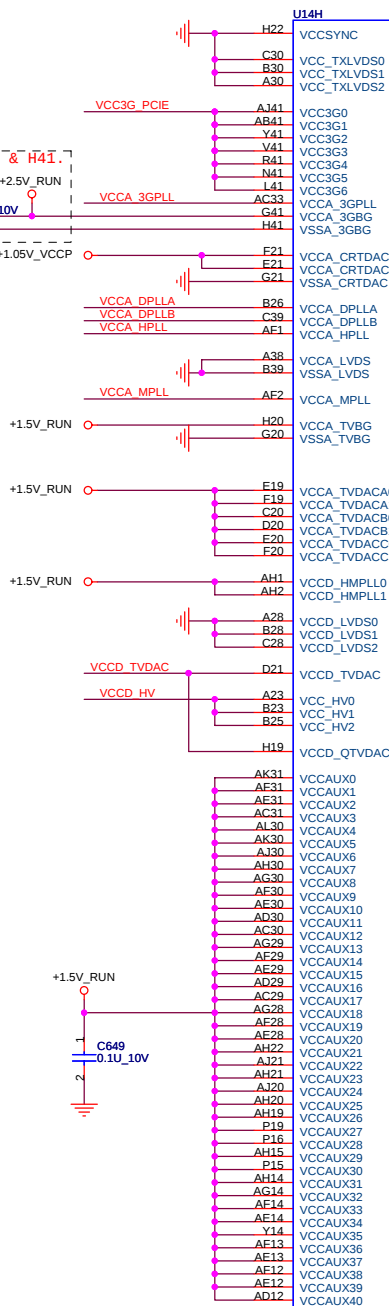
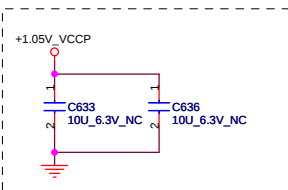
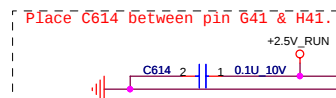
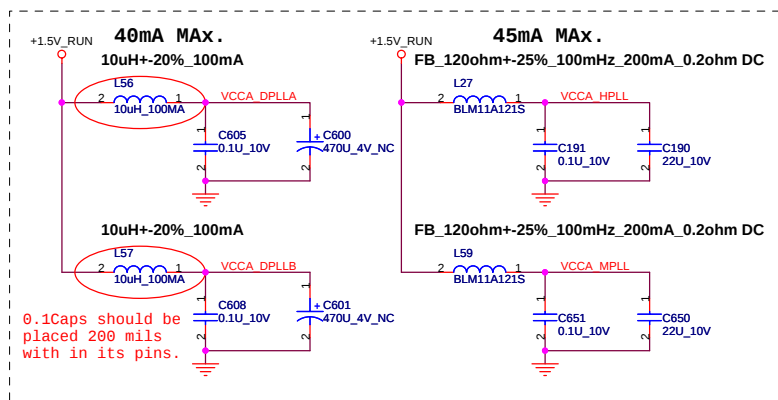
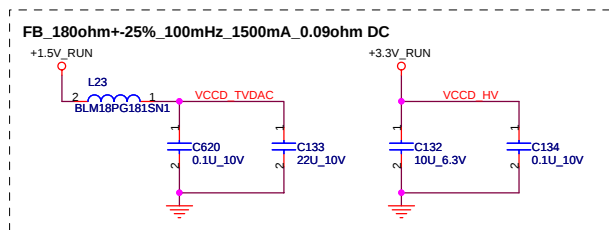
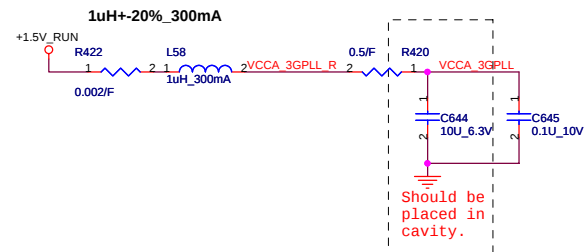
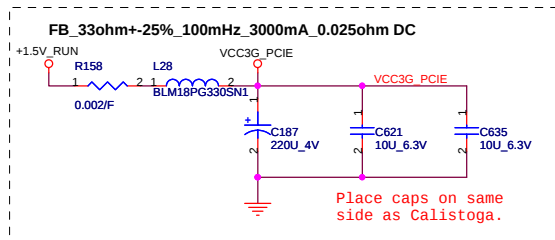
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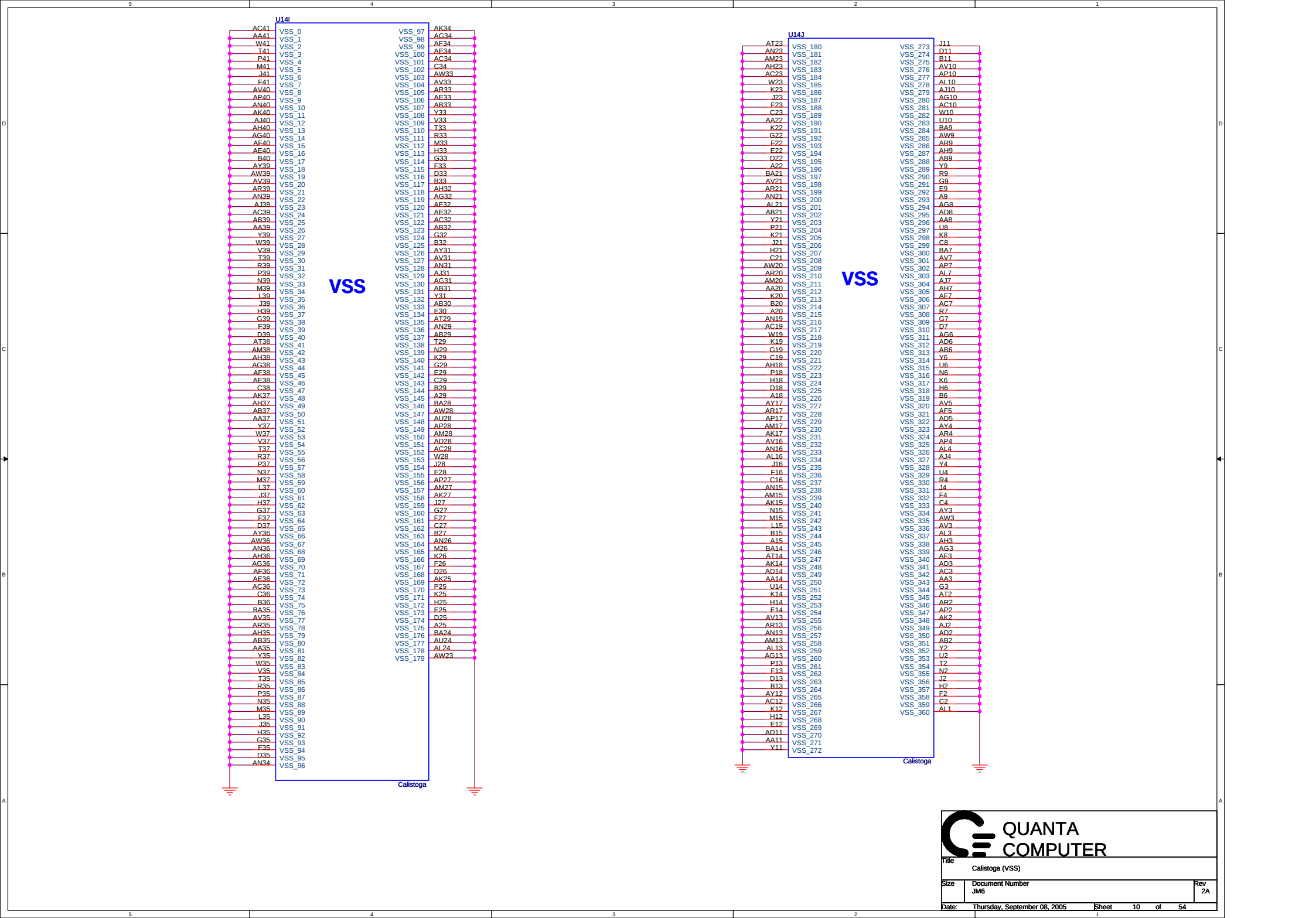
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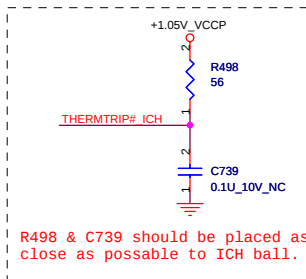
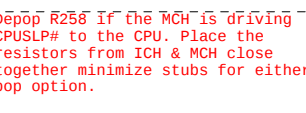
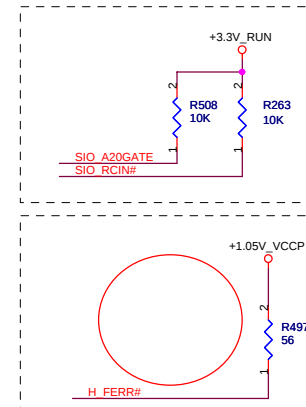
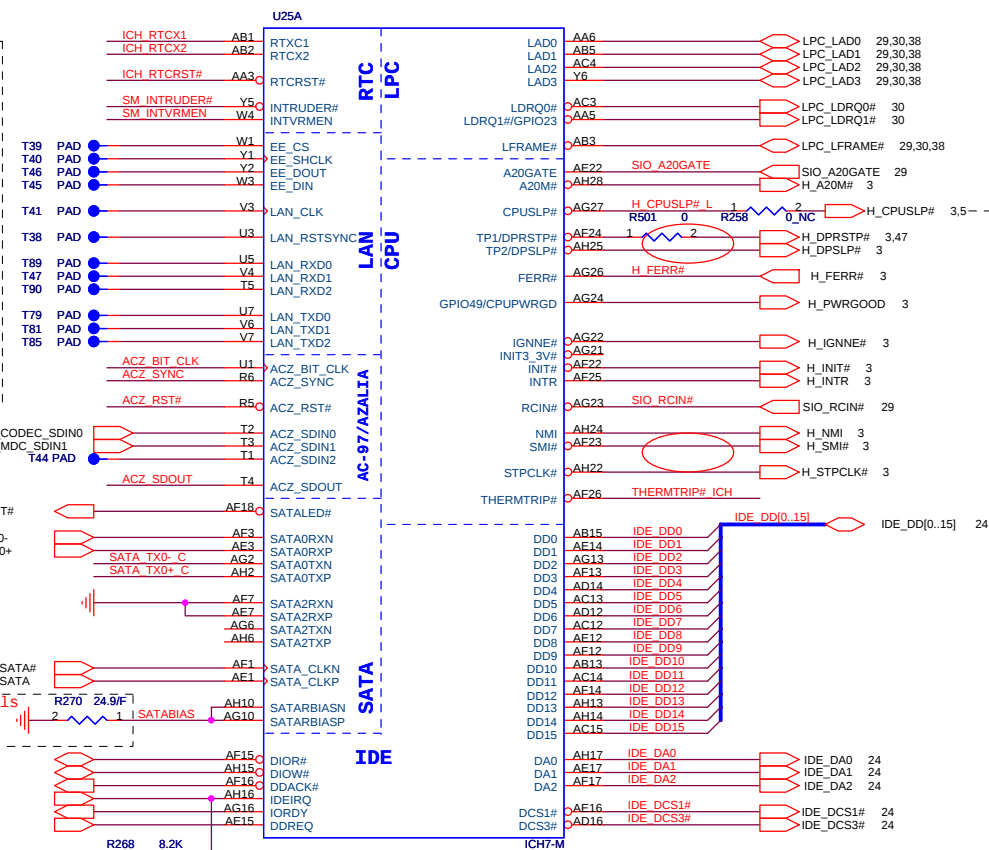
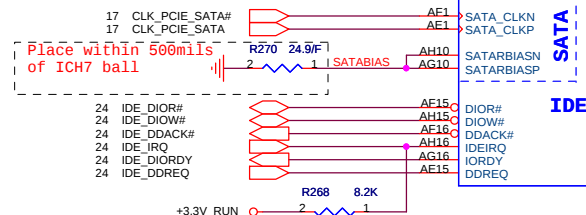
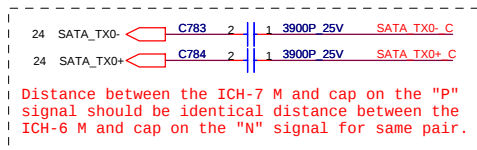
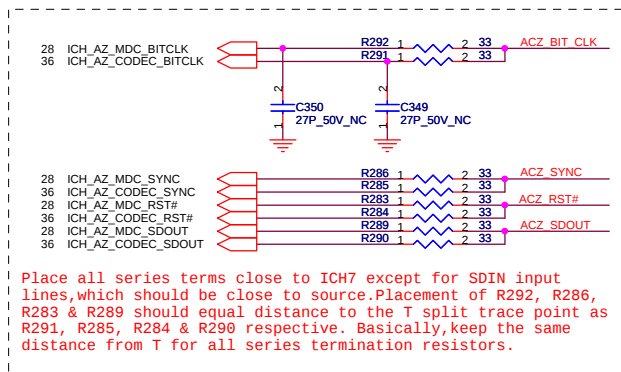
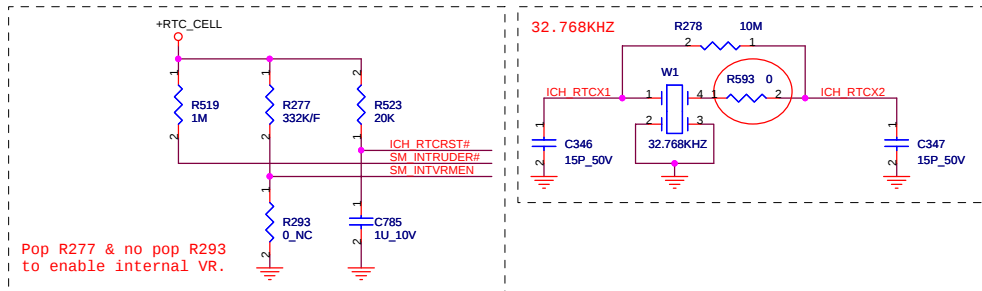


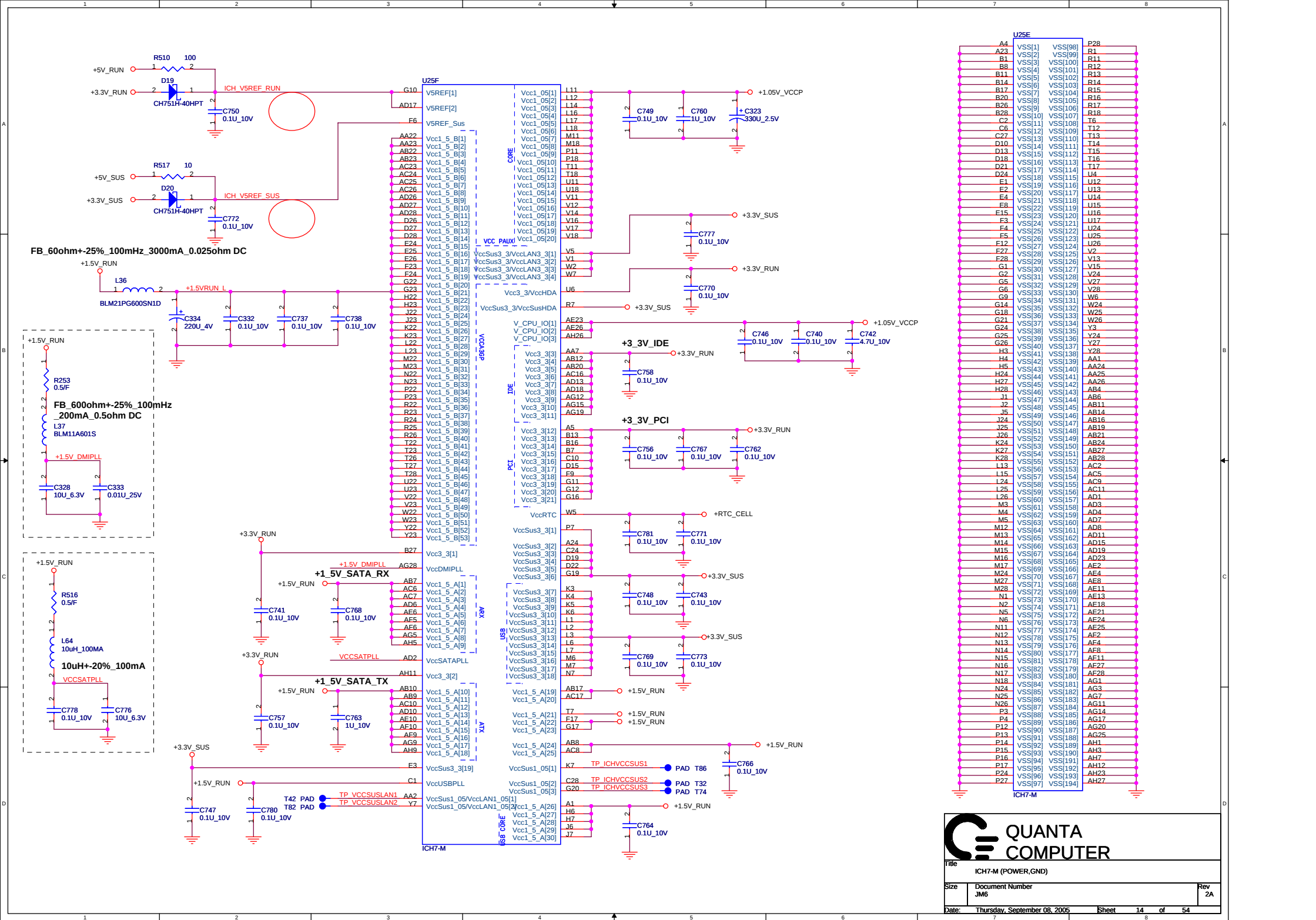


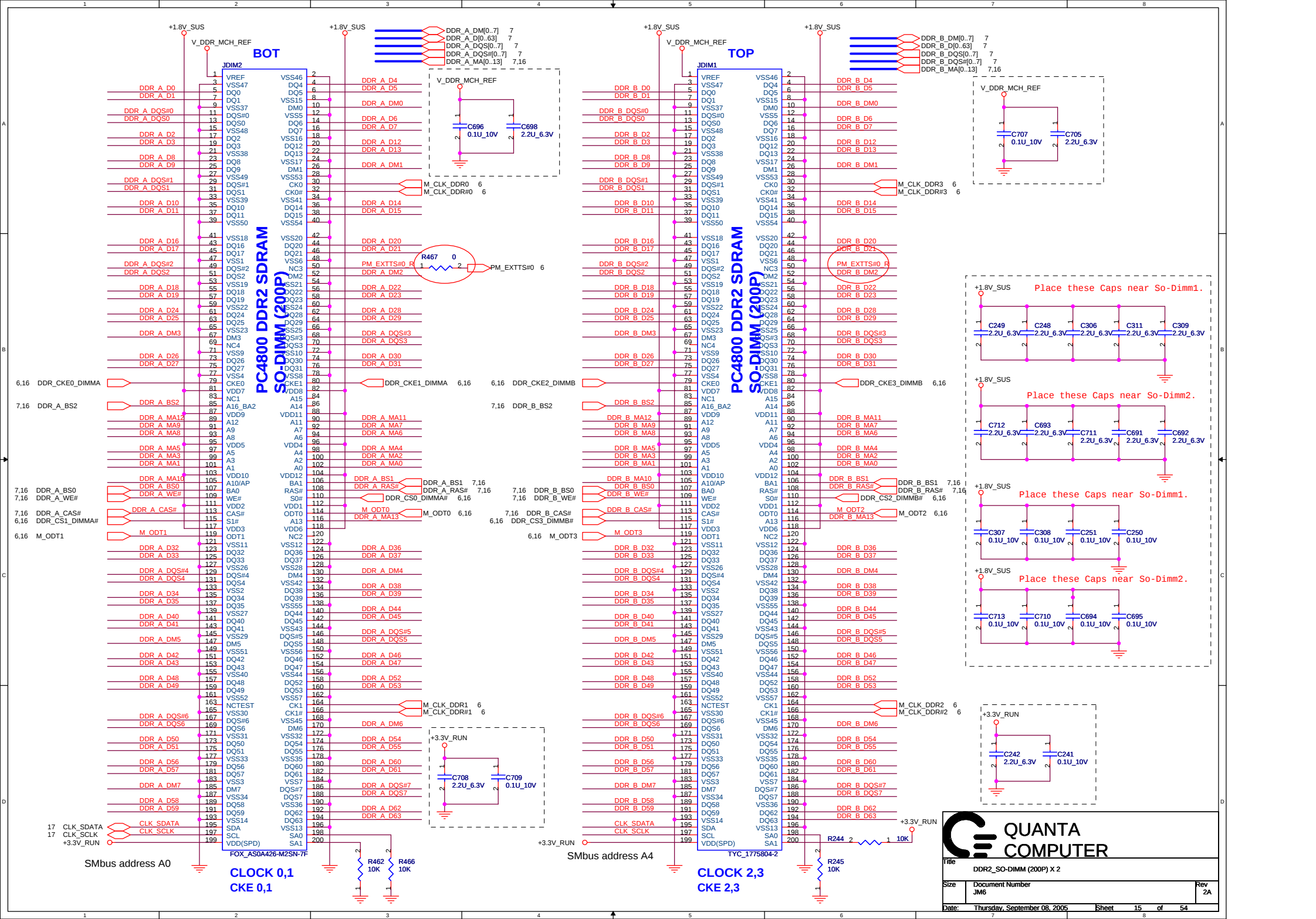


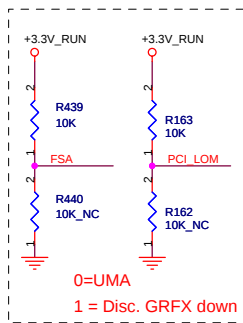
QUANTA
COMPUTER

Title Calistoga (VSS)		
Size JM6	Document Number	Rev 2A
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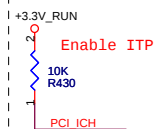
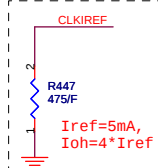
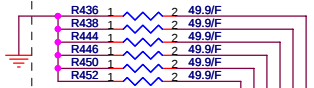






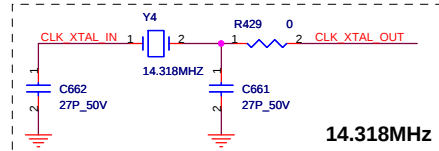
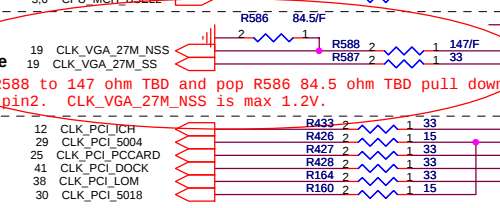


Place these termination to close CK410M.

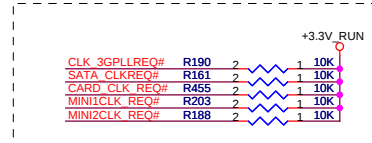


Discrete

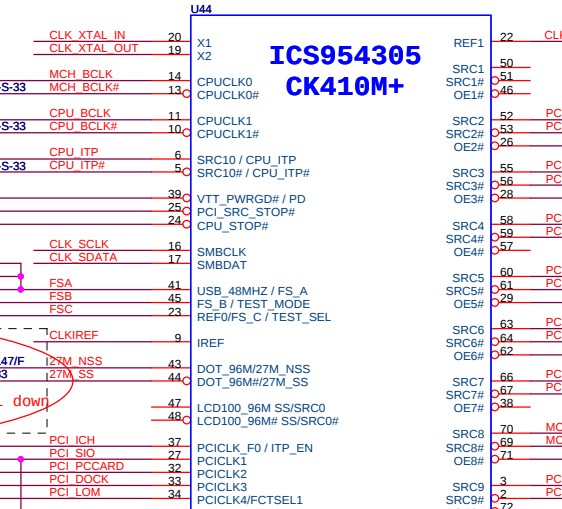
Change R588 to 147 ohm TBD and pop R586 84.5 ohm TBD pull down on R588 pin2. CLK_VGA_27M_NSS is max 1.2V.



14.318MHz

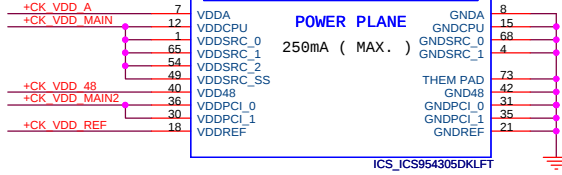
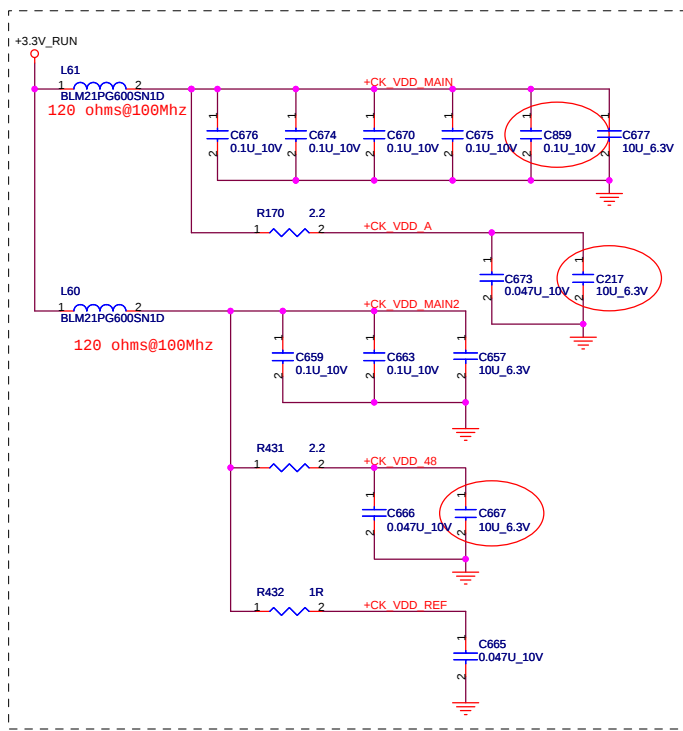


ICS954305
CK410M+



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	0	0	200	100	33
1	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

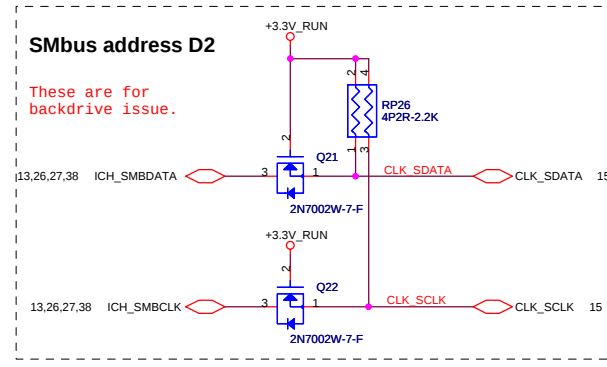
Discrete



POWER PLANE
250mA (MAX.)

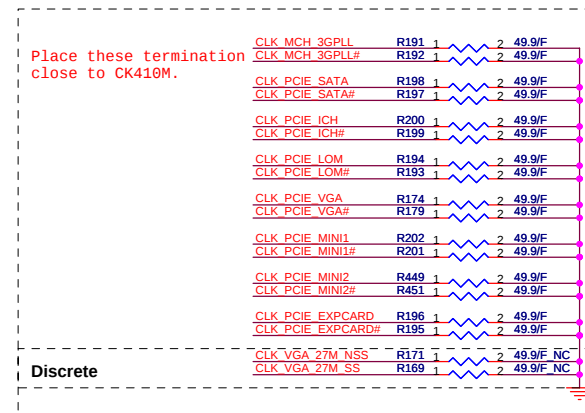
SMBus address D2

These are for backdrive issue.



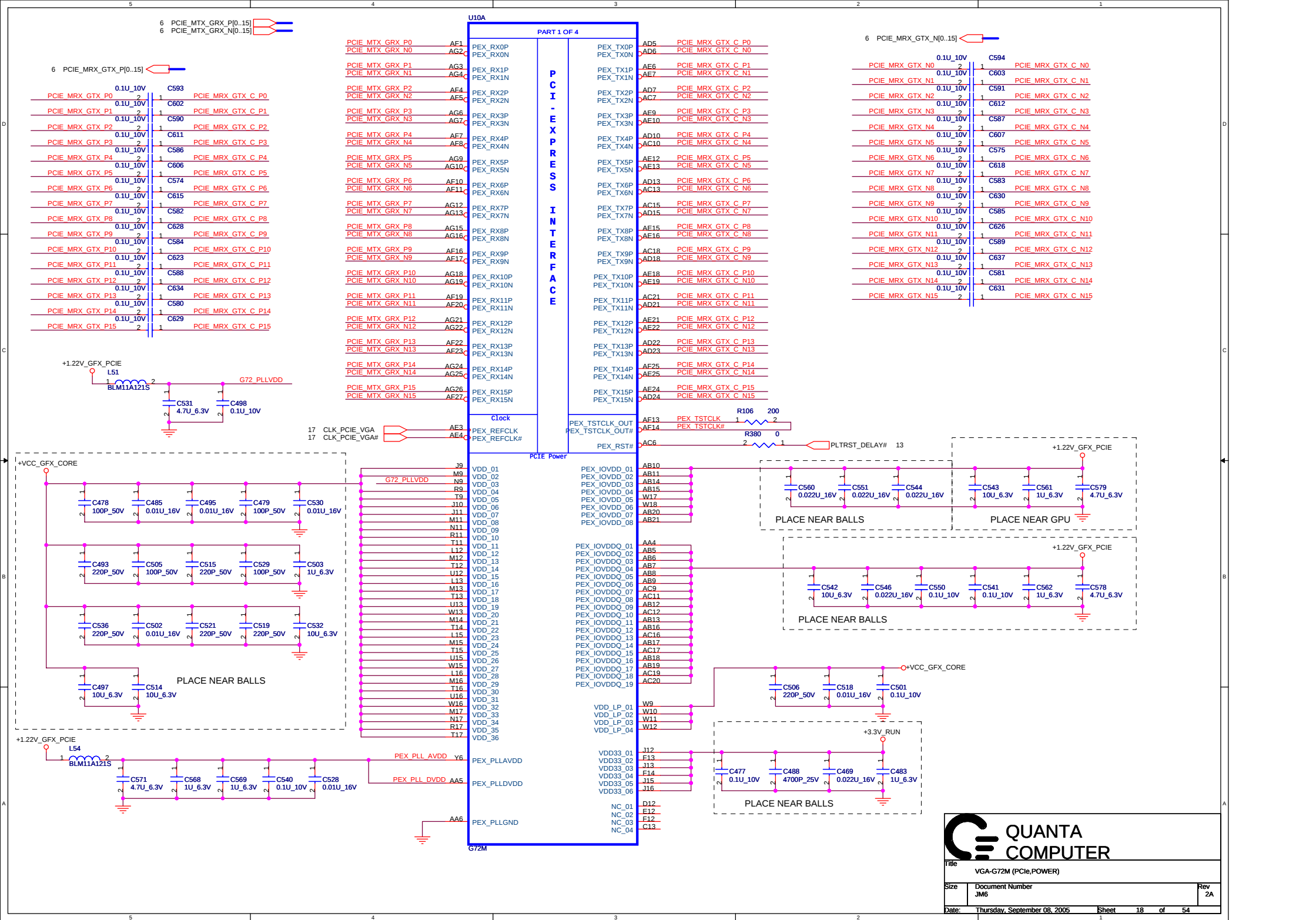
PCI_LOM = FCTSEL1

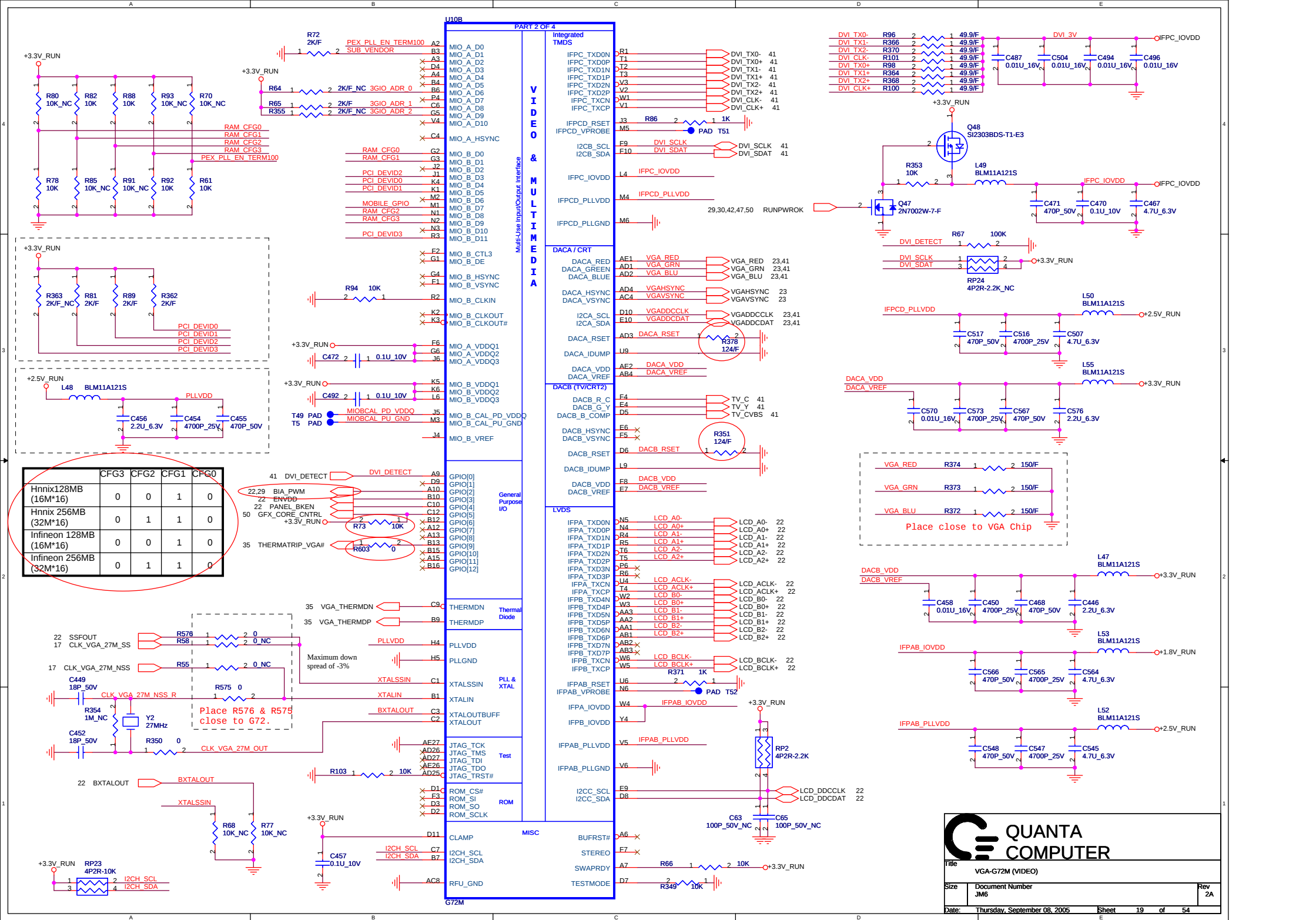
FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRC0	SRC0



Discrete

QUANTA
COMPUTER





FB_CMD[0..26] 21
FBD[0..63] 21
FBDQM[0..7] 21
FBDQS[0..7] 21
FBDQS#0..7 21

U10C

Part 3 of 4

MEMORY INTERFACE

FBD0 A26 FB_DQ0
FBD1 C24 FB_DQ1
FBD2 B24 FB_DQ2
FBD3 A24 FB_DQ3
FBD4 C22 FB_DQ4
FBD5 A25 FB_DQ5
FBD6 B25 FB_DQ6
FBD7 D23 FB_DQ7
FBD8 G22 FB_DQ8
FBD9 J23 FB_DQ9
FBD10 E24 FB_DQ10
FBD11 F23 FB_DQ11
FBD12 J24 FB_DQ12
FBD13 F24 FB_DQ13
FBD14 G23 FB_DQ14
FBD15 H24 FB_DQ15
FBD16 D16 FB_DQ16
FBD17 E16 FB_DQ17
FBD18 D17 FB_DQ18
FBD19 F18 FB_DQ19
FBD21 E19 FB_DQ20
FBD22 D20 FB_DQ21
FBD23 D19 FB_DQ22
FBD24 A18 FB_DQ23
FBD25 B18 FB_DQ24
FBD26 A19 FB_DQ25
FBD27 B19 FB_DQ26
FBD28 D18 FB_DQ27
FBD29 C19 FB_DQ28
FBD30 C16 FB_DQ29
FBD31 C18 FB_DQ30
FBD32 N26 FB_DQ31
FBD33 N25 FB_DQ32
FBD34 R25 FB_DQ33
FBD35 R26 FB_DQ34
FBD36 R27 FB_DQ35
FBD37 T27 FB_DQ36
FBD38 T25 FB_DQ37
FBD39 T26 FB_DQ38
FBD40 AB23 FB_DQ39
FBD41 Y24 FB_DQ40
FBD42 AB24 FB_DQ41
FBD43 AB22 FB_DQ42
FBD44 AC24 FB_DQ43
FBD45 AC22 FB_DQ44
FBD46 AA23 FB_DQ45
FBD47 AA22 FB_DQ46
FBD48 T24 FB_DQ47
FBD49 T23 FB_DQ48
FBD50 R24 FB_DQ49
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FBD57 AA27 FB_DQ56
FBD58 AB25 FB_DQ57
FBD59 AB26 FB_DQ58
FBD60 AB27 FB_DQ59
FBD61 AB28 FB_DQ60
FBD62 AA25 FB_DQ61
FBD63 W25 FB_DQ62
FB_DQ63

FB_CMD0 G27 FB_CMD0
FB_CMD1 D25 FB_CMD1
FB_CMD2 E26 FB_CMD2
FB_CMD3 E25 FB_CMD3
FB_CMD4 G25 FB_CMD4
FB_CMD5 J25 FB_CMD5
FB_CMD6 J27 FB_CMD6
FB_CMD7 M26 FB_CMD7
FB_CMD8 C27 FB_CMD8
FB_CMD9 C25 FB_CMD9
FB_CMD10 D24 FB_CMD10
FB_CMD11 N27 FB_CMD11
FB_CMD12 G24 FB_CMD12
FB_CMD13 J26 FB_CMD13
FB_CMD14 M27 FB_CMD14
FB_CMD15 C26 FB_CMD15
FB_CMD16 M25 FB_CMD16
FB_CMD17 D26 FB_CMD17
FB_CMD18 D27 FB_CMD18
FB_CMD19 K26 FB_CMD19
FB_CMD20 K25 FB_CMD20
FB_CMD21 K24 FB_CMD21
FB_CMD22 P9 FB_CMD22
FB_CMD23 K27 FB_CMD23
FB_CMD24 G26 FB_CMD24
FB_CMD25 B27 FB_CMD25
FB_CMD26 N24 FB_CMD26

FB_DQM0 D21 FBDQM0
FB_DQM1 E22 FBDQM1
FB_DQM2 F20 FBDQM2
FB_DQM3 A21 FBDQM3
FB_DQM4 V27 FBDQM4
FB_DQM5 W22 FBDQM5
FB_DQM6 V22 FBDQM6
FB_DQM7 V24 FBDQM7

FB_DQS_RN0 A22 FBDQS#0
FB_DQS_RN1 E22 FBDQS#1
FB_DQS_RN2 E21 FBDQS#2
FB_DQS_RN3 B21 FBDQS#3
FB_DQS_RN4 V26 FBDQS#4
FB_DQS_RN5 W23 FBDQS#5
FB_DQS_RN6 V23 FBDQS#6
FB_DQS_RN7 W27 FBDQS#7

FB_DQS_WP0 B22 FBDQS0
FB_DQS_WP1 D22 FBDQS1
FB_DQS_WP2 C21 FBDQS2
FB_DQS_WP3 E21 FBDQS3
FB_DQS_WP4 V25 FBDQS4
FB_DQS_WP5 W24 FBDQS5
FB_DQS_WP6 U24 FBDQS6
FB_DQS_WP7 W26 FBDQS7

FBVTT_01 E15
FBVTT_02 E16
FBVTT_03 J17
FBVTT_04 J18
FBVTT_05 L19
FBVTT_06 R19
FBVTT_07 U19
FBVTT_08 W19
FBVTT_09
FBVTT_10

FBVDDQ_01 E17
FBVDDQ_02 E19
FBVDDQ_03 J19
FBVDDQ_04 M19
FBVDDQ_05 T19
FBVDDQ_06 J22
FBVDDQ_07 L22
FBVDDQ_08 U22
FBVDDQ_09 Y22
FBVDDQ_10

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FBCAL_PU_GND E13
FBCAL_TERM_GND H22

U10D

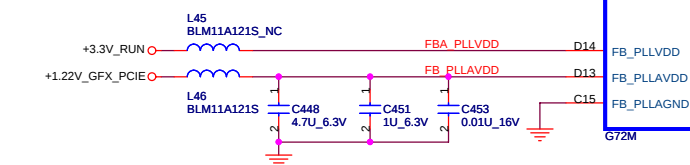
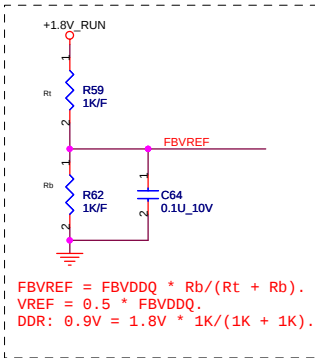
Part 4 of 4

GND

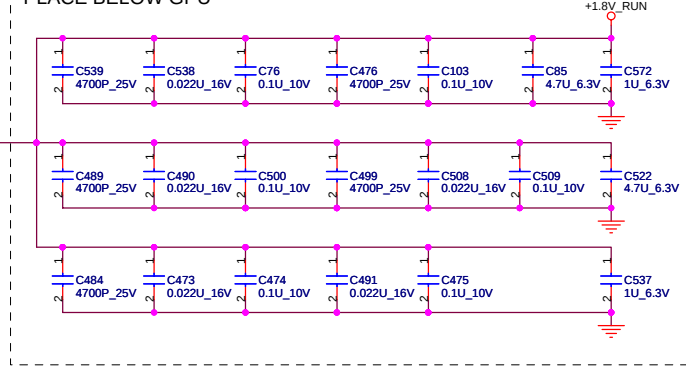
B2 GND_01
E2 GND_02
H2 GND_03
L2 GND_04
P2 GND_05
U2 GND_06
Y2 GND_07
AC2 GND_08
AE2 GND_09
AE3 GND_10
B5 GND_11
E5 GND_12
L5 GND_13
P5 GND_14
U5 GND_15
Y5 GND_16
AC5 GND_17
HE GND_18
AE6 GND_19
B6 GND_20
F8 GND_21
AD8 GND_22
K9 GND_23
P9 GND_24
V9 GND_25
AD9 GND_26
AE9 GND_27
B11 GND_28
E11 GND_29
L11 GND_30
P11 GND_31
U11 GND_32
AD11 GND_33
GND_34
P12 GND_35
R12 GND_36
GND_37
AD12 GND_38
AE12 GND_39
N13 GND_40
P13 GND_41
B14 GND_42
E14 GND_43
J14 GND_44
L14 GND_45
N14 GND_46
GND_47

GND_48 R14
GND_49 U14
GND_50 W14
GND_51 AC14
GND_52 AD14
GND_53 N15
GND_54 P15
GND_55 R15
GND_56 AE15
GND_57 N16
GND_58 P16
GND_59 R16
GND_60 AD16
GND_61 B17
GND_62 E17
GND_63 L17
GND_64 P17
GND_65 U17
GND_66 AD17
GND_67 AE18
GND_68 K19
GND_69 P19
GND_70 V19
GND_71 AD19
GND_72 B20
GND_73 E20
GND_74 AD20
GND_75 AE21
GND_76 B23
GND_77 E23
GND_78 H23
GND_79 L23
GND_80 P23
GND_81 U23
GND_82 Y23
GND_83 AC23
GND_84 AE24
GND_85 B26
GND_86 E26
GND_87 H26
GND_88 L26
GND_89 P26
GND_90 U26
GND_91 Y26
GND_92 AC26
GND_93 AE26
GND_94

G72M



PLACE BELOW GPU



Title VGA-G72M (MEMORY.GUD)

Size Document Number JM6

Date: Thursday, September 08, 2005

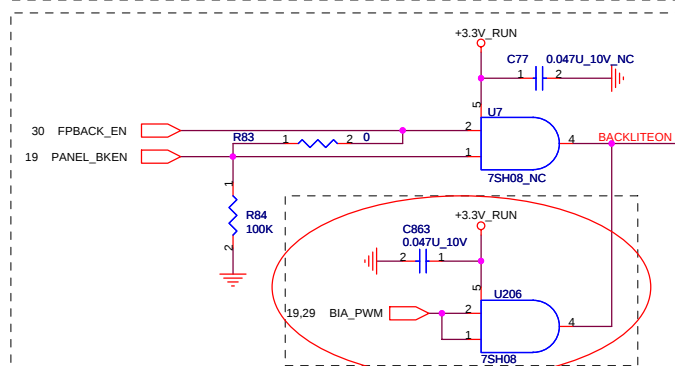
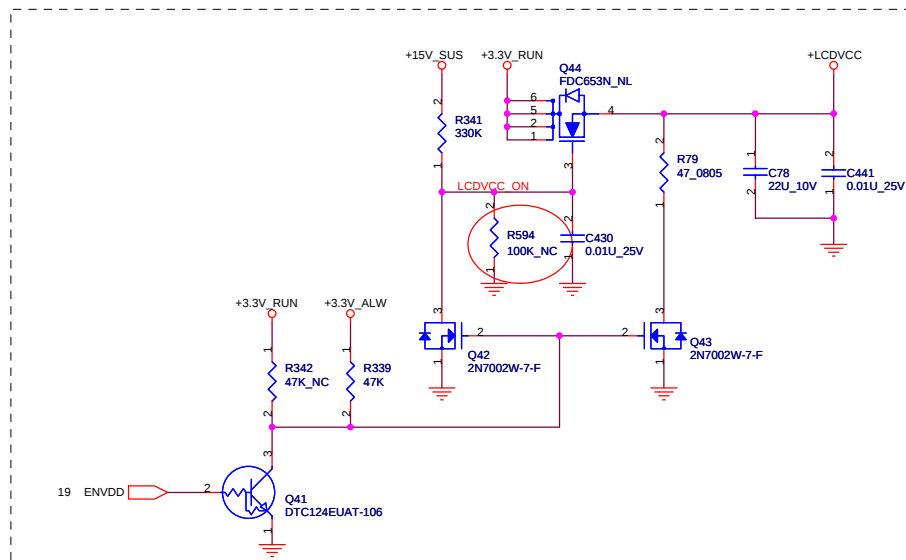
Rev 2A

Sheet 20 of 54

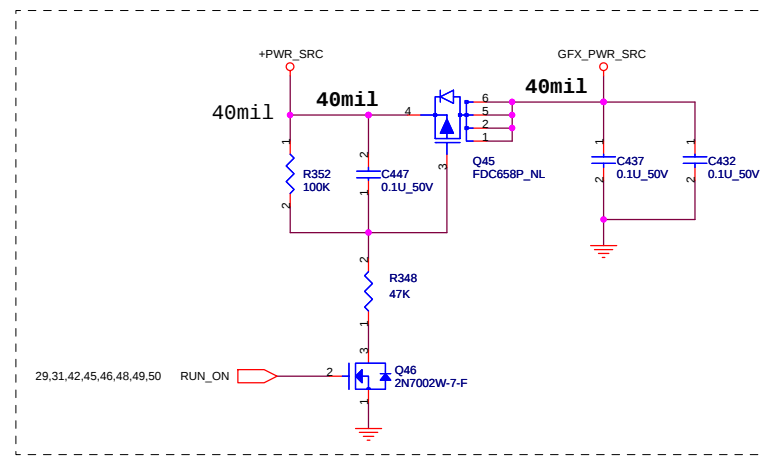
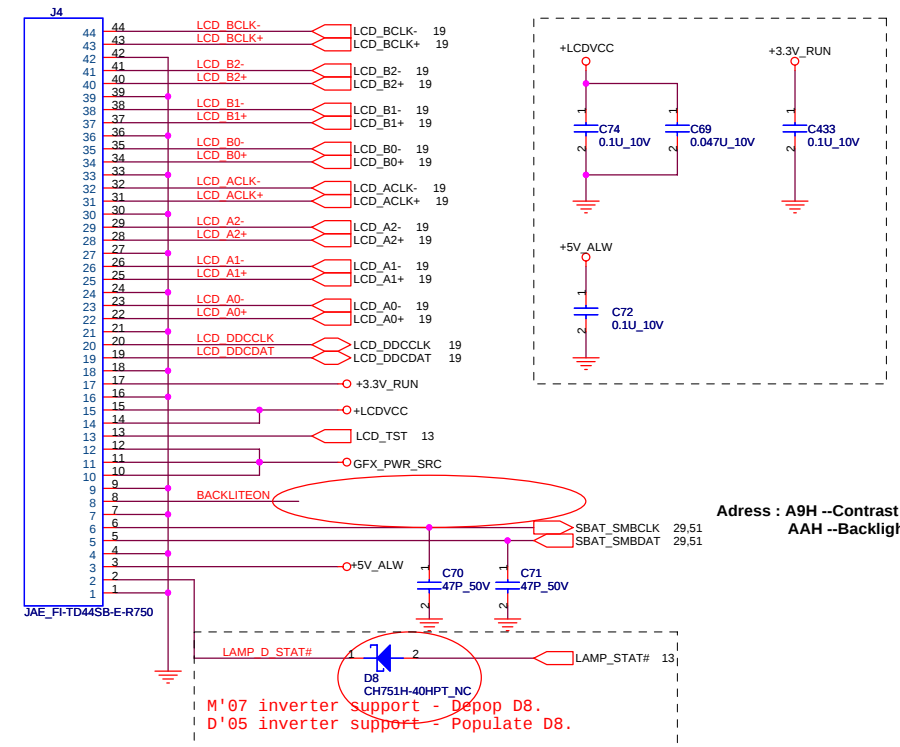
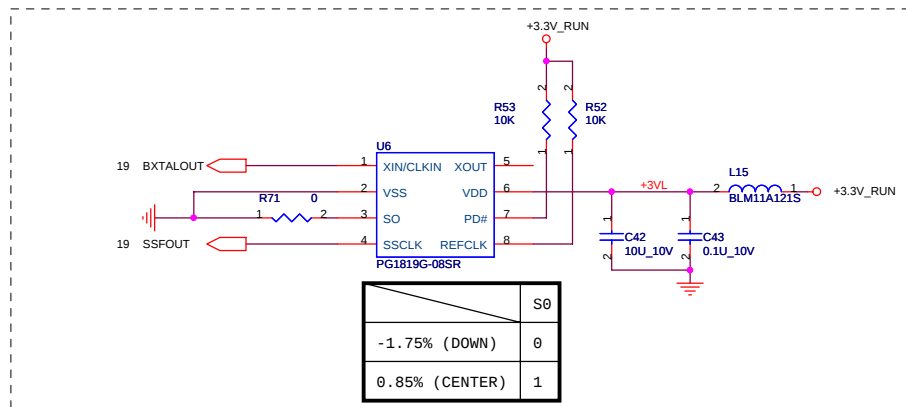


Rev

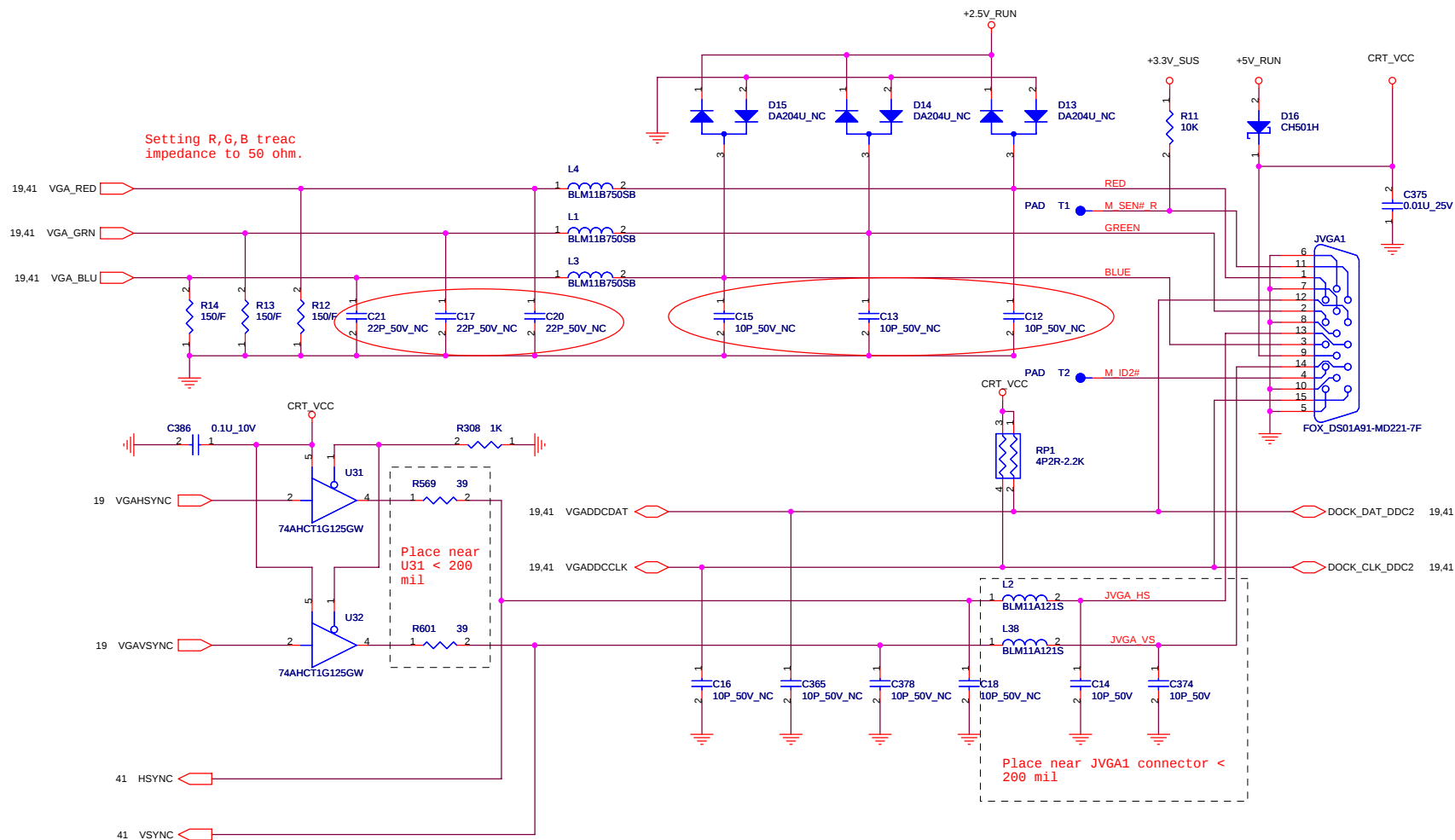
54



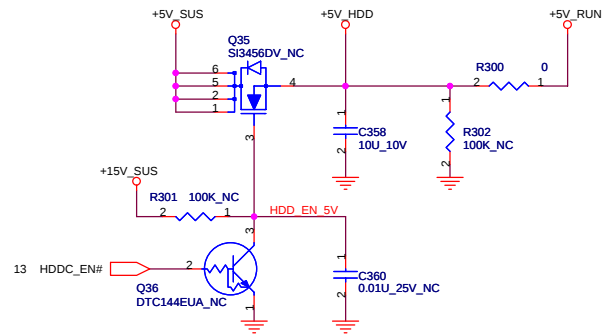
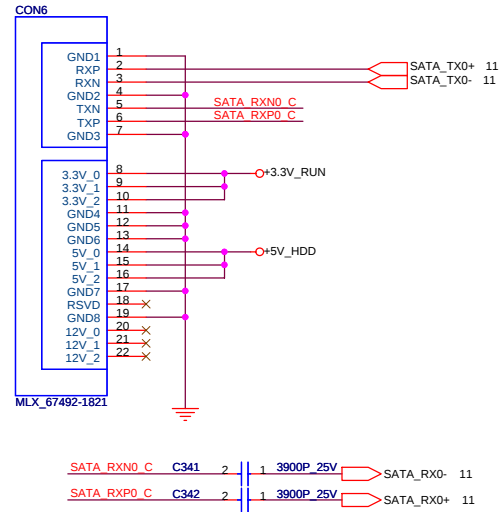
M'07 inverter support - Populate R83,U206,C863 Depop U7,C77.
D'05 inverter support - Populate U7,C77; Depop R83,U206,C863.



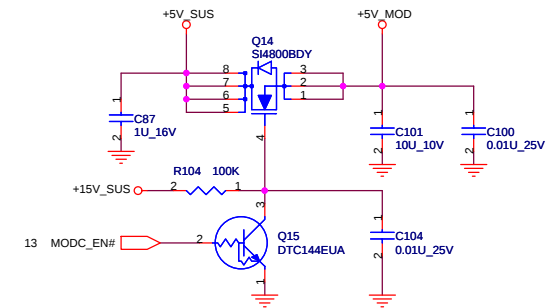
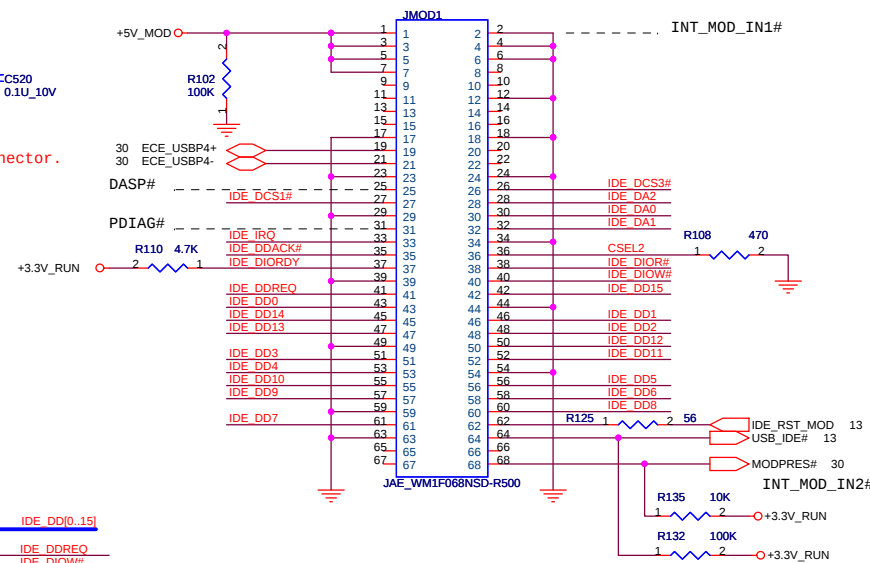
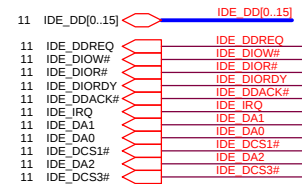
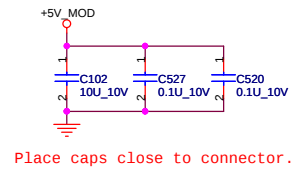
	S0
-1.75% (DOWN)	0
0.85% (CENTER)	1



SATA Connector.



ODD Connector.



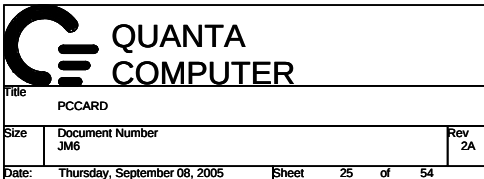
Title	IDE (HDD&CD_ROM)
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Size	Document Number JM6
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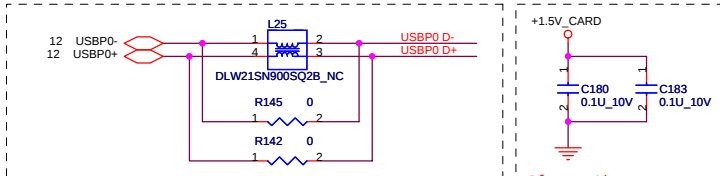
Rev
2A

Date: Thursday, September 08, 2005

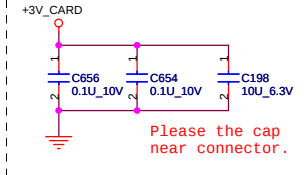
Sheet 24 of 54



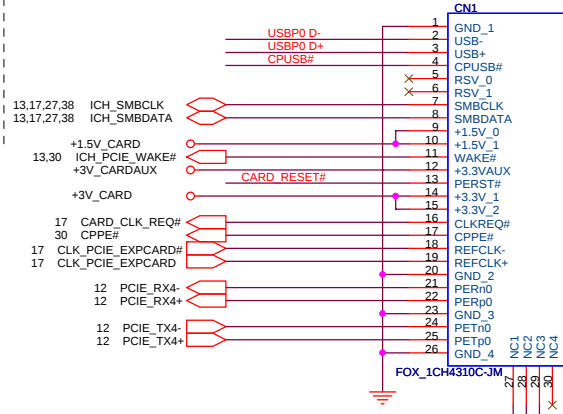
Express Card



Please the cap near connector.

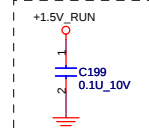
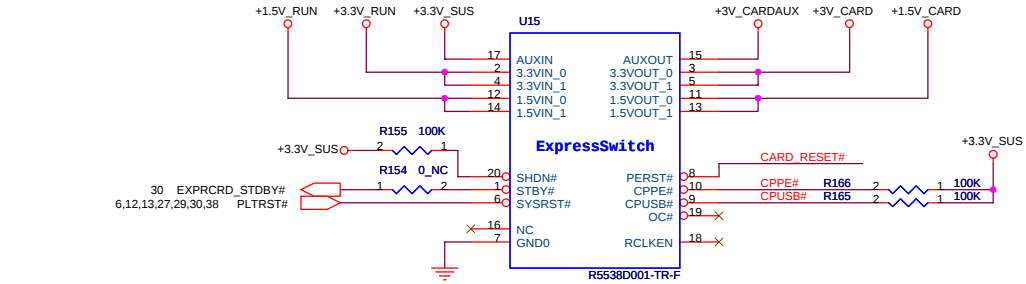


Please the cap near connector.

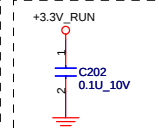


JAE PX10FS16PH-26P

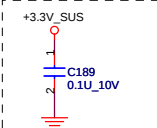
PCI-Express TX and RX direct to connector.



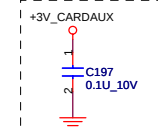
Please the cap near pin 12 & 14(1.5VIN).



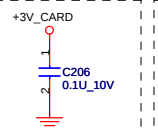
Please the cap near pin 2 & 4 (3.3VIN).



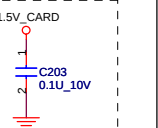
Please the cap near pin 17 (AUXIN).



Please the cap near pin 15 (AUXOUT).



Please the cap near pin 3 & 5 (3.3VOUT).



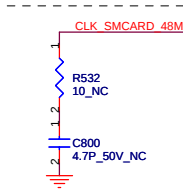
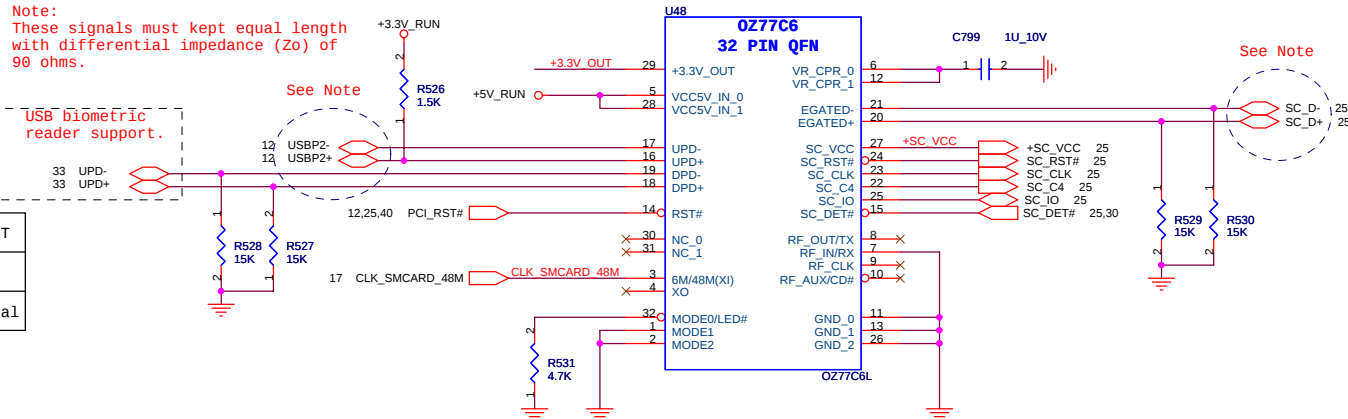
Please the cap near pin 11 & 13(1.5VOUT).

Smart Card

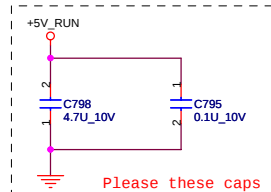
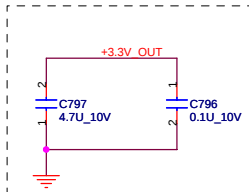
Note:
These signals must kept equal length with differential impedance (Z_0) of 90 ohms.

USB biometric reader support.

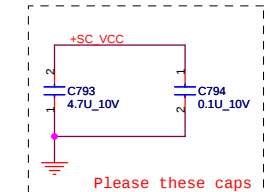
MODE1	CLOCK INPUT
LOW	48MHz
HIGH	6MHz Crystal



Reserved for EMI. Placce the parts near pin 45.



Please these caps near OZ77C6L.

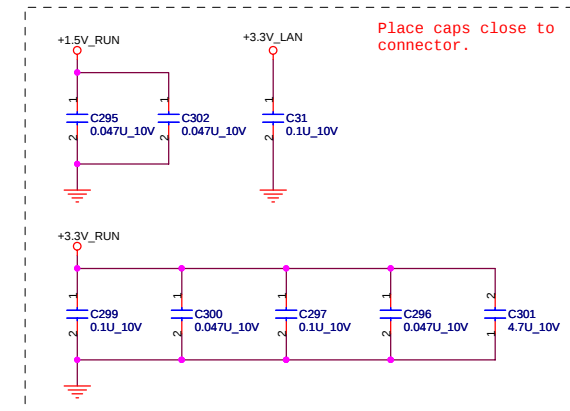
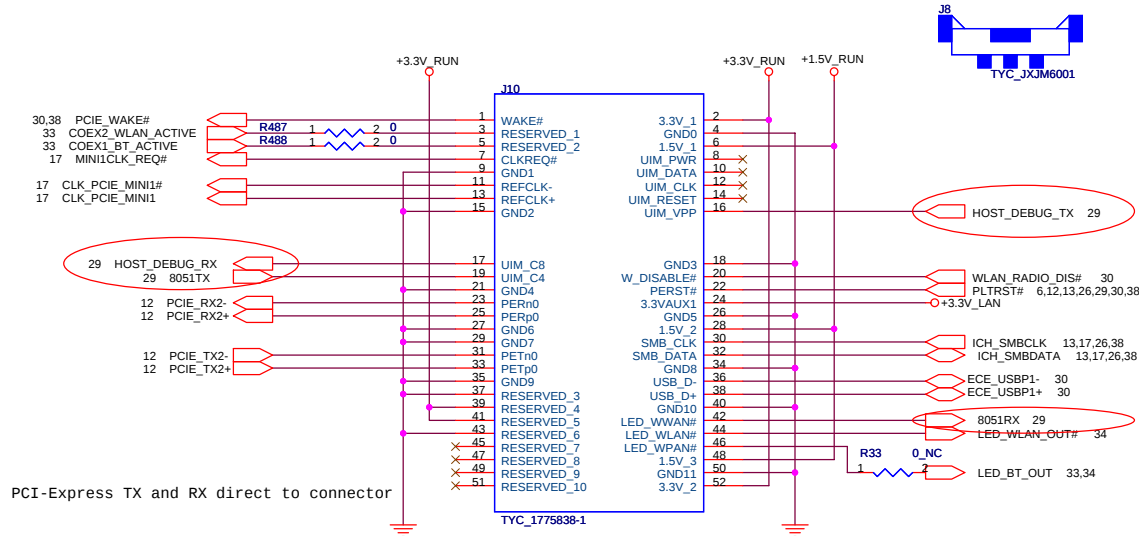


Please these caps near OZ77C6L.

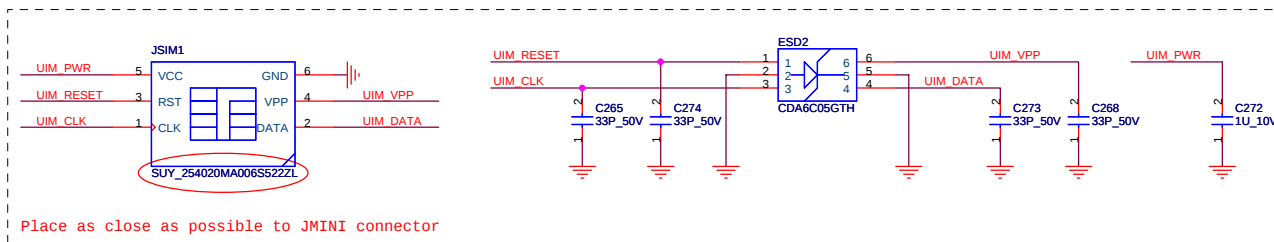
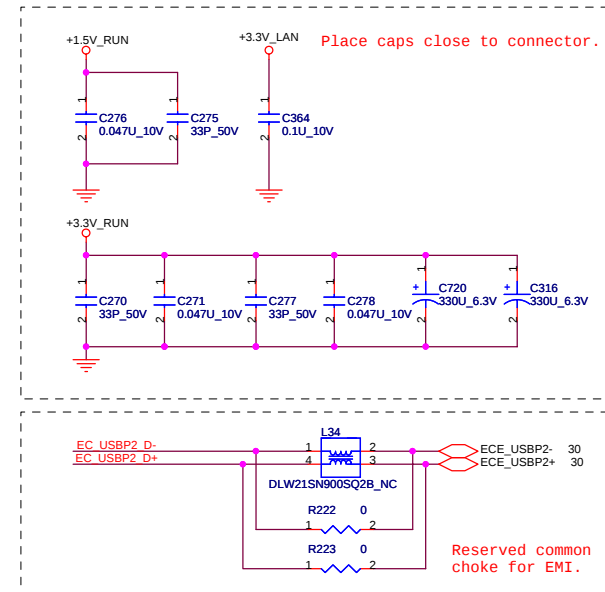
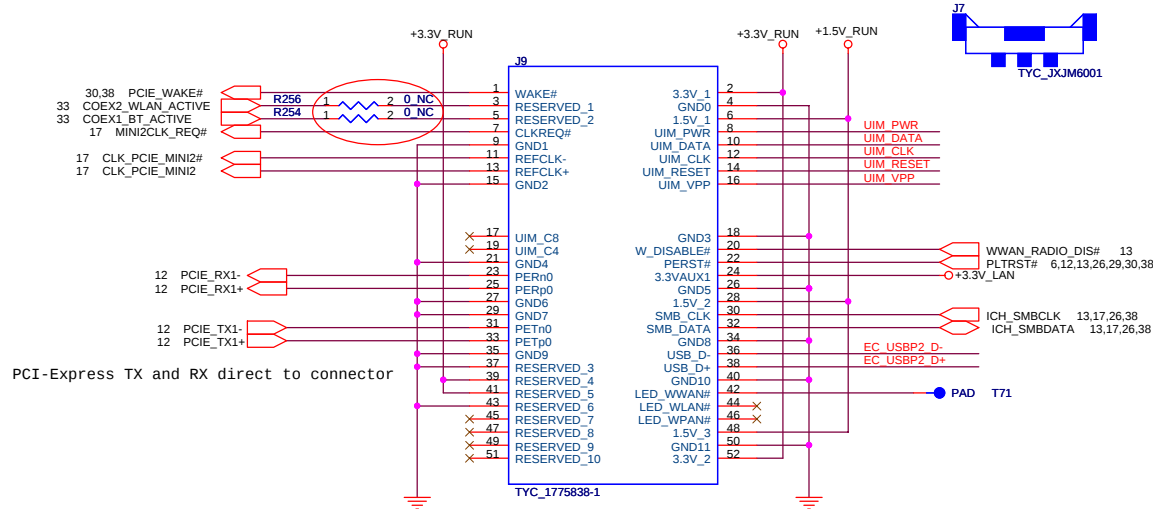
QUANTA COMPUTER

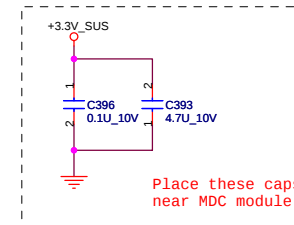
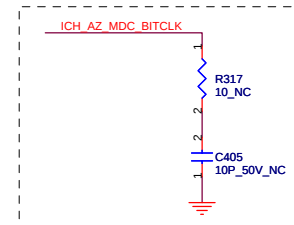
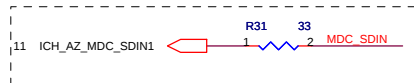
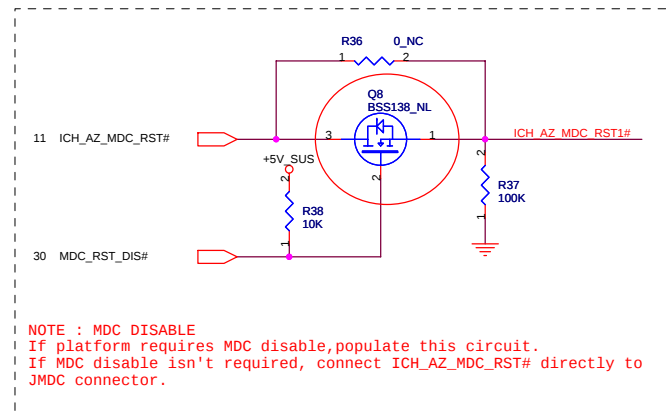
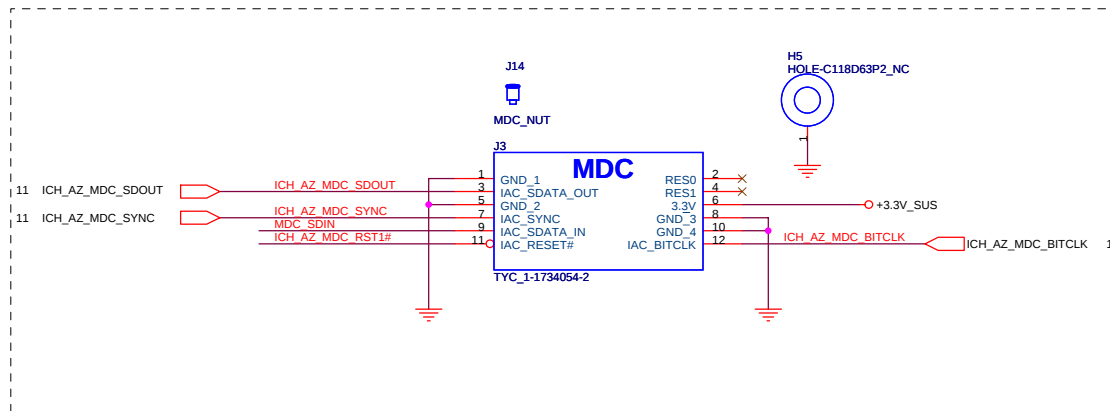
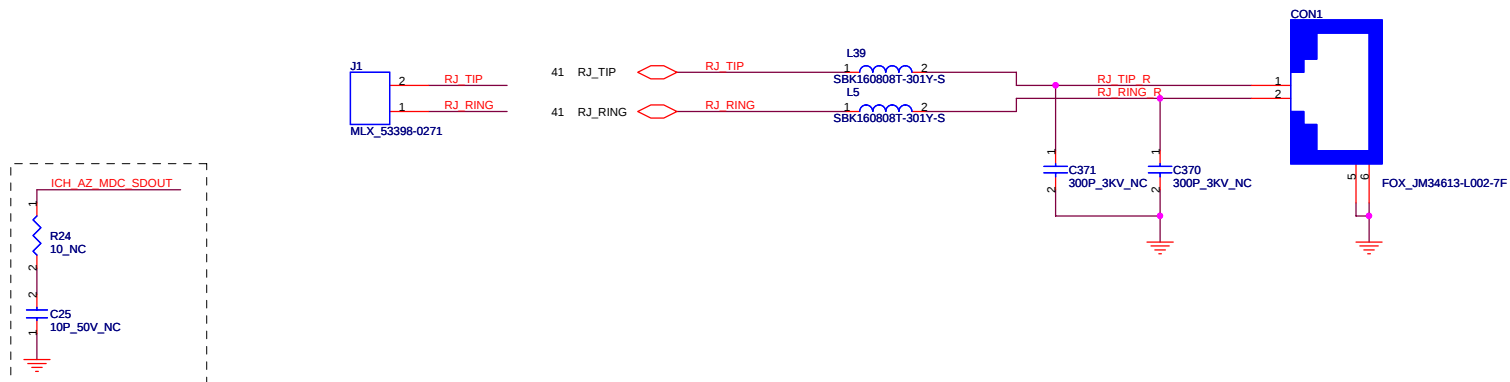
Title ExpressCard/SmartCard		
Size JM6	Document Number	Rev 2A
Date: Thursday, September 08, 2005	Sheet 26	of 54

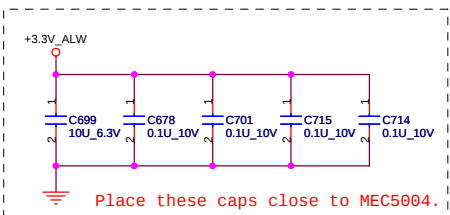
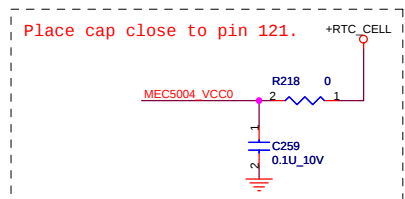
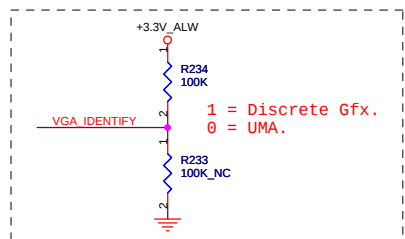
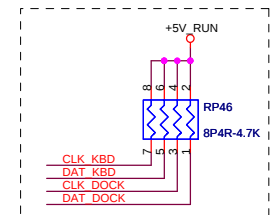
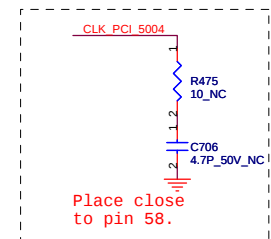
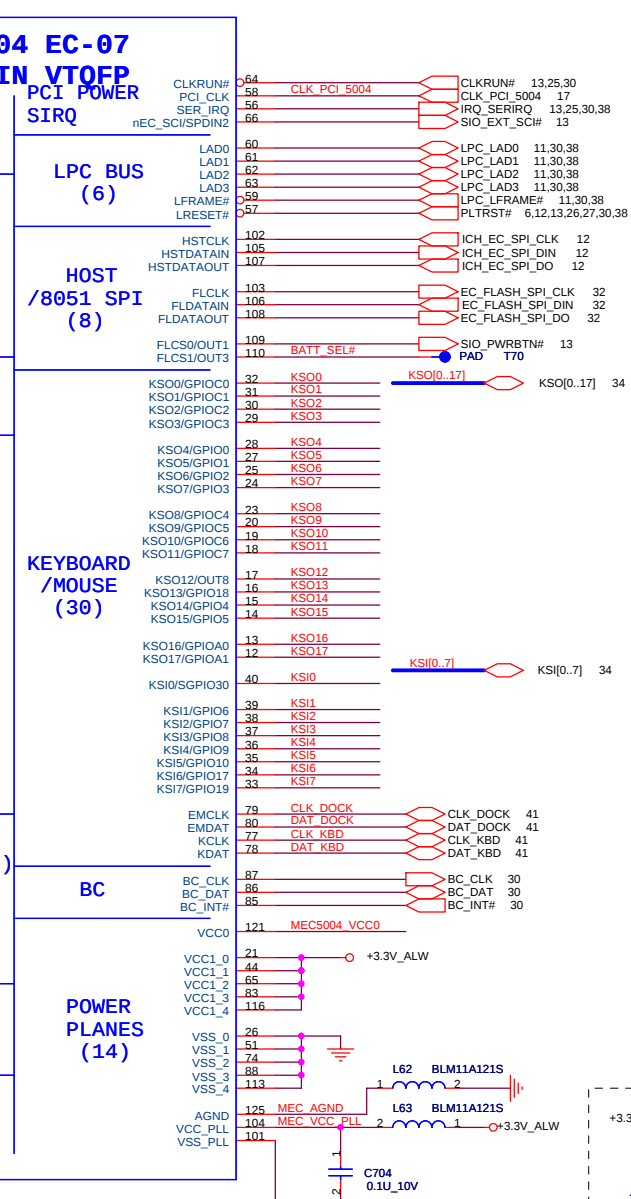
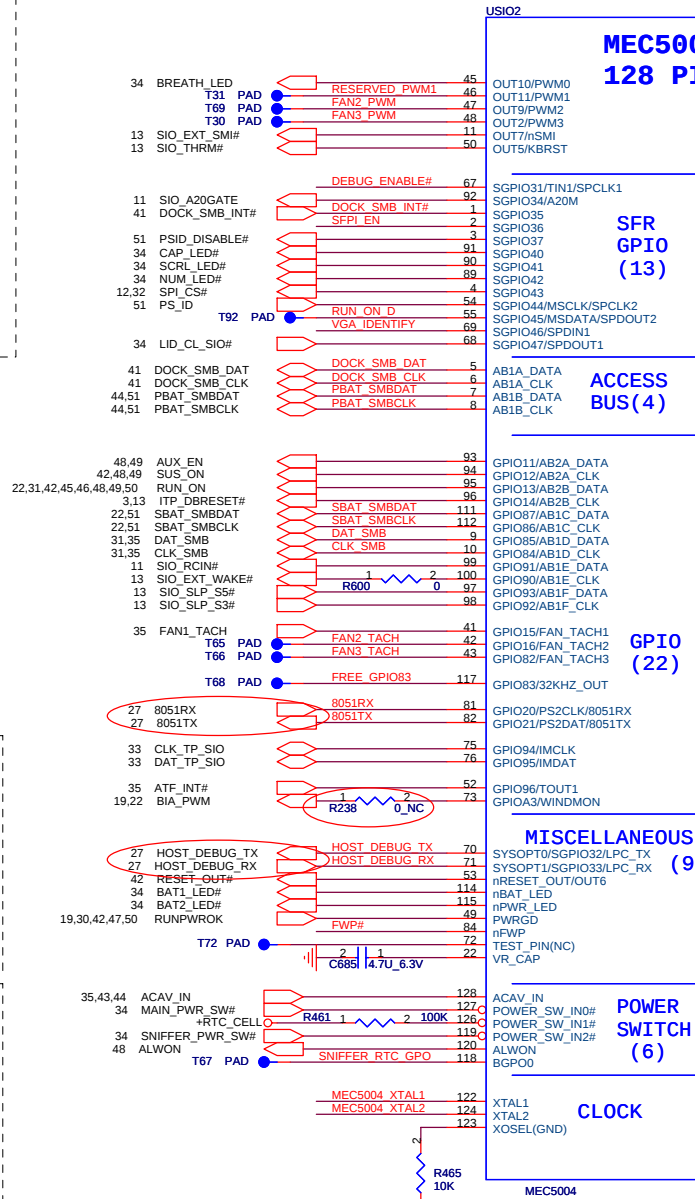
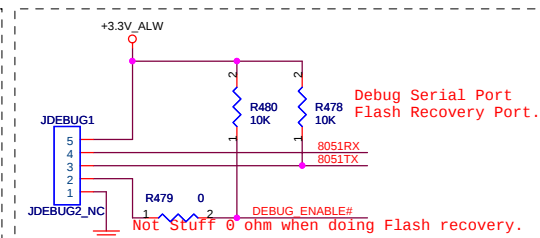
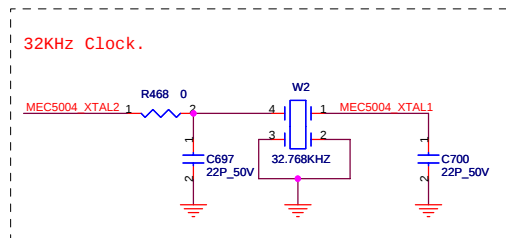
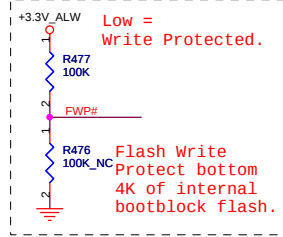
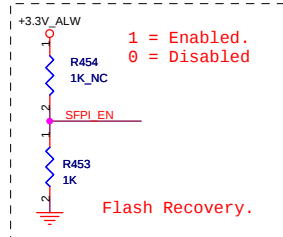
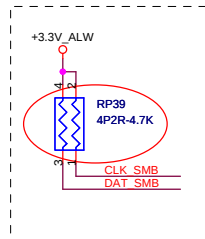
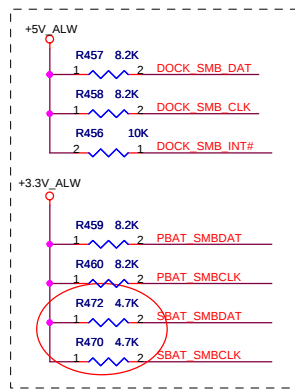
MiniCard WLAN connector

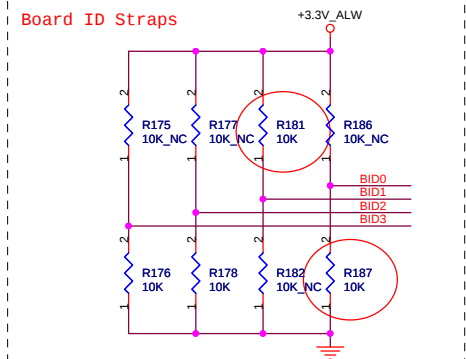
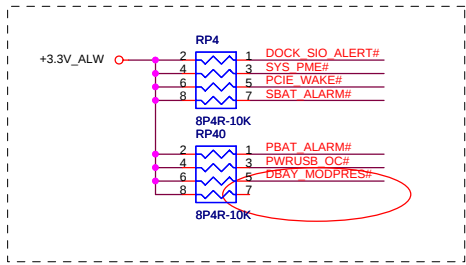


MiniCard WWAN connector

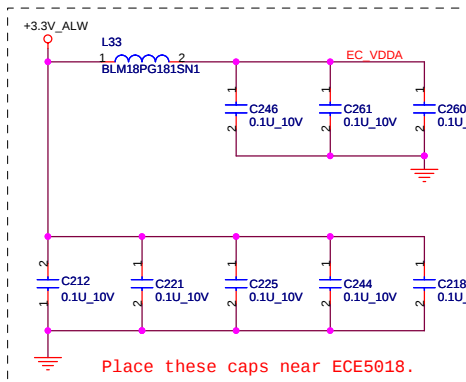
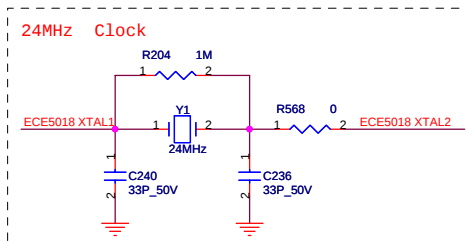




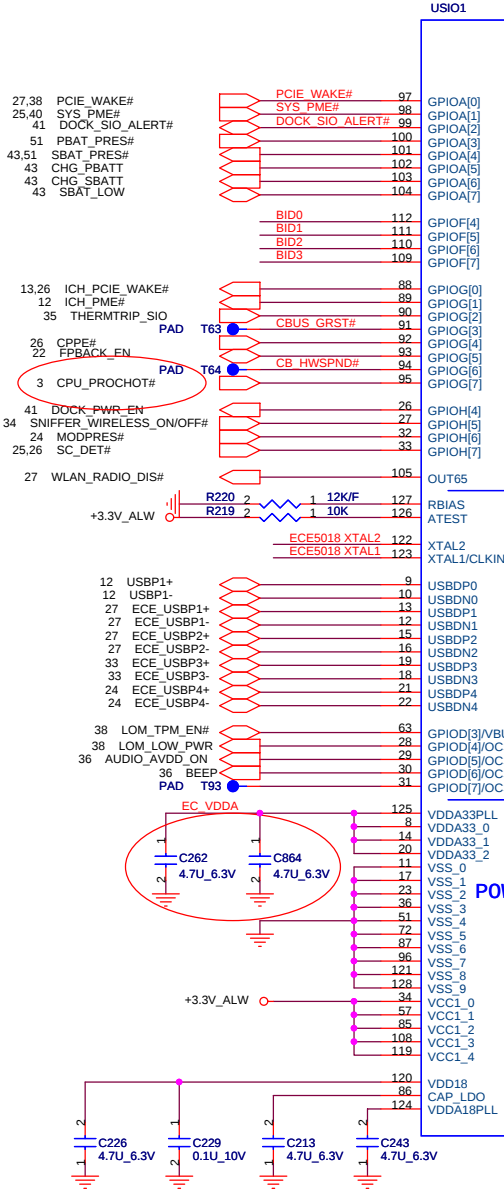




BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	ENG1 (M00)
0	0	0	1	ENG2 (X00)
0	0	1	0	ENG3 (X01)
0	0	1	1	ENG4 (X02)
0	1	0	0	QT (X03)
0	1	0	1	RAMP (A00)



Place these caps near ECE5018.



ECE5018 Midway 128 PIN VTQFP

PCI POWER SIRQ (3)

LPC BUS (8)

DOCKING LPC (8)

BC

PARALLEL PORT (17)

UART (8)

IRCC (8)

SIO RESET (4)

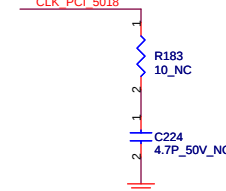
MISCELLANEOUS (4)

GPIO (25)

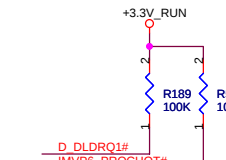
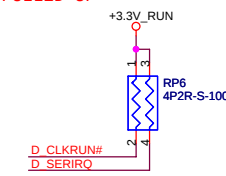
USB (19)

POWER PLANES (21)

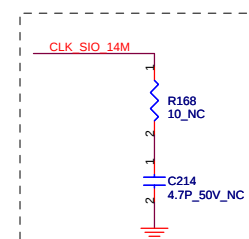
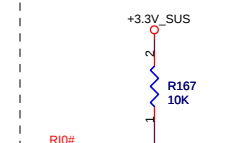
Place closely pin USIO2.



DOCKING
PULLED UP

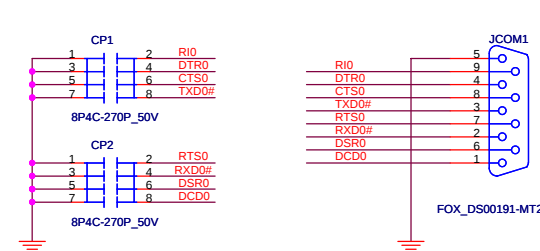
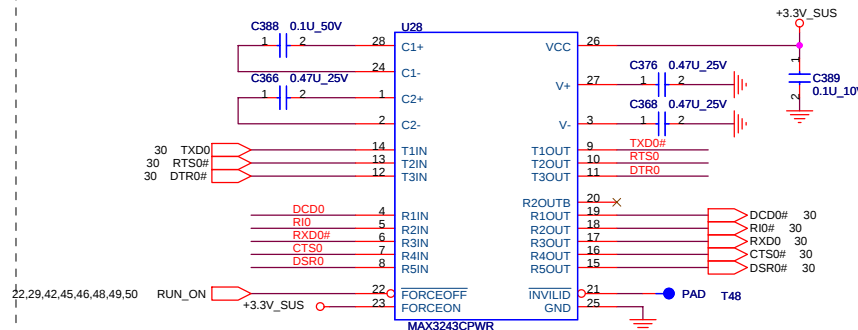
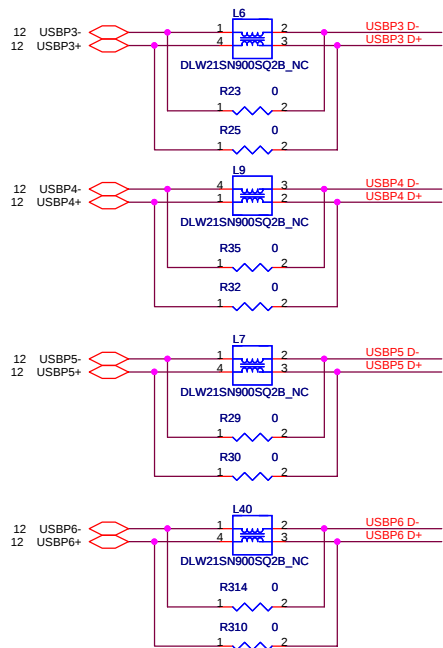


To MDC disable ckt.
Reserved.
To Express Card Pwr Switch.

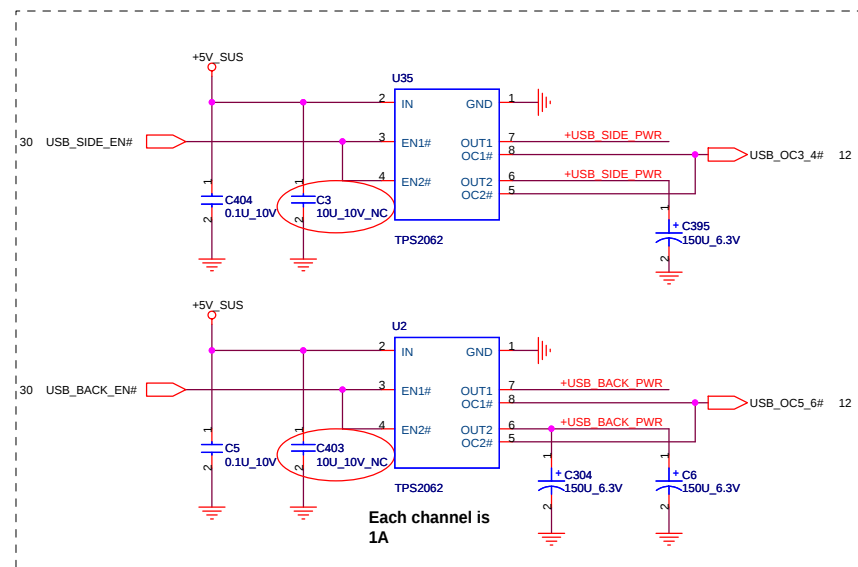


**QUANTA
COMPUTER**

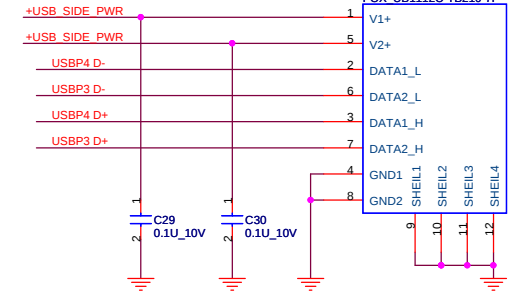
Title Ultra I/O Controller EEC5018			
Size JM6	Document Number	Rev 2A	
Date: Thursday, September 08, 2005	Sheet 30	of 54	



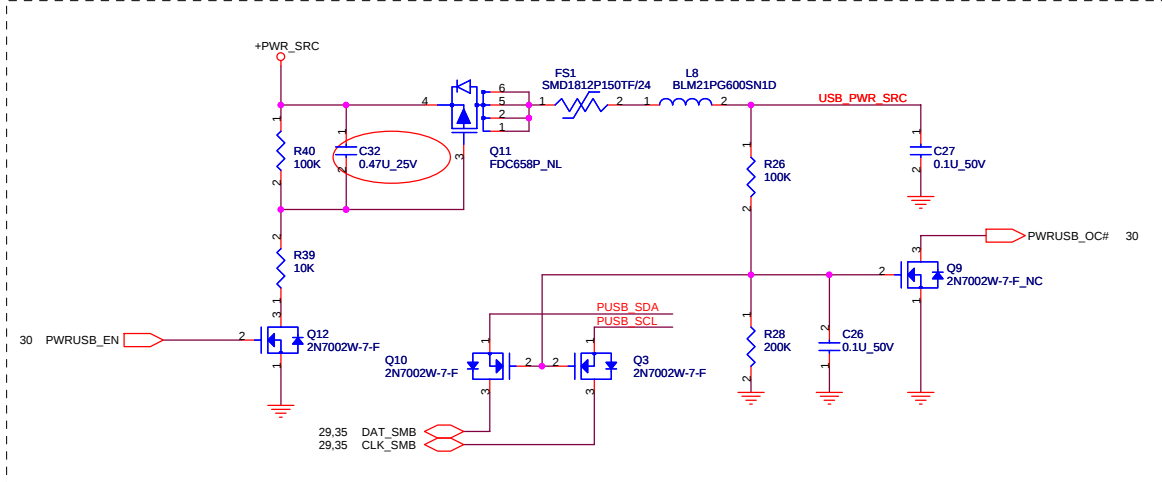
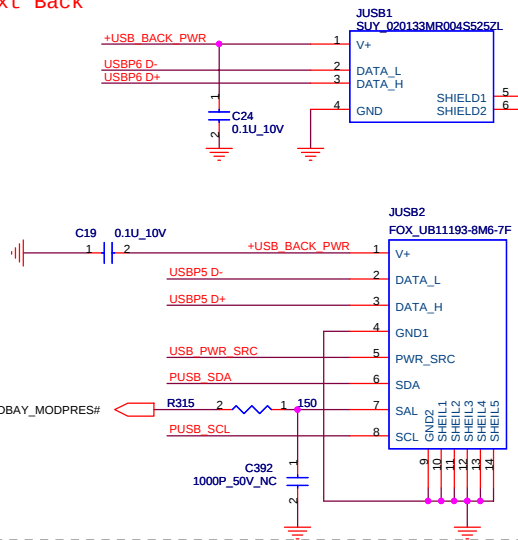
Place these beads close to JCOM1 as soon as possible
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out



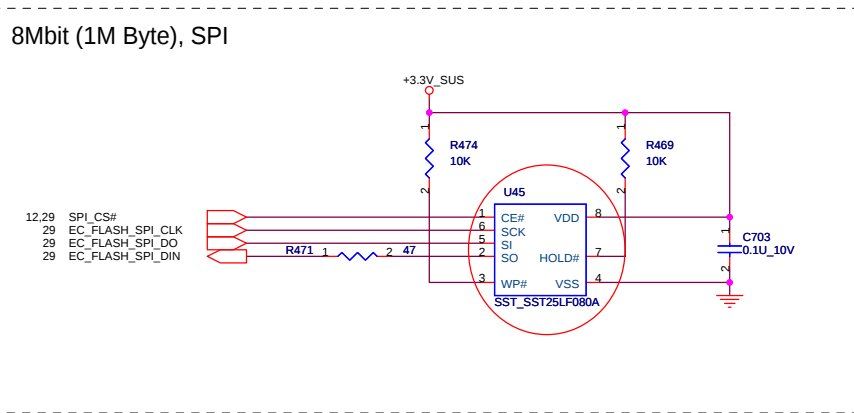
Ext Side



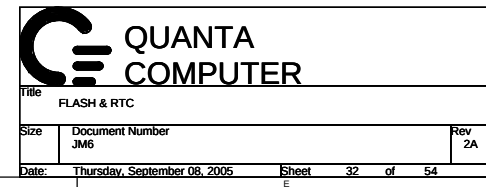
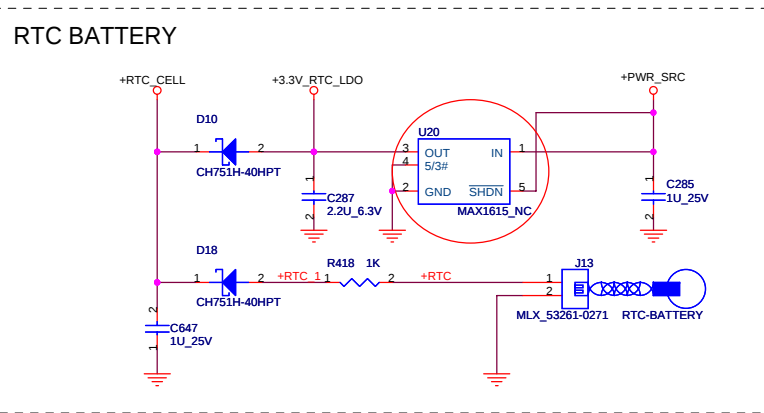
Ext Back

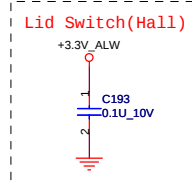
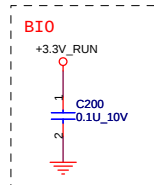


8Mbit (1M Byte), SPI

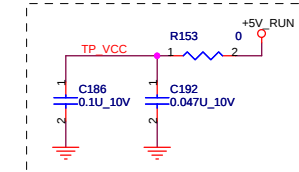
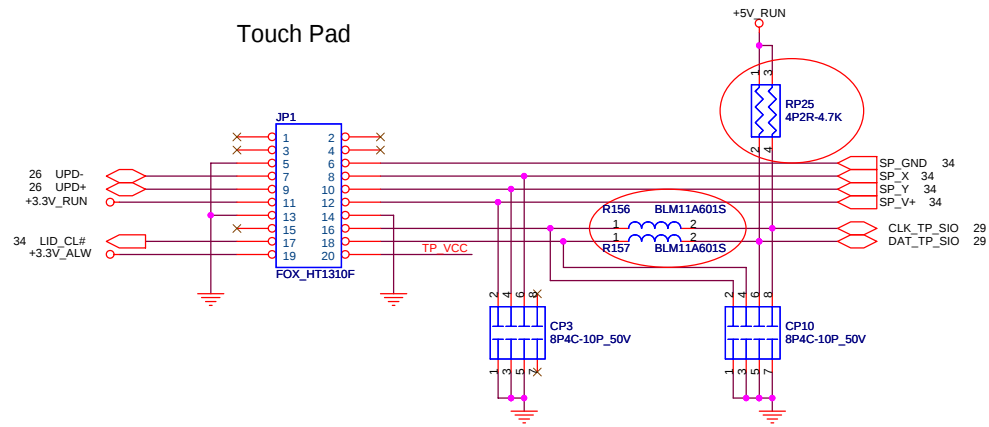


RTC BATTERY

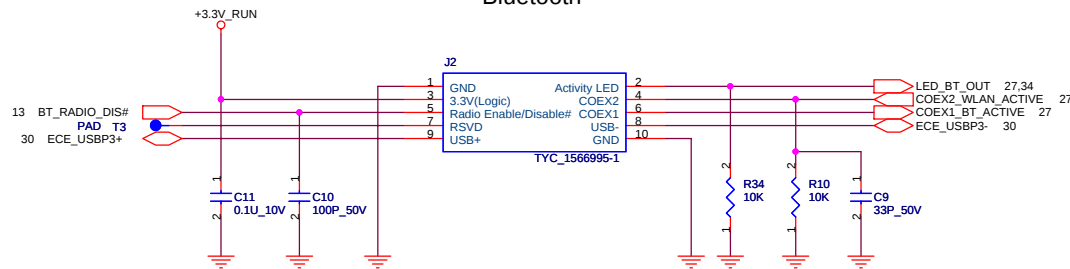




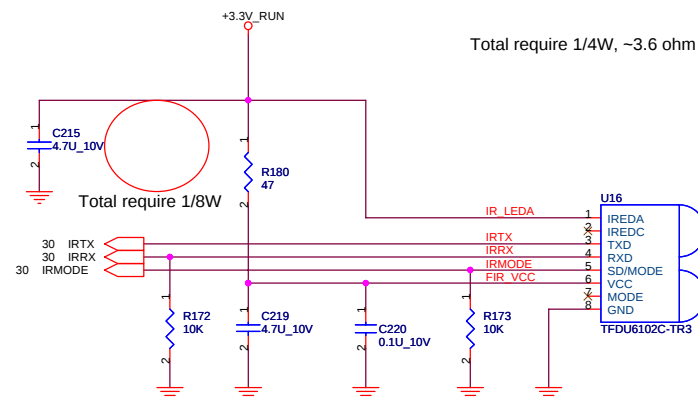
Touch Pad

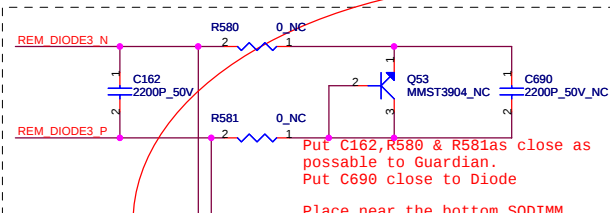
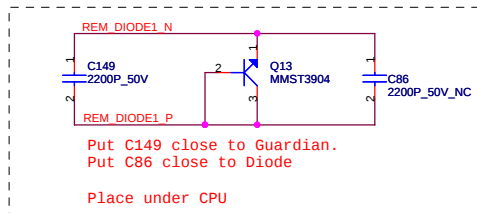
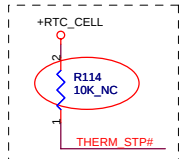
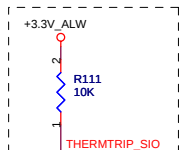
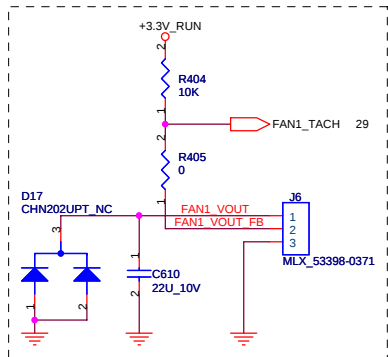


Bluetooth



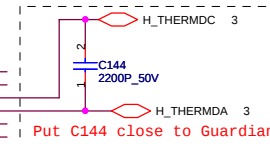
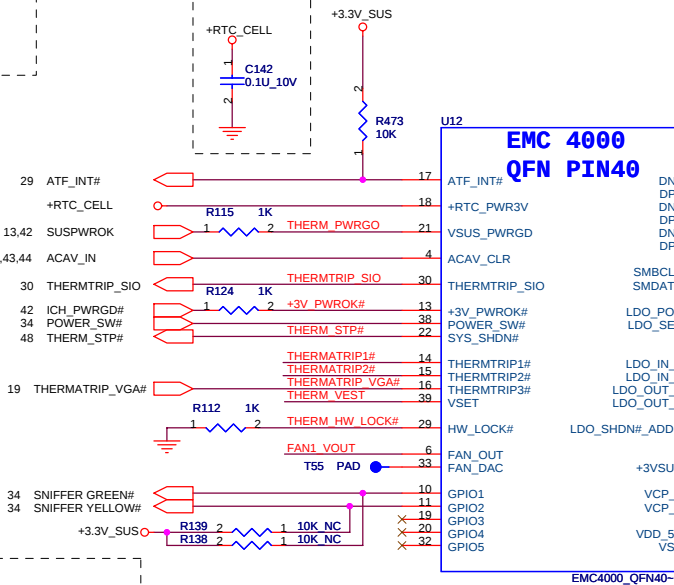
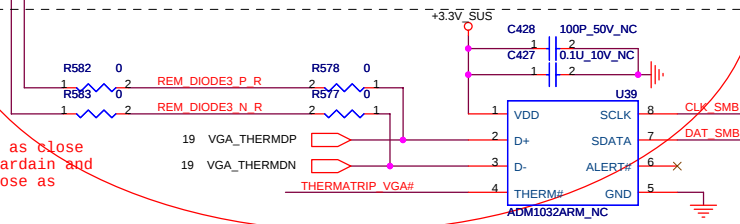
FIR





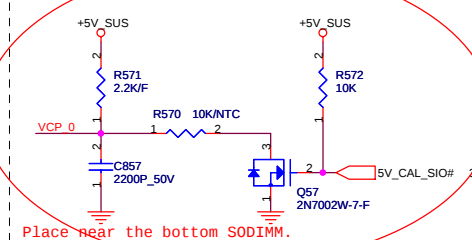
Discrete

Place R582 & R583 as close as possible to Guardian and R578 & R577 as close as possible to 1032.



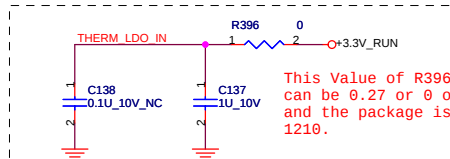
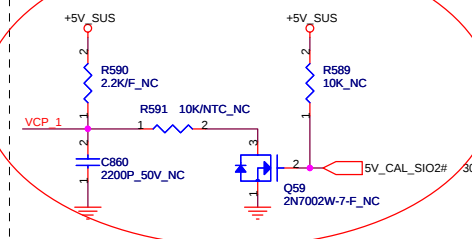
Put C144 close to Guardian.

Can place and stuff this thermistor circuit for additional sensor in Discrete Down Designs.



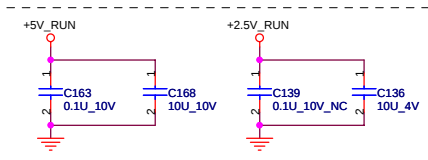
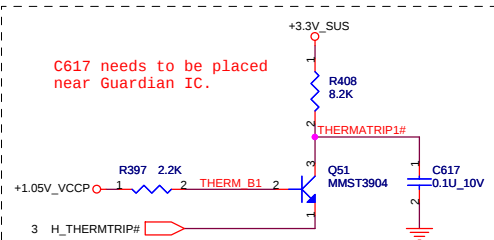
Place near the bottom SODIMM.

May need to place and stuff this thermistor circuit for additional sensor in Discrete Down Designs.

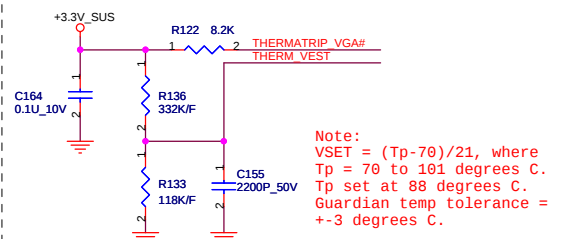
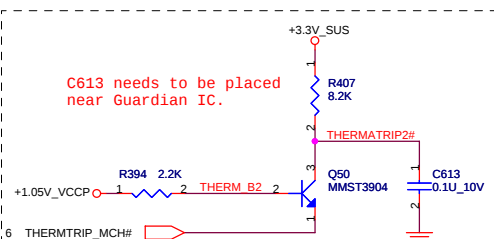


This Value of R396 can be 0.27 or 0 ohm and the package is 1210.

C617 needs to be placed near Guardian IC.



C613 needs to be placed near Guardian IC.



Note:
VSET = (Tp-70)/21, where
Tp = 70 to 101 degrees C.
Tp set at 88 degrees C.
Guardian temp tolerance =
+/- 3 degrees C.

0603 package.

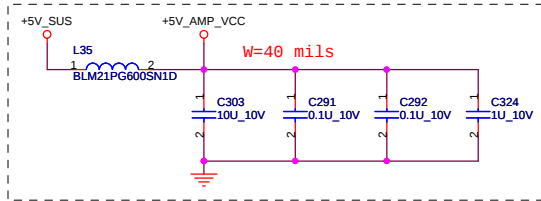
Voltage margining circuit for LDO output. For Vmargin stuff R31 and R27=30K. R27=1K for production.



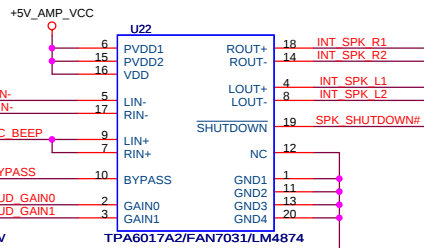
Title			FAN & THERMAL
Size	Document Number	Rev	
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INTERNAL SPEAKER AMP

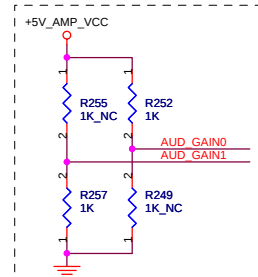
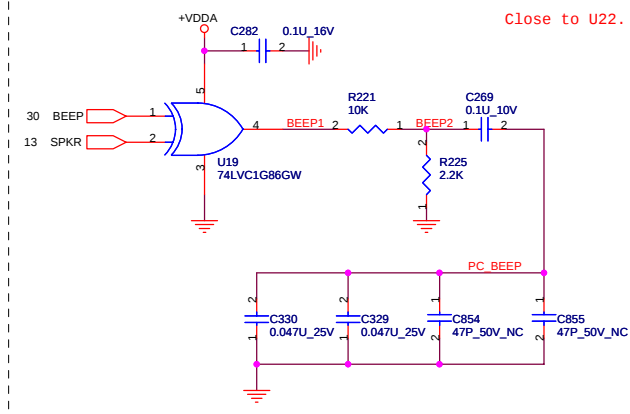
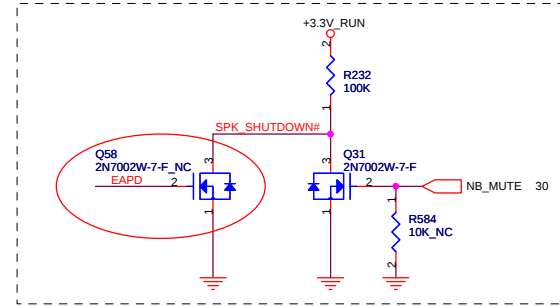
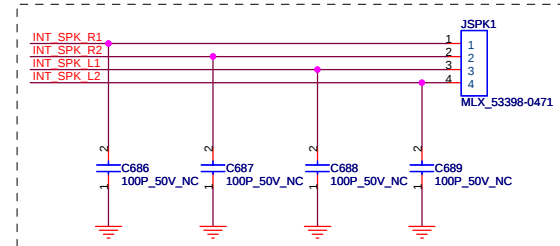
NOTE: Speaker trace width should be minimum 10 Mils.



AUD_LINE_OUT_L C326 1 2 0.047U 25V
AUD_LINE_OUT_R C290 1 2 0.047U 25V

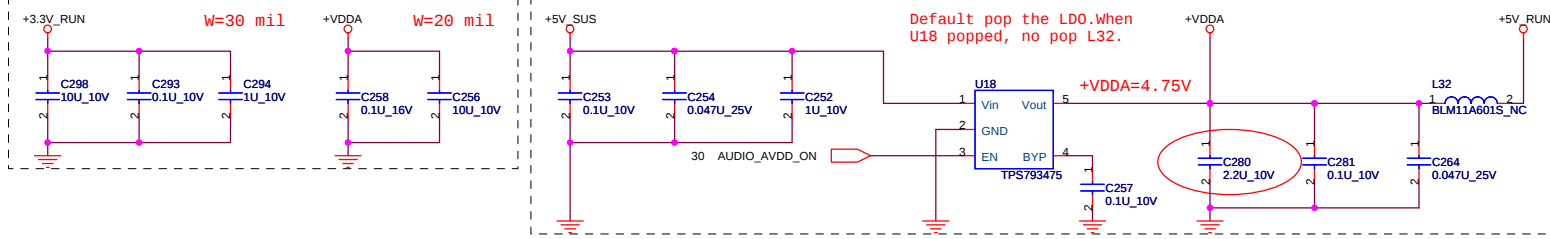
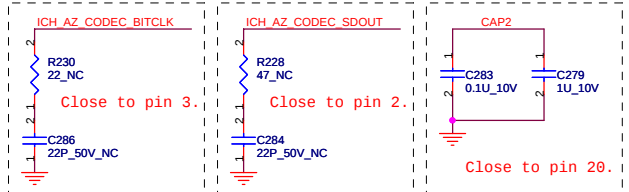
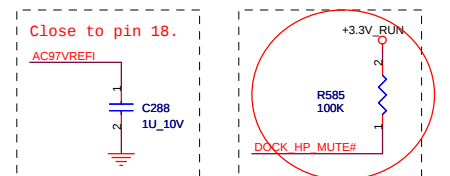
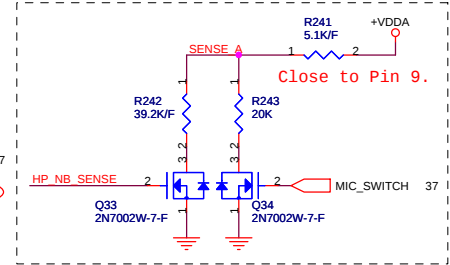
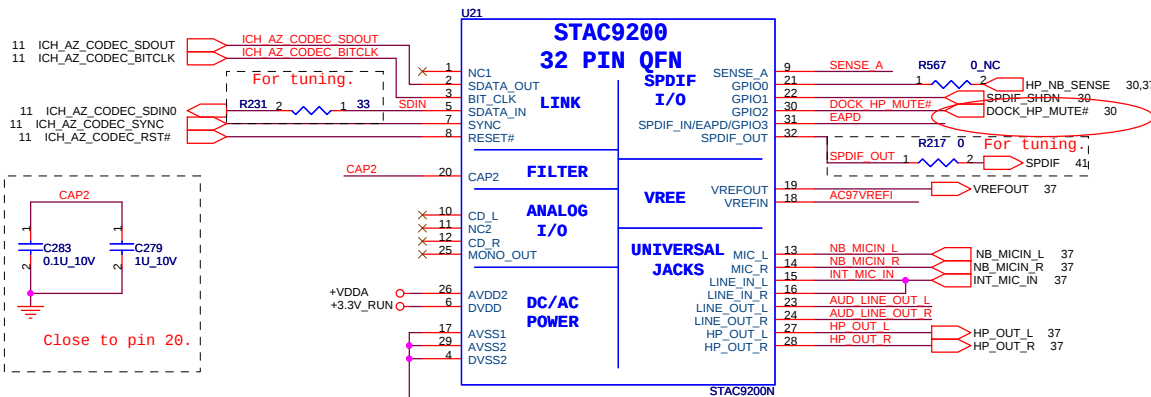


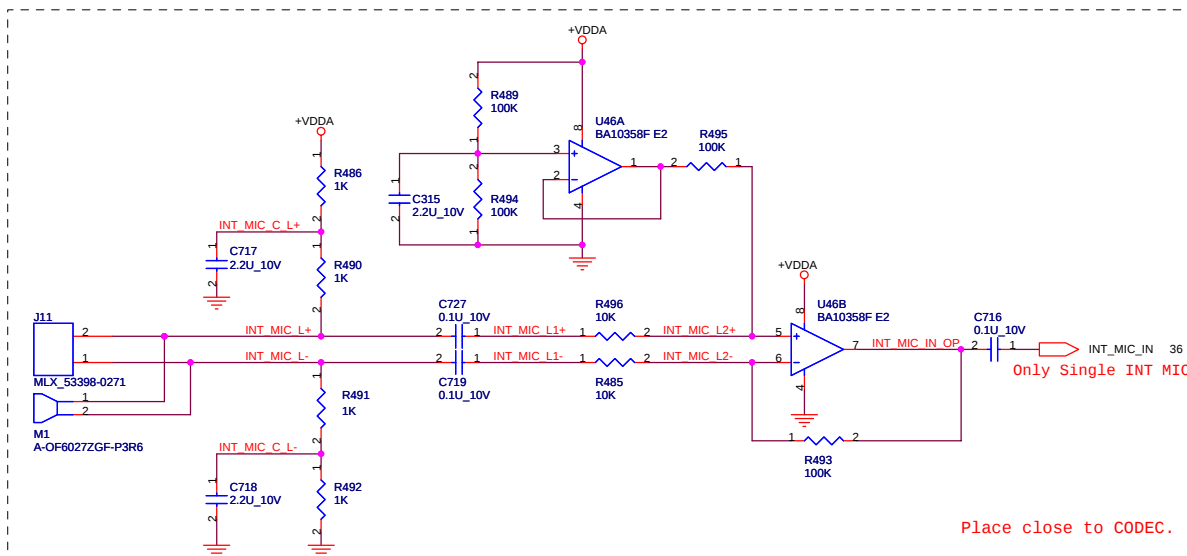
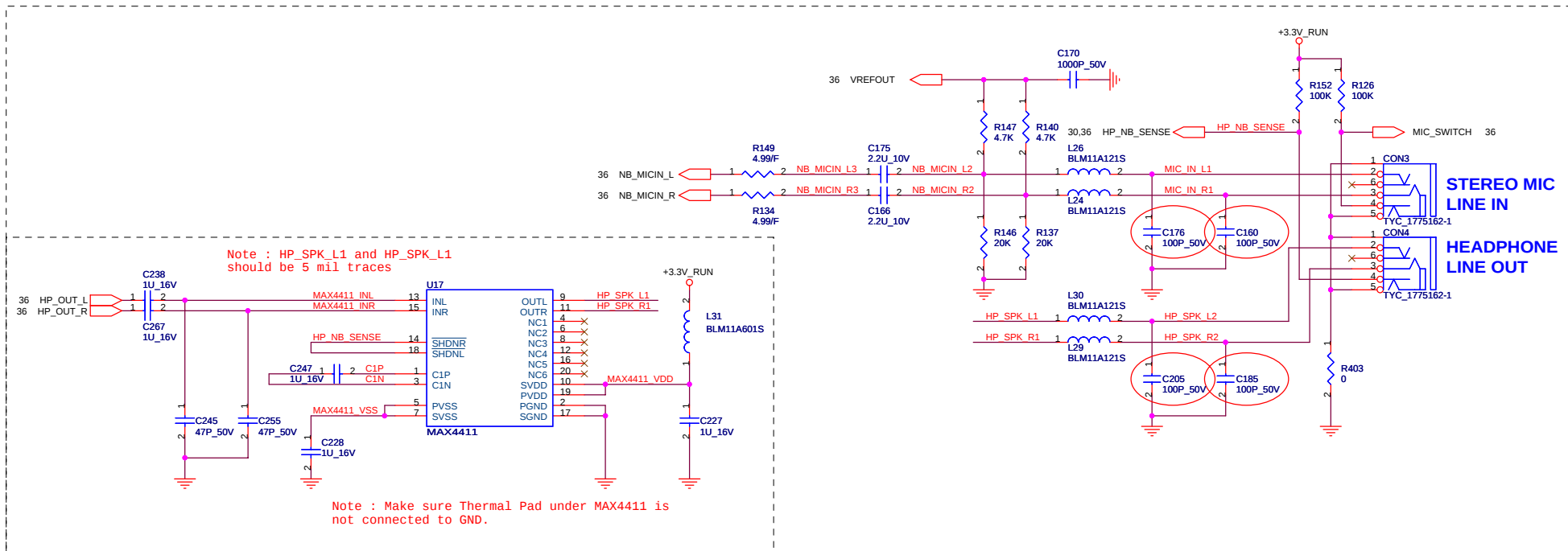
GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

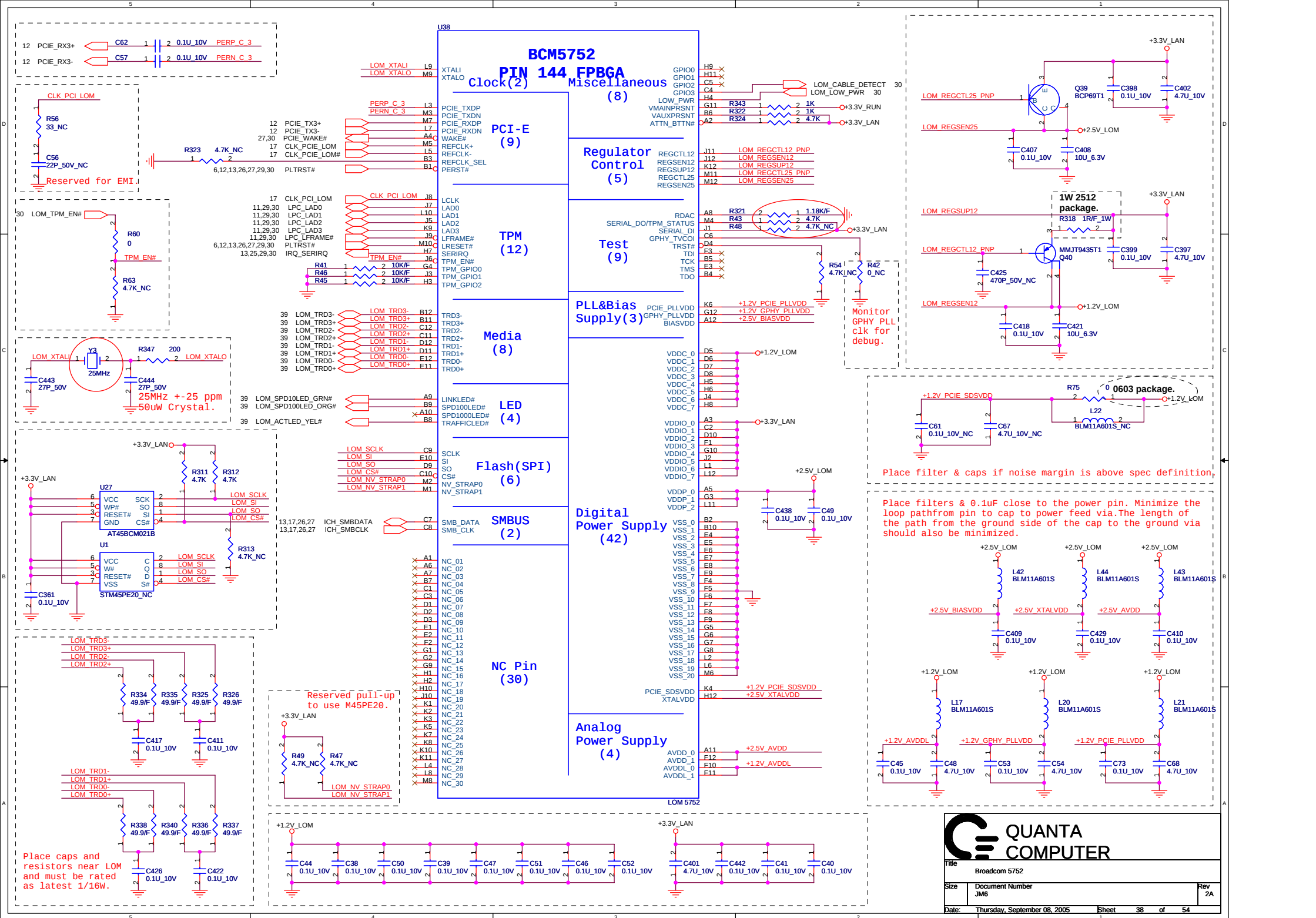


AZALIA (HD) CODEC

All CODEC analog audio inputs and outputs should be 5 Mil traces.

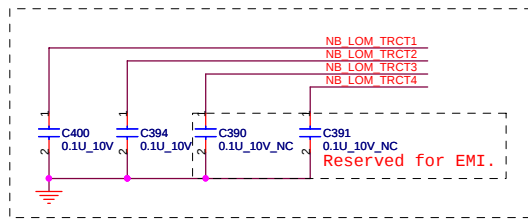
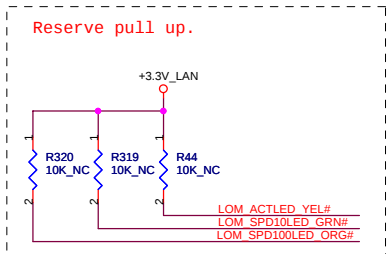
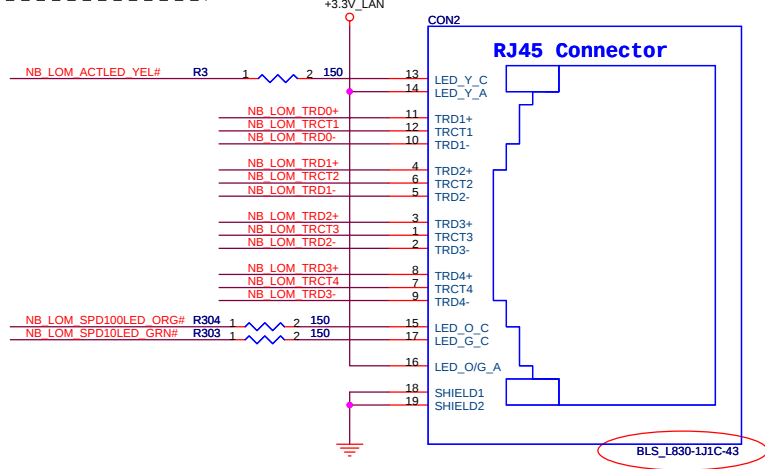
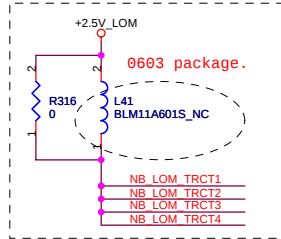
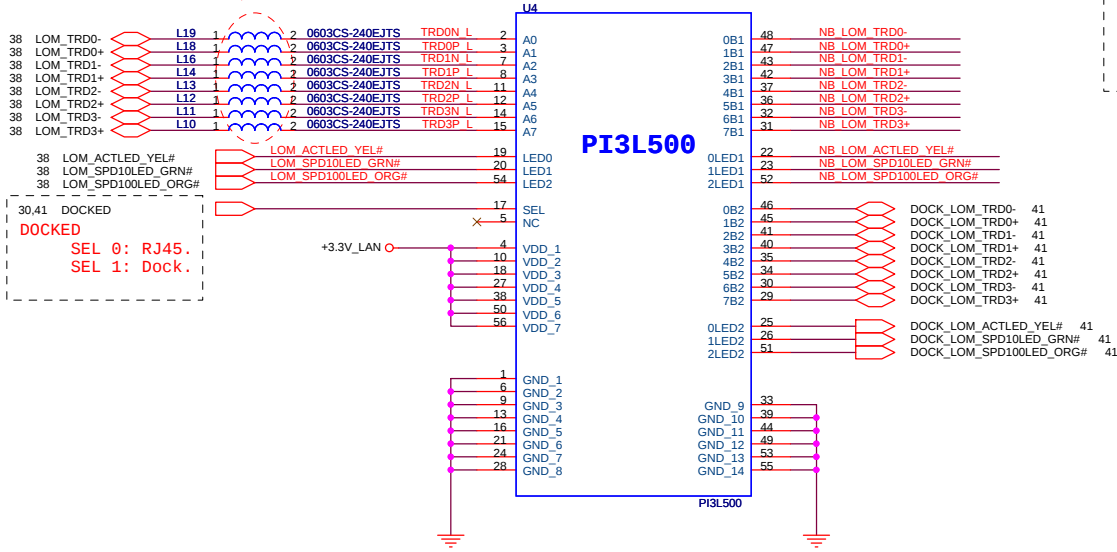


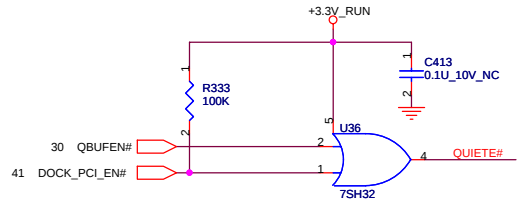
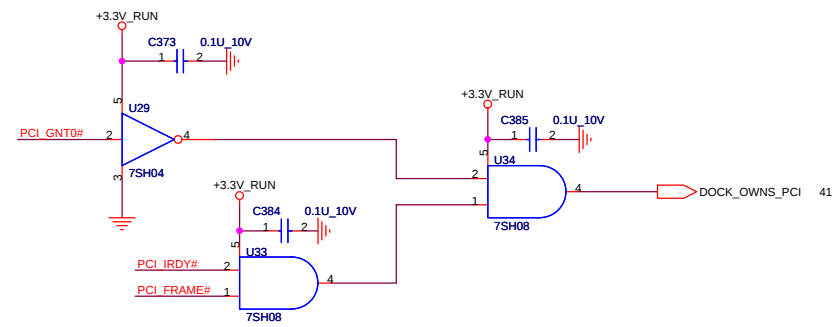
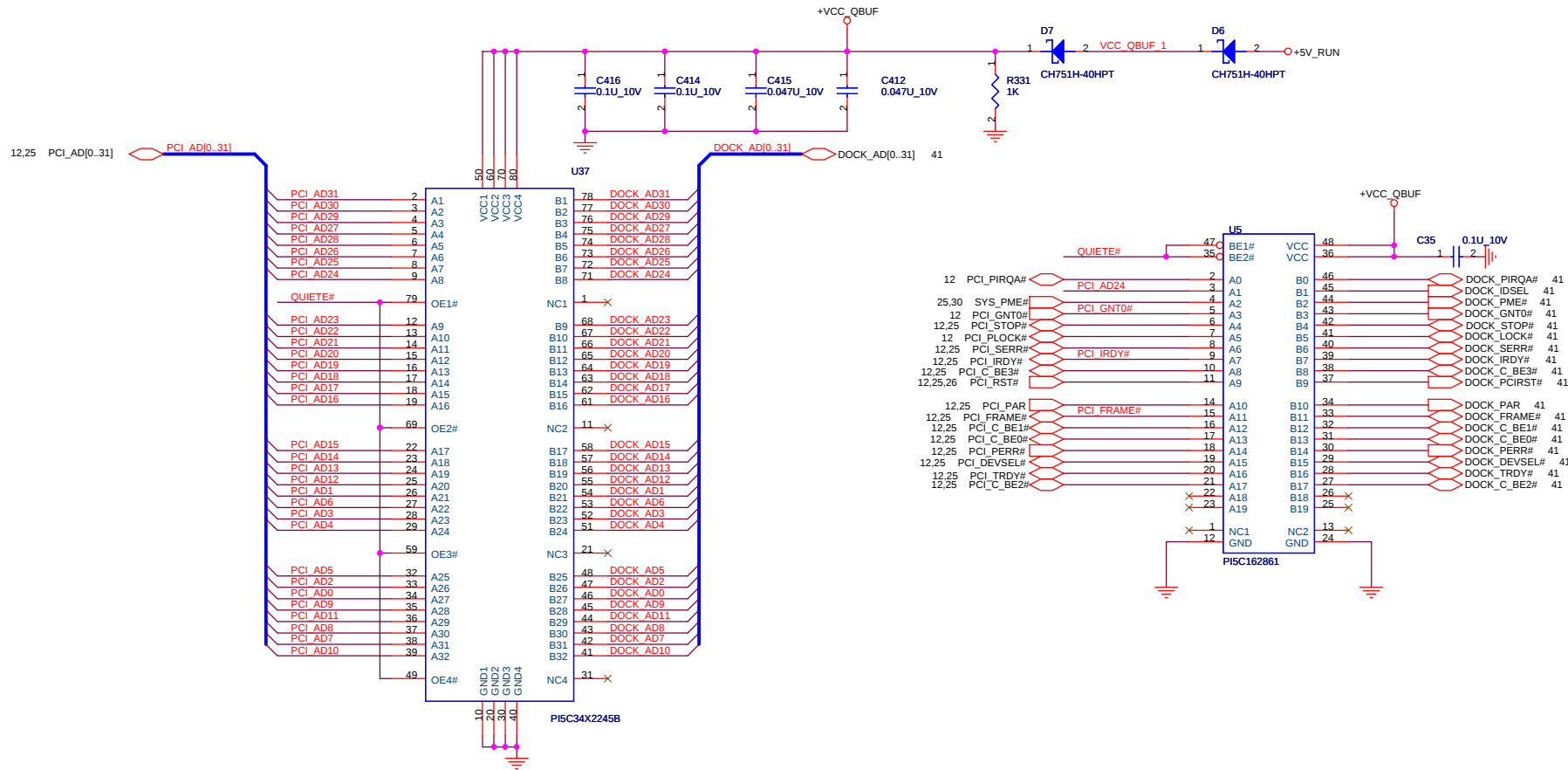


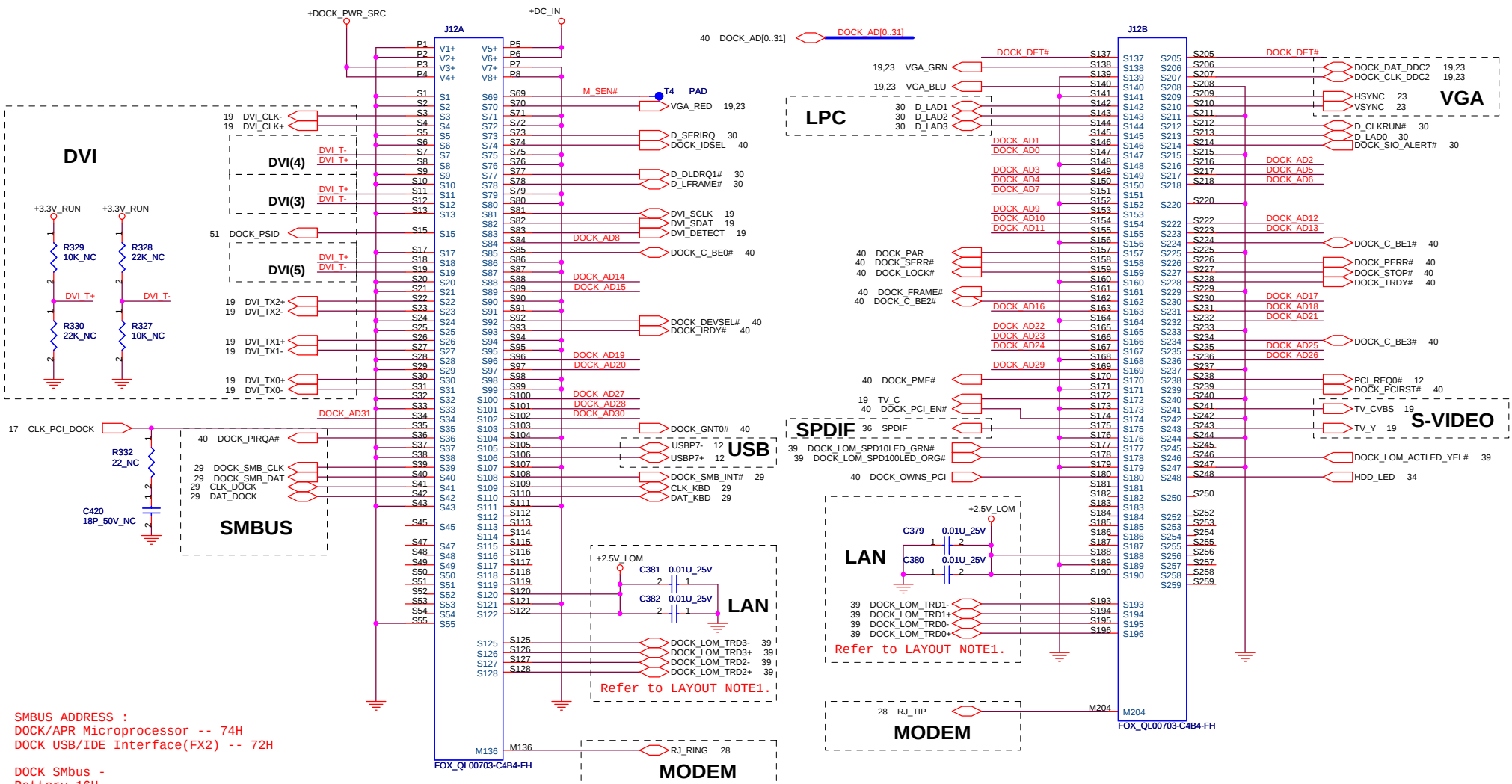


TRANSFORM+RJ45

24nH is a suggested value.
Actual value will be system dependent.
Must use 0603 package for lower DC resistance.







SMBUS ADDRESS :
DOCK/APR Microprocessor -- 74H
DOCK USB/IDE Interface(FX2) -- 72H

DOCK SMBus -
Battery 16H
Charger 12H
IDE I/F 70H
D-BAY 72H
SIO 48H

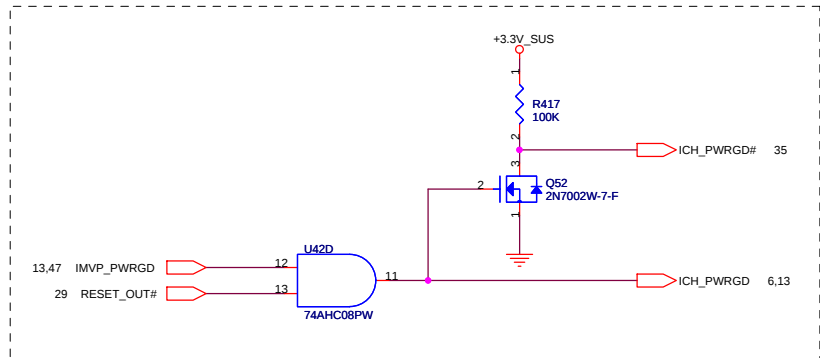
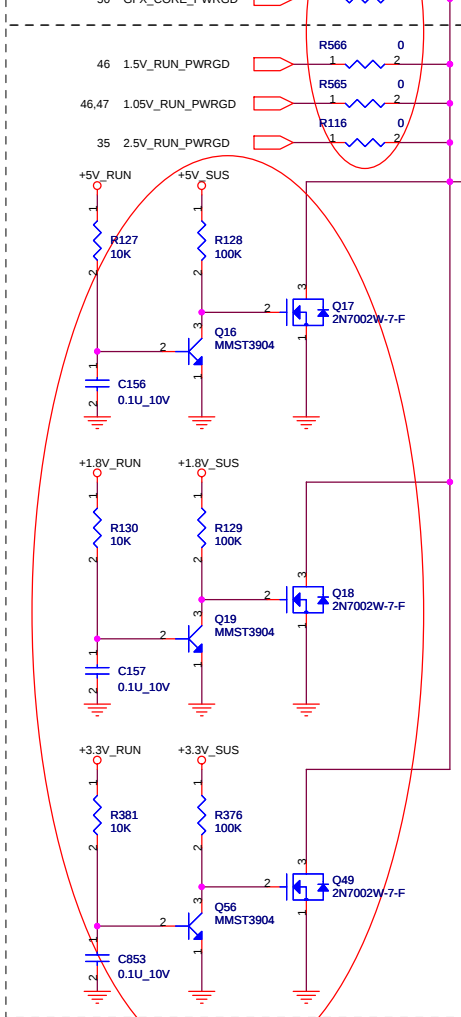
LAYOUT NOTES:
Follow the Intel Platform Design
Guideline routing recommendations
for the following buses: PCI, DVI,
LPC & USB.

LAYOUT NOTES1:
Terminators should be as close as
possible to dock connector pins.
Keep traces as short as possible.

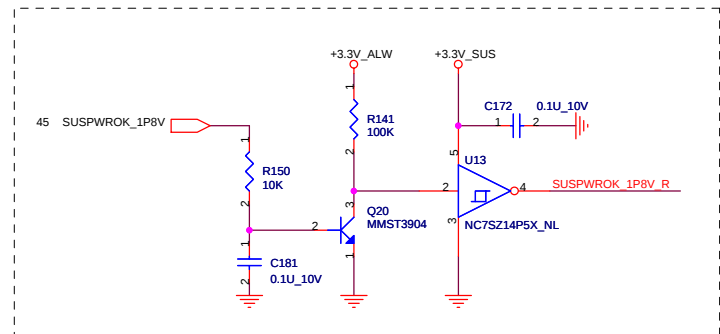
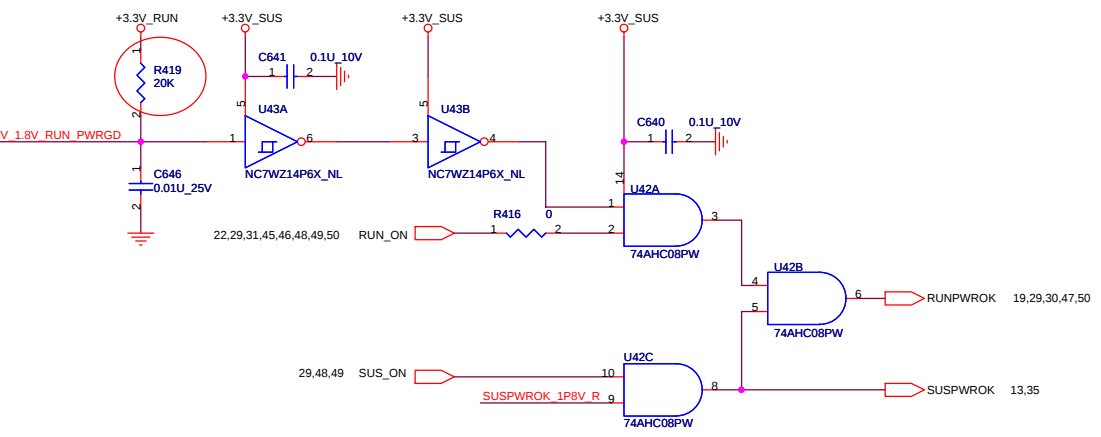


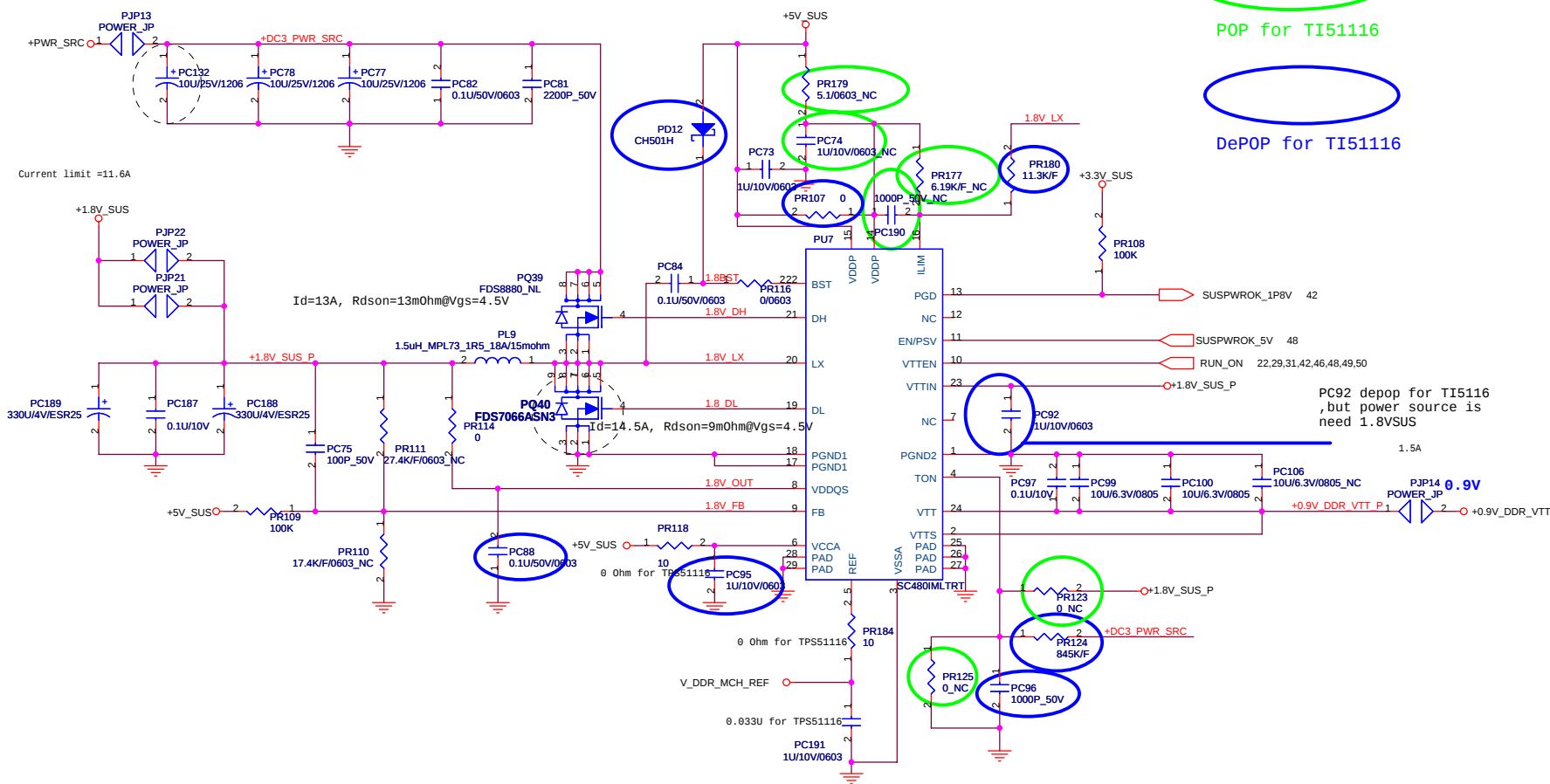
Title Docking Station Conn.		
Size	Document Number JM6	Rev 2A
Date:	Thursday, September 08, 2005	Sheet 41 of 54

Discrete



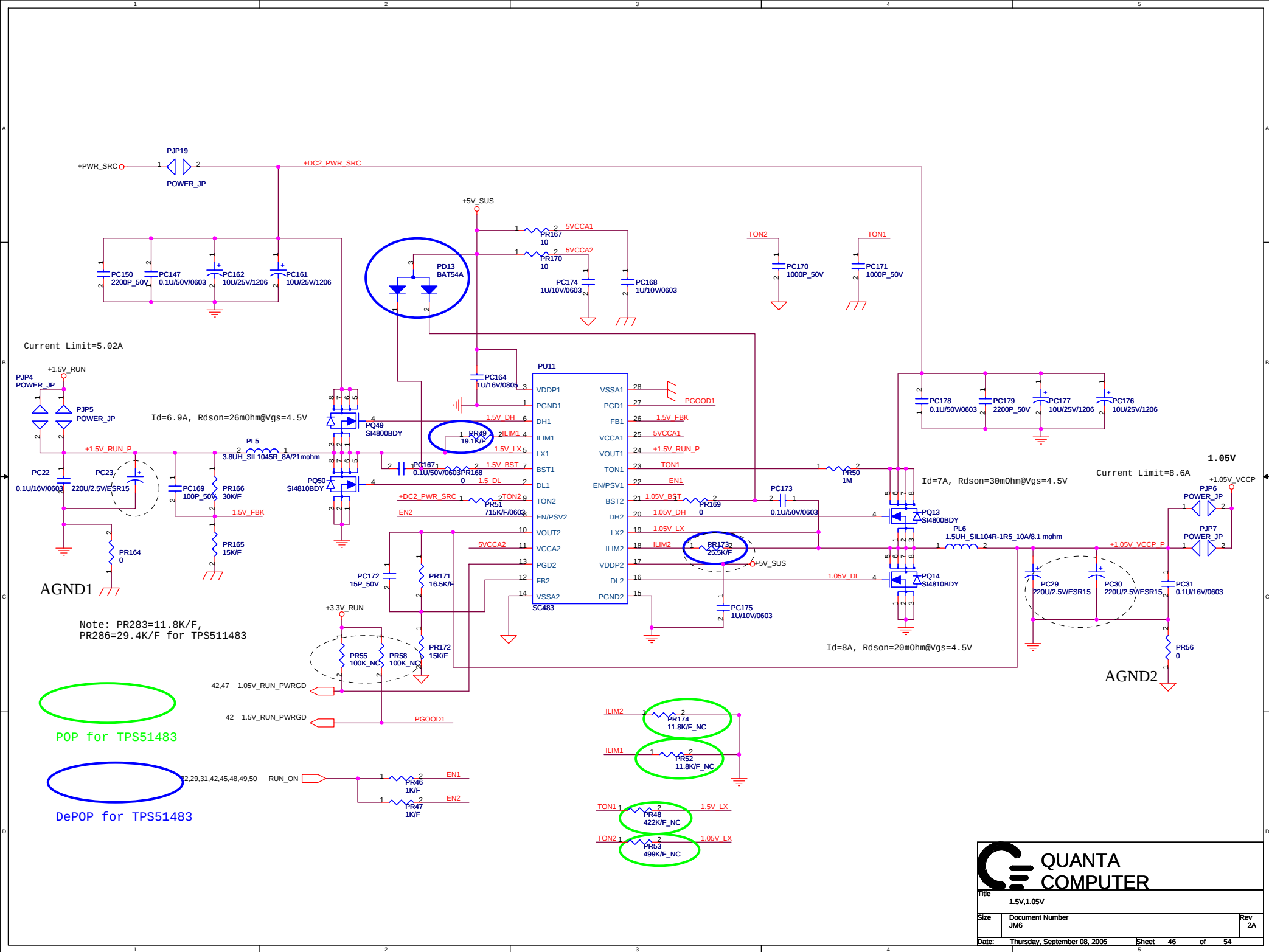
Keep Away from high speed buses

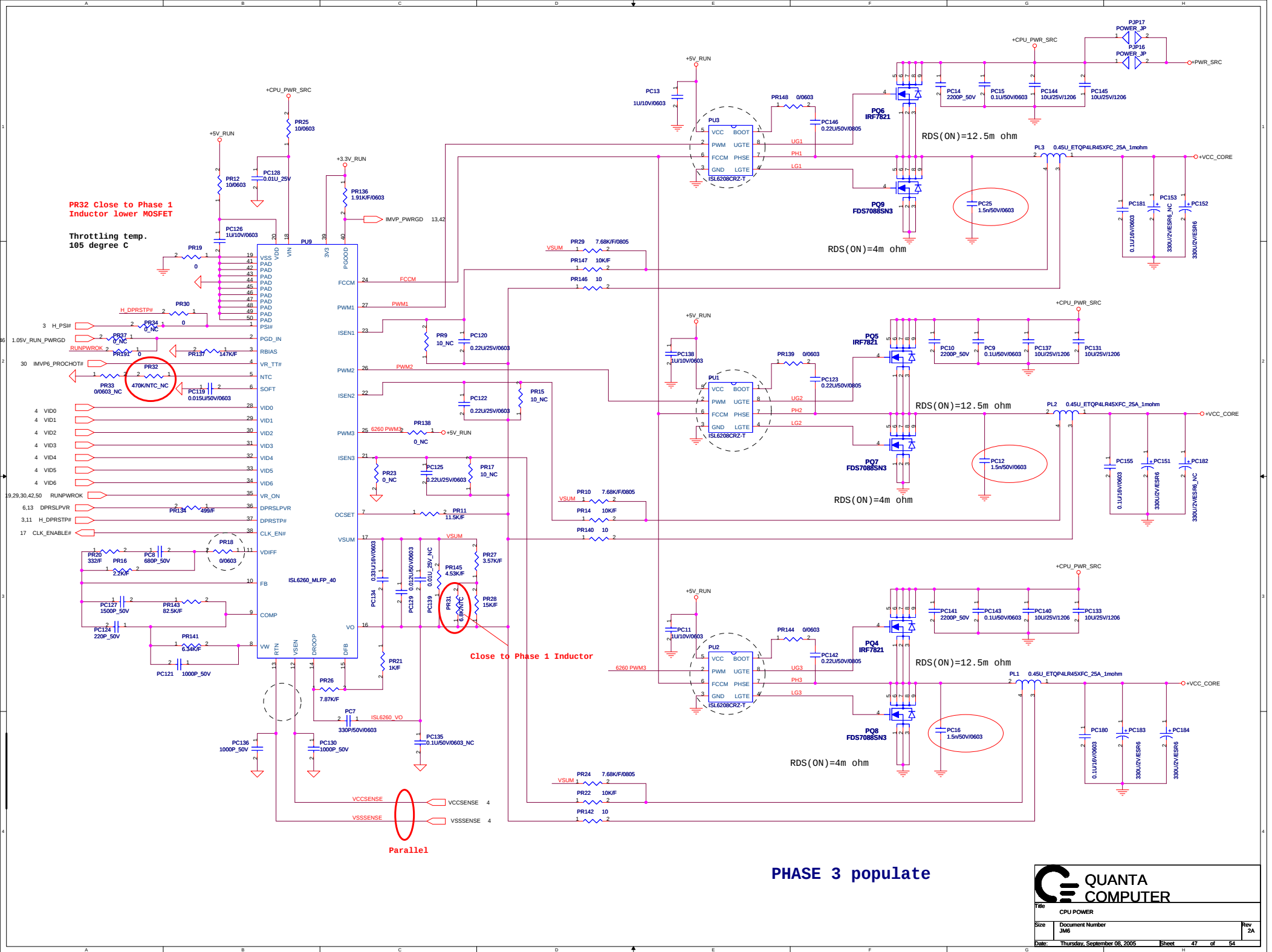




POP for TI51116

DePOP for TI51116





Design specc in default:
TDC: 4.67A
Peak: 6.67A
OCP: 7.2A-9.4A

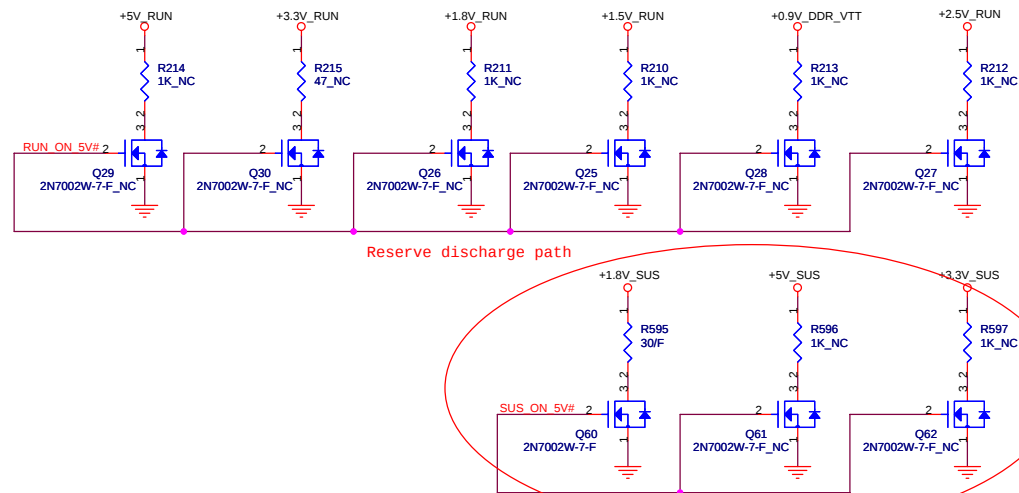
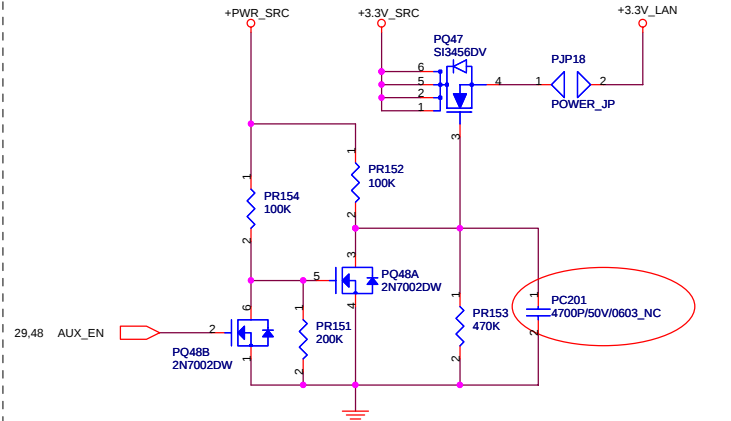
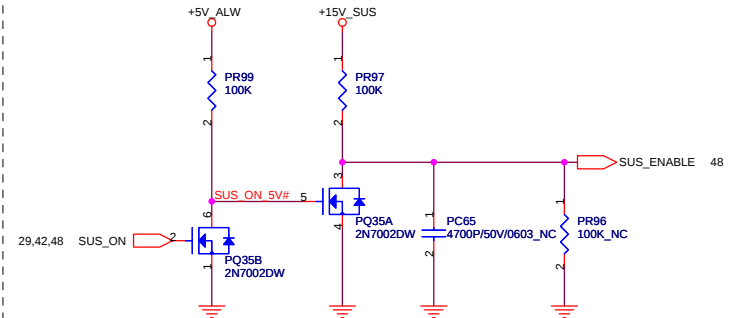
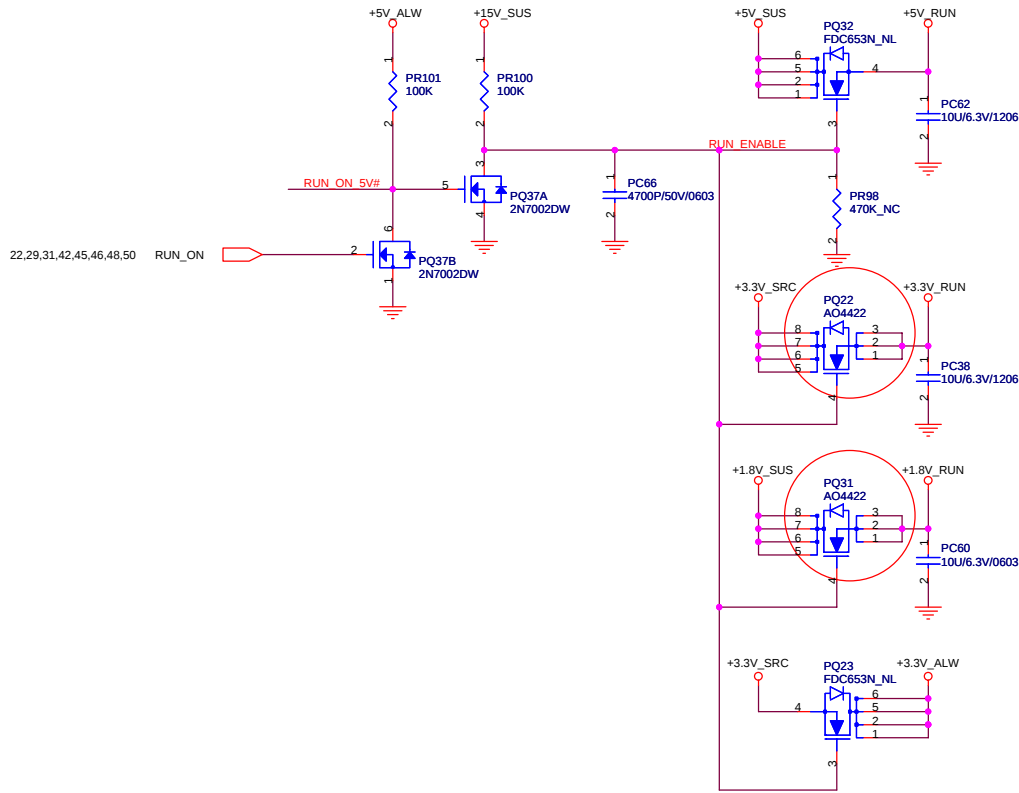
Place these CAPS
close to FETs

Place these CAPS
close to FETs

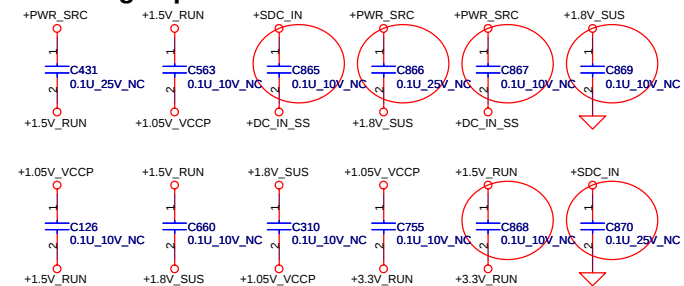
Design specc in default:
TDC: 3.93A
Peak: 5.61A
OCP: 6.2A-11.2A



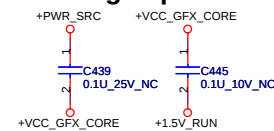
Title			3VALW.5V.3V, power on
Size	Document Number	Rev	
JM6		2A	
Date:	Thursday, September 08, 2005	Sheet	48 of 54



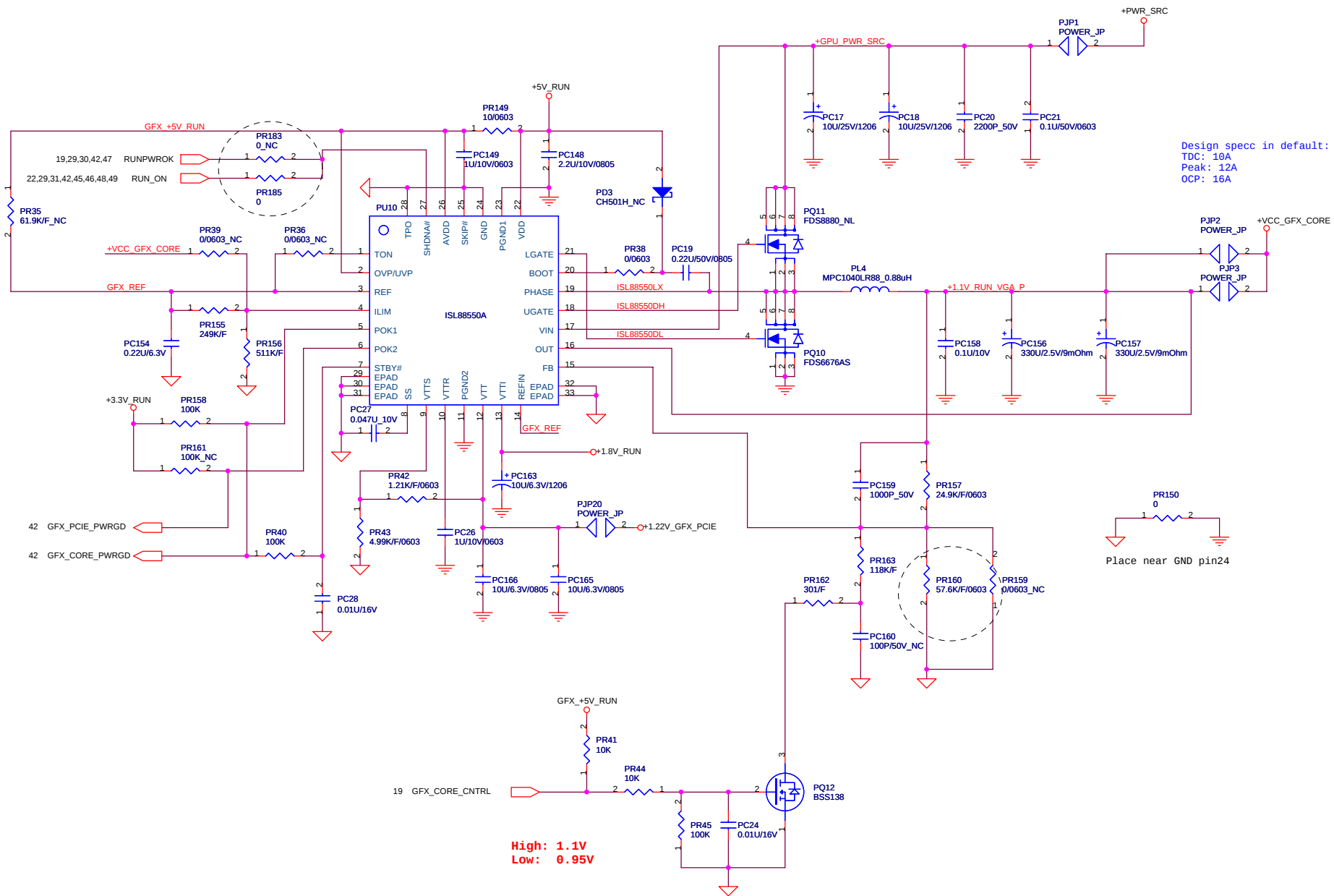
Stitching caps

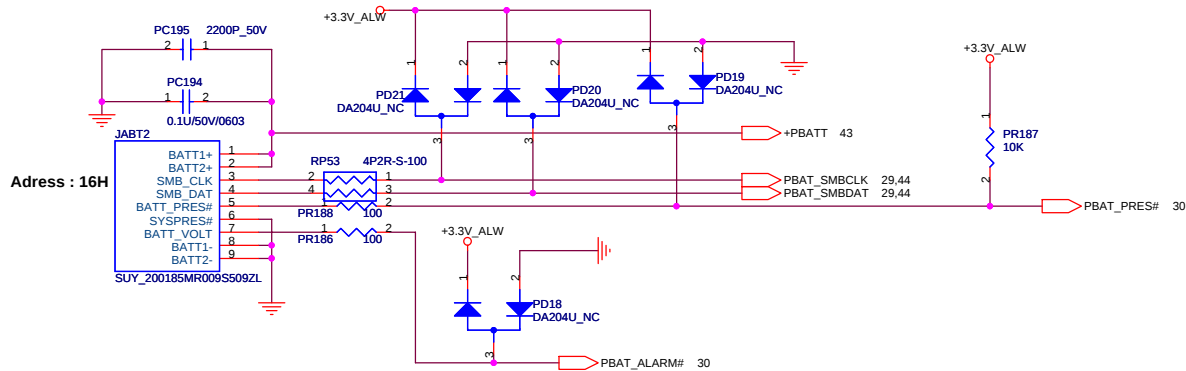
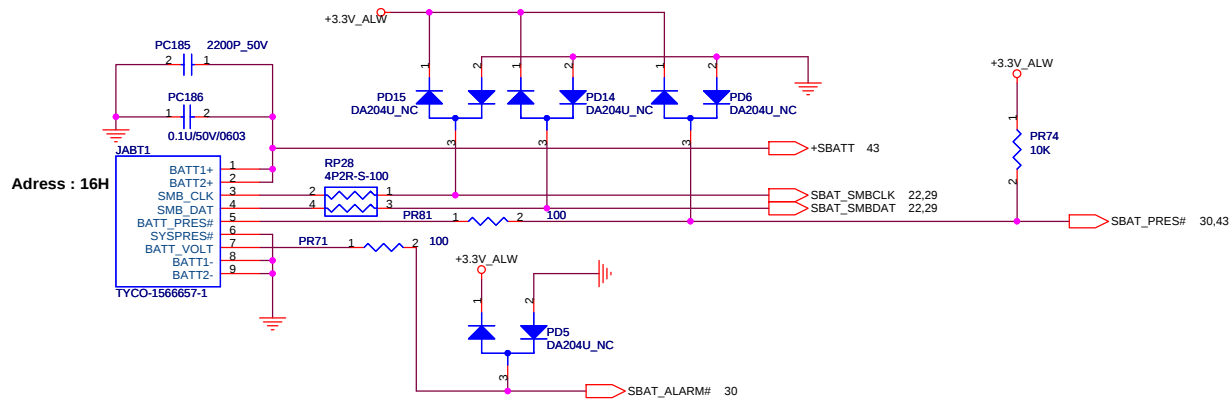


Stitching caps for Discrete



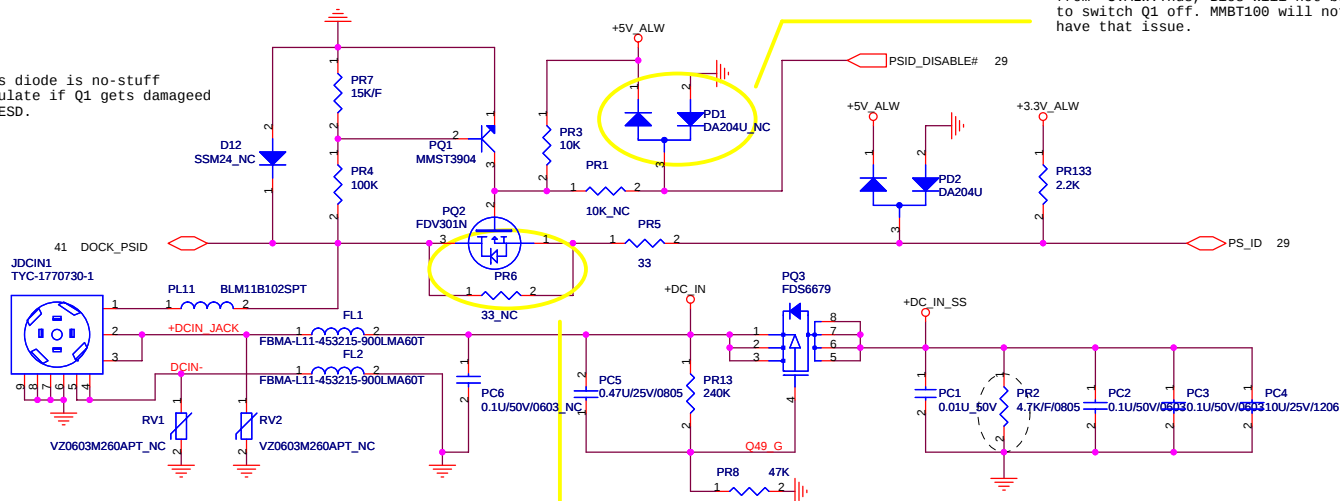
QUANTA COMPUTER	
Title: RUN POWER SW	
Size: JM6	Document Number: Rev 2A
Date: Thursday, September 08, 2005	Sheet 49 of 54





This resistor must be depopulated if FDV301N/FDV303 are used to avoid a 1.36mA constant current drain from +3VALW. Thus, Bios will not be to switch Q1 off. MMBT100 will not have that issue.

This diode is no-stuff populate if Q1 gets damaged by ESD.



Three transistor can be used for Q1 (pin compatible): FDV301N/FDV303N has low Vgs_on w/ built-in ESD protection. MMBT100 BJT works in reverse conduction mode.

QUANTA COMPUTER

Title DCIN, BATT CONNECTOR

Size Document Number JM6

Rev 2A

Date: Thursday, September 08, 2005

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